STUDY OF THRESHOLD VOLTAGE FOR DEEP-SUBMICRON MOSFETS

A Thesis submitted to the Electrical and Electronic
Engineering Department of BUET, Dhaka,
in partial fulfilment of the
requirements for the degree of

Master of Science in Enginnering

(Electrical and Electronic)

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DECLARATION

I hereby declare that this work has been done by me and it has not been submitted elsewhere for the award of any degree or diploma.

Countersigned

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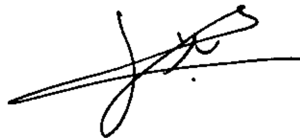
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ABSTRACT

MOSFETs are used extensively in very large scale integration (VLSI) Technology specially in various digital circuits such as microprocessor, semiconductor memories etc. Since the birth of Integrated Circuits (IC) fabrications the need for the reduction of device dimensions is driven by the requirement that IC of high complexity can be fabricated. The purpose of micro miniaturization of the MOSFET is not only to increase the packing density but also to improve the circuit performance at the same time. The fundamental issue of downsizing the MOS transistor is to preserve the long channel characteristics after miniaturization. But as the dimension of the MOSFET is reduced, departure from the long channel behavior occurs due to various undesirable short channel effects.

The threshold voltage V_{th}, for fully depleted MOSFETs with effective channel lengths down to submicrometer range has been investigated. In this thesis, a simple quasi-two-dimensional model is used, taking into account the effect of gate oxide thickness, source/drain junction depth and channel doping, to describe the accelerated V_{th} roll-off and drain voltage dependence. The proposed model retains accuracy because it does not assume *apriori* charge partitioning or constant surface potential. Also it is simple in functional form and hence computationally efficient.

List of Symbols

ϕ_s= Surface Potential.

ϕ_f= Fermi Level poptential of the substrate.

ϕ_{MS}= Alu min um and Silicon work function.

ε_{ox}= Permittivity of oxide thickness.

ε_s= Semicomductor dielectric cons tan t.

ε_0= Permittivity of free space.

L= The effective channel length of MOSFET.

V_T= Threshold voltage of MOSFET.

V_G Gate voltage.

V_{ox} Voltage across the gate oxide.

E_{ox} Electric field across oxide thickness.

t_{ox} Oxide thickness.

Q_s = Charge density in Silicon.

Q_{SS} = Surface charge density.

C_0 = Gate capacity per unit area.

Q_B Depletion layer charge.

q = Electric charge.

N_A= Effetive doping concentration.

X_d =Depletion layer width.

V_{th} Threshold voltage for a long n-channel device.

V_{FB} The flat-band voltage of a MOSFET.

V_{DS} =The drain voltage with respect to source.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Threshold voltage is a significant parameter for technology development and MOS device modelling. An accurate prediction of the threshold voltage is needed to determine circuit noise margins, speed, and required node voltages. In this chapter, surface properties of silicon for MOSFETS, review of recent works on MOSFET threshold voltage, objectives of this work and summery of this thesis are presented.

1.2 Energy-Band Diagram For the Ideal Case

The concept of the energy-band diagram is drawn along a single vertical axis only. In the case of pn junction, it was drawn as a function of distance x. In the case of a MOS structure, the energy band also changes as a function of distance, but the direction x is now defined to be from the gate into the silicon, therefore, in order to

maintain the similarity with the way band diagrams were drawn before, the MOS transistor should be turned on its side, as in Fig. 1-1.

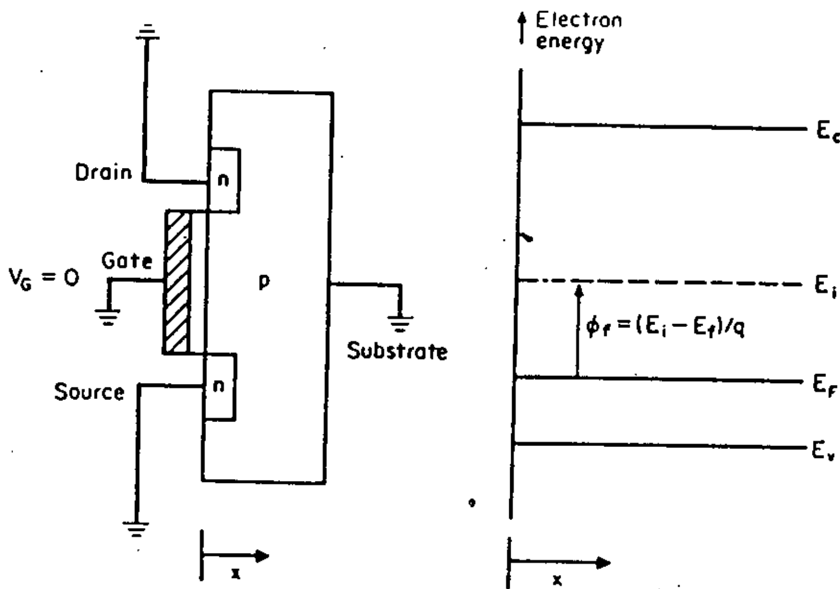

Fig. 1.1 Energy-band diagrams for gate region of a MOS transistor (ideal case).

In ideal case, and with no voltage applied, the energy bands would be perfectly flat. Hence this condition is called flatland. In the case of p-type bulk, a negative bias will attract mobile holes to the surface, making the material effectively more heavily doped p type. This is the accumulation condition as shown in Fig. 1.2a. When bias is changed to positive, the mobile holes are repelled from the surface, forming a depletion layer near the surface as in Fig. 1.2b. As the positive bias is increased, a point is reached when the oxide-semiconductor interface becomes intrinsic (E_F=E_i). Beyond that point, a special condition is reached when the surface potential, the amount of bending, reaches:

$$\phi_S = \frac{-(E_i \text{ at surface} - E_i \text{ at bulk})}{q} = 2\phi_f \qquad (1.1)$$

where ϕ_f is the Fermi potential. In the inversion condition Fig. 1.2c, is of particular interest because a layer of charge is now formed that can be used for conduction in a MOS transistor. The gate voltage that brings about this condition is called the threshold voltage.

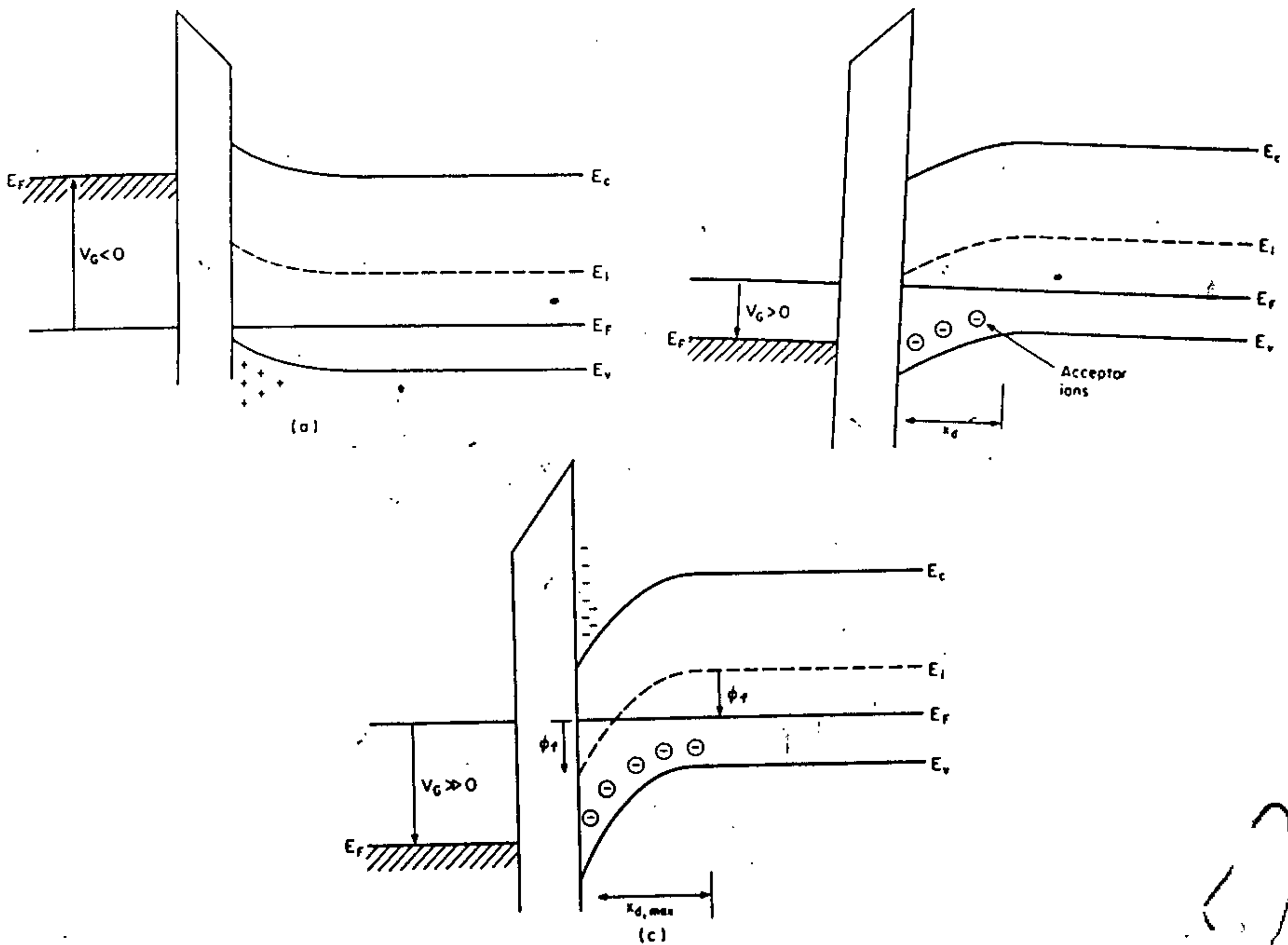

Fig. 1.2 Band bending in p-bulk silicon: (a) accumulation (b) depletion (c) inversion

In the case of an n-type bulk, the same sequence of events take place, but with the polarity of voltages reversed. With positive gate voltage, majority carriers accumulate at the surface making the silicon more n type. With negative gate voltage, a depletion layer is exposed as electrons are pushed back from the surface. Then at inversion, the depletion reaches a maximum width and any further increase in gate bias are balanced by the inversion -layer charge comprised of mobile holes.

1.3 Calculation of Threshold Voltage V_T

Inversion is achieved when the surface potential, i.e., surface and band bending, reaches

$$\phi_s = 2\phi_f \qquad (1.2)$$

However, it is more practical to work with the threshold voltage V_T, the gate voltage that is necessary to bring about this condition. An expression for V_T will now be derived. An applied gate voltage V_G becomes the sum of voltage drops across the oxide and across the silicon:

$$V_G = V_{OX} + \phi_s \qquad (1.3)$$

where V_{OX} is the voltage across the gate oxide, and ϕ_s is the surface potential, equivalents to the voltage drop across the depletion layer. The goal is to express V_{OX} in terms of ϕ_s, which can then be simply set to $2\phi_f$. By definition

$$V_{ox} = E_{ox}\, t_{ox} \qquad (1.4)$$

where E_{ox} is the electric field across the oxide thickness t_{ox}. However, the continuity of the displacement vector across the oxide-semiconductor interface requires that

$$E_{ox}\varepsilon_{ox} = E_{si}\,\varepsilon_{s} \tag{1.5}$$

Furthermore, Gauss's theorem states that the field into silicon surface is related to the amount of charge in the silicon by

$$E_{si} = \frac{-Q_s}{\varepsilon_s \varepsilon_o} \tag{1.6}$$

where Q_s is the charge density in the silicon. In depletion Q_s is simply the depletion-layer charge. But in inversion it also includes the inversion-layer charge. From Eqns. (1.4), (1.5), and (1.6) we obtain

$$V_{ox} = \frac{-Q_s t_{ox}}{\varepsilon_{ox}\varepsilon_o} = -\frac{Q_s}{C_o} \tag{1-7}$$

where the gate capacitor per unit area is defined as

$$C_o = \frac{\varepsilon_{ox}\varepsilon_o}{t_{ox}} \tag{1-8}$$

Therefore Eqn. (1.3) can be written as follows:

$$V_G = \frac{-Q_s}{C_o} + \phi_s \tag{1.9}$$

In depletion Q_s equals the depletion-layer charge Q_B

$$Q_s = Q_B = -q\,N_A\,X_d = -\sqrt{2\varepsilon_s\varepsilon_o q N_A \phi_s} \tag{1.10}$$

The last equality in Eqn. (1.10) comes from the fact that the depletion - layer width which is given by:

$$X_d = \sqrt{\frac{2\varepsilon_s \varepsilon_o \phi_s}{qN_A}} \tag{1.11}$$

Eqn. (1.9) now reduces to

$$V_G = \frac{-Q_B}{C_o} + \phi_s = \frac{\sqrt{2\varepsilon_s \varepsilon_o q N_A \phi_s}}{C_o} + \phi_s \tag{1.12}$$

At inversion condition, $\phi_s = 2\phi_f$, thus the threshold voltage for a long n-channel device is

$$V_{Tn} = \frac{\sqrt{2\varepsilon_s \varepsilon_o q N_A (2\phi_f)}}{C_o} + 2\phi_f \tag{1.13}$$

1.4 Nonideal Effects

There are several nonideal effects that perturb the ideal case .The effects on V_T of the nonzero ϕ_{MS} and nonzero Q_f will be presented here, and an expression for effects on V_T will be presented. In a MOS structure, work function is equivalent to the energy required to reach the oxide conduction band. The aluminum (metal) work function ϕ_M and silicon work function ϕ_S are not equal; thus when aluminum- oxide and an oxide-semiconductor system are brought together as in Fig.1.3 the work function difference will not be zero.

$$\phi_{MS} = \phi_M - \phi_S \neq 0 \tag{1.14}$$

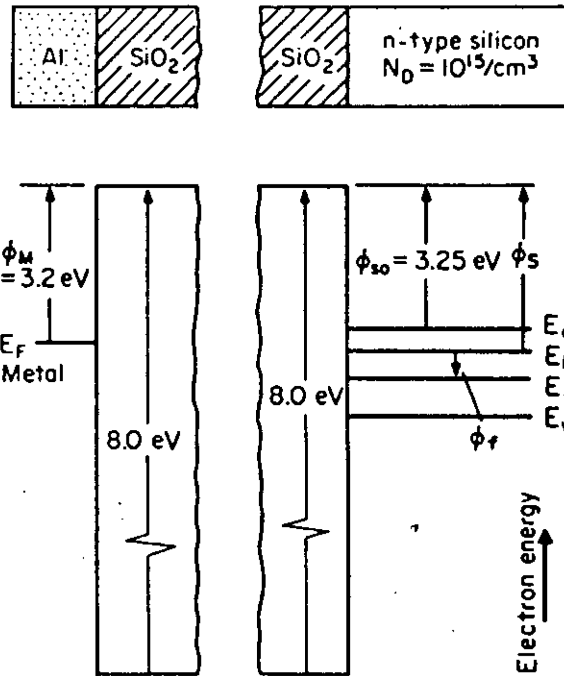

Fig. 1.3 The aluminum-SiO_2 and SiO_2 -silicon system.

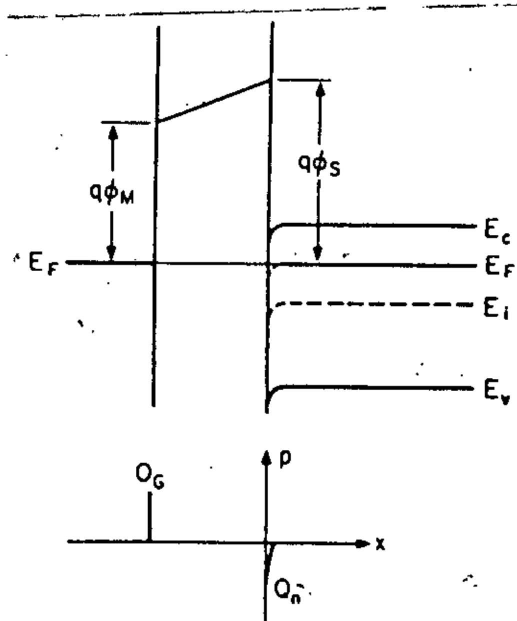

Fig. 1.4 Built-in charge due to nonzero ϕ_{MS}.

This results in a built-in charge as the Fermi levels on both sides of the oxide attempt to line up in Fig. 1.4, as they should in an equilibrium system.

Fig 1.5 shows that an external voltage of an amount V_{FB} would need to be applied to bring the MOS system to the flatband condition. V_{FB} is called the flatband voltage. Once V_{FB} is determined, by principle of superposition, all the previously developed expressions can still be utilized.

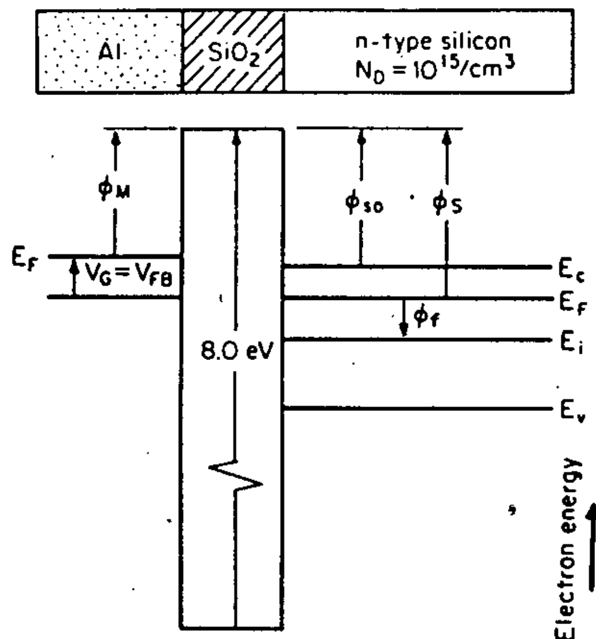

Fig. 1.5 Application of V_{FB} to bring about flatband condition for n-type-silicon.

The next most important nonideal perturbation of the MOS system is the presence of ionizes positive charge at the oxide-semiconductor interface. This is brought about by the oxidation process itself and is the result of dangling silicon bonds remaining after oxidation. It resides just slightly into the oxide side of the oxide-silicon

interface and is relatively independent of oxide thickness, doping type, or doping concentration. An external voltage needs to be applied in addition to nonzero ϕ_{ms} to restore flatband condition. An expression for V_{FB} that includes the effect of the different work functions in the gate and in the silicon as well as the influence of oxide charge can be written as follows:

$$ {}_{FB} = \phi_{MS} - \frac{Q_{SS}}{C_o} \tag{1.15} $$

where Q_{SS} is the surface charge density.

1.3 Review of recent works on MOSFET threshold voltage

The Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) has been the major device for integrated circuits over the past two decades. With technology advancement and the high scalability of the device structure. Silicon MOSFET based on very large scale integration (VLSI) circuits has resulted in miniaturization of MOSFET device. Recent works on threshold voltage have thus concentrated on short-channel devices.

The threshold voltage of MOSFETs, which has always been the major concern of device scaling is closely related to device structure parameters (e.g., oxide thickness, junction depth, gate length, etc.) and terminal voltages. The increasing complexity of modern MOS device structure requires clear understanding on the behavior of

threshold voltage, and many efforts have been devoted to the investigation of this electrical parameter.

Conventional long-channel theories were first challenged by the introduction of channel implantation in modern MOS devices [1]. Another challenge comes from the existence of source/drain diffusion islands. To physically interpret the short-channel effect, the roles of source/drain islands were first emphasized in the simplified Yau's charge-sharing scheme [2] for the threshold-voltage model with uniform substrate doping profile. The charge-sharing scheme had been improved by many authors (e.g., [3] and [4]), and the channel-length dependence of threshold voltage can be simulated with acceptable deviation. This scheme helps us to understand the behavior of short-channel MOSFET devices, however it's mathematical treatment with addition of artificial charge partition is too approximate to reveal any further physical insight of devices. As device dimensions fall into submicrometer range, the charge-sharing scheme fails to overcome these drawbacks.

Besides the charge-sharing scheme, another strategy to attack the above problem is to directly solve the two-dimensional Poisson's equation analytically [5]-[13]. Recently, a simplified threshold-voltage model for surface-channel MOSFETs with nonuiform substrate doping profile has been proposed by Lin and Wu [13], which is based on solving the depletion-approximate two-dimensional Poisson's equation using the Green function technique. The effects due to short channel, depletion-width broadening (increase of substrate depletion width with two-dimensional effects), and

charge screening (insensitivity of threshold voltage to substrate bias for short-channel devices) can be described by this model.

In the last few years, two-dimensional Poisson's equation in the depletion region reveal an expression for the threshold voltage that is exponentially dependent on effective channel length & agrees better with experimental results than do the charge-sharing models.

In the range of submicrometer channel length, the charge-sharing model assumptions of constant surface potential and no divergence of electric field lines in the gate oxide are invalid for high drain and substrate biases. Therefore, the charge-sharing model is unable to model the drain induced barrier lowering (DILB) or the body effects [14]. On the other hand when deriving the analytical solutions for the two-dimensional Poisson's equation in the depletion region, various approximations have been made for boundary conditions. Consequently, model parameters lack physical meanings.

1.4 Objective of this work

In a long-channel MOSFET, the drain, source and substrate voltages produce negligible influence on the potential distribution in the channel region. The threshold voltage is independent of the device parameters and the operating conditions in this case. However, the depletion region formed by the source and drain is comparable to

the channel length for short - channel devices. Influence of the drain, source and substrate voltages become significant in comparison to the gate voltage and as a result, the mathematical expressions developed for long-channel devices become invalid for such devices. Different 'Charge-sharing' models developed in recent years for short-channel devices are based on certain assumptions. These assumptions result in considerable error for devices with very small channel lengths and at large drain and gate bias voltages. The main objective of this work is to develop an exact analytical model for determining the threshold voltage of short-channel MOSFETs.

1.5 Summary of the thesis

Several models have been developed recently to determine the threshold voltage of MOSFETs. Different approaches are used by different authors to consider the short-channel effects. In this thesis, two-dimensional Poisson's equation is solved for MOSFET operating in the subthreshold region to determine the potential distribution inside the MOSFET analytically. The analytical model is used not only to calculate the threshold voltage but also to explain several short-channel effects.

The two-dimensional Poisson's equation is solved by using a quasi-two-dimensional approach for solving surface potential in the MOSFET. The energy-band diagram for the ideal case, calculation of threshold voltage, nonideal effects on MOSFET is discussed in chapter 1. In chapter 2 small geometry effects are discussed, such as, short-channel effect, effects of drain voltage on threshold voltage, narrow-width effect & small geometry effects.

The analytical model developed in chapter 3 is used to determine the threshold voltage of a MOSFET for different operating conditions and also for different effective channel lengths. The results are given in chapter 4. Several short-channel effects are also described in this chapter using the model in chapter 3.

Chapter 5 contains the concluding remarks along with recommendations for further work on this topic.

CHAPTER 2

SMALL GEOMETRY FFFECTS

2.1 Introduction

As MOS devices are scaled down to near and submicrometer dimensions, geometry effects resulting from this scaling can produce variations in device performance. Such variations can have a severe impact on circuit design and performance and therefore must be predictable. Geometry effects include the variations in the threshold voltage and sub-threshold current as a function of short, narrow, and small device dimensions. An accurate prediction of the threshold voltage is needed to determine circuit noise margins, speed, and required node voltages. An accurate prediction of the subthreshold current is needed to determine off-state power dissipation and memory refresh times. Other important effects that occur, as devices become smaller are velocity saturation, hot electron injection, and enhanced device performance as devices shrink.

2.2 Short-Channel Effect

A MOS device is considered short when the channel length is of the same order of magnitude as the source and drain junction depletion depths. Modulation of the threshold voltage for short-channel devices has been observed experimentally but is not predicted by the classical threshold voltage expression. This modulation results in a reduction of the threshold voltage as the channel lengths becomes small and is one of several of the short- channel effects.

Before discussing the various models describing the short-channel effect, it is relevant to review the classical threshold voltage derivation. The classical threshold voltage expression is derived by assuming that both the length and width of the devices are large. Thus we may assume that the electric field normal to the gate electrode is much greater than the electric field parallel with the channel. Hence a one - dimensional treatment of the problem is sufficient. It is important to note that this analysis implies that the built-in potentials produced by both the source- and drain-depletion regions can be neglected. This is not a valid assumption for short-channel devices.

The threshold voltage expression for a large-geometry MOSFET can be obtained from the charge conservation law in the region bounded by the gate electrode and the semiconductor bulk. The sum of this charge is

$$Q_G + Q_f - (Q_n + Q_B) = 0 \tag{2.1}$$

Where :

Q_G = charge on polysilicon electrode

Q_f = fixed charge in SiO2

Q_n = inversion-layer charge due to free carriers induced in channel region

Q_B = Bounded charge per unit area due to the ionized impurity concentration in the depletion region

The definition of the threshold voltage implies $Q_n = 0$. Expressing Eqn. (2.1) in terms of voltages for an n-channel MOSFET gives

$$_G = V_{FB} + \phi_S + \frac{Q_B}{Q_o} \tag{2.2}$$

Where

V_{FB} = flatband voltage, including effects of fixed surface charge, distributed charge in oxide, and difference in work functions

ϕ_s = Surface potential

C_o = oxide capacitance per unit area

At turn-on, the surface potential locks at approximately $2\phi_f$. Therefore, the threshold voltage for a large -geometry MOSFET is given by

$$_T = V_{FB} + 2\phi_f + \frac{Q_B}{C_o} \tag{2.3}$$

Where

$Q_B = qN_AW_C$

q = electric charge

N_A = effective doping concentration

W_C= channel-depletion depth

Eqn. (2.3) is valid as long as the channel length is long compared to the source and drain junction depletion depths and the width is wide compared to the depth of the gate-induced depletion region. Fig. 2.1 illustrates the cross section of a large geometry MOSFET. The depth of the source and drain -depletion regions W_S and W_D can be obtained from Poisson's equation using the abrupt junction approximation.

This is a good assumption since both source and drain regions are doped much higher than the substrate. The depletion approximation can be applied under gate in the substrate to obtain the channel depletion depth W_C. The concept of charge sharing both provides physical insight into the development of the threshold voltage

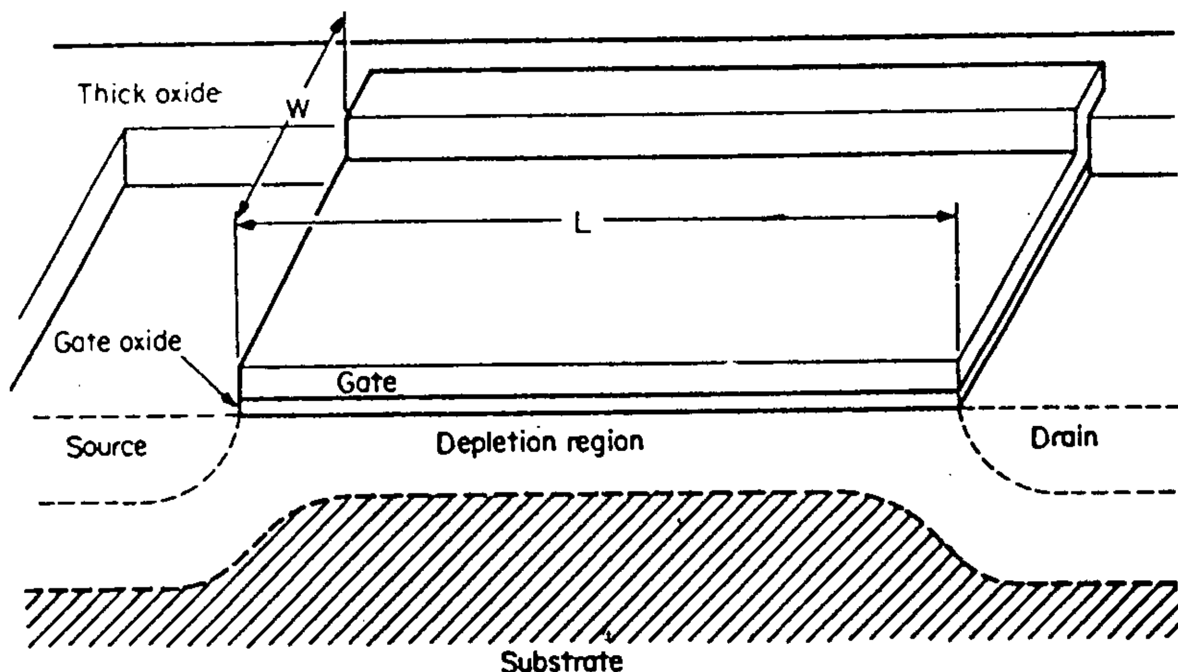

Fig. 2.1 Cross section of large geometry MOSFET.

expression and predicts trends correctly. From Eqn. (2.3) the total amount of charge under the gate determines in part the threshold voltage. If the channel length L is much greater than either the source- or drain -depletion regions, the charge sharing which occurs from these regions can be neglected. Using this assumption and Fig. 2-1, the total amount of charge induced by the gate voltage is approximately given by

$$Q_{BT} = q\, N_A W_C W L \qquad (2.4)$$

or

$$Q_B = q\, N_A W_C WL/WL = qN_A W_C \qquad (2.5)$$

where Q_{BT} is the total bound charge, and W is the width of the device .

Hence Eqn. (2.3) can be considered a very good approximation for the threshold voltage in large devices. If the length is reduced to a distance comparable to W_S and W_D, part of the charge, which is induced under the gate, is also contained in the source or drain regions (Fig. 2.2). In other words, charge sharing is occurring in both the source- and drain-depletion regions with the gate region. This implies that a rectangular region can no longer approximate the total effective charge induced under the gate. Hence the amount of the charge -reflected to the gate electrode can be expected to be reduced. Since Q_B reflects this charge reduction as L decreases, the threshold voltage given by Eqn. (2.3) will also decrease.

A two-dimensional model, which demonstrates the short-channel effect and also allows a close-form solution of the threshold voltage, is shown in Fig. 2.3

Though simple, this model provides physical insight into the charge -sharing concept. The area outlined by BCEM represents the rectangular region containing the total charge induced under gate for a long-channel device with the substrate grounded. As the channel length is reduced, the effects of the source- and drain-depletion regions cannot be neglected. For the case when both source and drain are grounded and the surface is strongly inverted, the potential along ABCD is zero.

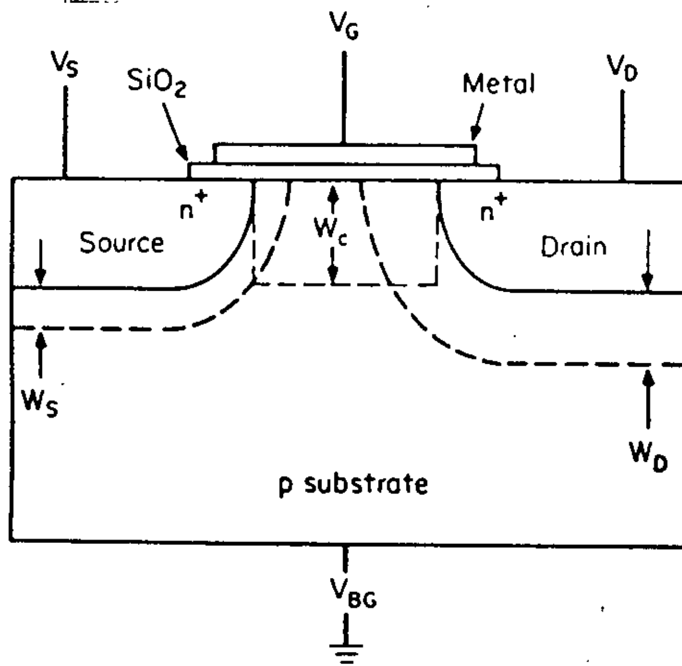

Fig. 2.2 Charge-sharing Model.

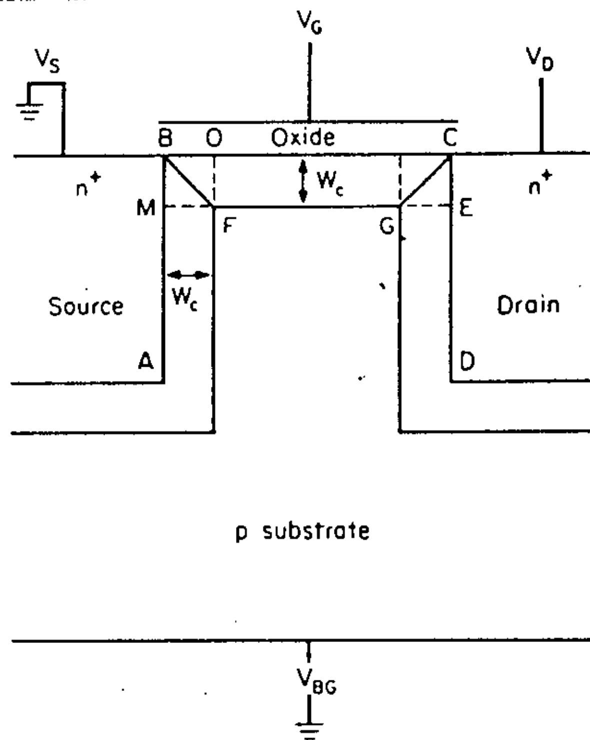

Fig. 2.3 Approximate short-channel model.

Hence, the potential of MBO is zero. The maximum potential from F to M is approximately equal to the maximum potential from F to O. This is true since at inversion the built-in potential V_{bi} is to a rough approximation equal to $2\phi_f$. Thus we may assume $W_S = W_C$. This implies that the charge contained in the square FMBO is equally supported by both source and gate. In other words, half the charge can be considered to be supported by the source. Assuming $V_D = 0$, the same analysis can be applied to the drain region. Hence the total charge enclosed can be approximated by the trapezoidal region BCGF. This simple model becomes more accurate with an applied back-gate bias since the maximum potential at FM and FO correspond to $V_{BG} + V_{BI}$ and $V_{BG} + 2\phi_f$ respectively at inversion. By substrating the triangular regions donated by FBM and CEG from the rectangular region MBCE, the total volume compromising the modified bulk charge term is

$$Q_{BT} = qN_A(WLW_C) - 2W\left(\frac{W_C W_C}{2}\right) \quad (2.6)$$

using Eqn. (1-21), the threshold voltage is

$$V_T = V_{FB} + 2\phi_f + qN_A\,(WLW_C - WW^2_C)/C_O WL \quad (2.7)$$

Or

$$V_T = V_{FB} + 2\phi_f + \frac{Q_B}{C_O}\left(1 - \frac{W_C}{L}\right) \quad (2.8)$$

with

$$W_C = \left[\frac{2\varepsilon_s\varepsilon_o(V_{BG}+2\phi_f)}{qN_A}\right]^{1/2}$$

where $2\phi_f$ is the surface potential at the onset of strong inversion, and $\varepsilon_s\varepsilon_o$ is the dielectric constant of the semiconductor.

2.3 Effects of drain voltage on threshold voltage

The model used to describe the MOSFET shown in Fig. 2.4 assumes the drain is shorted to the source.

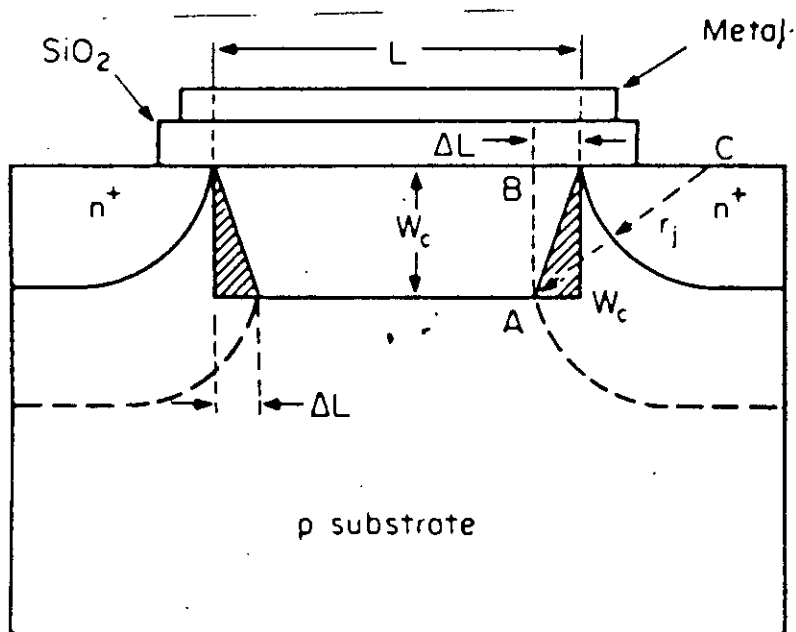

Fig. 2-4 short -channel model with curved source-drain junctions.

This configuration is of course not true in any realistic device structure. Therefore, we must modify the short-channel threshold voltage expression to include the drain voltage V_D. The most immediate effect of the drain voltage is the increase in the extent of the drain-depletion region into the channel. The extension of the depletion region into the channel can be approximated by the abrupt diode depletion depth as

$$\sqrt{\frac{2\varepsilon_s\varepsilon_o(V_{BI}+V_{BG})}{qN_A}} \tag{2.9a}$$

where V_{BG} is the back-gate bias, and V_{BI} is the built-in potential.

For zero back gate, the extent of the drain-depletion region is from 0.3 to 0.8 μm for most typical devices. If a drain voltage of 5 V is applied, the expression to calculate the extension of the depletion region is modified to be

$$\sqrt{\frac{2\varepsilon_o\varepsilon_s(V_{BI}+V_{BG}+V_D)}{qN_A}} \tag{2.9b}$$

for a drain voltage of 5V, the depletion region can expand to greater than 2 μm. This increase is not negligible and must be accounted for in our threshold voltage expression.

2.4 Narrow - width effect

A MOSFET is considered narrow if the width of the device is of the same order of magnitude as the depth of the channel-depletion region. In practice, for a channel - depletion depth of 0.5 μm, device widths of 5 μm or less affect the electrical behavior of the device.

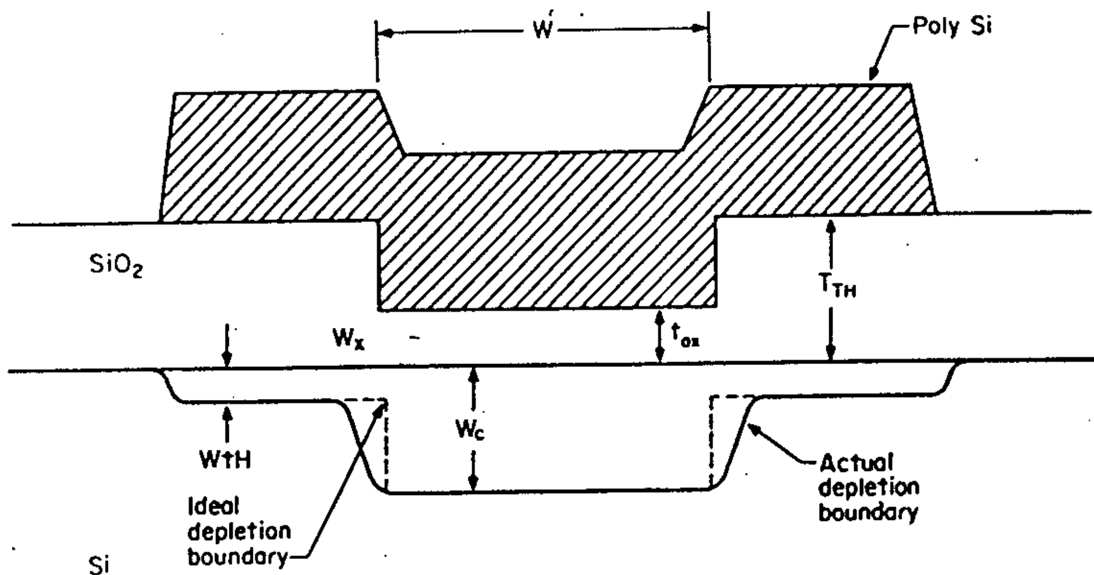

Fig. 2-5 Width crosses section.

The polysilicon gate overlaps the nonrecessed thick oxide on both sides of the thin gate oxide. The narrow-width effect is characterized by an increase in the threshold voltage as the width W is reduced. As W is reduced, the volume of charge in the gate region is reduced, whereas in the thick oxide region the volume of charge remains constant. This fixed amount of charge becomes increasingly significant as W is reduced and contributes to an increased threshold voltage.

2.5 Small-geometry effects

A small-geometry MOSFET is defined as a device with a channel length of the same order of magnitude as the junction-depletion depth and the channel width is of the same order of magnitude as the channel-depletion depth. For such small devices, neither just the short-channel nor the narrow-width expression is sufficient to predict the threshold voltage accurately. An expression that includes both of these effects plus the coupling of these effects is required.

CHAPTER 3

MATHMATICAL ANALYSIS FOR POTENTIAL DISTRIBUTION IN MOSFETS

3.1 Introduction

The characteristics of a MOSFET can be studied by obtaining the potential distribution within the device. In case of long-channel MOSFET, the effects of the source and the drain on the channel region are negligible and electric field lines originating from the gate are assumed to have no components in the lateral direction. Solutions of the Poisson's equation give the potential function in such devices. But in case of short-channel devices, the source and the drain junctions contribute to the potential function in the channel region and a two-dimensional analysis of Poisson's equation becomes necessary. The boundary conditions imposed by the source/drain

junctions are considered in addition to the gate and substrate voltage. When a short channel device is analysed the model fails to predict the accelerated V_{TH} reduction at very short-channel length. The technique of using a quasi-two-dimensional approach, the accelerated V_{TH} reduction observed in the very short-channel range can be accurately predicted. The technique is used in this chapter to find the analytical expression for the potential and threshold voltage expression.

3.2 Mathematical modelling of surface potential

By applying Gauss's law to a rectangular box (Gaussian box) of height X_{dep} and length Δy in the channel depletion region (Fig. 3.1) and neglecting mobile carrier charge, the following equation can be derived [15]

$$\varepsilon_{Si}\frac{X_{dep}}{\eta}\frac{dE_s}{dy}+\varepsilon_{OX}\frac{V_{GS}-V_{FB}-V_s(y)}{T_{OX}}=qN_{SUB}X_{dep} \tag{3.1}$$

where:

X_{dep} = the depletion layer thickness

$E_S(y)$ = the lateral surface electric field

$V_S(y)$ = the channel potential at the Si-SiO_2 interface

V_{GS} = the gate-source voltage.

V_{FB} = the flatband voltage.

N_{SUB} = channel doping.

T_{OX} = the gate-oxide thickness

ε_{SI} = Permittivity of Si

ε_{OX} = Permittivity of SiO_2

$$X_{dep} = \sqrt{\frac{2\varepsilon_{SI}(\phi_s - V_{BS})}{qN_{SUB}}}$$

V_{BS} = the substrate bias

$\phi_s = 2\phi_B$ the surface potential at the threshold of surface inversion

η = fitting parameter

The first term on the left hand side of Eqn. 3.1 is equal to the net electric **flux** entering the Guassian box along the y direction. The second term represents the electric flux entering the top surface of the Guassian box. There is no electric flux passing through the bottom of the Guassain box. The right hand side represents the total charge inside the guassian box.

The solution to Eqn. 3.1 under the boundary conditions of $V_S(0) = V_{bi}$ and $V_S(L) = V_{DS} + V_{bi}$ (the substrate potential is taken as ground) is

$$V_S(y) = V_{sL} + (V_{bi} + V_{DS} - V_{sL})\frac{\sinh(y/l)}{\sinh(L/l)} + (V_{bi} - V_{sL})\frac{\sinh[(L-y)/l]}{\sinh(L/l)} \quad (3.2)$$

where,

$V_{sL} = V_{GS} - V_{tho} + \phi_S$ represents the long-channel surface potential, and

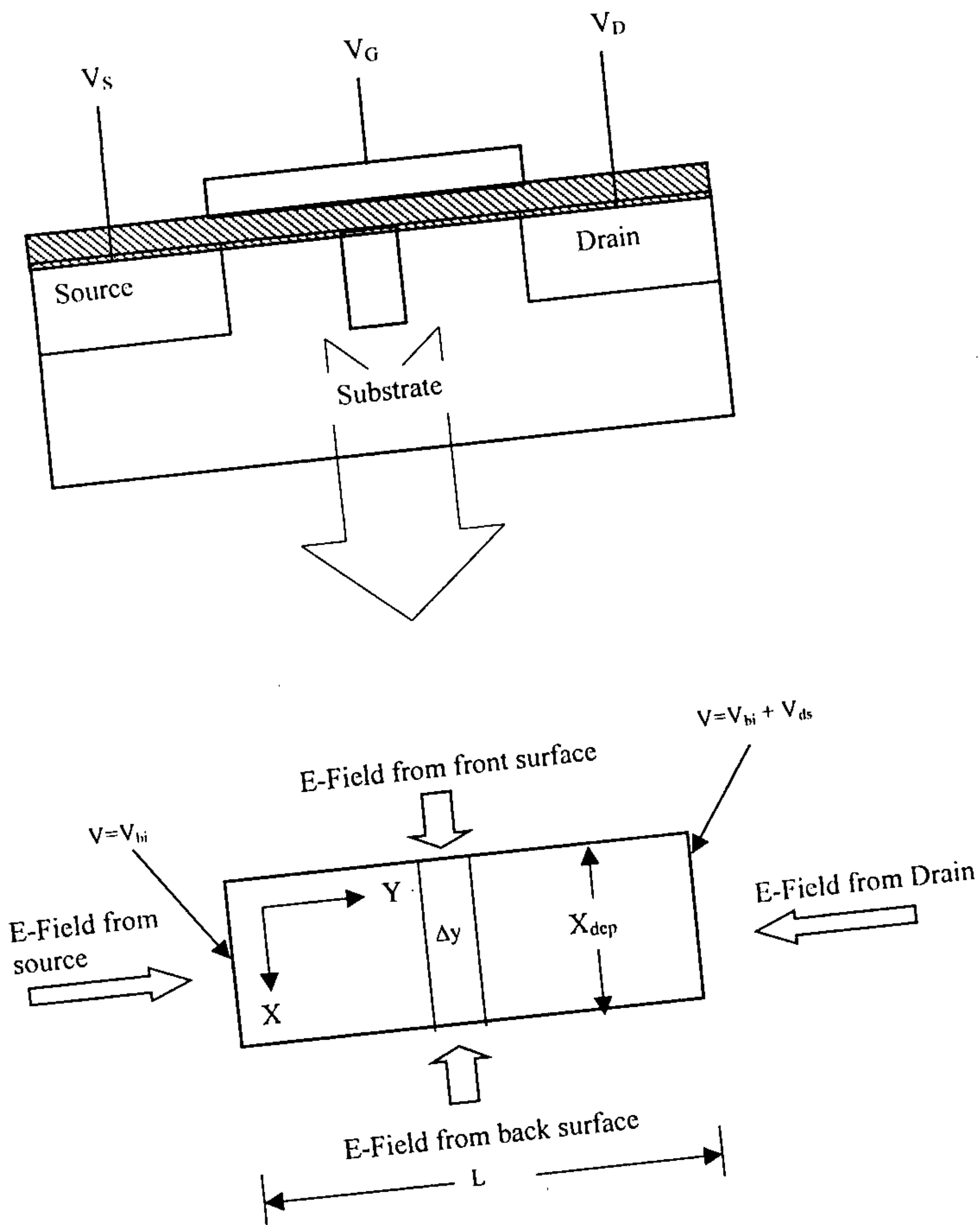

Fig. 3.1 A typical MOSFET is shown above and Guassian Box representation of its channel depletion region with boundary condition.

$V_{tho} = V_{FB}+qN_{SUB}X_{dep}T_{OX}/\varepsilon_{OX} + \phi_s$ represents the long-channel threshold voltage

V_{bi} = the built -in potential between the source-substrate and drain-substrate junctions

l = the characteristic length, defined as

$$l = \sqrt{\frac{\varepsilon_{Si} T_{OX} X_{dep}}{\varepsilon_{OX} \eta}} \quad (3.3)$$

Note that X_{dep} is assumed to be constant when solving Eqn. (3.1). In reality, X_{dep} is a function of the drain voltage and the channel length. Keeping in mind that the effects of the variation of the lateral field in the depletion layer under the channel are incorporated through the fitting parameter η, one may treat the term X_{dep}/η in Eqn. (3.3) as an average of the depletion layer thickness along the channel. Although η (hence Eqn. 3.1) may also be a function of the drain voltage. This quasi-two-dimensional approximation simplifies the solution of Eqn. 3.1, yet retains accuracy. Therefore, η is treated as a constant for a given technology in the following discussion unless otherwise specified.

3.3 Determination of Minimum Surface Potential

The channel potential has a minimum at y_0 which can be found by solving the equation $dV_s(y)/dy = 0$. Location y_0 and minimum potential V_S can be obtained numerically by solving

$$V_{smin} = V_s(y_0) \tag{3.4a}$$

$$\frac{dV_s}{dy}\Big|_{y=y0} = 0 \tag{3.4b}$$

The solution of Eqn. 3.4a for y_0 is given by:

$$y_0 = \frac{l}{2}\log\left(\frac{(V_{bi} - V_{sL})\exp(L/l) - (V_{bi} + V_{DS} - V_{sL})}{(V_{bi} + V_{DS} - V_{sL}) - (V_{bi} - V_{sL})\exp(-L/l)}\right) \tag{3.5}$$

When L >> l the above expression can be approximated as follows:

$$y_0 = \frac{L}{2} - \frac{l}{2}\log\left(\frac{V_{bi} - V_{sL} + V_{DS}}{V_{bi} - V_{sL}}\right) \tag{3.6}$$

Substituting Eqn. 3.5 for $y = y_0$ in Eqn 3.2, we get the minimum potential V_{smin} which is given by:

$$V_{smin} = V_{sL} + \frac{1}{\sinh(L/l)}\left(\begin{array}{l} 2V^2_{sL}(\cosh(L/l) - 1) \\ +2V_{sL}(-\cosh(L/l) + 1)(2V_{bi} + V_{DS}) \\ +2(V_{bi} + V_{DS})\cosh(L/l) - (V_{bi} + V_{DS})^2 - V^2_{bi} \end{array}\right) \tag{3.7}$$

2.4 Determination of Threshold Voltage

The threshold voltage, V_{th} is defined as the gate voltage at which $V_{smin} = 2\phi_F$.This equation can be solved analytically for V_{SL} and hence for V_{GS}. The result is given by

$V_{th} = V_{tho} - V_{TH}$ where

$$\Delta V_{TH} = 2\phi_F + \frac{b - \sqrt{b^2 - 4ac}}{2a} \tag{3.8}$$

where

$a = 2[\cosh(L/l) - 1] - \sinh^2(L/l)$

$b = 2[-\cosh(L/l) + 1](2V_{bi} + V_{ds}) + 4\phi_F \sinh^2(L/l)$

$c = 2V_{bi}(V_{bi} + V_{DS})\cosh(L/l) - (V_{bi} + V_{DS})^2 - V^2_{bi} - 4\phi_F^2 \sinh^2(L/l)$

From Eqn. 3.8 we conclude that the dependence of ΔV_{TH} on V_{DS} has a functional form of $AV_{DS} + B\sqrt{V_{DS}}$. To first order, A and B are dependent only on the device parameters. In the above analysis, we ignored voltage drop across the heavily doped drain region. This assumption is valid as long as V_{DS} is small. For large drain voltage, the voltage drop in the drain region should be subtracted from $V_{bi}+V_{DS}$.

CHAPTER 4

RESULTS BASED ON ANALYTICAL SOLUTION

4.1 Introduction

The characteristics of a MOSFET is determined by its physical parameters like channel length, oxide width, substrate doping, source/drain doping, junction depth, junction curvature etc. The operating conditions like drain-source voltage, substrate biasing etc. also produce considerable influence on device characteristics, especially in case of short-channel devices. The dependency of the potential distribution in a MOSFET on device configuration and operating conditions causes the device characteristics like surface potential, depletion width, channel conductivity etc. to vary from one transistor to another. This causes the threshold voltage of a MOSFET to depend on device parameters and operating conditions. The mathematical model developed in the previous chapter is used here to determine the threshold voltage along with other characteristics of a MOSFET. The effects of channel length and the drain voltage on these characteristics are particularly studied.

4.2 Results and discussion

4.2.1 The surface potential

The surface potential along the channel length is given by Eqn 3.2. The first term in (3.2) represents the effect of the depletion layer charge on the surface potential. The contribution of the gate, substrate, source and drain voltages are given by the successive terms, the effect of the source voltage is found to be maximum at the source end (y = 0) due to the presence of the factor $\frac{\sinh\ (L-Y)/l}{\sinh\ L/l}$. Similarly, the effect of drain voltage is distributed along the channel length by the factor $\frac{\sinh\ (y/l)}{\sinh\ (L/l)}$. The numeric value of these two hyperbolic factors decay almost exponentially along the direction away from the respective source or drain end. The consequence is the barrier-lowering effect as described in section 3.2. for shorter channel lengths, the hyperbolic terms decreases in a slower rate and the 'edge effects' become more prominent.

Fig 4.1a shows the surface potential along the channel for different channel lengths. The device parameters are : T_{OX}=100Å, N_{SUB}=5E10^{16}cm^{-3}, N^{+}=10^{20}cm^{-3} and η=1. In contrast to the constant channel potential assumed by the charge-sharing model, the new model predicts large variations in potential along the channel for devices with short-channel lengths even when the drain voltage is low. The channel potential has a minimum at y_0 which is given by (3.5).

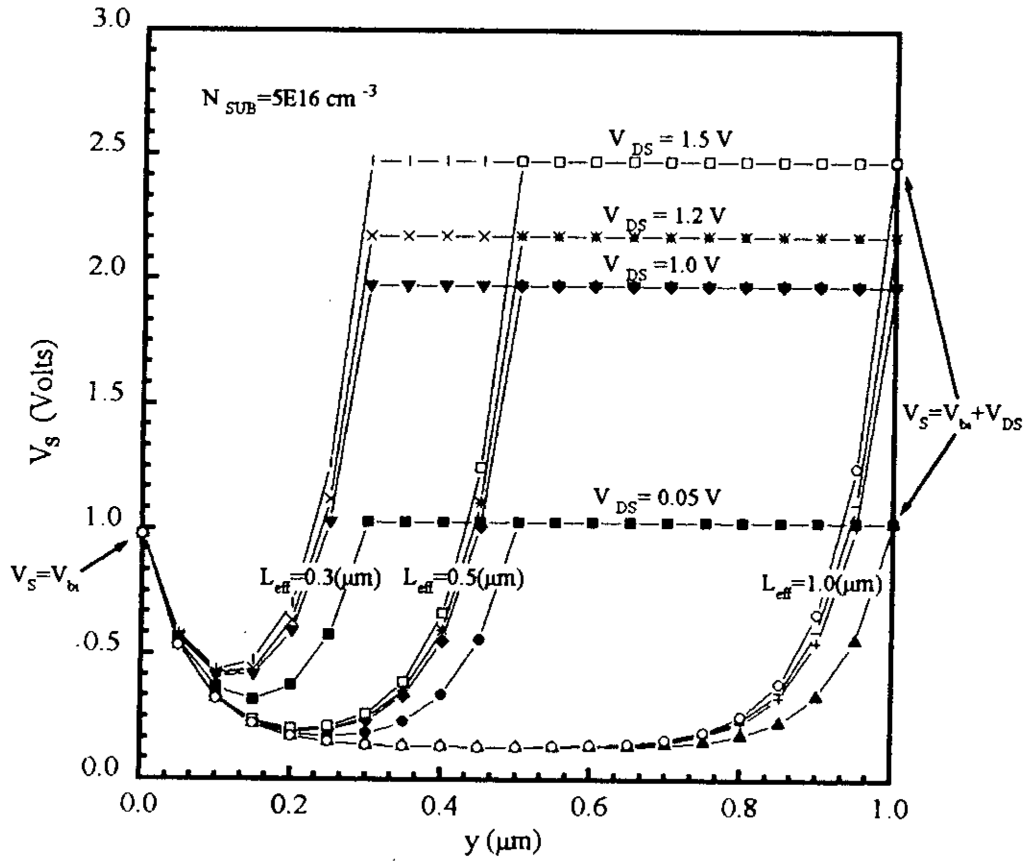

Fig. 4.1a Calculated surface potential along channel for different channel lenghts. The device parameters are : T_{ox}=100 A°, N_B=5E16 cm $^{-3}$, N^+=1E20 cm $^{-3}$.

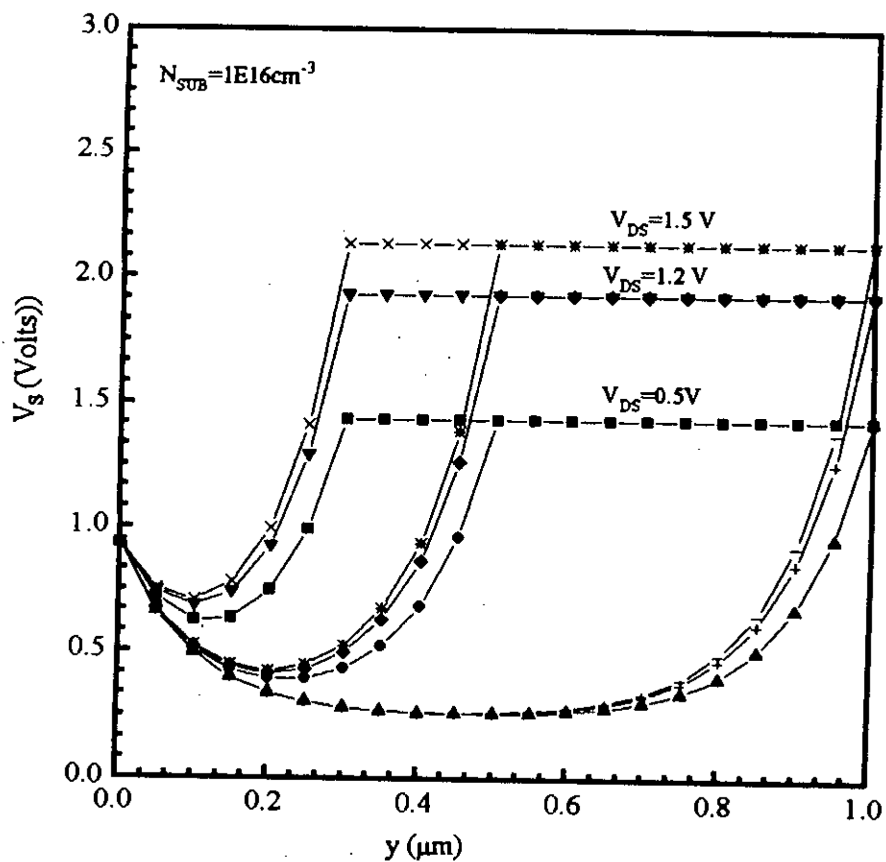

Fig. 4.1b Calculated surface potential along channel for different channel lengths. The device parameters are: T_{ox}=100 A^0, N_B=1E16 cm $^{-3}$, N^+=1E20 cm $^{-3}$.

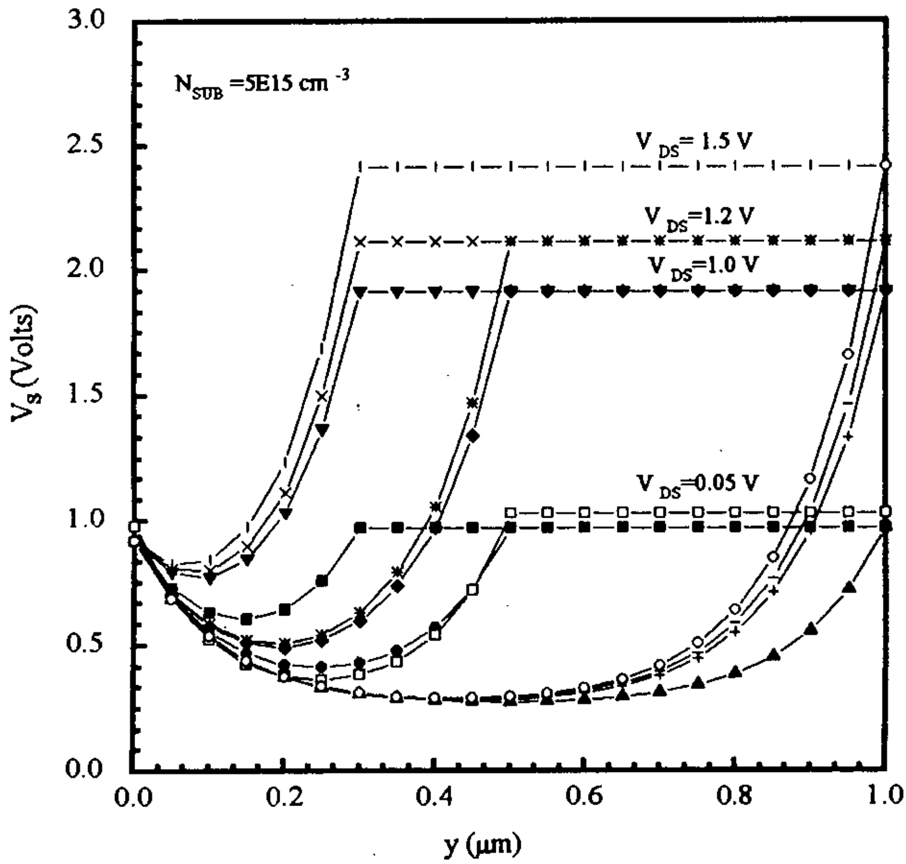

Fig. 4.1c Calculated surface potential along channel for different channel lengths. The device parameters are: T_{ox}=100 A^0, N_B=5E15 cm $^{-3}$, N^+=1E20 cm $^{-3}$.

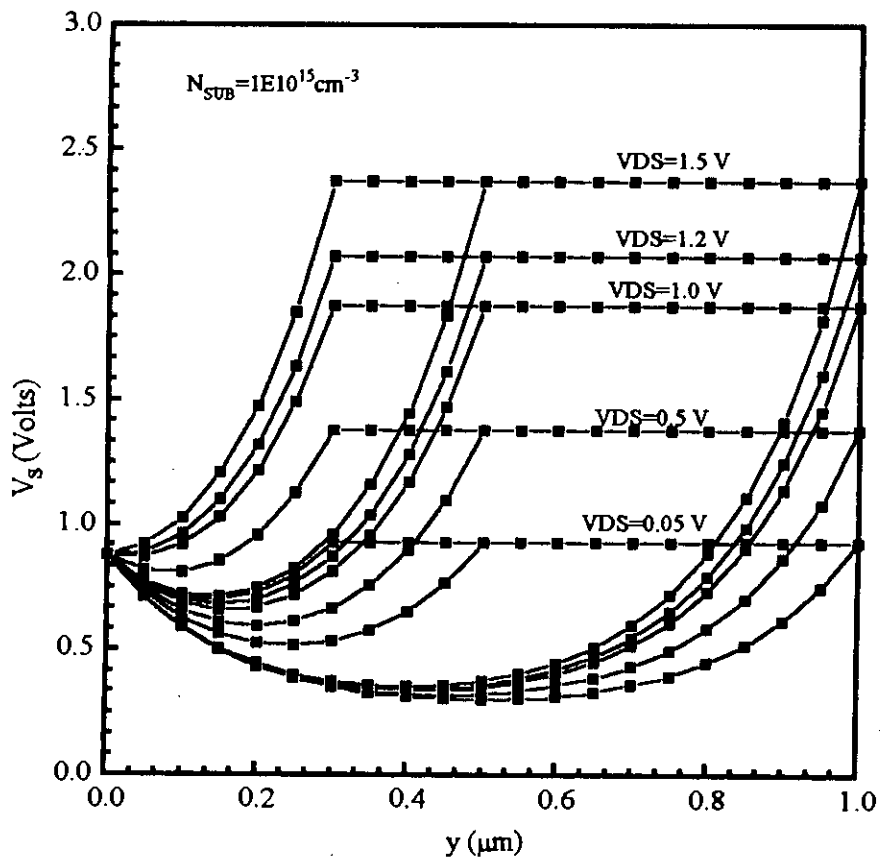

Fig. 4.1d Calculated surface potential along channel for different channel lengths. The device parameters are: T_{ox}=100 A^0, N_B=1E15 cm $^{-3}$, N^+=1E20 cm $^{-3}$.

Figs. 4.1(a) to 4.1(d) show the variation of surface potential with the channel length for different V_{DS} and substrate dopings. Large variations in channel potential are observed for high level of source to drain voltage. It is also observed that the effective channel length decreases with reducing the substrate doping. The minimum value of channel potential will increase, i.e., the potential barrier for electron flow from source to drain will decrease, with decreasing channel length and increasing drain voltage.

The location of barrier peak y_0 as a function of channel length is shown in Figs. 4.2(a)-(c) for different V_{DS}, the substrate doping as the parameter. The barrier peak y_o decreases with the increase of V_{DS} . However, these variation is small for high channel doping. It is also observed that the change in barrier height Δy_0 due to change in V_{DS} is small for higher substrate doping.

Fig. 4.3 shows the variation of y_o with V_{DS} for various substrate doping. This figure shows that the barrier peak y_0 decreases with reducing the channel doping for the same value of V_{DS}, that indicates the reduction of barrier height for low substrate doping

Figs. 4.2 and 4.3 can show that the location of barrier peak y_0 is approximately equal to L/2 when the drain to source voltage V_{DS} is small. In general, when V_{DS} is not small, y_0 will no longer equal to L/2.

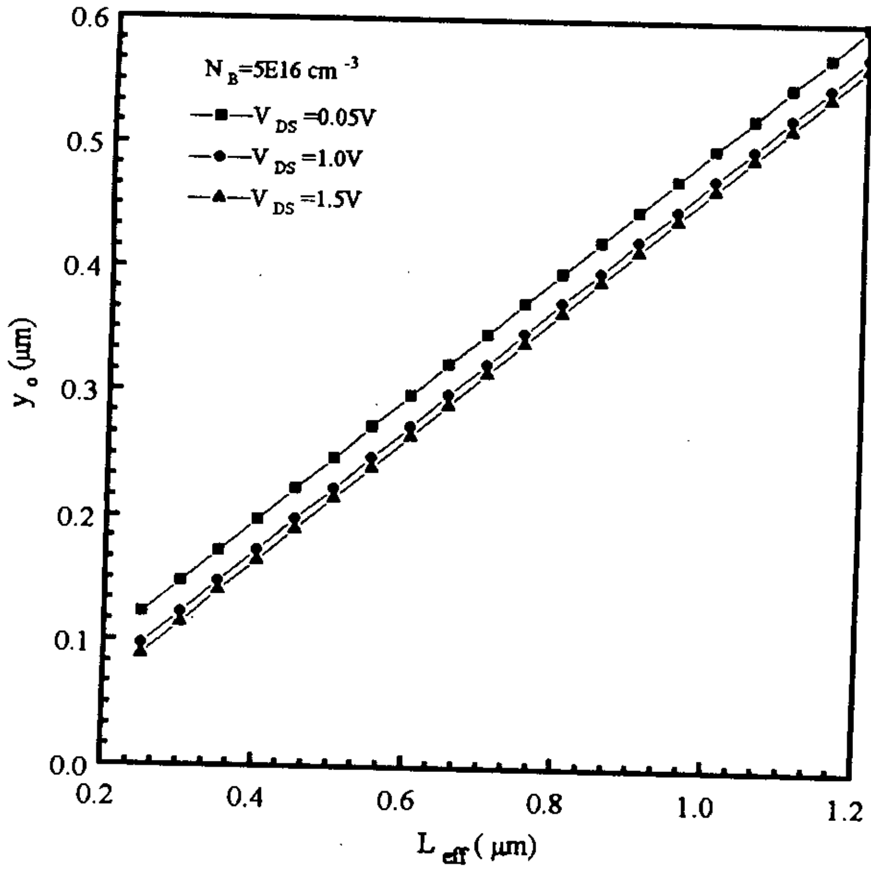

Fig. 4.2a Variations of barrier peak for N_B =5E16 cm $^{-3}$, with the channel lengths L_{eff} for different values of V_{DS}.

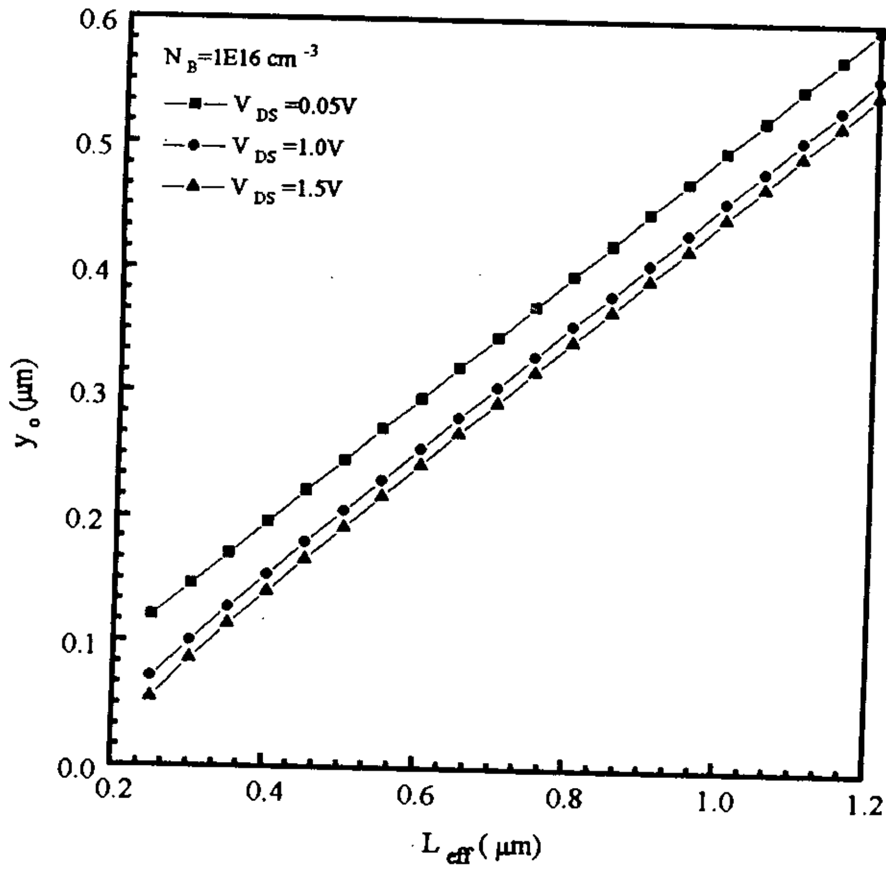

Fig 4.2b Variations of barrier peak for N_B = 1E16 cm $^{-3}$, with the channel lengths L_{eff} for different values of V_{DS}.

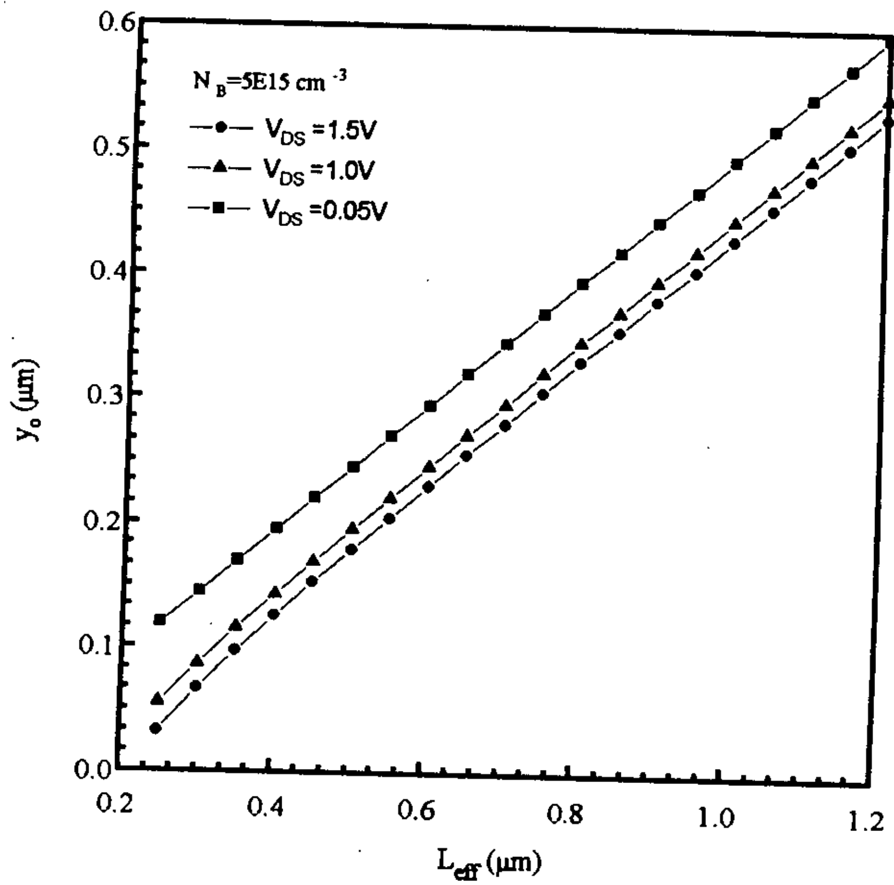

Fig 4.2c Variations of barrier peak for N_B=5E15 cm $^{-3}$, with the channel length L_{eff} for different values of V_{DS}.

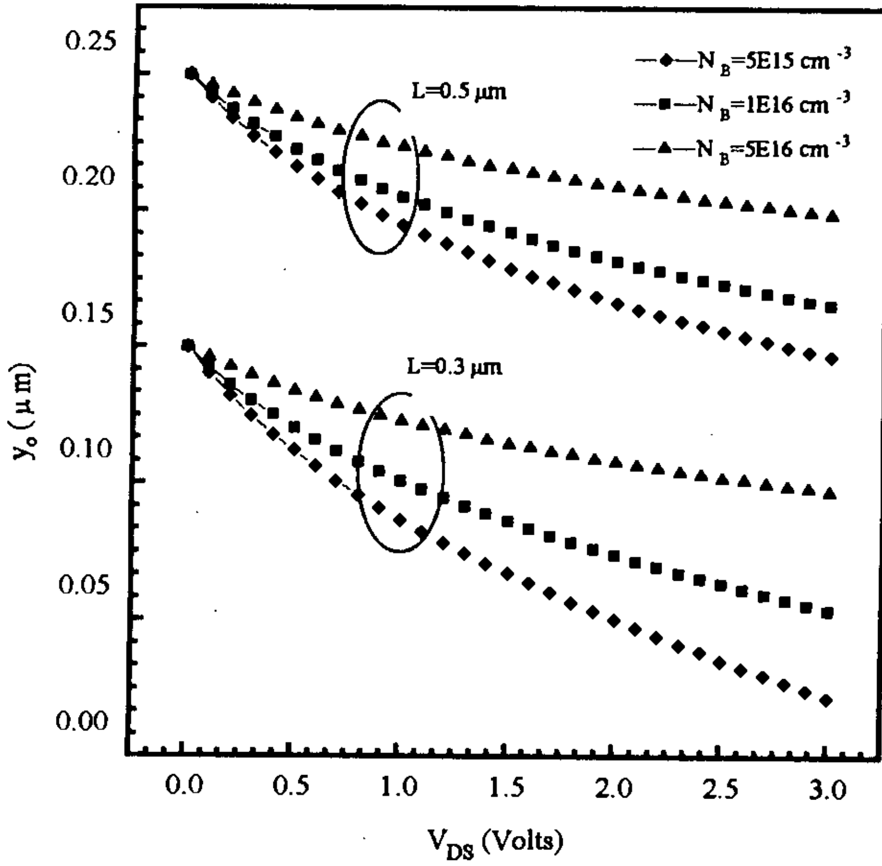

Fig. 4.3 Variations of barrier peak y_0 with V_{DS} for various channel doping N_B and channel lengths of L =0.3 μm and L =0.5 μm.

4.2.2 Threshold Voltage

Fig. 4.4 shows the threshold voltage versus drain voltage with different channel length for T_{OX} =50 Å. The figure shows that V_{th} decreases as V_{DS} increases. The shorter the channel length, the more severe the decrease of V_{th}. An accurate prediction by this model is that, when L_{eff} decreases, V_{th} is no longer linearly dependent on V_{DS} as was predicted by common drain induced barrier lowering (DIBL) models [14]. This non-linearly dependency of V_{DS} for every -short channel devices is predicted by Eqn. (3.9). According to (3.9), the relation between V_{th} & V_{DS} is linear at large values of V_{DS}.

Fig. 4.5 and 4.6 shows the same variation of threshold voltage with V_{DS} for different channel length for the oxide thickness of T_{OX} =100Å and T_{OX} =400Å respectively. For the short channel device, the decrease in threshold voltage is greater for the thick oxide. The above results implies that the two dimensional field distribution is more enhanced for the devices with thicker oxide.

Fig 4.7 shows the variation of V_{th} with V_{DS} for different source concentration for the channel length of 0.3 μm. Higher source concentration reduces the threshold voltages. However the nature of V_{th} variation with V_{DS} is same as observed in Figs. 4.4 to 4.6.

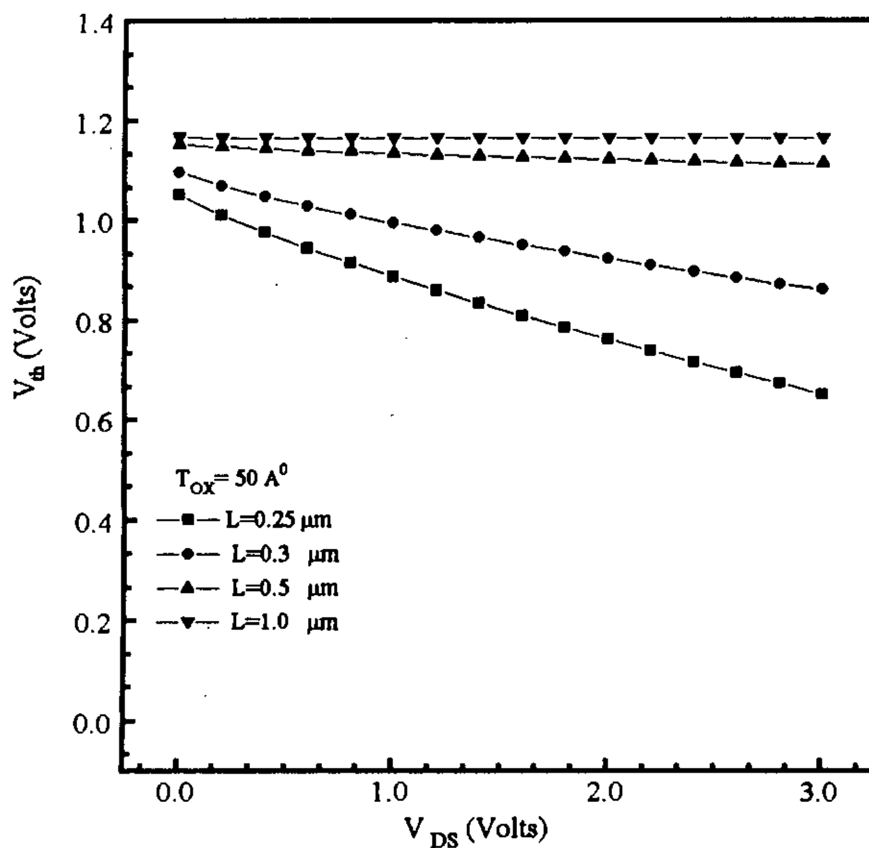

Fig 4.4 The threshold voltage versus drain voltage with different channel lengths for oxide thickness of $T_{OX} = 100A^0$.

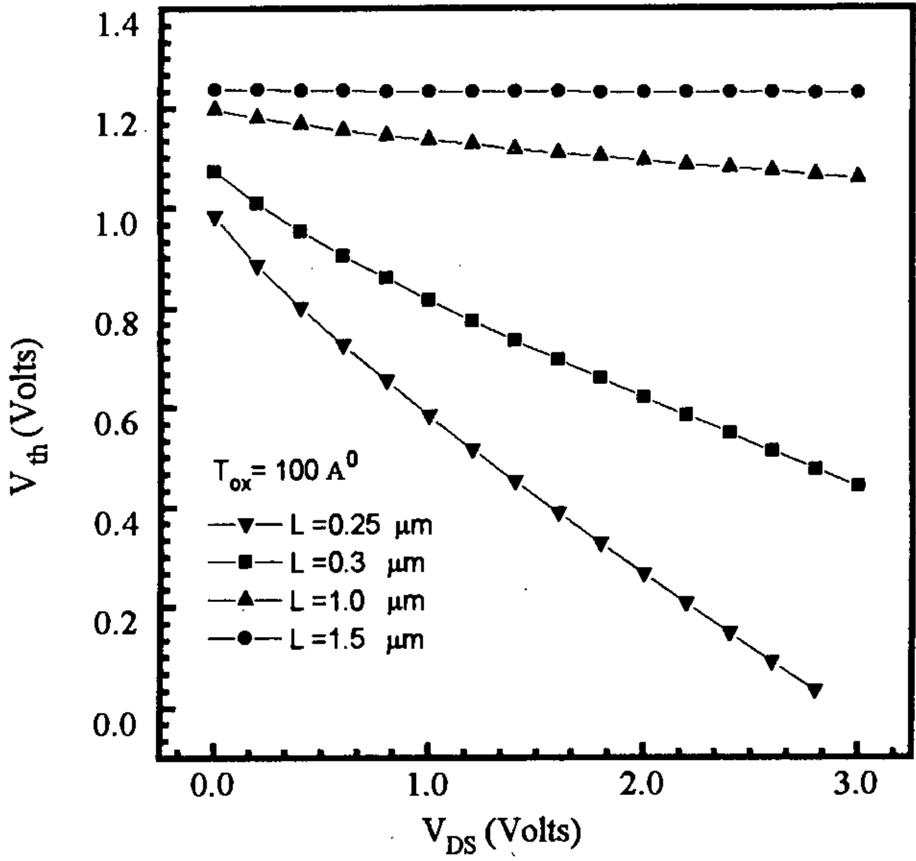

Fig. 4.5 The threshold voltage versus drain voltage with different channel length for T_{OX} = 100A ^{0}.

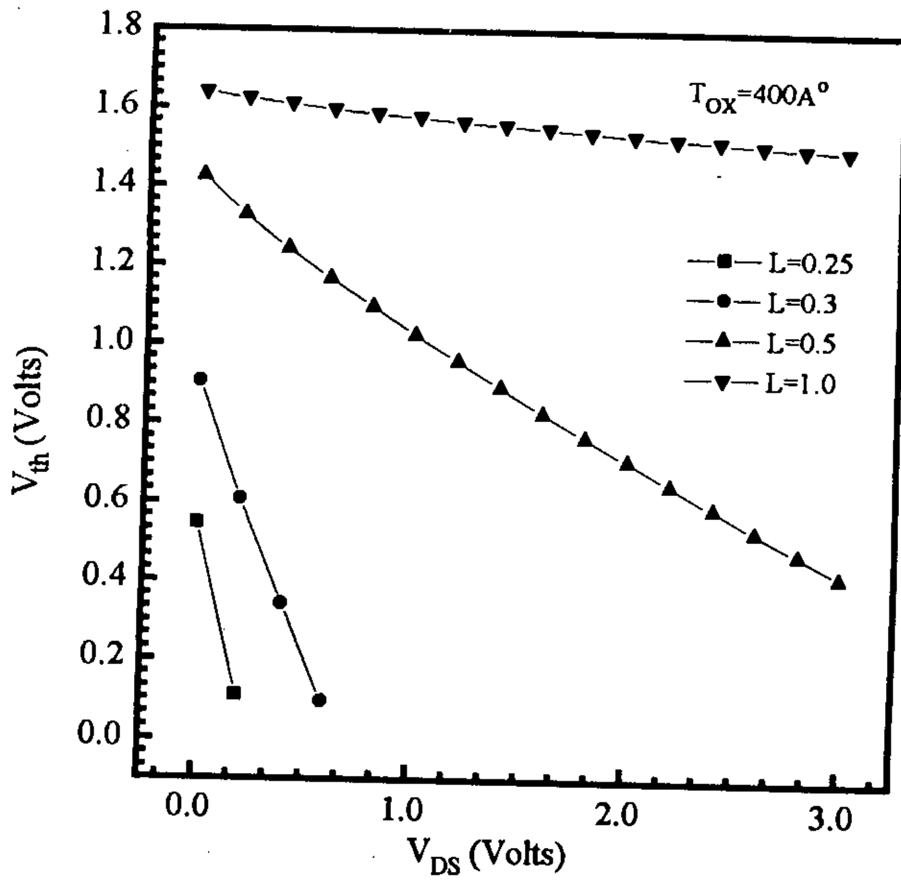

Fig. 4.6 The threshold voltage versus drain voltage with different channel lengths for T_{OX} = 400 A^0.

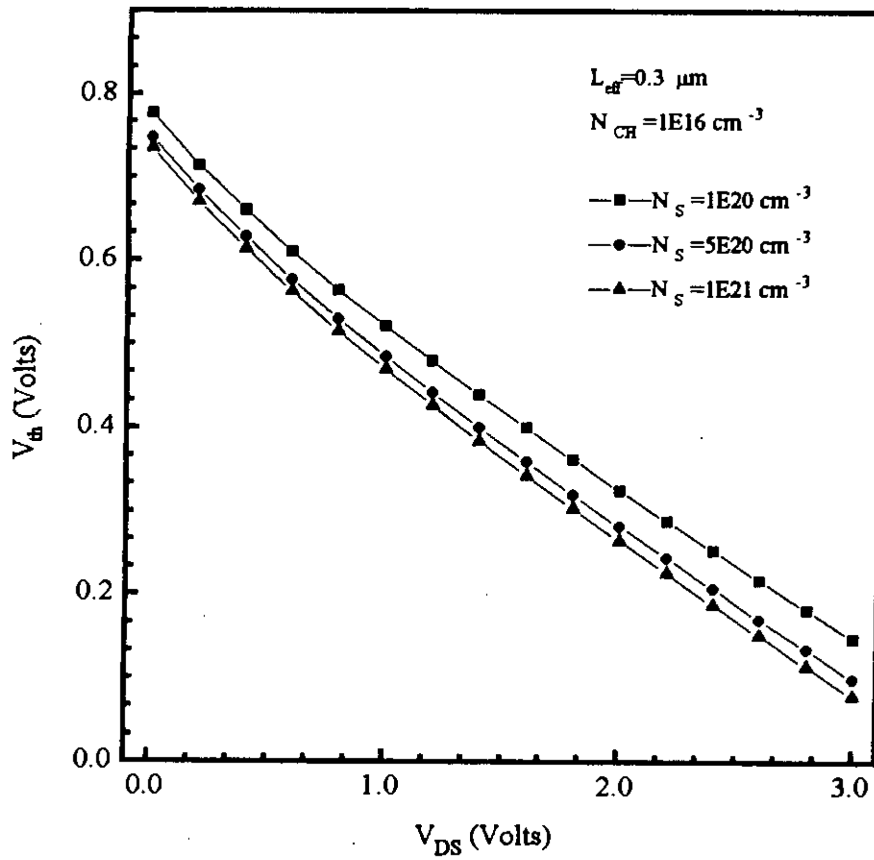

Fig. 4.7 The variations of V_{th} with V_{DS} for different source concentration for the channel length of 0.3 μm.

Figs. 4.8 and 4.9 show the shift of threshold voltage with the channel length for different oxide thickness for V_{DS} =0.005 V and 1 volt respectively. Large variations are observed for small channel lengths and thicker oxide layers. The shift in threshold voltage is independent of larger channel lenghts for thinner oxide thickness. The change in threshold voltage is almost independent for the device of large channel length with small oxide thickness.

The accelerated ΔV_{th} roll-off will set in at small channel lengths than in bulk due to small characteristic length "l". Large changes in ΔV_{th} is observed for high V_{DS} values if we compare Figs 4.8 and 4.9. These figures show that for very short channel-length devices a linear relation between V_{th} and $1/L_{th}$ is not observed.

Fig. 4.10 shows the drain induced barrier lowering (DIBL) versus effective channel length L_{eff} for different oxide thickness, where DIBL is defined as the difference between shift in threshold voltage at V_{DS}=0.005 V and V_{DS}=1.0V. From the figure, it is clear that by reducing the oxide thickness it is possible to make the MOS device small.

Fig. 4.11 shows the minimum effective length L_{eff} versus oxide thickness, considering (DIBL=200 mV/V). From the figure it is observed that a linear relationship between oxide thickness and minimum effective length is established. This linear relation will help to design the MOSFET devices.

3.3 Summary

The mathematical model developed in chapter three is used here to determine the threshold voltage and other characteristics of the MOS device which are related to the threshold voltage. The approach of the analysis and the computational method is also described. Emphasis is given on the effect of device length since miniaturization of the MOSFET has been the general trend of development in VLSI technology. The effect of the operating drain voltage also becomes significant for short channel devices and these effects are also studied. Careful selection of channel doping and oxide thickness for deep submicometer FD MOSFET is important for good device parameters.

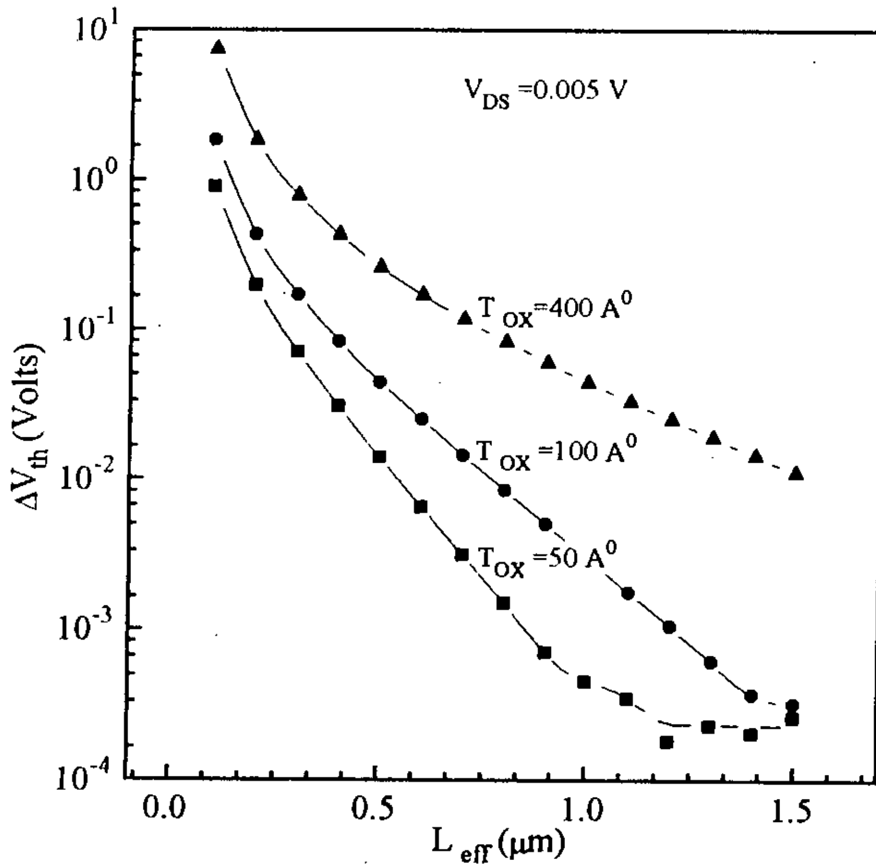

Fig. 4.8 Threshold voltage shift versus effective channel lengths at V_{DS}=0.005V for different oxide thicknesses.

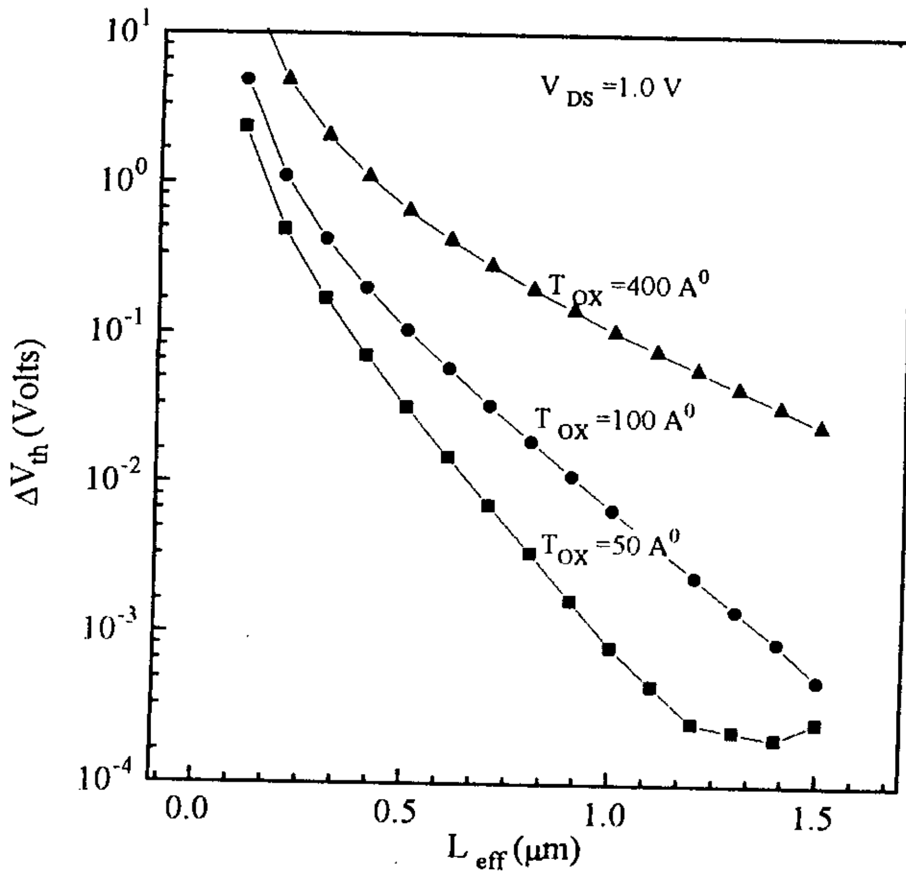

Fig. 4.9 Threshold voltage shift versus effective channel lengths at V_{DS}=1.0V for different oxide thicknesses.

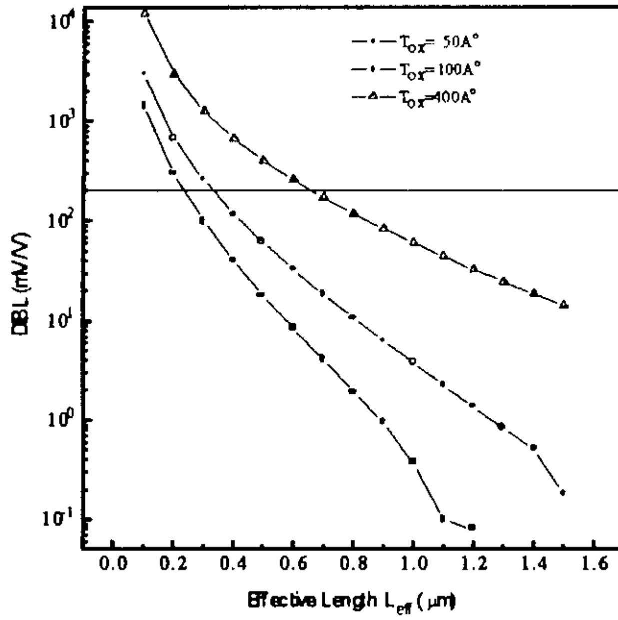

Fig. 4.10 Drain Induced barrier lowering (DIBL) versus effective channel length L_{eff}.

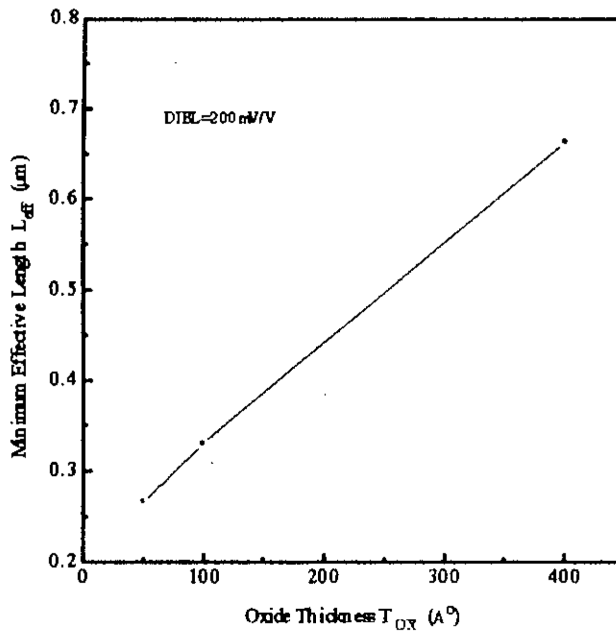

Fig. 4.11 Minimum effective length L_{eff} versus oxide thickness T_{OX}.

CHAPTER 5

CONCLUSIONS

5.1 Conclusions

In this work an analysis is presented to determine the threshold voltage of MOSFETs. The difference between characteristics of the long channel and the short channel MOSFETs are described by studying the effects of lateral electric field on short channel devices. Charge sharing models, which are used to analyze short channel MOSFETs are shown to be accurate only within a certain limits. In order to obtain an accurate expression for threshold voltage, a quasi two-dimensional Poisson's equation analysis is performed.

The assumptions of constant surface potential in charge sharing models are shown to be invalid by calculating the surface potential profile. The MOSFET

characteristics are found to be change drastically for short channel devices in comparison to those of the long channel devices. Influence of the drain voltage on the potential distribution becomes significant for short channel MOSFETs. The effects of drain voltage on the surface potential profile and threshold voltage are presented. The dependency of the threshold voltage on the device length, oxide thickness, channel doping are also shown.

The dependence of the threshold voltage of short channel MOSFETs on the channel length and drain to source voltage is predicted theoretically and is found to be in good agreement with published experimental data [21,22]. The results shows that successful scaling of MOS device feature size requires thinner oxide and higher levels of channel doping in order to minimized the short channel effects. The model is simple and helps give a better understanding of the physical mechanism involved in reducing the channel lengths.

5.2 Suggestions for future work

The mathematical model developed in this thesis describes the fully depleted MOSFET characteristics. By calculating the appropriate boundary conditions imposed by the inversion layer charges, it may be possible in future to develop similar model for partially depleted MOSFETs and silicon on Insulator (SOI) MOSFETs. Finding the effect of inversion layer charges on the potential

distribution may also result in the development of subthreshold current and subthreshold swing of short channel MOSFET.

APPENDIX A

A.1 Determination of Surface Potential

Equation 3.1 can be written as,

$$\frac{\varepsilon_{si} X_{dep}}{\eta \varepsilon_{ox}} T_{ox} \frac{dE}{dy} + (V_{GS} - V_{FB} - V_{sy}) = qN_{SUB} X_{dep} \frac{T_{ox}}{\varepsilon_{ox}} \qquad \text{A.1}$$

or,

$$l^2 \frac{dE}{dy} - V_{sy} = V_{FB} - V_{GS} + qN_{SUB} X_{dep} \frac{T_{ox}}{\varepsilon_{ox}}$$

$$= -\left[V_{GS} - (V_{FB} + qN_{SUB} X_{dep} \frac{T_{ox}}{\varepsilon_{ox}} + \phi_s + \phi_s \right]$$

$$= -\left[V_{GS} - V_{tho} + \phi_s \right]$$

$$= -V_{SL}$$

The parameters 'l' and V_{SL} is defined in Chapter 3.

The solution of the above equation can be written as,

$$V(y) = C_1 e^{\frac{y}{l}} + C_2 e^{-\frac{y}{L}} + V_{SL} \qquad \text{A.2}$$

Applying boundary conditions to Eqn. A.2,

At y =0 , $\quad V_{Bi} = C_1 + C_2 + V_{SL}$

At y =L , $\quad V_{Bi} + V_{DS} = C_1 e^{L/l} + C_2 e^{-L/l} + V_{SL}$ $\qquad$ A.3

We get, $C_1 = V_{Bi} - C_2$ & $C_2 = V_{Bi} - C_1$

From Eqn. A.3,

$$(V_{Bi} + V_{DS} - V_{SL}) = (V_{bi} - C_2) e^{L/l} + C_2 e^{-L/l}$$

$$= V_{bi} e^{L/l} - 2C_2 \frac{(e^{\frac{L}{l}} - e^{-\frac{L}{l}})}{2}$$

$$= V_{bi} e^{L/l} - 2C_2 \sinh(L/l)$$

We get $C_2 = \dfrac{V_{bi}(e^{\frac{L}{l}}-1)-V_{DS}+V_{SL}}{2\sinh(L/l)}$ and

$V_{bi} + V_{DS} = C_1 e^{L/l} + (V_{bi} - C_1) e^{-L/l}$

$$= \frac{2C_1(e^{\frac{L}{l}}-e^{-\frac{L}{l}})}{2}+V_{Bi}e^{-\frac{L}{l}}$$

$$= 2C_1\sinh(\frac{L}{l})+V_{Bi}e^{-\frac{L}{l}}$$

Then we get $C_2 = \dfrac{V_{bi}(1-e^{-\frac{L}{l}})+V_{DS}-V_{SL}}{2\sinh(\frac{L}{l})}$

Putting the values of C_1 and C_2 in Eqn. A.2 we get,

$$V = \frac{1}{2\sinh(\frac{L}{l})}\left[(V_{Bi}-V_{SL}(1-e^{-\frac{L}{l}})+V_{DS}e^{\frac{y}{l}}+\left[V_{Bi}(e^{\frac{L}{l}}-1)-V_{DS}\right]e^{-\frac{y}{l}}\right]+V_{SL} \qquad \text{A.4}$$

Rearranging equation A.4 we get the potentail distribution function in the following form which is given in Eqn. 3.2.

$$V_S(y) = V_{SL}+(V_{Bi}+V_{DS}-V_{SL})\frac{\sinh(y/l)}{\sinh(L/l)}+(V_{Bi}-V_{SL})\frac{\sinh[(L-y)/l]}{\sinh(L/l)} \qquad \text{A.5}$$

A2. Determination of Barrier peak y_o

Differentiating Eqn. 3.2 and applying Eqn. 3.4b we get,

$$\frac{dV_S}{dy} = \frac{(V_{BI}+V_{DS}-V_{SL})}{\sinh(L/l)}\cdot\frac{1}{l}\cosh(y/l) - \frac{(V_{BI}-V_{SL})}{\sin L/l}\cdot\frac{1}{l}\cos[\frac{L-y}{l}] = 0$$

or

$$(V_{BI}+V_{DS}-V_{SL})\cosh(y/l) = (V_{BI}-V_{SL})\cos[\frac{L-y}{l}]$$

$$(V_{BI}+V_{DS}-V_{SL})\frac{e^{\frac{y}{l}}+e^{-\frac{y}{l}}}{2} = (V_{BI}-V_{SL})\frac{e^{\frac{L-y}{l}}+e^{-(\frac{L-y}{l})}}{2}$$

$$e^{y/l}[(V_{bi}+Vds-V_{SL})-(V_{bi}-V_{SL})e^{-\frac{L}{l}}] = e^{-\frac{y}{l}}[-(V_{bi}+V_{ds}-V_{SL})+(V_{bi}-V_{SL})e^{\frac{L}{l}}$$

$$e^{2y/l} = \frac{(V_{bi}-V_{SL})e^{\frac{L}{l}}-(V_{bi}+V_{DS}-V_{SL})}{(V_{bi}+V_{DS}-V_{SL})-(V_{bi}-V_{SL})e^{-L/l}}$$

Therefore, the barrier peak is found to be y_o which is given by,

$$y_0 = \frac{l}{2}\log_e\left(\frac{(V_{bi}-V_{SL})e^{L/l}-(V_{bi}+V_{DS}-V_{SL})}{(V_{bi}+V_{DS}-V_{SL})-(V_{bi}-V_{SL})e^{-L/l}}\right)$$

For $L >> l$

$$e^{2y/l} = \frac{(V_{bi}-V_{SL})e^{L/l}}{(V_{bi}+V_{DS}-V_{SL})}$$

or $$e^{2/l(y-l/2)} = \frac{V_{bi}-V_{SL}}{V_{bi}+V_{DS}-V_{SL}}$$

$$e^{2(y-l/2)} = \log_e\left(\frac{V_{bi}-V_{SL}}{V_{bi}+V_{DS}-V_{SL}}\right)$$

$$y_0 = \frac{L}{2}-\frac{l}{2}\log_e\left(\frac{V_{bi}-V_{SL}+V_{DS}}{V_{bi}-V_{SL}}\right)$$

APPENDIX B

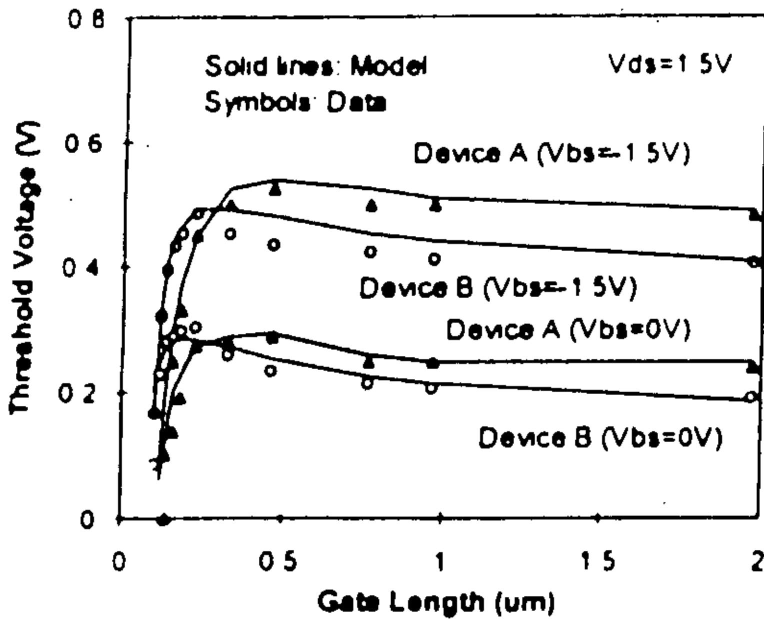

Fig. B.1 Measured characteristics of threshold Voltage vs channel length at V_{DS}=1.5. V and different body bias conditions, for the devices with different pocket process conditions (Ref. 21).

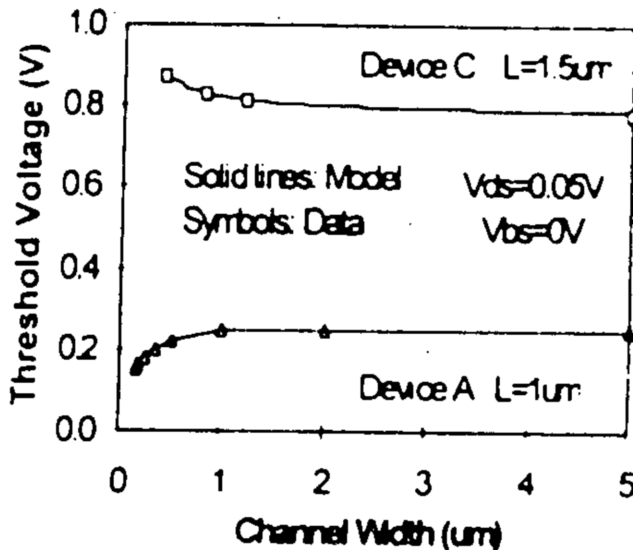

Fig. B.2 Experiment threshold voltage data of a conventianal 0.35μm technology. The V_{DS}=0.1 V, t_{OX}=7.8 nm and N_{SUB}=3.8E17 cm^{-3} (Ref. 22).

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