ANALYSIS AND DESIGN OF AN INVERTER

BY

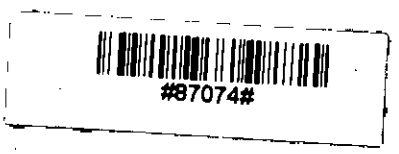
DILIP KUMAR PAUL

A PROJECT

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE

OF

MASTER IN ENGINEERING.



DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA.

DECEMBER,1993

ABSTRACT

A single phase inverter is designed and constructed to provide regulated output voltage at 220V. The output power stage is designed using two power transistors coupled to the load through a transformer. The output is a 50 Hz square wave which is obtained by push-pull operation of the two transistors using 50 Hz complementary trigger pulse stream. Feedback control is used for constant output voltage with load variation. A theoretical analysis of the inverter is presented.

The circuit is tested and it is found that the waveforms obtained at different stages of the circuit conform well with those obtained by computer simulation. The circuit is found to be efficient and economical for applications in appliances during power failures.

ACKNOWLEDGEMENTS

The author would like to acknowledge his heartiest gratitude and profound respect to his supervisor, Dr. Shahidul Islam Khan, Associate Professor of the Department of Electrical and Electronic Engineering, BUET for his valuable guidance, constant encouragement and whole hearted supervision throughout the progress of the work, without which this project would have never been materialised.

The author also expresses his sincere gratitude to Mr. Stephen Vardigans, Technical adviser and Mr. Zahurul Hoque, Assistant Professor, Electrical & Electronic Engineering Department, Technical Teachers' Training College, for their sincere help toward the progress of this work.

My indebtness to all my friends for the valuable discussions we shared.

The author thankfully acknowledges the valuable discussions made with Dr. Mohammad Ali Chowdhury, Associate Professor, Department of EEE, BUET.

Finally the author expresses his utmost gratitude to his mother without whose sacrifice the project work would not have been possible.

APPROVAL

Accepted as satisfactory in partial fulfilment of the requirements for the degree of Master in Engineering (Electrical and Electronic).

BOARD OF EXAMINERS

1. _____ 30.12.93 — Chairman (Supervisor)
(Dr. Shahidul Islam Khan)
Associate Professor,
Department of Electrical & Electronic Engineering, BUET, Dhaka.

2. _____ 30/12/93 — Member
(Dr. Saiful Islam)
Professor,
Department of Electrical & Electronic Engineering, BUET, Dhaka.

3. _____ — Member
(Dr. Mohammad Ali Chowdhury)
Associate Professor,
Department of Electrical & Electronic Engineering, BUET, Dhaka.

CERTIFICATE

Certified that this work was done by me and it has not been submitted elsewhere for the award of any degree or diploma.

Countersigned

20.12.93

(Dr. Shahidul Islam Khan)
Supervisor.

Signature of the student

20.12.93.

(Dilip Kumar Paul)

DEDICATED TO MY WIFE

AND

TO MY ONLY CHILD SHRAYA

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

w_i	=	Frequency of the input voltage
w_s	=	Switching frequency
w_o	=	Frequency of the output voltage
M	=	Modulation index
A_r	=	Reference signal amplititude
A_c	=	Carrier signal ampltitude
δ	=	Pulse width
p	=	No. of pulses per half cycle
f_c	=	Carrier frequency
f_o	=	Output frequency
q	=	No. of pulses in the 60° period
a_n, b_n	=	Fourier co-efficient
h_{fe}	=	Transistor current gain

CHAPTER -1

INTRODUCTION

1.1 Introduction

Utilities supply ac voltage at fixed voltage and frequency. However, there are many applications, where variable voltage and frequency are required. Inverter is an equipment which converts input dc voltage to variable frequency and variable amplitude ac voltage. One of the important application of inverters is variable speed ac drives, where input ac is made variable (frequency and amplitude) by rectifier - inverter configuration.

The output voltage waveforms of ideal inverters should be sinusoidal . However, the waveforms of practical inverters are nonsinusoidal and contain certain harmonics. For low and medium power applications[1], square wave or quasi square wave voltage may be acceptable; and for high power applications, low distorted sinusoidal waveforms are required.

In most inverter applications, it is necessary to be able to control both the output voltage and the output frequency. The controllable voltage requirement may arise out of the need to overcome regulation in the connected a.c. equipment or to maintain constant flux in a.c. motors driven at variable speed by variation of their supply frequency. If the d.c. input voltage is controllable, then an inverter with a fixed ratio of d.c. input voltage may be satisfactory. If the d.c. input voltage is not controllable, then control of output voltage must be obtained by employing pulse-width modulation.

Some applications [2] of inverters are:

1. Stand-by power supplies
2. Induction heating
3. Variable speed a.c. motor drives
4. Uninterruptible power supplies for computers
5. Aircraft power supplies
6. Output of d.c. transmission lines.

The input to an inverter may be a battery, fuel cell,solar cell or other d.c. source.

1.2 Different types of Inverter

Inverters can be classified into the following types:

(i) Single phase inverter

(ii) Three phase inverter

Each type can again be subdivided[1] into four main categories depending on the type of thyristor commutation used. They are :

i. Pulse width modulation (PWM) inverter

ii. Resonant inverter

iii. Auxiliary commutated inverter

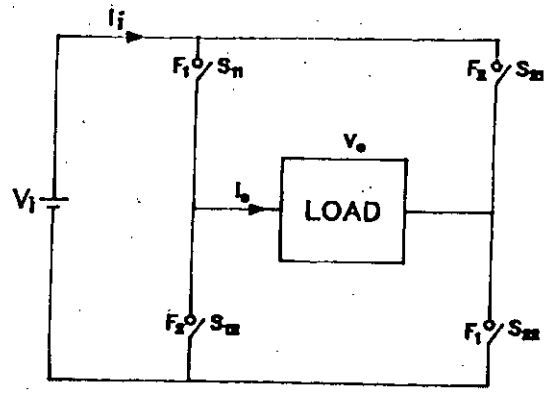
iv. Complementary commutated inverter.

An inverter is called a Voltage Fed Inverter (VFI) if the input voltage remains constant, a Current Feed Inverter (CFI) if the input current is maintained constant and a variable d.c. link inverter if the input voltage is controllable.

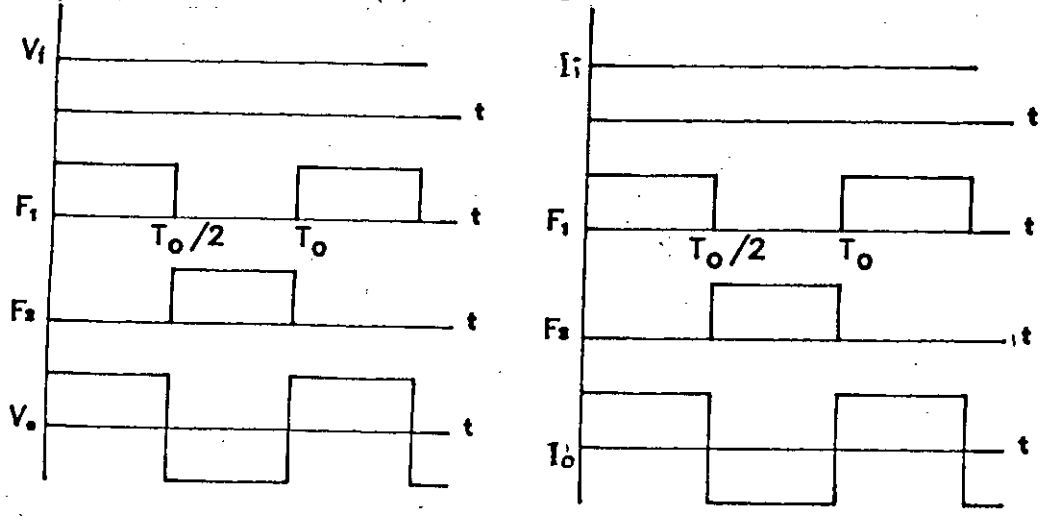
1.3 The Proposed Method

A single pulse square wave is used as switching function to operate the proposed single phase inverter. Transistors were used as switches. The triggering of these switching devices are controlled from a two complement square waves and by a feed back loop from output to the input. This produces closed loop control which maintains constant output voltage under varying load conditions.

The current capacity of the main inverter is improved by using transistor both common emitter and emitter follower mode[3]. A simplified block diagram of the proposed single phase inverter is shown in Fig. 1.1.



(a) Block diagram



(a) Output voltage (b) Input current

Figure 1.1 Block diagram of an inverter, and its input and output waveforms

1.4 Scope of the Project

At full load, it is difficult to keep the output voltage constant. The scope and objective of this project is to maintain the constant output voltage at different loads. To keep the output voltage constant, a feedback loop is used to control the drive level to the main switching transistors.

1.5 Introduction to the Chapters

The contents of this project have been organised as follows:

In Chapter 2, the principle of operation of single phase inverter is discussed. Mathematical derivation of output voltage and input current are analysed and are verified by computer analysis.

The output voltage of a single phase inverter can be controlled by different methods. These methods are discussed with mathematical analysis in Chapter-3 and are verified by computer analysis by using FORTRAN 77 and a software package GRAPHER.

Details design procedure, construction and testing are discussed in Chapter-4.

Chapter-5 presents conclusions on the prototype single phase inverter which was constructed according to the design presented Chapter-4 and makes commonent on its performance and future improvements.

CHAPTER 2

PRINCIPLE OF OPERATION AND COMPUTER SIMULATION

2.1 Introduction

In this chapter the principle of operation of a single phase inverter is discussed. Both half and full bridge inverter with mathematical analysis are discussed. Fourier series is used for mathematical analysis. The input current of the single phase inverter is also analysed.

A computer program is developed to analyze the output voltage and input current. Voltage and current waveshapes are plotted by using the data from the computer program. These computer simulated results are verified by laboratory prototype inverter in Chapter-4.

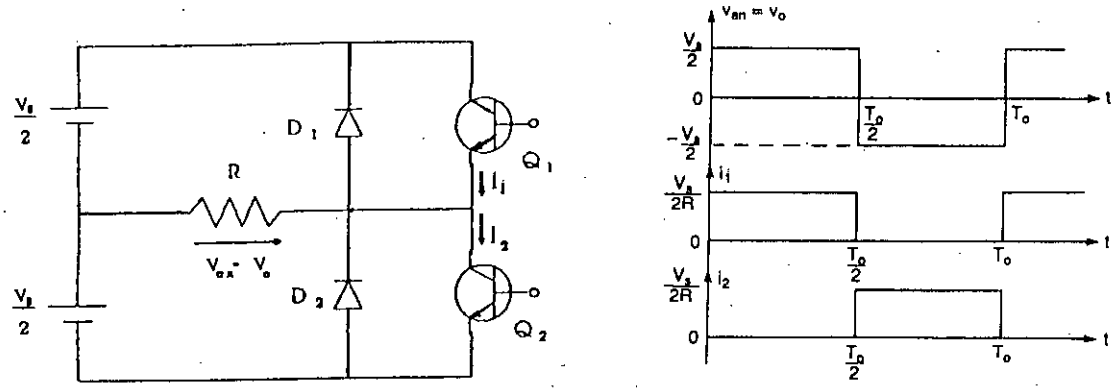
2.2 Principle of Operation

The operation of single phase half bridge and full bridge inverters are discussed in the following sub-sections:

2.2.1. Operation of a Single Phase Half Bridge Inverter

The principle of a single-phase half bridge inverter can be explained with the help of Fig. 2.1. The inverter circuit consists of two switches(transistors). When transistor Q_1 is turned on for a time $T_0/2$, the instantaneous voltage across the load V_0 is $V_s/2$. If transistor Q_2 is turned on for a time $T_0/2$, $-V_s/2$ appears across the load.

The logic circuit should be designed in such a way that Q_1 and Q_2 are not turned on at the same time. Figure 2.1(b) shows the waveforms for the output voltage and current with a resistive load. The inverter requires a three wire d.c. source, and when a transistor is off, its reverse voltage is V_s instead of $V_s/2$. This inverter is known as a half bridge inverter.



(a) Circuit (b) Waveforms

Figure 2.1 A single-phase half-bridge inverter.

The rms output voltage can be found from

$$V_0 = \left(\frac{2}{T_0}\int_0^{\frac{T_0}{2}} V_s^2 . dt\right)^{\frac{1}{2}} = \frac{V_s}{2} \tag{2.1}$$

The instantaneous output voltage can be expressed in Fourier series as

$$V_0 = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi} Sin(n\omega t) \tag{2.2}$$

and

$$V_o = 0 \quad for \quad n = 2,4,\ldots\ldots$$

where $\omega = 2\pi f_o$ is the frequency of output voltage in rad/second. For n = 1, the above equation gives the rms value of fundamental components as

$$V_1 = \frac{2V_s}{\sqrt{2}\pi} = 0.45V_s \tag{2.3}$$

2.2.2. Operation of a Single-Phase Full Bridge Inverter

A generalized model for derivation of individual converter is shown in Fig.2.2.

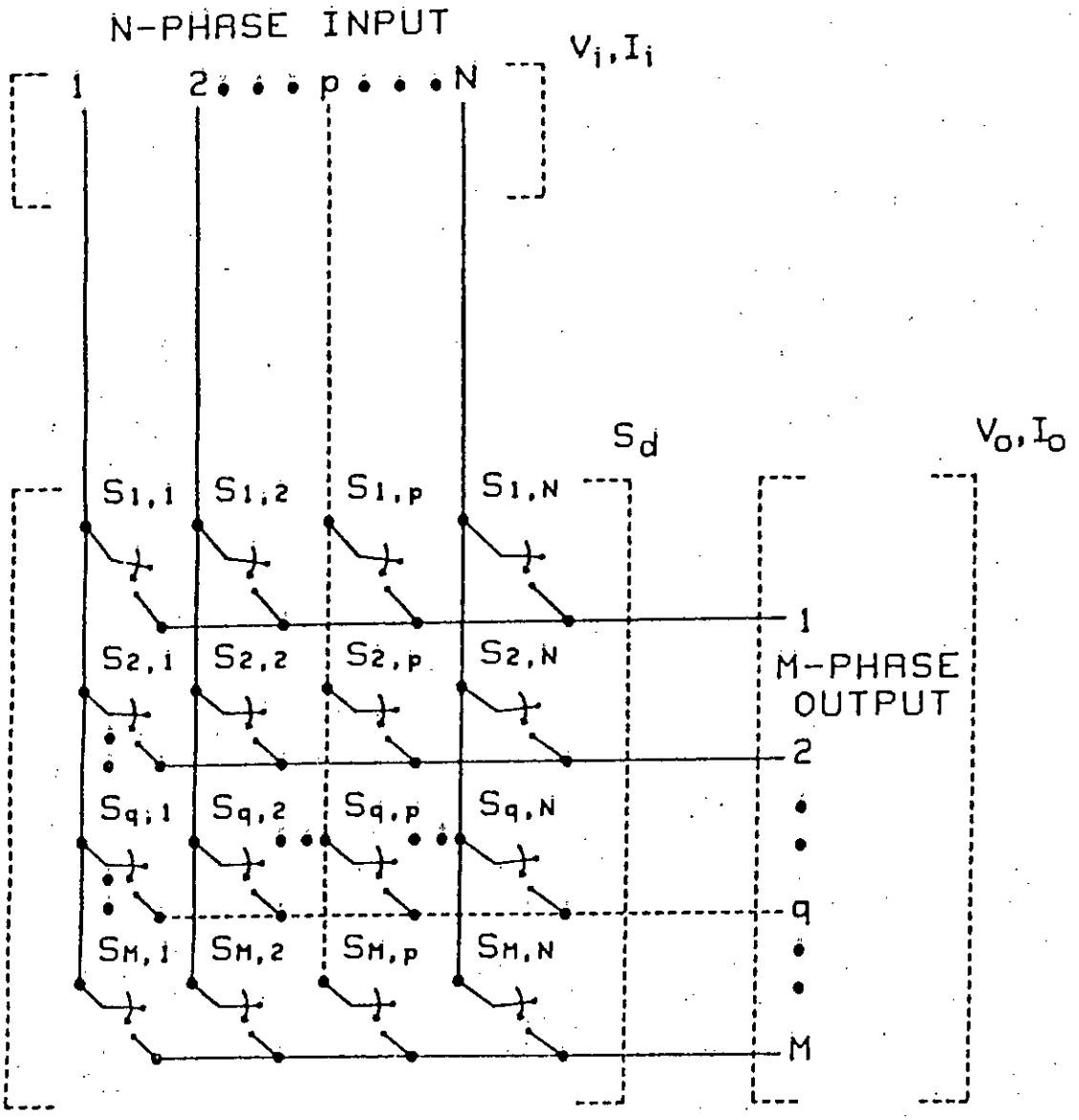


Figure 2.2 A generalized circuit model

The operation of this generalized model[5] can be explained as the switching model comprises of an "input matrix" of [Nx1] dimension, "converter switching matrix" of [MxN] dimension and an "output matrix" of [Mx1] dimension. The principle state that "the multiplication of a set of [Nx1] sinusoidal quantities (e.g., input voltage matrix) by a compatible set of [MxN] balanced sinusoidal quantities (e.g., converter transfer matrix) yields a third set of [Mx1] sinusoidal quantities (e.g.,output voltage matrix) that are also balanced". This model can be used readily to realise a practical converter circuit once the nature of the input/output quantity and phases (N,M) have been specified. Therefore, the analytical statement for this model, regarding converter output voltages[$V_o(w_ot)$] and input current [$I_i(w_it)$] are shown in Eqns. (2.4) and (2.5), where,

w_i is the input frequency,

w_s is the switching frequency and

$w_o = w_s - w_i$ is the output frequency,

$[V_o(w_ot)] = [F_d(w_st)][V_i(w_it]$

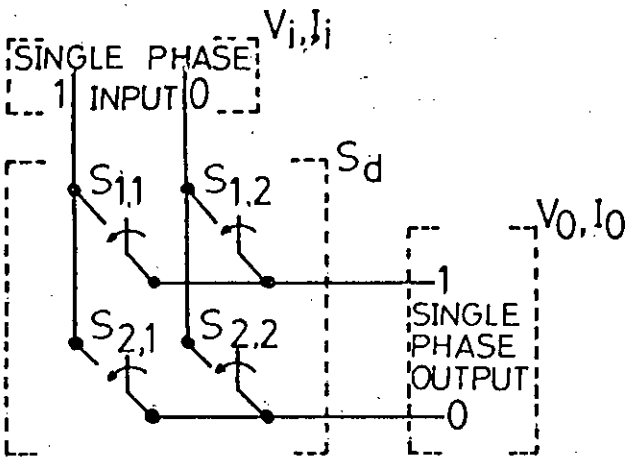
$$\begin{bmatrix} V_{o,1} \\ \vdots \\ V_{o,M} \end{bmatrix} = A \begin{bmatrix} f_{1,1} & \dots & f_{1,K} & \dots & f_{1,N} \\ f_{1,1} & \dots & f_{1,K} & \dots & f_{1,N} \\ f_{M,1} & \dots & f_{M,K} & \dots & f_{M,N} \end{bmatrix} .B \begin{bmatrix} V_{i,1} \\ \vdots \\ V_{i,K} \\ \vdots \\ V_{i,N} \end{bmatrix} \qquad (2.4)$$

and

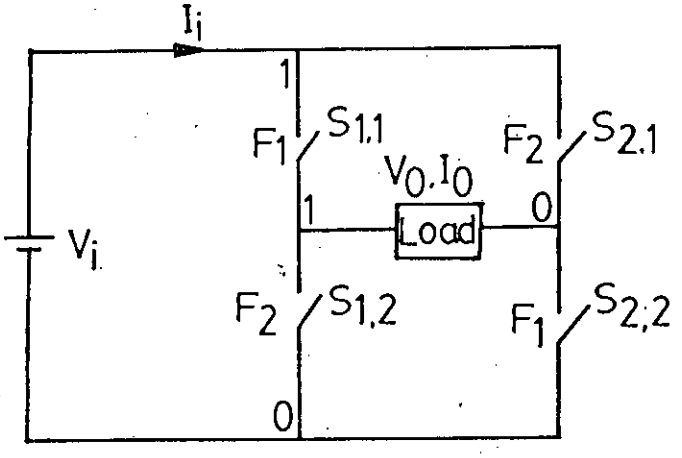
$$[I_i(w_it)] = [F_d(w_st)]^T [I_o(w_o)t]$$

$$\begin{bmatrix} I_{i,1} \\ \vdots \\ I_{i,K} \\ \vdots \\ I_{i,N} \end{bmatrix} = A \begin{bmatrix} f_{1,1} & \dots & f_{1,1} & \dots & f_{M,1} \\ f_{1,K} & \dots & f_{1,K} & \dots & f_{M,K} \\ f_{1,N} & \dots & f_{1,N} & \dots & f_{M,N} \end{bmatrix} .B \begin{bmatrix} I_{o,1} \\ \vdots \\ I_{o,1} \\ \vdots \\ I_{o,M} \end{bmatrix} \qquad (2.5)$$

The derivation of single phase inverter from this model is shown in Fig. 2.3(a) by setting N=1 and M=1. The simplified circuit is depicted in Fig.2.3(b) .F_1 and F_2 are the switching functions corresponding to the switches S_{11}, S_{22} and S_{12}, S_{21} respectively.



a. Switching diagram derived from Figure 2.2 for N=1, M=1



(b) Corresponding simplified circuit diagram

Figure 2.3 Realization of single phase inverter from generalized model

The equations for output a.c. voltage $V_o(w_o t)$ and input d.c. current I_i are derived from generalized Eqn.(2.4) and (2.5) as follows:

$$\begin{aligned}[V_o(w_o t)] &= [F_d(w_s t)].[V_i(w_i t)] \\ &= A[\cos(w_s t)].V_i[\cos(w_i t)] \\ &= AV_i \cos(w_o t) \\ &\quad [\text{as } w_i = 0 \text{ and } w_s = w_o]\end{aligned} \tag{2.6}$$

and the corresponding input current I_i equation is

$$\begin{aligned}[I_i(w_i t)] &= [F_d(w_s t)]^T [I_o(w_o t)] \\ &= A[\cos(w_s t)].I_o[\cos(w_o t)] \\ &= A[\cos(w_o t)].I_o[\cos(w_o t)] \quad [\text{as } w_s = w_o]\end{aligned}$$

$$= \frac{AI_o}{2} + \frac{AI_o}{2}\cos 2\omega_o t \tag{2.7}$$

The output a.c. voltage $V_o(w_o t)$ waveform and input d.c. current I_i waveform are shown in Fig.2.4 and 2.5 respectively. Corresponding spectra of voltage and current are depicted in Figs. 2.4(e) and 2.5(e).

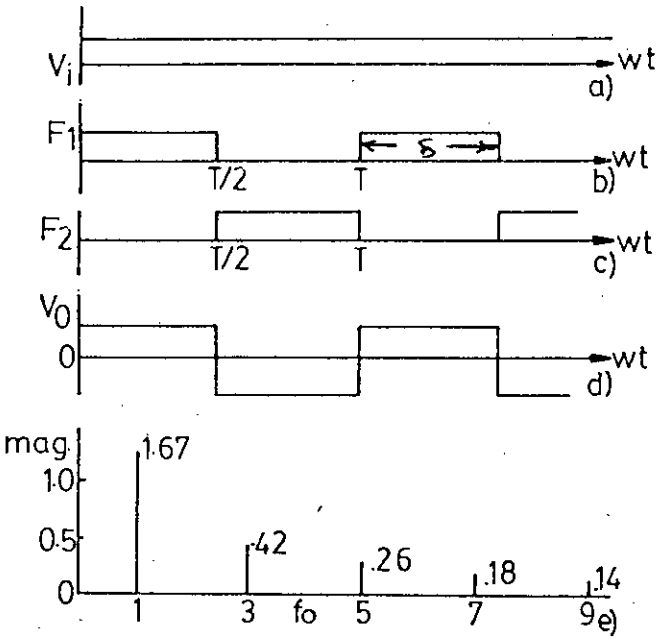


Figure 2.4 Output voltage waveforms(a-d) of inverter and its spectrum(e)

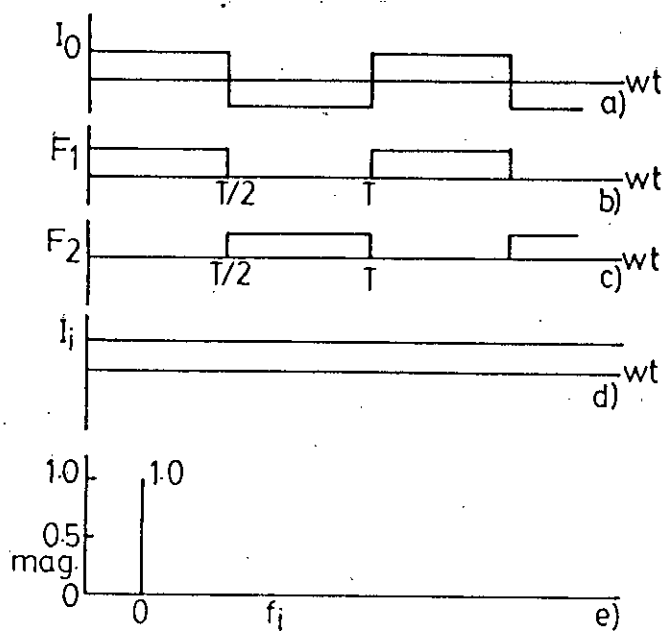
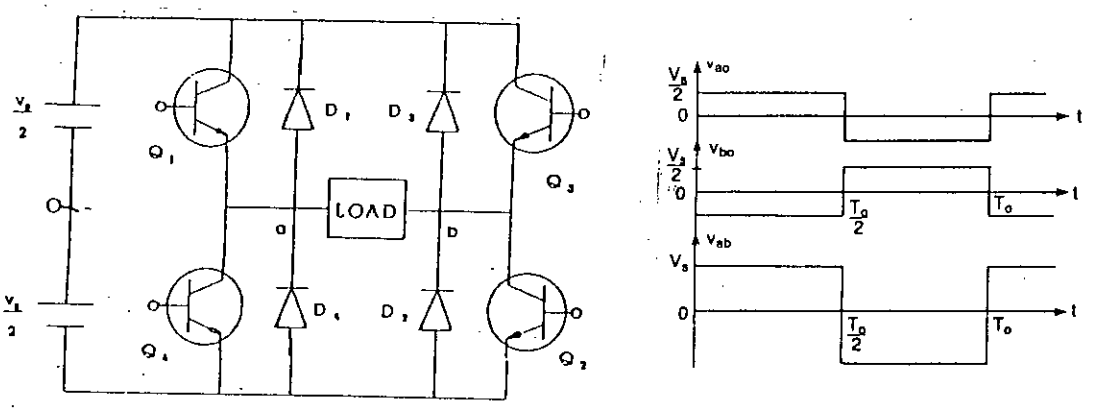


Figure 2.5 Input current waveforms (a-d) of inverter and its spectrum(e)

The principle of a single-phase full bridge inverter can be explained with the help of Fig. 2.6. The inverter consists of four transistors. When transistors Q_1 and Q_2 are turned on simultaneously, for a time period $T_0/2$, the input voltage V_s appears across the load. If transistors Q_3 and Q_4 are turned on at the same time for a another time $T_0/2$, the voltage across the load is reversed and is $-V_s$. The waveform for the output voltage is shown in Fig. 2.6(b).



a. Circuit b. Waveforms

Figure 2.6 A single phase full-bridge inverter using NPN transistors. The driving pulse feed circuit are not shown for simplicity.

When diodes D_1 and D_2 conduct, the energy is fed back to the dc source and they are known as feedback diodes.

2.3 Fourier Analysis of Inverter's Output Voltage and Input Current

Practical inverter switches operate in the ON/OFF mode yielding pulsed switching pattern rather than continuous mode. For this reason the output voltage and input current equations shown in Eqn. (2.4) and (2.5) need to be modified. The voltage equation then may be written as:

$$[V_o(\omega_o t) = \sum_{n=1,3,5,..}^{\infty} A_n \cos\omega_s t \ . \ V_i \cos\omega_i t$$

$$= V_i A_1 \cos\omega_o t + V_i \sum_{n=3,5,..}^{\infty} A_n \cos\omega_o t$$

(when $\omega_s = \omega_o$, $\omega_i = 0$ and $V_1 = 0$)

$$V_o(\omega_o t) = A_1 \cos\omega_o t + A_n \sum_{n=3,5,..}^{\infty} \cos\omega_o t \qquad (2.8)$$

The input current equation may be written as

$$[I_i(\omega_i t)] = [I_o \cos(\omega_o t)] \ . \ [\sum_{n=1,3,5,..}^{\infty} A_n \cos\omega_s t]$$

$$= \frac{A_1}{2} + \frac{A_1}{2}\cos 2\omega_o t + \sum_{n=3,5,..}^{\infty} \frac{A_n}{2}\cos(\omega_o \pm \omega_s) t \qquad (2.9)$$

(when $I_o = 1$)

where $A_n = (4/n\pi) \sin(n\delta/2)$, δ is the width (Fig. 2.4) of the pulse.

The output voltage and input current equations for this inverter are simulated by a computer program named INVERTER. This program is shown in Appendix-1. The Fourier coefficients of voltage and current are shown in Table-2.1. Using theses coefficients the output voltage and input current are reconstructed and depicted in Figs 2.7(a) and 2.7(b). The reconstructed waveforms conform with the actual waveforms(Fig.2.4 and 2.5).

Table 2.1	
Frequency spectra of waveforms associated with inverter output voltage	
Harmonic coefficients when δ=180°, M=1	
Order (n)	Amplitude (B_n)
1	1.27
3	0.42
5	0.25
7	0.18
9	0.14
11	0.11
13	0.09
15	0.08
17	0.07
19	0.06
21	0.06
23	0.05

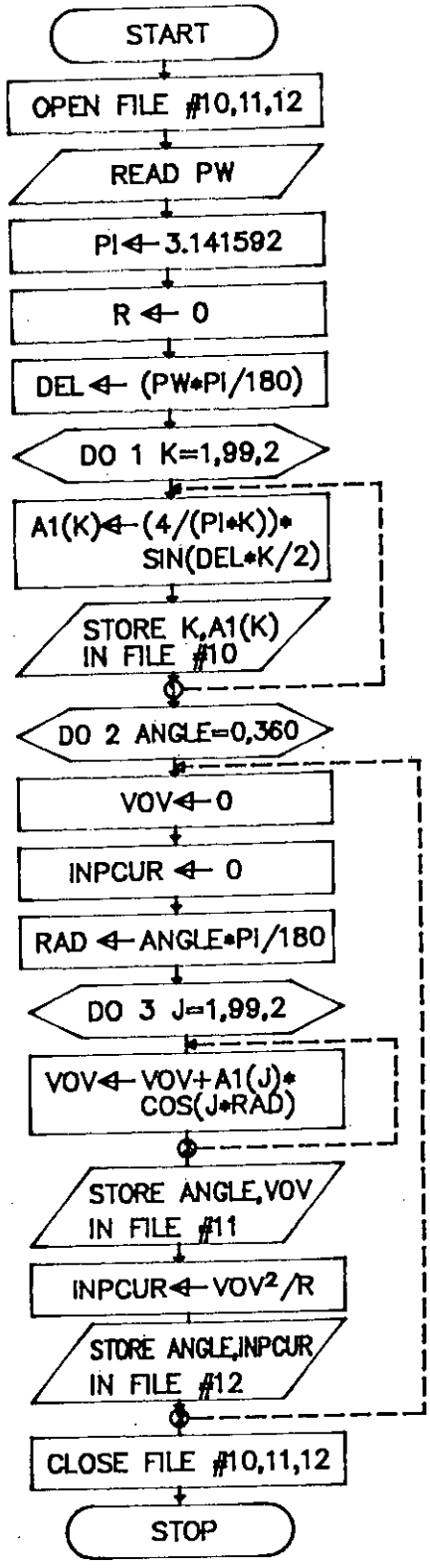
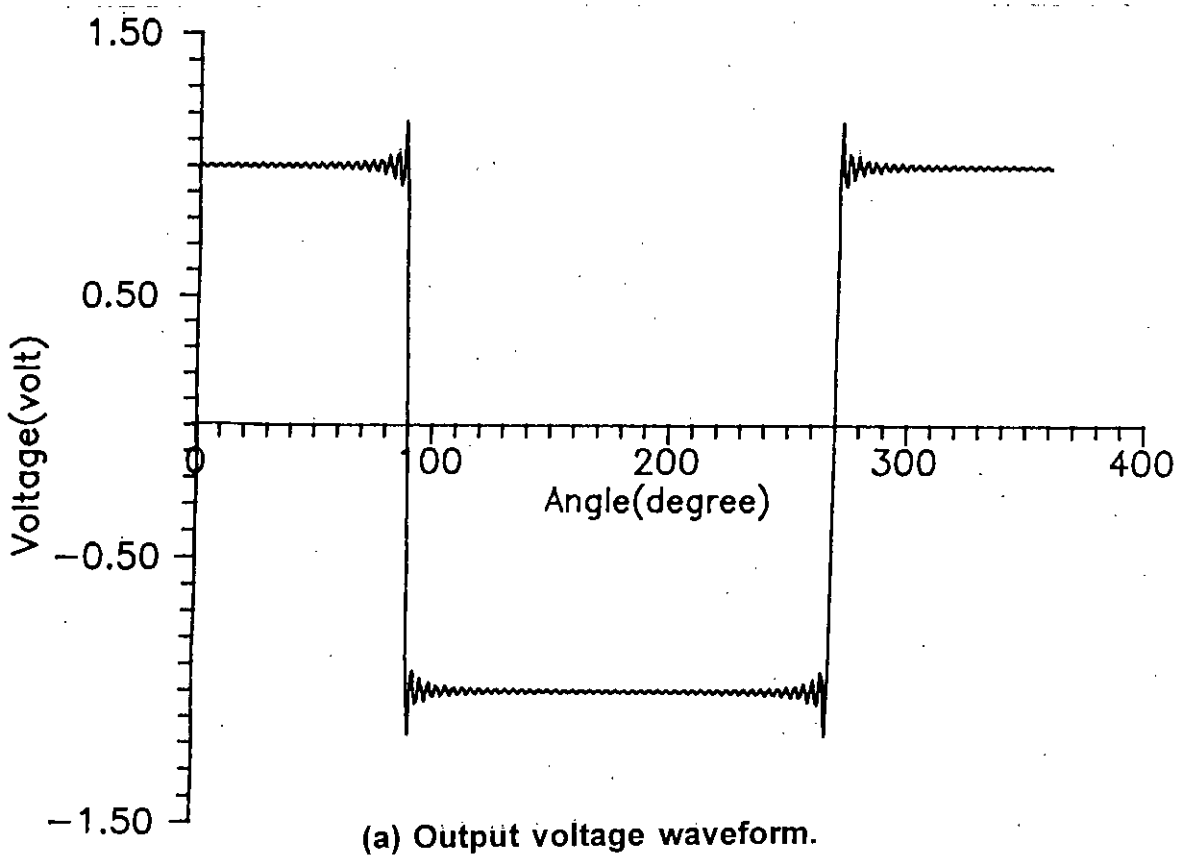
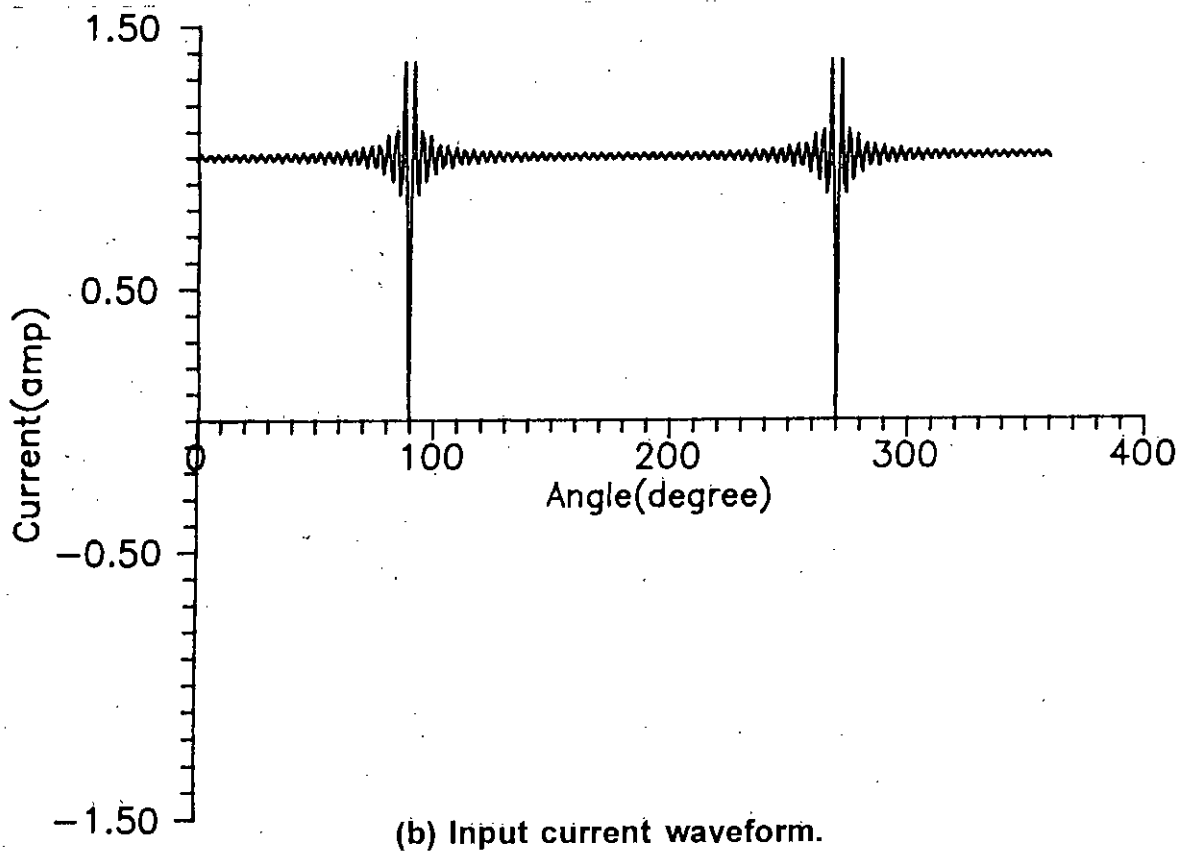


Fig.2.7 Flow chart of 'INVERTER' program



(a) Output voltage waveform.



(b) Input current waveform.

Figure 2.8 Output voltage and intput current waveshapes of a single phase inverter, where pulse width δ=180°

2.5 Summary

The principle of operation of a single phase inverter and computer analysis of output voltage and input current are discussed in this chapter. The output voltage will contain only fundamental frequency if all higher harmonics are filtered out.

The theoretical analysis is verified by the computer analysis.The computer simulated results are similar to the actual input, output waveforms.

CHAPTER-3

VOLTAGE CONTROL AND COMPUTER ANALYSIS OF SINGLE PHASE INVERTER

3.1 Introduction

The objective of this chapter is to analyse the inverter using different switching functions. The proposed single phase inverter is analysed for output voltage and input current. A single pulse modulation is used as switching functions for the analysis and implementation of the inverter.

In many industrial applications, it is often required to control the output voltage of inverters. Typical examples of such a requirements are: (1) an inverter system employing a battery as a d.c. source and required to deliver constant a.c. voltage to the load circuit must be able to eliminate the effect of battery voltage variation, (2) for voltage regulation of inverters, and (3) an inverter system driving an a.c. motor must be able to maintain an approximately constant ratio of output voltage to output frequency to avoid saturation of the iron in the motor.

3.2 Modulation Techniques

There are various techniques to vary the inverter gain. The most efficient method of controlling the gain (and output voltage) is to incorporate pulse width modulation (PWM) control within the inverter. The commonly used techniques are:

(i) Single-pulse-width modulation
(ii) Multiple-pulse-width modulation
(iii) Sinusoidal pulse-width modulation
(iv) Modified sinusoidal pulse-width modulation
(v) Phase displacement control.

3.2.1 Single-Pulse-Width Modulation

In single-pulse-width modulation control, there is only one pulse per half-cycle and the width of the pulse is varied to control the inverter output voltage. Figure 3.1 shows the generation of gating signals and output voltage of single phase full bridge inverters. The gating signals are generated by comparing a rectangular reference signal of amplitude, A_r with a triangular carrier wave of amplitude, A_c. The frequency of the carrier wave determines the fundamental frequency of output voltage. By varying A_r from 0 to A_c, the pulse width, δ, can be varied from 0 to 180°. The ratio of A_r to A_c is the control variable and defined as the *modulation index* (*M*).

The modulation index,

$$M = \frac{A_r}{A_c} \tag{3.1}$$

The rms output voltage can be found from

$$V_0 = \left[\frac{2}{2\pi}\int_{(\pi-\delta)/2}^{(\pi+\delta)/2} V_s^2 \; d(\omega t)\right]^{\frac{1}{2}}$$

$$= V_s\sqrt{\frac{\delta}{\pi}} \tag{3.2}$$

The fourier series of the output voltage of Fig. 3.1 may be described as,

$$v_0(t) = \sum_{n=1,3,5,..}^{\infty} a_n \sin(n\omega t) + \sum_{n=1,,3,5,..}^{\infty} b_n \cos(n\omega t) \quad volts \tag{3.3}$$

where,

$$a_n = \frac{2}{\pi}\int_0^{\pi} V_s \; Sin(n\omega t)\, d(\omega t)$$

$$= \frac{2V_s}{\pi}\int_{(\pi-\delta)/2}^{(\pi+\delta)/2} \sin(n\omega t)\, d(\omega t)$$

$$= \frac{4v_s}{n\pi}\sin\left(\frac{n\delta}{2}\right) \tag{3.4}$$

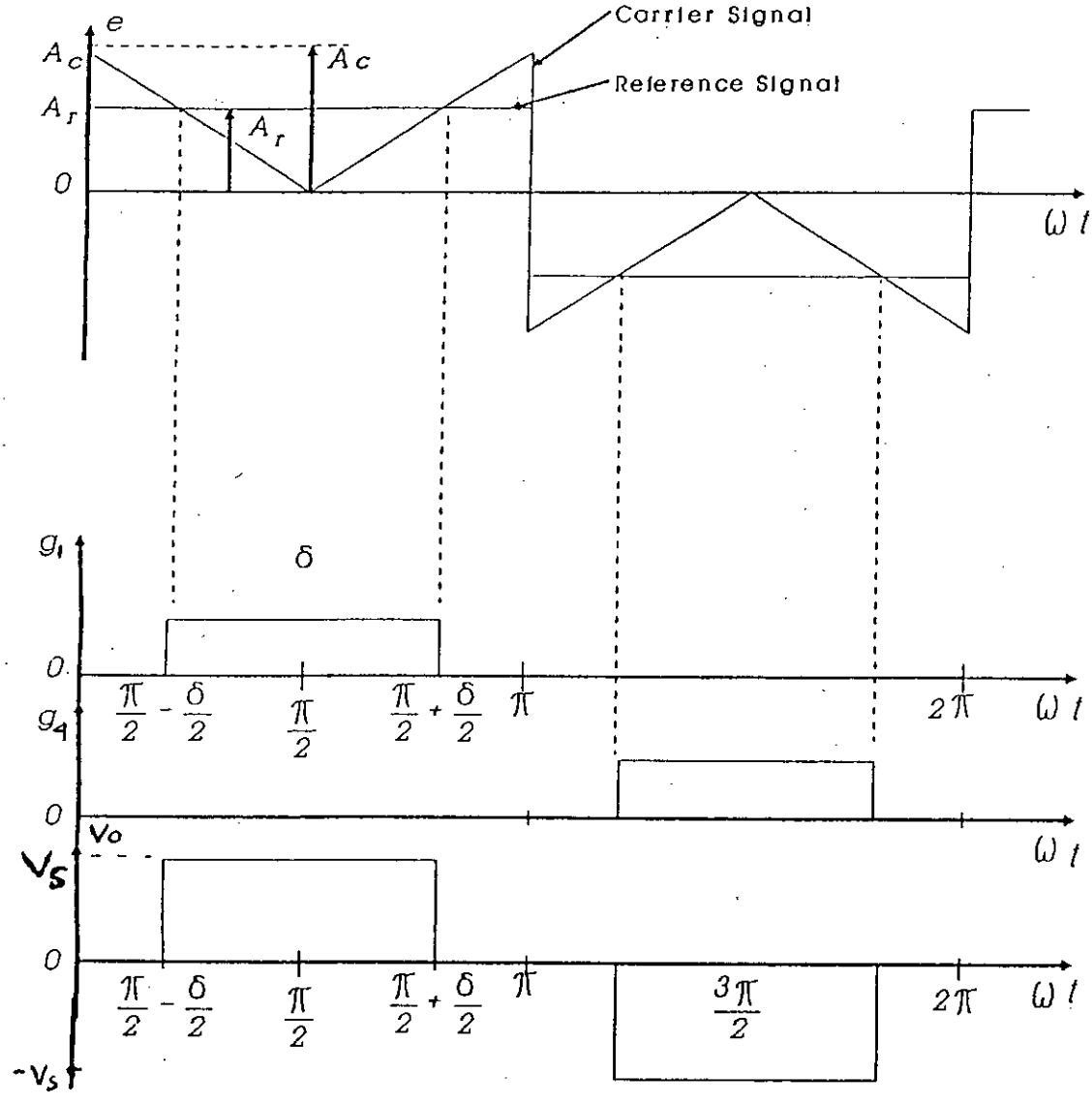


Figure 3.1 Single pulse-width modulation

and,

$$b_n = \frac{2}{\pi}\int_0^{\pi} V_s \cos(n\omega t)\, d(\omega t)$$

$$= 2\frac{V_s}{\pi}\int_{(\pi-\delta)/2}^{(\pi+\delta)/2} \cos(n\omega t)\, d(\omega t) = 0$$

Thus Eqn.(3.1) becomes,

$$v_0(t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi} Sin\left(\frac{n\delta}{2}\right) Sin(n\omega t) \quad volts \tag{3.5}$$

In Fig. 3.2, curves of the ratio a_n/a_{1max} versus δ are shown for n = 1,3,5, and 7, where a_{1max} is the amplitude of the fundamental component of the rectangular waveform obtained when $\delta = \pi$. From these curves it may be seen that, as δ is decreased, the harmonic content of the output voltage wavefrom increases until, when the amplitude of the fundamental component has been reduced to 20% of its maximum value, the amplitudes of the three harmonics illustrated are very nearly equal to that of the fundamental.

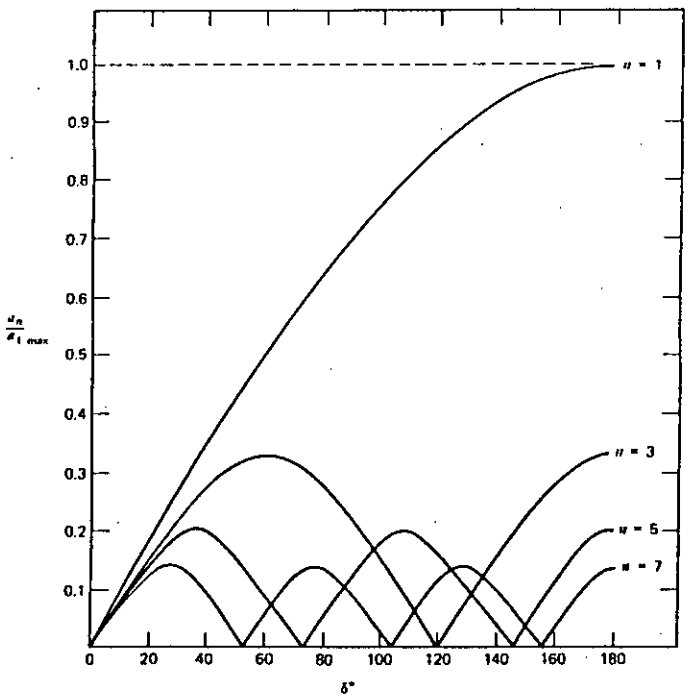


Fig. 3.2 Harmonic content [2] of waveform in Fig. 3.1

Equation (3.2) is simulated in computer program named "INVERTER" (Appendix-1).

3.2.2 Multiple Pulse-Width Modulation

The harmonic content at lower output voltage can be significantly reduced by using several pulses in each half cycle. The generation of gating signals for turning on and off of switches is shown in Fig.3.3 by comparing a reference signal with a triangular carrier wave. The frequency of reference signal sets the output frequency, f_o, and the carrier frequency, f_c, determines the number of pulses per half cycle, p. The modulation index controls the output voltage. This type of modulation is also known as *uniform pulse width modulation* **(UPWM)**.

The number of pulses per half cycle is

$$N=\frac{f_c}{2f_0}=integer \tag{3.6}$$

The variation of modulation index M from 0 to 1 varies the pulse width from 0 to π/p and the output voltage from 0 to V_s. The output voltage for single phase bridge inverter is shown in Fig. 3.3(b).

If δ is the width of each pulse, the rms output voltage can be found form

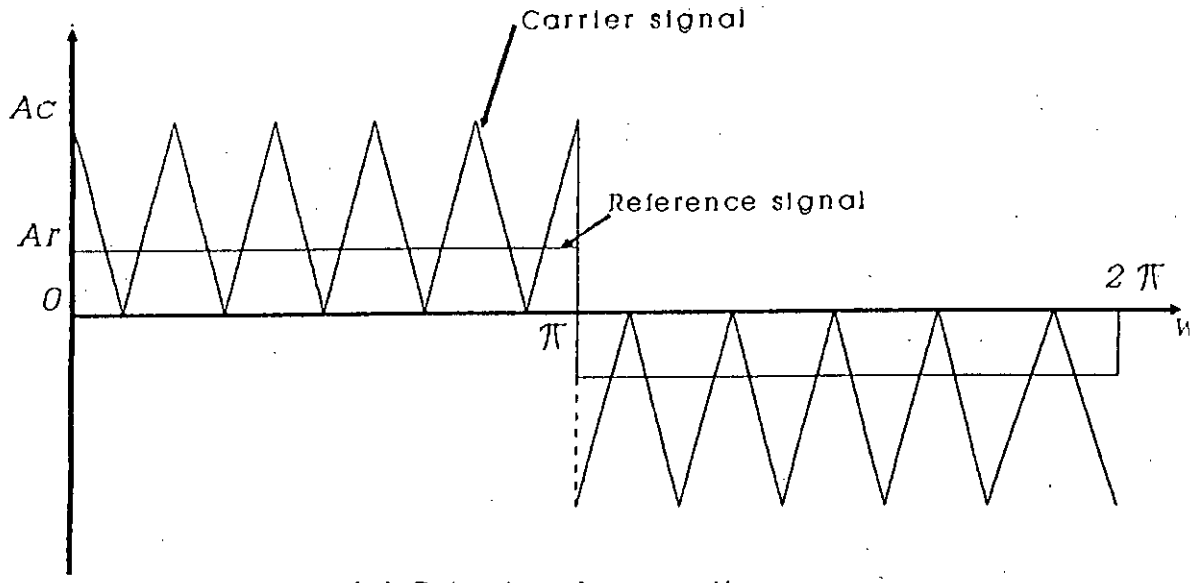
$$V_0=\left[\frac{2p}{2\pi}\int_{(\pi/p-\delta)/2}^{(\pi/p+\delta)/2} V_s^2\, d(\omega t)\right]^{\frac{1}{2}}$$

$$=V_s\sqrt{\frac{p\delta}{\pi}} \tag{3.7}$$

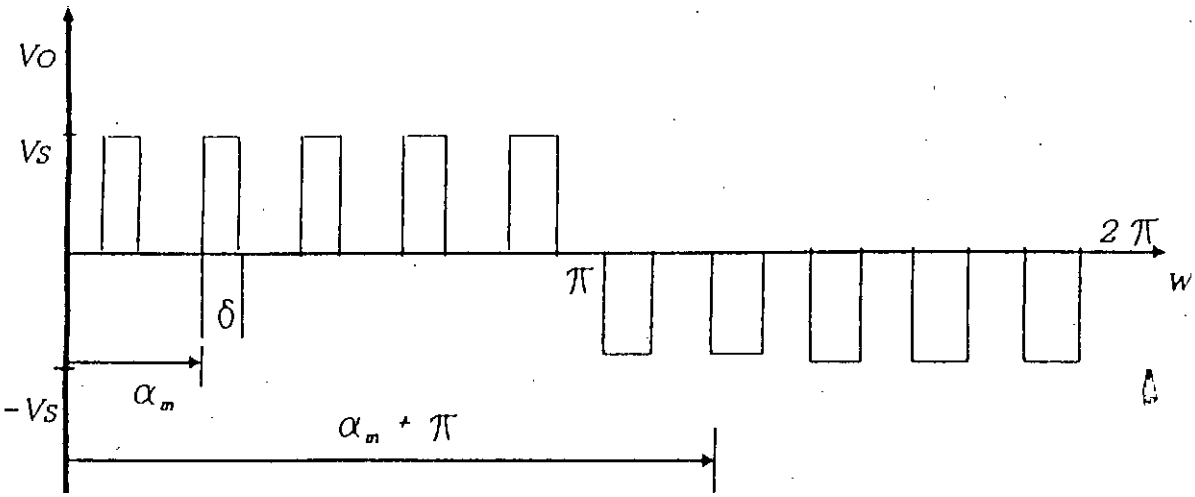
The general form of a Fourier series for the instantaneous output voltage is

$$v_0(t)=\sum_{n=1,3,5,..}^{\infty}(A_n\cos(n\omega t)+B_n\sin(n\omega t)\quad volts \tag{3.8}$$

The coefficients A_n and B_n in Eqn. (3.8) can be determined by considering a pair of pulses such that the positive pulse of duration δ starts at $\omega t = \alpha$ and the negative one of the same width starts at $\omega t = (\pi + \alpha)$. This is shown in Fig. 3.3(b). The effect of all pulses can be combined together to obtain the effective output voltage.



(a) Gate signal generation



(b) Output voltage

Figure 3.3 Multiple pulse-width modulation

If the positive pulse of *mth* pair starts at $\omega t = \alpha_m$ and ends at $\omega t = (\alpha_m + \pi)$, the Fourier coefficient for a pair of pulses are

$$a_n = \frac{2V_s}{\pi} \int_{\alpha_m}^{(\alpha_m+\delta)} \cos(n\omega t)\, d(\omega t)$$

$$= \frac{2V_s}{n\pi} [\sin n(\alpha_m + \delta) - \sin n\alpha_m]$$

$$= \frac{4V_s}{n\pi} \sin \frac{n\delta}{2} \cos n(\alpha_m + \frac{\delta}{2}) \qquad (3.9)$$

and,

$$b_n = \frac{2V_s}{\pi} \int_{\alpha_m}^{(\alpha_m+\delta)} \sin(n\omega t)\, d(\omega t)$$

$$= \frac{2V_s}{n\pi} [\cos n\alpha_m - \cos n(\alpha_m+\delta)]$$

$$= \frac{4V_s}{n\pi} \sin \frac{n\delta}{2} \sin n(\alpha_m + \frac{\delta}{2}) \qquad (3.10)$$

The coefficients of Eqn. (3.8) can be found by adding the effects of all pulses,

$$A_n = \sum_{m=1}^{p} \frac{4V_s}{n\pi} \sin \frac{n\delta}{2} \cos n(\alpha_m + \frac{\delta}{2}) \qquad (3.11)$$

and,

$$B_n = \sum_{m=1}^{p} \frac{4V_s}{n\pi} \sin \frac{n\delta}{2} \sin n(\alpha_m + \frac{\delta}{2}) \qquad (3.12)$$

So, the output voltage of Eqn. (3.8) becomes by using Eqns. (3.11) and (3.12)

$$v_0(t) = \sum_{n=1,3,5,..}^{\infty} \sum_{m=1}^{p} \frac{4V_s}{n\pi} \sin \frac{n\delta}{2} \cos n(\alpha_m + \frac{\delta}{2}) \cos(n\omega t) + \sum_{n=1,3,5,..}^{\infty} \sum_{m=1}^{p} \frac{4V_s}{n\pi} \sin \frac{n\delta}{2} \sin n(\alpha_m + \frac{\delta}{2}) \sin(n\omega t) \quad volts \qquad (3.13)$$

Simulation of UPWM waveforms are done in PROGRAM-2 (Appendix-1)

3.2.3 Sinusoidal Pulse-Width Modulation (SPWM)

Instead of maintaining the width of pulses the same as in the case of multiple pulse modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the center of the same pulse. The distortion factor and lower order harmonics are reduced significantly. The gating signals as shown in Fig. 3.4(a) are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency,f_c. This type of modulation is commonly used in industrial applications and abbreviated as **SPWM**. The frequency of reference signal,f_r,determines the inverter output frequency,f_o, and its peak amplitude, A_r, controls the modulation index, M, and rms output voltage,V_o. The number of pulses per half cycle depends on the carrier frequency. Within the constraint that two transistors of the same arm (Q_1 and Q_2) cannot conduct at the same time, the instantaneous output voltage is shown in Fig. 3.4(a). The same gating signals can be generated by using unidirectional triangular carrier wave as shown in Fig.3.4(b).

The rms output voltage can be varied from 0 to V_s by varying the modulation index M from 0 to 1. It can be observed that the area of each pulse corresponds approximately to the area under the sine wave between the adjacent midpoints of off periods on the gating signals. If δ_m is the width of mth pulse, Eqn.(3.7) can be extended to find the rms output voltage

$$V_0 = V_s \left(\sum_{m=1}^{p} \frac{\delta_m}{\pi} \right)^{\frac{1}{2}} \tag{3.14}$$

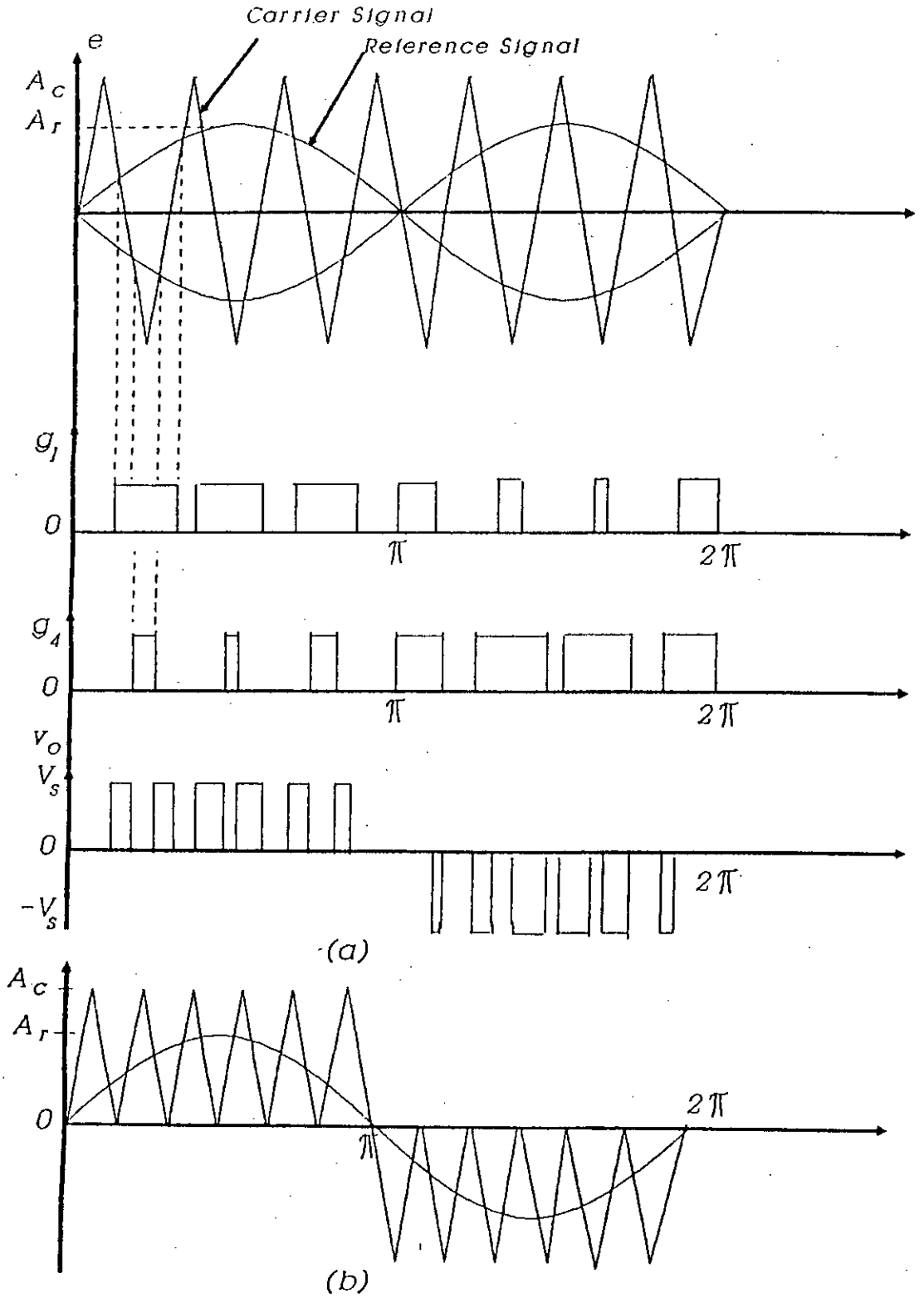


Figure 3.4 Sinusodial pulse-width modulation

Equations (3.11) and (3.12) in *multiple pulse width modulation* can also be applied to determine the Fourier co-efficients of output voltage as

$$A_n = \sum_{m=1}^{p} \frac{2V_s}{n\pi} [\sin n(\alpha_m+\delta_m) - \sin n\alpha_m] \quad (3.15)$$

and,

$$B_n = \sum_{m=1}^{p} \frac{2V_s}{n\pi} [\cos n\alpha_m - \cos n(\alpha_m+\delta_m)] \quad (3.16)$$

The output voltage can easily be obtained by using Eqns. (3.15) and (3.16).

A computer program named PROGRAM-3 in Appendix-1 is used to investigate the performance of Sinusoidal Pulse-Width Modulation.

3.2.4 Modified Sinusoidal Pulse Width Modulation(MSPWM)

In *sinusoidal pulse width modulation(SPWM)*, Fig. 3.4 indicate that the widths of pulses that are nearer the peak of the sine wave do not change significantly with the variation of modulation index. This is due to the characteristics of a sine wave, and the **SPWM** technique can be modified so that the carrier wave is applied during the first and last 60° intervals per half cycle (e.g.,0 to 60° and 120°to 180°), this type of modulation is known as **MSPWM** and shown in Fig. 3.5. The fundamental component is increased and its harmonic characteristics also improves. It reduces the number of switching of power devices and also reduces switching losses.

The number of pulses ,q, in the 60° period is normally related to the frequency ratio, particularly in three phase inverters, by

$$\frac{f_c}{f_0} = 6q + 3 \quad (3.17)$$

where, f_c is the carrier wave frequency and f_0 is the inverter output frequency.

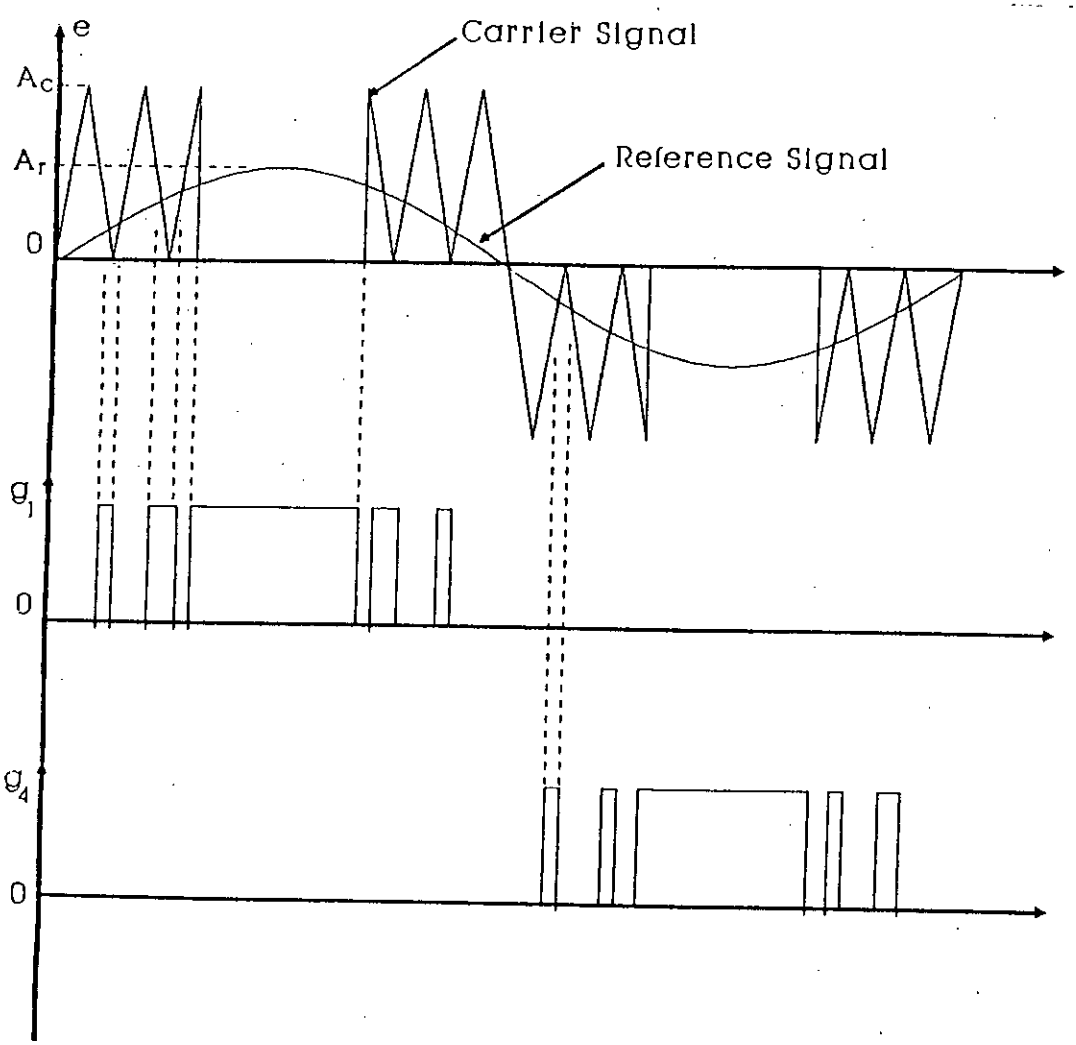


Figure 3.5 Modified sinusoidal pulse width modulation

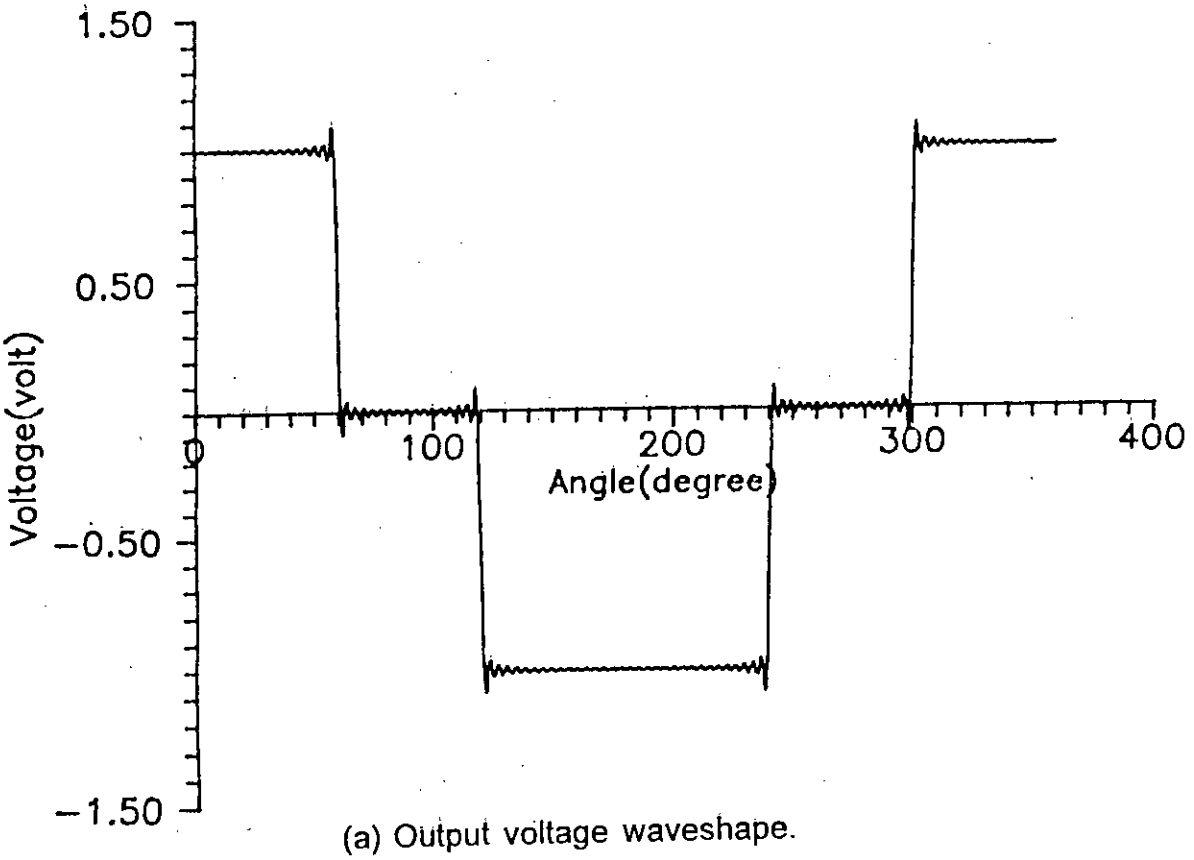
PROGRAM-4 in Appendix-1 is used to investigate the performance of Modified Sinusoidal Pulse-Width Modulation.

3.3 Computer Analysis

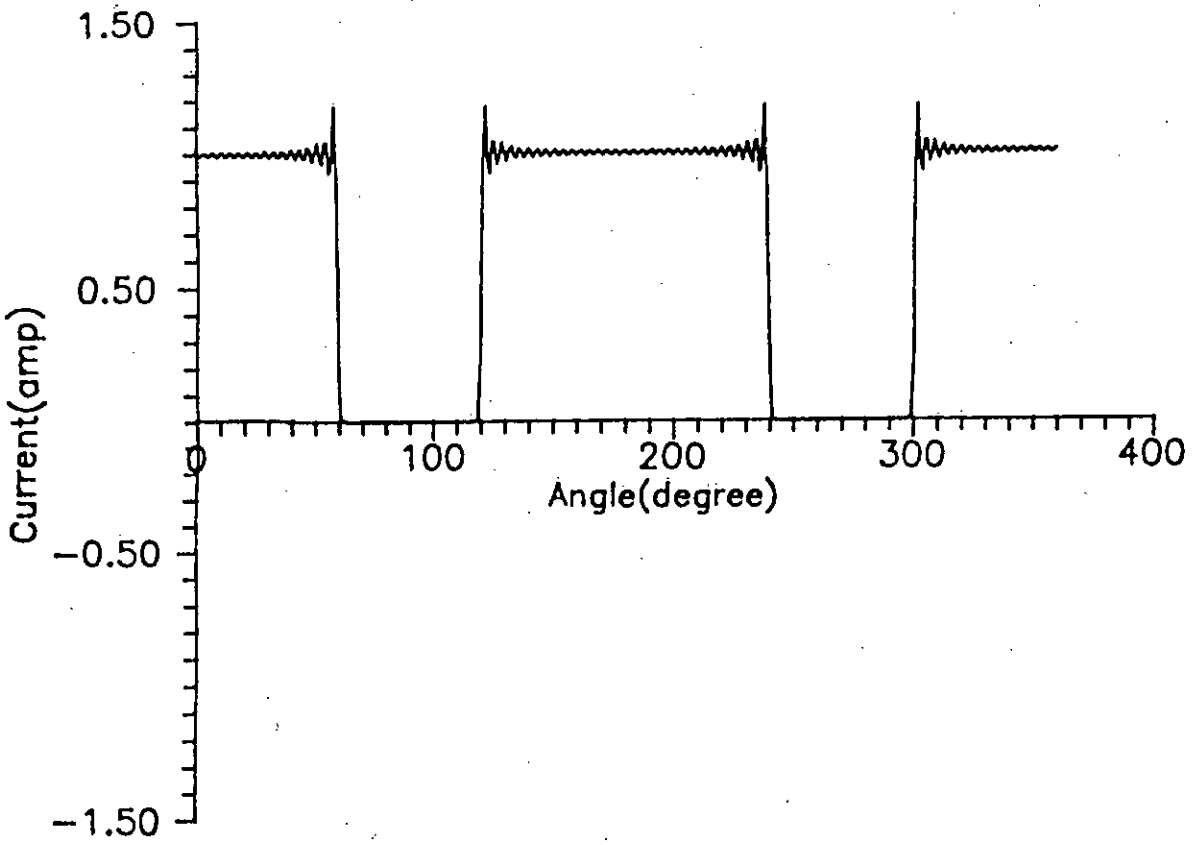
The output voltages and input currents waveshapes of different voltage controls can be graphically plotted by the use of data files programs shown in Appendix-1.

Using the computer program named "inverter" (in Appendix-1) the proposed single pulse modulation inverter is analysed. The simulated input, output waveforms for a modulation index of M=1 (δ = 180°) is shown in Chapter-2. The same waveforms for a controlled output voltage of 147 volt (M=0.67, δ = 120°) are shown in Fig. 3.6. The frequency spectra are tabulated in Table 3.1. By varying the modulation index(M), in term the pulse duration, δ, the output voltage can be varied.

Table 3.1	
Frequency spectra of waveforms associated with inverter output voltage	
Harmonic Coefficients when δ=120°	
Order (n)	Amplitude (B_n)
1	1.10
3	0.00
5	0.22
7	0.16
9	0.00
11	0.10
13	0.09
15	0.00
17	0.07
19	0.06
21	0.00
23	0.05



(a) Output voltage waveshape.



(b) Input current waveshape.

Figure 3.6 Output voltage and input current waveshapes of a single phase inverter, where pulse width δ=120°.

3.4 Conclusions

In most inverter applications, stepless control of the ratio of source voltage (which is d.c.) to a.c. voltage supplied to the load is necessary. Several techniques can be used to control the output voltage and they produce a range of harmonics on the output voltage. Sinusoidal Pulse Width Modulation (SPWM) is more effective in reducing the lower harmonics. With a proper choice of the switching patterns for power devices, certain harmonics can be eliminated.

The technique discussed to control the output voltage differ in the harmonic content that they produce in the inverter output voltage, thus the acceptable harmonic content is the factor that determines choice of techniques.

Various techniques of voltage control of single phase inverter are discussed in this chapter. Single pulse modulation is used for analysis and construction of the proposed inverter. The output voltage and input current and their spectra are also discussed in details in this chapter.

CHAPTER-4

DESIGN AND CONSTRUCTION

4.1 Introduction

The single phase inverter discussed in Chapter-3 has been implemented in this chapter. The single pulse modulation is taken as the switching function.

The determination of voltage and current ratings of power devices in inverter circuits depends on the type of inverters, load and methods of voltage and current control. A proper design gives an accurate result. There are many switching devices available to switch off and on in a particular circuit. The important task is to choose suitable devices considering data like power loss, power rating, etc.

4.2 Functional Description of the Inverter

The block diagram of the inverter [4] is shown in Fig. 4.1.

The squarewave generator stage produces two antiphase squarewaves,each of 50 Hz. These are applied to the bases of transistors in the push-pull driver stage which switches on and off according to the squarewaves.

The effective gain of the driver stage is controlled by the driver stage controller.

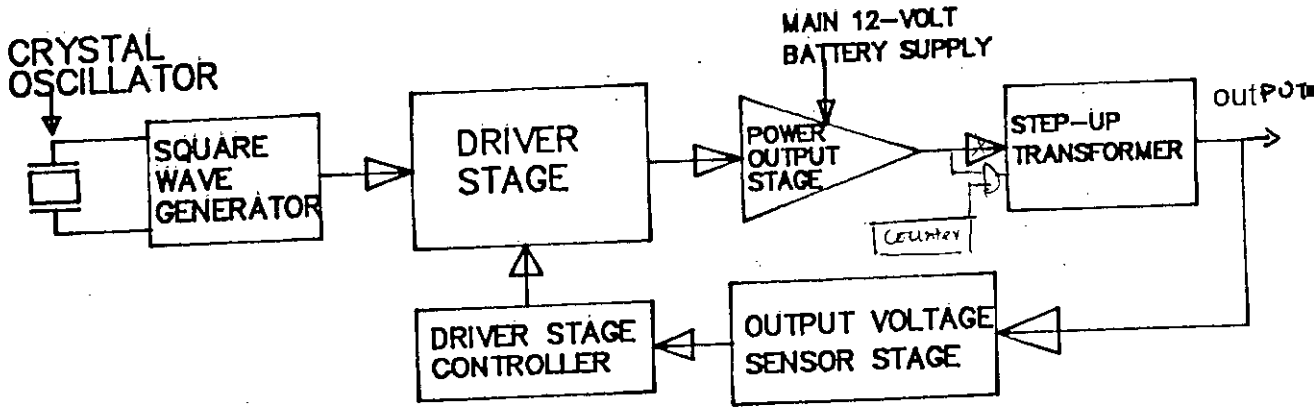


Fig. 4.1 Block diagram of the inverter

There are two push-pull power transistors in the power output stage. The bases of these transistors are driven from the driver stage. The transistors in the driver stage are switched on and off according to the input square waves. The collectors are fed from the main 12 volt battery supply.

The emitters of the power transistors are connected to the two ends of the low voltage side of a center tap step up transformer. The low side center tap terminal is connected to the negative terminal of the main 12 volts battery supply. When one of the power transistors is on, current flows from the battery via this power transistor,through the transformer winding and back to the negative terminal of the battery. Due to antiphase squarewaves, these two power transistors do not switch on at the same time. Transformer action occurs and a stepped up voltage is induced in the secondary.

A stepdown transformer and operational amplifier are used in the output voltage sensor stage. The output voltage is stepped down and then rectified and smoothed. This voltage, which is proportional to the output voltage is then compared with a fixed reference voltage using a 741 op-amp as a comparator.

The output of this comparator is fed into the gate of a MOSFET in the driver stage controller. When the output voltage is low, the output of the comparator increases and drives the MOSFET towards saturation. This allows the transistors in the driver stage to get more supply and correspondingly, more voltage to the bases of the power transistors. This increases the output voltage. When the output voltage is high, the reverse action occurs. The voltage is adjusted by a potentiometer in the op-amp comparator circuit which sets the threshold level.

4.3 Design Criteria

The specification of the inverter is given below:

Power output	100 watt
Output voltage	220 Volt A.C.
Input voltage	12 Volt D.C.
Frequency	50 Hertz
Single phase	
Regulated output	

4.3.1 Design of the 50 Hz Antiphase Squarewave Generator

There are several ways to generate 50 Hz antiphase square waves. In this case, a quartz crystal is used [7]. For this final frequency, a suitable crystal frequency is 3.2768 MHz . The crystal is operating in parallal resonance in conjunction with 4060 CMOS IC [8]. The 4060 CMOS chip is containing a 14 stage binary ripple counter and an internal high frequency oscillator which can be directly coupled to a crystal [12]. As there is an internal oscillator within the chip, this chip offers a great advantage to have 3.2768 MHz oscillation without using any additional active components. By cascading the counter stages, it is possible to divide the input crystal frequency by 2^n within the chip[14], where 'n' is the number of stages. There are 14 stages within the chip i.e. n = 14, so the output pulse will have a frequency of

$$= \frac{input\ \ frequency}{2^n}$$

$$= \frac{3.2768\ x\ 10^6}{2^{14}}\ \ Hz$$

$$= \frac{3.2768\ x\ 16^6}{16,384}$$

$$= 200\ Hz$$

Counter IC 4060 has only a single output [14]and the division ratio is insufficient to have 50 Hz, so extra stages in the form of a dual bistable IC are added at its output. There are several chips available to divide this 200 Hz into 50 Hz viz. CMOS 4013, dual D flipflop or CMOS 4027, dual J-K flipflop can be used. But in this case, CMOS 4013 is preferable as its current capacity is higher than the 4027 chip. The two bistables in IC 4013 are connected in series to provide a further division. The output at pin 3 of the chip 4060 is fed into the first D flipflop[11] of chip 4013 at pin 11 as a clock input. The output at pin 13 (Q_1) which is 100 Hz square wave pulse is fed into pin 3 of 2nd flipflop as clock input. The outputs of 2nd flipflop are two complementary square waves at pin 1 as Q_2 and at pin 2 as $\bar{Q}_2$.

The pin configuration and other information about these two chips are given in Appendix-2.

The internal connection of the frequency generator stage is shown below in Fig.4.2.

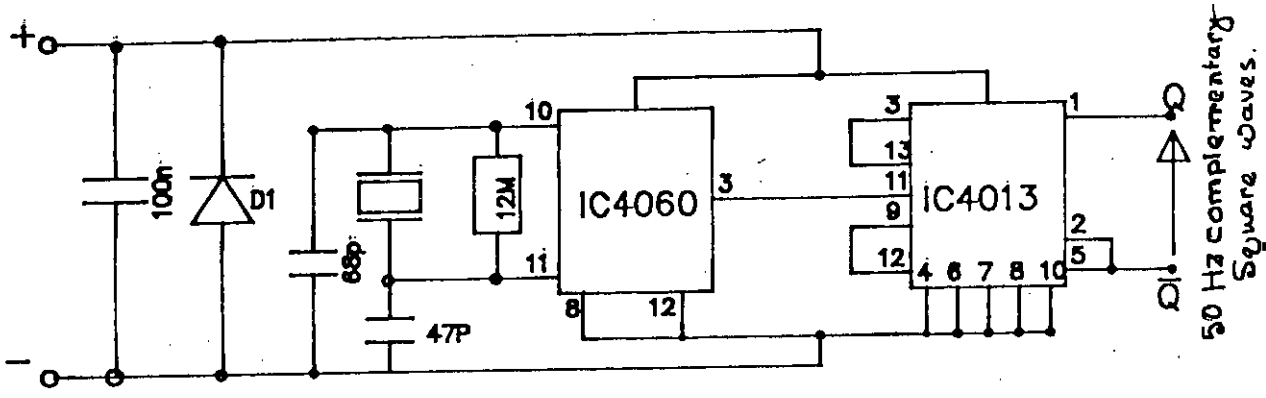


Fig.4.2 Schematic diagram of the frequency generator stage

As the supply voltage is 12 volts, the square waves pulse will be 12 volts peak to peak.

The two complementary 50 Hz output square waves are used to drive transistors. As transistors will be on and off simultaneously and high voltage spikes will be produced by the rapid switching of transformer. So the diode D_1 protects these ICs from these high voltage spikes and also give protection if the battery has reversed connection.

The rating of D_1 is IN4001, 1A, 50 volt.

4.3.2 Design of the Power Output Stage

The power rating is 100 watts and the output voltage is 220 volts.

Let the load is resistive, so the load current

$$I_2 = \frac{100}{220} = 0.4545\ A$$

Let the transformer primary voltage is 8-0-8 volt and transformation ratio is

$$a = \frac{V_1}{V_2} = \frac{8}{200} = 0.0366$$

The corresponding primary current

$$I_1 = \frac{I_2}{a} = \frac{0.4545}{0.0366} = 12.50\ A$$

Assume, the combined value of no load magnetizing current of the transformer and current for the feedback network is equal to 0.5 A.

So the total primary current is = 12.50 + 0.5 = 13 A.

A semiconductor switching device is needed which is able to carry this 13 A current. A suitable device is 2N3055H NPN transistor. It has a current rating of 15 A. So it can be connected as a emitter follower which is shown below in Fig. 4.3.

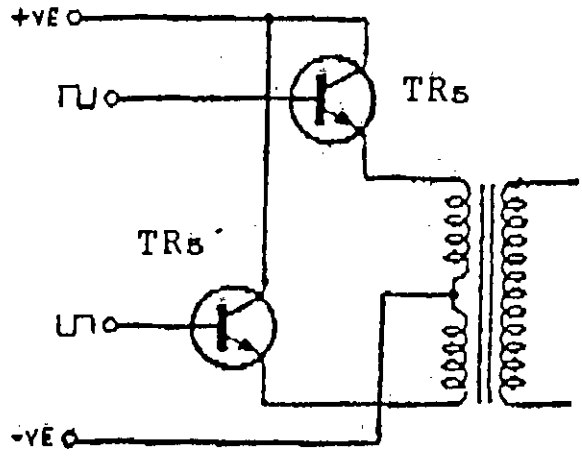


Fig. 4.3 Schematic diagram of the power output stage

From Fig. 4.3, assume $I_{C5} \approx I_{E5}$ = 13 A.

The current gain (h_{fe}) of 2N3055H is equal to 20 to 70. Taking h_{fe} as minimum. Therefore the base current is

$$I_{B5} = \frac{I_{C5}}{hfe} = \frac{13}{20} = 0.65\ A$$

The square wave generator stage is not able to carry this amount of current. So multiple stage amplification is required.

4.3.3 Design of the Driver Stage

The outputs of the square wave generator stage are fed to the bases of two transistors. The preferred transistors are BD556. The connections of these transistors are shown in Fig. 4.4

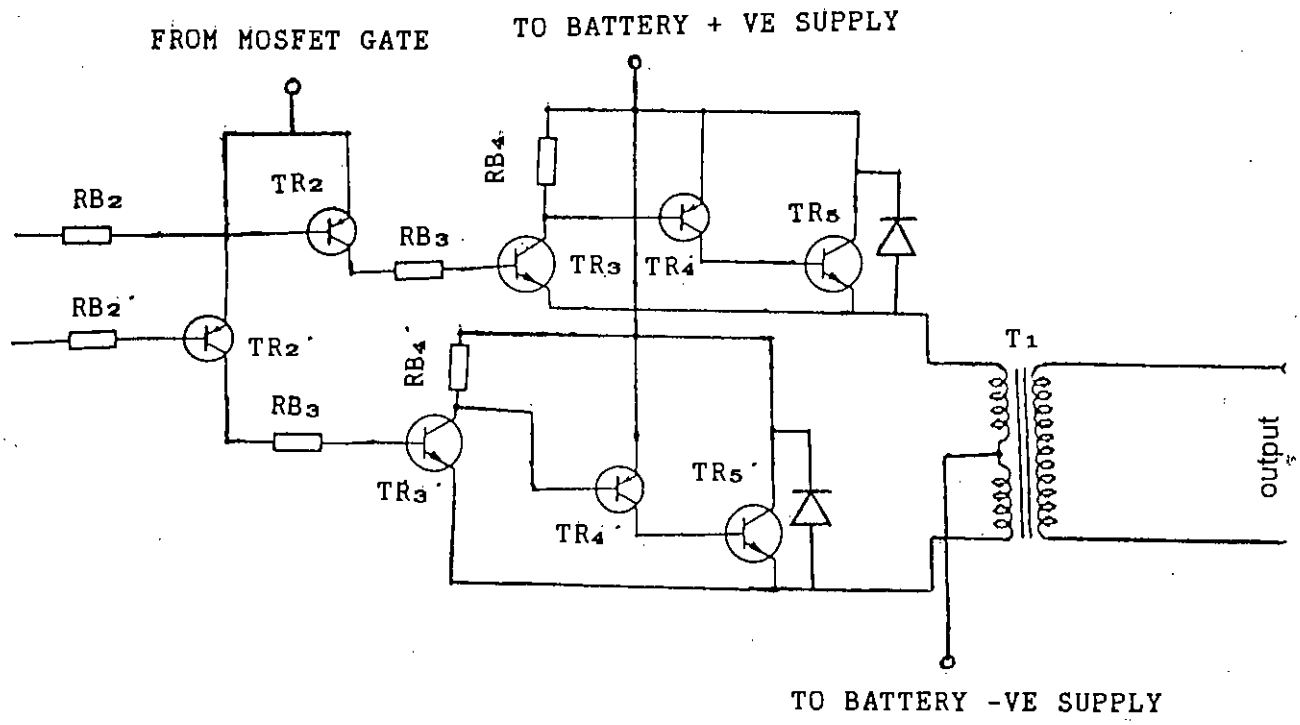


Figure 4.4 Shematic diagram of driver and power output stage

At saturation, the voltage at TR_2 base is [9]

$V_{B2} = 12 - V_{DS} - V_{BE}$

$= 12-0.3 -0.6 = 11.1$ V

To keep the base current of BD556(TR_2) at some micro ampere say, 2.50 μA which is sunk by the square wave generator stage, the required resistance is [10]

$$R_{B2} = \frac{11.10}{2.50X10^{-6}} = 4.44M\ \Omega$$

The nearest preferred value to 4.44 MΩ is 4.50 MΩ. From manufacturer data, the h_{fe} of the BD556, ranges from 125 to 500, so taking h_{fe} minimum

$$I_{C2} = I_{B2}\ x\ hfe = 2.50x10^{-6}\ x\ 125 = 0.31\ mA$$

A NPN transistor BC107(TR_3) is chosen whose connection is shown in Fig. 4.4 It has a collector current of 100 mA (max.) and h_{fe} lies between to 110 to 450. Therefore,

$$V_{C2} = 12 - V_{DS} - V_{CE2} = 12 - 0.3 - 0.3 = 11.4\ V$$

and the voltage at TR_3 base is,

V_{B3} = V_{BE3} + (voltage at transformer upper winding)

V_{B3} = 0.6 + 10 = 10.6 V.

Assuming, $V_{E2} \approx V_{C2}$.

As, $I_{C2} = I_{B3}$ = 0.31 mA, a resistance is required to maintain the current 0.31 mA, and the value of resistance is

$$R_{B3} = \frac{11.40 - 10.60}{0.31\ x\ 10^{-3}} = 2.58K\ \Omega \simeq 250K\ \Omega$$

The collector current of TR_3 is

$$I_{C3} = hfe\ x\ I_{B3}$$

$$I_{C3} = 110\ x\ 0.31\ x\ 10^{-3} = 34\ mA. \qquad (4.1)$$

A transistor is required to carry the base current 0.65 A of power transistor 2N3055H. The preferred transistor is BD132 PNP transistor whose h_{fe} is equal to 20 (min).

From Fig.4.4,

$I_{C4} = I_{B5}$

assuming, $I_{C4} \approx I_{E4}$

The base current of BD132 (TR_4) which is sunk by TR_3 is

$$I_{B4} = \frac{I_{B5}}{hfe_4}$$

$$I_{B4} = \frac{0.65}{20} = 32.5mA$$

From Eqn. 4.1, I_{C3} = 34 mA, so extra 34 - 32.5 = 1.5 mA is to be carried from the main positive supply through a resistance. The voltage at TR_4 base, which is also the collector voltage of TR_3, is

$$V_{B4} = V_{C3} = 12 - V_{BE4} = 12 - 0.7 = 11.3\ V$$

and the required resistance is

$$R_{B4} = \frac{12 - 11.3}{1.5 \times 10^{-3}} = 466\ \Omega$$

The nearest preferred value to 466 **Ω** is 470 **Ω**.

Due to rapid switching of transistors, the high voltage spikes are produced in the transformer T_1 primary. To protect transistors from these spikes two low rating diodes are used to absorb spikes.

The preferred value is IN4002, 100 V, 1 A.

Transistors TR_4,TR_4',TR_5 and TR_5' should be fitted with a heat sink to transfer heat.

4.3.4 Selection of the Output Transformer

Assuming a worst case battery regulation volt drop of 2V, plus a 2V collector to emitter output power transistor volt drop, then the available primary voltage will be 8V. So a center tap transformer of 8-0-8V primary and 220V secondary, 100 VA can be used.

4.3.5 Design of the Output Voltage Sensor Stage and Driver Stage Controller

To compare the output voltage with a fixed low level dc reference voltage, it is necessary to step down and rectify the inverter output voltage. The output voltage is stepped down using a 220/22 V, transformer, then rectified and smoothed. The feed back network is shown in Fig. 4.5.

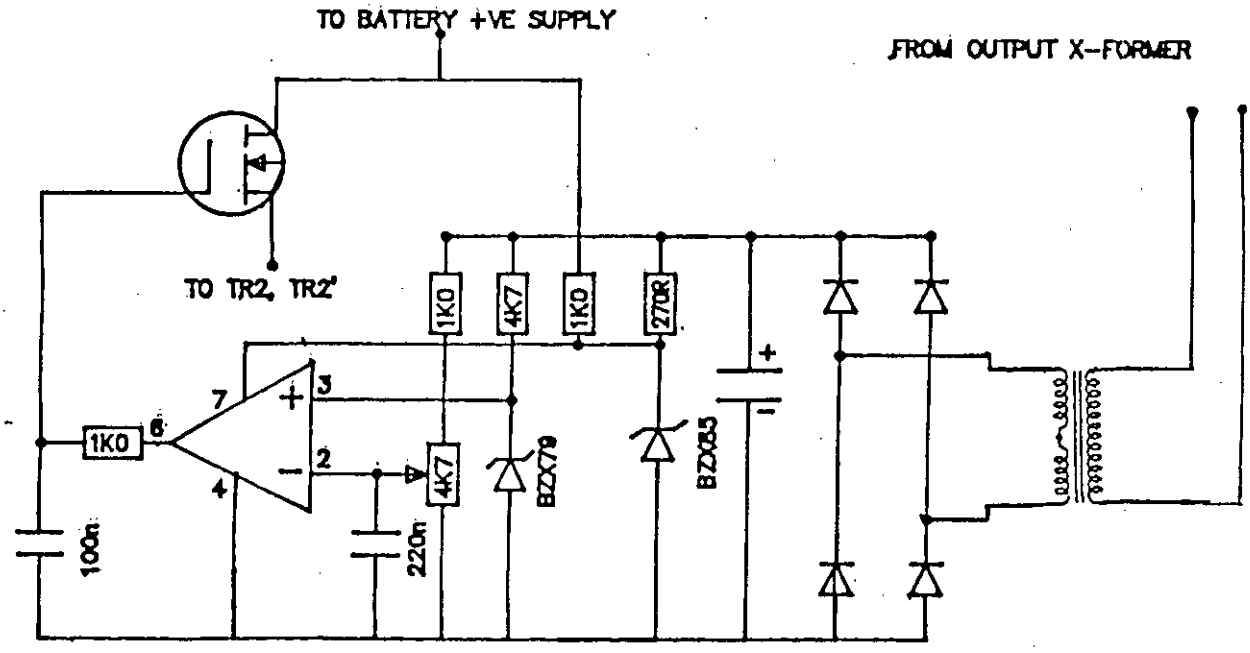


Fig. 4.5 Schematic diagram of the feed back stage.

The loop control component is a VN66AF N channel MOSFET which effectively controls the current levels being sourced by TR_2 and TR_2' first stage transistors. Since it is necessary to provide the field effect control transistor with a positive going gate voltage, then the op-amp comparator can be supplied from a positive unbalanced single rail source. This can be derived from the inverter output voltage once the circuit has started and from the 12V battery supply at start up (via a 1K resistor).

A 5.1V zener diode comparator reference is used to ensure that the op-amp input circuitry remains correctly biased and to give a convenient voltage level with which to compare the rectified proportion of the inverter output voltage. This reference is provided by a BZX79, 5.1V, 500mW zener diode.

A 741 operational amplifier is used on open loop as a high gain comparator, the high gain ensuring that the overall control loop is highly responsive to any output voltage variation. Since the MOSFET requires up to a 3V gate to source voltage before being fully switched on, its gate must be supplied from a voltage of at least 3V greater than the 12V which will appear at the source when the device is fully switched on. This implies that the op-amp output voltage driving the gate, must be able to supply 15V. To allow for op-amp saturation at about 1V less than the supply voltage, a 16V op-amp supply is chosen. This is derived from a BZX85, 1.3W, 16V zener diode.
The current rating of this diode is = 1.3/16 = 81.25 mA. The value of resistance connected in series with the zener diode if the zener diode operates at 25 mA is

$$R_{Z16} = \frac{22-16}{25 \times 10^{-3}} = 240\ \Omega$$

The nearest preferred value is 270 **Ω**.

The fixed 5.1V reference voltage at the non-inverting input is provided by a BZX79, 5.1 V, 500 mW zener diode. The current rating of this diode is = 500 mW/5.1 = 98.03 mA.

To operate the zener diode at a safety current of 4 mA, a resistance is required to be connected in series with the zener diode and the value is

$$R_{Z5.1} = \frac{22-5.1}{4x10^{-3}} = 4.82\ K\Omega$$

The nearest preferred value is 4.70 KΩ.

A porportion of the output voltage is fed to the inverting input via a potentiometer and a fixed value resistance in series. With an inverter output voltage of 220V, the voltage across the potentiometer is

$$= \frac{22}{(4.1+1)x10^{3}}\ x\ 4.7x10^{3} = 18\ V$$

Adjustment of the potentiometer wiper allows the inverter output voltage to be set.

From manufacturer data, the op-amp draws a current of 2.8 mA. The total current drawn by the feedback network is (25+4+4+2.8) = 35.8 mA. So the rating of the transformer is 1.5 VA, and the preferable diodes and capacitor are IN4002, 1A, 100 V and 50 μF, 100 V respectively.

The complete circuit with all stages is shown in Fig. 4.6.

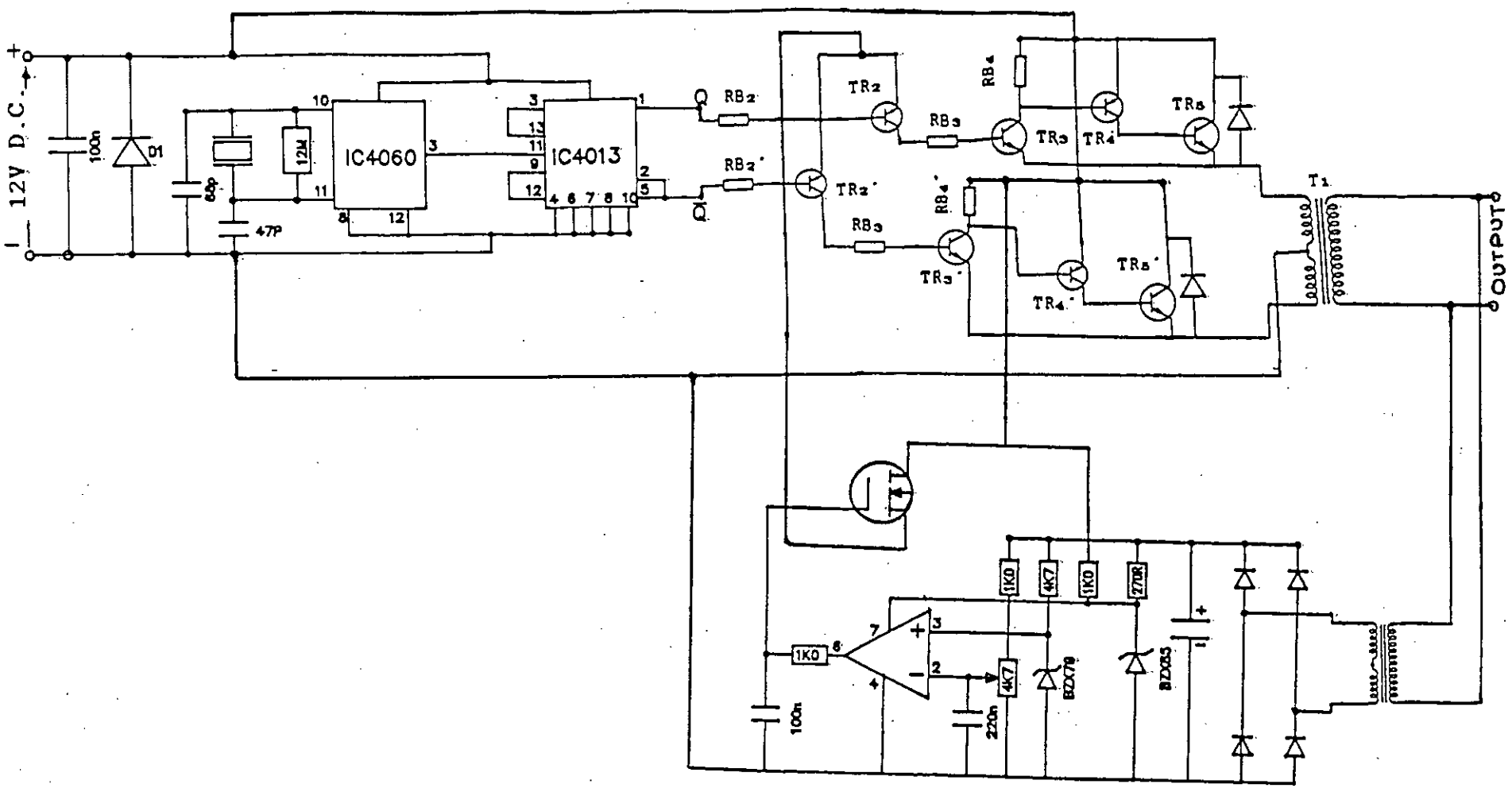


Fig. 4.6 Complete circuit diagram of the inverter.

4.4 CONSTRUCTION AND TESTING

4.4.1 Construction

The different blocks designed in article 4.3 were constructed in modular from on tag strips. This allowed each block to be tested individualy.

4.4.2 Testing

The following tests are made for calculating the performance of designed inverter.

4.4.2.1 Output Waveshape of Squarewave Generator

According to the design, the output wave shapes should be two antiphase square waves of 50 Hz, having 12 volt peak.

The photograph is shown below, is taken from a oscilloscope screen, when the oscilloscope is connected to the output of the stage.

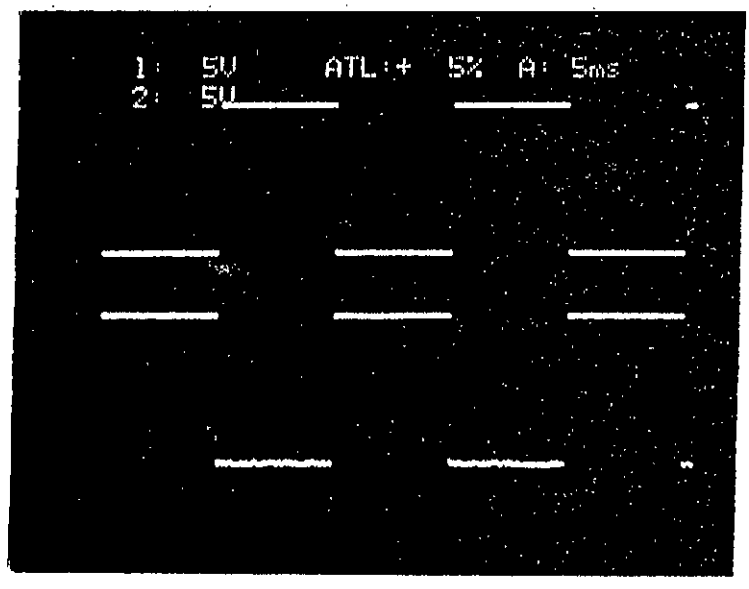
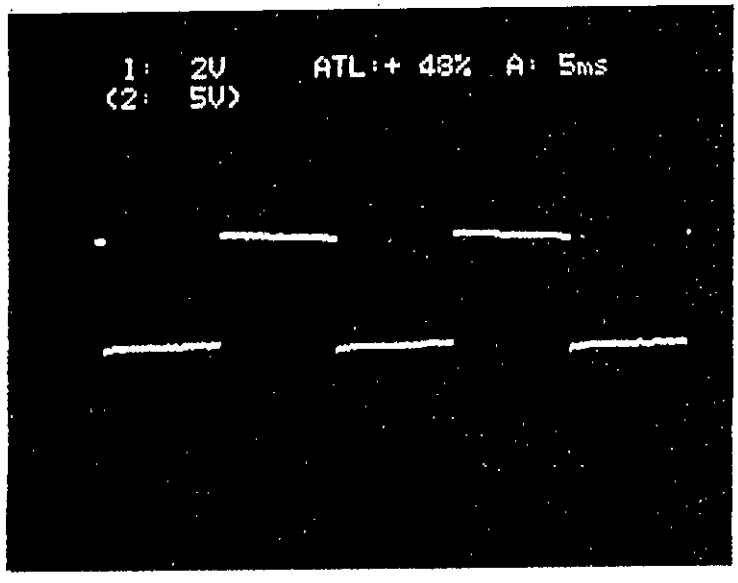


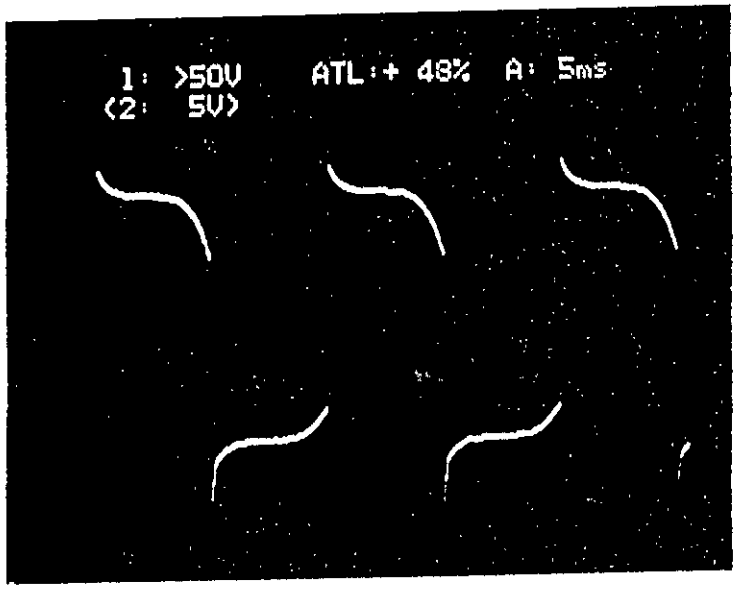
Figure 4.7 Experimental waveform of square waves

4.4.2.2 Voltage Waveshapes of Transformer Primary & Secondary.

The voltage waveshapes of transformer primary and secondary are shown below:

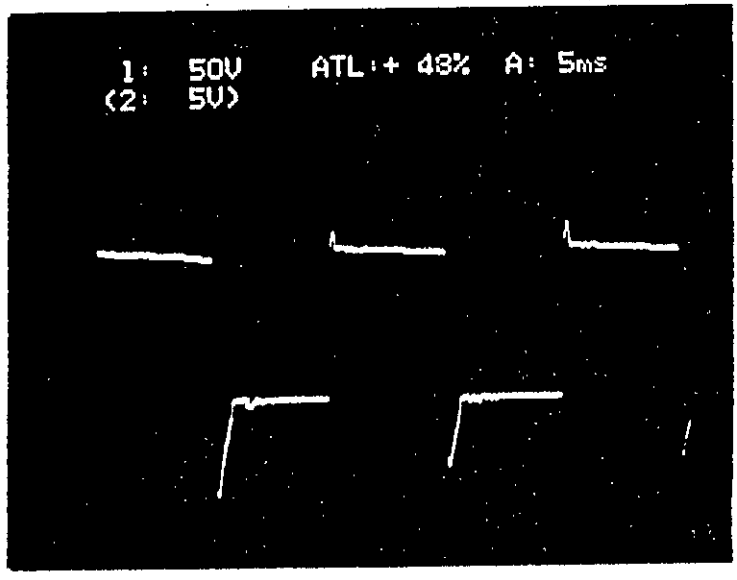


(a) Primary voltage waveshape at no load

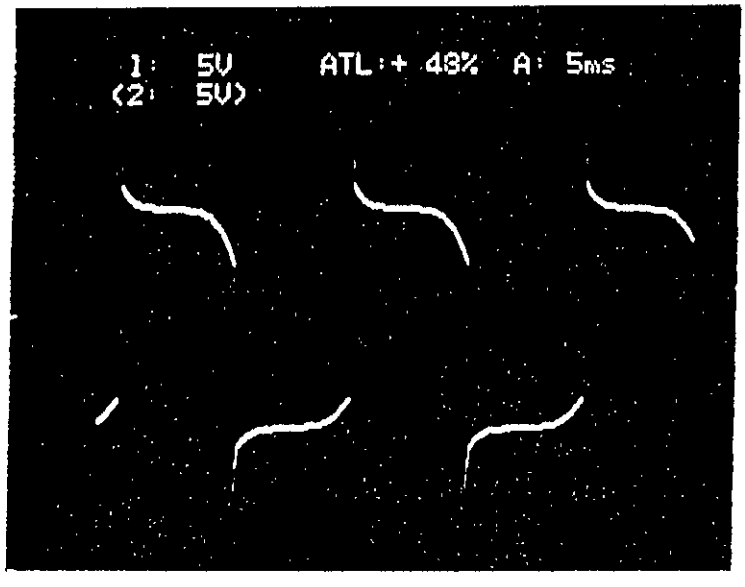


(b) Primary voltage waveshape at 30W load.

Figure 4.8 Experimental waveforms of primary voltage



(a) Secondary voltage waveshape at no load



(b) Secondary voltage waveshape at 30W load.

Figure 4.9 Experimental waveforms of secondary voltage

4.5 Conclusions

The inverter was constructed and tested and found to work satisfactorily with an operating input voltage of 12V. The output voltage of this inverter is almost constant at all loads. The experimental input and output waveshapes matches with the computer simulated waveshapes of Chapter-3.

CHAPTER-5

SUMMARY, CONCLUSIONS AND RECOMMENDATIONS

5.1 Summary

A single phase inverter under fixed output voltage is designed and constructed in this project. In Chapter-1, introductory discussion, proposed method and scope of this project is discussed. Principle of operation and voltage control of an inverter is discussed in Chapter-2 and Chapter-3 respectively. Various types of control and computer analysis is done in Chapter-3. In chapter-4, detail design procedure, construction and testing are discussed and studied.

5.2 Conclusions

The output voltage of this single phase inverter is squarewave. The square wave sometimes makes problem in reactive circuits. It contains several harmonics, which causes heating. But the important advantage of the squarewave is that it has zero rise time and zero fall time and peak value is constant with respect to time. To operate a transistor at a definite voltage, the squarewave voltage does not take any time whereas the sine wave takes some time for the transition to the peak.

The cost of this single phase inverter specially for low power is Tk.4,500/. The cost is not high enough but the main problem is to recharge the battery after it is discharged. However, this problem can be solved by using a front end rectifier.

The output voltage of this inverter is constant upto the designed load by turning the wiper at the feed back network. When the battery is near to discharge level the output voltage does not remain constant. By the proper design of a transformer and by the use of a fully charged battery this problem can easily be overcome.

Each of the power transistors have a current rating of 15 A. If some loss of regulation can be tolerated then it is possible to obtain upto 150 watts.

5.3 SUGGESTIONS FOR FUTURE WORK

The design and construction of a single phase inverter is presented in this project. The output voltage is square wave.

Filter may be used to study further the behavior of the output voltage waveshape.

Single phase inverter with advanced PWM can be further studied.

Moreover, where the cost of the low power single phase inverter is less or higher than the diesel or petrol driven generator is a case of further study.

REFERENCES

[1] Muhammad H. Rashid, " Power Electronics Circuits, Devices, and Applications", Prentice Hall, New Jersey, 1988.

[2] S.B.Dewan and A.Straughen, " Power Semiconductor Circuits ", Jhon Willey and Sons, Newyork, 1975.

[3] Mark Daniels, "Battery to mains inverter", Everyday Electronics, Wimborne, March'91, pp. 152-154

[4] Cyril W. Lander, " Power Electronics ", McGraw-Hill Book Company, Newyork.

[5] Shahidul I. Khan, M.H. Rashid, M.R. Khan," Generalized Circuit Model for Static Converters ", conference record, 32nd Midwest Symposium on circuits and Systems, IEEE-University of Illinois, Urbana, USA, Aug.,1989, PP. 771-776.

[6] David A. Bell, " Operational Amplifiers, Applications, Troubleshooting, and Design", Prentice Hall, Englewood Cliffs, New Jersey, 1990.

[7] Paul Horowitz and Winfield Hill, " The Art of Electronics ", Cambridge University Press, Cambridge, 1990.

[8] Donald G. Fink (Editor) and Donald Christiansen (Editor), " Electronics Engineers' Handbook", McGraw-Hill Book Company, Newyork, 1989.

[9] V.K.Metha,"Principles of Electronics", S.Chand & Company Ltd, New delhi, 1986.

[10] John C. Morris,"Electronics: Practical Applications and Design", Edward Arnold,London, 1989.

[11] D.C.Green," Digital Techniques and Systems ", Pitman, London, 1980.

[12] Don Lancaster," CMOS Cookbook ", SAMS (Macmillan Computer Publishing), Indiana, USA, 1990.

[13] R.M. Marston, " CMOS circuits Manual ", Heinemann Newness, Oxford, 1987.

APPENDICES

APPENDIX-1

COMPUTER PROGRAM-"INVERTER"

DETERMINATION OF NECESSARY DATA TO PLOT THE OUTPUT VOLTAGE AND INPUT CURRENT.

```
      REAL INPCUR
      INTEGER ANGLE
      DIMENSION A1(100)
      OPEN(10,FILE='COEFF4.DAT')
      OPEN(11,FILE='VOV4.DAT')
      OPEN (12,FILE='INPCUR4.DAT')
      WRIRE(*,*) 'PULSE WIDTH LESS THAN 180°?'
      READ(*,*) PW
      PI=3.141592
      R=1.0
      DEL=(PW*PI)/180
      DO 1 K=1,99,2
      A1(K)=(4/(PI*K))*SIN(DEL*K/2)
      WRITE(10,20)K,A1(K)
1     CONTINUE
20    FORMAT(4X,'A1(',I2,')=',F13.8)
      DO 2 ANGLE=0,360
      VOV=0.0
      INPCUR=0
      RAD=FLOAT(ANGLE)*PI/180
      DO 3 J=1,99,2
      VOV=A1(J)*COS(J*RAD)+VOV
3     CONTINUE
      WRITE(11,30)ANGLE,VOV
      INPCUR=(VOV**2)/R
      WRITE(12,40)ANGLE,INPCUR
2      CONTINUE
30    FORMAT(4X,'ANGLE=',I3,'°',2X,
     1'OUTPUT VOLTAGE=',F14.8,2X,'VOLTS')
40    FORMAT(4X,'ANGLE=',I3,'°',2X,'INPUT  CURRENT=',
     1F14.8,2X,'A')
      STOP
      END
```

PROGRAM-2

PROGRAM TO INVESTIGATE THE PERFORMANCE 0F UNIFORM PULSE WIDTH MODULATION.

```
      DIMENSION ALFAM(20),ALFAD(20),AN(100),BN(100),CN(100)
      INTEGER NM,IANGLE
      REAL INCUR
      OPEN(5,FILE='PMH.DAT')
      OPEN(6,FILE='ALFAD.DAT')
      OPEN(7,FILE='OPV2.DAT')
      OPEN(8,FILE='INCUR2.DAT')
      OPEN(9,FILE='HCOEFF2.DAT')
      WRITE(*,*) 'No. of pulses per half cycle ?'
      READ(*,*) NP
      WRITE(*,*) 'Modulation index less than 1 ?'
      READ(*,*) AMF
      WRITE(*,*)'Highest desired harmonic component less
     1 than 100?'
      READ(*,*) NM
      PI=3.14159297
      R=1
      DELTA=(PI/NP)*AMF
      DELTAD=(DELTA*180.0)/PI
      CENTR=(PI/NP)/2.0
      ALFAM(1)=CENTR-DELTA/2
      ALFAD(1)=ALFAM(1)*180.0/PI
      DO 100 M=2,NP
      ALFAM(M)=ALFAM(1)+(PI/NP)*(M-1)
      ALFAD(M)=ALFAM(M)*180.0/PI
100     CONTINUE
      WRITE(5,10)NP,AMF,NM
10     FORMAT(5X,'NO OF PULSES PER HALF
     CCYCLE=',I2/5X,'MODULATION INDEX=',F3.2/5X,'HIGHEST DESIRED
     CHARMONIC COMPONENT=',I2)
      WRITE(5,20)
20     FORMAT(//)
      DO 150 I=1,NP
      WRITE(6,30)I,ALFAD(I)
30     FORMAT(5X,'am(',I2,')=',F8.3,'°')
150     CONTINUE
      VS=1
      DO 200 N=1,NM
      A=0
      B=0
```

```
      DO 300 M=1,NP
      B=SIN(N*(ALFAM(M)+DELTA/2))+B
      A=COS(N*(ALFAM(M)+DELTA/2))+A
300     CONTINUE
      AN(N)=(((4*VS)/(N*PI))*SIN(N*DELTA/2))*A
      BN(N)=(((4*VS)/(N*PI))*SIN(N*DELTA/2))*B
      CN(N)=SQRT((AN(N)**2)+(BN(N)**2))
200     CONTINUE
      DO 350 N=1,NM,2
      WRITE(9,35)N,CN(N)
35     FORMAT(5X,'CN(',I2,')=',F13.8)
350     CONTINUE
      DO 400 IANGLE=0,360
      VOV=0
      INCUR=0
      DO 500 N=1,NM,2
      VOV=AN(N)*COS(N*FLOAT(IANGLE)*PI/180.0)+BN(N)
     C*SIN(N*FLOAT(IANGLE)*PI/180.0)+VOV
500     CONTINUE
      INCUR=(VOV**2)/R
      WRITE(7,40)IANGLE,VOV
40     FORMAT(5X,'ANGLE=',I3,'°',5X,
     C'OUTPUT VOLTAGE=',F12.8,'VOLTS')
      WRITE(8,50)IANGLE,INCUR
50     FORMAT(5X,'ANGLE=',I3,'°',5X,
     C'INPUT CURRENT=',F12.8,'A')
400     CONTINUE
      STOP
      END
```

PROGRAM-3

PROGRAM TO INVESTIGATE THE PERFORMANCE OF SINUSOIDAL PULSE WIDTH MODULATION.

```
      DIMENSIONC(25),CN(100),Y(90),X(90),ALFA(25),ALFAD(25),
     CAN(100),BN(100),SL(25)
      INTEGER ANGLE,NM
      REAL INCUR
      OPEN(5,FILE='PMHC3.DAT')
      OPEN(6,FILE='ALFADC3.DAT')
      OPEN(7,FILE='OPVC3.DAT')
      OPEN(8,FILE='INCURC3.DAT')
      OPEN(9,FILE='HCOEFF3.DAT')
      WRITE(*,*) 'No. of pulses per half cycle ?'
      READ(*,*) NP
      WRITE(*,*) 'Modulation index less than 1 ?'
      READ(*,*) AMF
      WRITE(*,*) 'Highest desired harmonic component less than
     C100?'
      READ(*,*) NM
      PI=3.141592
      R=1
      NS=2*NP
      TOL=.0001
      DO 100 M=1,NS
      SL(M)=((-1)**M)*((NS+2)/PI)
100   CONTINUE
      DO 200 M=1,NS,2
      C(M)=M+1
200   CONTINUE
      DO 300 M=2,NS,2
      C(M)=-M
300   CONTINUE
      Y(1)=AMF
      X(1)=PI/2.0
      DO 400 M=1,NS
      DO 500 I=1,90
      K=I+1
      X(K)=(Y(I)-C(M))/SL(M)
      Y(K)=AMF*SIN(X(K))
      XX=ABS(X(K)-X(K-1))
      IF (XX.LT.TOL) GOTO 600
500   CONTINUE
600   ALFA(M)=X(I)
400   CONTINUE
      DO 700 M=1,NS
```

```
      ALFAD(M)=ALFA(M)*180.0/PI
700   CONTINUE
      VS=1.0
      WRITE(5,10)NP,AMF,NM
10    FORMAT(5X,'NO OF PULSES PER HALF
      CYCLE=',I2/5X,'MODULATION INDEX=',F3.2/5X,'HIGHEST
      DESIRED CHARMONIC COMPONENT=',I3)
      WRITE(5,20)
20    FORMAT(//)
      DO 800 I=1,NS
      WRITE(6,30) I,ALFAD(I)
30    FORMAT(5X,'αm(',I2,')=',F8.3,'°')
800   CONTINUE
      WRITE(6,40)
40    FORMAT(//)
      DO 900 N=1,NM
      A=0
      B=0
      DO 1000 M=1,NS,2
      A=SIN(N*ALFA(M+1))-SIN(N*ALFA(M))+A
      B=COS(N*ALFA(M))-COS(N*ALFA(M+1))+B
1000  CONTINUE
      AN(N)=((2*VS)/(N*PI))*A
      BN(N)=((2*VS)/(N*PI))*B
      CN(N)=SQRT(AN(N)**2+BN(N)**2)
900   CONTINUE
      DO 1050 N=1,NM,2
      WRITE(9,45)N,CN(N)
45    FORMAT(5X,'CN(',I2,')=',F13.8)
1050  CONTINUE
      DO 1100 ANGLE=0,360
      VOV=0
      INCUR=0
      DO 1200 N=1,NM,2
      VOV=AN(N)*COS(N*FLOAT(ANGLE)*PI/180.0)+BN(N)
      *SIN(N*FLOAT(ANGLE)*PI/180.0)+VOV
1200  CONTINUE
      INCUR=(VOV**2)/R
      WRITE(7,50)ANGLE,VOV
50    FORMAT(5X,'ANGLE=',I3,'°',5X,
      'OUTPUT VOLTAGE=',F12.8,'VOLTS')
      WRITE(8,60)ANGLE,INCUR
60    FORMAT(5X,'ANGLE=',I3,'°',5X,'INPUT  CURRENT=',F12.8,'A')
1100  CONTINUE
      STOP
      END
```

PROGRAM-4

PROGRAM TO INVESTIGATE THE PERFORMANCE OF MODIFIED SINUSOIDAL PULSE WIDTH MODULATION.

```
      DIMENSIONC(25),CN(100),Y(90),X(90),ALFA(25),ALFAD(25),
     CAN(100),BN(100),SL(25)
      INTEGER ANGLE,NM
      REAL INCUR
      OPEN(5,FILE='HCOEFF4.DAT')
      OPEN(6,FILE='OPVCT4.DAT')
      OPEN(7,FILE='INCURCT4.DAT')
      WRITE(*,*)'How many No.of pulses in the first 60 degrees ?'
      READ(*,*) NP
      WRITE(*,*) 'Does Modulation index less than 1 ?'
      READ(*,*) AMF
      WRITE(*,*) 'Is highest desired harmonic component less than
     C100?'
      READ(*,*) NM
      PI=3.141592
      R=1
      NS=2*NP
      TOL=.0001
      DO 100 M=1,NS
      SL(M)=((-1)**M)*(3*(NS+1)/PI)
  100  CONTINUE
      DO 200 M=1,NS,2
      C(M)=M+1
  200  CONTINUE
      DO 300 M=2,NS,2
      C(M)=-M
  300  CONTINUE
      NAT=2*NS+2
      Y(1)=AMF
      X(1)=PI/2.0
      DO 400 M=1,NS
      DO 500 I=1,90
      K=I+1
      X(K)=(Y(I)-C(M))/SL(M)
      Y(K)=AMF*SIN(X(K))
      XX=ABS(X(K)-X(K-1))
      IF (XX.LT.TOL) GOTO 600
  500  CONTINUE
```

```
600   ALFA(M)=X(I)
400   CONTINUE
      ALFA(NS+1)=PI/3.0
      ALFA(NS+2)=2.0*PI/3.0
      NAS=NS+1
      DO 700 M=NAS,NAT
      J=NAT-M+1
      ALFA(M)=PI-ALFA(J)
700   CONTINUE
      DO 800 M=1,NAT
      ALFAD(M)=ALFA(M)*180.0/PI
800   CONTINUE
      VS=1.0
      DO 900 N=1,NM
      A=0
      B=0
      DO 1000 M=1,NAT,2
      A=SIN(N*ALFA(M+1))-SIN(N*ALFA(M))+A
      B=COS(N*ALFA(M))-COS(N*ALFA(M+1))+B
1000  CONTINUE
      AN(N)=((2*VS)/(N*PI))*A
      BN(N)=((2*VS)/(N*PI))*B
      CN(N)=SQRT(AN(N)**2+BN(N)**2)
900   CONTINUE
      DO 1050 N=1,NM,2
      WRITE(5,10)N,CN(N)
10    FORMAT(5X,'CN(',I2,')='F14.8)
1050  CONTINUE
      DO 1100 ANGLE=0,360
      VOV=0
      INCUR=0
      DO 1200 N=1,NM,2
      VOV=AN(N)*COS(N*FLOAT(ANGLE)*PI/180.0)+BN(N)
     C*SIN(N*FLOAT(ANGLE)*PI/180.0)+VOV
1200  CONTINUE
      INCUR=(VOV**2)/R
      WRITE(6,20)ANGLE,VOV
20    FORMAT(5X,'ANGLE=',I3,'°',5X,
     C'OUTPUT VOLTAGE=',F12.8,'VOLTS')
      WRITE(7,30)ANGLE,INCUR
30    FORMAT(5X,'ANGLE=',I3,'°',5X,'INPUT  CURRENT=',F12.8,'A')
1100  CONTINUE
      STOP
      END
```

APPENDIX-2

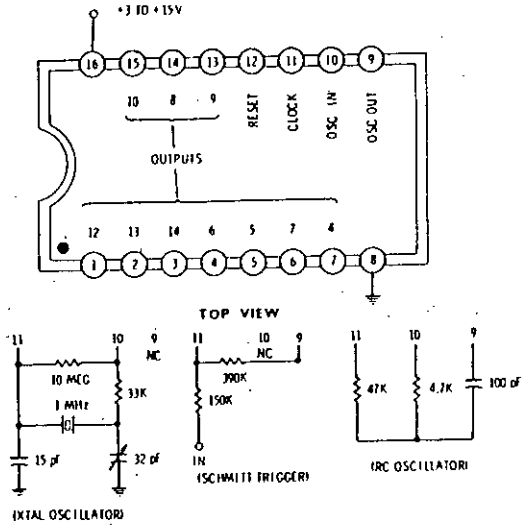
TECHNICAL SPECIFICATION OF IC 4060

IC 4060 is a binary ripple counter that counts in the up direction using positive logic. Feedback available at the clock input allows input conditioning or use of a self contained crystal or resistor-capacitor oscillator.

The reset input is normally held at ground. Each time the clock changes from to ground, the counter advances one count. The 14 output divides the input clock by 2 = 16,384. No outputs are available for divisions of 2,4, and 2048.

The crystal oscillator, schmitt trigger, and RC oscillator connections are shown in the circuit above. When used as a divider only, the clock input must be bounceless and noise free, and have rise and fall times faster than 5 microseconds.

Power supply current is 0.4 milliampere at 5 volts and 0.8 milliampere at 10 volts for a 1 megahertz clocking rate. An extra 2 milliamperes is needed if the is used in an astable or crystal mode. Maximum clock frequency is 1.75 megahertz at 5 volts and 4 mega hertz at 10 volts.



TECHNICAL SPECIFICATION OF **IC 4013**

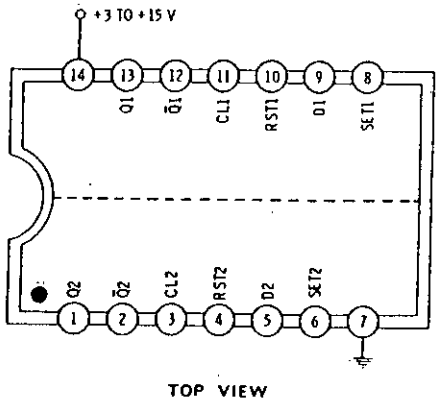
There are two flip-folp in IC 4013 and each flip-flop can be used independently. There are two modes, clocked and direct.

In the clocked mode, the direct set and reset inputs must remain at ground. The input to the ***D*** line decides what the flip-flop is going to do. The actual operation doesn't happen until the positive edge (ground to positive transition) of the clock.

If ***D*** is positive, clocking makes the Q output positive and Q grounded. If D is grounded, clocking makes the Q output grounded and $\bar{Q}$ positive.

87074

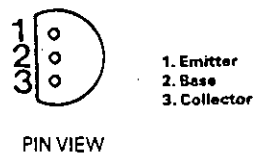
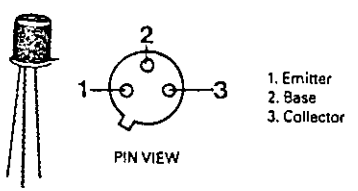
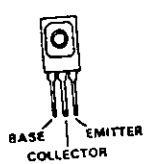
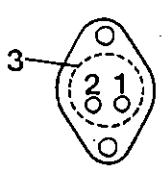
Each flip-flop may be made to binary-divide by cross coupling the Q output to the D input.



TOP VIEW

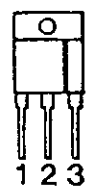
Maximum clock frequency is 10 megahertz at 10 volts and 4 megahertz at 5 volts. Total package current at a 1-MHZ clock frequency is 0.8 milliampere at 5 volts and 1.6 milliamperes at 10 volts.

SPECIFICATIONS

TRANSISTOR							
Type	Ic(max)	PD(max)	hfe(min - max) @	Ic	VCE	ft (typical)	Pinout
BC 556 PNP Small signal	-100 ma	625 mw	125-500	-2 ma	5 V	280 MHz	
BC 107 NPN Small signal	100 ma	300 mw	110-450	2 ma	5 V	300 MHz	
BD 132 PNP Power Transistor Low voltage	-3.0 A	15 w	20 (min)	-2.0 A	-1 V	60 MHz	
2N3055H NPN Power Transistor Low voltage	15.0 A	115 w	20 - 70	4.0 A	4 V	800 KHz	

SPECIFICATIONS

MOSFET

	ID(max)	PD(max)	VGS(max)	
N Channel, Power VN66AF Low voltage	1.46 A	15 w	2.5 V	 1 2 3 PIN VIEW 1. Source 2. Gate 3. Drain (tab)

SILICON RECTIFIER

Type	Voltage	Current	
1N4001	50 V	1 A	
1N4002	100 V	1 A	

SPECIFICATIONS

ZENER DIODE

Type	Power	Voltage	
BZX79	500 mw	5.1 V	
BZX85	1.3 mw	16 V	

OP - AMP

Type	Total supply voltage		Supply current	
	min (V)	max (V)	(ma)	
741C	10	36	2-8