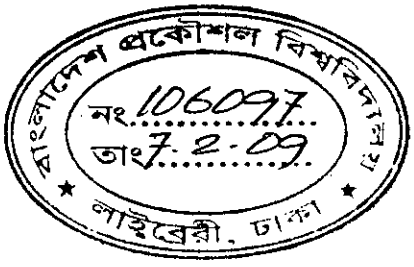
ANALYTICAL MODELING OF INVERSION CARRIER EFFECTIVE MOBILITY FOR DRAIN CURRENT OF NANOSCALE MOSFET



A thesis submitted to

the Department of Electrical and Electronic Engineering

of

Bangladesh University of Engineering and Technology

in partial fulfillment of the requirements

for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

by

E. J. Zinat Mahol Sathi

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY

This thesis titled "ANALYTICAL MODELING OF INVERSION CARRIER EFFECTIVE MOBILITY FOR DRAIN CURRENT OF NANOSCALE MOSFET" submitted by E J Zinat Mahol Sathi, Roll No: 040506234 P, Session: April/2005 has been accepted as satisfactory in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on December 31,2008.

Board of Examiners

1. _____ Chairman (Supervisor)

Dr. Quazi Deen Mohd Khosru
Professor,
Department of EEE,
BUET, Dhaka.

2. _____ 31/12/08 Member (Ex-Officio)

Dr. Aminul Hoque
Professor and Head,
Department of EEE,
BUET, Dhaka.

3. _____ 31/12/2008 Member

Dr. Md. Shafiqul Islam
Professor,
Department of EEE,
BUET, Dhaka.

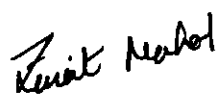
4. _____ 31.12.08 Member (External)

Dr. Md. Ashraful Hoque
Professor,
Department of EEE,
IUT, Dhaka.

Declaration

I hereby declare that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

Signature of the candidate



E J Zinat Mahol Sathi

Contents

List of Figures (vi)

List of Symbols (viii)

Acknowledgement (x)

Abstract (xi)

Chapter 1

Introduction

1.1 Literature Review 1

1.2 Scaling Devices to Their Limits 4

1.3 Objectives 5

1.4 Outline of the Thesis 5

Chapter 2

Basic MOSFET Theory

2.1 Introduction 7

2.2 Device Structure 8

2.3 Energy Band Diagram 9

2.4 Electric Fields in MOSFET 10

2.5 MOSFET Operation 10

2.6 I-V Characteristics of MOSFET 12

Chapter 3

Essential Physics of Carrier Transport in Nanoscale MOSFETs

3.1 Introduction 15

3.2 Scattering Theory 15

3.3 Mobility 17

3.3.1 Factors Influencing Mobility 18

3.3.2 Mobility and Velocity Saturation 19

3.4 Effective Electric Field calculation 19

3.5 Scattering Mechanisms 20

3.5.1 Phonon Scattering 21

3.5.2 Surface Roughness Scattering 23

3.5.3 Coulomb Scattering 23

3.6 Effective Mobility 25

3.7 Mobility Reduction in Nanoscale MOSFETs 25

Chapter 4

Results for Nanoscale MOSFETs

4.1 Test Device 27

4.2 Inversion Layer Carrier Concentration 28

4.3 Threshold Voltage Roll-off 30

4.4 Mobility Due to Phonon Scattering 33

4.5 Mobility Due to Surface Roughness Scattering 35

4.6 Mobility Due to Coulomb Scattering 36

4.7 Effective Mobility 38

4.8 Current-Voltage Characteristics

4.8.1 Transfer Characteristics 45

4.8.1.1 Effect of Drain Voltage 49

4.8.1.2 Effect of Channel Length 50

4.8.1.3 Effect of Oxide Thickness 51

4.8.2 Output Characteristics 52

4.8.2.1 Effect of Gate Voltage 55

4.8.2.2 Effect of Channel Length 57

4.8.2.3 Effect of Oxide Thickness 59

Chapter 5

Conclusions

5.1 Summary 61

5.2 Recommendations for Future Works 63

List of References 65

List of Figures

Figure	Page
Fig. 1.1 Evolution of the past and expected gate dimension of silicon Transistor (Moore's law)	1
Fig. 2.1 Physical structure of an n-channel enhancement type MOSFET	8
Fig. 2.2 Energy band diagram of MOSFET at thermal equilibrium	9
Fig. 2.4 MOSFET operated in the linear region	13
Fig. 3.1 Schematic representation of a nanoscale MOSFET according to scattering theory	16
Fig. 4.1 Test device of an n-channel enhancement type MOSFET	27
Fig. 4.2 Carrier concentration in inversion layer as a function of gate voltage	29
Fig. 4.3 Inversion carrier concentration versus effective electric field	30
Fig. 4.4 Decrease in threshold voltage (ΔV_{th}) with the channel length	32
Fig. 4.5 Threshold voltage roll-off of MOSFET for nanoscale channel length	33
Fig. 4.6 Mobility due to phonon scattering versus effective field	34
Fig. 4.7 Mobility limited by phonon scattering as a function of temperature	35
Fig. 4.8 Mobility due to surface roughness scattering versus effective electric field	36
Fig. 4.9 Mobility due to Coulomb scattering versus inversion carrier concentration	37
Fig. 4.10 Mobility due to Coulomb scattering versus effective electric field	38
Fig. 4.11 Effective mobility in nanoscale MOSFETs	40
Fig. 4.12 Effective mobility versus channel length	41
Fig. 4.13 Effective mobility versus effective electric field for different channel lengths	42

Fig. 4.14 Mobility versus effective electric field as a function of gate voltage 43

Fig. 4.15 Mobility versus effective electric field as a function of drain voltage 44

Fig. 4.16 Effective mobility as a function of gate voltage at a constant drain voltage 46

Fig. 4.17 Subthreshold drain current 47

Fig. 4.18 Drain current versus gate voltage 48

Fig. 4.19 Drain current versus gate voltage in semi log scale 49

Fig. 4.20 Effect of drain voltage on drain current versus gate voltage 50

Fig. 4.21 Drain current versus gate voltage for different channel lengths 51

Fig. 4.22 Drain current versus gate voltage at different oxide thickness 52

Fig. 4.23 Effective mobility as a function of drain voltage 53

Fig. 4.24 Drain current versus drain voltage 54

Fig. 4.25 Drain current versus drain voltage in semi log scale 55

Fig. 4.26 Effect of gate voltage on output characteristics 56

Fig. 4.27 Locus of saturation from the output characteristics 57

Fig. 4.28 Effect of channel length on the output characteristics 58

Fig. 4.29 Saturation drain current versus channel length 59

Fig. 4.30 Effect of oxide thickness on the output characteristics 60

List of Symbols

Symbols	Abbreviations
V_{Th}	Threshold voltage
V_{FB}	Flat-band voltage
N_a	Acceptor carrier concentration
n_i	Intrinsic carrier concentration
k	Boltzmann's constant
q	Charge of electron
T	Temperature in Kelvin
ψ_B	Bulk Fermi energy
E_F	Fermi level energy
E_i	Intrinsic Fermi level energy
$q\varphi s$	Work function of a semiconductor
$q\varphi_m$	Work function of metal
$q\chi$	Electron affinity
L_{ch}	Channel length
W	Width of the channel
μ_{eff}	Effective mobility
X_d	Depletion layer thickness
d	Oxide thickness
l	Critical length
τ_c	Mean free time
m_n	Effective mass
ε_{Si}	Permittivity of Si
N_{dpl}	Surface depletion carrier concentration

Symbols	Abbreviations
N_s	Surface inversion carrier concentration
r	Backscattering parameter
Eeff	Effective electric field
μ_{ph}	Mobility due to phonon scattering
μ_{sr}	Mobility due to surface roughness scattering
μ_c	Mobility due to Coulomb scattering
vth	Average thermal velocity
rj	Source/drain junction depth

Acknowledgements

At first, I want to express my gratefulness to Almighty Allah for giving me this opportunity to complete my research work and my thesis.

I am deeply indebted to my thesis supervisor Professor Dr. Quazi Deen Mohd Khosru for his help and advice through the course of my M.Sc study. Without his encouragement and support this work would not have been made possible. He spent a lot of his time for this work. He is a remarkable individual and I have truly benefited from the experience of working with him.

I am grateful to Professor Dr. Aminul Hoque, Head of the department of Electrical and Electronic Engineering of BUET for his all support and contribution during my M.Sc. study. He has given me the opportunity to use the BUET library and all other facilities, as I required to complete my research work. I am also grateful to all the teachers and all technical staffs of BUET.

There are many others at DUET who have influenced me in completing this research. As a lecturer of DUET, I would like to thank Professor Dr. Md. Shaheen Hasan Chowdhury, Head of the department of Electrical and Electronic Engineering, DUET for giving me the permission to continue my study at BUET. I am thankful to him for his valuable suggestions and inspiration to complete this work.

It is my pleasure to acknowledge Professors Dr. Aminul Hoque, Dr. Md. Shafiqul Islam and Dr. Md. Ashraful Hoque for being present on my examination committee and giving me valuable guidance and insightful suggestions to further improve the work.

Specially, I am deeply indebted to my family for their supports during the time.

Abstract

Critical transistor dimensions scale below the 100 nm regime, where quantum mechanical analysis is more appropriate than the semi-classical approach to model the device parameters. Simulation tools, which can be applied to design nanoscale transistors in the future, require new theory and modeling techniques that capture the physics of carrier transport accurately and efficiently. Quantum analysis needs rigorous calculation and it is time consuming. This thesis outlines an easy approach to model carrier transport in nanoscale transistors which is in between semi-classical and quantum mechanical analysis. The semi-classical expressions are modified so that the evaluated results are consistent with that derived quantum mechanically. In this work, carrier scattering in the inversion channel has been described in terms of mobility. A simple model of the effective mobility of MOSFET is proposed taking into account the carrier scattering mechanisms. Current-voltage characteristics are obtained using the effective mobility. The model shows good agreement with the simulation and experimental results for nanoscale MOSFETs.

Chapter 1

Introduction

1.1 Literature Review

CMOS technology has been proven as one of the most important achievements in modern engineering history [1]. It has been possible due to the exponential downscaling of MOS devices over the last 30 years. The minimum dimension of a single device for present day technology is about 100 nm in gate-length [1]. Continued success in device scaling is necessary for further development of the semiconductor industry in the years to come. According to the ITRS roadmap, the MPU physical gate length will be scaled down as small as 15 nm by the year 2009 as shown in Fig 1.1 [2,3].

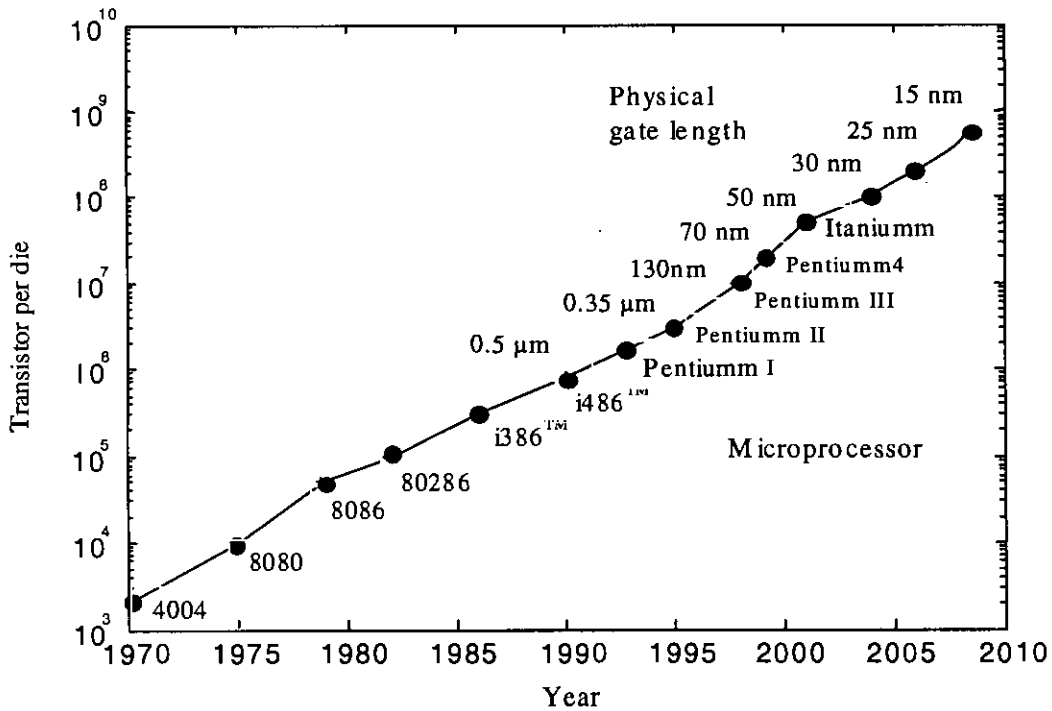


Fig. 1.1: Evolution of the past and expected gate dimension of silicon Transistor (Moore's law).

As the device feature size enters into the nanoscale, the modeling and simulation of carrier transport in MOS devices become challenging. MOSFET technologies under development have channel lengths well below 100 nm where near-ballistic operation becomes feasible. But device development and circuit simulation continue to be based on traditional MOSFET models whose physical basis is losing validity as channel lengths shrink below 100 nm [4]. As traditional MOS scaling methods become less effective, nanoscale device modeling is needed to provide innovative new MOS devices as well as to understand the limits of the scaling process. Modeling provides insight into the operation of modern semiconductor devices and circuits, and simulation dramatically reduces the development costs and time-to-market. Modeling is also needed to explore new device structures that may operate on principles different than those currently used. In practice, MOSFETs operate below the ballistic limit because carriers scatter within the device [5]. Mobility is an important parameter for carrier transport because it describes how strongly the motion of an electron is influenced by an applied electric field. Mobility is directly related to the mean free time between collisions, which in turn is determined by the various scattering mechanisms.

The MOSFET characteristics in previous models were expressed in terms of scattering parameters rather than mobility. MOSFET characteristics in presence of scattering were described in terms of channel transmission coefficient [5] by Lundstrom. The channel transmission coefficient was expressed in T, where $T < 1$ in the presence of scattering. Comparisons with experiment showed that T is bias dependent. At low drain bias, $T = 0.1$ for $L >> 100$ nm n-channel MOSFET, ($T = 0.05$ for a p-MOSFET) while at high drain bias, $T = 0$ for an n-MOSFET ($T = 0.5$ for a p-MOSFET). Computing T rigorously is a difficult problem that requires detailed numerical simulations. Lundstrom measured T in terms of mean-free-path, λ. According to him, two types of mean-free-path are present in MOSFET which are: the very short mean-free-path near the drain and the relatively long mean-free-path near the source. Because scattering rates generally increase with energy, the question of what mean-free-path is to use arised. Lundstrom saw that scattering in the low field region near the source controls the on-current, so the mean-free-path near the source was used in his work. According to him, carriers near the source gain little kinetic

energy from the channel electric field and the mean-free-path is close to its near-equilibrium value. The near-equilibrium mobility in a bulk semiconductor is related to the near-equilibrium mean-free-path. The mobility measured in a long channel MOSFET was used as a measure of the near-equilibrium mean-free-path for short channel device. But the short channel mobility is not the same as that of a long channel MOSFET. Because, mobility is measured in terms of the scattering mechanisms which are strongly dependent on the channel length. Moreover, Lundstrom has mentioned no process to measure the mobility for the derivation of mean-free-path.

Nanoscale MOSFET theory based on scattering was described by Anisur Rahman et al. [4] in terms of channel backscattering coefficient, r. According to his scattering theory, backscattering from the channel was determined only by a region of short length, l at the beginning of the channel [4]. l is the distance from the top of the barrier to the point where potential drops by kT/q volts. The channel backscattering coefficient was determined from l by the momentum relaxation length, λ in this low field kT layer. It was found by momentum relaxation time. The momentum relaxation time was calculated from low field mobility at the beginning of the channel and unidirectional thermal velocity. For the analysis of I-V characteristics, constant low field mobility (120 cm^2/V-s) was assumed throughout the model. The current-voltage (I-V) characteristics were expressed in terms of a backscattering parameter, r by Lundstrom [6]. It was stated that the concept of mobility continues to have relevance to ultrashort-channel MOSFETs as a measure of channel backscattering. It was said that the backscattering parameter can be estimated from the low field mobility. But how to measure the mobility was not described and no expression for mobility was given in both works [4,6]. No relationship was given between the mobility and the channel length. Also, the functional dependence on device parameters and terminal voltages of the backscattering parameter were not specified.

Mobility was modeled for long channel MOSFETs by Takagi et al. [7,8] considering different scattering mechanisms. They have given expressions for the mobility due to phonon scattering and surface roughness scattering. Then they found the total mobility

for this two scattering mechanisms. The Coulomb scattering was derived by subtracting the total mobility from the universal mobility curve. The mobility model mainly emphasizes on the substrate impurity concentration and on temperature. No relationship was developed with the channel length of the device.

1.2 Scaling Devices to Their Limits

There are two primary device structures that have being widely studied and used in CMOS technology. One is the bulk structure, where a transistor is directly fabricated on the semiconductor substrate. The other one is called SOI (silicon-on-insulator), where a transistor is built on a thin silicon layer, which is separated from the substrate by a layer of insulator. The bulk structure is relatively simple from a device process point of view, and it is still the standard structure in almost all CMOS based products until this day [1].

Regarding conventional silicon MOSFETs, the device size is scaled in all dimensions, resulting in smaller oxide thickness, junction depth, channel length, channel width, and isolation spacing. Currently, 90 nm (with a physical gate length of 50 nm) is the state-of-the-art process technology, but even smaller dimensions are expected in the near future [9]. Device miniaturization results in reduced unit cost per circuit function. As device dimensions decrease, the intrinsic switching time decreases. Higher speeds lead to expanded IC functional throughput rates. As devices become smaller, they also consume less power. Therefore, device miniaturization also reduces the energy used for each switching operation. The energy dissipated per logic gate has decreased by over one million times since 1959 [9].

For device scaling, it is basically tried to balance two things: device functionality and device reliability. Both of them have to be maintained at a smaller dimensional size [1]. To accomplish this, we need to suppress any dimension related effects or short channel effects (SCEs) as much as possible. SCEs include threshold voltage (V_{Th}) variations versus channel length, typically V_{Th} rolloff at shorter channel lengths. When the device channel length is reduced, carrier scattering mechanisms are no longer negligible.

Mobility is a measure of scattering phenomenon. Mobility for various scattering mechanisms can be modeled in terms of effective electric field. The effective mobility depends on the channel length of the device. Mobility degrades for shorter channel lengths. The mobility model developed for long channel MOSFET cannot effectively measure the mobility when the device channel length enters into the nanoscale region. The mobility for long channel length is called *ballistic mobility,* and for nanoscale channel length, the mobility is called *effective mobility*. In this work, by means of using semi-classical expressions, effective mobility has been calculated from the ballistic mobility. The effective mobility is related to the channel length of MOSFETs.

1.3 Objectives

The aim of this work is to model the exact influence of scattering in the inversion layer of nanoscale MOSFETs in terms of mobility. Mobility will be modeled for three types of scattering: phonon scattering, surface roughness scattering and Coulomb scattering. Effective mobility then will be derived from these mechanisms incorporating the effect of channel length. The current-voltage characteristics of MOSFET will be obtained by using the effective mobility model. The developed model will be applied to determine various parameters of nanoscale MOSFETs for the full range of gate voltage and drain voltage covering subthreshold, linear and saturation regions of operation. The results will be compared with the available experimental and simulation data.

The principal objectives of this work are: an implementation of appropriate physics and methodology in mobility modeling of nanoscale MOSFETs for various scattering mechanisms; examination and assessment of current-voltage characteristics incorporating the effective mobility.

1.4 Outline of the Thesis

Nanoscale device physics and its current-volatge characteristics are described in this work. Specially mobility in the channel inversion layer of MOSFET has been modeled to

obtain its current-volatge characteristics. Carrier transport in the inversion channel is dominated by different scattering mechanisms. The carrier scattering can be determined in terms of inversion layer mobility. For long channel devices, the scattering is ignored in developing the current-voltage characteristics and mobility is considered constant. But for nanoscale device, carrier scattering takes an important part in developing the drain current. Mobility is calculated to obtain the *I-V* characteristics of nanoscale MOSFETs. In this work, mobility has been measured in terms of different scattering mechanisms, namely the phonon scattering, surface roughness scattering and Coulomb scattering. For this, several works that were done on mobility has been considered [7-9]. Mobility due to each scattering phenomenon has been derived in terms of effective electric field. In order to determine the effective electric field in the MOSFET channel, the inversion layer charge density and the depletion layer charge density has been calculated by using semi-classical expressions. Respective curves of mobility have been plotted for a test device with different channel lengths in the nanoscale region. The plotted curves have been verified with the available curves obtained from simulation results [10]. The drain current has been calculated incorporating the mobility model for different operating regions of MOSFETs of different channel lengths. The results thus obtained have been compared with the reported simulation [10] as well as experimental data [11].

This paper is organized as follows. Basic MOSFET theory is described in chapter 2. Chapter 3 presents a full range analytic compact model for nanoscale MOSFETs according to scattering theory. The mobility in the inversion channel based on the carrier transport phenomenon is modeled for various scattering mechanisms. In chapter 4, a brief description of the model device parameters used in this work are described. The *I-V* characteristics of nanoscale MOSFETs for different channel length, oxide thickness and bias voltage are plotted. The results are discussed and compared with device simulation and numerical data. Chapter 5 contains summary and conclusions of this work and suggests possible areas for further investigation.

Chapter 2

Basic MOSFET Theory

2.1 Introduction

A field effect transistor (FET) operates as a conducting semiconductor channel with two ohmic contacts – the source and the drain – where the number of charge carriers in the channel is controlled by a third contact – the gate. The most important FET is the MOSFET (metal-oxide-semiconductor field-effect transistor). The MOSFET is composed of an MOS diode and two p-n junctions placed adjacent to the MOS diode. In a silicon MOSFET, the gate contact is separated from the channel by an insulating silicon dioxide (SiO_2) layer. In the MOSFET, an inversion layer at the semiconductor–oxide interface acts as a conducting channel. If the conducting channel is induced by the gate, the device is called enhancement type MOSFET. On the other hand if the conducting channel is diffused during fabrication it is called depletion type MOSFET. The MOSFET is composed of a channel of n-type or p-type semiconductor material and is accordingly called an n-channel MOSFET or a p-channel MOSFET. In an n-channel MOSFET, the substrate is p-type silicon and the inversion charge consists of electrons that form a conducting channel between the n^+ ohmic source and the drain contacts. In this chapter an overview of n-channel enhancement type MOSFET physics and operation is presented.

2.2 Device Structure

The physical structure of an n-channel enhancement type MOSFET is shown in Fig. 2.1. The transistor is fabricated on a p-type substrate, which is a single crystal silicon wafer. Two heavily doped n-type regions, the n^+ source and the n^+ drain are created in the substrate. A thin layer of silicon dioxide (SiO_2) is grown on the surface of the substrate that acts as an insulator. The metal plate (heavily doped polysilicon is commonly used instead of metal) on the oxide layer is called the gate.

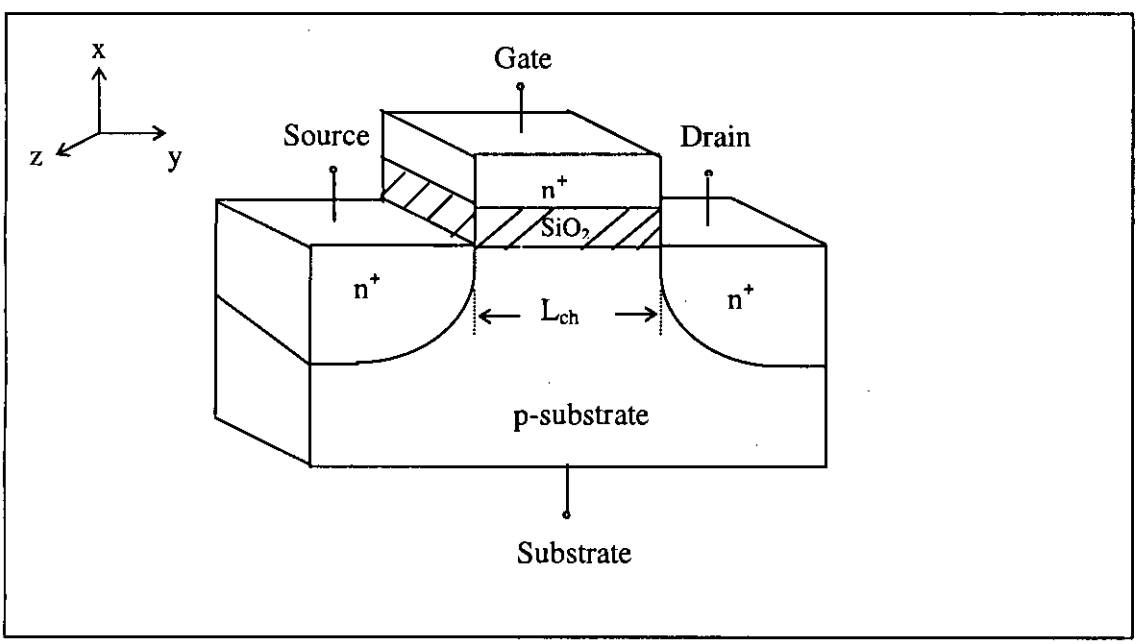


Fig. 2.1: Physical structure of an n-channel enhancement type MOSFET.

As described above for the MOS capacitor, inversion charge can be induced in the channel by applying a suitable gate voltage relative to other terminals. When positive voltage is applied to the gate of n-channel MOSFET, positive charges are accumulated on the gate metal and the negative charges are induced in the underlying Si-substrate, forming a depletion region consisting a thin sheet of mobile electrons. Concentration of the electrons in the channel can be changed by the variation of gate voltage. The onset of strong inversion is defined in terms of a threshold voltage, V_{Th} being applied to the gate electrode relative to the other terminals. In order to assure that the induced inversion

channel extends all the way from source to drain, it is essential that the MOSFET gate structure either overlaps slightly or aligns with the edges of these contacts (the latter is achieved by a self-aligned process). Self-alignment is preferable since it minimizes the parasitic gate-source and gate-drain capacitances.

2.3 Energy Band Diagram

The energy band diagram of an ideal MOS diode at zero applied voltage is shown in Fig.2.2. The work function of a semiconductor is $q\varphi s$, which is the energy difference between the vacuum level and the Fermi level, E_F. The work function of metal is $q\varphi_m$ and the work function difference is $q\varphi_{mS} = q\varphi_m - q\varphi_S$. The electron affinity $q\chi$ is defined as the energy difference between the conduction band edge, E_C and the vacuum level in the semiconductor and $q\psi_B$ is the energy difference between the Fermi level, E_F and the intrinsic Fermi level, E_i. At thermal equilibrium, the Fermi level must be constant and vacuum level must be continuous in the MOS diode. To accommodate the work function difference, the semiconductor bands bend downward.

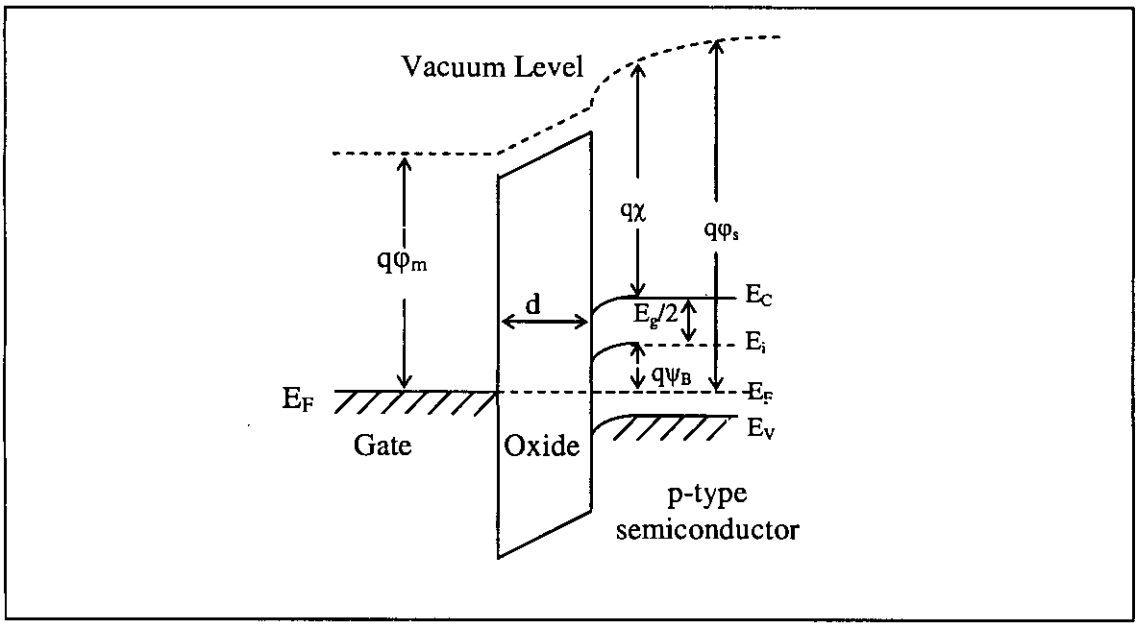


Fig. 2.2: Energy band diagram of MOSFET at thermal equilibrium.

The band bending can be compensated by applying a voltage across the gate and the substrate equals to the work function difference $q\varphi_{ms}$. This voltage is called the *flat-band voltage*, V_{FB} and is given by [12].

$$V_{FB} = q\phi_m - \left(q\chi + \frac{E_g}{2} + q\psi_B \right) \tag{2.1}$$

Here, ψ_B is the bulk Fermi energy, given by the following expression [12].

$$\psi_B = \frac{2kT}{q} \ln\left(\frac{Na}{n_i} \right) \tag{2.2}$$

Where, N_a is the acceptor concentration, n_i is the intrinsic carrier concentration, k is the Boltzmann's constant, q is the charge of electron and T is temperature in Kelvin.

2.4 Electric Fields in MOSFET

Two distinct electric field distributions exist in the MOSFET structure. The *transverse field* which is caused by the potential difference between the conductive gate and the substrate. This field supports the substrate depletion region and inversion layer. The *lateral field* which arises due to a non- zero source to drain potential. This is the main mechanism for current flow in the MOSFET.

2.5 MOSFET Operation

When the flat band voltage, V_{FB} is applied to the gate, the energy bands become flat and no charge is induced in the channel. For n-channel MOSFET at the flat-band condition, the concentration of holes at the insulator-semiconductor interface becomes equal to the equilibrium concentration of holes in the p-type semiconductor. When a positive bias (larger than V_{FB}) is applied to the gate of MOS diode, the energy bands near the semiconductor surface are bent downward and the majority carriers (holes) are depleted

at the insulator-semiconductor interface. This is called the *depletion* case. When a larger positive voltage is applied, the energy bands bend downward even more so that the intrinsic level E_i at the surface crosses the Fermi level. The number of minority carriers (electrons) at the surface becomes greater than majority carriers (holes) and the surface is thus inverted. This is called the *inversion* case. Initially the surface is in weak inversion as the concentration of electron is small. The concentration of electron increases exponentially with the increase of band bending. The inversion is called *strong inversion* when electron concentration near the insulator-semiconductor interface becomes equal to the substrate doping level. At the onset of strong inversion, the surface potential ψ_S is given by [12]:

$$\psi_S = 2\psi_B = 2\frac{kT}{q}\ln\frac{Na}{n_i} \tag{2.3}$$

The minimum gate voltage required to create strong inversion is called *threshold voltage*, V_{Th}. When a drain-source bias V_D is applied to an n-channel MOSFET in the above threshold conducting state, electrons move in the channel inversion layer from source to drain. A change in the gate-source voltage V_G alters the electron sheet density in the channel, modulating the channel conductance and the device current. The substrate contact can be at the reference voltage or reverse biased with respect to the source.

After the inversion channel is formed, if a small drain voltage is applied, electrons will flow from the source to the drain through the conducting channel. The current flows from the drain to the source. This current is proportional to the drain to source voltage. This region of MOSFET operation is called *linear region*. When the drain voltage is increased, eventually it reaches to a point at which the inversion layer density becomes very small (essentially zero) at the drain end. This is termed as the *pinch-off* point, which leads to a saturation of the drain current, I_D. The corresponding drain-source voltage, $V_D = V_{Dsat}$, is called the *saturation voltage*. This region is called *saturation region* of operation.

2.6 I-V Characteristics of MOSFET

After the inversion layer is formed by applying gate voltage, if drain voltage is applied, the charges in the inversion layer start to flow from the source to the drain. Current flows from the drain to the source through the channel. The MOSFET is operated in three regions: *subthreshold*, *linear* and *saturation* regions, depending on the value of bias voltage.

When the gate voltage is below the threshold voltage, the semiconductor surface is weakly inverted. According to the basic threshold model, the transistor is turned off, and there is no conduction between drain and source. In reality, the Boltzmann distribution of electron energies allows some of the more energetic electrons at the source to enter the channel and flow to the drain, resulting in a subthreshold current that is an exponential function of gate–source voltage. While the current between drain and source should ideally be zero when the transistor is being used as a turned-off switch, there is a weak-inversion current, called *subthreshold* current. This region of MOSFET operation for $V_G < V_{Th}$ is called *subthreshold* region.

In weak inversion, the current varies exponentially with gate-to-source bias V_G. In sub-threshold region, drain current is dominated by diffusion instead of drift. The sub-threshold current flowing through a transistor is given by [13].

$$I_{sub} = \frac{W}{L_{ch}} \mu_{eff} \sqrt{\frac{q\varepsilon_{Si} N_a}{2\psi_s}} v_{th}^{\,2} \exp\left(\frac{V_G - V_{th}}{m v_{th}}\right)\left(1 - \exp\left(\frac{-V_D}{v_{th}}\right)\right) \tag{2.4}$$

Where, L_{ch} is the channel length, W is the width of the channel, μ_{eff} is the effective mobility in the inversion layer. m is the body effect coefficient related to the sub-threshold swing. The body effect coefficient, m is given by [13].

$$m = 1 + \frac{3d}{X_d} \tag{2.5}$$

Here, X_d is the depletion layer thickness and d is the oxide thickness. MOSFET is operated in the *subthreshold* region when it is used as a switch or as a memory device.

When gate voltage is larger than the threshold voltage the channel acts as a resistor. The drain current is proportional to the drain voltage. This is called the *linear* region of operation as shown in Fig. 2.3.

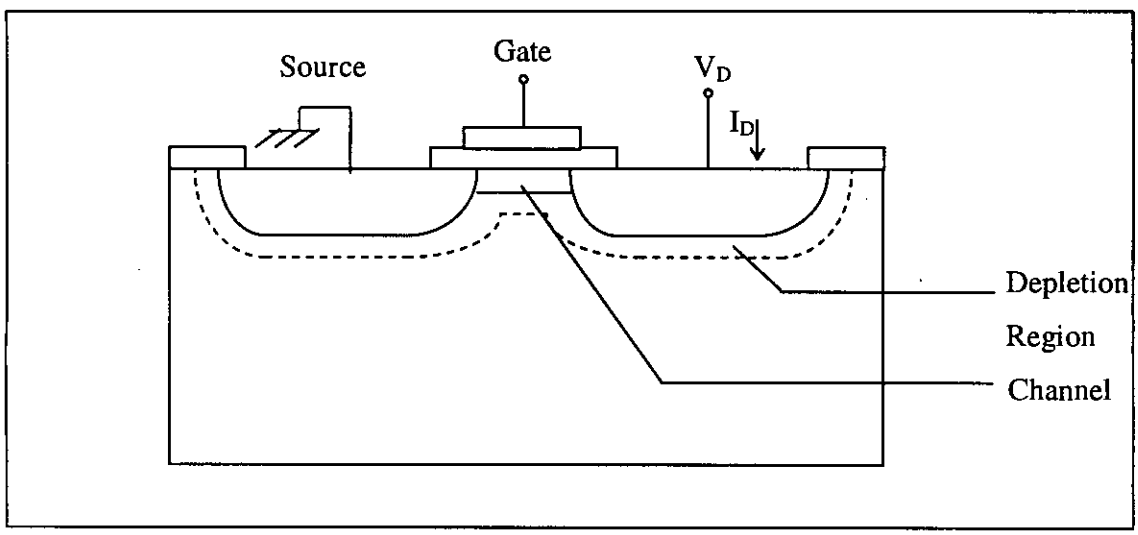


Fig. 2.3: MOSFET operated in the linear region.

In linear region, the drain current can be determined as [12].

$$I_D = \frac{W}{L_{ch}} \mu_{eff} C_o \left\{ (V_G - V_{th}) \times V_D - \frac{V_D^2}{2} \right\} \tag{2.6}$$

Where, μ_{eff} is effective mobility, determined by the carrier scattering mechanisms. The process of μ_{eff} calculation is described in the next chapter.

When the drain voltage is increased, after the inversion channel has been created, current starts to flow between the drain and source. Since the drain voltage is higher than the gate voltage, the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from

the interface and deeper in the substrate. The onset of this region is also known as *pinch-off* to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage. Then the pinch-off occurs. The drain current reaches to its saturation value. At this point, the drain voltage is called *saturation voltage* and the operating region is called *saturation* region. These values can be found by the following equations [12].

$$I_{DSat} = \frac{W}{2L}\mu_{eff} C_o \left(V_G - V_{th}\right)^2 \tag{2.7}$$

$$V_{Dsat} = V_G - 2\psi_B + K^2\left[1 - \sqrt{1 + \frac{2V_G}{K^2}}\right] \tag{2.8}$$

Here, K is given as follows [12].

$$K = \frac{\sqrt{\varepsilon_{Si} q N_a}}{C_o} \tag{2.9}$$

Chapter 3

Essential Physics of Carrier Transport in Nanoscale MOSFETS

3.1 Introduction

In the previous section, electron transport in the ballistic limit has been discussed. In practice, MOSFETs are observed to deliver an on current that is roughly 50% of the ballistic limit [6]. Real devices operate below this limit because carriers scatter within the device [1]. Dissipative transport can be due to many reasons. Microscopically, electrons are confined within a very thin channel in a MOSFET. The channel is either sandwiched by gate insulators (in thin body SOI structures), or by gate insulators and silicon substrates (in bulk structures). In principle, the insulator surfaces can never be perfectly smooth, and semiconductor lattices are never defect free. Also, both channel carrier densities and impurity concentrations are typically very large and devices typically work at relatively high temperature. All these factors contribute to carrier scattering. The goal of this chapter is to develop an understanding of how scattering affects transistors and to develop a simple model that extends Eqn. 2.6.

3.2 Scattering Theory

According to scattering theory, carriers are injected from the source to the low field region at the beginning of the channel over the source channel potential barrier [4]. Some of the injected carriers backscatter in this low field region. The length (l) of this low field critical region is the distance over which the channel potential drops by

approximately *kT/q* (called "*kT* layer"). The carriers that cross this *kT* layer feel the high drain electric field, which acts as an absorber for the carriers.

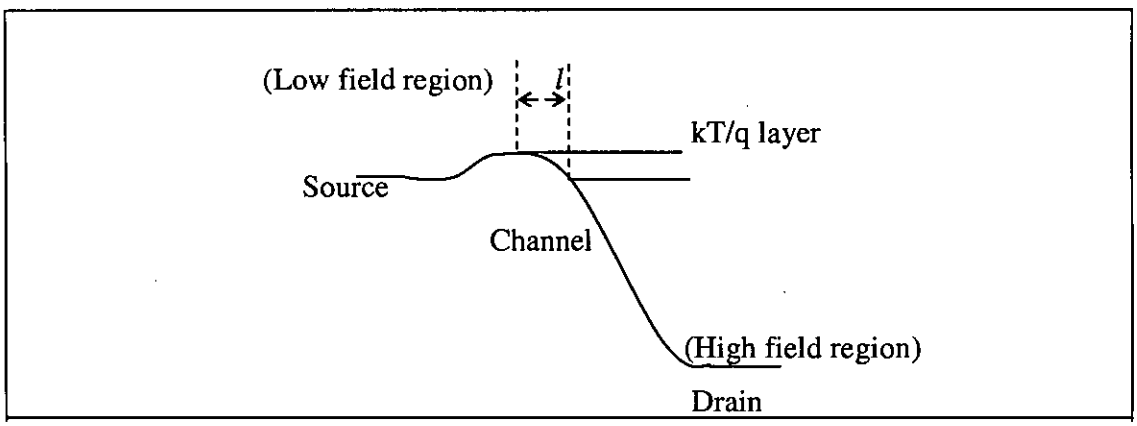


Fig. 3.1: Schematic representation of a nanoscale MOSFET according to scattering theory.

The charge at the beginning of the channel (at the top of the potential barrier) is controlled by MOS electrostatics so that the charge in the semiconductor balances that in the gate. Ren has shown that, under equilibrium conditions (V_D = 0 V) in an electrostatically well-tempered device, equilibrium, 1D MOS electrostatics apply at this point [1]. The inversion layer density can be computed as for a 1D MOS capacitor. The inversion layer density at the source end of the channel remains nearly equal to its equilibrium value even when a drain bias is applied. At low drain bias, the carrier distribution at this point assumes full-Maxwellian distribution. But when drain bias is high, the drain Fermi level is pulled down by drain bias as shown in Fig. 3.1.

For the past decade, much of the modeling and simulation work has focused on accurately describing carrier transport within the channel. Rahman et al. [4] have described carrier scattering in terms of a backscattering parameter, r. Some fraction of the carriers that are injected from the source into the channel backscatter and return to the source, while others flow out the drain and comprise the steady-state drain current. The backscattering parameter is defined as the fraction of source-injected carriers that are

backscattered. For MOSFET operated in the ballistic limit, r = 0. Backscattering from the channel was determined by the critical length, *l*, momentum relaxation time and unidirectional thermal velocity. Momentum relaxation time was calculated from low field mobility. The channel backscattering coefficient was calculated assuming mobility of 120 $cm^2/V\text{-}s$ for modeling a 20 nm DG MOSFET.

Lundstrom [6] developed a scattering theory of MOSFET in terms of a channel transmission coefficient. For modeling MOSFET with 100 nm of channel length, mobility was taken as 250 $cm^2/V\text{-}s$.

A conceptual view of the essential physics of carrier transport in nanoscale MOS transistors was presented and confirmed by numerical simulation. Key results of carrier transport in nanoscale MOSFET are:

1. the source velocity saturates and its limit is set by thermal injection,
2. the carrier density at the top of the source to channel barrier is fixed by MOS electrostatics,
3. scattering in very short region near the beginning of the channel limits the on-current.

For the drain current of MOSFET, carrier scattering was measured in terms of backscattering parameter, or channel transmission coefficient in previous models. In this work, carrier scattering is described in terms of mobility.

3.3 Mobility

Mobility (μ) is a measure of scattering, low mobility indicates a high level of scattering. The inversion layer mobility in MOSFETs has been a very important physical quantity as a parameter to describe the drain current and a probe to study the electric properties of a two-dimensional carrier system.

Mobility describes how strongly the motion of an electron is influenced by an applied electric field. When electric field is applied to the semiconductor, carriers experience a force from the field (in the opposite direction to the field) during the time between collisions. The movement of charged particles under the influence of an electric field is termed drift. Therefore an additional velocity component is superimposed upon the thermal motion of carriers. This additional component is called *drift velocity*. The drift velocity (v) is proportional to the applied electric field (E) and is given by the expression [12].

$$v = -\left(\frac{q\tau_c}{m_n}\right)E \tag{3.1}$$

Here, τ_c is the mean free time (or electron state lifetime), defined as the average time between collisions and m_n is the effective mass. The proportionality factor between the drift velocity and electric field is called *mobility* in unit $cm^2/V\text{-}s$ and is given as follows [12].

$$\mu = \frac{q\tau_c}{m_n} \tag{3.2}$$

Mobility is directly related to the mean free time between collisions (Eqn. 3.2), which in turn is determined by the various scattering mechanisms. Mobility is measured in terms of effective electric field.

3.3.1 Factors Influencing Mobility

The value of mobility (velocity per unit electric field) is influenced by several factors:

1. The mobility degradation increases with the gate bias because a higher gate bias draws the carriers closer to the oxide-silicon interface, where they are more influenced by the interfacial roughness.

2. The mechanisms of conduction through the valence and conduction bands are different, and so the mobilities associated with electrons and holes are different. The value for electrons is more than twice that for holes at low values of doping.

3. As the density of dopants increases, more scattering occurs during conduction. Mobility therefore decreases as doping increases.

4. At low temperature, electrons and holes gain more energy than the lattice with increasing temperature, therefore mobility increases. At high temperatures, lattice scattering dominates, and thus mobility falls.

3.3.2 Mobility and Velocity Saturation

At low values of electric field, the carrier velocity is proportional to electric field, *E,* the proportionality constant is the mobility. At low fields, the current density can therefore be written in terms of mobility.

At high electric field, scattering limits the velocity to a maximum value and the relationship above no longer holds - this is termed *velocity saturation.*

3.4 Effective Electric Field Calculation

The inversion layer mobility in MOSFETs has been a very important physical quantity as a parameter to describe the drain current and a probe to study the electric properties. It is well known that the inversion layer mobility in the MOS devices follows the universal mobility curve when the mobility is plotted as a function of effective electric field, E_{eff} independent of the substrate impurity concentration or the substrate bias. E_{eff} is defined by the following equation [7].

$$E_{eff} = \frac{q}{\varepsilon_{Si}}\left(N_{dpl} + \eta.N_s\right) \tag{3.3}$$

Where, q is the elementary charge, ε_{Si} is the permittivity of Si, N_{dpl} is the surface concentration of the depletion charge, N_s is the surface inversion carrier concentration. Here, η is a key parameter in defining E_{eff} and it has been reported that, in order to provide the universal relationship, the value of η should taken to be 1/2 for the electron mobility and 1/3 for the hole mobility [7,8]. That is, for determining the mobility of n-channel MOSFET, η is taken as 1/2 and for p-channel MOSFET, η is taken as 1/3.
Surface depletion carrier concentration can be given by the expression [7].

$$N_{dpl} = \sqrt{\left(4\varepsilon_{Si}\psi_B N_a / q\right)} \tag{3.4}$$

Where, ψ_B is the surface potential. The substrate impurity concentration (N_a) changes N_{dpl} and the resultant E_{eff}. The carrier concentration of the inversion layer also changes the effective field. The surface inversion carrier concentration can be determined from the charge of inversion layer per unit area (Q_n) since $N_s = Q_n/q$. The surface inversion carrier concentration is a function of bias voltages and can be found by using the following semi-classical expression [12].

$$Q_n(y) = -\left[V_G - V(y) - 2\psi_B\right]C_0 + \sqrt{\left(2\varepsilon_{Si}qN_a\left[2\psi_B + V(y)\right]\right)} \tag{3.5}$$

Where, $V(y)$ is the reverse bias applied between a point in the y direction (Fig. 2.1) along the channel and the source electrode (which is grounded).

3.5 Scattering Mechanisms

Scattering is a general physical process whereby moving particles (electrons or holes) are forced to deviate from a straight trajectory by one or more localized non-uniformities in the medium through which they pass.
The concept of mobility, resulting from an analysis of stationary transport where scattering phenomena limit carrier velocity, has been widely used till today in

microelectronics, as a measurable factor of merit and in analytic models developed to predict device operation. If scatterings are still playing a major role in decananometer MOSFET and cannot be neglected, ballistic transport in the channel takes a growing importance in device operation as the gate length of MOSFETs tends to the nanometer scale. The important scattering mechanisms affecting carrier transport in MOS devices are:

1. Phonon scattering.
2. Surface roughness scattering,
3. Coulomb scattering

3.5.1 Phonon Scattering

Phonons are an important source of scattering in charge transport. Collective vibrations of electrons are known as phonons. These processes are strongly dependent on phonon occupation. In phonon scattering a carrier moving through the channel is scattered by a vibration of the lattice, resulting from the temperature.

Electrons can be scattered into empty states at an energy E_1 from filled states at another energy E_1+hw by the emission of an optical phonon with energy hw. The in-scattering rate for this mechanism is proportional to the interaction strength, the electron density at energy E_1+hw, and the number of phonons [1]. Electrons with energy E_1-hw can also be scattered into empty states at energy E_1 due to phonon absorption. The in-scattering rate for this mechanism is again proportional to the interaction strength, the electron density at energy E_1-hw, and the number of phonons. Carrier scattering due to electron-phonon interaction is called phonon scattering.

The phonon scattering depends on the effective electric field and temperature. Mobility due to phonon scattering decreases at higher electric field. The mobility limited by photon scattering can be found by using the following formula [7].

$$\mu_{ph} = A.\left(E_{eff}\right)^{\gamma} T^{\alpha} \tag{3.6}$$

Here, A is a constant coefficient. From the universal mobility curve, the value of A has been selected as $1.75\times10^{9.15}$. The power of T, that is, α has been determined from the temperature dependence of the electron mobility at low electric field, where the contributions of surface roughness scattering and Coulomb scattering are so small that the temperature dependence of only phonon scattering can be determined. The value of α has been taken as 1.9. The electron mobilities at 300 K are represented by the universal curve as a function of E_{eff} independent of the substrate impurity concentrations by choosing the value of η to be 1/2. Similarly, the hole mobilities are also represented by the universal curve as a function of E_{eff} by choosing the value of η to be 1/3 as observed in [8]. Takagi et al [7,8] have shown that universal relationships of the electron and hole mobilities do hold up to the substrate impurity concentration of 10^{-18} cm^{-2}. It has been seen that the values of η for the electron and hole mobilities are 1/2 and 1/3, respectively, for a wide range of E_{eff} and the substrate impurity concentration. These values are in agreement with those reported previously [8,10].

By examining the mobility curves [7,8] at different temperatures it is seen that the mobility limited by phonon scattering is related to $E_{eff}^{-0.3}$. Hence, the value of γ is taken as (-0.3).

3.5.2 Surface Roughness Scattering

Surface roughness scattering or interface roughness scattering is the scattering of a charged particle by an imperfect interface between two different materials. In MOSFET, surface roughness scattering occurs due to the SiO_2/Si interface fluctuations. Scaling CMOS devices to smaller dimensions while maintaining good control of the short-channel effects makes it necessary to reduce the gate oxide thickness in close proportion to the channel length. Thus, for devices with gate lengths below 100 nm, gate oxides near to 2 nm are needed [14]. The use of such thin oxides leaves inversion layer electrons very

near to the interface formed by the gate material (metal or polycrystalline silicon) and the oxide, SiO_2 and SiO_2/Si interface. This proximity is sufficient for the transport properties of the electrons in the channel to be modified by the imperfections of this interface. The semiconductor/oxide interface is not perfectly smooth, and its deviation from an ideal plane produces a potential modification affecting the electrons in the channel. These potential modifications produce the electron scattering and consequently degradation in their mobility. The surface roughness scattering potential is affected by the screening of the mobile electrons in the inversion layer [14].

The electron mobility in high effective electric field is very sensitive to the surface roughness scattering. The mobility limited by surface roughness scattering is different for electron and hole. It is observed that in order to fit the existing mobility curves [7,8,14], the mobility due to surface roughness scattering varies with the effective electric field as a negative power of 2.6. The mobility limited by surface roughness scattering for electron follows the relation [7].

$$\mu_{sr} = B.E_{eff}^{-\beta} \tag{3.7}$$

Here, the parameter β is determined to be 2.6 so that the total mobility fits the experimental data. The constant coefficient B is selected to be $4.5 \times 10^{18.3}$.

3.5.3 Coulomb Scattering

Coulomb scattering occurs due to the substrate doping impurities and interface charges. Coulomb scattering results when a charge carrier travels past an ionized dopant impurity (donor or acceptor). The charge carrier path is deflected by owing to Coulomb force interaction. The probability of Coulomb scattering depends on the total concentration of ionized impurities, which is the sum of the concentration of negatively and positively charged ions. Coulomb scattering is less significant at higher temperature. Because, at higher temperatures, the carriers move faster and they remain near the impurity atom for a shorter time and are therefore less effectively scattered.

The mobility due to Coulomb scattering can be determined using the following formulae [8,12].

$$\tau_c = c.N_s^{.9} \tag{3.8}$$

$$\mu_c = \frac{\tau_c q}{m_n} \tag{3.9}$$

Where, τ_c is the mean free time between collisions due to Coulomb scattering and c is a fitting parameter. m_n is the effective mass of electron.

Coulomb scattering is a function rather of the inversion charge than a function of the effective field, for the same concentration. It has been shown that when bulk-impurity concentration, substrate bias, and charge trapped at the interface are increased, while a rise in the Coulomb-scattering rate is produced mainly through the following mechanisms:

a) An increase of the charged centers responsible for the scattering (interface charge and bulk-impurities).

b) A fall in the screening of these charged centers by mobile carriers (bulk-impurities and substrate bias).

It has been found that Coulomb scattering is actually the factor responsible for the deviation of mobility curves from universal behavior when they are plotted versus the transverse effective field [14]. Coulomb scattering increases as the inversion charge increases and it is very weak at high electric fields due to the increase in screening. The mobility behaves universally at high electric fields.

3.6 Effective Mobility

The effective mobility is the total mobility that considers the effect of all the scattering mechanisms. The effective mobility for phonon scattering, surface roughness scattering and Coulomb scattering can be determined using Matthiessen's rule [12].

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{c}} \tag{3.10}$$

The curve of effective mobility versus effective electric field follows the universal relationship [7,8]. In the mobility curve, the phonon scattering and surface roughness scattering mechanisms dominate at the higher value of electric field and the mobility due to Coulomb scattering dominates at low value of effective electric field.

There is no dependence of mobility on the oxide thickness when only phonon and surface roughness scattering mechanisms are taken into account, but when the effect of the Coulomb scattering is included a slight dependence on the oxide thickness appears. In theory, and for a given value of the transverse effective field (or inversion charge concentration) the only dependence of these scattering mechanisms on the oxide thickness arises from the screening of the scattering potentials [14].

3.7 Mobility Reduction in Nanoscale MOSFET

Recently, the dramatic reduction of the measured mobility when decreasing the gate length has been observed by different groups using accurate techniques [15]. The concept of mobility, resulting from an analysis of stationary transport where carrier velocity is limited by scattering phenomena, has been widely used till today in microelectronics as a measurable factor of merit and as a parameter of analytical models developed to predict device performance. If scatterings are still playing a major role in decananometer MOSFET and cannot be neglected [15-17], ballistic transport in the channel takes a growing importance as the gate length of MOSFETs tends to the nanometer scale.

The effective mobility determined by Eqn. 3.10 is said to be apparent mobility. Shur-based model [16] can be useful to describe the apparent decrease of extracted mobility with channel length. Shur defines K_{bal} as [15].

$$K_{bal} = \frac{2q}{\pi m_n v_{th}} \tag{3.11}$$

Here, v_{th} is the average thermal velocity, determined by [15].

$$v_{th} = \sqrt{\frac{8kT}{\pi m_n}} \tag{3.12}$$

Where, q is the electron charge, v_{th} is the average thermal velocity, k is the Boltzmann constant and T is the temperature. The effective mobility as a function of channel length can be found as [15].

$$\mu_{eff} = \frac{\mu_{tot}}{1 + a\frac{\mu_{tot}}{K_{bal} L_{ch}}} \tag{3.13}$$

Here, 'a' is a fitting parameter which has been introduced in this work in order to match with the experimental nanoscale data. The value of 'a' has been selected as 15 from the available experimental results.

Chapter 4

Results for Nanoscale MOSFETS

4.1 Test Device

The device structure that has been examined is shown in Fig. 4.1. This device is a simplified and ultra-scaled version of a MOS transistor. L_{ch} is the channel length or gate length of MOSFET. The MOSFET has been studied for gate lengths (or channel lengths) of 90 nm, 65 nm, 45 nm and 20 nm. d is the thickness of the SiO_2 layer. An intrinsic body is assumed in order to eliminate threshold voltage fluctuations due to variations in body doping and to reduce mobility degradation due to ionized impurity scattering. The substrate doping is selected ($N_a = 10^{18}/cm^3$) such that the threshold voltage is practical value. Here, r_j is the junction depth of the source and drain.

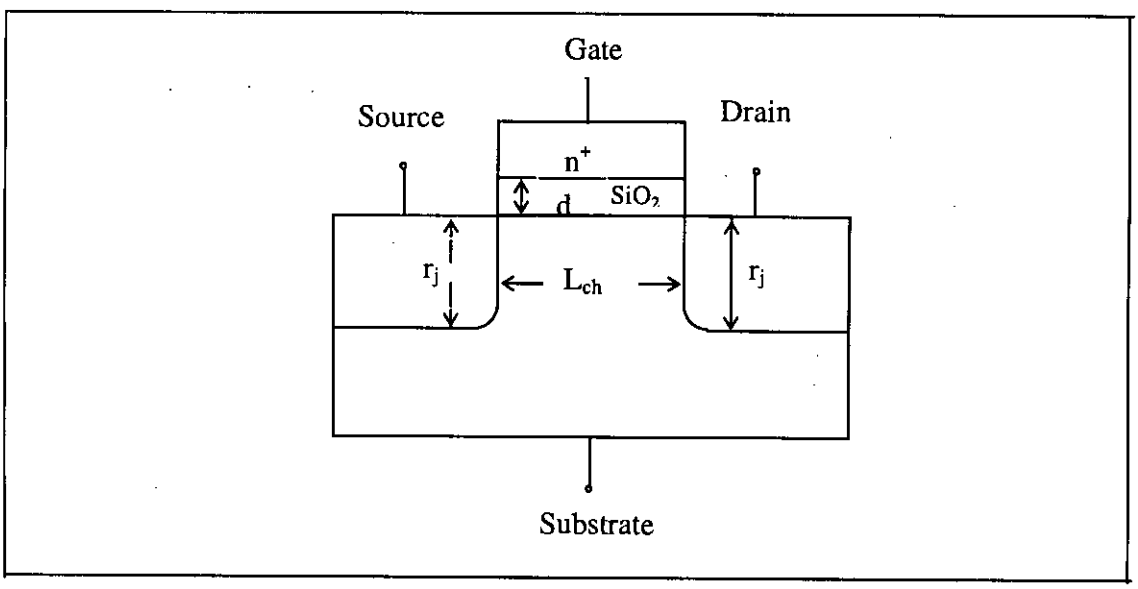


Fig. 4.1: Test device of an n-channel enhancement type MOSFET.

Following parameters of MOS device are usually considered for device scaling.

Gate oxide thickness (d) : The thickness of the gate dielectric of nanoscale MOS device must be decreased along with the channel length to enhance the gate control in order to overcome short-channel effects and transconductance degradation.

Junction doping : Junction depths have been controlled by ion-implantation of the dopants into selected regions. They are limited by diffusion during subsequent thermal cycles. Future generations of technology require steeper doping profile, but present annealing technology is unable to produce sufficiently steep doping gradients at the edge of the source/drain regions.

Source and drain (r_j) : Shallow junctions in the Source / Drain regions are needed to minimize the short channel effects in scaling of sub-100 nm MOSFETs. The ITRS roadmap predicts that the SD depths should be as low as 10 nm to achieve a channel length of 50 nm [18]. In this work, S/D junction depth is taken as one fifth of the channel length.

4.2 Inversion Layer Carrier Concentration

When a positive voltage is applied to the gate terminal of the n-channel MOSFET, electrons are induced under the Si-SiO_2 layer. When the voltage is increased, concentration of the carriers increases. A channel is formed in between the source and drain through the p-type substrate. The device is operated when strong inversion is occurred. Concentration of the inversion layer depends on the gate voltage as well as on the drain voltage. Fig. 4.2 shows the electron concentration in the channel as a function of gate voltage (V_G) in semi log scale. The continuous line shows the curve drawn using the proposed model. The symbols represent schred 2.0 predicted value of electron concentration done by Ren [1]. At moderate V_G, the predicted values are different from the proposed values. This is the subthreshold region. But beyond the subthreshold region, difference between the two values is almost undetectable.

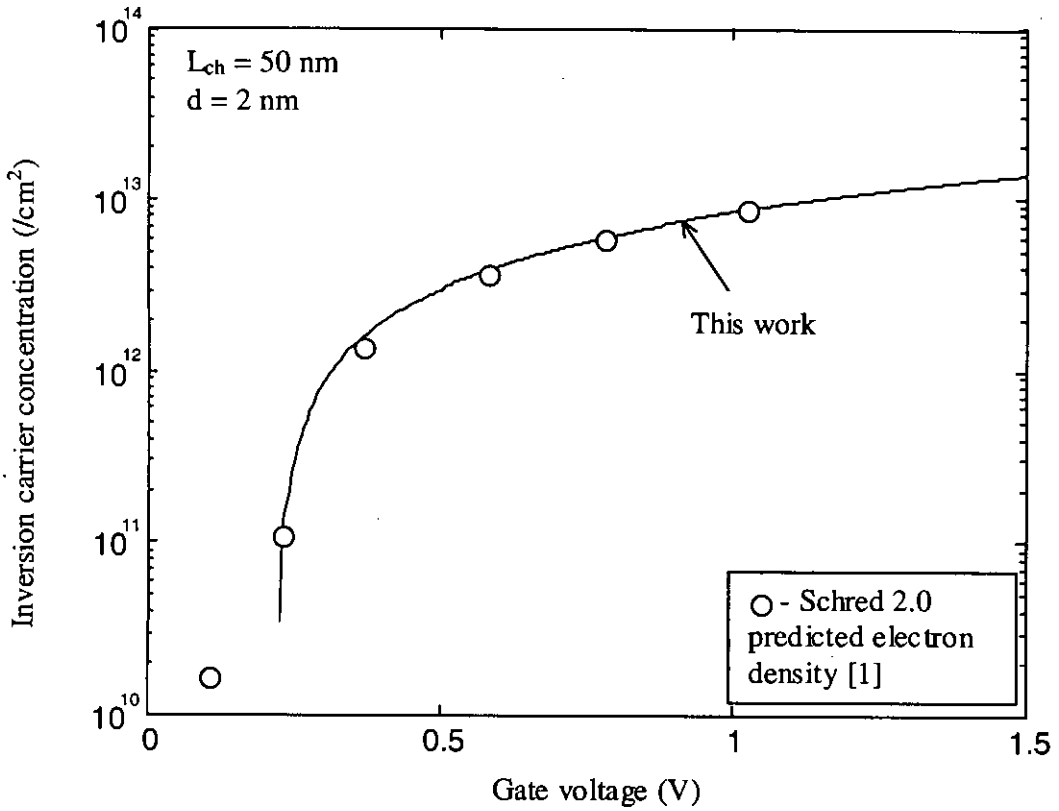


Fig. 4.2: Carrier concentration in inversion layer as a function of gate voltage.

The carrier concentration if is plotted against the effective field (Fig. 4.3), it is seen that the inversion charges increases with the effective field. Inversion carrier concentration increases at higher rate in low effective field. The increment rate of carrier concentration decreases at higher field. This is because the pinch-off point occurs and charges remain constant even if the voltage is increased beyond the saturation value.

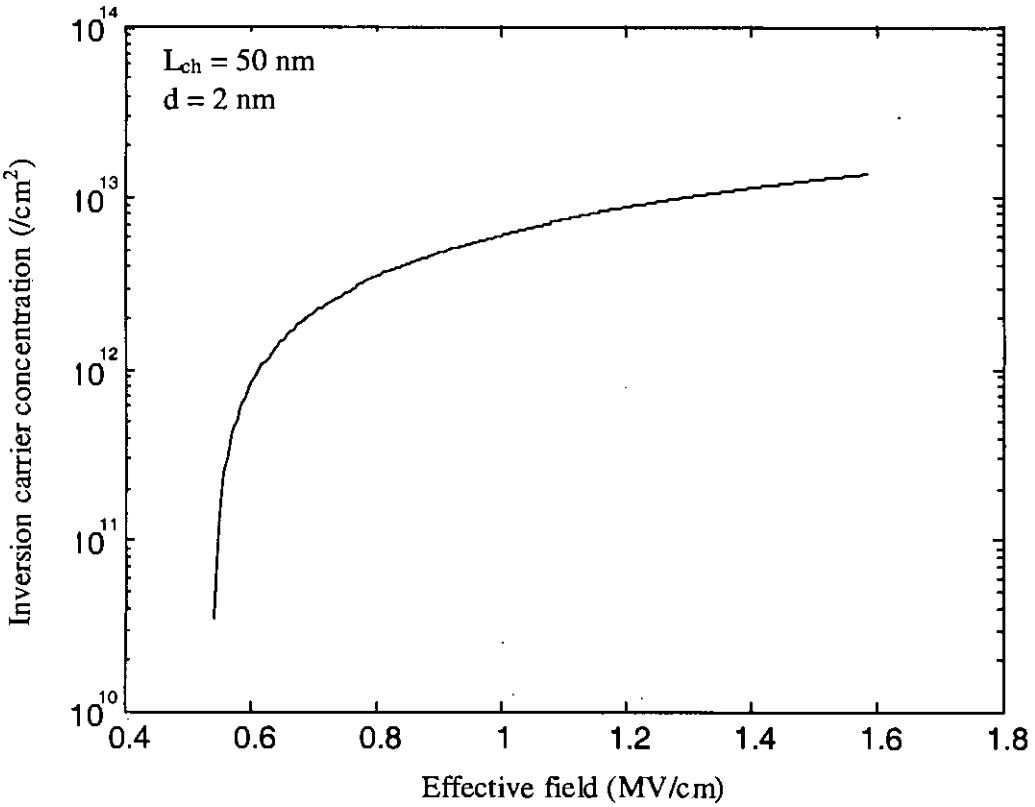


Fig. 4.3: Inversion carrier concentration versus effective electric field.

4.3 Threshold Voltage Roll-off:

The threshold voltage is defined for long-channel MOSFETs as the gate voltage that causes the channel inversion and then enables conduction. For short channel devices, the channel depletion region is influenced by source-bulk and drain-bulk junctions. Threshold voltage depends on geometrical parameters such as effective length and junction shape.

The short channel effect (SCE), one of the most critical problems of nanoscale MOSFET devices, will decrease the MOSFET threshold voltage, called V_{Th} roll-off. As the channel length of MOSFET is reduced to nanoscale region, the charge distribution in the channel

is influenced by the fields originating from the source/drain. Threshold voltage in the linear region becomes less positive for n-channel MOSFETs when the channel length is decreased. Threshold voltage fluctuation for channel length reduction can be determined using the following formula [12]:

$$\Delta V_{th} = -k \frac{qN_a W_m r_j}{C_o L_{ch}} \left(\sqrt{1 + \frac{2W_m}{r_j}} - 1 \right) \tag{4.1}$$

Here, r_j is the depth of source and drain junction, W_m is the maximum width of the depletion layer. The parameter k is introduced here and its value is selected from the experimental results [19] so that the semi-classical expression can be applied for nanoscale MOSFET. It is seen that k is equal to d/L_{ch}.

Figure 4.4 shows the relationship between the threshold voltage fluctuation and the nanoscale channel length. The continuous curve of threshold voltage shift versus gate length is obtained for the proposed model and the symbols are the experimental results of Fjeldly T. A. and Shur [19]. A good agreement between the model and experimental results are seen in the figure. It is seen that for channel length above 50 nm, threshold voltage fluctuation is less than that compared to channel length below 50 nm. That is, threshold voltage decreases very sharply when channel length is below 50 nm.

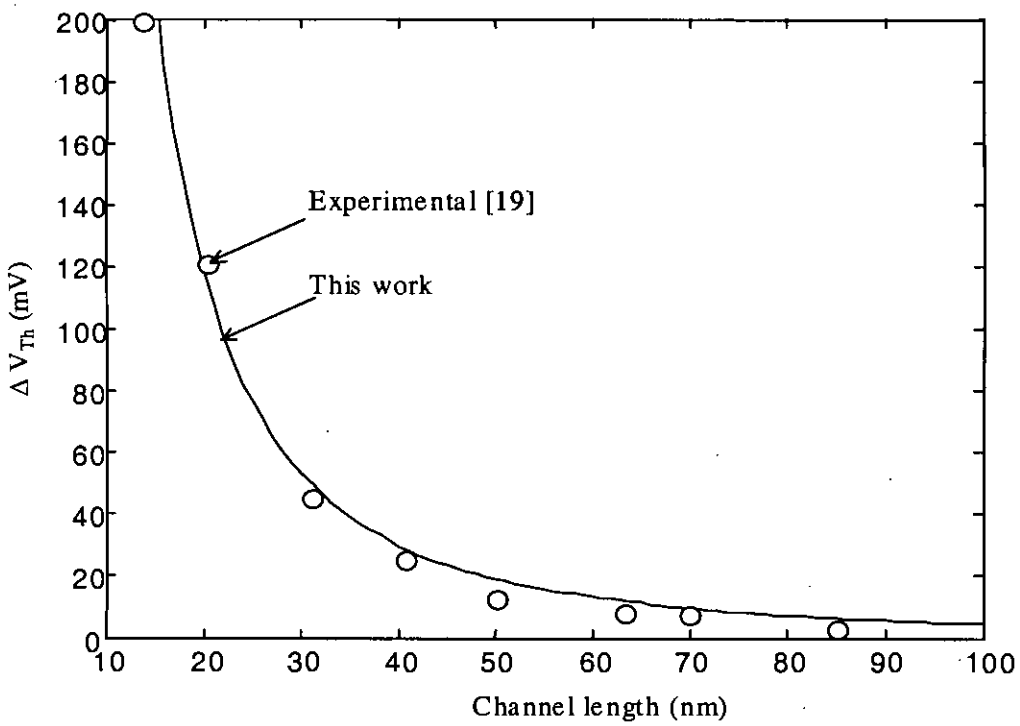


Fig. 4.4: Decrease in threshold voltage (ΔV_{th}) with the channel length. The symbols represent experimental result (Fjeldly T. A. and Shur [19])

Figure 4.5 shows that threshold voltage is near to 0.3 V for device channel length in the nanoscale region. For shorter channel lengths, value of the threshold voltage reduces. Threshold voltage shift is due to the reduction of charges in the depletion layer for channel length reduction.

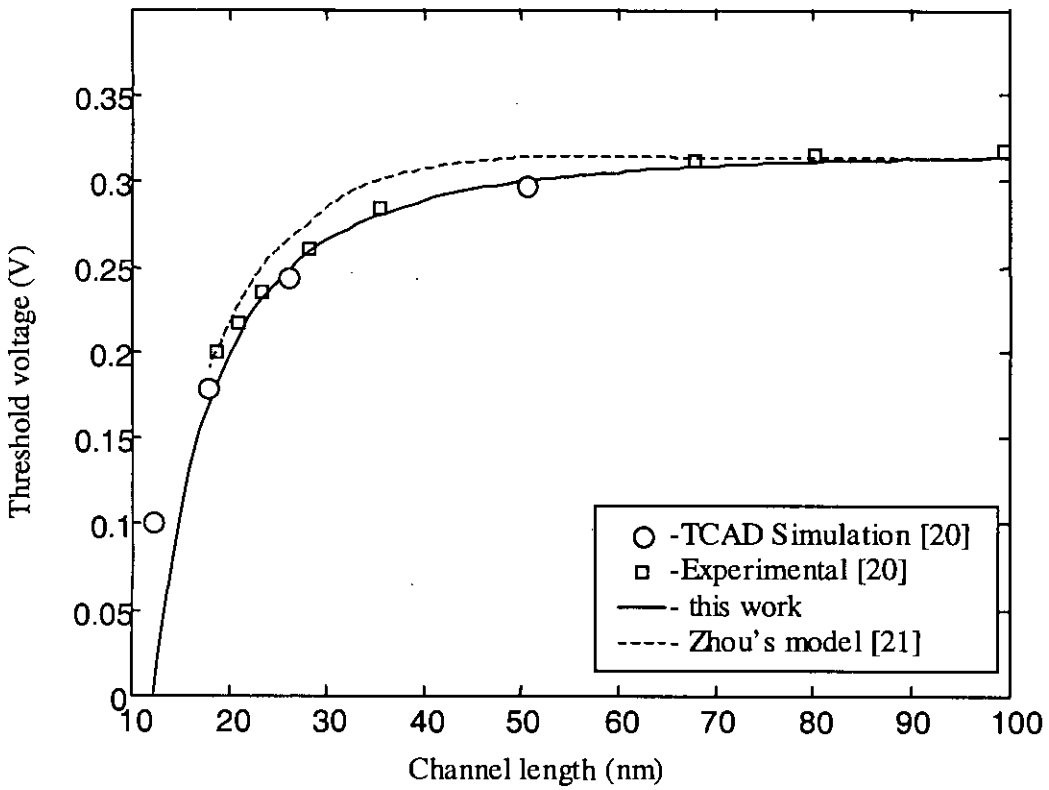


Fig. 4.5: Threshold voltage roll-off of MOSFET for nanoscale channel length.

Threshold voltage decreases as the thickness of SiO_2 is decreased. This is because, as the thickness of oxide is reduced, the amount of gate voltage required to create strong inversion is decreased.

4.4 Mobility Due to Phonon Scattering

Mobility limited by the phonon scattering degrades for increased effective field. This is because, as the effective field (energy) on the electron increases, the probability of scattering by phonon emission decreases. These dependencies are consistent with the previously reported theoretical and experimental results [7-9].

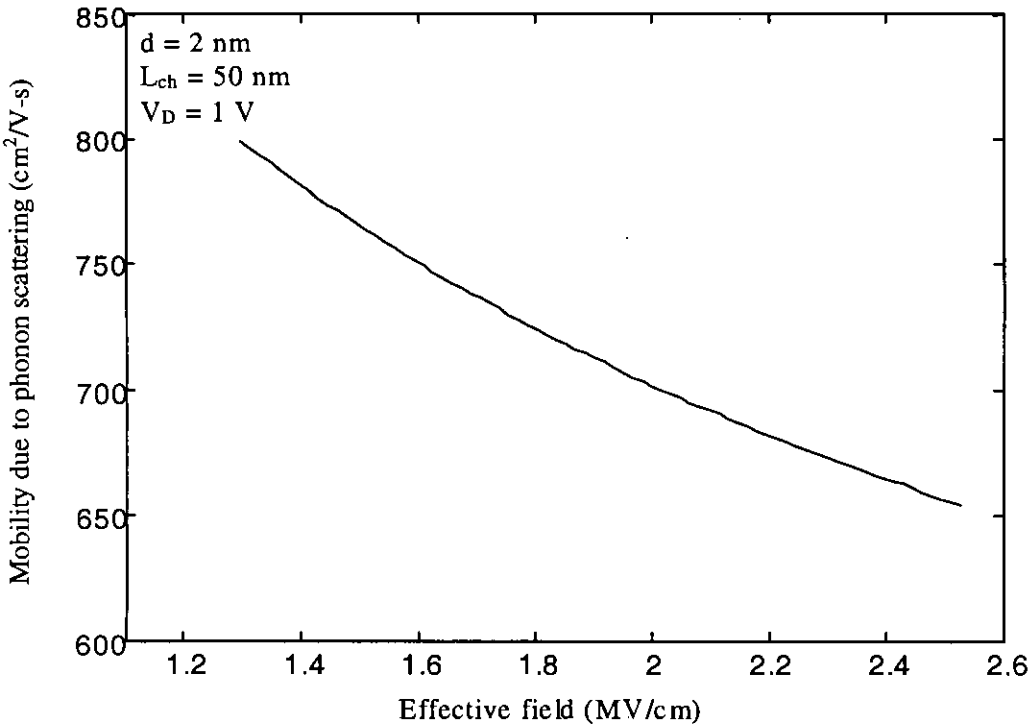


Fig. 4.6: Mobility due to phonon scattering versus effective field.

Phonon scattering depends on the temperature. Mobility limited by the phonon scattering is very high at lower temperature as shown in Fig. 4.7.

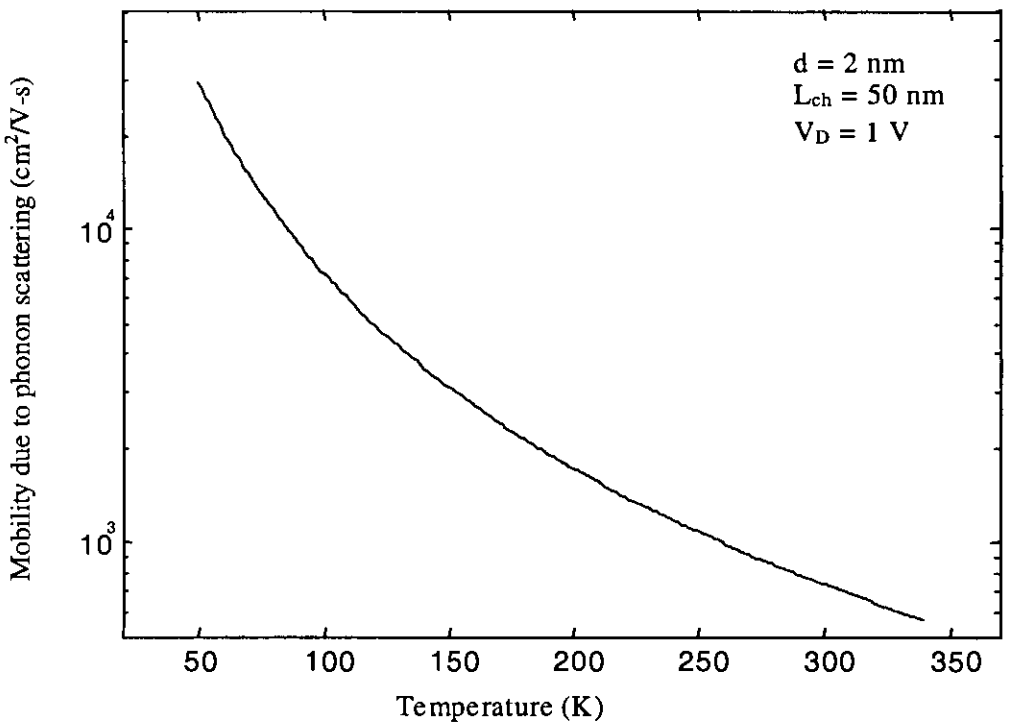


Fig. 4.7: Mobility limited by phonon scattering as a function of temperature.

An important effect that appears in inversion layer with decreasing thickness of the silicon layer is an increase in the phonon-scattering rate. For the same inversion charge concentration, the phonon-scattering rate is greater in thinner films than in thicker ones. Since the confinement is greater, reduction in the mobility occurs.

4.5 Mobility Due to Surface Roughness Scattering

The mobility limited by the surface roughness scattering is shown in Fig. 4.8. It is seen that the mobility deviates at high effective field. Mobility degrades due to the potential modification due to imperfect interface. These potential modifications produce the electron scattering and consequently degradation in the mobility. The surface roughness

scattering potential is affected by the screening of the mobile electrons in the inversion layer.

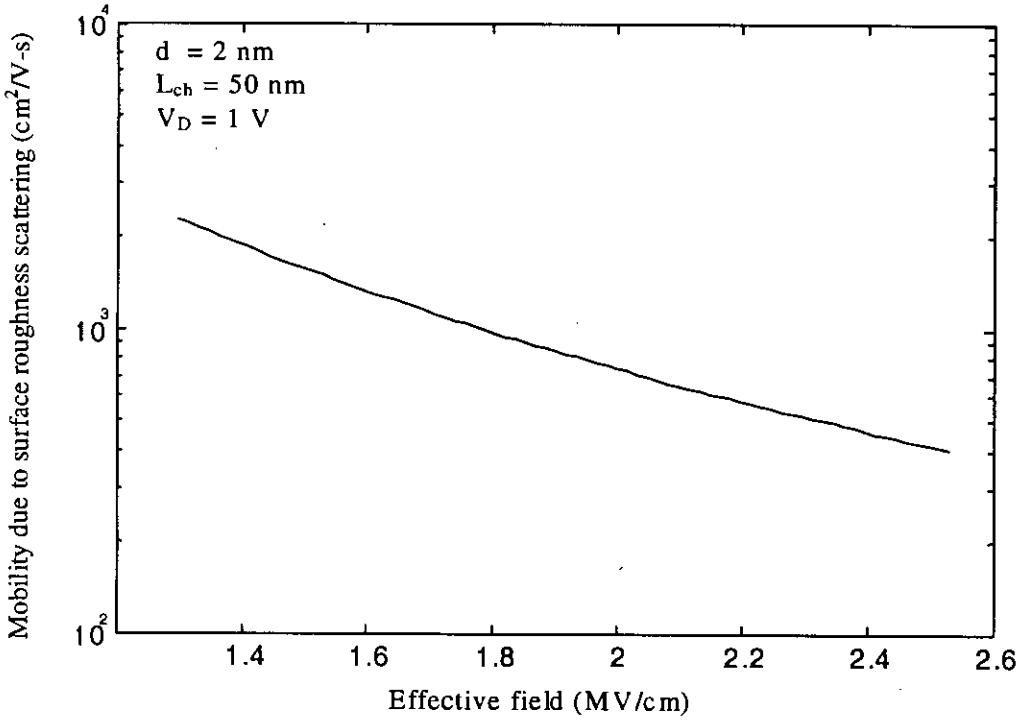


Fig. 4.8: Mobility due to surface roughness scattering versus effective electric field.

4.6 Mobility Due to Coulomb Scattering

It is known that there are three types of Coulomb scattering centers that can affect the inversion layer mobility; substrate impurities, interface state charges and charges trapped in SiO_2 for low value of N_a. The Coulomb interaction between the inversion layer electrons and the charges localized near the interface such as interface states or trapped charges become stronger with an increase in N_S, because the average position of electrons approaches the interface more. This effect can compensate the screening effect to some extent and as a result, the N_S dependence becomes weaker.

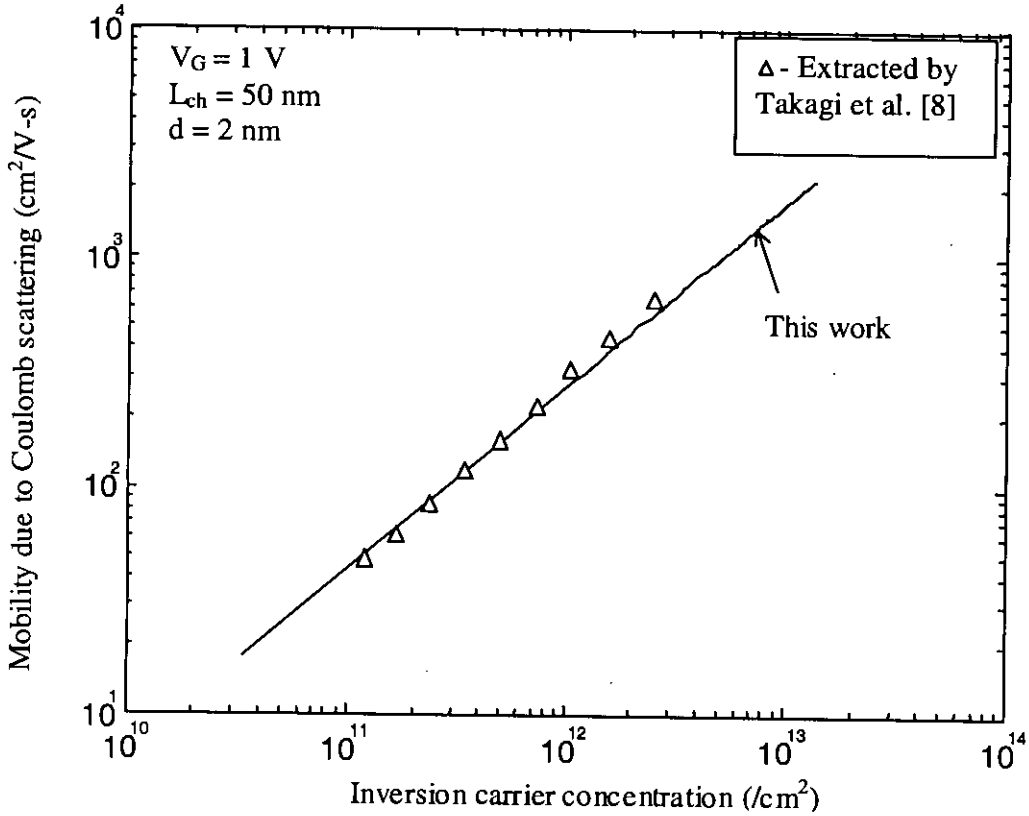


Fig. 4.9: Mobility due to Coulomb scattering versus inversion carrier concentration.

Coulomb scattering rate can be characterized as a function of inversion carrier concentration (N_S), which is directly related to the screening effect and the electron energy. In Fig. 4.9, mobility due to Coulomb scattering is plotted as a function of inversion carrier concentration. It is seen that Coulomb scattering rate increases with the increase of N_S. This is compared with that determined by Takagi et al. [8] at temperature 300K. Takagi determined the values from the deviation of universal mobility curve due to Coulomb scattering. For this, mobility determined by the combined effect of surface roughness and phonon scattering was subtracted from the universal mobility curve. These values (triangles) are in good agreement with the curve of proposed model.

Coulomb scattering versus effective field is plotted in Fig. 4.10. The higher the effective field, the lower the Coulomb scattering, due to a rise in the screening of the charged

centers as mobile-carrier density increases. On substrates with higher impurity concentrations, the electron and hole mobilities significantly deviate from the universal curves at lower surface carrier concentrations because of Coulomb scattering by the substrate impurity.

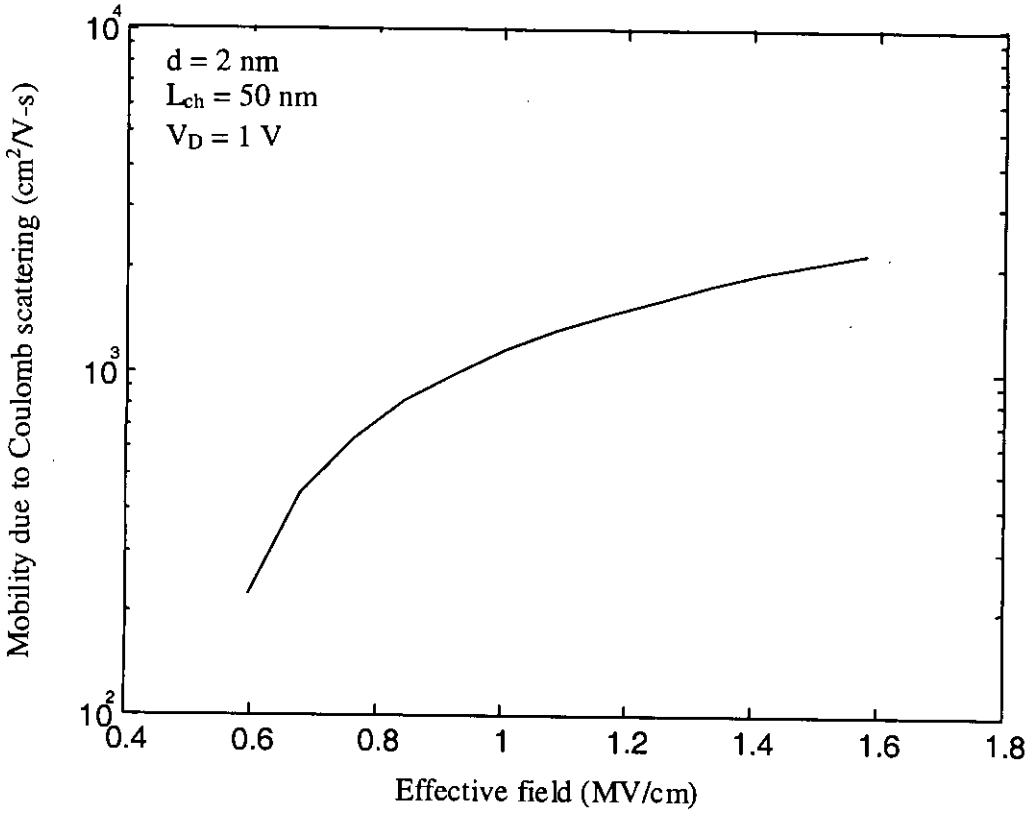


Figure 4.10: Mobility due to Coulomb scattering versus effective electric field.

4.7 Effective Mobility

The effective mobility is obtained considering three scattering mechanisms, phonon scattering, surface roughness scattering and Coulomb scattering. The effective mobility curve is similar to the universal mobility curve described by Takagi et al. [7,8]. At the lower value of electric field, Coulomb scattering is responsible for the deviation of the effective mobility curve. Because the surface inversion charge concentration is low at this

region. As the field increases, charge concentration increases (Fig. 4.3), the Coulomb scattering increases (Fig. 4.10). But surface roughness scattering and phonon scattering become stronger than Coulomb scattering at the higher value of carrier concentration, as the effective field is increased in proportion to the charge concentration. The effective mobility at higher electric field is due to the phonon scattering and surface roughness scattering.

If the nanoscale device physics is not considered in the mobility curve, the mobility is termed as the *ballistic* or *apparent* mobility. For MOSFETs with nanoscale channel lengths, the mobility thus obtained has to be modified. As experimentally observed elsewhere, the mobility extracted from electrical characteristics decreases with the shrinking of the channel length. The mobility may be linked to the long-channel mobility and to a *ballistic mobility* using Mathiessen's rule as described earlier. Relationship between the mobility and the channel length can be found by using equation no 3.11, 3.12 and 3.13. It has been seen that the mobility is degraded when modeled for nanoscale channel lengths.

Effective mobility for nanoscale MOSFETs is shown it the following figure. It shows the effective mobility for 50 nm of channel length considering the nanoscale device physics. Experimental and simulation results [28] are interpolated on this curve. It is seen that simulation curve of Walczak and Majkusiak deviate from the experimental results at lower effective field. The mobility curve for this model is very close to the experimental value and shows better result.

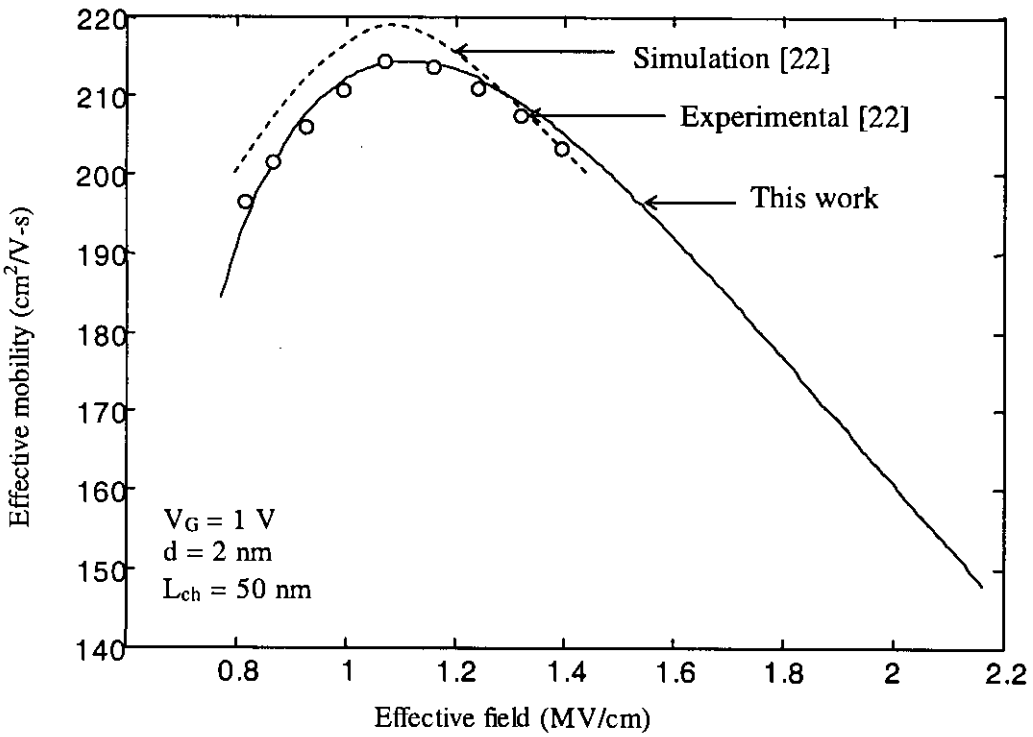


Fig. 4.11: Effective mobility in nanoscale MOSFETs.

Relationship between the effective mobility and channel lengths can be observed by plotting mobility curves at several channel lengths of MOSFET. When the channel length is decreased, the effective mobility is reduced.

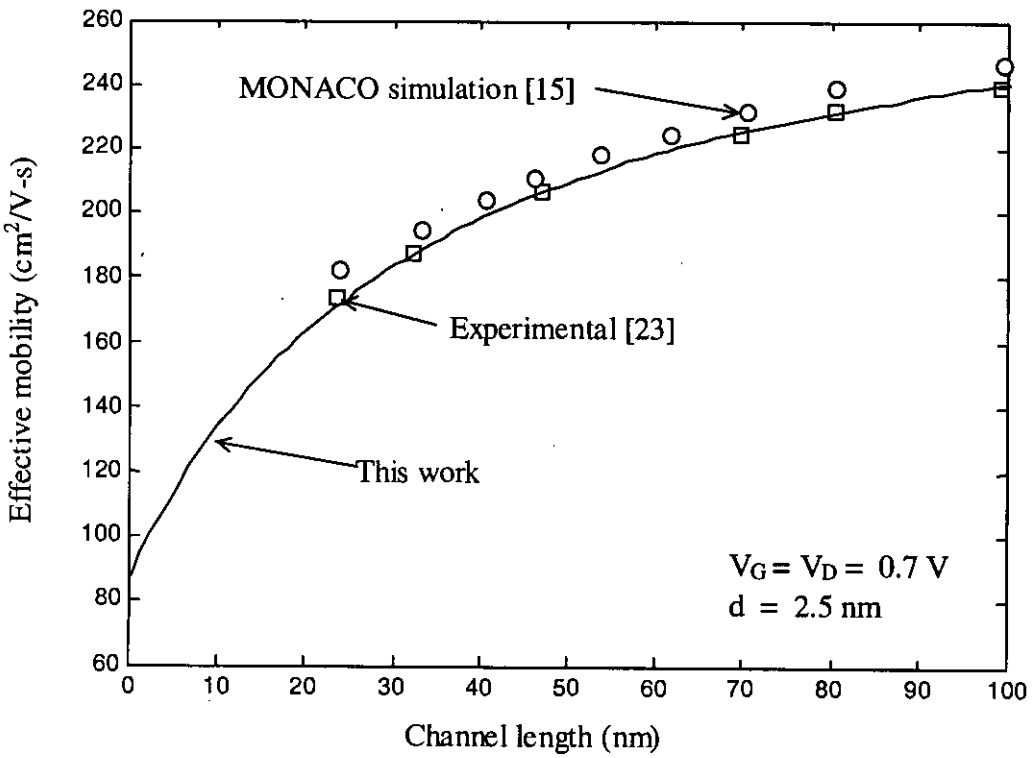


Fig. 4.12: Effective mobility versus channel length. Experimental mobility (squares) [23] and simulation results (circles) [15].

Using semi-classical Monte Carlo (MC) device simulator MONACO, mobility of nanoscale MOSFETs was obtained [15], shown as circles in Fig. 4.12. MONACO is a particle MC device simulator coupled with 2D or 3D Poisson's solver. In simulating MOSFET, scattering mechanisms related to phonons, ionized impurities and SiO_2/Si surface roughness were considered. Quantization effects were not taken into account. The proposed model is in good agreement with the MONACO simulation results. It is very close to all data observed experimentally in nanoscale devices [23].

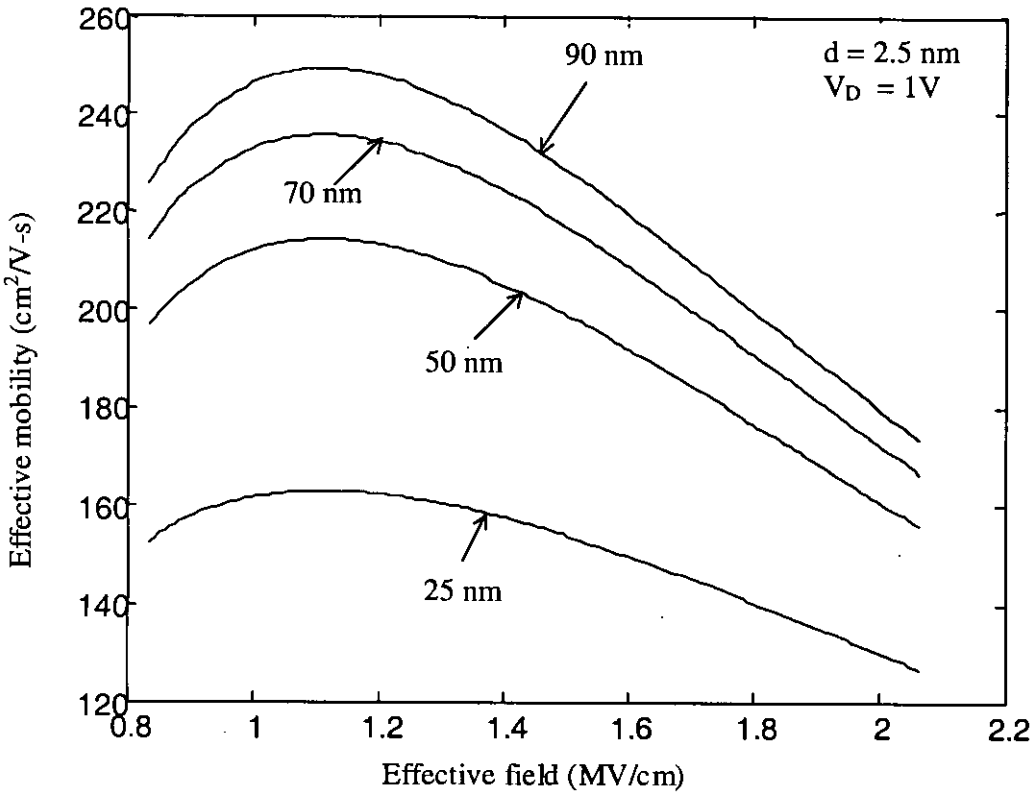


Fig. 4.13: Effective mobility versus effective electric field for different channel lengths.

The above figure shows the effective mobility curves for channel lengths of 90 nm, 70 nm, 50 nm and 25 nm. It shows that the maximum effective mobility is about 250 cm^2/V-s for MOSFET with 90 nm of channel length. Whereas, for channel length of 25 nm, the effective mobility is about 165 cm^2/V-s. So it is seen that mobility curve shifts downward for shorter channel lengths. Each mobility curve in the above figure is similar to the universal mobility curve [8,10]

In order to understand the E_{eff} dependences quantitatively, it is necessary to characterize the universal curve in terms of scattering mechanism. Figures 4.14 and 4.15 show a schematic diagram of the E_{eff} dependences on the basis of a general understanding of the inversion layer mobility. According to this diagram, the universal curve can be divided

into phonon scattering, Coulomb scattering and surface roughness scattering term. The individual and effective mobility curves for this model are plotted as a function of effective field. The effective field is a function of gate bias and drain bias. Figure 4.14 is plotted when effective field is a function of gate voltage, drain voltage is kept constant. Figure 4.15 is plotted when effective field is a function of drain voltage, gate voltage is kept constant. These figures are compared with Takagi's mobility curve [7,8] and very good agreement is obtained.

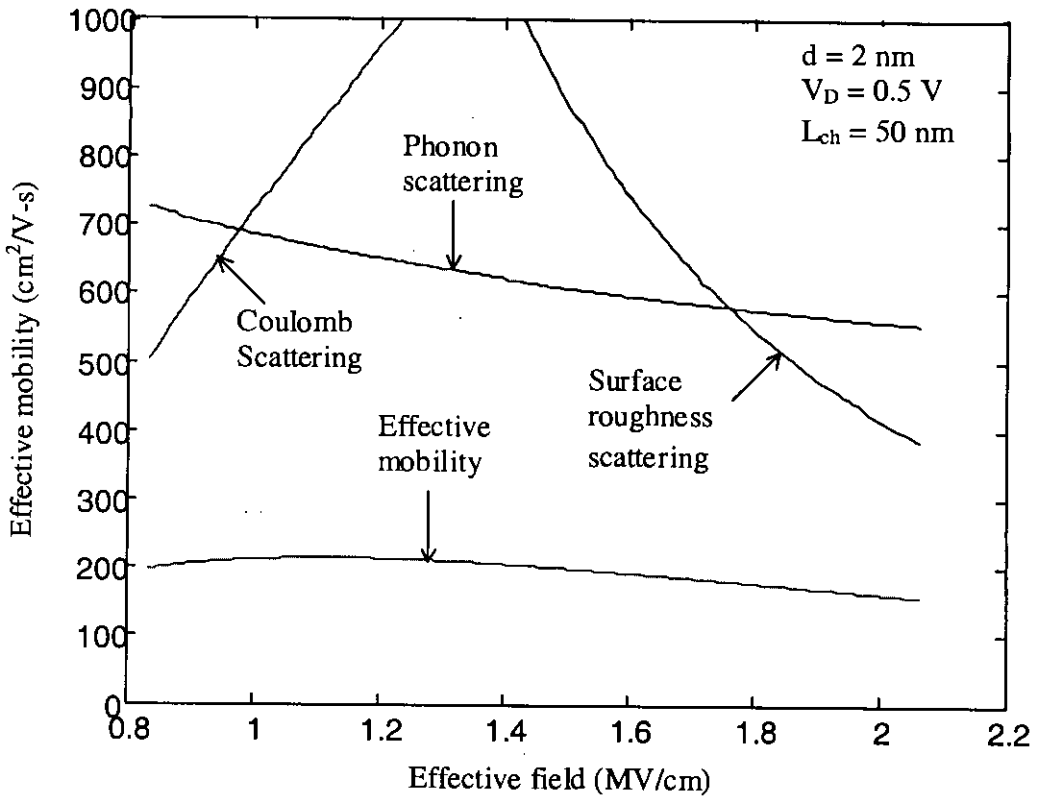


Fig. 4.14: Mobility versus effective electric field as a function of gate voltage.

The individual mobility curves for the proposed model are similar to Takagi's mobility curve of three scattering mechanisms. The effective mobility of the proposed model lies below that of Takagi when two figures are compared. The reason behind this is: in

Takagi's mobility model, no consideration for channel length was present. It is seen that mobility extracted from electrical characteristics decreases for shrinking of channel length [15]. In the proposed model, scattering mechanisms are channel length independent. The effect of channel length on the mobility is considered in deriving the effective mobility of nanoscale MOSFET. Ballistic mobility is determined from the scattering mechanisms and then effective mobility is determined from this ballistic mobility using Eqn. 3.13 by means of considering the effect of nanoscale channel length. Effective mobility is always less than the ballistic mobility as the mobility degrades for short channel when compared to the long channel device. Hence, the effective mobility curve for proposed model is below Takagi's effective mobility curve.

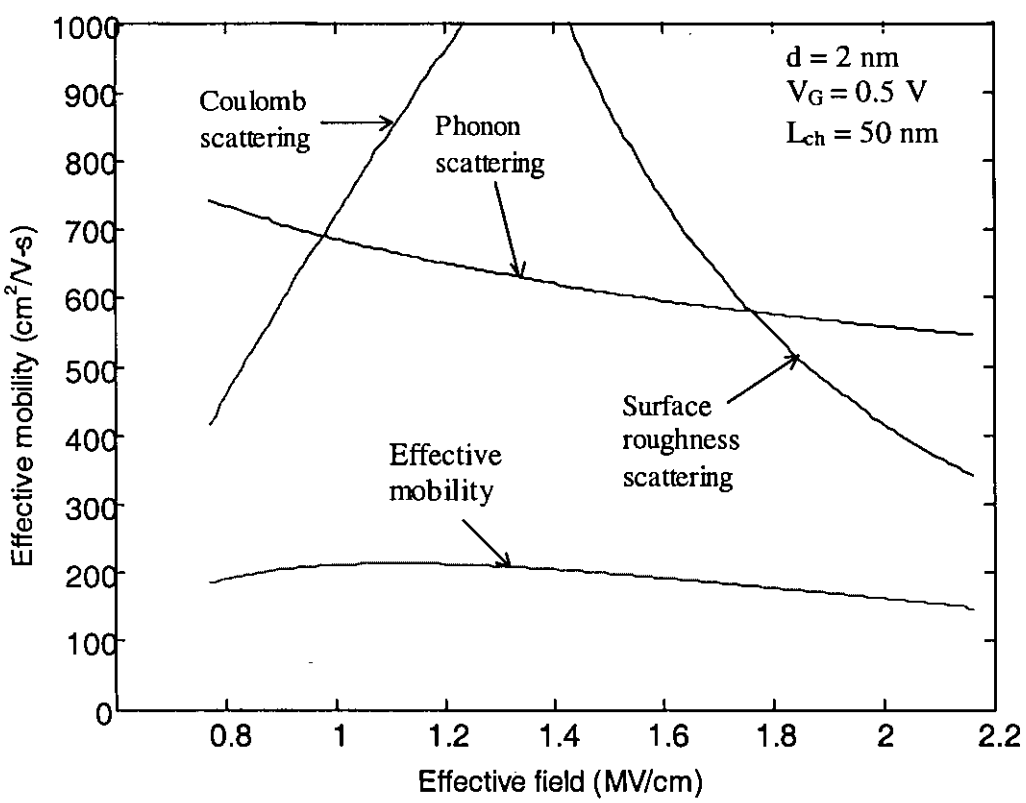


Fig. 4.15: Mobility versus effective electric field as a function of drain voltage.

4.8 Current-Voltage Characteristics

For the derivation of drain current, mobility has been determined for different scattering phenomenon. Mobility depends on the effective electric field in the inversion channel. Effective field is created by applying the gate voltage and the drain voltage. The *I-V* characteristics of MOSFET can be of two types: I_D-V_G curve or the transfer characteristics and I_D-V_D curve or the output characteristics. These are described as follows.

4.8.1 Transfer Characteristics (I_D-V_G)

In MOSFET operation, three different regions are distinguished; the "subthreshold" region, in which the transistor effectively passes extremely low current; the "linear" region, in which the behavior is ohmic, and the "saturation" region, in which the current is nearly constant.

If no charge is applied to the gate, the source and drain regions are separated by reverse biased pn junctions, and no current can flow between the source and drain of the transistor (the off impedance is normally of the order of thousands of mega ohms).

When the gate voltage is applied, charges in the inversion layer increases resulting in an increase in the effective field. The effective mobility increases with the gate voltage (Fig.4.16). The mobility curve degrades when the gate voltage is large enough. The degradation is due to the phonon scattering and surface roughness scattering.

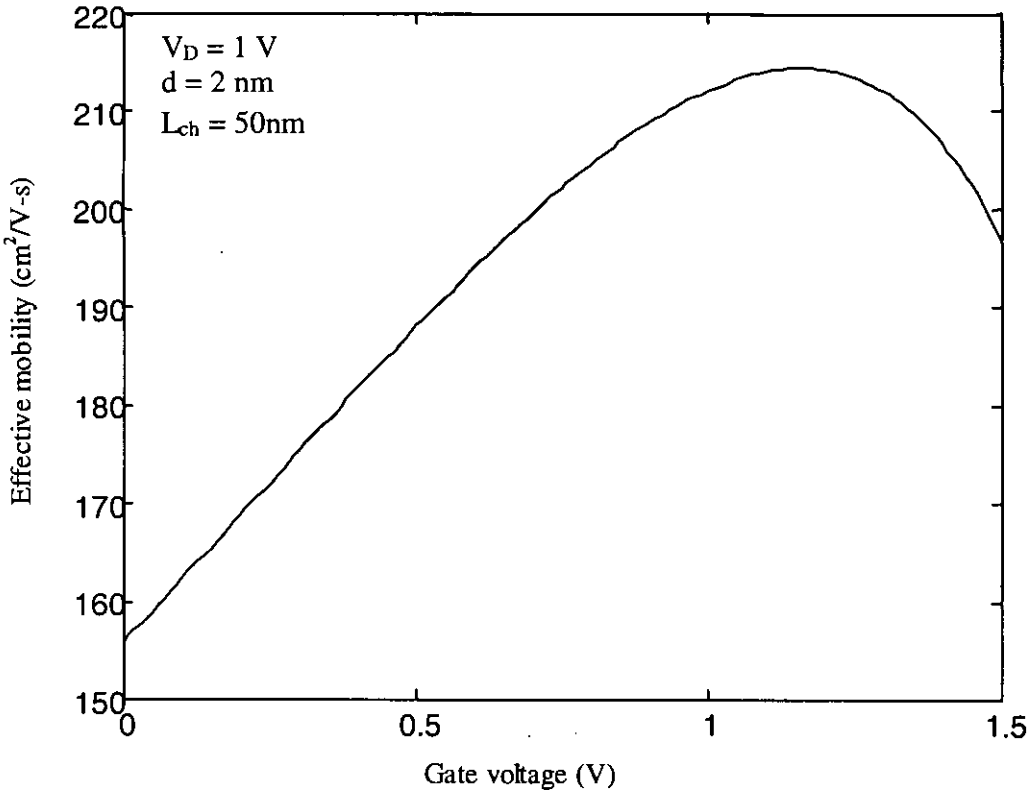


Fig. 4.16: Effective mobility as a function of gate voltage at a constant drain voltage.

The drain current in the subthreshold region occurs when V_G is below the threshold voltage. Subthreshold drain current is much lower than the device on-current. It depends on the channel length of the device. For 25 nm MOSFET with 1.5 nm of oxide thickness, the subthreshold current is shown in figure. The point on the curve where the slope changes is the threshold voltage.

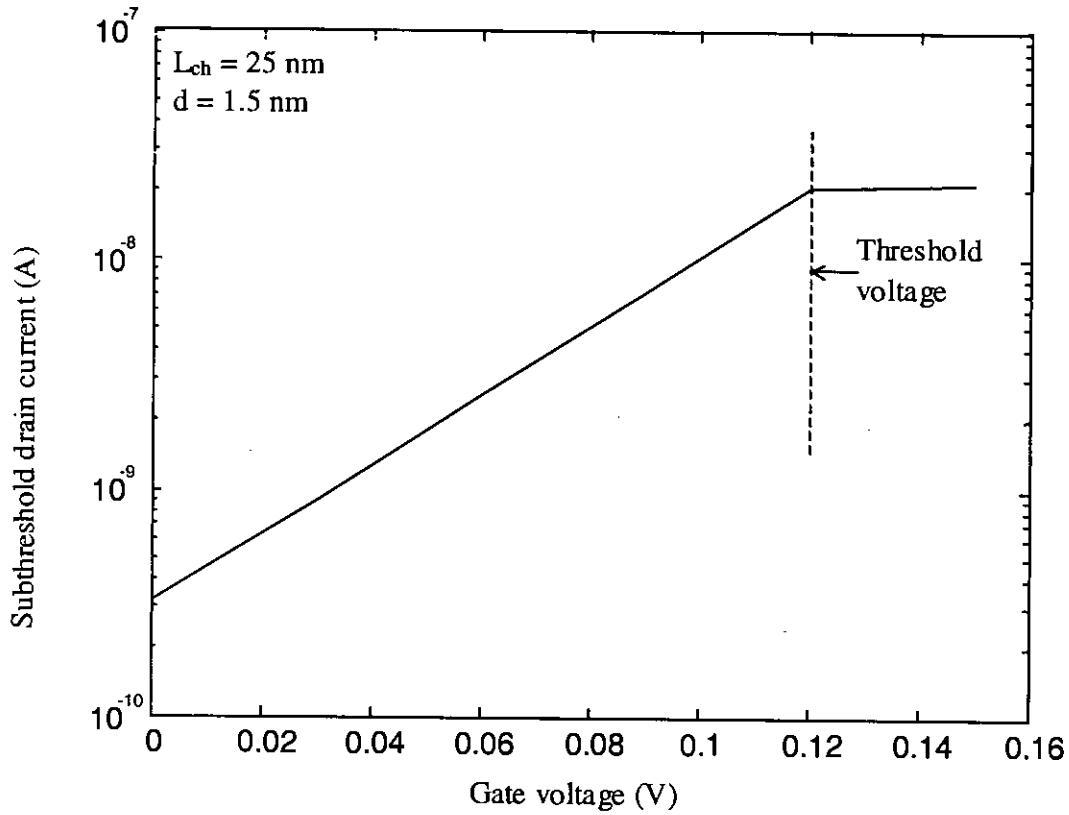


Fig. 4.17: Subthreshold drain current (L_{ch} = 25 nm, d = 1.5 nm MOSFET).

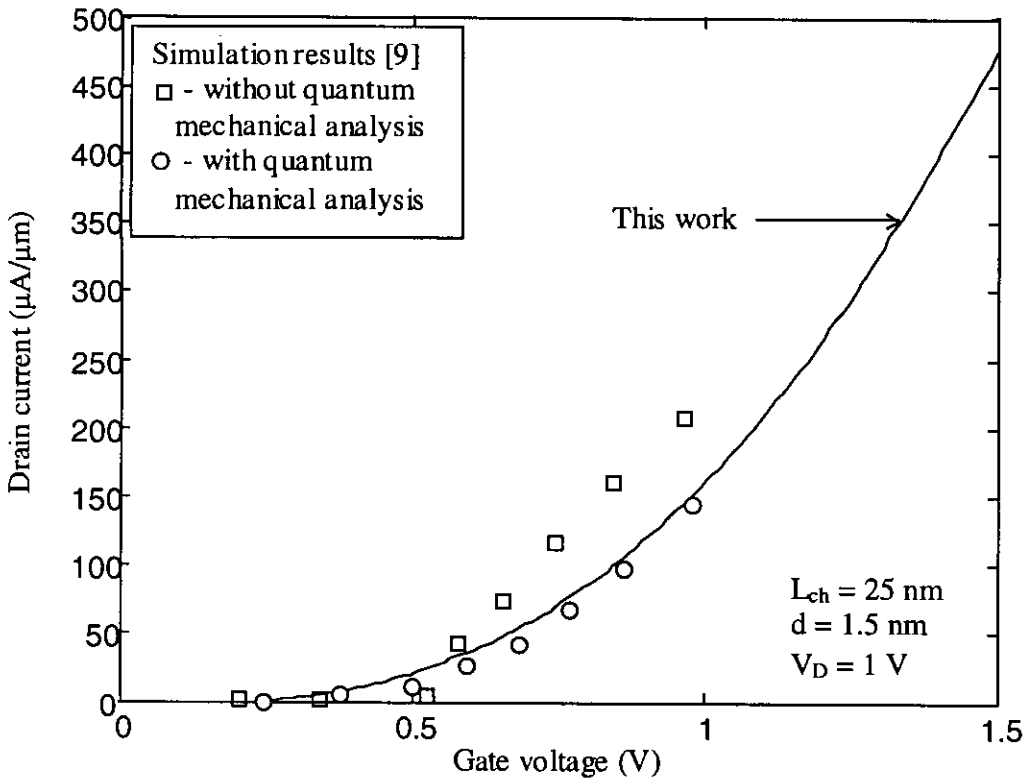


Fig. 4.18: Drain current versus gate voltage.

The drain current versus gate voltage characteristics or the transfer characteristics of n-channel MOSFET with 25 nm of channel length is shown in Fig. 4.18. White symbols represent data of quantum mechanical simulation result [9]. Black symbols represent simulated result without considering quantum mechanical effect [9]. From figure, it is seen that quantum analysis gives lower value of current than that obtained from barrier potential analysis. The quantization effects lead to threshold voltage increase of about 220 mV. The shift in the threshold voltage leads to a decrease in the on-state current by 30 % [9]. The transfer characteristics for the proposed model lies very close to the quantum mechanical simulation results, which shows the acceptability of the proposed model.

The I_D-V_G curve or the transfer characteristics in semi-logarithmic scale is shown in figure.

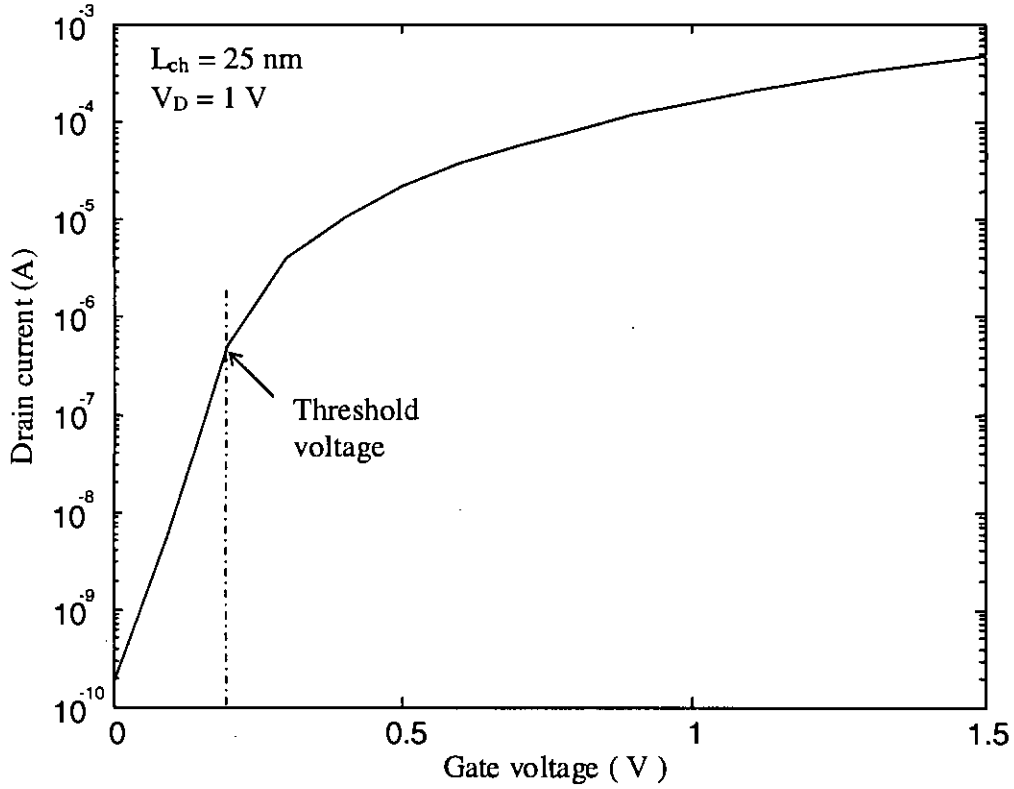


Fig. 4.19: Drain current versus gate voltage in semi log scale.

4.8.1.1 Effect of Drain Voltage

Effect of drain voltage on the output characteristics is shown in Fig. 4.20. It shows the effect of drain voltage on the drain current when plotted against the gate voltage of a nanoscale MOSFET with a channel length of 50 nm. One I_D -V_G curve is plotted for a fixed drain voltage. The upper curve is plotted for drain voltage of 1V. When lower drain voltages are applied, value of the drain current is decreased and the curves move

downward. Lower curves are plotted for drain voltages of 1V, 0.8V and 0.2V respectively.

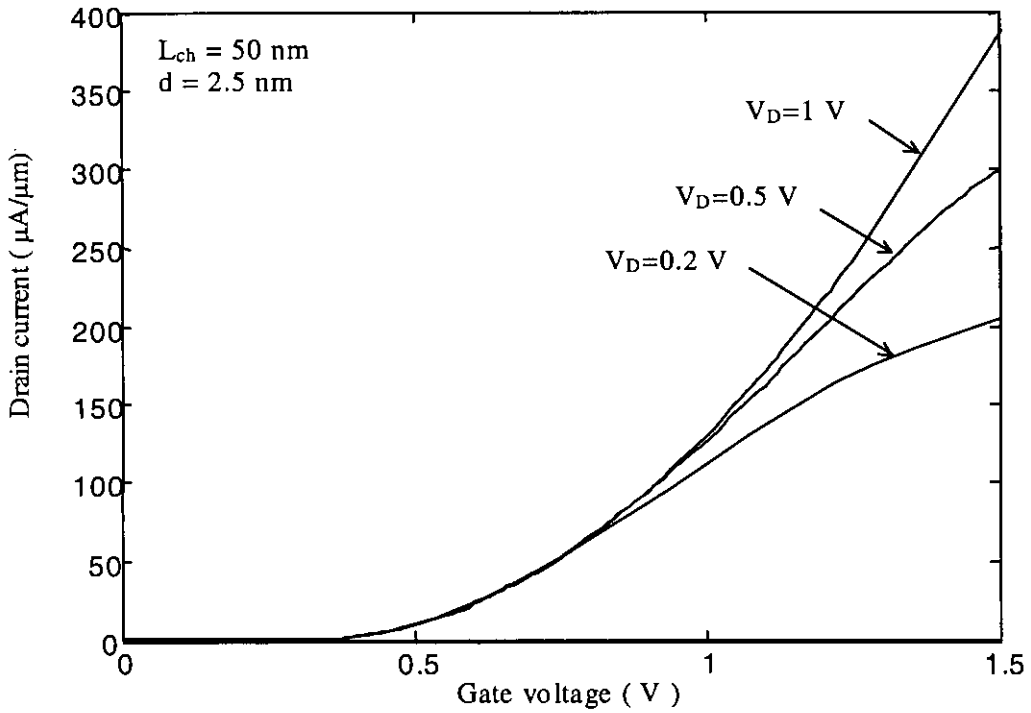


Fig. 4.20: Effect of drain voltage on drain current versus gate voltage.

4.8.1.2 Effect of Channel Length

The mobility of MOSFET strongly depends on the device channel length. Hence, the drain current is different when channel length is varied. Drain current plotted against the gate voltage for different channel lengths are shown in Fig. 4.21. The channel lengths are 90 nm, 70 nm, 50 nm and 25 nm. Current is higher for lower values of channel lengths. As the channel length is decreased, voltage required to turn on the device is reduced. The oxide thickness is 2.5 nm.

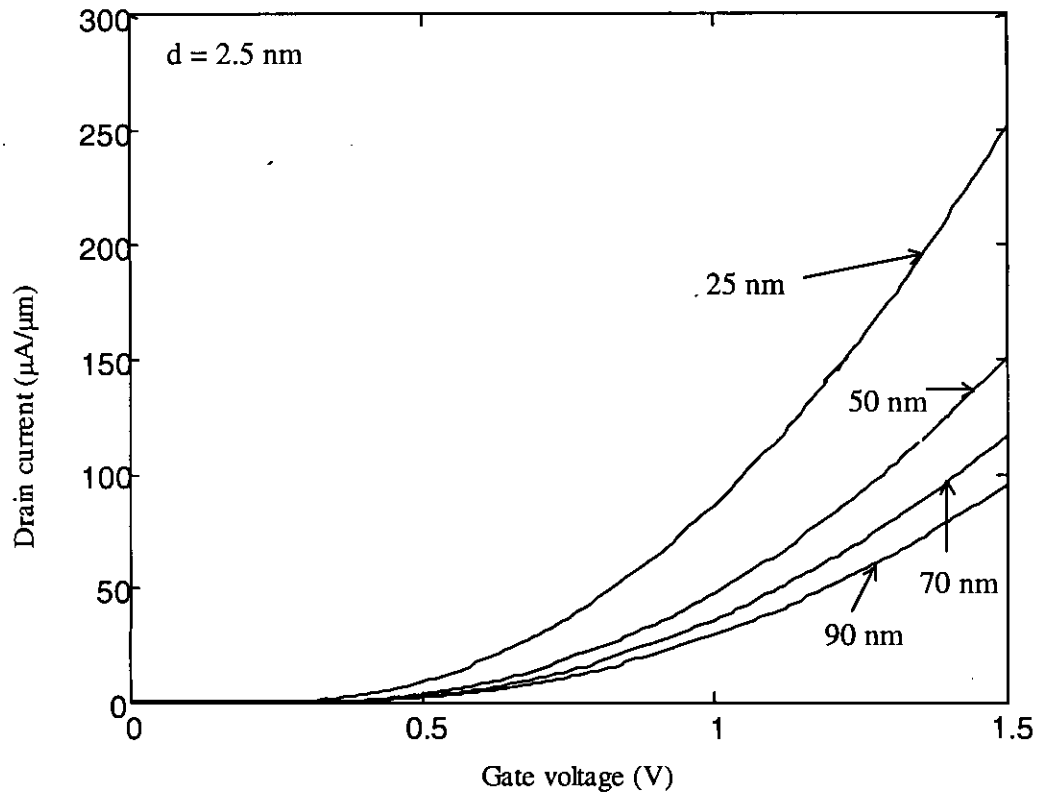


Fig. 4.21: Drain current versus gate voltage for different channel lengths.

4.8.1.3 Effect of Oxide Thickness

The gate current depends on the thickness of oxide. For thinner oxide, more charges are accumulated in the semiconductor/oxide interface and the drain current increases for the same amount of gate voltage. This is shown in the following figure.

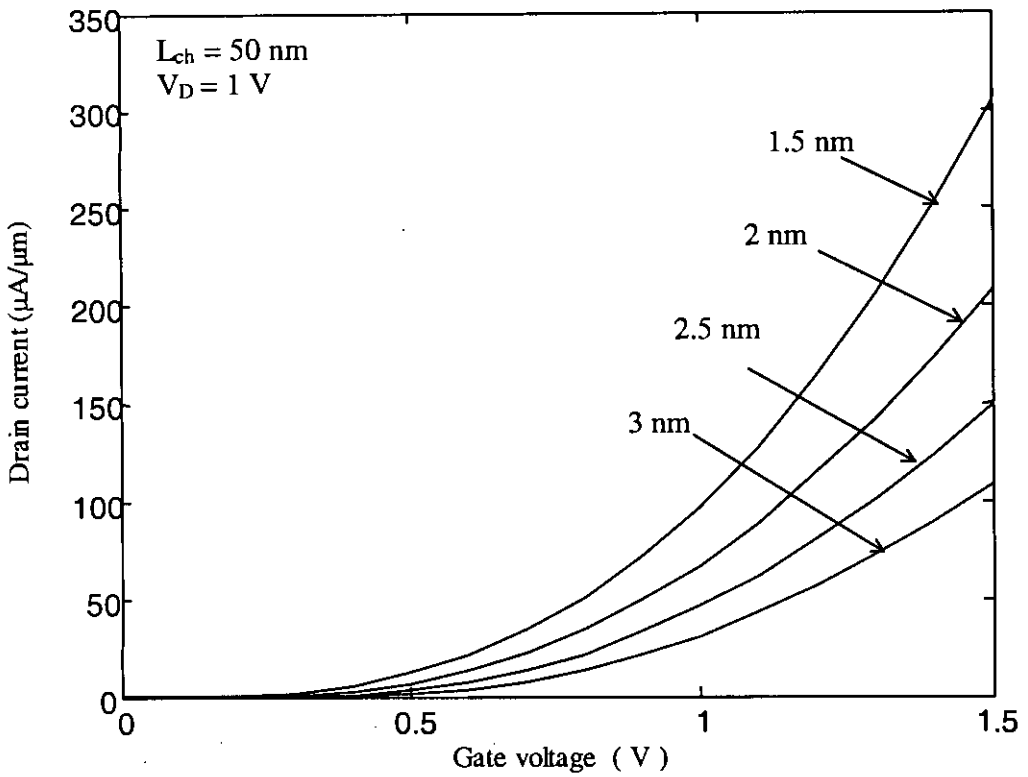


Fig. 4.22: Drain current versus gate voltage at different oxide thickness.

4.8.2 Output Characteristics (I_D - V_D)

The drain current of MOS device is proportional to the mobility of the inversion channel. At first the influence of the drain voltage on the mobility is considered. Figure 4.23 shows the effect of drain voltage on the effective mobility. Scattering in the inversion channel is very high at low drain bias. Carrier scattering at low bias plays an important role in the on-current of the device. As the drain bias in increased, the carriers cannot scatter as before and the mobility due to carrier scattering is limited.

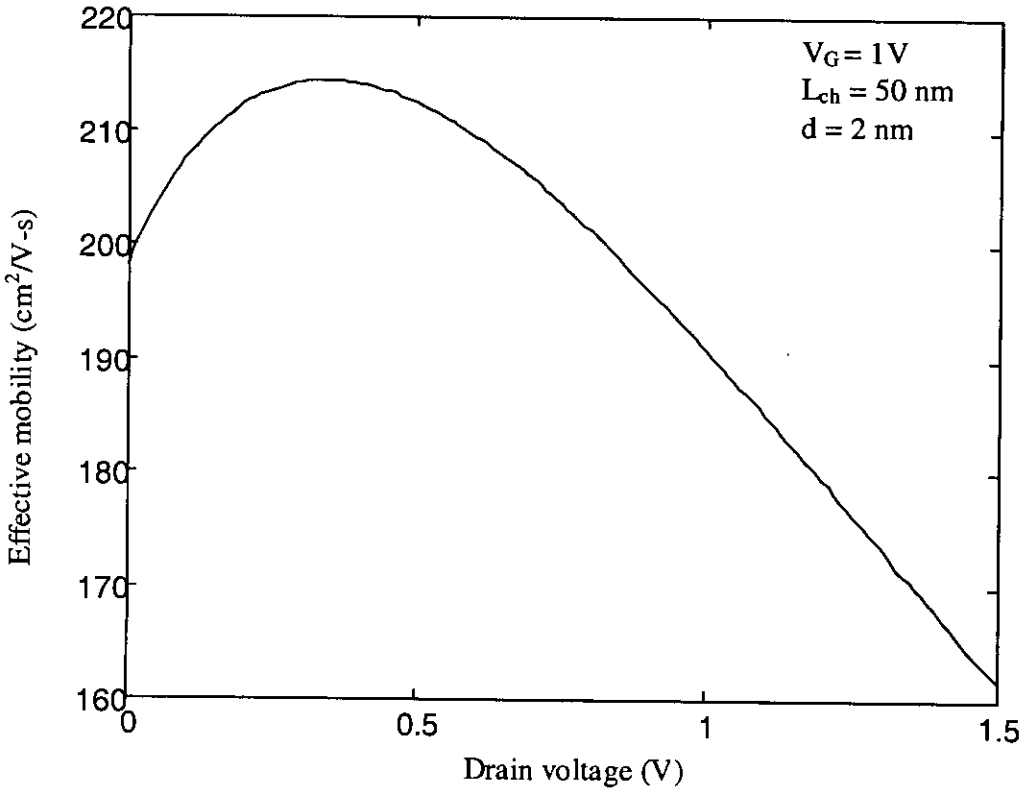


Fig. 4.23: Effective mobility as a function of drain voltage.

The drain current of an n-channel MOSFET with 50 nm of channel length is plotted in Fig. 4.24 considering the effect of mobility. The oxide thickness is taken as 2.5 nm and the gate voltage is 1V. An n-channel MOSFET with the same parameter is simulated by Choi [24] using nanoMOS simulator. The simulated values are shown as circles and interpolated on the output characteristics curve.

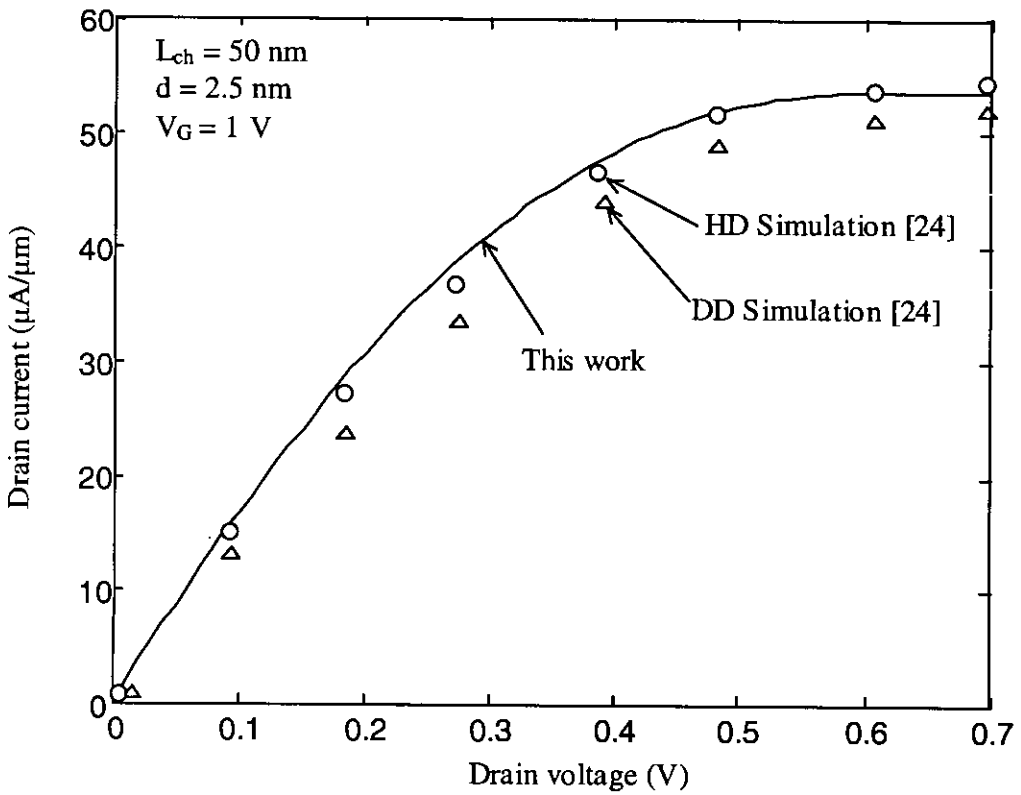


Fig. 4.24: Drain current versus drain voltage (output characteristics). The solid line is from the analytical models and the points are from nanoMOS simulations [24].

In the hydrodynamic (HD) model, the transport equations are derived taking moments of the Boltzmann transport equation (BTE), which are similar to the hydrodynamic flow equations of fluid dynamics [24]. The drift-diffusion model is a first-order approximation to the momentum balance equation; it ignores the spatial variation of the average carrier energy and assumes that the mobility is uniquely specified by the local electric field. The HD model includes the energy gradient in the current equation and assumes that the mobility is a function of the average carrier energy. The drift-diffusion (DD) approximation treats carrier transport in some average fashion, considering carriers to be in thermal equilibrium with the silicon lattice. The drift-diffusion model breaks down in

ultra-small devices where high fields and rapid spatial variations of the electric field are presented.

The transfer characteristics in semi log scale is plotted as shown in Fig. 4.25. The threshold voltage can be found from the curve at the point where the slope of I_D changes very sharply.

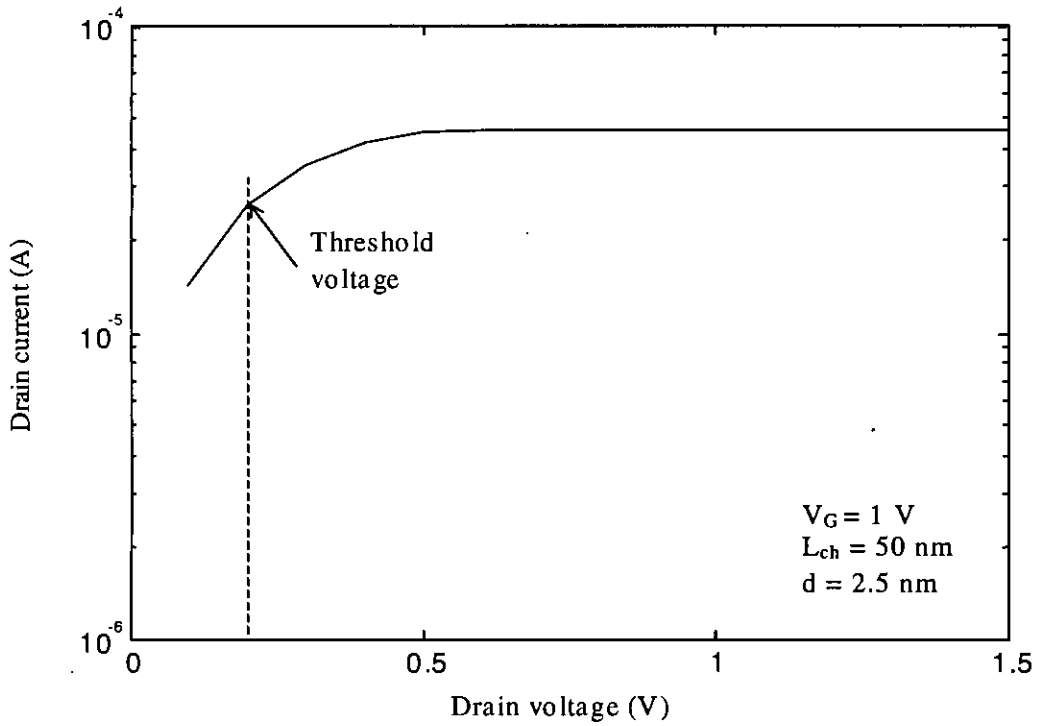


Fig. 4.25: Drain current versus drain voltage in semi log scale.

4.8.2.1 Effect of Gate Voltage

The drain current of an n-channel MOSFET whose effective channel length is 25 nm and physical oxide thickness is1.5 nm is simulated to observe the effect of gate voltage. The junction depth is 30 nm and the body thickness is assumed to be 45 nm. The parameters

of MOSFET are selected in order to compare with the available data of quantum mechanical analysis [18].

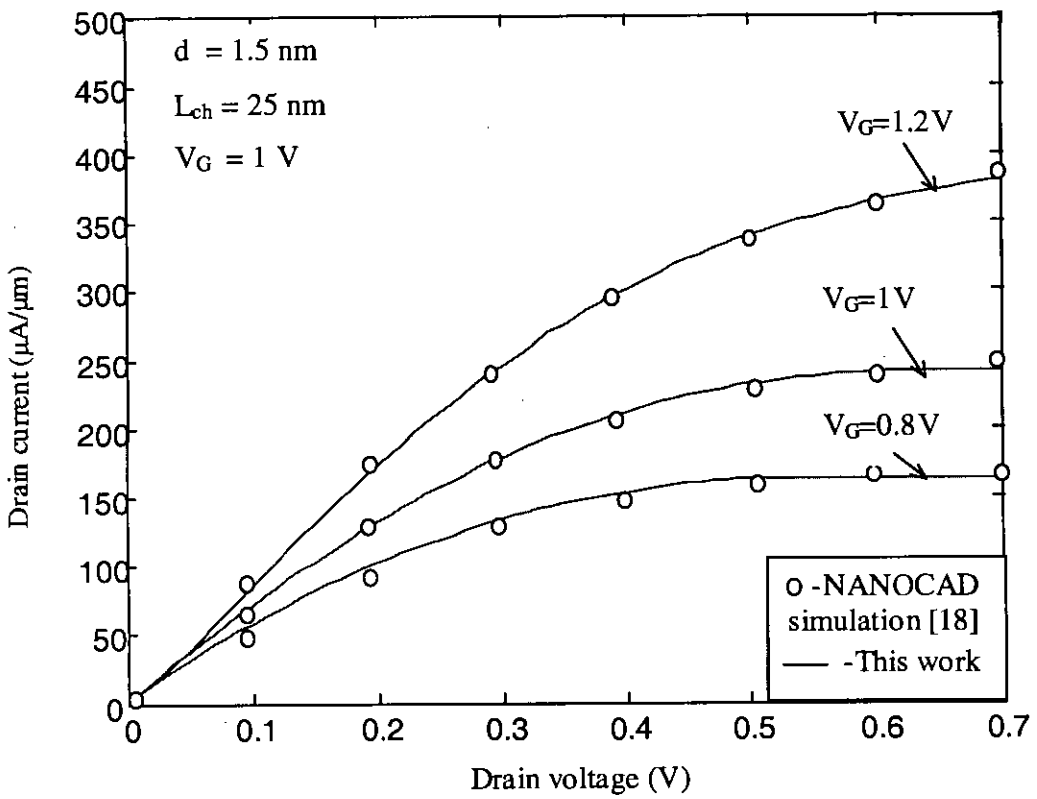


Fig. 4.26: Effect of gate voltage on output characteristics. Comparison of the I_D-V_D characteristics between developed model and NANOCAD simulation results [18].

Drain current versus drain voltage curve moves upward as the gate voltage is increased as shown in Fig. 4.26. The symbols (circle) represent the data obtained from NANOCAD program, which is used for the modeling and simulation of carrier transport in nanoscale MOSFET devices including quantum-mechanical effects [18]. The simulation in NANOCAD used DG (Density-gradient) model including an effective quantum potential in the drift term.

The saturation current increases for higher bias as seen from the above figure. The locus of saturation is shown in Fig. 4.27.

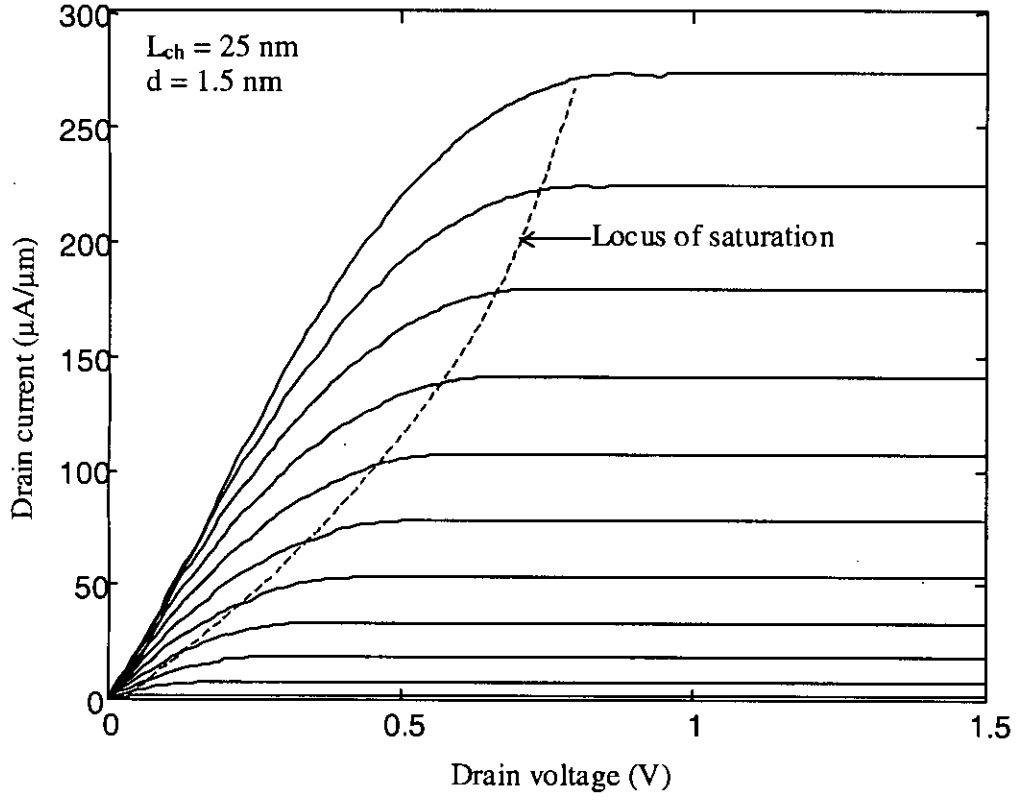


Fig. 4.27: Locus of saturation from the output characteristics. (V_G = 1.2 V, 1.1 V, 1 V, 0.9 V, 0.8 V, 0. 7 V, 0.6 V, 0.5 V, 0.4 V, 0.3 V, 0.2 V).The dashed line represents the locus of saturation drain current.

4.8.2.2 Effect of Channel Length

The drain current versus drain voltage is plotted in Fig. 4.28 for different channel lengths at an oxide thickness of 2.5 nm. As the channel length is decreased, the drain current is increased. The saturation voltage (drain) decreases for decreasing the channel length.

Drain current reaches to its saturation value earlier for device with decreased channel length.

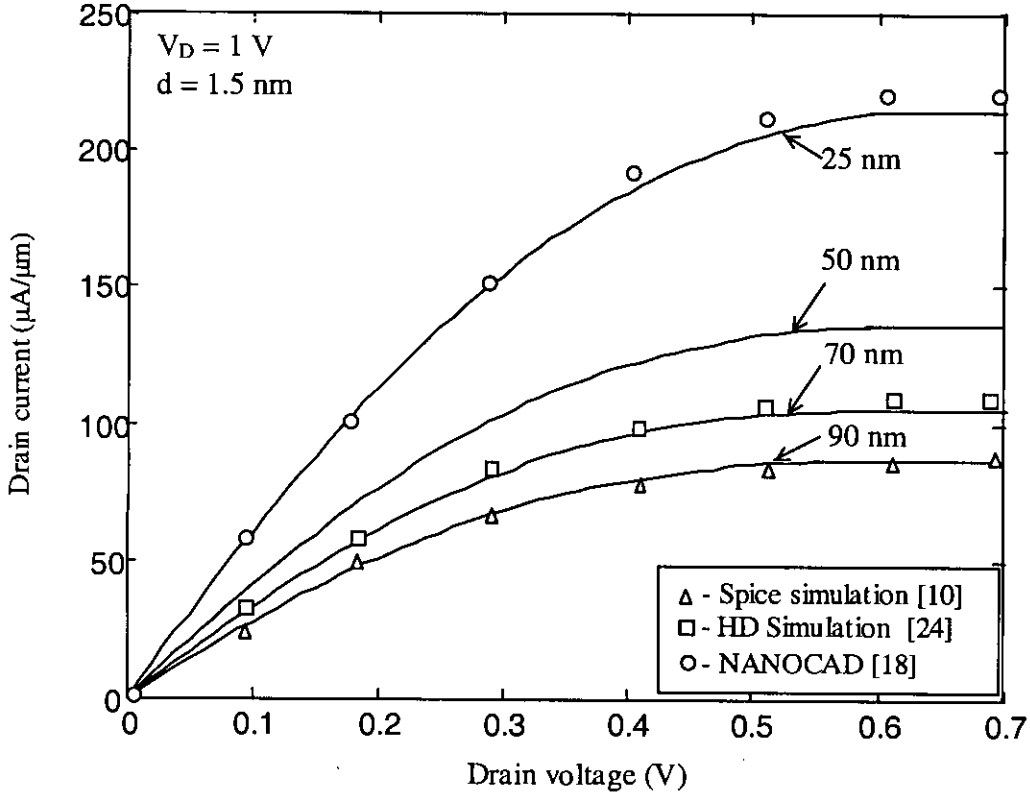


Fig. 4.28: Effect of channel length on the output characteristics.

The proposed model has been compared with various simulation results. The lowest curve stands for the output characteristics curve of 90 nm MOSFET. This I-V curve is compared with the SPICE simulation result done by Khafaji [10]. The proposed model shows good agreement with the simulation data.

The drain saturation current for shorter channel length is higher. This is shown in Fig. 4.29, where, saturation current is plotted against channel length and compared with Choi's simulation [17]. Some data lie on the curve drawn using the proposed model.

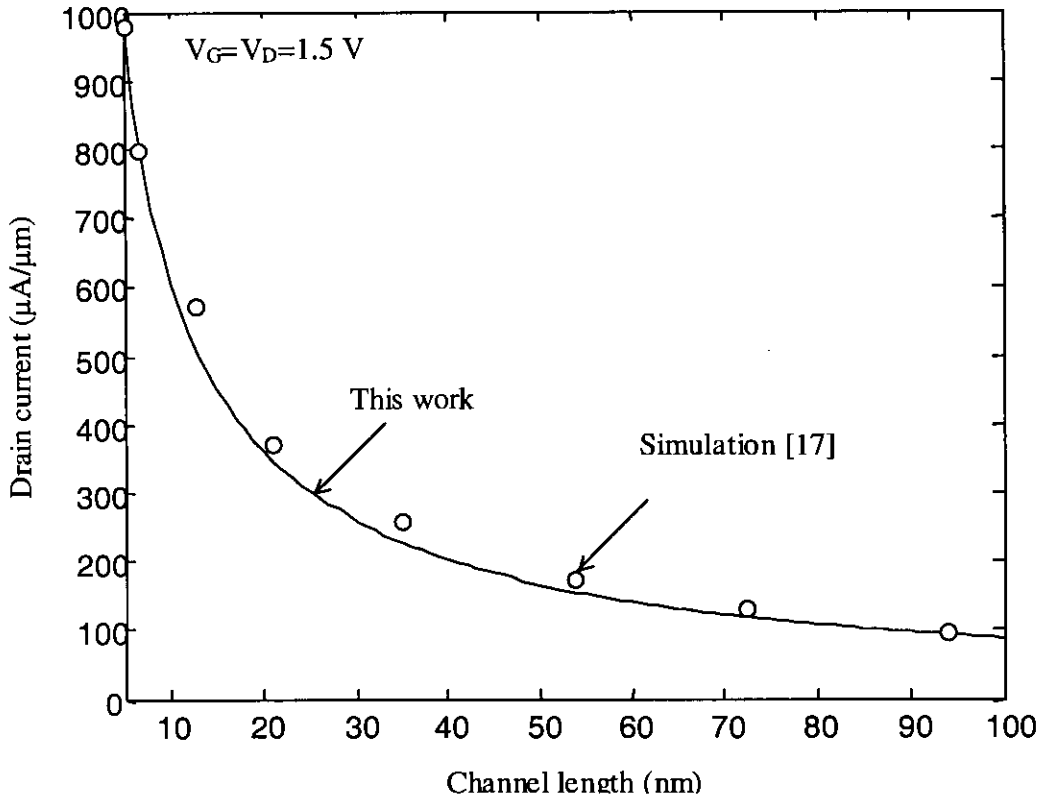


Fig. 4.29: Saturation drain current versus channel length.

4.8.2.3 Effect of Oxide Thickness

Drain current is highly affected by the thickness of oxide. As the oxide thickness is decreased, more charges are gathered in the Si/SiO_2 interface. So the inversion layer charge concentration increases, resulting in an increase in drain current as shown the following figure.

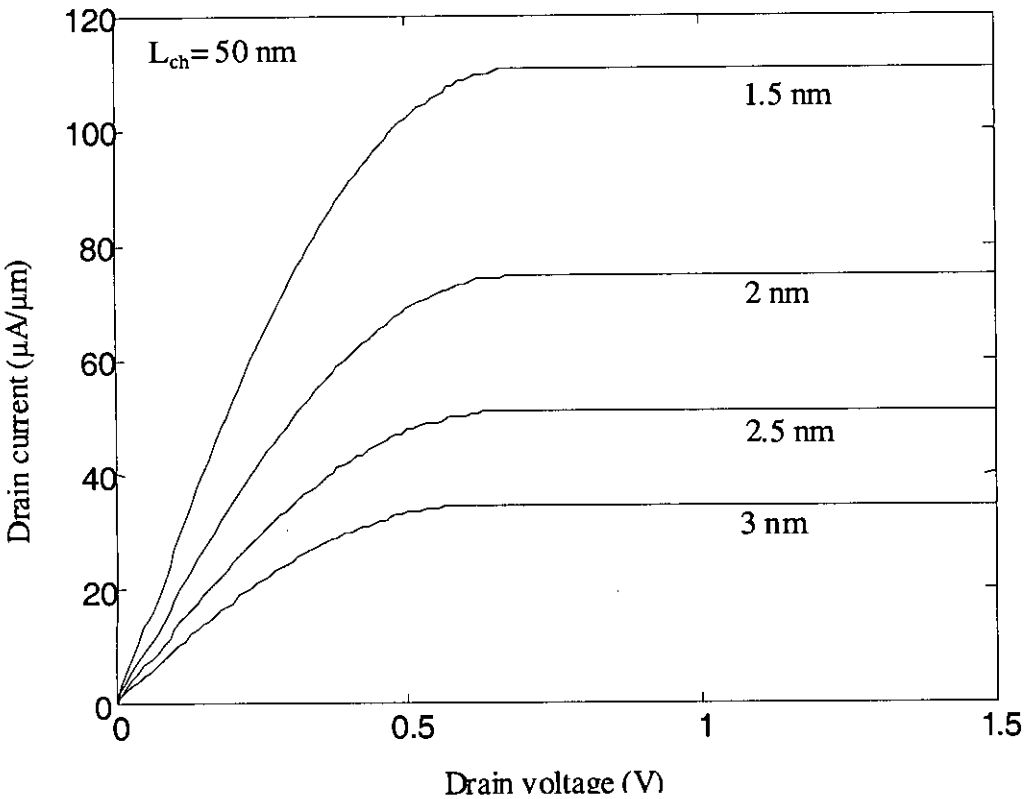


Fig. 4.30: Effect of oxide thickness on the output characteristics.

Chapter 5

Conclusions

5.1 Summary

There are a number of issues in scaling MOSFET devices, particularly for the sub-100 nm technology evolution. Even though Monte Carlo device simulation has been established as a powerful tool for the investigation of ballistic effects in deep submicron MOSFETs, its excessive computation time is a burden for practical design applications [21].

This thesis addresses device physics, modeling and design issues of nanoscale transistors. A simple drain current model considering the carrier transport in the inversion channel is presented. To model the carrier scattering in the channel region, new expressions for mobility are developed using semi-classical approach. This approach provides improved physical insight of carrier transport in nanoscale devices and shows good agreement with the device simulation results.

The effective mobility has been measured in the inversion channel of n-channel MOSFETs by means of calculating the effective electric field. The same expressions can be used for measuring inversion layer mobility and hence drain current of p-channel nanoscale MOSFETs if the value of η is taken as 1/3.

The remote surface roughness scattering is an important scattering mechanism that should be taken into account when oxide thickness is thin enough. In this mobility model,

mobility limited by remote surface roughness scattering has not been considered. However, when Coulomb scattering is considered, the effects of this new scattering source are partially masked by the contribution of Coulomb scattering [13].

The device structure studied is MOSFET, with extremely scaled channel lengths (90 nm, 70 nm, 50 nm, 25 nm) and oxide thickness (1.5 nm to 3 nm). A good fit is obtained for the subthreshold, linear, and saturation regions of the I-V characteristics. No additional assumptions are made to fit the subthreshold and saturation currents. This agreement between the theoretical and experimental *I-V* curves serves as a verification of the new mobility model developed in this work.

Limitations of gate length reduction in terms of the suppression of short channel effects are estimated to be around 25 nm [21]. In the ultra-short-channel device regime, the drift-diffusion model breaks down, especially where rapid spatial variations of potential are observed. In such cases, the scattering events are no longer localized, and carriers may acquire excess thermal energies near the drain. These carriers are not in thermal equilibrium with the silicon lattice, which is referred to hot carrier effects. Under these circumstances, it is possible for the carrier velocity to exceed the saturation velocity, which is so called velocity overshoot.

The results show that the physics that determines the steady-state current of a MOSFET can be understood in terms of a simple model. This view of nanoscale MOSFET device physics should provide a useful guide for experimental and theoretical work, for developing compact models, and for interpreting detailed simulations.

5.2 Recommendation for Future Works

For the future study of the present work, suggestions for several topics are as follows:

Other scattering mechanisms can be included in this model. A more rigorous treatment of carrier transport under spatially non-uniform high-field conditions can be modeled using quantum mechanical analysis. The scattering mechanisms can be classified into the phase breaking scattering mechanisms and the coherent scattering mechanisms. The phonon scattering considered in this work is one of the phase breaking scattering mechanisms, whereas the Coulomb scattering and the surface roughness scattering are coherent scattering mechanisms. The remote surface roughness scattering can be added to the mobility modeling, specially when the oxide thickness is less than 2 nm. In principle, we can include the coherent scattering mechanism by adding "static" perturbation potential to the external potential, which will give the characteristics of individual devices. Alternatively, we can consider the ensemble of devices, and include the average effect of coherent scattering mechanisms in the simulation.

The effect of strain and crystal orientation can also be included, which are practically important nowadays, since they can be utilized to enhance the performance of the transistors.

The gate tunneling current can be modeled in order to determine directions of future gate oxide scaling. When a large positive bias is applied to the gate electrode, electrons in the strongly inverted surface can tunnel through the oxide layer and hence produce a gate current. Similarly, if a large negative voltage is applied to the gate electrode, electrons from the n^+ polysilicon can tunnel in the opposite direction. Very thin gate oxides are required for sub-100 nm generations. For such thin oxides, gate leakage current due to direct tunneling becomes unacceptably large.

This model can be used as a verification tool of other simplified transport models. For example, the drift-diffusion model is still the most popular transport model in the

industry, and it will keep its role in the near future. Therefore, this model can guide its extendability and limitation. On the other hand, we can develop more accurate transport model that includes the quantum effects as well as the effects of the quasi-ballistic transport with the help of the model developed.

To farther develop this circuit model, several additional factors have to be addressed (e.g. 2D electrostatics and the influence of degenerate carrier statistics on the critical channel length). New models of this class can provide a useful conceptual guide for device development as well as circuit models for new, unconventional transistors.

The demand for new material and technologies becomes increasing in the nanometer CMOS regime. Hence, understanding of mobility enhancement in the germanium strained silicon, reliability and mobility degradation in the high-k gate dielectrics, and various device parameters in the metal electrodes are required. Scaling CMOS towards the 25 nm channel length generation requires innovative device structures to circumvent barriers due to the fundamental physics in the conventional MOSFETs. These are SOI, back-gate FET, double-gate FET and FinFET. Fundamental issues for these structures such as the physics of carrier transport in very thin silicon channel must be further understood.

List of References

[1] Z Ren.," Nanoscale MOSFETs: Physics, Simulation and Design," Ph.D. Thesis, Pardue University, 2001.

[2] Moore's Law. Available at: http://norrie.files.wordpress.com//moores-law.png, 2008.

[3] Y. Taur, H. Morkoc," A View of Nanoscale Electronic Devices, " *Journal of the Korean Physical Society*, vol. 42, pp. 555-573, 2003.

[4] A. Rahman., M Lundstrom.," A Compact Model for the Nanoscale Double Gate MOSFET, " *IEEE Trans . on Electron Devices.*, 2001.

[5] M Lundstrom.," Fundamentals of Carrier Transport, " 2nd edition, Cambridge University Press, Cambridge, UK, 2000.

[6] M Lundstrom.," Elementary Scattering Theory of the Si MOSFET, " *IEEE Electron Device Letters*, vol. 18, pp. 361-363,1997.

[7] S. Takagi, A. Toriumi, M. Iwase, H. Tango," On the University of Inversion Layer Mobility in Si MOSFET 's: Part I-Effects of Surface Impurity Concentration, " *IEEE Trans. on Electron Devices*, vol. 41, pp. 2357-2362,1994.

[8] S. Takagi, A. Toriumi, M. Iwase, H. Tango," On the University of Inversion Layer Mobility in Si MOSFET 's: Part II-Effects of Surface Orientation," *IEEE Trans. on Electron Devices*, vol. 41, pp. 2363-2368,1994.

[9] D. Vasileska, H. R. Khan, S. S. Ahmed," Quantum and Coulomb Effects in Nanodevices, " *International Journal of Nanoscience*, vol. 4, pp. 305–361, 2005.

[10] M. M. Khafaji, M. Kamarei, B. Forouzandeh,"Modified Analytical Model for Subthreshold Current in Short Channel MOSFETs," *IEICE Electronics Express*, vol. 4, pp.114-120, 2007.

[11] C. L. Huang, Sh. Gennady, Gildenblat," Measurements and Modeling of the n-Channel MOSFET Inversion Layer Mobility and Device Characteristics in the Temperature Ranee 60-300 K," *IEEE Trans. on Electron Devices*, vol. 37, pp. 1289-1300, 1990.

[12] S. M. Sze," Physics Of Semiconductor Devices, " Second Edition, John Wiley & Sons, Singapore.

[13] B. C. Paul, A. Raychowdhury, K. Roy," Device Optimization for Digital Subthreshold Logic Operation,"*IEEE Trans. on Electron Devices*, vol. 52, pp. 337-347, 2005.

[14] F. Gamiz, J. A. Lopez-Villanueva, J. E. Carceller, P. Cartujo,"Universality of Electron Mobility Curves in MOSFETs: A Monte Carlo Study," *IEEE Trans. on Electron Devices*, vol. 42, pp. 258-265, 1995.

[15] K Huet., J. Saint-Martin, A. Bournel, S. Galdin-Retailleau, P. Dollfus, G. Ghibaudo and M. Mouis, " Monte Carlo Study of Apparent Mobility Reduction in Nano-MOSFETs," *37th European Solid State Device Research Conference, 2007.* ESSDERC Volume , pp. 382 – 385, 2007.

[16] M. S. Shur, " Low ballistic mobility in submicron HEMTs, " *IEEE Electron Device Letters.*, vol. 23, pp. 511-513, 2002.

[17] Y. J Choi., " CMOSFET below 0.1 μm: Suppression of Short Channel Effect, " SMDL Annual Report, *School of Electrical Engineering, Seoul National University*, 1998.

[18] S. Jin, C. H. Park, I. Y. Chung, Y. J. Park, H. S. Min, "NANOCAD Framework for Simulation of Quantum Effects in Nanoscale MOSFET Devices," *Journal of Semiconductor Technology and Science*, vol. 6, 2001.

[19] T. A. Fjeldly and M Shur., "Threshold voltage modeling and the subthreshold regime of operation of short-channel MOSFETs," *IEEE Trans. on Electron Devices*, vol. 40, pp137–145, 1993.

[20] H. S. Huang, S. Y. Chen, Y. H. Chang, H. C. Line, W. Y. Lin, "TCAD Simulation of Using Pocket Implant in 50nm N-MOSFETS," 2004 *International Symposium on Nano Science and Technology,* Tainan, Taiwan, 2004.

[21] X. Zhou, K. Y. Lim, D. Lim, "A General Approach to Compact Threshold Voltage Formulation Based on 2-D Numerical Simulation and Experimental Correlation for Deep-Submicron ULSI Technology Development," *IEEE Trans. on Electron Devices*, vol. 47, pp 214–221, 2000.

[22] J. Walczak, J. Majkusiak," Electron mobility and drain current in strained-Si MOSFET," available at: *http://www.nit.eu/czasopisma/JTIT/3/84*.pdf, 2007.

[23] F. Andrieu, "Transistors CMOS décananométriques à canaux contraints sur silicium massif ou sur SOI", Ph. D. thesis, CEA-LETI, Inst. Nat. Polytech. Grenoble, Grenoble, France, 2005.

[24] C. Choi, "Modeling of Nanoscale MOSFETS," Ph.D Thesis, Stanford University, 2002.

[25] S. Jin, "Modeling of Quantum Transport in Nano-Scale MOSFET Devices," Ph.D. dissertation, Seoul National University, 2006.

[26] A. Svizhenko and M. P. Anantram," Role of scattering in nanotransistors," *IEEE Trans. Electron Device*s, vol. 50, pp. 1459-1466, 2003.

[27] J. Saint Martin, A. Bournel, and P. Dollfus," On the ballistic transport in nanometer-scaled DG MOSFETs," *IEEE Trans. Electron Device*s, vol. 51, pp. 1148-1155, 2004.