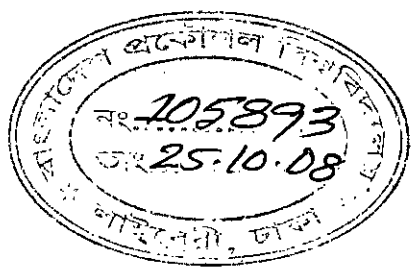
Analytical Modeling of Threshold Voltage of Deca-nano n-MOS Transistor

A thesis submitted to the Electrical and Electronic Engineering Department of BUET, Dhaka. in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronic Engineering**



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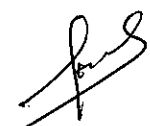

(Fouzia Ferdous)

CONTENTS

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ABSTRACT

The conventional threshold voltage model is derived for the homogeneous doping concentration. As the channel length of MOSFETs is scaled down to deep-submicrometer or sub-100 nm regime, we observe short-channel effects, such as, steep threshold voltage roll-off, increased off-state leakage current and bulk punch-through. The short channel effects arise as results of two dimensional potential distribution and high electric fields in the channel region. Lateral channel engineering utilizing halo or pocket implant surrounding drain and source regions is effective in suppressing short channel effects. An extension of the homogeneous model to the nonhomogeneous impurity pileup in the vertical direction has been reported previously. However, the reported model cannot be extended further to the pocket implantation, where inhomogeneity along the channel is the main cause for the reverse short channel effect. A strong reverse short channel effect suppresses the short channel effect on threshold voltage of the MOSFET. Another threshold voltage model for pocket implanted MOSFETs with resolving circuit simulation based on simplified pocket implanted profile, does not describe the case of sub-100 nm. Extrapolation of the threshold voltage versus gate length curve cannot predict the threshold voltage accurately. Therefore, we propose a threshold voltage model that describes the threshold voltage for the gate length down to 50 nm. Advanced MOSFETs are non-uniformly doped as a result of complex process flow. Therefore, one of the key factors to model threshold voltage (V_{th}) accurately is to model its non-uniform doping profile of the MOSFET. The focus here is to transform the lateral 1-D pocket profile across the channel to an effective doping concentration expression that can be applied directly to the V_{th} expression incorporating V_{th} shift due to short channel effect in the model to suppress the short channel effect. There are other pocket profiles found in the literature, such as, Gaussian distribution, hyperbolic cosine profile etc. for the threshold voltage model of the MOS devices. Our simulation results are compared with the simulation results using these pocket profiles for various device and pocket profile parameters. The comparison shows

that the proposed model has a simple compact form that can be used to study and characterize the pocket implanted advanced ULSI devices down to 50 nm gate length. It also proves the validity and usefulness of our proposed model of the threshold voltage for circuit simulation. Our model is also compared with experimental data.

LIST OF SYMBOLS

V_{th}	Threshold voltage of MOSFET
V_{FB}	Flat–band voltage of the MOSFET
V_{BS}	The substrate voltage with respect to the source
ψ_s	The surface potential
ψ_B	The bulk potential of semiconductor
Q_f	Fixed charge density
C_{ox}	Oxide capacitance
N_{pm}	Peak doping concentration
N_{sub}	Doping concentration of substrate
N_{eff}	Effective pocket concentration
n_i	Intrinsic doping concentration
φ_{ms}	Metal semiconductor work function difference
$\rho(x)$	Space charge density
L_p	The pocket length
L	The channel length/gate length
ΔV_{th}	Threshold voltage shift
Wm	The maximum width of depletion region
r_j	The junction depth

Chapter 1

INTRODUCTION

1.1 Introduction

A MOSFET (n-channel) consists of a p-type semiconductor substrate into which two n regions, the source and the drain, are formed. The region between the source and the drain is called the channel and it is separated from the metal gate electrode by an insulating oxide layer. The gate voltage determines the degree of inversion of the channel and hence controls the conductivity of the device. The MOS device is simpler to fabricate and its dimensions can be reduced to extremely small values. The principal applications of MOSFETs are in VLSI technology, specially in case of digital systems such as semiconductor memories, long shift registers, microprocessors etc. In digital applications the device is operated either in saturation or cut-off and the threshold voltage becomes an important parameter.

1.2 Threshold Voltage of MOSFETs

The threshold voltage of a MOSFET is usually defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor.

In an n-MOSFET the substrate of the transistor is composed of p-type silicon which has positively charged mobile holes as carriers. When a positive voltage is applied on the gate, an electric field causes the holes to be repelled from the interface, creating a depltion region containing immobile negatively charged acceptor ions. A further increase in the gate voltage eventually causes electrons to appear at the interface, in what is called an inversion layer, or channel. Historically the gate voltage at which the electron density in the interface

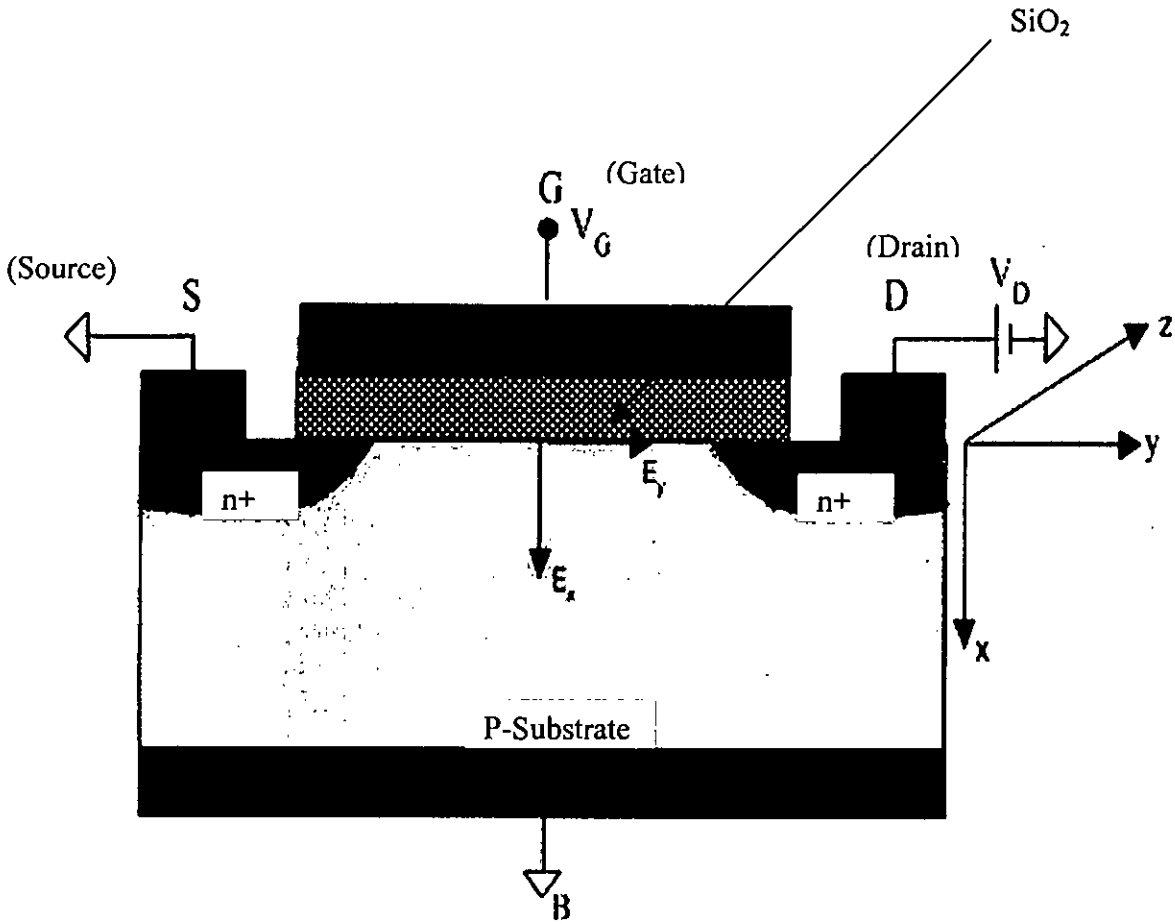

Fig 1.1 n-MOSFET Structure

is the same as the hole density in the neutral bulk material is called the threshold voltage. Practically speaking the threshold voltage is the voltage at which there are sufficient electrons in the inversion layer to make a low resistance conducting path between the MOSFET source and drain.

In the fig.1 the source and drain are labeled n^+ to indicate heavily doped n-regions. The depletion layer dopant is labeled N_A^- to indicate that the ions in the depletion layer are negatively charged and there are very few holes.

If the gate voltage is below the threshold voltage, the transistor is turned off and ideally there is no current from the drain to the source of the transistor. In fact, there is a current even for gate biases below threshold, although it is small and varies exponentially with gate bias.

If the gate voltage is above the threshold voltage, the transistor is turned on, due to there being many electrons in the channel at the oxide-silicon interface, creating a low-resistance channel where current can flow from drain to source. For voltages significantly above threshold, this situation is called strong inversion. The channel is tapered when $V_D > 0$ because the voltage drop due to the current flowing in the resistive channel reduces the oxide field supporting the channel as the drain is approached.

1.3 Short-channel effects

When the total depletion region formed by the source and the drain of a MOSFET becomes comparable to its channel length, it is defined to be a short channel device. In this case, considerable portion of the depletion layer is influenced by the source/drain and the 'edge' effects along these two sides are needed to be considered.
The lateral electric field produced by the drain to source voltage becomes stronger as the

channel length decreases. Horizontal component of the electric field, which is neglected in long channel analysis becomes significant in short channel devices. The perturbation of the vertical electric field lines by the lateral fields results in decrease in the threshold of a short channel MOSFET.

For short-channel MOSFETs, a considerable portion of the channel is occupied by the source and drain. The gate voltage therefore depletes the region under the inversion layer up to more depth. The deeper the depletion region is accompanied by a large surface potential, which makes the channel more attractive for electrons. As a result, the device shows more conductivity than what would be predicted from long channel theory for a given V_{GS} and thus the threshold voltage is decreased. The depletion region under the channel can also be widened and the corresponding surface potential can be increased, by raising the potential of the drain (Fig-1.1). Hence, the threshold is also a decreasing function of V_{DS}. An increase in surface potential corresponds to a decrease of potential energy barrier to the entrance of electrons in the channel and thus this concept of describing the short-channel effect on threshold voltage is called " barrier lowering" effect [1].

1.4 Review of recent works on threshold voltage of conventional MOSFET

The very large scale integration (VLSI) of MOS circuits has resulted in miniaturization of the MOSFET device. Recent works on threshold voltage have thus concentrated on short-channel devices. In last two decades, a large number of analytical/empirical models were developed for short channel devices using the technique of 'charge sharing' [1]-[8] these models are based on the sharing of depletion charge under the gate between the gate and the drain, gate and the source. The models differ from each other with respect to the geometrical shape for the boundary of the charge induced by the gate and the procedure to calculate the area of the geometrical shape. Each model contains refinements for a more accurate derivation of the average depletion charge density for the gate induced depletion region.

Taylor [9] proposed an improved charge-sharing model in which the drain and source diffusions are described as cylindrical junctions. The accuracy of the charge sharing models are limited by the arbitrary division of charge between the gate, the source and the drain .In last few years, two dimensional numerical analysis has been used to investigate many device parameters [10]-[11]. However such analysis, although accurate, needs excessive computing time and do not provide a simple model of efficient calculation. Recently, the analytical techniques to characterize short channel MOSFETs have been obtained by solving the two dimensional Poission's equation with approximate boundary conditions. However the accuracy of the analytical solution of Poission's equation is strongly dependent on the simplified assumptions used in the derivation. Toyabe et.al. [12] derived an analytical threshold voltage model based on a quasi –two dimensional Poisson's equation ; however, they introduced some arbitrary constants to give the best fit in certain ranges of process parameters. Further improvements in this direction proposed, in which the effects of source drain junction depth were included and no empirical constants were required.

1.5 Review of recent works on threshold voltage of pocket implanted MOSFET

Advanced MOSFETs are nonuniformly doped as a result of complex process flow. Therefore, one of the key factors to model threshold voltage (V_{th}) accurately is to model its non-uniform doping profile. Currently there are many V_{th} models [12]-[17], [35]-[36] that are able to model the vertical non-uniform doping profile of a MOSFET. However, all the V_{th} models are lateral non-uniform doping profiles due to reverse short channel effect (RSCE) [18]-[23] are empirical, which are normally modeled by simply adding exponential functions to its long channel V_{th} expression. In one of the threshold voltage models with reverse short channel effect there is 2-D pile up profile across the channel to an effective doping expression and applied direct to V_{th} expression. It is very abrupt in turn, is unphysical to actual transistor structures [24], [33]-[34].

The RSCE due to the pocket implant is much stronger than that due to unintended impurity pile up caused by the interstitial movement [25]-[26]. The impurity pile up mainly

induces a vertical inhomogeneity located beneath the SiO_2 /Si interface near source and drain, and the induced RSCE caused by the pocket implantation, is clearly above 100 mV. Previous attempts for including the strong RSCE due to the pocket implantation in to a circuit simulation model were done by introducing model parameters without connection to the pocket profile (Ref.[27]).Another V_{th} model for pocket implanted MOSFET – which is mainly targeted at resolving the circuit simulation issue on the basis of a simplified pocket implant profile. This V_{th} model reproduces measured V_{th} even in its simplified form within inaccuracy of a few millivolts [28]. Another model for anomalous bchaviors but suitable for use in compact modeling in analog devices [29].

Other threshold voltage model for pocket implanted MOSFETs with resolving circuit simulation based on simplified pocket implanted profile, does not describe the case of sub 100-nm.[30]-[32],[37]-[39] and from extrapolation of the threshold voltage versus gate length curve we get channel length down to 50 nm. The focus here is to transform the lateral 1-D pocket profile across the channel to an effective doping concentration expression that can be applied directly to the V_{th} expression. There are pocket profiles found in the literature such as Gaussian distribution, hyperbolic cosine profile etc. for the threshold voltage model of the MOS devices. Our proposed model efficiently determines the threshold voltage of scaled MOSFETs having channel lengths in sub-100 nm regime. The simulated results by changing various device and pocket profile parameters are shown with verification from basic concept.

1.6 Objective of the work

The objective of this work is to derive an analytical model of V_{th} for pocket implanted nMOSFET . The result is compared with the other pocket profiles used to derive the threshold voltage models of nMOSFETs. The model is verified with experimental reported data also. Here, we are deriving a model which will describe gate length down to 50 nm. Currently there are many threshold voltage models that are able to model vertical non-uniform doping profile of a MOSFET. However, all the threshold voltage models due to reverse short channel effect are empirical. Some are abrupt in turn and some are unphysical to actual transistor structure and do not describe the case of sub 100 nm. Our model

efficiently determines the threshold voltage of scaled nMOSFETs having channel length sub100nm regime.

1.7 Organization of the thesis

Several models have been developed recently to determine the threshold voltage of MOSFETs. Different approaches are used by different authors to consider the short channel effects. In this thesis, 1-D Poisson's equation is solved and then Gauss's Law is applied at the surface to determine the threshold voltage. In this model, two linear equations are used to simulate the pockets along the channel at the surface from the source and drain edges towards the center of MOSFET.

The analytical method developed in chapter 2 is used to determine the threshold voltage of a pocket implanted MOSFET.

The results are given in chapter 3. Here we have performed comparison with other models and verification with experimental reported data.

Chapter 4 contains the concluding remarks along with recommendations for further work on this topic.

CHAPTER 2

Threshold Voltage Modeling

2.1 Introduction

The characteristics of a MOSFET can be studied by obtaining the potential distribution within the device. In case of long channel MOSFETs, the effects of the source and the drain on the channel region is negligible and electric field lines originating from the gate are assumed to have no components in the lateral direction. Solution of one-dimensional Poisson's equation gives the potential function in such devices. But in case of short-channel devices, the source and the drain junctions contribute to the potential function in the channel region.

2.2 Threshold Voltage for conventional MOSFET

The nMOSFET structure shown in Fig.2.1 is considered in this work and assumed co-ordinate system is shown at the right side of the structure. All the device dimensions are measured from the oxide-silicon interface. In the structure, the junction depth (r_j) is 30 nm. The oxide thickness (t_{ox}) is 2.5 nm and its SiO_2 with a fixed oxide charge density of 10^{11} cm^{-2}. Uniformly doped p-type Si substrate is used with doping concentration of N_{sub} = 3.5×10^{17} cm^{-3}.

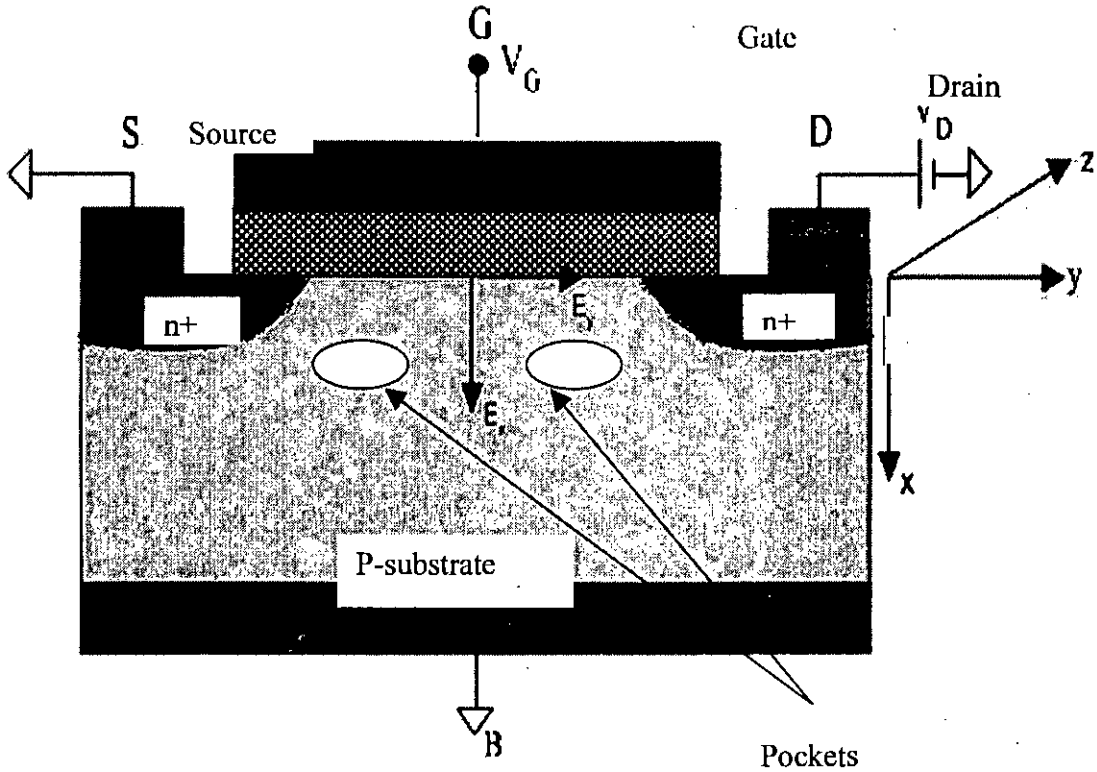

Fig.2.1: n-Channel MOSFET structure with pockets.

Here we derive the relations between the surface potential, and electric field space charge and electric field.

The potential ψ is defined as zero in the bulk of the semiconductor and at the semiconductor surface, $\psi = \psi_s$ and the ψ_s is called the surface potential.

The electron and hole concentrations as a function of ψ are as follows where ψ is positive when the band is bent downward.

$$n_p = n_{po} \exp(q\psi / kT) = n_{po} \exp(\beta\psi) \quad \text{.....(2.1)}$$

$$P_p = p_{po} \exp(-q\psi / kT) = p_{po} \exp(-\beta\psi) \quad \text{.....(2.2)}$$

n_{po} and p_{po} are the equilibrium densities of electrons and holes respectively in the bulk of the semiconductor and $\beta = q / kT$.

At the surface the densities are

$$n_s = n_{po} \exp(\beta\psi_s) \quad \text{.....(2.3)}$$

$$p_s = p_{po} \exp(-\beta\psi_s) \quad \text{.....(2.4)}$$

The following regions of surface potential can be distinguished:

$\psi_S < 0$ accumulation of holes(bands bend upward)

$\psi_s = 0$ flat band condition

$\psi_B > \psi_S > 0$ depletion of holes (bands bend downward)

$\psi_s = \psi_B$ midgap with $n_s = p_s = n_i$ (intrinsic concentration)

$\psi_s > \psi_B$ inversion enhancement, (bands bend downward)

The potential ψ as a function of distance can be obtained by using the one-dimensional Poisson equation

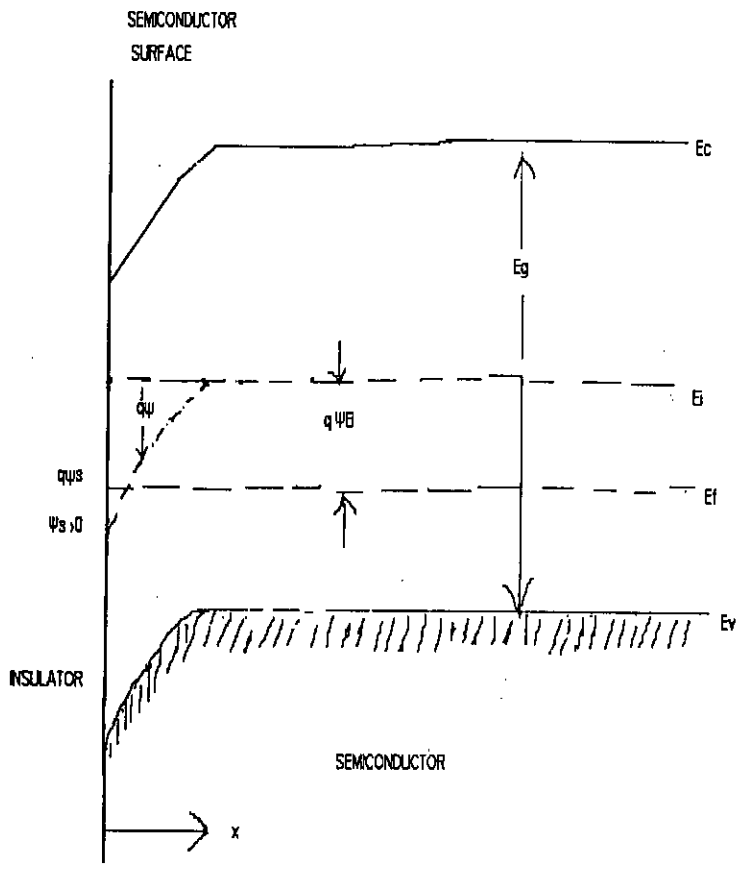

Fig: 2.2 Energy band diagram of surface of a p type semiconductor

$$\frac{d^2\psi}{dx^2} = \frac{-\rho(x)}{\epsilon_s} \quad \text{.....(2.5)}$$

where ϵ_s is the permittivity of the semiconductor and $\rho(x)$ is the total space-charge density given by

$$\rho(x) = q\left(N_D^+ - N_A^- + p_P - n_p\right) \quad \text{.....(2.6)}$$

where N_D^+ and N_A^- arc the densities of the ionized donars and acceptors respectively.

Now , in the bulk of the semiconductor, far from the surface, charge neutrality must exist. Therefore, $\rho(x) = 0$ and $\psi = 0$, so

$$N_D^+ - N_A^- = n_{po} - p_{po} \quad \text{.....(2.7)}$$

In general, for any value of ψ we have

$$p_p - n_p = p_{po}\exp(-\beta\psi) - n_{po}\exp(\beta\psi) \quad \text{.....(2.8)}$$

The resultant Poisson's equation

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\epsilon_s}\left[p_{po}\left(e^{-\beta\psi} - 1\right) - n_{po}\left(e^{\beta\psi} - 1\right)\right] \quad \text{.....(2.9)}$$

Integrating both sides from bulk toward the surface

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\epsilon_s}\left[p_{po}\left(e^{-\beta\psi} - 1\right) - n_{po}\left(e^{\beta\psi} - 1\right)\right] \quad \text{.....(2.10)}$$

Integrating both sides from bulk toward the surface

$$\int_0^{\frac{\delta\psi}{\delta x}} \left(\frac{\delta\psi}{\delta x}\right) d\left(\frac{\delta\psi}{\delta x}\right) = -\frac{q}{\epsilon_s}\int_0^{\psi}\left[p_{po}\left(e^{-\beta\psi} - 1\right) - n_{po}\left(e^{\beta\psi} - 1\right)\right] d\psi \quad \text{.....(2.11)}$$

gives the relation between the electric field $\left(\xi = -\frac{d\psi}{dx}\right)$ and the potential ψ ;

$$\xi^2 = \left(\frac{2kT}{q}\right)^2 \left(\frac{qp_{po}\beta}{2\epsilon_s}\right)\left[\left(e^{-\beta\psi} + \beta\psi - 1\right) + \frac{n_{po}}{p_{po}}\left(e^{-\beta\psi} - \beta\psi - 1\right)\right] \quad \text{.....(2.12)}$$

Extrinsic Debye length for holes

$$L_D = \sqrt{\frac{kT\,\epsilon_S}{p_{po}q^2}} = \sqrt{\frac{\epsilon_s}{qp_{po}\beta}} \quad \text{.....(2.13)}$$

Thus the electric field becomes

$$\xi = -\frac{\delta\psi}{\delta x} \pm \frac{\sqrt{2}kT}{qL_D} F\left(\beta\psi, \frac{n_{po}}{p_{po}}\right) \quad \text{.....(2.14)}$$

The surface charge per unit area after strong inversion is given by

$$Q_S = Q_n + Q_B \quad \text{.....(2.15)}$$

where

$$Q_n = -qN_A W_m = -\sqrt{2qN_A W_m (V_D + 2\psi_B)} \quad \text{.....(2.16)}$$

and Q_n the charge due to minority carriers within the inversion layer, is

$$|Q_n| = q\int_0^{x_1} n(x)dx = \int_{\psi_s}^{\psi_B} \frac{n(\psi)d\psi}{d(\psi)/dx}$$

or,

$$|Q_n| = q\int_{\psi_s}^{\psi_B} \frac{n_{po}e^{(\beta\psi - \beta V_D)}d\psi}{\left(\sqrt{2}kT/qL_D\right)F\left(\beta\psi, V_D n_{po}/p_{po}\right)} \quad \text{.....(2.17)}$$

where x_i denotes the point at which the intrinsic Fermi Level intersects the impurity reference level for electrons.

The expression for Q_n is derived under the condition $V_{BS} = 0$.

2.3 Threshold voltage for Long channel MOSFET

Now for the basic MOSFET characteristics the following ideal conditions should be considered:

i) There are no interface traps, fixed oxide charge or work function difference and so on;

ii) Only the drift current will be considered;

iii) Carrier mobility in the inversion layer is constant;

iv) Doping in the channel is uniform ;

v) Reverse leakage current is negligibly small

vi) The transverse field (ξ_x in the x direction) in the channel is larger than the longitudinal field (ξ_y in the y direction). The last condition corresponds to the so called gradual channel approximation.

Under such idealized conditions, the total charge induced in the semiconductor per unit area Q_S at a distance y from the source is given by

$$Q_s(y) = \left[-V_G + \psi_S(y)\right] C_i \quad \text{.....(2.18)}$$

where $C_i = \epsilon_s / d$ is the capacitance per unit area .The charge in the inversion layer is given by

$$Q_n(y) = Q_S(y) - Q_B(y)$$

$$= -\left[V_G + \psi_S(y)\right] C_i - Q_B(y)$$

The surface potential $\psi_s(y)$ at inversion can be approximated by $2\psi_B + V(y)$ where $V(y)$ is the reverse bias between point y and the source electrode (which is assumed to be grounded). The charge within the surface depletion region

$$Q_B(y) = -qN_A W_m = \sqrt{2\epsilon_s qN_A \left[V(y) + 2\psi_B\right]} \quad \text{.....(2.19)}$$

Now

$$Q_N(y) = -\left[V_G - V(y) - 2\psi_B\right]C_i + \sqrt{2 \in_s qN_A\left[V(y) + 2\psi_B\right]} \quad \text{.....(2.20)}$$

The conductivity of the channel can be approximated by

$$\sigma(x) = q\,n(x)\,\mu_n(x) \quad \text{.....(2.21)}$$

The channel conductance is then given by

$$g = \frac{Z}{L}\int_0^{x_i} \sigma(x)dx \quad \text{.....(2.22)}$$

For a constant mobility, the channel conductance

$$g = \frac{qZ\mu_n}{L}\int_0^{x_i} n(x)dx = qZ\mu_n |Q_n| / L \quad \text{.....(2.23)}$$

The channel resistance of an incremental section is given by

$$dR = \frac{dy}{gL} = \frac{dy}{Z\,\mu_n\,|Q_n(y)|} \quad \text{.....(2.24)}$$

and the voltage drop across this elemental section is given by

$$dV = I_D dR = \frac{I_D dy}{Z\mu_n |Q_n(y)|}$$

I_D is the drain current and constant independent of y.

Now Drain current,

$$I_D = \frac{Z}{L}\left\{\left(V_G - 2\psi_B - \frac{V_D}{2}\right)V_D - \frac{2}{3}\frac{\sqrt{2 \in_S qN_A}}{C_i}\left[\left(V_D + 2\psi_B\right)^{3/2} - \left(2\psi_B\right)^{3/2}\right]\right\} \quad \text{.....(2.25)}$$

for the present idealized case.

The above equation predicts that for a given V_G the drain current first increases linearly with drain voltage(the linear region), then gradually levels off, approaching a saturated value (the saturated region).

Considering the above mentioned two regions for the case of small V_D

$$I_D = \frac{Z}{L}\mu_n C_i \left[(V_G - V_T)V_D - \left(\frac{1}{2} + \frac{\sqrt{\epsilon_S \, qN_A / \psi_B}}{4C_i} \right) \right] \quad \text{.....(2.26)}$$

or,

$$I_D = \frac{Z}{L}\mu_n C_i (V_G - V_T)V_D \quad \text{.....(2.27)}$$

for

$V_D = V_G - V_T$

where V_T (The threshold voltage) is given by

$$V_T = 2\psi_B + \frac{\sqrt{2 \epsilon_s \, qN_A (2\psi_B)}}{C_i} \quad \text{.....(2.28)}$$

By plotting I_D versus V_G (for a given small V_D) the threshold voltage can be deduced from the linearly extrapotated value at the V_G axis. In the linear region, the channel conductance g_D and the transconductance g_m are given as

$$g_D \equiv \left. \frac{\delta I_D}{\delta V_D} \right|_{V_G=CONST} = \frac{Z}{L}\mu_n C_i (V_G - V_T)$$

$$g_D \equiv \left. \frac{\delta I_D}{\delta V_D} \right|_{V_G=CONST} = \frac{Z}{L}\mu_n C_i V_D$$

The Drain voltage (V_{Dsat}) and drain currents (I_{Dsat}) are in saturation region beyond the pinch off point

When

$$Q_n(L) = 0;$$

$$V_{Dsat} = V_G - 2\psi_B + K^2\left(1 - \sqrt{1 + 2V_G / K^2}\right) \quad \text{.....(2.29)}$$

where $K \equiv \sqrt{\epsilon_S qN_A / C_i}$ .The saturation current becomes

$$I_{Dsat} = \frac{mZ}{L}\mu_n C_i (V_G - V_T)^2 \quad \text{.....(2.30)}$$

where m is a function of doping concentration and approaches ½ at low dopings.

The transconductance in the saturation region

$$g_m = \left.\frac{\delta I_D}{\delta V_G}\right|_{V_D = CONST} = \frac{2mZ}{L}\mu_n C_i (V_G - V_T) \quad \text{.....(2.31)}$$

The main effect of the fixed oxide charges and the difference in the work functions is to cause a voltage shift corresponding to the flat-band V_{FB}. This in turn causes a change in the threshold voltage V_T; in the linear region V_T becomes

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2\epsilon_s qN_A(2\psi_B)}}{C_i} \quad \text{.....(2.32)}$$

$$V_T = \left(\phi_{ms} - \frac{Q_f}{C_i}\right) + 2\psi_B + \frac{\sqrt{4\epsilon_s qN_A\psi_B}}{C_i} \quad \text{.....(2.33)}$$

2.4 Threshold Voltage for Short Channel MOSFET

Departure from long channel behavior can be obtained by applying the charge conservation principle to the region bounded by the metal gate and bulk of the semiconductor:

$$Q_M' + Q_0' + Q_n' + Q_B' = 0 \quad \text{.....(2.34)}$$

where Q_M' is the total charge on the gate , Q_0' is the total effective oxide charges at the Si-SiO_2 interface, Q_n' is the total inversion layer charge, and Q_B' is the total ionized impurity in the depletion region. The following equation may be written as

$$V_G = V_{FB} + \psi_S + Q_B' / C_i A \quad \text{.....(2.35)}$$

where V_{FB} is the flat-band shift, ψ_s is the surface potential and A is the area.

The threshold voltage is given by setting $\psi_S \approx 2\psi_B$.

$$V_T = V_{FB} + 2\psi_B + Q_B' / C_i A \quad \text{.....(2.36)}$$

For short channel devices, the full effect of Q_B' on the threshold voltage is reduced, because near the source and drain ends of the channel, some field lines originating from the source or drain terminate at the bulk charges in the channel region for $V_D = 0$. For $V_D > 0$ depletion region near the drain expands further. The horizontal depletion layer widths y_s and y_D are smaller than the vertical depletion layer widths W_S and W_D respectively, because the transverse field strongly influences the potential distribution at the surface.

Because the reduction of the bulk charge Q_B' , surface potential for a gate voltage increases to a leading to an increase of subthreshold current. The surface potential can be found from the following expression

$$V_G - V_{FB} = \psi_S + \frac{1}{C_i}\sqrt{q \in_s N_A (\psi_S + V_{BS})/2}\left(1 + \frac{L - W_D - W_S}{L - y_D - y_s}\right) \quad \text{.....(2.37)}$$

Where W_D and W_S are the depletion widths of drain and source respectively.

And

$$y_s = \sqrt{\frac{2\epsilon_s}{qN_A}(V_{bi} - \psi_s)}$$

$$y_D = \sqrt{\frac{2\epsilon_s}{qN_A}(V_{bi} - \psi_s + V_D)}$$

The subthreshold current is given by

$$I_D = \mu_n \left(\frac{Z}{L - y_S - y_D}\right) \frac{aC_i}{2\beta^2} \left(\frac{n_i}{N_A}\right)^2 \left(1 - e^{-\beta V_D}\right) e^{\beta\psi_s} (\beta\psi_s)^{1/2} \quad \text{.....(2.38)}$$

where $L_{eff} = L - y_s - y_D$

From the first order estimation of the threshold voltage the total bulk charge inside the trapezoide is

$$\frac{Q_B}{Z} = qN_A W_m \left(\frac{L + L'}{2}\right) \quad \text{.....(2.39)}$$

By straightforward trigonometric analysis,

$$\frac{L + L'}{2L} = 1 - \frac{r_j}{L}\left(\sqrt{1 + \frac{2W_m}{r_j}} - 1\right) \quad \text{.....(2.40)}$$

The threshold voltage shift is then

$$\Delta V_T = \frac{1}{C_i}\left(\frac{Q'_B}{ZL} - qN_A W_m\right) = -\frac{qN_A W_m}{C_i}\left(1 - \frac{L + L'}{2L}\right) \quad \text{.....(2.41)}$$

$$= -\frac{qN_A W_m r_j}{C_i L}\left(\sqrt{1 + \frac{2W_m}{r_j}} - 1\right)$$

These relations are then used to derive by solving Poisson's equation and Gauss Law expressions of surface charge is derived. Then surface potential and next expression is found.

In the conventional long channel bulk-MOSFET , the threshold voltage model is given in equation(2.42) and for short channel bulk –MOSFET a threshold voltage shift is derived as in equation. (2.43).

$$V_{th} = V_{FB} + \psi_S + \frac{\sqrt{2q \in_s N_{sub} \psi_s}}{C_{OX}} \quad \text{.....(2.42)}$$

$$\Delta V_{th} = -\frac{qN_{sub} W_m r_j}{C_{ox} L}\left(\sqrt{1+\frac{2W_m}{r_j}} - 1\right) \quad \text{.....(2.43)}$$

where, the maximum width of the depletion region is given by V_{BS} being the substrate bias voltage:

$$W_m = \sqrt{\frac{2 \in_s (\psi_s + V_{BS})}{qN_{sub}}}$$

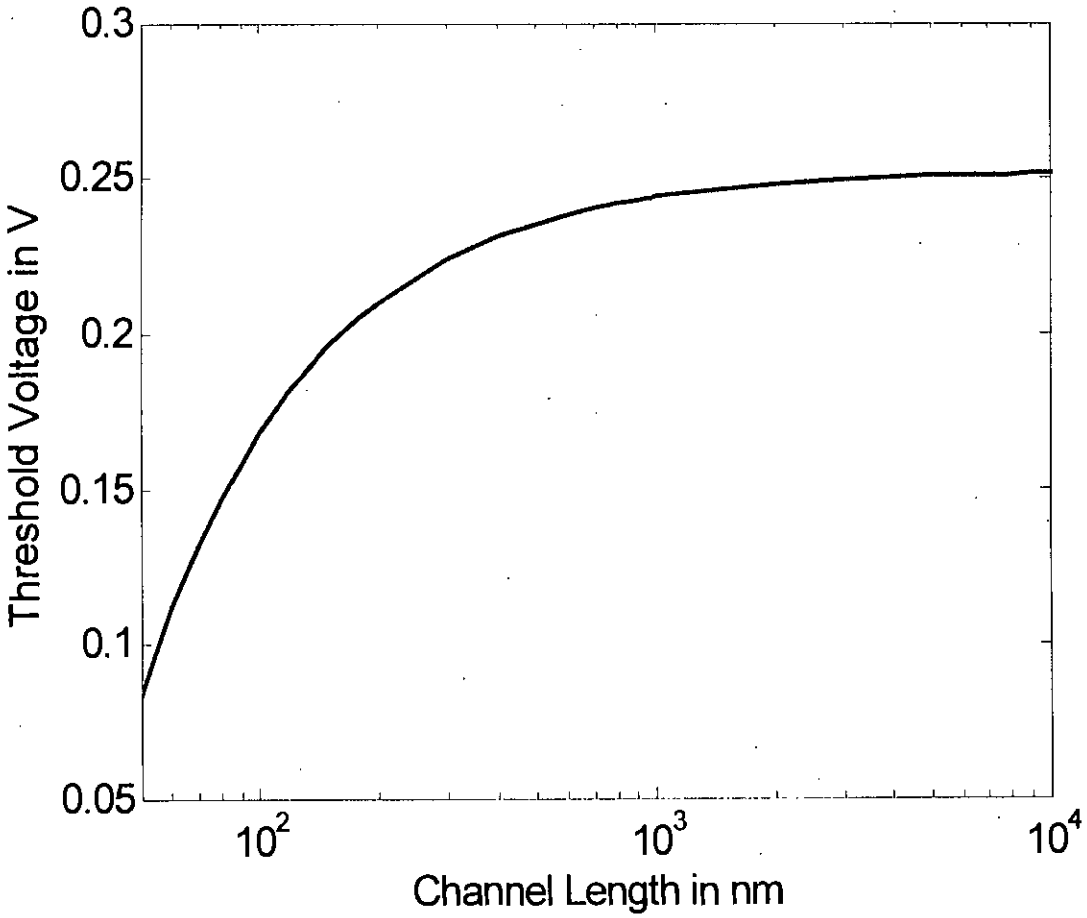

Fig.2.3 Short channel effect due to reduction in gate length of conventional bulk-nMOSFET

Finally the threshold voltage becomes,

$$V_{th} = V_{th} + \Delta V_{th} \quad \text{.....(2.44)}$$

This model is simulated for a particular device and the threshold voltage vs. gate length curve is shown in Fig. 2.3. It shows that the threshold voltage reduces drastically as gate length reduces beyond 100 nm.

2.5 Doping profiles for pocket implants

To preserve the long channel threshold voltage behavior for the short channel device, pocket implantation, which causes reverse short channel effect (RSCE), is done by adding donor atoms both from the source and drain edges. The peak pocket concentration, N_{pm} gradually decreases towards the substrate level concentration, N_{sub} with a pocket length from both the source and drain edges. The basis of the model of the pocket is to assume two linear doping profiles from both the source and drain edges across the channel as shown in Fig.2.4 and Fig.2.5

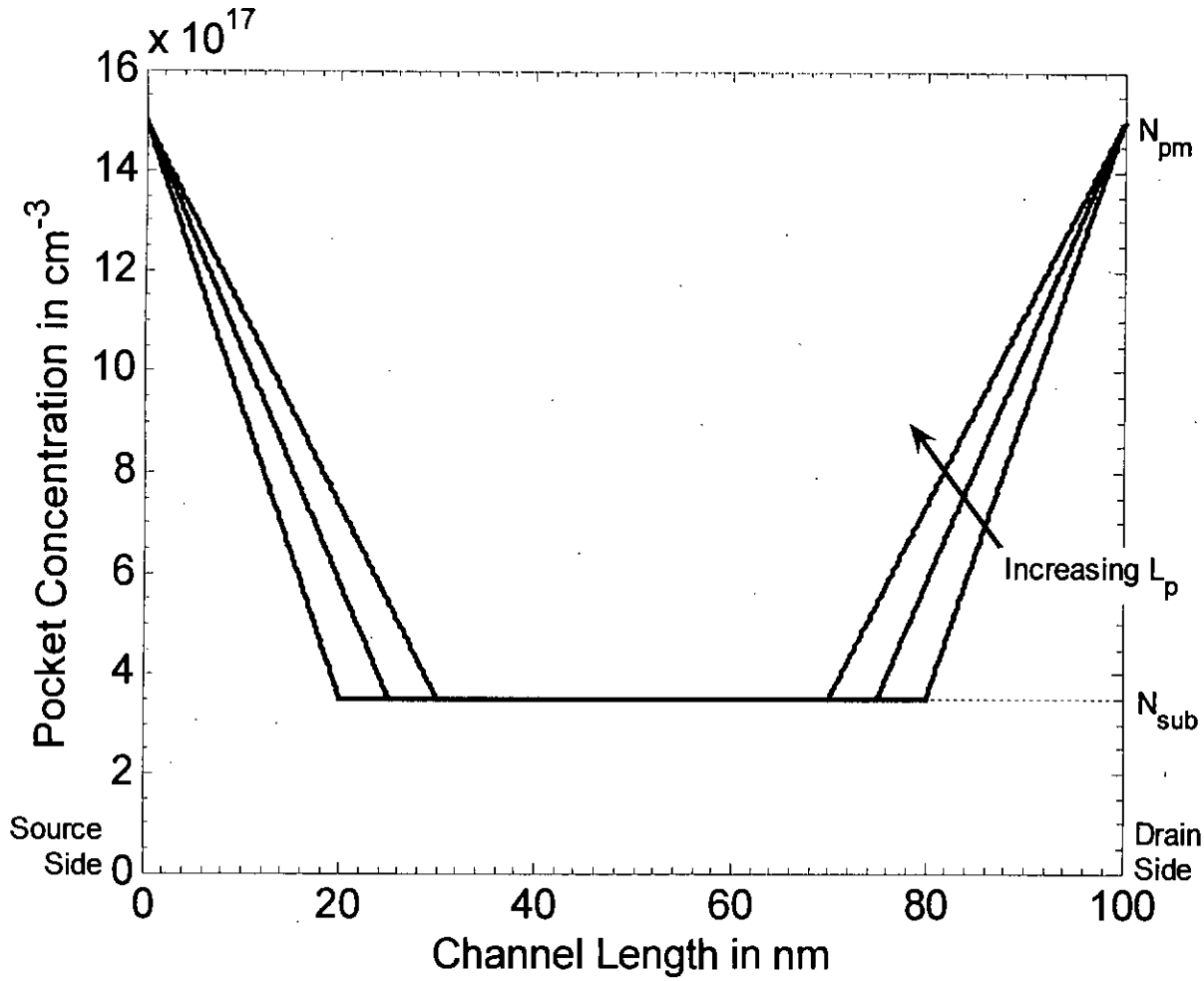

Fig.2.4 Simulated Pocket profiles for L_p = 20 nm, 25 nm and 30 nm and $N_{pm} = 1.5\times10^{18}$ cm^{-3}.

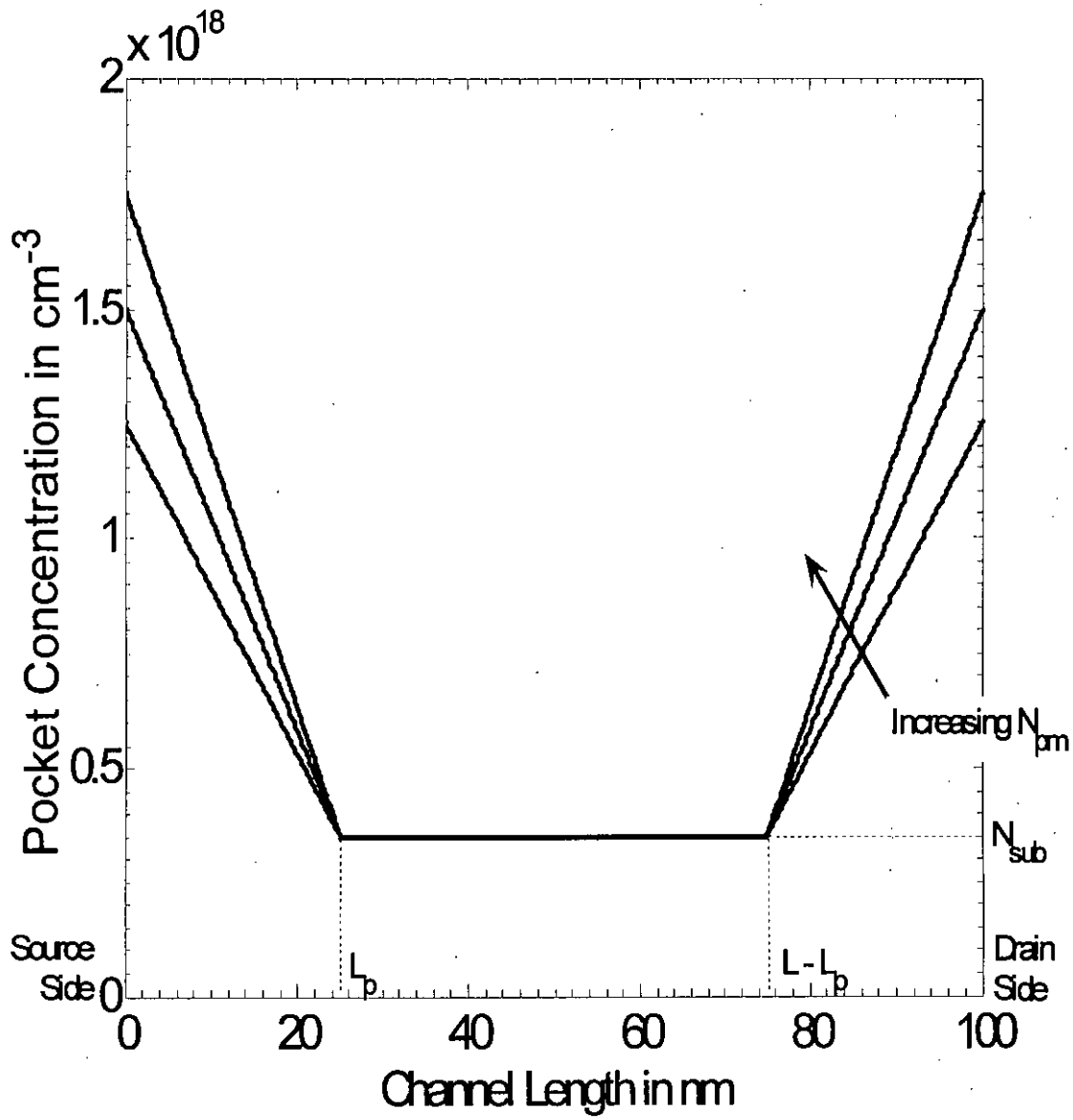

Fig. 2.5 Simulated Pocket profiles for $N_{pm} = 1.25\times10^{18}$ cm^{-3}, 1.5×10^{18} cm^{-3} and 1.75×10^{18} cm^{-3}, $L_p = 25$ nm.

2.6 Threshold Voltage for pocket implanted MOSFET

At the source side, the pocket profile is given as:

$$N_s(y) = -\frac{N_{pm} - N_{sub}}{L_p} y + N_{pm}$$

$$= N_{sub}\frac{y}{L_p} + N_{pm}\left(1 - \frac{1}{L_p} y\right) \quad \text{.....(2.45)}$$

At the drain side, the pocket profile is given as:

$$N_d(y) = \frac{N_{pm} - N_{sub}}{L_p}\left[y - \left(L - L_p\right)\right] + N_{sub}$$

$$= N_{pm}\left(1 - \frac{L}{L_p} + \frac{1}{L_p} y\right) + N_{sub}\left(\frac{L}{L_p} - \frac{1}{L_p} y\right) \quad \text{.....(2.46)}$$

(Equations of straight lines are used for both the pocket profiles.)

where y represents the distance across the channel, N_{pm} and L_p are peak doping concentration and the pocket length, respectively.

Since the pile-up profile is due to the direct pocket implant at the source and drain side, it is assumed symmetric at both sides. With these two conceptual pocket profiles, the profiles are integrated mathematically along the channel length and then divided by it to derive an average effective concentration as in equation (2.47):

$$N_{eff} = \frac{1}{L}\int_0^L \left[N_s(y) + N_d(y) + N_{sub}\right] dy \quad \text{.....(2.47)}$$

Putting the expressions of $N_s(y)$ and $N_d(y)$ in equation (2.47) the effective doping concentration is obtained as follows:

$$N_{eff} = N_{sub}\left(1 - \frac{L_p}{L}\right) + \frac{N_{pm} L_p}{L} \quad \text{.....(2.48)}$$

When $L_p << L$ for long channel device then pocket profile has no effect on V_{th}, But when L_p is comparable with L for short channel MOSFET then there is a effect of pocket profile on V_{th}.

The threshold voltage expression given in equation (2.32) is obtained by solving the 1-D Poisson equation and then applying Gauss's law. Thus in our proposed threshold voltage model, the space-charge is obtained by incorporating the effective doping concentration of pocket profiles given in equation (2.48) into equation (2.44) for zero substrate bias voltage condition as follows:

$$V_{th} = V_{FB} + \psi_s + \frac{\sqrt{2q\varepsilon_s N_{eff}\psi_s}}{C_{ox}} + \Delta V_{th} \quad \text{.....(2.49)}$$

where the bulk potential, threshold voltage shift from the long channel device and the maximum width of the depletion region are given by

$$\psi_B = \frac{kT}{q}\ln\frac{N_{eff}}{n_i} \quad \text{.....(2.50)}$$

$$\Delta V_{th} = -\frac{qN_{eff}W_m r_j}{C_{ox}L}\left(\sqrt{1+\frac{2W_m}{r_j}}-1\right) \quad \text{.....(2.51)}$$

$$\text{and } W_m = \sqrt{\frac{2\varepsilon_s(\psi_s + V_{BS})}{qN_{eff}}}$$

where V_{FB}, n_i, ϕ_{ms}, ψ_B, C_{ox} and Q_f are the flat band voltage, intrinsic doping concentration, metal-semiconductor work function difference, oxide capacitance and fixed oxide charge respectively.

CHAPTER 3

RESULTS AND DISCUSSION

3.1 Introduction

The Threshold voltage V_{th} model is derived by assuming linear pocket profile. The effective doping concentration is obtained from equation 2.48.

When $L_p << L$ for long channel device then pocket profile has no effect on V_{th}, But when L_p is comparable with L for short channel MOSFET then there is a effect of pocket profile on V_{th}.

The threshold voltage expression given in equation (2.32) is obtained by solving the 1-D Poisson equation and then applying Gauss's law. Thus in our proposed threshold voltage model, the space-charge is obtained by incorporating the effective doping concentration of pocket profiles given in equation (2.48) incorporated into equation (2.44) for zero substrate bias voltage condition the threshold voltage is obtained as in equation (2.49). Some possible outcomes are getting of a simple V_{th} model, reducing circuit simulation problems for short channel nMOSFET and we can go beyond 100nm to calculate V_{th}.

3.2 Simulation Results of the Model

The simulated V_{th} vs. L curve has been drawn for this new model is shown in Figures 2.31 and 2.32. The parameters L_p and N_{pm} play an important role on this curve. The peak value of the V_{th} vs. L curve increases with increasing pocket lengths as shown in above figures. Also as L_p increases the onset of V_{th} roll-up happens at a longer channel length and the onset of V_{th} roll-off happens at a shorter channel length.

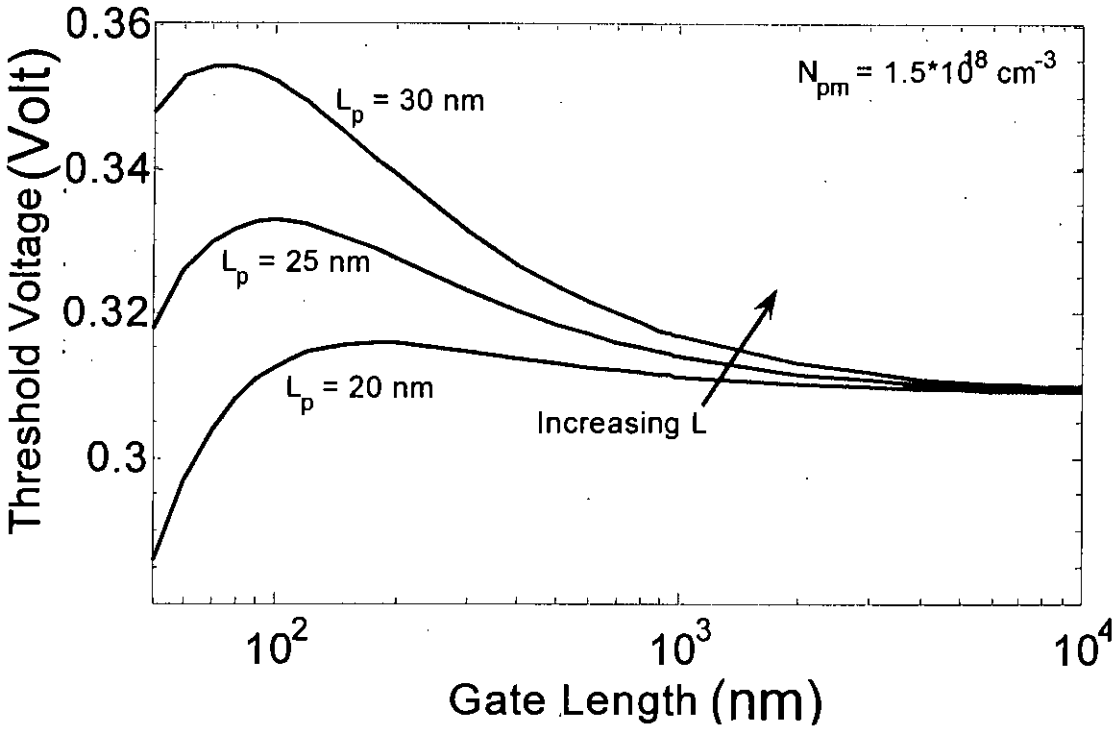

Fig. 3.1 Reverse short channel effect due to pocket implantation in NMOSFET for L_p = 20 nm, 25 nm and 30 nm and $N_{pm} = 1.5\times10^{18}$ cm^{-3}.

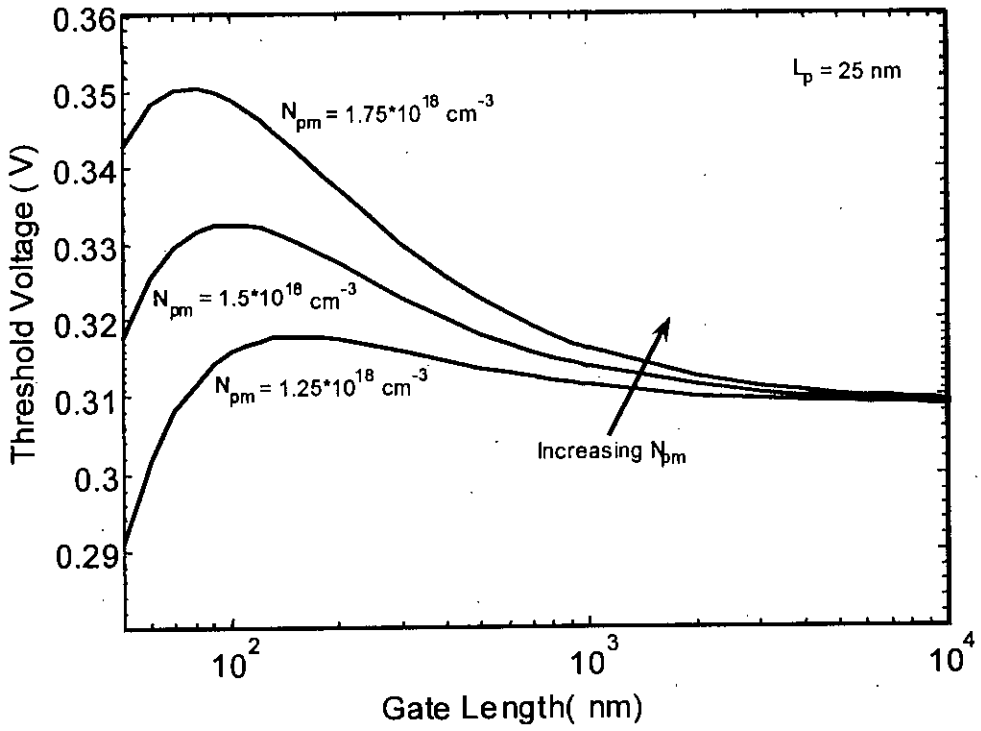

Fig. 3.2 Reverse short channel effect due to pocket implantation in NMOSFET for $N_{pm} = 1.25\times10^{18}$ cm^3, 1.5×10^{18} cm^{-3} and 1.75×10^{18} cm^{-3} and L_p = 25 nm.

This result is expected because as the pocket length increases it exhibits a strong reverse short channel effect.

Similarly, as the peak value of the pocket concentration , N_{pm} increases, the onset of V_{th} roll-up occurs at longer channel length the onset of V_{th} roll-off occurs at shorter channel length as shown in Figure 3.2. If L_p and N_{pm} increase further by keeping the substrate concentration and other parameters constant then V_{th} roll-off starts to vanish.

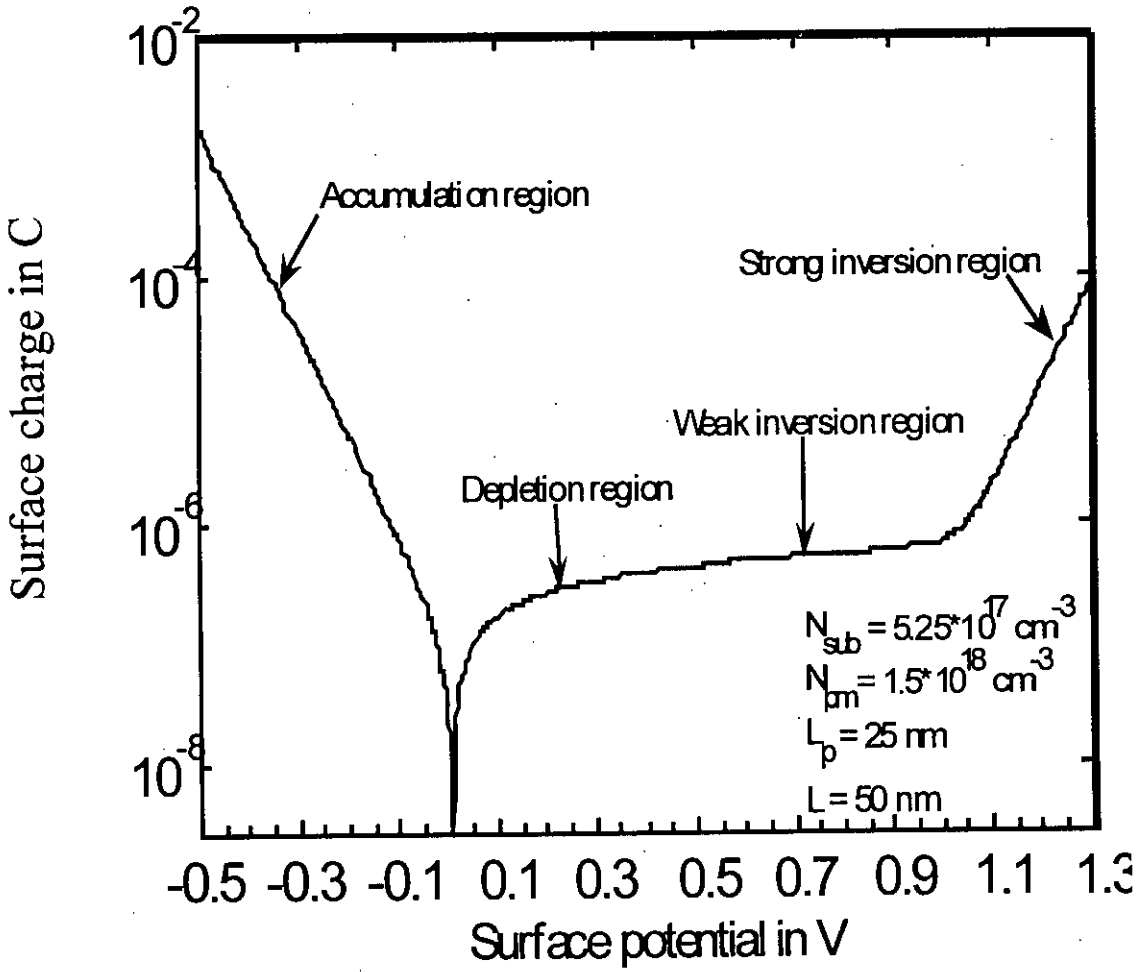

Fig. 3.3 Surface charge vs.surface potential for pocket implanted MOSFET of 50 nm channel length

To verify the results further, the surface charge versus surface potential curve is simulated for different gate lengths. Here in Fig. 3.3. the charge profile is shown for pocket implanted MOSFET for 50 nm channel length.

Besides, the value of surface potential is calculated by using numerical techniques at threshold condition i.e. at gate voltage equal to threshold voltage and was found as 0.88 V and 0.93 V for 10 μm and 50 nm pocket implanted nMOSFET respectively. Thus it is clear that the proposed model can accurately model the threshold voltage for different device as well as different pocket profile parameters.

3.3 Comparison with available experimental data

Wc have also put experimental data and compared with our model. We found that our model approximately fit with the experimental data and we get better result from our model. Below 100 nm gate length we get threshold voltage decreasing and we get data down to 50 nm. But experimental data shows increasing of threshold voltage above 300 nm and then decreases up to 100 nm. In experimental data below 100 nm channel length data is not found. So our model shows better result of reverse short channel effect.

The simulated data is plotted [41].

Gate lengths are in micron

L = [0.12e-4 0.18e-4 0.24e-4 0.3e-4 0.44e-4 0.6e-4 0.7e-4 o.9e-4 1.1e-4 2.5e-4 3.5e-4 4.4e-4 5.8e-4 8.2e-4 10e-4];

Threshold voltage is in volt

V_{th} = [0.33 0.356 0.37 0.37 0.36 0.354 0.352 0.35 0.35 0.35 0.35 0.35 0.35 0.35 0.35];

All parameters are in MKS units,

But Lengths & Carrier concentrations are in cm & cm^{-3}

N_{sub} = 1.84e17;

N_{pm} = 5.8 e17;

L_p =40e-7;

ni = 1.45e10;

φ_{ms} = -0.904V

V_{FB} = -0.9318 V

d = 6e-7

r_j = 80e-7

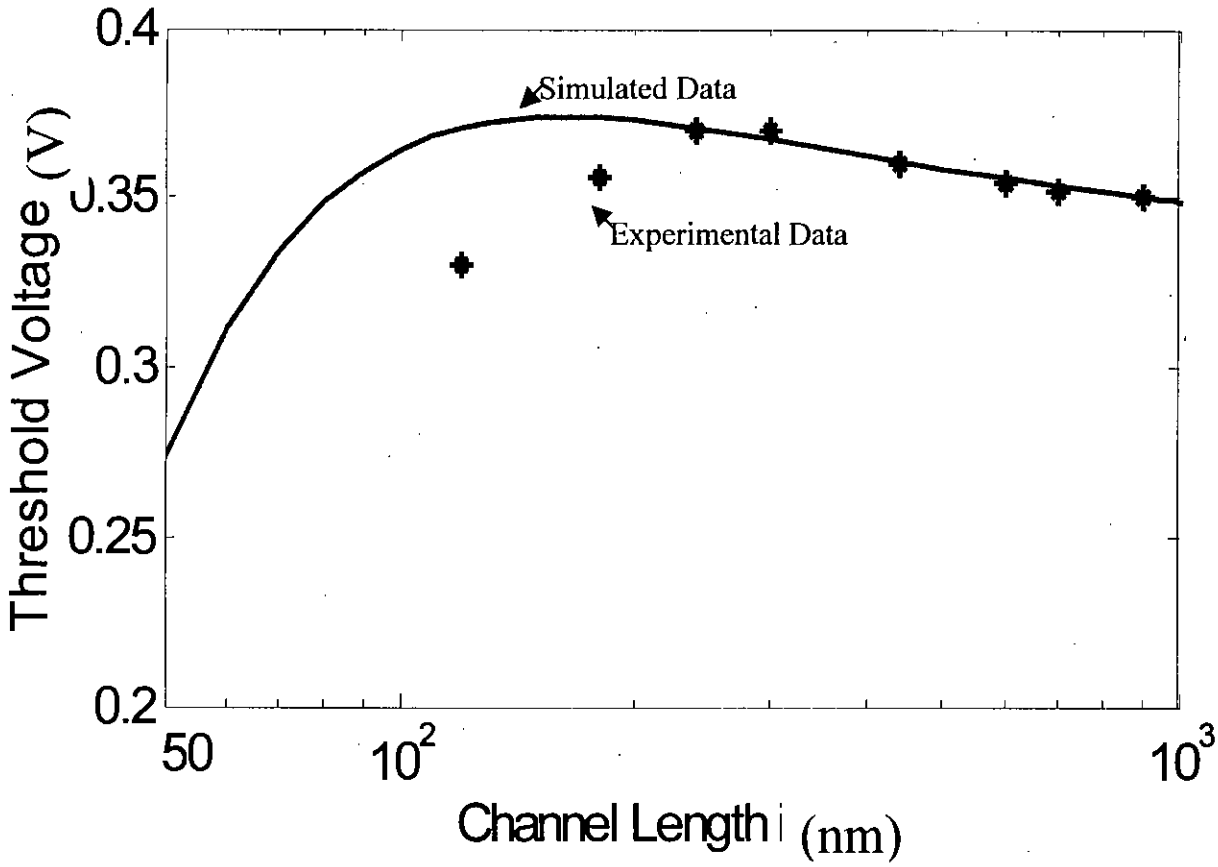

Fig 3.4 : Threshold voltage vs. gate length in comparison with experimental data

3.4 Comparison of our Model with others

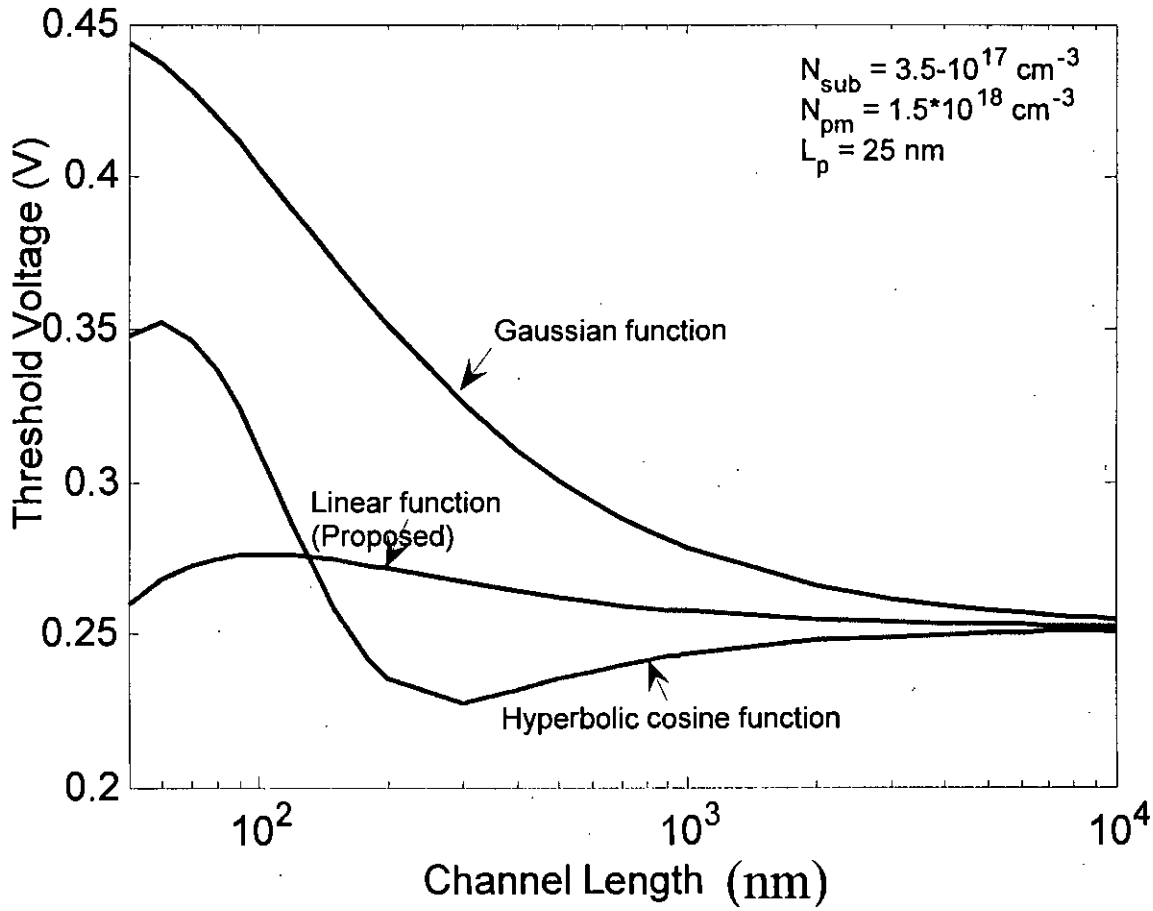

Fig.3.5 Threshold voltage variation with gate lengths for two other pocket profile based on Gaussian and hyperbolic cosine function in comparison with the linear pocket profile based threshold voltage model for $N_{pm} = 1.5\times10^{18}$ cm^{-3} and $L_p = 25$ nm with $N_{sub} = 3.5\times10^{17}$ cm^{-3}.

Figure 3.5 shows that our proposed model based on linear profile exhibits better result of suppressing short channel effect in comparison with the other proposed model for the pocket profiles such as Gaussian profile and hyperbolic cosine function. This can be explained using the Fig. 3.6 where we show the effective carrier concentration variation with the channel length. Here we see that the effective carrier concentration increases very smoothly for our proposed linear pocket profile as the channel length shrinks. But in case of hyperbolic cosine function model it does not increase until 200 nm. Therefore, for hyperbolic cosine model at first we observe short channel effect starts and then again RSCE becomes stronger as before 100 nm we see from Fig. 3.6 that the effective carrier concentration increases more rapidly than that in the linear model.

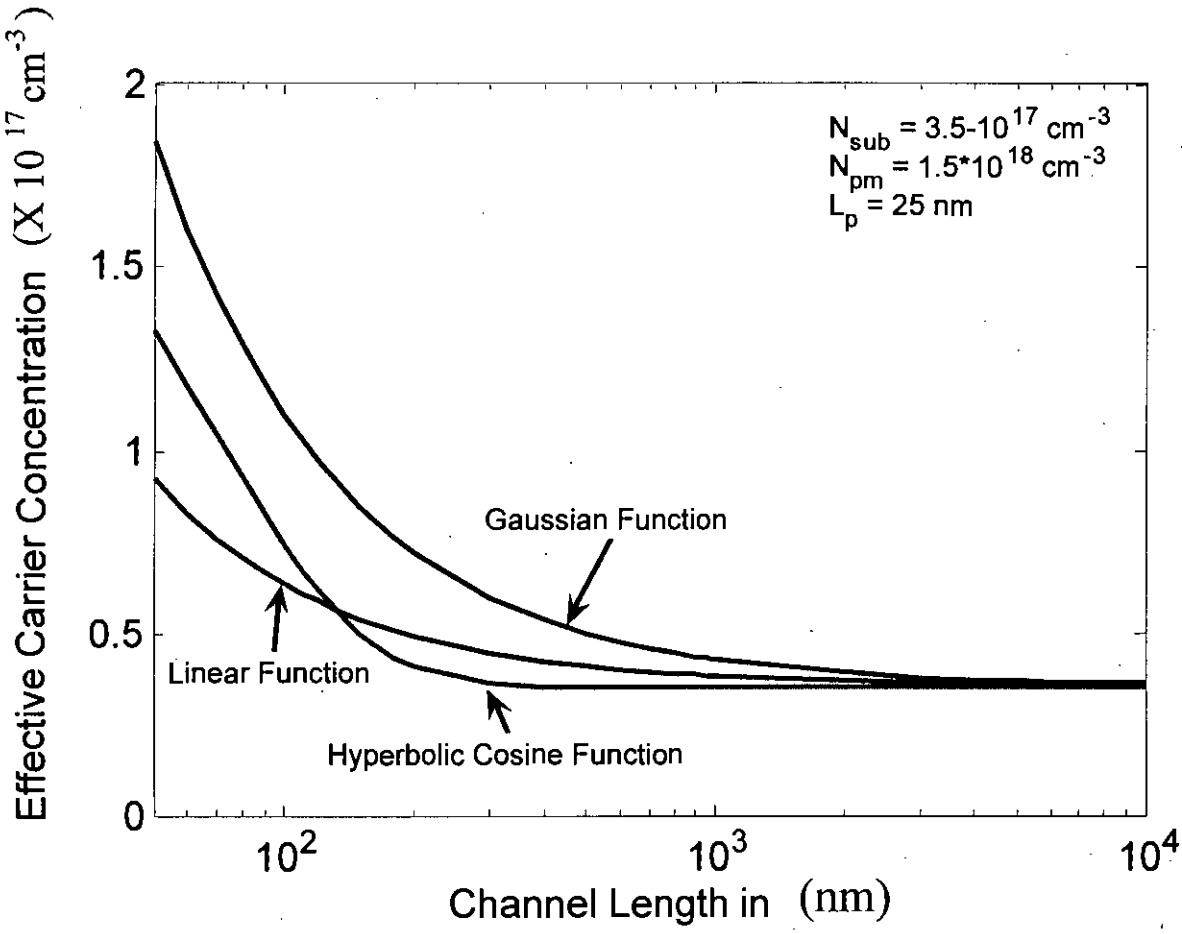

Fig. 3.6 Effective carrier concentration with channel lengths for other pocket profiles based on Gaussian and hyperbolic cosine function in comparison with the linear pocket profile for $N_{pm} = 1.5\times10^{18}$ cm^{-3} and $L_p = 25$ nm with $N_{sub} = 3.5\times10^{17}$ cm^{-3}.

On the other hand, in case of Gaussian function effective carrier concentration increases more rapidly than that in the linear model. Therefore, in Fig.3.5 we observe that RSCE is stronger here and therefore in this case threshold voltage is increasing until 50 nm. But in sub-100 nm regime our purpose is to suppress the SCE only by the RSCE by implanting the pockets. Besides, simulation time taken to calculate threshold voltage by using our model for pocket profile is less than that by using Gaussian function and hyperbolic cosine function.

In Fig.3.7 threshold voltage is compared with two other models and also with available experimental data. From this figure we find that our model gives the best result and better fit with available experimental data.

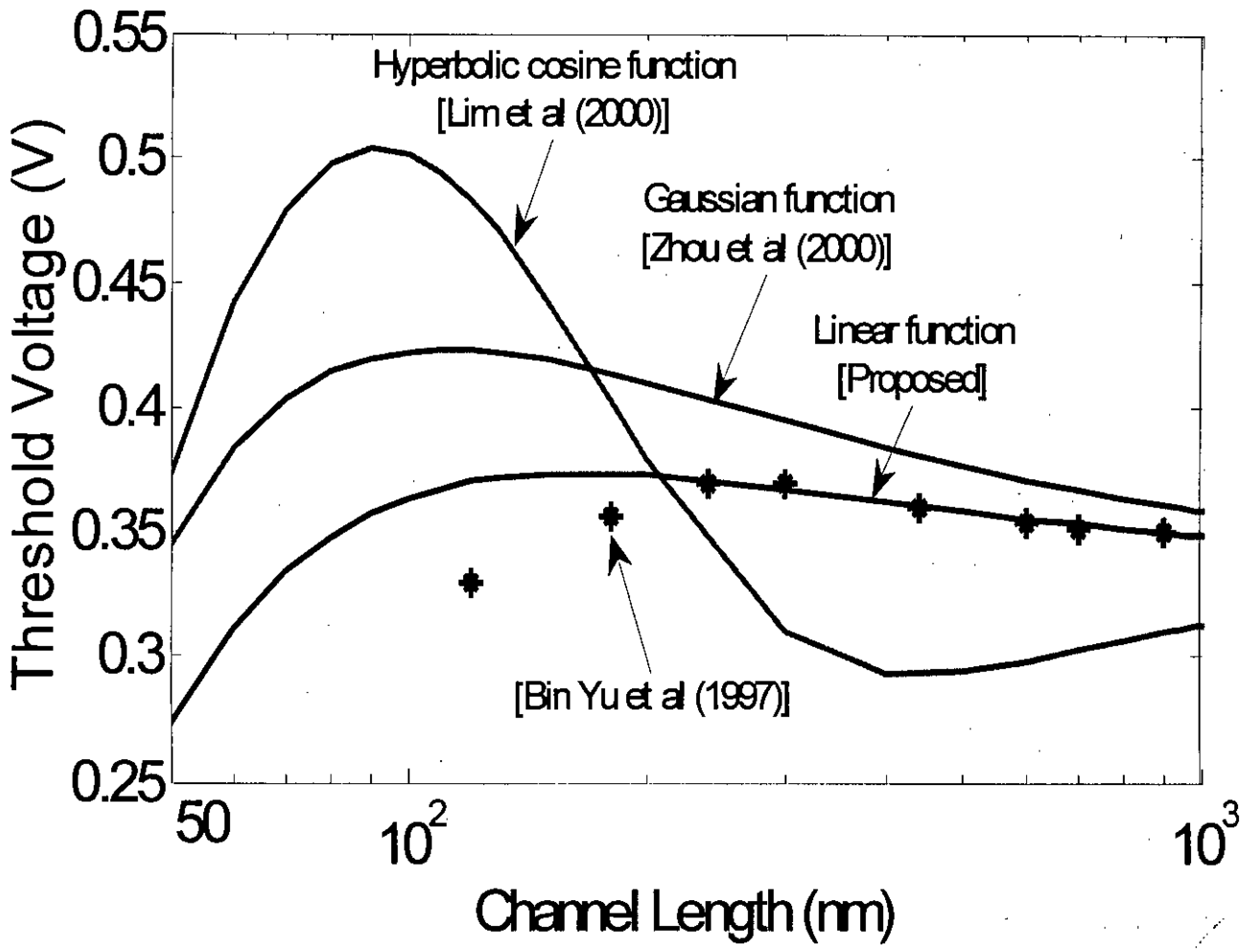

Fig.3.7 Threshold voltage comparison with two other models

Chapter 4

Conclusions

4.1Conclusion

In this work an analysis is presented to determine the threshold voltage of deca-nano MOSFETs. The difference between the characteristics of the long channel and the short channel MOSFETs are described by studying the effects of lateral electric field on short channel devices. The models used to analyze short –channel MOSFETs fail to determine threshold voltage of deca-nano MOSFETs.

A threshold voltage model for ultra thin oxide and sub-100 nm pocket implanted nMOSFET has been developed. The well-known reverse short channel effect has been observed through the proposed model. The model is developed assuming two linear pocket profiles along the channel at the surface of the MOS device from the source and drain edges. The proposed model along with other two models of threshold voltage has been simulated using the same values for the different parameters and compared for V_{th} vs. L_g characteristics. It is found that our model efficiently determines the threshold voltages of scaled nMOSFETs having channel lengths in sub-100 nm regime and shows better performance than the other two models.

4.2 Suggestions for future work

We have not considered the effect of drain. It can be incorporated. In order to obtain an accurate expression for threshold voltage, a two–dimensional analysis can be performed.

For inversion layer we have used Classical Treatment for calculation of charge. If we incorporate Quantum Mechanical Treatment our model will be more accurate.

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