IMPACT OF MULTIPLE GATE BIAS ON THE CAPACITANCE-VOLTAGE (C-V) CHARACTERISTICS OF THIN-FILM FULLY-DEPLETED FOUR GATE TRANSISTOR

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by

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The thesis titled "**IMPACT OF MULTIPLE GATE BIAS ON THE CAPACITANCE-VOLTAGE (C-V) CHARACTERISTICS OF THIN-FILM FULLY-DEPLETED FOUR GATE TRANSISTOR**" submitted by **K. M. Masum Habib**, Student No: **100606247P**, Session: **October 2006** has been accepted as satisfactory in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on August 19, 2009.

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To My Parents

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Abstract

The impact of the back gate and the junction gate biases on front gate Capacitance-Voltage ($C-V$) characteristics of the fully depleted (FD) Four Gate Transistor (G^4–FET) has been studied by means of systematic semi-classical 2-D simulations. It has been revealed that in strong inversion and strong accumulation of the front interface, back gate bias does not have significant effect on $C-V$. However, in weak inversion, weak accumulation and depletion, the back gate bias has significant effects. An accumulation/inversion channel at back gate retards zero capacitance to be achieved. A very strong inversion/accumulation channel of back gate cannot be mitigated by applying front gate bias, that is zero capacitance cannot be achieved unlike in case of a usual fully depleted device. A weaker inversion at the back gate causes the region of zero capacitance to become smaller. The effect of junction gate bias has been found to be more interesting. In accumulation region of the front gate, the greater the junction gate voltage, the smaller the capacitance at a particular front gate voltage. In other words, accumulation is easily achieved if junction gate bias is *lower*. In inversion and depletion of front gate, an opposite phenomenon is exhibited. In this case, capacitance increases with junction gate voltage. That is, inversion is easily achieved if junction gate bias is *higher*. Thus, a *higher* junction gate voltage *assists* inversion, while *retards* accumulation. The effects of back gate bias are found to be independent of junction gate bias and vice versa. Thus, it is concluded that back gate and junction gate biases have significant influence on front gate capacitance.

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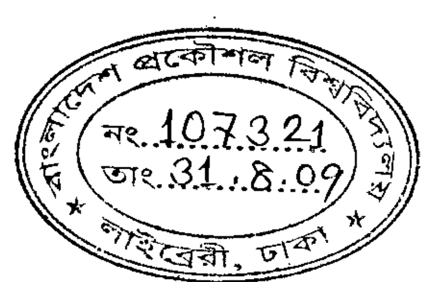
Chapter 1



Introduction

Over the last four decades, the advancement made in the Silicon CMOS technology has followed Moore's Law as predicted by Gordon Moore [1]. Since the invention of the integrated circuit (IC) in 1958, a systematic geometric scaling has been applied to increase the number of transistors placed inexpensively on an IC that has resulted in increased transistor count and operating frequencies, thus enabling tremendous technological progress. However, down-scaling device dimensions lead to some small-dimension effects in Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) which are mostly associated with the reduction in channel length (L). Reducing channel length below some minimum value may lead to velocity saturation, parasitic BJT action and even modification in the threshold voltage for the MOSFET [2]. Moreover, the conduction channel must be controlled by the gate, not by the drain. As L is reduced, drain-to-channel capacitance increases. Therefore, to increase the drive current, gate-to-channel capacitance must also be raised, i.e., oxide must be thinner. Thinner oxide results some undesirable effects such as greater leakage current which results in greater standby power consumption.

The International Technology Roadmap for Semiconductors (ITRS) projects a device gate-length of $\sim$9 nm for the year 2016 [3]. Scaling devices to these dimensions is much more difficult and different compared to existing scaling methodologies. This is because, MOS technology is approaching its limits at these dimensions. Reducing channel length below some minimum value may lead to some small dimension effect such as short channel effects (SCE)[4]. SCEs include threshold voltage (V_{TH}) variations versus channel length and drain induced barrier lowering (DIBL). Threshold voltage roll-off due to SCEs, results in a degraded sub-threshold swing (S), which in turn renders it difficult to turn off a device, while DIBL results in a drain voltage dependent V_{TH}, which complicates CMOS design

at a circuit level. As critical transistor dimensions are scaled, reliability concerns become more pronounced. Unwanted leakage currents due to gate tunneling and junction tunneling rapidly increase, resulting in high "OFF" state power dissipation. Therefore, device scaling increasing the number of transistors cannot continue forever.

The ITRS forecasts a transition from bulk to silicon-on-insulator (SOI) and then to multiple-gate SOI for high-performance digital integrated circuits [3]. In this respect, partially and fully depleted single-gate SOI MOSFET structures have been investigated as candidates for device below $\sim$25nm because they offer improved electrical isolation between substrate and the active device region, no body-effect, no latch-up, reduced S/D junction capacitance and better sub-threshold slope [5]. However, since these single-gate MOSFETs have a thick buried oxide which cannot terminate the electric field lines from the drain end, they exhibit severe SCEs [6, 7]. Recent studies indicate that ultra-thin body dual gate SOI MOSFETs are better suited for ultimate scaling.

The ITRS recommends not only switching from bulk to SOI, but also evolving from single-gate planar SOI transistors to multiple-gate devices [8] with improved current drive and short-channel characteristics. In an ever increasing need for higher current drive and better short-channel characteristics, silicon-on-insulator MOS transistors are evolving from classical, planar, single-gate devices into three-dimensional devices with multiple gates (double-, triple- or quadruple-gate devices) [9]. In a multi-gate device, the channel is surrounded by several gates on multiple surfaces, allowing more effective suppression of "OFF" state leakage current. Multiple gates also allow enhanced current in the "ON" state, also known as drive current. These advantages translate to lower power consumption and enhanced device performance. Nonplanar devices are also more compact than conventional planar transistors, enabling higher transistor density which translates to smaller overall microelectronics. Considering this technology trend, it is highly desirable to incorporate analog circuits into CMOS SOI.

In these devices, the term "multiple" generally represents the number of channels switched by one gate and not the number of gates. For example, the "tri-gate transistor" has only one gate covering the three sides of the body which leads to the three conduction channels switched together [10]. The four-gate transistor (G^4–FET), formerly known as MOS-JFET, was first introduced in 2002, features the maximum number of gates that can be accommodated in a single device and is a genuine four-gate transistor whose four gates

can be biased independently [11, 12]. Preliminary investigations confirm the potential of the G^4–FET for innovative analog circuits that can be conceived within a standard partially depleted SOI technology [13, 14, 15, 16]. Due to its multiple independent gates, the use of the G^4–FET enhances circuit design flexibility while reducing transistor count as compared to standard CMOS implementations [13, 14].

1.1 Literature Review

The novel idea of G^4–FET was first demonstrated by Blalock *et al.* in 2002 [11]. The G^4–FET was then known as MOS-JFET as the structure resembles a combination of MOSFET and JFET and the device can be operated either as a MOSFET or a JFET or a combination of both. The experimental results shown in Ref. [11] revealed that the fabricated device is fully functional and combines the effect of MOSFET and JFET. In the same year Cristoloveanu *et al.* provided the numerical studies to clarify the mechanisms of operation of G^4–FET [12].

A saturation current model for G^4–FET has been proposed by Dufrene *et al.* in 2003 based on conventional first order JFET model where the JFET gate-to-source voltage is replaced by V_{JG}, the bias voltage applied to the G^4–FETs junction (or lateral) gates [17]. Then, to include the additional MOS gate bias effects exhibited by the G^4–FETs saturation I-V characteristics, the new model develops hierarchical equations for the JFET zero-bias saturation current parameter, I_{D0}, and the pinch-off voltage, V_P.

High voltage performance of G^4–FET has been studied by Dufrene *et al.* in 2003 and it has been shown that the breakdown voltage of G^4–FET is beyond 15V [18], which is high compared to the breakdown voltage achievable by conventional SOI MOSFETs, making it suitable for high voltage applications.

The threshold voltage, sub-threshold swing, and mobility (viewed from the top gate or from the lateral gates) have been determined and discussed with the other gate biases as parameters by Akarvardar *et al.* in 2003 [19]. The sub-threshold slope modulations has been further examined and explained by Dufreene *et al.* in 2004 [20]. New data and an advanced analysis of G^4–FET features and performance by revealing the main conduction and gate-coupling mechanisms have been explained by Dufrene *et al.* in the same year [21]. The results have been explained using physics-based models of the G^4–FET as well as 3-D simulations. It has been shown that the sub-threshold swing carrier mobility and the

threshold voltages are functions of biases applied to the gates. With adjusted gate bias, the G^4–FET can offer a clear improvement in sub-threshold swing values (~65mV/decade for junction gates and ~73mV/decade for top gate). A high value of mobility, ~800cm^2/Vs, can be achieved by placing the channel in the middle of the film where electrons do not experience surface scattering.

An analytical threshold voltage model has been proposed by Akarvardar *et al.* in 2004 [22] where 2-D analytical relation for fully depleted body potential has been derived. Later in 2006 Akarvardar *et al.* have published another paper where the 2-D potential distribution in G^4–FETs is modeled based on a parabolical potential variation between the junction-gates [23]. The potential model is used to derive analytical expressions for the front threshold voltage of the G^4–FET for all possible steady-state charge conditions at the back interface.

In the G^4–FETs, the conducting channel can be surrounded by depletion regions induced by independent vertical MOS gates and lateral JFET gates. This unique conduction mechanism, named depletion-all-around (DAA) [24, 25], enable majority carriers to flow in the volume of the silicon film far from the silicon/oxide interfaces. The DAA operation of the SOI G^4–FET has been presented by means of experimental characteristics, 3-D simulations, and analytical modeling by Akarvardar *et al.* in 2007 [26]. It has been found that the biasing of the extra (front and back) gates can be used to considerably improve the performance while fully enjoying the integration density benefit of SOI CMOS technology. Especially when both interfaces are driven from depletion to inversion, the DAA operation provides a subthreshold swing of 60 mV/decade, high mobility, high transconductance, very high transconductance-to-current ratio and Early voltage, minimum-noise operation, and intrinsic radiation hardness.

The fully-depleted version of the G^4–FET is introduced and its characteristics are systematically investigated by Akarvardar *et al.* in 2007 [27]. It has been shown that the thinning-down of the silicon film promotes vertical coupling between the front and the back gates while mitigating the horizontal coupling between the lateral gates. As a consequence, the direct influence of the lateral junction-gates on the body potential distribution is reduced. However, by biasing the back interface in inversion the junction-gates can indirectly modulate the body potential. This provides a very efficient control of the front-channel conduction parameters–such as threshold voltage, sub-threshold swing

and transconductance–by the junction-gates regardless the device width. The experimental results are clarified by 3-D device simulations and analytical modeling.

1.2 Objective

The G^4–FET is a novel and emerging device that has attractive and promising features suitable for analog, mixed signal, RF, and single transistor logic applications. It has attracted attention of many researchers. So far, research is focused mainly in the functionality and performance study of G^4–FET: $I-V$ characteristics, threshold voltage, sub-threshold swing, mobility, transconductance [19, 20, 21, 24]. Some works has also been done in numerical and analytical modeling of output $(I-V)$ characteristics [17].

Circuit simulations are essential part of any kind of circuit design before it is practically implemented. Thus, simulation of circuits containing G^4–FET will also be necessary. And the simulations cannot be done without proper modeling of various characteristics of G^4–FET. Moreover, characterization of fabricated devices is also important. For determining the amount of trap charge inside the oxide region, threshold voltage, effective oxide thickness, $C-V$ characteristics are used. Although some numerical and analytical modeling of output $(I-V)$ characteristics has been performed by researchers, the Capacitance-Voltage $(C-V)$ characterization and modeling is yet to be done.

In this respect, the objectives of this thesis is to simulate and study the effects of multiple gate bias on the $C-V$ characteristics. In order to achieve this goal, the steps we have performed are:

- Implementation of a 2-D numerical $C-V$ model for simulating $C-V$ characteristics of the front gate of Fully Depleted (FD) G^4–FET while keeping other gate biases as parameters.

- Checking the validity the simulator (i) by performing $C-V$ simulation for G^4–FET in single MOSFET-like configuration and then by comparing it with the result obtained from 1-D simulator like Schred [28] (ii) by comparing the simulated surface potential profile of G^4–FET with published results [27].

- Performing simulations for multiple bias configurations of the other gates and to compare the results.

1.3 Organization of the Thesis

The thesis is organized as follows: The basic concepts, device structure, modes of operation and features and applications of G^4–FET is discussed in chapter 2. The Capacitance-Voltage modeling of G^4–FET is presented in chapter 3. Results of the proposed model are presented and discussed in chapter 4. And finally, chapter 5 concludes the thesis.

Chapter 2

The Four Gate Transistor: G^4–FET

2.1 Introduction

The G^4–FET, a novel and recent device, combines both MOS field-effect and junction field-effect for conduction control within a single transistor body taking full advantage of unique flexibility and isolation capability of SOI technology [11, 12]. Unlike in bulk-CMOS technology, where implementation of a transistor with more than two gates is difficult to imagine, the SOI-based G^4–FET allows manipulation of multiple gates through the combination of MOS gates and junction gates, from one to four, according to the application envisioned. Utilizing these gates separately, or in a combinatorial fashion, provides new circuit opportunities for analog, RF, mixed-signal and digital applications [13, 14, 16, 25, 29].

It should be noted that CMOS technology scaling should enhance the performance of the G^4–FET as MOS gate length shrinks (therefore reducing the lateral separation between the junction gates) [11]. This implies that it should be easier to pinch-off the conduction channel as technology is scaled, particularly if body doping of the transistor is optimized. Consequently, the G^4–FET is highly amenable to modern trends in the microelectronics industry.

2.2 Device Structure

An n-channel G^4–FET (the 3-D schematic diagram is shown in Figure 2.1(a), top view and cross section is shown in Figure 2.2) is formed from a p-channel SOI MOSFET (shown in Figure 2.1b) with two body contacts one on each side of the channel. The conversion between a *p*-channel SOI MOSFET and an *n*-channel G^4–FET is shown in Table 2.1. The

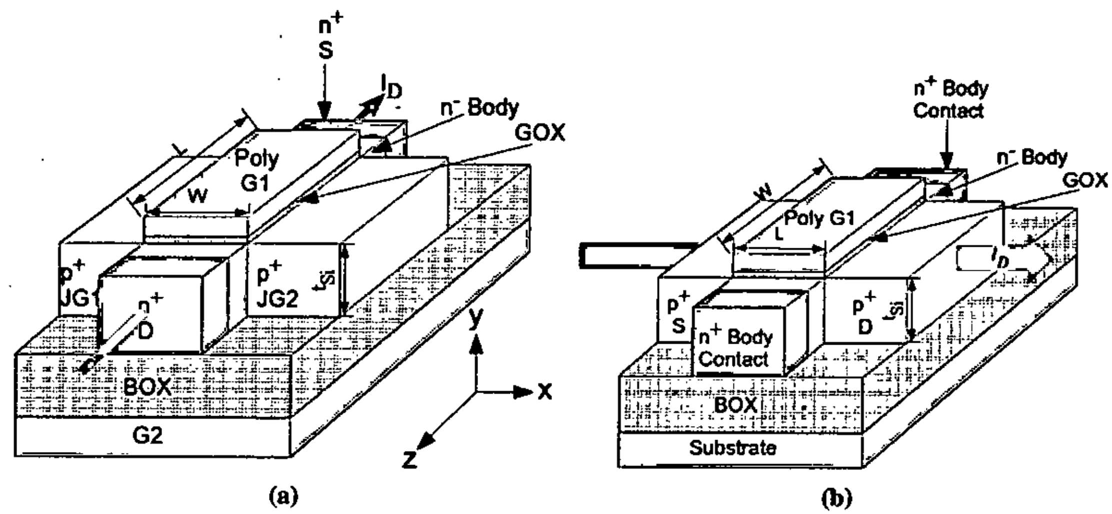


Figure 2.1: Three dimensional schematized structure of (a) an *n*-channel G^4–FET and (b) a *p*-channel SOI MOSFET. The arrow shows direction of current.

MOSFET	⟺	G^4–FET
p-channel	⟺	*n*-channel
n-channel	⟺	*p*-channel
Length	⟺	Width
Width	⟺	Length
Drain/Source	⟺	Lateral Junction Gates
Body Contacts	⟺	Drain/Source

Table 2.1: Conversion from MOSFET to G^4–FET.

n^+ body contacts of SOI MOSFET, connected to the *n*-type body acts as the source and drain of the G^4–FET. The former p^+ doped source and drain of the original *p*-channel SOI MOSFET play the role of *lateral junction gates (JG1 and JG2)* which controls the channel cross-section. With the possibility to bias the substrate as a *back-gate (G2)* and the poly-Si as a *top-gate (G1)*, the new device is indeed a four-gate transistor with narrow channel and accumulation mode operation [12].

Despite the structural similarity, there are some significant differences between the G^4–FET and the original MOSFET. In a G^4–FET, the drain current is composed of majority carriers unlike conventional SOI MOSFET where current flows due to minority carrier and flows in a direction perpendicular to that in the original inversion-mode MOSFET. The gate length of MOSFET defines the channel width W of the G^4–FET and the channel width of MOSFET defines the gate length L of G^4–FET. It should be emphasized that The G^4–FET does not require any special processing and is naturally adapted to CMOS technology

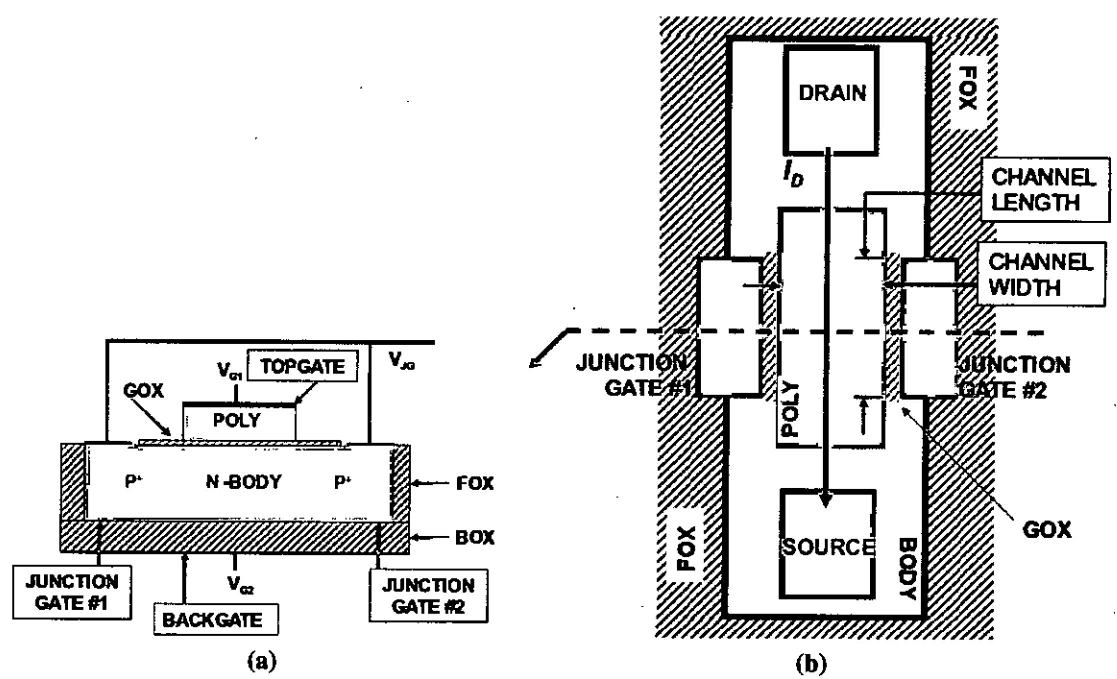


Figure 2.2: (a) Cross section and (b) top view of the G⁴–FET .

scaling. Device control is expected to increase as the two junction-gates come closer to one another [12].

2.3 Modes of Operation

The G^4–FET can be operated either like a JFET or like a MOSFET or like a combination of both. This section explains the operating modes of G^4–FET by showing the experimental and simulation results presented in Ref. [21].

Typical output $(I - V)$ characteristics of the n-channel G^4–FET are presented in Figure 2.3, where the different gate voltages are chosen to separately expose the operation of the lateral, front and back gates. For $V_{G1} = V_{G2} = 0$ V, the front and the back interfaces are weakly depleted so that the three bottom curves correspond only to the modulation of the volume current by the JFET effect of the lateral junction gates [see also cross section in Figure 2.4(a)]. For $V_{JG} = -1.6$ V, the body is pinched-off ($I_D = 0$). As V_{JG} approaches to 0 V, a volume channel appears and gradually widens. From the third to fourth curve, only the front gate voltage is changed ($V_{G1} = 1$ V), hence the front interface is driven from depletion to accumulation. In this case, the total drain current is the sum of the volume current and top interface accumulation current [cross section shown in Figure 2.4(b)]. Between the two

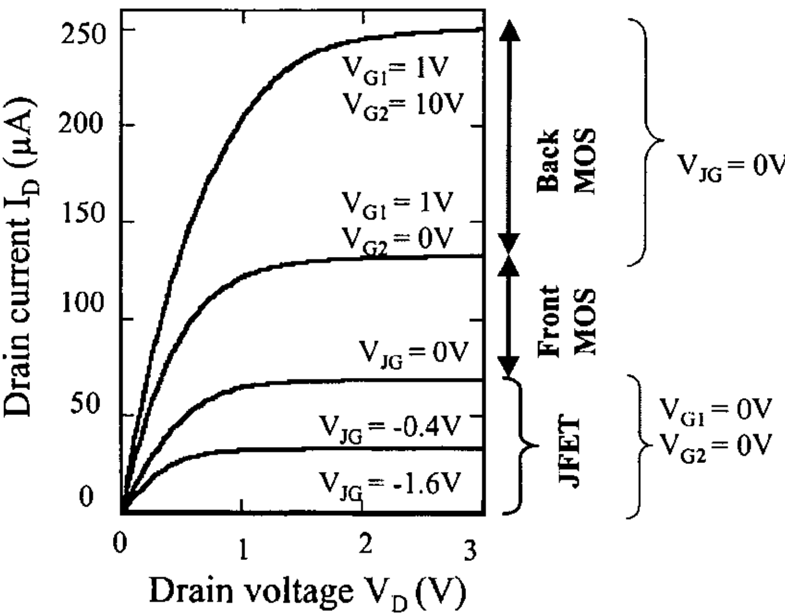
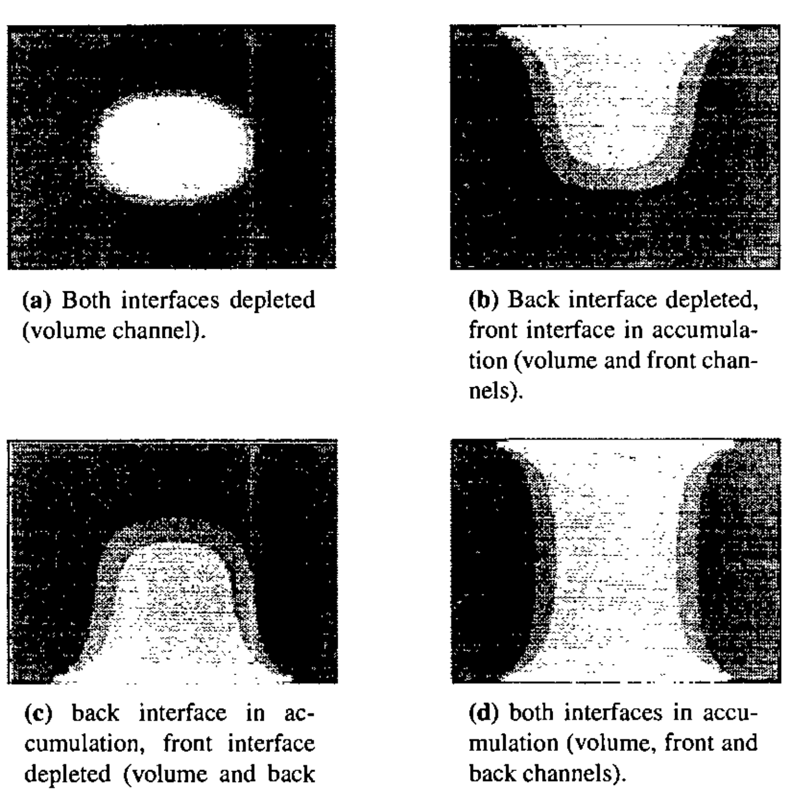


Figure 2.3: Typical output $(I-V)$ characteristics of the G^4–FET for various gate bias combinations [21].



(a) Both interfaces depleted (volume channel).

(b) Back interface depleted, front interface in accumulation (volume and front channels).

(c) back interface in accumulation, front interface depleted (volume and back channels).

(d) both interfaces in accumulation (volume, front and back channels).

Figure 2.4: Three-dimensional simulation of current density (J_D) in the channel cross section. Parameters: ohmic region ($V_D = 50$ mV), weak lateral depletion ($V_{JG} = 0$ V). Colors: white $J_D = J_{DMAX}$, grey $0.1J_{DMAX} < J_D < J_{DMAX}$, black $J_D < 0.1J_{DMAX}$ [21].

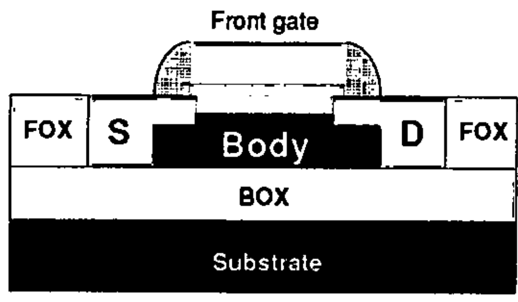


Figure 2.5: Partially depleted SOI MOSFET.

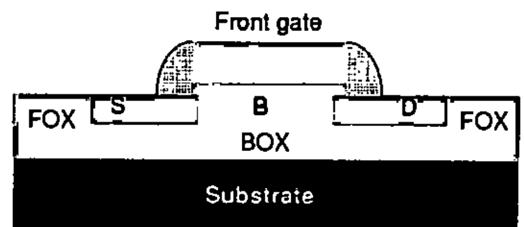


Figure 2.6: Fully depleted SOI MOSFET.

uppermost curves, the back-gate voltage is changed from 0 to 10 V while the other input voltages are held constant, so that an additional current flows at the accumulated back channel. The upper curve reflects the sum of all three possible components of the current [cross section shown in Figure 2.4(d)].

It should be apparent from Figure 2.3 that, in partially depleted G^4–FETs, two distinct modes of operation are identifiable [21]:

- **MOSFET mode**: operation based on the front-surface accumulation current controlled by V_{G1} while V_{G2} and $V_{JG1} = V_{JG2} = V_{JG}$ are parameters.
- **JFET mode**: operation based on the volume 'neutral' current controlled by V_{JG} while V_{G1} and V_{G2} are parameters inducing depletion or inversion at the interfaces.

However, in recently introduced fully depleted G^4–FET (FD G^4–FET) the volume component of the drain current is negligible due to full depletion and so, only MOSFET mode is available [27].

2.4 Partially and Fully Depleted G^4–FET

SOI devices can be fully depleted or partially depleted, where the amount of depletion refers to the channel region of a transistor. Partially depleted SOI transistors, as shown in Figure 2.5, resemble their bulk counterparts, where doping concentrations in the channel determine the depletion depth, leaving a neutral silicon "floating body" isolated from the grounded substrate residing below the buried oxide.

In contrast, a thin-film SOI transistor in which the depletion region extends down to the buried oxide, leaving no neutral region, is considered fully depleted. Fully depleted

transistors, as shown in Figure 2.6, require an ultra-thin silicon film to control short-channel effects, where the threshold voltage (V_T) depends heavily on the gate length, and in general provide only low-V_T transistors.

G^4–FET devices can also be fully depleted (FD G^4–FET) or partially depleted (PD G^4–FET). Earlier work on G^4–FETs has concentrated on thick film partially depleted devices [21, 26]. Only recently, Akarvardar *et al.* have introduced the characteristics of the thin film fully depleted G^4–FET [27]. It is important to underline that even in a PD G^4–FET, where the classical maximum depletion depth is less than the silicon film thickness ($x_{dmax} < t_{Si}$), the body can be fully depleted by the reverse-bias on the junction-gates [21]. However in a FD G^4–FET, full body depletion is enabled just by the doping-thickness combination ($x_{dmax} > t_{Si}$). In this thesis our investigations are focused on FD G^4–FET.

2.5 Features and Applications of G⁴–FET

The G^4–FET is a scalable device, adaptable to more aggressive technology nodes. The channel-length of the G^4–FET is as scalable as the channel-width of the regular SOI MOSFETs. A shorter MOSFET length means a narrower G^4–FET channel where the action of the lateral gates is further increased. If needed, the G^4–FET length can be reduced below 0.5 um. A specific limitation is to prevent direct tunneling between the adjacent n^+ and p^+ regions. However, the G^4–FET will not compete, on the size-related road-map, with FinFETs and double-gate ultra-thin MOSFETs which are more amenable to reach the 10 nm barrier. Instead, the G^4–FET is highly attractive in the future context of a functionality-related road-map.

The G^4–FET has the unique feature to allow independent switching of its four gates. It is demonstrated that the threshold voltage and other parameters associated with one gate depend on the biasing of the remaining gates. This property may be used to design circuits with programmable threshold devices in a given technology without additional process alterations (i.e., dopant adjustments, thick oxide). For example, the voltage reference circuit based on this concept [29] exhibits improved performance over the conventional SOI CMOS counterparts. In a similar way, the adjustable transconductance property of the G^4–FET can be used to design single-transistor adjustable-gain amplifier. The G^4–FET is suitable for both low-voltage (volume conduction) and high-voltage (increasing the distance between the channel and the drain) applications [18], which makes it an attractive

candidate for mixed-signal and RF applications. Low noise and high mobility are available, especially in volume conduction mode, giving rise to high-performance circuits.

The potential of the G^4–FET for digital applications warrants special consideration. In principle, the sectional dimensions (W and t_{Si}) and the body doping of the G^4–FET can be tailored to realize four-input NAND (case where a single input is sufficient to cut-off the current) or NOR (multiple inputs needed to switch off the transistor) functions using a single G^4–FET as a computation device. Furthermore, for a given device architecture, the G^4–FET can realize different functions (majority voting, NAND or NOR) with two or three inputs depending on the voltage applied to its fourth gate. However, the performance gain of such structures over conventional SOI CMOS is not known and it will depend on the circuit architectures. It is also interesting to note that the single device inverter [30] (which uses sequentially the lateral p-MOSFET and perpendicular accumulation mode n-MOSFET) has basically the same structure as the G^4–FET.

Another remarkable attribute of the G^4–FET is that the cross sectional position and size of the conducting channel within the body can be controlled. This feature promotes the potential to elucidate basic issues in device physics such as coupling effects, quantization effects in one-dimensional (quantum wires) versus two-dimensional systems, bulk versus surface transport, and noise.

The G^4–FET provides many exciting new circuit opportunities. Given the four-gate modulation demonstrated in [11] , ultra low-noise high-speed analog circuits should be realizable ("high-speed" based on the fact that bulk mobility is greater than surface mobility). The depletion-mode nature of the G^4–FET makes is well suited for low-voltage analog circuits. Single-stage, low power, high frequency modulators and RF mixers are also conceivable given the multiple input terminals per transistor. Combinatorial manipulations of the G^4–FET gates imply high-density (per transistor) digital logic. And given the high V_{DS} breakdown of these device, the G^4–FET is also suitable for 5V interface circuits and mixed-voltage systems-on-chip (SoC) requiring MEMS control functions. And finally, through four-gate modulation, electrically controlled wires seem plausible using the G^4–FET.

Chapter 3

The Capacitance-Voltage (C-V) Model

3.1 Capacitance

Since each of the four gates can modulate the conduction channel of G^4–FET [21], Capacitance of G^4–FET should be defined separately for each gate. Hence, we define the Capacitance with respect to the front gate (G1) as follows:

$$C_{G1} = \frac{\mathrm{d}Q_{G1}}{\mathrm{d}V_{G1}} \tag{3.1}$$

where, Q_{G1} is the total charge deposited on the front gate metal and V_{G1} is the front gate voltage. If we change the front gate voltage by a very small amount $\mathrm{d}V_{G1}$, the charge of the front gate changes. And in order to maintain charge neutrality, the charge of the Si body also changes by exactly same amount but opposite type. Thus,

$$C_{G1} = \frac{\mathrm{d}Q_{G1}}{\mathrm{d}V_{G1}} = \frac{-\mathrm{d}Q_{Si}}{\mathrm{d}V_{G1}} \tag{3.2}$$

where, Q_{Si} is the total charge deposited inside the Si body.

As the length of practical FD G^4–FET (~8μm) is much greater than its Si body thickness (~80 nm) [27], for calculating the capacitance we have ignored the effect of drain and source. In this regard, although, the G^4–FET is a 3-D device (see Figure 2.1(a)), a 2-D cross-section is used in our $C-V$ model, i. e., we assume that the potential distribution is constant along the z-direction. Hence, we redefine the front gate capacitance in *per unit (channel) length* as,

$$C'_{G1} = -\frac{\mathrm{d}Q'_{Si}}{\mathrm{d}V_{G1}} \tag{3.3}$$

where, Q'_{Si} is the charge per unit length deposited inside the Si body.

The cross section that has been used for our study is shown in Figure 3.1. Here, W is the width, t_{Si} is the thickness of Si body, t_{GOX} is the front gate oxide thickness and

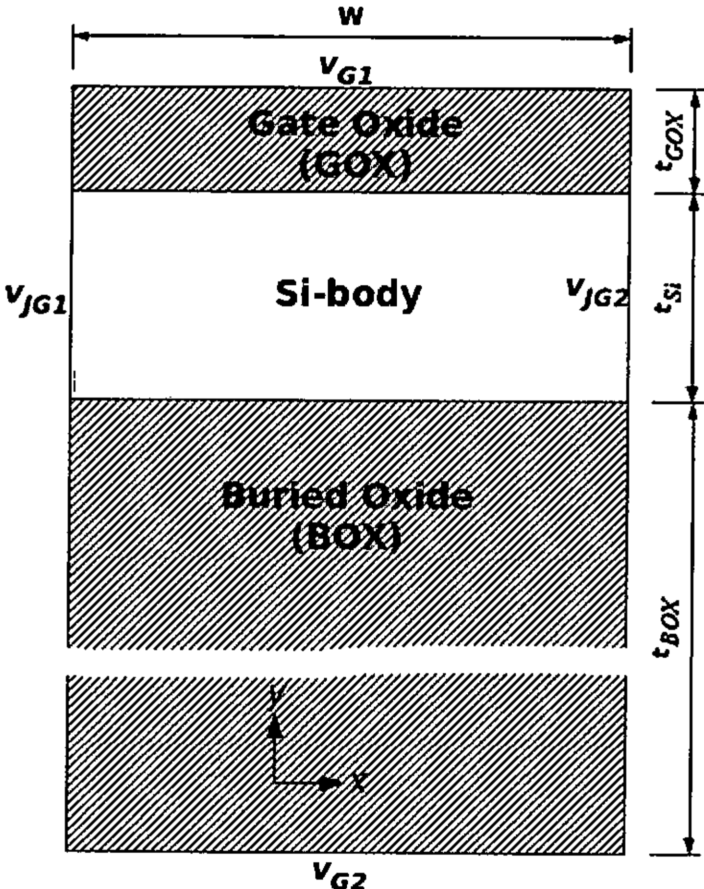


Figure 3.1: The geometry used in simulation (Cross section of the G^4–FET).

t_{BOX} is the buried/back-gate oxide thickness. It should be mentioned that the structure we have used to simulate the G^4–FET does not contain the junction gates and the front and back gates, since we assume that the p^+ junction gates, the poly-Si gate and the back substrate acts as a conductor and have negligible effect on $C-V$. In order to calculate the capacitance, we have to calculate the change in charge per unit area inside the Si body of G^4–FET for a very small change in front gate voltage V_{G1}.

3.1.1 Poisson's Equation

The electrostatics inside the G^4–FET is governed by Poisson's equation. The general form of it in three dimensional Cartesian co-ordinate system is given by,

$$-\nabla.(\varepsilon\nabla V) = \rho \tag{3.4}$$

where, $\nabla \equiv (\hat{x}\frac{\partial}{\partial x} + \hat{y}\frac{\partial}{\partial y} + \hat{z}\frac{\partial}{\partial z})$, V is the electrostatic potential, ρ is the charge density (charge per unit volume) and ε is the permitivity. Both V and ρ are functions of space

co-ordinates.

In two dimension, Eq. (3.4) reduces to the following form and is used to find the potential profile inside the cross section of G[4]–FET as shown in Figure 3.1,

$$(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2})V(x,y)=\begin{cases}\frac{\rho(x,y)}{\varepsilon_0\varepsilon_{Si}}, & \text{if } 0\leq x\leq W \text{ and } 0\leq y\leq t_{Si}\\ 0, & \text{if } 0\leq x\leq W,\ t_{Si}<y\leq t_{Si}+t_{GOX}\\ & \text{and } -t_{BOX}\leq y<0\end{cases} \tag{3.5}$$

where, ε_{Si} is the dielectric constant of silicon ε_0 is the free space permitivity.

3.1.2 Semi-classical Formalism

Semi-classically, the charge density inside the Si body can be calculated from ,

$$\rho(x,y)=q[p(x,y)-n(x,y)+N_D^+-N_A^-] \tag{3.6}$$

where, q is the magnitude of the charge of an electron, $p(x,y)$, $n(x,y)$, N_D^+ and N_A^- respectively being the electron, hole, ionized donor and acceptor concentration. If complete ionization is assumed, $N_D^+=N_D$ and $N_A^-=N_A$. Concentrations of hole and electron are calculated using semi-classical formula,

$$p(x,y)=p_0\exp(\frac{-\phi(x,y)}{\phi_t}) \tag{3.7}$$

and

$$n(x,y)=n_0\exp(\frac{\phi(x,y)}{\phi_t}) \tag{3.8}$$

where, n_0 and p_0 are equilibrium electron and hole concentrations, respectively and $\phi(x,y)$ and ϕ_t are band bending profile and thermal potentials, respectively. The band bending profile $\phi(x,y)$ is actually equal to $V(x,y)$ when the applied voltages of the front and back gates are adjusted with the flat band voltages of the respective gates and the junction gate voltage is adjusted with built-in potential of the junction gates.

3.1.3 The $C-V$ Model

For particular values of front gate voltage V_{G1}, back gate voltage, V_{G2} and junction gate voltage V_{JG}, the Poisson's equation, (Eq. (3.5)) and the charge density equation, (Eq. (3.6))

can be solved iteratively to calculate the electrostatic potential profile inside the 2-D G^4–FET subject to the boundary conditions:

$$V(x,y) = \begin{cases} V_{G1}, & \text{if } 0 \leq x \leq W \text{ and } y = t_{Si} + t_{GOX} \\ V_{G2}, & \text{if } 0 \leq x \leq W \text{ and } y = -t_{BOX} \\ V_{JG}, & \text{if } x = 0 \text{ or } x = W \text{ and } 0 < y < t_{Si} \end{cases} \tag{3.9}$$

After the iteration process has converged, the band bending profile $\phi(x,y)$ is calculated from potential profile $V(x,y)$, and the charge density inside the G^4–FET is calculated from Eq. (3.6). Once the charge distribution is known, the total charge inside the Si cross section, Q'_{Si} is obtained from Eq. (3.10).

$$Q'_{Si} = \int_{x=0}^{W} \int_{y=0}^{t_{Si}} \rho(x,y)\,\mathrm{d}y\,\mathrm{d}x \tag{3.10}$$

And then the whole process is repeated for a new front gate voltage $V_{G1} + \mathrm{d}V_{G1}$ while keeping the other voltages constant and for this voltage a new charge $(Q'_{Si} + \mathrm{d}Q'_{Si})$ is obtained from Eq. (3.10). In theory, the capacitance, C'_{G1} is then calculated by using Eq. (3.3).

3.2 Implementation of the Proposed Model

The implementation of the proposed $C-V$ model involves calculation of the numerical solution of Eq. (3.5), a second order partial differential equation (PDE), with Eq. (3.6) iteratively, and performing numerical integration and differentiation. The Finite Element Method (FEM) is used for solution of the PDE.

In COMSOL Multiphysics, Poisson's equation in general co-efficient form in three dimension is,

$$-\nabla.(c\nabla u) = f \tag{3.11}$$

where, c is the diffusion co-efficient, f is the source term and u is the dependent variable. Comparing Eq. (3.4) and Eq. (3.11) the following relationships between the co-efficients can be established,

$$\begin{aligned} u &\equiv \text{Electrostatic Potential, } V \\ c &\equiv \text{Dielectric Permitivity, } \varepsilon \text{ and} \\ f &\equiv \text{Charge Density, } \rho \end{aligned} \tag{3.12}$$

In two dimension, everything holds except that ∇ is translated to $\hat{x}\frac{\partial}{\partial x}+\hat{y}\frac{\partial}{\partial y}$.

The simulation process is started by defining the 2-D geometry of G^4–FET as shown in Figure 3.1. This is done by invoking MATLAB interface of COMSOL. The geometry consists of Gate Oxide (GOX), Si Body and Buried Oxide (BOX) (see Figure 3.1). In COMSOL, each of this regions is termed as subdomain and is identified by a unique numeric value. Here, the source term, f of Eq. (3.11) can be defined separately for each subdomain. For our case, inside the subdomains GOX and BOX, ρ is zero which implies, $f=0$ and $c=\varepsilon_0\varepsilon_{SiO_2}$, and inside the Si-body, $\rho(x,y)$ is calculated using Eq. (3.6) and $c=\varepsilon_0\varepsilon_{Si}$. Each edge of the geometry is termed as boundary and is identified by a unique numeric value. For every boundary, either Dirichlet or Neumann condition can be applied. The application of various gate voltages are translated to Dirichlet boundary conditions applied on the edges.

After specifying all subdomain settings and boundary conditions, an initial voltage profile is used to calculate the initial charge density profile of Si body. At the beginning of simulation, the voltage all over the geometry is assumed to be zero. Charge density is then calculated using Eq. (3.6). The Poisson's equations is then solved by using this initial charge density profile. From the solution of Poisson's equation, new voltage profile is obtained and is used for calcuation of new charge density profile. The new charge density profile is then used as input to Poisson's equation. The whole process is repeated iteratively until the maximum difference between the voltages calculated from two successive iterations is less than a predefined error. When this difference is less than the predefined error value, the solution is said to have converged.

For the numerical convergence a weighting factor is used which is shown in Eq. (3.13),

$$V_{intrp}=V_{old}\times\alpha+V_{new}\times(1-\alpha) \tag{3.13}$$

where, V_{intrp} is the new interpolated voltage profile for calculating the charge density profile, V_{old} is the previous profile, V_{new} is the new profile, α is the weighting factor. At the end of an iteration, the V_{intrp} is assigned into V_{old}.

After the convergence, numerical integration is performed to calculate the charge inside the Si as dictated by Eq. (3.10). For every 0.05V interval of front gate voltage, V_{G1}, charge $Q^{'}_{Si}$ is calculated using above procedure. $C-V$ is obtained by performing numerical differentiation of $Q^{'}_{Si}$ with respect to V_{G1}.

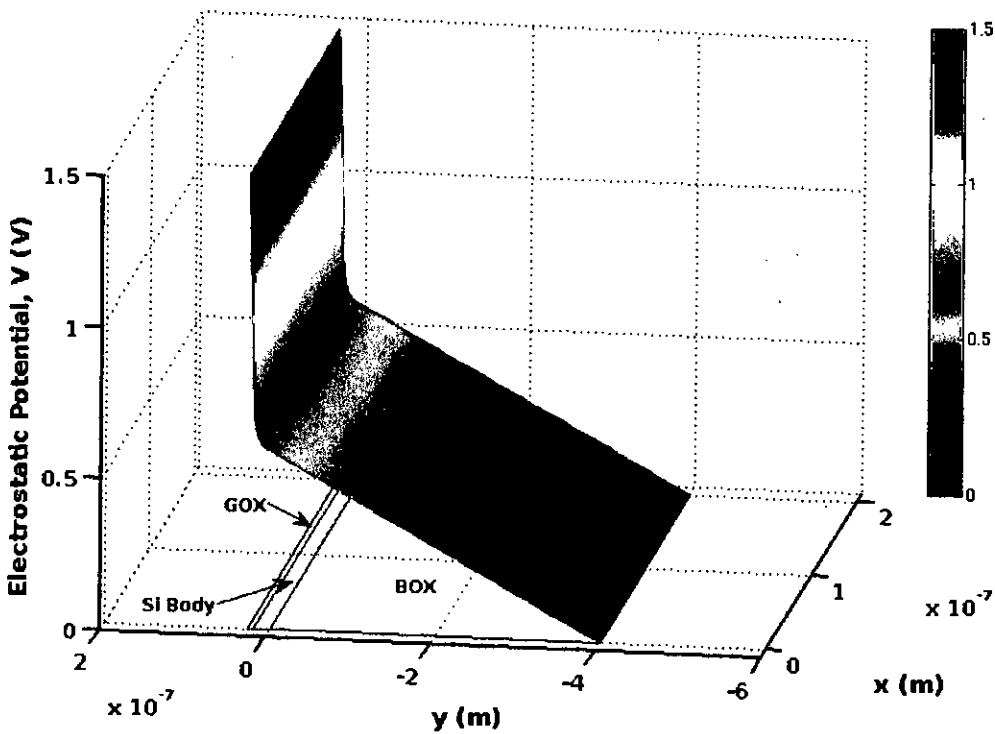


Figure 3.2: Electrostatic Potential profile inside the DGMOSFET for $V_{G1} = 1.5$ V and $V_{G2} = 0$ V.

3.2.1 Simulator Validation

The validity of proposed model and simulator have been checked by comparing its results with semi-classical results predicted by Schred [28] and with the results provided by Akarvardar *et al.* [27].

Comparison with Schred

Schred is a 1-D single/double gate MOS capacitance simulator. For comparing our results with that given by Schred, simulation of an n-channel double gate MOSFET (DGMOSFET) has been performed where following parameters have been used [27]: gate oxide thickness, $t_{GOX} = 7$ nm, buried oxide thickness, $t_{BOX} = 400$ nm, Si-body thickness, $t_{Si} = 20$ nm doping density, $N_A = 1 \times 10^{-13}$ cm^{-3}, metal work function $\phi_m = 4.05$ eV and ionization energy of the dopant atom is 0.05 eV. As the proposed simulator is 2-D whereas Schred is a 1-D single/double gate MOS simulator, junction gates have been kept floating in order for configuring implemented simulator as a 2-D *double gate* MOS simulator and for maintaining compatibility with Schred.

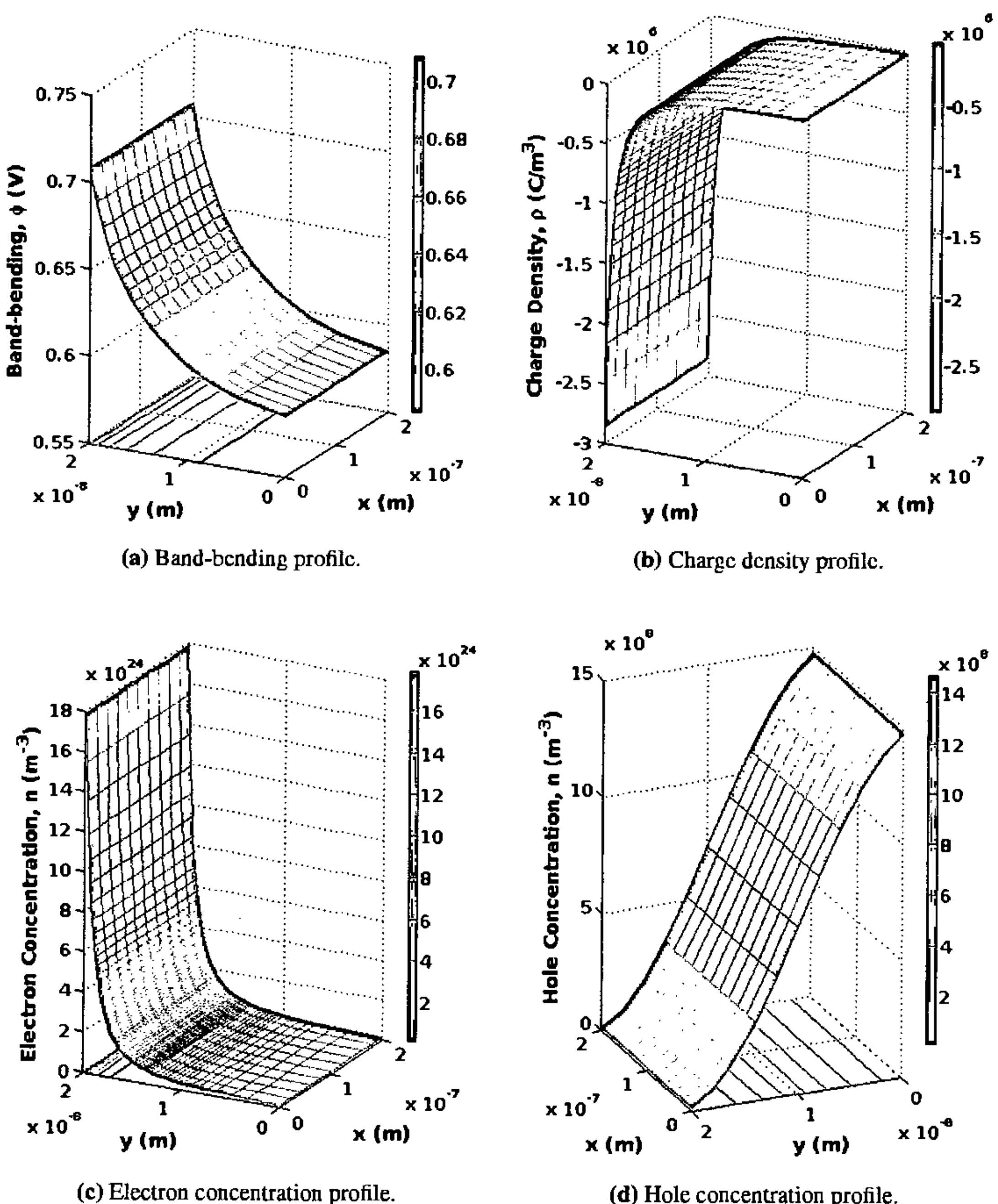
Firgue 3.2 shows simulated the voltage profile of the double gate device with front gate voltage, $V_{G1} = 1.5$V and back gate voltage, $V_{G2} = 0$V. It is noted that there is no variation of potential profile along the x direction which is a direct consequence of keeping the junction gates floating. In this configuration, results of the proposed simulator resembles results of a 1-D simulator.

Figure 3.3 provides the simulated band-bending, charge density, electron and hole concentration profiles. As expected, at $V_{G1} = 2.26$ V and $V_{G2} = 0$ V, the front gate is in strong inversion. In this condition, inversion charge resides near the front Si/SiO_2 interface which is evident from Figure 3.3(b). This inversion layer is formed by electron [see Figure 3.3(c) and Figure 3.3(d)] which is the minority carrier of the Si-body.

The $C-V$ characteristics of the above mentioned device predicted by our simulator and Schred are shown in Figure 3.4. Here, we have assumed the flatband voltage of the front gate to be -0.76 V. From the figure it is clear that the result of our simulator is in good agreement with the result of Schred.

Comparison with Results of Akarvardar *et al.* [27]

Akarvardar *et al.* has demonstrated FD G^4–FET for the first time in 2007 [27]. In order to clarify the FD G^4–FET operation, 3-D dimensional simulation using Silvaco tools has also been provided there. Two dimensional simulation of the cross section of the same device has been performed by using the proposed model for the same parameters: gate oxide thickness, $t_{GOX} = 7$ nm, buried oxide thickness, $t_{BOX} = 400$ nm, Si-body thickness, $t_{Si} = 20$ nm, doping density, $N_A = 1 \times 10^{-16}$ cm^{-3}, front gate voltage, $V_{G1} = -0.75$ V, backgate voltage, $V_{G2} = 0$ V, and junction gate voltage, $V_{JG1} = V_{JG2} = V_{JG} = 0$ V). Figure 3.5 shows the comparison between the two results. Results are found to be quite close.



(a) Band-bending profile.

(b) Charge density profile.

(c) Electron concentration profile.

(d) Hole concentration profile.

Figure 3.3: Two-dimensional simulation results of DGMOSFET in the channel cross section in inversion. Parameters: $V_{G1} = 2.26\text{V}$ and $V_{G2} = 0\text{V}$.

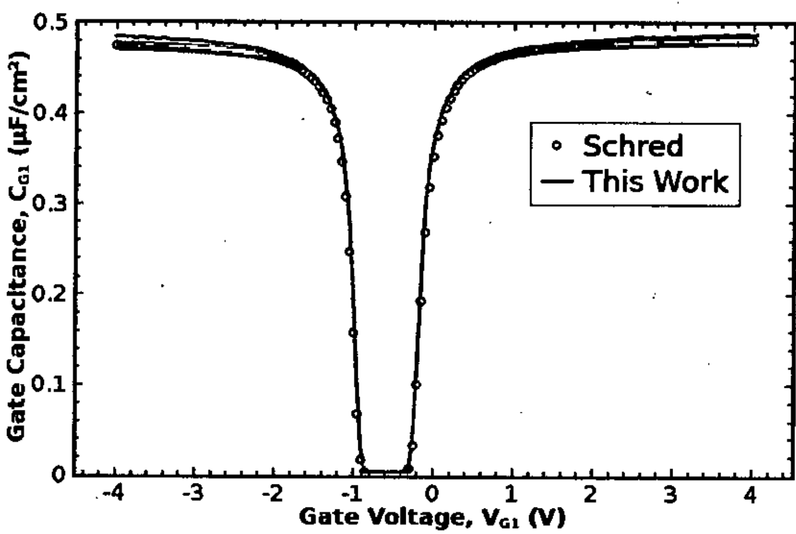


Figure 3.4: $C-V$ characteristics of DGMOSFET. Comparison between proposed simulator with Schred is shown.

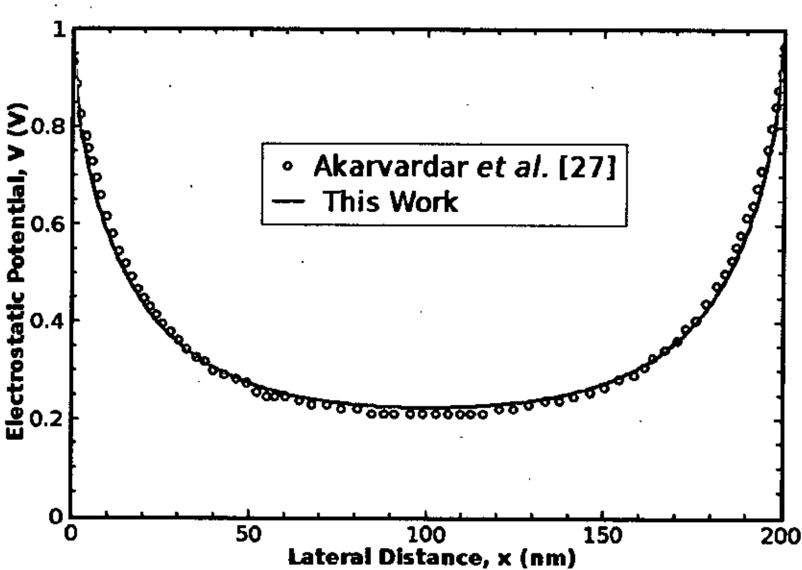


Figure 3.5: 2-D simulation results for the front surface potential profiles between the junction-gates at mid-length of a 1μm long p-channel G^4–FET. Comparison between the result of proposed model and that of Akarvardar *et al.* [27] is shown.

Chapter 4

Results and Discussions

4.1 Introduction

In order to find out the impact of multiple-gate biases on front gate $C-V$ characteristics, some systematic simulations has been performed. A set of simulations has been performed to calculate front gate capacitance for different back gate voltages while keeping junction gate voltage constant. Another set of simulations has been performed to calculate the front gate capacitance for different junction gate voltages while keeping back gate voltage constant.

The geometry of G^4–FET structure used in our simulations is shown in Figure 3.1 with the parameters used by Akarvardar *et al.* in their simulations [27]. The parameters are: gate oxide thickness, $t_{GOX} = 7$ nm, buried oxide thickness, $t_{BOX} = 400$ nm, Si-body thickness, $t_{Si} = 20$ nm, doping density, $N_A = 1 \times 10^{16}$ cm^{-3}. The front and back flat-band voltages, V_{FB1} and V_{FB2} and junction built-in potential V_{bi} are assumed to be zero. For simplicity, the two junction gates are assumed to be tied together.

4.2 Effects of Back Gate Bias

4.2.1 Observations

In order to find out the effects of back gate bias on $C-V$, simulations have been performed for back gate voltages, $V_{G2} = -30$, 0, 30 and 60 V while keeping junction gate voltage, $V_{JG} = 0$ V. The results are shown in Figure 4.1. It is observed that in strong inversion or accumulation of front gate, effect of back gate bias is insignificant.

But in weak accumulation, weak inversion and in depletion of the front gate, the back gate bias causes a significant change on $C-V$. For $V_{G2} = 0$ V, the device is fully depleted

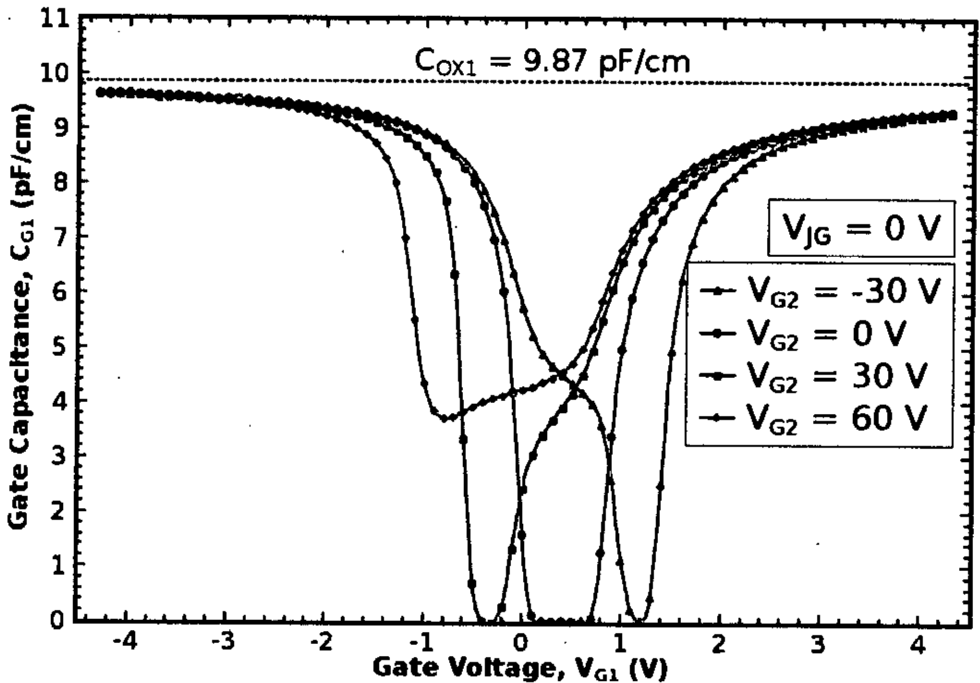


Figure 4.1: $C-V$ characteristics of front gate for various back gate biases: $V_{G2} = -30$, 0, 30 and 60 V with junction gate voltage, $V_{JG} = 0$ V.

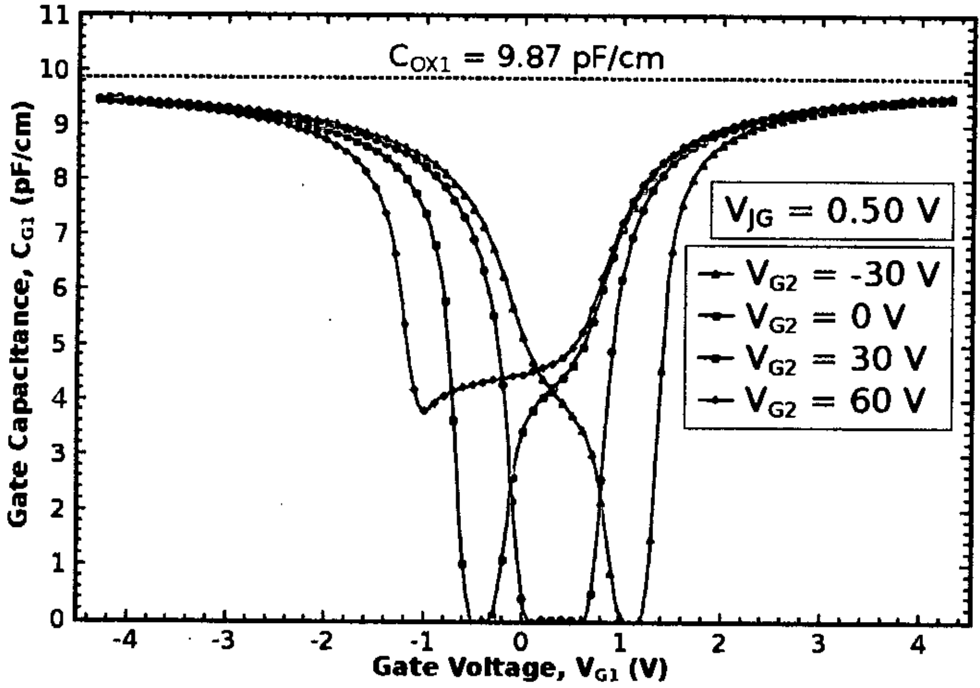


Figure 4.2: $C-V$ characteristics of front gate for various back gate biases: $V_{G2} = -30$, 0, 30 and 60 V with junction gate voltage, $V_{JG} = 0.50$ V.

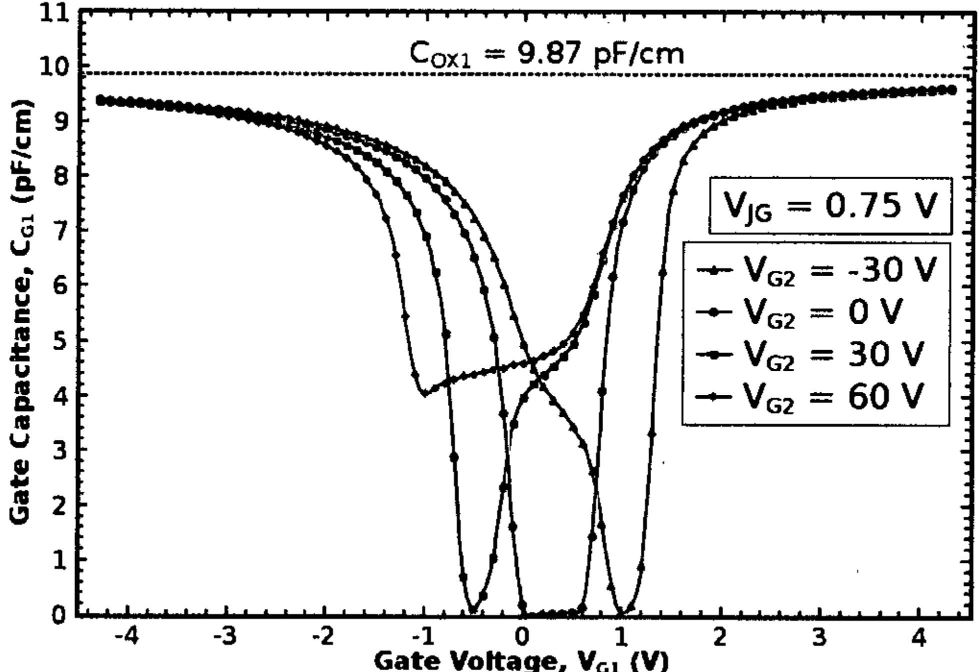


Figure 4.3: $C-V$ characteristics of front gate for various back gate biases: $V_{G2} = -30$, 0, 30 and 60 V with junction gate voltage, $V_{JG} = 0.75$ V.

and hence capacitance becomes zero in between $V_{G1} = 0.1$ V and $V_{G1} = 0.7$ V. However, when the back gate is in inversion at $V_{G2} = 30$ V, the full depletion can not be achieved for $V_{G1} = 0.1$ to 0.7 V. In this case, full depletion occurs for $V_{G1} = -0.4$ to -0.3 V. It is also noted that for strong inversion of the back gate at $V_{G2} = 60$ V, the device can not be fully depleted at all, that is, the back gate inversion charge can not be removed totally by means of front gate voltage.

The $C-V$ curve at $V_{G2} = -30$ V (back gate accumulation), is almost the mirror image of the $C-V$ curve at $V_{G2} = 30$ V (back gate inversion). Whatever happens in weak inversion of front gate for $V_{G2} = 30$ V, happens in weak accumulation of front gate for $V_{G2} = -30$ V. In this case, a positive voltage on front gate is required in order to achieve full depletion where the capacitance is zero.

Another noticeable effect is that the onset of accumulation is shifted by the back gate bias voltage. For $V_{G2} = 0$ V, accumulation starts at approximately $V_{G1} = -0.1$ V, for $V_{G2} = 30$ V, however, accumulation starts at approximately, $V_{G1} = -0.5$ V and for $V_{G2} = 60$ V onset of accumulation is approximately, $V_{G1} = -1$ V. Similar phenomena are observed for $V_{JG} = 0.50$V [Figure 4.2] and $V_{JG} = 0.75$V [Figure 4.3].

Therefore, we conclude that impacts of back gate bias are:

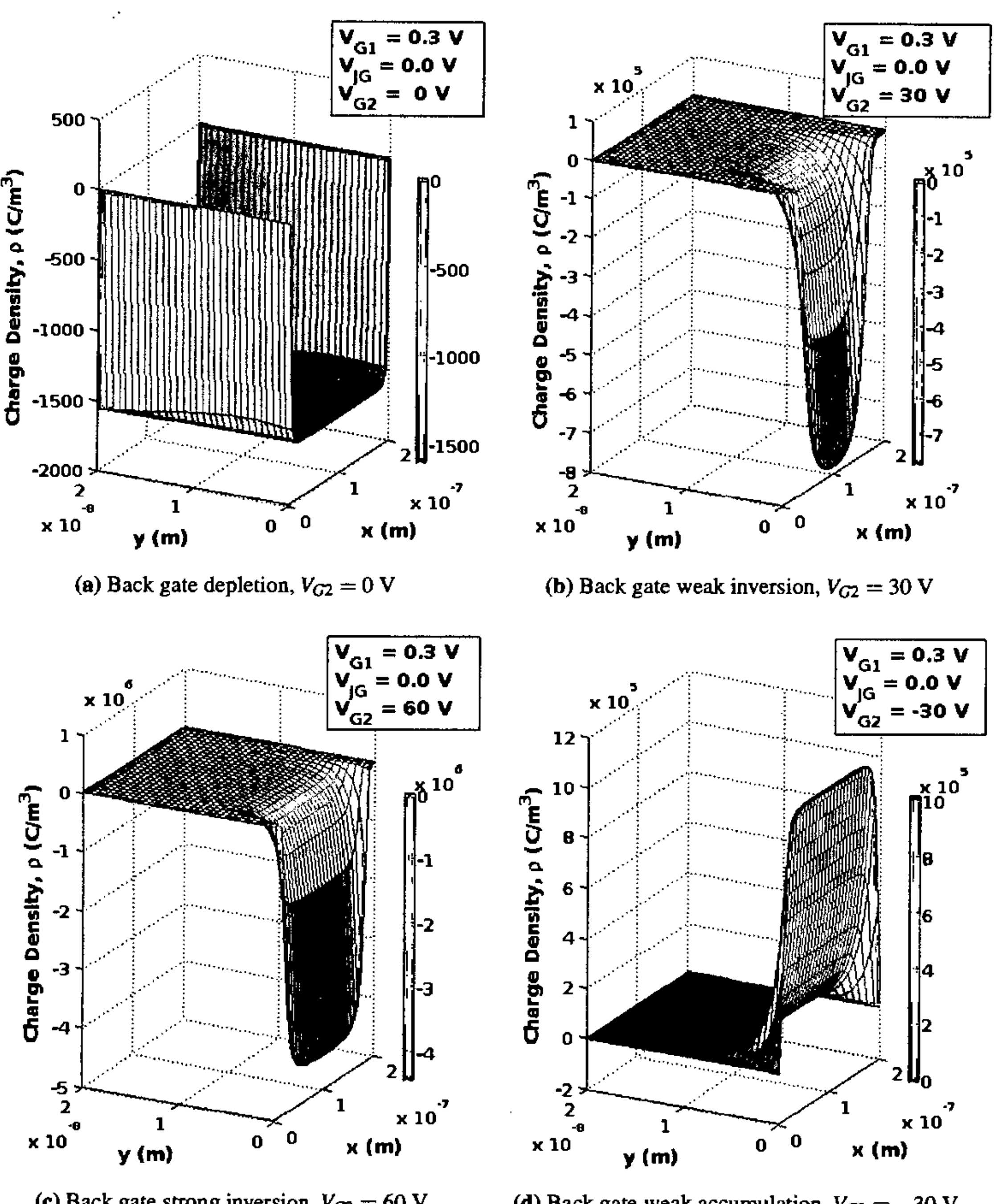
- *Insignificant* in strong inversion and strong accumulation of front gate.
- *Significant* in depletion, weak inversion and weak accumulation of front gate. An accumulation/inversion channel at back gate retards zero capacitance to be achieved. A very strong inversion/accumulation channel of back gate cannot be mitigated by applying front gate bias, that is zero capacitance cannot be achieved.
- *Similar* for different junction gate biases.

4.2.2 Physical Explanation

As defined by Eq. (3.3), the negative rate of change of total charge inside the Si body cross section with respect to applied front gate voltage is the measure of the capacitance of the front gate. Thus, if one calculates the rate of change of charge *density* profile, $\Delta\rho(x,y)$ with respect to front gate voltage, one gets an idea of which parts of the Si body have significant contribution to the gate capacitance. From this calculation, the impacts of back gate bias on $C-V$ characteristics can be explained. Figure 4.4 shows the charge density profiles, $\rho(x,y)$ inside the Si body of G^4–FET for $V_{G1} = 0.3$ V, $V_{JG} = 0$ V and for different back gate bias conditions, $V_{G2} = -30,\ 0, 30$ and 60 V. The change in charge density profiles, $\Delta\rho(x,y)$ for a small change in applied front gate bias voltage are shown in Figure 4.5.

From Figure 4.4(a) it is obvious that the body is fully depleted when the back gate is biased with $V_{G2} = 0$ V. As the body is fully depleted, the change in charge density, $\Delta\rho(x,y)$ is very small as shown in Figure 4.5(a). A very small change in charge density provides a very small change in total charge inside the body cross section which in turn dictates the capacitance to become zero. Thus the capacitance at ($V_{G1} = 0.3$ V, $V_{JG} = 0$ V, $V_{G2} = 0$ V) is almost zero.

When the back gate is biased with $V_{G2} = 30$ V, the back interface becomes weakly inverted as shown in Figure 4.4(b). As the Si body is very thin, the coupling between the front and the back gate is strong and hence a small change in front gate voltage is translated to a large change in back interface inversion charge [Figure 4.5(b)]. Thus the capacitance in this case ($V_{G1} = 0.3$ V, $V_{JG} = 0$ V, $V_{G2} = 30$ V) is *nonzero*. From Figure 4.5(b), it is evident that maximum amount of change occurs at the back interface and the change is negligible elsewhere. Thus the device acts as if two parallel plates of a capacitor were placed apart by



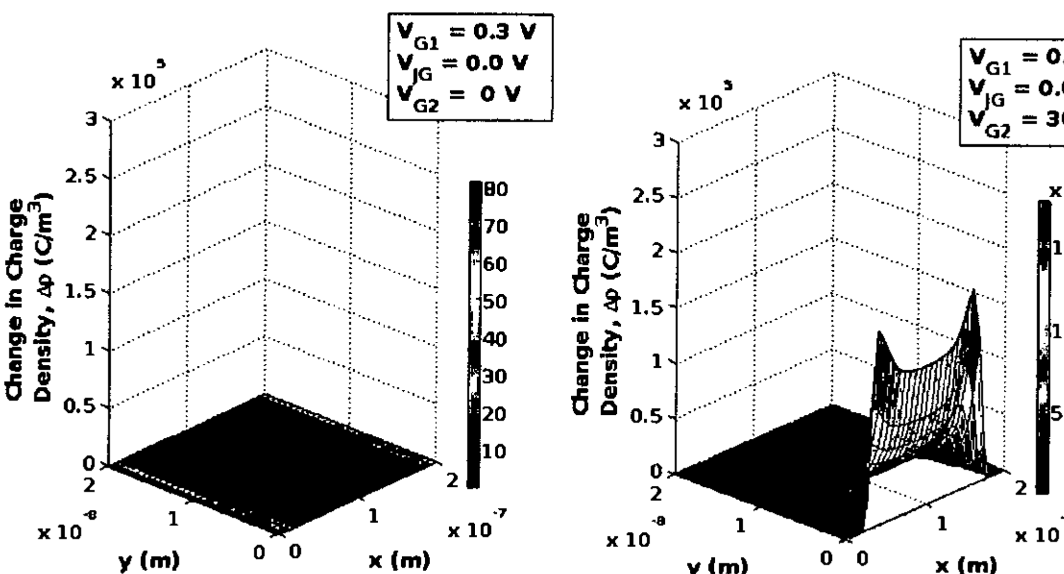
(a) Back gate depletion, $V_{G2} = 0$ V

(b) Back gate weak inversion, $V_{G2} = 30$ V

(c) Back gate strong inversion, $V_{G2} = 60$ V

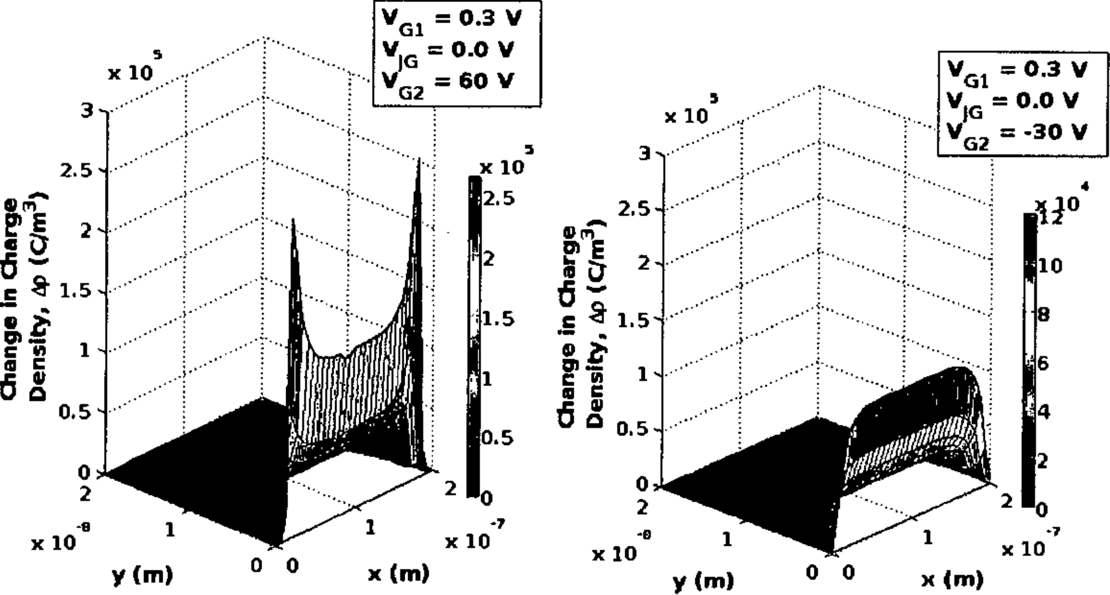
(d) Back gate weak accumulation, $V_{G2} = -30$ V

Figure 4.4: Charge density profile inside the channel cross section for different back gate bias conditions.



(a) Back gate depletion, $V_{G2} = 0$ V. Change in charge density is very small.

(b) Back gate weak inversion, $V_{G2} = 30$ V. Change in charge density of back interface inversion layer determines the capacitance.



(c) Back gate strong inversion, $V_{G2} = 60$ V. Change in charge density of back interface increases and so, the capacitance increases.

(d) Back gate weak accumulation, $V_{G2} = -30$ V. Change in charge density of back interface accumulation layer determines the capacitance.

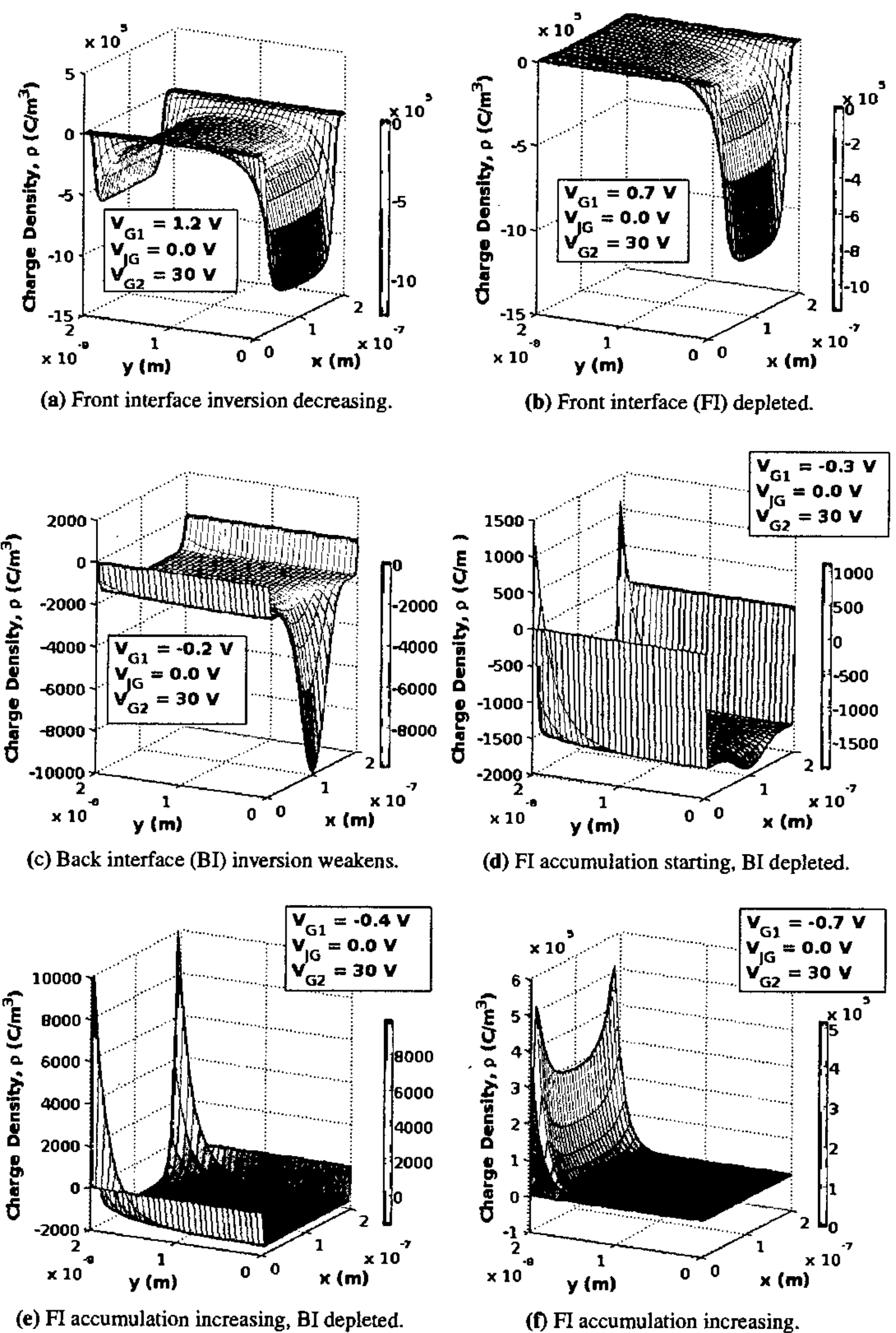
Figure 4.5: Change in charge density profile inside the channel cross section for different back gate bias conditions.

a layer of SiO_2 (with thickness, t_{GOX}) and a layer of depleted Si (with thickness, t_{Si}) side by side inside them. Therefore, effectively, the capacitor thickness ($t_{GOX} + t_{Si}$) becomes larger than the oxide thickness alone (t_{GOX}) and the capacitance becomes less than the oxide capacitance alone ($0 < C < C_{ox1}$). Similar phenomenon is observed for back gate accumulation [Figure 4.4(d) and 4.5(d)] but in this case the back gate *accumulation* charge is modulated by the front gate voltage.

The shape of $C - V$ curves for back gate inversion ($V_{G2} = 30$ V) is further clarified by Figure 4.6 and 4.7. The charge density profile $\rho(x,y)$ and the change in charge density profile, $\Delta\rho(x,y)$ inside the Si body cross section for different front gate voltages (starting from inversion to accumulation) are shown in Figure 4.6 and 4.7, respectively.

At $V_{G1} = 1.2$ V, the front interface inversion layer is weakening but back interface inversion layer remains almost unchanged [Figure 4.6(a), Figure 4.7(a)]. Hence the capacitance is determined by the change in front interface charge density. With the decreasing front gate bias, the level of front interface inversion weakens and change in the front interface charge density decreases; and so, capacitance decreases. At $V_{G1} = 0.7$ V, the front interface inversion layer vanishes [Figure 4.6(b)] and the capacitance decreases but does not become zero as the change in charge density of back interface starts to dominate [Figure 4.7(b)]. Further decrease in front gate bias weakens the back interface inversion layer. At $V_{G1} = -0.2$ V, the back interface inversion layer further weakens [Figure 4.6(c)] and the capacitance decreases as the change in charge density decreases [Figure 4.7(c)]. If more negative voltage is applied, the back interface inversion layer mitigates and front interface accumulation layer starts to appear [Figure 4.6(d), Figure 4.7(d)] and the capacitance becomes very low. At $V_{G1} = -0.4$ V, the front interface is very weakly accumulated [Figure 4.6(e)] and change in front interface charge density starts to take over [Figure 4.7(e)]; hence, the capacitance starts to increase. With the decreasing front gate bias, the level of front interface accumulation increases and the capacitance increases. At $V_{G1} = -0.7$ V, the front interface is weakly accumulated [Figure 4.6(f)] and change in front interface charge density becomes dominating [Figure 4.7(f)] and so, the capacitance starts to increase. In similar fashion, the shape $C - V$ curve for back gate accumulation ($V_{G2} = -30$ V) can be explained.

The back interface goes deeper into inversion if 60 V is applied to the back gate [Figure 4.4(c)] and the change in charge density [Figure 4.5(c)] is increased further along



(a) Front interface inversion decreasing.

(b) Front interface (FI) depleted.

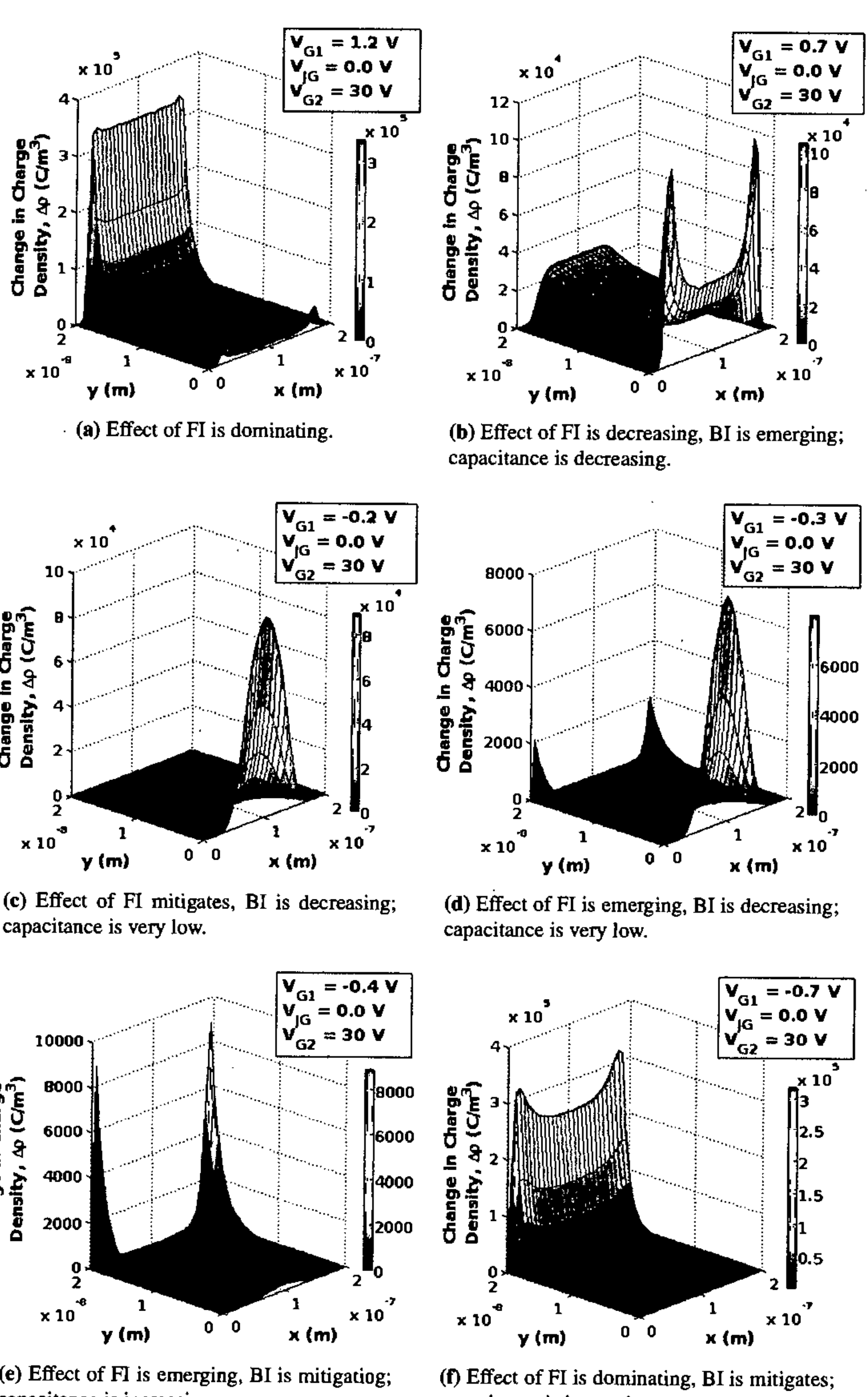
(c) Back interface (BI) inversion weakens.

(d) FI accumulation starting, BI depleted.

(e) FI accumulation increasing, BI depleted.

(f) FI accumulation increasing.

Figure 4.6: Charge density profile inside the channel cross section for different front gate bias conditions: from inversion to accumulation. Parameters: $V_{JG} = 0$ V, $V_{G2} = 30$ V.



(a) Effect of FI is dominating.

(b) Effect of FI is decreasing, BI is emerging; capacitance is decreasing.

(c) Effect of FI mitigates, BI is decreasing; capacitance is very low.

(d) Effect of FI is emerging, BI is decreasing; capacitance is very low.

(e) Effect of FI is emerging, BI is mitigatiog; capacitance is increasing.

(f) Effect of FI is dominating, BI is mitigates; capacitance is increasing.

Figure 4.7: Change in charge density profile inside the channel cross section for different back gate bias conditions: from inversion to accumulation. Parameters: $V_{JG} = 0$ V, $V_{G2} = 30$ V.

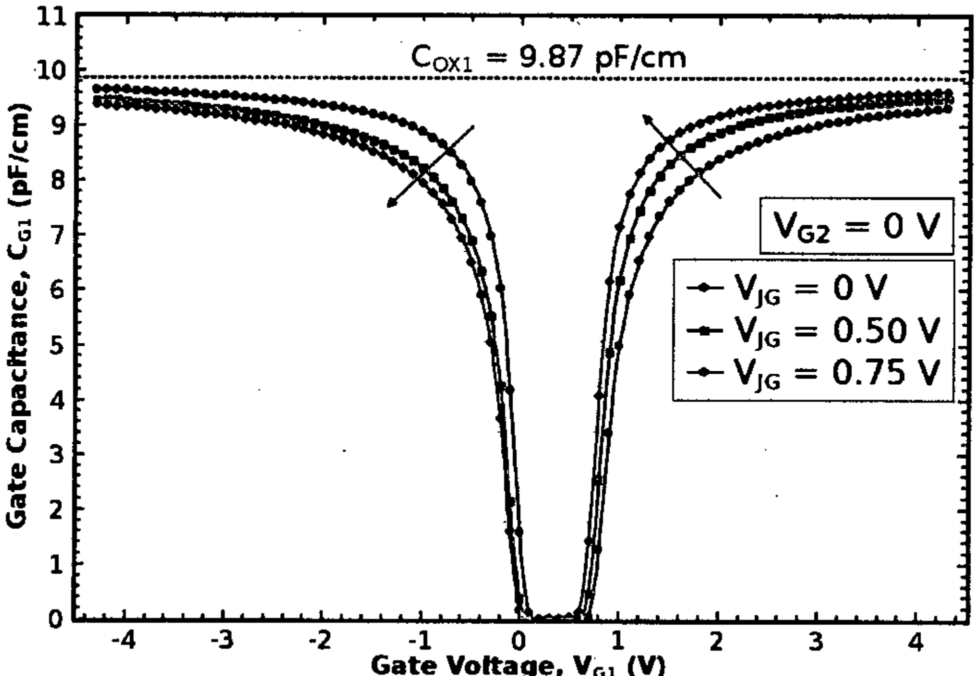


Figure 4.8: $C-V$ characteristics of front gate for various junction gate biases: $V_{JG} = 0, 0.50$ and 0.75 V with back gate voltage, $V_{G2} = 0$ V.

the back interface. Additional simulations show that in this case, the back gate inversion layer is so strong that it cannot be mitigated by applying front gate bias. Thus capacitance does not become zero.

4.3 Effects of Junction Gate Bias

4.3.1 Observations

The effects of junction gate bias has been investigated by calculating $C-V$ for junction gate voltages $V_{JG} = 0$, 0.50 and 0.75 V while keeping back gate voltage, $V_{G2} = 0$ V.

The results for $V_{JG} = 0$ V for various V_{G2} are shown in Figure 4.8. In depletion, no noticeable effect of junction gate bias is observed. It is observed that in inversion, the capacitance increases with junction gate bias voltage, V_{JG}. At any particular front gate voltage, the capacitance is minimum for $V_{JG} = 0$ V and maximum for $V_{JG} = 0.75$ V. In other words, for $V_{JG} = 0.75$ the rate at which the front gate approaches to strong inversion is fastest and for $V_{JG} = 0$, the rate is slowest. It is also observed that the difference between the capacitances for different junction gate biases decreases as the front gate goes deeper into the inversion.

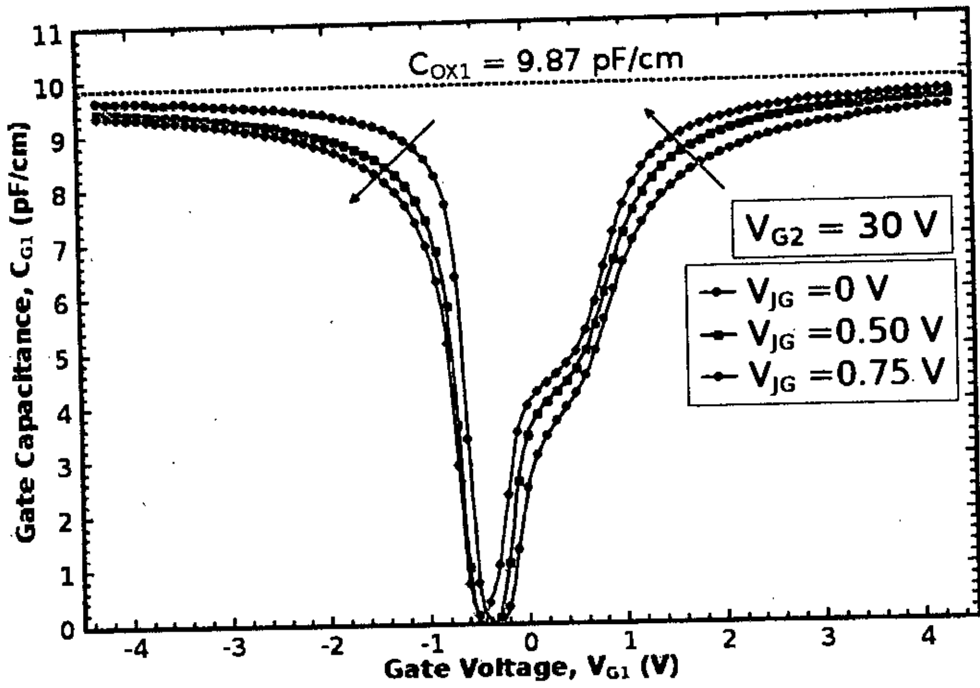


Figure 4.9: $C-V$ characteristics of front gate for various junction gate biases: $V_{JG} = 0$, 0.50 and 0.75 V with back gate voltage, $V_{G2} = 30$ V.

In accumulation, however, the capacitance decreases with increasing junction gate bias voltage, V_{JG}. At any particular front gate voltage, the capacitance is minimum for $V_{JG} = 0.75$ V and greatest for $V_{JG} = 0$ V. In other words, for $V_{JG} = 0.0$ the rate at which the front gate approaches to strong accumulation is the fastest and for $V_{JG} = 0.75$, the rate is the slowest. It is also observed that the difference between the capacitances for different junction gate biases decreases as the front gate goes deeper into the accumulation.

Similar effects are observed for back gate accumulation and inversion, $V_{G2} = -30$ V, $V_{G2} = 30$ V and $V_{G2} = 60$ V except that in depletion of front gate there exist a noticeable effect. At $V_{G2} = 60$ V, the capacitance increases with the increasing junction gate voltage. And for $V_{G2} = -30$ V, $V_{G2} = 30$ V and $V_{G2} = 60$ V, the depletion region gets narrower and the onset of accumulation shifts to the left.

Therefore, we conclude that impacts of junction gate bias are:

- Inversion is easily achieved if junction gate bias is *higher*.
- Accumulation is easily achieved if junction gate bias is *lower*.
- Thus, a *higher* junction gate voltage *assists* inversion, while *retards* accumulation.

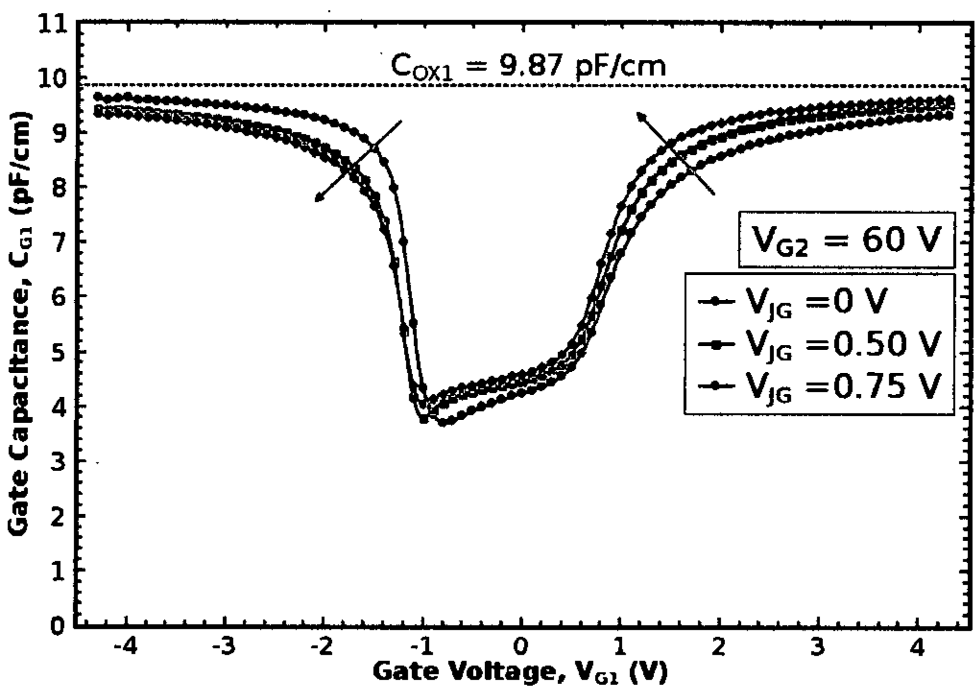


Figure 4.10: $C-V$ characteristics of front gate for various junction gate biases: $V_{JG} =$ 0, 0.50 and 0.75 V with back gate voltage, $V_{G2} = 60$ V.

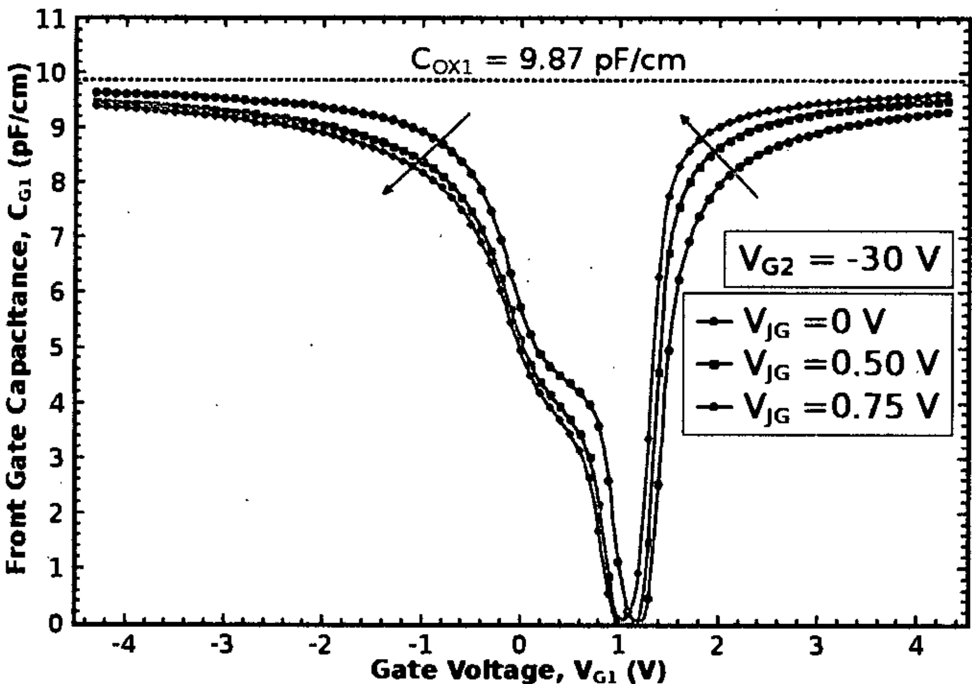


Figure 4.11: $C-V$ characteristics of front gate for various junction gate biases: $V_{JG} =$ 0, 0.50 and 0.75 V with back gate voltage, $V_{G2} = -30$ V.

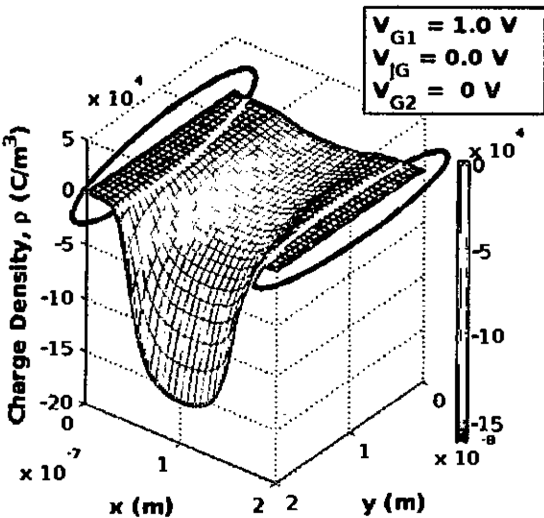
4.3.2 Physical Explanation

The impacts of junction gate biases on $C-V$ characteristics can be explained with the help of surface potential profiles along the lateral distance [Figure 4.14 and 4.15], charge density profile [Figure 4.12] and change in charge density profile [Figure 4.13] inside the Si body cross section.

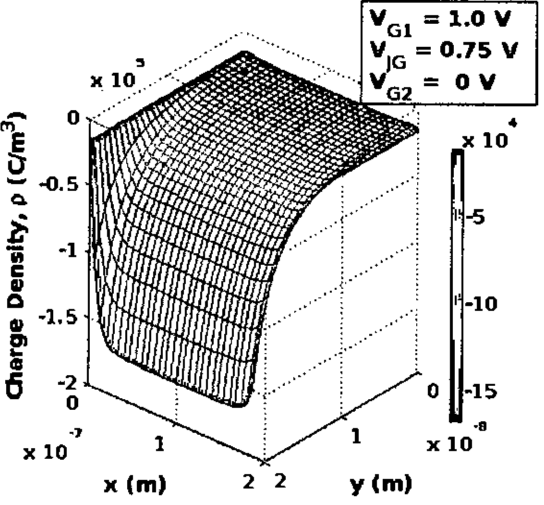
When a positive voltage is applied to the front gate, it first tries to deplete the region near the front interface. A higher front gate voltage tries to invert the interface. In the vicinity of junction gates, the coupling of junction gate bias is greater than that of front or back gate. If the junction gates are tied to zero potential, charge neutrals regions exist along the junctions as indicated in Figure 4.12(a). A change in front gate voltage can not make much change the charge density in this region due to applied junction gate bias and for greater coupling with junction gates [Figure 4.13(a)]. However, if the junction gates are tied to a positive potential, the junctions become reversed biased, and depletion occurs in the vicinity of the junction gates. Therefore, it becomes easier for front gate bias to achieve inversion [Figure 4.12(b)]. In this case a change in front gate bias is responded by the whole front surface (from one junction gate to another) as shown in Figure 4.13(b). Which means that the capacitance is greater for higher junction gate bias. Thus, a positive junction gate bias assists inversion.

This phenomenon is further confirmed by the surface potential profiles along the lateral distance as shown in Figure 4.14. The arrows indicate the regions in which stronger level of surface potential and, therefore, stronger level of inversion prevails. It is evident from the plots that stronger inversion prevails inside a larger region for $V_{JG} = 0.75$ V than that for $V_{JG} = 0$. This happens because, for $V_{JG} = 0.75$ V regions near the junctions are already depleted but for $V_{JG} = 0$ V regions near the junctions are held charge neutral by the junction gate bias due to strong coupling. Thus, for same level of front gate bias, a deeper level of inversion is achieved for higher junction gate bias. As the front interface becomes strongly inverted, the difference between surface potentials for various junction gate biases decreases and so diffrence in capacitance also decreases.

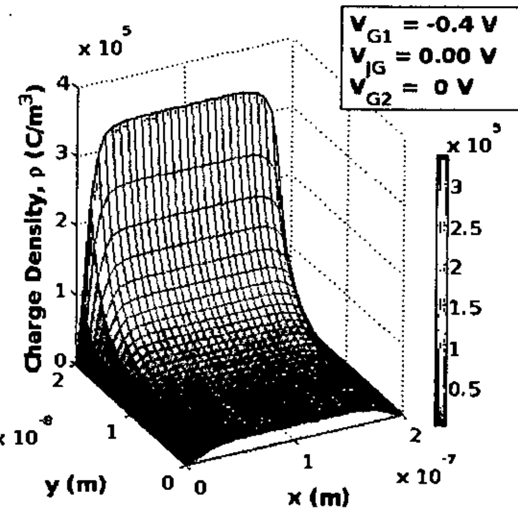
When a negative voltage is applied to the front gate, it first tries accumulate charge in the region near the front interface. A higher front gate voltage tries to accumulate more charge in the interface. In the vicinity of junction gates, the coupling of junction gate bias is greater than that of front or back gate. If the junction gates are tied to a positive potential,



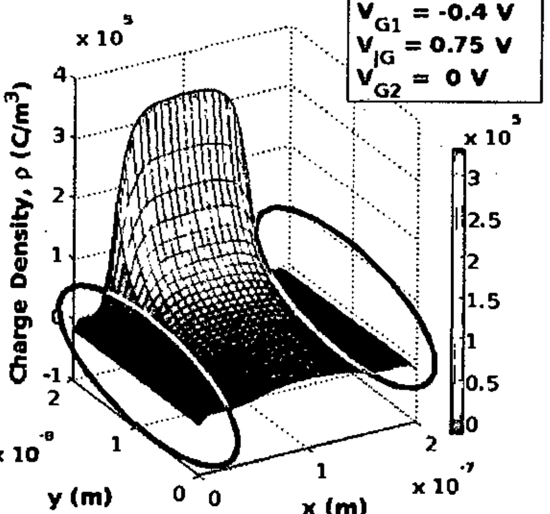
(a) Front interface inversion, $V_{G1} = 1.0$ V; junction gate voltage, $V_{JG} = 0$ V. The marked regions along the junction gates remains charge neutral.



(b) Front interface inversion, $V_{G1} = 1.0$ V; junction gate voltage, $V_{JG} = 0.75$ V.

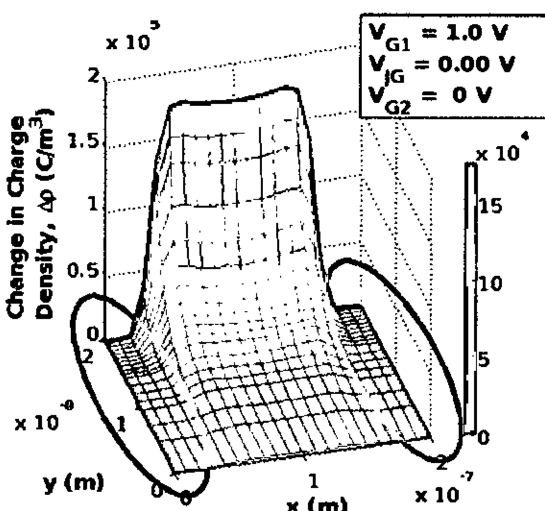


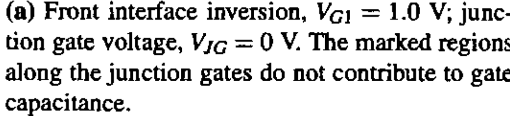
(c) Front interface accumulation, $V_{G1} = -0.4$ V; junction gate voltage, $V_{JG} = 0$ V.

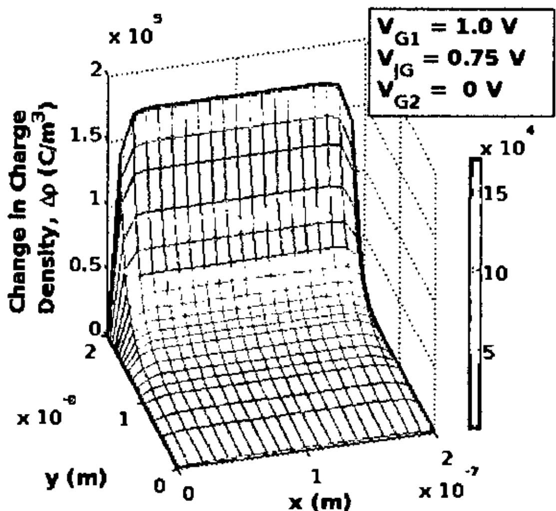


(d) Front interface accumulation, $V_{G1} = -0.4$ V; junction gate voltage, $V_{JG} = 0.75$ V. The marked regions along the junction gates remains charge neutral or depleted.

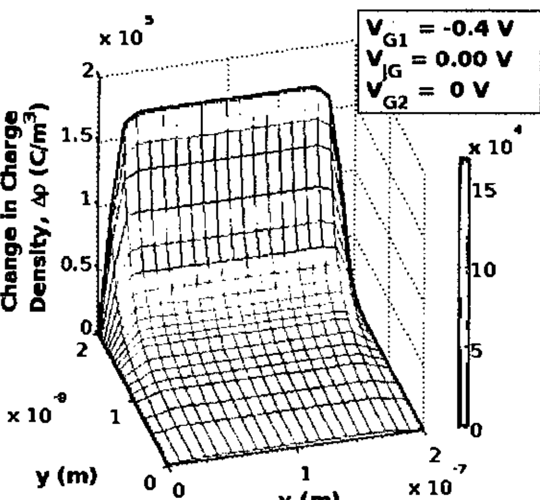
Figure 4.12: Charge density profile inside the channel cross section for different junction gate bias conditions.



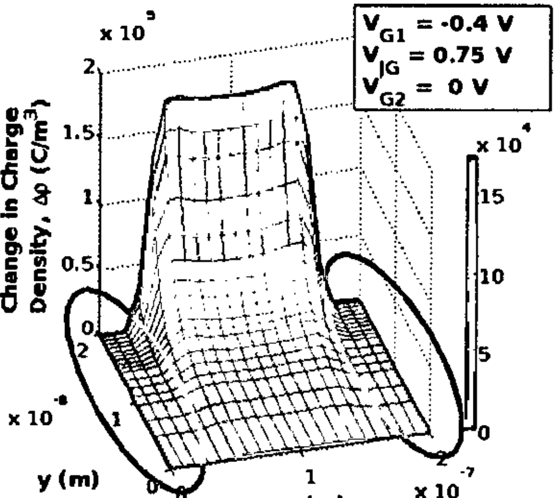

(a) Front interface inversion, $V_{G1} = 1.0$ V; junction gate voltage, $V_{JG} = 0$ V. The marked regions along the junction gates do not contribute to gate capacitance.



(b) Front interface inversion, $V_{G1} = 1.0$ V; junction gate voltage, $V_{JG} = 0.75$ V. The whole region contributes to gate capacitance.



(c) Front interface accumulation, $V_{G1} = -0.4$ V; junction gate voltage, $V_{JG} = 0$ V. The whole region contributes to gate capacitance.



(d) Front interface accumulation, $V_{G1} = -0.4$ V; junction gate voltage, $V_{JG} = 0.75$ V. The marked regions along the junction gates do not contribute to gate capacitance.

Figure 4.13: Change in charge density profile inside the channel cross section for different junction gate bias conditions.

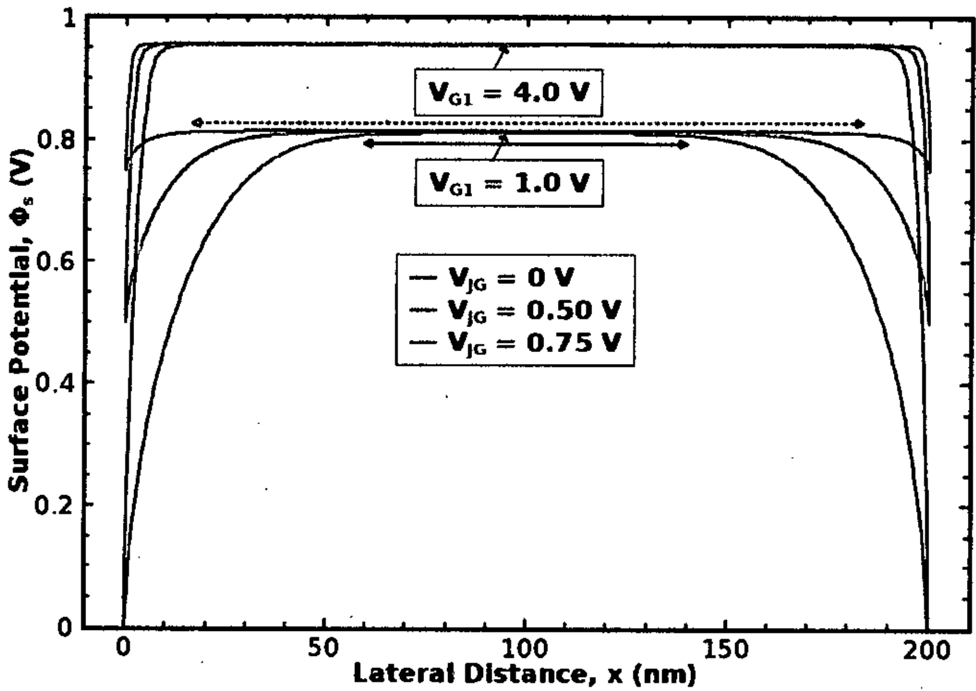


Figure 4.14: Surface potential profile along lateral distance for different junction gate voltages: $V_{JG} = 0$, 0.50 and 0.75 V at strong and weak inversion.

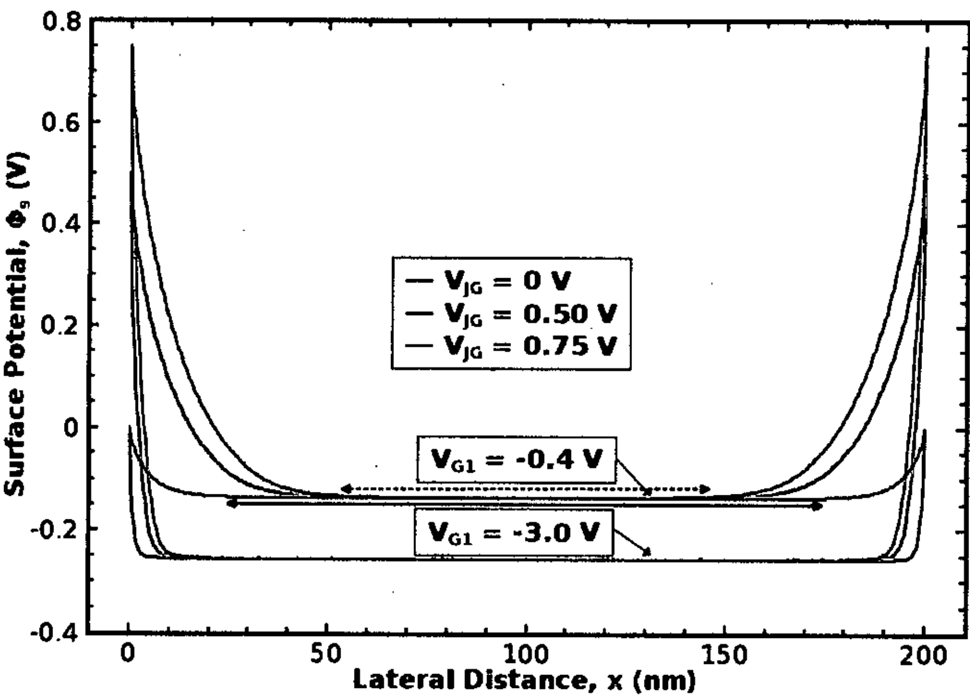


Figure 4.15: Surface potential profile along lateral distance for different junction gate voltages: $V_{JG} = 0$, 0.50 and 0.75 V at strong and weak accumulation.

the junctions become reversed biased and depletion regions exist along the junctions as indicated in Figure 4.12(d). A change in front gate voltage can not make much change the charge density in this region due to applied junction gate bias and for greater coupling with junction gates [Figure 4.13(d)]. Because, the front gate has to convert the depleted regions to charge neutral regions first, and then it can accumulate charge. However, if the junction gates are tied to zero potential, no depletion regions can be found in the vicinity of the junction gates. Therefore, it becomes easier for front gate bias to achieve accumulation [Figure 4.12(c)]. In this case a change in front gate bias is responded by the whole front surface (from one junction gate to another) as shown in Figure 4.13(c). Which means that the capacitance is smaller for higher junction gate bias. Thus, a positive junction gate bias retards accumulation.

This phenomenon is further confirmed by the surface potential profiles along the lateral distance as shown in Figure 4.15. The arrows indicate the regions in which stronger level of negative surface potential and, therefore, stronger level of accumulation prevails. It is evident from the plots that stronger inversion prevails inside a larger region for $V_{JG} =$ 0 V than that for $V_{JG} = 0.75$. This happens because, for $V_{JG} = 0$ V regions near the junctions are already charge neutral but for $V_{JG} = 0.75$ V regions near the junctions are held depleted by the junction gate bias due to strong coupling. Thus, for same level of front gate bias, a deeper level of inversion is achieved for smaller junction gate bias. As the front interface becomes strongly accumulated, the difference between surface potentials for various junction gate biases decreases and so difference in capacitance also decreases.

Chapter 5

Conclusion

5.1 Summary

A simple method of semi-classical calculation of front gate capacitance of fully depleted Four Gate Transistor (G^4–FET) has been proposed and a 2-D simulator based on this model has been implemented. Systematic simulations has been performed for studying the impact of the front gate and the junction gate biases on $C-V$ characteristics. As the G^4–FET is a novel and recent device, to best of our knowledge, this is the first attempt of such kind of study.

It has been found that the back gate bias does not have any noticeable effect on strong inversion and strong accumulation capacitance. However, it has significant effects on $C-V$ characteristics in weak inversion, weak accumulation and depletion of front gate. Since the device is fully depleted, it is expected that the depletion capacitance would be zero. Interestingly, it is found that strong enough inversion in the back gate can not be mitigated by the front gate bias and hence the front gate capacitance can not be made zero unlike what is expected from a FD device.

The effects of junction gate (reverse) bias on the $C-V$ characteristics have been found to be quite interesting. The effects are opposite for accumulation and inversion of the front gate. In the inversion region of the front gate, the capacitance for any particular value of V_{G1} is greater for greater junction gate bias. This means that if junction gate bias is present, inversion is achieved quickly. On the other hand, in the accumulation region of the front gate bias, the capacitance is lower for greater junction gate bias which implies that if junction gate bias is applied, accumulation is achieved slowly.

Thus it is concluded that back gate and junction gate biases have significant influence on front gate $C-V$ characteristics of G^4–FET.

5.2 Suggestions for Future Work

In this work, semi-classical treatment of the charge carriers has been applied for calculating the $C-V$ characteristics of G^4–FET. As the dimensions of G^4–FET is small, the quantum mechanical effects are expected to be significant. Hence, a self-consistent Schrödinger-Poisson solver is the next step of $C-V$ modeling.

This work was focused on front gate capacitance only. There is a scope for performing similar study for the other gates also.

The thickness, width and doping density of the Si body of G^4–FET should have significant effects on $C-V$ characteristics which has not been studied in this work.

Compact models are computationally efficient and are effective in VLSI circuit simulations. A compact model for gate capacitance is yet to be developed.

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