DEVELOPMENT OF A NEW CURRENT CONTROLLED PULSE WIDTH MODULATOR FOR VOLTAGE SOURCE INVERTERS

A Thesis Submitted to the Department of Electrical and Electronic Engineering in Partial Fulfillment of the Requirement for the Degree of DOCTOR OF PHILOSOPHY

By

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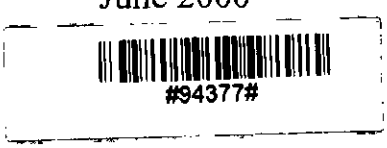

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Abstract

This thesis is concerned with the improvement of current controllers for use with voltage source inverters. Analysis of hysteresis current controller (HCC) is presented. The common problems of non-uniform and burst switching of scalar type controllers (hysteresis current controller and ramp comparison controller (RCC)) are addressed. An improved model of HCC, referred to as PRC is proposed for uniform switching frequency operation. Theoretical basis is established where, an add-on function of programmed amplitude and slope can keep the switching frequency of HCC to a predefined value. In addition to uniform switching frequency operation, the proposed model has significant improvement on the total harmonic distortion coefficient. Analysis of the predictive controller is also made in this research. The shoot through current behavior of predictive controller is improved by the use of a voltage vector limiter. A generalized approach is proposed for the design of the proposed predictive controller with inductive load. Separate schemes are proposed for implementation of PRC and predictive controllers based on general purpose PC architecture. Incorporating the merits of both PRC and predictive controller, a new and novel current controller (referred to as NEW-CC) is developed in this work. This controller operates on regular sampled basis and predicts pulse widths of individual phases once on each carrier period. The load parameters are tracked on each fundamental as well as carrier cycles. Uniform switching as well as shoot through current limiting is achieved in this new controller. The performance of this new controller is compared with the other current controllers and is found to give better performance. The new current controller has lower total harmonic distortion than other current controllers. This controller do not have sub-harmonics in the load current spectrum as is normally encountered in scalar type current controllers at large bands. The new current controller has been experimentally tested. Its performance is in good agreement with the theoretical results.

Contents

List of Abbreviations

ADC	Analog to digital converter
AMPRC	Amplitude modulated programmable ramp controller
ASIC	Application specific integrated circuits
BJT	Bipolar junction transistor
CSI	Current source inverter
DAS	Data acquisition system
DSP	Digital signal processor
GTO	Gate turn off thyristor
HCC	Hysteresis current controller
IGBT	Insulated gate bipolar transistor
IGCT	Insulated gate controlled transistor
KW	Kilo-watt
LSI	Large scale integration
MCT	MOS controlled thyristor
MOSFET	Metal oxide semiconductor field effect transistor
MSF	Maximum switching frequency
NEW-CC	New current controller
RCC	Ramp comparison controller
RMS	Root mean square
RSPWM	Regular sampled PWM
PC	Personal computer
PI	Proportional integral
PLL	Phase locked loop

PRC	Programmable ramp controller
PWM	Pulse width modulation
SIT	Static induction transistor
SITH	Static induction thyristor
SCR	Silicon controlled rectifier
SPWM	Sine pulse width modulation
SHEPWM	Specific harmonic elimination PWM
SPDT	Single pole double throw
THD	Total harmonic distortion
TI	Texas instruments
VCO	Voltage controlled oscillator
VLSI	Very large scale integration
VSI	Voltage source inverter

List of Principal Symbols

α	Modulation angle
β	HCC band
$Counter_a(n)$	A counter related to Phase A at the n^{th} PWM pulse
$Counter_b(n)$	A counter related to Phase B at the n^{th} PWM pulse
$Counter_c(n)$	A counter related to Phase C at the n^{th} PWM pulse
$D_1 - D_6$	Free-wheeling diodes of inverter
ΔI_t	Amplitude of triangular carrier signal
$Data_a(n,r)$	Real time data signal for Phase A
$Data_b(n,r)$	Real time data signal for Phase B
$Data_a(n,r)$	Real time data signal for Phase C
$Data(n,r)$	Combined real time signal data
f	Reference frequency
f_0	Fundamental frequency
f_s	Switching frequency
f_{sn}	MSF at normalized THD
G	A constant
i^*	Reference current
$i^*(n)$	n^{th} sample of combined reference current vector
$i_a^*(n)$	n^{th} sample of Phase A reference current
$i_b^*(n)$	n^{th} sample of Phase B reference current
$i_c^*(n)$	n^{th} sample of Phase C reference current
$i(n)$	n^{th} sample of combined load current vector
I_m	Reference current maximum value

I_{rms}	RMS value of load current
I_{a1}, I_1	Maximum value of fundamental load current
i_a	Phase A load current
$i_a(n)$	n^{th} sample of Phase A load current
i_b	Phase B load current
$i_b(n)$	n^{th} sample of Phase B load current
i_c	Phase C load current
$i_c(n)$	n^{th} sample of Phase C load current
i_a^+	Rising current segment (load current)
i_a^-	Falling current segment (load current)
$\Im$	Imaginary part
$K(n)$	Duty cycle at the n^{th} switching period
$K_a(n)$	Duty cycle for Phase A
$K_b(n)$	Duty cycle for Phase B
$K_c(n)$	Duty cycle for Phase C
L	Inductance per phase of the star connected load
L_{new}	Current value of load inductance
L_{old}	Previous value of load resistance
m	Slope of load current
m_t	Slope of triangular carrier signal
m_t^+	Positive slope of triangular carrier signal
m_t^-	Negative slope of triangular carrier signal
n	Sample number
N_{max}	Total number of PWM pulses in a fundamental period
ω	Angular frequency of reference signal
p	Sector number
$Q_1 - Q_6$	Inverter switches (transistors)
R	Resistance per phase of the star connected load
R_{new}	Current value of load resistance
R_{old}	Previous value of load resistance

$\Re$	Real part
r_{max}	Real time data samples in a carrier period
$S_A - S_C$	SPDT switches of phases A, B and C
T, T_s	Switching period
t_1, T_1	ON time duration in a switching period
t_2, T_2	OFF time duration in a switching period
t_x	Time related to V_x
t_y	Time related to V_y
t_z	Free-wheeling time in a period (T_s)
t_{c1}	Rise time of triangular carrier signal in T_t
t_{c2}	Fall time of triangular carrier signal in T_t
T_t	Period of triangular carrier signal
T_{lock}	Lockout time
τ	Time duration by which a data is latched to the parallel port
θ	Load power factor angle
θ_1	Phase angle of Phase voltage (fundamental)
θ_2	Phase angle of load current (fundamental)
V_s, V_a	Inverter dc supply voltage
$V(n)$	n^{th} sample of combined voltage vector
$V_1 - V_6$	Inverter voltage vectors
V_x	Contribution of $V(n)$ on the adjacent right arm vector
V_y	Contribution of $V(n)$ on the adjacent left arm vector
V_{an}, V_{bn}, V_{cn}	Inverter output voltage for Phases A, B, C (line to neutral)
Z	Load impedance
Z_{new}	Current value of load impedance
Z_{old}	Previous value of load impedance

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Chapter 1

Introduction

1.1 General

The availability of power semiconductor switches in the late 1970's resulted in a major change in control and conversion of electrical power by electronics. Among the different static power converters, the dc-to-ac converter, called inverter has widespread application in various forms of power supplies, active power filters, high frequency heating and ac motor drives. Prior to the introduction of static power inverters, ac motors were considered as constant speed drives depending mainly on the frequency of the supply. In variable speed applications, dc motors were the only choice.

Variable frequency inverters have widened the application of ac motors in the industrial sector. The cage type three-phase induction motor is considered as the work-horse in the industry because of its robustness, reliability, efficiency and low cost. Before the mid 1980's analog and LSI (large scale integration) digital integrated circuits were used for control signal generation of inverters. A large number of integrated circuits were required for control purposes. The VLSI (very large scale integration) technology flourished in the late 1980's. The VLSI technology helped the design of powerful programmable devices such as microprocessors, digital signal processors and application-specific-integrated-circuits (ASIC). Inverter and motor drive controls using microprocessors have become the interest of engineers and researchers because of the advanced programmable features, flexibility in the implementation and the increasing trend of generalization.

The models of the inverter and ac motors are inherently non-linear. These models are associated with many interdependent parameters. An efficient scheme should have the capability of considering all the parameters to provide good system performance. The present trend of fast computing microprocessors is making the task of on-line implementation of the inverter operation and motor control an affordable one. Computation intensive schemes are getting widely used for real time implementation. New computation techniques are rapidly evolving to improve the steady state and dynamic performances of the inverter and drive systems.

The availability of high speed and high power semiconductor devices such as BJT, MOSFET, IGBT, SITH, MCT, IGCT etc. allow higher switching frequencies with low losses. As a result, the application area of inverters has increased. On line control of voltage, frequency and current of an inverter during dynamic loading involves extensive computations, and requires complex schemes of implementation by a microprocessor and a digital signal processor. Researchers are trying to simplify complicated schemes with advanced/easy control algorithms. Continuous efforts are being made and newer schemes are evolving with better results but with new limitations. Because of the diversity of inverters and drive controls, various non-linear parallel control strategies such as neural network and fuzzy controller are also being advocated for new state and parameter estimation. There are different types of inverters for different applications. Control methods are also different for different inverter types.

1.2 Inverter Types and Controls

The function of an inverter is to change a dc-input voltage to a symmetrical ac output voltage. The output voltage could be at a fixed or variable frequency. A variable output voltage can be obtained by varying the input dc voltage. On the other hand, if the dc input voltage is fixed and is not controllable, a variable output voltage can be obtained by varying the duty cycle of the inverter, which is normally accomplished by pulse-width-modulation (PWM) control of the inverter.

The output voltage waveforms of ideal inverters should be sinusoidal. However, the

waveforms of practical inverters are non-sinusoidal and contain harmonics. For low and medium-power applications, square-wave or quasi-square-wave voltages may be acceptable, but for high-power applications, sinusoidal waveforms with distortions as low as possible, are required. With the availability of high-speed power semiconductor devices, the harmonic contents of output voltage can be reduced significantly by switching techniques.

Inverters can broadly be classified into two types: single-phase inverters and three-phase inverters. In each type, controlled turn-on and turn-off devices (e.g., BJTs, MOSFETs, IGBTs, MCTs, SITs, GTOs) or forced-commutated thyristors can be used depending on applications. These inverters generally use PWM control signals for producing an ac output voltage. An inverter is called a voltage source inverter (VSI) if the input voltage remains constant or an inverter is called a current source inverter (CSI) if the input current is maintained constant. The structure of a CSI is costlier compared to VSI. Applications of CSI are limited to low-switching frequencies because of its current commutation requirement. On the other hand, VSI has large range of the switching frequency and modern high speed switching devices can be used in such inverters. For this reason, VSIs are preferred for most applications including ac motor drives. During the last three decades, different schemes of inverter control in voltage reference PWM and current reference PWM have been proposed for VSIs.

1.3 Pulse Width Modulation (PWM) Techniques

The output voltages of a modern power inverter are controlled by pulse width modulation (PWM) techniques. Many modulation techniques are available in the literature for the control of VSIs. A VSI can be operated in the output voltage or output current control modes. In either control modes, the schemes support reduction of low frequency harmonic contents by voltage or current reference PWM techniques. In a VSI inverter, the voltage reference PWM techniques basically control the inverter output voltage using standard schemes and do not have direct control over the load current. Their harmonic behaviours are well defined. On the other hand, a current-reference-modulation technique controls

the operation of the VSI by means of feedback from the load current and other system parameters. Current-reference-modulation techniques have control over the load current, but their implementation is complex compared to voltage reference schemes because of the feedback requirement.

1.3.1 Voltage Reference PWM

The earliest modulation techniques applied to inverter operation are the single pulse and the multiple pulse modulations [1, 2]. These techniques are capable of providing inverter output voltages with low total harmonic contents. However, the output voltages contain low order harmonics that are harmful for drive applications. To overcome the effect of low order harmonics these techniques were replaced by the sinusoidal pulse width modulation (SPWM) [3].

In SPWM technique, the switching points of the PWM pattern (modulated wave) are obtained by comparing a sine wave with a high frequency triangular wave (carrier). Based on the carrier generation, there are different types of carrier waves [4-9]. The basic analog SPWM with asynchronous carrier generates sub-harmonics. Complex schemes are required to remove the sub-harmonics. Moreover, analog schemes are not suitable for inverter operation in wide range of frequency because of component drift and offset problem. The microprocessor implementation of the basic naturally sampled SPWM is difficult because of the involvement of transcendental equations in the computation of the switching points. However, schemes are available in the literature for implementation of naturally sampled SPWM with a microcomputer using advance computational algorithm [10]. Researchers have simplified the basic SPWM for use with a microprocessor.

The simplified numerical form of SPWM is popularly known as Regular Sampled PWM (RSPWM) [11]. The Regular Sampled PWM generates a stream of regularly spaced pulses whose widths are modulated by the amplitude of the sinusoidal modulating wave (fundamental voltage). The spectral distribution of RSPWM depends on the carrier frequency. The harmonic spectrum of the output waveform primarily contains the fundamental modulating frequency, the carrier, multiples of carrier and side bands. The harmonic contents are negligible at intermediate frequencies by the nature of the modulation process. By

choosing a relatively high carrier frequency a small filter is sufficient to filter out all the harmonic contents to acceptable range. Different schemes and implementation strategies are reported in the literature for RSPWM [12-29].

The Harmonic Minimized Sampled PWM (HMSPWM) is similar to RSPWM but, here, third harmonic is added intentionally to some extent to the sine-modulating wave. Third harmonics and its multiples cancels out in a star connected load with insulated neutral. For the same modulation index, HMSPWM gives higher voltage than RSPWM. It is observed that for HMSPWM, the output voltage maintains a linear relationship with the modulation index upto 120% [30], whereas, for RSPWM the linear relation holds upto 100%. The linear over-modulation feature of HMSPWM makes it suitable for certain applications (for example, in the constant power operating region of drives) requiring high voltages [30, 31].

The Specific Harmonic Elimination PWM (SHEPWM) generates a regularly sampled pulse stream and the switching edges are obtained analytically by eliminating certain specific harmonic contents [32-36]. This technique is particularly suitable for very high power drives where thyristors or GTO switches are the only choice (because of very high power handling requirement). The switching frequency is maintained as low as possible. The low order harmonic contents such as 5th, 7th, 11th, 13th, 17th, 19th harmonics are generally eliminated. The SHEPWM technique is computation intensive. These are generally calculated off-line and implemented with a microprocessor using ROM based look-up tables.

In Regular Sampled Harmonic Elimination PWM, the leading edge of a PWM pattern is calculated from the reference modulating signal and the trailing edge is determined from the shifted reference signal. The PWM pattern obtained in this technique is close to that obtained by SHEPWM [37]. The switching edges can be calculated on-line and the implementation scheme is similar to that of RSPWM.

The Delta Modulation (DM) technique is a simple scheme for generating switching waveforms of inverters [38]. The DM scheme is capable of on-line harmonic minimization. Tuning the feedback filter can control its performance. Several types of delta modulation have been investigated so far for various power converter operations including inverters

[39-41]. The DM schemes have the disadvantages of non-uniform switching and suffer from sub-harmonic problems in case of wide bands.

Besides the above mentioned standard modulation techniques, there are some space vector PWM techniques commonly known as field oriented flux vector controllers [42-45]. The field oriented flux vector controllers are associated with ac motor drives and calculates the voltage vector from motor parameters, flux magnitude and position of the motor's shaft. The inverter switching states are selected from lookup tables with the information of the magnitude and position of the voltage vector. The PWM pattern for the inverter switches are close to regular sampled PWM. However, flux vector control techniques support linear over-modulation and hence are suitable for high-speed operation of motors (in constant power region). The vector controllers are computation intensive. The vector controllers are generally implemented with a Digital Signal Processor (DSP) and hence the overall cost of the controller is much greater than all other voltage reference controllers. However, now a days low cost DSPs are emerging.

1.3.2 Need for Current Control

The VSI is composed of power semiconductor devices. Semiconductor switches do not have over current capability except the thyristor family. Thyristors such as silicon controlled rectifier (SCR) and gate turnoff thyristors (GTO) can withstand high surge current for few milliseconds but they are slow devices and hence are not suitable for modern drives requiring high switching frequencies. The current flow to the load in a VSI depends on the load characteristics as well as on the input supply voltage. If the load impedance is constant during the entire operating period of the inverter, the current flow through the inverter will be constant. On the other hand, if the load impedance varies over a wide range during the operation of the inverter there is the risk of over-current. For example, ac motors are highly non-linear and their equivalent impedance vary over a wide range from start-up to steady state operation. Wide impedance variation also occurs during load change in the steady state operating condition.

In a VSI fed ac motor drive, there exists over-current conditions and thus instantaneous over-current control is necessary so that the current does not exceed the current limit

of the inverter switches. Sinusoidal current waveform is the requirement for smooth motor operation over wide speed range. If the motor phase current contains considerable harmonics, then there will be torque pulsation and noise. Hence, in high performance drive systems the PWM control technique should have a current limiting feature and lower harmonic distortion.

1.4 Current Reference PWM

In the current reference techniques, a current controller forces the load current to follow the current command which is usually a sinusoid. Common strategies of current controllers can be classified as hysteresis controller, ramp comparison controller and predictive controller. In a hysteresis current controller (HCC) a PWM pattern is generated comparing a reference sinusoidal current waveform with the actual load current. Hysteresis comparators are used to impose a dead-band or hysteresis around the reference current. The PWM pattern forces the load current to follow the sinusoidal reference current limiting the current ripple within the hysteresis band. The hysteresis control scheme provides good dynamic performance [46-49], because it acts quickly. However, the main disadvantage of this type of controller is the variation of the switching frequency within the fundamental period. Also, the limit cycle behaviour is present in case of HCC.
The ramp comparison controllers' compares the error current signal to a triangular wave to generate the drive pulses for the inverters [50]. The advantages of the ramp comparison technique is that the inverter switching frequency is usually limited to the frequency of the triangular waveform and produces well defined harmonics. However, the system response is affected by the stability requirement of the feedback loop, which also depends on load parameters. Thus, inherent phase and amplitude errors arise even in the steady state condition. Predictive controllers calculate the required inverter voltage forcing the current to follow the current references. Different types of current controlled PWM are found in the literature. During the last three decades a large number of schemes have been developed by different research groups for controlling ac drives, UPS and active power filtering applications.

All these techniques have their own merits and de-merits. These are discussed in detail in the following sections.

1.5 Literature Review of Current Controllers

Many researchers have focused on the development of different types of current controllers in the categories of hysteresis, ramp comparison and predictive control.

1.5.1 Hysteresis Current Controllers

A. B. Plunkett [47] introduced a current controller for operation with a transistorized three-phase voltage source inverter. It was a fixed band hysteresis current controller (HCC) with three analog-type independent hysteresis comparators. Further investigation was made on the drive system by S. C. Peak et al. [48]. Lajoie-Mazenc et al. [49] studied the performance of hysteresis current controlled inverter on a permanent magnet synchronous machine, where it was found that the current would occasionally exceed the limit set by the hysteresis band, overshooting on the down-slope of the waveform when motoring and on the up-slope when regenerating. D. M. Brod et al. [50] used a graphical switching diagram to explain some of the characteristics of hysteresis controllers. From the switching diagram, it was evident that for neutral unconnected star loads, theoretically the maximum line current could be double the hysteresis band. It was suggested that the control could be improved by means of a more complex system that switched between comparators with and without hysteresis according to the magnitude and the duration of the current error, but at the expense of an increase in switching frequency. Pfaff et al. [51] made a comparative study of HCC with ramp comparison current controller for motor drive applications. It was found that the hysteresis method had a better response to large disturbances compared to the ramp comparison method, but it gave a less smooth torque under small disturbance conditions due to the poor use of the zero voltage vector. The authors attempted to use the zero voltage vectors more effectively by switching between comparators with and without hysteresis and managed to retain control within the hysteresis band with a decrease in the switching frequency.

Brod and Novotny [50] who made a simulation of all three controllers, found that for the hysteresis controller at low speed there was a limit cycle behavior in which there were burst of high frequency switching with occasional use of the zero voltage vector. This effect was explained by means of a switching diagram. They recommended that the ramp-comparison scheme be used for low-speed operation and the hysteresis control be used only for high-speed operation. Over the past two decades a number of schemes have been proposed using HCC for drive applications.

Kazmierkowski et al. [52] presented a novel vector control scheme for induction motor drive based on a current control loop. A three-level hysteresis strategy was adopted to coordinate the switches of three phases in the d-q plane and apply zero voltage vectors for reducing the switching frequency. By transforming into the d-q domain, coordination of the three phase switching can be considered and only two hysteresis controllers are required for three phase applications. In addition, zero voltage vectors can be applied while encountering the zero current error to reduce the switching frequency. It was evident from the simulations as well as experimental results that the three level controller scheme gives less average switching frequency. Liu et al. [53] presented a microprocessor-based controller for a permanent magnet synchronous motor (PMSM) drive, where the motor is fed from a HCC VSI.

A technique was proposed to improve the operation of the hysteresis current controller at low speed by controlling the duration of the free-wheeling period. However, this type of control technique reduces the average torque and degrades the overall performance of the drive. Pillay et al. [54] proposed a DSP-based vector and current control scheme for a PMSM drive. The design is centered on the TI TMS320E17 and TMS320E15 DSPs. The TMS320E17 is used to implement the vector control algorithm while the TMS320E15 is used to implement the current controller. The relatively slow speed of the DSPs affects the performance of the current controllers due to the high bandwidth and high sampling requirement.

Since the command signal and the load terminal voltage may greatly influence the current error under some conditions, if some information of the derivative of the current error is also available, then one would know the changing tendency of the current error. Therefore,

one can take more advantage of the zero voltage vectors to reduce the switching frequency substantially. C. T. Pan et al. [55, 56] proposed an approach of adding the information of the derivative of the current error to the hysteresis current controller. In their scheme they coordinated the switching of the three phases in the d-q phase plane. The inverter voltage vectors were selected from the d-q axis current errors and their derivatives. Simulation and experimental results showed improved performance of the controller.

Survey of the current controllers shows that the performance of hysteresis current controllers in the steady state and dynamic conditions are good, but its switching frequency distribution is non-uniform [57, 63]. In order to overcome these disadvantages, many schemes have been proposed in the literature. Nabae et al. [64] proposed a current deviation vector control scheme. Ogasawara et al. [65] devised a high performance ac servo system with a switching frequency feedback scheme. L Malesani and P. Tenti [66] proposed a novel hysteresis current control method, where constant modulation frequency is achieved by partial phase de-coupling control method. The method needs approximate knowledge of the load parameters.

T. Kato and K. Miyao [67] proposed a modified hysteresis current controller using the double current tolerance band concept. The controller normally uses the lower band as the hysteresis limiter and continuously monitors the switching frequency. If the switching frequency tends to exceed a predefined value, the load current is allowed to reach the outer band. The resulting switching frequency is not constant. However, a less average switching is achievable by this method.

J. D. VanWyk et al. [68] proposed a modification to the hysteresis current controller using inner-feedback concept and applied it to a single-phase reactive power compensator. It was observed that the controller has less load dependency on the switching frequency. Nasser H. Rashidi [69] applied the inner-feedback concept to a three-phase current- controlled inverter. He showed that less load dependent switching is achievable by simple feedback loops within the hysteresis comparators of hysteresis current controllers.

Some techniques are available using adaptive variable band to the hysteresis current controllers to maintain almost uniform switching frequency with computation intensive schemes [70-72]. Theoretically, it is possible to correlate the switching frequency with the

load parameters, current magnitude and the hysteresis band [70]. The switching frequency can be made uniform by using an adaptive time varying hysteresis band. As evident from the simulation results, for insulated neutral system the current waveforms are more distorted and may contain low order harmonics which is harmful for drives. The scheme is computation intensive and needs major refinement for practical implementations.

A Tripathi et al. [73] proposed a sinusoidal band hysteresis current controller and compared its performance with the fixed band controller. It was found that the sinusoidal band controller has low harmonic content than the fixed band. However, the switching frequency of the controller becomes extremely high near the natural zero band of the sinusoidal controller. Hence, it is not realizable in practical application.

Recently, a variable band scheme has been proposed keeping the advantages of sinusoidal band current controller [74]. It is found that a mixed band controller having a variable band resulting from the addition of a fixed band to the sinusoidal band works well [74]. Because of their fast response, hysteresis current controllers find application in instantaneous current correcting applications such as var compensation and active power filtering. Active power filtering needs current injection with minimum delay. The conventional HCC can be applied in such cases. However, with conventional HCC, the semiconductor switches are required to be selected for the worst case maximum switching frequency, which increases the cost of the inverter.

Several hysteresis current controllers have been reported in the literature for active power filtering applications [75-79]. Attempts have been made by researchers for constant switching operation to reduce the cost of the inverter. Constant switching frequency operation is achieved by a variable band strategy, however, the approach is different from that of B. K. Bose [70]. To control the band for a fixed frequency, a phase-locked loop (PLL) is used. This solution [74-77] employs the hysteresis comparator as a nonlinear voltage control oscillator (VCO). When locked to a suitable clock signal, the PLL not only ensures constant modulation frequency, but also minimizes the phase displacement between the output voltage pulses and the clock itself with an accuracy limited only by the control loop gain. The PLL loop includes a proportional-integral block, which integrates the phase displacement and tends to reduce it to zero [77-79]. This feature is particularly

important for three phase insulated neutral systems, where the "center pulse" condition results in optimal reduction of the current ripple [45].

The PLL based current controllers need prediction of the hysteresis band to keep the switching frequency uniform. Most PLL based systems use a complicated scheme for the band prediction that affect their responses. Recently L. Malesani et al. [80] proposed an improved scheme of the PLL controller. A simple and fast prediction method of the hysteresis band is added to a linearized version of the phase-locked loop control ensuring constant switching frequency and tight control of the position of modulation pulses. This allows accuracy in tracking distorted current waveforms and minimizes the ripple in multi-phase systems. The PLL based schemes are prone to instability at large disturbances because of the limited lock in range.

1.5.2 Ramp Comparison Current Controllers

In the early days of current controllers, attempts were made to have a simple fixed switching current control. It was observed that a triangular (ramp) waveform of high frequency added to the feedback path of the HCC can force the PWM switching frequency to remain constant [50] at the triangular wave frequency. A simplified schematic of the conventional RCC is shown in Fig. 1.1. A carrier signal i_t (ramp waveform) is added to the sinusoidal reference current $i* = I_m \sin \omega t$. The error between the composite reference current $(i* + i_t)$ and the load current, is applied to a two level comparator. The output of the comparator is passed through a lockout circuit that produces two pulses adding considerable amount of lockout times between them. The pulses B_U and B_L of the lockout block are applied to the switches S_U and S_L of the inverter.

Investigation shows that the ramp comparison controller needs proper tuning of its ramp signal amplitude, otherwise, there may be extremely high switching because of the multiple crossing of the current error with the ramp. The multiple crossing problem is normally compensated by using a PI (proportional and integral) controller in the feedback path. This approach degrades the controller response. Several researchers tried to improve the response of ramp-comparison controllers. Schauder and Caddy [81] raised the issue of reference frame to be used for current control and compared the stationary and rotor

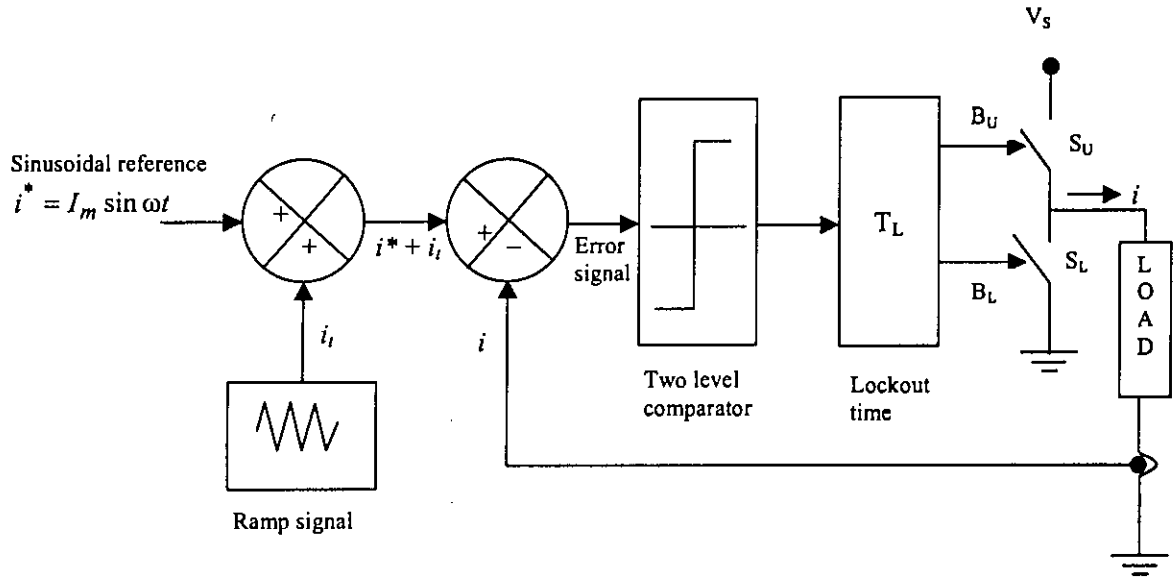

Fig. 1.1: Conventional Ramp Comparison Controller scheme.

reference frames. Nagase et al. [82] used the stationary frame, recognized the loss of bandwidth with increasing frequency, and improved the system by the pragmatic approach of increasing regulator gain with frequency. Brod and Novotny [50] showed that the response could be improved by phase lead compensation. Rowan and Kerkman [83] demonstrated that the synchronous frame controller is more robust in that it is more insensitive to slip frequency and motor impedance. Most papers consider the design of a ramp-comparison scheme in the frequency domain, thus optimizing the response for small disturbances only. Gosbell et al. [84] proposed a clocked current control technique for use with ramp comparison controllers. They investigated the effects of clocking the controller, injecting zero sequence into the current reference and rotating the switching lines. These modifications were found to give significant improvements to current control for both large and small disturbances. The scheme was modeled for induction motors at low speeds only. At high speeds, the scheme was not investigated. Recently M. Azizur

Rahman et al. [85] proposed a ramp comparison controller with three ramps for three phases. The current error signals are compared to three 120^0 phase-shifted triangular waveforms. This modification eliminates the zero voltage applied to the inverter and reduces the amplitude and phase errors.

1.5.3 Predictive Current Controllers

The increase in the power of microprocessors and the introduction of very fast digital signal processors has encouraged the development of current control methods that attempt to solve the machine equations in real time. These methods are generally known as predictive methods. One of the first suggestions was from Pfaff et al. [86]. In his scheme, unlike three independent controllers of hysteresis control scheme, a single controller is used for the motor current vector. The currents are sampled at a constant rate. The current vectors are first calculated and then compared to the reference current vector. An appropriate voltage vector that would reduce the current error vector to zero is calculated and produced. Alternate methods are available for prediction of the voltage vector. Pfaff et al. [86] proposed a two-stage calculation method for the prediction purpose. J. Holtz and Stadfeld [87] discarded the use of the zero voltage vectors in case of large current error. Some application specific schemes are available in the literature [88-95] using sophisticated processors.

LeHuy and Dessaint [96] presented an elaborate analysis of the predictive controller and compared its performance with the hysteresis control scheme. The simulation results show that the predictive control schemes provide constant switching frequency and less current ripple compared to HCC. The performance at low-level current is better than that obtained with hysteresis control scheme with comparable switching frequency. However, its implementation is complex compared to hysteresis control schemes. The predictive control scheme provides good result if the motor parameters are known with sufficient accuracy. The current ripple cannot be explicitly specified, but the inverter switching frequency is well defined. The controller does not provide an inherent instantaneous current limit.

It was observed [96] that at high-level currents and high speeds, the response of predic-

tive controllers is slow due to the reduction of the available voltage that can force the current to flow in the motor. In order to develop an efficient scheme, Dessiant et.al. [96] suggested an adaptive current control scheme that has two operation modes, predictive mode and hysteresis mode. The mode selection is based on the magnitude of the current error vector $|i|$. The predictive control mode is selected when $|i|$ is less than the mode switching level. When $|i|$ goes beyond this limit, the controller is switched to the hysteresis mode in order to reduce the current error vector as fast as possible. In this manner, the adaptive current controller operates in predictive mode in the steady state and small current transient conditions. During dynamic and large current transient conditions such as starting and load variations the adaptive controller operates in the hysteresis mode. J. Holtz and S. Stadtfeld [45, 97] proposed a predictive controller having a lower switching frequency. The proper inverter voltage vector is determined from the knowledge of the load and operating conditions. When the current error vector magnitude exceeds a specified value, the controller predicts the current trajectory for each possible inverter state and determines the length of time that the current error vector will remain within the specified value. Selecting the state of the inverter from the trajectory of the error current vector minimizes the inverter switching frequency. The controller response is slower than that of the hysteresis controllers due to the computational requirement.

1.6 Problem Identification

It is evident from the literature review that the different current controllers have individual advantages and disadvantages. The basic hysteresis current controller gives fast response, can limit the load current even in transient states but has the drawback of non-uniform switching. The Ramp Comparison Controller (RCC), a modified model of HCC, provides constant switching at steady state, can limit the load current in transient states, but has burst switching effect in transient conditions. Moreover there are possibilities of unstable operation (because of the presence of sub-harmonics) at variable loads. The predictive controller gives constant switching, works very fast at transient conditions but has no control on the load current at transient conditions. In case of dynamic conditions, the

shoot through current is excessive and occasionally exceeds the recommended limit. The implementation of RCC is simpler and more economic than predictive controller, however, has the risk of burst switching and sub-harmonic effects because of the free running carrier. Researchers have tried to solve the problems in different applications, but no standard and unique solution came out in the past. There are ample scope of performance enhancement of the current controllers.

1.7 Contribution

The goal of this thesis is to enhance the performance of current controllers and develop general purpose application schemes taking advantage of the modern high speed computing facilities. Particular attention is given to maintain uniform switching frequency keeping the current ripple as low as possible.

The main contribution of this thesis is a new and novel current controller (NEW-CC) having the lowest harmonic distortion among all of the state-of-the-art current controllers. The new current controller always operate at constant switching frequency and have integer number of pulses in a fundamental period. The controller is designed using regular sampling approach and the PWM patterns are calculated on carrier cycle basis. The reference current is a sinusoid and is sampled regularly. The width of a two level pulse is computed such that the load current follows the profile of the sampled reference current. Three phase patterns are computed separately and the PWM patterns (in a carrier period) are aligned in center justification. With this center justification technique , the phase voltage pattern has double number of pulses than the PWM pattern of inverter switches. Thus an advantage of double carrier frequency [45] is ensured in the proposed design. The overall current ripple is less in the proposed design because of the double carrier frequency effect. Theoretical model as well as practical implementation scheme is proposed for the NEW-CC. Simplified mathematical model is formulated for switching points computation for three phases. A fast algorithm is developed for computation of the six state waveform pattern from the three phase switching points. Analytical formulas have been devised for estimation of the current ripple as functions of the inverter sup-

ply voltage, switching frequency and load parameters. This would help in choosing the correct switching frequency for any application. An R-L parameter estimation technique is proposed for use with the NEW-CC. A detail PC based scheme is also proposed for practical implementation of the controller. The controller is designed with equivalent load parameters and hence is suitable for applications with R-L load including all types of ac drives.

The performance of the new controller is studied through simulation and experimentation. Experimental results are found very close to theoretical ones.

1.8 Thesis Outline

The thesis is divided into five chapters. In Chapter 2, a modified version of HCC is described. Detailed analytical procedures are presented showing theoretical basis of making uniform switching frequency by the addition of a programmed carrier waveform in a hysteresis current controller. Simplified mathematical model is extracted for computation of the carrier amplitude and slope for stable operation in all operating conditions. A simple microcomputer implementation scheme is presented. Results are presented showing controller performances in steady state, startup and dynamic operating conditions.

In chapter 3, an improved version of predictive controller is suggested. New feature is added to the conventional predictive current controllers to improve response at startup and dynamic operating conditions. A simplified method is described to compute voltage vectors and other associated modulation parameters from reference currents. Generalized approaches are presented using equivalent R-L parameters for use in any inductive load including ac motor drives. The mathematical model of the improved versions are elaborately described in this chapter including schemes for implementation.

A new and novel current controller is presented in chapter 4, using carrier cycle basis estimation of PWM patterns. Mathematical model for pulse widths estimation are elaborately described. Theoretical analysis is made for the load current ripple computations including maximum and minimum ripples. Methods for load parameter estimation on fundamental as well as carrier cycle basis are presented for operation in steady state and

dynamic conditions respectively. Implementation scheme is described in detail along with real time algorithms. Results and performance comparison with other controllers are presented in this chapter.

Conclusion and future research directions are given in chapter 5.

Chapter 2

Development of a Programmed Ramp Current Controller

2.1 Introduction

Conventional hysteresis current controllers (HCC) have good steady state and dynamic performances. Their implementation is easy when compared to other current controllers [98]. Limitations like switching at high frequency and non-uniform switching make the use of conventional HCC limited [99,100]. Several techniques have been proposed in the past to reduce the non-linear switching of conventional HCC [56,69,74]. Some of the techniques used adaptive variable band strategy to maintain uniform switching frequency [70-72]. In these techniques, the load current spectra contain substantial low order harmonics and hence they are not suitable for industrial drives. There are some improved schemes based on phase locked loops (PLL) [78]. A reference carrier frequency (equal to the desired switching frequency) is supplied to one input of the phase detector and the hysteresis controller output to the other input. The loop filter (low pass) output determines the band width of the hysteresis controller. These schemes work well as far as the disturbance remains within the lock-in-range of the PLL. For large disturbances (which is common in variable speed ac drives), additional filter loops are required to reduce the disturbance [79]. Addition of filter loops degrades the controller performance in respect of current ripple and response time. PLL based schemes give better performance

for fixed frequency applications such as active power filtering in power system [80]. Some researchers intuitively added a triangular carrier waveform (named as ramp comparison controller, RCC) in the feedback path of the conventional HCC and found that in some cases the switching frequency remains uniform [50]. In some cases, it was observed that there were burst switching. Close graphical analysis revealed that the burst switching occurs due to the slope overloading of the feedback current[50, 83-86]. If the ramp waveform is chosen such that its slope is always greater than the worst case (maximum switching frequency), there would be no burst switching [101-103]. No theoretical basis have been developed so far for determination of the carrier slope or amplitude for constant switching in all operating conditions. The RCC works well in the steady state but has poor performance in the dynamic state of operation. Several techniques have been proposed in the literature to remove slope overloading by introducing proportional-integral (PI) controller in the feedback path [84]. But this arrangement degrades the response of the controller although the switching frequency remains constant.

None has successfully solved the problem of non-uniform switching during slope overloading without degrading the controller response of the ramp comparison controller.

In this chapter, a theoretical basis is established showing that a carrier waveform of programmed amplitude and slope when added to the feedback path of HCC would maintain uniform switching frequency. The proposed programmed ramp comparison controller generates the PWM waveforms by comparing the error between the reference current and actual phase current to a triangular carrier waveform of pre-calculated amplitude and frequency. There is no need for introducing any proportional-integral (PI) controller and hysteresis limiter in the feedback path. The dynamic response of the proposed controller is good and comparable to the conventional HCC. A complete mathematical analysis of the controller is discussed in section 2.2. Section 2.3 shows some simulated results of the proposed controller reflecting its performance in different operating conditions.

2.2 Analysis of Conventional HCC

A three phase VSI is considered with a star connected load as shown in Fig. 2.1. For simplicity of analysis the neutral of the star load is connected to the mid-point of the dc supply.

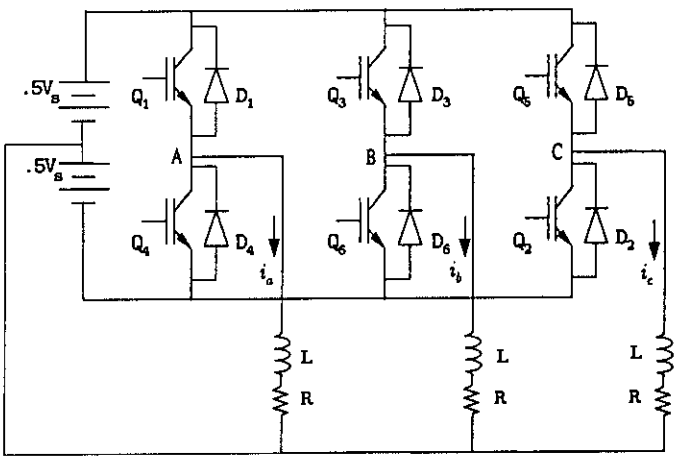

Fig. 2.1: Three phase inverter with star connected load and the neutral connected to the dc supply mid-point.

The inverter consists of six semiconductor switches ($Q_1 - Q_6$) and six diodes ($D_1 - D_6$) in a full bridge configuration. The semiconductor switches and the diodes are considered to be ideal with no switching delays. The switches in any phase are connected to either $(+V_s/2)$ or$(-V_s/2)$. For practical implementation some lockout delays are normally provided between the top and bottom switches in any phase of the inverter to overcome short circuit between the positive and negative bus. Incorporation of small lockout delays do not have significant effect on the operation and performance of an inverter. Moreover, there is no significant variation on the analytical results.

The analysis also holds good for three phase VSI inverters with no neutral connection to the supply mid-point. The analysis is done for one phase (phase A) of the inverter with $R - L$ loads. For motor loads having counter EMF, the equivalent $R - L$ should be considered.

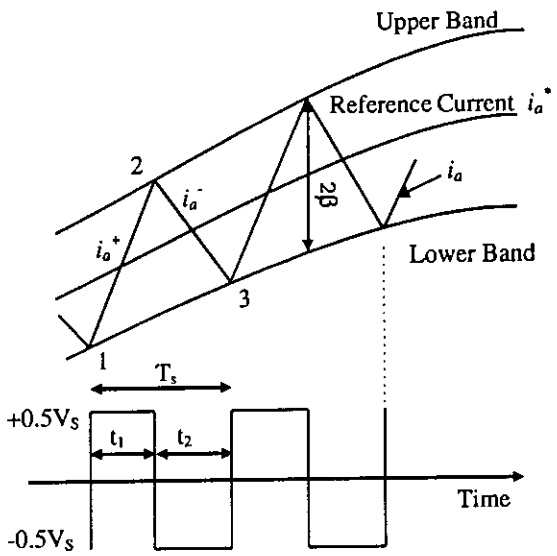

Fig. 2.2: Current and voltage waveform of one phase (Phase A) of a voltage source inverter (VSI) with a current controller.

A sinusoidal reference current is considered, $i_a^* = I_m \sin(\omega t)$. Considering an R-L load fed from phase A of the inverter as shown in Fig. 2.1, the upper switch Q_1 is switched-ON and Q_4 switched-OFF at point 1. This is illustrated in Fig. 2.2. The voltage across the load is positive, and hence the load current (i_a) increases. The rising current segment (i_a^+) then reaches the upper band at point 2 of Fig. 2.2, where, the transistor Q_4 is switched-ON and Q_1 is switched-OFF. At this stage the voltage across the load is negative, hence the load current falls. The falling current segment (i_a^-) touches the lower band at point 3 of Fig. 2.2. The following equations can be written in the respective switching intervals t_1 and t_2

$$Ri_a^+ + L\frac{di_a^+}{dt} = \frac{V_s}{2} \tag{2.1}$$

$$Ri_a^- + L\frac{di_a^-}{dt} = -\frac{V_s}{2} \tag{2.2}$$

where L is the load inductance, R is the load resistance. From the geometry of Fig. 2.2 one can write

$$\frac{di_a{}^+}{dt}t_1 - \frac{di_a{}^*}{dt}t_1 \quad = \quad 2\beta \tag{2.3}$$

$$\frac{di_a^-}{dt}t_2 - \frac{di_a^*}{dt}t_2 = -2\beta \tag{2.4}$$

$$t_1 + t_2 = T_s = \frac{1}{f_s} \tag{2.5}$$

where t_1 and t_2 are the respective switching intervals, β is the hysteresis band width (current ripple band), and f_s is the switching frequency. Adding (2.3) and (2.4) and substituting in (2.5), one can write

$$\frac{di_a^+}{dt}t_1 + \frac{di_a^-}{dt}t_2 - \frac{1}{f_s}\frac{di_a^*}{dt} = 0 \tag{2.6}$$

Subtracting (2.4) from (2.3), one gets

$$4\beta = \frac{di_a^+}{dt}t_1 - \frac{di_a^-}{dt}t_2 - (t_1 - t_2)\frac{di_a^*}{dt} \tag{2.7}$$

For low value of the band β, the rising and falling currents i_a^+ and i_a^- can be approximated to i_a. With this approximation, combining (2.1), (2.2) and (2.6) one gets

$$\frac{t_1}{L}\left(\frac{V_s}{2} - Ri_a\right) - \frac{t_2}{L}\left(\frac{V_s}{2} + Ri_a\right) - \frac{m}{f_s} = 0 \tag{2.8}$$

Where m is the slope of the reference current wave ($m = \frac{di_a^*}{dt}$). Simplification of (2.8) yields

$$t_1 - t_2 = \frac{2L}{V_s f_s}\left(\frac{Ri_a}{L} + m\right) \tag{2.9}$$

From (2.1), (2.2), (2.7) and (2.9) one can write

$$\begin{aligned} 4\beta &= \frac{t_1}{L}\left(\frac{V_s}{2} - Ri_a\right) + \frac{t_2}{L}\left(\frac{V_s}{2} + Ri_a\right) - \frac{2Lm}{V_s f_s}\left(\frac{Ri_a}{L} + m\right) \\ &= \frac{V_s}{2f_s L} - \frac{Ri_a}{L}(t_1 - t_2) - \frac{2Lm}{V_s f_s}\left(\frac{Ri_a}{L} + m\right) \\ &= \frac{V_s}{2f_s L} - \frac{2Ri_a}{V_s f_s}\left(\frac{Ri_a}{L} + m\right) - \frac{2Lm}{V_s f_s}\left(\frac{Ri_a}{L} + m\right) \\ &= \frac{V_s}{2f_s L}\left[1 - \frac{4L^2}{{V_s}^2}\left(\frac{Ri_a}{L} + m\right)^2\right] \end{aligned} \tag{2.10}$$

$$\text{or,} \qquad f_s = \frac{0.125V_s}{\beta L}\left[1 - \frac{4L^2}{{V_s}^2}\left(\frac{Ri_a}{L} + m\right)^2\right] \tag{2.11}$$

Equation (2.11) shows that the switching frequency f_s of the HCC have time varying quantity like m and i_a and hence the switching frequency (f_s) would vary over the fundamental period. The time varying component of the switching frequency expression is

$(\frac{Ri_a}{L} + m)$. For fixed switching frequency operation of the inverter, there should be no time dependent term in the switching frequency equation. i.e.,

$$\frac{Ri_a}{L} + m = \text{Constant} \tag{2.12}$$

It is shown in the following few paragraphs that constant switching frequency can be attained in practice by addition of a triangular carrier (i_t) to the reference current i_a^*. The underlying philosophy is that, if a triangular carrier at the desired switching frequency is added to the sinusoidal reference current, the slope of the carrier will be dominant and the squared slope term in (2.11) would be almost constant.

The carrier waveform is illustrated in Fig. 2.3. The abrupt change observed in Fig. 2.3 at the start of a new carrier period is due to carrier period based amplitude adjustment.

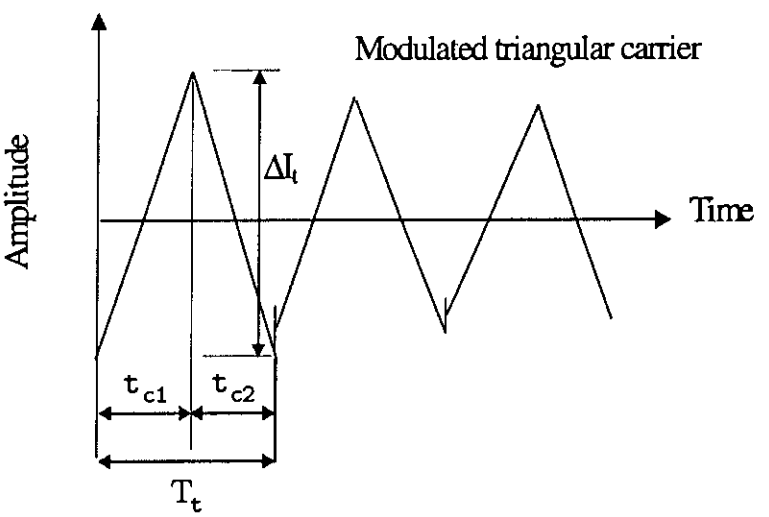

Fig. 2.3: Variable-slope amplitude modulated triangular waveform carrier to be added to a current controller.

The triangular carrier is super-imposed to the sinusoidal reference and the switching points are obtained from natural sampling process by comparison with the load current. The new reference current $(\widehat{i_a^*})$ can be expressed as

$$\widehat{i_a^*} = I_m \sin \omega t + i_t \tag{2.13}$$

With the introduction of the add-on function (i_t) with the sine reference current, (2.12) can be rewritten as

$$\frac{Ri_a}{L} + \widehat{m} = G \tag{2.14}$$

Where $\widehat{m}$ is the slope of the new reference current and G is a constant.

Differentiating (2.13) one gets

$$\frac{d\widehat{i_a^*}}{dt} = \widehat{m} = I_m\omega\cos\omega t + m_t \tag{2.15}$$

where m_t is the slope of the carrier waveform, $m_t = \frac{di_t}{dt}$.

Combining (2.14) and (2.15), one can write

$$\frac{Ri_a}{L} + I_m\omega\cos\omega t + m_t = G \tag{2.16}$$

For the rising and falling edges of the carrier, (2.16) can be written in the form

$$\frac{Ri_a}{L} + I_m\omega\cos\omega t + {m_t}^+ = |G| \tag{2.17}$$

$$\frac{Ri_a}{L} + I_m\omega\cos\omega t - {m_t}^- = -|G| \tag{2.18}$$

Where, m_t^+ and m_t^- are the slopes of the rising and falling segments of the carrier waveform.

Assuming $i_a \cong i^*$ (i.e., $i_a \cong I_m\sin(\omega t)$), (2.17) and (2.18) can be rewritten as

$$\begin{aligned} {m_t}^+ &= |G| - \frac{I_m}{L}(R\sin wt + L\omega\cos\omega t) \\ &= |G| - \frac{E_m\sin(\omega t+\theta)}{L} \end{aligned} \tag{2.19}$$

$$\begin{aligned} {m_t}^- &= |G| + \frac{I_m}{L}(R\sin wt + L\omega\cos\omega t) \\ &= |G| + \frac{E_m\sin(\omega t+\theta)}{L} \end{aligned} \tag{2.20}$$

where $E_m = I_m\sqrt{R^2+(\omega L)^2} = I_m Z$, $Z = \sqrt{R^2+(\omega L)^2}$ and $\theta = \tan^{-1}\frac{\omega L}{R}$.

The positive and negative slopes of the triangular carrier waveform (Fig. 2.3) may be assumed constant within the respective rising and falling segments of the carrier period. The slopes may be obtained as

$$m_t^+ = \frac{\Delta I_t}{t_{c1}} \tag{2.21}$$

$$m_t^- = \frac{\Delta I_t}{t_{c2}} \tag{2.22}$$

Where ΔI_t is the peak to peak amplitude of the carrier waveform, t_{c1} is the rise time of the carrier from its negative peak to the positive peak and t_{c2} is the fall time of the carrier from its positive peak to the negative peak in a carrier period.

Combining (2.21), (2.22), (2.19) and (2.20) one gets

$$\begin{aligned} T_t &= \frac{1}{f_t} \\ &= \Delta I_t \left[\frac{1}{|G| - \frac{E_m}{L}\sin(\omega t + \theta)} + \frac{1}{|G| + \frac{E_m}{L}\sin(\omega t + \theta)} \right] \qquad (2.23) \\ &= \frac{2\Delta I_t}{|G|} \left[\frac{1}{1 - \frac{{E_m}^2}{2G^2L^2}\{1 - \cos(2\omega t + 2\theta)\}} \right] \qquad (2.24) \\ \Delta I_t &= \frac{|G|}{2f_t} \left[1 - \frac{{E_m}^2}{2G^2L^2} + \frac{{E_m}^2}{2G^2L^2}\cos(2\omega t + 2\theta) \right] \qquad (2.25) \end{aligned}$$

Combining (2.11) and (2.14), one gets

$$f_s = \frac{0.125V_s}{\beta L}\left[1 - \left(\frac{2LG}{V_s}\right)^2\right] \tag{2.26}$$

$$\text{or,} \qquad \beta = \frac{0.125V_s}{f_s L}\left[1 - \left(\frac{2LG}{V_s}\right)^2\right] \tag{2.27}$$

Thus for the $R-L$ load, constant switching frequency can be attained by the addition of an amplitude modulated triangular carrier described by (2.25).

To get uniform switching pulse patterns, it must be ensured that there should be one crossing of the load current in a half carrier cycle. To achieve this in practice, the magnitude of G should be as large as possible. A large value of G is associated with high carrier amplitude. The magnitude of G can be determined from (2.27). Keeping in mind that β is to be positive quantity, the term within braces of (2.27) should be positive. This means that $1 - \left(\frac{2LG}{V_s}\right)^2$ should have a magnitude between 0 and 1. Taking an average value of 0.5, one gets

$$1 - \left(\frac{2LG}{V_s}\right)^2 = 0.5 \tag{2.28}$$

$$\text{or,} \qquad G = \frac{V_s}{2\sqrt{2}L} \tag{2.29}$$

Substituting G from (2.29) to (2.25) yields,

$$\Delta I_t = \frac{V_s}{4\sqrt{2}Lf_t}\left\{1 - \left(\frac{2E_m}{V_s}\right)^2 + \left(\frac{2E_m}{V_s}\right)^2 \cos\left(2\omega t + 2\theta\right)\right\} \tag{2.30}$$

The current ripple can be obtained by combining (2.27) and (2.29) (and using $f_s = f_t$) as

$$\beta = \frac{0.0625V_s}{f_t L} \tag{2.31}$$

The switching frequency equation in (2.26) has no time dependent terms, indicating a constant switching frequency. This means that a constant switching PWM pattern can be obtained in a current controller by introducing an amplitude modulated triangular carrier waveform (i_t). This scheme has been referred to as AMPRC (amplitude modulated programmed ramp controller) in the later sections. The modulation function has a raised double frequency cosine wave and is dependent on the dc supply voltage V_s , fundamental voltage amplitude E_m, load inductance L, carrier frequency f_t and the phase angle θ of the load. By programming the amplitude of the triangular carrier by (2.30) a constant switching operation of the inverter can be ensured.

2.2.0.1 Simplified Constant Amplitude Carrier Waveform

Instead of giving a variable amplitude triangular carrier, the maximum amplitude of the triangular carrier obtained from (2.30) can be applied to the entire fundamental period for constant switching operation. With this simplification the amplitude of the triangular carrier will be

$$\Delta I_t = \frac{V_s}{4\sqrt{2}Lf_t} \tag{2.32}$$

This scheme is referred to PRC (programmed ramp comparison current controller) in the later sections. The PRC scheme is shown in Fig. 2.4. A ramp signal of frequency f_t and amplitude given by (2.32) are added to the current feedback path. Equations (2.29)-(2.31) gives some useful information about the new controller. It is evident from (2.30) and (2.32) that the ramp signal amplitude can be programmed from the information of the supply voltage V_s and the load inductance L to have a constant switching PWM pattern.

In the new controller, the current ripple magnitude is given by (2.31) and hence can be pre-calculated from the information of V_s, L and f_t . Since the worst case (maximum) amplitude of the ramp signal is used for the entire fundamental period there is no risk of exceeding the current ripple beyond that given by (2.31). Also, there will be no risk of multiple crossing of the load current which arises due to slope overloading in conventional ramp comparison controllers.

2.3 Controller Scheme

A scheme of the proposed current controller is shown in Fig. 2.4. For AMPRC, the scheme needs information of the load inductance (L) and peak value of the phase voltage (E_m). However, for PRC the inductance information is enough for computing the slope and amplitude of the carrier add on function (i_t). The magnitudes of L and E_m are extracted from the phase voltage (v_{an}) and phase current (i_a) using the "DFT and other processing" block. The computations require fundamental voltage, current and their associated phase angles which is obtained by DFT method. The "carrier parameter computation block" compute the slope and amplitude of the carrier (ramp signal) from V_s, E_m, L and θ using (2.30) or (2.32). The carrier signal is added to reference currents i_a^*, i_b^* and i_c^*. The resultant signals are then compared to the corresponding load currents (i_a, i_b, i_c) using two level comparators. The comparator outputs drive the inverter (Fig. 2.5).

2.3.1 Performance Study

The performance of the proposed programmed ramp comparison controllers are studied through simulations using Matlab [104]. The simulation is done on a three phase VSI with $R-L$ load as shown in Fig. 2.5. The inverter consists of three single-pole-double-throw ($SPDT$) switches Q_A, Q_B, Q_C. This means that the switches in any phase are connected to either the positive or the negative bus of the dc supply. The switches are assumed to be ideal having no ON/OFF delay. In a neutral unconnected system as shown in Fig. 2.5, the dc voltage across the phase is either one third or two third of the supply voltage during the inverter operation. The average dc voltage across the load is thus half the supply

voltage (i.e. $V_s/2$). Hence, the analysis described in section 2.2 is applicable for neutral unconnected system as well. The simulator circuit of Fig. 2.4 generates three phase reference current signals (i_a^*, i_b^* and i_c^*) of desired amplitude and frequency. The ramp generator generates a triangular waveform as calculated from (2.30) or (2.32). The PWM waveforms for phases A, B, C are obtained by comparing the respective phase current errors to the ramp waveform. Few samples of the simulated outputs of the proposed controller are shown in Figs. 2.6-2.12.

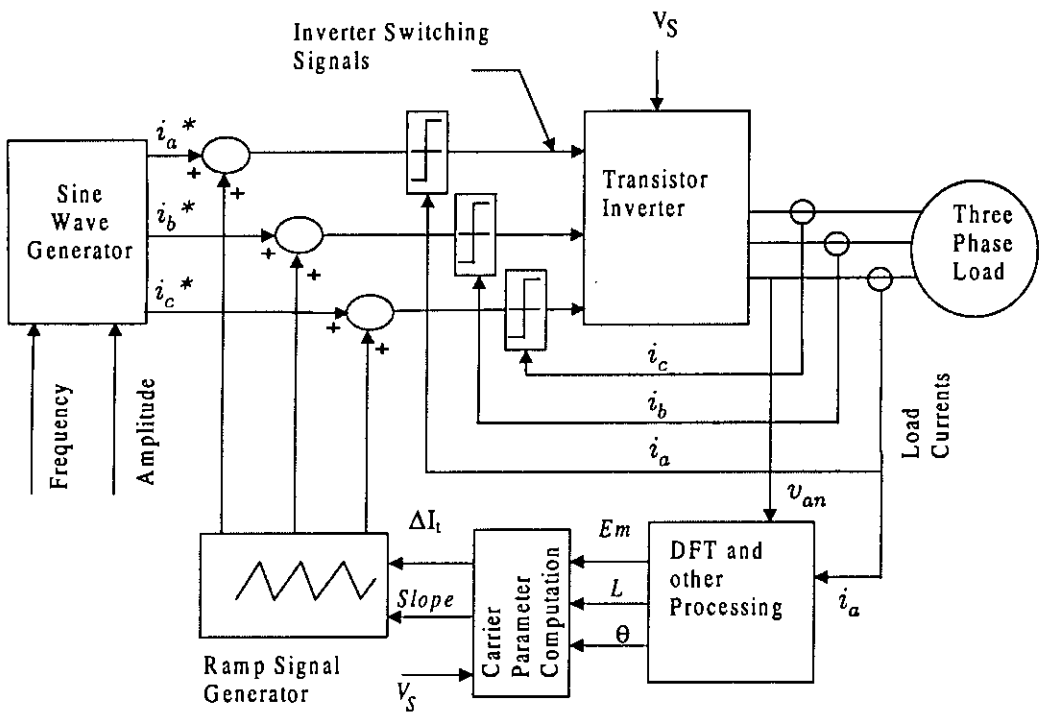

Fig. 2.4: Implementation scheme of the proposed programmed ramp comparison current controller.

2.3.1.1 Amplitude Modulated Programmed Ramp Controller (AMPRC)

The triangular carrier waveform is computed using (2.30). The simulation is done with a sampling rate of 1024 per fundamental period. The PWM patterns for Q_A , Q_B , and Q_C are obtained by comparing the individual phase current errors with the amplitude modulated carrier waveform. There is no need for three separate carrier waveforms for

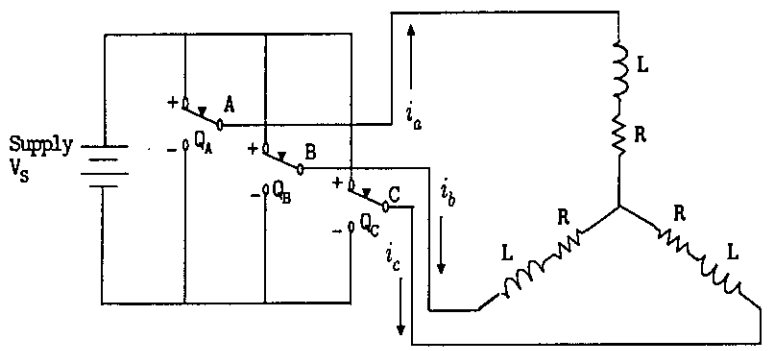

Fig. 2.5: Three phase voltage source inverter (VSI) with ideal (SPDT) switches in each phase connected to star connected $R-L$ load.

three phases in a neutral unconnected system since the phases are interdependent. Typical simulation results of the proposed Amplitude Modulated Programmed Ramp Comparison Controller are shown in Figs. 2.6-2.9. Response of the controller for both steady and dynamic states are studied through simulation. Simulation results of three phase load currents, complex plot of the load current vector, PWM pattern for the SPDT switches of one phase, phase voltage waveform in per unit, carrier waveform, switching frequency distribution, net current error and frequency spectra of the load current are shown in the figures. The simulation is done at 50 Hz for a load with $R = 8\Omega$, $L = 19.1mH$, $V_s = 240$ volts, $I_m = 5A$. The triangular carrier is set at 1200 Hz. The steady state responses are shown in Figs. 2.6-2.7. The current ripples are within that of the theoretically calculated values. The switching frequency distribution is constant and equals to the frequency of the amplitude modulated triangular carrier (1200 Hz).

The start up response of the controller with the same load and frequencies are shown in Figs. 2.8-2.9. The load currents for the three phases start from zero initial conditions. The load currents of all three phases tracks the reference within 30^0 from the start without any overshoot. From Fig. 2.9 it is clear that the switching frequency distribution is still uniform.

Figures 2.10-2.11 show the dynamic performance of the controller during running conditions. A current step of 5A to 10A is applied at 90^0 keeping the load parameters constant. The controller tracks the load current reference within 30^0 of the disturbance. There are no overshoots in any phases during the dynamic state change. The switching frequency does not increase at the dynamic state, rather it decreases as is evident from Fig. 2.11(b). After the transition the switching frequency remains uniform.

2.3.1.2 Programmed Ramp Controller (PRC)

The amplitude modulated programmed ramp comparison controller is computation intensive and will require fast processing for real time implementation. The computational requirement is substantially reduced in the simplified programmed carrier defined by (2.32). The steady state, start-up and dynamic response of the PRC are studied for the same load as that of AMPRC. The steady state output of the controller are shown in Figs. 2.12-2.13. The switching frequency (Fig. 2.13) is constant at 1200 Hz which is equal to the frequency of the programmed ramp waveform. The start-up response as shown in Figs. 2.14-2.15 of the PRC is also smooth as AMPRC. The switching frequency is constant from start-up to steady state and equals the triangular carrier frequency. The dynamic response of the PRC are studied for two cases. In the first case a step change of current reference from 5A to 10A is applied at 90^0. The responses of the controller are shown in Figs. 2.16-2.17. The switching frequency goes low at the dynamic change point and there are no current overshoots during the dynamic state. In the second case, a change of load from $R = 8\Omega$, $L = 19.1mH$ to $R = 4\Omega$, $L = 28.6mH$ is applied at 90^0 to see the dynamic response. The output of the controller are shown in Figs. 2.18-2.19. The controller quickly adapts to the new load and maintains constant switching frequency (Fig. 2.19).

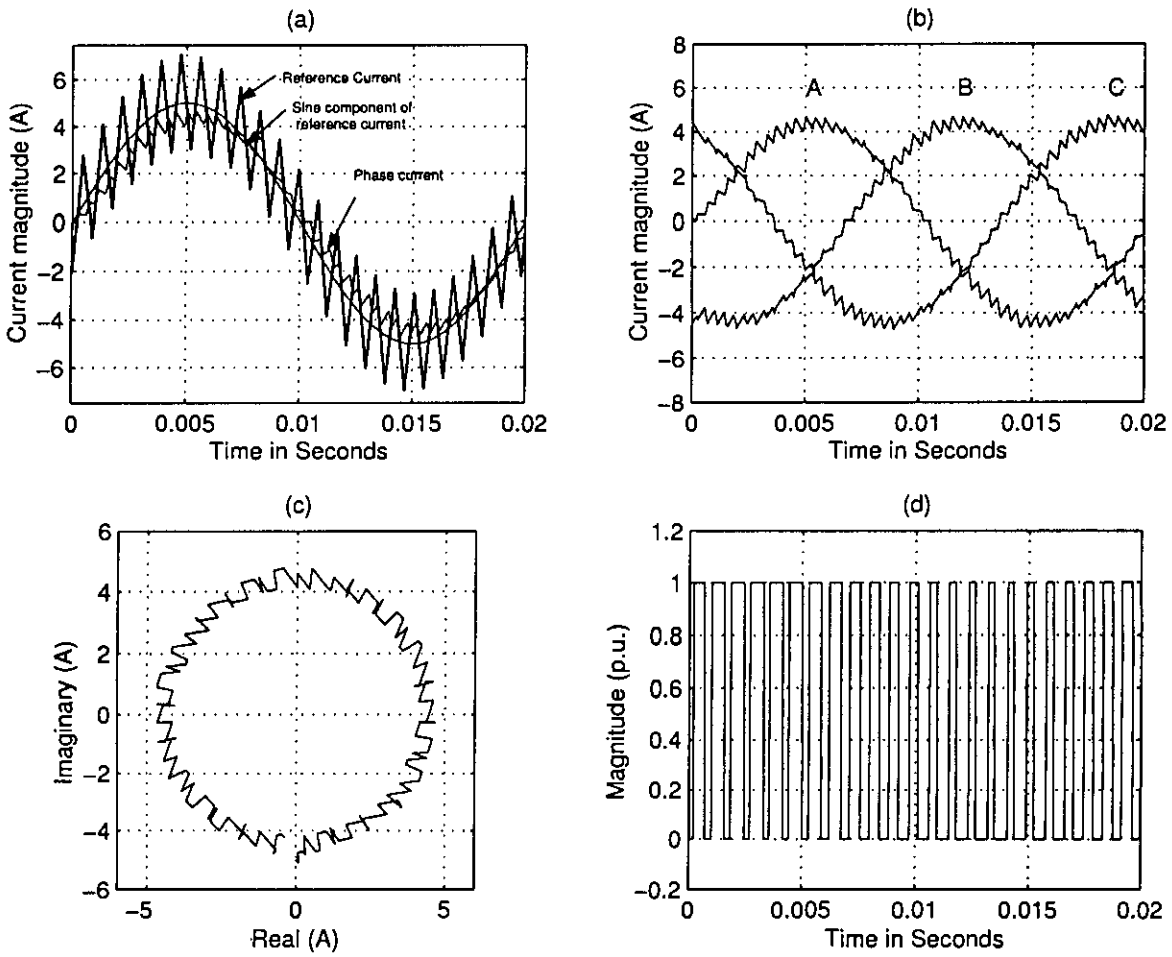

Fig. 2.6: Steady state response of the Amplitude Modulated Programmed Ramp Comparison Controller (AMPRC) with $f = 50Hz$, $R = 8\Omega$, $L = 19.1mH$, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$: (a) Reference current and phase current (for phase A), (b) Load current waveforms for phases A, B and C , (c) Combined current vector in complex plane , (d) PWM switching pattern for switch Q_1.

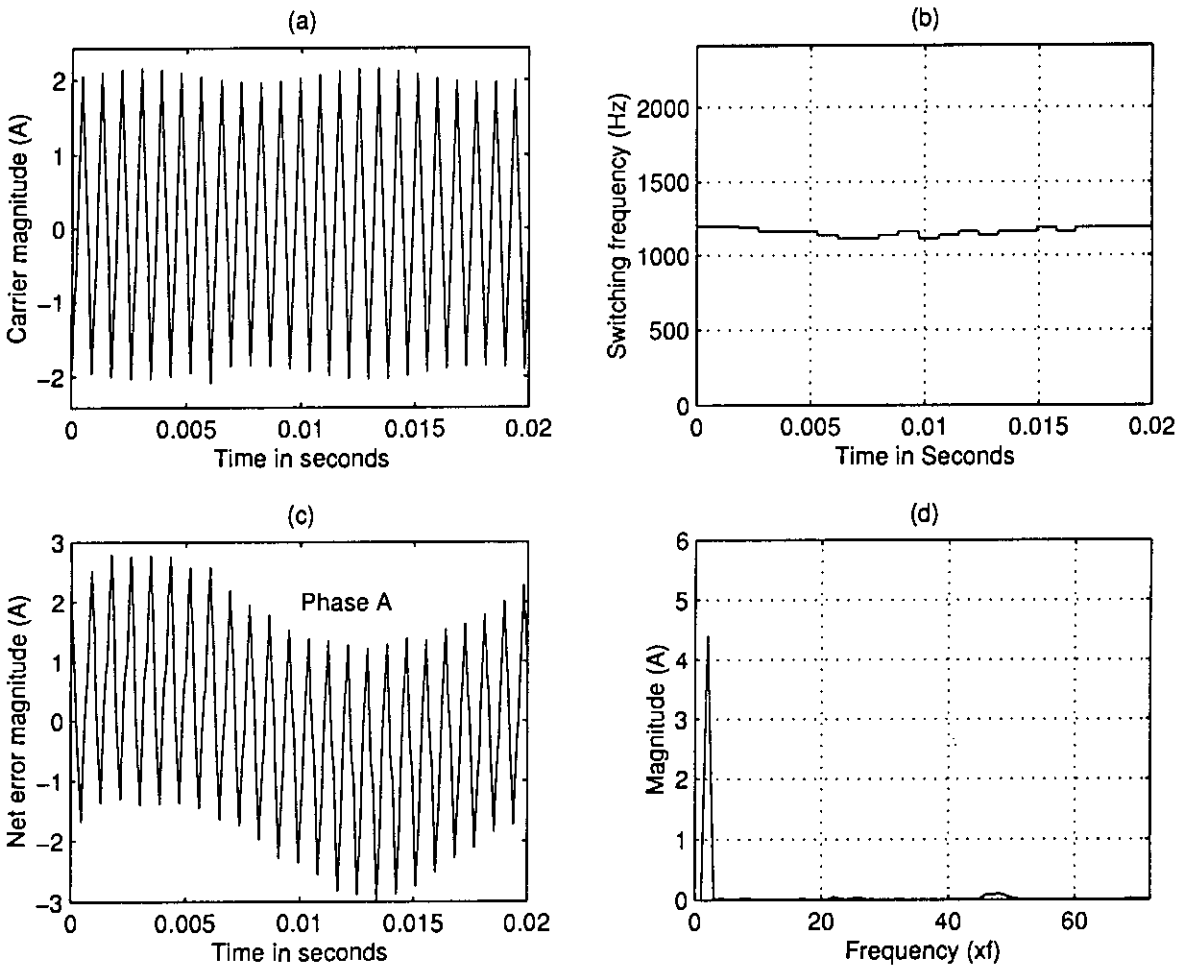

Fig. 2.7: Steady state response of the Amplitude Modulated Programmed Ramp Comparison Controller (AMPRC) with $f = 50Hz$, $R = 8\Omega$, $L = 19.1mH$, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$: (a) Modulated ramp waveform , (b) Switching frequency distribution over the fundamental period, (c) Net error signal for phase A prior to comparator, (d) Spectrum of the load current.

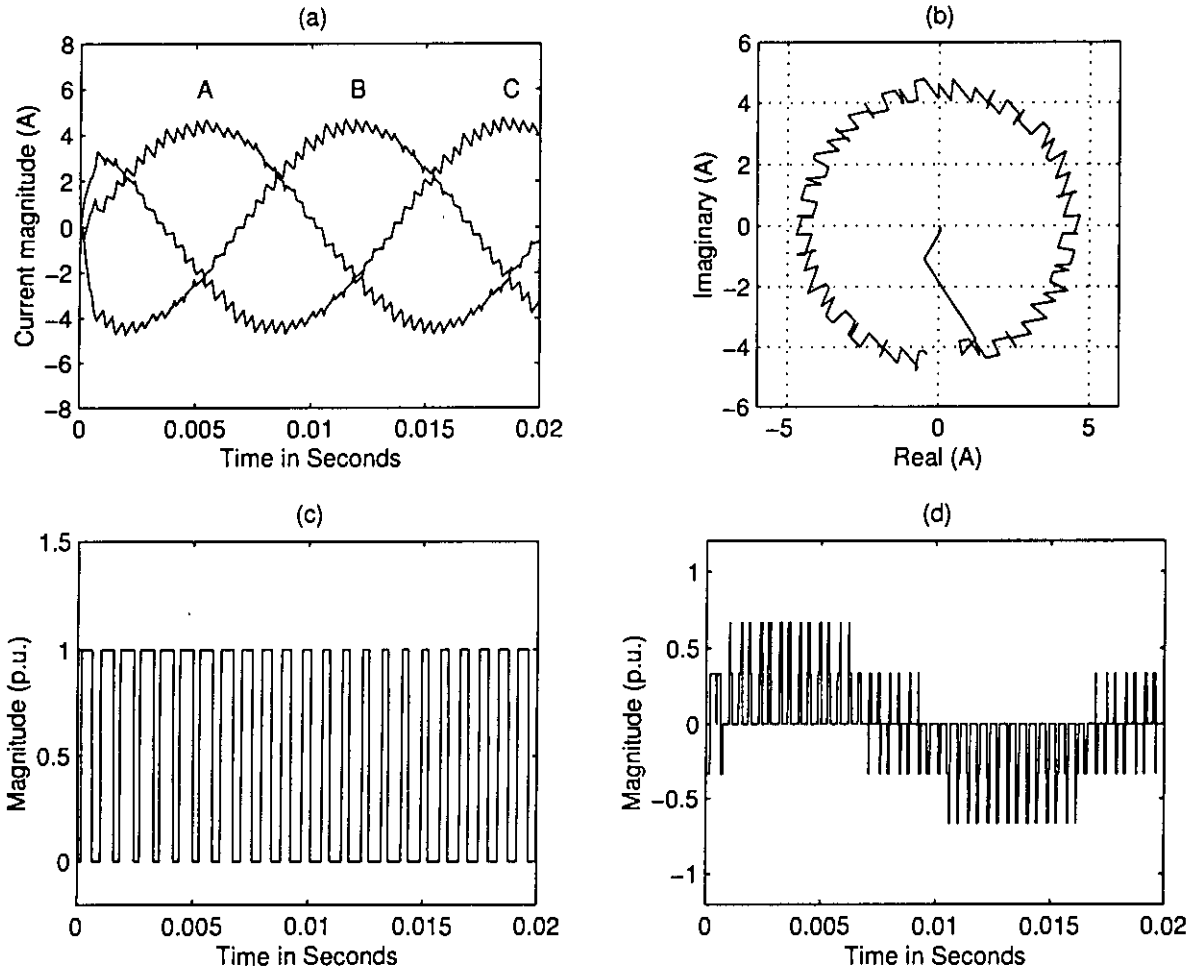

Fig. 2.8: Start-up response of the Amplitude Modulated Programmed Ramp Comparison Controller (AMPRC) with $f = 50Hz$, $R = 8\Omega$, $L = 19.1mH$, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$: (a) Load current waveforms for phases A, B and C , (b) Combined current vector in complex plane , (c) PWM switching pattern for switch Q_1 , (d) Line to neutral voltage waveform of phase A in p.u.

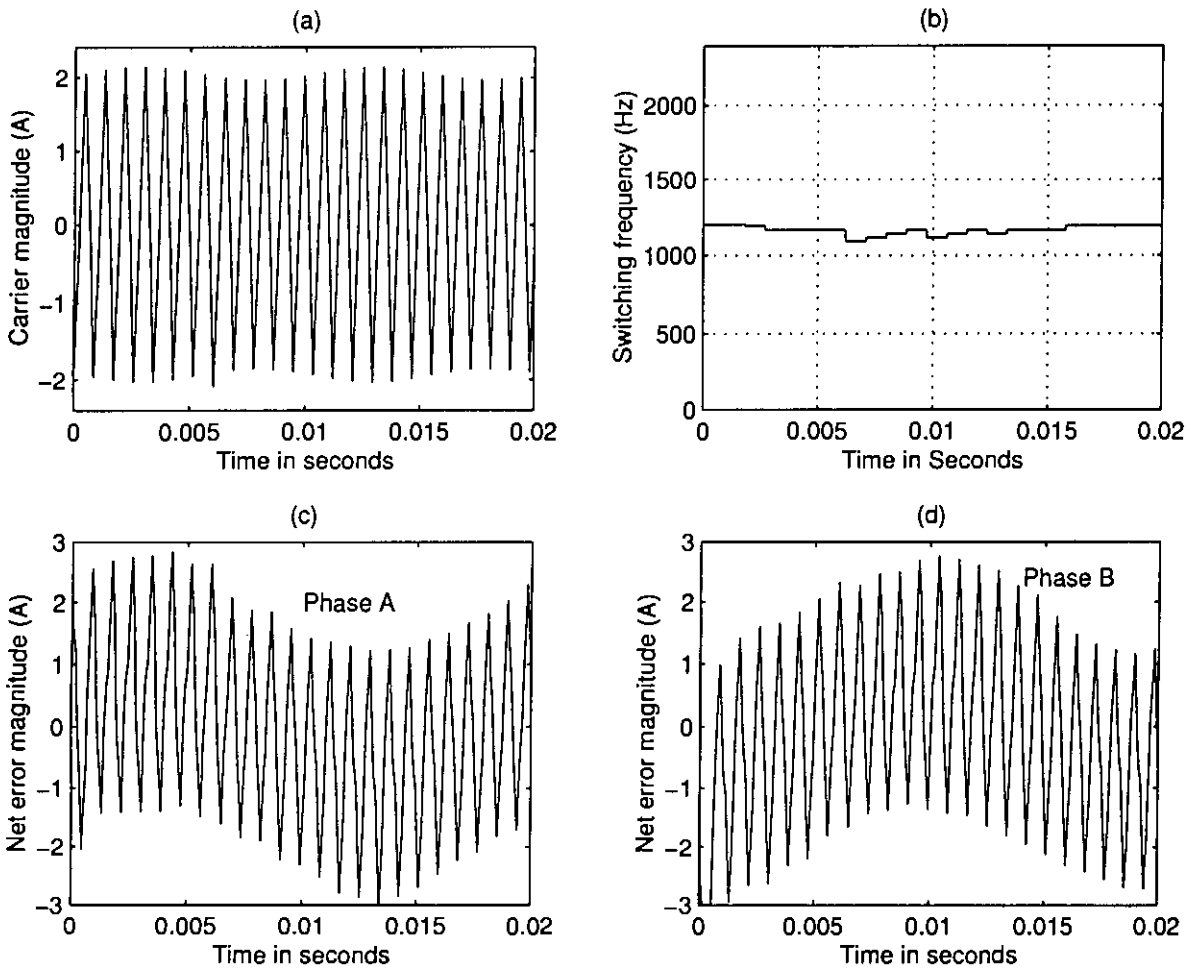

Fig. 2.9: Start-up response of the Amplitude Modulated Programmed Ramp Comparison Controller (AMPRC) with $f = 50Hz$, $R = 8\Omega$, $L = 19.1mH$, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$: (a) Modulated ramp waveform , (b) Switching frequency distribution over fundamental period, (c) Net error signal for phase A prior to comparator, (d) Net error signal for phase B prior to comparator.

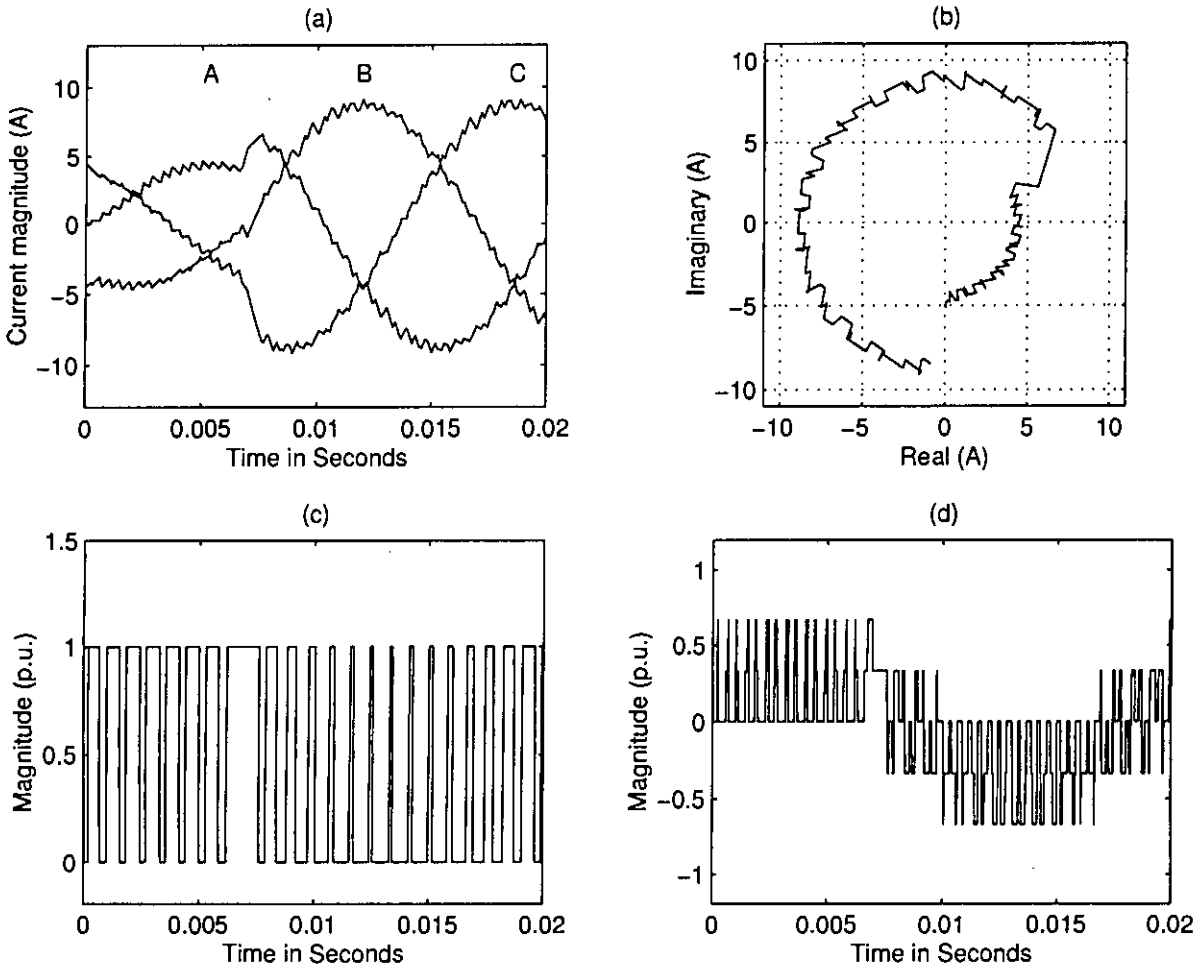

Fig. 2.10: Dynamic response of the Amplitude Modulated Programmed Ramp Comparison Controller (AMPRC) with $f = 50Hz$, $R = 8\Omega$, $L = 19.1mH$, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$ to $10A$ at 90^0: (a) Load current waveforms for phases A, B and C , (b) Combined current vector in complex plane , (c) PWM switching pattern for switch Q_1 , (d) Line to neutral voltage waveform of phase A in p.u.

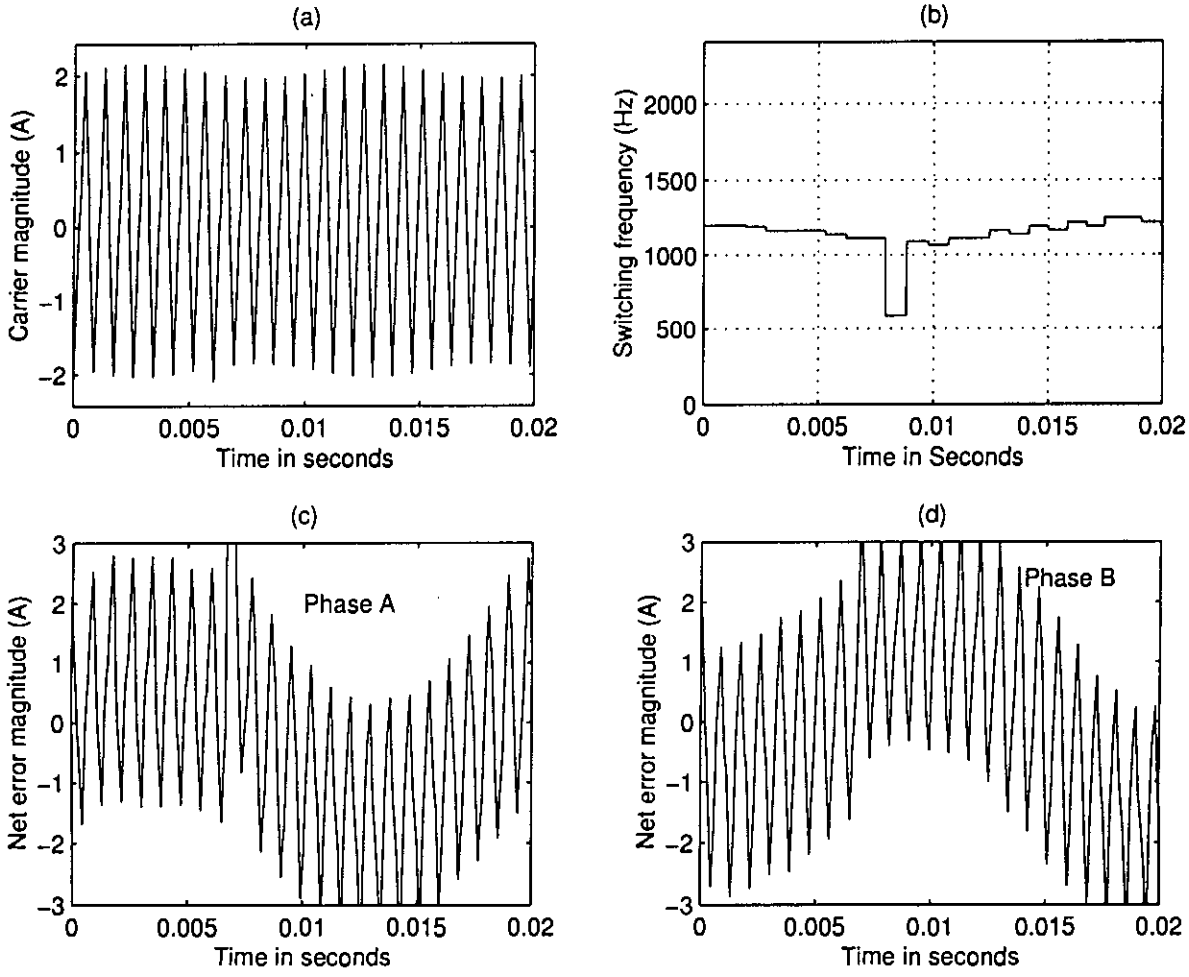

Fig. 2.11: Dynamic response of the Amplitude Modulated Programmed Ramp Comparison Controller (AMPRC) with $f = 50Hz$, $R = 8\Omega$, $L = 19.1mH$, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$ to $10A$ at 90^0: (a) Modulated ramp waveform , (b) Switching frequency distribution over the fundamental period, (c) Net error signal for phase A prior to comparator, (d) Net error signal for phase B prior to comparator.

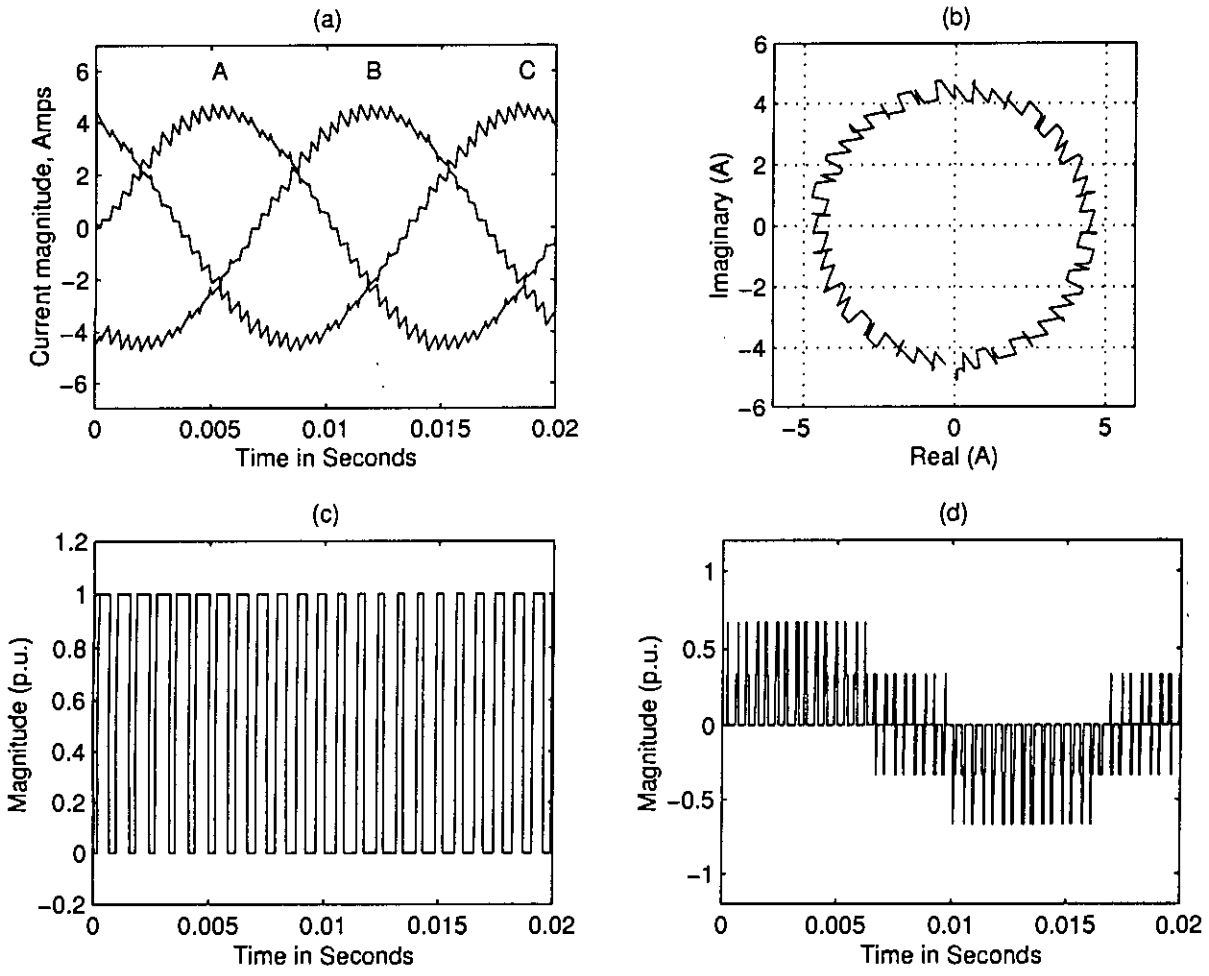

Fig. 2.12: Steady state response of the Programmed Ramp Comparison Controller (PRC) with $f = 50Hz$, $R = 8\Omega$, $L = 19.1mH$, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$: (a) Load current waveforms for phases A, B and C , (b) Combined current vector in complex plane , (c) PWM switching pattern for switch Q_1 , (d) Line to neutral voltage waveform of phase A in p.u.

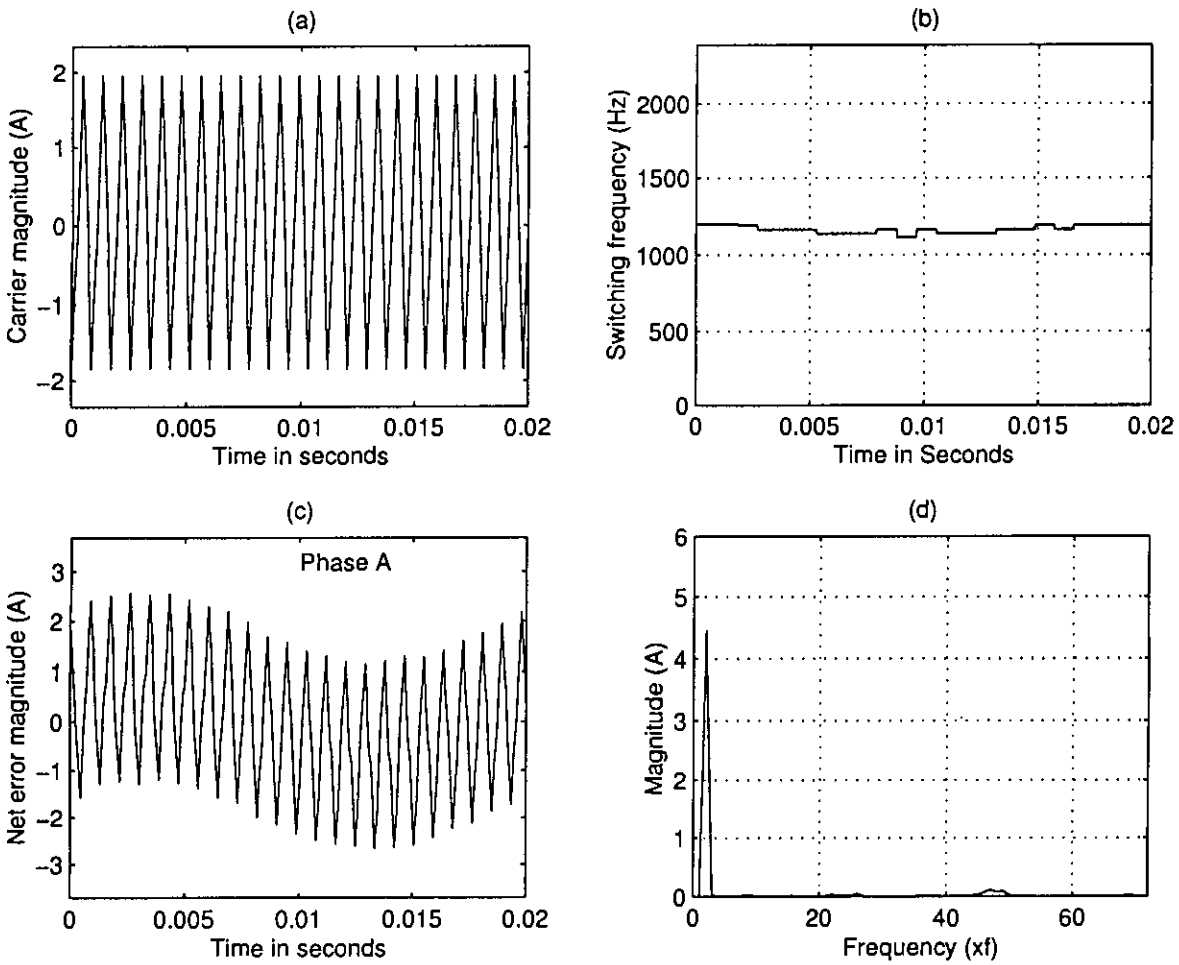

Fig. 2.13: Steady state response of the Programmed Ramp Comparison Controller (PRC) with $f = 50Hz$, $R = 8\Omega$, $L = 19.1mH$, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$: (a) Ramp waveform , (b) Switching frequency distribution over the fundamental period, (c) Net error signal for phase A prior to comparator, (d) Spectrum of the load current.

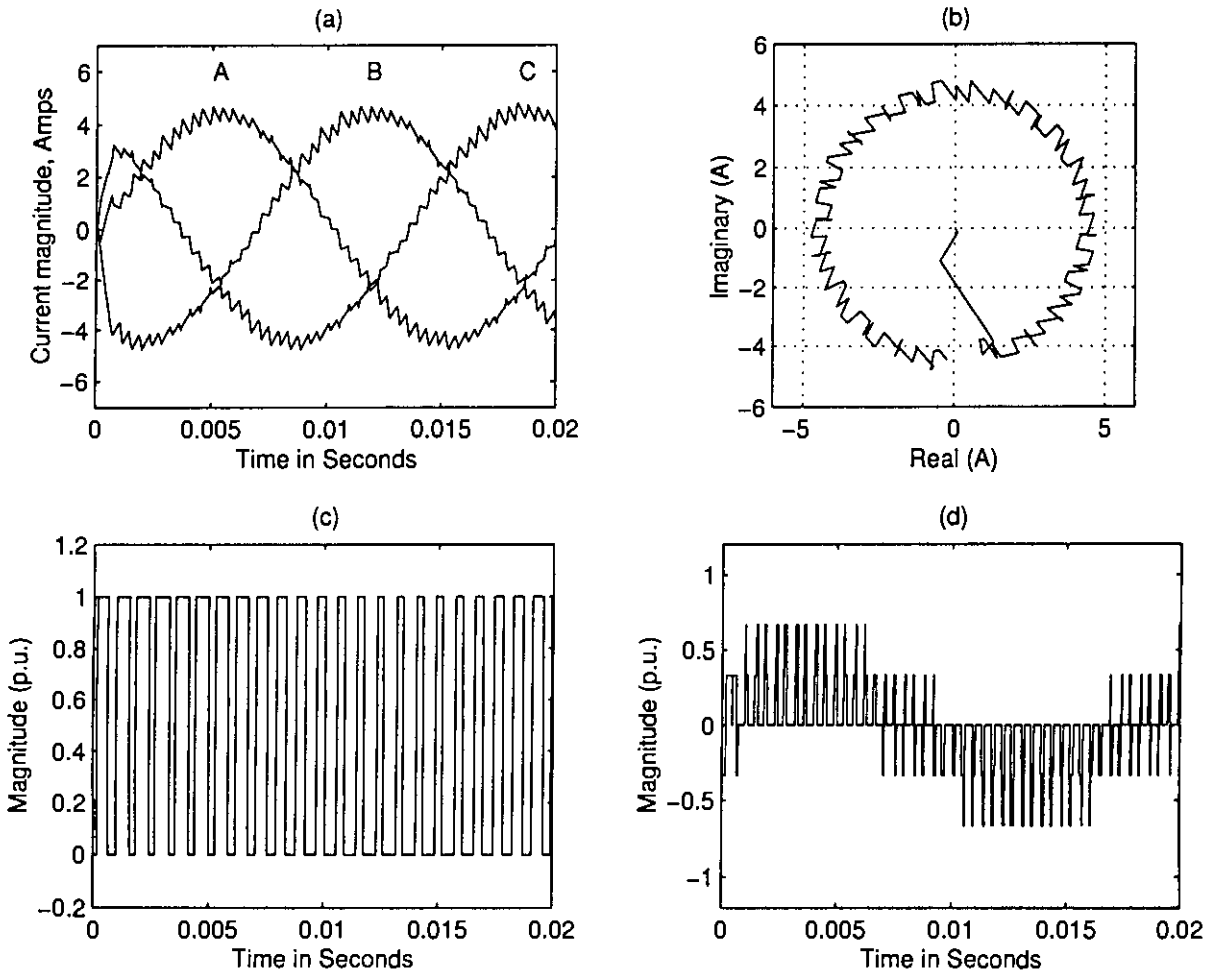

Fig. 2.14: Start-up response of the Programmed Ramp Comparison Controller (PRC) with $f = 50Hz$, $R = 8\Omega$, $L = 19.1mH$, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$: (a) Load current waveforms for phases A, B and C , (b) Combined current vector in complex plane , (c) PWM switching pattern for switch Q_1 , (d) Line to neutral voltage waveform of phase A in p.u.

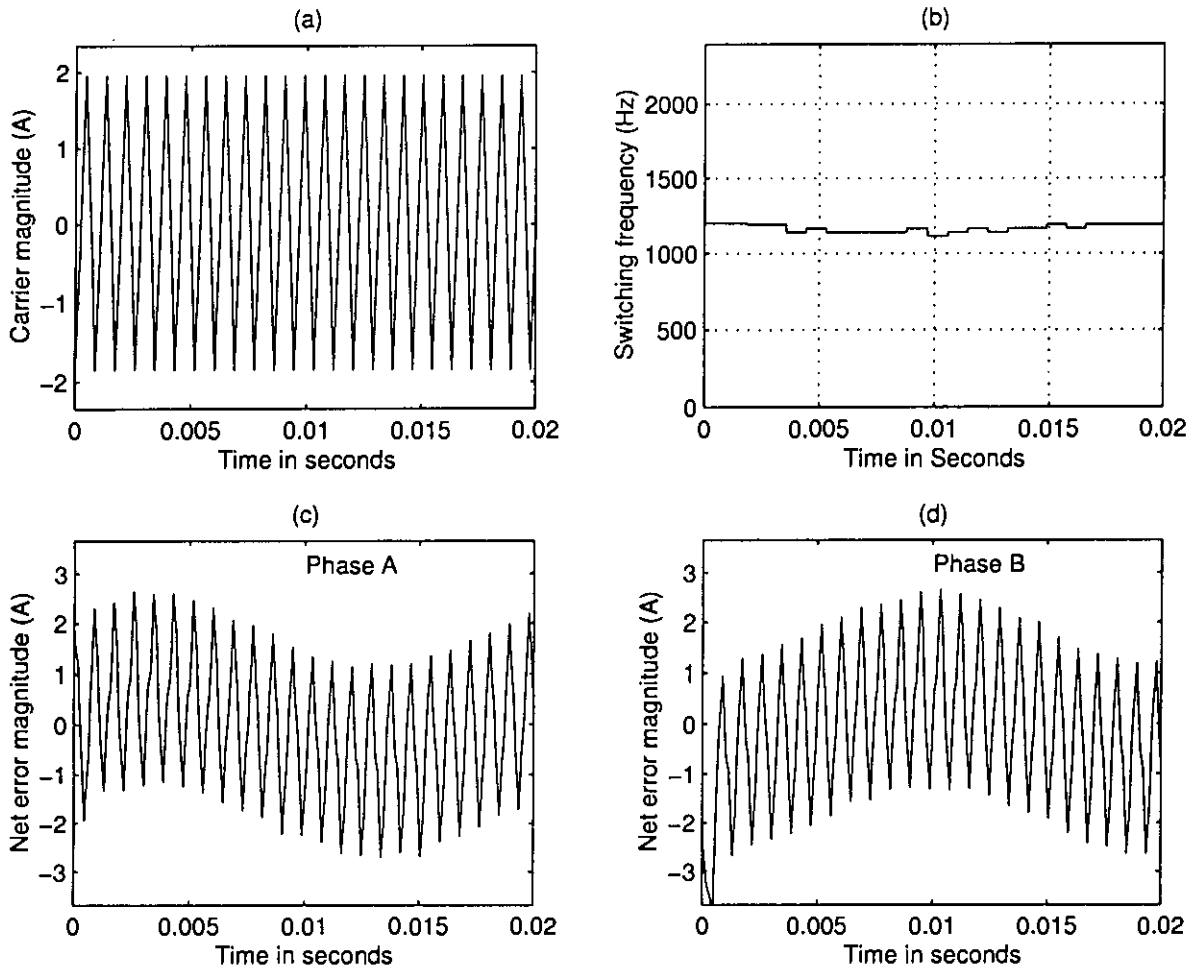

Fig. 2.15: Start-up response of the Programmed Ramp Comparison Controller (PRC) with $f = 50Hz$, $R = 8\Omega$, $L = 19.1mH$, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$: (a) Ramp waveform , (b) Switching frequency distribution over the fundamental period, (c) Net error signal for phase A prior to comparator, (d) Net error signal for phase B prior to comparator.

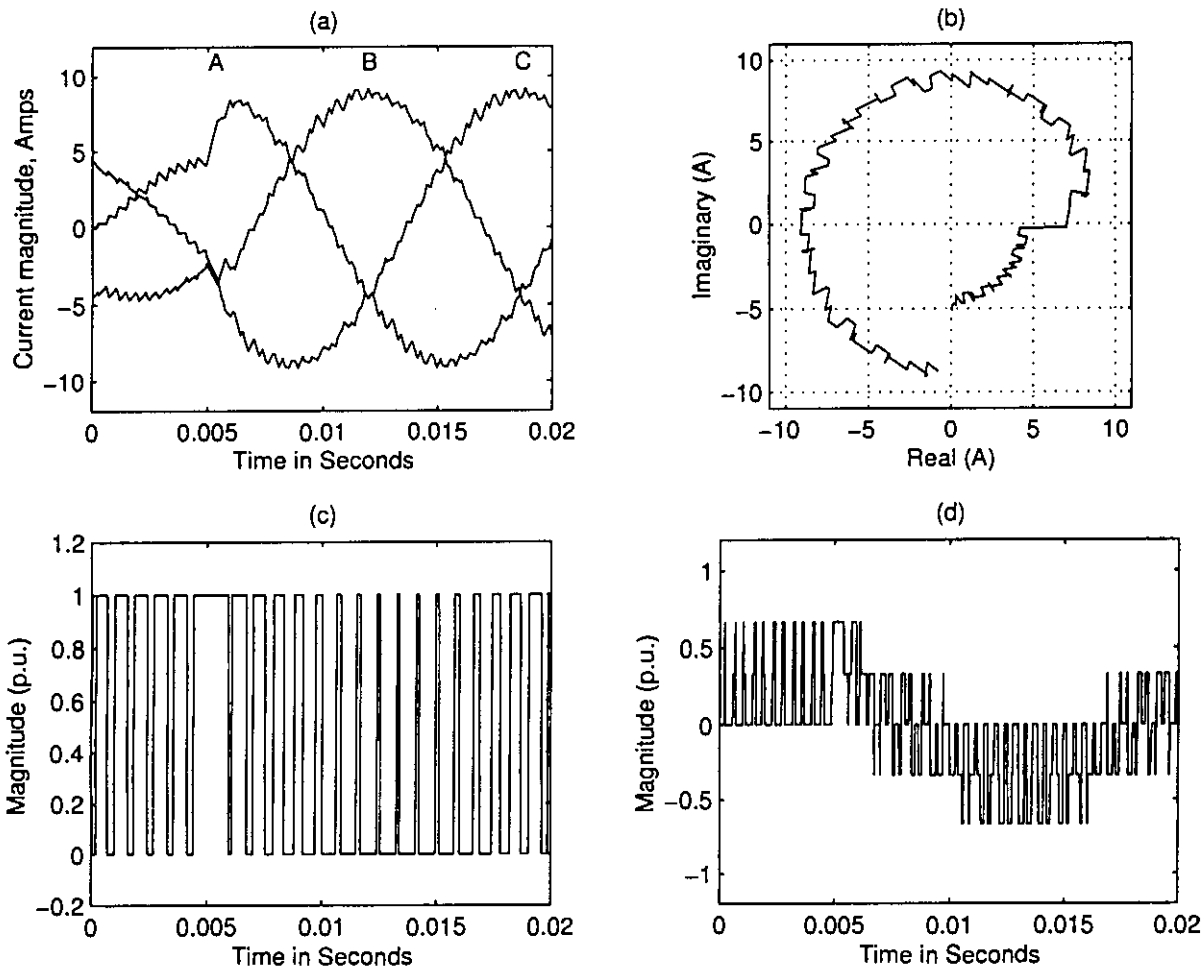

Fig. 2.16: Dynamic response of Programmed Ramp Comparison Controller (PRC) with $f = 50Hz$, $R = 8\Omega$, $L = 19.1mH$, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$ to $10A$ at 90^0: (a) Load current waveforms for phases A, B and C , (b) Combined current vector in complex plane , (c) PWM switching pattern for switch Q_1 , (d) Line to neutral voltage waveform of phase A in p.u.

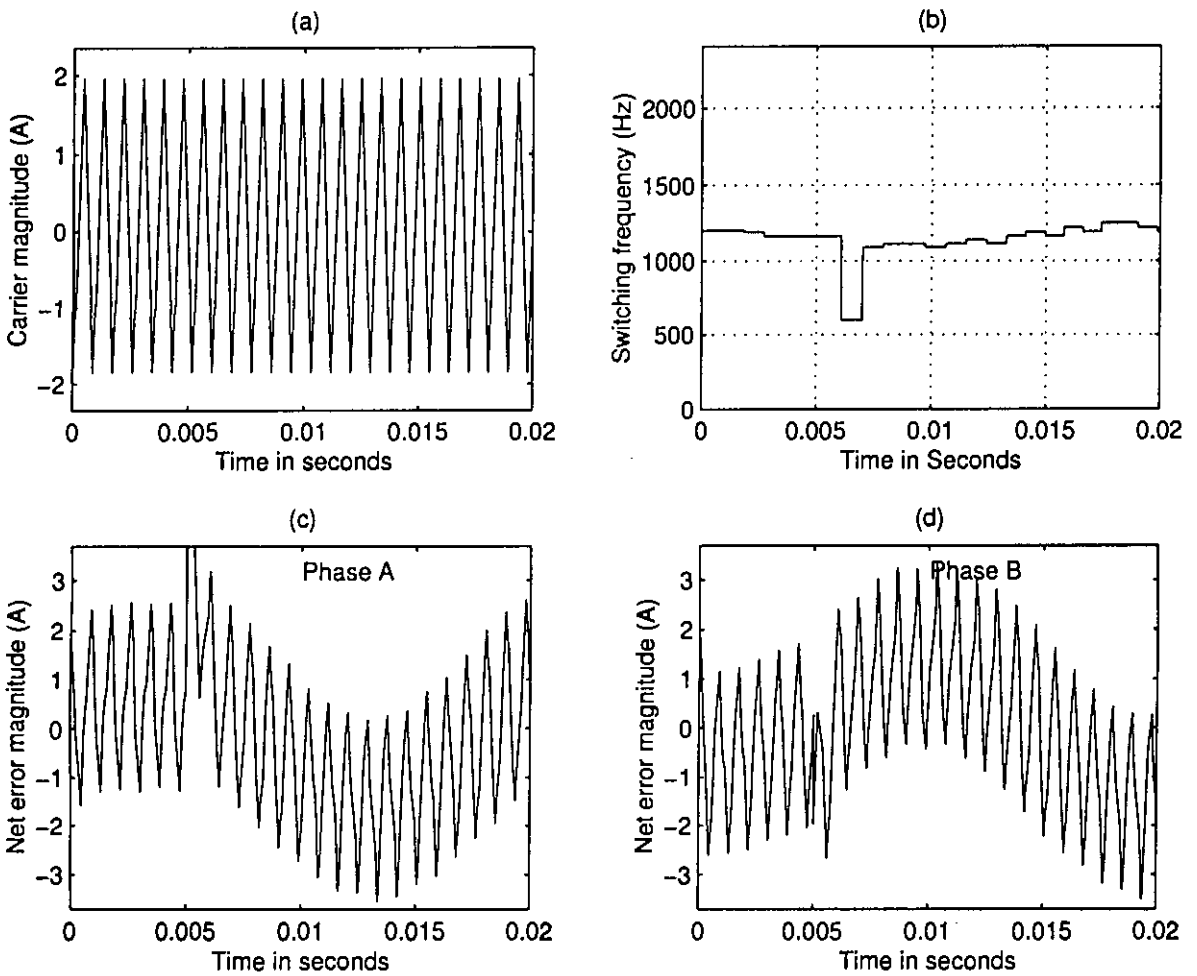

Fig. 2.17: Dynamic response of the Programmed Ramp Comparison Controller (PRC) with $f = 50Hz$, $R = 8\Omega$, $L = 19.1mH$, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$ to $10A$ at 90^0: (a) Ramp waveform , (b) Switching frequency distribution over the fundamental period, (c) Net error signal for phase A prior to comparator, (d) Net error signal for phase B prior to comparator.

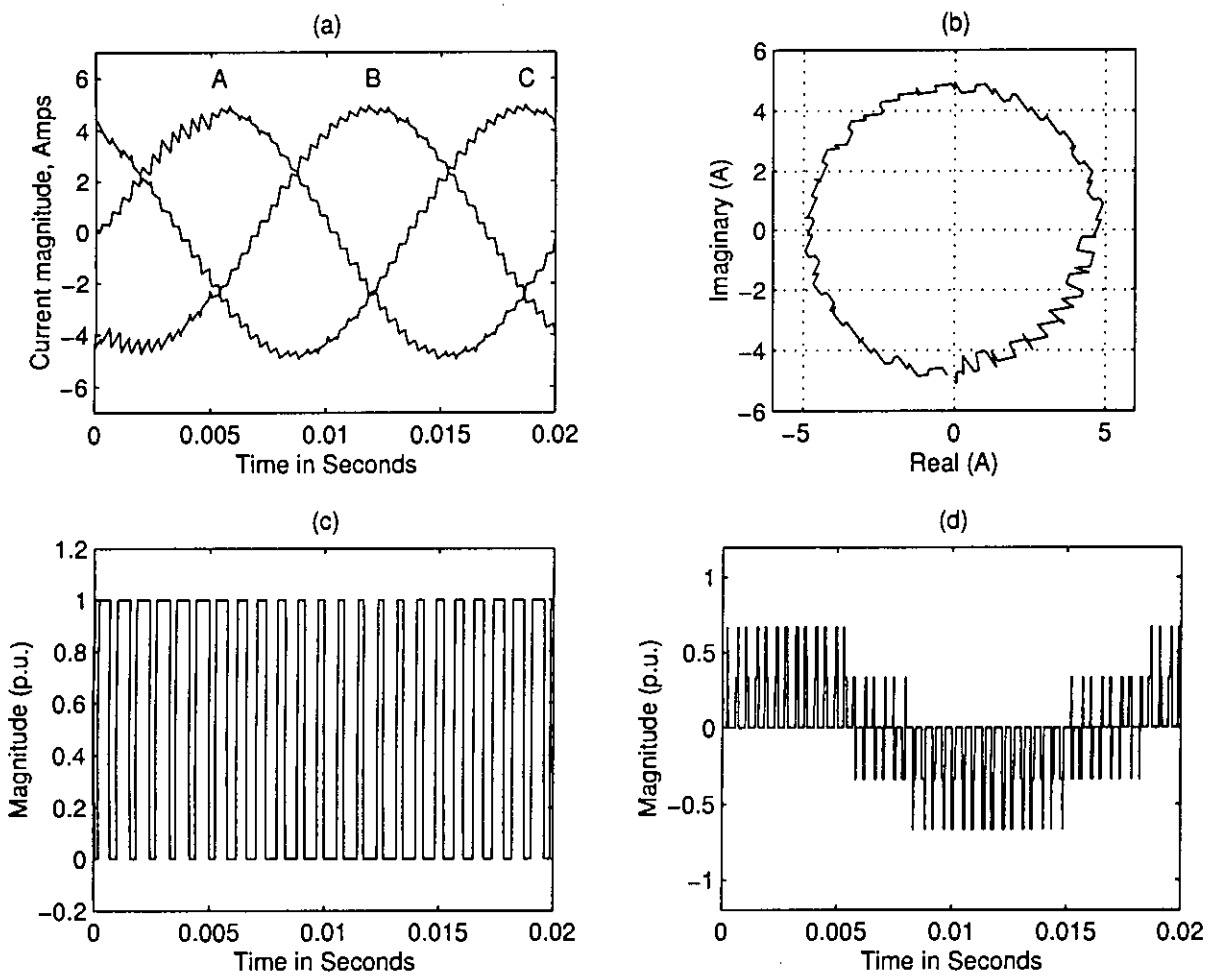

Fig. 2.18: Dynamic response of the Programmed Ramp Comparison Controller (PRC) with $f = 50Hz$, $R = 8\Omega$ to 4Ω at 90^0, $L = 19.1mH$ to $28.2mH$ at 90^0, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$: (a) Load current waveforms for phases A, B and C , (b) Combined current vector in complex plane , (c) PWM switching pattern for switch Q_1 , (d) Line to neutral voltage waveform of phase A in p.u.

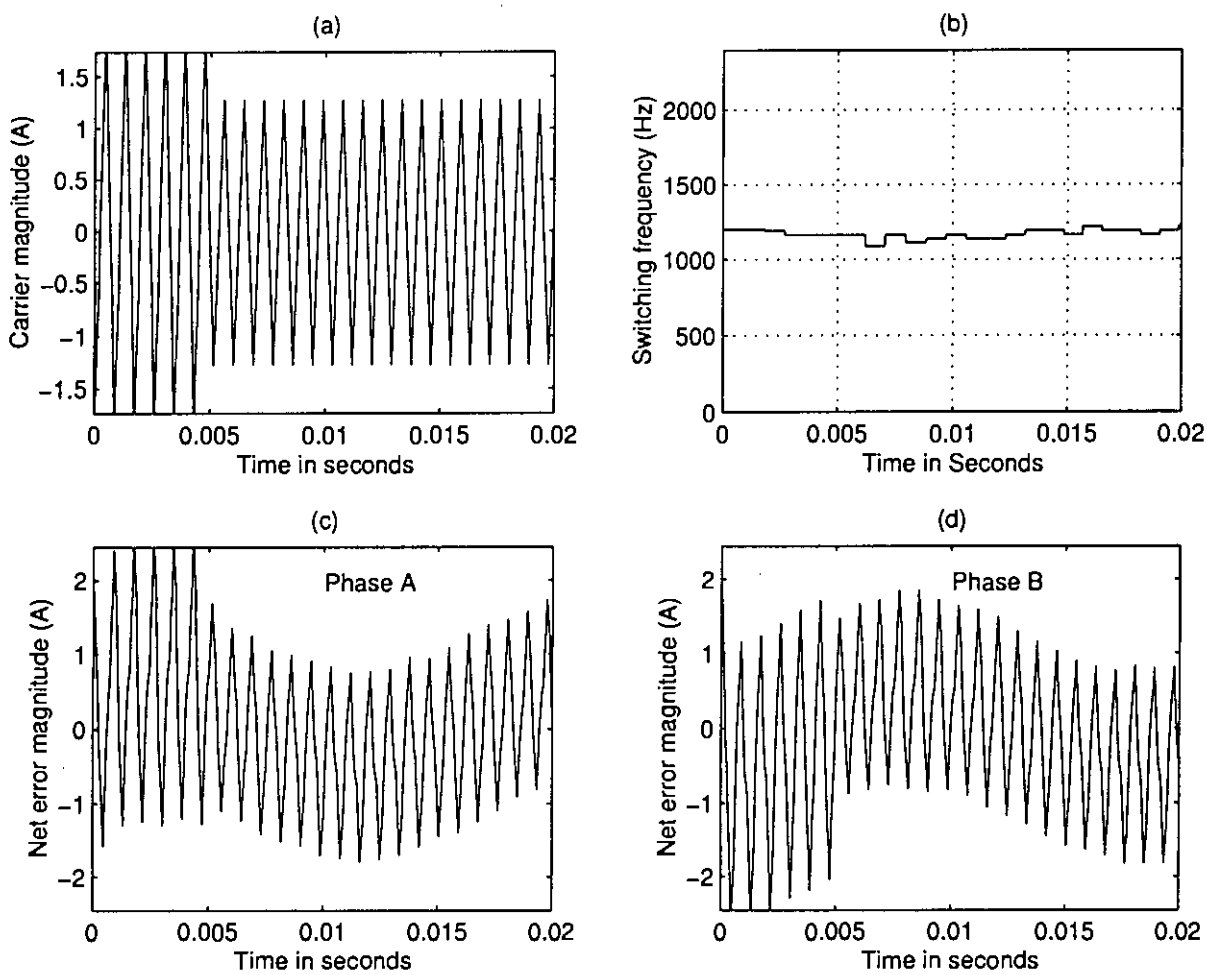

Fig. 2.19: Dynamic response of the Programmed Ramp Comparison Controller (PRC) with $f = 50Hz$, $R = 8\Omega$ to 4Ω at 90^0, $L = 19.1mH$ to $28.2mH$ at 90^0, $f_s = 1200Hz$, $V_s = 240V$, $I_m^* = 5A$: (a) Ramp waveform , (b) Switching frequency distribution over the fundamental period, (c) Net error signal for phase A prior to comparator, (d) Net error signal for phase B prior to comparator.

2.4 Performance Comparison of AMPRC and PRC with HCC

A comparative analysis is presented in this section showing the improvement of AMPRC and PRC over HCC from performance point of view. The performances are studied for a common peak current ripple of 0.65A (load current fundamental peak value = 5A). A performance comparison table is given in 2.1, which shows that for the same peak current ripple the AMPRC, PRC and HCC have THD of 0.0515, 0.0492 and 0.0565 respectively. For HCC the current ripple is constant (0.65A) over the fundamental period. But for both AMPRC and PRC the current ripple is not constant. In both cases the average peak current ripple is less than 0.65A. For this reason the THD is less in case of AMPRC and PRC.

Table 2.1: PERFORMANCE COMPARISON BETWEEN PRC AND HCC FOR OPERATION WITH A THREE PHASE INVERTER WITH STAR CONNECTED LOAD HAVING $V_s = 240$V, R = 8 Ω, L = 0.0191H, $f = 50$Hz AND $I_m = 5$A.

Controller	HCC	AMPRC	PRC
Load Current Ripple (Maximum)	0.65	0.65	0.65
THD	0.0565	0.0515	0.0492
Maximum Switching Frequency	3.93kHz	1218Hz	1218Hz
Minimum Switching Frequency	404Hz	1055Hz	1150Hz

It is seen from Table 2.1 that the maximum and minimum switching frequencies of HCC are 3.93kHz and 404Hz respectively. It clearly shows that the switching frequency of HCC is extremely non-uniform. The switching frequency distribution over one fundamental period is shown in Fig. 2.20. As seen from Fig. 2.20, the switching frequencies of AMPRC and PRC are almost uniform (1200Hz) and overlaps each other.

Table 2.1 shows that the performance of PRC is better than AMPRC. This happens because the analysis presented in this thesis is based on single phase. In case of three phase three wire system, the current in any of the phases depends on the switching

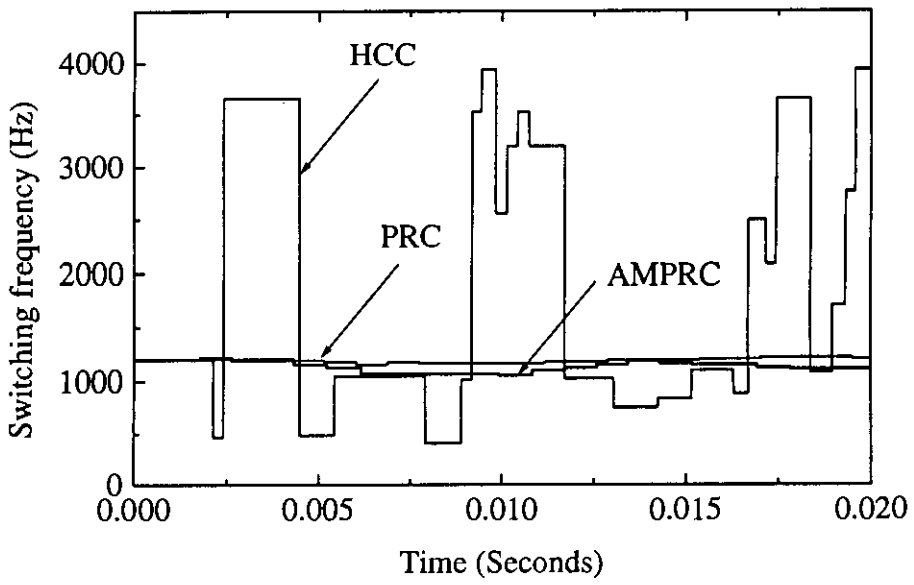

Fig. 2.20: Switching frequency distribution of PRC and HCC over a fundamental period for operation with a three phase inverter with star connected load having V_s = 240V, R = 8 Ω, L = 0.0191H, f = 50Hz and I_m = 5A.

conditions of other phases and may deviate from the single phase. This interdependence of the three phase switching condition have a greater effect on AMPRC when compared to PRC. For this reason the THD of PRC is lower than the THD of AMPRC.

For single phase applications or, three phase applications having the neutral connected to the mid point of the supply source, the AMPRC would definitely perform better than PRC. For this reason AMPRC is recommended for single phase applications and the PRC is recommended for three phase inverters having neutral insulated loads.

2.5 Conclusion

A detailed analysis of HCC is made in this chapter. Earlier researchers intuitively added a triangular carrier in the feedback path of conventional HCC for uniform switching frequency operation and called it Ramp Comparison Controller (RCC). Because of the lack

of analytical basis, the amplitude and slope of the add-on function (triangular carrier) was unknown. Because of improper amplitude and slope selection, the RCC occasionally found to give high frequency switching in some operating points. This drawback is removed in this chapter by establishment of an analytical basis for the add-on function. Analytical model is proposed for the amplitude and slope of the add-on function which are functions of the load parameters, carrier frequency and the dc supply voltage.

Two improved current controllers results from the analytical model. They are: (1) Amplitude Modulated Programmed Ramp Comparison Controller (AMPRC) and, (2) Programmed Ramp Comparison Controller (PRC).

In the AMPRC an amplitude modulated triangular carrier is computed from the supply voltage V_s, and $R - L$ parameters of the load. The carrier is added to the feedback path of the controller to maintain an uniform switching frequency during the steady state and dynamic state of operation. The PRC is a simplified version of AMPRC and is found to perform better than the AMPRC. In PRC the maximum amplitude of the modulated carrier is applied to the feedback path during the whole operating period. Detailed mathematical analysis and simulation results of the proposed current controllers are presented in this chapter. Both the controllers discussed have good steady state and dynamic responses.

Chapter 3

Improvement of Conventional Predictive Current Controllers by Imposing New Constraint

3.1 Introduction

Predictive current controllers are field oriented schemes and are intended for ac drive applications. The design methodologies require information about motor speed, shaft position, flux vector and motor phase currents. Hence, overall scheme is complicated in nature. Moreover, the dynamic performance is reported to be not good. This happens because motor speed and shaft position are not accurately reflected during dynamic states because of large time constants. Different types of predictive controllers are found in the literature [49-53]. Attempts have been made by different research groups to improve the dynamic performance [54, 55, 90]. It is observed that the dynamic performance can be improved by using the load current derivative into consideration. But these methods are subjected to instability in digital implementation schemes.

In this chapter, a predictive controller is designed with equivalent R-L parameters. The equivalent R-L parameters always reflect the load condition. Thus, the new design improves the dynamic response and also allows predictive controllers for general purpose use. During large disturbances conventional predictive controllers give high current over-

shoots and may become unstable. A thorough examination of the conventional predictive controllers show that the current overshoots are caused due to erratic voltage vector that results from the analytical calculations. In the new design, this problem is overcome by introducing a limiter in the voltage vector.

Two methods of voltage vector computation are proposed: The first one computes the voltage vector from feedback currents and the second one computes the voltage vector from reference currents only.

Section 3.2 of this chapter gives detailed mathematical analysis of the improved predictive controller. Typical simulation results for steady state and dynamic response of the controllers are given in section 3.5.

3.2 Analysis of Predictive Current Controller with equivalent R-L load

The inverter circuit shown in Fig. 2.1 is redrawn for a neutral unconnected load as shown in Fig. 3.1. The concept of voltage and current space vectors are used to represent a set of three phase voltages and currents. For a three phase system, the reference currents are defined by

$$i_a^* = I_m \sin(\omega t) \tag{3.1a}$$

$$i_b^* = I_m \sin\left(\omega t - \frac{2\pi}{3}\right) \tag{3.1b}$$

$$i_c^* = I_m \sin\left(\omega t - \frac{4\pi}{3}\right) \tag{3.1c}$$

where i_a^* , i_b^*, i_c^* are the reference currents for Phases A, B, C and ω is the angular frequency, given by $\omega = 2\pi f$.

Equations (3.1a)–(3.1c) can be written in numerical form as

$$i_a^*(n) = I_m \sin(2\pi f n T_s) \tag{3.2a}$$

$$i_b^*(n) = I_m \sin\left(2\pi f n T_s - \frac{2\pi}{3}\right) \tag{3.2b}$$

$$i_c^*(n) = I_m \sin\left(2\pi f n T_s - \frac{4\pi}{3}\right) \tag{3.2c}$$

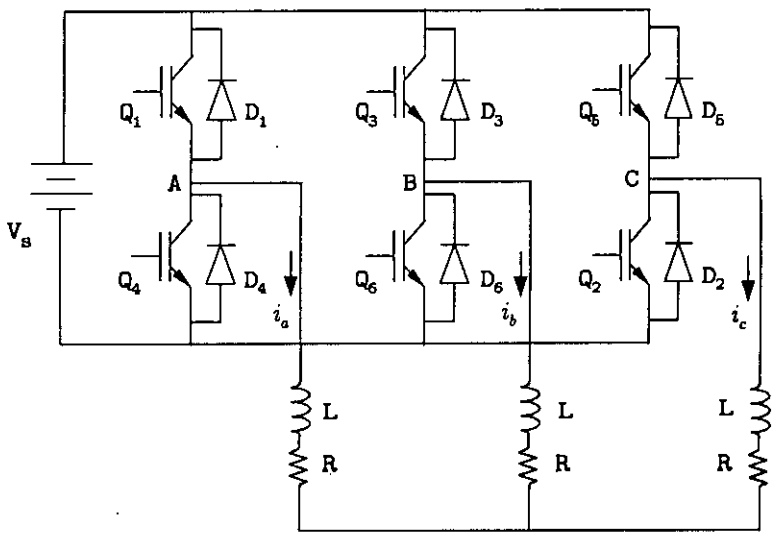

Fig. 3.1: Three phase inverter with neutral unconnected star load.

where T_s is the sampling interval and n is the sample number.

The reference current vector at the n^{th} sampling instant $i^*(n)$ and the load current vector $i(n)$ are defined by,

$$i^*(n) = \frac{2}{3}\left[i_a{}^*(n) + a i_b{}^*(n) + a^2 i_c{}^*(n)\right] \tag{3.3}$$

$$i(n) = \frac{2}{3}\left[i_a(n) + a i_b(n) + a^2 i_c(n)\right] \tag{3.4}$$

where, $a = e^{j2\pi/3}$.

Taking $i_a{}^*(n)$ as the reference, the reference current vectors and the load current vectors can be resolved in direct and quadrature axes components as follows:

$$\begin{aligned} i^*(n) &= \frac{2}{3}\left[i_a{}^*(n) + i_b{}^*(n)\left(\cos\frac{2\pi}{3} + j\sin\frac{2\pi}{3}\right) + i_c{}^*(n)\left(\cos\frac{4\pi}{3} + j\sin\frac{4\pi}{3}\right)\right] \\ &= \frac{2}{3}\left[\left\{i_a{}^*(n) - 0.5\left[i_b{}^*(n) + i_c{}^*(n)\right]\right\} + j\left\{\frac{\sqrt{3}}{2}\left[i_b{}^*(n) - i_c{}^*(n)\right]\right\}\right] \end{aligned} \tag{3.5}$$

For neutral unconnected load $i_a{}^*(n) + i_b{}^*(n) + i_c{}^*(n) = 0$. Hence (3.5) can further be simplified as,

$$i^*(n) = i_a{}^*(n) + j\frac{1}{\sqrt{3}}\left\{i_a{}^*(n) + 2i_b{}^*(n)\right\} \tag{3.6}$$

Similarly the load current vector $i(n)$ can be shown to be,

$$i(n) = i_a(n) + j\frac{1}{\sqrt{3}}\{i_a(n) + 2i_b(n)\} \tag{3.7}$$

The inverter voltage space vector $V(n)$ is defined as a combination of the phase voltages v_{an}, v_{bn} , v_{cn} as,

$$V(n) = \frac{2}{3}\left[v_{an}(n) + av_{bn}(n) + a^2v_{cn}(n)\right] \tag{3.8}$$

For inverter operation in *two levels* any one switch is *ON* from each leg of the inverter. The switching states of the inverter legs for phases A, B and C are represented by S_A , S_B and S_C respectively. Referring to Fig. 3.1, a '1' state means the upper switch of the leg is *ON* while the '-1' state means that the lower switch is *ON*. The inverter can have $(2^3 = 8)$ operating states resulting eight voltage vectors as shown in Table 3.1.

Table 3.1: INVERTER SWITCHING STATES AND DOMINANT VOLTAGE VECTORS.

Number	S_C	S_B	S_A	Leg C	Leg B	Leg A	Voltage Vector
0	-1	-1	-1	Q_2	Q_6	Q_4	V_0
1	-1	-1	1	Q_2	Q_6	Q_1	V_1
2	-1	1	-1	Q_2	Q_3	Q_4	V_3
3	-1	1	1	Q_2	Q_3	Q_1	V_2
4	1	-1	-1	Q_5	Q_6	Q_4	V_5
5	1	-1	1	Q_5	Q_6	Q_1	V_6
6	1	1	-1	Q_5	Q_3	Q_4	V_4
7	1	1	1	Q_5	Q_3	Q_1	V_7

The eight voltage vectors that correspond to eight switching states of the inverter are shown in Fig. 3.2. There are six active states $V_1 - V_6$ and two free-wheeling or zero states V_0 & V_7. The active voltage vectors are of length $2V_s/3$ and form a hexagon as shown in Fig. 3.2. The vectors divide the plane into six sectors each of 60^0 angular span.

The motor current vector is controlled by one controller instead of three independent controllers. The currents are sampled at a constant rate and are synchronized to the

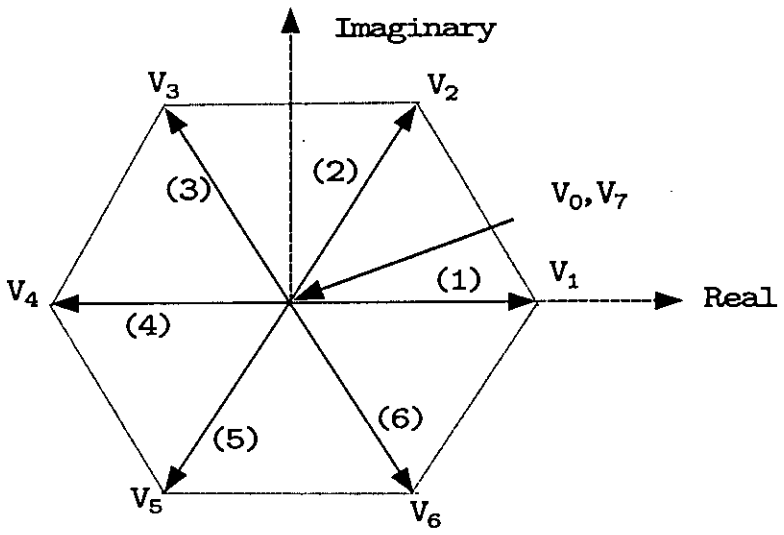

Fig. 3.2: Voltage vectors of a three phase inverter in the complex plane.

fundamental reference current signal. An appropriate voltage vector is calculated in each sampling instant for current tracking. The desired voltage vectors can be calculated using two different methods. In the first method the voltage vector is computed from the feedback currents and the load parameters. In the second method the voltage vector is computed from the equivalent load parameters and the sinusoidal current reference only.

3.2.1 Method 1: Vector Prediction Based on Load Parameters and Feedback Currents

In this method, the load current vector is calculated and compared to the reference current vector. An appropriate voltage vector that would reduce the current error vector $i^* - i$ to zero is calculated.

For $R-L$ loads as shown in Fig. 3.1, the voltage space vector at the n^{th} sampling instant $V(n)$ can be evaluated in numerical form as,

$$V(n) = Ri(n) + \left(\frac{L}{T_s}\right)\{i^*(n+1) - i(n)\} \tag{3.9}$$

where $i^*(n+1)$ is the reference current vector for the $(n+1)^{th}$ sample, $i(n)$ is the load current vector at the n^{th} sampling instant and T_s is the sampling interval. The selection

of inverter switching states is dependent on the magnitude and phase of the voltage vector $V(n)$ as shown in Table 3.2. Vector (3.9) can be expressed as real and imaginary parts written in terms of a , b , c. The real part of $V(n)$ can be obtained as,

$$\Re[V(n)] = \Re[Ri(n)] + \Re\left[\left(\frac{L}{T_s}\right)\{i^*(n+1) - i(n)\}\right] \tag{3.10}$$

Equating the real part of reference and load current vectors from (3.6) and (3.7), and putting their values in (3.10) yields,

$$\Re[V(n)] = Ri_a(n) + \left(\frac{L}{T_s}\right)\{i_a{}^*(n+1) - i_a(n)\} \tag{3.11}$$

The imaginary part of the voltage vector can be written as,

$$\Im[V(n)] = \Im[Ri(n)] + \Im\left[\left(\frac{L}{T_s}\right)\{i^*(n+1) - i(n)\}\right] \tag{3.12}$$

Equating the imaginary part of reference and load current vectors from (3.6) and (3.7), and putting their values in (3.12) yields,

$$\Im[V(n)] = R\left[i_a(n) + 2i_b(n)\right] + \left(\frac{L}{T_s}\right)\left[i_a{}^*(n+1) + 2i_b{}^*(n+1) - i_a(n) - 2i_b(n)\right] \tag{3.13}$$

3.2.2 Method 2: Vector Prediction Based on Load Parameters and Reference Current

In this method a voltage vector $V(n)$ is computed at the n^{th} sampling instant so that it forces the load current vector i^* to go from $i^*(n)$ to $i^*(n+1)$. Using this criteria (3.9) can be rewritten in the form

$$V(n) = Ri(n) + \left(\frac{L}{T_s}\right)\{i^*(n+1) - i^*(n)\} \tag{3.14}$$

Vector (3.14) can be expressed as real and imaginary parts written in terms of a , b , c. The real part of $V(n)$ can be obtained as

$$\Re[V(n)] = \Re[Ri(n)] + \Re\left[\left(\frac{L}{T_s}\right)\{i^*(n+1) - i^*(n)\}\right] \tag{3.15}$$

Equating the real part of reference current vector from (3.6) and putting its value in (3.15) yields

$$\Re[V(n)] = Ri_a(n) + \left(\frac{L}{T_s}\right)\{i_a{}^*(n+1) - i_a^*(n)\} \tag{3.16}$$

The imaginary part of the voltage vector can be written as

$$\Im[V(n)] = \Im[Ri(n)] + \Im\left[\left(\frac{L}{T_s}\right)\{i^*(n+1) - i^*(n)\}\right] \tag{3.17}$$

Equating the imaginary part of reference current vector from (3.6) and putting its value in (3.17) yields

$$\Im[V(n)] = R[i_a(n) + 2i_b(n)] + \left(\frac{L}{T_s}\right)[i_a{}^*(n+1) + 2i_b{}^*(n+1) - i_a^*(n) - 2i_b^*(n)] \tag{3.18}$$

3.2.3 Modulation Process

The voltage vector $V(n)$ calculated by either method (method 1 or method 2) can be used for the modulation process to determine the switching table and their durations. The modulation process needs amplitude and phase angle of the vector $V(n)$ which can be calculated as

$$|V(n)| = \sqrt{\{\Re[V(n)]\}^2 + \{\Im[V(n)]\}^2} \tag{3.19}$$

$$\angle V(n) = \tan^{-1}\left\{\frac{\Im[V(n)]}{\Re[V(n)]}\right\} \tag{3.20}$$

Table 3.2: SWITCHING STATES AND ACTIVE VOLTAGE VECTORS IN DIFFERENT SECTORS OF THE COMPLEX PLANE

Sector	Active Voltages	S_C	S_B	S_A
1	V_1, V_2	-1	-1/1	1
2	V_2, V_3	-1	1	1/-1
3	V_3, V_4	-1/1	1	-1
4	V_4, V_5	1	1/-1	-1
5	V_5, V_6	1	-1	-1/1
6	V_6, V_1	1/-1	-1	1

The conduction time of inverter switches are modulated according to the amplitude and angle of $V(n)$. The angle of $V(n)$ evaluated from (3.20) permits determination of the sector of the complex plane, where, the vector $V(n)$ lies. To compute the contribution of

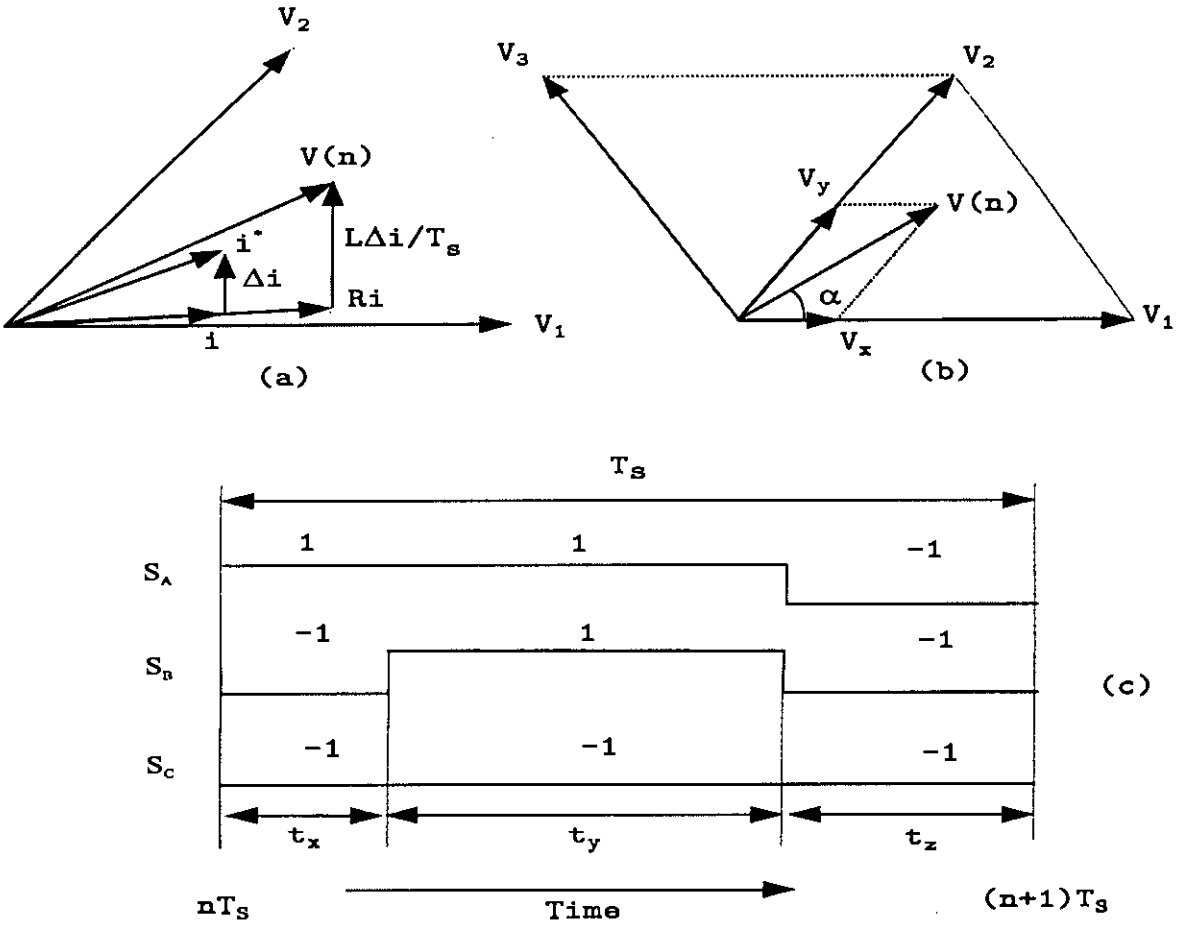

Fig. 3.3: Predictive current control scheme (a) Detailed vector diagram, (b) Vector diagram showing projection of a typical vector $V(n)$ on the inverter state vectors V_1 and V_2 , (c) A computation example showing switching states during a sampling interval, T_s.

the appropriate inverter vectors in any sector, it is required to know the position of the rotating voltage vector from the adjacent right arm inverter vector. This angular position of the rotating space vector may be called the modulation angle α as shown in Fig. 3.3(b). It can be evaluated from

$$\angle V(n) = (p-1)\frac{\pi}{3} + \alpha \tag{3.21}$$

$$\alpha = \angle V(n) - (p-1)\frac{\pi}{3} \tag{3.22}$$

where p is the sector number as identified in Fig. 3.2 and α is the modulation angle. The active voltages and switches for modulation are determined from Table 3.2. Since the

inverter can take one of the eight conduction states, pulse width modulation can be used to provide the voltage vector $V(n)$. In the example shown in Fig. 3.3(b), the inverter is switched from V_1 to V_2 with the duty cycle determined by the values of V_x and V_y . By referring to Fig. 3.3(b),

$$\begin{aligned} & V_y \sin(60^0) && = V(n)\sin(\alpha) \\ \text{or,} \quad & V_y && = \frac{2}{\sqrt{3}}|V(n)|\sin\alpha \qquad (3.23) \\ \text{and} \quad & V_x + V_y\cos(60^0) && = |V(n)|\cos(\alpha) \\ \text{or,} \quad & V_x && = |V(n)|\cos\alpha - 0.5V_y \qquad (3.24) \end{aligned}$$

For two level PWM, V_x and V_y can have a maximum magnitude of $2V_s/3$. Hence the time duration of the states V_1 , V_2 and V_0 are given by

$$\begin{aligned} t_x &= \frac{V_x}{2V_s/3}T_s \\ &= 1.5\left(\frac{V_x}{V_s}\right)T_s \qquad (3.25) \end{aligned}$$

$$\begin{aligned} t_y &= \frac{V_y}{2V_s/3}T_s \\ &= 1.5\left(\frac{V_y}{V_s}\right)T_s \qquad (3.26) \\ t_z &= T_s - t_x - t_y \qquad (3.27) \end{aligned}$$

where V_s is the dc input voltage. With the condition $t_x+t_y+t_z = T_s$, the obtainable voltage vector resides inside the hexagon formed by the six active voltage vectors corresponding to six active states of the inverter. The controller is operated in two level PWM mode during the active states (t_x and t_y periods) and all three phases are inactive (freewheeling state) during t_z period. The inverter switching for a particular voltage vector $V(n)$ are assigned according to Table 3.3. The inverter switches are operated according to their state assignments. The state '1' means the upper switch is conducting, state '-1' means the lower switch is conducting.

Table 3.3: STATE ASSIGNMENT OF INVERTER SWITCHES FOR TWO LEVEL PWM AT DIFFERENT SECTORS OF THE VOLTAGE VECTOR $V(n)$ AND TIME ZONES.

Time Zone	Sector	S_A	S_B	S_C	V_{an}	V_{bn}	V_{cn}
t_x	1	1	-1	-1	$2V_s/3$	$-V_s/3$	$-V_s/3$
t_x	2	1	1	-1	$V_s/3$	$V_s/3$	$-2V_s/3$
t_x	3	-1	1	-1	$-V_s/3$	$2V_s/3$	$-V_s/3$
t_x	4	-1	1	1	$-2V_s/3$	$V_s/3$	$V_s/3$
t_x	5	-1	-1	1	$-V_s/3$	$-V_s/3$	$2V_s/3$
t_x	6	1	-1	1	$V_s/3$	$-2V_s/3$	$V_s/3$
t_y	1	1	1	-1	$V_s/3$	$V_s/3$	$-2V_s/3$
t_y	2	-1	1	-1	$-V_s/3$	$2V_s/3$	$-V_s/3$
t_y	3	-1	1	1	$-2V_s/3$	$V_s/3$	$V_s/3$
t_y	4	-1	-1	1	$-V_s/3$	$-V_s/3$	$2V_s/3$
t_y	5	1	-1	1	$V_s/3$	$-2V_s/3$	$V_s/3$
t_y	6	1	-1	-1	$2V_s/3$	$-V_s/3$	$-V_s/3$
t_z	1-6	-1	-1	-1	0	0	0

3.3 Improvement of Dynamic Performance

The poor dynamic performance of conventional predictive controllers is due to the inaccuracy in the evaluation of the voltage vector during large disturbances. This happens due to the involvement of the derivative term in the computation of the voltage vector. In case of sudden change in reference current or in the load impedance, the derivative term overshoots. The predictive controller responds very fast and it causes the shoot through current to go beyond the recommended limit. The shoot through current can be limited if one can slow down the response of the predictive controller in dynamic states.

In the proposed controller, the response time is made slower by reducing the voltage supply to the load. To achieve this a voltage vector limiter is proposed to be added to the conventional predictive controller that would work when critical dynamic states are detected. Critical dynamic states are those dynamic states that result unacceptable

current overshoots. Critical dynamic states are determined from the magnitude of the computed voltage vector. When the voltage vector exceeds $2V_s/3$, then it is considered as a critical dynamic state. With the introduction of the vector limiter in critical dynamic states, the time response would be slower, but the shoot through current would be low.

3.4 Proposed Controller Scheme

The proposed controller is implemented using the scheme as shown in Fig. 3.4. The scheme has four major building blocks. The sine wave generator block generates sinusoidal reference currents i_a^* and i_b^* at 120^0. The frequency and amplitude commands are externally given. In case of dynamic loads (like induction motors) pre-calculated standstill load parameters are stored in the **load parameter estimation** block. Major computations are done in the **voltage vector calculation** block. Two phase currents (i_a and i_b) and two phase voltages (v_{an} and v_{bn}) are used along with the two phase reference currents (i_a^* and i_b^*) to calculate the voltage vector as well as the load parameters $R - L$.

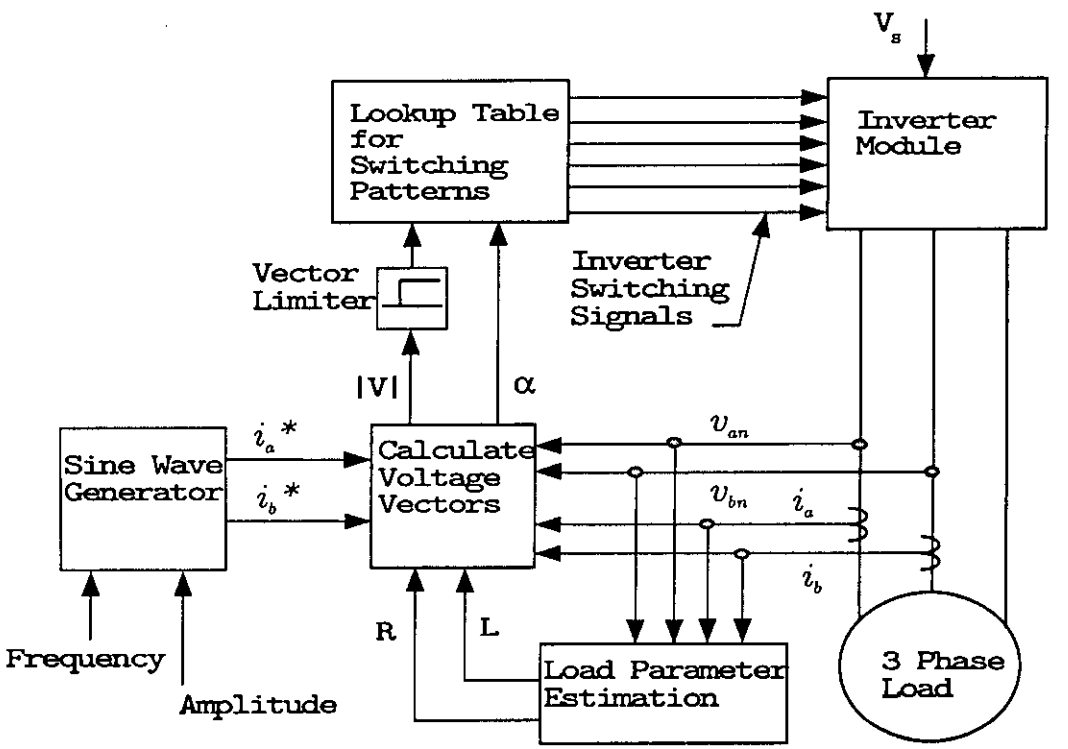

Fig. 3.4: Proposed predictive controller scheme for 3 phase VSI and star connected load.

For the running condition, the load parameters are evaluated from the fundamental component of the phase voltage and phase current (details in section 4.6.2). The voltage vector, its phase angle and position in the complex plane (Fig. 3.2) are calculated from (3.19)-(3.20). The modulation angle α is evaluated using (3.22). The pulse widths are determined from (3.25)-(3.27). Then the switching patterns are selected from the lookup tables. Table 3.3 is used for selection of the switching pattern.

3.5 Performance Study

The performance of the improved predictive current controller are studied by simulation. The initial values of the equivalent R and L parameters for the controller are obtained from the fundamental voltage, load current, frequency and power factor as follows:

$$Z = \frac{V_m}{I_m} \tag{3.28}$$

$$\theta = \cos^{-1}(p_f) \tag{3.29}$$

$$R = Z\cos\theta \tag{3.30}$$

$$L = \frac{Z\sin\theta}{2\pi f} \tag{3.31}$$

where V_m is the peak value of fundamental phase voltage, I_m is the peak value of the fundamental phase current, p_f is the power factor of the load, Z is the impedance and f is the fundamental frequency. Typical simulation results are shown in Figs. 3.5-3.12. The simulation is done for a three phase star connected R-L load with neutral not connected. The simulation parameters are shown in Table 3.4. The response of the proposed predictive current controller are studied for different operating conditions. Simulation outputs of the three phase load current waveform, overall current vector in complex plane, switching patterns of Q_1, Q_3 and load current spectrum are recorded. Performances are studied for alternate methods of voltage vector computations.

3.5.1 Space Voltage Vector Computed by Method 1

Figures 3.5-3.11 show the steady state, startup and dynamic responses of the proposed predictive controller when the voltage vector is computed using Method 1. As evident from

Table 3.4: LOAD PARAMETERS USED FOR SIMULATION OF THE PROPOSED PREDICTIVE CONTROLLER

Resistance per phase, $R = 8\Omega$	Inductance per phase, $L = 19.1$ milli-henry
Fundamental frequency, $f = 50$ hertz	Switching frequency, $f_s = 1200$ Hz
Inverter dc supply voltage, $V_s = 240$ volts	Reference current, $I_m^* = 5.0$ amps

the recorded waveforms and spectrum, the steady state, startup and dynamic response of the controllers are good. The dynamic response are studied for two separate cases. In the first case a step change in current reference is applied from 5A to 10A and in the second case a step change in load impedance is applied. In both cases the controller response is fast (Figs. 3.9 - 3.11) and no significant overshoots occur during the dynamic state.

3.5.2 Space Voltage Vector Computed by Method 2

Performance of the predictive controller are also studied using Method 2 for the computation of the voltage vector. Typical performance results at different operating conditions are shown in Figs. 3.6-3.12. The spectral data of the load current (for both methods) are shown in Table 4.1 for the first 25 harmonics. The individual harmonic contents in Method 2 are less than that of Method 1. The fundamental current magnitude (4.56A) in Method 2 is less than that (5.27A) in Method 1. Although the individual harmonic contents in Method 2 is less compared to Method 1, the total harmonic distortion in Method 2 (THD = 0.0865) is greater than that in Method 1 (THD = 0.0822). The overall performance of a controller is measured by the THD parameter, and hence Method 1 shows better performance than Method 2.

The startup response is faster in Method 1 compared to that in Method 2. The dynamic response in Method 1 is better than that in Method 2.

Method 2 is especially suitable for those applications, where the load impedance is fixed in nature and no feedback of load current is available.

Table 3.5: LOAD CURRENT SPECTRUM COMPARISON

Frequency component $\times f_0$	Magnitude (A) (Method 1)	Magnitude (A) (Method 2)
1	5.2717641e+000	4.5645819e+000
2	1.9825811e-002	1.0866202e-005
3	1.5290716e-002	7.9560236e-006
4	1.1982533e-002	6.1947732e-006
5	6.1238611e-002	7.8744040e-002
6	5.9628831e-003	4.2496764e-006
7	5.0726560e-002	2.4584255e-002
8	2.9291725e-003	3.2206858e-006
9	4.2374677e-003	2.8710418e-006
10	6.1118034e-003	2.5892819e-006
11	1.3292339e-002	9.3568956e-003
12	8.6927638e-003	2.1636250e-006
13	8.7726931e-003	7.7838600e-003
14	9.0104506e-003	1.8576535e-006
15	8.3934539e-003	1.7348726e-006
16	7.4314452e-003	1.6272732e-006
17	1.1224004e-002	8.0633434e-003
18	5.1266631e-003	1.4476255e-006
19	3.5087476e-002	1.1911147e-002
20	3.4011734e-003	1.3036521e-006
21	4.5788012e-003	1.2418871e-006
22	7.2819048e-003	1.1857074e-006
23	2.4665683e-001	2.3481727e-001
24	3.3018653e-003	1.0873305e-006
25	3.3806300e-001	3.0299545e-001

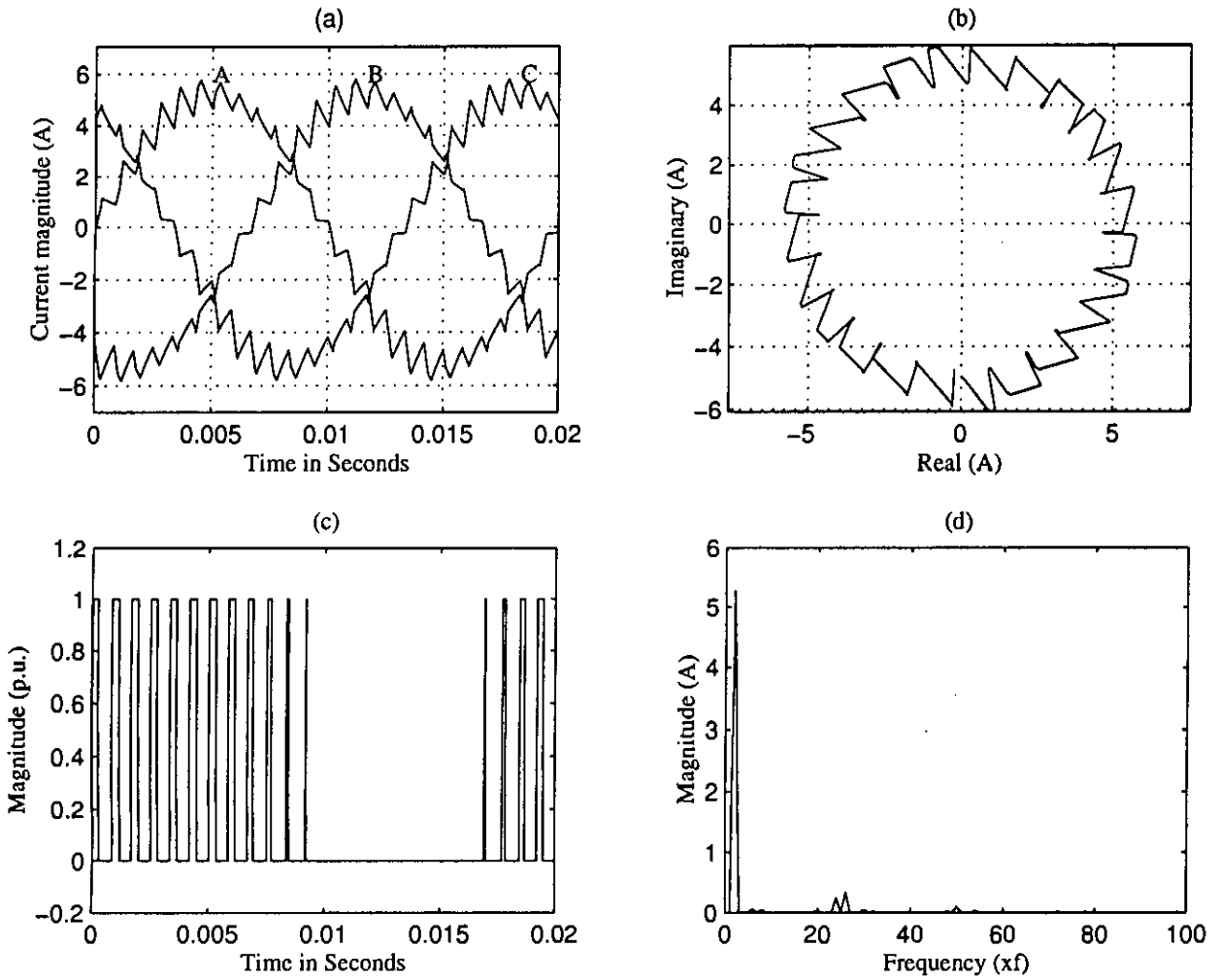

Fig. 3.5: Steady state response of the proposed predictive controller (**Method 1**) with R = 8Ω , L = 19.1mH, f = 50Hz, f_s = 1200Hz, I_m = 5A, V_s = 240V : (a) Load current waveforms, (b) Load current vector in complex plane, (c) PWM switching pattern for switch Q_1, (d) Load current spectrum.

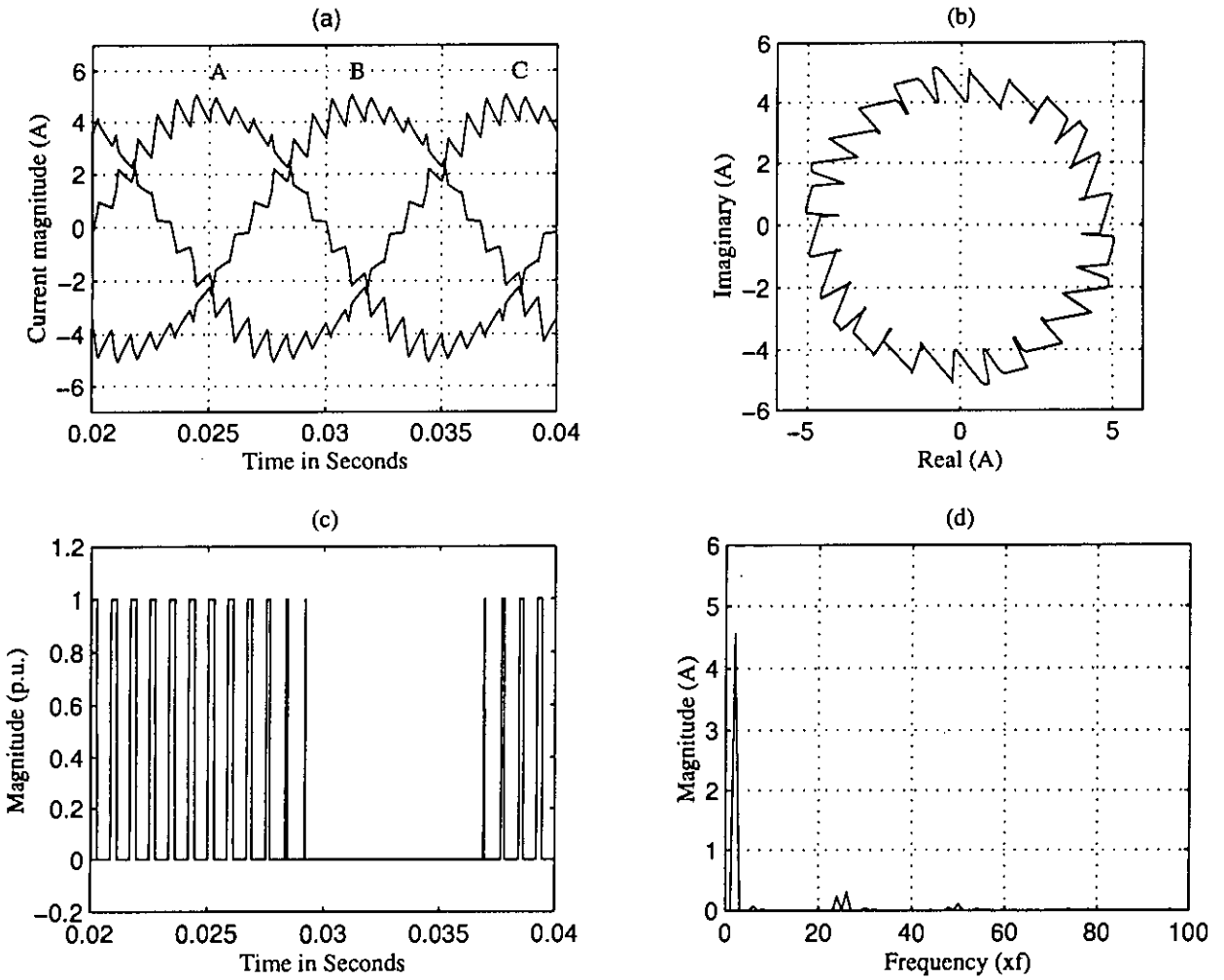

Fig. 3.6: Steady state response of the proposed predictive controller (**Method 2**) with R = 8Ω , L = 19.1mH, f = 50Hz, f_s = 1200Hz, I_m = 5A, V_s = 240V : (a) Load current waveforms, (b) Load current vector in complex plane, (c) PWM switching pattern for switch Q_1, (d) Load current spectrum.

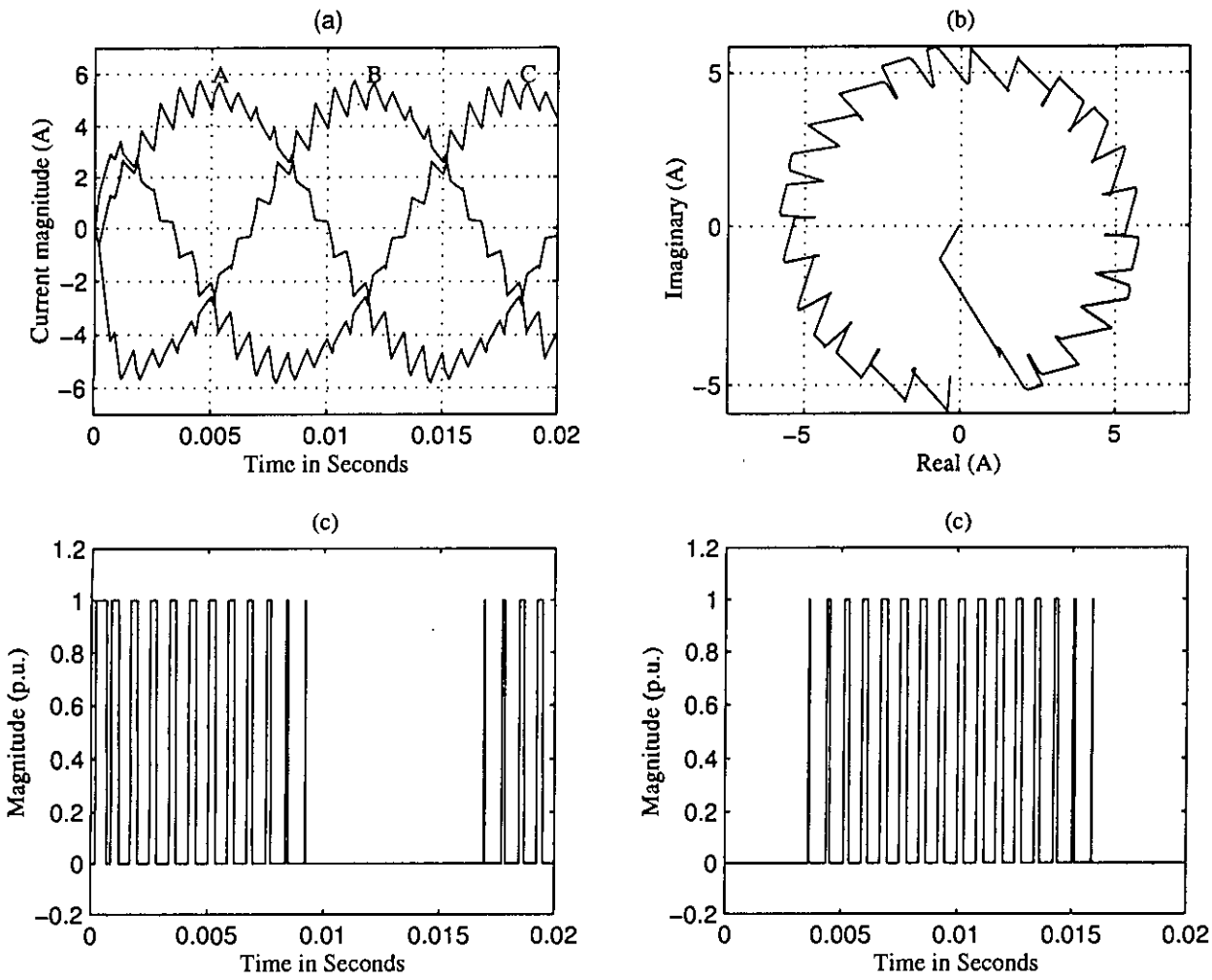

Fig. 3.7: Startup response of the proposed predictive controller (**Method 1**) with R = 8Ω , L = 19.1mH, f = 50Hz, f_s = 1200Hz, I_m = 5A, V_s = 240V : (a) Load current waveforms, (b) Load current vector in complex plane, (c) PWM switching pattern for switch Q_1, (d) PWM switching pattern for switch Q_3.

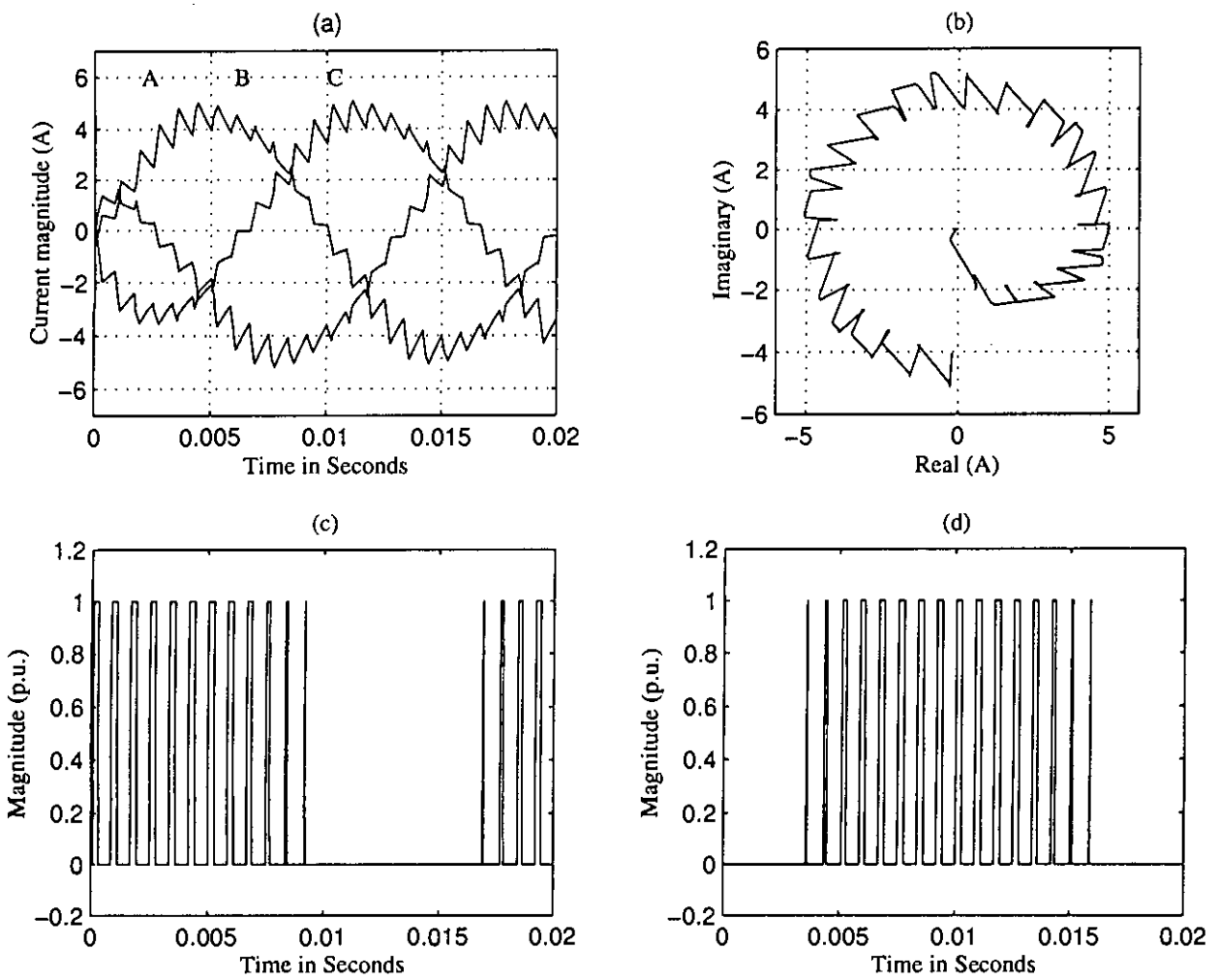

Fig. 3.8: Startup response of the proposed predictive controller (**Method 2**) with R = 8 Ω , L = 19.1mH, f = 50Hz, f_s = 1200Hz, I_m = 5A, V_s = 240V : (a) Load current waveforms, (b) Load current vector in complex plane, (c) PWM switching pattern for switch Q_1, (d) PWM switching pattern for switch Q_1.

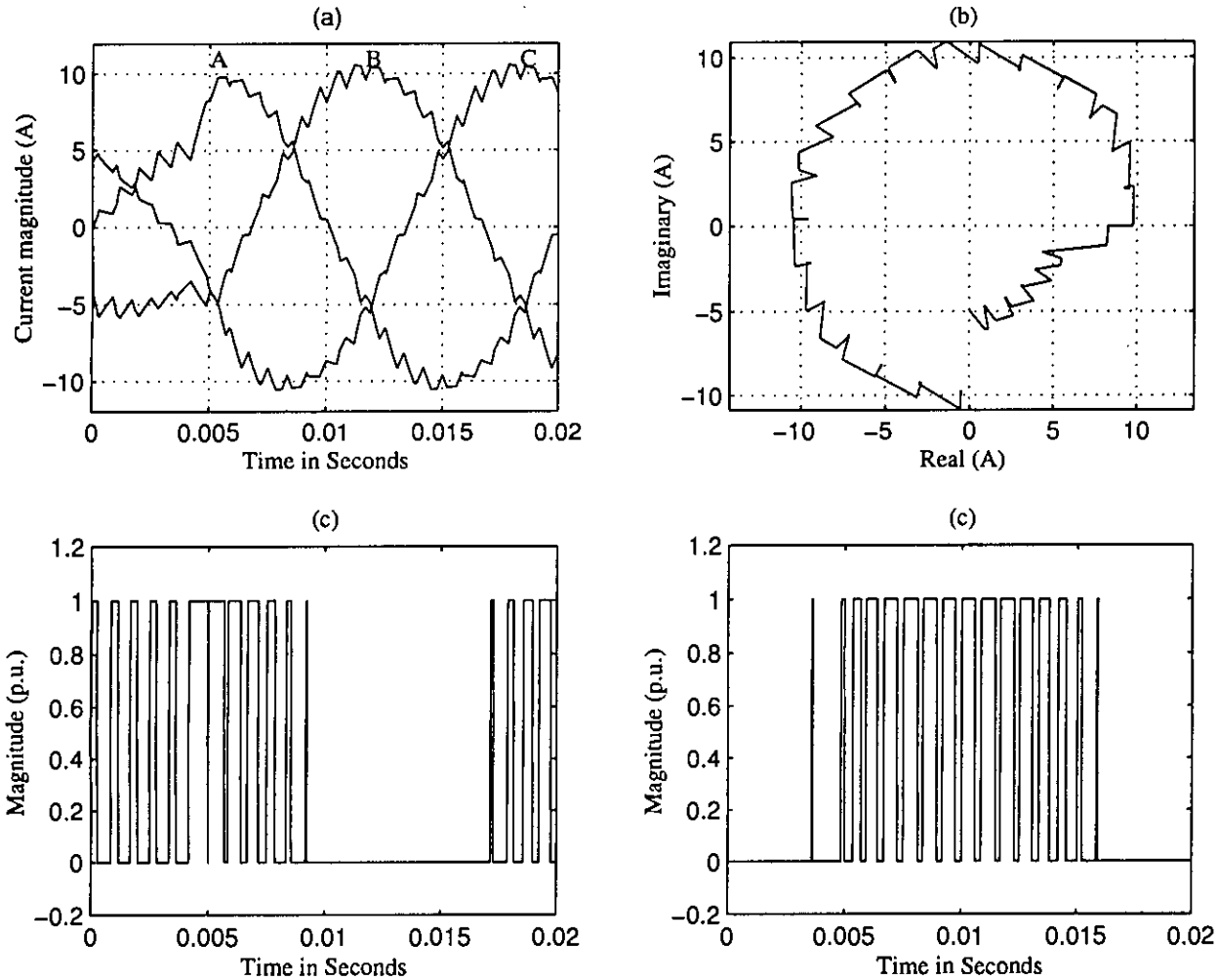

Fig. 3.9: Dynamic response of the proposed predictive controller (**Method 1**) for a step change in current reference by 200% (I_m = 5A to 10A) with R = 8 Ω , L = 19.1mH, f = 50Hz, f_s = 1200Hz, V_s = 240V : (a) Load current waveforms, (b) Load current vector in complex plane, (c) PWM switching pattern for switch Q_1, (d) PWM switching pattern for switch Q_3.

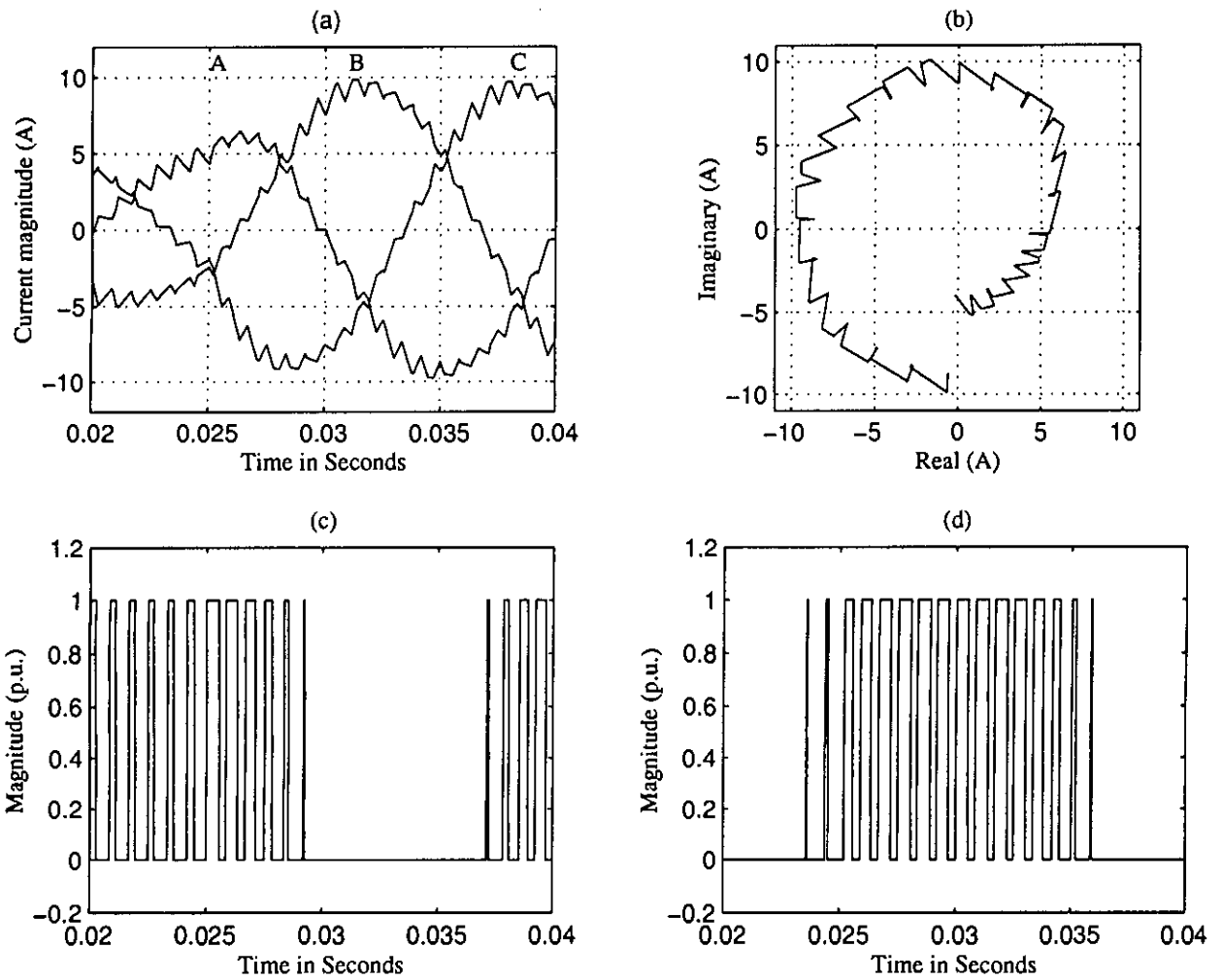

Fig. 3.10: Dynamic response of the proposed predictive controller (**Method 2**) for a step change in current reference by 200% (I_m = 5A to 10A) with R = 8 Ω , L = 19.1mH, f = 50Hz, f_s = 1200Hz, V_s = 240V : (a) Load current waveforms, (b) Load current vector in complex plane, (c) PWM switching pattern for switch Q_1, (d) PWM switching pattern for switch Q_1.

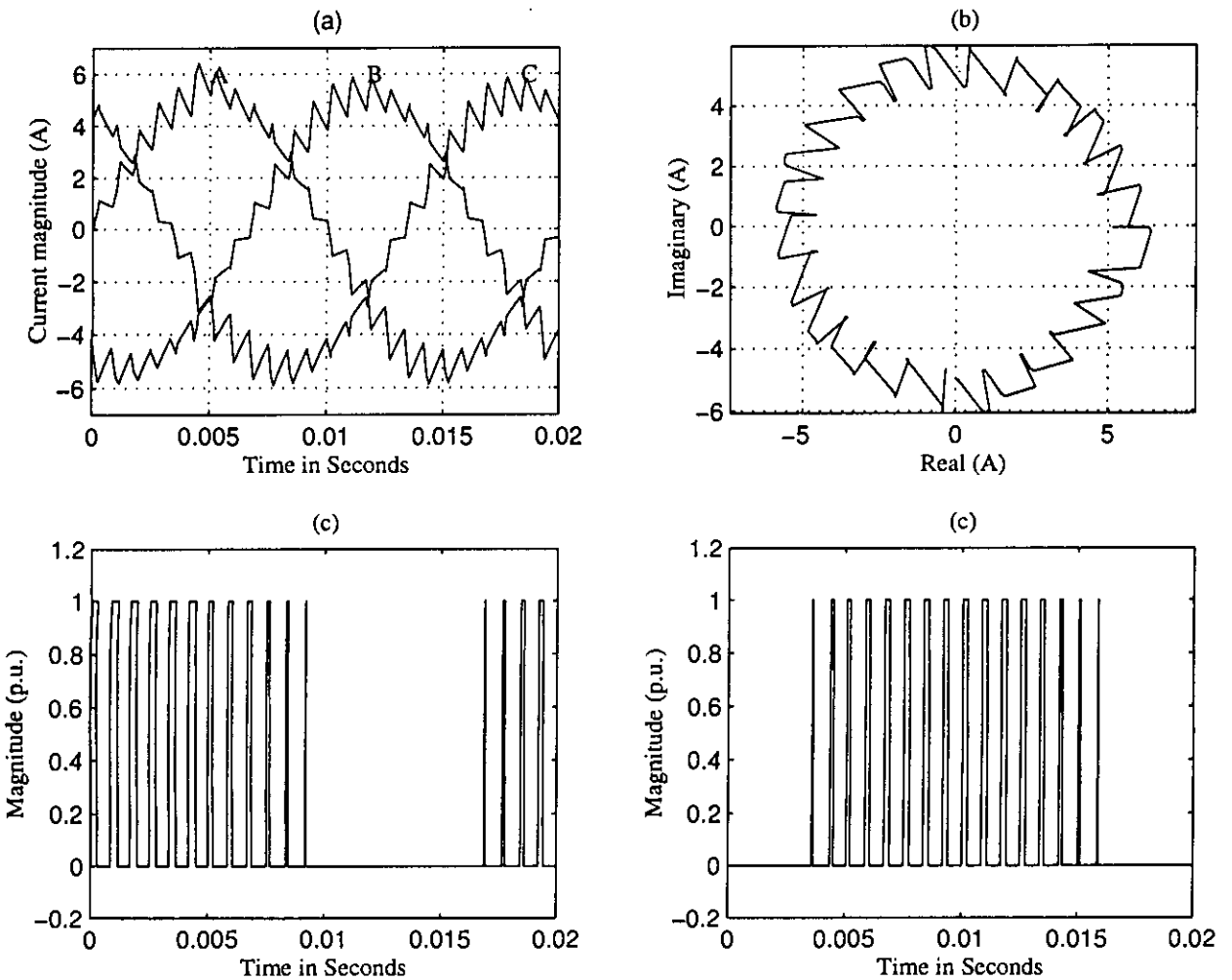

Fig. 3.11: Dynamic response of the proposed predictive controller (**Method 1**) for a step change in load impedance (R = 8Ω to 4Ω , L = 19.1mH to .096mH) with f = 50Hz, f_s = 1200Hz,I_m = 5A, V_s = 240V : (a) Load current waveforms, (b) Load current vector in complex plane, (c) PWM switching pattern for switch Q_1, (d) PWM switching pattern for switch Q_3.

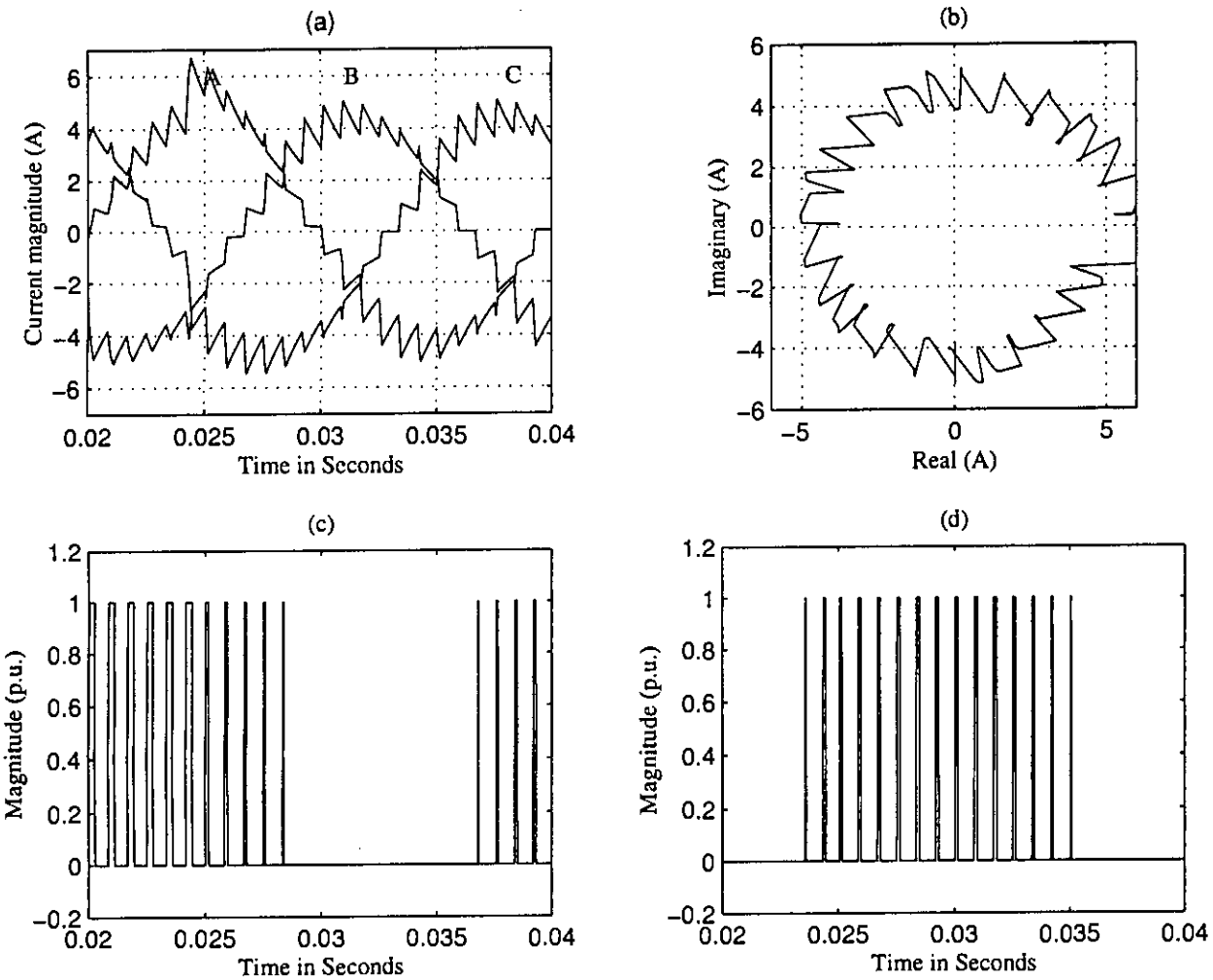

Fig. 3.12: Dynamic response of the proposed predictive controller (**Method 2**) for a step change in load impedance (R = 8Ω to 4Ω , L = 19.1mH to .096mH) with f = 50Hz, f_s = 1200Hz,I_m = 5A, V_s = 240V : (a) Load current waveforms, (b) Load current vector in complex plane, (c) PWM switching pattern for switch Q_1, (d) PWM switching pattern for switch Q_3.

3.6 Response in Case of Large Disturbance

Predictive current controllers do not incorporate instantaneous current limits. Hence there are chances of current overshoots in the case of load (reference current or load impedance) change. For small disturbances the current overshoot may be acceptable, but for large disturbances the current overshoot may go beyond the recommended limit.

In the case of motor drives, if a sudden change in current reference is needed (such as sudden loading during no-load running condition) , while the motor is operated in full speed, the voltage vector magnitude may remain greater than $2V_s/3$ for few carrier cycles. This would force the controller to run in over modulation region. In the over modulation region, it is difficult to control the load current. In such cases, the peak phase current may occasionally go beyond the recommended limit. To get rid of such problems, separate outer loops are normally employed [93-95] in drive applications.

In the proposed controller, the controller operation in over modulation region is discarded. Any over-modulation case is treated as dynamic condition and the voltage vector is rounded to a predetermined value. The rounded value (magnitude) greatly affects the current overshoots.

The current overshoots of predictive controllers are due to their very fast response. The controller uses the derivative control approach for its compensation purpose. The established fact is that derivative controllers always overshoots much. The only way of reducing overshoots is to put a damping device in the controller. The damping function may be calculated from the system dynamics, but it would be an involved process. In the proposed controller, a constant magnitude limiter is put to the voltage vector with its position remaining unaffected.

The proposed controller is tested for large disturbances of a typical motor load with the peak back emf of 40.0 volts. Current overshoots with different disturbances are observed with different vector limits. The peak phase currents in conventional predictive controller and the proposed **Method 1** are presented in the Table 3.6.

For a step change in current reference from 5A to 10A, the current overshoot in the proposed controller is 1.07A, when the vector limiter is set at $1.8V_s/3$. This overshoot is

0.46A less than the conventional predictive controller. When the vector limiter is set at $1.6V_s/3$, the current overshoot reduces to 0.42A, which is 1.1A less than the conventional predictive controller. Similar trends are observed for step change in current references of 2.5A to 5A and 6A to 12A.

Table 3.6: CURRENT OVERSHOOTS WITH LARGE DISTURBANCE (AT 90^0) WITH V_s = 240V, R = 8Ω, L = 19.1mH, E = 40V, f = 50Hz, f_s = 1200Hz.

Disturbance	Vector limit set	Peak current (A)	
		Conventional predictive	Proposed predictive Method 1
I_m = 5A⟶10A	$1.8\frac{V_s}{3}$	11.53	11.07
I_m = 5A⟶10A	$1.6\frac{V_s}{3}$	11.53	10.42
I_m = 2.5A⟶5A	$1.8\frac{V_s}{3}$	5.76	5.53
I_m = 2.5A⟶5A	$1.6\frac{V_s}{3}$	5.76	5.21
I_m = 6A⟶12A	$1.8\frac{V_s}{3}$	13.83	13.29
I_m = 6A⟶12A	$1.6\frac{V_s}{3}$	13.83	12.51

3.7 Conclusion

An improved predictive current controller is presented in this chapter. Alternate methods are described for prediction of voltage vectors from equivalent load parameters. In Method 1 the switching voltage vector prediction is based on load parameters and feedback currents. In Method 2 the vector prediction is based on load parameters and command reference currents. Detailed procedures are described for implementation of the proposed controllers. The design approach proposed in this chapter provides better dynamic performance. Current overshoots during large disturbances are significantly reduced in the new design. It is observed that the controller designed with Method 1 gives better performance (compared to Method 2) in startup and dynamic conditions. The switching frequency of the proposed controllers are uniform in both dynamic and steady states.

The time required for computations of voltage vectors and associated switching pattern is more compared to the programmed ramp comparison controller described in chapter 2. However, the proposed predictive controllers have defined switching sequence and can run at constant switching frequency in all operating conditions.

Chapter 4

New and Novel Regular Sampled Current Controller for Voltage Source Inverters

4.1 Introduction

Analysis of HCC reveals that the switching frequency is non-uniform with a fixed band. The add-on function explained in chapter 2, can keep the switching frequency constant. While making the switching frequency constant, the hysteresis band becomes a time varying quantity. The PRC adopts natural sampling process and hence the PWM pattern for all fundamental periods may not be same, which means that unwanted sub-harmonics would be generated. The sub-harmonic effect is inherent in all the HCC, RCC and PRC schemes.

In the PRC, the load current cuts the triangular carrier either in the up-slope (rising side) or the down slope (falling side). Hence, in any carrier period, the load current ripple would not exceed the peak value of the triangular carrier. Thus, the amplitude of the carrier would determine the band limit of the load current ripple. This leads to an important idea that if by any means the proper duty cycle can be predicted on carrier cycle basis, then the load current ripple would be confined within a band limit.

The predictive current controller discussed in chapter 3, predicts a duty cycle using the

vector control approach. The duty cycle needs information of the voltage vector, its position and the load current vector in addition to the reference current vector. Due to the integrated nature of the predictive controller, the PWM patterns for three phases are correlated. Treatment on individual phases are not possible in predictive controller, hence, there are current overshoots in dynamic states. In steady state, the THD of predictive controller is more compared to PRC, however, it (predictive controller) is free from sub-harmonic effects because the computations are done using regular sampling strategy.

If the advantages of PRC and predictive controller can be combined in a single scheme, then it would result in a new controller with better overall performance. In this chapter, a new and novel current controller, referred as the NEW-CC, is proposed where scalar type prediction is employed for switching points. The reference current of the NEW-CC is a sinusoid and is sampled at regular intervals. Then a suitable bipolar (two level) pulse pattern is calculated for the respective inverter phase so that it forces the load current to follow the reference current profile. Separate PWM patterns are computed for individual phases so that they remain un-correlated during transient periods. Regular sampling strategy is adopted for the NEW-CC on carrier cycle basis and an integer number of pulses are ensured in each fundamental cycles discarding the possibility of introduction of unwanted sub-harmonic effects. The PWM patterns for each phase are center justified on each carrier period to take advantage of double carrier frequency effect on the load.

In the NEW-CC, the switching frequency of the inverter switches are equal to the sampling frequency and is maintained almost uniform during operation of the inverter. The controller needs information of the load parameters and the dc input voltage of the inverter. To generalize the application of the proposed controller to any type of balanced three phase load, the equivalent resistance and inductance per phase are used in the computation process. The performance of the new controller (NEW-CC) are compared with HCC, RCC and Predictive controllers for an induction motor load. Detailed mathematical model have been developed. Implementation scheme and experimental results are also presented.

Since the output of a VSI is stepped in nature, the general form of current through a series R-L network with a step input voltage is used for computation of the switching points

(duty cycles) of the new controller. An R-L network with a step excitation is described in the next section.

4.2 Current in the R-L Load with a Step Voltage Input

An R-L load is connected in series to a voltage source (with supply voltage V_s) through a switch (S_w) as shown in Fig. 4.1. The switch S_w is closed at $t = 0$. Applying Kirchoff's voltage law one can write

$$Ri + L\frac{di}{dt} = V_s \tag{4.1}$$

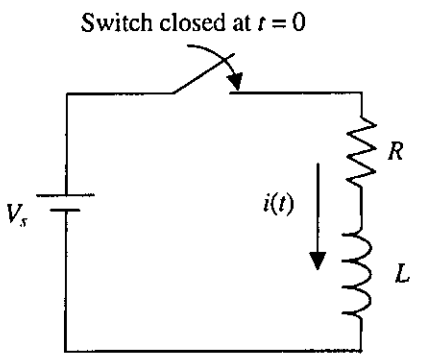

Fig. 4.1: An unit step applied to an R-L load.

With initial condition: $i(t = 0) = I_0$. In Laplace's domain, Eq. (4.1) becomes

$$RI(s) + LsI(s) - LI_0 = \frac{V_s}{s} \tag{4.2}$$

Solving (4.2) for $I(s)$ gives

$$\begin{aligned} I(s) &= \frac{V_s}{Ls(s + \frac{R}{L})} + \frac{I_0}{s + \frac{R}{L}} \\ &= \frac{V_s}{R}\left(\frac{1}{s} - \frac{1}{s + \frac{R}{L}}\right) + \frac{I_0}{s + \frac{R}{L}} \end{aligned} \tag{4.3}$$

Taking inverse transform of Eq. (4.3) yields

$$i(t) = I_0 e^{-\frac{Rt}{L}} + \frac{V_s}{R}\left(1 - e^{-\frac{Rt}{L}}\right) \tag{4.4}$$

Equation (4.4) can be applied to a sampled R-L network. If the sampling time is T and the network current at the n^{th} sample is $I(n)$, then the current at the $(n+1)^{th}$ sample would be

$$I(n+1) = I(n)e^{-\frac{RT}{L}} + \frac{V_s}{R}\left(1 - e^{-\frac{RT}{L}}\right) \tag{4.5}$$

Equation (4.5) is useful to all sampled R-L networks, where the supply voltage term V_s would be replaced by the system excitation function.

4.3 Analysis of Regular Sampled Current Controller

A half bridge inverter is considered with an R-L load as shown in Fig. 4.2. In the two level PWM, switches Q_1 and Q_4 are operated in a complementary fashion. One switch is turned ON while the other is OFF and vice versa. When Q_1 is turned ON (while Q_4 is OFF) a positive voltage V_a appears across the load ($V_{AN} = V_a$). The current through the load rises in the positive direction. When Q_1 is turned OFF, D_4 is forward biased by the inductance voltage and free-wheels the load current via $-V_a$. Next when Q_4 is turned ON (while Q_1 is OFF), a negative voltage $-V_a$ appears across the load ($V_{AN} = -V_a$). The current through the load falls in the negative direction. After some time, when Q_4 is turned OFF, D_1 becomes forward biased by the inductance voltage and free-wheels the load current via $+V_a$.

A current reference i_a^* is considered in this case as shown in Fig. 4.2(b). The current is sampled at an interval of T_s ($T_s = T$). An average voltage of magnitude $V_{an}(n)$ can force the load current i_a from $I(n)$ to $I(n+1)$ during the n^{th} sampling interval. Using (4.5), the current in this case would be obtained as

$$I(n+1) = I(n)e^{-\frac{RT_s}{L}} + \frac{V_{an}(n)}{R}\left(1 - e^{-\frac{RT_s}{L}}\right) \tag{4.6}$$

Simplification of (4.6) yields

$$V_{an}(n) = R\left[\frac{I(n+1) - I(n)e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right] \tag{4.7}$$

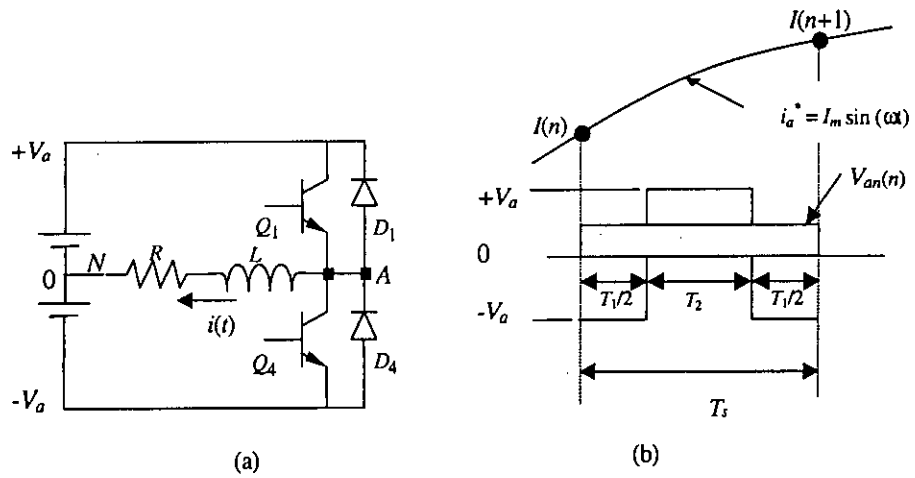

Fig. 4.2: An $R-L$ load connected to a half bridge inverter and current waveform to a two level PWM pulse.

The average voltage V_{an} can be obtained from the two level voltage. The PWM waveform has voltages of $-V_a$ and V_a for durations of T_1 and T_2 seconds respectively. The duty cycle of the PWM pulse is defined as $K(n)$ and is given by

$$K(n) = \frac{T_2}{T_s} \tag{4.8}$$

$$T_2 = K(n)T_s \tag{4.9}$$

The following relationships hold in this case.

$$T_1 + T_2 = T_s \tag{4.10}$$

$$\text{or,} \quad T_1 = T_s - T_2 \tag{4.11}$$

Combining (4.9) and (4.11) yields

$$T_1 = [1 - K(n)]T_s \tag{4.12}$$

The average voltage over the n^{th} sampling period is given by

$$V_{an}(n) = \frac{T_1(-V_a) + T_2 V_a}{T_s} \tag{4.13}$$

Combining (4.9), (4.12) and (4.13) yields

$$V_{an}(n) = \frac{K(n)T_sV_a - V_aT_s\left(1-K(n)\right)}{T_s} \tag{4.14}$$

$$= \left[2K(n)-1\right]V_a \tag{4.15}$$

Substituting $V_{an}(n)$ from (4.15) in (4.7) yields

$$\left[2K(n)-1\right]V_a = R\left[\frac{I(n+1)-I(n)e^{-\frac{RT_s}{L}}}{1-e^{-\frac{RT_s}{L}}}\right] \tag{4.16}$$

$$K(n) = 0.5\left[1+\frac{R}{V_a}\left(\frac{I(n+1)-I(n)e^{-\frac{RT_s}{L}}}{1-e^{-\frac{RT_s}{L}}}\right)\right] \tag{4.17}$$

A bipolar pulse with a duty of $K(n)$ would force the load current from $I(n)$ to $I(n+1)$. Although the initial and final current stay on the sinusoidal reference, the intermediate current would deviate from the reference envelop because of the pulsed voltage. The deviation of the load current path from the reference one is referred to as current ripples and can be determined with few assumptions.

4.4 Current Ripple

The load current contains ripples around the fundamental component. The load current ripple can be computed with fair accuracy assuming a piece-wise linear version of the fundamental. Referring to Fig. 4.3, during $\{1-K(n)\}T_s/2$ one can write

$$Ri_a + L\frac{2\Delta i_a^-}{\{1-K(n)\}T_s} = -V_a \tag{4.18}$$

where Δi_a^- is the fall of load current i_a during $\{1-K(n)\}T_s/2$.

Assuming a current ripple of β one can write

$$\Delta i_a^- = -\beta + \frac{m\{1-K(n)\}T_s}{2} \tag{4.19}$$

where m is the slope of the fundamental current i_a^*. Combining (4.18) and (4.19) gives

$$-\{1-K(n)\}T_s\left[\frac{V_a+Ri_a}{2L}\right] = -\beta + \frac{m\{1-K(n)\}T_s}{2} \tag{4.20}$$

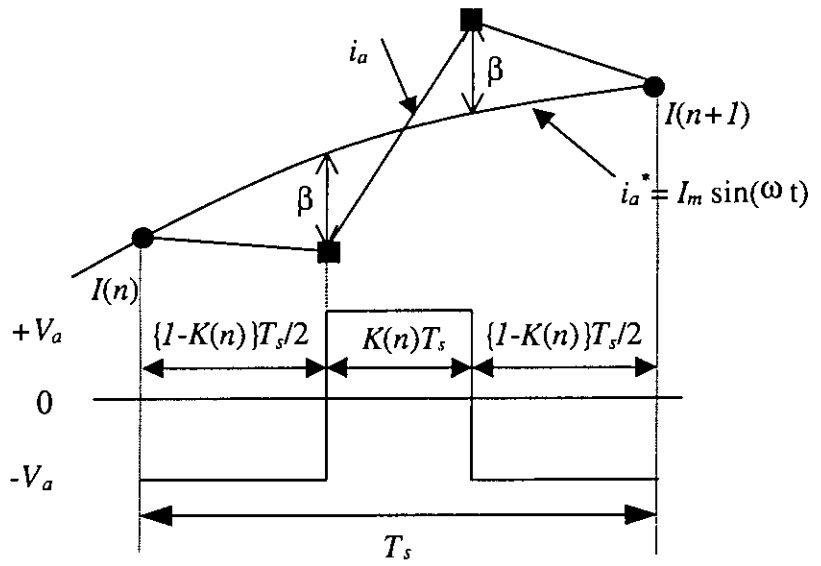

Fig. 4.3: Current ripple in an R-L load with two level PWM.

Simplification of (4.20) yields

$$\{1 - K(n)\}T_s = \frac{2\beta L}{V_a + Ri_a + mL} \tag{4.21}$$

For the positive pulse duration $K(n)T_s$ one can write

$$Ri_a + L\frac{\Delta i_a^+}{K(n)T_s} = V_a \tag{4.22}$$

where Δi_a^+ is the rise of load current i_a during $K(n)T_s$. In terms of β, Δi_a^+ can be written as

$$\Delta i_a^+ = 2\beta + mK(n)T_s \tag{4.23}$$

Combining (4.22) and (4.23) yields

$$K(n)T_s\left[\frac{V_a - Ri_a}{L}\right] = 2\beta + mK(n)T_s \tag{4.24}$$

Simplification of (4.24) yields

$$K(n)T_s = \frac{2\beta L}{V_a - Ri_a - mL} \tag{4.25}$$

Adding (4.21) and (4.25) results

$$T_s = \frac{2\beta L}{V_a + Ri_a + mL} + \frac{2\beta L}{V_a - Ri_a - mL} \tag{4.26}$$

Putting $f_s = \frac{1}{T_s}$ in (4.26) and simplying one can get

$$\frac{1}{f_s} = 2\beta L\left[\frac{2V_a}{V_a^2 - (Ri_a + mL)^2}\right] \tag{4.27}$$

$$\text{or,} \quad \beta = \frac{1}{4V_aLf_s}\left[V_a^2 - (Ri_a + mL)^2\right] \tag{4.28}$$

With a sinusoidal reference current $i_a^* = I_m \sin(\omega t)$, $m = \frac{di_a^*}{dt} = I_m\omega\cos(\omega t)$. Assuming $i_a \approx i_a^*$ and inserting the value of m in (4.28) yields

$$\beta = \frac{1}{4V_aLf_s}\left[V_a^2 - \{RI_m\sin(\omega t) + I_m\omega L\cos(\omega t)\}^2\right] \tag{4.29}$$

Let $R = Z\cos\theta$ and $\omega L = Z\sin\theta$. With this identity, (4.29) can be written as

$$\beta = \frac{1}{4V_aLf_s}\left[V_a^2 - I_m^2Z^2\sin^2(\omega t + \theta)\right] \tag{4.30}$$

where $Z = \sqrt{R^2 + (\omega L)^2}$ and $\theta = tan^{-1}\frac{\omega L}{R}$. Using the trigonometric identity, $2\sin^2 A = 1 - \cos(2A)$, (4.30) can be further simplified as

$$\beta = \frac{1}{4V_aLf_s}\left[V_a^2 - \frac{I_m^2Z^2}{2}\{1 - \cos(2\omega t + 2\theta)\}\right] \tag{4.31}$$

$$\text{or,} \quad \beta = \frac{V_a}{4Lf_s}\left[1 - \frac{I_m^2Z^2}{2V_a^2} + \frac{I_m^2Z^2}{2V_a^2}\cos(2\omega t + 2\theta)\right] \tag{4.32}$$

From (4.32) it is evident that the current ripple is a time varying function. The average ripple would be

$$\beta_{av} = \frac{V_a}{4Lf_s}\left(1 - \frac{I_m^2Z^2}{2V_a^2}\right) \tag{4.33}$$

4.4.1 Maximum and Minimum Ripples

The maximum and minimum current ripples can be derived from (4.32) by differentiation. Differentiating (4.32) yields

$$\frac{d\beta}{d(\omega t)} = -\frac{V_a}{4Lf_s} \times \frac{2I_m^2Z^2}{2V_a^2}\sin(2\omega t + 2\theta) \tag{4.34}$$

Imposing the constraint for maxima and minima on (4.34), i. e., $\frac{d\beta}{d(\omega t)} = 0$ one can write

$$\sin(2\omega t + 2\theta) = 0 \tag{4.35}$$

Simplification of (4.35) yields

$$2\omega t + 2\theta = q\pi \quad q = 0, 1, 2 \cdots \tag{4.36}$$

$$\text{or,} \quad \omega t = q\frac{\pi}{2} - \theta \tag{4.37}$$

Combining (4.32) and (4.36) the maximum/minimum ripples come as

$$\beta_m = \frac{V_a}{4Lf_s}\left[1 - \frac{I_m^2 Z^2}{2V_a^2} + \frac{I_m^2 Z^2}{2V_a^2}\cos(q\pi)\right] \tag{4.38}$$

From (4.38) it is clear that the maximum ripple would occur when $\cos(q\pi) = 1$, i. e., at $q = 2, 4, 6 \cdots$. The minimum ripple would occur when $\cos(q\pi) = -1$ i. e., at $q = 1, 3, 5 \cdots$. The maximum and minimum ripples are given by

$$\beta_{max} = \frac{V_a}{4Lf_s} \tag{4.39}$$

$$\beta_{min} = \frac{V_a}{4Lf_s}\left[1 - \frac{I_m^2 Z^2}{V_a^2}\right] \tag{4.40}$$

The maximum ripple depends only on inductance L of the load and not on the overall impedance Z.

4.5 Application of the Current Controller to Three Phase Inverter with Star Connected Load

Three phase inverters are intended for applications to balanced loads only. For unbalanced loads three individual single phase inverters are used. Balanced loads may be either star connected or delta connected. Delta connected loads are equivalent to star loads with insulated neutral. Star loads with connected neutral are discarded for use with inverters since in that case the supply voltage has to be split into two equal parts. In case of connected neutral system, the load may be treated as a combination of three isolated single phase loads spaced at 120^0.

The analysis presented in section 4.2.1 assumes a single phase half bridge inverter. The duty cycle equation (4.17) can be used for three phase Y-connected load with the neutral connected to the dc supply midpoint. For a neutral connected system, V_a would be half the total dc supply ($V_a = V_s/2$).

But for a neutral unconnected system as shown in Fig. 4.4, the magnitude of V_a (to be applied across a phase) is unknown. (V_a is the average voltage that is to be applied across a phase so that the load current is forced to follow the command reference which is a sinusoid).

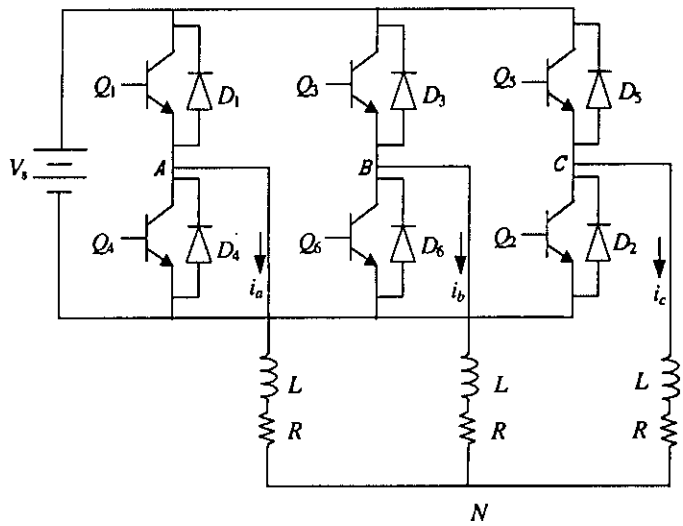

Fig. 4.4: A three phase inverter with star connected R-L load.

A three phase inverter when operated in two levels, have a stepped pulse phase voltage waveform. In active modes, there are stepped voltages with magnitudes of $\frac{2}{3}V_s$ and $\frac{1}{3}V_s$. A proper value of V_a is determined from an analysis of the phase voltage as presented in section 4.5.1.

4.5.1 Phase Voltages in Star Connected Load with Insulated Neutral

In a three phase full bridge inverter driving an insulated neutral star load, the phase voltage waveform patterns are different from the switching pattern of the inverter switches. The effective average phase voltage in any carrier cycle depends on the state of all the switches of the inverter. A typical PWM sample of three phases $K_a(n), K_b(n), K_c(n)$ are considered for the n^{th} carrier cycle as shown in Fig. 4.5 . The PWM patterns are such that $K_c(n) > K_a(n) > K_b(n)$. From Fig. 4.5 it is seen that in the n^{th} carrier period, voltages

$-V_s/3$ and $V_s/3$ are impressed across phase A for time durations of $[K_c(n) - K_a(n)]T_s$ and $[K_a(n) - K_b(n)]T_s$ respectively. The average voltage of phase A at the n^{th} carrier period would be

$$\begin{aligned} v_{an}(n) &= \frac{(K_c(n) - K_a(n))T_s \times \frac{-V_s}{3} + (K_a(n) - K_b(n))T_s \times \frac{V_s}{3}}{T_s} \\ &= \{2K_a(n) - K_b(n) - K_c(n)\}\frac{V_s}{3} \end{aligned} \tag{4.41}$$

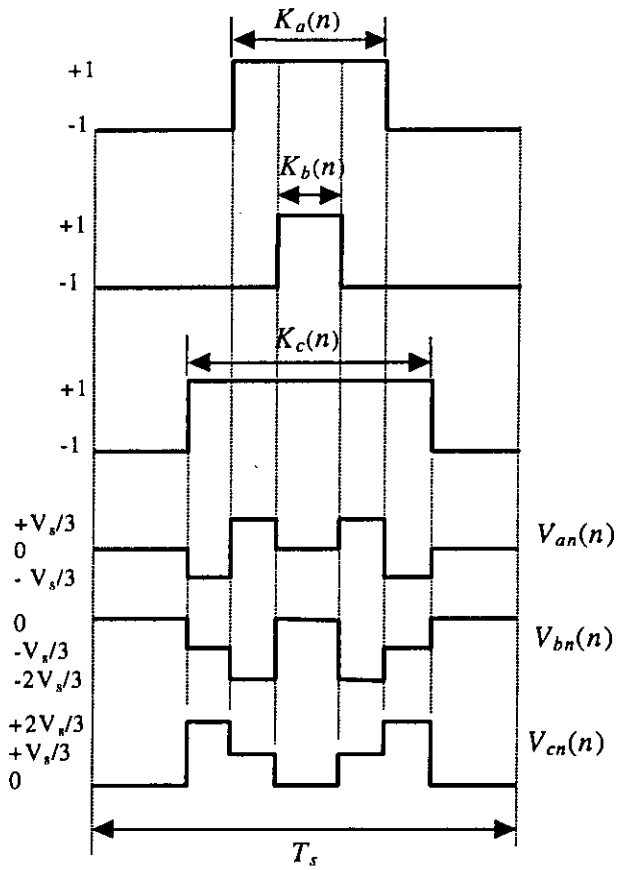

Fig. 4.5: Phase voltages in NEW-CC with star load (Neutral unconnected).

Voltages $-2V_s/3$ and $-V_s/3$ are impressed across phase B for time duration of $[K_a(n) - K_b(n)]T_s$ and $[K_c(n) - K_a(n)]T_s$ respectively. The average voltage of phase B at the n^{th} carrier period would be

$$v_{bn}(n) = \frac{(K_a(n) - K_b(n))T_s \times \frac{-2V_s}{3} + (K_c(n) - K_a(n))T_s \times \frac{-V_s}{3}}{T_s}$$

$$= \{2K_b(n) - K_c(n) - K_a(n)\}\frac{V_s}{3} \tag{4.42}$$

In phase C the impressed voltages are $V_s/3$ and $2V_s/3$ for time duration of $[K_a(n) - K_b(n)]T_s$ and $[K_c(n) - K_a(n)]T_s$ respectively. The average voltage of phase C at the n^{th} carrier period would be

$$\begin{aligned} v_{cn}(n) &= \frac{(K_a(n) - K_b(n))T_s \times \frac{V_s}{3} + (K_c(n) - K_a(n))T_s \times \frac{2V_s}{3}}{T_s} \\ &= \{2K_c(n) - K_a(n) - K_b(n)\}\frac{V_s}{3} \end{aligned} \tag{4.43}$$

Although (4.41), (4.42) and (4.43) are derived using the condition $K_c(n) > K_a(n) > K_b(n)$, the same expressions are obtained for all other possible combinations of $K_a(n)$, $K_b(n)$ and $K_c(n)$. The reference currents for the three phases are considered to be sinusoidal. The sampled three phase current references are

$$i_a^*(n) = I_m \sin(\omega n T_s) \tag{4.44}$$

$$i_b^*(n) = I_m \sin(\omega n T_s - \frac{2\pi}{3}) \tag{4.45}$$

$$i_c^*(n) = I_m \sin(\omega n T_s - \frac{4\pi}{3}) \tag{4.46}$$

where I_m is the peak current, $\omega = 2\pi f$, n is the sample number, $n = 1, 2, 3, ...$ and T_s is the sampling time, f is the reference frequency and i_a^* , i_b^* , i_c^* are reference currents for phases A, B and C respectively. Putting the values of $K_a(n)$, $K_b(n)$ and $K_c(n)$ in (4.41) yields

$$\begin{aligned} v_{an}(n) = &\left[1 + \frac{R}{V_a}\left(\frac{I_m \sin\{\omega(n+1)T_s\} - I_m \sin\{\omega n T_s\}e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right)\right. \\ &-0.5 - \frac{R}{2V_a}\left(\frac{I_m \sin\{\omega(n+1)T_s - \frac{2\pi}{3}\} - I_m \sin\{\omega n T_s - \frac{2\pi}{3}\}e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right) \\ &\left.-0.5 - \frac{R}{2V_a}\left(\frac{I_m \sin\{\omega(n+1)T_s - \frac{4\pi}{3}\} - I_m \sin\{\omega n T_s - \frac{4\pi}{3}\}e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right)\right]\frac{V_s}{3} \end{aligned} \tag{4.47}$$

$$\begin{aligned} = &\left[\left(\frac{\sin\{\omega(n+1)T_s\} - \sin\{\omega n T_s\}e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right)\right. \\ &+0.5\left(\frac{-\sin\{\omega(n+1)T_s - \frac{2\pi}{3}\} + \sin\{\omega n T_s - \frac{2\pi}{3}\}e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right) \\ &\left.+0.5\left(\frac{-\sin\{\omega(n+1)T_s - \frac{4\pi}{3}\} + \sin\{\omega n T_s - \frac{4\pi}{3}\}e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right)\right]\frac{RI_m V_s}{3V_a} \end{aligned} \tag{4.48}$$

$$
\begin{aligned}
= & \left[\left(\frac{1.5\sin\{\omega(n+1)T_s\} - 1.5\sin\{\omega nT_s\}e^{-\frac{RT_s}{L}}}{1-e^{-\frac{RT_s}{L}}}\right)\right. \\
& +0.5\left(\frac{-\sin\{\omega(n+1)T_s\} + \sin\{\omega nT_s\}e^{-\frac{RT_s}{L}}}{1-e^{-\frac{RT_s}{L}}}\right) \\
& +0.5\left(\frac{-\sin\{\omega(n+1)T_s - \frac{2\pi}{3}\} + \sin\{\omega nT_s - \frac{2\pi}{3}\}e^{-\frac{RT_s}{L}}}{1-e^{-\frac{RT_s}{L}}}\right) \\
& \left.+0.5\left(\frac{-\sin\{\omega(n+1)T_s - \frac{4\pi}{3}\} + \sin\{\omega nT_s - \frac{4\pi}{3}\}e^{-\frac{RT_s}{L}}}{1-e^{-\frac{RT_s}{L}}}\right)\right]\frac{RI_mV_s}{3V_a} \qquad (4.49)
\end{aligned}
$$

The last three terms of (4.49) under braces adds up to zero. Hence (4.49) simplifies to

$$
\begin{aligned}
v_{an}(n) &= \left[\frac{1.5\sin\{\omega(n+1)T_s\} - 1.5\sin\{\omega nT_s\}e^{-\frac{RT_s}{L}}}{1-e^{-\frac{RT_s}{L}}}\right]\frac{RI_m}{3} \\
&= \left[\frac{\sin\{\omega(n+1)T_s\} - \sin\{\omega nT_s\}e^{-\frac{RT_s}{L}}}{1-e^{-\frac{RT_s}{L}}}\right]\frac{RI_mV_s}{2V_a} \qquad (4.50)
\end{aligned}
$$

For small values of T_s, $e^{-\frac{RT_s}{L}} \approx 1-\frac{RT_s}{L}$. With this approximation (4.50) can be rewritten as

$$
\begin{aligned}
v_{an}(n) &= \left[\frac{\sin\{\omega(n+1)T_s\} - \sin\{\omega nT_s\}\left(1-\frac{RT_s}{L}\right)}{\frac{RT_s}{L}}\right]\frac{RI_mV_s}{2V_a} \\
&= \left[\sin\{\omega(n+1)T_s\} - \sin\{\omega nT_s\}\left(1-\frac{RT_s}{L}\right)\right]\frac{I_mLV_s}{2T_sV_a} \\
&= \left[L\left\{\sin\{\omega(n+1)T_s\} - \sin\{\omega nT_s\}\right\} + \sin\{\omega nT_s\}RT_s\right]\frac{I_mV_s}{2T_sV_a} \qquad (4.51)
\end{aligned}
$$

Considering a piece-wise linear version of the sine wave, $\sin\{\omega(n+1)T_s\} - \sin\{\omega nT_s\} = \omega T_s\cos\{\omega nT_s\}$. Equation (4.51) can be written as

$$
\begin{aligned}
v_{an}(n) &= \left[\omega LT_s\cos\{\omega nT_s\} + RT_s\sin\{\omega nT_s\}\right]\frac{I_mV_s}{2T_sV_a} \\
&= \frac{I_mV_s}{2V_a}\left[\omega L\cos\{\omega nT_s\} + R\sin\{\omega nT_s\}\right] \\
&= I_mZ\frac{V_s}{2V_a}\sin(\omega nT_s - \theta) \qquad (4.52)
\end{aligned}
$$

where $Z = \sqrt{(R^2 + (\omega L)^2)}$ and $\theta = tan^{-1}\frac{\omega L}{R}$. Since Z is the impedance per phase of the load, it is evident from (4.52) that the voltage impressed across phase A would be a time

averaged (carrier cycle basis) sinusoid if $\frac{I_m Z V_a}{2V_a} = I_m Z$. With this identity one can get

$$\begin{aligned} \frac{V_s}{2V_a} &= 1 \\ \text{or, } V_a &= \frac{V_s}{2} \end{aligned} \tag{4.53}$$

Putting the value of V_a from (4.53) to (4.52) yields

$$v_{an}(n) = I_m Z \sin(\omega n T_s - \theta) \tag{4.54}$$

From (4.54) it is clear that NEW-CC would maintain proper magnitude and phase relations (as is required in a balanced circuit) with $V_a = V_s/2$. In a similar way it can be shown that the impressed voltages across other phases (phases B and C) also maintain proper magnitude and phase relations.

4.5.2 Duty Cycles in NEW-CC for Neutral Insulated System

For NEW-CC with neutral unconnected Y load, the duty cycle for any phase would be obtained from (4.17) with $V_a = V_s/2$.

$$K(n) = 0.5\left[1 + \frac{2R}{V_s}\left(\frac{I(n+1) - I(n)e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right)\right] \tag{4.55}$$

For the n^{th} carrier period, let the duty cycles for phases A, B, C would be $K_a(n)$, $K_b(n)$, $K_c(n)$ respectively. The duty cycles for the three phases are obtained from (4.55) as

$$K_a(n) = 0.5\left[1 + \frac{2R}{V_s}\left(\frac{I_m \sin\{\omega(n+1)T_s\} - I_m \sin\{\omega n T_s\}e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right)\right] \tag{4.56}$$

$$K_b(n) = 0.5\left[1 + \frac{2R}{V_s}\left(\frac{I_m \sin\{\omega(n+1)T_s - \frac{2\pi}{3}\} - I_m \sin\{\omega n T_s - \frac{2\pi}{3}\}e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right)\right] \tag{4.57}$$

$$K_c(n) = 0.5\left[1 + \frac{2R}{V_s}\left(\frac{I_m \sin\{\omega(n+1)T_s - \frac{4\pi}{3}\} - I_m \sin\{\omega n T_s - \frac{4\pi}{3}\}e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right)\right] \tag{4.58}$$

The total number of PWM pulses in one fundamental period N_{max} is given by

$$N_{max} = \frac{f_s}{f} \tag{4.59}$$

4.6 Estimation of R-L Parameters of the Load

The controller computes the duty cycles at regular intervals from information of the supply voltage V_s, f, f_s and equivalent $R-L$ parameters of the load. For fixed load, there would be no need for continuous estimation of the load parameters. But for dynamic loads such as ac motors the load parameters may vary. During startup the load parameters changes because of the continuous change in the motor slip. In steady state running condition, the load is fixed since slip is constant. During running condition, if sudden change in load is applied to the motor, the rotor would accelerate or decelerate depending upon the type of load change. Hence, during startup and dynamic loading conditions the $R-L$ parameters of the load would vary. If the load parameters are not properly inserted in the computation process, the controller would fail to track the load current.

The equivalent load parameters can be estimated from the load current by computing its fundamental magnitude and phase shift from the reference current. For this, load current data for a fundamental period is required. The load parameter estimation on fundamental cycle basis yields good results at steady state, when the load current waveforms are symmetrical. At dynamic loading condition, it would not work because of the unsymmetrical current wave shape. At dynamic loading conditions, the load parameters may be estimated on carrier cycle basis which involves two phases for the computation. The latter one is a fair estimator due to finite and limited carrier frequency. However, the parameters estimated on carrier cycle basis would help resolving the problem of current overshoots that occur during step load change. Both methods would be used in the implementation scheme to have good steady state and dynamic performance.

4.6.1 R-L Parameter Estimation on Carrier Cycle Basis from Two Phase Data

To estimate the load parameters from a previous carrier cycle data, two phase voltages and currents are required. The average phase voltages $V_{an}(n-1)$ and $V_{bn}(n-1)$ at the $(n-1)^{th}$ carrier cycle would be used for the computation process.

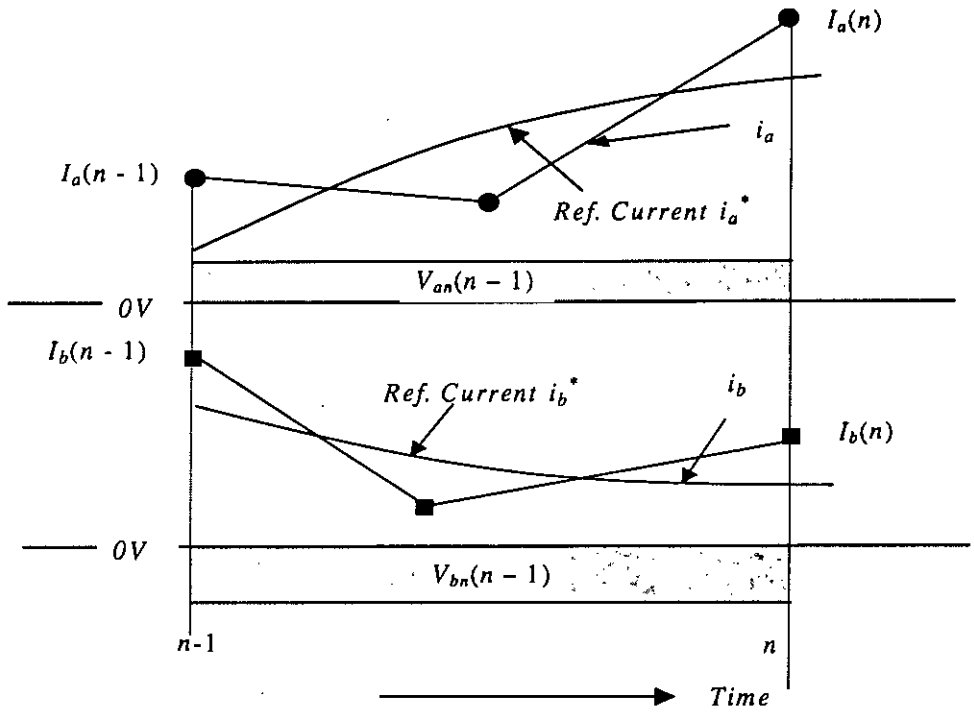

Fig. 4.6: Load parameter estimation on carrier cycle basis.

In the $(n-1)^{th}$ carrier period the following difference equations hold

$$RI_a(n-1) + L\frac{\Delta I_a(n-1)}{T_s} = V_{an}(n-1) \tag{4.60}$$

$$RI_b(n-1) + L\frac{\Delta I_b(n-1)}{T_s} = V_{bn}(n-1) \tag{4.61}$$

where $\Delta I_a(n-1) = I_a(n) - I_a(n-1)$ and $\Delta I_b(n-1) = I_b(n) - I_b(n-1)$. Solution of (4.60) and (4.61) yields

$$R = \frac{V_{an}(n-1)\Delta I_b(n-1) - V_{bn}(n-1)\Delta I_a(n-1)}{I_a(n-1)\Delta I_b(n-1) - I_b(n-1)\Delta I_a(n-1)} \tag{4.62}$$

$$L = T_s\frac{V_{bn}(n-1)I_a(n-1) - V_{an}(n-1)I_b(n-1)}{I_a(n-1)\Delta I_b(n-1) - I_b(n-1)\Delta I_a(n-1)} \tag{4.63}$$

4.6.2 R-L Parameter Estimation on Fundamental Cycle Basis from Fourier Analysis

The load parameters estimated from (4.62) and (4.63) deviate from actual parameters when the carrier frequency (f_s) is not sufficiently high. In practice, the carrier frequency

is limited to 2kHz or less because of switch limitations. In steady state if (4.62) and (4.63) are used for R-L estimation, there would always be an error in the duty cycle calculations and hence the load current would not be able to track the reference. Instead, for steady state, a fundamental cycle based estimation would yield better results. In this method, the R-L parameters are initialized from the equivalent circuit model obtained from test results or from computed impedance of previous cycle, ($R = R_0$ and $L = L_0$). The load current for the fundamental period is analyzed using Fourier series. The fundamental current amplitude and phase are computed using the following equations.

$$i_{a1} = I_{a1}\sin(\omega n T_s + \theta_2) \tag{4.64}$$

$$I_{a1} = \sqrt{A_1^2 + B_1^2} \tag{4.65}$$

$$\theta_2 = \tan^{-1}\frac{A_1}{B_1} \tag{4.66}$$

where

$$A_1 = \frac{1}{\pi}\sum_{n=0}^{n=N} i_a(n)[\cos\{\omega n T_s\} - \cos\{\omega(n+1)T_s\}]$$

$$B_1 = \frac{1}{\pi}\sum_{n=0}^{n=N} i_a(n)[\sin\{\omega(n+1)T_s\} - \sin\{\omega n T_s\}]$$

There may be errors in magnitude, phase or both in the load impedance prediction. Typical relations of the reference and actual load currents are shown in Fig. 4.7. The error can be compensated from information of the magnitude and phase angle of i_{a1}. For example, the phase difference (θ_2) between the load current and the reference current would deviate from zero if there is an error in the previously estimated load parameters.

The following equation may be used for the error correction.

$$|Z_{new}| = |Z_{old}| \times \frac{I_m}{I_{a1}} \tag{4.67}$$

$$\theta = \theta_1 - \theta_2 \tag{4.68}$$

$$R_{new} = |Z_{new}|\cos(\theta) \tag{4.69}$$

$$L_{new} = \frac{|Z_{new}|\sin(\theta)}{\omega} \tag{4.70}$$

where θ_1 is the computed impedance angle of the previous cycle.

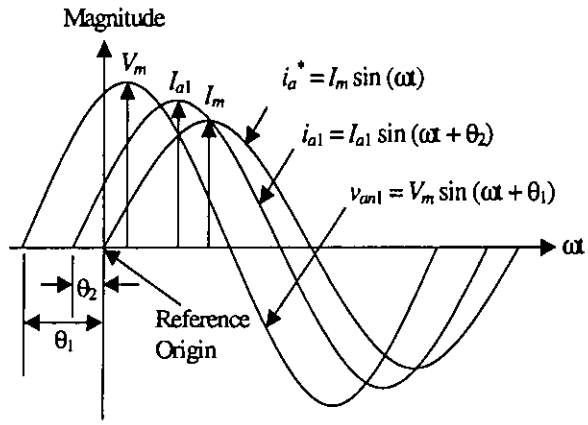

Fig. 4.7: Waveforms showing relations between fundamental voltage, reference and fundamental load currents.

4.7 Controller Scheme

The proposed regular sampled current controller can be realized by using the functional block diagram as shown in Fig. 4.7. The duty cycle computations are done by block 2 using (4.56), (4.57) and (4.58). During start-up since the initial current in all the phases are zero, use of (4.56), (4.57) and (4.58) would cause overshoots in load currents especially in phases B and C. To overcome the effect of overshoots, the initial current terms of (4.56), (4.57) and (4.58) should be replaced by the load current samples. Thus at startup the duty cycles of different phases would be given by

$$K_a(n) = 0.5\left[1 + \frac{2R}{V_s}\left(\frac{I_m \sin\{\omega(n+1)T_s\} - i_a(n)e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right)\right] \tag{4.71}$$

$$K_b(n) = 0.5\left[1 + \frac{2R}{V_s}\left(\frac{I_m \sin\{\omega(n+1)T_s - \frac{2\pi}{3}\} - i_b(n)e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right)\right] \tag{4.72}$$

$$K_c(n) = 0.5\left[1 + \frac{2R}{V_s}\left(\frac{I_m \sin\{\omega(n+1)T_s - \frac{4\pi}{3}\} - i_c(n)e^{-\frac{RT_s}{L}}}{1 - e^{-\frac{RT_s}{L}}}\right)\right] \tag{4.73}$$

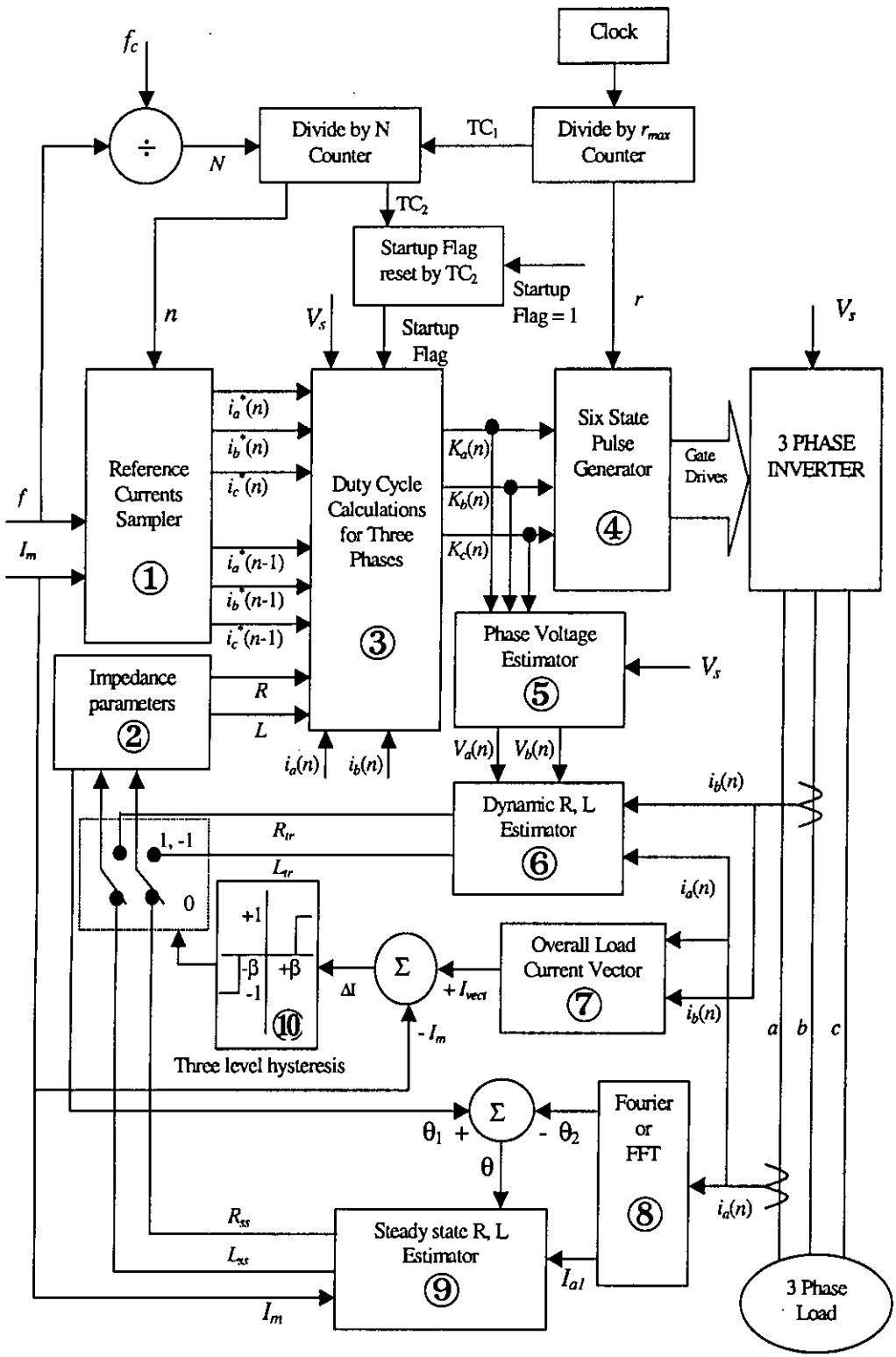

Fig. 4.8: Scheme of the new current controller for three phase VSI.

In the proposed scheme, no feedback of phase C current $i_c(n)$ is taken. It can be derived from the other phase currents as $i_a(n) + i_b(n) + i_c(n) = 0$ for a neutral unconnected star load. Thus $i_c(n)$ becomes

$$i_c(n) = -\{i_a(n) + i_b(n)\} \tag{4.74}$$

The startup cycle is differentiated from others by the "Startup Flag" which is initially "1" and becomes "0" after the first cycle. During steady state, block 9 estimates the load parameters R and L, whereas at dynamic state block 6 is used for this purpose.

The steady state and dynamic states are ascertained from the reference current, I_m and overall load current vector I_{vect}. For a star load with unconnected neutral, the load current vector is given by

$$I_{vect}(n) = \left[i_a(n)^2 + \frac{1}{3}\{i_a(n) + 2i_b(n)\}^2\right] \tag{4.75}$$

The current error vector ΔI is compared using a three level comparator having a hysteresis band of β. A "0" at the output of the comparator means that the current error vector ΔI is within the hysteresis band $\pm\beta$. This is identified as steady state condition. In all other cases, the comparator output would be "+1" or "-1" depending on the magnitude and sign of ΔI.

During running condition if sudden change in load occurs, the overall load current vector ($I_{vect}(n)$) would deviate from the reference one (I_m). If the disturbance is large, the new load parameters would be determined on carrier cycle basis using block 6. The phase voltages $V_a(n)$ and $V_b(n)$ are required for the computation that are to be obtained from (4.41) and (4.42). Initially, the equivalent $R - L$ parameters of the load are estimated. The three phase current generator generates the reference currents of desired amplitude and frequency. The duty cycles of the PWM pulses for the three phases are determined by the switching point calculation block using (4.56-4.58). In the two level PWM, sufficient lockout time T_{LOCK} should be inserted between the top and the bottom switches in one pole so as to overcome dc bus short circuit. A typical PWM pulse with lockout is shown in Fig. 4.9. The lockout time is inserted symmetrically around the switching edges so that it shares the positive and negative pulses equally. This arrangement has negligible effect on the spectrum of the PWM waveform.

4.7.1 Real Time PWM Waveform Generation

For generating the real time waveform, a carrier cycle is divided into r_{max} samples, where r_{max} is an integer and divisible by 2. The magnitude of r_{max} determines the resolution of the PWM pattern and is chosen as high as possible. The base/gate drive circuit of the inverter is connected to the output data pins of the standard parallel port. The data bits and port pins are assigned to the inverter switches as per Table 4.1 shown below.

Table 4.1: DATA BITS AND PORT PIN ASSIGNMENT OF THE INVERTER SWITCHES IN A PC BASED IMPLEMENTATION SCHEME

Data bits	D_5	D_4	D_3	D_2	D_1	D_0
Decimal value	2^5	2^4	2^3	2^2	2^1	2^0
Inverter switch	Q_2	Q_6	Q_4	Q_5	Q_3	Q_1
Parallel port pin	7	6	5	4	3	2

A data byte $Data(n, r)$ is calculated and send to the port. The data is latched to the port for a time duration of τ given by

$$\tau = \frac{T_s}{r_{max}} \tag{4.76}$$

The real time PWM pulses are generated on carrier cycle basis by block 4 using the following algorithm:

Step. 1 Compute the serial number of the PWM pulse (n) in a cycle, set counter $r = 0$.

Step. 2 Compute a counter value for each phases using the following formula:

$$Counter_a(n) = K_a(n) \times r_{max} \tag{4.77a}$$

$$Counter_b(n) = K_b(n) \times r_{max} \tag{4.77b}$$

$$Counter_c(n) = K_c(n) \times r_{max} \tag{4.77c}$$

where r_{max} is the total count in one switching period, T_s and $Counter_a(n)$, $Counter_b(n)$, $Counter_c(n)$ are the count values for phases A, B, and C.

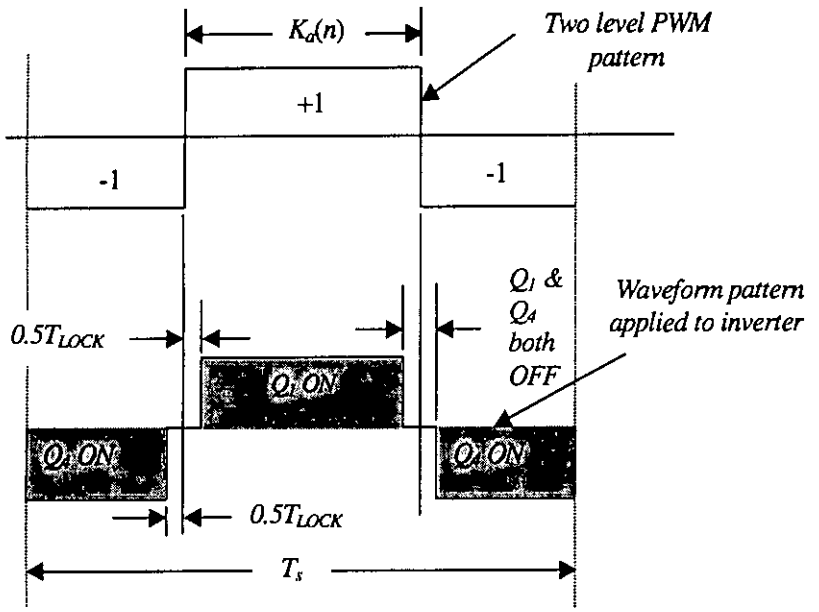

Fig. 4.9: Real time control waveform for phase A (two level PWM).

Step. 3 Compute $Data_a(n,r)$ using

$$Data_a(n,r) = \begin{cases} 2^0 & \left\{\frac{r_{max}+Counter_a(n)}{2} - \frac{T_{lock}}{2\tau}\right\} > r > \left\{\frac{r_{max}-Counter_a(n)}{2} + \frac{T_{lock}}{2\tau}\right\} \\ 2^3 & \left\{\frac{r_{max}-Counter_a(n)}{2} - \frac{T_{lock}}{2\tau}\right\} > r > \left\{\frac{r_{max}+Counter_a(n)}{2} + \frac{T_{lock}}{2\tau}\right\} \\ 0 & \text{otherwise} \end{cases} \tag{4.78}$$

Step. 4 Compute $Data_b(n,r)$ using

$$Data_b(n,r) = \begin{cases} 2^2 & \left\{\frac{r_{max}+Counter_b(n)}{2} - \frac{T_{lock}}{2\tau}\right\} > r > \left\{\frac{r_{max}-Counter_b(n)}{2} + \frac{T_{lock}}{2\tau}\right\} \\ 2^5 & \left\{\frac{r_{max}-Counter_b(n)}{2} - \frac{T_{lock}}{2\tau}\right\} > r > \left\{\frac{r_{max}+Counter_b(n)}{2} + \frac{T_{lock}}{2\tau}\right\} \\ 0 & \text{otherwise} \end{cases} \tag{4.79}$$

Step. 5 Compute $Data_c(n,r)$ using

$$Data_c(n,r) = \begin{cases} 2^4 & \left\{\frac{r_{max}+Counter_c(n)}{2} - \frac{T_{lock}}{2\tau}\right\} > r > \left\{\frac{r_{max}-Counter_c(n)}{2} + \frac{T_{lock}}{2\tau}\right\} \\ 2^1 & \left\{\frac{r_{max}-Counter_c(n)}{2} - \frac{T_{lock}}{2\tau}\right\} > r > \left\{\frac{r_{max}+Counter_c(n)}{2} + \frac{T_{lock}}{2\tau}\right\} \\ 0 & \text{otherwise} \end{cases} \tag{4.80}$$

Step. 6 Compute composite data byte, $Data(n,r)$: $Data(n,r) = Data_a(n,r) + Data_b(n,r) + Data_c(n,r)$.

Step. 7 Send $Data(n,r)$ to the parallel port.

Step. 8 Delay for τ seconds.

Step. 9 Increment counter r .

Step. 10 If $r \leq r_{max}$ go to step 3, else go to step 11.

Step. 11 Return.

4.8 Data Acquisition for Load Current

Feedback of i_a and i_b are taken through two channels of a multi-channel data acquisition system (DAS) card (PCLS-812PG) [105]. The DAS card has one programmable timer (Intel 8253) and 1k byte FIFO (First in First out) RAM. It supports data transfer by DMA and program control approach. The core of the DAS is a 12-bit successive approximation type Analog to Digital Converter (ADC). The DAS has 16 channels and there are provisions for programming the gain of individual channels. The gain amplifier has separate address and the gain can be programmed to 5 discrete levels (1, 2, 4, 8 and 16 times). The DAS card is inserted in the ISA slot of the PC. The ADC has two separately addressable 8-bit buffers for its converted data. The data bus of the DAS is of 8-bits. Hence the ADC output can not be directly read through the DAS data bus. Instead the upper and lower buffers of the ADC are read separately. The data obtained from the upper 8-bit buffer is shifted left by 8-bits and then added to the lower buffer data.
The steps for A/D conversion of any channel are as follows:

- Select channel 0 or 1. (0 for phase A, and 1 for phase B).
- Start A/D conversion. (Just write any data to the ADC).
- Wait for end of conversion (EOC) signal. The EOC signal is obtained by masking the 5^{th} bit of the ADC output buffer (upper). This can be done by a mask pattern

of hexadecimal data 10 (0x10). The ADC puts an active low signal to the EOC pin after completing the conversion process.

- Read the upper buffer data and store it in a variable D_U.
- Read the lower buffer data and store it in a variable D_L.
- Left shift D_U by 8-bits and add the result to D_L to obtain the 12-bit data ($D_{12} = (D_U << 8) + D_L$.
- Obtain the value of I using
  $I = \frac{(V_{max}-V_{min})\times D_{12}}{G\times 2^{12}} + V_{min}$
  where, V_{max} = Positive peak value of ADC (hardware setting), V_{min} = Negative peak value of ADC (hardware setting) and G = Gain of the channel.

The above steps are required for each sample of the load current.

4.9 Performance Study

The controller operates most of the time in steady state, hence its performance in the steady state is very important. The total harmonic distortion (THD) is a tool of measuring the steady state performance. For a current controller the THD may be defined as the ratio of the total harmonic content to the fundamental. Mathematically, it can be represented as

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \tag{4.81}$$

In Fourier series terms, the RMS load current is defined as

$$I_{rms} = \sqrt{\sum_{n=0}^{\infty} I_n^2} \tag{4.82}$$

In the steady state condition there is no dc component (i.e. $I_0 = 0$) in the load current. Hence (4.82) can be written as

$$I_{rms} = \sqrt{\sum_{n=1}^{\infty} I_n^2} \tag{4.83}$$

$$\text{or,} \quad I_{rms}^2 - I_1^2 = \sum_{n=2}^{\infty} I_n^2 \tag{4.84}$$

Combining (4.81) and (4.84) yields

$$THD = \frac{\sqrt{I_{rms}^2 - I_1^2}}{I_1} \tag{4.85}$$

The RMS value of the load current may be obtained from its samples taken over one fundamental cycle using the following formula:

$$I_{rms} = \sqrt{\frac{1}{j_{max}} \sum_{j=1}^{j=j_{max}} I(j)^2} \tag{4.86}$$

where j_{max} is the total current samples over one fundamental period. To test the steady state performance of the proposed controller, a three phase induction motor is considered as a load. The motor is star connected with floating neutral. A standard equivalent circuit of the induction motor is shown in Fig. 4.10.

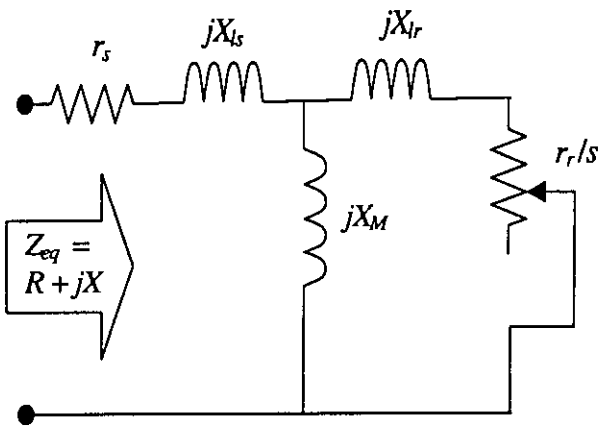

Fig. 4.10: Equivalent circuit of an induction motor, (core loss shunt admittance neglected)

The motor parameters are obtained from standard test at rated frequency ($f_b = 50$ Hz) and are tabulated in Table 4.2.

In variable speed drives, the motor may run at frequencies (f) other than the base frequency (f_b). The reactances of the equivalent circuit changes with frequencies and are given by

$$X_{ls} = X'_{ls}\frac{f}{f_b}$$

Table 4.2: THREE PHASE INDUCTION MOTOR PARAMETERS AT $f_b = 50$ Hz.

KW = 1.0	Volts = 415 V (line to line)	$I_{abc} = 2.0$A
RPM = 1275	$r_s = 7.5\ \Omega$	$r_r = 12.61\ \Omega$
$X'_{ls} = 12.94\ \Omega$	$X'_{lr} = 12.94\ \Omega$	$X'_M = 152.3\ \Omega$

$$\begin{aligned} X_{lr} &= X'_{lr}\frac{f}{f_b} \\ X_M &= X'_M\frac{f}{f_b} \end{aligned} \tag{4.87}$$

The equivalent impedance (Z_{eq}) is given by

$$Z_{eq} = r_{ls} + jX_{ls} + \frac{jX_M\left(\frac{r_r}{s} + jX_{lr}\right)}{\frac{r_r}{s} + j\left(X_{lr} + X_M\right)} \tag{4.88}$$

$$= R + jX \tag{4.89}$$

The equivalent resistance and inductance are given by

$$R = \Re(Z_{eq}) \tag{4.90}$$

$$L = \frac{\Im(Z_{eq})}{2\pi f} \tag{4.91}$$

In a current controller, one should give emphasis on the maximum switching frequency, MSF (f_{smax}) and total harmonic distortion (THD). The switching frequency determines stress on the inverter switches, whereas, the THD determines the quality of the load current. The switching frequency of the proposed new current controller (NEW-CC) is constant and is depicted as f_s. Hence for NEW-CC, MSF equals to f_s. Some performance data of the proposed new current controller along with other controllers are shown in Tables 4.3-4.5. For the hysteresis current controller (HCC), a band of $\beta = 0.1A$ is considered. The amplitude of the carrier of the ramp comparison controller (RCC) is chosen such that no high frequency multiple crossing occurs. The performance data for HCC and RCC are obtained by simulating standard schemes. A 3-phase induction motor with parameters shown in Table 4.2 is used as a load. Performances are studied at standstill and running conditions.

4.9.1 Performance at Standstill (Slip = 1.0)

Table 4.3 show the steady state behaviour at standstill (slip = 1.0) operation at a switching frequency of 720 Hz. The magnitude of THD indicates the total harmonic distortion at a given maximum switching frequency. A low value of THD is always desired, since it indicates a more smooth waveform having less harmonic contents and imparts better performance. A plot of THD is shown in Fig. 4.11. Keeping MSF constant at 720Hz, the distortion coefficient increases as the fundamental frequency f is increased. The increase in THD with fundamental frequency is linear. This happens since the number of pulses in a fundamental period decreases. For the entire frequency range (f=10Hz to 50Hz), NEW-CC have the lowest THD.

To see the effect of increasing the switching frequency (while the motor is at standstill condition, slip = 1.0), performance data are noted at f_s = 900Hz and shown in Table 4.4. In this case there is a slight increase in the maximum switching frequency of the RCC at higher fundamental frequencies. Plots of the distortion coefficient with fundamental frequency are shown in Fig. 4.12. The distortion coefficient (THD) for the RCC comes closer to the proposed NEW-CC at higher fundamental frequencies. But still the NEW-CC have the lowest THD. The effect of THD on switching frequency is clearly observed from Fig. 4.13. For a fixed fundamental, the THD at 900 Hz is less than that at 720Hz. This is true for NEW-CC, HCC, RCC and Predictive controller as well.

To see the effect of switching frequency on THD, the switching frequency is scaled for a normalized THD. The MSF at normalized THD would be given by

$$f_{sn} = \frac{\text{THD at a given MSF} \times \text{MSF}}{\text{Desired THD}} \tag{4.92}$$

where f_{sn} is the maximum switching frequency at the desired THD. A plot of f_{sn} versus fundamental frequency is shown in Fig. 4.14 for a THD of 0.025. From 4.14 it is clear that at standstill condition, for a given THD the proposed NEW-CC offers least MSF, whereas, the HCC offers the highest MSF. At a given THD the MSF increases as the fundamental frequency is increased in all controllers.

Table 4.3: PERFORMANCE DATA AT STEADY STATE OF THE NEW-CC AND OTHER CONTROLLERS: $V_s = 587V$, $I_m = 2.0A$, $f_s = 720Hz$, $\beta = 0.1$, SLIP = 1.0, FOR 1KW INDUCTION MOTOR.

f, Hz	THD				$f_s(max)$, Hz			
	NEW-CC	HCC	RCC	Predictive	NEW-CC	HCC	RCC	Predictive
10	0.0374	0.4477	0.0441	0.0507	720	720	720	720
15	0.0379	0.5305	0.0463	0.0686	720	720	720	720
20	0.043	0.5733	0.0485	0.0808	720	720	720	720
30	0.054	0.5618	0.0559	0.0987	720	720	722	720

Table 4.4: PERFORMANCE DATA AT STEADY STATE OF THE NEW-CC AND OTHER CONTROLLERS: $V_s = 587V$, $I_m = 2.0A$, $f_s = 900Hz$, $\beta = 0.1$, SLIP = 1.0, FOR 1KW INDUCTION MOTOR.

f, Hz	THD				$f_s(max)$, Hz			
	NEW-CC	HCC	RCC	Predictive	NEW-CC	HCC	RCC	Predictive
10	0.0325	0.3581	0.0395	0.0407	900	900	900	900
15	0.0307	0.4244	0.0416	0.055	900	900	900	900
20	0.0374	0.4586	0.0406	0.0649	900	900	909	900
25	0.0394	0.4597	0.0429	0.0723	900	900	900	900
30	0.045	0.4494	0.0462	0.0793	900	900	900	900
45	0.0528	0.4713	0.0544	0.0973	900	900	903	900
50	0.0552	0.4908	0.0569	0.1034	900	900	913	900

Table 4.5: PERFORMANCE DATA AT STEADY STATE OF THE NEW-CC AND OTHER CONTROLLERS: $V_s = 587V$, $I_m = 2.0A$, $f_s = 900Hz$, $\beta = 0.1$, SLIP $= 0.05$, FOR 1KW INDUCTION MOTOR.

f, Hz	THD				$f_s(max)$, Hz			
	NEW-CC	HCC	RCC	Predictive	NEW-CC	HCC	RCC	Predictive
10	0.0117	0.0667	0.0136	0.0178	900	900	900	900
15	0.0127	0.0660	0.0145	0.0238	900	900	900	900
20	0.0174	0.0675	0.0165	0.0286	900	900	910	900
25	0.0181	0.0651	0.0195	0.0321	900	900	913	900
30	0.0208	0.0750	0.0225	0.0345	900	900	916	900
45	0.0287	0.0689	0.033	0.0376	900	900	970	900
50	0.0317	0.0731	0.0368	0.0381	900	900	975	900

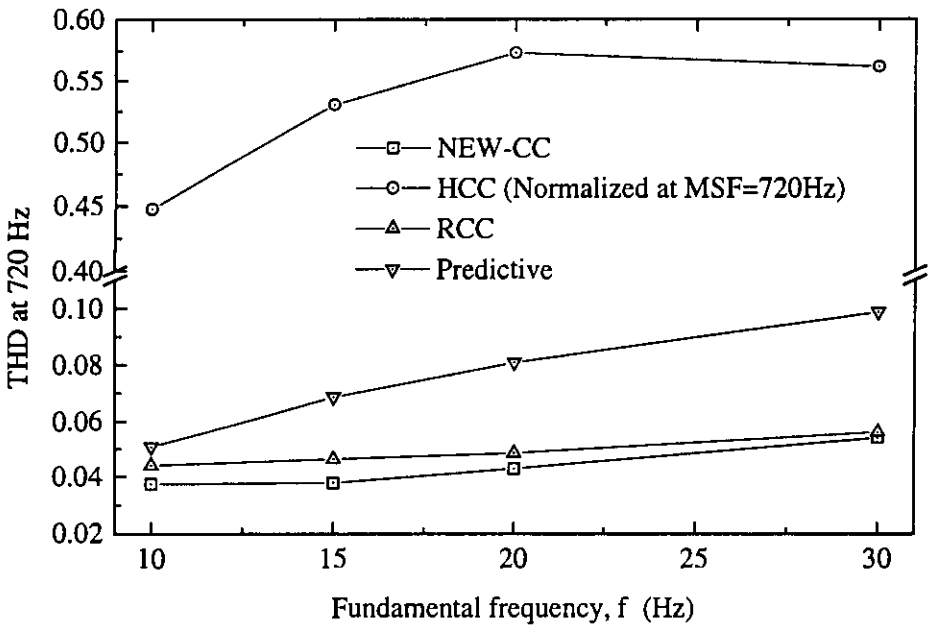

Fig. 4.11: THD at MSF = 720Hz for 1kW 3-phase induction motor load at unity slip.

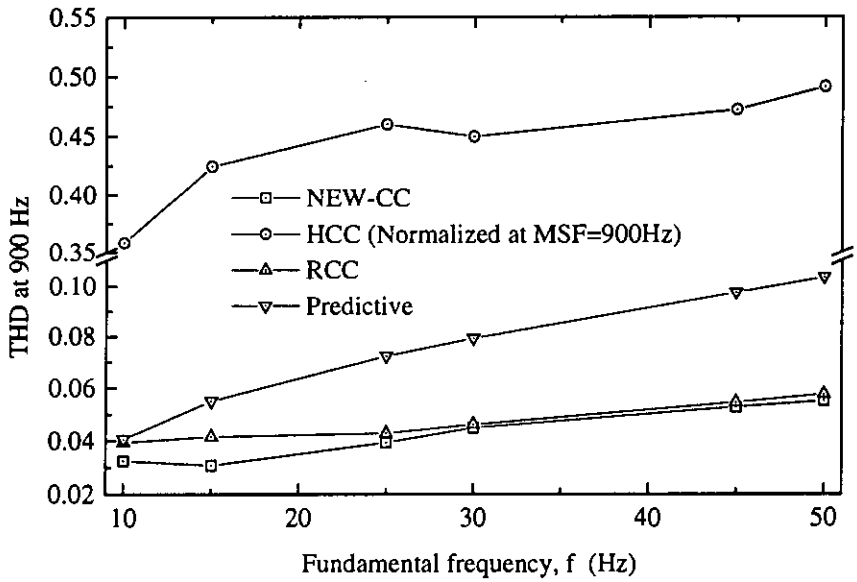

Fig. 4.12: THD at MSF = 900Hz for 1kW 3-phase induction motor load at unity slip.

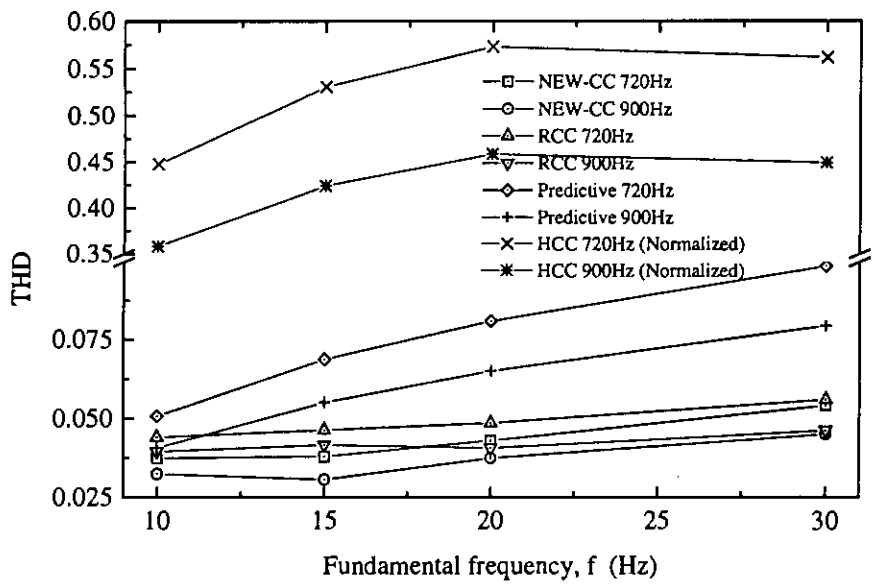

Fig. 4.13: THD at different switching frequencies at unity slip.

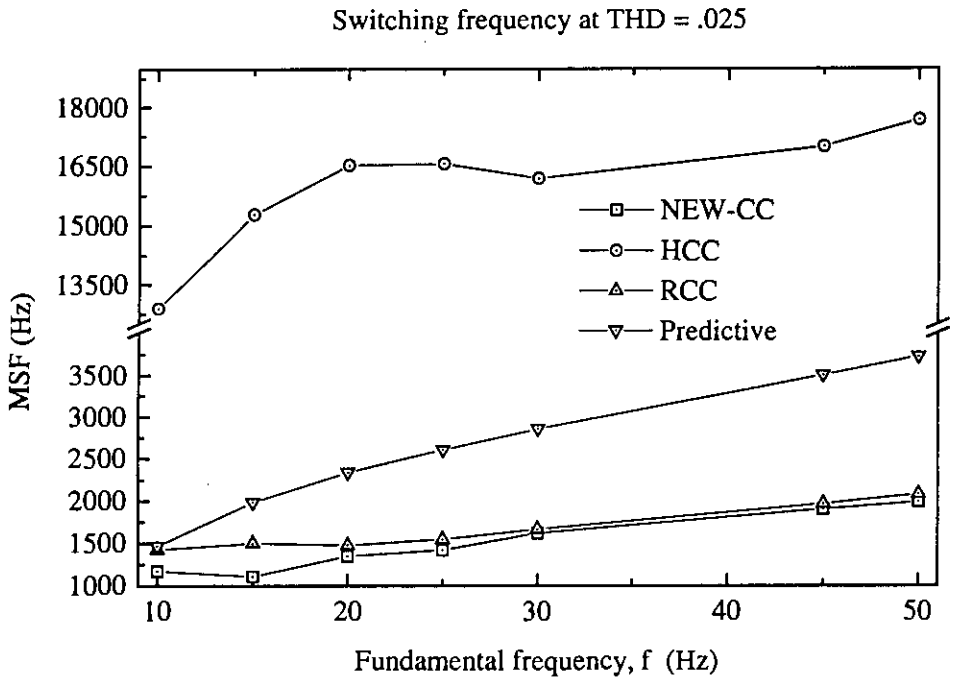

Fig. 4.14: Maximum switching frequency (MSF) curves at THD = 0.025 at unity slip for 1kW induction motor.

4.9.2 Performance at Running Condition (Slip = 0.05)

The running performance of the proposed NEW-CC along with other controllers are recorded at a slip of 0.05 and is given in Table 4.5. Plots of total harmonic distortion at 900Hz are shown in Fig. 4.15. In this case the HCC have the highest THD and the proposed NEW-CC have the lowest. The magnitude of THD at 5% slip is less than that was at 100% slip. At 50Hz the predictive controller has low THD than RCC.

Total harmonic distortions at 5% slip are plotted in Fig. 4.15 for MSF = 900Hz. At 50Hz, the THD of predictive controller is less than RCC but greater than NEW-CC. As the trend shows the predictive controller curve may cross the NEW-CC at some fundamental frequencies greater than the base frequency. This happens because of the limit of the input dc supply. The proposed controller don't get enough input voltage to force the load

current to follow the reference and hence change the pulse widths to 100%. Thus the output lose PWM pattern and at certain stage becomes a square wave.

However, since drives are operated at light load beyond the base frequency, the new controller would have low THD than predictive controllers. Another important point to be noted here is that as the slip decreases, the performance of predictive controller becomes better than RCC at higher fundamental frequencies. The performance of NEW-CC compared to RCC becomes more distinct as the motor slip decreases.

Fig. 4.16 shows the effect of THD on MSF as the fundamental frequency is increased. A similar trend like that at unity slip is observed. At unity slip, the difference in MSF's of NEW-CC and HCC were extremely large. But at 5% slip this difference is not that much high. For the same slip as the fundamental frequency increases, the difference between the MSF's of RCC and NEW-CC increases.

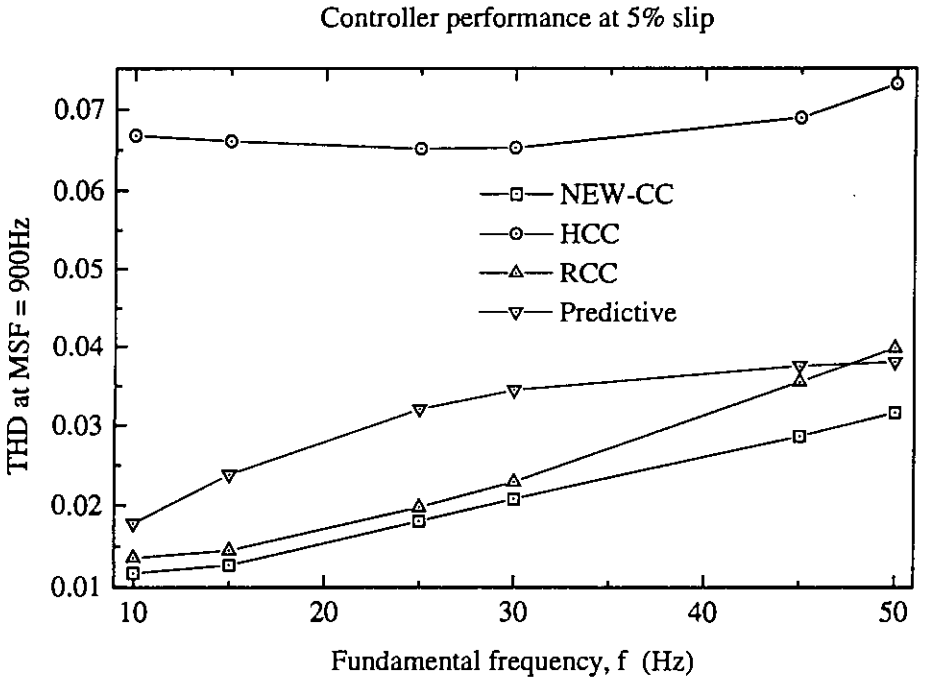

Fig. 4.15: THD at MSF = 900Hz at Slip = 0.05 for 1kW induction motor.

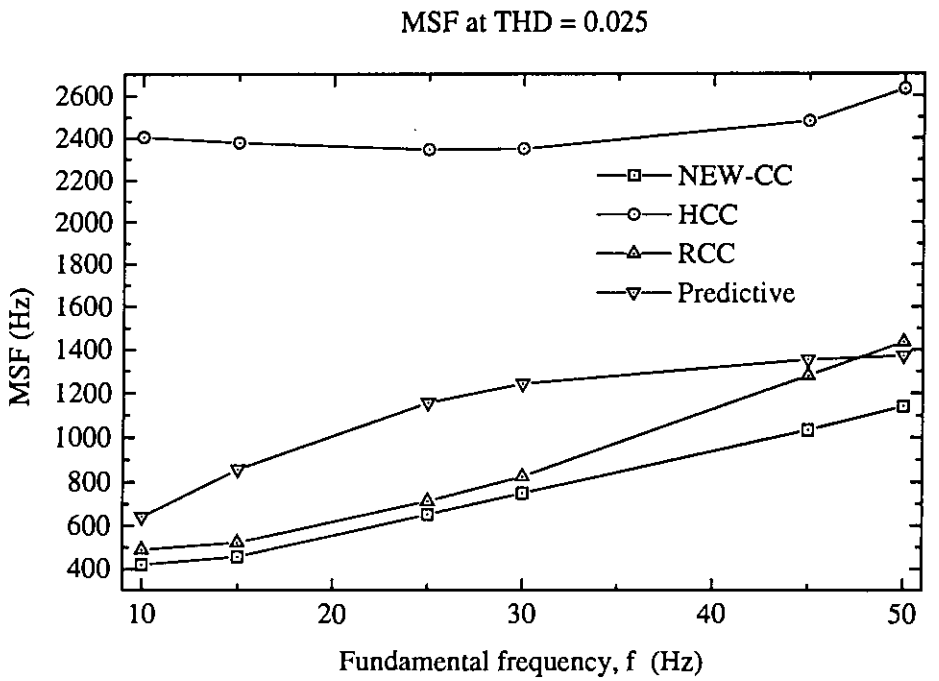

Fig. 4.16: MSF at THD = 0.025 at Slip = 0.05 for 1kW induction motor.

4.10 Steady State Waveforms of the NEW-CC

The dc input voltage of an inverter is normally derived from three phase ac mains by full wave rectification. A large capacitor is used at the rectifier output to hold the voltage at a constant value. For the 415V ac mains, the peak voltage is 587V. For this reason, steady state current waveforms are recorded for different frequencies with an inverter supply voltage of 587V. Fig. 4.17 shows the motor phase currents at 20Hz with a switching frequency of 900Hz. The corresponding switching waveform for inverter switch S_1 is shown in Fig. 4.18. As evident from the switching waveform, the switching frequency is uniform in all carrier cycles. Frequency spectrum of the load current is shown in Fig. 4.19. Harmonic contents upto 900Hz are absent in the current spectrum. This advantage is obtained due to the centre pulse modulation concept used in designing the new current controller. The centre pulse modulation technique produces double frequency waveform for the phase voltage in a Y-connected load.

The current ripple and associated phase A current are shown in Fig. 4.20. The peak value of current ripple is less than 0.1A, whereas, the total harmonic distortion is 0.0192. The position of the peak value of the current ripple depends on the power factor of the load. In this case it occurs near 45^0, 135^0, 225^0 and 315^0.

Steady state behaviour of the new current controller are experimentally studied with an inverter using MOSFETs. The inverter is controlled from a PC (Pentium 200MHz MMX). The inverter is designed with IRF540N MOSFETs and is supplied from a dc voltage source of 90V. The inverter can supply 2.0A to the test motor (upto 25Hz) in blocked rotor mode. Typical experimental waveforms along with simulated ones are shown in Figs. 4.21 - 4.26. The experimental waveforms are close to the simulated ones. No significant discrepancies are observed between the experimental and simulated current waveforms.

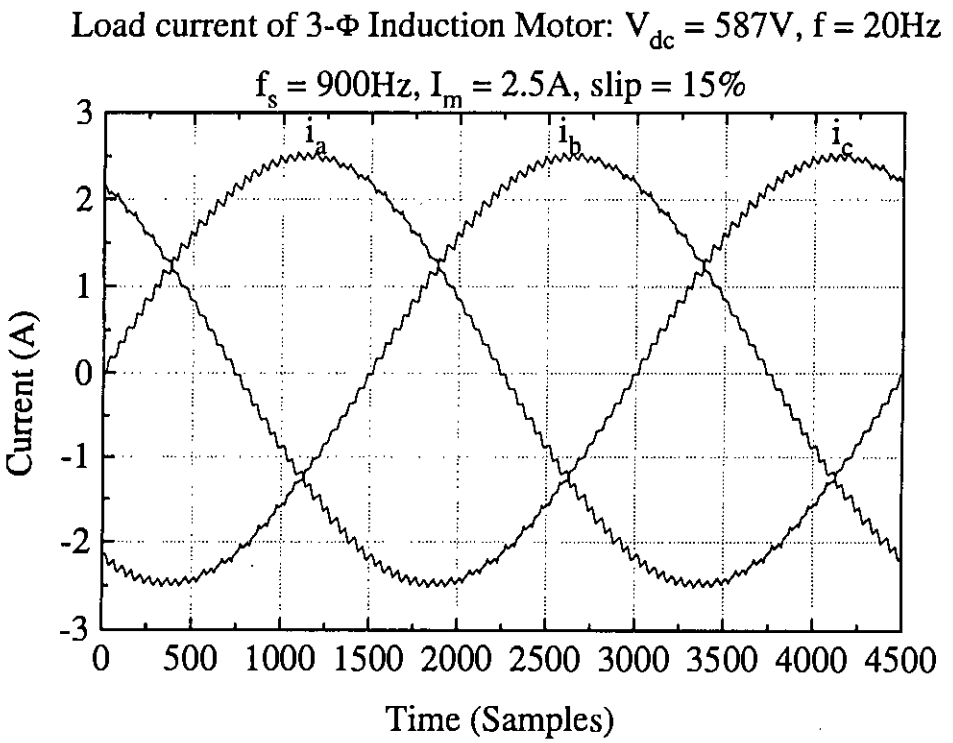

Fig. 4.17: Motor phase currents at Slip = 0.15 with V_s = 587V, f = 20Hz, f_s = 900Hz, I_m = 2.5A

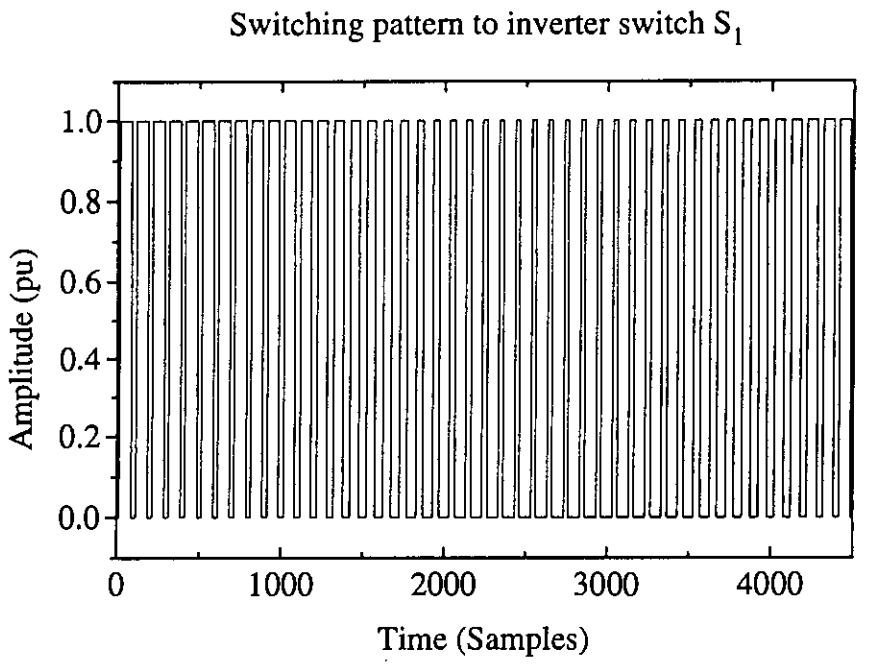

Fig. 4.18: Switching waveform of S_1 of the inverter at Slip = 0.15 with V_s = 587V, f = 20Hz, f_s = 900Hz, I_m = 2.5A

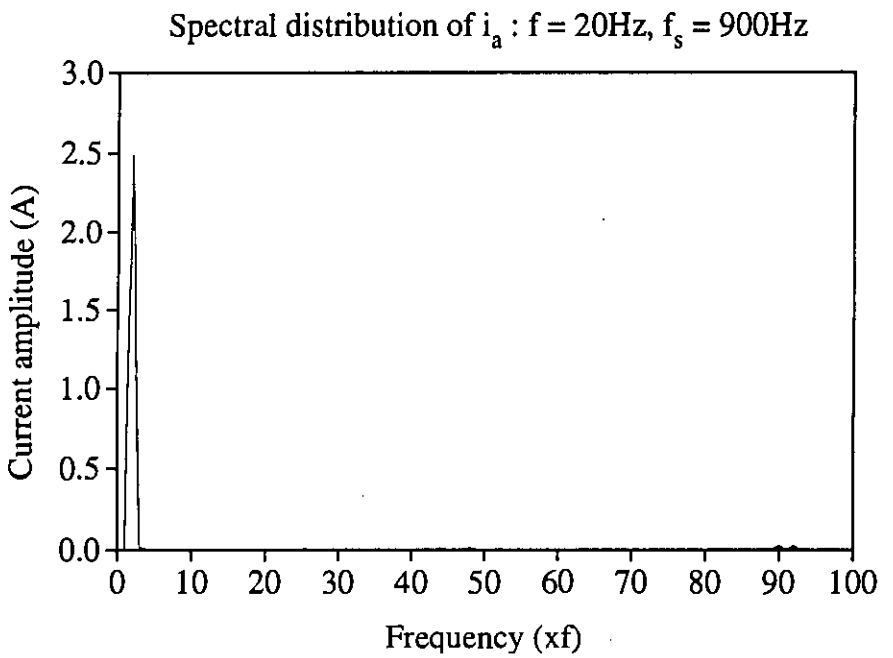

Fig. 4.19: Spectrum of motor phase current at Slip = 0.15 with V_s = 587V, f = 20Hz, f_s = 900Hz, I_m = 2.5A

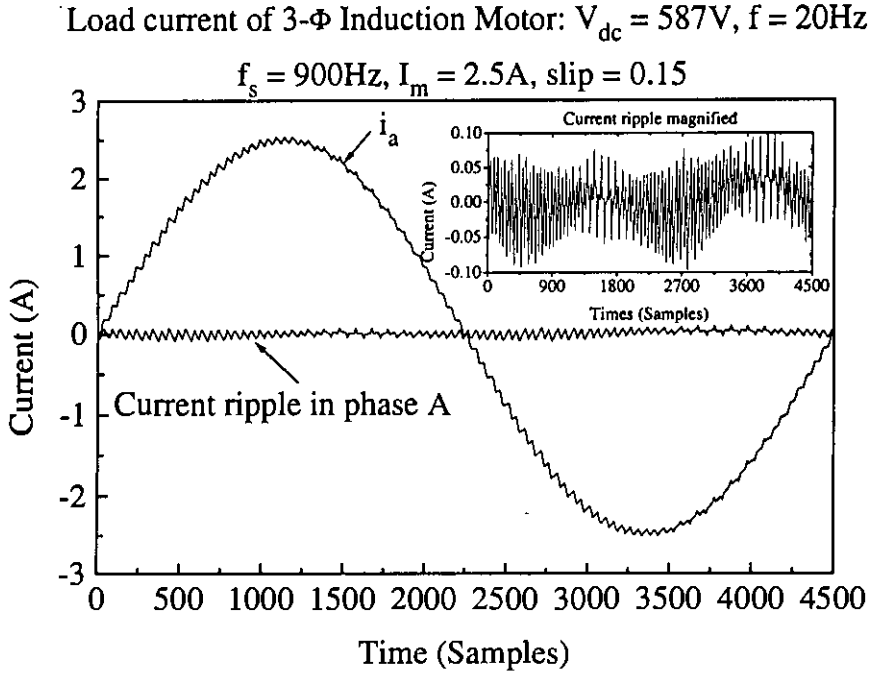

Fig. 4.20: Motor phase current and current ripple at Slip = 0.15 with V_s = 587V, f = 20Hz, f_s = 900Hz, I_m = 2.5A.

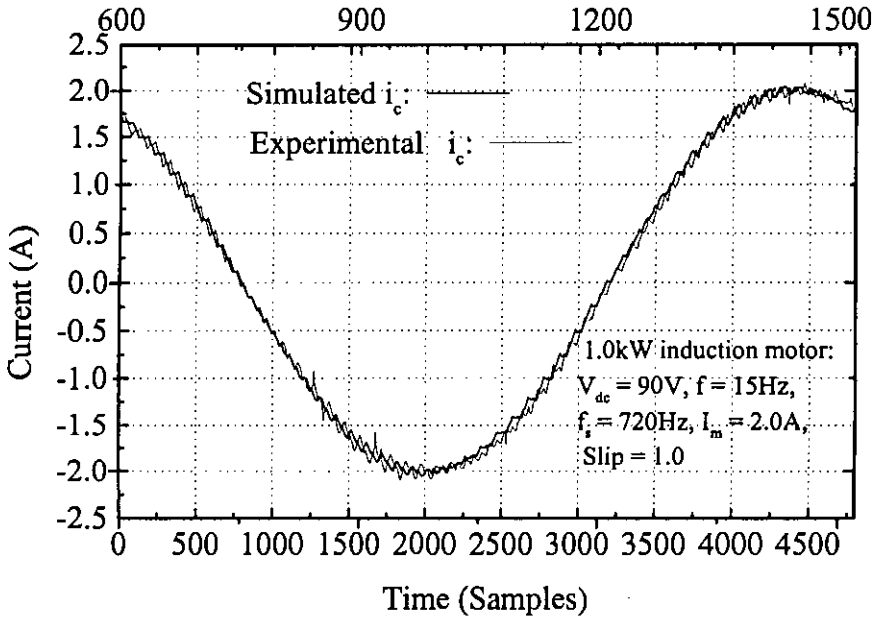

Fig. 4.21: Simulated and experimental load current for i_c at Slip = 1.0 with V_s = 90V, f = 15Hz, f_s = 720Hz, I_m = 2.0A.

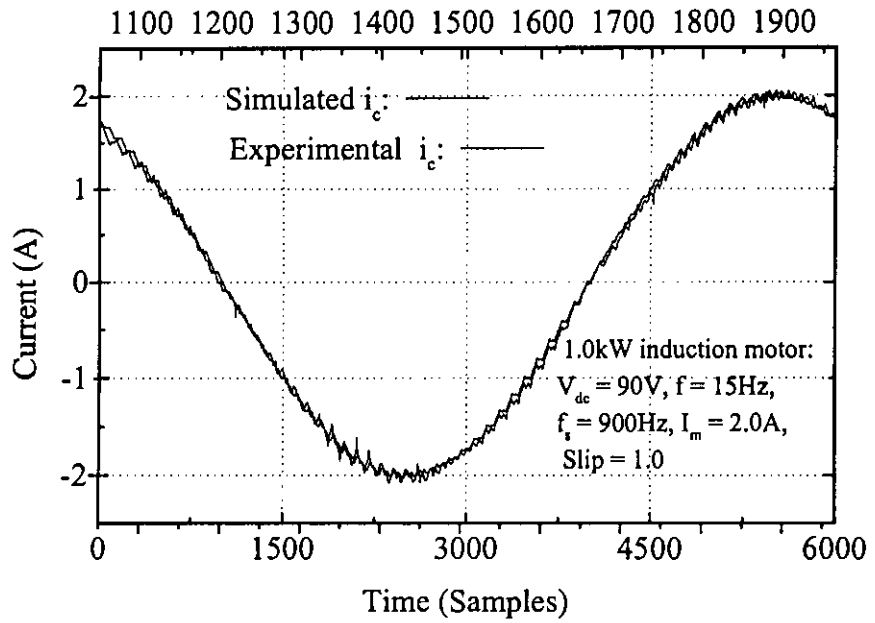

Fig. 4.22: Simulated and experimental load current for i_c at Slip = 1.0 with V_s = 90V, f = 15Hz, f_s = 900Hz, I_m = 2.0A.

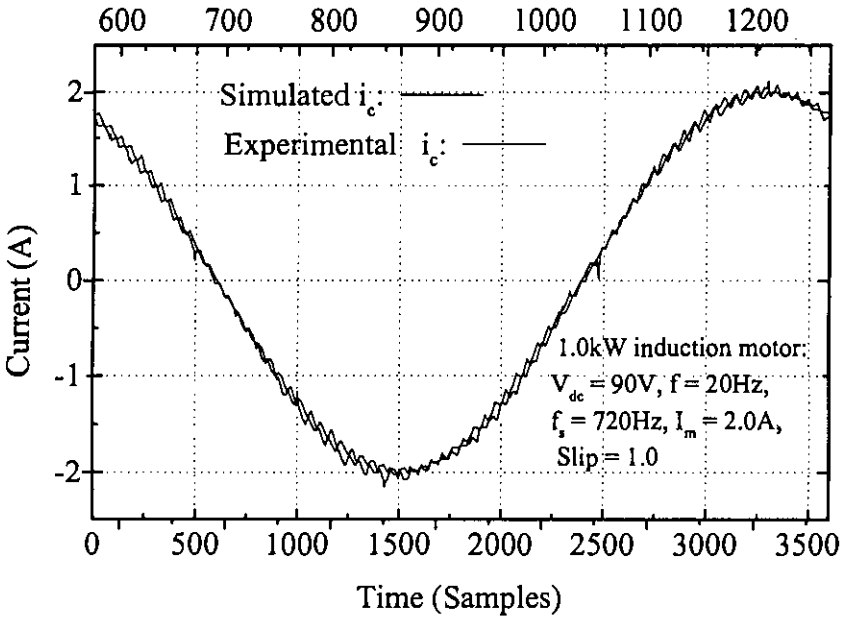

Fig. 4.23: Simulated and experimental load current for i_c at Slip = 1.0 with V_s = 90V, f = 20Hz, f_s = 720Hz, I_m = 2.0A.

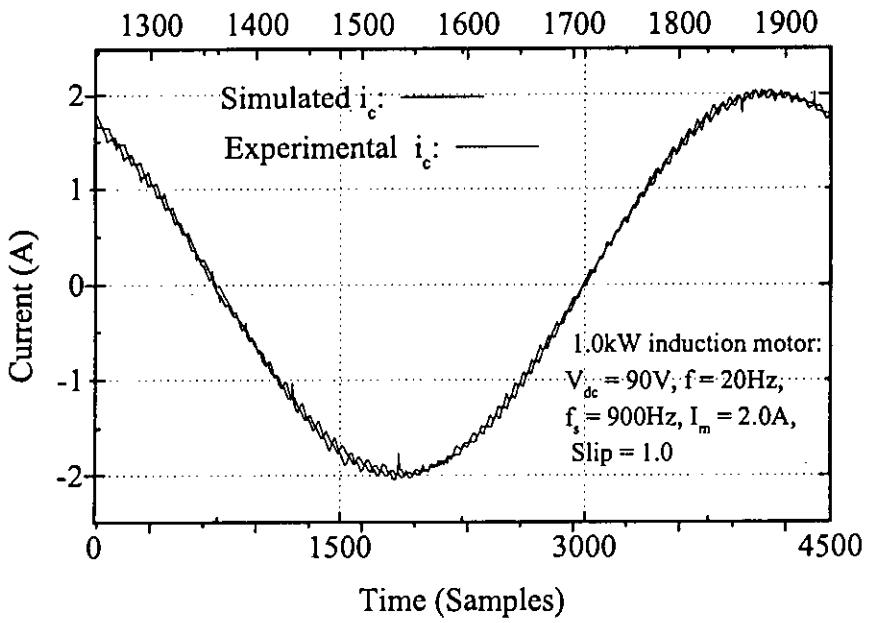

Fig. 4.24: Simulated and experimental load current for i_c at Slip = 1.0 with V_s = 90V, f = 20Hz, f_s = 900Hz, I_m = 2.0A.

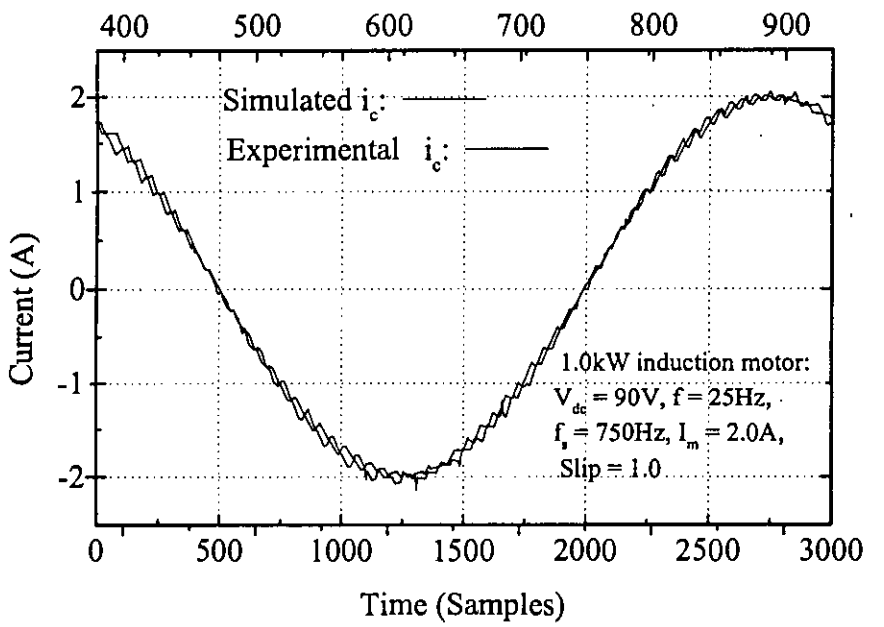

Fig. 4.25: Simulated and experimental load current for i_c at Slip = 1.0 with V_s = 90V, f = 25Hz, f_s = 750Hz, I_m = 2.0A.

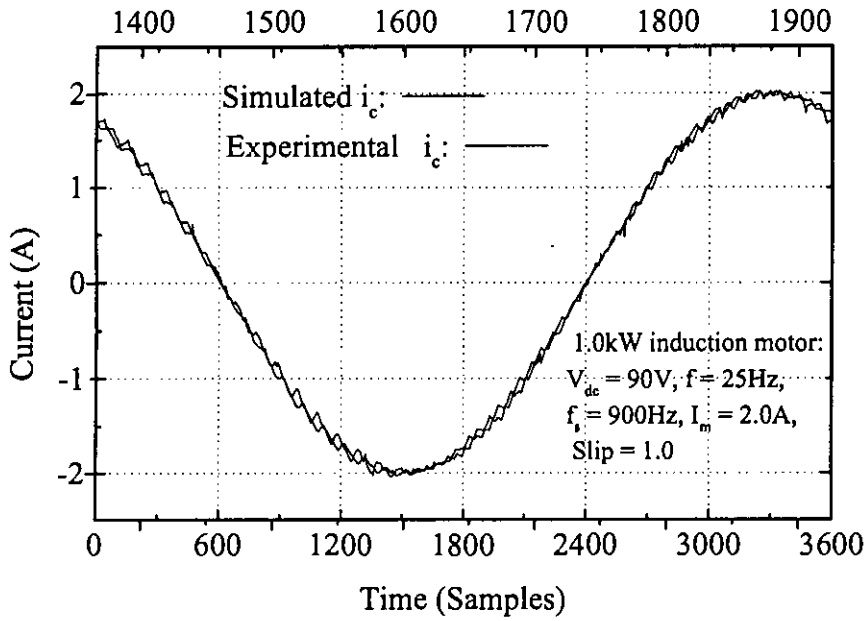

Fig. 4.26: Simulated and experimental load current for i_c at Slip = 1.0 with V_s = 90V, f = 25Hz, f_s = 900Hz, I_m = 2.0A.

4.11 Start-up Waveforms

The start-up current waveforms of the new controller are recorded with V_s = 587V, I_m = 2.5A, f = 20Hz and f_s = 900Hz. Three phase load currents, current ripples of phase A and switching pattern to S_1 are presented in Figs. 4.27, 4.28 and 4.29 respectively. As evident from Fig.4.27, the load currents in all three phases quickly adopts the respective reference currents. The start-up response time is less than 10^0 and is an indication of fast response. Some experimental waveforms are shown in Figs. 4.30-4.35 with an inverter supply of 90V. Waveforms are recorded at 15Hz, 20Hz and 25Hz at different switching frequencies. Currents are taken from three CT's connected in series with the load. Load currents of phases A and B are occupied by the controller. Phase C is not used by the controller. Hence experimental waveforms are presented for phase C current. From Figs. 4.30-4.35 it is observed that the experimental starting current waveforms follow the theoretical ones after about 30^0 from starting point. This happens because of the dc link inductance of the inverter. For this reason experimental inverters are built with very short dc link.

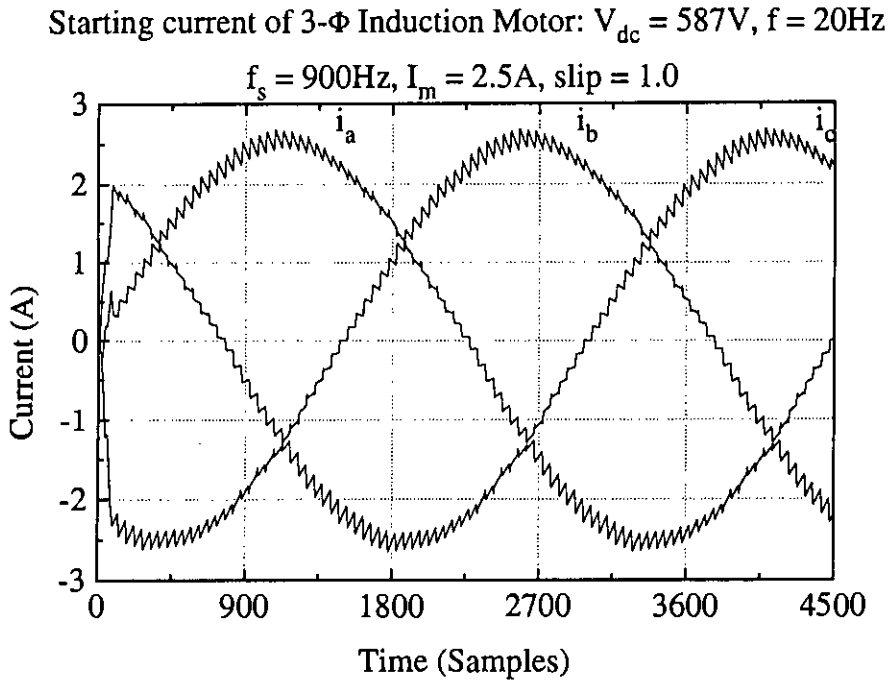

Fig. 4.27: Motor starting current (Slip = 1.0) with V_s = 587V, f = 20Hz, f_s = 900Hz, I_m = 2.5A.

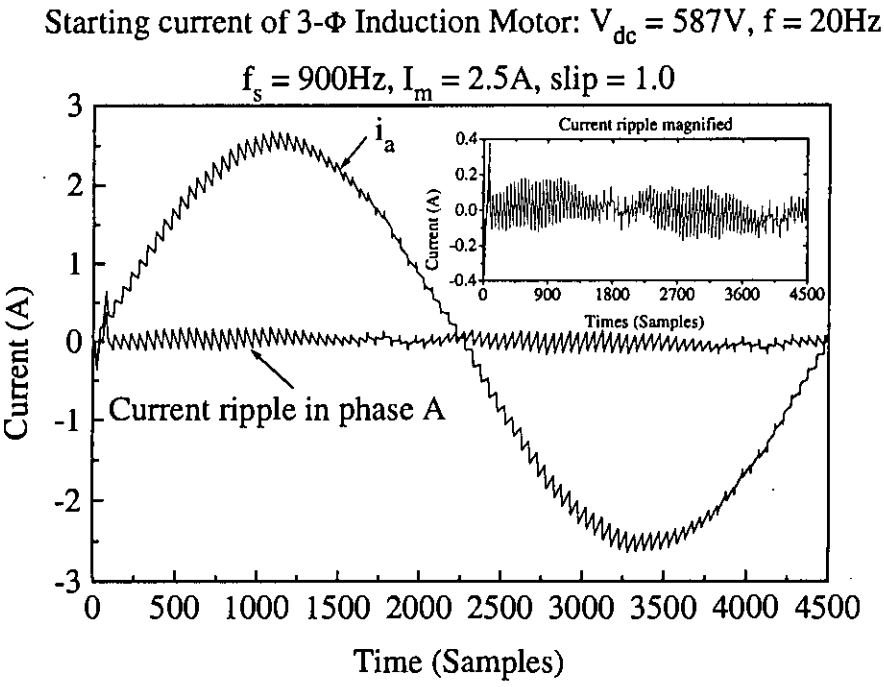

Fig. 4.28: Starting phase current and current ripple (Slip = 1.0) with V_s = 587V, f = 20Hz, f_s = 900Hz, I_m = 2.5A.

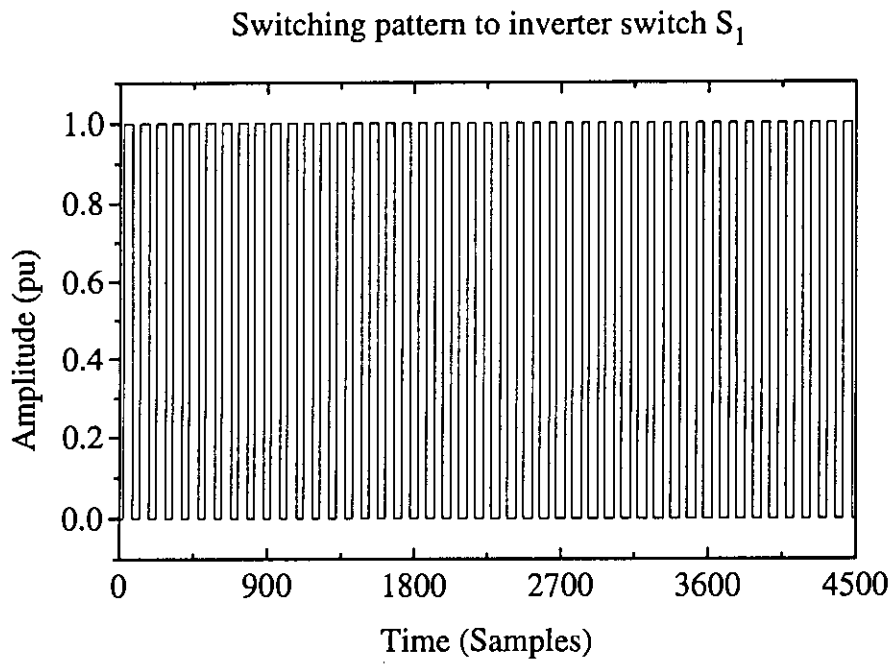

Fig. 4.29: Start-up switching pattern of S_1 (Slip = 1.0) with V_s = 587V, f = 20Hz, f_s = 900Hz, I_m = 2.5A.

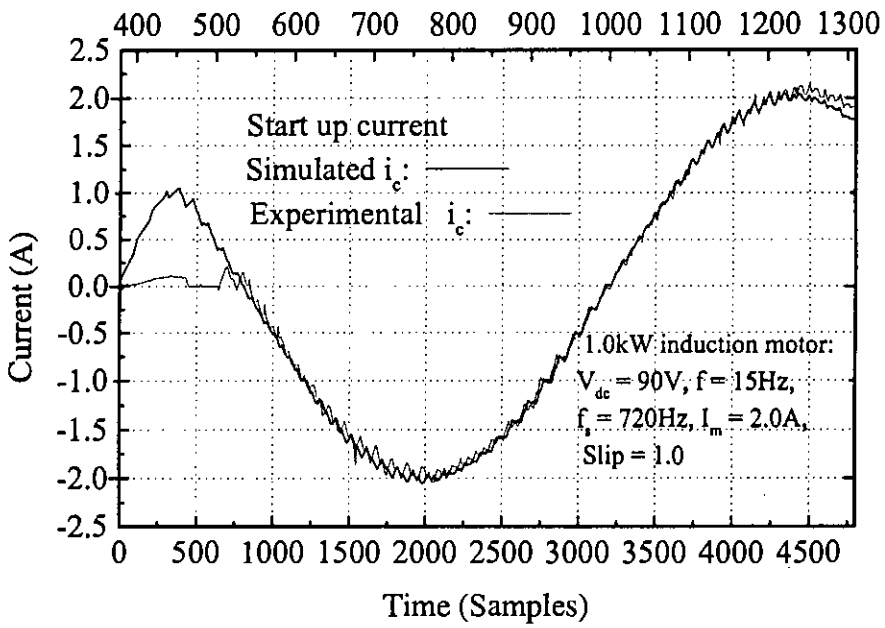

Fig. 4.30: Experimental start-up current waveform of i_c at Slip = 1.0 with V_s = 90V, f = 15Hz, f_s = 720Hz, I_m = 2.0A.

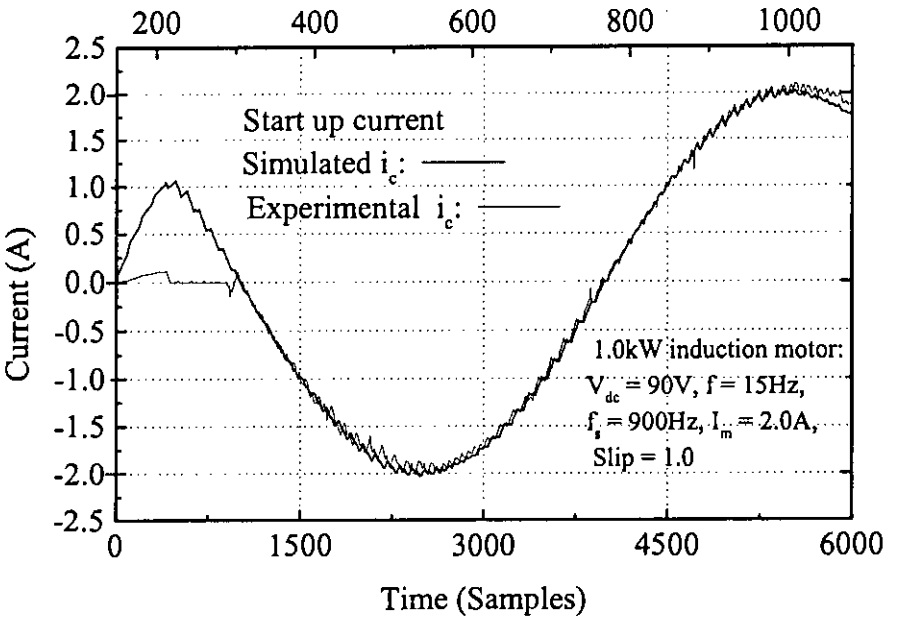

Fig. 4.31: Experimental start-up current waveform of i_c at Slip = 1.0 with V_s = 90V, f = 15Hz, f_s = 900Hz, I_m = 2.0A.

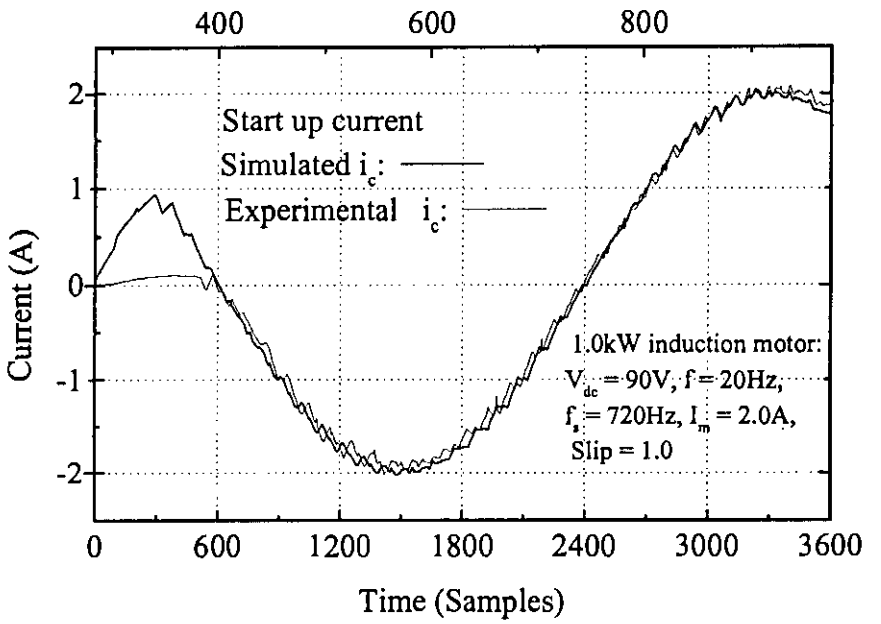

Fig. 4.32: Experimental start-up current waveform of i_c at Slip = 1.0 with V_s = 90V, f = 20Hz, f_s = 720Hz, I_m = 2.0A.

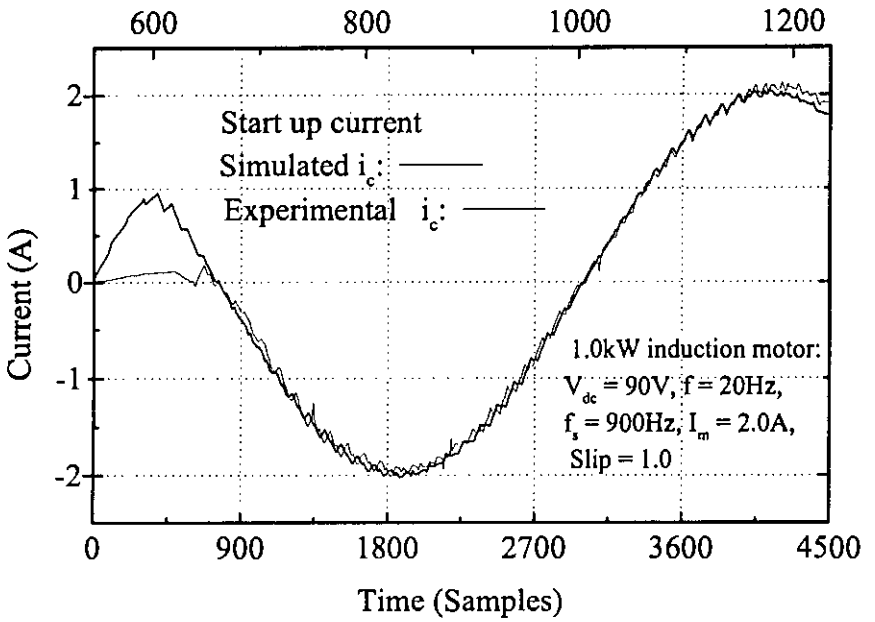

Fig. 4.33: Experimental start-up current waveform of i_c at Slip = 1.0 with V_s = 90V, f = 20Hz, f_s = 900Hz, I_m = 2.0A.

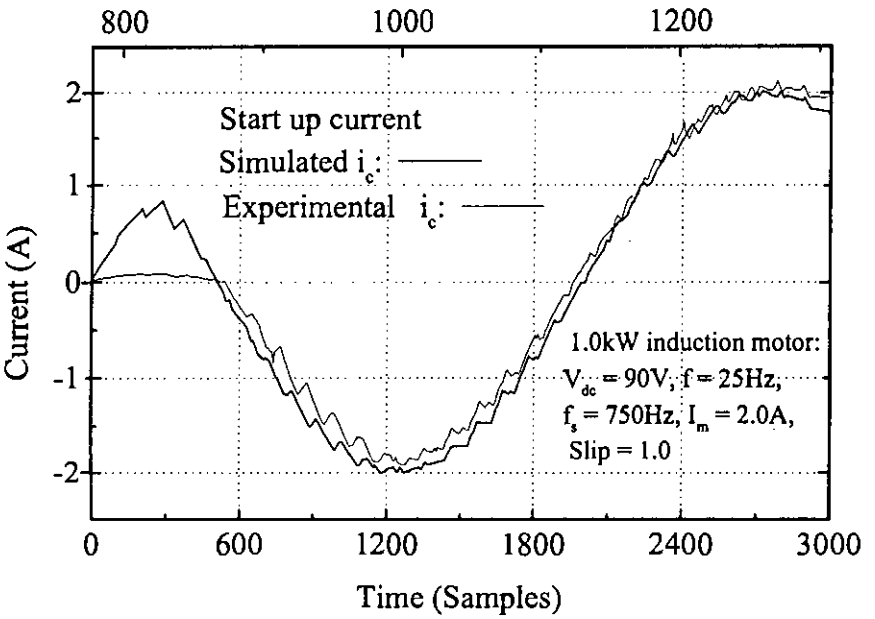

Fig. 4.34: Experimental start-up current waveform of i_c at Slip = 1.0 with V_s = 90V, f = 25Hz, f_s = 750Hz, I_m = 2.0A.

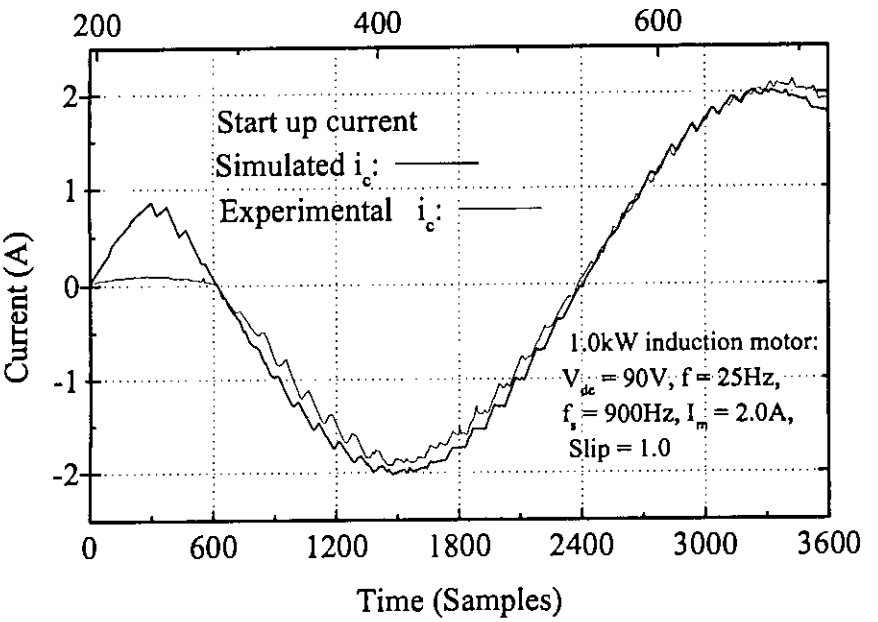

Fig. 4.35: Experimental start-up current waveform of i_c at Slip = 1.0 with V_s = 90V, f = 25Hz, f_s = 900Hz, I_m = 2.0A.

4.12 Dynamic Response

The response of the new current controller for a step change in reference currents are studied with an inverter supply of 90V. Experimental waveforms are recorded at 15Hz, 20Hz and 25Hz at different switching frequencies (f_s = 720Hz,750Hz and 900Hz). The reference current is changed from I_m = 1.5A to 2.0A (i.e., $i = 1.5\sin(\omega t+\theta)$ to $2.5\sin(\omega t+\theta)$).

The experimental waveforms and the corresponding simulated waveforms are inserted in the same plot. From Figs. 4.36-4.41 it is evident that the experimental waveforms are close to the simulated waveforms. The step response of the new current controller is excellent. Other dynamic responses like step change in impedance could not be tested because of experimental limitations.

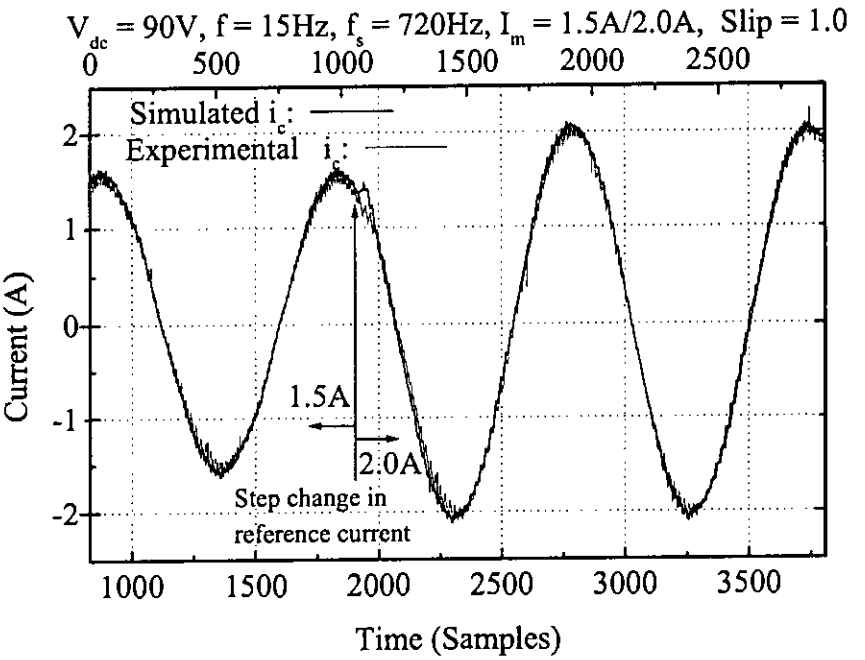

Fig. 4.36: Experimental current waveform of i_c with a step change in current reference from I_m = 1.5A to 2.0A (Slip = 1.0, V_s = 90V, f = 15Hz, f_s = 720Hz.)

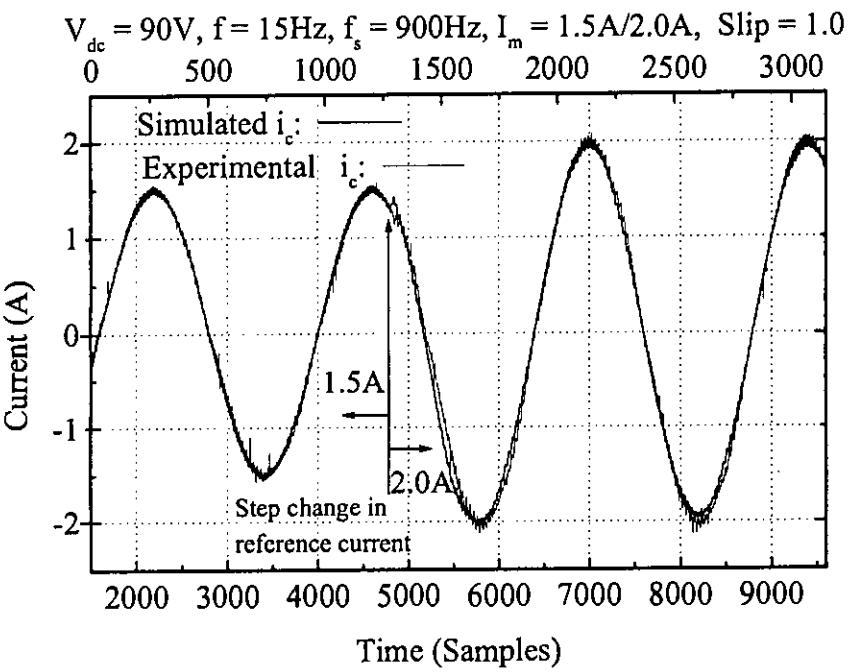

Fig. 4.37: Experimental current waveform of i_c with a step change in current reference from I_m = 1.5A to 2.0A (Slip = 1.0, V_s = 90V, f = 15Hz, f_s = 900Hz.)

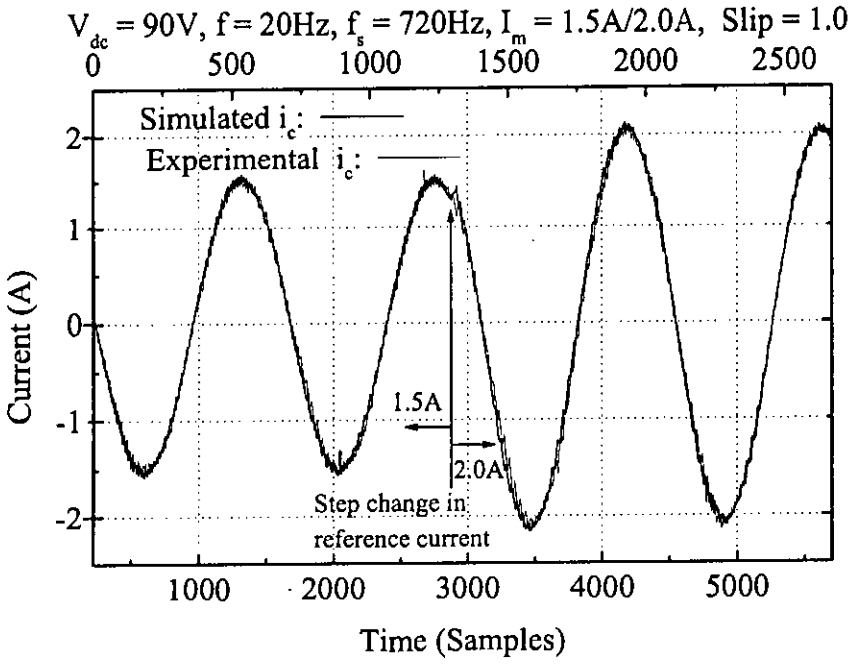

Fig. 4.38: Experimental current waveform of i_c with a step change in current reference from I_m = 1.5A to 2.0A (Slip = 1.0, V_s = 90V, f = 20Hz, f_s = 720Hz.)

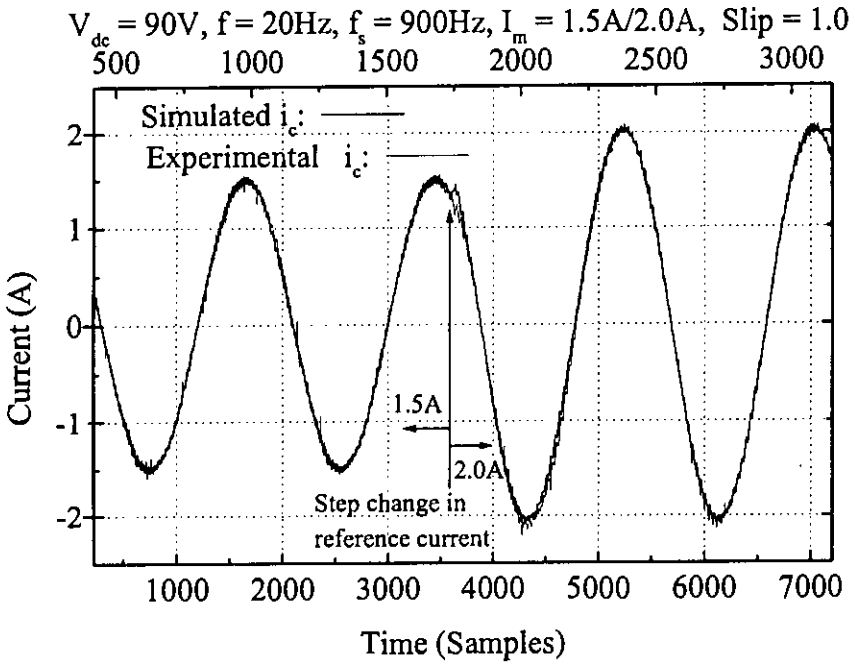

Fig. 4.39: Experimental current waveform of i_c with a step change in current reference from I_m = 1.5A to 2.0A (Slip = 1.0, V_s = 90V, f = 20Hz, f_s = 900Hz.)

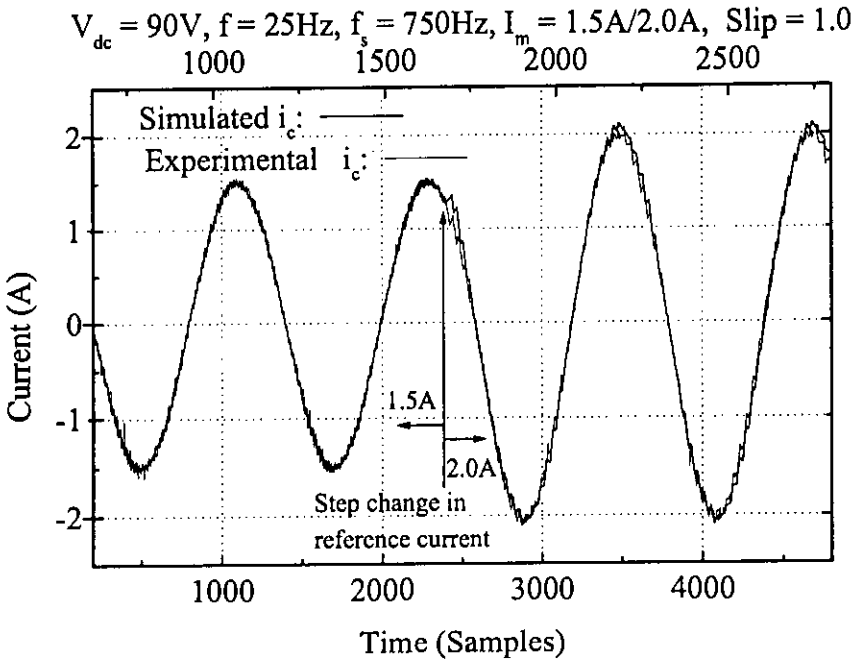

Fig. 4.40: Experimental current waveform of i_c with a step change in current reference from I_m = 1.5A to 2.0A (Slip = 1.0, V_s = 90V, f = 25Hz, f_s = 750Hz.)

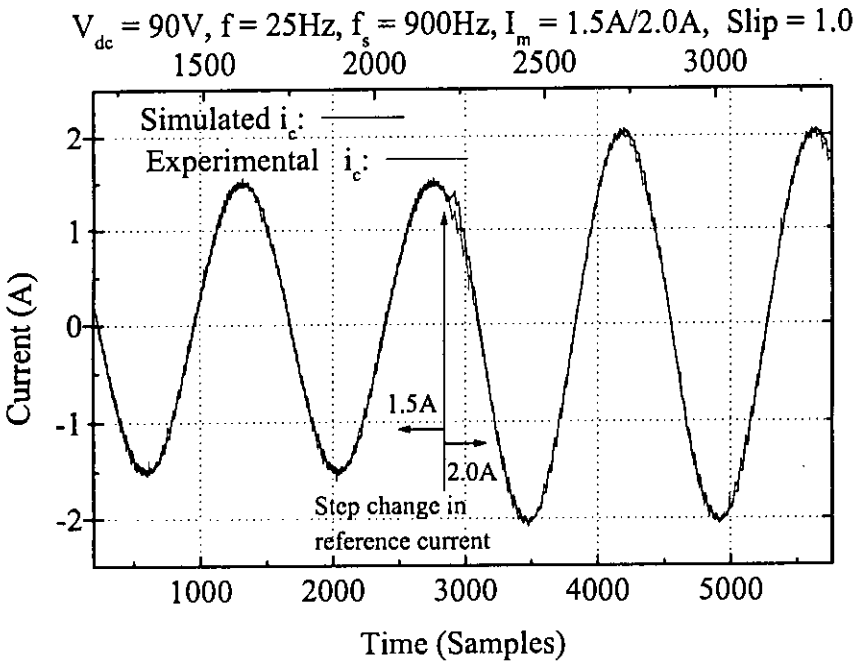

Fig. 4.41: Experimental current waveform of i_c with a step change in current reference from I_m = 1.5A to 2.0A (Slip = 1.0, V_s = 90V, f = 25Hz, f_s = 900Hz.)

4.13 Comparison of the NEW-CC with Other Conventional Current Controllers

A comparison of the NEW-CC is made with conventional HCC, RCC and Predictive controllers. The start-up, steady state and dynamic performances are studied. The steady state comparison are shown in Table 4.6 for a 1kW IM at f = 50Hz, V_{dc} = 587V, I_m = 2.0A, f_s = 900Hz and β = 0.2A. It is observed that the steady state performance of NEW-CC, RCC and Predictive controllers are better than HCC. The NEW-CC shows better performance than all other current controllers.

The dynamic performance are studied to see how these controllers behave for step change in reference and also for step change in load. The dynamic performance data are shown in Table 4.7. The time required to adapt the new reference is considered in the case of step change in reference current.

The response of NEW-CC is pretty good (100 μs) and comparable to HCC and RCC. For a step change in load, the HCC and RCC have burst switching effect, however, there is no overshoot in the load current. In case of predictive controller, the switching frequency is constant (900Hz), however, there is an overshoot of 22.5% in the load current. For the NEW-CC, the switching frequency is constant and there is a nominal overshoot of 10%.

The start-up data are shown in Table 4.8 for a 1kW IM at f = 25Hz. The startup time of NEW-CC is pretty good and comparable to HCC and PRC.

Table 4.6: STEADY STATE PERFORMANCE COMPARISON OF THE NEW-CC WITH THE EXISTING CURRENT CONTROLLERS.

Criteria	HCC	RCC	Predictive	NEW-CC
THD at 15% slip	0.112	0.0558	0.0883	0.0534
MSF at 15% slip	1.8kHz	900Hz	900Hz	900Hz
Sub-harmonic effect	Yes	Yes	No	No

Table 4.7: DYNAMIC STATE PERFORMANCE COMPARISON OF NEW-CC WITH HCC, RCC AND PREDICTIVE CONTROLLERS.

Criteria	HCC	RCC	Predictive	NEW-CC
Step change in Ref. I_m = 1A to 2A	90 μs	100 μs	80 μs	100 μs
Step change in Load slip = 15% to 30%	No overshoot 6kHz	No overshoot 51kHz	Overshoot 0.45A (900Hz)	Overshoot 0.2A (900Hz)

Table 4.8: START-UP PERFORMANCE COMPARISON OF NEW-CC WITH HCC, RCC AND PREDICTIVE CONTROLLERS.

Criteria	HCC	RCC	Predictive	NEW-CC
Startup Time (μs)	87	97	77	100

4.14 Conclusion

The new and novel current controller, presented in this chapter, is realized from information of the load parameters and the inverter supply voltage. This current controller regularly samples the reference command currents at the switching frequency. It generates a sequential pulse stream which forces the load current to follow the command current reference. Normally (during steady state condition) the controller estimates the load equivalent R-L parameters on fundamental cycle basis. In case of dynamic states (sudden load change), it estimates R-L parameters on carrier cycle basis. Separate loops are added in the controller scheme for startup, steady state and dynamic state of operation. Addition of these loops for different operating conditions improves the controller performance. The steady state and dynamic states are sensed by a three level hysteresis comparator that compares the instantaneous load current vector with the reference one. In case of load change the controller computes the switching pulses with the new load parameters, ensuring good performance during dynamic loading.

The start-up and dynamic loading performance of the NEW-CC is comparable to HCC and RCC. The superiority of the new controller to other controllers is that it operates at

constant switching in dynamic conditions with only 10% current overshoot. The steady state performance of the new controller is better than all other controllers and it has the lowest THD.

The new current controller discussed in this chapter shows good all round performance. Performances at different operating conditions are tested in the laboratory on a prototype inverter driven from a 90V source. Due to limitation on dc input voltage, the controller can not supply rated current to the load at frequencies greater than 25 Hz. For this reason the operation of the controller upto 25Hz (at rated current) are tested. However, simulations are shown for full operating range. Experimental current waveforms at different operating conditions are close to the theoretical (simulated) waveforms showing effectiveness of the proposed controller. Slight deviation of the experimental result from the simulated one is due to the fact that lockout time is neglected in the simulation. The computational requirement of the controller is simplified and hence can be applied to any three phase balanced load or ac motor drives economically.

Chapter 5

Conclusions

5.1 Conclusion

Current controllers play an important role in modern voltage source inverters for their performances. Because of the peak current limiting feature of current controlled PWM there is no risk of secondary or avalanche breakdown of the inverter switches. However, the conventional hysteresis current controllers which offer fast dynamic responses have the drawback of non-uniform switching. As a result during the worst conditions, the heating losses associated with high frequency switching may cause thermal breakdown due to increased switching losses. In this thesis, different approaches are proposed to solve the problem of non-uniform switching. Different current controllers are studied for use with voltage source inverters. Analysis shows that the switching frequency is dependent on the load parameters, reference current waveform and the supply voltage of the inverter.

An analysis of the conventional HCC is made in chapter 2. The switching frequency is found to be a time varying function. It is observed that the switching frequency becomes time independent by addition of a triangular carrier of programmed amplitude to the sinusoidal reference current. The proposed technique, designated as programmed ramp comparison controller (PRC), is studied in detail for start-up, steady state and dynamic performances. In steady state, the switching frequency of PRC is almost constant and it has low THD than the HCC for the same maximum switching frequency. The start-up and dynamic responses of PRC is comparable with HCC. Both HCC and PRC is

seen to have burst switching effects in case of dynamic loading. Besides, both HCC and PRC have sub-harmonic effects because of the natural sampling process involved in the implementation.

Sub-harmonic effects are almost unavoidable in case of all naturally sampled current controllers. Regular sampled current controllers do not have the problems of sub-harmonic effects because of the symmetric PWM patterns. The predictive controllers operate on regular sampled basis and have constant switching frequency. However, the predictive controller have high current ripples during large disturbances. A detail analysis of the predictive controller is made in chapter 3. It is observed that the current overshoots during large disturbances can be reduced by addition of a vector limiter. The performance of the modified predictive controller is studied for the normal operating conditions as well as for large disturbances. Significant improvement is observed in the proposed modification. However, the THD of the predictive controller is found to be higher when compared to the PRC.

Although, the PRC has less THD than the predictive controller, due to the burst switching effect and sub-harmonic contents it is not feasible for high performance current control applications.

The salient advantages of PRC and predictive controller have been accommodated in the new controller described in chapter 4, discarding their inherent disadvantages. The new current controller (NEW-CC) is developed using the regular sampling strategy. Instead of waiting for a natural switching edge like PRC or HCC (that leads to the introduction of sub-harmonics), in the NEW-CC the duration of the PWM pulse is predicted once in each carrier period so that the load current follow the reference current profile which is a sinusoid. The prediction of the PWM pulse width is based on the load parameters (R-L), reference current and inverter supply voltage. Scalar type prediction process are adopted and pulse width for three phases are computed separately. In transient states, the pulse widths for the three phase becomes un-correlated. Thus NEW-CC have better control over the load current during transient states and hence the current overshoot during large disturbance is small compared to predictive controller.

Detailed design procedure is presented for the NEW-CC that includes switching edges

computations and generation of six state switching patterns for real time implementation. Besides, analytical formulas have been developed for estimation of current ripple. A PC based scheme is developed for implementation of the NEW-CC. The NEW-CC scheme needs information of the load parameters with reasonable accuracy. Separate on-line R-L parameter estimation schemes are proposed for steady state and dynamic states respectively. The R-L parameter estimation process, responsible for steady state conditions, is computed on the basis of the fundamental voltage, fundamental load current and their phase shift. In case of dynamic loading, the R-L parameters are estimated on carrier cycle basis. The steady state and dynamic states of the controller are differentiated by comparing the overall load current vector to a three level hysteresis comparator.
The performance of the NEW-CC is studied for different operating conditions. It gives the lowest total harmonic distortion among all the conventional current controllers (including HCC, RCC and Predictive Controllers). The startup and dynamic responses are found pretty well and comparable to other conventional controllers. The new current controller is experimentally tested on an inverter drive. The experimental results are found very close to the theoretical ones. The NEW-CC gives smooth operation of the motor and do not destabilize as is observed in case of RCC and HCC.

5.2 Future Works

Having reviewed the contributions made in this thesis, there are ample opportunity and scope of extending this work in future to meet other goals.

- The proposed current controllers need equivalent load parameters. In this thesis, the parameter estimation blocks are integrated in the implementation schemes. Due to limitations on sampling frequencies of A/D converter, and the program control approach adopted in this thesis, the PWM waveforms deviate from ideal ones. For high power drives it may affect the overall performance. Future schemes may be investigated using DSP boards with complex direct memory access (DMA) strategies.

- Multimedia approach can be considered in future for practical implementation of the current controllers for use with PCs. In this approach a VLSI chip may be designed

which would integrate most functional blocks of the current controller, where, the PC would be used as a supervisor only. This type of approach would reduce the computational burden on the PC and allow remote control through networks.

- Neural and fuzzy based schemes may be investigated as future works on current controllers. Large number of PWM switching patterns may be stored in look up tables based on off-line computations on dynamic and steady state load models. A neuro-fuzzy algorithm may be used for selection of the switching table.

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