QUANTUM MECHANICAL MODELING OF CHARGE TRAPPING/DETRAPPING PHENOMENA IN CMOS DEVICES WITH HIGH-k STACK GATE DIELECTRICS

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2007

#104319#

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A thesis submitted to
The Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology, Dhaka, Bangladesh
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
2007

The thesis titled "**Quantum Mechanical Modeling of Charge Trapping/Detrapping Phenomena in CMOS Devices with High-K Stack Gate Dielectrics**", submitted by Khan Mohammad Farhan Shahil, Roll No: 100506240P, Session: October 2005 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of Master of Science in Electrical and Electronic Engineering on July 28, 2007.

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ACKNOWLEDGMENT

The author likes to express his sincere gratitude and respect to his supervisor Dr. Quazi Deen Mohd Khosru, Professor, Department of EEE, BUET for his sincere guidance and supervision throughout the work. He is thankful to the Dr. Satya Prasad Majumder, Professor, Head, Dept. of EEE, and BUET for his support and kind co-operation.

The author wishes to express his profound indebt ness to Dr. M. Rezwan Khan, Professor and Vice chancellor, United International University (UIU), and Dr. Anisul Haque, Professor and Chairperson, Dept. of EEE, East West University for their encouragement, valuable suggestions and providing me their helping hands whenever required .

The author likes to express his sincere thanks to his colleagues, staffs and friends specially Md Nayeem Arafat, Lecturer, AIUB and Abu Naser Mohammad Zainuddin, Ex-lecturer, Dept. of EEE, BUET, for valuable discussions.

The author likes to express his gratitude to his sister and parents for their selfless inspiration and encouragement throughout the progress of the work. Finally, the author reminds with gratitude the names of all those who were directly or indirectly involved with this work.

DEDICATION

To my Family

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ABBREVIATIONS

DT	Direct Tunneling
FN	Fowler-Nordheim
EOT	Effective oxide thickness
MOSFET	Metal Oxide Field Effect Transistor
QMTC	Quantum Mechanical Transmission Co-efficient
QMWI	Quantum Mechanical Wave Impedance
QPC	Quantum Point Contact
TAT	Trap Assisted Tunneling
TDDB	Time Dependent Dielectric Breakdown
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration
VRH	Variable Range Hopping
WKB	Wentzel-Kramer-Brillouin

ABSTRACT

Electrical instability is one of the major concerns regarding high-κ-based field-effect transistors (FETs); threshold-voltage (VT) shifts observed in pulsed measurements is considered to originate from the tunneling of channel electrons into traps in the gate dielectrics. Although some experimental models done by previous researcher are useful for providing qualitative explanations, a device-level numerical model is nonetheless necessary to quantitatively analyze the origin and impact of the electrical instability in such multistack systems. The charge trapping/detrapping model to analyze the gate threshold voltage instability reported so far have been using detrapping of the trapped charges back to the channel alone ignoring the detrapping to the gate. But a complete quantum mechanical is necessary to observe the behavior of charge trapping and threshold voltage instability. In this context, a quantum mechanical model (QM) is presented for analyzing the threshold voltage instability induced by charge trapping/detrapping for the inversion gate capacitance of MOS structures with high-k gate dielectrics. The threshold voltage shifts are modeled based on a modified rate equation and the properties of carriers in inversion layers are studied by solving coupled Schrödinger's and Poisson's equation self consistently. The model incorporates the effects due to detrapping of charges to the gate region which has been taken as negligible before. The accuracy of the model has been verified with some reported experimental results. It is evident from the results that, not only the further shrinking of Effective Oxide Thickness (EOT) but also increasing gate pulse width influence the detrapped charges that play a significant role in the threshold voltage instability. And these detrapped charges to the gate region also increase the gate current of the MOS devices, which is under estimated if calculated without considering these charges.

CHAPTER 1

INTRODUCTION

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1.1 GENERAL OVERVIEW

External electric fields can change the properties of semiconductor surfaces significantly, and the consequences of such changes have been systemically explored for many years. More recently there has been considerable work on the quantum effects that arise when band bending confines the carriers to a narrow surface channel. To model the effects of quantum confinement, quantum allows the self-consistent solution of the Schrödinger equation with Poisson's equation. Poisson's equation is solved in two dimensions over the entire device while Schrödinger's equation is solved in one dimensional slice across the device. These solutions provide calculations of the bound state energies (Eigen energies), the carrier wave functions (Eigen functions), and carrier concentrations in the presence of quantum mechanical confining potential variations. The calculation of eigen energies and wave functions in quantum wells is important in many applications. Several techniques have been proposed to perform these calculations.

Accurate determination of eigen energies in an arbitrary quantum well under an applied bias is not trivial. Moreover, the normalization of the wave function calculated by numerical integration of Schrödinger's equation can be computationally intensive. This is particularly true if a self-consistent solution including the space charge is desired. An accurate description of metal-oxide-semiconductor devices requires careful modeling of inversion and accumulation layers at the semiconductor-oxide interface. Importance of quantum effects in inversion and accumulation layers is well known. According to the International Technological Roadmap for Semiconductors (ITRS), the device requirements dictate that the gate oxide thickness be scaled down to below 2nm. Aggressive scaling in microelectronics to achieve higher performance and circuit density necessitates the thinning of the SiO_2 gate dielectric [1]. With the advent of ULSI (Ultra Large Scale Integrated) circuit technology, MOS transistors featuring gate oxide of sub-1.5 nm have already been fabricated [2],[3]. However, the electronic structure at the atomic scale seems to limit practical oxide thicknesses to 0.7–1.2 nm [4]. This is a fundamental limit which cannot be overcome by technological advancements. In this ultrathin (<3nm) gate oxide regime, the reliability has become one of the most important concerns.

1.2 LITERATURE REVIEW

Since its use as gate insulator in 1957 [5], the degradation of thin silicon dioxide films was observed over three decades ago [6]-[9]. The scaling of complementary metal oxide semiconductor (CMOS) transistors has led to the silicon dioxide layer used as a gate dielectric becoming so thin (1.4 nm) that its leakage current is too large.

It is necessary to replace the SiO_2 with a physically thicker layer of oxides of higher dielectric constant (κ) or 'high K' gate oxides such as hafnium oxide and hafnium silicate. Little was known about such oxides, and it was soon found that in many respects they have inferior electronic properties to SiO_2, such as a tendency to crystallize and a high concentration of electronic defects. Intensive research is underway to develop these oxides into new high quality electronic materials. This review covers the choice of oxides, their structural and metallurgical behaviors, atomic diffusion, their deposition, interface structure and reactions, their electronic structure, bonding, band offsets, mobility degradation, flat band voltage shifts and electronic defects. The use of high K oxides in capacitors of dynamic random access memories is also covered. Electrically active defects are defined as atomic configurations which give rise to electronic states in the band gap of the oxide. Typically these are sites of excess or deficit of oxygen or impurities. Defects are undesirable for four reasons. Firstly, charge trapped in defects causes a shift in the gate threshold voltage of the transistor, the voltage at which it turns on. Secondly, the trapped charge will change with time so the threshold voltage will shift with time, leading to instability of operating characteristics. Thirdly, trapped charge scatters carriers in the channel and lowers the carrier mobility. Fourthly, defects cause unreliability; they are the starting point for electrical failure and breakdown of the oxide.

So electrical instability is one of the major concerns regarding high-κ-based field-effect transistors (FETs); threshold-voltage (VT) shifts observed in pulse measurements is considered to originate from the tunneling of channel electrons into traps in the gate dielectrics [10]–[12]. Of particular interest is the experimentally observed dependence of VT shifts on the pulse-height and logarithmic stress time. The former effect has been suggested to be due to the relative shift of trap energy

level with respect to the channel quasi-Fermi level as gate bias varies [10], and the latter effect has been attributed to the distributed bulk electron traps [11] based on the tunneling front model [13]. A distributed charge trapping/de-trapping model based on tunneling has also been presented by Leroux et al. [14]. Some other possible explanations may involve variable range hopping [15] or a continuous time random walk [16]. Although these theoretical models are useful for providing qualitative explanations, a device-level numerical model is nonetheless necessary to quantitatively analyze the origin and impact of the electrical instability in such multi stack systems.

1.3 OBJECTIVE AND SCOPE OF THE WORK

Charge trapping /detrapping phenomena has become a decisive criterion as it makes the threshold voltage instable. However, before their final integration in industry, significant issues remain to be overcome as there are mobility degradation, metal gate incompatibility and threshold voltage instability. To address this last issue, hysteresis phenomena [10, 11, 12, and 14] are measured and it becomes important to know the trapping/detrapping mechanisms in pre-existing defects. Although these models are useful for providing qualitative explanations, a device-level numerical model is nonetheless necessary to quantitatively analyze the origin and impact of the electrical instability in such multi stack systems.

1.4 THESIS LAYOUT

This thesis consists of five chapters of which chapter one gives an introduction followed by literature review and objective of this study.

Chapter 2 deals with brief description of MOSFET fundamentals and charge trap behavior and gate current. It also contains a brief description of the origin of traps creation, oxide degradation and an overview of charge trapping phenomenon.

In Chapter 3, the quantum mechanical calculations and the trap assisted discharged current expression for MOS capacitors are discussed.

The simulation results are presented in Chapter 4 based on the expressions developed in Chapter 3. Conclusive remarks and discussions are given in chapter 5.

CHAPTER 2

CHARGE TRAPPING/DETRAPPING PROCESS

INTRODUCTION

Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), briefly termed as MOS, is the building block of the complex Integrated Circuits (IC), such as microprocessors, graphics, and Digital Signal Processing (DSP) chips. Each IC packs more than 100 million MOS transistors on a single chip. Integration of one billion transistors into a single chip will become a reality before 2010.

The basic operation of a MOS is analogous to that of a capacitor. Here, one plate acts as conducting channel between two ohmic contacts (termed as the Drain and the Source) and the other (called the Gate) controls the charge inducted in the channel. An ideal insulator is placed between the gate and the channel to prevent the flow of any current flow. This research is focused on the reliability of this gate insulator. If a conducting channel is induced by the gate then this type of structure is called enhancement type MOSFET. On the other hand, if the conducting channel is diffused during fabrication the device is called depletion type MOSFET. Enhancement type MOSFET is the most popular used MOSFET. Each MOSFET has an *n* and *p* sub-type depending on the type of carriers (electrons and holes) contributing the current. In this chapter, we focus on the MOSFET structure, operation, its history and the degradation of the Gate of MOSFET.

2.1 A BRIEF HISTORY OF MOSFET

The operating principle of the MOSFET transistor was first described in Lilienfield's historical patent issued in 1926. It took another 34 years before Dawon Kahng and Martin Atalla successfully built a working MOSFET in 1960.

For the past 40 years, the semiconductor industry and academia have relentlessly pushed transistor scaling. Along with scaling, the MOSFET transistor evolved from the p-MOSFET in the 1960's to the n-MOSFET in the 1970's. A good understanding of gate oxide quality, such as interface traps, fixed and mobile charges, and a good control of gate oxide quality in a manufacturing environment enabled industry to make the transition from PMOS technology to a higher-performing NMOS technology in 1970's.

2.3 THE MOSFET STRUCTURE AND OPERATION

The structure of an n-channel enhancement type MOSFET, shown in the figure consists of a moderately doped p-type silicon substrate into which two heavily doped n+ regions, the source and the drain are diffused. Between these two regions there is a narrow region called the channel. A layer of SiO_2 insulator is sandwiched between the channel and the gate made of poly crystalline silicon.

When a positive voltage is applied across the gate and substrate, positive charges are accumulated on the gate. Consequently electrons drift towards the insulator in the region between the drain and source. An increasing gate voltage changes the channel to a conductive path between the drain and source. When, a voltage is applied between drain and source, electrons move from the source to the drain creating an electric current.

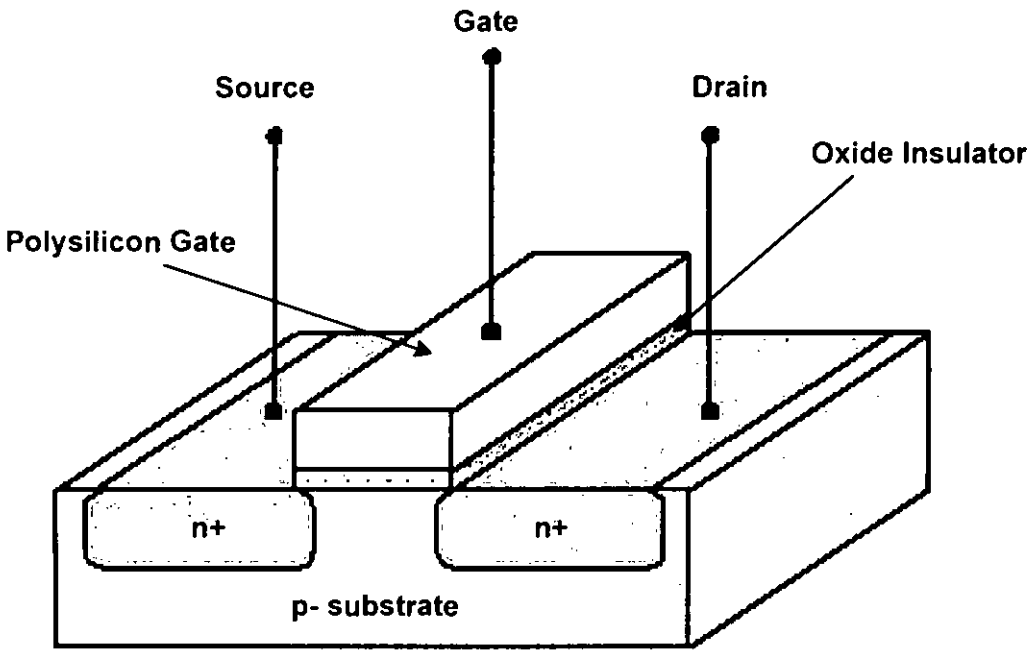

Fig. 2.1: A basic n-channel MOSFET structure.

2.4 MOSFET SCALING AND RECENT TRENDS

Over the past decades, the MOSFET has continually been scaled down in size to achieve lower switching time, reduced cost and lower power consumption. Typical MOSFET channel lengths were once several micrometres, but modern integrated circuits are incorporating MOSFETs with channel lengths of less than a tenth of a micrometre long. Indeed Intel will begin production of a process featuring a 65nm channel length in early 2006. Until the late 1990s, this size reduction resulted in great improvement to MOSFET operation with no deleterious consequences.

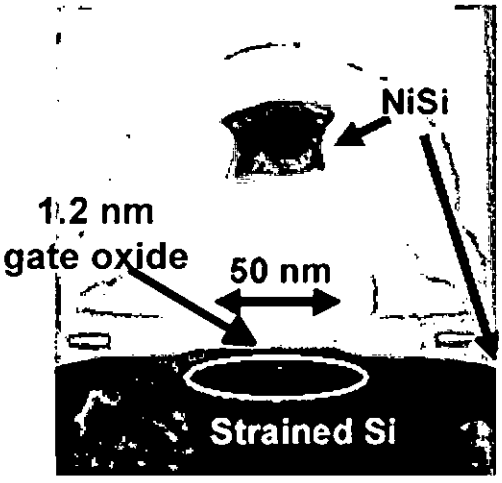

Fig. 2.2: 45-nm transistor presented in IEDM 2003 (Ref. [3]).

The most advanced MOS transistors used in volume production today are probably those of Intel's used in their 130nm logic technology with transistor gate length and gate oxide thickness are 60nm and 1.5nm, respectively. At IEDM 2003 [3], Intel presented a manufacturing-ready 90nm technology, with transistor gate length 50nm and gate oxide thickness 1.2nm. As of 2nd half of 2004, 90nm technology is at the beginning of manufacturing life cycle at a very limited number of top semiconductor manufacturers. For majority of IC manufacturers, 90nm technology is in the qualification stage or in the middle of development.

2.5 THE GATE AND GATE DIELECTRICS

Early MOSFET used metal (such as aluminum) as a gate electrode; hence the name MOSFET was came. However, in fabrication processes high temperature causes metal to melt. Moreover, MOSFETs with metal gates have higher threshold voltage. Thus poly-crystalline silicon was preferable to metal as gate material as it has higher melting point. However, polysilicon is highly resistive (approximately 1000 times more resistive than metal) which reduces the signal propagation speed through the material. To lower the resistivity, dopants are added to the polysilicon. Sometimes additionally, high temperature metal such as Nickel layered onto the top of the polysilicon which decreases the resistivity. Such a blended material is called silicide. The silicide-polysilicon combination has better electrical properties than polysilicon alone and still does not melt in subsequent processing. Also the threshold voltage is not significantly higher than polysilicon alone, because the silicide material is not near the channel.

In case of the Gate Oxide, the insulator should be of high insulating property to resist leakage current from gate to the channel. As the device is scaled down, the tunneling phenomena become prominent leading to increased power consumption. (The various degradation of oxide are discussed in the following sections). Insulators that have a larger dielectric constant than SiO_2, such as group IV(B) metal silicates e.g. Hafnium and Zirconium Silicates and Oxides, are now being researched to reduce the gate leakage. Increasing the dielectric constant of the gate oxide material allows a thicker layer while maintaining a high capacitance. The higher thickness reduces the tunneling current between the gate and the channel. An important consideration is the barrier height of the new gate oxide; the difference in conduction band energy between the semiconductor and the oxide will also affect the leakage current level. For the traditional gate oxide, silicon dioxide, the former barrier is approximately 3 eV. For many alternative dielectrics the value is significantly lower, somewhat negating the advantage of higher dielectric constant.

2.6 QUANTUN CONFINEMENT IN MOS STRUCTURE

It has been well known since the late sixties, that for a better description of the MOS structure, the conventional semi-classical approach is not very adequate. In the semi-classical approach, the density of states above the conduction band is assumed to be continuous, and using this continuous density of states model and the Fermi function, the classical description of the electron concentration can be obtained. This approach works well if the bands are slowly varying compared to the electron's deBroglie wavelength. However, in case of an MOS Capacitor, Fig. 2.3 shows that the band bending near the surface can form a quantum well, which introduces energy quantization. So the semi-classical approach does not work well for these problems, and for a precise description a quantum mechanical approach has to be used.

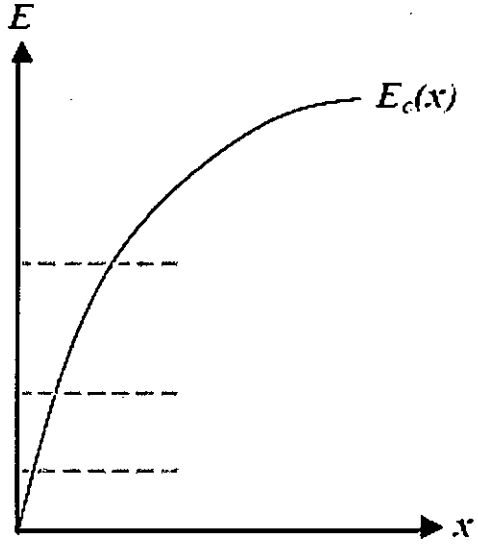

Fig. 2.3: Potential well formed at oxide semiconductor interface. (Ref: Schred 2.1 Tutorial, Purdue University, April 28, 2003)

2.7 SILICON BAND STRUCTURE AND SUBBANDS

There is a little modification of the above procedure when applied to the silicon MOS Capacitor. That is due to the band structure of silicon (Fig. 2.4). As is well known, the effective mass is inversely proportional to the curvature of the constant energy ellipsoids. The two ellipsoids along the x direction have their longitudinal effective mass perpendicular to the surface. So they respond to the external field

with their longitudinal effective mass, which is $0.916m_0$ (where m_0 is the mass of free electron). The other four respond with the transverse effective mass $0.19m_0$ because their transverse effective mass is perpendicular to the surface.

Thus the Schrödinger equation has to be solved twice, once for the longitudinal effective mass and again for the transverse effective mass. Thus for each effective mass a set of subbands will be obtained. Each set of subbands can be visualized as a ladder. Thus two different ladders will be obtained for each effective mass, as shown in Fig. 2.5. Subbands from ladder corresponding to the longitudinal effective mass, are called unprimed subbands, and subbands from the other ladder are called primed subbands. It should be noted that, subbands of unprimed ladder have a degeneracy of 2 as there are two ellipsoids in this group, and subbands of primed ladder have a degeneracy of 4. The unprimed ladder has a larger effective mass, so their energies are relatively smaller than the primed ladder. Normally, the lowest 3 or 4 unprimed subbands and lowest 2-3 primed subbands are occupied at room temperature; other subbands can be safely ignored as they have negligible population.

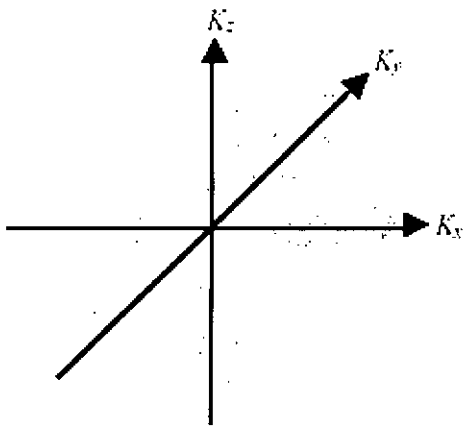

Fig. 2.4: Constant energy ellipsoids for silicon along (100) surface. (Ref: Schred 2.1 Tutorial, Purdue University, April 28, 2003)

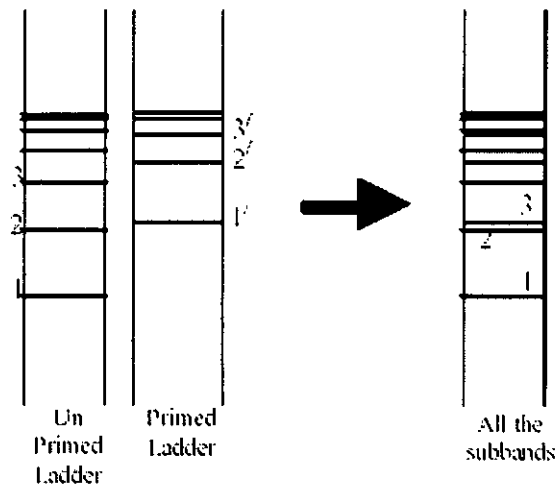

Fig. 2.5: Primed and unprimed ladders are shown schematically. At left, the two ladders are shown separately, while at right, the combined subband structure is shown. (Ref: Schred 2.1 Tutorial, Purdue University, April 28, 2003)

2.8 QUANTUM EFFECTS IN MOS STRUCTURES

So far we have outlined the mechanics of the quantum mechanical calculation for MOS structures. What we understood is: why we need quantum approach and how we solve the problem quantum mechanically. But, we may want to know how these quantum results differ from the semi-classical result. There are actually two key effects. To see this let us consider Fig. 2.6 and 2.7. Figure 2.6, shows one of the effects, that is the quantization of the energies above conduction band, which is assumed to be continuous in classical model. The direct effect of these on MOS capacitors or on MOSFETs is an increase of threshold voltage, because the threshold voltage is approximately the gate voltage for which, the conduction band goes below the Fermi level. However, due to the energy quantization, the lowest level that electrons occupy is not the bottom of conduction band, rather it is the first energy level, which is little higher than the conduction band edge. So to bend this band below the Fermi level, a little more gate voltage is needed. This gives rise to a threshold voltage rise in MOSFETs.

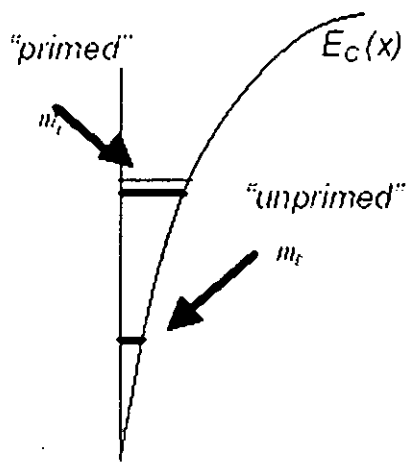

Fig. 2.6: Potential well formed at the oxide semiconductor interface. Horizontal lines represent the subbands. (Ref: Schred 2.1 Tutorial, Purdue University, April 28, 2003)

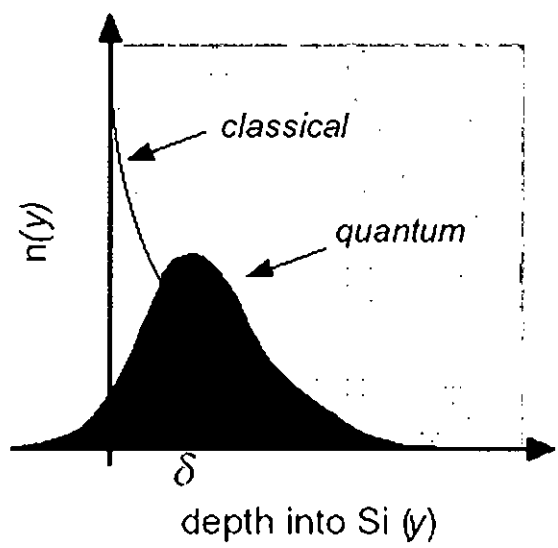

Fig. 2.7: Classical and quantum mechanical charge distribution inside semiconductor. (Ref: Schred 2.1 Tutorial, Purdue University, April 28, 2003)

Another effect comes from the spatial distribution of inversion charge. Both the classical and the quantum distribution of inversion charge along the depth of the device (x direction) are shown in Fig. 2.7. The classical distribution shows a peak at the oxide semiconductor interface while the quantum mechanical distribution is totally different from that and shows a peak inside. The net effect is that the actual profile (quantum mechanical) has an average distance from the surface that is larger than that predicted by the classical calculations. As we know, the average carrier distance has the effect of increasing the effective oxide thickness. Thus the quantum mechanical calculation predicts a larger effective oxide thickness, which means a lower gate capacitance. Thus for a certain gate voltage, the amount of inversion charge will be somewhat smaller than that, predicted by the classical analysis. This is more important as the oxide thickness becomes smaller with each technology generation.

2.9 GATE OXIDE TUNNELING

According to quantum physics electrons behave both like particles and like waves and are described by the solutions of Schrödinger equation. These waves can penetrate a potential barrier that would be a forbidden area if the particle was considered in the classical way. The term tunneling phenomenon refers to this property-the particle "tunnels" through the forbidden area.

2.9.1 Interband Tunneling

The interband tunneling occurs because of the finiteness of the height and width of the oxide barrier. It can be either direct (DT) or Fowler-Nordheim (FN) tunneling depending upon the magnitude and polarity of the applied gate voltage. The mechanisms are governed by the shape of the tunneling barrier. If the oxide barrier is trapezoidal and the electrons do not transit through the conduction band states of the barrier, then that is called Direct Tunneling (Fig. 2.8 (a)[i]). If the tunneling barrier is triangular and the transported electrons partly transit through the conduction band states of the barrier, then FN tunneling (Fig. 2.8 (a)[ii]) occurs [17],[18].

2.9.2 *Trap-Assisted Tunneling*

With advent of modern ULSI (Ultra Large Scale Integrated) technology, the grown SiO_2 has reached a satisfactory purity level. However, still the SiO_2 is not devoid of impurities. Such impurities and oxide defects are modeled as oxide traps which in turns lead to additional leakage current. Detailed description is presented in the subsequent sections.

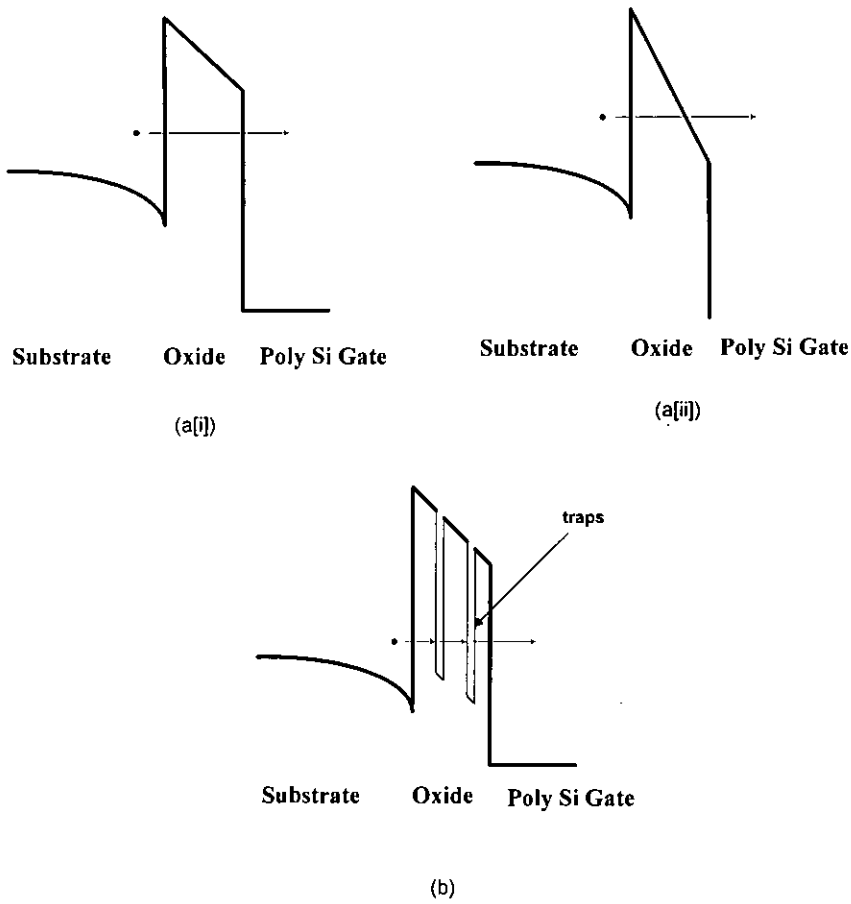

Fig. 2.8: (a) Energy band diagram of two types of Interband tunneling- [i] Direct Tunneling (DT), [ii] Fowler-Nordheim (FN) Tunneling, (b) Trap Assisted Tunneling (TAT).

2.10 DEFECT STATES

The electron traps can be of two types depending upon their origin- i) traps during formation or the 'as grown' traps and ii) traps due to the applied electrical stress. Traps formed during the fabrication steps are intrinsic oxide traps, intrinsic interface

traps and impurities. To take into account this polarity and time dependence, a team [10] has initially proposed a simple model with a defect band in HfO_2 layer located in energy between the silicon and Hafnium conduction band [Fig. 2.9(a)]. This model has some attractive features, since it explains qualitatively, for negative and positive gate bias, the charging and discharging of defects by tunneling through the interfacial SiO_2 layer. At the same time, studying the mobility degradation in high-k MOS devices, Morioka et al. [19] proposed to locate hysteresis traps at the $HfSiO_2/SiO_2$ interface as shown in Fig. 2.9(b). Thus, two types of models are encountered in the literature. To address the critical issue of the location of the trapped charge (bulk of the high- film or the interface high- /interface layer), Young et al. [36] have characterized the hysteresis phenomena on samples with different HfO2 thicknesses. Their results suggest the trapping occurs mostly in the bulk of high- material rather than only at the interface.

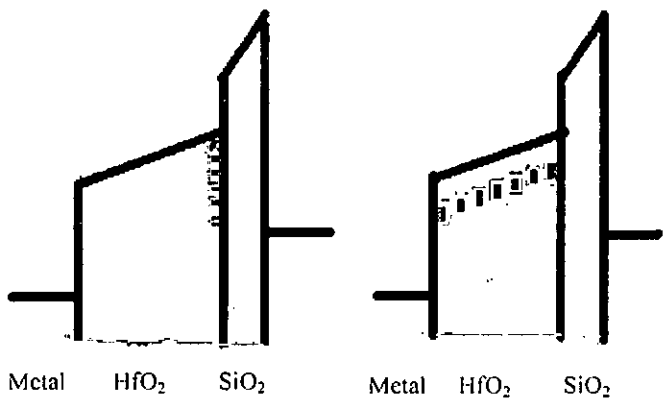

Fig 2.9 Two types of model: defects are located (a) at the SiO_2 /HfO_2 interface or (b) in the bulk of high-k film.

In the work of Torii et al. [20], the empty oxygen vacancies (VO_2+) in HfO_2 were suggested to be responsible for the electron trapping; the polaron-induced defect level shift for VO+ and VO were calculated by first principle method. A review on ab initio calculations of high-κ trap energy levels has been given in [35].

2.11 CHOICE OF HfO_2 AS GATE DIELECTRIC

Silicon dioxide is the key reason that microelectronics technology uses Si and not some other semiconductor. Si is an average semiconductor in performance, but in all other aspects SiO_2 is an excellent insulator. SiO_2 has the key advantage that it can be made from Si by thermal oxidation, whereas every other semiconductor (Ge, GaAs, GaN, SiC...) has a poor native oxide. SiO_2 is amorphous, has very few electronic defects and forms an excellent interface with Si. It can be etched and patterned to a nanometer scale. Its only problem is that when very thin it is possible to tunnel across it. Hence, we must loose these advantages of SiO_2 and start to use a new high K oxide. We can in principle choose from a large part of the Periodic table. The requirements of a new oxide are six-fold:

i. It must have a high enough K that it will be used for a reasonable number of years of scaling.
ii. The oxide is in direct contact with the Si channel, so it must be thermodynamically stable with it.
iii. It must be kinetically stable, and be compatible with processing to 1000° C for 5 seconds.
iv. It must act as an insulator, by having band offsets with Si of over 1 eV to minimize carrier injection into its bands.
v. It must form a good electrical interface with Si.
vi. It must have few bulk electrically active defects.

Among the high-k dielectrics being studied, HfO_2 appears promising due to its relatively high dielectric constant (25) as compared to Si_3N_4 and Al_2O_3 [21], its relatively high free energy of reaction with Si (47.6 Kcal/mole at 727 C) as compared to TiO_2 and Ta_2O_5 [22], and its relatively large bandgap (5.8 eV) [23]. Although there has been some recent work done on HfO_2 and its MOS capacitors [24], [25], the charge-trapping properties of this material are still unclear. In this thesis, the effects of stress voltage, trapping time, backward detrapping, and gate electrode on charge trapping in HfO_2 are reported.

2.12 CHARE TRAPPING/DETRAPPING PHENOMENA IN GATE DIELECTRICS

We have already noted that high-K oxides possess a larger bulk density of defects and trapped charge than SiO_2 [26]. It is now well known that the channel mobility in a high-k gated MOSFET is typically much lower than its SiO_2-gated counterpart. Since it is also well known that high-k gated MOSFET tends to have more oxide charge and interface traps than its SiO_2-gated counterpart. It should be noted that trapping/detrapping time constants for some of the high-k gate dielectrics, including HfO_2 and Al_2O_3, are much shorter than those for SiO_2 [27], and therefore the DC measurement methodology commonly used for MOS devices with SiO_2 gate dielectric will likely to miss these traps. A transient (pulsed) measurement methodology has been introduced to reveal more fully the traps in high-k gate dielectrics [27]. Charge trapping leads to instability in the flat band voltage and gate threshold voltage. It is seen as hysteresis on a drive current vs. gate voltage plot. The effect can be demonstrated by charge pumping experiments. It is notable that HfSiOx gate oxides have less hysteresis than HfO_2 and also that nitrogen addition reduces it below 70 meV. The amount of trapped charge can be reduced by various annealing cycles and by design of the oxide. It would also be helped by a clearer understanding of its origin. The origin of this trapped charge is becoming clearer. The first source is intrinsic defects in the oxide and interface traps. Zafar et al. [12] showed that trapping in HfO_2 and Al_2O_3 occurs by the filling of existing defect levels rather than the creation of new defects. This indicates that bulk defects in high K oxides are a serious problem. Kumar [28] showed that hot carriers can create additional defects, but this is an additional effect. The trapped charge can be reduced by annealing. This can be carried out in forming gas (N_2/H_2 mixture), or other nitrogen containing gases such as ammonia.

The detrapping process can originate from three possible mechanisms. The first may be due to a back tunnelling of electron from traps to substrate and the second, resulting from a Poole–Frenkel-like electrons conduction from traps to traps toward the gate electrode, which we have neglected (Fig. 2.10). And the third mechanism is tunneling of electrons from channel to poly-silicon gate. Our treatment of the nonlocal tunneling process derives from a general approach originally proposed for Schottky barrier tunneling [38]

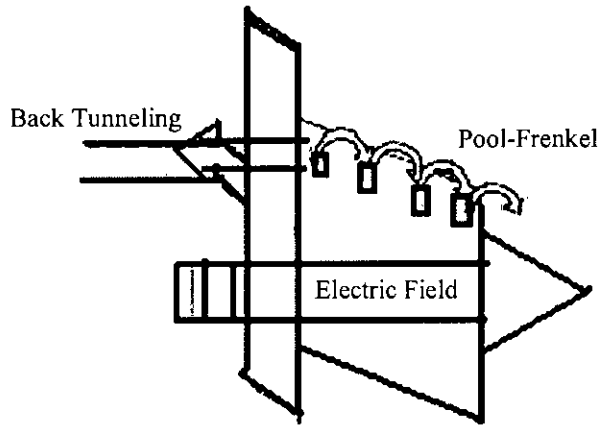

Fig 2.10 Two mechanisms which may take part in the detrapping at positive bias: back tunnelling and Poole–Frenkel.

2.13 CONCLUSION

Here in this chapter the choice of high-k dielectrics as a replacement of conventional SiO_2 is described. But due to higher bulk trap in HfO_2 another problem arises which is threshold voltage instability. Recently different processes have been adopted to reduce charge trapping such as post deposition annealing, deuterium (D_2O) annealing during the ALD process. In this dissertation effect of post deposition annealing on charge trapping is presented in chapter 4. Another noticeable phenomena is with the further shrinking (EOT<2nm) of oxide thickness charges get detrapped through the gate oxide interfaces which will also increase the gate current which has been considering as a major advantages to take high-k dielectric instead of conventional SiO_2

CHAPTER 3

TRAPPED CHARGE DENSITY AND GATE CURRENT

3.1 INTRODUCTION

Over the past decades, the MOSFET has continually been scaled down in size to achieve lower switching time, reduces cost and lower power consumption The scaling trend for gate dielectric is such that for sub-100 nm generation devices an equivalent gate oxide thickness of less than 2 nm will be required. In order to meet the requirement, the conventional gate oxide dielectric will need to be replaced by higher dielectric constant materials. Hafnium based dielectrics are being widely investigated as a potential replacement for the silicon oxi-nitride. However, before the final integration in to the industry, several important issues, such as mobility degradation, metal gate incompatibility and threshold voltage instability is needed to be considered. As high k oxides posses a large bulk density of defects, charge trapping leads to instability in the gate threshold voltage. Although there is some recent work done on HfO_2 and its MOS capacitor, the effect of charge trapping needs further investigation to ascertain the quality of performance. A distributed charge trapping/detrapping model based on tunneling has been presented by Leroux et al. [14]. Charge trapping in the HfSiON and HfO_2 gate dielectric has also been studied by Shanware et al. [11]. Liu et al. [29] simulated the charge trapping effects to obtain a reasonable match with the experimental results of [11]. However, the simulation assumed that both charge trapping and detrapping take place from and to the channel. The authors ignored the possibility that charges may detrap by tunneling to the gate layer.

In this thesis, simulation results are presented to show that the effect of charge detrapping to the gate region can have considerable effect on the instability of the gate threshold voltage and also on the gate leakage current, particularly with decreasing EOT and increasing pulse width. Ignoring the detrapping of the charges from the oxide layer to the gate ultimately ignores the component of gate leakage current altogether

3.2 SELF-CONSISTENT MODEL

Properties of carriers in MOS inversion layers are studied by solving coupled Schrödinger's and Poisson's equations self-consistently within the effective-mass approximation.

The 1D Schrödinger Equation is given by

$$\left[-\frac{\eta^2}{2m_{Zi}} \frac{d^2}{dz^2} + eV(z) \right] \psi_{ij}(z) = E_{ij} \psi_{ij}(z) \tag{3.1}$$

Here m_{Zi} is the effective-mass perpendicular to the interface in the ith valley, V (z) is the electrostatic potential and E_{ij} and Ψ_{ij} are the eigenenergy and the wave function corresponding to the jth subband in the ith valley.

The potential is calculated from Poisson's equation which is as follows

$$\in_0 \in_r \frac{d^2 V(z)}{dz^2} = -[\rho_{dep}(z) - en(z)] \tag{3.2}$$

Where n(z) represents the total inversion electron density. The inversion layer electron can exist only at eigen energies and their spatial distribution in described by the respective wave function. Under such conditions, n(Z) is calculated from

$$n(z) = \sum_{ij} (n_{vi} m_{di} k_B T / \Pi\eta^2) \ln\left(1 + \exp\left(\frac{E_F - E_{ij}}{k_B T}\right)\right) \left|\psi_{ij}\right|^2 \tag{3.3}$$

Where n_{vi} and m_{di} are the velley degeneracy and the density of states effective mass for the ith valley, respectively.

The boundary conditions commonly used to solve Schrödinger's equation are that the wave function goes to zero at z = 0 and at z = 1 where z = 0 is at the silicon-oxide interface and z = 1 is deep inside silicon [30].

In this paper, we use a technique, based on Green's function formalism, to solve Schrödinger's equation with wave function penetration. This technique is described in detail in [31], [32]. Open boundary conditions are used, which are based on the assumption that the potential profile is flat at deep inside the gate metal as well as at

deep inside the bulk semiconductor. Our assumption implies that the wave function deep inside the semiconductor is exponentially decaying and deep inside the gate metal, the wave function is a plane wave.

The eigenenergies of the quasi-bound states are calculated by locating the peaks of the one-dimensional (1-D) density-of-states [33]. The corresponding wave functions including penetration can easily be obtained using the relationships described in [34]. Once the eigen-energies and the wave functions are calculated, the self-consistent formulation is applied with appropriate modifications to include penetration effects also in the solution of Poisson's equation. Since a fraction of inversion charge resides within the gate-oxide due to wave function penetration, Poisson's equation is solved for the combined oxide and semiconductor regions with the boundary conditions applied at the gate metal-oxide interface

3.3 CHARGE TRAP MODEL

The self consistent model, capable of simulating pulsed operations of Hafnium based n-FET, presented by Liu et al. [29] uses the following rate equation for distributed trapped electrons

$$\frac{dn_t}{dt} = \frac{n}{N_O} \cdot \frac{N_t - n_t}{\tau^*} \cdot \frac{1}{1+\exp((E_t^* - E_f)/kT)} - \frac{n}{N_O} \cdot \frac{n_t}{\tau_1} \cdot \left[1 - \frac{1}{1+\exp((E_t - E_f)/kT)}\right] \quad (3.4)$$

where n_t is the trapped electron density, N_t the density of the uniform bulk traps in HfO_2, n the electron concentration in the channel, N_0 a unit normalization factor, E^*_t the empty defect level, E_t the occupied defect level, E_f the channel electron quasi-Fermi level. In this model, the tunneling of trapped electrons to the gate has been neglected, due to lowering of charged trap levels. The equation basically consists of two terms, the first term represents the charge trapping rate from the channel and the second term accounts for the detrapping of the trapped charges back to the channel. Hence, the very mechanism assumed in this model leaves no room for leakage current flow from the channel to the gate irrespective of the parameters like EOT and time constants. On the other hand, neglecting the detrapping of charge to the

gate over-estimates the trapped charge in the oxide layer showing greater instability of threshold voltage.

We have modified the rate equation [3.4] for the distributed trapped electrons incorporating detrapping of electrons to the gate given by

$$\frac{dn_t}{dt} = \frac{n}{N_o}\cdot\frac{N_t - n_t}{\tau^*}\cdot\left[\frac{1}{1+\exp((E_t^* - E_f)/kT)}\right] - \frac{n}{N_o}\cdot\frac{n_t}{\tau_1}\cdot\left[1 - \frac{1}{1+\exp((E_t - E_f)/kT)}\right]$$
$$- \frac{n}{N_o}\cdot\frac{n_t}{\tau_2}\cdot\left[1 - \frac{1}{1+\exp((E_t - E_{fm})/kT)}\right] \qquad (3.5)$$

Here the third term of the modified Eqn.3.4 incorporates the detrapping of electrons to the poly-silicon gate, where E_{fm} is the poly-silicon gate Fermi level, τ^* is the tunneling time constant for the forward trapping process from channels to trap, τ_1 is the tunneling time constant for the detrapping process from occupied defect state to the channel and τ_2 is the tunneling time constant for the detrapping process from occupied defect states to the gate. All these time constants are obtained using WKB approximation [13]. For the forward tunneling process from channel to traps, it is given by

$$\tau = \tau_O \exp\left[\frac{4\sqrt{2m^* m_O}}{3\eta qE} \times \left(\left(E_c^{ox} - E_t^* - qEx\right)^{\frac{3}{2}} - \left(E_c^{ox} - E_t^*\right)^{\frac{3}{2}}\right)\right] \qquad (3.6)$$

Considering the fact that, trap level in the oxide layer is at a high energy level from the Fermi level of the gate, trapping from the gate side is neglected.

The electron-trap centers are distributed in the HfO_2 bulk region as well as in the HfO_2/SiO_2 interface [35]. Liu et al. [29] have characterized the hysteresis phenomena on samples with different HfO_2 thickness. Their results suggest that trapping occurs mostly in the bulk on high-k materials rather than only at the interface. We also make the following assumptions:

1) The electrons tunnel from the channel to the empty defect states. While detrapping, trapped charges tunnel both to the channel and gate electrode.
2) Here we neglect the detrapping resulting from a Pool-Frenkel-like electrons [37] conduction from traps to traps. So we have adopted a general approach originally proposed for Schottky barrier tunneling [38] to model trapping/detrapping process.

3.4 QUANTUM MECHANICAL CALCULATIONS FOR POTENTIAL BARRIERS

The calculation of Quantum Mechanical Transmission Co-efficient (QMTC) is necessary for analyzing the current–voltage (I-V) characteristics of resonant tunneling and quantum size devices [39]. In this work the QMTC is calculated by Quantum Mechanical Wave Impedance (QMWI) method formulated by Khondker *et al.* [32].

Using the effective mass approximation the one dimensional Schrödinger Equation is written as

$$-\frac{\eta^2}{2}\frac{d}{dx}\left(\frac{1}{m^*(x)}\frac{d\psi}{dx}\right)+\left[V(x)-E\right]\psi(x)=0 \tag{3.7}$$

where, $\psi(x)$ is the envelope wave function, E is the energy of incident electron and V(x) is the potential energy. Here, $m^*(x)$ is the effective mass and $\hbar$ is the reduced Planck's constant. If we consider constant effective mass and potential constant then the Schrödinger equation reduces to,

$$\frac{d^2\psi}{dx^2}+\frac{2m^*}{\eta^2}\left[E-V(x)\right]\psi(x)=0 \tag{3.8}$$

and the solution of the Eqn. (3.2) is,

$$\psi(x)=A^+\left(e^{\gamma x}-\rho e^{-\gamma x}\right) \tag{3.9}$$

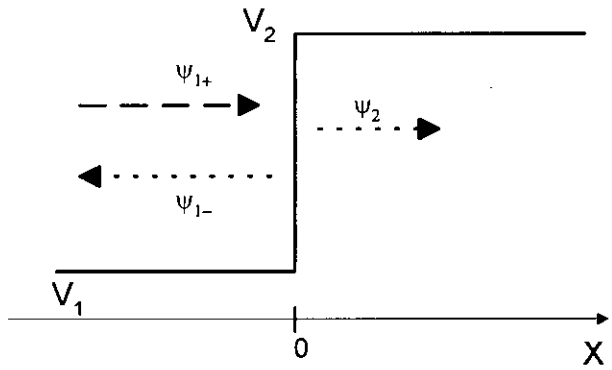

Fig. 3.1: A step potential barrier with potential height of (V_2-V_1). Where, the propagation constant, γ is given by

$$\gamma = \alpha + j\beta = j\sqrt{\frac{2m^*[E - V(x)]}{\eta}} \tag{3.10}$$

In Fig. 3.1, the wave function $\psi(x)$ in the region where x<0, can be defined as the superposition of two waves – one the incident wave ψ_+ and another is the reflected wave ψ_- that is reflected from the potential discontinuity at x=0.

Calculation of QMTC

Now, differentiating Eqn. (3.3) w.r.t. *x* and multiplying on both sides by factor ($\hbar/jm^*$) we get,

$$\phi(x) = A^+ Z_0 \left(e^{\gamma x} + \rho e^{-\gamma x}\right) \tag{3.11}$$

Where,

$$Z_0 = \eta / jm^* \tag{3.12}$$

According to Khondker *et al.* [32] the terms $\psi(x)$ and $\phi(x)$ are analogous to the distributed parameters I(x) and V(x) of transmission lines respectively. The term Z_0 is regarded as characteristic impedance of the region with potential V(x) that is analogous to the characteristic impedance of transmission line. The new parameter introduced by Khondker *et al.* [32] is Quantum Mechanical Wave Impedance, which is defined as [32],

$$Z(x)=\frac{\phi(x)}{\psi(x)}=R(x)+jX(x) \tag{3.13}$$

Where, R(x) and X(x) are the real and imaginary parts of the QMWI at any point.

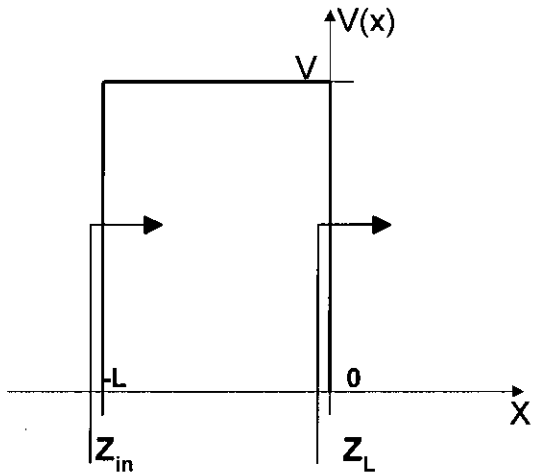

Fig. 3.2: Calculation of QMWI for a potential barrier of length L.

Fig. 3.2 illustrates the calculation of Z(x) using simple formula. If the load impedance at point x=0 is Z_L, then the input impedance at point x=-L will be Z(x) $=Z_{in}$ (Fig. 3.2).

Here,

$$Z_{in}=Z_0\frac{Z_L\cosh\gamma L-Z_0\sinh\gamma L}{Z_0\cosh\gamma L-Z_L\sinh\gamma L} \tag{3.14}$$

In similar way, the QMWI can be determined at the potential boundaries. Such method can also be applied for potential profiles that vary continuously with x. In such case, the potential profile is approximated as multi step functions with a sequence of N segments each having a length of L.

Here, the QMWI of the segment 1 at the boundary is considered Z_L (or Z_1) looking to the right. By using Eqn. (3.8) we determine the input QMWI of segment 1 (or Z_2). This input impedance serves as the load QMWI for segment 2. In this way, the input QMWI of N-th segment can be determined, which is the input QMWI of the whole potential profile.

Now, after determining the QMWI of the whole potential structure, the amplitude reflection co-efficient is calculated by,

$$\rho(E)=\frac{Z_L - Z_0}{Z_L + Z_0} \tag{3.15}$$

The Quantum Mechanical Transmission Co-efficient (QMTC) will be determined by,

$$T(E)=1-|\rho(E)|^2 \tag{3.16}$$

The next section will be dedicated to a detailed numeric example for calculating QMWI and QMTC.

3.5 CURRENT DENSITY FORMULA

The gate current has two components-the direct tunneling current and the trap assisted discharged current. Here we mainly concentrate on the determination of discharging current. The gate current is calculated using Tsu-Esaki equation which consists both the direct tunneling current and Fowler-Nordheim tunneling current.

3.5.1 Discharged Current due to trap:

To calculate discharging current from the gate electrode, we have used the following equation

$$J_d = q \times \sum \frac{n}{N_O} \cdot \frac{n_t}{\tau_2} \left[1 - \frac{1}{1+\exp((E_t - E_{fm})/kT)} \right] \tag{3.17}$$

Here in Eqn. 3.17 we simply sum up the detrapped charges through the gate/oxide interface and calculate the current contributed by each charge.

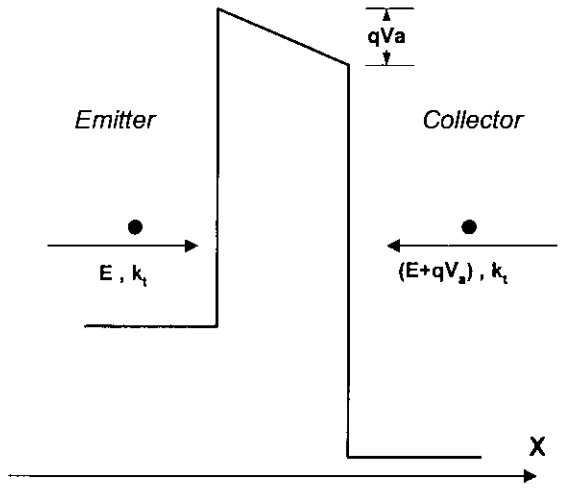

Fig. 3.3: A schematic representation of a potential energy profile employed in the derivation of the current density expression.

3.5.2 Gate current

The nonzero probability for tunneling of electrons through potential barrier offers the possibility of measurable currents. A typical situation is shown in Fig. 3.3 where an electron plane wave is specified by a total energy E and a transverse wave vector k_t. For arbitrary potential barrier, electrons incident upon the potential from both the electrodes will contribute to the total current. First, let us consider the contribution from electrons incident from the emitter. Since electrons are fermions, these electrons will contribute to the total current only if there are corresponding empty states on the side to which the electrons can tunnel. Assuming conservation of total energy and transverse momentum [40], the tunneling current density J_{E-C} from a unit volume of k-space is [41].

$$J_{E-C} = \frac{q}{\eta}\left(\frac{\partial E}{\partial k_x}\right)_E g(k) f_E(E)\left[1 - f_C(E + qV_a)\right] T(E, k_t) \tag{3.18}$$

where, f_E (E) and f_C (E) are the Fermi-Dirac electron distribution function at the emitter and collector electrode respectively. g(k) is the density of states per unit volume of k-space.

A similar analysis can be used to obtain the contribution from electrons of energy ($E+qV_a$) incident from the collector. Since the tunneling probability is equal for both directions, the tunneling current density $J_{C\text{-}E}$ from the collector to the empty states of the emitter is given by,

$$j_{C\text{-}E} = \frac{q}{\eta}\left(\frac{\partial E}{\partial k_x}\right)_{(E+qV_a)} g(k) f_C(E+qV_a)[1-f_E(E)]T(E,k_t) \tag{3.19}$$

The net tunneling current density per unit volume of k-space is,

$$J_t = J_{E\text{-}C} - J_{C\text{-}E} \tag{3.20}$$

The density of states per unit volume of k-space is evaluated to be [64]

$$g(k) = \frac{2}{(2\pi)^3} \tag{3.21}$$

The Fermi-Dirac electron distribution function is given by,

$$f(E) = \frac{1}{1+\exp\left(\frac{E-E_F}{k_B T}\right)} \tag{3.22}$$

where, E_F is the Fermi energy, k_B Boltzman's constant and T is the absolute temperature.

To simplify the analysis, we neglect the velocity difference between the electrons of emitter and collector and evaluate the derivative in Eqn. (3.13) at E instead of at ($E+qV_a$). The assumption of parabolic energy momentum relationship for states describing the contacts reduces Eqn. (3.14) to,

$$J_t = \frac{2}{(2\pi)^3}\frac{q\eta k_x}{m^*}[f_E(E) - f_C(E+qV_a)]T(E,k_t) \tag{3.23}$$

The electron effective masses for the two electrodes are assumed to be equal. Integrating J_t over the entire k-space the total current density can be obtained

$$J = \frac{2}{(2\pi)^3}\frac{q\eta}{m^*}\int_0^\infty\int_0^\infty k_x T(E,k_t)[f_E(E) - f_C(E+qV_a)]2\pi k_t\, dk_t dk_x \tag{3.24}$$

$$\therefore J = \frac{2qm^*}{(2\pi)^2\eta^3}\int_0^\infty\int_0^\infty T(E,k_t)[f_E(E) - f_C(E+qV_a)]dE_t dE_x$$

(3.25)

Where,

$$E = \frac{\eta^2 k_t^2}{2m^*} + E_x \tag{3.26}$$

The effect of mass variation on the transverse motion can be neglected, as done by several authors [40], [41], [39]. This makes the transmission coefficient dependent only on the longitudinal energy E_x=E-E_t. The E_t integral can now be performed giving the usual Tsu-Esaki expression [40]:

$$\therefore\ J = \frac{qm^* k_B T}{2\pi^2 \eta^3} \int_0^\infty T(E_x) \ln\left[\frac{1+\exp\left\{\frac{(E_{F_E} - E_x)}{k_B T}\right\}}{1+\exp\left\{\frac{(E_{F_C} - E_x - qV_a)}{k_B T}\right\}}\right] dE_x \tag{3.27}$$

The spatial dependence of effective mass is however taken into account to calculate $T(E_x)$ in Eqn. (3.27).

In the derivation of tunnel current expression the velocity of an electron of energy ($E+qV_a$) incident from the collector is assumed to be equal to that of an electron of energy E incident from the emitter. Collins *et al.* [41] found the contribution to J due to the velocity difference to be less than 10% for physically relevant tunneling systems. This is conceivable, since at low voltages the velocity difference is small, while at higher voltages the contribution from the collector is insignificant.

3.6 CONCLUSION

A quantum mechanical charge trapping model is developed by modifying the rate equation proposed by [29]. Here the modified equation incorporates the detrapping of charges to the poly-silicon gate. And the current contributed by these charges has been calculated using Eqn. [3.17] shown as "discharged current" in chapter 4.

By solving this self-consistent model we get the properties of carriers in inversion layer such as band bending, Eigen states, wave function distribution, carrier concentration, position of Fermi-level etc. Then the trapped electron density, nt is calculated using the Eqn. 3.5 at a fixed inversion charge. Change in electric field due to trap charge is calculated using Poisson's equation. Then again we recalculate inversion charge and repeat the process self consistently until the result converges. Following Khondker et al. [32] we get Transmission Co-efficient, T (E) and then gate current is calculated using Eqn. 3.27.

CHAPTER 4

RESULTS

4.1 INTRODUCTION

In this chapter, the simulated results using the expressions summarized in the previous chapter are presented in details. The aim of this work is to find out the charge trapping behavior of gate dielectric stacks. The focus of this work is two-fold; (i) to investigate the role of detrapped charges to the gate, which has been neglected so far and (ii) to calculate the current contribution by the detrapped charges. A predominant role of that effect has been observed with decreasing effective oxide thickness and increasing pulse width.

4.2 PARAMETER

The implemented model is then used for two-dimensional simulations of nFETs with SiO_2/HfO_2/poly-Si gate stacks.

Default values for some simulation parameters are:

Relative dielectric constant of HfO_2	=25
Tunneling effective mass, m^*_t	$=0.2Xm_0$
A characteristic tunneling time, τ_0	=10 ps
Unit normalization factor N_0	$= 10^{19}/cm^3$
HfO_2/Si conduction band offset.	=1.4 eV
A fixed interface charge density	$=3X10^{12}/cm^2$
total surface density of bulk traps is	$=1.2\ X10^{13}/cm^2$
Empty defect level, E^*_t	= 0.4 and
Occupied defect level E_t	=1.4 eV below the HfO_2

Conduction band minimum (CBM), respectively.

4.3 POTENTIAL PROFILE OF NMOS STRUCTURE:

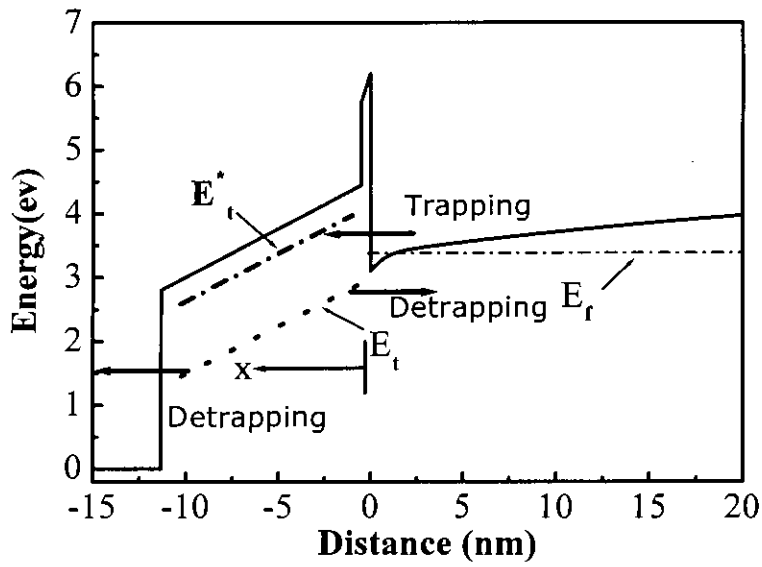

Fig. 4.1 Potential profile of a multi-stack (Si/SiO_2 /HfO_2/poly-Si) containing empty defect level and occupied defect level in the HfO_2 layer at positive gate bias using an EOT of 2.1 nm consisting of 0.5 nm SiO_2 and 1.6 nm EOT of HfO_2. Here substrate doping density, $Na=5\times10^{17}$ cm^{-3}

An EOT of 1.6 nm is used according to the experiments [11] and the SiO2 interfacial layer thickness is set to be 0.5 nm. We conducted transient simulations with trapezoidal pulses applied at the gate. The pulse width is 200 μs and the rise and fall times are both 80 μs. The potential profile of Si inversion layer has been shown in Fig. 4.1. E_t^* and E_t are set to 0.4 ev and 1.4 ev below the HfO_2 conduction band minimum (CBM), respectively [29]. These values are close to those of the oxygen vacancy-related defects from first principle calculations (0.3, 1.3, 1.6 eV below CBM for VO2+, VO+, and VO, respectively [20]), corroborating their assumed role in electron trapping. A fixed interface charge density $3\times10^{12}cm^{-3}$ is considered. Both the trapping and detrapping process are shown in the figure. Here electrons trap to the empty defect level from the channel and detrap to the channel and also to the gate electrode.

4.4 SIMULATED THRESHOLD VOLTAGE SHIFT FOR NMOS STRUCTURES:

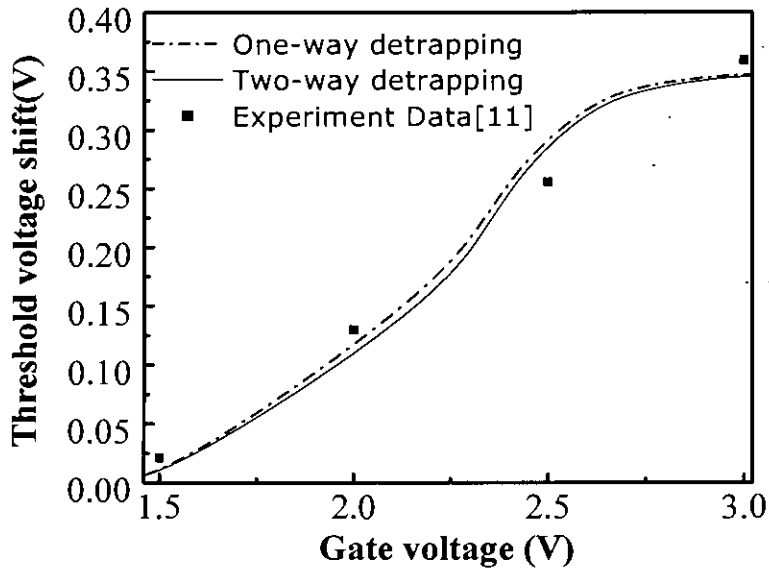

Fig. 4.2 Experimental result [11] and simulated threshold-voltage shift as a function of gate voltage considering only one-way detrapping and then two-way detrapping using an EOT of 1.6 nm according to experiments [11] and the SiO_2 thickness is set to be 0.5 nm [29].

In Fig. 4.2 we simulate our model keeping all the parameter same as used by Liu et al. [29] and present the threshold voltage shift considering two-way detrapping. For the shake of comparison, similar simulating result is also derived as [29] keeping all the parameters same, which has been presented in the same figure marked as 'one-way detrapping'. The pulse-width is 200 μs and the rise and fall times are both 80 μs [29]. Here we found negligible difference between these two approaches. Because due to comparatively higher physical thickness of HfO_2 and lower pulse width the electrons cannot trap at the oxide region near the poly-silicon gate, and there remain only a few electrons to tunnel through the gate/oxide interface.

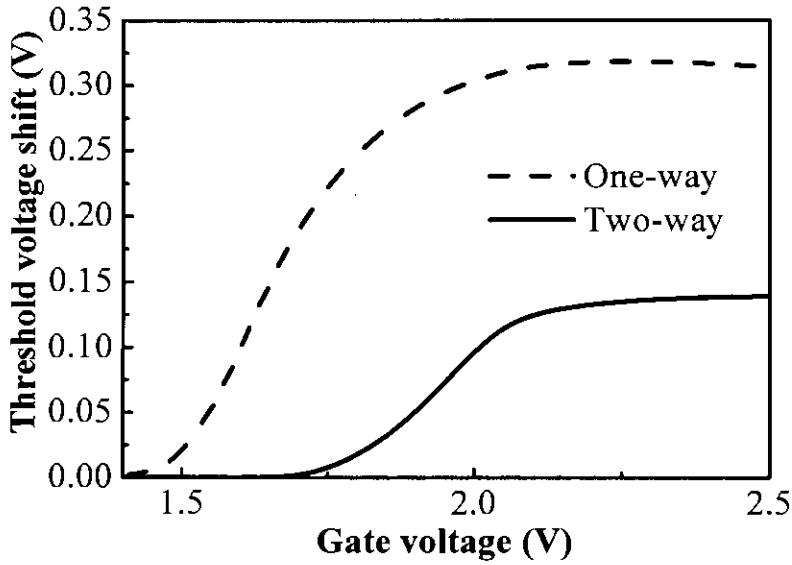

Fig. 4.3 Both trapping and detrapping tunneling time profile in the bulk of the HfO_2 considering 2.1nm EOT and 1.5nm.

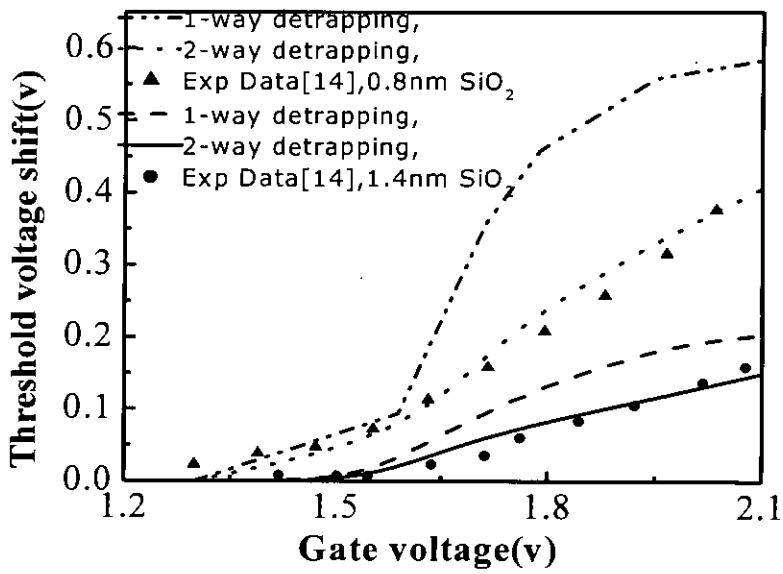

Fig. 4.4 Experimental result [14] and simulated threshold-voltage shift as a function of gate voltage considering only one-way detrapping and then two-way for two different PDA temperature

In Fig. 4.3 same simulated results for threshold voltage shift for EOT=1.5 nm have been shown keeping all the parameters same and we find that two-way detrapping effect becomes dominating as the EOT is reduced. In Fig. 4.4 same simulated results for threshold voltage shift have been performed on two different stacks

corresponding to 4.5nm HfO_2 thickness and two different N_2 Post Deposition Annealing (PDA) temperatures (interfacial SiO_2 thickness of 0.8nm for 600° PDA and 1.4nm for 800° PDA)[14]. Here a good agreement between simulated results considering two-way detrapping and experimental results [14] is achieved. The post deposition annealing (PDA) condition affects the trap density. The trapped charge can be reduced by annealing. Here it can be seen that the 800° C anneal is much more effective than the 600° C anneal in reducing the bulk-effective trap density.

4.5 SIMULATED THRESHOLD VOLTAGE SHIFT FOR PMOS STRUCTURES

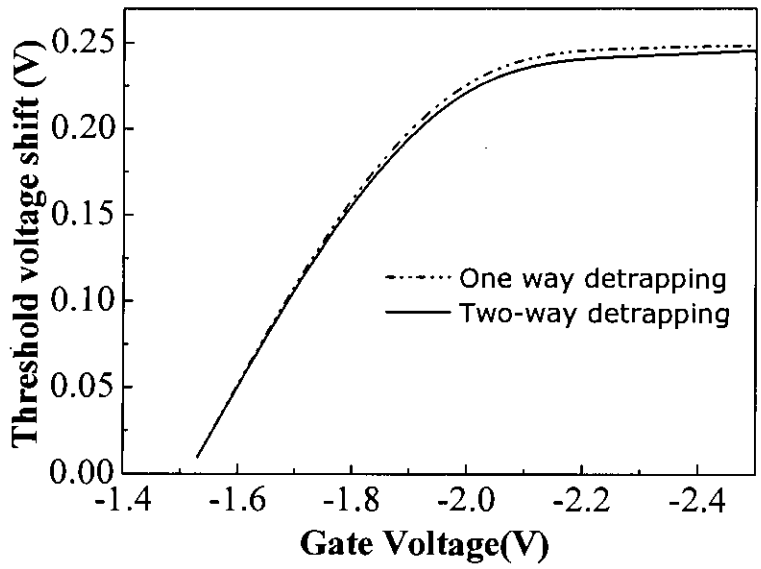

Fig. 4.5 Simulated threshold-voltage shift for PMOS as a function of negative gate voltage at EOT=2.1nm (consisting of 0.5 nm SiO_2 and 1.6 nm EOT of HfO_2) considering both one way detrapping and two way detrapping.

We simulate our model for hole trapping/detrapping in PMOS structure. The electronic structure of defects has been described by Robertson [35]. Here in Fig 4.5 we show the simulation results for an EOT of 2.1 nm (consisting of 0.5 nm SiO2 and 1.6 nm EOT of HfO_2). We find the difference between the two approaches is also negligible due to large oxide thickness.

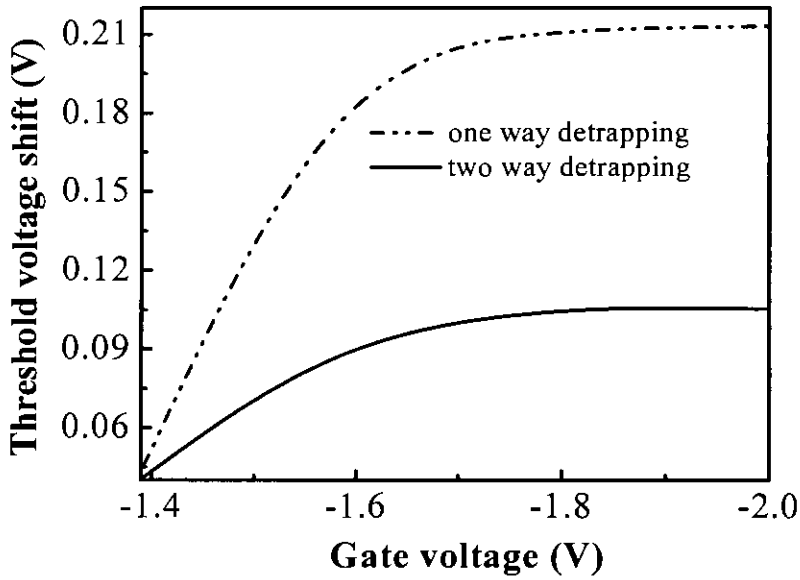

Fig. 4.6 Simulated threshold-voltage shift for PMOS as a function of negative gate voltage at EOT=1.5nm (consisting of 0.5 nm SiO2 and 1.0 nm EOT of HfO_2) considering both one way detrapping and two way detrapping.

In Fig. 4.6 simulated results for threshold voltage shift for EOT=1.5 (consisting of 0.5 nm SiO_2 and 1.0 nm EOT of HfO_2) nm have been shown keeping all the parameters same and we find that two-way detrapping effect becomes apparent with decreasing EOT, as expected . Due to the large barrier of HfO_2 for holes (3.4 eV) as compared to electrons (1.8 eV), the probability of hole injection is much smaller than electron injection for HfO_2 dielectric.

4.6 TUNNELING TIME PROFILE

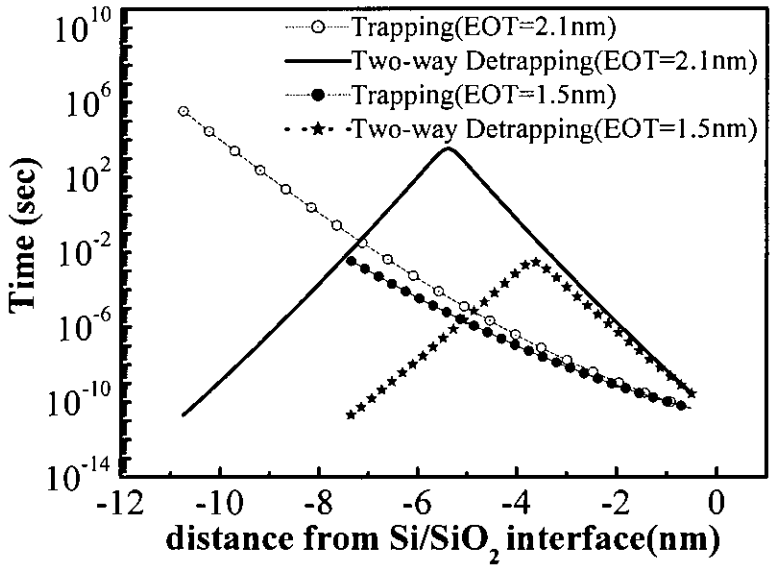

Fig. 4.7 Both trapping and detrapping tunneling time profile in the bulk of the HfO_2 considering 2.1nm EOT [3] and 4.5nm HfO2 [1] with interfacial SiO_2 thickness 0.8 nm according to the PDA temperature (600°C)

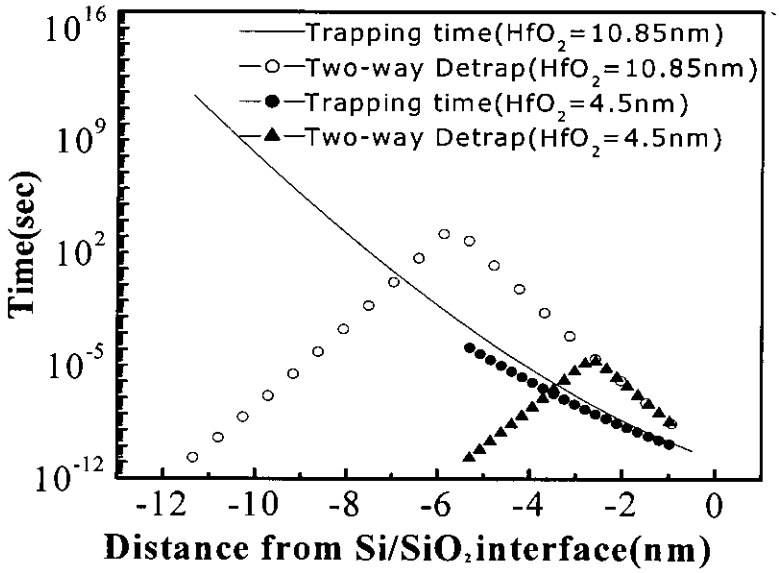

Fig. 4.8 Both trapping and detrapping tunneling time profile in the bulk of the HfO_2 considering 2.1nm EOT [29] and 4.5nm HfO_2 [14] with interfacial SiO_2 thickness 0.8 nm according to the PDA temperature (600^0C)

The trapping and detrapping time profiles in the bulk of the HfO_2 at an EOT of 2.1nm and 1.5 nm are shown in Fig. 4.7. Similar time profiles in the bulk of the HfO_2 at an EOT of 2.1nm (consisting of 0.5 nm SiO_2 and 1.6 nm EOT of HfO_2) and 4.5nm HfO_2 [14] with interfacial SiO_2 thickness 0.8 nm according to the PDA temperature (600°C) are shown in Fig. 4.8. From a same location it is found that detrapping time constant is higher than trapping time constant. It is because the electrons detrap from occupied defect level which is at lower energy level than the empty defect level to which electrons are trapped. The trapping time constant increases from the interface to the deep oxide. Here due to higher physical thickness (EOT=2.1nm) of HfO_2 the trapping time is high enough ($\sim 10^6$sec) not to reach the trap near the gate electrode. At higher gate voltage the two-way detrapping becomes negligible as the electric field becomes higher. But with the lowering of gate oxide thickness (EOT=1.5 nm), trapping time ($\sim 10^{-3}$sec) is small enough to make electrons transition near the gate side. That is why electrons also get detrapped to the gate. And this two-way detrapping plays a dominant role on lowering of threshold voltage shift. And at the middle of the HfO_2 oxide, the detrapping time is highest as trapped electrons have to transit a longer distance to detrap to both of the sides.

4.7 TRAP OCCUPATION FACTOR

Trap occupation factor is defined as ratio of trapped charge to the total density of surface bulk trap. It describes the trapped charge profile inside the HfO_2.

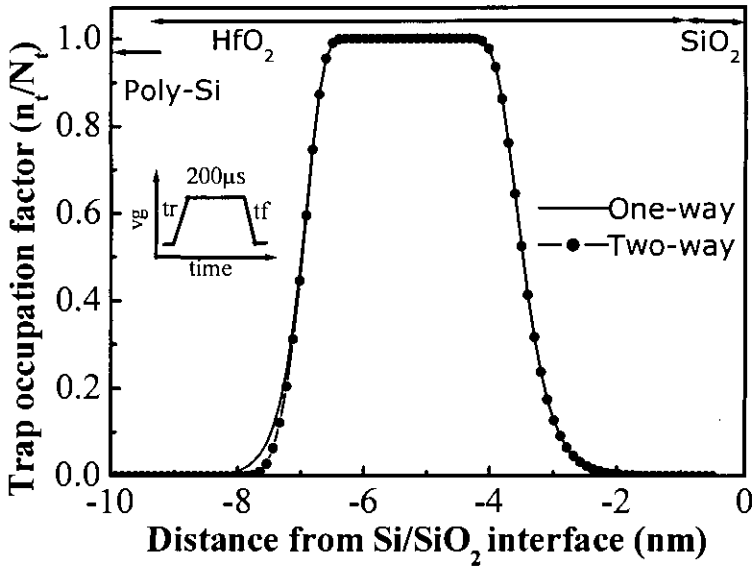

Fig. 4.9 Simulated profiles of trap occupation factor (n_t/N_t) inside the dielectric of 2.1 nm EOT (consisting of 0.5 nm SiO_2 and 1.6 nm EOT of HfO_2) for 2.5 V pulse height and width of the pulse is 200μs and $N_o=10^{19}/cm^3$)

The spatial profile of trapped electrons for EOT=2.1nm has been presented in Fig. 4.9. The shape of the curve shows that charges near the Si/Oxide interface get detrapped to the channel and also the charges near the gate/oxide region also discharges to the gate electrode. Here due to a higher physical thickness of HfO_2, electrons don't get trapped near the gate region and when we consider two-way detrapping a little charges tunnel to the gate. But at the middle of the oxide layer, charges can not detrap either to the channel or to the gate due to comparatively long distance. That is why we get higher charge density at the middle of the oxide region (4nm ~6nm).

4.7.1 EFFECT OF PULSE WIDTH

Here we demonstrate the effect of pulse width on the spatial profile of trapped electrons. We take a pulse width of 10 ms keeping other parameters same as Fig 4.9

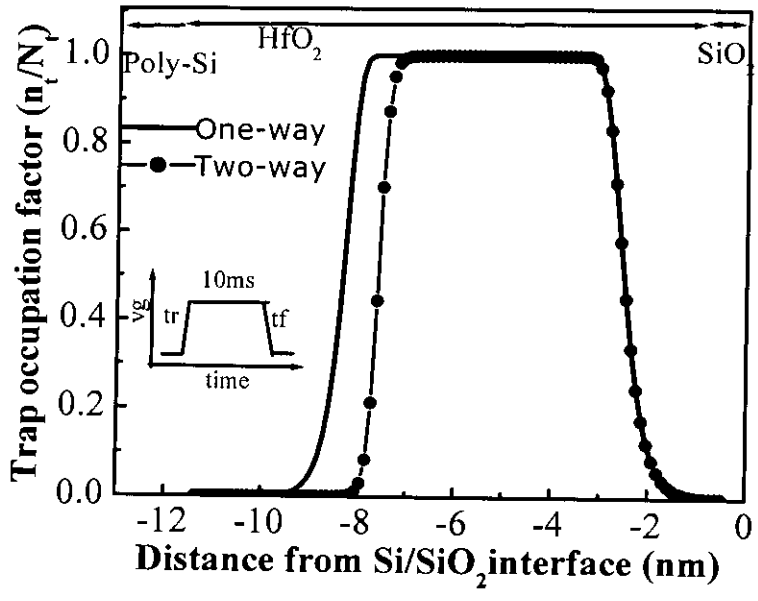

Fig. 4.10 Simulated profiles of trap occupation factor (n_t/N_t) inside the dielectric of 2.1 nm EOT 5nm (consisting of 0.5 nm SiO_2 and 1.6 nm EOT of HfO_2) for 2.5 V pulse height and width of the pulse is 10ms and $N_o=10^{19}/cm^3$)

In spite of having same physical thickness (EOT=2.1nm) we find that, the two-way detrapping effect is no longer negligible due to higher trapping time. It is because here the pulse width (10 ms) is large enough to make the electron transition near the gate/oxide region and we find the tail of the spatial profile curve up to ~9nm. And now sufficient electrons remains to detrap through the gate/oxide region and the tail of the spatial profile curve considering two-way detrapping reaches up to ~8nm near the gate region.

4.7.2 EFFECT OF EOT

Another parameter that can be a decisive parameter in our discussion is Effective Oxide Thickness (EOT). It has become a crying need to reduce the oxide thickness (EOT) in order to achieve lower switching time, reduces cost and lower power consumption.

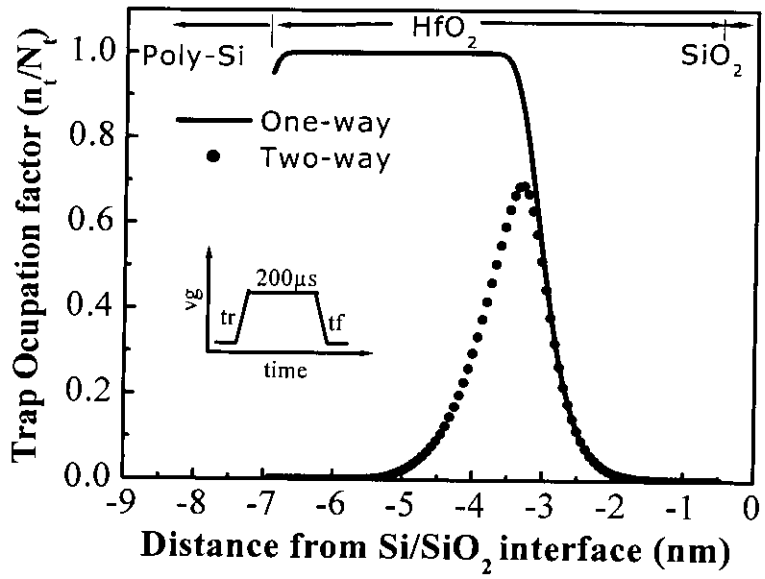

Fig. 4.11 Simulated profiles of trap occupation factor (n_t/N_t) inside the dielectric of 1.5 nm EOT (consisting of 0.5 nm SiO_2 and 1.0 nm EOT of HfO_2) for 2.5 V pulse height and width of the pulse is 200μs and $N_o=10^{19}/cm^3$)

So we reduce the EOT to 1.5nm and keep all other parameter same as Fig 4.9. And Fig. 4.11 shows the spatial profile of trapped electrons for EOT=1.5 nm. Here due to decreased physical thickness of HfO_2 the charges get trapped at the HfO_2 region adjacent to gate and in this case of one-way detrapping, these charges near the gate region cannot make transition to the channel due to long distance. But in case of two-way detrapping these accumulated charges can easily detrap to the gate electrode.

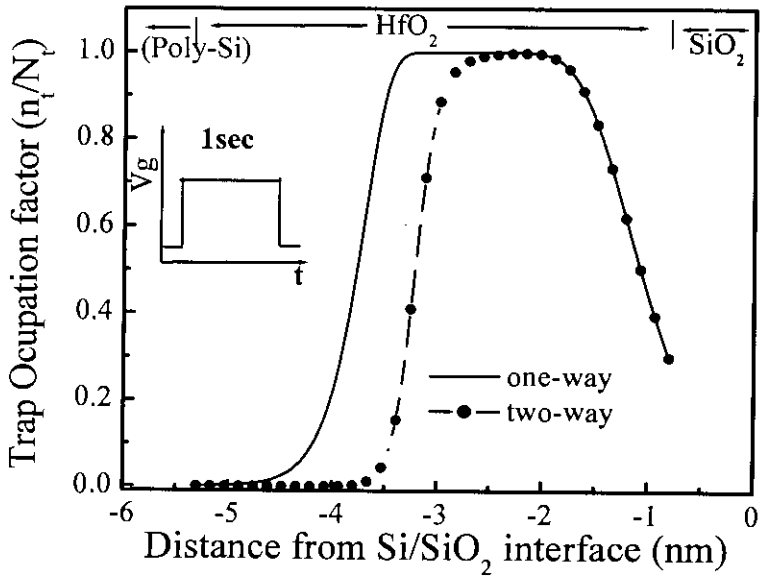

Fig. 4.12 Simulated profiles of trap occupation factor (n_t/N_t) inside the dielectric of 4.5nm HfO_2 [14] with interfacial SiO_2 thickness 0.8 nm according to the PDA temperature (600^0C) for 1.79 V pulse height and width of the pulse is 1s

Fig. 4.12 shows the spatial profile of trapped electrons for 4.5nm HfO_2 [14] with interfacial SiO_2 thickness 0.8 nm according to the PDA temperature (600°C). We simulate our model for the experimental model described by [14] and these curves pronounce our hypothesis more strongly as EOT is being reduced.

4.8 THRESHOLD VOLTAGE SHIFT AS A FUNCTION OF PULSE WIDTH

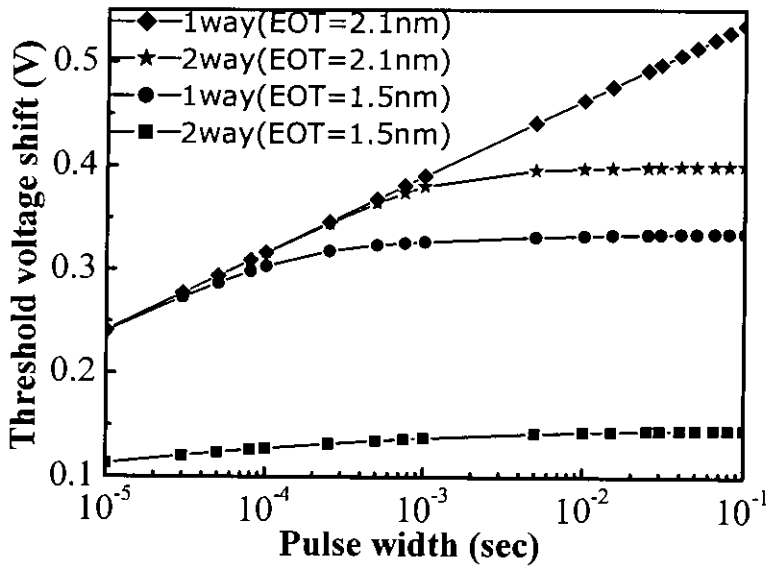

Fig. 4.13 Threshold voltage shift as a function of pulse width at EOT=2.1nm (consisting of 0.5 nm SiO_2 and 1.6 nm EOT of HfO_2) and at EOT=1.5nm (consisting of 0.5 nm SiO_2 and 1.0 nm EOT of HfO_2).

In Fig. 4.13 we show the threshold voltage shift verses trapping time at different EOT considering both one way-detrapping and two-way detrapping. We consider a rectangular pulse and increase the width of the pulse up to 0.1 second at a fixed inversion charge, $2\times10^{13}cm^{-2}$. For 2.1 nm EOT, threshold voltage shift increases with time due to higher physical thickness and up to 1ms we find a negligible difference between these two approaches. But the role of the detrapped electrons becomes more noticeable as we increase trapping time further. And by considering two-way detrapping we find that threshold voltage shift becomes almost saturated after 1ms. And the calculated threshold voltage shift will be overestimated while neglecting these detrapped electrons. Similar simulation for an EOT of 1.5 nm is also shown in the same figure. Here two-way detrapping effect indicates both

qualitative and quantitative changes in threshold voltage shift, which, we believe, is more realistic.

4.9 DISCHARGED CURRENT VS GATE VOLTAGE

Since charges detrap through the gate/oxide region so time has come to calculate the current contributed by those charges as it will become an additive quantity with the gate current. Here we calculate this current termed as "discharged current" by summing up all the current component of each detrapped charge using Eqn. 3.17

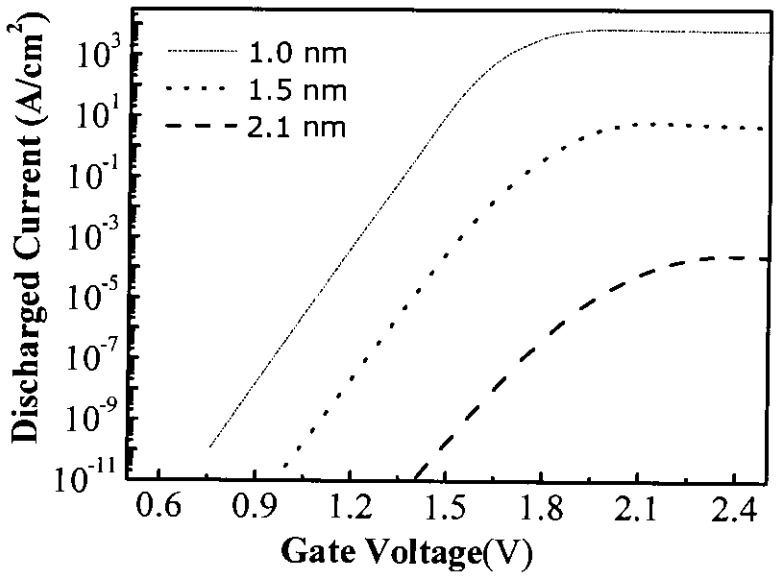

Fig. 4.14 Discharged current density versus gate voltage at different oxide thickness. Here substrate doping density, Na=5e17 cm^{-3}

The discharged current has been calculated and shown in Fig. 4.14. And this discharged current is higher to a great extent at lower EOT. For an oxide thickness of 1 nm (consisting of 0.5 nm SiO_2 and 0.5 nm EOT of HfO_2), this current density is ~10^4 A/cm^2 at a gate voltage of 2.5 V and neglecting the effect (two-way detrapping) the calculated total gate current will be underestimated as this current is an additive component with the gate current.

4.10 DISCHARGED CURRENT VS INVERSION CHARGE

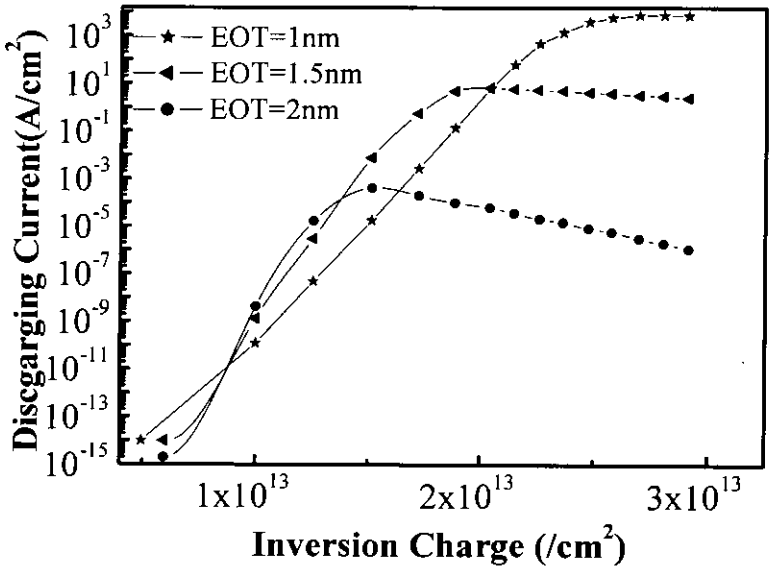

Fig. 4.15 Discharged current density versus inversion charge at different oxide thickness. Here substrate doping density, Na=5e17 cm^{-3}

This discharged current is shown as a function of inversion charge in Fig. 4.15 Here at lower inversion charge discharged current increases with lower EOT. Then opposite characteristic has been found but for higher inversion charge again discharged current increases with lower EOT. This phenomenon has been observed due to oxide-electric field variation caused by trapped charge in the HfO_2. For an oxide thickness of 1 nm (consisting of 0.5 nm SiO_2 and 0.5 nm EOT of HfO_2).This discharged current is high enough to limit further oxide thickness scaling. So this effect is no longer negligible as discharged current density increases with decreasing oxide thickness.

4.11 GATE CURRENT VS INVERSION CHARGE

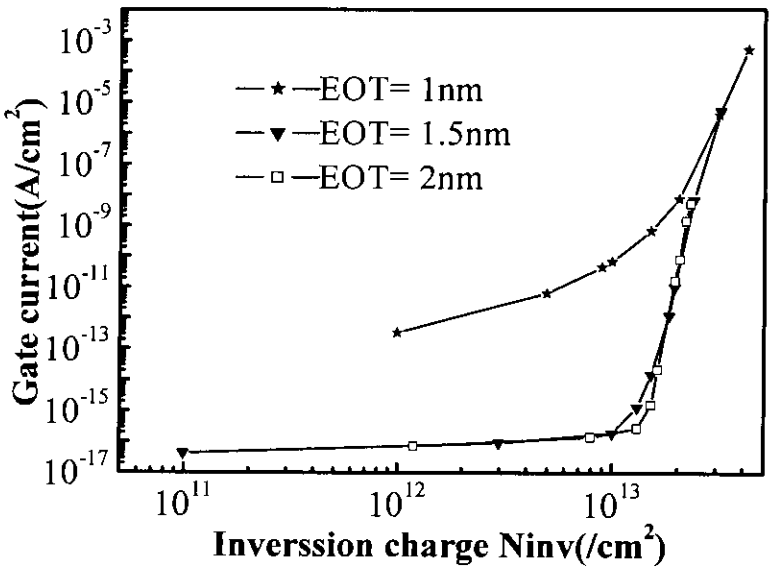

Fig. 4.16 Gate density versus inversion charge at different oxide thickness.

We have also calculated gate current shown in Fig 4.16. This current exhibits direct tunneling current at a lower inversion charges and with increasing inversion charges this current curve exhibits Fowler-Nordheim (FN) tunneling current. For different EOT (2nm, 1.5nm, and 1nm) this current component is comparatively low as expected for high-k materials. It increases with the increases of inversion charge because electron tunnels directly through the triangular potential well to the poly-silicon gate. Here we observe the variation of gate current with inversion charges of the channel. At low inversion charge ($\sim 10^{12}$), the magnitude of gate current is small ($\sim 10^{-17}$ for EOT of 2.1 nm) but with the increase of inversion charge, the gate current also increases.

4.12 GATE CURRENT VS GATE VOLTAGE

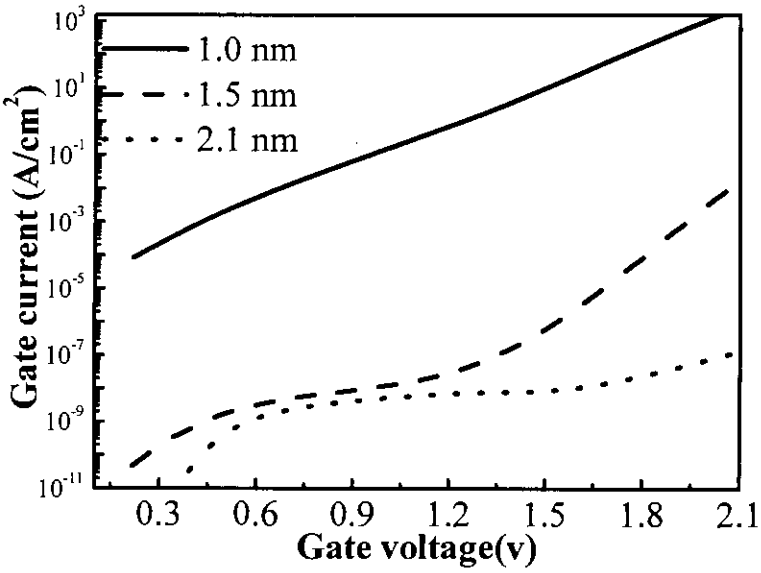

Fig. 4.17 Gate tunneling current density as a function of gate voltage at different oxide thicknesses.

Here the same gate current is shown as a function of gate voltage. For different EOT (2nm, 1.5nm, and 1nm) this current component is comparatively low as expected for high-k materials. The gate current shows different characteristics in two different regimes; the direct tunnelling (DT) regime and the Fowler-Nordheim (FN) regime. In case of 2.1 nm (0.5nm of SiO_2 and 1.6 nm EOT HfO_2) gate oxides, the direct tunneling current exhibits fluctuations when the applied voltage is less than 1.5V. However, the current rises sharply with the increase in the applied voltage as it enters the FN tunneling regime. In this regime the gate current shows an oscillating behaviour. At a gate voltage of 1.5V, the calculated gate current is approximately 2 A/cm^2 for an EOT of 1.0nm and the discharged current shown in Fig 4.14 is almost ~10A/cm^2. At a gate voltage of 2v we find the discharged current ~$10^4 A/cm^2$ and the gate current is ~10^2 cm/A^2 for an EOT of 1.0nm. So the discharged current is almost 5-100 times larger than the gate current. And to find out the total gate current we have to add these two current components. For an EOT of 2nm the gate current will be low as calculated before. But for lower EOT(1.5nm, 1nm), the discharging

current is high enough to increase the total gate current which was low for high-k dielectric stacks-a major feature of using dielectric stacks.

4.13 CONCLUSION

Here we have developed a model to simulate the charge trapping dynamics in HfO_2. With shrinking of physical size of the devices, EOT less than 2nm may be needed. Under this circumstance, two-way detrapping becomes an important phenomenon which can not be neglected. At the same time simulated results for higher pulse width will be overestimated by neglecting this effect. By reducing gate oxide thickness we can achieve lower threshold voltage but the detrapped electrons may have considerable effect on the instability of threshold voltage also the gate current increase. So there should be a good agreement between these two mechanisms to continue a further device scaling.

CHAPTER 5

CONCLUSION

5.1 SUMMARY

Here we develop a model to simulate the charge trapping dynamics in HfO_2. With shrinking of physical size of the devices, EOT less than 2nm may be needed. The charge trapping/detrapping model to analyze the gate threshold voltage instability reported so far have been using detrapping of the trapped charges back to the channel alone ignoring the detrapping to the gate. Here we show that neglecting the detrapping of the charges to the gate electrode may not have significant impact on threshold voltage instability for 2.1 nm EOT of HfO_2 and 200μs pulse width. But with further shrinking of device size, gate thickness is also expected to reduce and proposed two-way detrapping model presented here shows significant difference when compared to one-way detrapping model. The model proposed here is compared with reported experimental results and good agreements are achieved. Under this circumstance, two-way detrapping becomes an important phenomenon which can not be neglected. At the same time simulated results for higher pulse width will be overestimated by neglecting this effect. By reducing gate oxide thickness we can achieve lower threshold voltage but the detrapped electrons may have considerable effect on the instability of threshold voltage. Also these detrapped charges may increase the gate current as shown in this literature. One of the important features of using High-k material is to keep the gate current lower as compared to conventional thin oxide. This is because for a same EOT the physical thickness of High-k materials is larger than SiO_2. And its large physical thickness keeps the gate current lower. But as high-k materials posses large bulk trap centers which make charges get trapped and finally these charges detrap to the gate layer making the gate current larger as expected. So there should be more discussion on High-k materials using as a gate dielectrics with further device scaling.

5.2 SUGGETION FOR FUTURE WORK

Here we have modeled a quantum mechanical numerical study of charge trapping/detrapping phenomena in CMOS structures with high-k dielectric stacks.
We have considered Schottky barrier tunneling for trapping and detrapping time profile and neglected the Pool-Frenkel like electrons. And the effect of these charges can also be incorporated with necessary modification of the model. Here we use a normalize factor in the charge trapping equation and necessary modification can be made on that equation to avoid this fitting parameter. Another thing on which we can concentrate, that is the way of reducing charge chapping.

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