Application of a Single Electron Transistor in a Rate Controlled Oscillator

A thesis submitted to the Department of Electrical and Electronic Engineering of Bangladesh University of Engineering and Technology in partial fulfillment of the requirement for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

by

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DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY

2008

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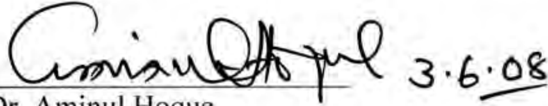

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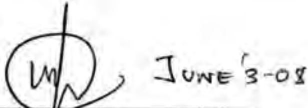

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I hereby declare that this thesis work or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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DEDICATION

To My Parents,

To my Sisters Keya, Ripa, Moni and Sony

And to our dearest Saba

Acknowledgement

I am grateful to the Almighty Allah for giving me the strength, courage and potentiality to complete this thesis.

I would like to express my heartiest gratitude to my supervisor Prof. Dr. Quazi Deen Mohd Khosru, Professor, Department of Electrical and Electronic Engineering (EEE), Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh. I am incredibly fortunate to be able to work with and learn from Prof. Khosru. Over the years, I came to realize what a great teacher and a great person he is. His constant pursuit of new ideas and uncompromising attention to important details imprinted in my mind a model of a great mentor to which I will endeavor to come close in coming years. I am afraid that I cannot thank Prof. Khosru enough for his trust and patient guidance (academically and personally) throughout my whole thesis work.

I am equally grateful to Prof. Dr. Aminul Hoque, Professor and Head, Dept of EEE, BUET and Prof. Dr. Satya Prasad Majumder, Professor and Former Head, Dept. of EEE, BUET for their support through out the period of the thesis work.

I would also like to thank Power IC ltd., the only IC design company in Bangladesh, at this moment, where I work as an IC design Engineer, for the support it provided and the environment it offered to me. It's the place where I have come to intimate contact with a group of utmost brilliant and most proactively intelligent group of colleagues whose positive criticism, outstanding understanding capability and endless thirst for innovation have driven me to a great extent. Their help is invaluable to me.

I express my wholehearted thanks to Aditya, Munna, Nayan, Omer, Riaz, Shimul, Suman, Tareq and my other circle of friends. Without their inspiration I might not be able to do this piece of work. I feel great to get this gifted group of friends.

And last, but not the least, I feel glad to thank my family members for their support. Their support and advices helped me a lot to make my way out towards the finishing line of this thesis work. I am grateful and would like to offer my deepest love to them.

Abstract

An application of the nano-electronic quantum device single electron transistor (SET) is presented in this thesis work. With the operating principle described, a circuit is proposed with the name of 'rate controlled oscillator'. The proposed circuit takes any small signal voltage wave as input variable and produces a pulse train of square wave with low duty cycle. The frequency of the pulses occurring at the output node is directly proportional to the slope (dv/dt) of the input voltage signal. The circuit thus generates a pulse with frequency proportional to the rate of change of the input signal and hence the name is given 'rate controlled oscillator'. This circuit is expected to find its application in many daily life applications as well as in many high end research projects.

A proposed adaptive sample and hold circuit which uses SET based rate controlled oscillator as its sampling frequency generator is also presented which is named 'adaptive sample and hold circuit'. The adaptive sample and hold circuit is capable of detecting the slope of the incoming signal and thereby generates proportional (to slope) sampling frequency – thus making it an intelligent circuit which is capable of employing variable sampling frequency depending on the slope of the input signal. This circuit maximizes performance and minimizes bit rate as compared to conventional sample and hold circuit whose sampling frequency has a preset value and is not capable of changing the sampling frequency when in operation. Simulation based comparison among adaptive sample and hold circuit and conventional sample and hold circuit is presented which reveals that adaptive sampler offers better performance regarding the sampling of signal with unpredictable composite frequency component and it also requires lower bit rate than conventional sample and hold circuit.

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CHAPTER 1
Introduction

1.1 Introduction

With increasing demand of higher processor speed and power efficient integrated circuit components scientist are in pursuit of newer devices. Although few works had been done in the similar field earlier [1-5], for the last few years tremendous advancement has been made on nano-electronics circuits and devices. Single Electron Transistor (SET) is one of those unique devices which hold promise to dominate the future world of minuscule circuitry. This chapter focuses on the history of this quantum device, discusses the basic physics of the transistor and finally explains the motivation of this thesis work.

1.2 History of Single Electron Transistor

The effects of charge quantization were first observed in tunnel junctions containing metal particles as early as 1968 [6]. Later, the idea that the Coulomb blockade can be overcome with a gate electrode was proposed by a number of authors [7-10], and Kulik and Shekhter [11] developed the theory of Coulomb-blockade oscillations, the periodic variation of conductance as a function of gate voltage. Their theory was classical, including charge quantization but not energy quantization. However, it was not until 1987 that Fulton and Dolan [12] made the first SET, entirely out of metal and observed predicted oscillation. They made a metal particle connected to two metal leads with tunnel junctions, all on top of an insulator with a gate electrode underneath. Since then, the capacitances of such metal SETs have been reduced to produce very precise charge quantization.

The first semiconductor SET was fabricated accidentally in 1989 by Scott-Thomas *et al.* [13] in narrow Si field effect transistors. In this case the tunnel barriers were produced by interface charges. Shortly thereafter Meirav *et al.* [14] made controlled devices, albeit with an unusual heterostructure with AlGaAs on the bottom instead of the top. In these and similar devices the effects of energy quantization were easily observed. [15-17] Only in the past few years have metal SETs been made small enough to observe energy quantization. [18] Foxman *et al.* [13] also measured the level width Γ and showed how the energy and charge quantization are lost as the resistance decreases toward h/e^2. In most cases the potential confining the electrons in a SET is of sufficiently low symmetry that one is in the regime of quantum chaos: the only quantity that is quantized is the energy. In this case there is a very sophisticated approach, based in part on random matrix theory, for predicting the distributions of peak spacing and peak heights [19-21]. There are challenging problems in this area that are still unsolved. In particular, there is great interest in how the interplay of exchange and level spacing determines the spin of a small metal SET [22].

In a SET of sufficiently high symmetry, angular momentum in the plane of the 2DEG is conserved, so shell structure is apparent. Another way to eliminate the scattering that destroys angular momentum conservation is to apply a magnetic field perpendicular to the 2DEG. At sufficiently high fields elegant patterns are seen in the single-electron-peak positions as a function of field. [23]

The evolution of Coulomb charging peaks with magnetic field has been interpreted with various degrees of sophistication, imitating the development of the theory of atoms. First one tries the "constant interaction model" in which electrons are treated as independent except for a constant Coulomb charging energy. This gives only a qualitative picture of the physics. In order to be quantitative, one needs to at least treat the electron-electron interactions self-consistently (analogous to the Thomas – Fermi model) [24], and for some cases one needs to include exchange and correlations.

In particular, it is found that electrons in an SET undergo a series of phase transitions at high magnetic field. [25]. One of these is well described by Hartree-Fock theory, but others appear to require additional correlations.

The future of research on SETs looks very bright. There are strong efforts around the world to make the artificial atoms in SETs smaller, in order to raise the temperature at which charge quantization can be observed. These involve self-assembly techniques [26] and novel lithographic and oxidation methods [27] whereby artificial atoms can be made nearly as small as natural ones. This is, of course, driven by an interest in using SETs for practical applications. However, as SETs get smaller, all of their energy scales can be larger, so it is very likely that new phenomena will emerge.

1.3 Basic Physics of Single Electron Transistor

A conventional field-effect transistor, the kind that makes all modern electronics work, is a switch that turns on when electrons are added to a semiconductor and turns off when they are removed. These on and off states give the ones and zeros that digital computers use for calculation. Interestingly, these transistors are almost completely classical in their physics. Their behavior are rarely affected by quantum mechanics. However, if one makes a new kind of transistor, in which the electrons are confined within a small volume and communicate with the electrical leads by tunneling, all this changes. One then has a transistor that turns on and off again every time one electron is added to it; we call it a single electron transistor (SET). Furthermore, the behavior of the device is entirely quantum mechanical.

The manipulation of single electrons was demonstrated in the seminal experiments by Millikan at the very beginning of the century, but in solid state circuits it was not implemented until the late 1980s, despite some important earlier background work [1-5]. The main reason for this delay is that the manipulation requires the reproducible fabrication of very small conducting particles, and their accurate positioning against

external electrodes. The necessary nanofabrication techniques have become available during the past two decades, and have made possible a new field of solid state physics,

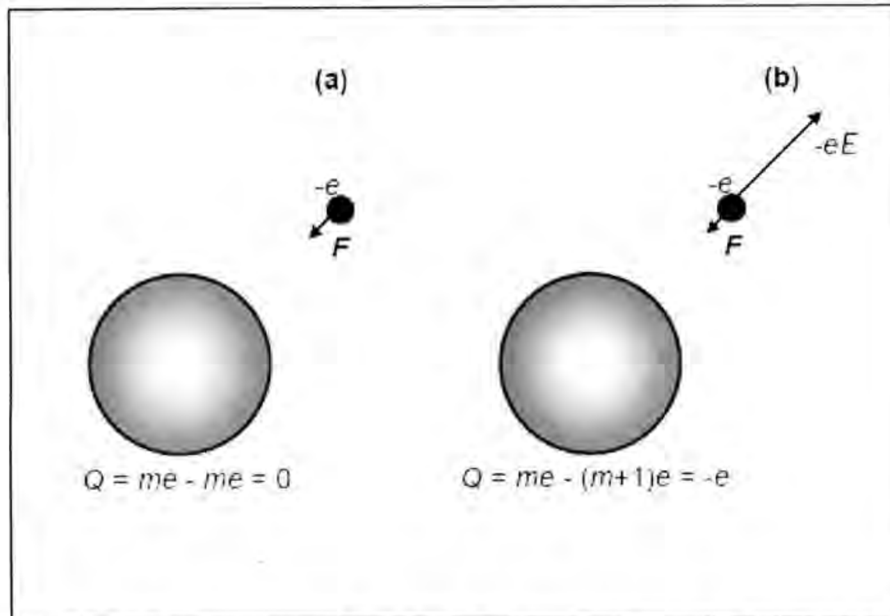

Fig. 1.1. The basic concept of single-electron control: a conducting island (a) before and (b) after the addition of a single electron. The addition of a single uncompensated electron charge creates an electric field ***E*** which may prevent the addition of the following electrons.

The basic concept of single-electronics is illustrated in Fig. 1.1. Let a small conductor (traditionally called an *island*) be initially electro-neutral, i.e. have exactly as many (m) electrons as it has protons in its crystal lattice. In this state the island does not generate any appreciable electric field beyond its borders, and a weak external force ***F*** may bring in an additional electron from outside. (In most single-electron devices, this injection is carried out by tunneling through an energy barrier created by a thin insulating layer). Now the net charge Q of the island is ($-e$), and the resulting electric field E repulses the following electrons which might be added. Though the fundamental charge $e \approx 1.6\text{x}10^{-19}$ Coulomb is very small on the human scale of things, the field E is inversely proportional to the square of the island size, and may become rather strong for nanoscale structures. For example, the field is as large as ~ 140 kV/cm on the surface of a 10-nm sphere in vacuum. The theory of single-electron phenomena shows that a more adequate measure of the strength of these effects is not the electric field, but the *charging energy*

$$E_c = e^2/C \qquad (1.1)$$

where C is the capacitance of the island (For a two-electrode capacitor, the elementary charging energy is of course $e^2/2C = E_c/2$, rather than E_c. However, if a single small conductor is charged with electrons from a source kept at a fixed electrochemical potential μ, this is E_c which gives the electrostatic contribution to the energy necessary for the transfer of one additional electron to the conductor: $e\Delta\mu \equiv E_a \approx E_c$ + kinetic energy – in Eqn. (1.2) this relationship is established) .

When the island size becomes comparable with the de Broglie wavelength of the electrons inside the island, their energy quantization becomes substantial. In this case the energy scale of the charging effects is given by a more general notion, the *electron addition energy* E_a. In most cases of interest, E_a may be well approximated by the following simple formula:

$$E_a = E_c + E_k. \qquad (1.2)$$

Here E_k is the quantum kinetic energy of the added electron; for a degenerate electron gas, $E_k = 1/g(\varepsilon_F)V$, where V is the island volume and $g(\varepsilon_F)$ is the density of states on the Fermi surface.

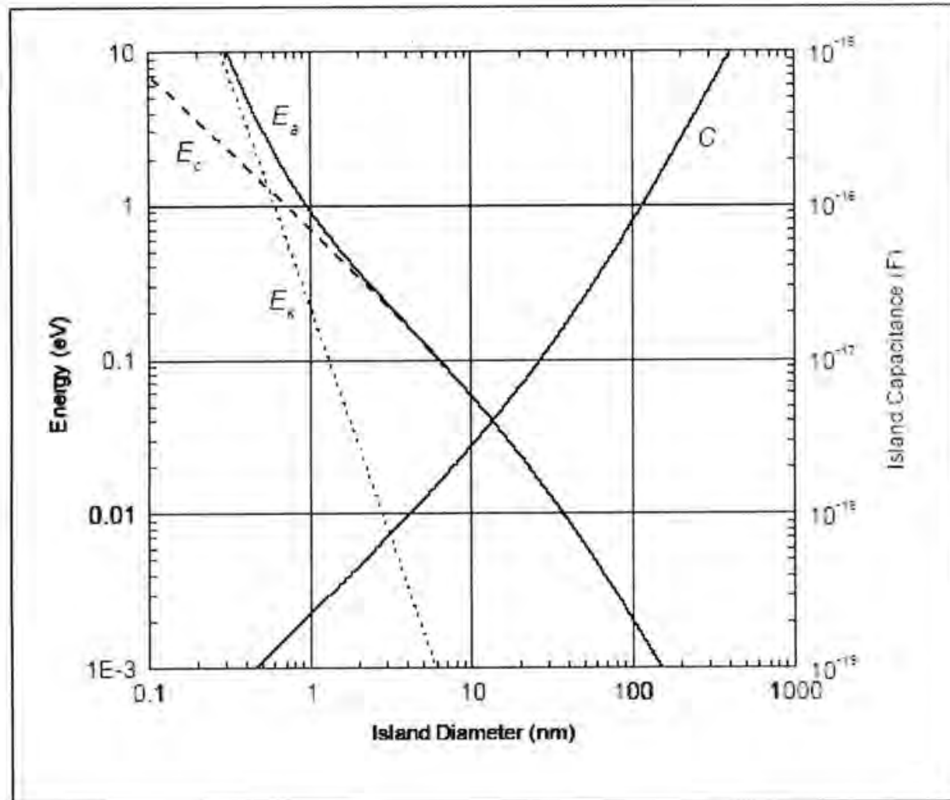

Fig. 1.2 Single-electron addition energy E_a (solid line), and its components: charging energy E_c (dashed line) and electron kinetic energy E_k (dotted line), as calculated using Eqs. (1.1) and (1.2) for a simple model of a conducting island. In this model the island is a round 3D ball with a free, degenerate electron gas (electron density n = 1022 cm^{-3}, electron effective mass $m = m_0$), embedded into a dielectric matrix (dielectric constant, ε_r = 4), with 10% of its surface area occupied by tunnel junctions with a barrier thickness d = 2 nm.

Fig. 1.2 shows the total electron addition energy as a function of the island diameter, as calculated using Eqn. (1.2) for a simple but representative model. For 100-nm-scale devices which were typical for the initial stages of experimental single-electronics, E_a is dominated by the charging energy E_c and is of the order of 1 meV, i.e. ~ 10 K in temperature units. Since thermal fluctuations suppress most single-electron effects unless

$E_a \gtrsim 10\ k_BT$ these experiments have to be carried out in the sub-1-K range (typically, using helium dilution refrigerators). On the other hand, if the island size is reduced below ~10 nm, E_a approaches 100 meV, and some single-electron effects become visible at room temperature. However, most suggested digital single-electron devices require even higher values of E_a (~ 100 k_BT) in order to avoid thermally-induced random tunneling events, so that for room temperature operation the electron addition energy E_a has to be as large as a few electron-volts, and the minimum feature size of single-electron devices has to be smaller than ~1 nm (Fig. 1.2). In this size range the electron quantization energy E_k becomes comparable with or larger than the charging energy E_c for most materials; this is why islands this small are frequently called *quantum dots*. Their use involves not only extremely difficult nanofabrication technology (especially challenging for large scale integration), but also some major physics problems including the high sensitivity of transport properties to small variations of the quantum dot size and shape. This is why it is very important to develop single-electron devices capable of operating with the lowest possible ratio E_a/k_BT . As we will see below, some devices may work in the size range where $E_c > E_k$ even at room temperature, thus avoiding complications stemming from the energy quantization effects.

1.4 Motivation

Single Electron Transistor (SET) is continually being tested by researchers and engineering scientist in various applications. Being a nano-electronic device, SET is a potential candidate for components of molecular computing, quantum computing and nano-electro-mechanical devices (NEMS). SET island is also explained to behave like artificial atom because electrons are confined in the quantum dot island.

This work introduces a new type of application of SET that will eventually open many other doors to the different branches of nano-electronics. Detecting the rate of change of any signal is vital in many applications. However, since the future world is expected to be dominated by the nano-scale transistors it's now well-timed to search for plausible application of these nano devices. Using the SET, this work proposes a circuit which senses the slope of the incoming signal and produces a frequency proportional to the slope of the input signal and hence it is named as rate (dv/dt) controlled oscillator.

Sample and hold circuits are one of the most important circuit blocks in the present world where everything comes in digital format. Conventional sample and hold circuit which employs fixed frequency sampling has major drawback of ignoring unpredicted high frequency signal component. To eliminate this limitation in signal sampling, an adaptive sample and hold circuit is proposed which makes an effective use of the SET implemented Rate Controlled Oscillator. It is likely that this application circuit will be useful in many practical signal sampling applications, e.g. all sorts of analog to digital converter, accelerometer, digital seismograph etc.

CHAPTER 2
SET Structure, Operation and Fabrication

2.1 Introduction

Single electron transistor is unique in its structure, operation and characteristics. The fabrication process of SET requires delicate methodology and machinery. This chapter describes the physical structure of SET. The equivalent circuit is also discussed with simplified transistor view. The theory of Coulomb blockade which is the heart of the transistor operation is discussed which is followed by the operating principle of the transistor itself. Later, a brief discussion on SET fabrication technology is presented.

2.2 Physical Structure of Single Electron Transistor

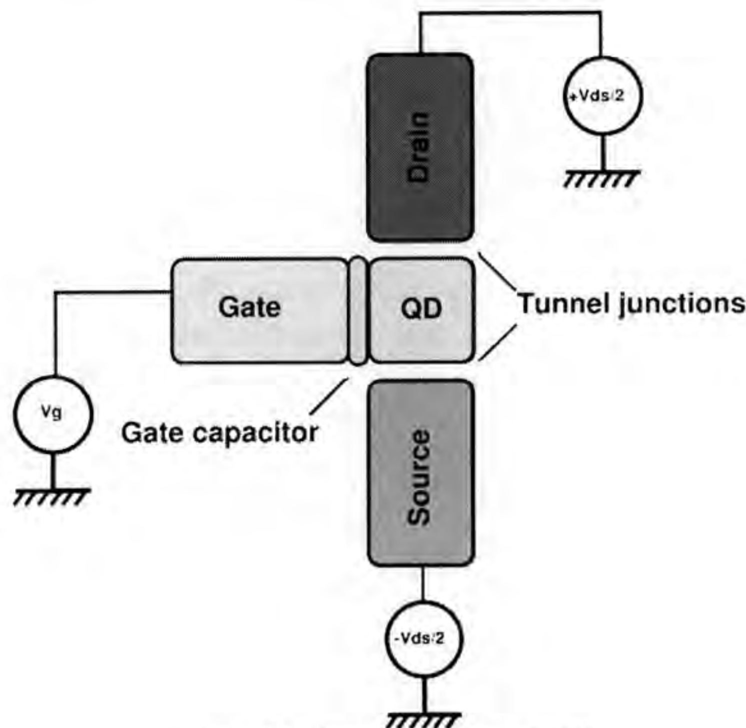

Fig. 2.1: Structural view of SET

The SET transistor can be viewed as an electron box that has two separate junctions for the entrance and exit of single electrons (Fig. 2.1). It can also be viewed as a field-effect transistor in which the channel is replaced by two tunnel junctions forming a metallic

island. The voltage applied to the gate electrode affects the amount of energy needed to change the number of electrons on the island.

The SET transistor comes in two versions that have been nicknamed "metallic" and "semiconducting". These names are slightly misleading, however, since the principle of both devices is based on the use of insulating tunnel barriers to separate conducting electrodes.

In the original metallic version fabricated by Fulton and Dolan, a metallic material such as a thin aluminum film is used to make all the electrodes. The metal is first evaporated through a shadow mask to form the source, drain and gate electrodes. The tunnel junctions are then formed by introducing oxygen into the chamber so that the metal becomes coated by a thin layer of its natural oxide. Finally, a second layer of the metal - shifted from the first by rotating the sample - is evaporated to form the island.

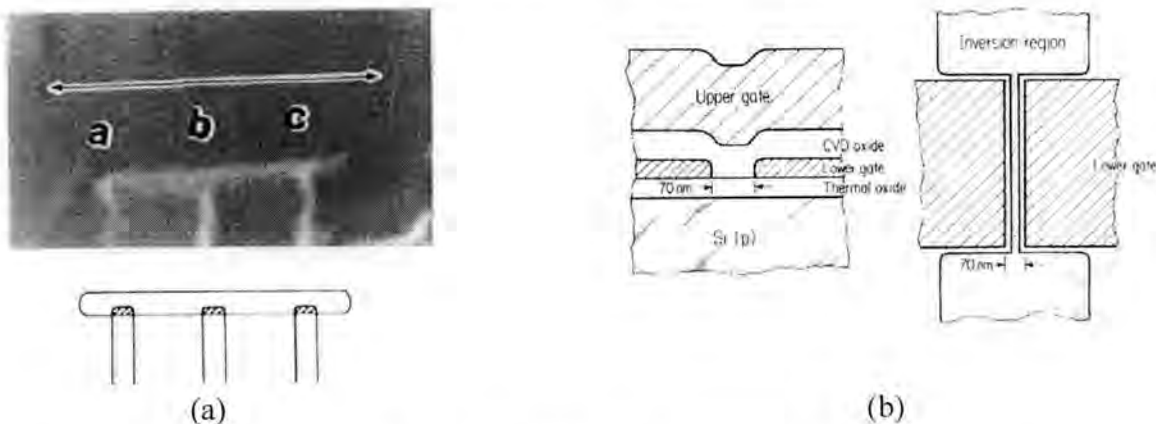

Fig. 2.2: Different types of SET proposed earlier (a) metallic SET [12] (b) semiconducting SET [13]

In the semiconducting versions, the source, drain and island are usually obtained by "cutting" regions in a two-dimensional electron gas formed at the interface between two layers of semiconductors such as gallium aluminum arsenide and gallium arsenide. In this case the conducting regions are defined by metallic electrodes patterned on the top semiconducting layer. Negative voltages applied to these electrodes deplete the electron gas just beneath them, and the depleted regions can be made sufficiently narrow to allow tunneling between the source, island and drain. Moreover, the electrode that shapes the island can be used as the gate electrode.

In this semiconducting version of the SET, the island is often referred to as a quantum dot, since the electrons in the dot are confined in all three directions. In the last few years researchers at the Delft University of Technology in the Netherlands and at NTT in Japan have shown that quantum dots can behave like artificial atoms. Indeed, it has been possible to construct a new periodic table that describes dots containing different numbers of electrons [28]

A simplified schematic representation of SET may look like as shown in Fig. 2.3, where drain, source and the gate electrodes are shown capacitively coupled to the quantum dot island. In this model all isolation barriers are replaced by capacitor including the gate dielectric.

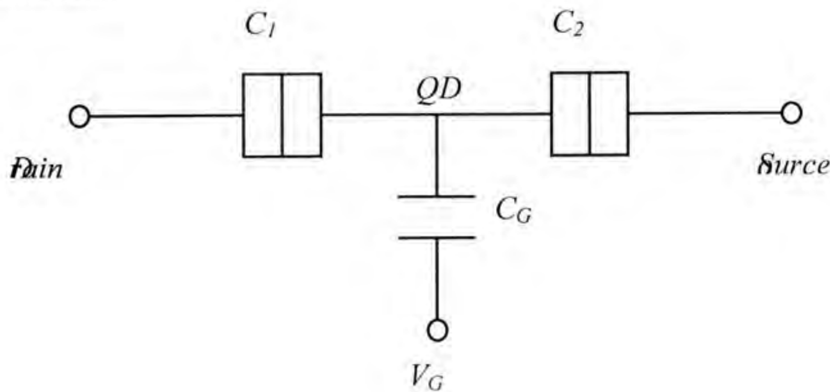

Fig. 2.3: Schematic representation of SET

The following figure shows a possible 3-D view of a SET where quantum dot island is exaggerated for illustration purposes. In reality, the island is usually 35~50nm in length/width.

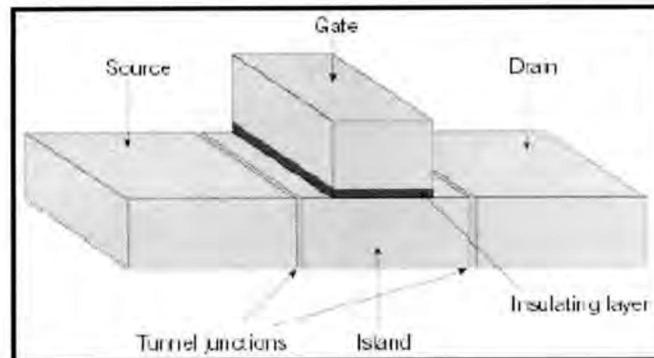

Fig. 2.4: A 3-D representation of SET [29]

An atomic force microscopy image of a fabricated SET is shown in Fig. 2.5. This fabricated SET is demonstrated to operate at room temperature [30].

2.3 Coulomb Blockade:

In physics, a Coulomb blockade, named after Charles-Augustin de Coulomb, is the increased resistance at small bias voltages of an electronic device comprising of at least one low-capacitance tunnel junction.

A tunnel junction is, in its simplest form, a thin insulating barrier between two conducting electrodes. If the electrodes are superconducting, Cooper pairs with a charge of two elementary charges carry the current. In the case that the electrodes are normal-conducting, i.e. neither superconducting nor semiconducting, electrons with a charge of one elementary charge carry the current. The following reasoning is for the case of tunnel junctions with an insulating barrier between two normal-conducting electrodes (NIN junctions).

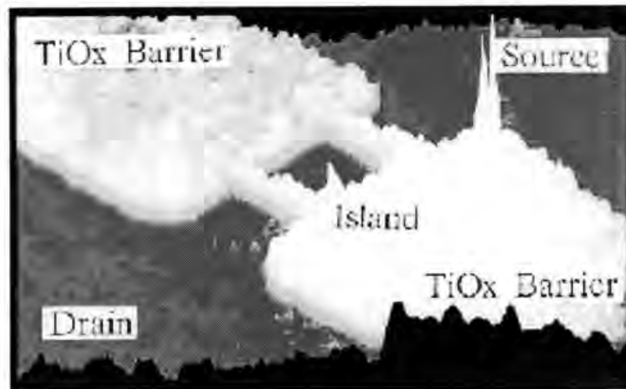

Fig. 2.5: An AFM (atomic force microscopy) image of a SET built by the STM (scanning tunneling microscope) nano-oxidation process. The TiOx tunneling barrier shown here surrounds the quantum dot island which is 35nm X 35nm in area, the width of the TiOx dielectric is 20nm with a relative permittivity of $\varepsilon_r=24$ and barrier height of 285meV. With the 3-nm thick Ti blanket layer this structure ensures small tunneling junction area and corresponding tunnel capacitance becomes as small as 10^{-19} F, which allows the set to be operated at room temperature. [30]

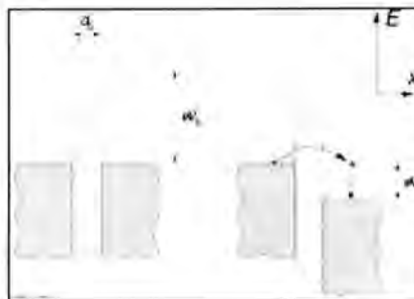

Fig. 2.6: Schematic representation of an electron tunneling through a barrier [31]

According to the laws of classical electrodynamics, no current can flow through an insulating barrier. According to the laws of quantum mechanics, however, there is a nonvanishing (larger than zero) probability for an electron on one side of the barrier to reach the other side which is generally known as quantum tunneling. When a bias voltage

is applied, this means that there will be a current flow. In first-order approximation, that is, neglecting additional effects, the tunneling current will be proportional to the bias voltage. In electrical terms, the tunnel junction behaves as a resistor with a constant resistance, also known as an ohmic resistor. The resistance depends exponentially on the barrier thickness. Typical barrier thicknesses are on the order of one to several nanometers.

An arrangement of two conductors with an insulating layer in between not only has a resistance, but also a finite capacitance. The insulator is called dielectric in this context, as the tunnel junction behaves as a capacitor.

Due to the discreteness of electrical charge, current flow through a tunnel junction is a series of events in which exactly one electron passes (tunnels) through the tunnel barrier (We neglect events in which two electrons tunnel simultaneously). The tunnel junction capacitor is charged with one tunneling electron (elementary charge unit), causing a voltage buildup $U = e / C$, where e is the elementary charge of 1.6×10^{-19} Coulomb and C the capacitance of the junction. If the capacitance is very small, the voltage buildup can be large enough to prevent another electron from tunneling. The electrical current is then suppressed at low bias voltages; the resistance of the device is no longer constant. The increase of the differential resistance around zero bias is called the Coulomb blockade.

In order for the Coulomb blockade to be observable, the temperature has to be low enough so that the characteristic charging energy (the energy that is required to charge the junction with one elementary charge) is larger than the thermal energy of the charge carriers. For capacitances below 1 femto-farad (10^{-15} farad), this implies that the temperature has to be below about 1 Kelvin. This temperature range is routinely reached for example by dilution refrigerators.

To make a tunnel junction in plate condenser geometry with a capacitance 1 femto-farad, using an oxide layer of electric permeability 10 and thickness one nanometer, one has to create electrodes with dimensions of approximately 100 by 100 nanometers. This range of dimensions is routinely reached for example by electron beam lithography and appropriate pattern transfer technologies, like the Niemeyer-Dolan technique, also known as shadow evaporation technique.

Another problem with the observation of the Coulomb blockade is the relatively large capacitance of the leads that connect the tunnel junction to the measurement electronics.

The simplest device in which the effect of Coulomb blockade can be observed is the so-called single electron transistor. It consists of two tunnel junctions sharing one common electrode with a low self-capacitance, known as the *island*. The electrical potential of the island can be tuned by a third electrode (the *gate*), capacitively coupled to the island.

In the blocking state, as shown in the Fig. 2.7 (top portion), no accessible energy levels are within tunneling range of the electron on the source contact. All energy levels on the island electrode with lower energies are occupied.

In Fig. 2.7 (bottom portion), when a positive voltage is applied to the gate electrode the energy levels of the island electrode are lowered. The electron (marked 1.) can tunnel onto the island (marked 2.), occupying a previously vacant energy level. From there it can tunnel onto the drain electrode (marked 3.) where it inelastically scatters and reaches the drain electrode Fermi level (marked 4). [31]

The energy levels of the island electrode are evenly spaced with a separation of ΔE. ΔE is the energy needed to each subsequent electron to the island, which acts as a self-capacitance C. The lower the C, the bigger ΔE gets. It is crucial for ΔE to be larger than the energy of thermal fluctuations k_BT, otherwise an electron from the source electrode can always be thermally excited onto an unoccupied level of the island electrode, and no blocking can be observed.

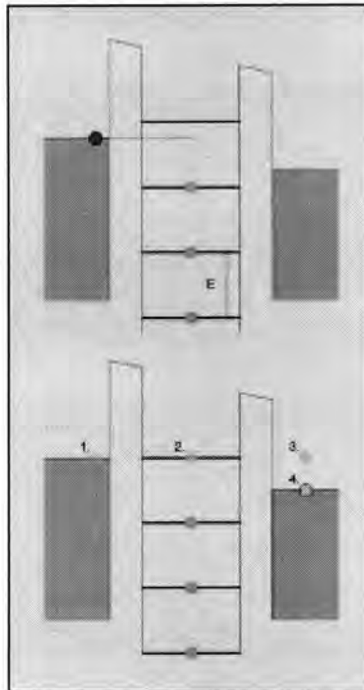

Fig. 2.7: Energy level of source, island and drain of a SET (left to right). (top) blocking stage and (bottom) transmitting stage [31]

2.4 Theory of Operation

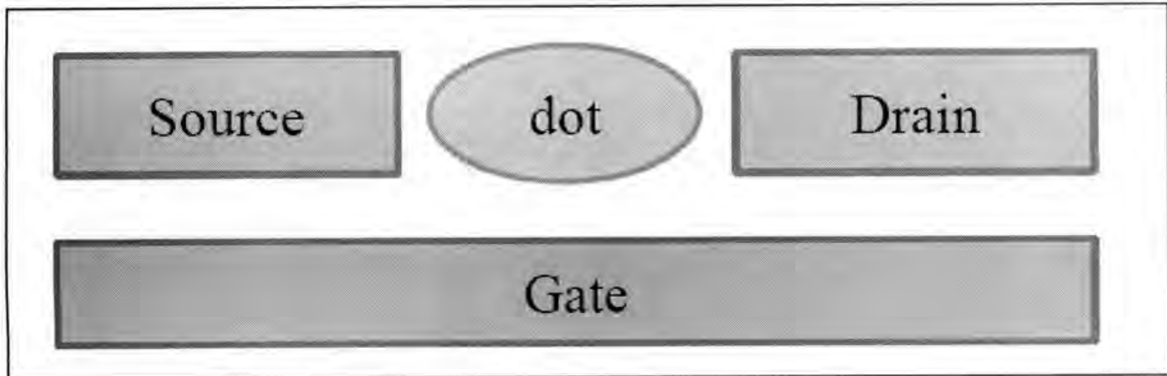

Fig. 2.8 The single electron transistor. A small dot is separated from the source and drain electrodes by tunnel barriers. It is also coupled to the gate electrode capacitively.

Fig. 2.8 shows a device schematic of a single electron transistor, where a dot is surrounded by three electrodes. All three electrodes are coupled to the dot capacitively; a Potential change in any of them can cause an electrostatic energy change in the dot. Only two electrodes (source and drain) are tunnel coupled to the dot and electron transport is allowed only between the dot and these two electrodes. Since the dot is connected to the source and drain electrodes by a tunnel barrier (meaning an electron is either on the dot or one of the electrodes), the number of electrons on the dot, N is well defined. We assume that all interactions between an electron on the dot and all other electrons on the dot or on the electrodes can be parameterized by the total capacitance C. We also assume that C does not depend on different charge states of the dot. Then the total electrostatic energy for a dot with N electrons will become $Q^2/2C = (Ne)^2/2C$. When N electrons reside on the dot, the total energy is

$$U(N) = \sum_{i=1}^{N} E_i + \frac{(Ne)^2}{2C} \tag{2.1}$$

After an additional electron is added to the dot, the total energy increases to

$$U(N+1) = \sum_{i=1}^{N+1} E_i + \frac{[(N+1)\cdot e]^2}{2C} \tag{2.2}$$

Here E_i is the chemical potential of the dot with i electrons. This is the energy of the orbital of the dot that the i-th electron would occupy if there were no electron-electron interactions. The electrochemical potential μ_N is then,

$$\mu_N = E_N + \left(N + \frac{1}{2}\right)\cdot\frac{e^2}{C} \tag{2.3}$$

By definition, the electrochemical potential μ_N is the minimum energy required for adding N-th electron. As long as μ_N is below both μ_S and μ_D , the N-th electron will be added to the dot. Likewise, to add one more electron to a dot with N electrons,

$$\mu(N+1) = \mu_N + \frac{e^2}{C} + \Delta E \tag{2.4}$$

needs to be lower than both μ_S and μ_D, where $\Delta E = E_{N+1} - E_N$. For simplicity, we will assume that ΔE does not change for different charge states of the dot.

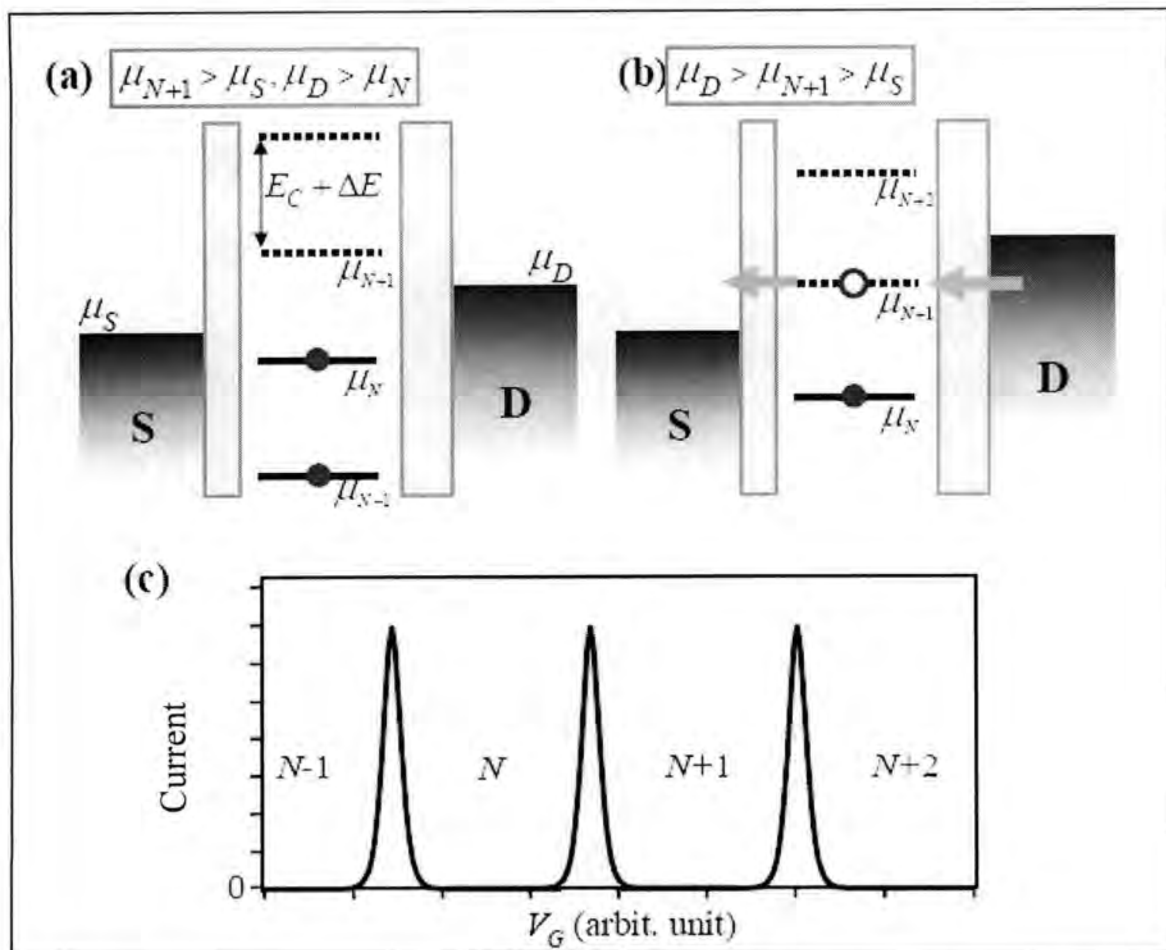

Fig. 2.9 Electron transport in a single electron transistor and I-V characteristics of SET. Energy diagrams for two different energy configurations are shown. In (a), the number of electrons on the dot is fixed at N ("off"-state) and the current is blocked. In (b), the electron number on the dot oscillates between N and N+1 ("on"-state). (c) The drain-source current as a function of the gate bias (V_G) displays the Coulomb oscillation. Each valley of current is labeled by the number of electrons on the dot.

This allows us to drop the subscript N for ΔE . Therefore, the N+1-th electron needs to have an energy larger than the one for the N-th electron by $e^2/C + \Delta E$. This is the charge addition energy. The first term $e^2/C \equiv E_C$, which is called the charging energy, is the energy that is required to overcome the Coulomb repulsion among different electrons.

The second term ΔE is the result of quantized excitation spectrum of the dot. Fig. 2.9(a) illustrates the energy diagram of a single electron transistor with $\mu_{N+1} > \mu_S$ *and* $\mu_D > \mu_N$. The dot will have N electrons and the solid lines below μ_N represent all the filled electrochemical levels. The lowest dotted line represents μ_{N+1} and it cannot be occupied since it is above the electrode Fermi levels. Therefore, the dot is stable with N electrons and hence the current cannot flow through the dot. In other words, the current is "blocked" due to the charge addition energy. Fig. 2.9(b) illustrates another case where $\mu_D > \mu_{N+1} > \mu_S$. In this case, the $N+1$-th electron can be added from the drain and then it can leave the source electrode. This process allows electric current to flow, constantly switching the charge state of the dot between N and $N+1$.

When we sweep the gate voltage V_G, the electrochemical potential of the dot changes linearly with V_G and this allows one to change the number of electrons on the dot. The drain source current as a function of V_G at a low bias is illustrated in Fig. 2.9(c). The current characteristic shows a series of peaks as well as valleys. In the valleys, the number of electrons on the dot is fixed and the current is blocked by the charge addition energy $e^2/C + \Delta E$. This corresponds to the case depicted in Fig.2.9(a). The dot has a well-defined electron number in each valley; N, N+1, N+2 and so on. The conductance peak in this plot corresponds to the case depicted in Fig. 2.9(b), where the dot can oscillate between two adjacent charge states. For example, the conductance peak located between the N-electron valley and the (N+1)-electron valley represents the dot carrying current by oscillating between N and N+1 electron states. These conductance peaks are called Coulomb oscillations. To be able to observe Coulomb oscillations, the charge addition energy should be much larger than the thermal energy k_BT. Otherwise, thermal fluctuation effect will be dominant and the Coulomb oscillation will disappear. Also the electron number on the quantum dot should be a well-defined observable, which requires the contact between the dot and the leads to be resistive. Quantitatively, the contact resistance needs to be larger than the resistance of a single conductance channel (*e.g.* a point contact),$h/e^2 \sim 25.81 k\Omega$. These conditions are summarized below.

$$e^2/C + \Delta E. >> k_BT \tag{2.5}$$
$$R_{contact} >> he^2 \tag{2.6}$$

To date, single electron transport behavior has been observed from many different nanostructures. They include metallic nanoparticles [12], semiconductor heterostructures [13, 32], carbon nanotubes [33, 34] and semiconducting nanocrystals[34]. More recently, similar behaviors were observed from devices made from single molecules [24-25, 35].

2.4 Stability Plot, Regions of Operation and I-V characteristics

Proper operation of the SET requires proper biasing of gate and drains electrodes with respect to the gate electrode. Depending on the biasing, the SET can exhibit continuous oscillation characteristics in the drain current or a static ON state operation or a static OFF condition. Different regions of operation based on different level of biasing are best studied via stability plots. Depending on the biasing level, stability plot identifies the operating point of the SET describing whether the transistor will remain ON or OFF

Fig. 2.10 shows a typical stability plot with Coulomb diamonds. The diamond shaped shaded regions shown in the middle of the figure is called Coulomb diamond. These shaded regions correspond to particular value of gate and drain biasing (V_G and V_D respectively). These shaded diamonds are also known as stable regions for SET operation. While inside the region, there is always an excess amount of electron in the quantum dot island and so electron transport is effectively suppressed by the Coulomb blockade. Outside the stable region, there are numerous operating points where SET can be operated in a mode when it allows tunneling. In this mode of operation, the tunneling is not suppressed by the Coulomb blockade energy. The operating point, hence the mode of operation is defined both by the gate voltage (V_G) and the drain-source voltage difference (V_D).

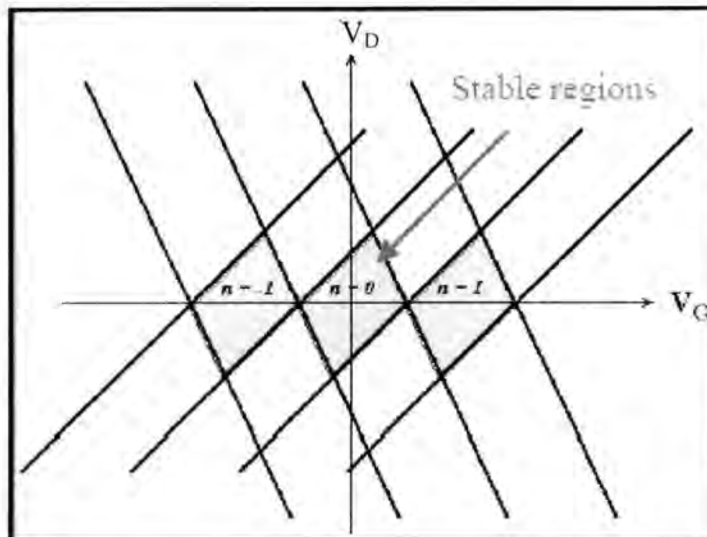

Fig. 2.10: Stability plot. Shaded diamonds corresponds to stable region where electron transportation is effectively suppressed by Coulomb blockade.

Two separate conditions are described below to clarify the operating regions.
Condition 1: Gate voltage fixed, Drain bias swept.

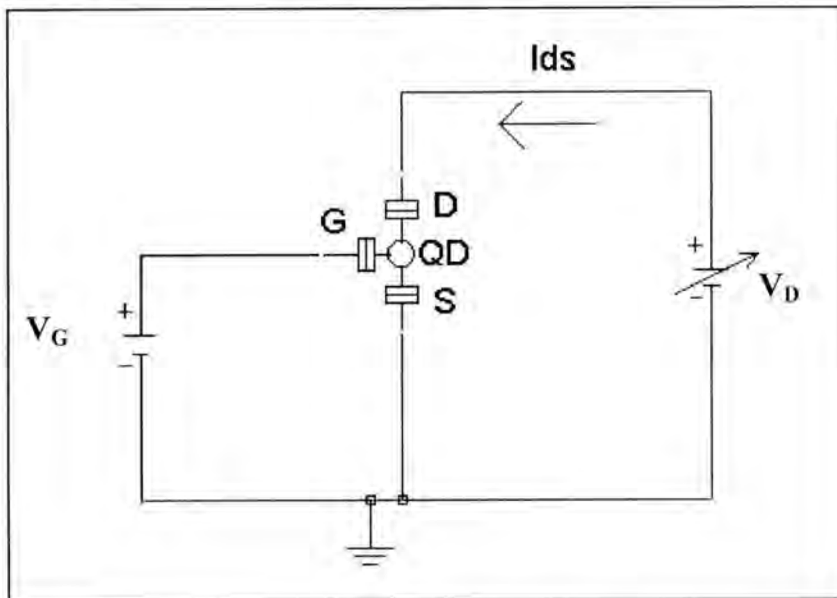

Fig. 2.11: A circuit setup for stability plot

Fig. 2.11 shows a typical circuit setup for stability plot. As shown in Fig. 2.12, the gate voltage is fixed at some level and the drain-source voltage is swept from one direction to the other. One can observe three distinct regions of operation. Internal shaded region, where the electron tunneling is suppressed by the Coulomb blockade is surrounded by the regions where tunneling is allowed. This region pattern doesn't repeat. Once the transistor is out of the stable region in either side, if the bias voltage continues to move in the same direction, it will never get another stable region.

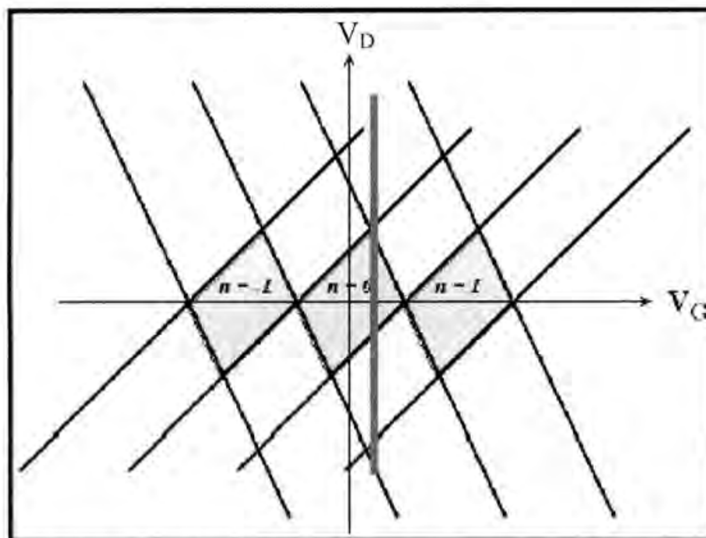

Fig. 2.12: Stability plot. V_D (connected to drain electrode) is being swept while gate bias is kept constant

Thus at this condition the transistor has only one stable region (OFF state) which is bounded by two unstable regions (ON state). The resulting current voltage characteristic is shown in Fig. 2.13.

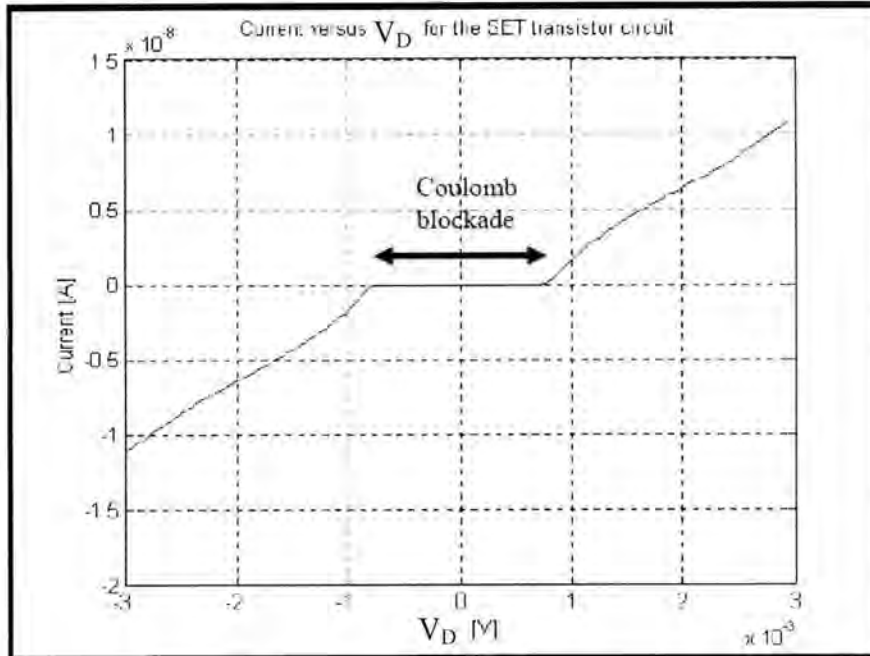

Fig. 2.13: I_D vs V_D characteristics for a fixed gate bias. Two unstable (tunneling allowed) and stable (tunneling blocked) region are obvious.

<u>Condition 2:</u> Drain bias fixed, Gate voltage swept.

Similarly, if we can now setup the circuit as shown in Fig. 2.14, where the drain bias is fixed and the gate bias is being swept.
This condition is much more interesting than the earlier condition. It is clearly seen from Fig. 2.15 that sweeping the gate potential from left to right while keeping the V_D fixed, traverses the transistor into alternating stable (OFF state) and unstable regions (ON state) of operation repeatedly. This condition gives a clear idea, how the changing potential at gate electrode creates OFF and ON states alternatively. Also it shows that, the V_D potential must be leveled to a certain value so as to ensure the successive ON-OFF regions of operations. If V_D is kept at zero level, the transistor will always remain in stable (OFF) condition. This happens as it enters a diamond immediately after coming out of another diamond-ensuring guaranteed OFF state. On the other hand if V_D is leveled too high so as not to intersect any shaded diamond, it keeps the transistor in permanent ON state. By carefully choosing V_D one can get alternative ON and OFF state by sweeping V_G. Such a level of V_D is illustrated in the Fig. 2.15.

As the gate voltage moves, the transistor experiences successive stable and unstable regions. This results, oscillating drain to source current. The result is shown in Fig. 2.16 depicting successive current peaks and valleys.

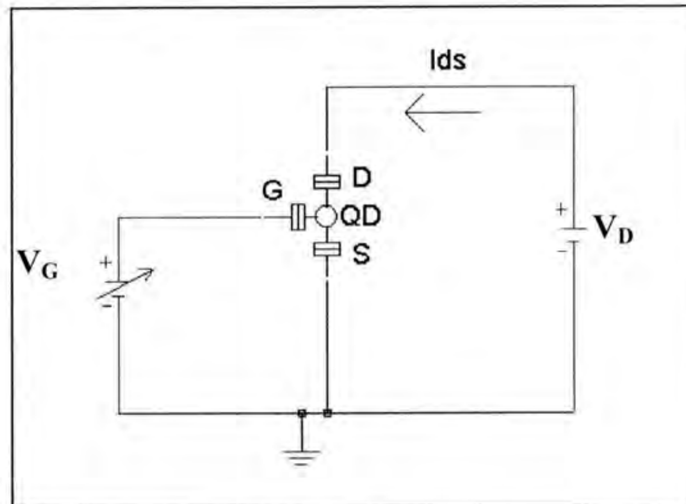

Fig. 2.14: Modified circuit setup for stability plot

Stability plot (also called stability diagram) gives a clear insight of the region of operation as well as better understanding of the I-V characteristics of the SET. By selecting biasing voltages the desired region of operation of the SET can be chosen which will deliver predicted current voltage characteristics.

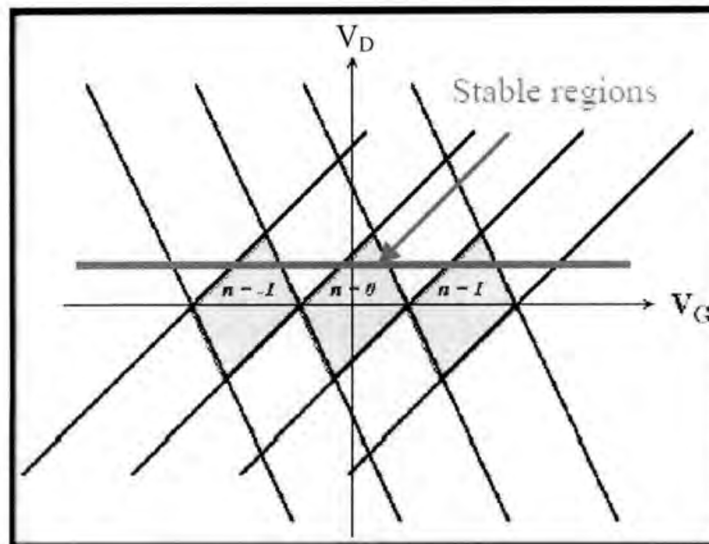

Fig. 2.15: Sweeping V_G while V_D is kept constant. The transistor undergoes repetitive stable and unstable regions resulting oscillation drain current.

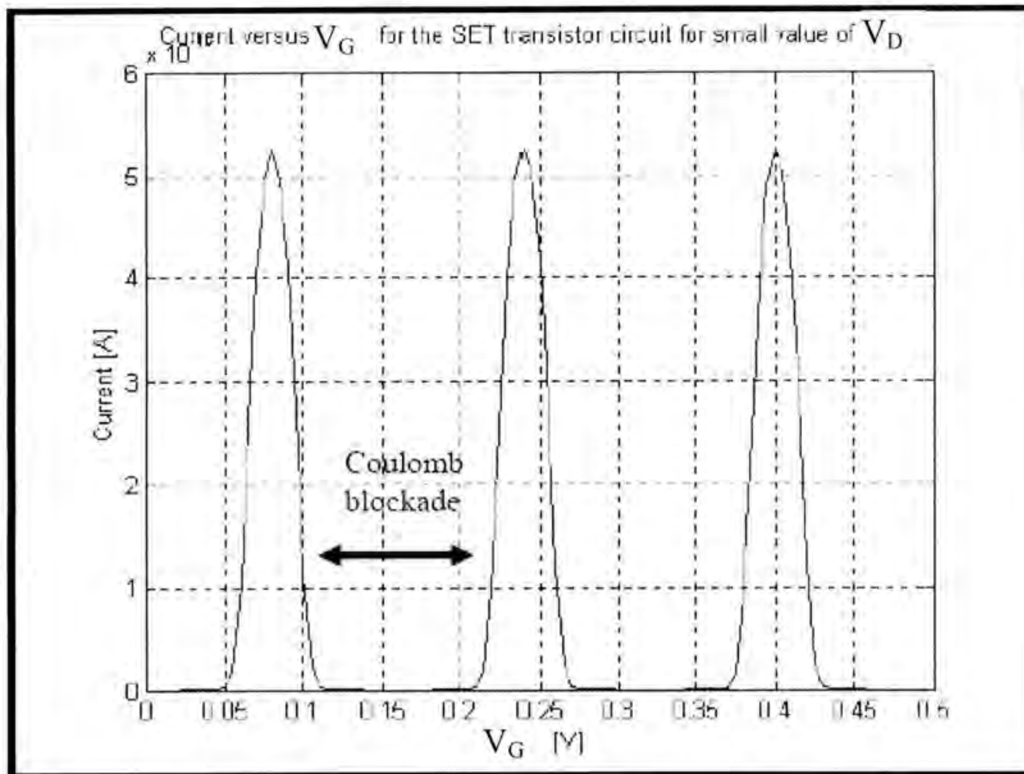

Fig. 2.16: I-V characteristics of SET. Coulomb oscillation with successive peaks and valleys resulting from the repetitive traversing of the transistor through unstable and stable regions

2.5 SET Fabrication Technique

SET, being a novel device, still has major fabrication challenges. The ultra small quantum dot island requires tremendously expensive and accurate fabrication facility. Basic limitation comes even from the operation itself. To be able to observe Coulomb oscillations, the charge addition energy should be much larger than the thermal energy k_BT. Otherwise, thermal fluctuation effect dominates and the Coulomb oscillation will disappear. This can be expressed through the relationship stated $e^2/C >> k_BT$. This is a fundamental barrier of SET operation. Either the capacitance of the total system has to be small enough so that the Coulomb blockade energy is larger than the thermal energy or the operating condition has to be cryogenic. For a typical example at room temp (T=300K) the capacitance has to be ~ 3aF with an island diameter less than 50nm.

Scientists are in constant pursuit of fabricating SET that is able to operate at room temperature. Fig. 2.5 shows an atomic force microscopy image of a fabricated SET. This fabricated SET is demonstrated to operate at room temperature.

An artificial pattern formation method based on the scanning tunneling microscope (STM) which avoids the control problems in self- organized structures.[35]. Using this

technique, a group of scientist have succeeded in fabricating an SET. The SET operates at room temperature, showing a clear Coulomb staircase with a ~150 mV period at 300 K. [30]

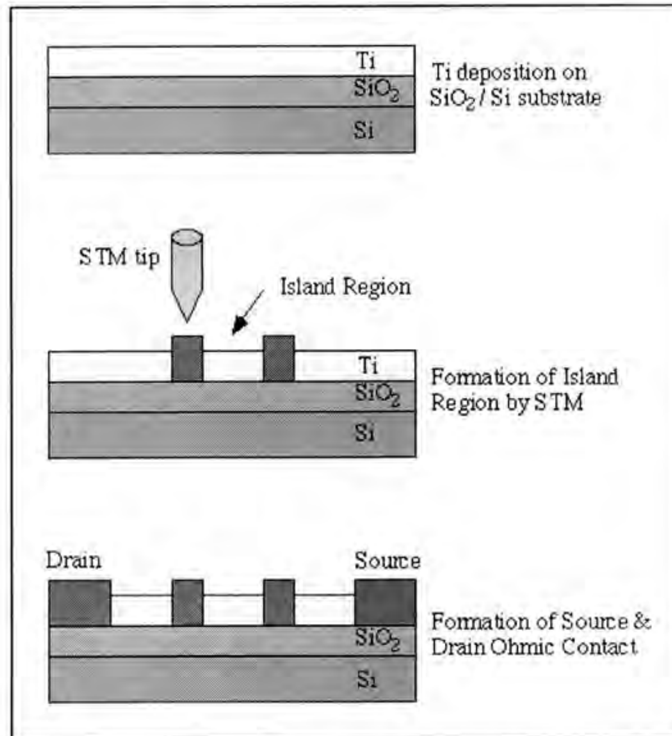

Fig. 2.17: Fabrication of the Ti/TiOx SET by the STM nano-oxidation process [36].

A description of the STM nano-oxidation process is shown in Fig. 2.17. A 3 nm thin titanium (Ti) metal film is deposited on a 100 nm thermally oxidized SiO_2/n-Si substrate. The Ti surface was oxidized by anodization through the water adhered to the surface of the Ti from the atmosphere, using the STM tip as a cathode, forming nanometer size Ti oxide (TiOx) lines. The barrier height of the TiOx/Ti junction has been found to be 285 meV for the electron from the temperature dependence of the current. The relative permittivity of the TiOx has been determined as e_r = 24 from the electric field dependence of the TiOx barrier height.[36]

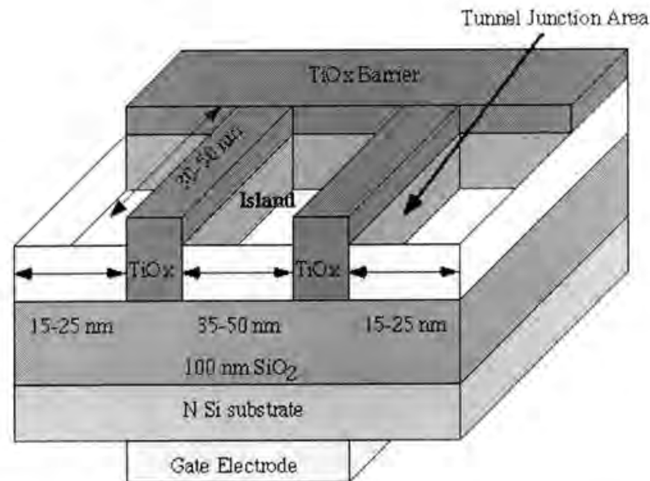

Fig. 2.18: Schematic of a single electron transistor [36]

A schematic illustration of the SET made by the STM nano- oxidation process is shown in Fig. 2.18. At both ends of the 3 nm thick Ti layer the source and drain ohmic contacts are formed, and on the back side of the n-Si substrate, the gate ohmic contact is formed. At the center region of the Ti layer, formed the island region, surrounded by two parallel, narrow TiOx lines, that serve as tunneling junctions for the SET, and two large TiOx barrier regions. Fig. 2.5 is an atomic force microscopy (AFM) image of the island region of a fabricated SET.

Typical sizes of the TiOx lines are 15-25 nm widths and 30-50 nm lengths. Typical island sizes are 30-50 nm by 35-50 nm. The most important feature of this structure is the small tunnel junction. The junction area corresponds to the cross section of the TiOx line, and is as small as 2-3 nm (the thickness of the Ti layer) by 30-50 nm (the length of the TiOx line). The deposited Ti layer is as thin as 3 nm, and the surface of the Ti layer is naturally oxidized to a depth of ~1 nm. Thus, the intrinsic Ti layer thickness is considered to be less than 3 nm. Owing to this small tunneling junction area, the tunnel capacitance becomes as small as 10^{-19} F, which allows the SET to be operated at room temperature.

The drain current-voltage characteristics of the SET were measured at room temperature and are shown in Fig. 2.19. The gate bias was set to 2 V. In Fig. 2.19, the solid line shows the current of the SET, and the dashed line shows the conductance of the SET. Between the drain bias of 0 V and -0.75 V, four clear Coulomb staircases with a 150 mV period are observed. The conductance oscillates with the increase of the drain bias with almost the same 150 mV period. The lower peaks of the conductance oscillation correspond to the flat regions of the current of the Coulomb staircase.

The Coulomb staircase shown in Fig. 2.19 may be attributed to the asymmetrical structure of the two tunneling junctions. One TiOx tunneling junction has a width of 18 nm, while the other junction is 27 nm wide. Due to this difference in junction widths, each tunneling junction has different values of conductance and capacitance, which produces the Coulomb staircase.

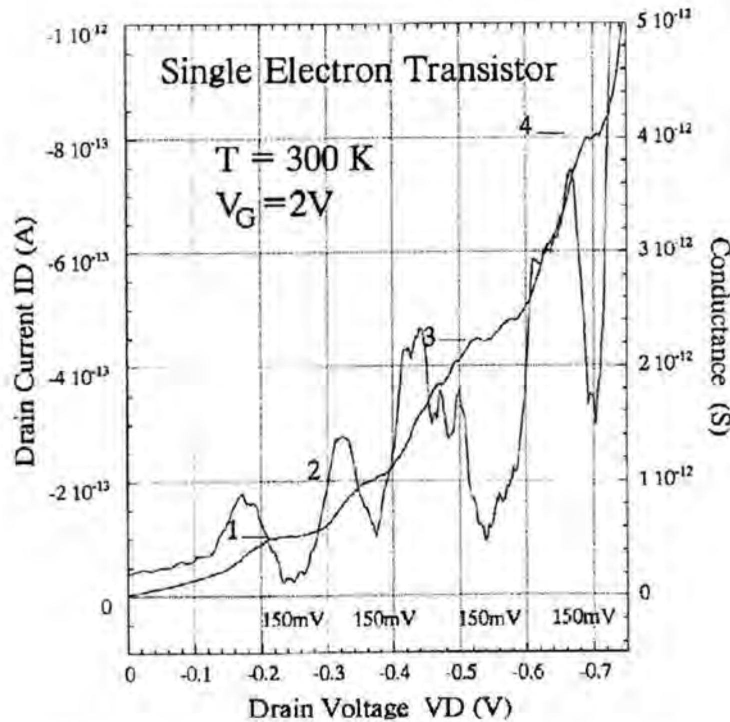

Fig. 2.19. Drain current v. drain voltage characteristics of the SET at 300 K [36]

The height of the Coulomb steps becomes larger with larger drain bias. This may be attributed to the increase of the tunneling probability of the electron through the TiOx tunneling barrier. The Fowler-Nordheim tunneling current increases as the applied drain bias lowers the height of the TiOx tunneling barrier.

The drain current v. gate bias characteristics with 150 mV drain bias at room temperature exhibit clear current oscillations with a period of ~460 mV, implying a periodic Coulomb oscillation of the current. The tunneling capacitance (C_t) and gate capacitance (C_g) could be roughly estimated from the period of the Coulomb staircase and oscillation. Their values were found to be C_t = ~3.6 x 10^{-19} F and C_g = ~3.5 x 10^{-19} F. These estimated values of the capacitances coincide well with the calculated capacitances from the SET's structural parameters. These results confirm the existence of Coulomb blockade phenomena at room temperature, and are due to the small dimensions of the SET island formed by the STM nano-oxidation process.

The fabricated SET shows a Coulomb staircase with periods of 150 mV at a temperature of 300 K. The Coulomb gap and staircase observed at high temperatures are attributed to the small tunneling junction area made by the STM nano- oxidation process. The fabrication process is quite easy and could be applicable to many kinds of devices.

Besides the AFM nano-oxidation process there are several other existing processes. A group of scientists from the University of Manchester has reported that they have

manufactured a single electron transistor out of graphene sheet [37]. These researchers have used the world's thinnest material to create the world's smallest transistor – a breakthrough that could spark the development of a new type of super-fast computer chip. Graphene is a single planar sheet of sp2 – bonded carbon atoms that are densely packed in a honeycomb crystal lattice – shown in Fig. 2.20. The carbon-carbon bond length in graphene is approximately 1.42 angstrom. This sheet is only one-atom thick. The research team suggests that future electronic circuits can be carved out of a single graphene sheet. Such circuits would include the central element or 'quantum dot', semitransparent barriers to control movements of individual electrons, interconnects and logic gates – all made entirely of grapheme as can be seen in Fig. 2.21.

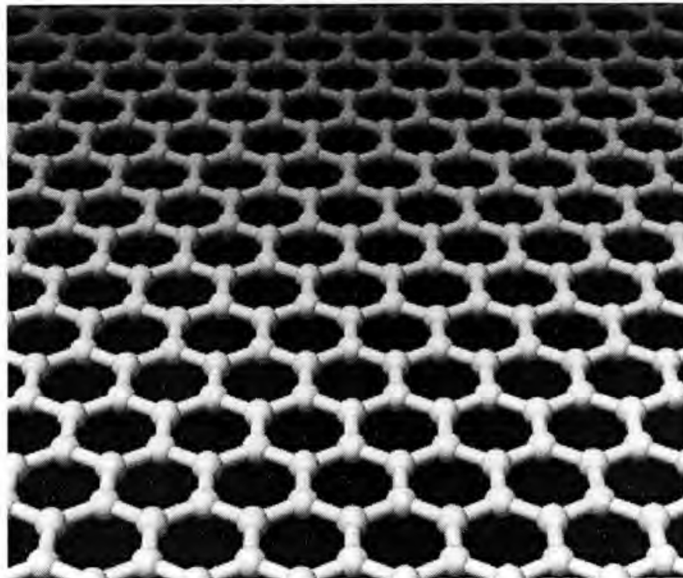

Fig. 2.20: Graphene sheet. Graphene is an atomic scale chicken wire made of carbon atoms. [37]

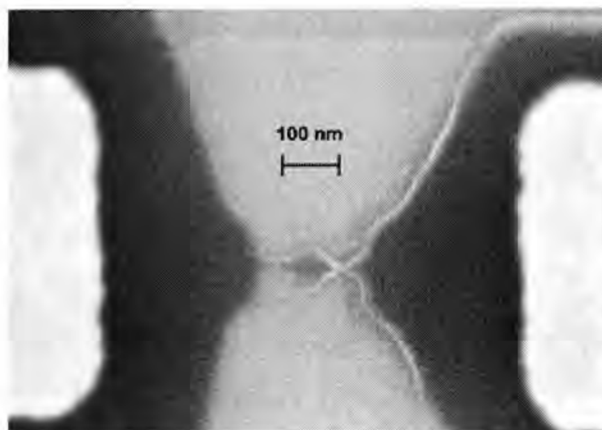

Fig. 2.21: Single-electron transistors carved entirely in a graphene sheet. The central elements are so-called quantum dots allowing electrons to flow one by one. The dots are connected to wider regions (contact pads by nm-wide constrictions) that work as tunnel barriers. [37]

CHAPTER 3
Rate Controlled Oscillator

3.1 Introduction

In this chapter a proposal to use SET (Single Electron Transistor) in a rate controlled oscillator (RCO) circuit will be discussed in detail. The concept of a voltage controlled oscillator is common in which the frequency of a system is the function of the input voltage level of the system. The VCO plays a vital role in stabilizing the PLL and many other system level applications. While VCO is a known concept and application, the proposed rate controlled oscillator (RCO) is a unique and new idea. This section will describe the operation of the system which uses the SET in a RCO, i.e. the output frequency of the proposed system will be a function of the rate of change of the input voltage signal. Unlike VCO, the output frequency of the RCO doesn't depend on the signal level but on the rate (dv/dt) of the signal level.

3.2 Coulomb Oscillation

The name "Single Electron Transistor" comes from the observation that the transistor turns on and off again every time a single electron is added to it. For current to flow the number of electrons on the droplet must fluctuate, say between N and $N+1$. Thus the Nth peak in the conductance occurs when the state of the droplet containing N electrons is in equilibrium with the state containing $N+1$ electron. This will occur when the electrostatic potential of N+1 electron will be equal to the sum of energy contribution of gate voltage and previously occupied energy of N electrons.
Therefore, a conductance peak occurs when

$$eV_G(N) = E(N+1) - E(N) \quad (3.1)$$

where $E(N)$ is the total energy of the droplet with N electrons. Equating we get

$$V_G(N) = e(N+1/2)/C \quad (3.2)$$

And change in gate voltage for adding one electron is

$$\Delta V_G = e / C \quad (3.4)$$

Also equivalent energy gap (coulomb gap voltage)

$$\Delta E = e^2 / C \quad (3.4)$$

To add a charge Q to the particle requires energy $Q^2/2C$, where C is the total capacitance between the particle and the rest of the system. Setting $Q = -Ne$ in Eqn. 3.1 gives values of the peak positions that are equally spaced in gate voltage with separation $\Delta V_G = e/C_G$ where C_G is the drain to island capacitance. This result is a direct consequence of the charge quantization. Taking $E(Q) = Q^2/2C$ means that the energy as a function of Q is a parabola with minimum at Q_0. Were not the charge quantized, by varying Vg we can choose any value of Q_0, the charge that would minimize the energy,. However, because the real charge *is* quantized, only discrete values of the energy E are possible. When $Q_0 = -Ne$, for which an integer number N of electrons minimizes E, the Coulomb interaction

results in an energy difference $U = e^2/2C$ for increasing or decreasing N by one. There is thus an energy gap that suppresses charge fluctuations. For all values of Q_0 except $Q_0 = -(N + 1/2)e$ there is a smaller, but non-zero, energy gap for adding or subtracting an electron. Under these circumstances no current can flow at temperature $T = 0$.
However, when $Q_0 = -(N + 1/2)e$, the state with $Q = -Ne$ and that with $Q = -(N + 1)e$ are degenerate; the charge fluctuates between the two values even at zero temperature. Consequently, the energy gap disappears and current can flow. The peaks in conductance are, therefore, periodic, occurring whenever the average charge on the quantum dot island is $Q_0 = -(N + 1/2)e$. This is illustrated in Fig. 3.1

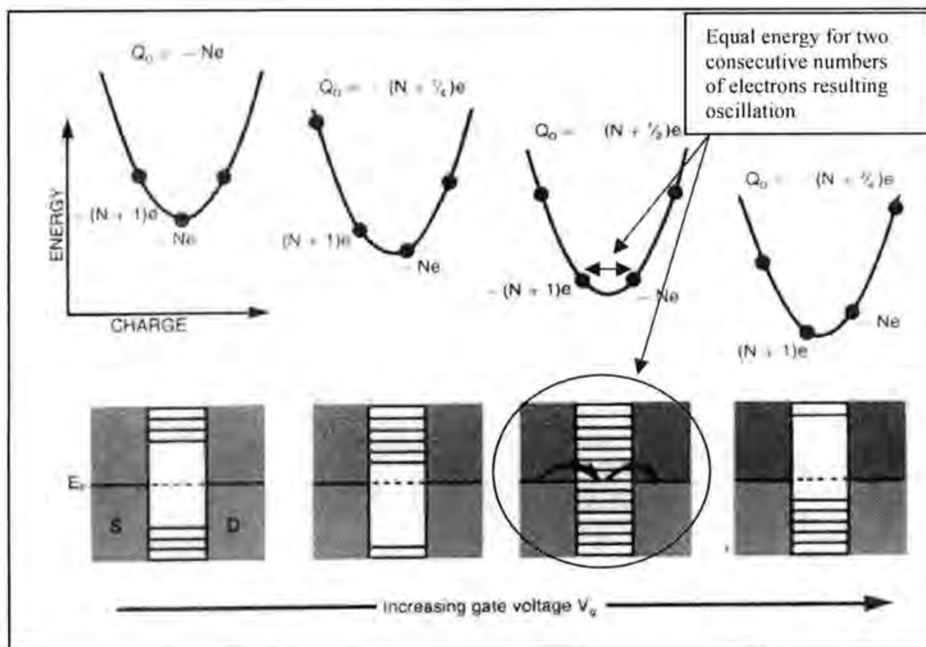

Fig. 3.1: Increasing the gate voltage is equivalent to adding electron to the quantum dot, which modulates the total accumulated energy associated with the island. Tunneling is allowed only when the amount of gate voltage is such that two consecutive numbers of electron result in same energy value (third condition, marked with circle)

To summarize, the conductance of the SET is periodic with the gate voltage and consecutive conductance peaks appear at a distance of $\Delta V_G = e/C$.

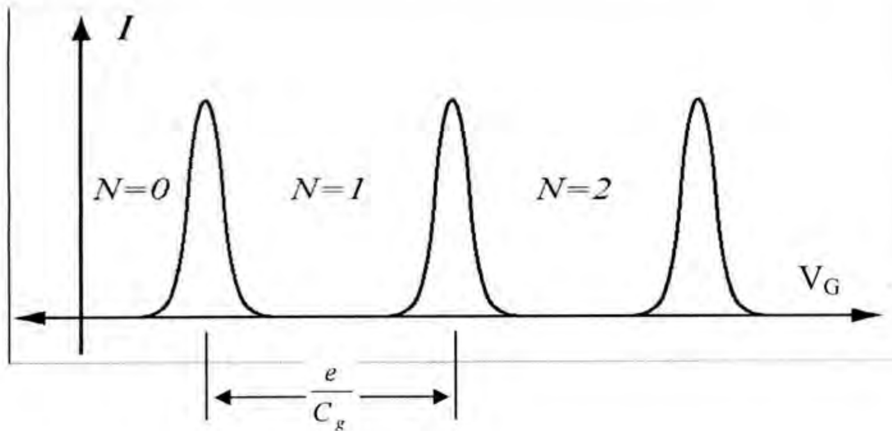

Fig. 3.2: Conductance peak as a function of gate voltage.

Fig. 3.2 can also be viewed as the following Fig. 3.3, where the conductance peak is plotted as a function of the numbers of electron in the quantum dot.

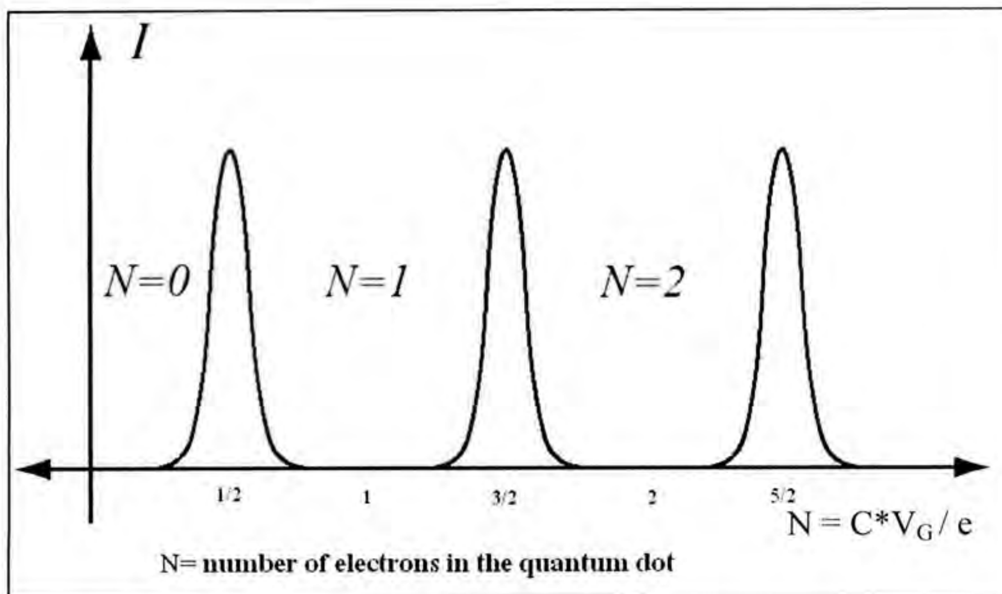

Fig. 3.3: Conductance peak as a function of the numbers of electrons in the quantum dot.

3.3 RCO: Circuit Setup, Stimuli and Theory of Operation

Let us consider a circuit consisting of the SET and a set of stimuli. As seen in Fig. 3.4, the SET is biased with V_{DRAIN} connected at drain electrode and the gate is connected to a variable voltage source V_{GATE}.

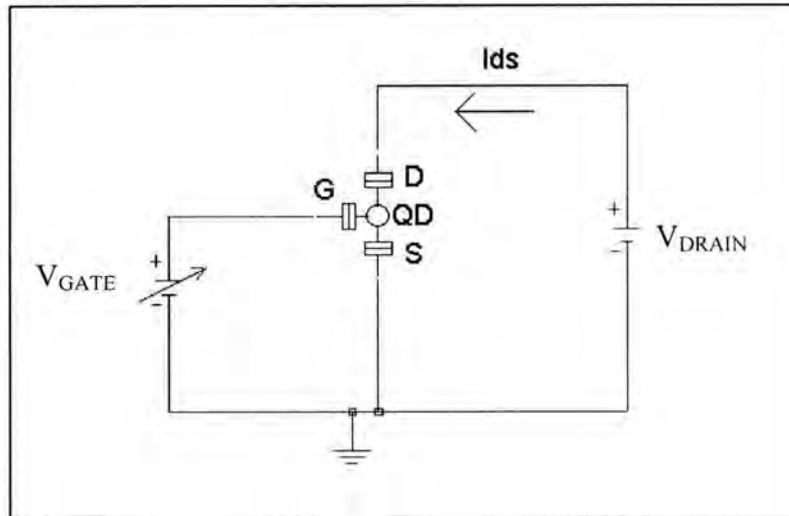

Fig. 3.4 Basic Schematic setup of SET as the core of a rate controlled oscillator with gate and drain bias

The V_{DRAIN} is setup to such level to ensure that the V_{GATE} is swept such that the transistor passes through ON and OFF states repetitively.
From the concept of coulomb oscillation we know that each change in $\Delta V_G = e/C$ at gate voltage will cause the transistor to switch between successive conductance peak.
Let us consider following three cases, where the gate voltage is swept at different dv/dt rate.

Condition 1: lowest dv/dt

Let us consider Fig. 3.5. the gate voltage is changing with respect to time at such a rate that at each $\Delta T1$ sec it traverses ΔV_G (= e / C) amount voltage. In this case, since every ΔV_G = e / C amount is associated with a conductance peak, it is expected to get a periodic current at drain with peaks appearing at an interval of $\Delta T1$.

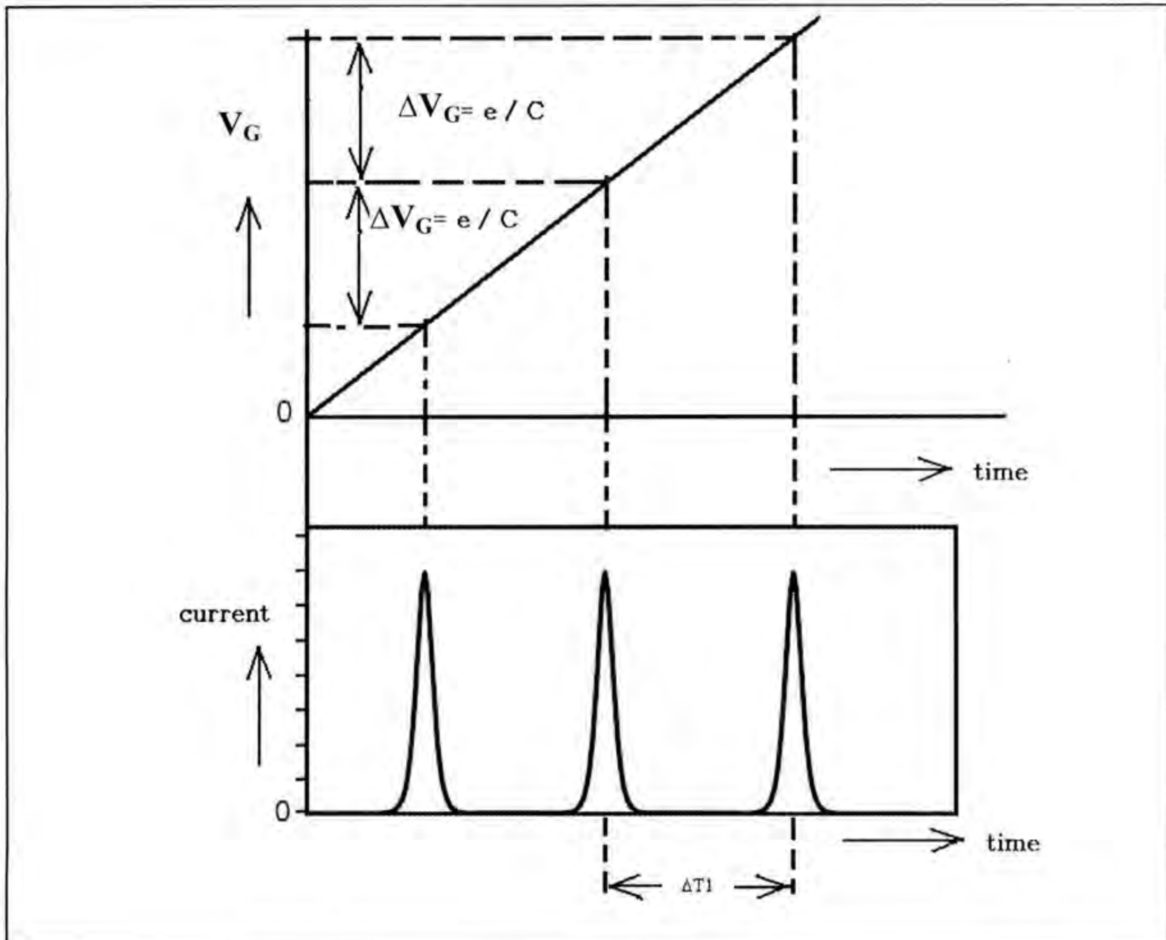

Fig. 3.5: Gate voltage changing at a rate of ΔV_G (= e / C) in $\Delta T1$ sec.

Condition 2: Medium dv/dt

In this case the dv/dt of the gate voltage is increased. The following Fig. 3.6 shows the change in the slope of the gate voltage and the consequence in the conductance peaks.

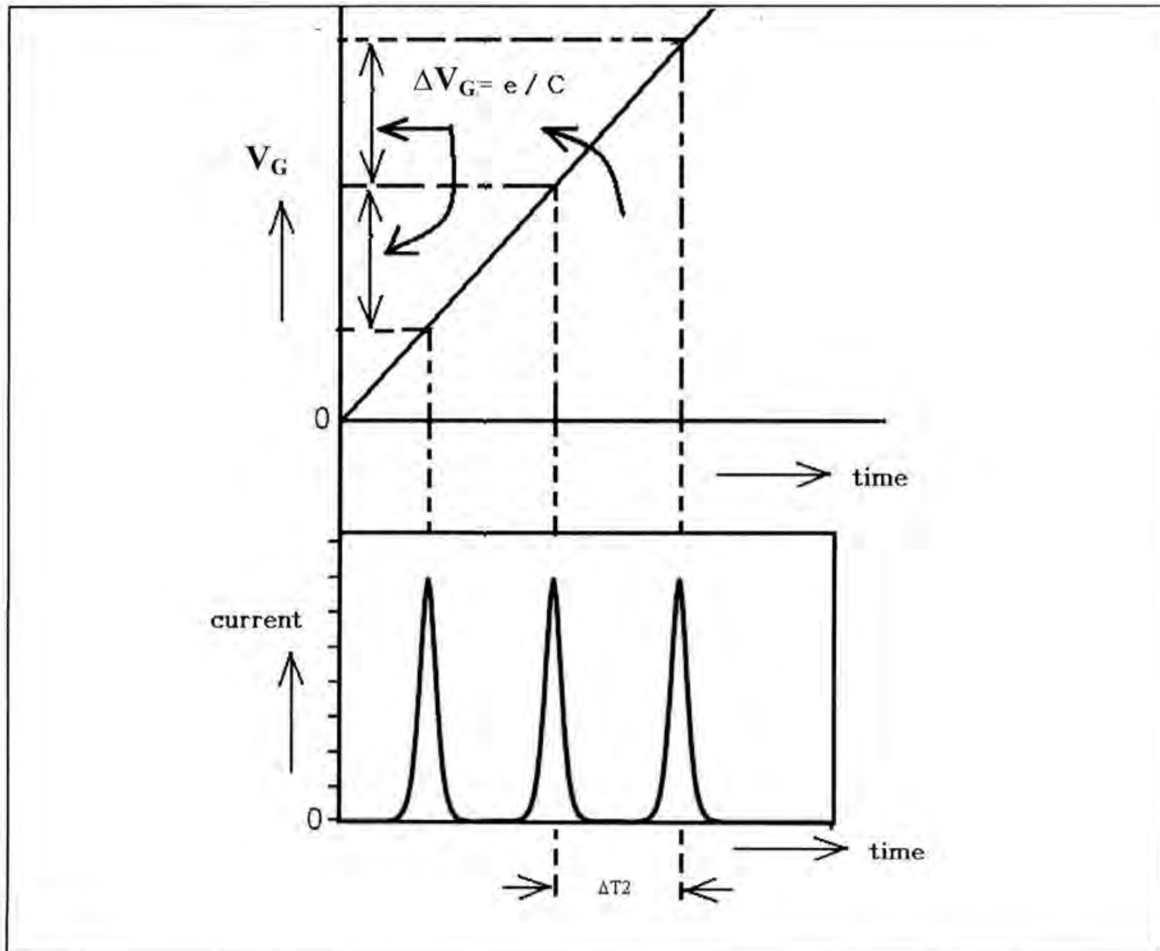

Fig. 3.6: The rate of change of gate voltage is increased. Gate voltage is now changing at a rate of ΔV_G (= e / C) in $\Delta T2$ sec. note that $\Delta T2 < \Delta T1$

Condition 3: Highest dv/dt

In the last condition, we change the gate voltage in such a manner that it shows a dv/dt which is highest among these three conditions. Fig. 3.7 shows the details of the dv/dt and the change in the period of conductance peaks.

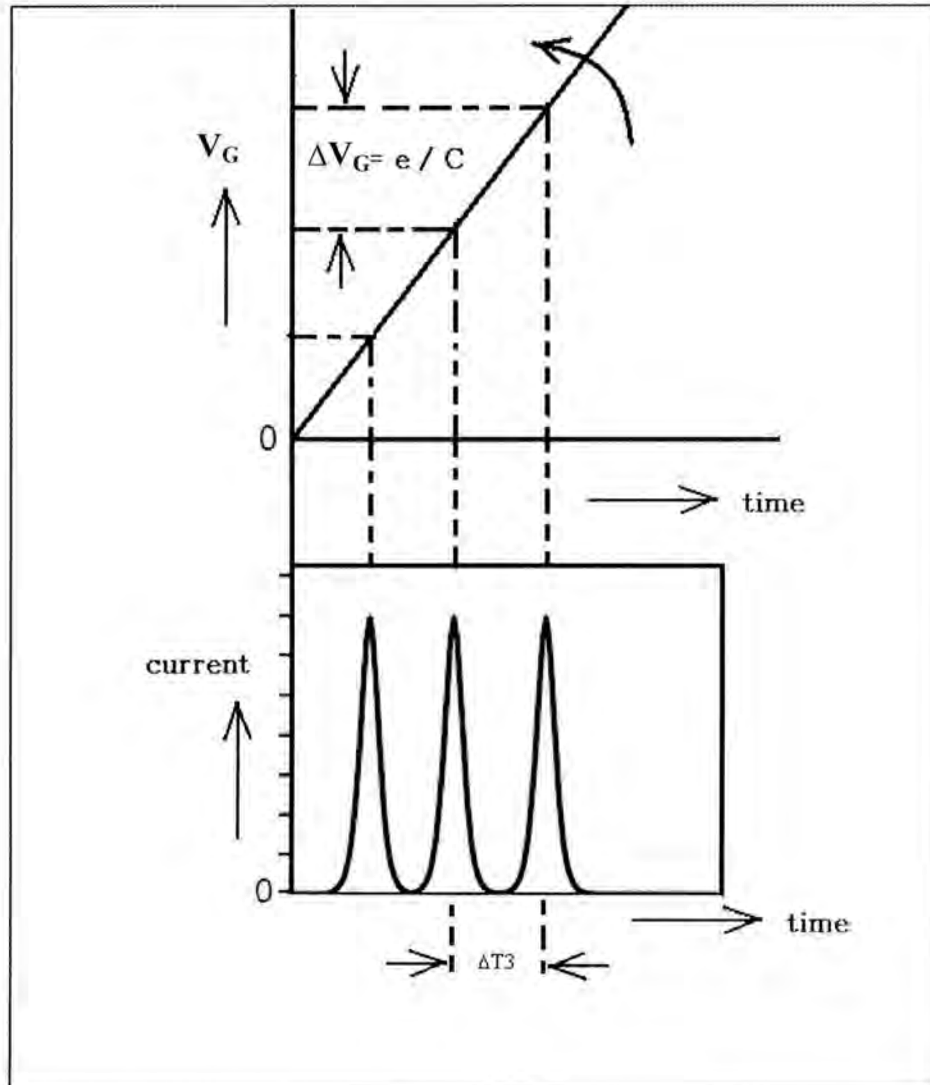

Fig. 3.7: The rate of change of gate voltage is further increased. Gate voltage is now changing at a rate of ΔV_G (= e / C) in $\Delta T3$ sec. obviously $\Delta T3 < \Delta T2 < \Delta T1$

What we see from the above three conditions simply establishes the relationship of the period of conductance peak and the slope of the gate input signal of the SET. As the slope of the input signal increases from condition 1 to condition 2, the period of oscillating current decreases from $\Delta T1$ to $\Delta T2$. Further increase of the slope from condition 2 to condition 3 produces a similar decrement in oscillation period. It is given that the slope at condition 3 is highest among all and the period of oscillation found is the lowest. So it is

evident that the higher the slope the lower the period. This relationship can be equated as following equation,

$1 / T_{period} \propto S_{gate}$ (3.5)

Where S_{gate} is the slope of the gate signal and T_{period} is the period of conductance oscillation

Since frequency is inverse of the time period, the equation takes the following format,

$f_{osc} = k.\ S_{gate}$ (3.6)

Where k is an arbitrary constant and f_{osc} is the frequency of oscillation at the output node.

This equation expresses the phenomenon that the SET is an inherent slope to frequency converter. When a continuously changing signal is applied to the gate electrode of the SET, the drain-source register an oscillating current with a frequency of oscillation proportional to the slope of the input signal.

Rate Control Oscillator circuit:

We have discussed how the SET converts the slope into frequency through coulomb oscillation. Fig. 3.8 shows a complete circuit which would generate a series of digital pulses whose frequency is variable and is a function of the slope of the input signal.

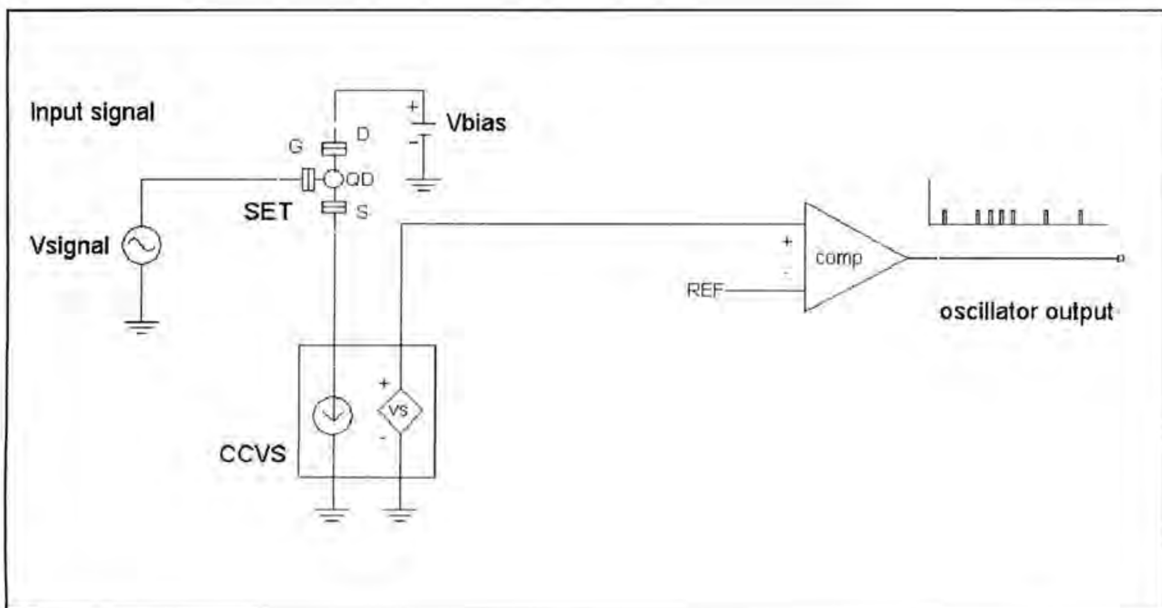

Fig. 3.8: Rate Controlled Oscillator Circuit using SET

The circuit is simple in configuration regarding the number of components and complexity of connection. The first section is simply a properly biased SET device. The input of the rate controlled oscillator (RCO) is the gate node of the single electron transistor (SET). As the signal changes in the input the energy level of the SET moves back and forth allowing the electrons to tunnel one moment and blocking them on the

next. Thus the SET registers a drain to source current which is oscillatory in behavior. The frequency of the oscillation is directly proportional to the value of the slope of the input signal.

The current that flows from drain to source in a SET is very small in magnitude (usually in the nano-ampere range). It is very difficult to use this small magnitude of current in manipulating other variable if not amplified. An effective amplification mechanism is current controlled current source (CCCS) which effectively amplifies current. The amplification may vary depending on circuit implementation and requirement. Usually 10x-100x magnification is used in integrated circuit blocks. A CCCS of 100x amplification would serve the purpose in a typical RCO circuit. When the current is amplified is it converted into voltage by simple resistive mechanism. Effectively, if we look from the input to output of this block – we give a small current as input and getting large voltage signal which is in phase with the input current. This is what is meant by the current controlled voltage source (CCVS) in Fig. 3.8.

After the oscillatory current is amplified and effectively converted into voltage, next the voltage is fed to the positive input of a high speed comparator. The negative input is connected to a preset reference voltage which is roughly the mid range value of the amplified output of the CCVS. Now at the output of the comparator we get a digital pulse whose frequency is proportional to the slope of the input signal applied to the gate electrode of the SET.

The duty cycle of the output pulse can be adjusted by just moving the reference voltage up and down. The value of the output pulses can be changed easily with the bias voltage of the comparator. The overall circuit delay is the delay produced by all three stages – the SET device, the CCVS block and the output comparator block.

3.4 Possible Application of RCO

Some of the future application of single electron transistor based rate controlled oscillator may be in automobile accelerometer, automobile safety and collision sensor, cyclone monitoring system, wind power generator controller, power system glitch monitor/protector, *g*-monitoring in fighter aircraft and elevator braking system.

A wide range of micro electronic circuits are expected to use this RCO. In systems where signals with unpredictable frequency are expected, dv/dt controller circuits which protect many important other circuit, systems that works with wide band of frequencies are major areas where the RCO circuit will play very important role.

CHAPTER 4

Practical Implementation of SET based RCO: Adaptive Sample and Hold Circuit

4.1 Introduction

In the 21st century everything comes in digital format. Nevertheless, the world remains analog and it will remain so forever. This dilemma is solved by the analog to digital conversion – what is now a necessary part of our everyday issues. To extract information from analog signals for further processing, sample and hold circuits are used. These circuits are simple and easy yet it plays vital role because the resolution of the overall data conversion is practically limited by the design and the efficiency of the sampler.

4.2 Conventional Sampler Circuit

A conventional sample and hold circuit has two basic modes of operation. These are sample and hold. In a particular instance it opens a channel to sample the input signal and then shuts the switch off. The sampled value is stored in a capacitor and then is fed to VOUT until the next sampling instance arrives. At the next sampling point, the sample again allows the channel to store the input value which overwrites the previous data in the same capacitor and then hold again the latest value. A simple sample and hold (S/H) circuit may look like Fig. 4.1.

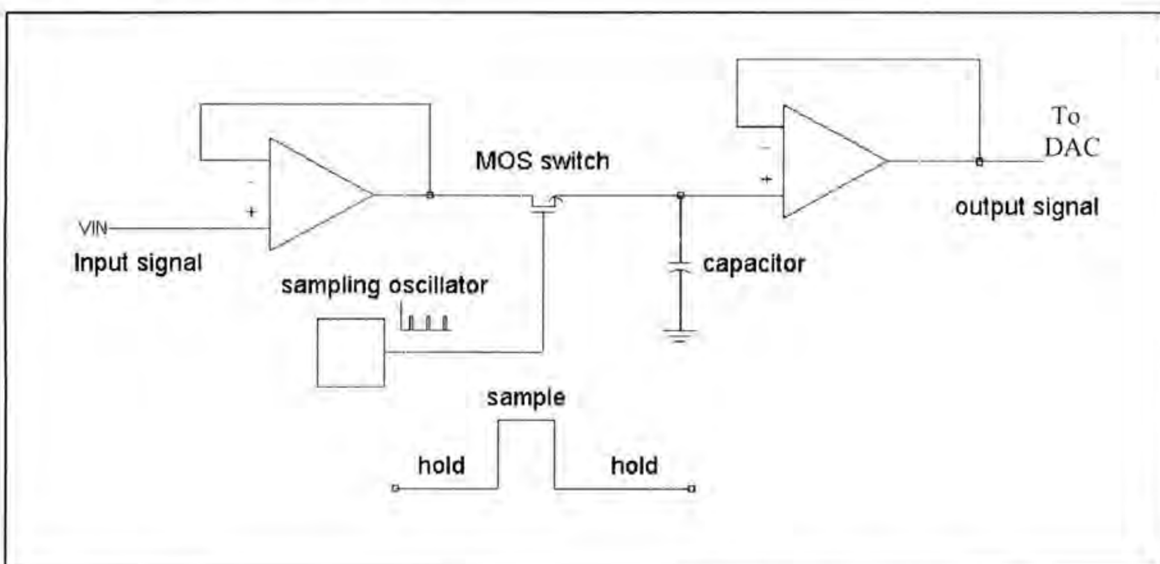

Fig. 4.1: A simple sample and hold circuit implemented with voltage followers.

Fig. 4.1 shows basic building blocks of a S/H circuit. Input signal is buffered through a input stage voltage follower which is then connected to an NMOS switch. The source side of the FET is connected to the capacitor. The output stage voltage follower is connected with the capacitor whose output is the sampled signal of the input. The sampling interval is defined by the time period of the sampling oscillator. The gate of the NMOS is switched between sample and hold mode by the output of the sampling oscillator. Fig. 4.2 shows the output of the sampler (at VOUT node) along with the input signal.

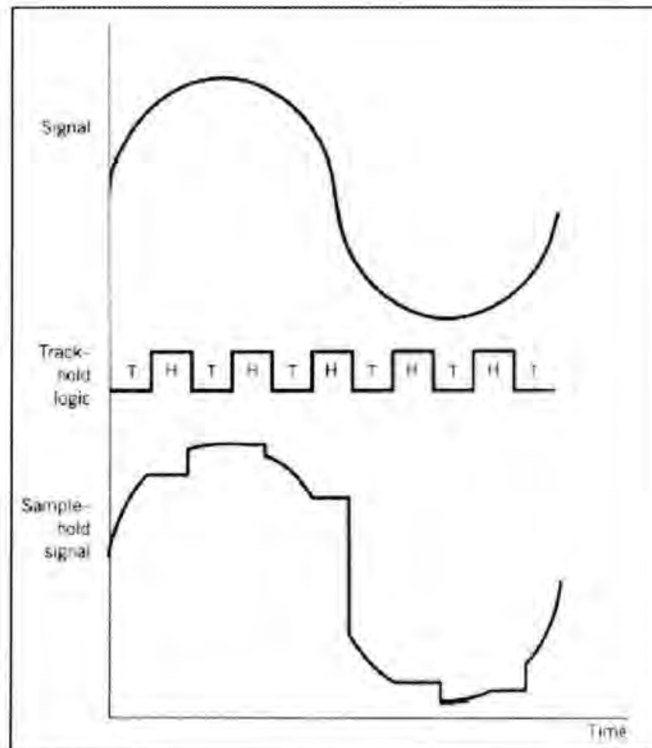

Fig. 4.2: Input (top) and output (bottom) of the sample and hold circuit. The sampling oscillator output is also shown as sample (track) and hold logic.

4.3 SET based RCO Implemented Adaptive Sampler

The efficiency of a sampler lies in how well is the sampling frequency selected. The sampling frequency must be large enough to meet Nyquest rate. At the same time it has to be as low as possible to minimize the numbers of sampling point. Since bit rate is directly proportional to the sampling point, minimizing sampling points ensure minimum bit rate.

In most cases, the incoming signal is composite in nature, that is, it is a mixture of signals of different frequencies. Usually the sampling rate is fixed at a rate more than twice of the maximum frequency present in the composite signal stream. It ensures the correct

sampling of the signal with maximum frequency and guaranties the enough room for the lower frequencies.

There is a major drawback of the system. The sampling frequency can not be less than the twice of the maximum frequency of the composite signal- otherwise it will lose information on the maximum frequency. Since the whole stream is sampled at a higher rate it guaranties no loss of information but at the same time the lower frequencies are over sampled. Over sampling means inefficient system - since we are allowing sampling points those are not required. Even when the signal is varying with lower frequency, the system is sampling it at a higher rate - thinking that there is a higher frequency present. This is causing higher bit streams which carries redundant information. This dilemma is the outcome of fixed sampling frequency.

Let's now imagine a system that allows us to sample the signal at a rate that is just required. It neither over samples nor under samples the signal. To do so, it has to be intelligent enough to vary its sampling frequency adaptively. It has to check the incoming signal, analyze its slope and the way it is currently varying and then decide at what frequency it should be sampled. That's precisely what the SET implemented adaptive sampler does.

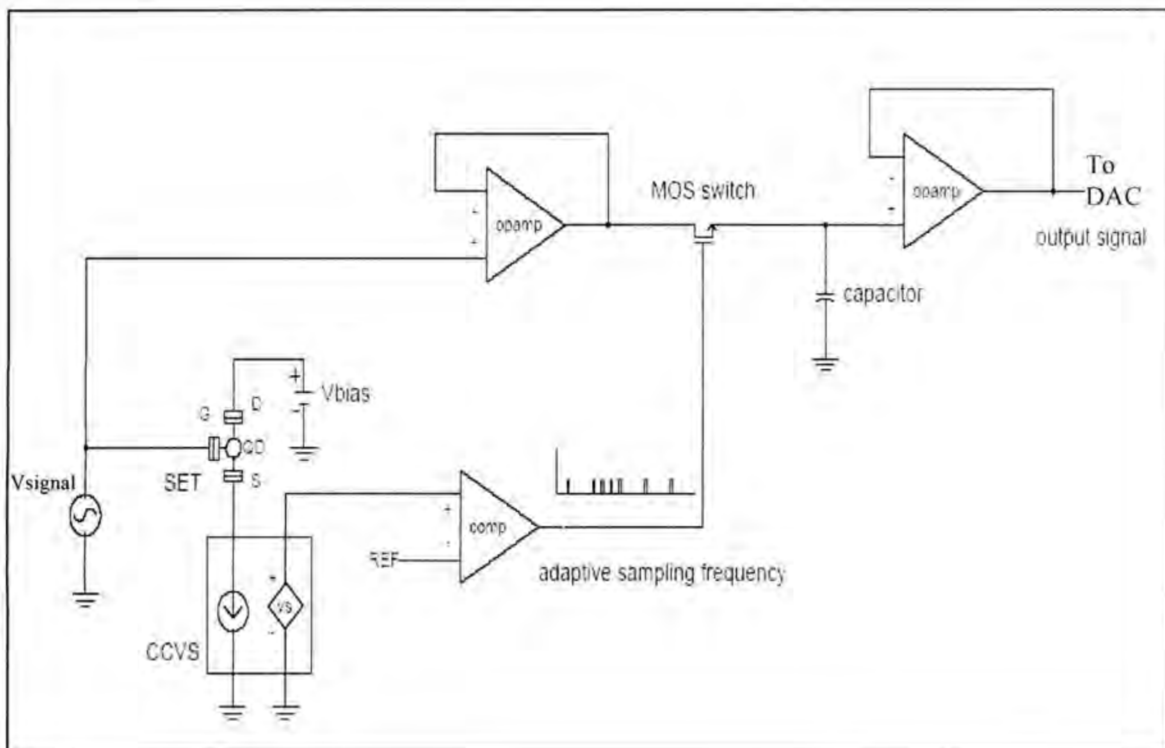

Fig. 4.3: SET based RCO implemented sample and hold circuit.

Fig. 4.3 shows a schematic view of a sample an hold circuit based on SET-RCO. As seen from the schematic, the input signal is fed to the gate electrode of the SET along with the input voltage follower stage. Every part of the circuit is similar to that of the conventional circuit presented in Fig. 4.1 except the sampling frequency generator section.

The input signal, that is applied to the gate of the SET forces the transistor to sweep back and forth among the ON and OFF states. In doing so, it produces an oscillating current through drain and source of the transistor. We have seen in the earlier section that the frequency of the oscillating current in SET is directly proportional to the absolute slope of the signal applied to the gate. So we get a current whose frequency is proportional to the slope of the input signal applied to the gate and the input voltage follower stage. This oscillation current in then passed through a current controlled voltage source (CCVS) which produce a pulsating voltage of varying frequency similar to that of the oscillating current. Now this pulsating voltage is compared with a reference voltage, amplified and then applied to the gate of the NMOS switch that controls the sampling of input signal. Now we have got a sampler whose frequency is no more blind rather it is continuously monitoring the input signal and adaptively changing. And this change is ensured in the right direction, that is when it registers higher slope the sampling frequency increasing (which is required, so that it doesn't miss any portion of the information) and when it finds a lower slope it decreases the sampling frequency (to avoid over sampling and to minimize numbers of bit to represent the signal stream). And thus we get an intelligent system which varies its sampling frequency in accordance to the demand as it decides from the slope.

4.4 Comparison

Having discussed the sampling method both by conventional fixed frequency sampling scheme and proposed adaptive frequency sampling scheme, it is now convenient to compare these schemes.

System with signal with unpredictable frequency:

Let's imagine a system where signals with unpredictable frequencies are expected. A seismic monitoring system is an ideal example. A seismograph keeps record of the p-wave and s-wave of the earthquake. A typical P-wave and S-wave is shown in Fig. 4.4.

An earthquake detection system has to continuously monitoring ground waves. But what would be the frequency of the earthquake? That is not predictable. It depends on the geographical point where the epicenter is located and the cause of the earthquake. However we cannot afford to miss any of the information. So we have to initially analyze maximum recorded frequencies of earthquakes and design the system to cover those frequency ranges with some margin. But thing might get worse as there is no limit to how intense the earthquake is. So theoretically we don't have a solution and then we have to practically design a system which will have enough margins to catch up several times

higher intensity than that of the recorded maximum. So we need to fix the sampling frequency to a much higher rate than typical so that it is able to read more intense magnitude of earthquakes.

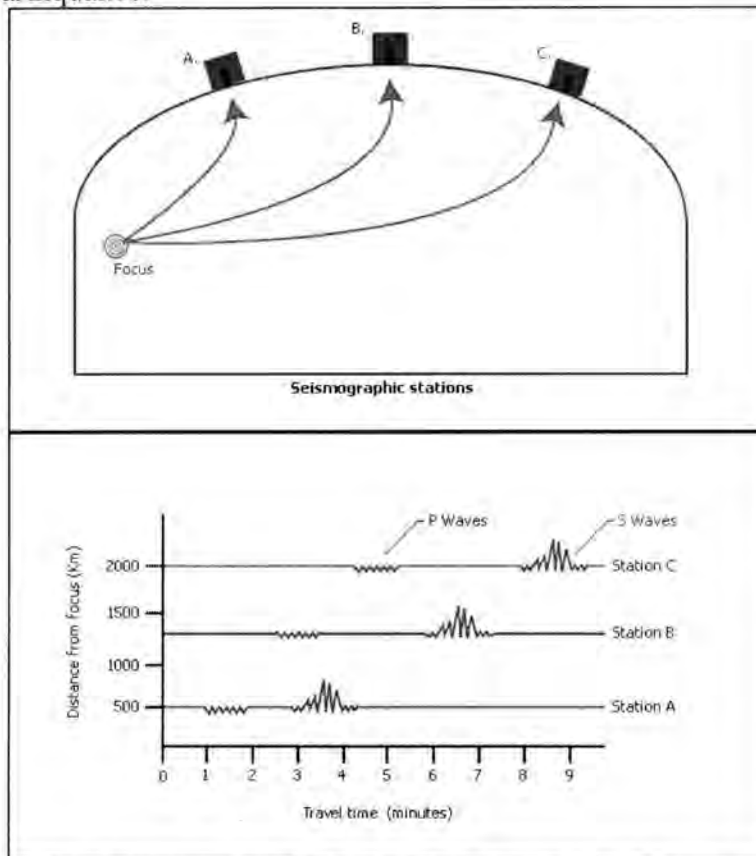

Fig. 4.4: (Top) Seismographic station location along with the earthquake focus point and (Bottom) P and S waves as recorded in three stations

As Fig. 4.4 depicts, the P wave and S wave are not continuous but occurs intermittently– a short burst of 4 ~ 5 minutes may be once in a month or once in a week or at most once in a day. Even in the most intense earthquakes, almost 99% of time the signal is of very low frequency. The summary is simple, we are over sampling the whole signal stream unnecessarily for more than 99% of time to record the vital 1% information. Which is in turn saying 99% of our data is unnecessary and we are consuming 99 times extra bandwidth.

Now, in the real world there exists numerous applications where systems are employed to monitor situation that might occur (like fault in power line, sudden radio signal receive from distant galaxies etc.). In these cases, it's not feasible to sample the complete incoming stream at a high rate so as not to miss anything nor it's wise to let go the high frequency component. In the first case we will be gathering too much redundant information and would require tremendous bandwidth unnecessarily thus making the whole setup inefficient. While in the later case there is a strong chance that we will be missing important parts of the information stream thus making the whole project a failure. The solution is to design a system that intelligently monitors the incoming signal

and decides based on the slope of the signal which frequency needs to be used. These cases are discussed here along with simulation results.

To simulate these kinds of situations, let us first consider a system where the input signal consists of both high and low frequency waves.

Condition 1: Let's think, the system is designed to sample correctly only the low frequency waves. The designers were unaware that there might be a high frequency component or this is first case where the system is registering a higher frequency signal component for the first time (may be, signals from some extra-terrestrial intelligence or some deep space pulsar). In any case, since the system was ready for low frequency waves it will simply overlook the higher frequency component as it has no adaptability. This case of sampling is shown in Fig. 4.5.

The reproduced signal from the sample and hold system in this case is shown in Fig. 4.6. As predicted, the reproduced signal is missing the information of the high frequency portion.

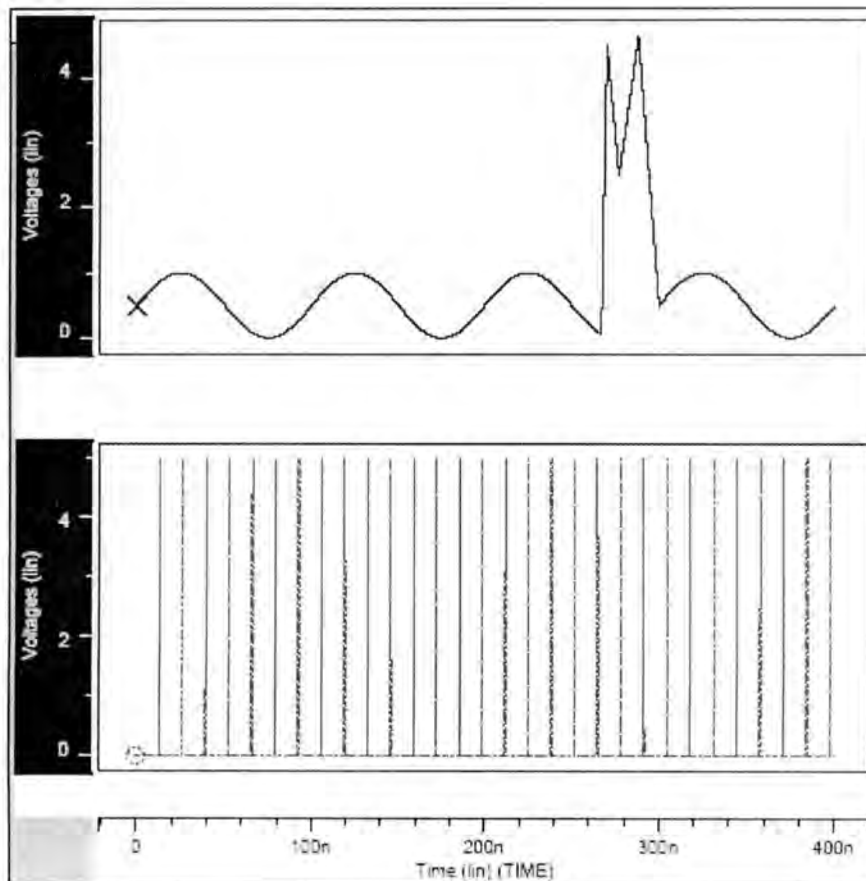

Fig. 4.5: Simulation of a system with composite frequency signal. The sampling frequency is selected erroneously based on the lower frequency. The low frequency portion is correctly sampled and the high frequency portion is under sampled.

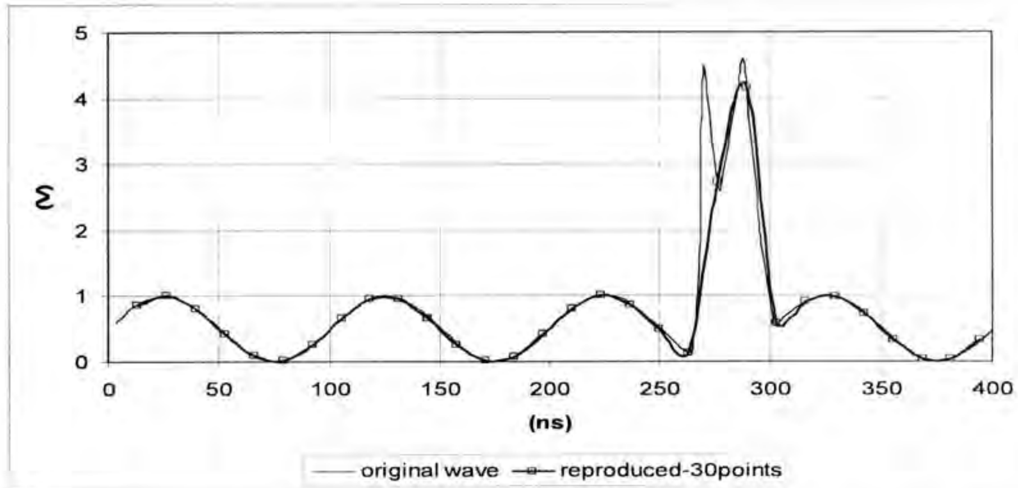

Fig. 4.6: Reproduced wave from conventional sample and hold circuit with 30 point sampling. The thin line is the original signal and the thick line represents the signal reproduce from 30 points under sampling.

As seen from Fig. 4.6, the high frequency portion is missing one of its peaks when reproduced. The whole information with the missing peak is lost forever and the system is obviously a failure. A closer look reveals further details in Fig. 4.7.

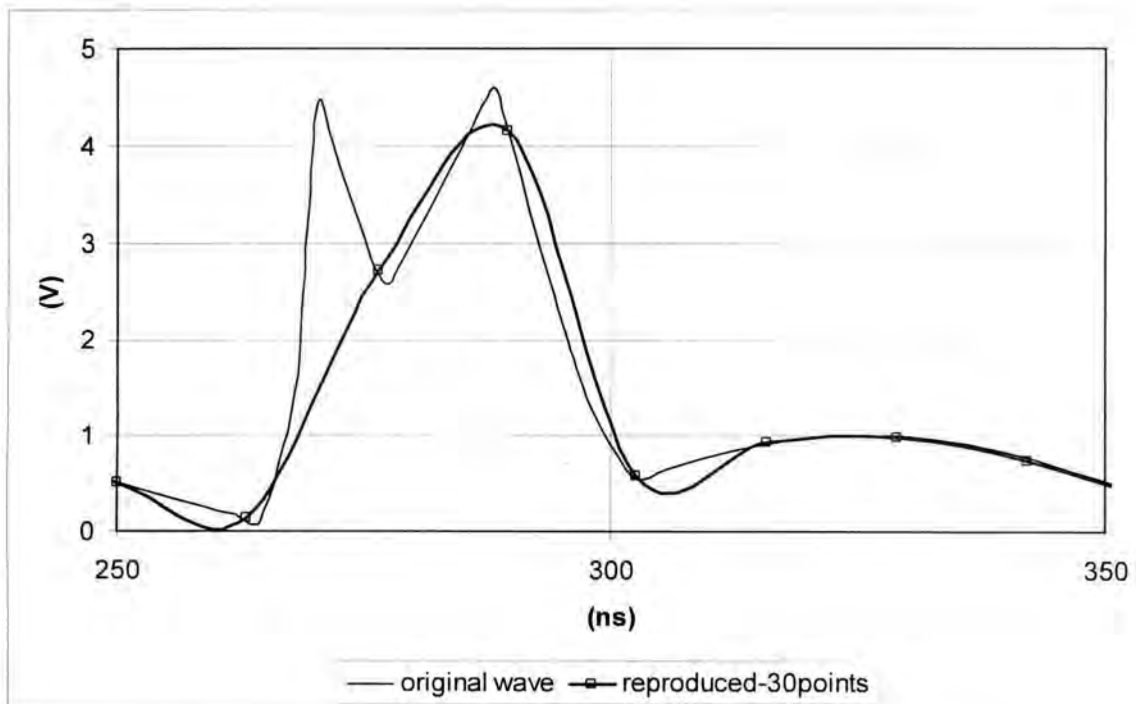

Fig. 4.7: Zoomed view of the high frequency portion. The reproduce version with one peak is way different from the original signal with two dominant peaks.

Condition 2: The system is adjusted to catch up the maximum frequency

This time the system designers have selected the sampling frequency so that it doesn't miss any portion of the frequency band. To do so they have increased the sampling frequency to cover the maximum frequency present in the signal stream. Increased sampling frequency ensures correct sampling of high frequency portion but at the same time it over samples the lower frequency range. Over sampling means more sampling points per unit time than required. Over sampling doesn't hurt signal reproduction but is redundant. With limited available bandwidth, the luxury to produce redundant bit stream which occupy costly bandwidth cannot be afforded. Fig. 4.8 shows the case with 120 points sampling. Fig. 4.9 shows the reproduced signal from the sample and hold circuit which sampled the whole stream in to 120 points.

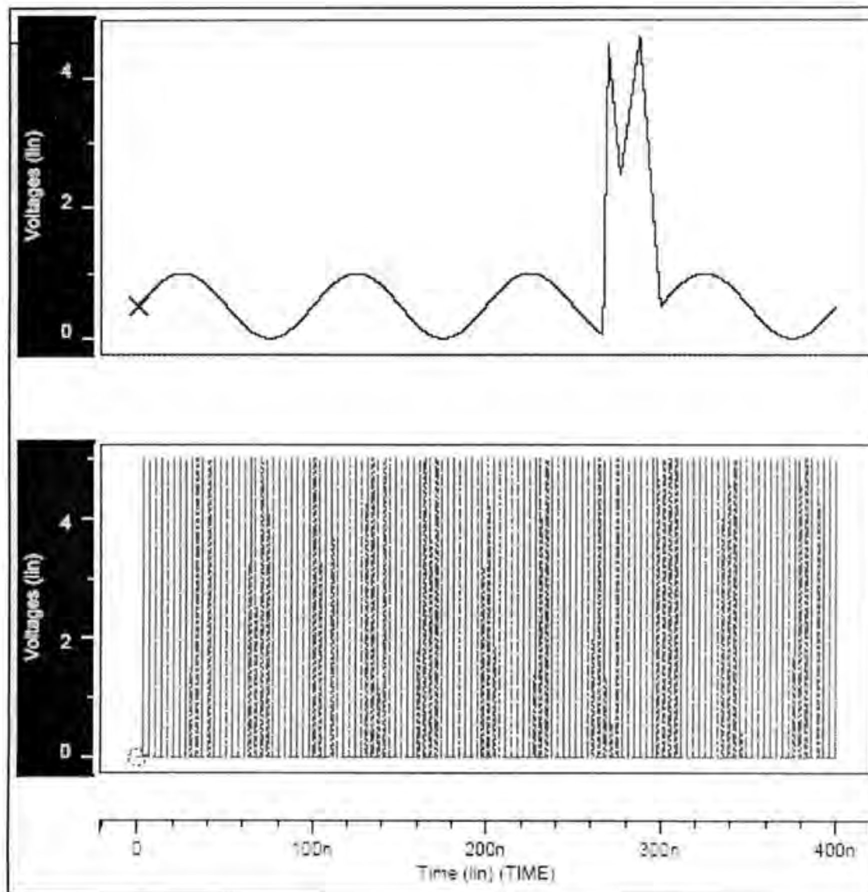

Fig. 4.8: Simulation of a system with composite frequency signal. The sampling frequency is selected based on the maximum predictable frequency. The low frequency portion is over sampled and the high frequency portion is correctly sampled.

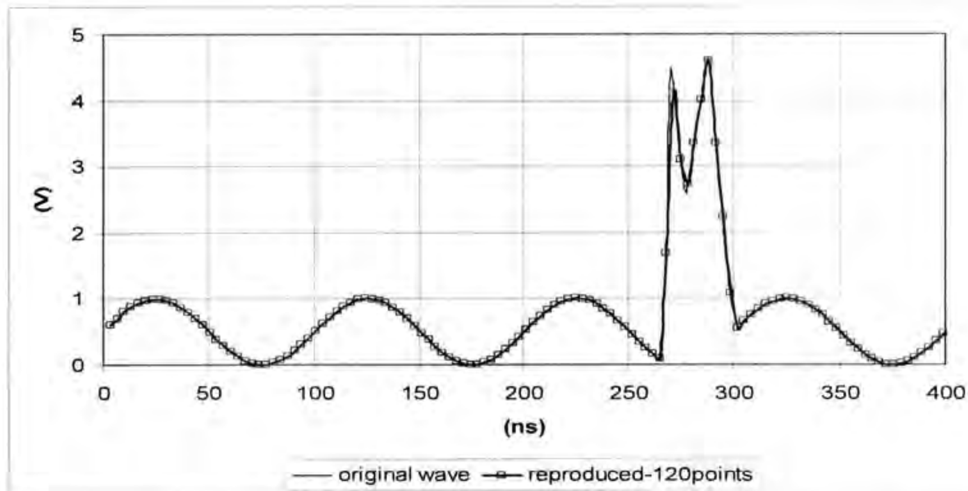

Fig. 4.9: Reproduction with 120 points fixed frequency sampling.

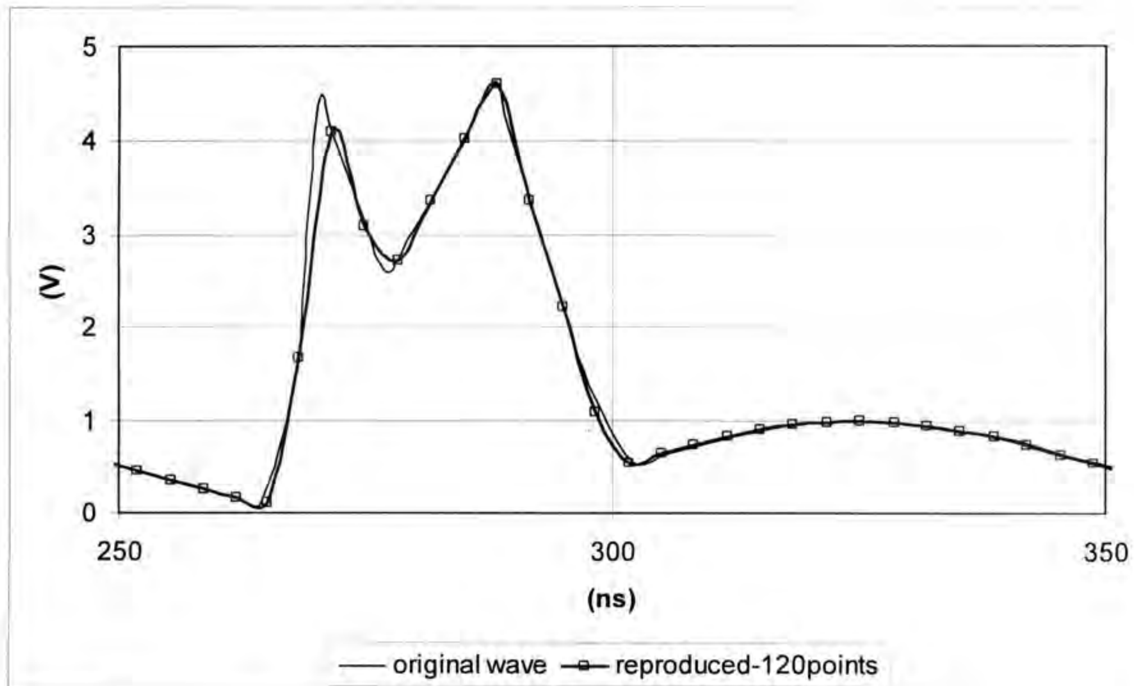

Fig. 4.10: Zoomed view of reproduced wave from 120 point sampling.

Reproduction of 120 points sampling predicts both high frequency and low frequency portions almost accurately as shown closely in Fig. 4.10. This is a solution to our first problem of signal loss. It reproduces a signal almost accurately. But at the same time it introduces another problem – higher bit rate. Since the number of sampling points has increased 4 times, so does the bit rate. It means higher bandwidth and higher cost. So, in the course of solving a problem we have actually introduced another. It's a dilemma which can only be solved by implementing a system with the capability to change

sampling frequency adaptively. That is, the system should keep the sampling frequency lower when the incoming signal is of lower frequency and immediately change the sampling frequency to higher one whenever a high frequency component arrives. This can be done by monitoring the slope of the incoming signal stream based on which the sampling frequency for the signal can be determined.

Condition 3: SET based RCO implemented sample and hold circuit

Fig. 4.11 shows the simulation result of the circuit shown in Fig. 4.3. The input signal is fed to the gate electrode of the SET along with the input buffer stage. The SET produces an oscillation current whose frequency is proportional to the slope of the incoming signal. The oscillating current is converted to pulsating voltages. These voltage pulses produce digital ON-OFF pulse through successive blocks thus exhibiting the same frequency. These pulses are used to sample the same incoming wave whose slope has produced the particular frequency at that moment. At each instant the incoming slope monitored and then a particular frequency is produced depending on the slope at that instant and a sampling signal of that frequency is employed to sample the incoming signal.

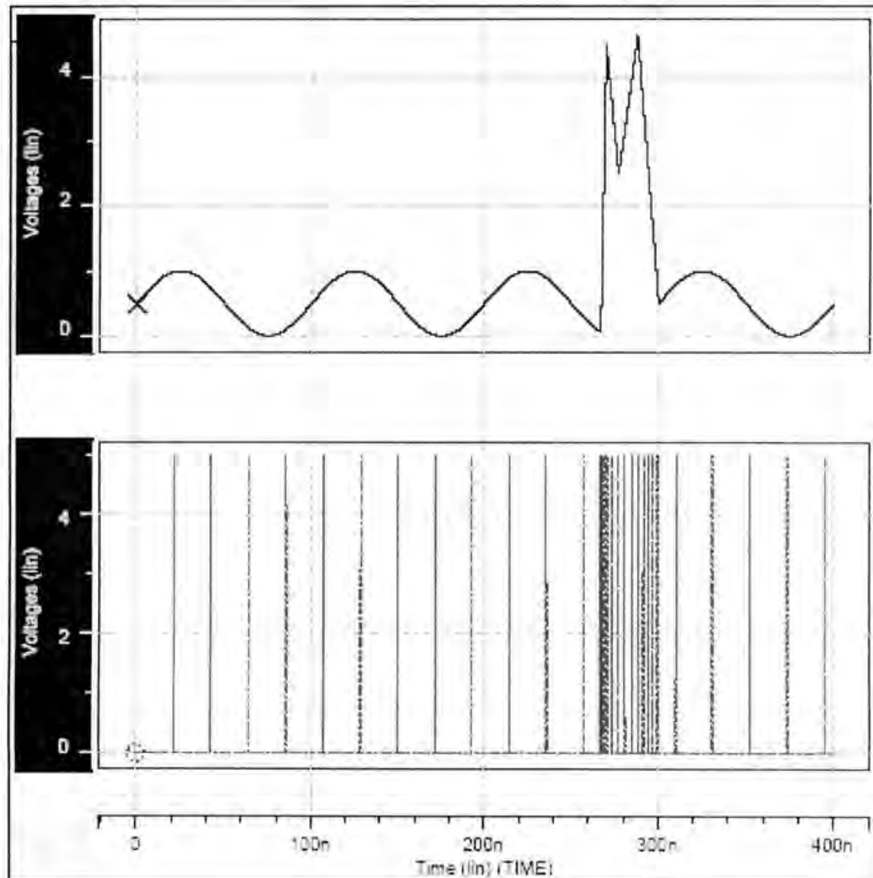

Fig. 4.11: Sampling with adaptive sampler implement by SET based RCO

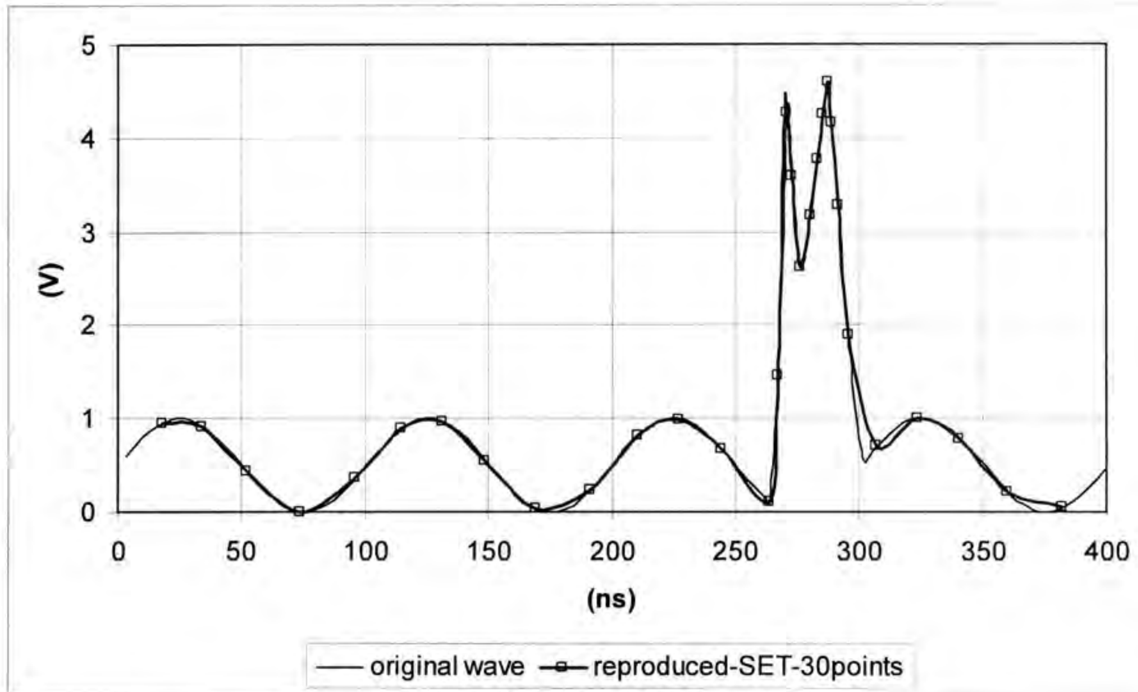

Fig. 4.12: Signal reproduction after sampling by adaptive sampler

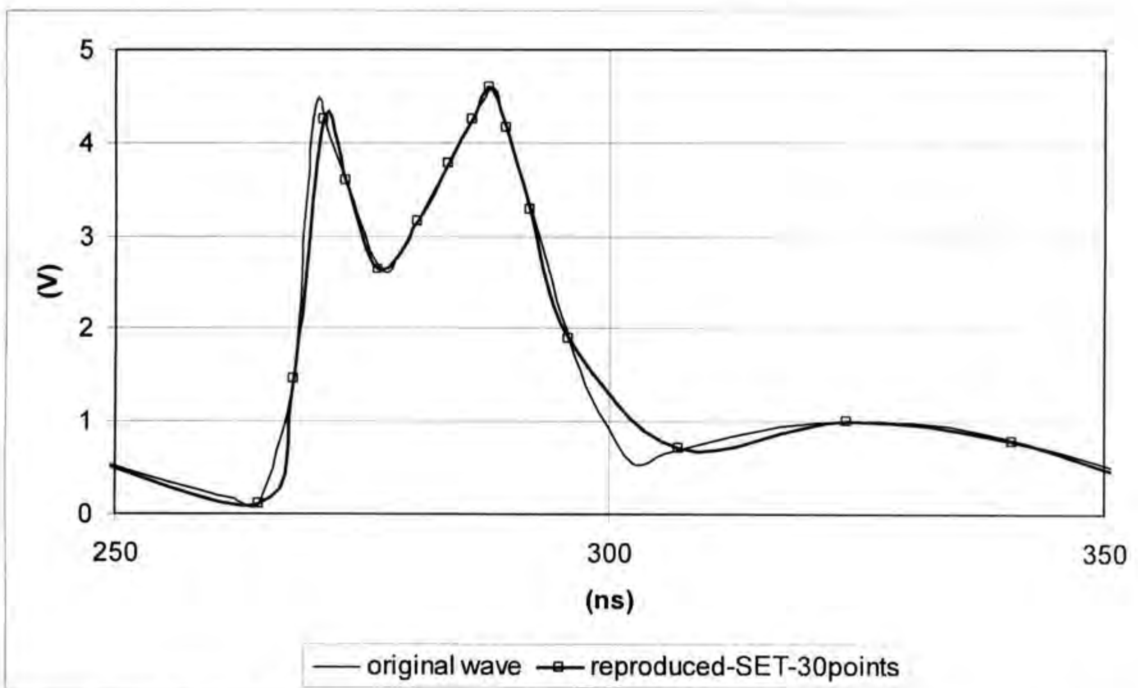

Fig. 4.13: Zoomed view of the high frequency portion of the wave of the reproduced signal. The reproduced signal is almost an exact replica of the original signal although requires only 30 sampling points.

Fig. 4.11 show the incoming signal and the sampling wave shape. As the frequency varies at a lower frequency rate in the first part of the signal, the sampling frequency is low, just enough to meet the Nyquest criterion. Later, the signal changes quickly. The SET RCO immediately registers the change and generates a higher sampling frequency for that part of the wave. As the input signal frequency reduces, the sampling frequency adaptively changes to lower value not to over sample signal stream and thus save valuable bandwidth. As evident from Fig. 4.12 and 4.13, the 30 point sampling of the signal stream produces a good result. The reproduced signal is almost an exact replica of the input signal. In contrast to the conventional system, where exact replication of the input signal requires 120 points of sampled data and 30 points conventional sampling reproduced an incomplete signal. The SET based RCO sampler reproduce a good replica with only 30 sampling points.

Fig. 4.14 shows the comparison of conventional 30 points sampling to SET RCO based 30 point sampling. Though both samplers used 30 data points, the conventional sampler failed to reproduce the input signal. Fig. 4.15 compares the reproduced wave between the conventional sampler at a higher rate (total 120 points) and that of the SET sampler with much lesser data points (30 points). Both the schemes reproduce the signal with good accuracy where the SET sampler uses only one-fourth the data points compared to the conventional sampler. This means the SET sampler would require only 25% of bandwidth required by the conventional sampler.

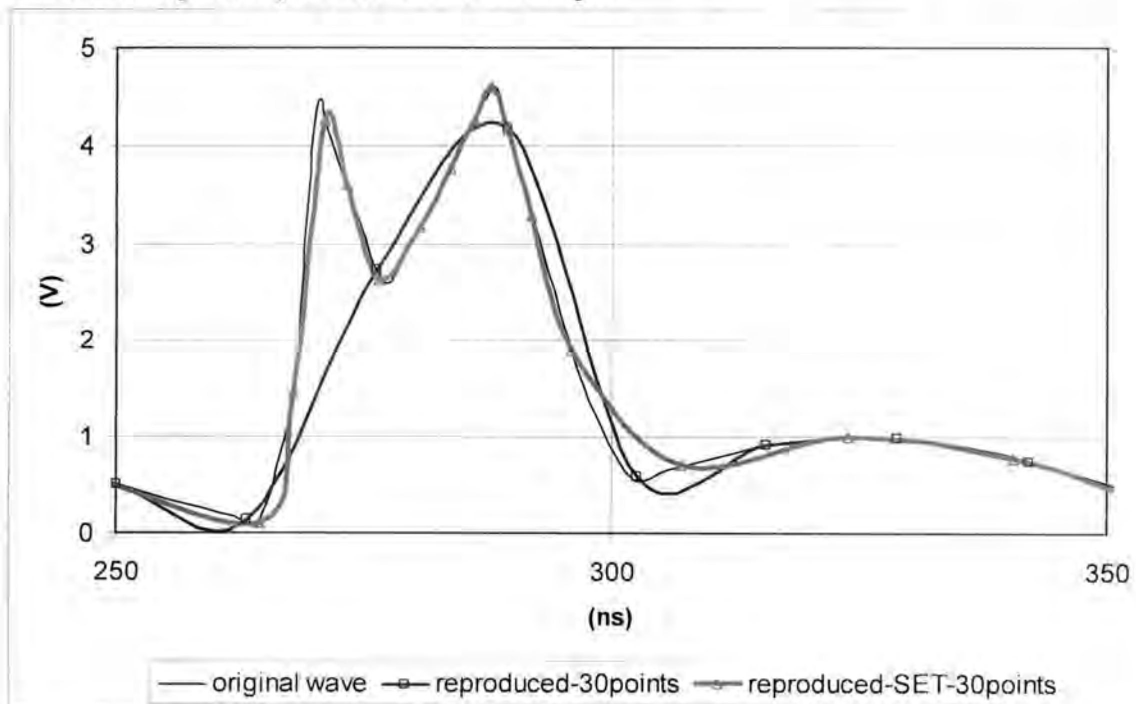

Fig. 4.14: Conventional sampler and SET based sampler reproduced output. Conventional sampler failed to detect signal peaks while adaptive sampler produces almost exact replica.

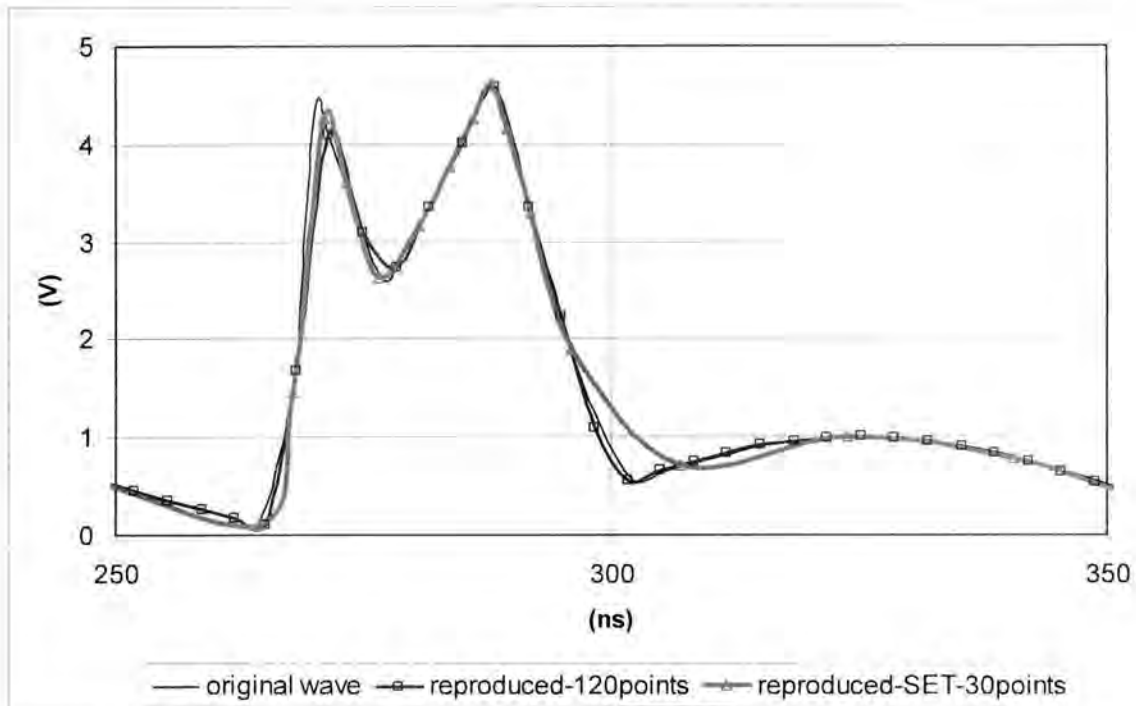

Fig. 4.15: Conventional sampler with 120 points and the SET sampler with 30 points. Both reproduce the signal with enough accuracy but SET sampler requires only one-fourth data points than those of the conventional sampler.

4.5 Circuit Issues

The circuit we have discussed has some implementation issues these issues are discussed in this section.

Single electron transistor is sensitive down to one electron. One electron can switch the transistor from ON state to OFF state. This extreme sensitivity also has its drawbacks. An electron injected from a noisy surroundings might upset the circuit operation. Adequate noise isolation and filtering must be considered while implementing circuits those uses the single electron transistors.

Another problem is the delay produced by the rate controlled oscillation generator. Since the SET is sensing the slope of the signal and then converting the information of the slope into a variation of frequency of the oscillator through consecutive circuit sections, a finite delay is expected. If the delay is significant compared to the change in slope of the input signal, the sampling frequency might miss parts of the quickly changing signal. The sampling frequency generation path has to be as fast as possible. In fact, the maximum possible frequency that might be sampled by this adaptive sampler will be determined by the fastest possible response of the sampler frequency generator path. Proper biasing and use of small and fast devices will allow minimize delay in these circuits.

In the operation of SET, the total capacitance of the system plays a vital role in determining the Coulomb gap voltage. The junction capacitance at the gate electrode and the two tunneling junction must be kept as small as possible which will facilitate the use of the circuit at higher temperature. Specially designed fabrication process minimizes capacitance. Short description of a relatively new and feasible fabrication process in discussed in chapter 2.

Besides, the interface of quantum nano-devices like the SET to external world of electronics is another engineering challenge. Since for successful operation of SET at room temperature, the junction capacitance has to be as small as atto-farad (10^{-18} F), the interface capacitance might outweigh the junction capacitance which might upset the operating point of the device.

CHAPTER 5
Conclusion

This thesis work focuses on the application of the single electron transistor which is considered as a promising nano-electric device to meet the ever increasing demand of the new millennium. Here a specific circuit setup is proposed using single electron transistor which will act as a rate controlled oscillator. The main function of the rate controlled oscillator will be to detect the slope (rate of change of signal, dv/dt) of the incoming signal that is fed to the gate of the SET device and generate a frequency which is exactly proportional to the amount of the slope.

The rate controlled oscillator will find its application in many everyday circuits and will be equally possible to use in high end research projects. Such an application is also focused in this work. Since almost every form of signal handing system now-a-days first convert the analog signal to digital format for further processing and also for storing for future use, a sample and hold circuit is one of the most common of all elementary circuit configurations. The SET based rate controlled oscillator is applied in a sample and hold circuit. The rate controlled oscillator provides significant advantage over conventional way of sampling. It is seen from the simulation data that the adaptive sample and hold circuit in fact performs far better than conventional way sampler. The adaptive sampler based on SET implemented rate controlled oscillator, samples a stream of signal composed with multiple frequency components with better accuracy and at the same time with fewer sampling point. It thus provides a twofold advantage over conventional technology. It can change the sampling frequency based on the detected slope of the incoming signal. The system intelligently detects the slope and adaptively changes the sampling frequency – which is not possible with conventional systems. Moreover, proposed adaptive system requires only a fraction of the bandwidth necessary for a conventional system to represent the same signal stream.

Single electron transistor is being studied extensively all over the world – in universities and in industries. The potential it possesses has merely been started to be revealed. The outstanding characteristics of this quantum device will be uncovered soon.

CHAPTER 6
Scopes for future work

Single electron transistor is now-a -days considered a fundamental building block of the future sub-micron electronics. Because of its total quantum phenomenal behavior it possesses unique characteristics like no other electronic devices. This device thus promises a new dimension in electronics if the quantum characteristics is to be exploited. With the continuously shrinking of transistors as predicted by the Moore's Law, which has been true for the last 40 years, scientists and engineers are now nearing the limit of the old fashion transistor technology. With the transistor length now below 45nm (even 35nm transistor used in Intel Penryn processor fabricated in early 2007), engineers are experiencing an extraordinary problem for the first time in the history. They are running out of atomic layers. Conventional transistors required gate dielectric which has also shrank with transistor size. For the 45 nm transistor the gate dielectric thickness is approximately 1.2 nm which is roughly equal to 5 atomic layers of the regular dielectric material. The 5 atomic layers of dielectric is not a sufficiently good insulator. The leakage current is large making the transistor unreliable and unworkable. Intel has addressed the problem with two changes in technology – they no longer use silicon dioxide as dielectric and they are not using polysilicon as gate electrode material. Instead, they are using hafnium based high-k dielectric as gate dielectric and a metal for gate material for the first time in the commercial integrated circuit fabrication history [38-39]. Based on this technology, Intel will lunch its first processor on a 32nm technology in 2010 and on a 22nm technology in 2011 [40]. But this is not going to last long. Soon this technology will be demanding another change. And conventional technology can't keep up with Moore's law due to the constraint of atomic layer.

Having seen the limits of conventional shrinking transistor, scientists are in a hurry searching for suitable alternatives. Single Electron Transistor is considered a good choice because of its unique nature and also since engineers have already fabricated the device with convincing performance. This is why single electron transistor seems to be good area of exploration for the future engineering.

This thesis work proposes a plausible application for the SET. This work is based on theoretical analysis. With proper fabrication facility this idea can be implemented in a physical circuit.

Other issue like the delay of the slope to frequency converter circuit of the proposed rate controlled oscillator circuit is another area to be analyzed further. Since the delay of the slope to frequency conversion segment determine the maximum speed to the overall circuit it is the bottleneck of the overall bandwidth performance. The rate controlled oscillator will not and cannot process signal with accuracy whose frequency is higher than the bandwidth of the slope to frequency converter. Speeding up the slope to frequency generator circuit will increase the bandwidth of the rate controlled oscillator and will make it ready to sample signal with higher order frequency.

Another possible application area of SET can be analyzed focusing the inherent slowness of the device. Since the SET permits only one electron to be passed through the channel at any particular instant, the amount of current passed through the SET is inherently limited by the speed of electron through the quantum dot. This might lead to the velocity saturation effect of the SET. In addition to the physical property of saturation effect one might think of using this limitation as an advantage.

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