STUDY OF THE ANOMALOUS THRESHOLD VOLTAGE OF A SHORT-CHANNEL MOSFET

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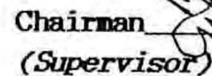
   Chairman 
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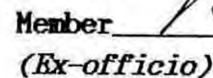
   Member 
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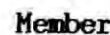
   Member 

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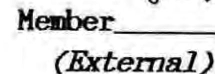
   Member 
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DECLARATION

I hereby declare that this work has been done by me and it has not been submitted elsewhere for the award of any degree or diploma.

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ABSTRACT

MOSFETs in integrated circuits have become smaller and smaller in order to achieve higher packaging density and to reduce cost. Reducing channel length of a MOSFET leads to undesirable effects in device characteristics. In order to get higher performance MOS devices, the modern fabrication technologies such as gate polysilicon, lightly doped drain (LDD) structure, heavy doping at the edge of the channel by halo ion implantation, very lightly doped region at the edge of the source/drain junction at the boundary to the channel by salicidation process and formation of salicide simultaneously in the source, drain and polysilicon gate regions are used. Also overlapping of gate to the source and drain junctions are avoided so that stray capacitance does form at the gate-drain and gate-source regions. All fabrication techniques mentioned above result the potential barrier at the source and/or drain junction to the boundary of the surface channel. This potential barrier can severely degrade the drain current and transconductance of the device. Also, this barrier causes increased threshold voltage as the channel length of the device is decreased. As the behaviour of the device deviates from its normal characteristics, the resulting phenomena is known as anomalous behaviour of short-channel MOSFET. In this thesis the I-V characteristics and transconductance of short channel device have been modeled by considering the barrier potential both in the subthreshold and active regions incorporating the physics of the anomalous behaviour. The results have been compared with the long-channel MOS behaviour.

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LIST OF SYMBOLS

1. w cm Depletion width.
2. W_S cm Source depletion width.
3. W_D cm Drain depletion width.
4. w_i cm Inversion layer width.
5. L cm Effective channel length.
6. V_T V Threshold voltage.
7. n cm^{-3} Electron concentration.
8. p cm^{-3} Hole concentration.
9. N_A cm^{-3} Substrate doping.
10. ψ V Intrinsic level potential.
11. ψ_S V Surface potential.
12. Φ_f V Fermi potential.
13. Φ_{si} V Surface potential at strong inversion
14. Q_B cm^{-2} Bulk charge.
15. Q_I cm^{-2} Inversion layer charge.
16. Q_S cm^{-2} Surface charge.
17. Q_G cm^{-2} Gate charge.
18. V_G V Gate voltage.
19. V_{FB} V Flat band voltage.
20. V_O V Oxide voltage.
21. V_{SB} V Surface-bulk voltage.
22. C_o Fcm^{-2} Oxide capacitance per unit area.
23. t_{ox} cm Oxide thickness.
24. ϵ_s Fcm^{-1} Permittivity of silicon.
25. ϵ_{ox} Fcm^{-1} Permittivity of oxide.

26.	E_x	Vcm^{-1}	Transverse electric field.
27.	E_Y	Vcm^{-1}	Lateral electric field.
28.	ϕ_m	V	Potential at the metal surface.
29.	ϕ_s	V	Potential at the silicon surface.
30.	χ	V	Potential at the conduction band.
31.	I_O	A	Saturation current.
32.	I_D	A	Drain current.
33.	V_C	V	Channel drop.
34.	μ	$cm^2V^{-1}S^{-1}$	Effective surface mobility.
35.	R	Ω	Source/drain resistance.
36.	V_R	V	Source/drain resistance drop.
37.	G_m	mho	Channel conductance.
38.	V_D	V	Drain voltage.
39.	θ	V^{-1}	Mobility reduction factor.
40.	V_B	V	Barrier potential.

CHAPTER 1

INTRODUCTION

1.1 Short-channel MOSFETs

A MOSFET is a unipolar voltage controlled device in which the lateral current is controlled by an externally applied vertical electrical field. A typical n-channel enhancement MOS transistor consists of source, gate, drain and substrate. The n^+ source and drain regions are diffused or implanted into a relatively lightly doped p-type substrate and a thin oxide layer separates the aluminium metal gate from the silicon surface (Fig. 1.1). No current flows from drain to source without a conducting n-channel between them, since the drain-substrate-source combination includes oppositely directed p-n junctions in series.

When a positive voltage is applied to the gate relative to the substrate, positive charges are in effect deposited on the gate metal. In response, negative charges are induced in the underlying Si, by the formation of a depletion region and a thin surface region containing mobile electrons. These induced electrons form the channel of the MOSFET, and allow current to flow from drain to source. The effect of the gate voltage is to vary the conductance of this induced channel for low drain to source voltage.

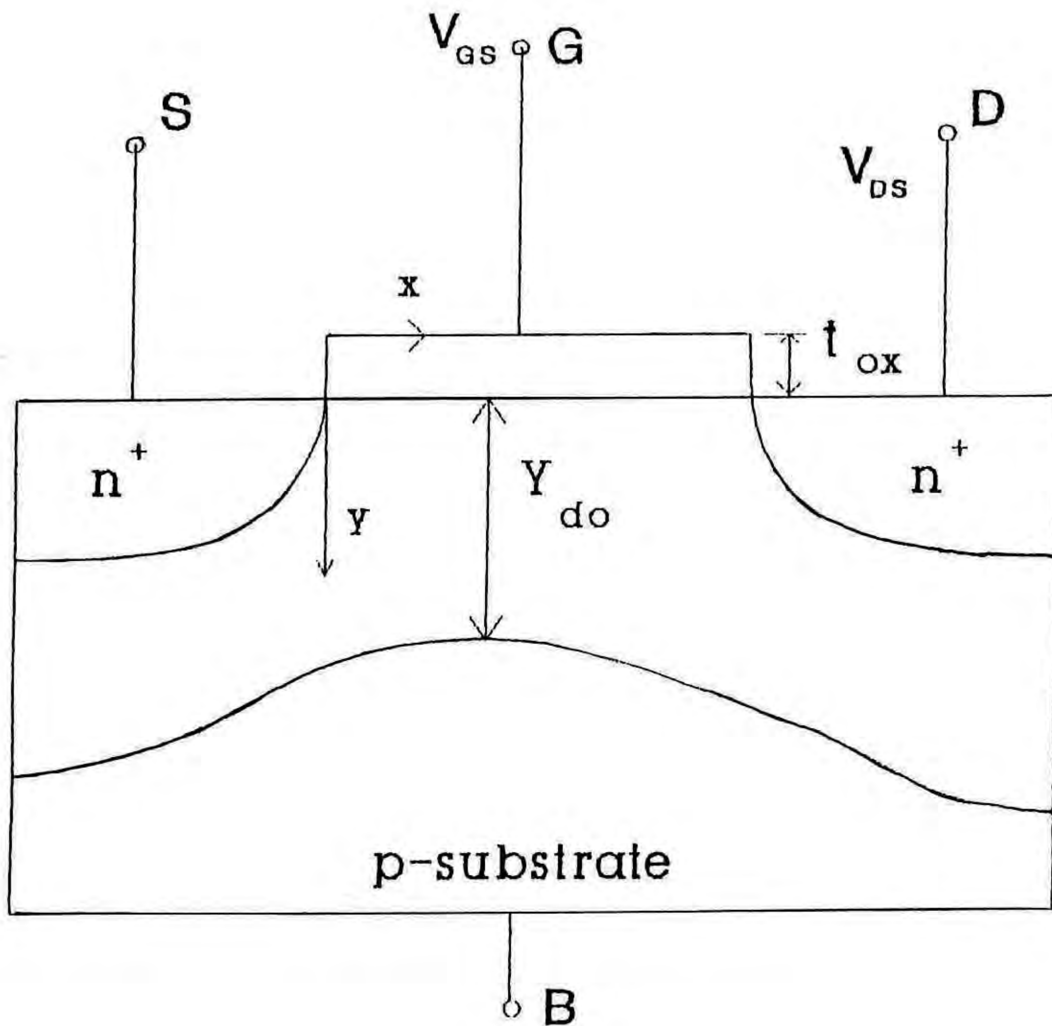

Fig.1.1 The schematic cross-section of an n-channel MOSFET.

Based on the channel length dimension between the source and drain, MOSFETs are classified as short and long n-channel MOSFETs. The principal applications of MOSFETs are in VLSI technology, specially in case of digital systems such as semiconductor memories, long shift registers, microprocessors etc. The purpose of microminiaturization is to increase the packing density and to improve the circuit performance. When the channel length L is much larger than the sum of the source and drain depletion widths (W_S+W_D) (Fig. 1.2), it is called long channel MOSFET and when $L \leq (W_S+W_D)$, the MOSFET is called short-channel MOSFET. Generally, the MOSFET having the channel length less than 1μm is called short-channel MOSFET. But when device dimension is reduced by reducing the channel length, the behaviour of the MOSFET departs from the long-channel behaviour and we have to consider the short-channel effects which arise due to two dimensional potential distribution and high electric field in the channel region.

1.2 Threshold voltage of MOSFETs

The threshold voltage V_T of a MOSFET is defined as the minimum gate voltage required to induce the conduction channel. It is an important parameter of MOS transistor.

The electron and hole concentrations in the p-type substrate are given [1] as,

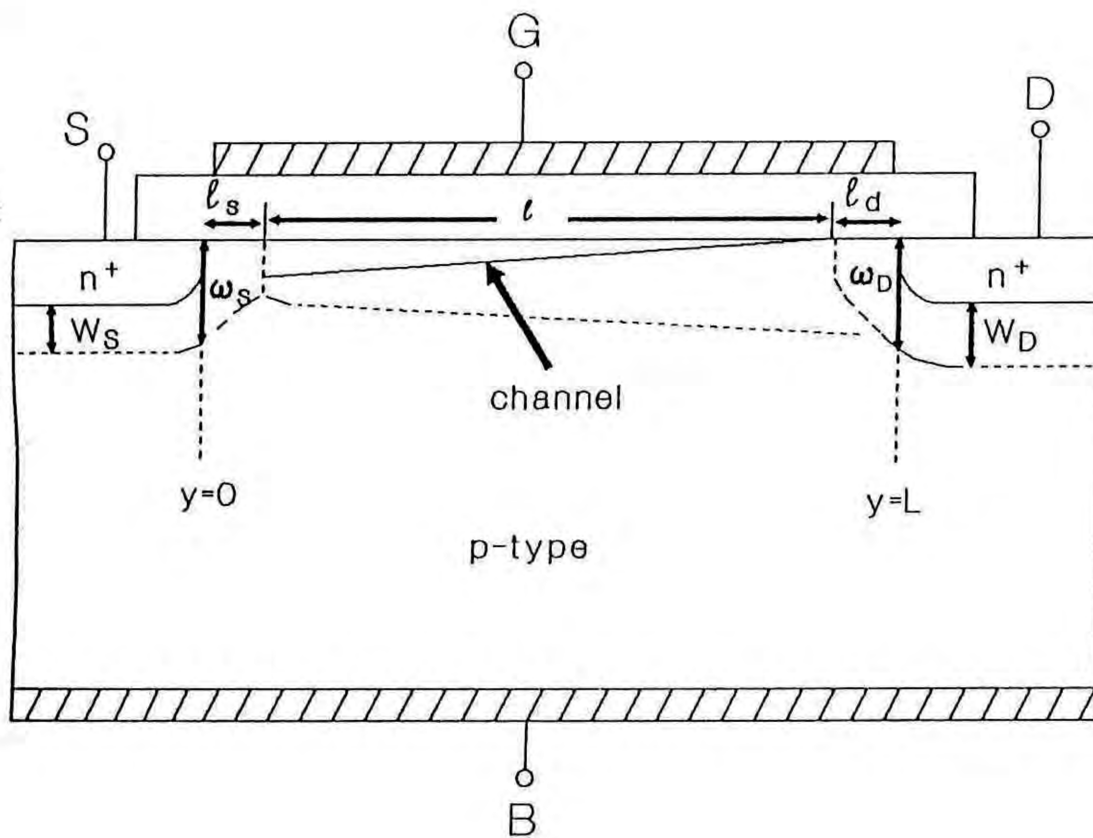

Fig.1.2 Simplified diagram of an n-channel MOSFET.

$$n = n_i e^{\frac{q}{kT}(\psi - \phi_f)} \qquad (1.1)$$

and

$$p = n_i e^{\frac{q}{kT}(\phi_f - \psi)} \qquad (1.2)$$

where, n_i is the intrinsic concentration, ϕ_f and ψ are the potentials of the Fermi level and the intrinsic level respectively.Taking the intrinsic level potential in the bulk region of the substrate as zero, the electron concentration can be written as

$$n = N_A e^{\frac{q}{kT}(\psi - 2\phi_f)} \qquad (1.3)$$

where, N_A is the doping density of the substrate.

When a positive gate voltage is applied to a MOSFET it causes a band bending in the substrate material and the potential of the substrate called surface potential increases from zero to a value of ψ_s with respect to the bulk (Fig. 1.3). Increase of the value of u results in depletion of majority carriers in the substrate region as given by equation(1.2). When the potential increases to $\psi = \phi_f$, the majority and minority carrier concentrations become equal. If sufficient band bending is produced by the gate voltage such that the surface potential ψ_s exceeds the value of ϕ_f, electron concentration in the surface exceeds the intrinsic value and the surface is said to be inverted.

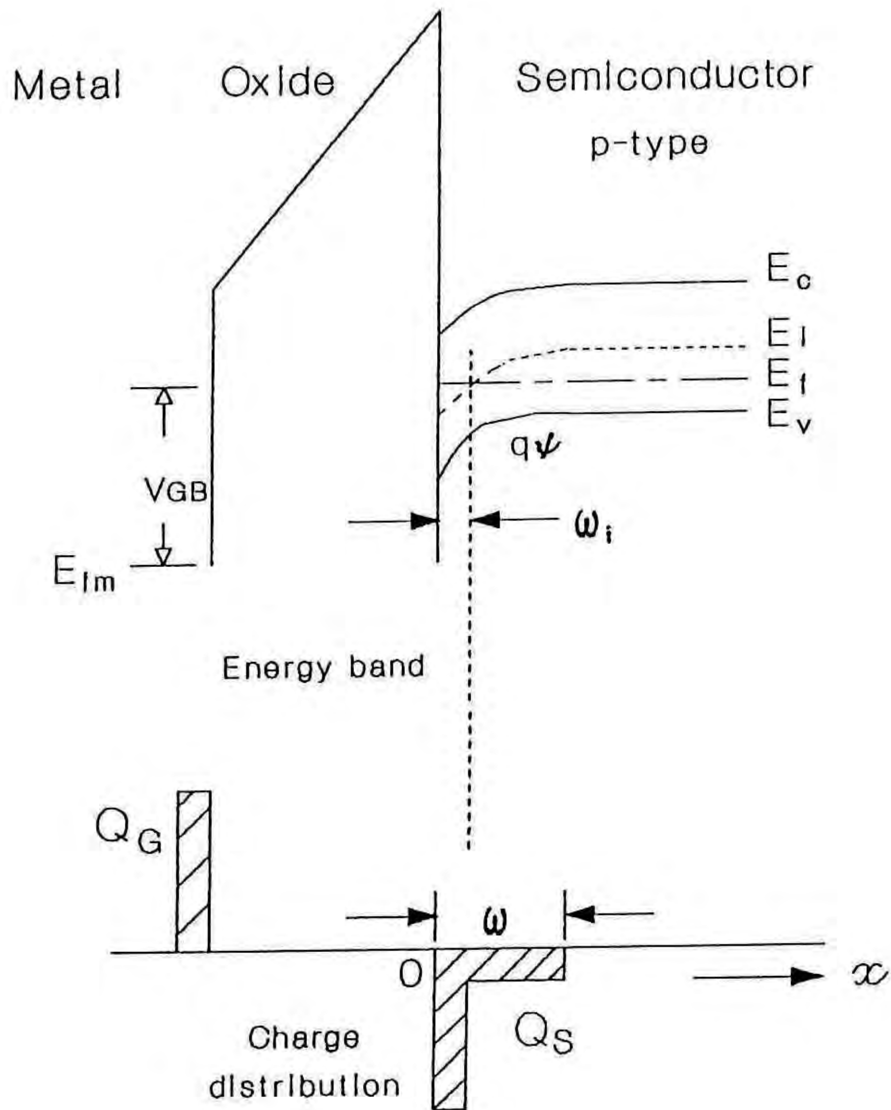

Fig.1.3 Energy band and charge distribution diagram of a MOSFET.

As the surface is inverted whenever ψ_s is larger than ϕ_f, a practical criterion is needed to tell us whether a true n-type conducting channel exists at the surface. The best criterion for moderate inversion is that the surface should be as strongly n-type as the substrate p-type. Therefore, the surface potential under moderate inversion is given by (Fig. 1.4)

$$\psi_s=2\phi_f=\phi_{si} \tag{1.4}$$

within this region, the inversion layer charge is small compared to the depletion layer charge. From the band bending of $2\phi_f$ to approximately $2\phi_f+6\phi_T$ [2], the incremental change of the inversion layer charge is comparable to that of depletion layer charge. This region is defined as the moderate inversion region. If the surface potential exceeds the value of $2\phi_f+m\phi_T$, where m is usually taken as 6, the inversion layer charge becomes very large in comparison to the depletion layer charge and the transistor is said to be in strong inversion mode. The left side of X_I (Fig. 1.4) remains n-type, whereas, the right side remains p-type. So at the left side of X_I a region of inversion layer of width w_1 and at the right hand side of X_I, a surface depletion region of w is produced which extends up to bulk. The depletion layer width w and bulk charge Q_B is given by,

$$w=\sqrt{\frac{2\epsilon_s(\psi_s+V_{SB})}{qN_A}} \tag{1.5}$$

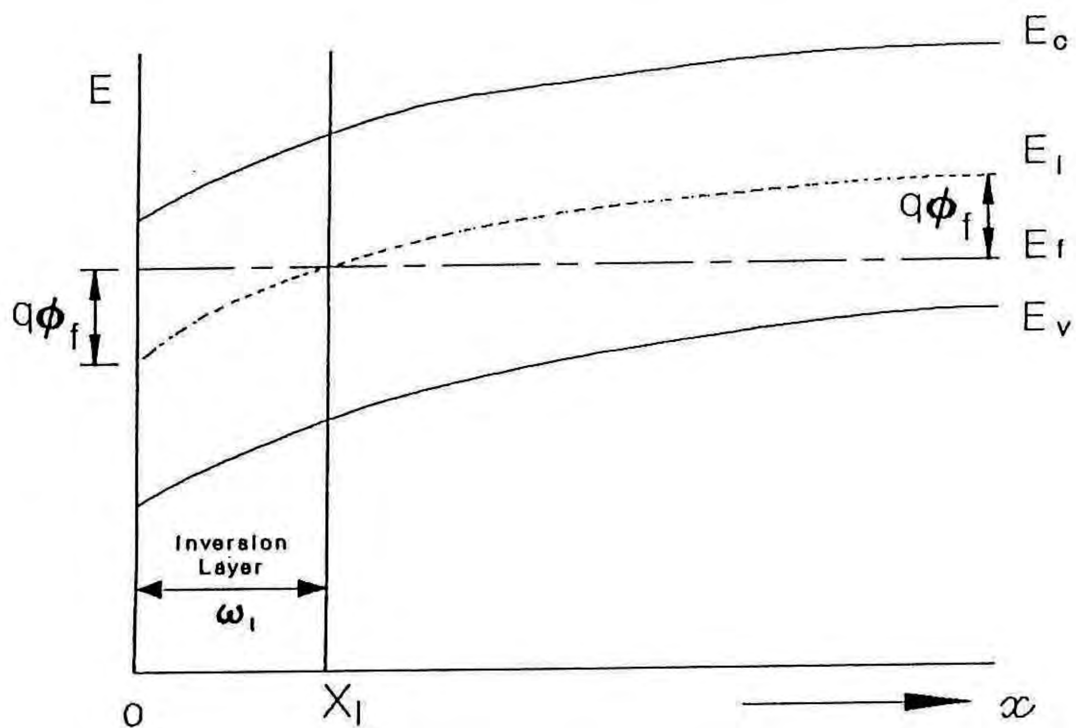

Fig.1.4 Energy band diagram of a MOSFET at the onset of strong inversion.

and

$$Q_B=-qN_A W \tag{1.6}$$

where, V_{SB} is the substrate biasing.

The charge balance equation in the surface region of a MOSFET can be written as

$$Q_S=Q_I+Q_B \tag{1.7}$$

$$=Q_G \tag{1.8}$$

where, Q_S, Q_I and Q_G are total charge, inversion layer charge and gate charge respectively.

The applied gate voltage V_G in a MOSFET is shared by the flat band voltage V_{FB}, surface potential ψ_S and voltage across the oxide V_O and it is given by,

$$V_{GB}=V_{FB}+\psi_S-\frac{Q_S}{C_O} \tag{1.9}$$

$$=V_{FB}+\psi_S+\gamma\sqrt{(\psi_S+V_{SB})} \tag{1.10}$$

where,

$$\gamma=\frac{\sqrt{2q\epsilon_s N_A}}{C_O} \qquad (1.11)$$

In this expression Co is the oxide capacitance per unit area and is given by,

$$C_O=\frac{\epsilon_{ox}}{t_{ox}} \qquad (1.12)$$

where, tox is the oxide thickness.

The threshold voltage is defined as the sum of the flat-band voltage, the voltage to support a depletion region charge Q_B and the voltage to produce band bending for strong inversion. So from the expression of gate voltage the threshold voltage can be represented by,

$$V_T=V_{FB}+2\phi_f-\frac{Q_B}{C_O} \qquad (1.13)$$

$$=V_{FB}+2\phi_f+\frac{\sqrt{2q\epsilon_s N_A(2\phi_f+V_{SB})}}{C_O} \qquad (1.14)$$

The threshold voltage of a MOSFET for a certain operating condition can be obtained from equation(1.14). However, this can only be applied for long channel devices.

1.3 Short channel effects of a MOSFET

For a given channel doping concentration, as the channel length is reduced, the depletion-layer width of the source and drain junctions become comparable to the channel length. The potential distribution in the channel now depends on both transverse field E_x (controlled by the gate voltage and back-surface bias) and longitudinal field E_y (controlled by the drain bias). Due to this two dimensional potential distribution the gradual channel approximation (i.e. $E_x \gg E_y$) is no longer valid. This two dimensional potential distribution results in degradation of the subthreshold behaviour, dependence of the threshold voltage on channel length and biasing voltage, and failure of current saturation due to punch through. If the channel is both short and narrow then a three dimensional analysis is required. Though three dimensional analysis is accurate it is very complex and can be replaced by a model for simple calculation using empirical approximations and examining different phenomena one at a time.

In short-channel MOSFET the charges at the drain and source edges must be taken into account while calculating the threshold voltage of the MOSFET. In short-channel MOSFET the lateral extension of the depletion layer region reduces the effective channel length after the channel is pinched off and is known as channel length modulation (Fig. 1.5). When the lateral electric field is increased, the channel mobility becomes field dependent and eventually velocity saturation

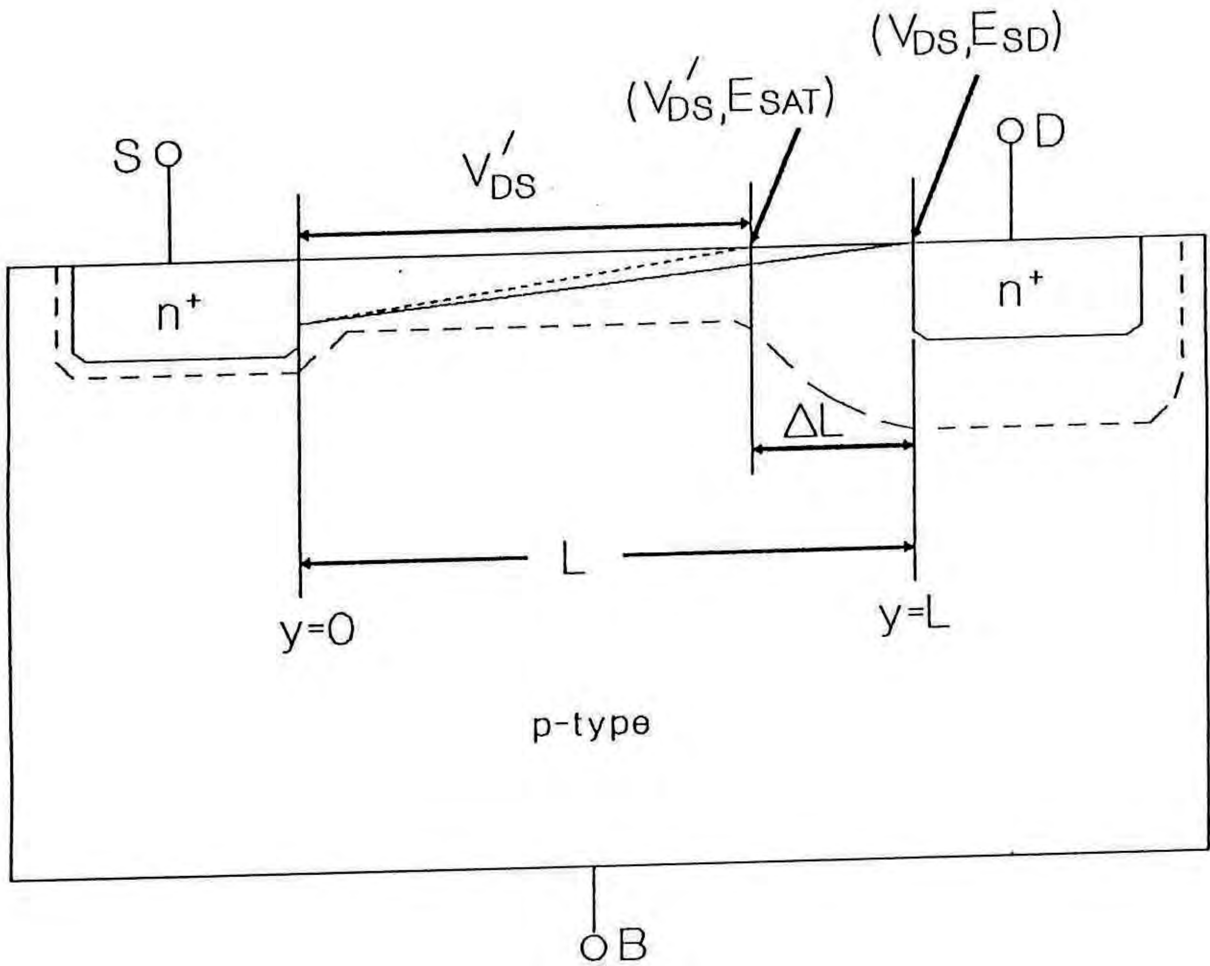

Fig.1.5 Channel length modulation of MOSFET.

occurs. When the lateral field is increased further, carrier multiplication near the drain occurs, leading to substrate current and parasitic bipolar transistor action. High field also causes hot-carrier injection into the oxide, leading to oxide charging and subsequent threshold voltage shift. This short-channel effect should be eliminated or minimized so that a physical short-channel device can preserve the electrical long-channel behaviour.

1.4 Effect of substrate bias

In a MOSFET it is assumed that the source is generally connected to the substrate and both terminals are grounded. In fact it is possible to apply a voltage between source and body. With a reverse bias between the substrate and the source, the depletion region is widened and the threshold gate voltage required to achieve inversion must be increased to accommodate the larger Q_B.

When V_{SB} is zero, the charge in the space charge layer is given by,

$$Q_B=-qN_A w=-\sqrt{(2q\epsilon_s N_A \Phi_{B1})} \quad (1.15)$$

for an arbitrary reverse bias voltage V_{SB}, we have

$$Q_B=-\sqrt{2q\epsilon_s N_A (V_{SB}+\Phi_{B1})} \quad (1.16)$$

Therefore the incremental charge is,

$$\Delta Q_B=-\sqrt{2q\epsilon_s N_A}\left(\sqrt{V_{SB}+\Phi_{Bi}}-\sqrt{\Phi_{Bi}}\right) \tag{1.17}$$

To reach the condition of strong inversion, the applied gate voltage must be increased to compensate for Q_B. Therefore,

$$\Delta V_T=-\frac{\Delta Q_B}{C_O} \tag{1.18}$$

If the substrate bias V_{SB} is much larger than Φ_{Bi}, the threshold voltage is dominated by V_{SB} and

$$\Delta V_T=\frac{\sqrt{2q\epsilon_s N_A V_{SB}}}{C_O} \tag{1.19}$$

When a positive V_{SB} is applied to the substrate with respect to source then the situation will be reversed. The source-substrate and the channel-substrate junctions both will be forward biased and to maintain the charge balance equation the inversion layer charge must be increased, whereas, the depletion layer charge is decreased. So in an n-channel MOSFET, V_{SB} must be zero or negative to avoid the forward bias of the source junction.

1.5 Short-channel effect on threshold voltage

A MOS device is considered short when the channel length is of the same order of magnitude as the source and drain

depletion depth. Depending on the variety of parameters and applied biases, a channel length of less than 1μm can be considered short. The threshold voltage of a short-channel device decreases as the channel length becomes small.

For short-channel MOSFETs, a considerable portion of the channel is occupied by the depletion layers formed by the source and drain. The gate voltage therefore deplete the region under the inversion layer up to more depth. The deeper depletion layer is accompanied by a large surface potential, which makes the channel more attractive for electrons. As a result, the device shows more conductivity than that would be predicted from long-channel theory for a given V_{GS} and thus the threshold voltage is decreased. The depletion region under the channel can also be widened and the corresponding surface potential can be increased by raising the potential of the drain (Fig-1.3). Hence, the threshold voltage is also a decreasing function of V_{DS}. An increase in surface potential corresponds to a decrease of potential energy barrier to the entrance of electrons in the channel and thus this concept of describing the short channel effect on threshold voltage is called barrier lowering effect [2].

Another concept called charge sharing approach is introduced to explain the threshold voltage. It provides physical insight into the development of the threshold voltage expression. The threshold voltage expression for a long-channel MOSFET is obtained from equation(1.14) and is

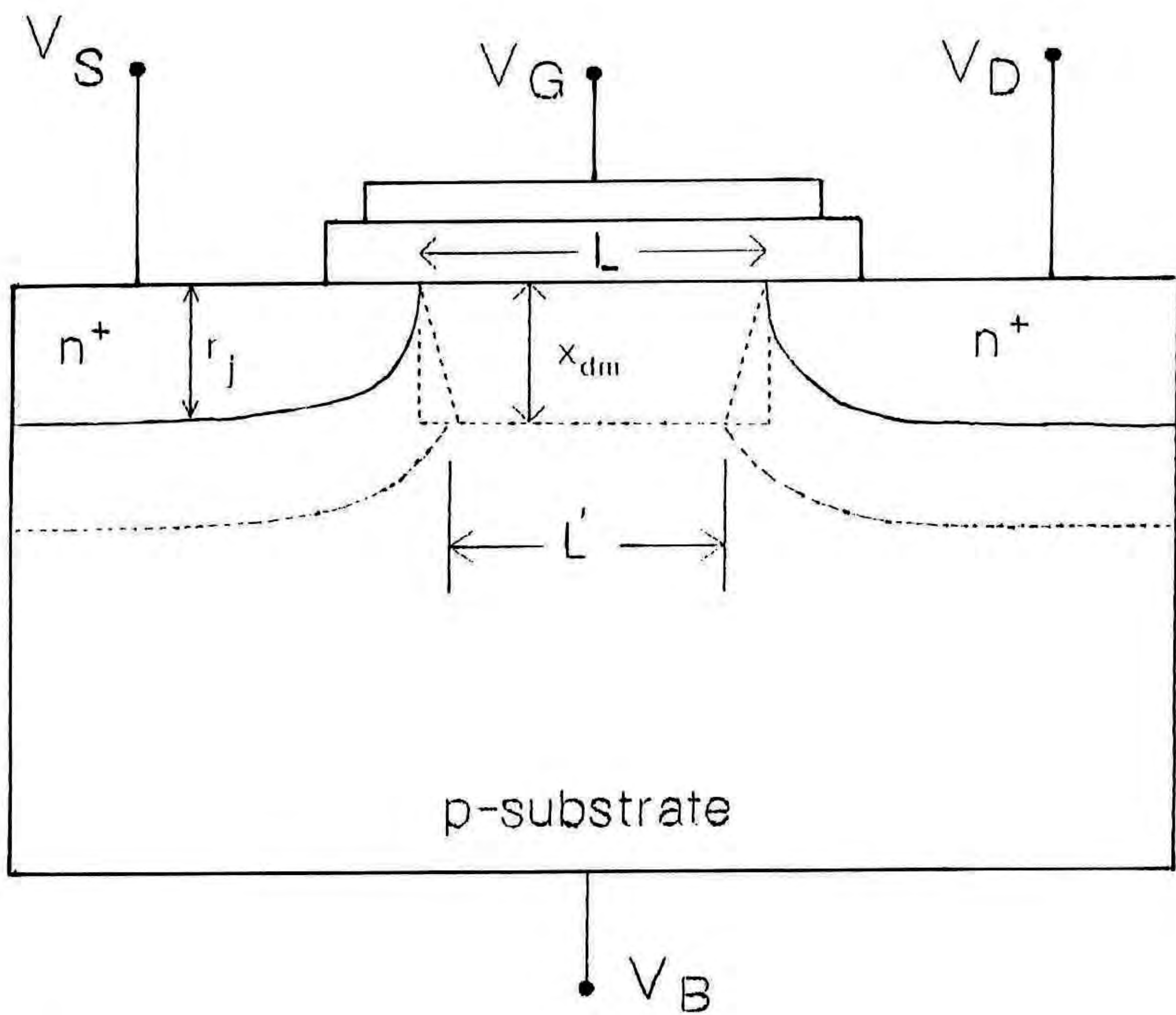

Fig.1.6 Charge sharing model.

$$V_T = V_{FB} + 2\phi_f - \frac{Q_B}{C_O} \tag{1.20}$$

where, Q_B is given by equation(1.6).

The total charge contributing to the threshold voltage under the gate contact is WLQ_B, which is represented by the rectangle with a width of x_{dm} and a length of L (Fig. 1.6). However, if we assume part of this charge is shared by the source and the drain such that only the area insight the trapezoid is controlled by the gate, the bulk charge becomes,

$$Q_B'L = qN_A x_{dm} \frac{(L+L')}{2} \tag{1.21}$$

Thus the total charge contribution to the gate voltage is taken as WLQ_B' instead of WLQ_B and expression(1.14) is used to calculate the threshold voltage. As $L'<L$, $Q_B' < Q_B$ and the threshold voltage is seen to be decreased in case of short-channel device.

1.6 Effect of insufficient gate overlap to the source and drain junctions

A troublesome stray capacitance results from the overlap of the gate with the source and drain regions. Usually overlapping is avoided. But because of insufficient gate overlap to the source/drain junction the inversion layer is formed within the range y as shown in fig.1.7, due to the perpendicular electric field created by the gate voltage. Therefore n^+p junctions are formed at the source and drain

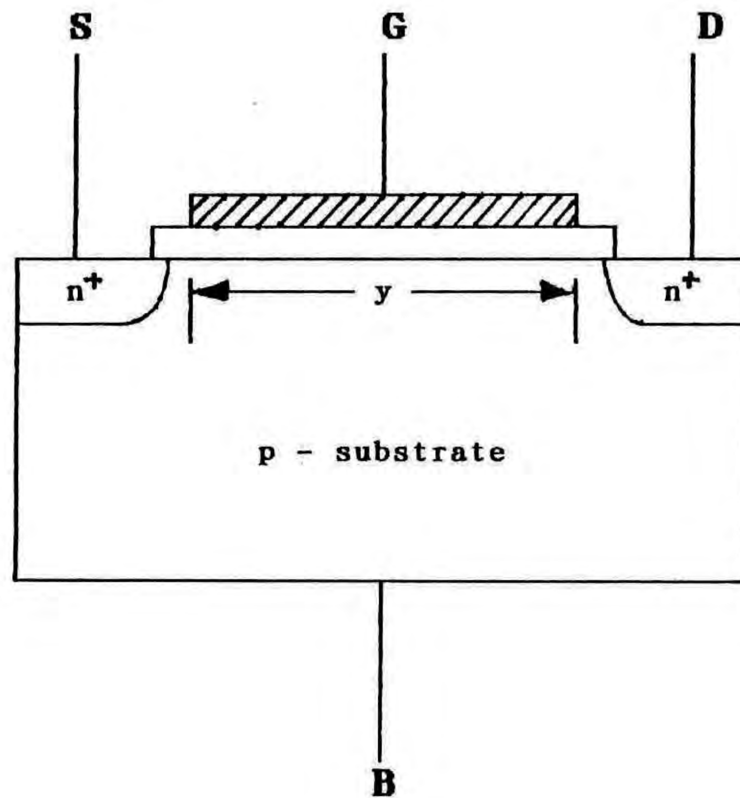

Fig.1.7 Insufficient gate overlap to the source and drain junctions.

junctions with channel. These $n^{+}p$ junctions can be assumed as the metal semiconductor junctions if the source and drain dopings are very high. Hence built-in potentials create at the source and drain junctions.

1.7 Isolation process and formation of bird's beak

Since a low value of V_T is usually desired, a thin oxide layer is used to gate region to increase the gate capacitance. Although a low threshold voltage is desired in the gate region of a transistor, a large value of V_T is needed between devices. For example, if several transistors are interconnected on a single silicon chip, we do not want inversion layers to be formed inadvertently between the devices. Therefore junction isolation is used as shown in the fig.1.8, to avoid this situation.

A disadvantage of the junction isolation method is the capacitance inherent at the isolating p-n junctions. The capacitance associated with the sidewalls between n region and the diffused junctions can be eliminated by the use of oxide isolation configurations, shown in the fig.1.9. The oxide isolation takes advantage of the fact that silicon nitride can be used to mask the underlying silicon against the oxidation. The area that contains the transistor is covered with Si_3N_4. By oxidation process, SiO_2 grows in the areas not protected by the nitride.

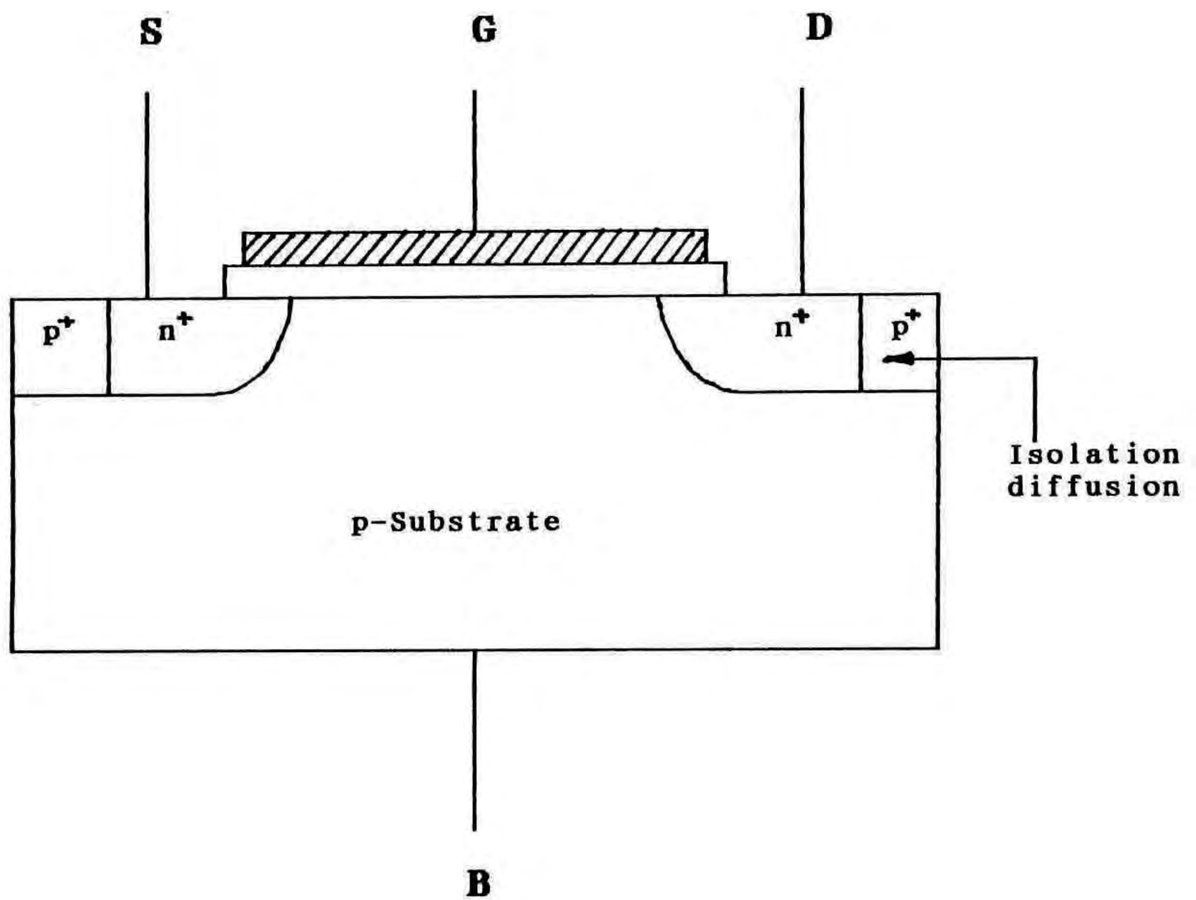

Fig.1.8 Junction isolation of MOSFET by semiconductor.

When the oxidation takes place near the edge of the nitride mask, there is intrusion of oxidation laterally under the nitride. As a result, SiO_2 is pushed up slightly, forming an irregular surface resembling a bird's beak as shown in fig.1.9 Because of positive induced charge at the bottom layer of bird's beak, the electron concentration is increased at the drain junction, which is the minority carrier of p-substrate. Hence $n^{++}p$ junction is formed at the drain-channel surface. This junction can be considered as Schottky junction.

1.8 Hot electron effects of short channel device

As the drain depletion region continues to increase with reverse bias, it can actually interact with the source-to-channel junction and lower the potential barrier. This problem is known as drain-induced barrier lowering (DIBL). When the source junction barrier is reduced, electrons can easily inject into the channel and the gate voltage no longer has control of the drain current.

Electric field tends to be increased at small geometries as device voltages are difficult to scale to arbitrary small values. As a result, various short carrier effects appear in short-channel devices. The field in the reverse biased drain junction can lead to impact ionization and carrier multiplication. The resulting holes contribute to the substrate current and some may move to the source, where they lower the source barrier and results in electrons injected from the source into the p-region. In fact, n-p-n transistor

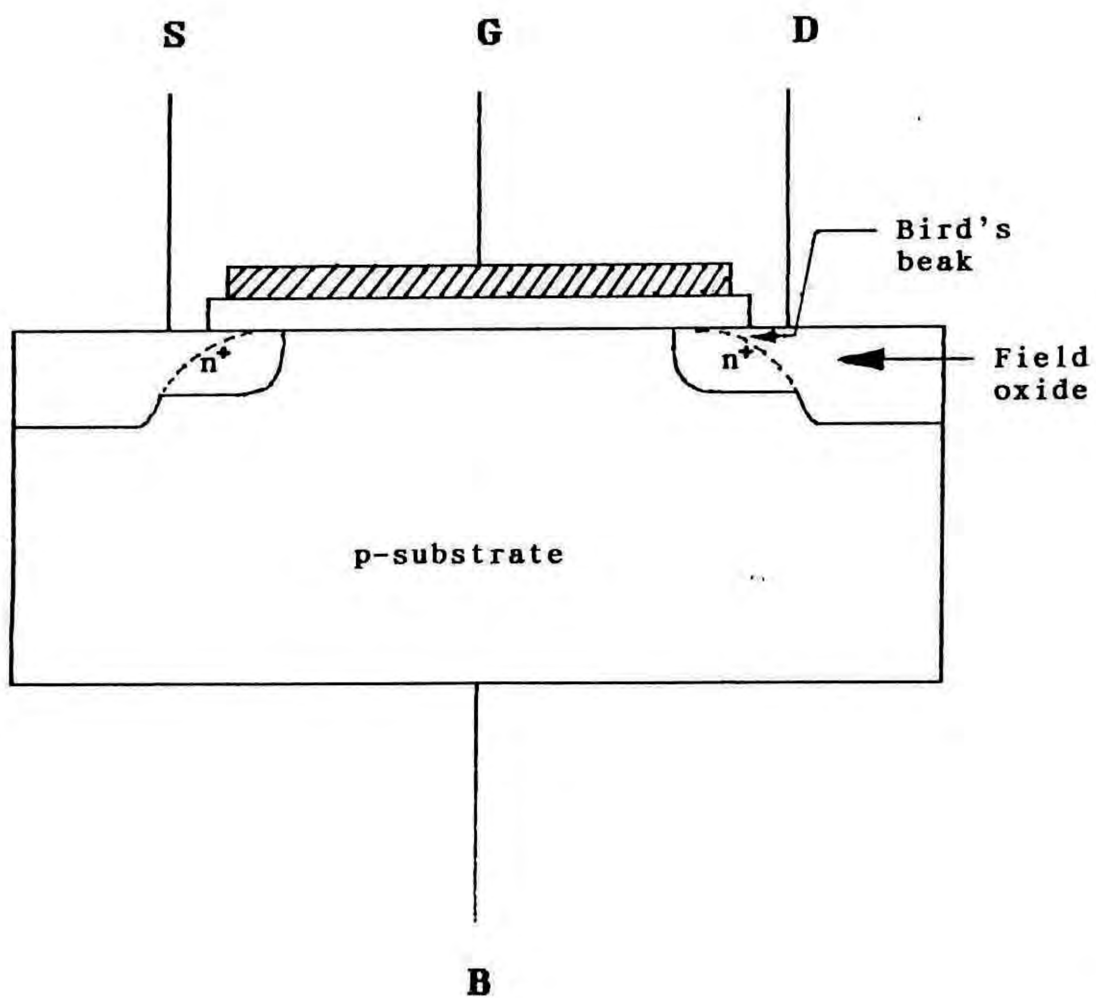

Fig.1.9 Oxide isolation of MOSFET by field oxide.

action can result within the source-channel-drain configuration and prevent gate control of the current.

Another hot electron effect is the transport of energetic electrons over the barrier into the oxide. Some electrons can be trapped in the oxide, where they change the threshold voltage and the I-V characteristics of the device.

1.9 LDD and sidewall spacer and the formation of potential barrier

Hot electron effects can be reduced by reducing the doping in the source and drain regions, so that the junction fields are smaller. However, lightly doped source and drain regions are incompatible with small geometry devices because of contact resistance. A compromise design called the lightly doped drain (LDD) uses two doping levels, with heavy doping over most of the source and drain areas but with light doping in a region adjacent to the channel as shown in the fig.1.10. The LDD structure decreases the field between the drain and channel regions, thereby reducing carrier injection into the oxide, impact ionization and other hot electron effects. An important aspect of LDD fabrication is the use of sidewall spacers on each side of the gate. The sidewall spacers serve as a mask for the n-type implant. The high dose n^+ implant is driven by the diffusion process.

Since it is very important to decrease the series resistance of the gate and the source and drain regions for

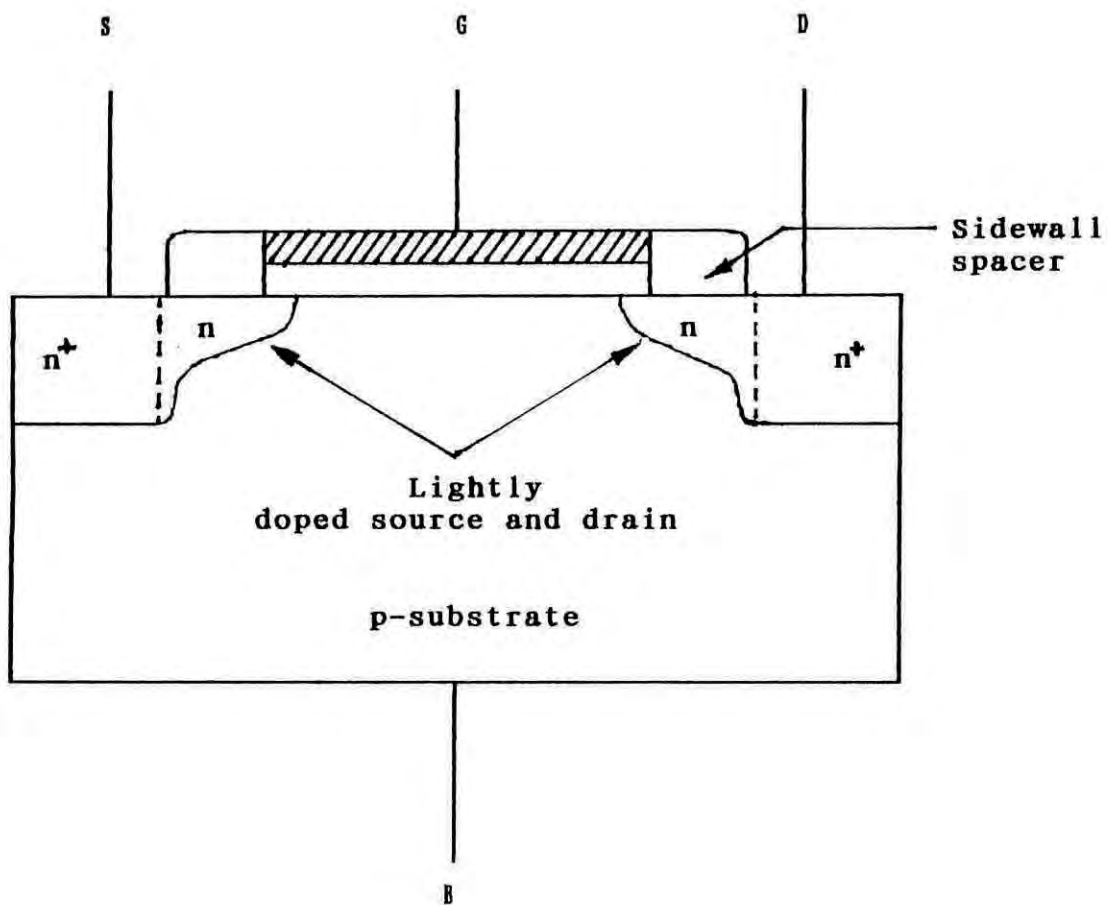

Fig.1.10 The lightly doped drain (LDD) structure of MOSFET.

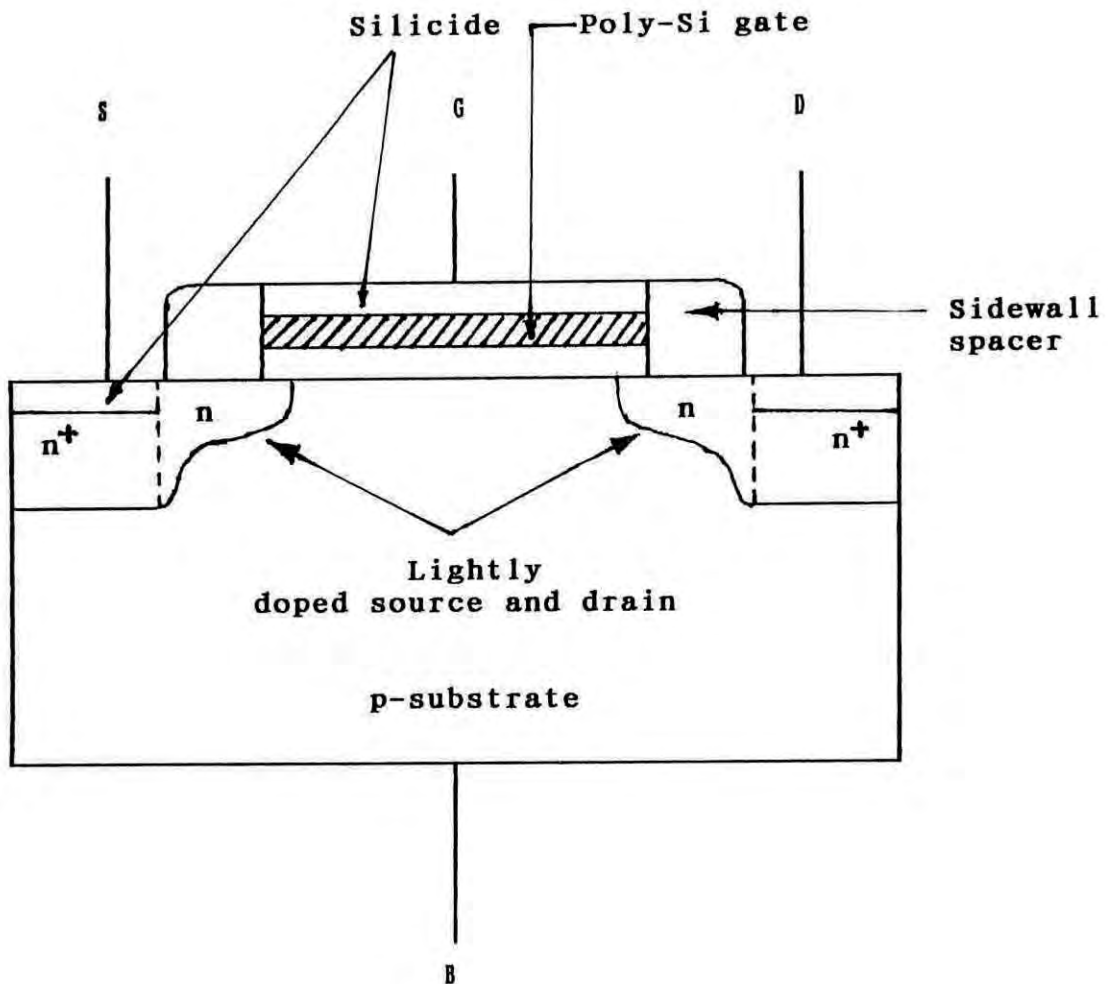

Fig.1.11 MOS transistor with silicidation.

small geometry devices, several techniques have been developed to improve the contact resistance. This is important not only because the area of these regions decrease with smaller geometries, but also because shallower source and drain (LDD) junctions are necessary as the device is scaled down, resulting in higher resistance regions. One way to reduce the resistance of the source and drain regions and also the polysilicon gate region, is to use a refractory metal silicide to contact these regions. In fig.1.11 the source-drain implant and sidewall spacer steps are followed by the formation of a silicide simultaneously in the source, drain and polysilicon gate regions. In this process a thin layer of refractory metal is deposited and heated to form silicide wherever it touches exposed silicon. The normally used silicide materials are PtSi, $MoSi_2$, $CoSi_2$ and $TiSi_2$. During silicidation, dopants in silicon surrounding the refractory metal diffuse to and segregate into and at the interface of the silicide layer. A thin lightly doped region may exist in the silicon near the boundary of the silicide. Therefore, the doping density at the LDD region of a salicide LDD MOS transistor is further reduced by the salicide process. A potential barrier may exist at the LDD region of a salicide LDD MOS transistor.

1.10 Reverse short-channel effect

The threshold voltage for long-channel MOSFET is independent of the channel length of the device. For short-channel MOS device the threshold voltage decreases as the channel length of the device is decreased. But it is found

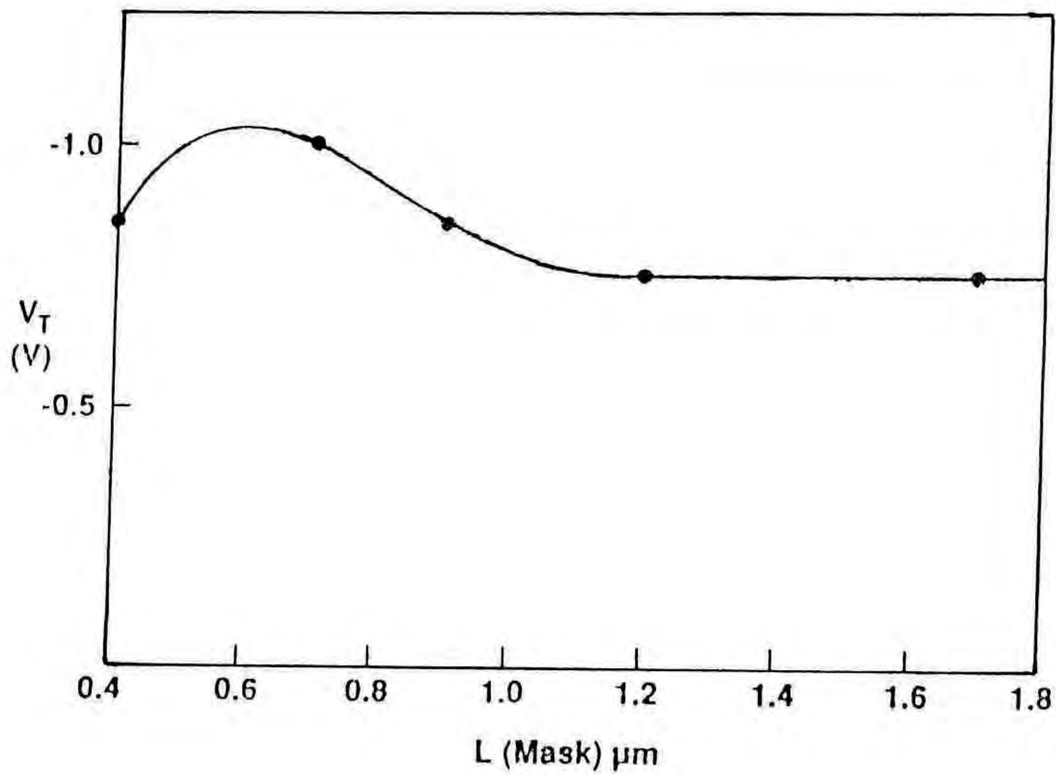

Fig.1.12 Threshold voltage vs channel length of p-channel MOS transistor with "reverse short-channel effect" [4].

that the threshold voltage of sub-micron MOS transistor at the beginning increases with decreasing channel length, then drastically decreases of the device [4]. This is known as the reverse short-channel effect. The reverse short-channel effect occurs when there is a potential barrier at the boundary of the channel to the source and drain junctions. This potential barriers due to the insufficient gate overlap to the source and drain junctions, a large "bird's beak" at the edge of the gate polysilicon, a very lightly doped region at the edge of the source/drain junction, or heavy doping at the edge of channel by halo-ion implantation [4]. Due to the potential barrier at the source/drain junction the performance of the MOS transistor degrades from the normal behaviour. The variation of the threshold voltage with channel length of the MOS device is shown in (Fig. 1.12) taken from the literature [4].

1.11 Objective of this work

The main objective of this work is to give a mathematical model of drain current and transconductance considering reverse short-channel effect due to potential barrier at the source/drain junction. The variation of characteristic curves from normal behaviour of MOSFET has also been shown. Moreover, this theoretical result has been compared with the experimental one [4]. Finally the characteristics of long-channel MOS transistor have been derived from proposed short-channel device analysis.

1.12 Summary of the thesis

Various methods have been developed to determine the I-V characteristics of short-channel MOSFETs. But due to anomalous threshold voltage behaviour of sub-micron MOSFETs the characteristic curves also differ from the normal characteristics. No analytical model has been developed so far which can explain the drain current and the transconductance versus gate-voltage characteristics of short-channel length MOS transistors considering reverse short channel effect.

In chapter 2, the mathematical modelling for I-V and G_m-V characteristics equations have been developed by considering barrier potential and the voltage drop due to series resistance at the source and the drain junctions of the device. This chapter also describes the behaviour of short-channel MOS transistor considering variation of mobility with gate voltage. The barrier potential depends on the gate voltage, hence diverts the threshold voltage of the device. Finally in this chapter the characteristics of long-channel device have been modeled from that of short-channel device.

In chapter 3 results of the analytical model of chapter 2 are given. Comparison with the experimental results available in the literature [4] also have been shown in this chapter.

The final chapter contains the concluding remarks along with recommendations for further works on this topic.

CHAPTER 2

MATHEMATICAL ANALYSIS FOR I-V CHARACTERISTICS OF MOSFETs CONSIDERING REVERSE SHORT-CHANNEL EFFECT.

2.1 Introduction

Several models have been reported to describe the I-V characteristics of MOSFETs [6-8]. For a short-channel MOSFET the potential barrier arises at the channel-drain and channel-source junctions. Due to these barriers the characteristics curve deviates from those without potential barrier.The threshold voltage of short-channel device increases with the decrease of channel length and then drastically decreases. The above phenomena is known as reverse short-channel effect.

When the gate has no overlap to the source and/or drain junctions, or a very large channel oxide bird's beak, or a very high dose shallow halo-ion implantation, or the source and drain doping density at the edge of the channel is too low due to either a very low dose of LDD ion implantation or due to channel diffusion of dopants by oxidation or salicidation, a potential barrier exists at the boundary of the source and/or drain to the surface channel. The characteristics analysis has also been done by considering the mobility

reduction factor. The dependence of channel current in subthreshold operation upon drain, source and substrate voltage has been formulated in terms of simple model considering the barrier potential.

2.2 Potential barrier of a Schottky diode

The work function $q\phi_m$ of a metal is defined as the energy required to remove an electron at the Fermi level to the vacuum outside the metal. When a metal with work function $q\phi_m$ is brought in contact with a semiconductor having a work function $q\phi_s$, charge transfer occurs until the Fermi levels align at equilibrium (Fig-2.1). For example when $\phi_m > \phi_s$, the semiconductor Fermi level is initially higher than that of the metal before contact is made. To align the two Fermi levels, the electrostatic potential of the semiconductor must be raised (i.e. the electron energy must be lowered) relative to that of metal. In the n-type semiconductor of Fig-2.1, a depletion region w is formed near the junction. The positive charge due to uncompensated donar ions within w matches the negative charge on the metal.

The equilibrium contact potential V_o, which prevents further net electron diffusion from the semiconductor band into the metal, is the difference in work function potential $\phi_m - \phi_s$. The potential barrier height V_B for electron injection from the metal into the semiconductor conduction band is $\phi_m - X$, where qX (called the electron affinity) is measured from the vacuum level to the semiconductor conduction band edge. The

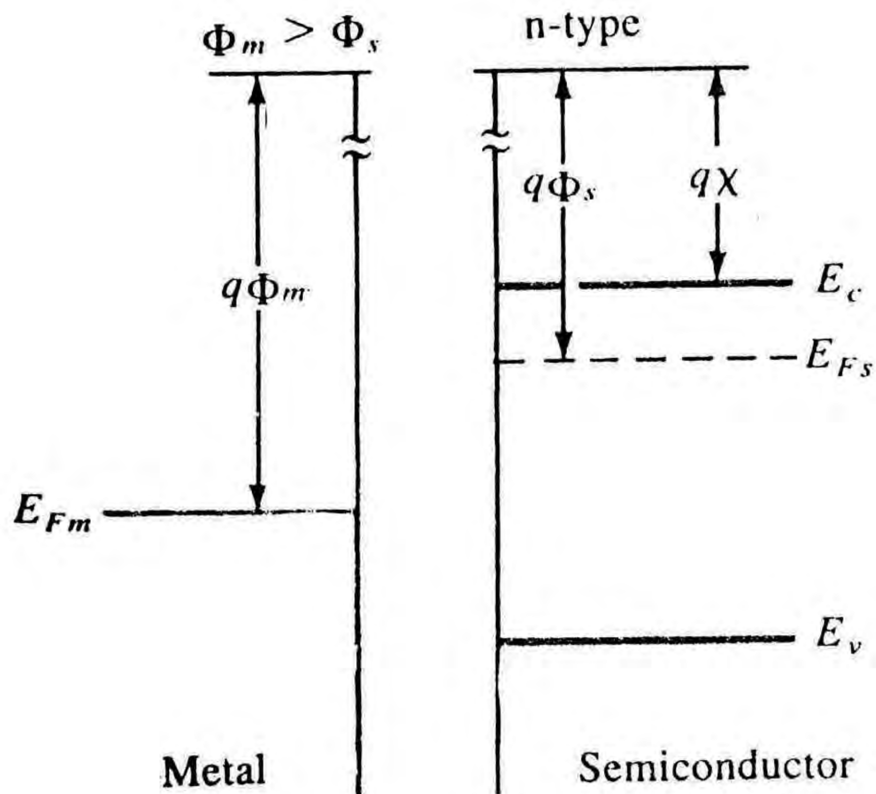

Fig.2.1 Band diagram of Schottky barrier formed by metal-semiconductor before joining.

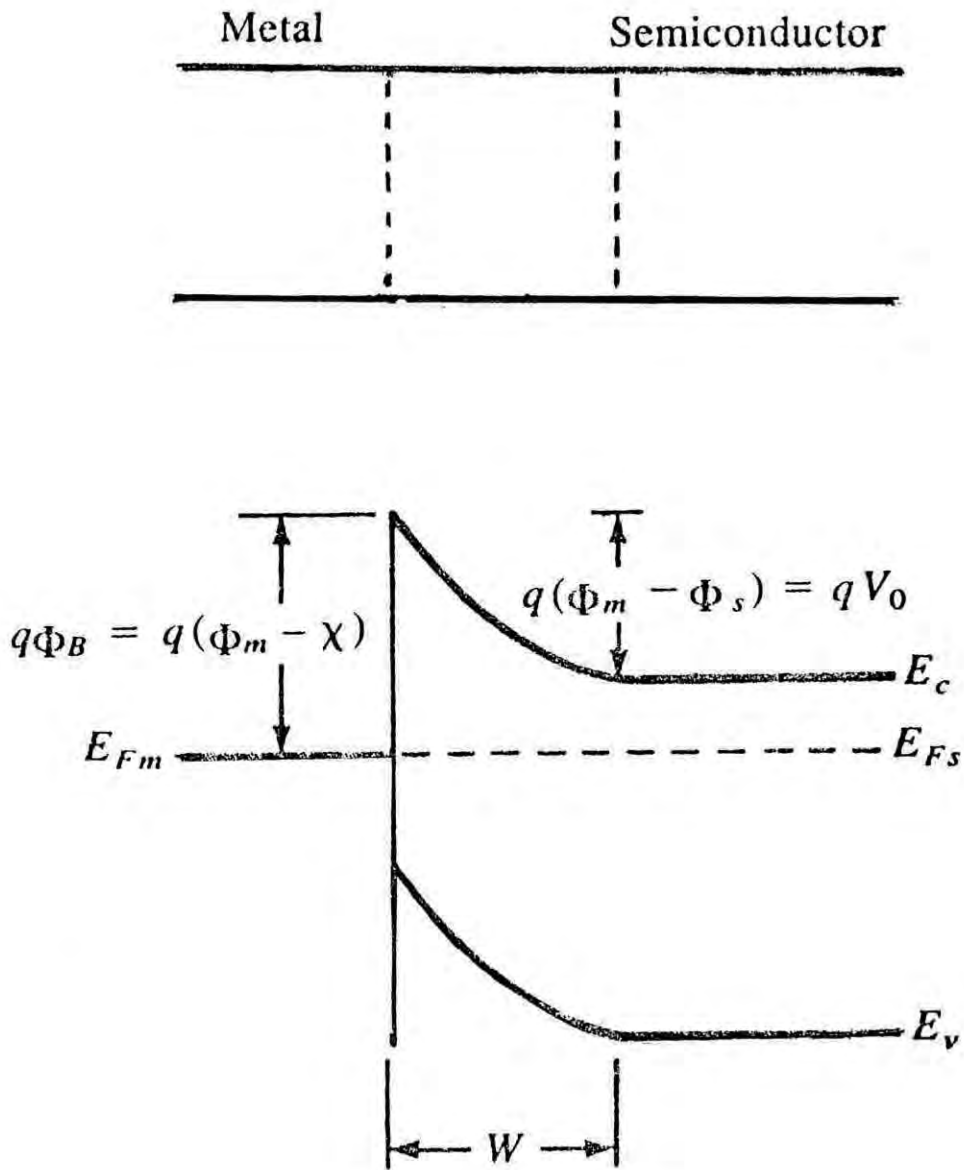

Fig.2.2 Equilibrium band diagram for metal-semiconductor junction.

equilibrium potential difference V_o can be decreased or increased by the application of either forward or reverse-bias voltage, as in the p-n junction.

When a forward bias voltage V is applied to the Schottky barrier of Fig-2.2 the contact potential is reduced from V to (V_o-V) (Fig-2.3). As a result, electrons in the semiconductor conduction band can diffuse across the depletion region to the metal. This gives rise to a forward current (metal to semiconductor) through the junction. Conversely, a reverse bias increases the barrier to (V_o+V_r) (Fig. 2.4) and electrons flow from semiconductor to metal becomes negligible. In either case, flow of electrons from the metal to the semiconductor is retarded by the barrier $\phi_m-\chi$. The resulting diode equation is similar in form to that of the p-n junction [3,4] and is given by,

$$I=I_0 e^{-\frac{V_B}{V_t}}(e^{\frac{V}{V_t}}-1) \quad (2\cdot1)$$

where, I_0 is the saturation current, V_B is the barrier potential, V is the applied voltage and

$$V_t=\frac{kT}{q} \quad (2.2)$$

at room temperature V_t is equal to 0.0259.

The equation (2.1) represents the current passing through the Schottky barrier.

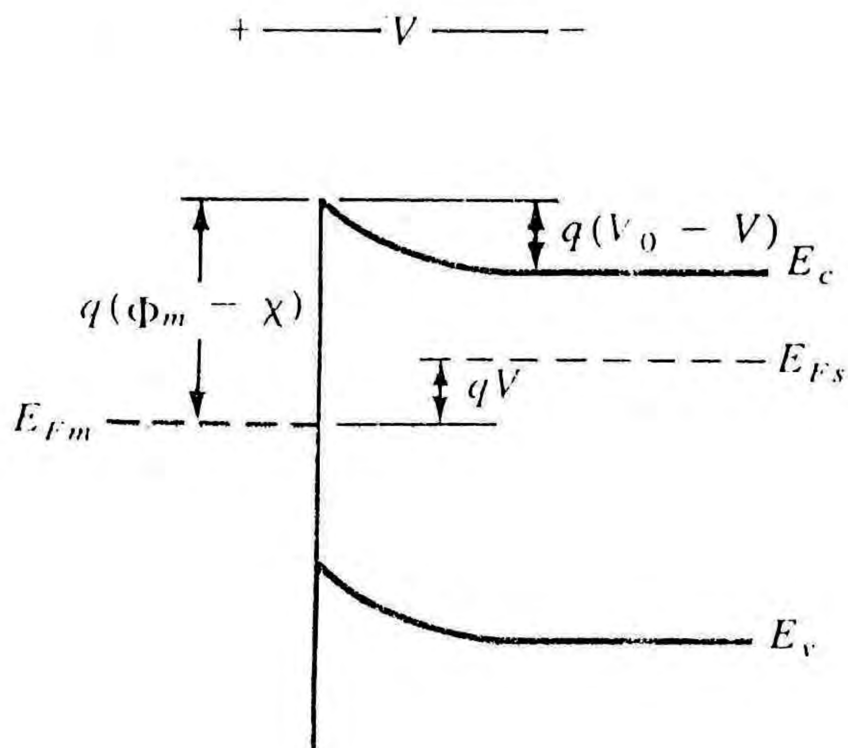

Fig.2.3 Band diagram for metal-semiconductor junction at forward biased condition.

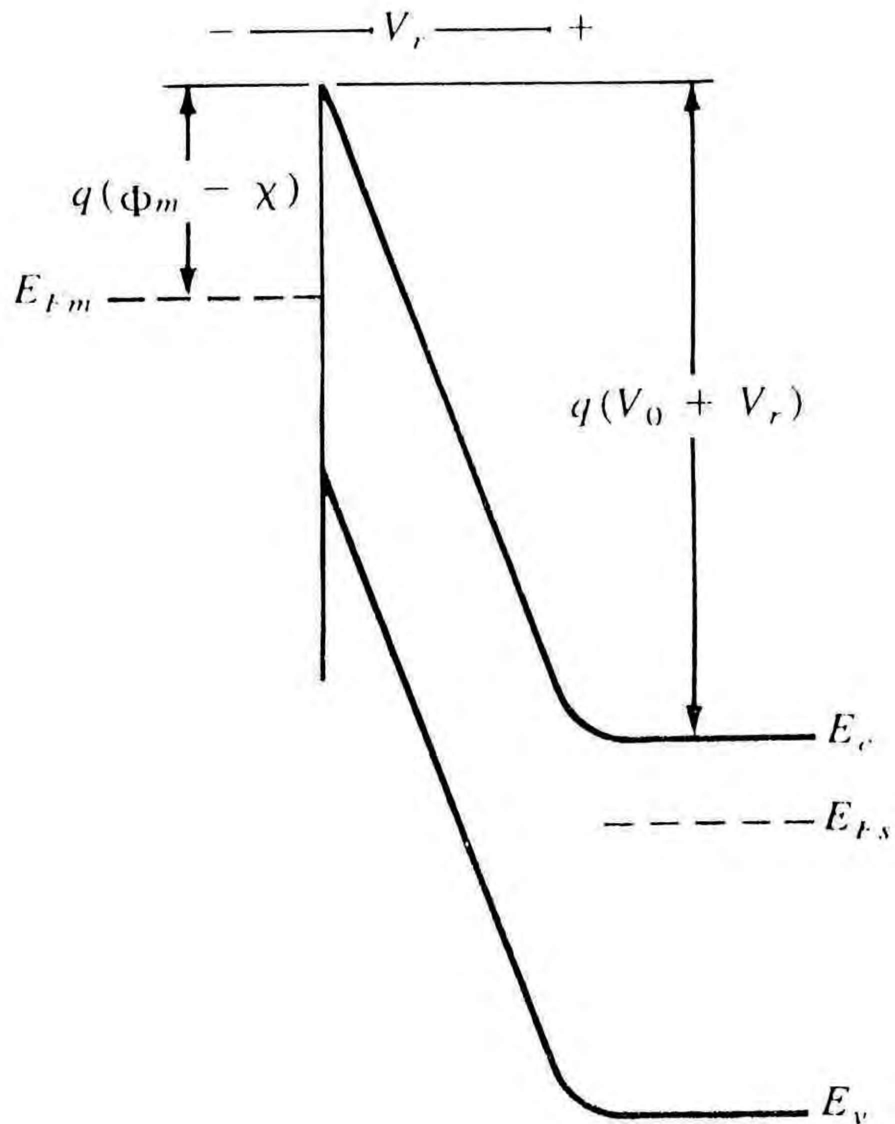

Fig.2.4 Band diagram for metal-semiconductor junction at reverse biased condition.

2.3 Analysis

The models for drain current and transconductance characteristics have been developed in this section .

2.3.1 Drain current and transconductance considering barrier potential and drain/source series resistance.

The current I, flow over the potential barrier is given in equation (2.1). For $V>V_t$, this equation reduces to

$$I \approx \frac{I_0 V}{V_t} e^{-\frac{V_B}{V_t}} \tag{2.3}$$

On the assumption that the effective mobility of conducting channel is independent of the gate-bias voltage, the drain current I_D is given by [2]

$$I_D = K\left(V_G - V_T - \frac{V_C}{2}\right) V_C \tag{2.4}$$

where,

$$K = \frac{w \mu C_O}{L} \tag{2.5}$$

μ is the effective surface mobility, C_o is the unit area gate-oxide capacitance, w and L are the effective channel width and length of the device respectively, V_T is the threshold voltage and V_C is the voltage drop across the surface conduction channel. If the sum of the series resistances at the source and drain junctions is R and V_R is the voltage drop across the

series resistance, the drain voltage V_D can be written as

$$V_D = 2V + V_C + V_R \tag{2.6}$$

using the equations (2.3) and (2.4) we can write,

$$V_D = \frac{2I_D V_t}{I_0 e^{-\frac{V_B}{V_t}}} + \frac{I_D}{K(V_G - V_T - 0.5V_C)} + I_D R \tag{2.7}$$

where, $V_D = I_D R$.

Assuming $(V_G - V_T) \gg V_C$

$$V_D \approx \frac{2I_D V_t}{I_0 e^{-\frac{V_B}{V_t}}} + \frac{I_D}{K(V_G - V_T)} + I_D R \tag{2.8}$$

Rearranging the equation (2.8), it can be shown,

$$I_D = \frac{KV_D(V_G - V_T)}{1 + \frac{2KV_t(V_G - V_T)}{I_0 e^{-\frac{V_B}{V_t}}} + KR(V_G - V_T)} \tag{2.9}$$

The numerator of equation (2.9) is the channel current of the device without a potential barrier. The denominator is the current reduction factor by the potential barrier and the series resistance of the device. The factor 2 at the denominator is due to the potential barrier at both drain and source junctions.

Let us write the equation (2.5) as,

$$K=\frac{A}{L} \tag{2.10}$$

where, $A=w\mu C_o$

Therefore, combining equations (2.9) and (2.10) we can get,

$$I_D=\frac{AV_D(V_G-V_T)}{L+\frac{2AV_t(V_G-V_T)}{I_o e^{-\frac{V_B}{V_t}}}+AR(V_G-V_T)} \tag{2.11}$$

For short-channel devices, the second and third terms of the denominator of equation (2.11) dominates on the 1st factor. Hence the potential barrier and series resistance of short-channel devices reduce the drain current. For long-channel MOSFETs the second and third terms of the denominator become negligible compared to the 1st term. So for long-channel devices the potential barrier have small effect on drain current. Therefore for long-channel device the drain current can be represented as

$$I_D\approx\frac{w\mu C_o V_D}{L}(V_G-V_T) \tag{2.12}$$

From equation (2.9) transconductance of the MOS transistor operated in the linear region can be derived as

$$G_m=\frac{dI_D}{dV_G} \tag{2.13}$$

$$=\frac{KV_D[1-\frac{2V_B'K(V_G-V_T)^2}{I_O e^{-\frac{V_B}{V_t}}}]}{[1+KR(V_G-V_T)+\frac{2KV_t(V_G-V_T)}{I_O e^{-\frac{V_B}{V_t}}}]^2} \tag{2.14}$$

where V_B' is the first derivative of the potential barrier height with respect to the gate voltage. If there is no potential barrier and no series resistance the transconductance reduces to,

$$G_m=KV_D=\frac{w\mu C_O}{L}V_D \tag{2.15}$$

and is predicted by the simple depletion model of MOS transistor theory. The above expression represents the transconductance of long-channel MOSFETs. Because for long channel devices the second and third terms of the denominator of equation (2.14) are negligible compared to the first term. But in case of short- channel devices, the second and third terms dominates over the first term. So, barrier potential and series resistance affects on the transconductance of short-channel MOSFETs.

The denominator of equation (2.14) is the square of equation (2.9). The device is expected to have a very small transconductance, particularly at low gate biases.

2.3.2 Drain current and conductance considering mobility reduction factor

The equations (2.9) and (2.14) are derived assuming constant effective mobility. Mobility reduction is caused by the transverse field influencing the mobility of the carriers. The expression which models mobility reduction [6] is

$$\mu_1=\frac{\mu}{1+\theta(V_G-V_T)} \qquad (2.16)$$

where, μ is the mobility at the threshold voltage and θ is the mobility reduction factor.

Defining the factor K_1 as,

$$K_1=\frac{w\mu C_0}{L[1+\theta(V_G-V_T)]} \qquad (2.17)$$

combining equations (2.5) and (2.17) we have

$$K_1=\frac{K}{[1+\theta(V_G-V_T)]} \qquad (2.18)$$

From the equations (2.3) and (2.18) we can write the drain current expression as,

$$I_D=\frac{K(V_G-V_T-0.5V_C)V_C}{1+\theta(V_G-V_T)} \qquad (2.19)$$

using the equations (2.3), (2.6) and (2.19) the drain to source voltage can be written as,

$$V_D=\frac{2I_DV_t}{I_0e^{-\frac{V_B}{V_t}}}+\frac{I_D[1+\theta(V_G-V_T)]}{K(V_G-V_T)}+I_DR \qquad (2.20)$$

the expression for I_D can be obtained from equation (2.20) and can be written as,

$$I_D=\frac{\frac{V_DK(V_G-V_T)}{1+\theta(V_G-V_T)}}{1+\frac{KR(V_G-V_T)}{1+\theta(V_G-V_T)}+\frac{2V_tK(V_G-V_T)}{I_0e^{-\frac{V_B}{V_t}}[1+\theta(V_G-V_T)]}} \qquad (2.21)$$

The denominator of equation (2.21) is the current reduction factor by the potential barrier and series resistance. If there is no potential barrier and neglecting the drop across the series resistance the drain current expression is

$$I_D=\frac{KV_D(V_G-V_T)}{1+\theta(V_G-V_t)} \qquad (2.22)$$

and this is the drain current expression for long-channel devices.

The expression for transconductance which is defined as $G_m=dI_C/dV_G$, can be derived as,

$$G_m = \frac{\frac{KV_D}{[1+\theta(V_G-V_T)]^2}\left[1-\frac{2KV_B(V_G-V_T)^2}{I_0 e^{-\frac{V_B}{V_t}}}\right]}{\left[1+\frac{KR(V_G-V_T)}{1+\theta(V_G-V_T)}+\frac{2V_tK(V_G-V_T)}{I_0 e^{-\frac{V_B}{V_t}}[1+\theta(V_G-V_T)]}\right]^2} \tag{2.23}$$

If there is no potential barrier and neglecting the series resistance drop, the transconductance can be written as

$$G_m = \frac{KV_D}{[1+\theta(V_G-V_T)]^2} \tag{2.24}$$

The above equation represents the transconductance for long-channel devices.

2.3.3 Drain current and transconductance in subthreshold region

The drain current in the subthreshold region is given by [5]

$$I_D = KV_t^2(n-1)(1-e^{-\frac{V_c}{V_t}})\,e^{\frac{(V_G-V_T)}{nV_t}} \tag{2.25}$$

where,

$$n=1+\frac{\gamma}{2\sqrt{(2\Phi_f-V_{BS})}} \qquad (2.26)$$

and

$$\gamma=\frac{\sqrt{2q\epsilon_s N_A}}{C_O} \qquad (2.27)$$

Rearranging the equation (2.25) we can have,

$$V_c=-V_t \ln[1-\frac{I_D e^{\frac{(V_T-V_G)}{nV_t}}}{KV_t^2(n-1)}] \qquad (2.28)$$

considering the second term of logarithm in equation (2.28) less of unity the above equation can be approximated as,

$$V_c \approx \frac{I_D e^{\frac{(V_T-V_G)}{nV_t}}}{K(n-1)V_t} \qquad (2.29)$$

Using the equations (2.3), (2.6) and (2.29) the expression for drain voltage V_D can be represented as

$$V_D=\frac{2I_D V_t}{I_0 e^{-\frac{V_s}{V_t}}}+\frac{I_D e^{\frac{(V_T-V_G)}{nV_t}}}{KV_t(n-1)}+I_D R \qquad (2.30)$$

Rearranging the equation (2.30) we can have,

$$I_D=\frac{\dfrac{KV_tV_D(n-1)}{e^{\frac{(V_T-V_G)}{nV_t}}}}{1+\dfrac{KRV_t(n-1)}{e^{\frac{(V_T-V_G)}{nV_t}}}+\dfrac{2KV_t^2(n-1)}{I_0e^{-\frac{V_B}{V_t}+\frac{(V_T-V_G)}{nV_t}}}} \qquad (2.31)$$

The denominator of the above equation is the current reduction factor due to potential barrier and series resistance. If there is no potential barrier and neglecting the drop across series resistance, the drain current can be expressed as,

$$I_D=\frac{KV_tV_D(n-1)}{e^{(V_T-V_G)}} \qquad (2.32)$$

which is same as the drain current for long-channel device.

The expression for transconductance which is defined as $G_m = dI_D/dV_G$, can be derived from equation (2.31) as,

$$G_m=\frac{\dfrac{KV_D(n-1)}{ne^{\frac{(V_T-V_G)}{nV_t}}}\left[1-\dfrac{2KV_t^2V_B'n(n-1)}{I_0e^{-\frac{V_B}{V_t}+\frac{V_T-V_G}{nV_t}}}\right]}{\left[1+\dfrac{KRV_t(n-1)}{e^{\frac{(V_T-V_G)}{nV_t}}}+\dfrac{2KV_t^2(n-1)}{I_0e^{-\frac{V_B}{V_t}+\frac{V_T-V_G}{nV_t}}}\right]^2} \qquad (2.33)$$

If there is no potential barrier and neglecting the drop across the series resistance we can have the conductance

$$G_m=\frac{K(n-1)\,V_D}{ne^{\frac{V_T-V_G}{nV_t}}} \qquad (2.34)$$

which is the expression of conductance for long-channel device.

2.4 Conclusion

The expressions for drain current and transconductance are derived in active region considering barrier potential and series resistance with and without considering mobility reduction factor. The drain current and conductance are also derived in the subthreshold region. So we can get the characteristics curves both in subthreshold and active regions.

CHAPTER 3

RESULTS AND DISCUSSIONS

3.1 Introduction

The output characteristics (I-V) and transconductance of a device can be determined by its physical parameters like substrate doping, channel length, oxide thickness etc. using the models derived in chapter 2. The characteristics curves have been drawn by considering the barrier potentials at the source and drain junctions and the series resistance at the source/drain junction. This result has been compared with the results obtained without considering any potential barrier. It has been shown in the characteristic curves that the potential barrier can strongly degrade the performance of MOS transistor. The results obtained from mathematical models developed in the previous chapter have also been compared with the experimental results taken from a literature [4]. As the experiment was based on a p-channel device, the analysis in this paper is also on p-channel MOSFET. The theoretical results are in good agreement with the experimental data.The characteristics curves obtained in the subthreshold region have also been added with that in the active region. So this model gives the exact characteristics of short channel MOS transistor. However all the physical measurements of MOS device have been taken from the literature [4].

3.2 Output characteristics and transconductance

The analytical models developed in chapter 2 have been used to find various characteristics of a short-channel MOSFET considering barrier potential and series resistance. The analysis is done on the p-channel device. The channel length of the device is 0.5μm, channel width is 10μm and the gate oxide thickness is 12nm. The drain bias voltage is -0.1V, effective mobility is 200cm²/Vs, I_O=1mA, $V_B/V_t=7.7-1.2V_G^{-3}+1.3V_G^{-2}+0.6V_G$ and θ=0.04. This corresponds to have conduction channel depth of 1nm and threshold voltage of 0.57eV.

3.2.1 Drain current as a function of substrate doping

Drain current of a MOS device varies as the doping level of the substrate is varied. Equation (2.9) has been plotted in Fig. 3.1 for two different levels of substrate doping. In higher doping level of substrate, drain current decreases with constant gate voltage. However, if the barrier potential V_B=0, the drain current increases rapidly with constant doping density and gate voltage. Hence barrier potential decreases the drain current level. The decrease of drain current in higher doping of substrate can be explained by equation (2.9). From equation (1.10) we can see that with the increase of substrate doping, the threshold voltage increases. With this increased threshold voltage, equation (2.9) gives the decreasing drain current level. Again because of barrier potential the denominator of equation (2.9) increases for a

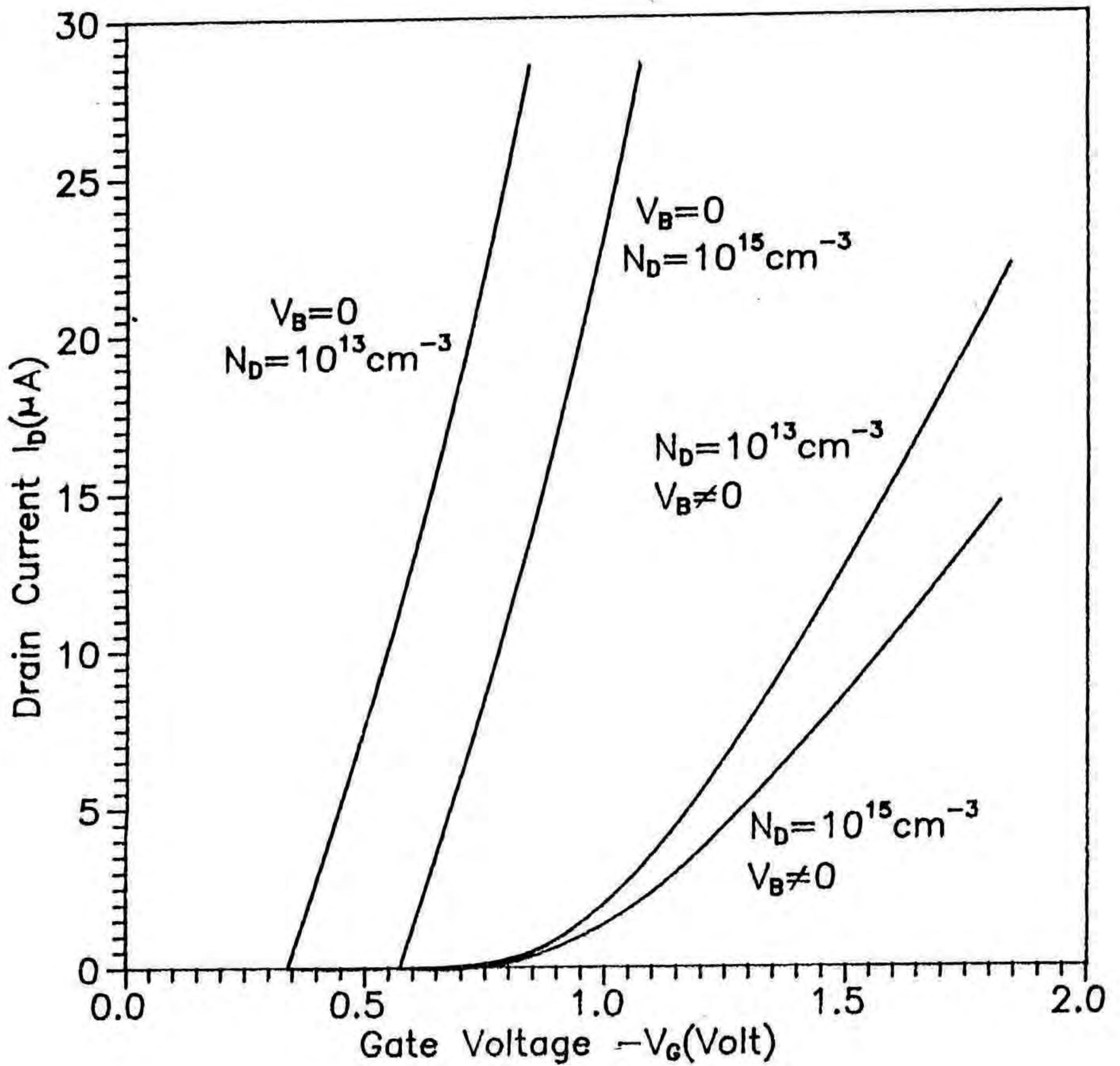

Fig.3.1 Drain current vs gate voltage considering different substrate doping.

increase of barrier potential.

3.2.2 Conductance as a function of substrate doping

The variation of conductivity with substrate doping has been shown in Fig. 3.2. A negligible variation of transconductance occurs with substrate doping. As the doping level of substrate is changed, the threshold voltage also changes as shown in equation (1.10). Also from equation (2.14) we can see that both the numerator and denominator have square terms. Therefore, the rate of change of both the numerator and denominator are approximately same with the change of threshold voltage. Both the terms increase or decrease with the increase or decrease of substrate doping respectively. Hence the substrate doping has no such effects on the transconductance of MOS device.

3.2.3 Drain current as a function of series resistance

Equation (2.9) has been plotted in Fig-3.3, which shows the drain current characteristics for two different series resistances of 955 ohms and 0 ohm considering potential barrier that is also a function of gate voltage. As the series resistance increases, the denominator of equation (2.9) increases. So the drain current decreases with this increasing series resistance for fixed gate voltage and potential barrier. Therefore, we can say that drain current is inversely proportional to the series resistance.

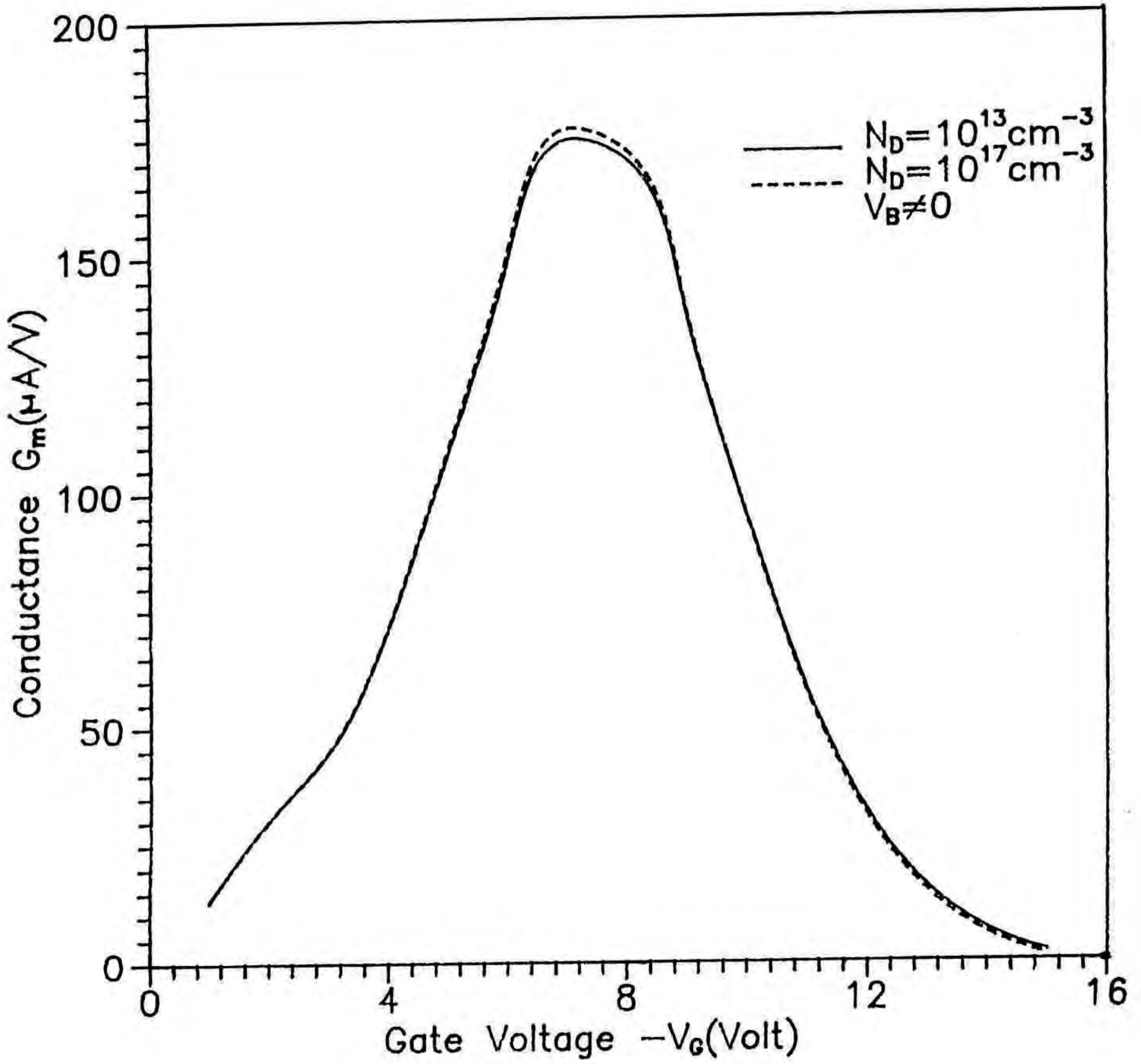

Fig.3.2 Transconductance vs gate voltage considering different substrate doping.

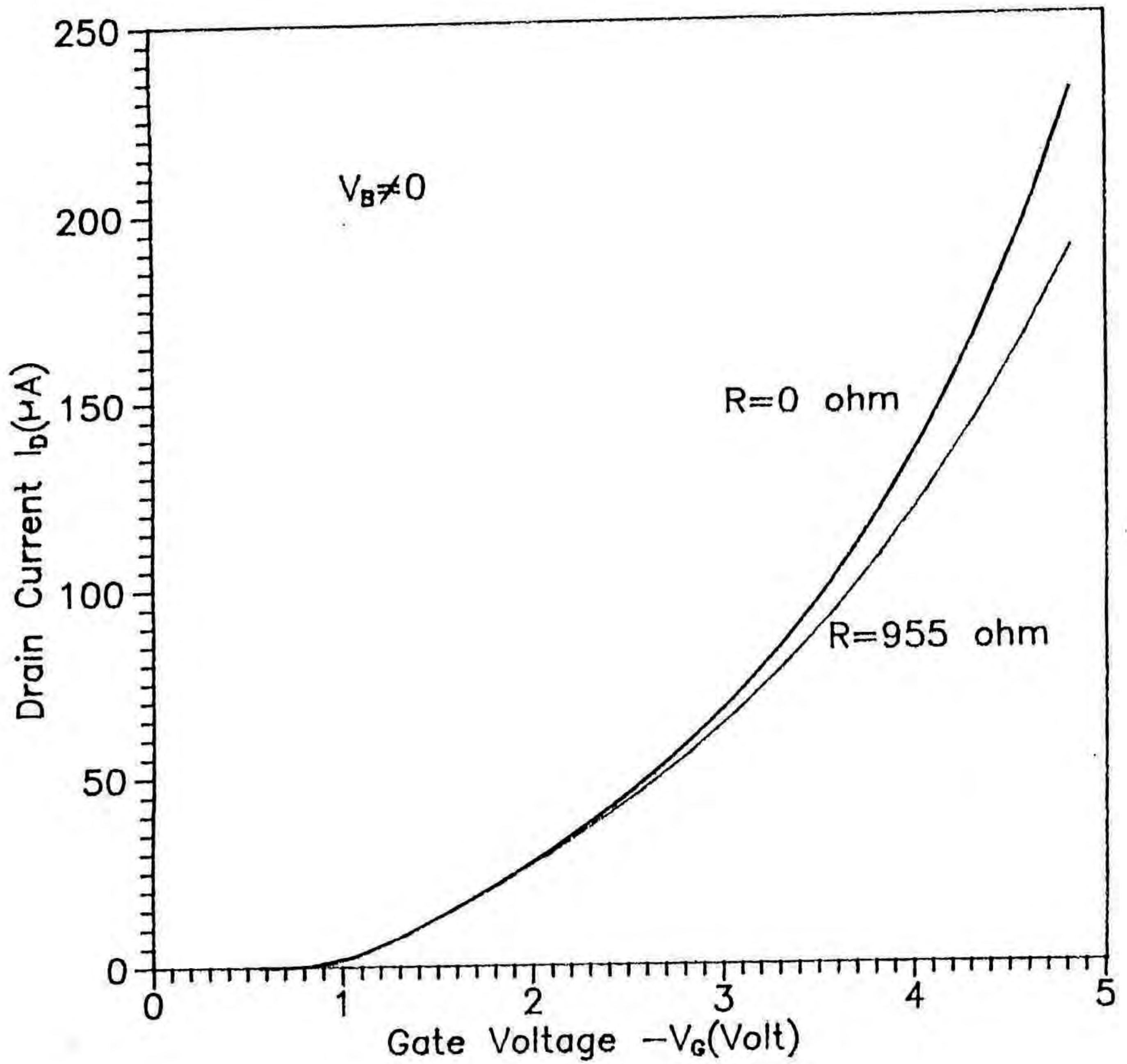

Fig.3.3 Drain current vs gate voltage considering different series resistances.

3.2.4 Conductance as a function of series resistance

Series resistances between source/drain and channel greatly affects the conductivity of the channel. The variation is shown in Fig-3.4. This characteristics can be explained by equation (2.14). As the series resistance terms appear at the denominator of this equation, so transconductance decreases with the increase of resistance for constant barrier potential and gate voltage.

3.2.5 Conductance as a function of potential barrier

Fig-3.5 shows the variation of channel conductivity with respect to potential barrier. Equation (2.14) explains this variation. If there is no potential barrier, the second term of numerator is equal to zero. Therefore the conductance decreases with the increase of gate voltage, as the gate voltage terms appear at the denominator. The variation is not linear, because of square at the denominator.

Equation (2.14) shows that conductance decreases with the increase of gate voltage. Also from the literature [4] with the increase of gate voltage, V_B increases whereas V_B' decreases. At low gate voltage the rate of decrease of V_B' is higher than the rate of increase V_B. Hence conductance increases because of the presence of V_B' at the numerator of equation (2.14). However, at higher gate voltage, increasing nature of V_B dominates over the decreasing nature of V_B'. So conductance decreases at this higher gate voltage.

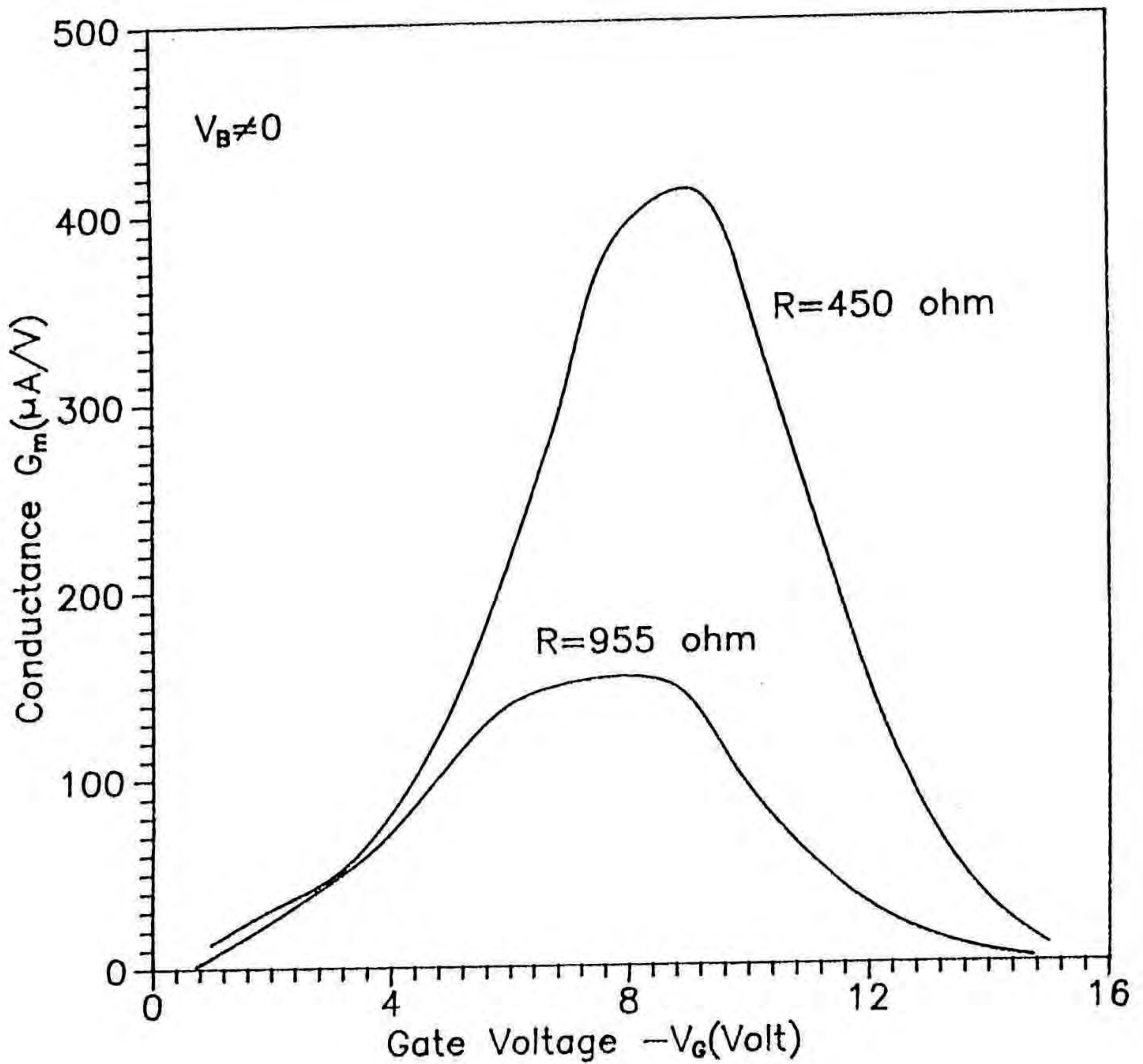

Fig.3.4 Transconductance vs gate voltage considering different series resistances.

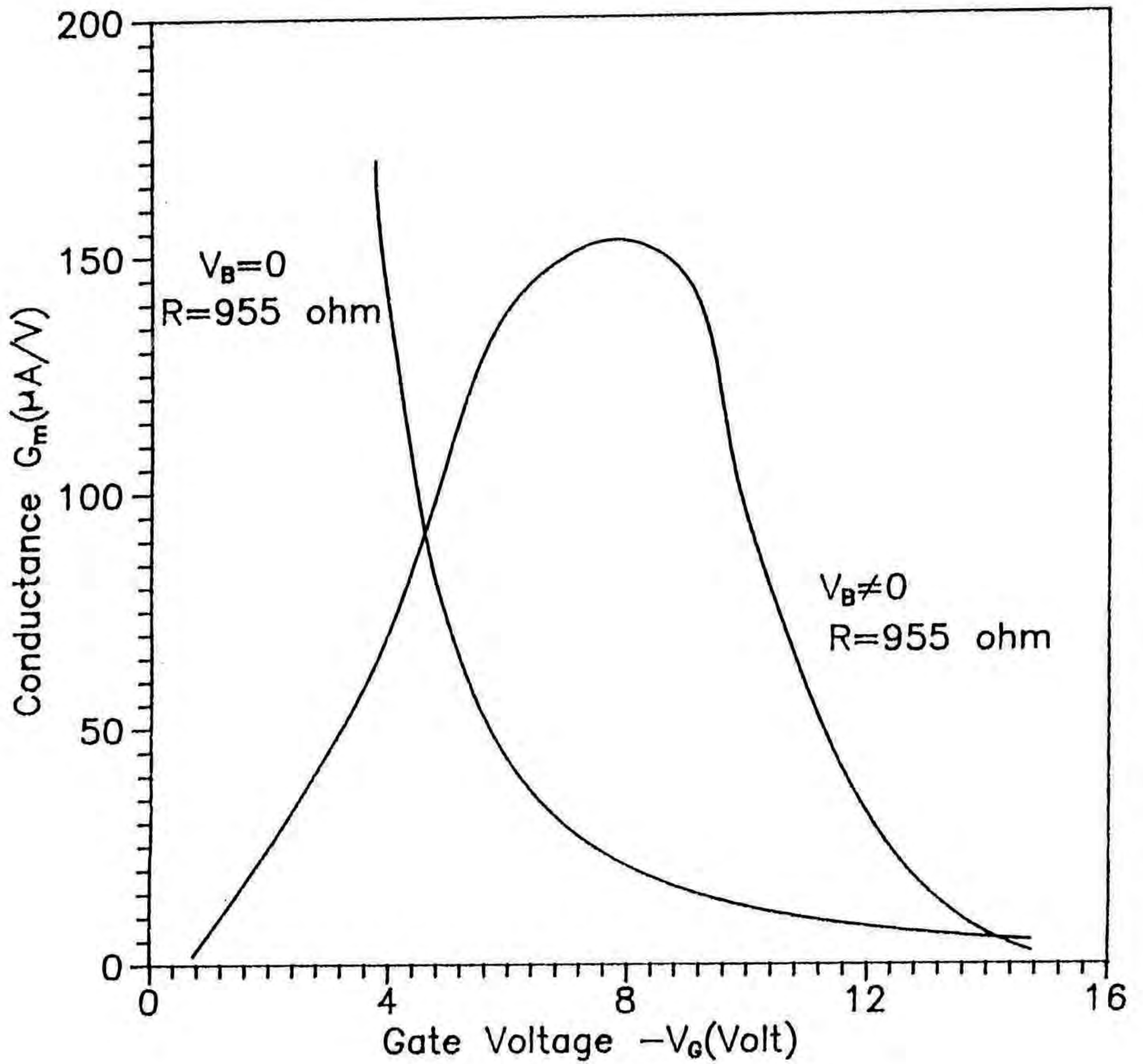

Fig.3.5 Transconductance vs gate voltage for a series resistance of 955 ohms.

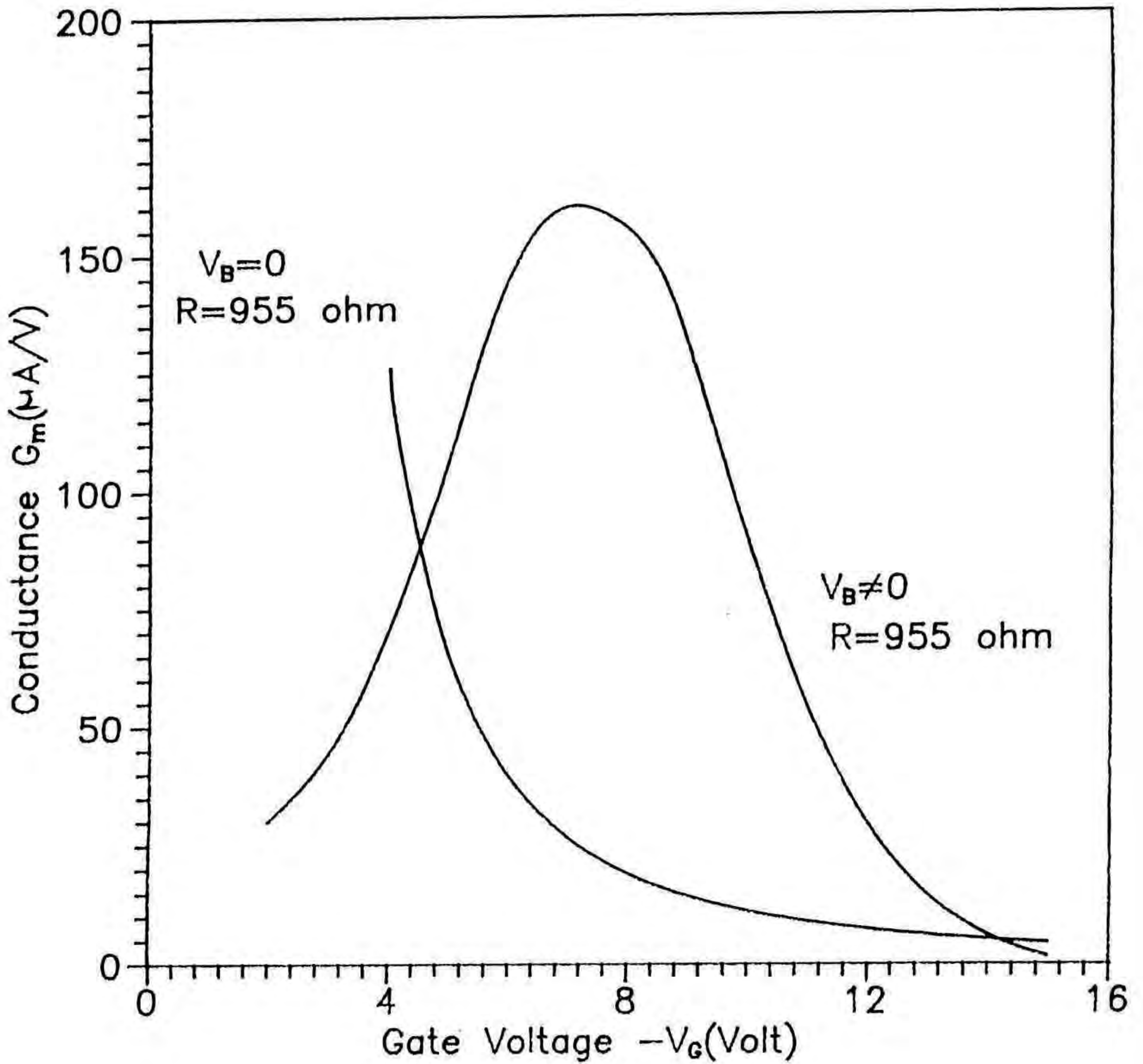

Fig.3.6 Transconductance vs gate voltage considering mobility reduction factor for a series resistance of 955 ohms.

Fig-3.6 shows the variation of conductance with barrier potential considering mobility reduction factor. The effect is almost same as that if we consider constant mobility.

3.2.6 Drain current as a function of potential barrier

Drain current is an important parameter of MOSFET. Fig-3.7 presents the variation of drain current with gate voltage with and without barrier potential. This variation can be explained by equation (2.9). If there is no potential barrier, the second term of the denominator is equal to zero. The denominator of this equation is the current reduction factor by the potential barrier and series resistance. So with the increase of barrier potential, drain current decreases for a fixed series resistance. For a small variation of gate voltage drain current increases rapidly because of barrier potential. The theoretical results obtained from the model derived in chapter 2 are in good agreement with the experimental data from the literature [4] considering series resistance equal to 955 ohms as shown in Fig-3.7.

3.3 Conclusion

The mathematical models developed in chapter 2 are used to see the effect of barrier potential on drain current and conductance of short-channel MOS device. The mobility reduction factor has also been considered, but the difference of this characteristics curve with that of constant mobility

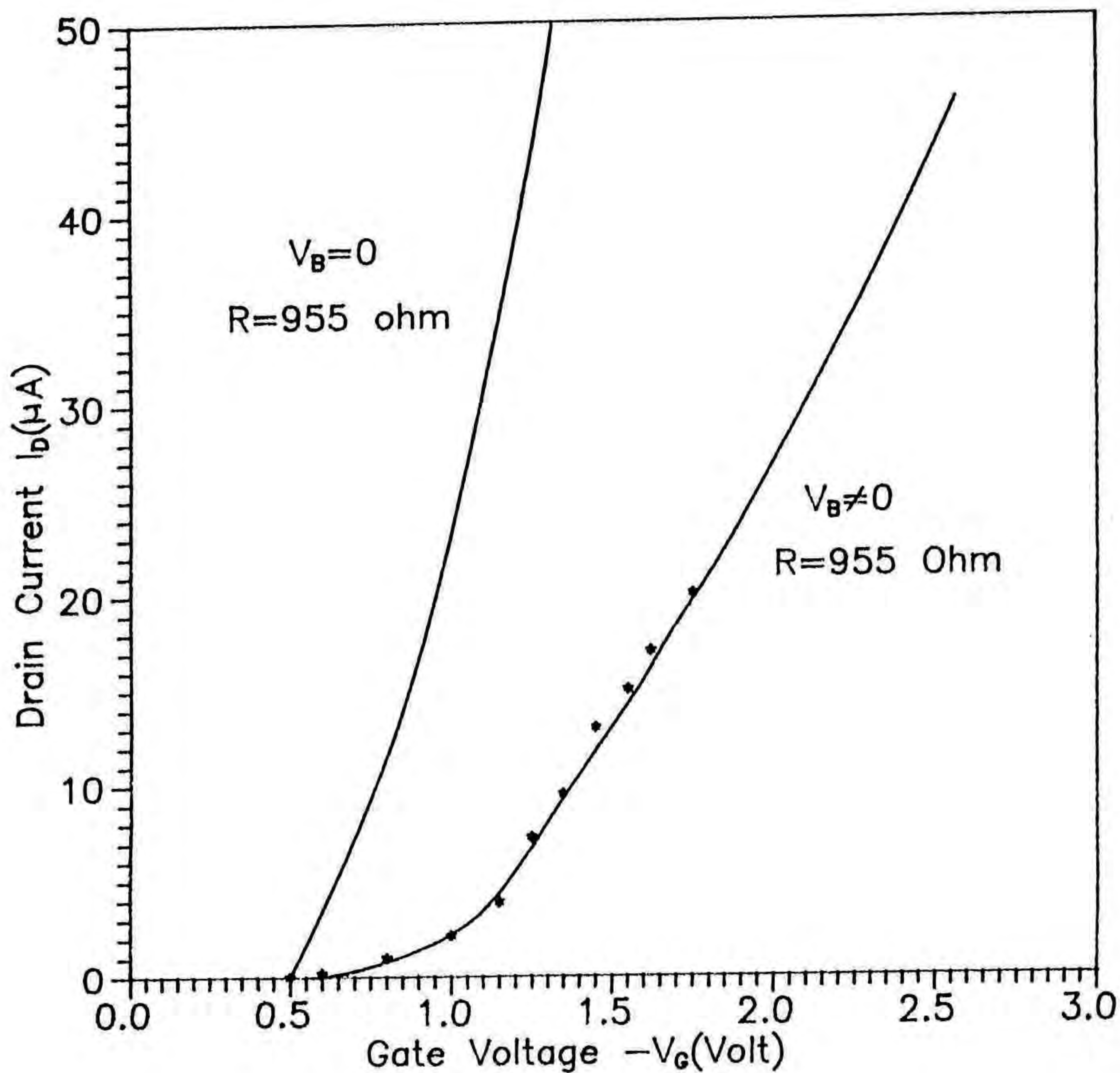

Fig.3.7 Drain current vs gate voltage for a series resistance of 955 ohms.

——— calculated from equation (2.11)

***** measured data taken from the literature[4].

of channel is insignificant. That is why, the characteristic curves considering mobility reduction factor have not been shown though the models have been developed in chapter 2. The variation of drain current and conductance with respect to series resistance are also studied in this chapter. The characteristics curves in the subthreshold region are also studied. But in this region the drain current and conductance of the device are so small that we can consider that values almost equal to zero. Also the variation of device characteristics due to different substrate doping has been studied in this chapter.

CHAPTER 4

CONCLUSION AND SCGGESTIONS

4.1 Conclusion

An analytical model of drain characteristics curve and conductance for short-channel MOS device has been presented in this work. The model has been developed in subthreshold and active region and considers mobility reduction factor as well. Several models have been developed so far but those models could not explain clearly the variation of the device characteristics considering potential barrier. The source/drain to channel series resistance also greatly affects the device characteristics. But reported models have neglected this resistance effect. Because of the extensive use of short-channel MOSFETs we should always consider these effects. In this work, a complete explanation of the graphical results have been given by analytical model developed in chapter 2. The device characteristics have been explained with the variation of substrate doping. So, there should be a relation between the doping level, barrier potential and series resistance so that we can have a reasonable characteristics of the short-channel MOS device. If the maximum potential is far away from the gate electrode, the gate voltage has very small control to potential maximum. The reverse short-channel effect is small in this case but the device series resistance is very

large. The results show that the potential barrier can severely degrade the drain current and transconductance of the device. For a high performance circuit application the "reverse short-channel effect" of the device must be completely eliminated.

4.2 Suggestions

In this model there is no complete explanation of variation of threshold voltage with channel length of the device considering barrier potential. So one can explain the threshold voltage variation with channel length. Also this work is based on one dimensional analysis. As the characteristics of MOSFET depends on both vertical and horizontal electric field, further study on this topic can be done considering multi-dimensional analysis.

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