ANALYTICAL MODELLING AND TEMPERATURE DEPENDENCE OF THRESHOLD VOLTAGE IN SHORT CHANNEL FULLY DEPLETED CYLINDRICAL GATE MOSFET

A Thesis submitted to
the Department of Electrical and Electronic Engineering of BUET, Dhaka
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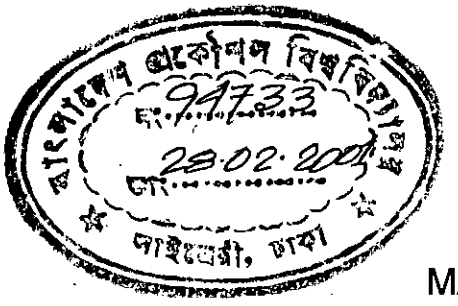
for the degree of
Master of Science in Engineering
(Electrical & Electronic)



by

MAHBUBA RAHMAN

December, 2000

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APPROVAL

This thesis titled "**Analytical modelling and temperature dependence of threshold voltage in short channel fully depleted cylindrical gate MOSFET**" submitted by **Mahbuba Rahman**, Roll No. 9506215P, session 1994-95-96 to the Department of Electrical & Electronic Engineering, BUET, Dhaka has been accepted as satisfactory for the partial fulfillment of the requirements for the degree of **Master of Science in Engineering (Electrical & Electronic)**.

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ABSTRACT

A novel physics-based analytical model for short-channel effects in thin film fully depleted cylindrical gate MOSFET has been presented in this thesis. The scaling parameter was derived from the cylindrical form of Poisson's equation by assuming a parabolic potential in the radial direction.

Analytical expressions for natural length, λ, threshold voltage, V_{th}, threshold voltage shift, ΔV_{th}, sub-threshold swing, S, and drain-induced barrier lowering, *DIBL*, were derived for the cylindrical gate MOSFET and their response to the variation in parameters like gate length, silicon film thickness, drain voltage, etc. have been carefully studied. The results obtained from these analyses were compared to those of the double gate silicon-on-insulator MOSFETs (DG-SOI MOSFETs). The cylindrical gate MOSFET exhibits better short-channel effect immunity compared to the DG-SOI MOSFETs.

Finally, an analytical temperature dependent model for threshold voltage in thin film fully depleted cylindrical gate MOSFET has also been developed using a Gaussian doping profile and is compared with that of the DG-SOI MOSFETs.

LIST OF FIGURES

LIST OF PRINCIPAL SYMBOLS AND ABBREVIATIONS

C_{ox}	Oxide capacitance (= ε_{ox}/t_{ox})
C_{si}	Silicon film capacitance (= ε_{si}/t_{si})
DG	Double gate
DIBL	Drain induced barrier lowering
k_B	Boltzman constant
L_G	Gate length
N_A	Acceptor concentration
N_{p+poly}	Doping concentration of the p^+ polysilicon
n^+	Source/drain concentration
q	Electronic charge
Q	Channel implant dose
r	Channel radius of cylindrical gate MOSFET
R_p	Projected range
S	Sub-threshold swing (S-swing)
SG	Single gate
SOI	Silicon-on-insulator
T	Temperature
t_{si}	Silicon film thickness
t_{ox}	Oxide thickness
V_{bi}	Built-in potential
V_D	Drain voltage
V_G	Gate voltage
V_S	Source voltage
V_{FB}	Flat-band voltage
V_{FBp+}	Flat-band voltage associated with the p^+ polysilicon gate

V_{th} Threshold voltage

V_{th1} Threshold voltage associated with the n^+ polysilicon gate

V_{th2} Threshold voltage associated with the p^+ polysilicon gate

V_{thDG} Threshold voltage associated with the double gate MOSFET

V_{thCL} Threshold voltage associated with cylindrical gate MOSFET

ΔV_{th} Threshold voltage shift

ΔV_{thDG} Threshold voltage shift of double gate SOI MOSFET

ΔV_{thCL} Threshold voltage shift of cylindrical gate MOSFET

W Channel width

α Scaling parameter

α_{DG} Scaling parameter of DG-SOI MOSFET

α_{CL} Scaling parameter of cylindrical gate MOSFET

β Thermal constant ($= \frac{q}{k_B T}$)

λ Natural/characteristic length

λ_{DG} Natural length of double gate SOI MOSFET

λ_{CL} Natural length of cylindrical gate MOSFET

γ Constant ($= \varepsilon_{si}/\varepsilon_{ox}$)

ϕ Channel potential

ϕ_c Center potential of channel

ϕ_s Surface potential of channel

ϕ_{gs} Gate potential

ϕ_{sth} Surface potential of channel at $V_G = V_{th}$

ϕ_F Fermi level potential

ε_{ox} Permittivity constant of SiO_2

ε_{si} Permittivity constant of Si

σ Standard deviation

CHAPTER 1

INTRODUCTION

1.1 Introduction

The invention of transistor in 1948 by Bardeen, Brattain and Shockley at the Bell Telephone Laboratory in the USA made a complete revolution in the electronic industries. In fact, modern era of semiconductor electronics started after this invention. Prior to this invention, valve was the only device in the world of electronics. Due to the multi-dimensional advantages of transistor, vacuum tubes or valves were almost replaced after the emergence of transistor. Transistors began to be used as amplifiers, detectors, rectifiers, oscillators, mixers, modulators, etc. Some of the advantages of transistors over vacuum tubes are as follows:

- No heater or filament is required, hence no warming-up time needed.
- Smaller in size and hence are light in weight.
- Requires very low operating voltages.
- Consumes little power, resulting in greater circuit efficiency.
- Much more reliable because of solid construction, extremely rugged and can be made impervious to many severe environmental and bias stress conditions.
- Longer life with essentially no aging effect.

The Noble prize in Physics was awarded in 1956 to three scientists who invented transistor in 1948. In fact, transistors opened the door to further developments in electronics. Within almost ten years of this invention, the process of miniaturization of electronic devices had gained significant momentum and the

first Integrated Circuit (IC) appeared around 1960. Man's desire to conquer the space accelerated this effort even further. The purpose of miniaturization was to increase the packing density (i.e., more components could be accommodated on a single IC/chip with the same area) and to improve the circuit performances such as speed, response time, etc. With the advent of ICs, many circuit functions could be packed into a small area and complex electronic equipments could be employed in many applications where space and weight are critical, such as in aircraft or space vehicles. The use of valves nearly became obsolete during the sixties and novel semiconductor devices were emerged/developed day-by-day with perspective and promising features for various aspects, specially for circuit miniaturization. In this respect, the field-effect-transistor or FET was developed in the early 1960s. Like the bipolar junction transistor (BJT), the FET is a three-terminal device in which the current through two terminals is controlled by a voltage at the third terminal (unlike the BJT which is controlled by a current). Another difference is that the FET is a unipolar device (i.e., its current involves majority carriers only) whereas the BJT is a bipolar device (i.e., its current involves both majority and minority carriers).

With the passage of time, FETs came in several forms, e.g., JFET, MESFET and MOSFET. In a junction FET (JFET), the control or gate voltage varies the depletion width of a reverse-biased p-n junction. In a metal-semiconductor FET (MESFET), the junction of a JFET is replaced by a Schottky barrier. The FET that has the greatest commercial importance in the metal-oxide-semiconductor FET (MOSFET, sometimes called MOST). Also known as insulated-gate FET (IGFET), a MOSFET uses an oxide layer to separate its gate electrode from the semiconductor. Field effect transistors combine the inherent advantages of solid state devices (e.g., small size, low power consumption and mechanical riggedness) with a very high input impedance and a square-law transfer characteristic that is specially suitable for use as voltage amplifiers. Since its invention, the field effect transistors (FETs) became a superior rival to its

counterparts, the bipolar junction transistors or BJTs. Some of the advantages of FET over BJT are as follows:

- Exhibit a higher input impedance (typically many megaohms), since the control (or gate) voltage is applied to a reverse-biased junction or Schottky barrier or across an insulator.
- Simpler to fabricate and occupies less space in ICs, hence it is specially suitable for integration of many devices on a single chip.
- Well suited for controlled switching between an ON state and an OFF state and is therefore useful in digital ciucuits.
- Less noisy.

Among the members of FET family and other semiconductor devices, metal-oxide-semiconductor FET or MOSFET has gained special significance and prominence over the past two decades. The dominating factor behind such specialty is that the MOS transistor is very well suited to the IC technology, owing to the advantages that it is simpler or easier to fabricate and its size can be reduced with less degree of *small-geometry-effects*. In the past few years, MOSFET has emerged as the most important electronic devices for the researchers, superseding its bipolar counterpart and other devices in both sales volume and applications. MOS transistor has already confirmed its state as a better choice for use in densely packed circuits like ultra large scale integration (ULSI) circuits. Also the fact that digital circuits require only on-off response is an advantage for the MOS device and so MOS transistor is widely used in digital circuits like logic gates, registers or memory arrays.

1.2 Choice of Technology

As said earlier that IC technology was a great advancement of mankind in the world of electronics. The rapid developments in integrated circuit technology

started in 1960. At that time, IC/chip size and transistor dimensions were such that only a few simple gates offering primitive logic functions such as NOT, NAND, NOR, etc. could be accommodated . This level of integration is called Small Scale Integration (SSI). Improvements in the processing techniques in subsequent years have resulted in a steadily decreasing chip area and a progressively reducing feature size. This has allowed a complexity increase of approximately 100 every ten years. Thus by 1970, Medium Scale Integration (MSI) circuits with about a thousand transistors appeared, while by 1980 Large Scale Integration (LSI) circuits of approximately one hundred thousand devices were possible. In the same way, in 1990 Very Large Scale Integration (VLSI) circuits appeared with $10^7 - 10^8$ transistors in a single chip. Very recently, Ultra Large Scale Integration (ULSI) circuits with billions of transistors are available in the market. The vast changes that have taken place during the last 40 years can best be understood by noting the reduction in size and price of modern computers. A modern personal computer (PC) is more than 100 times smaller in size and $1/100^{th}$ of the price of a computer designed 20 years ago to do the same job. Applications of ICs are now pervasive in such consumer products as watches, calculators, automobiles, telephones, television and other home appliances.

Although other materials are available for manufacturing integrated circuits, silicon remains the most economically effective way of implementing VLSI/ULSI. Two distinct types of technology are fabricated in silicon based on the BJT and the MOS transistor. Since the processing for these technologies is very different, it is not practical to mix them within a chip or in a wafer of chips.

MOS logic occupies a much smaller area of silicon than the equivalent bipolar logic. This is partly due to a smaller device size and partly due to the fact that MOS structures require few components. Thus MOS technology has a much higher potential packing density. A MOS logic circuit requires appreciable less current and hence less power than its bipolar counterparts. However, bipolar circuit operates faster than MOS circuit. Even the speed power product of MOS

circuit is more favorable than bipolar circuit. The structure of a MOS transistor is much simpler than that for bipolar devices and this makes its manufacturing process easier. This in turn should result in fewer faults occuring in fabrication and hence increase the number of working chips compared with the number obtainable in a similar area from bipolar technology. The greater yield of good chips offered by MOS technology is of importance, since a high proportion of chips does not function correctly owing to manufacturing defects.

MOS technology also offers the advantage of being able to implement dynamic logic, where states are stored temporarily on capacitance inherent in the circuit structure; this leads to further reductions in area and power, and such circuits are obviously important in the context of VLSI/ULSI. It is not possible to implement dynamic logic in bipolar technology and thus MOS offers a greater choice of design implementations. Thus in terms of area, power dissipation, product yield, reliability and flexibility MOS technology is superior to bipolar technology. Furthermore, of the two technologies, only MOS is capable of realizing VLSI/ULSI.

Although the speed of the present BJT is faster than the MOS devices, this situation is likely to change in the future. As we know the speed of the bipolar device depends on its base width, which is at its minimum (quantum) level. So further increase of speed of bipolar devices can not be achieved. But the speed of MOS device depends on its gate length and as shown in the sebsequent sections, we will find that a very reduced gate length (less than 0.1 μm) can be achieved for this device. As a result MOS devices with a speed faster than bipolar devices can be realized in practice.

1.3 Review of the Previous Work on MOSFETs

As said earlier, the metal-oxide-semiconductor FET or MOSFET has been the major device for integrated circuits over the past two decades and this was due to the fact that scaling down of the MOSFET provided high performance gain and smaller die size. The twin benefits of smaller die size (more chips per wafer and higher fractional yield) exert downward pressure on die cost. As a natural and consequential effort, industrial research has already set sight on MOSFETs of channel length of 0.1 μm and below [1]. The motivations for continued scaling include not only better speed and density but also less power consumption for integrating a complete system on a chip. There have been numerous device structures of sub-micrometer MOSFET reported in the literature, such as MOSFET with uniformly doped substrate (UD), delta doped MOSFET (DD), partially depleted silicon-on-insulator (SOI) MOSFET and fully depleted SOI MOSFET. Among these, fully depleted SOI MOSFET (which has an additional oxide layer just below the Si film) has attracted considerable attention as a potential candidate for future VLSI/ULSI generations, because it offers superior electrical characteristics over bulk MOSFETs, such as reduced junction capacitances, attenuated short-channel effects, improved sub-threshold characteristics, increased channel mobility, reduced hot carrier effects and so on. As a consequence, sub-micrometer and deep-sub-micrometer SOI circuit design and simulation are becoming increasingly important in VLSI/ULSI technology research. In the subsequent sub-sections, scaling in various MOSFET structures will be ameliorated.

1.3.1 Performance of Bulk MOSFETs in VLSI and ULSI Levels

Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) has been the major device for integrated circuits (ICs) over the past two decades. The initial objective of VLSI has been the integration of an ever-increasing number of

devices with high yield and reliability. Integration of billions of MOS transistors in a single chip beyond 2000 will require that device dimensions be reduced to below 0.1 μm levels. However, as MOS device dimensions enter into the deep-sub-micrometer regime, the characteristics of a conventional MOSFET becomes similar to that of a resistor i.e. the saturation current does not remain constant with increasing drain voltage, V_D. Traditionally the problem is solved through increased channel doping that increases the threshold voltage [2].

A variety of other effects occur as the MOS device dimensions are reduced such as *drain-induced barrier lowering* (DIBL) [3] that results in loss of gate control. An effect that is exacerbated by short-channel designs is the *sub-threshold current.* This effect is made worse by the DIBL effect, which increases the injection of electrons from the source. Electric fields tend to be increased at small geometries, since device voltages are difficult to scale to arbitrarily smaller values. As a result various hot carrier effects appear in short-channel devices [4-6]. The field in the reverse-biased drain junction can lead to impact ionization and carrier multiplication. Another hot electron effect is the transport of energetic electrons tunneling through the barrier into the oxide. Such electrons can become trapped in the oxide, where they can change the threshold voltage and the *I-V* characteristics of the device. Hot electron effects can be reduced by using a design called the *lightly doped drain* (LDD) [7] that uses two doping levels, with heavy doping over most of the source and drain areas but with light doping in a region adjacent to the channel. The LDD structure decreases the field between the drain and the channel regions, thereby reducing injection into the oxide, impact ionization, and other hot electron effects.

In the subsequent sections, step-by–step procedures have been followed for the development of Double-Gate (DG) SOI MOSFETs. Starting with the scaling of bulk MOSFETs, scaling theories of Single-Gate (SG) and DG-SOI MOSFETs are critically analyzed. Brew's empirical scaling rule [8] has provided a successful guideline for the design of the conventional MOSFET. We will

analyze the implications of the rule in the deep-sub-micrometer regime and study how fully depleted SOI structures attempt to circumvent the limitations faced by conventional deep-sub-micrometer devices. We provide a comparative analytical framework, within which scaling may be naturally understood, supporting the analytical treatment, where appropriate. We conclude by describing a particular device structure, which may realize the promise of a well-behaved, deep-sub-micrometer device operating at room temperature.

1.3.2 Scaling in MOSFET Structures

A. Direct Scaling in Bulk MOSFETs

Various device-scaling rules have been proposed. Brews empirical rule [8] provides a general guideline for the sub-threshold region and is considered the basic guideline for applications such as dynamic and static memory circuits, where leakage currents in the off-state of the devices are important. Yan et al. [9] formulated in the following way to relate the channel doping to the intrinsic device parameters:

$$N_A \geq 1.8\times10^{17} cm^{-3} \frac{\left[\sqrt{V_{bi}}+\sqrt{V_{bi}+V_D}\right]^2}{volts} \cdot \frac{t_j}{50nm} \cdot \left[\frac{0.1\mu m}{L_{eff}} \cdot \frac{t_{ox}}{4nm}\right]^3 \qquad (1.1)$$

Using this relation it was found that in a structure of 0.1 μm channel length, 4 nm gate oxide, 50 nm junction depth and 1.0 V power supply voltage, the channel doping has to be $\geq 10^{18}$ cm^{-3}. Again to suppress the short channel effects such high doping is necessary. However, high doping leads to high capacitance, severely limiting the circuit speed. For an NMOS the resultant vertical fields induced by the high doping degrades the surface mobility of the p-doping region. Both problems caused by direct scaling. Therefore, high capacitance and mobilility degradation must be solved for deep-sub-micrometer devices to work successfully.

B. Scaling in SG-SOI MOSFETs

An interesting and useful extension of the silicon MOS process can be achieved by growing very thin films of single crystal silicon, *Si*, on insulating substrates. The *Si* films being very thin (100 nm) the source and drain regions can be made to extend entirely through the film to the buried insulator and as a result the junction capacitances are remarkably reduced. Such a device with *Si* film sandwiched between two insulating oxide layers is known as *Silicon-On-Insulator* MOSFET or SOI MOS (Fig. 1.1).

To resolve the problem of high capacitance by direct scaling, the heavy doping has to be reduced at the drain end, while maintaining good sub-threshold characteristics. One approach is to operate the device at low temperature. The effective barrier height for electrons increases as temperature decreases [10]. A doping of 10^{17} cm^{-3} can be used at 77 K with good turn-off behaviour [11].

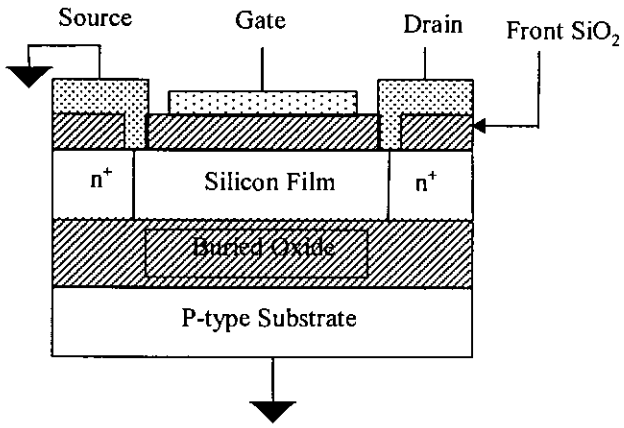


Fig. 1.1. Cross sectional view of a SG-SOI MOSFET.

An important approach is to use fully depleted SOI. The buried oxide reduces the junction capacitances dramatically. Furthermore, the high channel doping can be reduced because of the additional advantage introduced by using the thin *Si* layer in the structure. Basically, the electrical field profile undergoes a rapid change in the vertical direction and induces a large potential curvature in the

lateral direction helping to build up the potential barrier required to prevent electron flow from the source. Therefore, one could control horizontal leakage through vertical structures. However, in deep-sub-micrometer regime, SG-SOI MOSFET is found to be disadvantageous, as short-channel effects become prominent. So a further modification is required. The modification is DG-SOI MOSFETs.

C. Scaling in DG-SOI MOSFETs

The *Gate-All-Around* [9] structure has been proposed as a way to improve the drive capability of SOI devices. Basically, a gate oxide replaces the buried oxide and the same gate voltage is applied to both the top and bottom gates (Fig. 1.2). A DG-SOI MOSFET, in which the potential is controlled by front and back gates, is proposed to circumvent the scaling limitations of bulk MOSFETs. The characteristics of this device have been studied [9, 12-14], revealing its ideal sub-threshold factor, high transconductance and short channel effect immunity. Since DG-SOI MOSFETs are free from the bulk MOSFETs scaling limit [5, 8,10], detailed scaling theory of DG-SOI MOSFETs will be analyzed further in the next section.

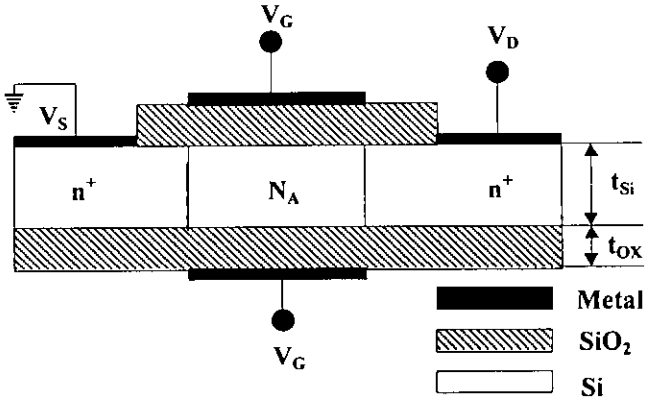


Fig. 1.2. Cross-sectional view of double-gate SOI MOSFET.

1.3.3 Scaling Theory of DG-SOI MOSFETs

Gate Material:

Work function difference between the gate material and *Si* (ϕ_{ms}) plays an important role in determining threshold voltage. For usual *Al* gate this ϕ_{ms} is relatively high and thus contributes a high negative term in the threshold voltage equation. As a consequence, the n-channel MOSFETs tend to operate in depletion mode. To reduce this contribution due to ϕ_{ms} we have to find out a new gate material. A straightforward method for reducing ϕ_{ms} is to deposit polycrystalline *Si* (poly-*Si*) as a gate conductor. This provides a close match between ϕ_m and ϕ_s. There are additional advantages of this method that makes it attractive for MOS IC applications. Unlike *Al*, a poly-*Si* gate layer can be raised to high temperature allowing considerable flexibility in device processing.

Threshold Voltage Models for p^+-p^+ & n^+-p^+ MOSFETs:

As in the case of bulk MOSFETs, the threshold voltage of a double-gate SOI MOSFET depends on gate material. Depending on doping, two types of poly-*Si* can be used as gate conductor, such as p^+ and n^+. Consequently we will get two different threshold voltages. Throughout this analysis we will assume that the following conditions are always maintained:

- In p^+-p^+ and n^+-p^+ structures, both gate oxide thicknesses t_{ox} are the same.
- The same gate voltage V_G is applied to both gates.
- The channel doping concentration is constant and is in the range of 10^{15} cm^{-3}.

The threshold voltage, V_{th}, of a double-gate SOI MOSFET is given by [15]

$$V_{th}(p^+ - p^+) = V_{FBp} + 2\phi_F + \frac{(1+\frac{4C_{Si}}{\beta Q_{Si}})}{2} Q_{Si}\left(\frac{1}{4C_{Si}} + \frac{1}{C_{ox}}\right) + \frac{1}{\beta}\ln\left(\frac{4C_{Si}}{\beta Q_{Si}}\right). \qquad (1.2)$$

Here,

$$\frac{1}{\beta}=\frac{k_B T}{q}, \phi_F=\frac{1}{\beta}\ln\left(\frac{N_A}{\eta_i}\right), V_{FBp^+}=\frac{1}{\beta}\ln\left(\frac{N_{p^+poly}}{N_A}\right), Q_{Si}=qN_A t_{Si}, C_{Ox}=\frac{\epsilon_{Ox}}{t_{Ox}} \text{ and}$$

$$C_{Si}=\frac{\epsilon_{Si}}{t_{Si}}.$$

k_B is the Boltzmann constant, T is the absolute temperature, η_i is the intrinsic carrier concentration, V_{FBp+} is the flat band voltage associated with the p^+ polysilicon gate, N_{p+poly} is the doping concentration of the p^+ polysilicon, ϵ_{Ox} and ϵ_{Si} are the permittivity constants of SiO_2 and Si, respectively.

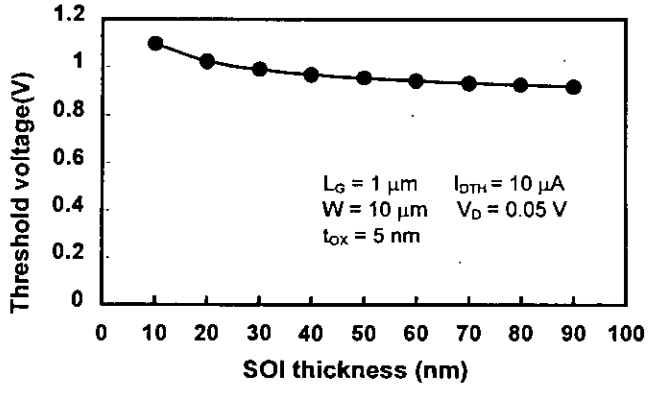


Fig. 1.3. Dependence of threshold voltage of p^+-p^+ double-gate devices on SOI thickness.

Threshold voltage is almost independent on SOI thickness (Fig. 1.3). The third and fourth term of the threshold voltage expression (eqn. 1.2) depend on device parameter t_{ox} and t_{Si}, but their contribution is negligible. Thus the threshold voltage of a DG-SOI MOSFET is insensitive to t_{ox} and t_{Si}. Work function of the gate material predominantly determines the threshold voltage. Its value is around 1 V if we use p^+ polysilicon and below 0 V if we use n^+ polysilicon. But for high speed and low power operation in deep-sub-micrometer gate length regimes, 1 V is too high and negative threshold voltage is also not acceptable.

To make such a device acceptable we must use either (i) a new gate material such as TiN [16] or (ii) n^+-p^+ double-gate SOI MOSFETs [17]. An n^+- p^+ double-gate SOI MOSFET (Fig. 1.4) has two different threshold voltages [17] related to each gate material. Thus V_{th} can be controlled through the interaction between the both gates [18, 19].The threshold voltage associated with the n^+ polysilicon gate [17] is,

$$V_{th1} = V_{th}(p^+ - p^+) - \frac{\gamma t_{Ox} + t_{Si}}{2\gamma t_{Ox} + t_{Si}} \Delta V_{FB} \qquad (1.3)$$

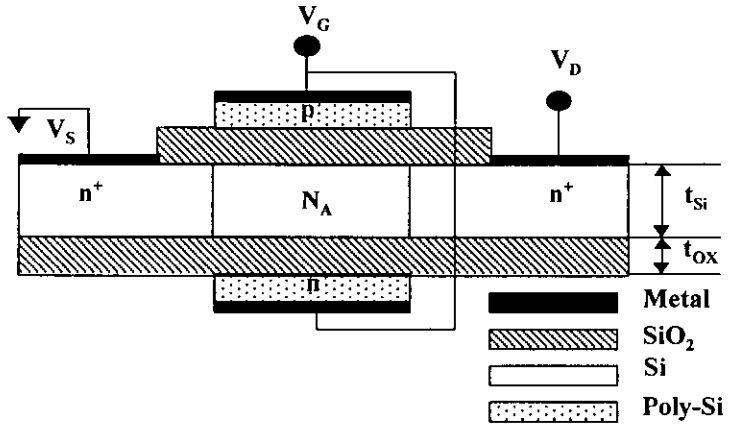


Fig. 1.4. n^+- p^+ double-gate SOI MOSFET.

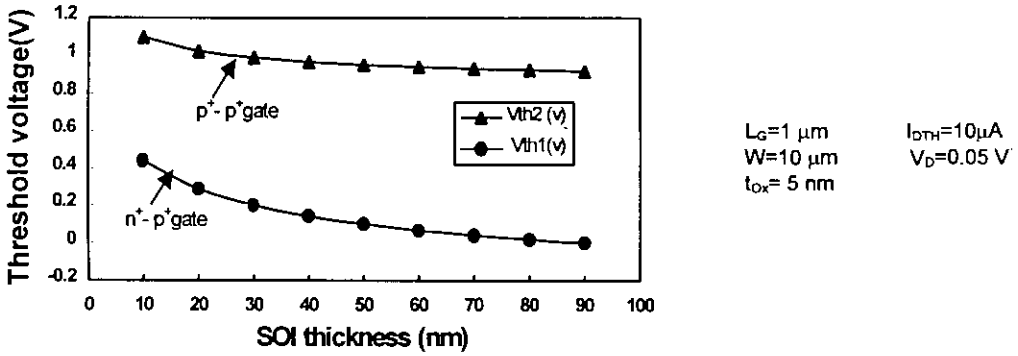


Fig. 1.5. Dependence of threshold voltages of p^+-p^+ and n^+- p^+ double gate device on SOI thickness.

The second threshold voltage associated with the p^+ polysilicon gate is,

$$V_{th2} = V_{th}(p^+ - p^+) \tag{1.4}$$

Thus, V_{th1} is a function of t_{Ox} and t_{Si}. It is about 0.25 V for $t_{Ox}/t_{Si} = 5$ (Fig. 1.5). As shown earlier (Fig. 1.3), V_{th2} is independent of the device parameters and is around 1 V. Therefore, both channels contribute to conduction when the gate voltage exceeds 1 V, but the p^+ polysilicon gate only controls V_{th1} when the gate voltage is less than 1 V.

1.3.3.1 Short Channel Effects for DG-SOI MOSFETs

Scaling theory of DG-SOI MOSFETs is completely different from that of bulk MOSFETs. Yan et al. [9] proposed a unique scaling theory for DG-SOI MOSFETs. They proposed a natural length scale, which can be effectively used as a design guideline. According to their theory, the device should be designed maintaining,

$$\alpha = \frac{L_G}{2\lambda} \tag{1.5}$$

where λ is the so-called natural length, which characterizes the short-channel effect and is given by

$$\lambda = \sqrt{t_{Si} t_{Ox} \frac{\epsilon_{Si}}{2\epsilon_{Ox}}} \tag{1.6}$$

This natural length is an easy guide for choosing device parameters and has simple physical meaning that a small natural length corresponds to superb short channel effect immunity. In the following subsections we will show that this natural length is larger for the p^+-p^+ double gate than that of the n^+-p^+ double gate SOI MOSFETs. This is due to the fact that punch through current flows along the surface for n^+-p^+ double gate but it flows at the center of SOI in the p^+-p^+ double gate SOI and the potential is controlled more strongly at the surface.

A. Scaling Theory for p^+-p^+ Double Gate SOI MOSFETs

For p^+-p^+ double gate SOI MOSFETs, the maximum potential at the SOI center, ϕ_c, is more sensitive to gate length than that at the surface, ϕ_s, and furthermore, as pointed [12], the absolute value of ϕ_c is smaller than that of ϕ_s. Therefore, the punchthrough current dominantly flows at the SOI center. Starting from the Poisson equation of potential, ϕ, [20] we get,

$$\frac{d^2\phi(x,y)}{dx^2}+\frac{d^2\phi(x,y)}{dy^2}=\frac{qN_A}{\epsilon_{Si}}, \tag{1.7}$$

where N_A is the channel doping concentration and the y-axis is perpendicular and the x-axis is parallel to the channel (Fig. 1.6).

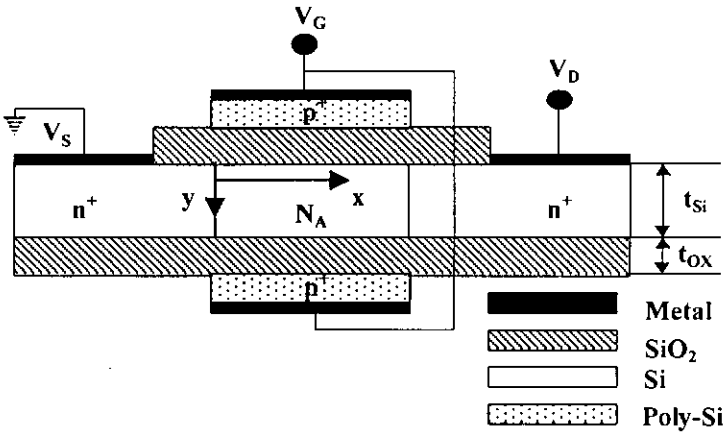


Fig. 1.6. p^+- p^+ double-gate SOI MOSFET.

Using the same parabolic potential profile in the vertical direction as Young used [20] and applying the boundary condition of $d\phi/dy = 0$ for $y = t_{si} / 2$, the expression for $\phi(x, y)$ is given by,

$$\phi(x,y)=\phi_s(x)+\frac{\epsilon_{ox}}{\epsilon_{si}}\frac{\phi_s(x)-(V_G-V_{FB})}{t_{ox}}y-\frac{\epsilon_{ox}}{\epsilon_{si}}\frac{\phi_s(x)-(V_G-V_{FB})}{t_{ox}t_{si}}y^2, \tag{1.8}$$

where V_G is the gate voltage and V_{FB} is the flatband voltage. Since ϕ_c should be relevant to the punchthrough current, the relation between ϕ_s and ϕ_c can be established by substituting y = t_{si}/2 in eqn. (1.8):

$$\phi_s(x) = \frac{1}{1+\frac{\epsilon_{Ox}}{4\epsilon_{Si}}\frac{t_{Si}}{t_{Ox}}}\left[\phi_c(x)+\frac{\epsilon_{Ox}}{4\epsilon_{Si}}\frac{t_{Si}}{t_{Ox}}(V_G-V_{FB})\right] \quad , \tag{1.9}$$

and then expressed $\phi(x,y)$ using ϕ_c as,

$$\phi(x,y) = \left[1+\frac{\epsilon_{Ox}}{\epsilon_{Si}}\frac{y}{t_{Ox}}-\frac{\epsilon_{Ox}}{\epsilon_{Si}}\frac{y^2}{t_{Ox}t_{Si}}\right]\cdot\frac{\phi_c(x)+\frac{\epsilon_{Ox}}{4\epsilon_{Si}}\frac{t_{Si}}{t_{Ox}}(V_G-V_{FB})}{1+\frac{\epsilon_{Ox}}{4\epsilon_{Si}}\frac{t_{Si}}{t_{Ox}}} - \frac{\epsilon_{Ox}}{\epsilon_{Si}}\frac{y}{t_{Ox}}(V_G-V_{FB})+\frac{\epsilon_{Ox}}{\epsilon_{Si}}\frac{y^2}{t_{Ox}t_{Si}}(V_G-V_{FB}) \tag{1.10}$$

Substituting (1.10) into (1.7) we obtain,

$$\frac{d^2\phi_c(x)}{dx^2}+\frac{V_G-V_{FB}-\phi_c(x)}{\lambda_2{}^2}=\frac{qN_A}{\epsilon_{Si}} \tag{1.11}$$

where λ_2 is the natural length having the same physical meaning as λ, and is,

$$\lambda_2 = \sqrt{\frac{\epsilon_{Si}}{2\epsilon_{Ox}}t_{Si}t_{Ox}\left(1+\frac{\epsilon_{Ox}}{4\epsilon_{Si}}\frac{t_{Si}}{t_{Ox}}\right)} \tag{1.12}$$

B. Scaling Theory for n^+-p^+ DG-SOI MOSFETs

Yan et al. [9] assumed that punchthrough current flows along the surface, which is also valid for n^+-p^+ double gate SOI MOSFETs. Consequently the natural length of these type of MOSFETs should have the same value as defined by Yan et al. [9], that is,

$$\lambda_1 = \sqrt{t_{Si}t_{Ox}\frac{\epsilon_{Si}}{2\epsilon_{Ox}}} \tag{1.13}$$

As λ_2 is greater than λ_1, p^+-p^+ double-gate SOI MOSFETs suffer from the short channel effects more than n^+-p^+ MOSFETs.

C. Models for Short Channel in n^+-p^+ Devices

In the earlier section we have shown the threshold voltage for the long channel device can be given as,

$$V_{th} = \phi_{sth} + V_{FBn} + \frac{\gamma t_{Ox}}{2\gamma t_{Ox} + t_{si}} \Delta V_{FB} \tag{1.14}$$

where ϕ_{sth} is the surface potential at $V_G = V_{th}$ and is given by,

$$\phi_{sth} = 2\phi_F + \frac{(1+\frac{4C_{Si}}{\beta Q_{Si}})}{8C_{Si}} Q_{Si} + \frac{1}{\beta} \ln(\frac{4C_{Si}}{\beta Q_{Si}}) \tag{1.15}$$

However, we neglect both charges in the derivation of the short channel model which gives, $\phi_{sth} = 2\phi_F$.

This approximation is valid for DG-SOI MOSFETs because of their low doping concentrations and the potential deviation due to this approximation is less than 0.1 V. However the deviation due to this approximation is not negligible. In order to improve the accuracy of the model we will derive the short channel threshold voltage shift using the above approximation but use the original expression for threshold voltage.

The Poisson equation of potential, ϕ, is given by

$$\frac{d^2\phi(x,y)}{dx^2} + \frac{d^2\phi(x,y)}{dy^2} = \frac{qN_A}{\epsilon_{Si}} \approx 0, \tag{1.16}$$

where the x-axis is parallel to the channel, and the y-axis is perpendicular to the channel. Using a parabolic potential profile in the vertical direction as Young [20] used and applying the boundary conditions so that the potentials and electric flux are the same at both gate oxide-SOI interfaces, we obtained a potential expression of

$$\phi(x,y)=\phi_f(x)-\frac{\phi_{gf}-\phi_f(x)}{\gamma t_{Ox}}y+\frac{(2+\frac{t_{Si}}{\gamma t_{Ox}})[\phi_{gf}-\phi_f(x)]-\Delta V_{FB}}{2\gamma t_{Ox}t_{Si}+t_{Si}^2}, \quad (1.17)$$

where the origin is set at the SOI/gate oxide interface on the n^+ polysilicon side. ϕ_f is the potential at y=0 and ϕ_{gf} is ($V_G - V_{FBn}$). Substituting (1.17) into (1.16), we obtain

$$\frac{d^2\phi_f(x)}{dx^2}+\frac{\phi_{gf}-\phi_f(x)}{\lambda^2}=\frac{\Delta V_{FB}}{2\lambda^2(1+\frac{t_{Si}}{2\gamma t_{Ox}})}, \quad (1.18)$$

where λ is the characteristic length expressing short channel immunity and is given by

$$\lambda=\sqrt{\frac{\gamma t_{Si}t_{Ox}}{2}}. \quad (1.19)$$

Introducing a variable

$$\eta(x)=\phi_f(x)-\phi_{gf}+\frac{\Delta V_{FB}}{2(1+\frac{t_{Si}}{2\gamma t_{Ox}})} \quad (1.20)$$

(1.18) reduces to

$$\frac{d^2\eta(x)}{dx^2}+\frac{\eta(x)}{\lambda^2}=0. \quad (1.21)$$

The boundary conditions for the differential equation of (1.21) are

$$\eta(0)=\phi_f(0)-\phi_{gf}+\frac{\Delta V_{FB}}{2(1+\frac{t_{Si}}{2\gamma t_{Ox}})}\equiv\eta_S \quad (1.22)$$

$$\eta(L_G)=\phi_f(L_G)-\phi_{gf}+\frac{\Delta V_{FB}}{2(1+\frac{t_{Si}}{2\gamma t_{Ox}})}\equiv\eta_D=\eta_S+V_D \quad (1.23)$$

where ϕ_f (0) equals the built-in potential between the source and the natural channel regions, V_{bi}, and it is given by

$$\phi_f(0) = V_{bi} = \frac{1}{\beta}\ln\left(\frac{N_D N_A}{n_i^2}\right). \tag{1.24}$$

N_D is the doping concentration in the source and drain regions. Then (1.21) is solved as

$$\eta(x) = \frac{\eta_S \sinh\left(\frac{L_G - x}{\lambda}\right) + \eta_D \sinh\left(\frac{x}{\lambda}\right)}{\sinh\left(\frac{L_G}{\lambda}\right)}. \tag{1.25}$$

The position x_m where ϕ_f is minimum and ϕ_f at x_m are

$$x_m = \frac{L_G}{2} - \frac{\lambda}{2}\ln\left(\frac{\eta_D}{\eta_S}\right) \tag{1.26}$$

$$\phi_f(x_m) = \phi_{gf} - \frac{\Delta V_{FB}}{2(1+\frac{t_{Si}}{2r_{Ox}})} + 2\sqrt{\eta_S \eta_D e^{-\alpha}} \tag{1.27}$$

where $\alpha = \frac{L_G}{2\lambda}$. (1.28)

It is assumed that a transistor switches on when $\phi_f(x_m)$ is ϕ_{sth}. From (1.27), the short channel threshold voltage shift, ΔV_{th}, is then given by

$$\Delta V_{th} = 2\sqrt{\eta_S \eta_D e^{-\alpha}}, \tag{1.29}$$

where ΔV_{th} is defined by

$$\Delta V_{th} = V_{thL} - V_{th}. \tag{1.30}$$

η_S and η_D are also functions of gate voltage, and hence they are also functions of V_{th}. Therefore, right hand side of (1.29) includes V_{th} and (1.29) leads to the second order equation of ΔV_{th} as

$$\left(\frac{1}{4}e^{2\alpha}-1\right)\Delta V_{th}^2-2\left(V_{bi}-2\phi_F+\frac{V_D}{2}\right)\Delta V_{th}-(V_{bi}-2\phi_F)(V_{bi}-2\phi_F+V_D)=0 \quad (1.31)$$

which gives

$$\Delta V_{th}=\frac{1}{\frac{1}{4}e^{2\alpha}-1}\left[\left(V_{bi}-2\phi_F+\frac{V_D}{2}\right)+\sqrt{\left(V_{bi}-2\phi_F+\frac{V_D}{2}\right)^2+\left(\frac{1}{4}e^{2\alpha}-1\right)(V_{bi}-2\phi_F)(V_{bi}-2\phi_F+V_D)}\right]. \quad (1.32)$$

Assuming $L_G >> \lambda$, and hence $e^{\alpha} >> 1$, (1.32) reduces to

$$\Delta V_{th}=2(V_{bi}-2\phi_F)\sqrt{1+\frac{V_D}{V_{bi}-2\phi_F}e^{-\alpha}}. \quad (1.33)$$

It is often used for threshold voltage shift due to the drain voltage (DIBL) [21], which is defined by

$$DIBL = V_{th}(V_D=0) - V_{th}(V_D). \quad (1.34)$$

Substituting (1.33) into (1.34), *DIBL* is given by

$$DIBL=\frac{2V_De^{-\alpha}}{\sqrt{1+\frac{V_D}{V_{bi}-2\phi_F}}+1}. \quad (1.35)$$

DIBL in limiting cases is simplified to

$$DIBL=\begin{cases} V_De^{-\alpha} & for\ V_D << V_{bi}-2\phi_F \\ 2\sqrt{V_D(V_{bi}-2\phi_F)}e^{-\alpha} & for\ V_D >> V_{bi}-2\phi_F \end{cases} \quad (1.36)$$

Therefore, *DIBL* is proportional to V_D when V_D is smaller than V_{bi}-$2\phi_F$, and proportional to the square root of V_D when V_D is larger than V_{bi}-$2\phi_F$. Therefore, the gradient of *DIBL* subjected to small V_D is

$$\frac{\partial DIBL}{\partial V_D}=e^{-\alpha}, \quad (1.37)$$

which is substantially related to the short channel parameters.

We assume that the sub-threshold-swing (S-swing) depends primarily on the carrier concentration, n_m, at x_m given by,

$$n_m = \frac{n_i^2}{N_A}\exp[\beta\phi_f(x_m)]. \tag{1.38}$$

S-swing is then derived as

$$S = \frac{\partial V_G}{\partial \log(I_D)} = \ln 10 \frac{\partial V_G}{\partial \log(n_m)} = \frac{\ln 10}{\beta}\frac{1}{\frac{\partial \phi_f(x_m)}{\partial V_G}} = \frac{\ln 10}{\beta}\frac{1}{1-\frac{2\eta_S + V_D}{\sqrt{\eta_S(\eta_S + V_D)}}e^{-\alpha}} \tag{1.39}$$

When $V_G = V_{thL} - \phi_F$, (1.39) becomes

$$S = \frac{\ln 10}{\beta}\frac{1}{1-\frac{2(V_{bi}-\phi_F)+V_D}{\sqrt{(V_{bi}-\phi_F)}(V_{bi}-\phi_F+V_D)}e^{-\alpha}}. \tag{1.40}$$

When the drain voltage, V_D, is small (1.40) reduces to

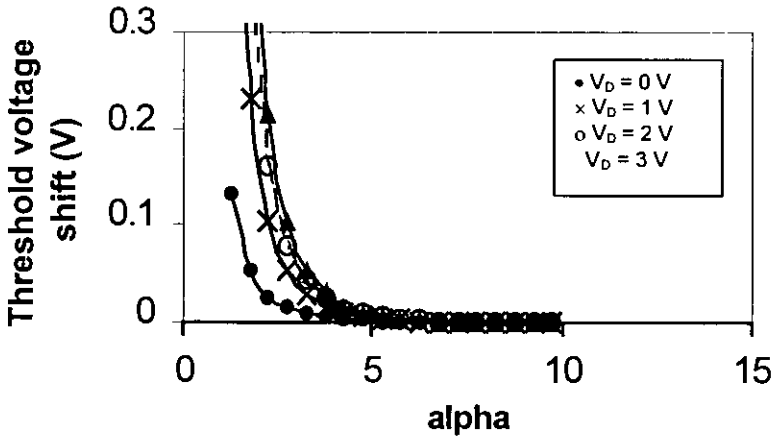
$$S = \frac{\ln 10}{\beta}\frac{1}{1-2e^{-\alpha}}. \tag{1.41}$$

D. Results and Discussions

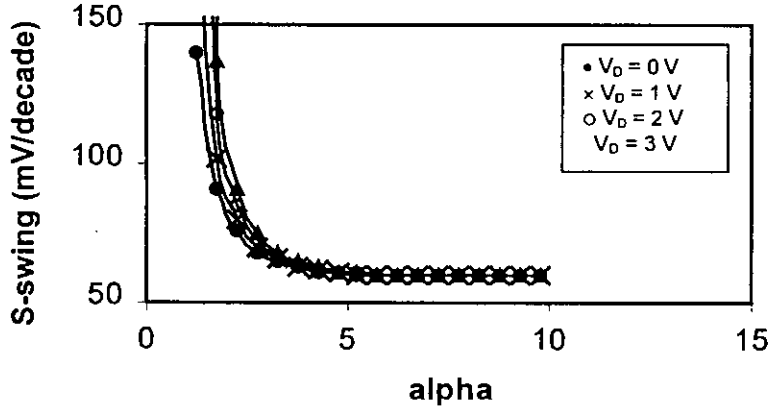
The dependence of ΔV_{th} and S-swing on α(alpha) are shown in Fig. 1.7. The allowable ΔV_{th} and S-swing are not clearly determined, but the ranges are roughly ΔV_{th} of below 0.2 V (Fig. 1.7(a)) and S-swing of below 100 mV/decade (Fig. 1.7(b)). Smaller ΔV_{th} and S-swing values require a larger α. Again the short-channel effects are negligible when α is above 5. However, a larger α requires a thinner gate oxide or thinner SOI layer. Therefore, we should select α to be as small as possible to relax the process margin in consideration of the desired ΔV_{th} and S-swing.

After determining desired ΔV_{th} and S-swing from (1.33) and (1.40), corresponding α values are given by

$$\alpha(\Delta V_{th}) = \ln\left[\frac{2(V_{bi}-2\phi_F)\sqrt{1+\dfrac{V_D}{V_{bi}-2\phi_F}}}{\Delta V_{th}}\right] \tag{1.42}$$



(a)



(b)

Fig. 1.7. Dependence of short channel effects on scaling parameter α ($L_G/2\lambda$): (a) Threshold voltage lowering/shift, ΔV_{th}, and (b) Sub-threshold-swing, S-swing.

$$\alpha(S) = \ln\left[\frac{2(V_{bi}-2\phi_F)+V_D}{\sqrt{(V_{bi}-2\phi_F)(V_{bi}-2\phi_F+V_D)}\left(1-\frac{\ln 10}{S\beta}\right)}\right] \tag{1.43}$$

Since a larger α value requires a smaller t_{Ox} or t_{Si}, the device should be designed using the larger α satisfying the requirements for both ΔV_{th} and S-swing. The final α (α_F) should be such that,

$$\alpha_F = max[\alpha(\Delta V_{th}), \alpha(S)] \tag{1.44}$$

From (1.42) and (1.43) both α's depend on ΔV_{th}, V_D and S-swing. As shown in [22], the value of α is between 1 and 3 for our device parameters.

E. Scalability

In this section using the scaling theory of bulk MOSFETs, we will evaluate the scalability of the above mentioned device. The supply voltage is decreased with decreasing the gate length adhering the scaling theory of the bulk MOSFETs as in [23]

$$V_{DD} = 1.8\sqrt{\frac{L_G(\mu m)}{0.18\mu m}}V \tag{1.45}$$

To improve the transconductance, the gate oxide thickness should be such that,

$$t_{Ox} = \begin{cases} 3\dfrac{L_G(\mu m)}{0.1\mu m}nm & for \quad L_G > 0.1\mu m \\ 3nm & for \quad L_G < 0.1\mu m \end{cases} \tag{1.46}$$

where the gate oxide thickness is limited to 3 nm due to tunneling [24]. To set a proper threshold voltage, the SOI thickness is taken to be

$$t_{Si} = 4t_{Ox} \tag{1.47}$$

This provides a V_{thL} about 0.2 V, independent of gate length [22]. From (1.32) and (1.40) we can observe the dependence of S-swing and ΔV_{th} on L_G. For gate length,

L_G > 0.1 μm, short-channel effects cannot be observed as t_{Ox} and t_{Si} decrease linearly with the decrease of L_G and α remains constant at 6.8. But as L_G decreases below 0.1 μm, short-channel effects arise and at the gate length of 0.05 μm, ΔV_{th} is 0.025 V and S-swing is 65 mV/decade. This can be taken as the scalability limit of this device. This limitation can be overcome if a gate oxide thinner than 3 nm could be used.

F. Summary

Starting from the bulk MOSFETs, we have discussed the problems associated with the operation of MOSFETs in the deep-sub-micrometer regimes. In several respects the double-gated SOI MOSFETs offer better characteristics than the conventional bulk Si MOSFETs. These improvements arise because it has gate electrodes on both sides of the channel, rather than only on one side as in conventional MOSFETs. When there are two gates, the electric field generated by the drain electrode is better screened from the source end of channel. Also, two gates can control roughly twice as much current as a single gate resulting in stronger switching signals. However, the developed scaling theory for DG-SOI MOSFETs works well when gate length ≥0.1 μm. In the push to make MOSFETs gate length smaller than 0.1 μm (i.e., deep-sub-micrometer regime), it is necessary to change the structure of MOSFETs in order to achieve satisfactory electrical behaviour and short-channel effects immunity.

A comparative study has been shown between p^+-p^+ and n^+-p^+ DG-SOI MOSFETs, giving n^+-p^+ a better solution for operation in the deep-sub-micrometer regimes. A threshold voltage model has been derived for this device. The short-channel effect is expressed by the function of $\exp(-L_G/2\lambda)$, where λ is

$$\lambda = \sqrt{\frac{\gamma t_{Si} t_{Ox}}{2}}.$$

Using this theory, we evaluated the scalability of the device. When L_G is 0.05 μm, t_{Ox}=3 nm and $t_{Si} = 4t_{Ox}$, a device with a V_{th} of about 0.2 V, a ΔV_{th} of 0.025 V, and an S-swing of 65 mV/decade are obtained. Further scaling is possible if the gate oxide thinner than 3 nm could be used which may cause tunneling through the oxide and can degrade the performances of the devices. Therefore, alternative solutions/structures should be found out in order to have better short-channel effects immunity of SOI MOSFETs in the deep-sub-micrometer regime.

1.4 Objectives of the Present Research

The main objective of this research is to develop a novel physics-based analytical model for threshold voltage shift in short channel fully-depleted cylindrical gate MOSFET. Temperature dependence model of threshold voltage and threshold voltage shift in cylindrical gate MOSFET will also be developed. The objectives, at large are as follows:

To develop an accurate expression for channel potential of a thin-film fully-depleted cylindrical gate MOSFET.

To develop a novel physics-based analytical model for threshold voltage shift of a thin-film fully-depleted cylindrical gate MOSFET.

To develop a temperature dependence model for threshold voltage and threshold voltage shift of cylindrical gate MOSFET.

To compare the short-channel effects of novel cylindrical gate MOSFET with those of the double gate SOI MOSFET.

1.5 Organisation of the Thesis

This thesis is organised into four chapters. The theoretical background of semiconductor electronics and integrated circuit (IC) technology is presented in chapter 1. Research survey related to various kinds of MOSFETs is also presented in this introductory chapter, with an emphasis on DG-SOI MOSFETs.

Chapter 2 presents sequentially a model for channel potential using Poisson's equation, then the model for threshold voltage shift, temperature dependence of threshold voltage of a cylindrical gate MOSFET. Short-channel effect models of cylindrical gate MOSFET are also compared with those of DG-SOI MOSFETs in this chapter.

The results and discussions are presented in chapter 3.

Chapter 4 presents the conclusions of this research and offers suggestions for further study.

CHAPTER 2

ANALYTICAL MODELLING OF SHORT CHANNEL EFFECTS IN THIN FILM FULLY DEPLETED CYLINDRICAL GATE MOSFET

2.1 Introduction

The state of the art VLSI/ULSI technology requires deep sub-micrometer MOS transistors to achieve higher packing density and lower power consumptions. Conventional bulk and epitaxial MOSFETs [25, 26] are not suitable in the deep sub-micrometer regime because of higher junction capacitances and other short-channel effects causing severe problems such as threshold voltage shift/lowering, substrate bias effect, drain induced barrier lowering (DIBL), sub-threshold current, impurity scattering, etc. [3, 5]. Single-gate SOI MOSFETs have been developed to overcome some of the above mentioned short-channel effects [27, 28]. DG SOI MOSFETs are free from the bulk MOSFETs scaling limit [8, 10]. Although superb short-channel effect immunity, higher transconductance and ideal sub-threshold factor have been reported by many theoretical and experimental studies on DG SOI MOSFET [13, 15, 29], the extensive use of this device is limited by higher cost, process complexity and tunneling through thinner (<3 nm) oxide. Therefore, alternative strutures should be developed for deep-sub-micrometer MOS devices.

In order to overcome above problems, a novel cylindrical gate MOS structure has already been proposed [30]. The cylindrical gate MOSFET has greater control over the channel potential, smaller substrate bias effect and higher

reliability over the conventional planar transistors. A device with such numerous advantages over the conventional MOSFETs needs to be investigated in details. In past the studies on cylindrical gate MOSFETs have been on fabrication procedures [30] and scaling theory [31]. Until now very few papers are available on modelling of cylindrical gate device.

In this chapter analytical models for short-channel effects and temperature dependence of threshold voltage in fully-depleted cylindrical gate MOSFET have been developed. The analytical results will be compared to those of DG SOI MOSFETs.

2.2 Model Development

2.2.1 Derivation of DG-SOI MOSFET Natural Length

Scaling theory of DG-SOI MOSFETs has already been developed in section 1.3.3. According to this theory, the device should be designed maintaining,

$$\alpha = \frac{L_G}{2\lambda}. \tag{2.1}$$

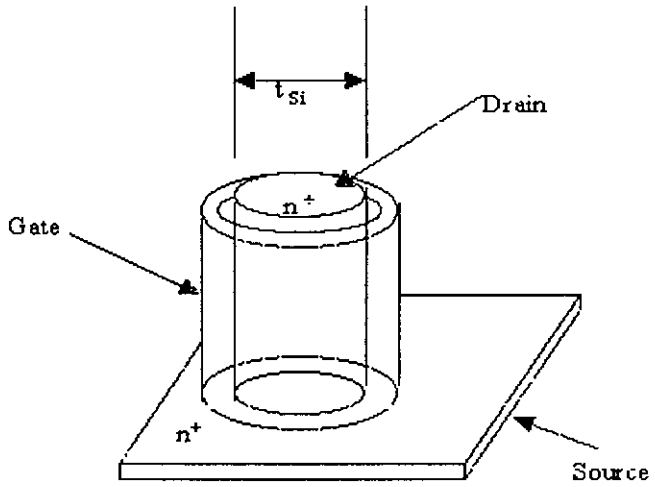
Where L_G is the gate length and λ is the so-called natural length, which characterizes the short-channel effect. As mentioned earlier, this natural length is an easy guide for choosing device parameters and has simple physical meaning that a small natural length corresponds to superb short channel effect immunity. For DG SOI MOSFETs natural length is found to be (from equation 1.13)

$$\lambda_{DG} = \sqrt{t_{Si} t_{ox} \frac{\epsilon_{Si}}{2\epsilon_{ox}}}. \tag{2.2}$$

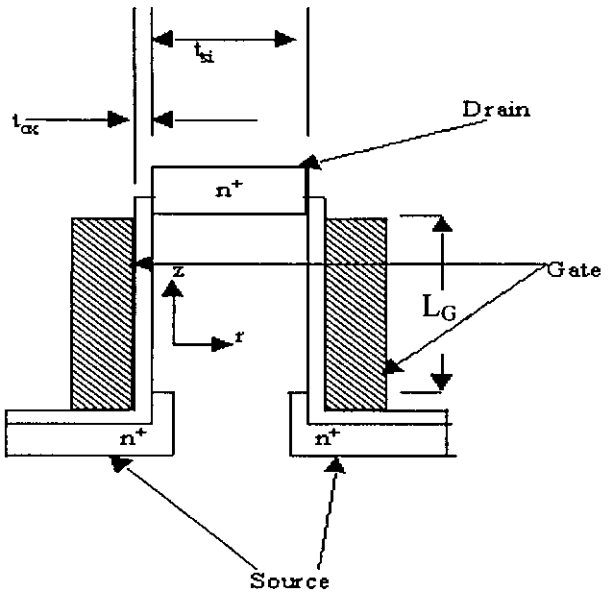
Where t_{Si} is the silicon thickness, t_{ox} is the oxide thickness, ε_{Si} is the permittivity of silicon and ε_{ox} is the permittivity of oxide.

2.2.2 Derivation of Cylindrical Natural Length

Figure 2.1(a) shows a cylindrical gate MOSFET and it's cross-sectional view is shown in Fig. 2.1(b). Poisson's equation for potential, $\phi(r, z)$, in the cylindrical coordinates is given by



(a)



(b)

Fig. 2.1. (a) Cylindrical gate MOSFET and (b) cross-sectional view of cylindrical gate MOSFET.

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\phi(r,z)\right)+\frac{\partial^2}{\partial z^2}\phi(r,z)=\frac{qN_A}{\varepsilon_{si}}, \tag{2.3}$$

where N_A is the channel doping (assumed to be uniform) and q is electronic charge. The potential distribution of a MOSFET can be approximated by a parabolic profile in the radial direction [20] and is given by;

$$\phi(r,z)=c_0(z)+c_1(z)r+c_2(z)r^2, \tag{2.4}$$

where $c_0(z)$, $c_1(z)$ and $c_2(z)$ are contants. Three boundary conditions required for the solution are listed below:

(i) The center potential (ϕ_c) is a function of z only

$$\phi(0, z) = \phi_c(z) = c_0(z). \tag{2.5a}$$

(ii) The electric field in the center of the silicon pillar is zero

$$\frac{d}{dr}\phi(r,z)\Big|_{r=0} = 0 = c_1(z). \tag{2.5b}$$

(iii) The electric field at the silicon/oxide interface can be derived from the gate potential (ϕ_{gs}), the surface potential (ϕ_s), and silicon pillar and gate oxide thicknesses

$$\left.\frac{d}{dr}\phi(r,z)\right|_{r=\frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\phi_{gs}-\phi_s(z)}{\frac{t_{si}}{2}\ln\left(1+\frac{2t_{ox}}{t_{si}}\right)}\right) = t_{si}c_2(z). \tag{2.5c}$$

Substituting (2.4) in (2.3) and considering the boundary conditions (2.5) as given in [31], the expression for $\phi(r, z)$ in the silicon film has been obtained as;

$$\phi(r,z)=\phi_c(z)+\left(\frac{2\varepsilon_{ox}r^2(\phi_c(z)-\phi_{gs})}{\varepsilon_{si}t_{si}^2\ln\left(1+\frac{2t_{ox}}{t_{si}}\right)}\right) \tag{2.6}$$

where $\phi_c(z)$ is the center potential, ϕ_{gs} is the gate potential, ε_{ox} is the dielectric permittivity of oxide, ε_{si} is the dielectric permittivity of silicon, t_{si} is the silicon film thickness and t_{ox} is the oxide layer thickness. Using this potential, Poisson's equation can be solved at the pillar center, r = 0

$$\frac{\partial^2}{\partial z^2}\phi_c(z) + \frac{\left(\phi_c(z) - \phi_{gs}\right)}{\lambda_{CL}^2} = \frac{qN_A}{\varepsilon_{si}} \tag{2.7}$$

where λ_{CL} is

$$\lambda_{CL} = \sqrt{\frac{\varepsilon_{si} t_{si}^2 \ln(1 + \frac{2t_{ox}}{t_{si}})}{8\varepsilon_{ox}}} \tag{2.8}$$

λ_{CL}, the natural length of cylindrical gate MOSFET, has the same physical significance as λ_1 and λ_2 (equation 1.12 & 1.13) given by Yan et al. [9] and Suzuki et al. [22], respectively.

The remaining analysis is identical to work done by Yan et al. [9] resulting in a scaling parameter, α_{CL}, for cylindrical gate MOSFET of

$$\alpha_{CL} = \frac{L_G}{2\lambda_{CL}}. \tag{2.9}$$

2.3 Threshold Voltage Shift (ΔV_{th}) Model

Assuming $L_G >> \lambda_{DG}$, threshold voltage shift for DG-SOI MOSFET is given by equation (1.33) as

$$\Delta V_{thDG} = 2(V_{bi} - 2\phi_F)\sqrt{1 + \frac{V_D}{V_{bi} - 2\phi_F} e^{-\alpha_{DG}}}\ , \tag{2.10}$$

where V_{bi} built-in potential, ϕ_F is the Fermi level potential and V_D is drain voltage. The threshold voltage shift for cylindrical gate MOSFET is identical to equation (2.10) with α_{DG} replaced by α_{CL} of equation (2.10) and is given by

$$\Delta V_{thCL} = 2(V_{bi} - 2\phi_F)\sqrt{1 + \frac{V_D}{V_{bi} - 2\phi_F} e^{-\alpha_{CL}}} \,. \tag{2.11}$$

It is often used for threshold voltage shift due to the drain voltage known as *DIBL*. For DG-SOI MOSFET, *DIBL* is given by equation (1.35) as

$$DIBL = \frac{2V_D e^{-\alpha_{DG}}}{\sqrt{1 + \frac{V_D}{V_{bi} - 2\phi_F}} + 1}. \tag{2.12}$$

The same *DIBL* expression can be used for cylindrical gate MOSFET with α_{DG} replaced by α_{CL} of equation (2.12) and is given by

$$DIBL = \frac{2V_D e^{-\alpha_{CL}}}{\sqrt{1 + \frac{V_D}{V_{bi} - 2\phi_F}} + 1}. \tag{2.13}$$

2.4 Model for Sub-threshold Swing (S-swing)

An important parameter characteristic of sub-threshold region of MOSFET operation is sub-threshold swing (*S-swing*), defined as the change in the gate voltage required to reduce the drain current (I_D) by one decade. The sub-threshold swing primarily depends on the carrier concentration [22] and is given by equation (1.40) for a DG-SOI MOSFET as

$$S-swing=\frac{\ln 10}{\beta}\frac{1}{1-\frac{2(V_{bi}-\phi_F)+V_D}{\sqrt{(V_{bi}-\phi_F)}(V_{bi}-\phi_F+V_D)}e^{-\alpha_{DG}}}. \tag{2.14}$$

When the drain voltage, V_D, is small (2.14) reduces to

$$S-swing=\frac{\ln 10}{\beta}\frac{1}{1-2e^{-\alpha_{DG}}}. \tag{2.15}$$

For cylindrical gate MOSFET, equations (2.14) and (2.15) can be expressed by the equations (2.16) and (2.17), respectively.

$$S-swing=\frac{\ln 10}{\beta}\frac{1}{1-\frac{2(V_{bi}-\phi_F)+V_D}{\sqrt{(V_{bi}-\phi_F)}(V_{bi}-\phi_F+V_D)}e^{-\alpha_{CL}}}. \tag{2.16}$$

$$S-swing=\frac{\ln 10}{\beta}\frac{1}{1-2e^{-\alpha_{CL}}}. \tag{2.17}$$

2.5 Temperature Dependent Model for V_{th}

Threshold voltage, V_{th}, is the critical voltage at which the inversion layer is formed to a significant extent, giving rise to rapid increase of the inversion charge for higher gate voltages. In other words, the threshold voltage specifies the gate voltage at the onset of strong inversion. This voltage takes into account the flat-band voltage, the moderate inversion onset voltage (i.e. $2\phi_F$) and voltage due to depletion layer and oxide layer charges. Threshold voltage is a very significant parameter of a MOS circuit. Generally, a lower threshold voltage is desirable since it allows the use of a small supply voltage and so lower power consumption. Lower threshold voltage also allows smaller swing during switching.

The thermal characterization is essential when the device is scaled down and operated over a large temperature range. SOI technologies extended the temperature range of the device substantially [32, 33]. In this section, a temperature dependent model of a short channel cylindrical gate MOSFET has been proposed for the first time with a Gaussian doping profile. The results obtained from this model will be compared with those of DG-SOI MOSFETs.

A non-uniform doping distribution [34] caused by thermal annealing which resembles a Gaussian distribution is given by

$$N_A(r) = \frac{Q}{\sigma\sqrt{2\pi}} \exp\left(\frac{-(r-R_p)^2}{2\sigma^2}\right) \tag{2.18}$$

where Q is the channel implant dose, R_p is the projected range and σ is standard deviation. Following Young [20], the potential distribution in the silicon film can be approximated by a parabolic profile for low source-drain voltages. Considering the boundary conditions as given in [31] and following the approach of [22], the expression for short channel threshold voltage is obtained as

$$V_{thCL} = V_{FB} + 2\phi_F + \frac{qN_A t_{si}^2 \ln\left(1+\frac{2t_{ox}}{t_{si}}\right)}{8\varepsilon_{ox}} - \Delta V_{thCL} \tag{2.19}$$

where V_{FB} denotes the flat-band voltage, ϕ_F denotes the Fermi potential, N_A is the doping concentration of the silicon film and ΔV_{thCL} is the short channel threshold voltage shift which is obtained as

$$\Delta V_{thCL} = \frac{-b+\sqrt{(b^2-4ac)}}{2a} \tag{2.20}$$

where

$$a = \sinh^2\left(\frac{L_G}{\lambda_{CL}}\right) - \left(\exp\left(\frac{L_G}{\lambda_{CL}}\right) + \exp\left(\frac{-L_G}{\lambda_{CL}}\right) - 2\right),$$

$$b = -\left[\exp\left(\frac{L_G}{\lambda_{CL}}\right) + \exp\left(\frac{-L_G}{\lambda_{CL}}\right) - 2\right].\left[2(V_{bi} - 2\phi_F) + V_D\right]$$

$$\text{and } c = -(V_{bi} - 2\phi_F)\left(\exp\left(\frac{L_G}{\lambda_{CL}}\right) + \exp\left(\frac{-L_G}{\lambda_{CL}}\right) - 2\right).\left[(V_{bi} - 2\phi_F) + V_D\right] - {V_D}^2$$

Also, following [22] the expression for threshold voltage for a DG-SOI MOSFET is derived as

$$V_{thDG} = V_{FB} + 2\phi_F + \frac{k_B T}{q}\ln\left(\frac{4\varepsilon_{si}}{{t_{si}}^2 k_B T N_A}\right) + \frac{qN_A {t_{si}}^2}{8\varepsilon_{si}}\left(1 + \frac{4\varepsilon_{si}}{{t_{si}}^2 k_B T N_A}\right) - \Delta V_{thDG} \quad (2.21)$$

where ΔV_{thDG} is given by (2.20), in which characteristics length is expressed as in equation (2.2) instead of equation (2.8).

The temperature dependence of threshold voltage can be obtained by temperature sensitive parameters like silicon band gap, built-in potential, Fermi potential, flat-band voltage, intrinsic carrier concentration and ionized doping concentration the expressions of which are given in [34-37].

In the present analysis the temperature range studied has been divided into two regions – low temperature region and intermediate temperature region. The formulae for the Fermi level and the corresponding carrier concentration in both regions were obtained similar to that given in [38]. The expressions of carrier concentrations and Fermi levels as a function of temperature thus derived are substituted in equations (2.19) and (2.21) to obtain temperature dependence of threshold voltage.

CHAPTER 3

RESULTS AND DISCUSSIONS

Following the theoretical analysis presented in chapter 2, the models for short-channel effects, such as threshold voltage shift, channel shortening effect, oxide thickness on natural/characteristic length, etc. of cylindrical gate MOSFET are simulated and tested on a microcomputer by computer programs. These programs written in Turbo C++, provide a lucid and flexible simulation environment so that each model can be easily checked and tested from diverse point of view. The results obtained from the analysis were compared to those of the DG-SOI MOSFETs to show the short-channel effect immunity of novel thin-film fully-depleted cylindrical gate MOSFET in sub-micrometer and deep-sub-micrometer regimes.

As mentioned in chapter 2, the natural/characteristic length of SOI device plays important role in determining its sub-threshold characteristics. In fact, characteristic length has the simple physical meaning that a small natural length corresponds to superb short channel effect immunity. For $t_{Si}/2 >> t_{ox}$ (usual case) and comparing (2.2) and (2.8) we find that,

$$\lambda_{DG} = 1.4142\lambda_{CL} \tag{3.1}$$

The factor 1.4142 reduces the characteristic length of a cylindrical gate structure by ~29.3% ($\lambda_{CL} = 0.707\lambda_{DG}$) in comparison to a double gate structure assuming the same silicon dimensions, t_{ox} and doping geometry, thereby enabling a larger α ($L_G/2\lambda$), giving greater short channel immunity and improved sub-threshold

characteristics over double gate structure. This can be understood to result from the tighter confinement present in the cylindrical MOSFET – whereas the DG structure has only one small transverse dimension, the cylindrical structure offers confinement from all transverse directions. This tighter confinement leads to a faster exponential decay of the potential along the channel length.

In Fig. 3.1, we compare λ for a DG- and a CL-MOSFET as a function of t_{ox}. We can clearly see the advantage of the cylindrical structure, which gives a ~29% smaller λ compared to the DG structure.

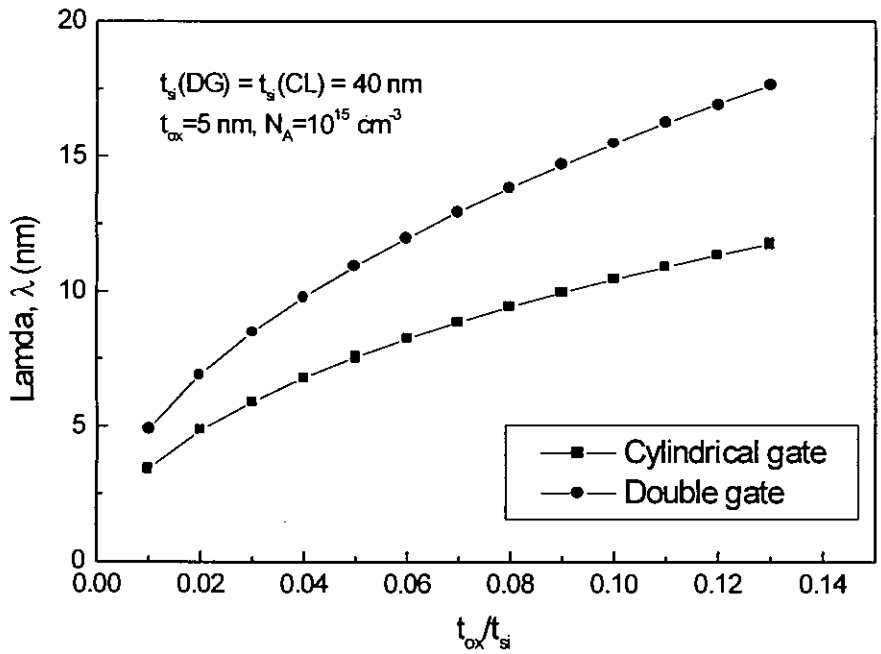


Fig. 3.1. Comparison of DG- and CL-MOSFET results of natural/characteristic lengths, λ, for identical device dimensions.

For t_{Si}=1.273 μm and t_{ox}=20 nm, equations (2.10) and (2.11) are plotted for various gate lengths (L_G > 0.25 μm, i.e. above deep-sub-μm regime) and drain voltages in Fig. 3.2 and Fig. 3.3, respectively. From Fig.3.2, it is seen that the cylindrical gate device has reduced short channel effect when compared with

double gate structure. This is due to the difference in characteristic lengths in two devices. Figure 3.3 indicates that the variation of threshold voltage shift with drain voltage is more dominant in double gate as compared to cylindrical gate devices and hence *DIBL* is less prominent in cylindrical gate devices.

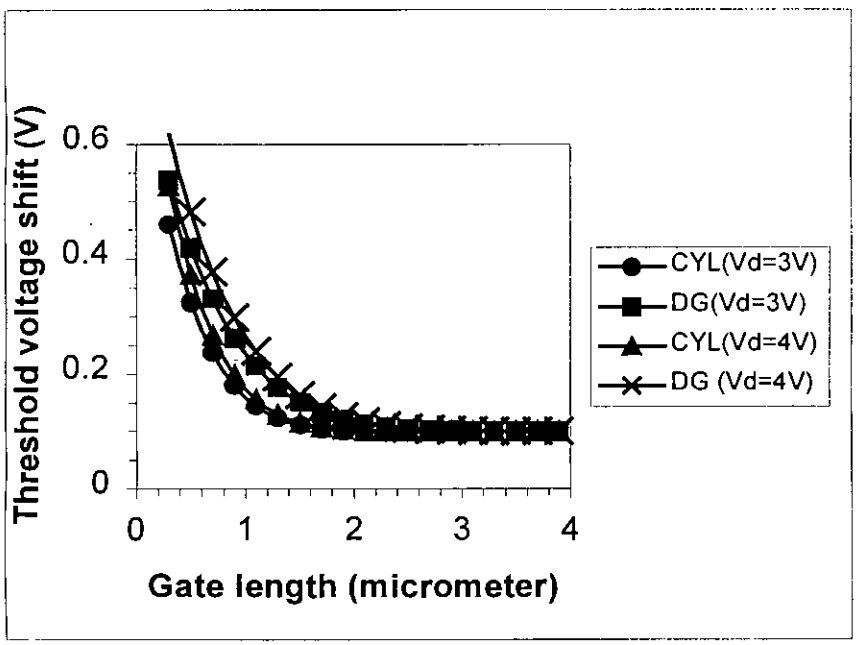


Fig. 3.2. Variation of threshold voltage shift with gate length above deep-sub-μm regime for cylindrical and double gate devices.

In the deep-sub-μm regime, equations (2.10) and (2.11) are also plotted in Fig. 3.4 and Fig. 3.5. Figure 3.4 shows the threshold voltage shift as a function of gate length at different values of drain voltage for both cylindrical and double gate devices. As the gate length is increased the threshold voltage shift decreases and eventually will approach a lowest fixed value signifying long channel (L_G> 1 μm) operation (Fig. 3.2). The *DIBL* effect is also more predominant in double gate devices when compared to cylindrical gate device structure in the deep-sub-μm

regime (Fig. 3.5). These govern greater short-channel effect immunity of the cylindrical gate structure.

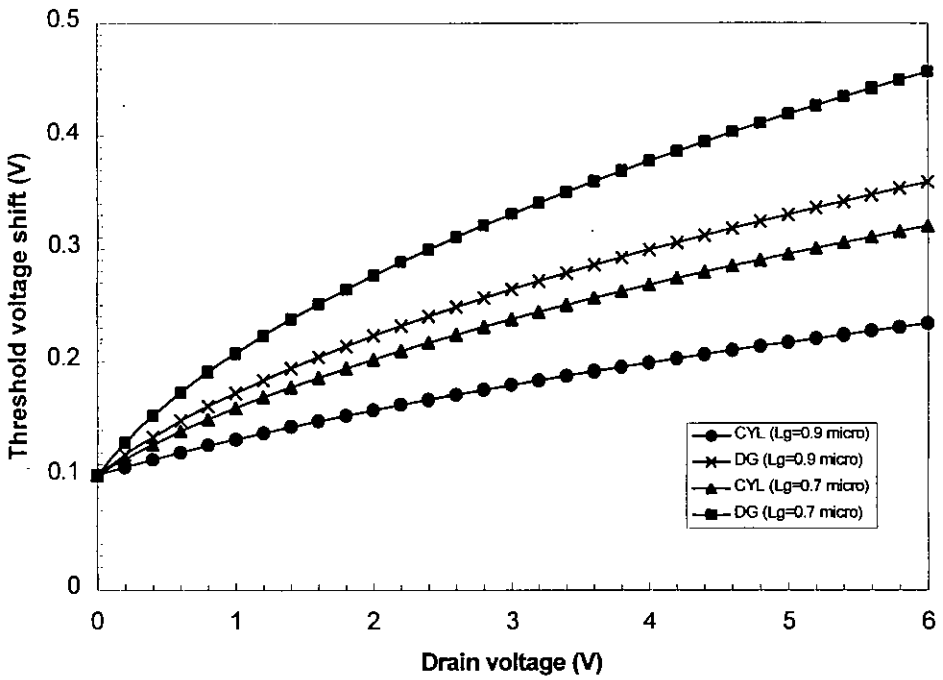


Fig. 3.3. Variation of threshold voltage shift with drain voltage above deep-sub-μm regime for cylindrical and double gate devices.

For different values of drain voltage, the variations of threshold voltage shift with alpha, sub-threshold swing (S-swing) with alpha and DIBL with alpha are shown in Fig. 3.6, Fig. 3.7 and Fig. 3.8, respectively. The shapes of all curves are almost identical signifying long channel operation. From these graphs it is clear that *DIBL* increases with the increase in drain voltage.

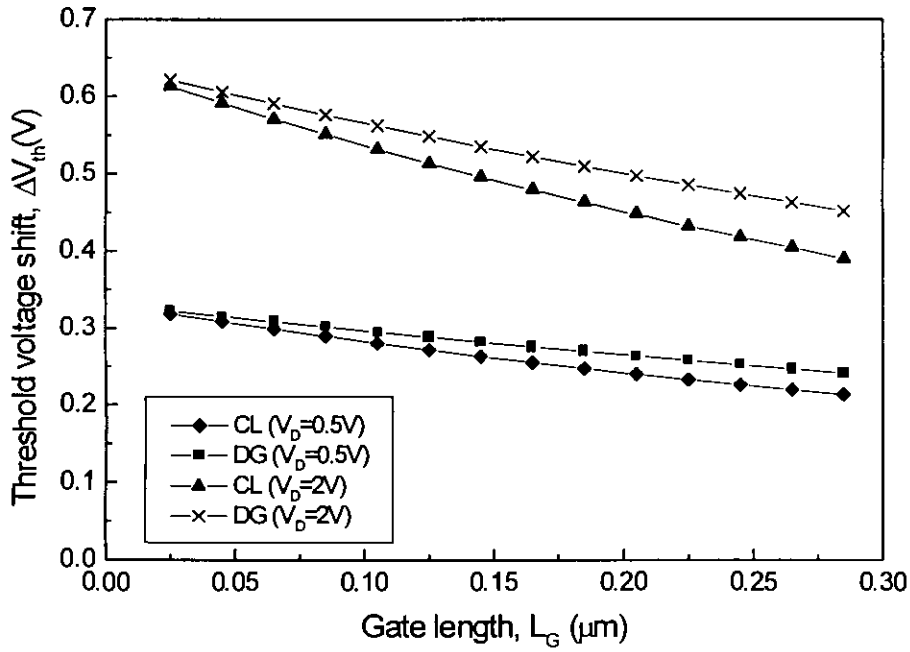


Fig. 3.4. Variation of threshold voltage shift with gate length in the deep-sub-μm regime for cylindrical and double gate devices.

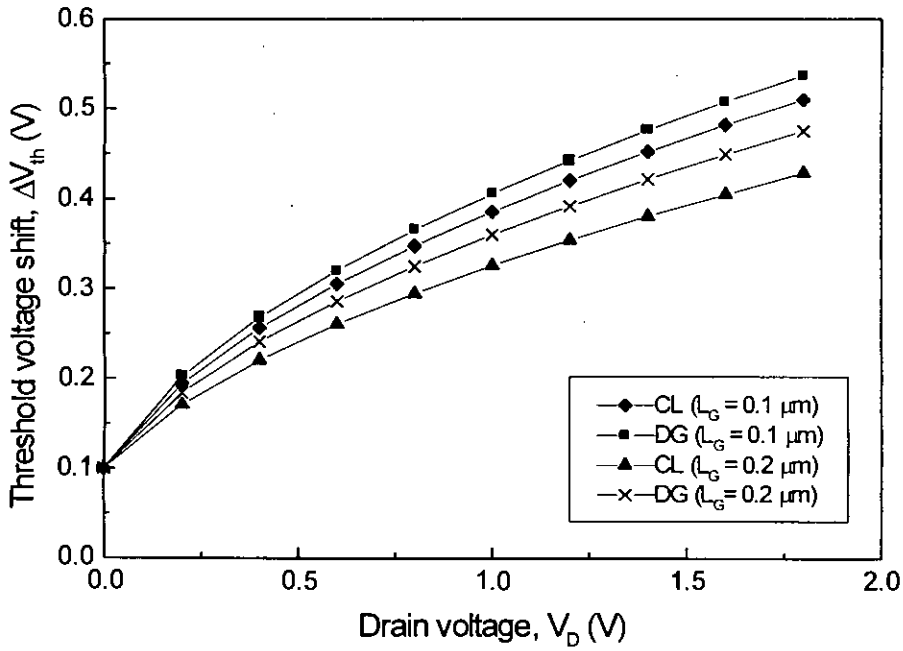


Fig. 3.5. Variation of threshold voltage shift with drain voltage in the deep-sub-μm regime for cylindrical and double gate devices.

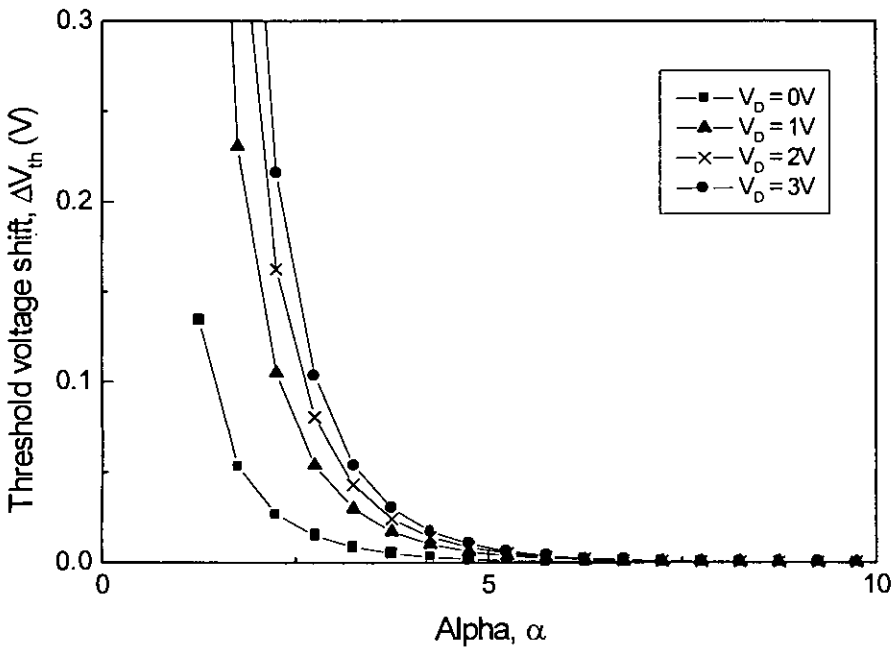


Fig. 3.6. Variation of threshold voltage shift with alpha for different values of drain voltage.

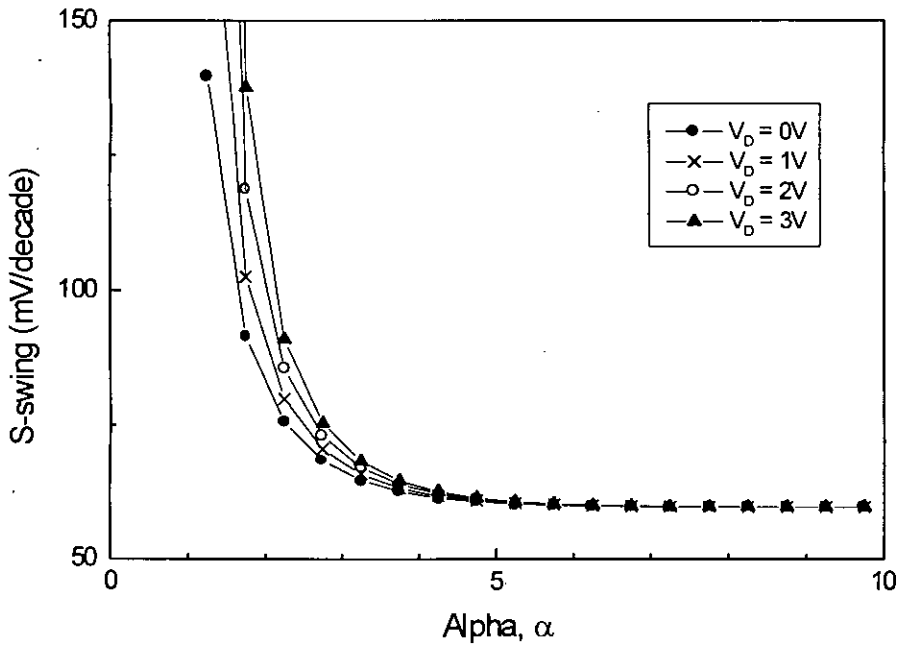


Fig. 3.7. Variation of sub-threshold swing with alpha for different values of drain voltage.

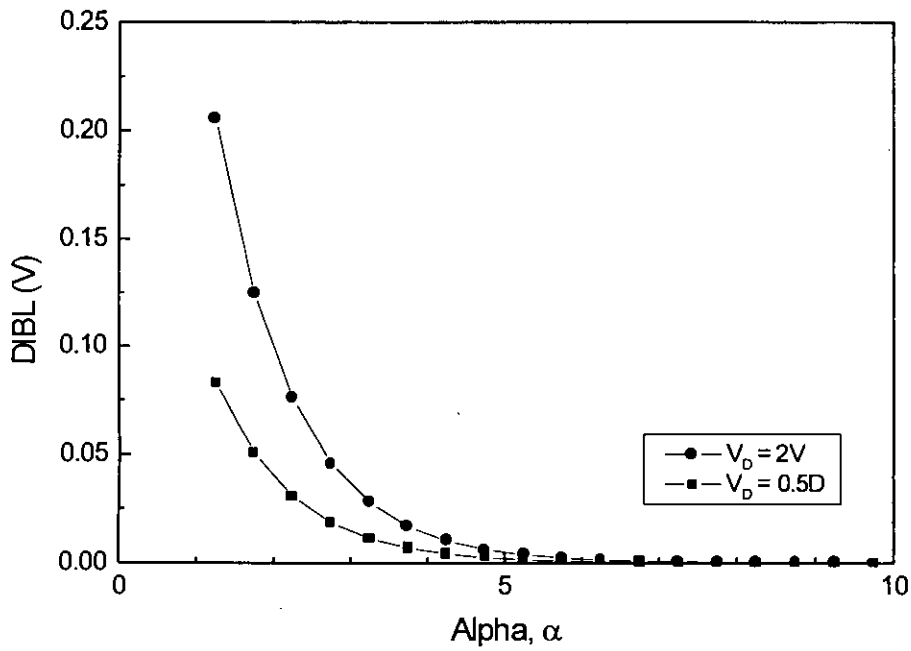


Fig. 3.8. Variation of *DIBL* with alpha for different values of drain voltage.

For a given silicon thickness, t_{si}, and oxide thickness, t_{ox}, it is possible to determine a minimum gate length, L_G. A plot of the minimum L_G versus the silicon thickness, t_{si}, illustrates the advantage of a cylindrical device when compared to a double-gate device (Fig. 3.9). Under the given conditions, the minimum gate length is ~30% smaller for a cylindrical channel. This is particularly important for vertical surrounding-gate structures, where the silicon thickness, t_{si}, is limited by available lithography.

The variations of threshold voltage with temperature for cylindrical and double gate devices are shown in Fig. 3.10. As gate length is decreased, drain and source regions overlap and as a result the effective charge reduces thereby reducing the threshold voltage. It is also observed that the threshold voltage reduces when the temperature is increased. The temperature dependence Fermi potential and flat-band voltage primarily governs this threshold voltage reduction. From Fig. 3.10 it can also be seen that the threshold voltage of the cylindrical device is lower than that of double gate device and is predominantly due to the

difference in device geometry. Since the cylindrical structure has gate wrapped all around the channel, hence at a comparatively small value of the gate voltage a channel will be formed and the corresponding value of the threshold voltage will be lower than that of a double gate device. An increase in temperature will cause the generation of carriers in the silicon film, which causes the threshold voltage to become negative. At this stage the device operation changes from enhancement mode to depletion mode. Moreover, with increase in temperature threshold voltage difference between the long channel (5 μm) and the short channel (0.2 μm) decreases. This difference is found to be 0.076V at 77K and 0.06V at 520K for cylindrical gate device. For double gate device, this difference is 0.27V at 77K and 0.25V at 520K. An increase in the difference at low temperatures is due to the increase in depletion layer thickness which intern depends on the temperature dependence of the Fermi level. As the temperature decreases the Fermi level approaches the band edge and the mobile carriers begin to freeze out. Thus short channel effects are more predominant at lower temperatures.

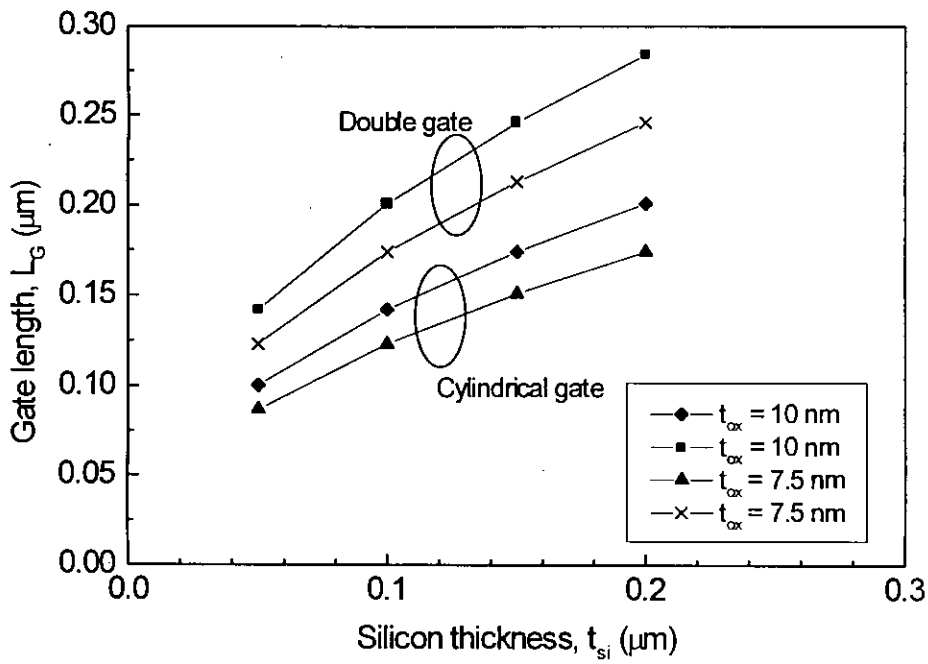


Fig. 3.9. Variations of gate length, L_G, with silicon thickness, t_{si}, for particular oxide thickness, t_{ox}, of cylindrical and double gate devices.

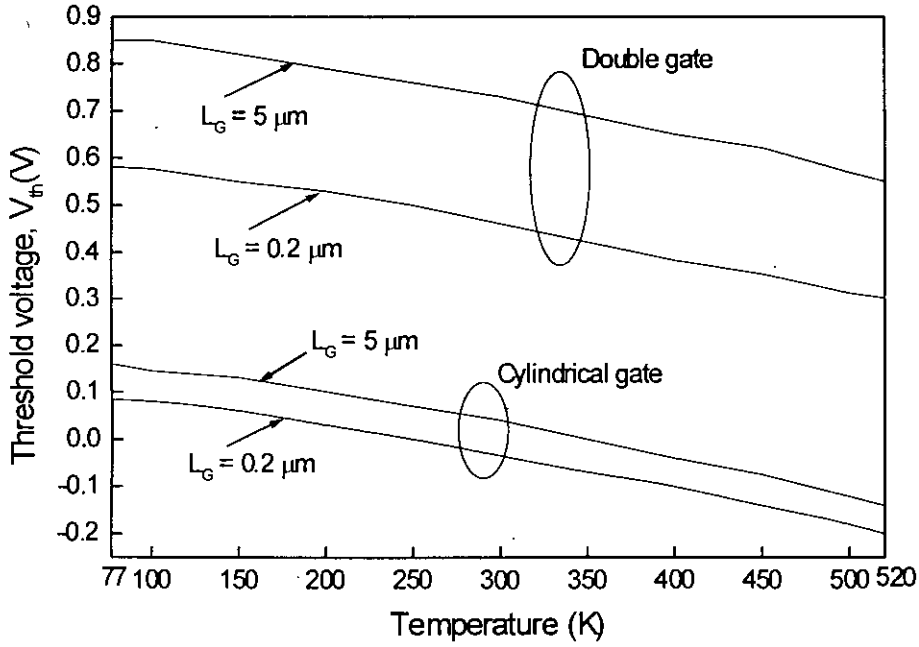


Fig. 3.10. Variation of threshold voltage, V_{th}, with temperature for different gate lengths (Q =1.12 x 10^{16} m^{-2}, R_p = 3.9 x 10^{-2} μm, σ = 2.9878 x 10^{-2} μm).

Figure 3.11 shows a plot of threshold voltage shift versus gate length for cylindrical and double gate devices at 300K. Here we also see that cylindrical gate device exhibits better short channel effect immunity compared to double gate structure.

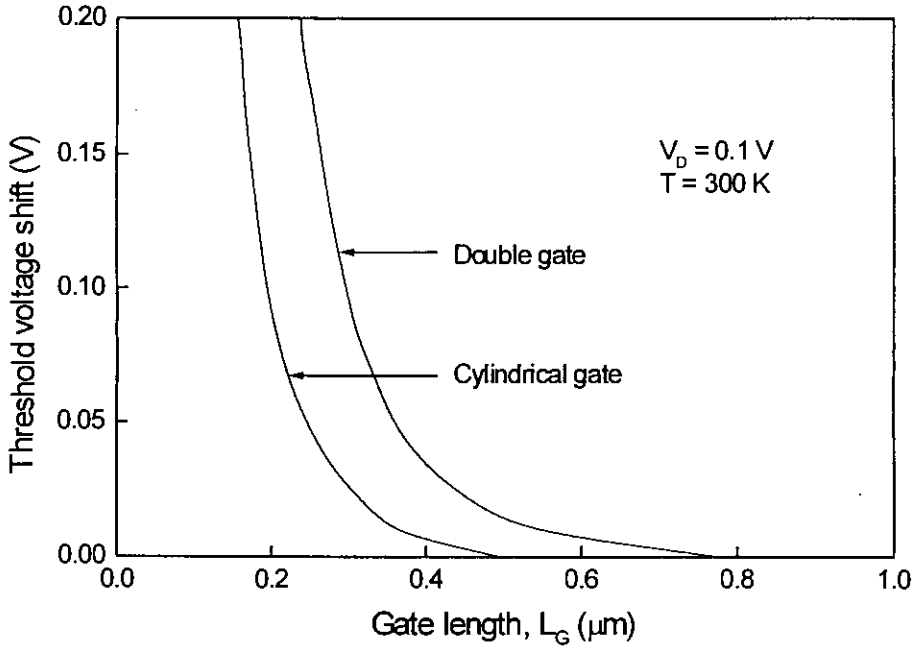


Fig. 3.11. Variation of threshold voltage shift, ΔV_{th}, with gate length, L_G, for cylindrical and double gate devices.

CHAPTER 4

CONCLUSIONS AND SUGGESTIONS FOR FUTURE RESEARCH

4.1 Conclusions

It is important to model and predict circuit behaviour in the early state of technology development in order to speed up VLSI/ULSI circuit design and simulation. Since SOI MOS devices offer better short-channel effect immunity in the VLSI/ULSI level compared to bulk MOS devices, analytical models and simulations are available on the former MOS technology. Among the SOI MOS devices, double gate SOI MOEFETs (DG-SOI MOSFETs) are free from bulk scaling limits and show superior short-channel effect immunity. However, the extensive applications of DG-SOI MOSFETs are limited by higher cost, process complexity and tunneling through thinner oxide in the deep-sub-micrometer regime. Therefore, alternative MOS structures should be developed in order to overcome the limitations of DG-SOI MOSFETs.

The main objective of this study was to develop a physics-based analytical model for short-channel effects in thin film fully depleted cylindrical gate MOSFET. Starting with the Poisson's equation in cylindrical co-ordinates and considering parabolic potential distribution in the channel, the models for charactertistic/natural length, threshold voltage, threshold voltage shift/lowering, sub-threshold swing, DIBL, etc. of cylindrical gate MOSFET were developed in this study. The results obtained from the above models were compared to those of the DG SOI MOSFETs.

A complete model on natural length has been developed analytically and its variations with parameters like silicon film thickness, t_{si}, and oxide thickness, t_{ox}, have been investigated. For the threshold voltage shift, ΔV_{th}, model, the effects of channel shortening, drain voltage, etc. were presented. The effects of drain voltage on (i) ΔV_{th} versus alpha, (ii) S-swing versus alpha, and (iii) DIBL versus alpha graphs were also investigated. It is found that the gate in cylindrical device has a greater control over the channel and also a cylindrical device has higher alpha ($\alpha = L/2\lambda$) ratio, thus enabling greater short channel effect immunity and improved sub-threshold characteristics. The tighter confinement from all directions allows the cylindrical gate MOSFET to be scaled to 29% shorter channel lengths compared to DG-SOI MOSFETs.

Finally, a temperature dependent analysis model for threshold voltage of a cylindrical gate MOSFET has been presented using a Gaussian doping distribution profile covering temperature range from 77K to 520K. The model also extended for a DG-SOI MOSFET. It is found that although the cylindrical device has higher packing density and reduced short channel effects than double gate device, its operation over larger temperature range is limited by the fact that gate loses control over the channel as the temperature increases. To overcome this problem, the threshold voltage of the cylindrical device can be raised by increasing the channel impurity concentration and/or by gate work function control.

4.2 Suggestions for Future Research

The present research is simple in functional form and it can easily be extended to study the substrate current and drain current behaviour of the device in the deep-sub-micrometer regime. For future research with cylindrical gate MOSFET, the following suggestions are made:

The substrate current that results from the accelerated carriers in the high electric field near the drain can become significant in very short-channel devices; this hot carrier effect then should be taken into account.

In the drain current behaviour model, the parasitic source-drain resistance effect must be incorporated since it becomes stronger in the short-channel devices, specially in the deep-sub-micrometer regime.

To overcome the problem with higher temperature operation, the channel impurity concentration and/or gate work function could be increased.

Cylindrical gate MOSFETs could be fabricated in order to verify the developed analytical models.

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