Development of an On-chip Current Mode Synchronous Step-up Converter without External Compensating Network and Slope Compensation.

বাংলাদেশ প্রকৌশল বিশ্ববিদ্যালয়
নং 104286
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লাইব্রেরী, ঢাকা

A thesis submitted to the Department of Electrical and Electronic Engineering (EEE)
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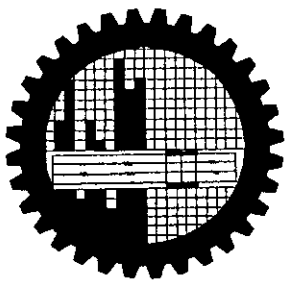
MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

by

Mohiuddin Md. Hafiz



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The thesis titled "**Development of an On-chip Current Mode Synchronous Step-up Converter without external Compensating Network and Slope Compensation**" submitted by Mohiuddin Mohammad Hafiz, Roll No.: 040406244P, Session: April 2004 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on May 26, 2007.

BOARD OF EXAMINERS

1. Dr. A.B.M Harun Ur-Rashid — Chairman (Supervisor)
   Professor
   Department of Electrical and Electronic Engineering
   BUET, Dhaka—1000,
   Bangladesh.

2. Head — Member (Ex-Officio)
   Department of Electrical and Electronic Engineering
   BUET, Dhaka—1000,
   Bangladesh.

3. Dr. Mohammad Ali Choudhury — Member
   Professor
   Department of Electrical and Electronic Engineering
   BUET, Dhaka—1000,
   Bangladesh.

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   Department of Electrical and Electronic Engineering
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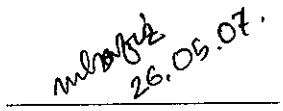

(Mohiuddin Md. Hafiz)

DEDICATION

To My Parents

Acknowledgement

I would like to express my profound and sincere gratitude to my supervisor Dr. A.B.M Harun Ur-Rashid, Professor Department of Electrical and Electronic Engineering (EEE), Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, whose patient guidance and encouraging attitude have motivated me much to have this thesis materialized.

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Finally I am grateful to the Almighty for giving me the strength and courage to complete this thesis.

Abstract

A monolithic current mode CMOS DC-DC converter with new control topology and integrated power switches has been developed in this thesis. A unified modulator model is also established for the topology, following the steps, used for deriving familiar models. System and circuit level implementation of the converter have been accomplished for the converter. Afterwards, this converter has been fabricated with a standard 0.5 μm CMOS process. The remarkable features of the converter are complete discharge of the output voltage, pulse-by-pulse current limiting, pulse-skipping mode in light load operation etc. Modulator gain F_m has been found to be a finite quantity and is independent of duty cycle, which reveals the fact that the control loop's stability is independent of compensating signal. In addition, no external components except the inductor and output capacitor and no extra I/O pins are needed for the current mode controller. The simulation and test data are in good agreement. The experiment results show that this converter operates around 1MHz with the supply voltage from 0.8V to 5V, which is suitable for single cell lithium-ion applications. The power efficiency is over 80% for load current from 50mA to 100mA, load regulation 1.6%, for the load variation 0-100mA.

Contents

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List of Symbols

Symbols	Description
m_1	Positive slope of the inductor current (up slope)
m_2	Negative slope of the inductor current (down slope)
M_c	Slope of the compensating ramp signal.
D	Average duty cycle
d	Small signal duty cycle (generally used as a variable quantity)
$\hat{d}$	Perturbed form of duty cycle
T_s	Time period
T_{ON}	Time for the charge phase of the converter.
T_{OFF}	Time for the boost phase of the converter.
V_{eff}	Average effective voltage across the switches when they remain OFF.
$\hat{v}_{eff}$	Perturbed form of effective voltage across the switches when they remain OFF.
F_m	Gain of the modulator of the converter.
K	Boltzmann constant
T	Absolute temperature.
q	Charge of an electron.
I_s	Saturation current.
A	Base-emitter junction area of a bipolar transistor.
g_m	Trans-conductance of a MOS.
μ_p	Mobility of holes
C_{ox}	Gate capacitance of a MOS.
V_A	Early Voltage.

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Chapter 1

Introduction

1.1 Background

Among the switching regulators, voltage mode DC-DC conversion was the initial approach, but it required a large number of external components for compensation and the design of the compensation network was too involved. This is due to the fact that the loop gain was sensitive to the load and input supply variation. The above fact made it difficult to use in situations where the supply and load vary widely, since the transfer function (line-to-output) is a strong function of input supply voltage. Because of the complexity of the double pole transfer function in the voltage mode conversion, it was soon felt necessary to simplify the transfer function so that it appears as a single pole. The obvious result was the current-mode control which requires a much simpler compensation scheme compared to its voltage-mode counterpart. The first monolithic current-mode DC-DC converter was introduced in 1985(LTC) and the first on-chip compensated switching regulator was introduced by NSC in 1988 *[1]*. Current-mode has two feedback loops: an outer one which senses DC output voltage and delivers a DC control voltage to an inner loop which senses power transistor currents and keeps them constant on a pulse-by-pulse basis. Among the several current-mode control techniques, constant-frequency current programmed mode (CPM) control, also known as peak current-mode (PCM) control, is a popular control technique for switch mode power converters. In this control scheme, peak power transistor currents are kept constant on a pulse-by-pulse basis. There are several advantages in this scheme; like built-in over-current protection, robust dynamic responses, simplified voltage-loop compensator design, rejection of input voltage disturbances and relatively simple current sharing for power modules operating in parallel. However, this scheme has also got some disadvantages. The main disadvantage is found during the continuous conduction mode (CCM). This is because of the limited duty cycle that requires compensation to extend the duty-ratio range beyond 50%. Another disadvantage of CPM control is relatively high sensitivity to noise related to sensing the instantaneous current and comparing the sensed signal

to the current command. To enable the converter, operating in CCM, run at higher duty cycle, theoretically above 50%, a compensating ramp is added to current sense signal. Moreover to reduce the sensitivity to noise, the compensation ramp is commonly added in practical CPM designs, even when operating the converter at duty cycles less than 0.5 *[2]*.

1.2 Compensation Issue:

As mentioned earlier, peak current control mode forces the peak power transistor current to be constant at a level needed to supply the DC load current at the DC output voltage dictated by the voltage error amplifier. The DC load current is the average of the output inductor current, however, and keeping the peak transistor current constant keeps the peak output inductor current constant but does not keep the average inductor current constant. Because of this, in the uncompensated current-mode scheme, changes in the DC input voltage will cause momentary changes in the DC output voltage. The output voltage will be corrected by the voltage error amplifier outer feedback loop. Again, however, the inner- loop, in keeping peak inductor current constant, does not supply the correct average inductor current and output voltage changes again. The effect is then an oscillation in the output voltage. Moreover, for a fixed DC input voltage, there can also be an oscillation. This occurs, when for some reasons an initial current disturbance gets induced in the current loop while the converter is running at duty cycle above 50%. In that case, the current disturbance will grow in pulse by pulse basis first, and then decreases in the next consecutive pulses and afterwards it will grow again. This sort of oscillation is also called as sub-harmonic oscillation, as this occurs at half the switching frequency when the converter runs above the maximum allowable duty cycle, without being compensated *[3]-[6]*.

Another industrially used topology is the Average Current-Mode Control Scheme. In this topology the inductor current is averaged by a current compensator, which is basically an integrator. Integrator adds additional pole to the current loop and this pole needs to be compensated. Hence, external components are needed in the board. This need for the extra components costs severely where space requirements in the board are stringent.

1.3 The Recent Research Trend:

Various works have been carried out relevant to the stability of current mode converters operating in CCM. Different topologies have also been introduced along with several analyzing techniques. Middlebrook contributed much to the modeling of PWM converters and analyzing their various features *[3]-[5]*. A low frequency circuit oriented approach was proposed in *[3]*, though this approach had simplicity and that is why it was widely accepted, it had some issues to be resolved and one of the major insights in *[3]* was that the crossover frequency of the current loop was considered wideband, implying possible degradation of performance of low frequency model. To cope with potential deficiencies in the earlier approaches, a separate earlier work *[7]* needed to be used, which could predict the well known sub-harmonic oscillation, occurring at duty cycle greater than 50% with no compensating ramp. A general expression for the current loop gain is derived, from which it is seen that the crossover frequency of the current loop is limited approximately to one third of the switching frequency. A few authors have contested this result on the ground that Shannon's sampling theorem limits the crossover frequency to half the switching frequency. This apparent contradiction has apparently been resolved in *[4]*.The most common topology, used in industry nowadays, is fixed frequency Peak Current Mode control. Brayant and Kazimierczuk presented the analysis of open-loop power stage dynamics *[8]* and the modeling of closed current loop configuration, relevant to current-mode control for a boost pulse width-modulated (PWM) dc–dc converter operating in continuous-conduction mode (CCM) is presented in *[9]*. In *[8]*, the small signal output current to inductor current transfer function accounting for MOSFET delay and input voltage to inductor current have been derived. In *[9]* the transfer function from the error voltage to duty cycle has been derived. Another earlier work *[10]* suggested that the modulator gain factor F_m can approach to infinity at the limit of stability. In *[4]*, Middlebrook along with Tan developed a unified model for current mode converters where they determined a unified modulator model and current loop gain incorporating sampling effect. Ridley, in *[11]* and *[12]* introduced a continuous time model, where sampling gain is incorporated into the current loop. Ridley et. al. proposed another topology other than PCM control in *[13]*, where in stead of peak current, average inductor current is used to control the loop dynamics. Another control technique, valley current mode technique, also known as 'leading edge

modulation' has been introduced in *[14]*, which has some advantages. One of the advantages it offers is the elimination of the positive zero in fixed frequency operation *[15]*.

1.4 Review of the Existing Compensation Techniques:

As mentioned above, sub-harmonic oscillation generally occurs for the duty cycle above 50%. This type of oscillation can be stopped by adding a compensation ramp by ensuring that a current perturbation in a switching period diminishes in the next period. For Average Current-Mode Control scheme, some sorts of external compensators are needed. In Average Current-Mode Control, inductor current is averaged by an RC network, which is basically an integrator. Though a huge gain is available in this scheme, the main challenge is to stabilize such loop, as the integrator adds an additional pole to the loop. Hence, to cancel the effect of this additional pole, a zero is needed in the loop, and the addition of this zero is accomplished by the use of external components.

1.5 Objectives of This Thesis:

The objectives of this thesis are to develop a new topology of synchronous step-up converter, which can run at higher duty cycle without addition of any kind of compensating signal and then to implement the converter paying heed to all the design issues that may have to be encountered in real world. In developing a new topology, the mathematical model for the modulator of the converter will be derived first, considering all the small signal phenomena. This converter will then be implemented using various functional blocks. While designing the functional blocks all the supply, process and temperature dependent parameters will be taken into account. The fabricated chip will then be tested and the test results will be studied in details to evaluate its performance.

Chapter 2

Current Mode Converters in Brief

2.1 Synchronous Converter in Brief:

In the synchronous converter, both the switches are controlled unlike the case in its asynchronous counterpart, where only one switch is controlled and in stead of using the other switch, generally a diode is used. However, there is no 100% synchronism in the synchronous converter, i.e. there is no such case where a switch is turned ON at the instant the other is turned OFF or vice versa because of the internal delay in the signal propagation. There are also some design requirements especially for safety purposes and in those cases, one switch is turned OFF first and then the other is turned ON. Fig 2.1 illustrates a synchronous boost converter with a modulator. The two switches SW1 and SW2 are turned ON alternately to have charge and boost phase of the converter. Before one is turned ON, it is ensured that other has been turned OFF. In an open loop boost converter, the input voltage is stepped up to another higher level based on the duty cycle of operation (the clock that is provided externally to the switches). However, to have a regulated output voltage a closed loop control mechanism is needed. The modulator serves that purpose. It senses the parameters like portion of output voltages or the current through the inductor or both and controls the loop operation by converting those signals to time domain signals (i.e. duty cycle). The overall stability of the loop depends; to a great extend, on the stability of the modulator.

2.2 Basic Idea about the Current Mode Converter:

The block diagram shown in Fig 2.2 was the approach used for the first switching regulator designs *[16]*. This is also known as Voltage Mode Control Topology. The major characteristics of this topology are that there is a single voltage feedback path, with pulse-width modulation performed by comparing the voltage error signal with a constant ramp. Current limiting must be done separately. As a single loop is associated, tasks like designing of that loop and analyzing the loop dynamics are simpler. But there are also some disadvantages of such topology like

slow response (as any change in line or load must first be sensed as an output change and then corrected by the feedback loop.) and relatively more complicated compensation (as the output filters adds two poles to the control loop and the loop gain varies with the input voltage).

To get rid of the voltage mode deficiencies, another control technique called Current Mode Topology has been introduced and it is illustrated in Fig 2.3. As it is evident from Fig 2.3 that, basic current-mode control uses the oscillator only as a fixed-frequency clock and the ramp is replaced with a signal derived from output inductor current. It has got some advantages like fast response with the change in the line voltages (as inductor current rises with a slope determined by V_{in}-V_o), simpler loop compensation (Since the Error Amplifier is now used to command an output current rather than voltage, the effect of the output inductor is minimized and the filter now offers only a single pole to the feedback loop.) Moreover, the current mode topology also provides some additional features like: pulse-by-pulse current limiting, and the ease of providing load sharing when multiple power units are paralleled.

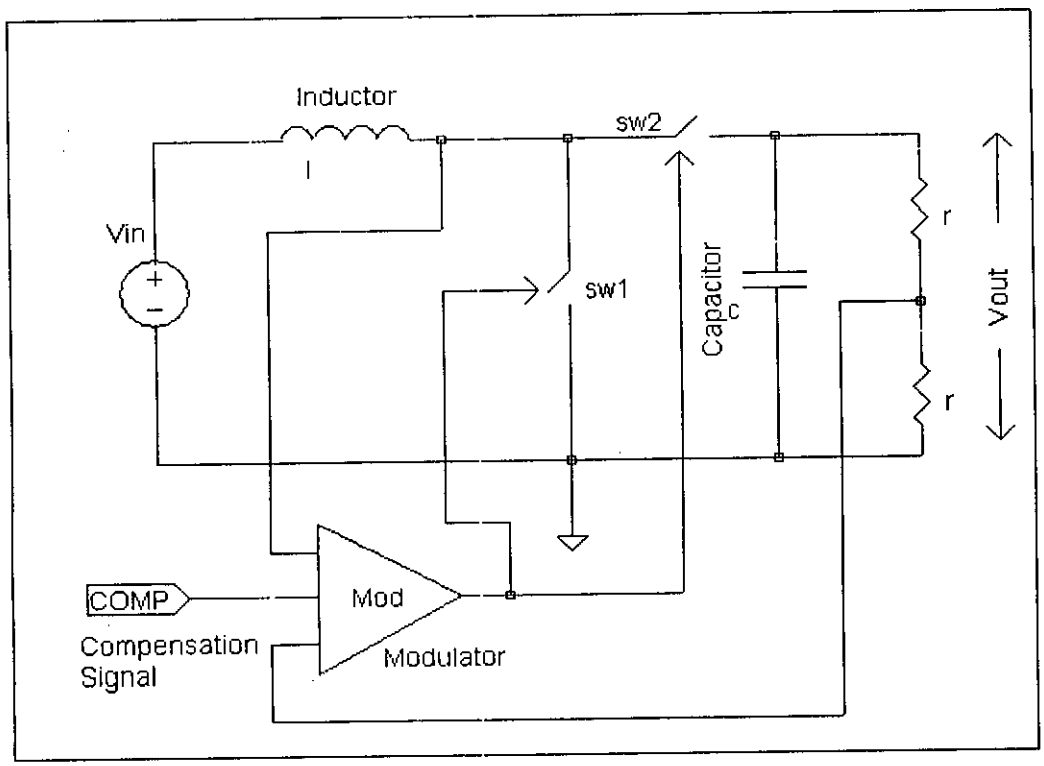

Fig 2.1: *Synchronous boost regulator with modulator*

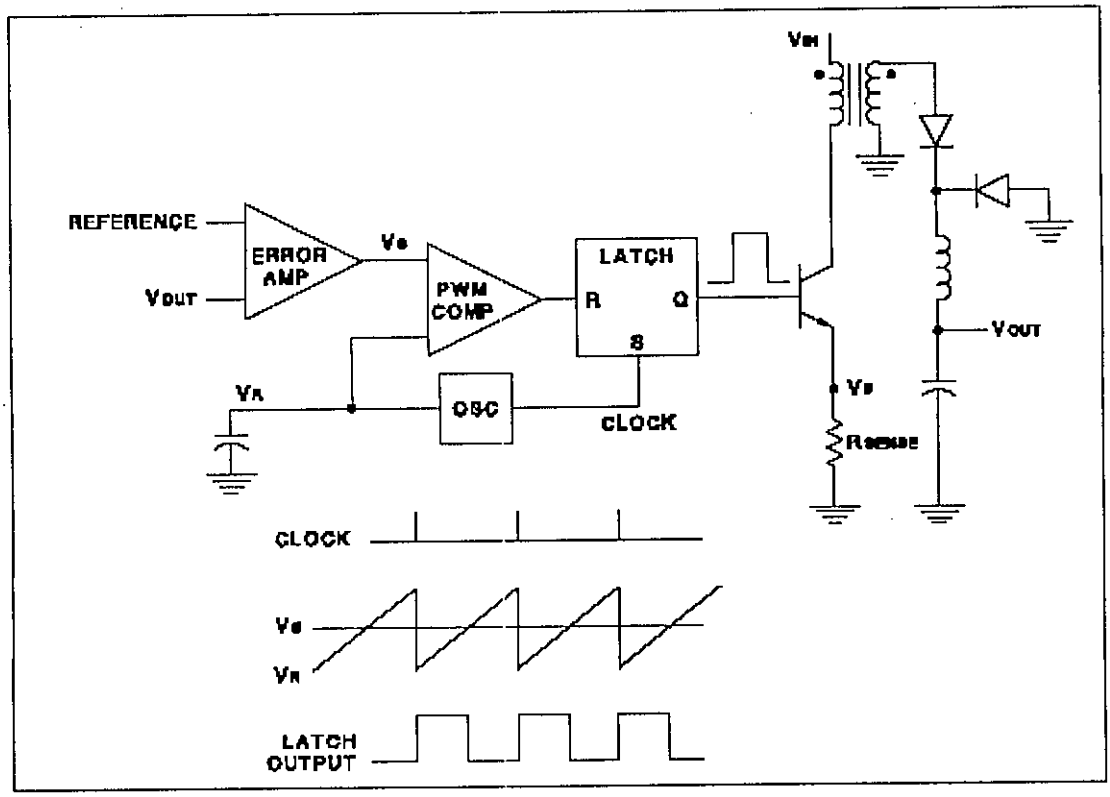

Fig 2.2: *Voltage mode control mechanism [16]*

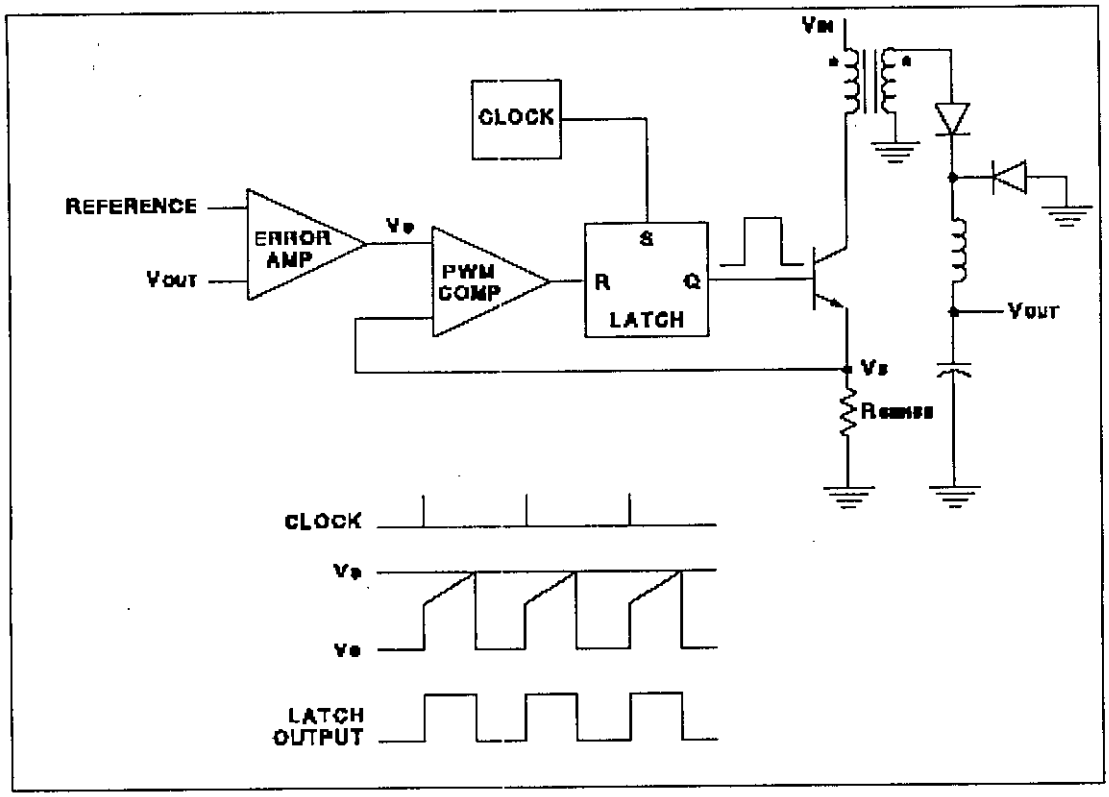

Fig 2.3: *Current mode control [16]*

2.3 Deficiencies in Current Mode Control Mechanism & Their Remedies:

In spite of several advantages, there are also some sorts of deficiencies associated with the current mode control mechanism. A brief idea has been given in previous discussions. In this subsection, those problems have been illustrated more precisely. First, let us have a look at the case of sub-harmonic oscillation. One of the ways such kind of oscillation occurs, when a current disturbance gets induced in a converter running at high duty cycle, for a fixed input. For a fixed DC input voltage,

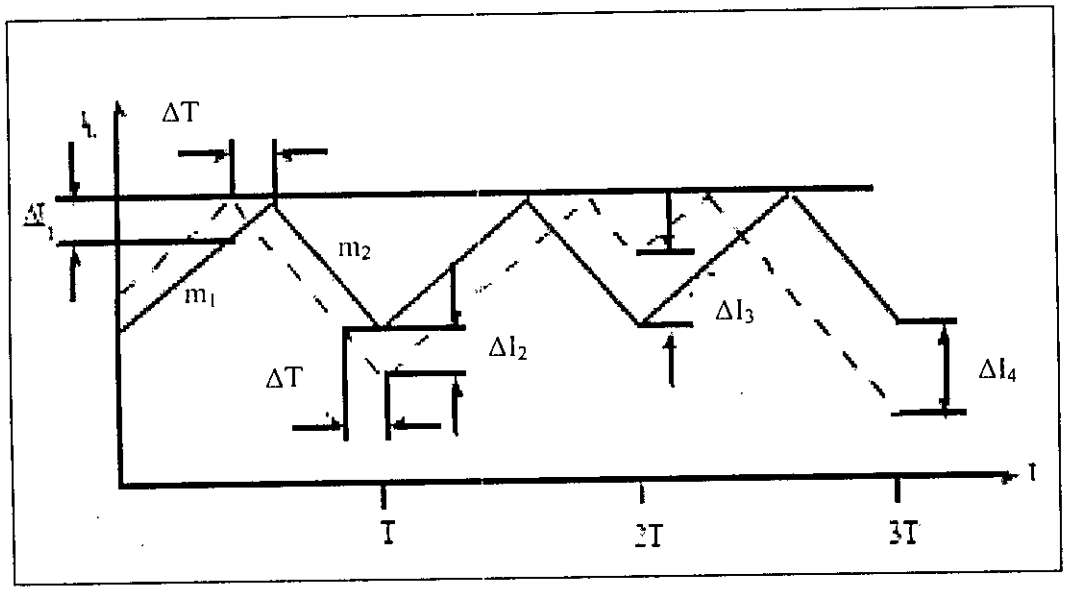

Fig 2.4: *Current loop oscillation for duty cycle greater than 50% [25]*

if for some reasons there is an initial current disturbance ΔI_1, after a first down-slope the current will be displaced by an amount ΔI_2 .If the duty cycle is above 50% ($m_2 > m_1$ in Fig 2.4), the output disturbance after one cycle ΔI_4 is greater than the input disturbance ΔI_3. This can be further explained from Fig 2.4. For a small current displacement ΔI_1, the current reaches the original peak value earlier in time by an amount *dt*, where $dt = \Delta I_1/m_1$. ON the inductor down-slope, at the end of the ON time, the current is lower than its original value by an amount ΔI_2 where

$$\Delta I_2 = m_2 dt = \Delta I_1 \frac{m_2}{m_1}$$

Now with $m_2 > m_1$, the disturbances will continue to grow but eventually decay, giving rise to an oscillation. As mentioned earlier, this sort of

oscillation is also called as sub-harmonic oscillation, when the converter runs above the maximum allowable duty cycle, without being compensated *[3],[5],[6]*. This PCM (Peak Current Mode, as the peak current is regulated) control, however, is a widely used topology in industrial purposes and the above mentioned type of oscillation is eliminated by the addition of a compensating signal with slope $M_c > 0$. The way in which such compensating technique works, has been illustrated in Fig 2.5.

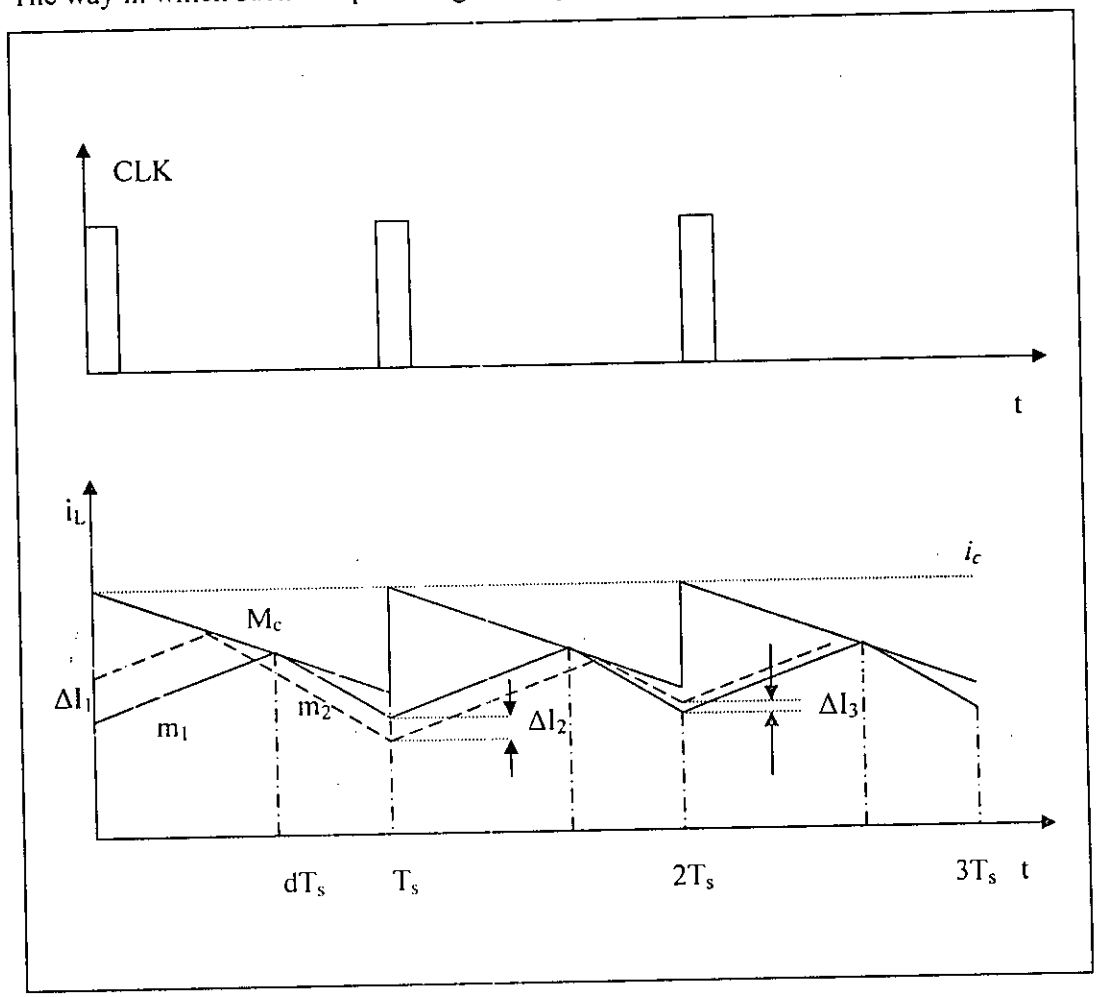

Fig 2.5: *Correction of the oscillation by compensation ramp [25]*

From a simple geometrical argument, the condition to prevent sub-harmonic oscillation is:

$$\left|\frac{\Delta I_2}{\Delta I_1}\right| = \left|\frac{m_2 - M_c}{m_1 + M_c}\right| < 1 \qquad (2.1)$$

where, $m_1 = V_{in}/L > 0$ is the inductor current slope in the charge phase

(dT_s),when sw1 in Fig 2.1 is ON, and $m_2=(V_{out}-V_{in})/L>0$ is the inductor current slope in the boost phase [$(1-d)T_s$] when sw2 in Fig 2.1 is ON. From the equation 2.1, it is evident that, by selecting $M_c>m_2/2$, stable operation of the current loop under all steady-state conditions is possible to be achieved. Besides, in *[3],[17],[18]* modulator model for the current programmed converters was derived, experimented and modified. A model for current-mode converter consists of two parts: 1) the model for the power stage, and 2) the model for the modulator *[3]*. The model of power stage in *[19], [20]* is now widely accepted, hence the actual task is reduced to the establishment of a modulator model. A modulator is expected to be expressed in terms of the average inductor current i_l, the average control current i_c and an effective voltage v_{eff}, which determines the slopes of the inductor current. Satisfying the conditions, a unified modulator model has been developed in *[3]* and the modulator gain F_m is expressed as:

$$F_m = \frac{2L}{T_s v_{eff}\left[\left(\frac{2LM_c}{D'v_{eff}}+2\right)D'-1\right]} \qquad (2.2)$$

From the equation (2.2), it is seen that, F_m approaches infinity for

$$D' = \frac{1}{\left[\frac{2LM_c}{D'v_{eff}}+2\right]} \qquad (2.3)$$

where, $D' = 1-D$

Equation (2.3) is the minimum value for D' to maintain a finite positive value for F_m. Hence, we have:

$$D'_{min} = \frac{0.5}{\left[1+\frac{M_c}{D'v_{eff}/L}\right]}$$

$$\Rightarrow D'_{min} = \frac{0.5}{\left[1+\frac{M_c}{m_1}\right]} \qquad (2.4)$$

Hence, from equation (2.4), the current loop becomes unstable for $D'_{min}=0.5$, if $M_c=0$, which implies that in the absence of M_c, the loop oscillates for

D_{max}=0.5. Addition of slope compensating signal demands extra care and attention. The addition of the slope compensating signal, does not depend on any kind of internal tracking within the chip, it is one sort of asynchronous phenomenon. This compensating signal shows up as a percentage error in the output voltage i.e. it increases the load regulation number of the chip. Moreover, generally this signal is added relative to the ground potential and in doing there also arise some design issues. If this signal is small in magnitude and is fed to the input of a MOS device, the offset of the MOS affects and if this signal is added to the base of a bipolar device, extra input linearity is needed. This is sometimes a design constraint, in case of low voltage application.

In average current control scheme, the existence of the current compensator makes the modeling of the average current-mode control more complicated *[13]*. The modulator of the average current control scheme has been shown in Fig 2.6.

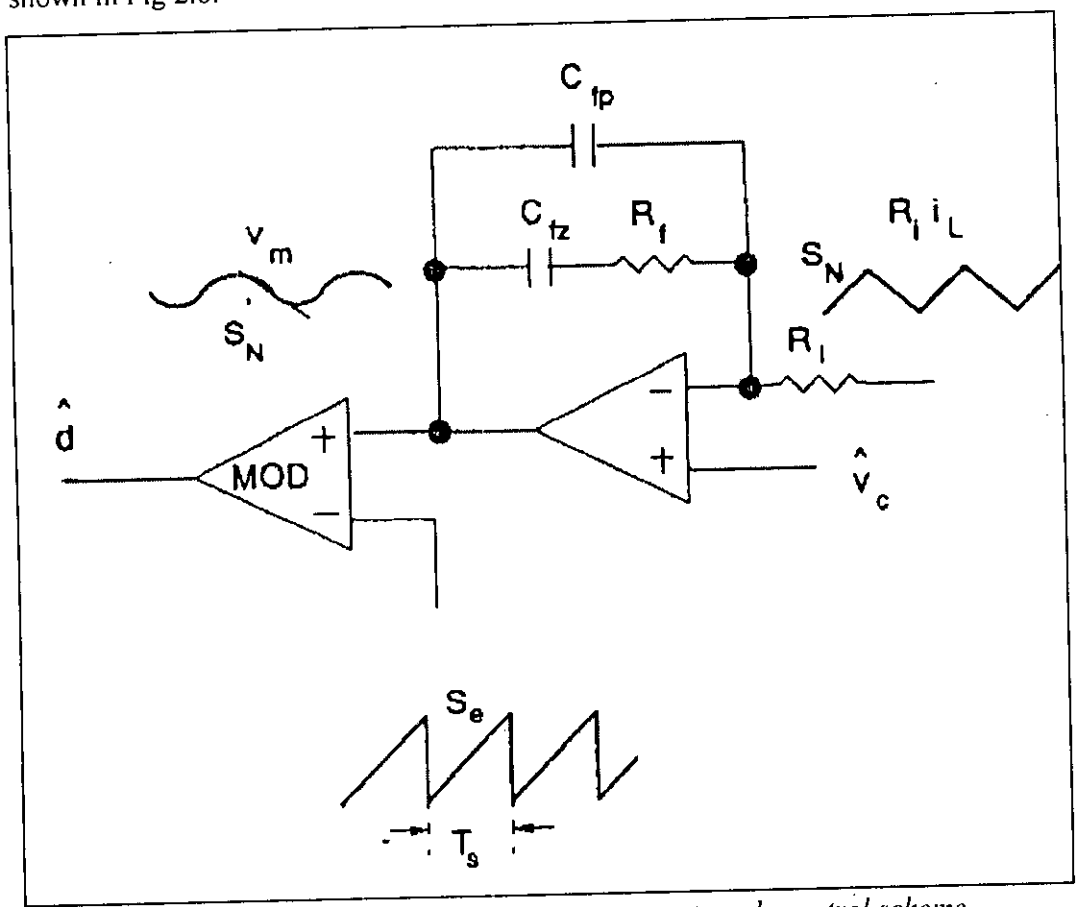

Fig 2.6: *The modulator of the average current-mode control scheme [13]*

As it is evident from Fig 2.6, an integrator (compensator), consisting of R-C network has been used to have the average of the inductor current. This integrator adds a pole at $\frac{1}{2\pi C_f R_f}$ in the current loop, the effect of which has to be cancelled by an external compensator.

2.4 Control Topologies & Conduction Modes:

In dc-dc converters current mode Pulse Width Modulation (PWM) and current-limited Pulse Frequency Modulation (PFM) control schemes are widely used in industries due to their fast dynamic response and automatic over-current protection *[21]-[23]*. In PWM control, the inductor current is sensed and is made to modify the pulse-width, whereas, in PFM control inductor current modifies the oscillation frequency for voltage regulation. One of the methods to regulate output voltage, while supplying a specific load demand, in PWM control employs switching at a constant frequency and adjusting the ON duration of the switch. In PFM, however, the switching frequency is varied with the change in load demand while regulating the output voltage. For a certain load, this PFM scheme may turn into a PWM scheme. Usually a converter, though it is not designed to operate in fixed frequency, runs in PWM scheme for a certain load range and then operating frequency becomes constant for that condition. However, when the output load demand becomes very low, numbers of pulses are skipped and hence it seems like it is modulating its operating frequency.

A current mode converter has two types of conduction modes *[24]*; namely

a). Continuous Conduction Mode (CCM) and

b). Discontinuous Conduction Mode (DCM).

a).Continuous Conduction Mode:

In the continuous conduction mode, current flows continuously in the inductor during the entire switching cycle in steady-state operation. In this mode, the boost power stage assumes two states per switching cycle. In the ON state, SW_1 (Fig 2.1) is ON and SW_2 is OFF. The duration of the ON state is $D \times T_S = T_{ON}$, where D is the duty cycle set by the control circuit, expressed as a ratio of the switch ON time to

the time of one complete switching cycle, T_S. The duration of the OFF state is T_{OFF}. Since there are only two states per switching cycle for continuous conduction mode, T_{OFF} is equal to $(1-D) \times T_S$. The timing waveforms have been illustrated in Fig 2.7. In the CCM, average inductor current tracks the output current, i.e., if the output current decreases, then so does the average inductor current exactly.

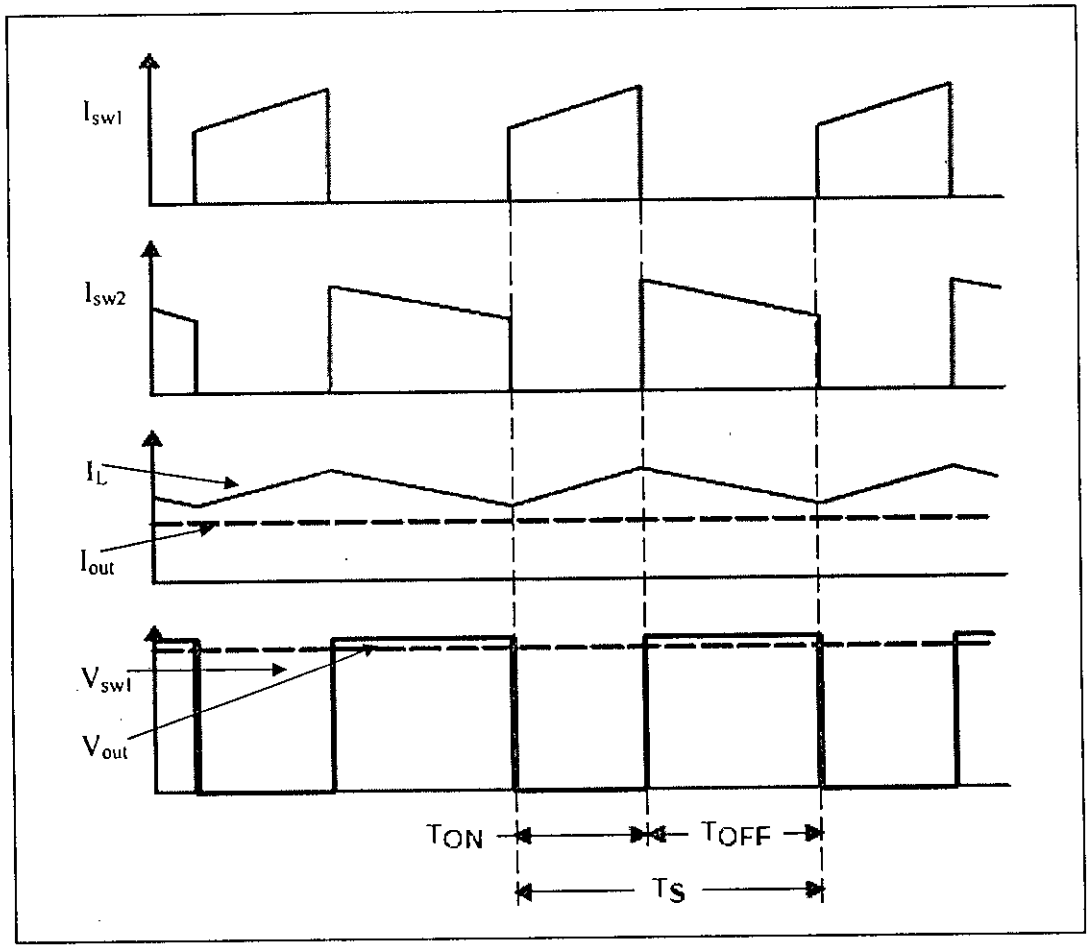

Fig 2.7: *Continuous conduction mode operation* [24]

b). Discontinuous Conduction Mode:

In the Discontinuous Conduction Mode, the output load current is reduced below the critical current level so that, the inductor current will be zero for a portion of the switching cycle. The facts are evident in Fig 2.8 and Fig 2.9. There are three unique states that a converter assumes during the DCM. The ON state is when SW_1 is ON and SW_2 is OFF. The OFF state is when SW_1 is OFF and SW_2 is ON. The idle state is when both SW_1 and SW_2 are OFF. Now, $T_{ON} = D \times T_S$, $T_{OFF} = D_2 \times T_S$;

and the remainder idle time is given as $T_S - T_{ON} - T_{OFF} = D_3 \times T_S$, where D_2 and D_3 are the portions of the total time T_S, when charge of the inductor is being dumped to the capacitor and the current through the inductor remains at the zero level, respectively.

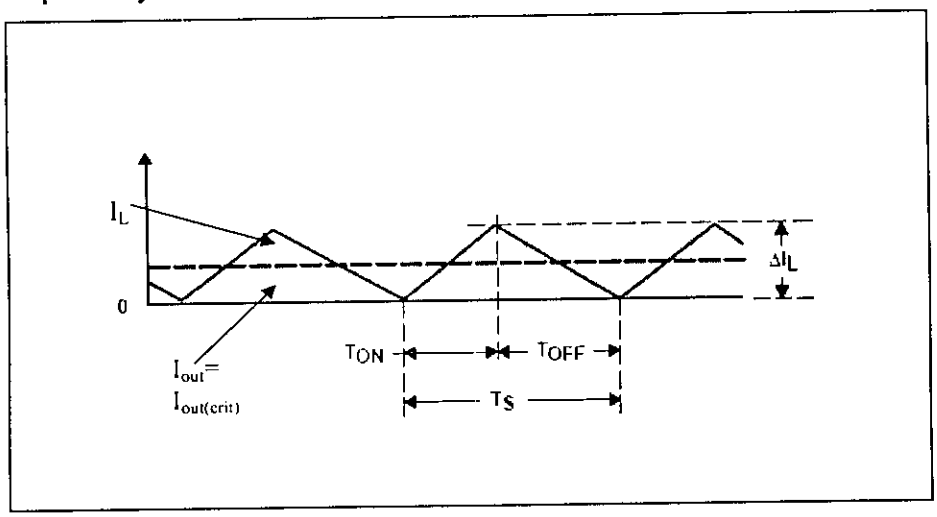

Fig 2.8: *The boundary between CCM and DCM* [24]

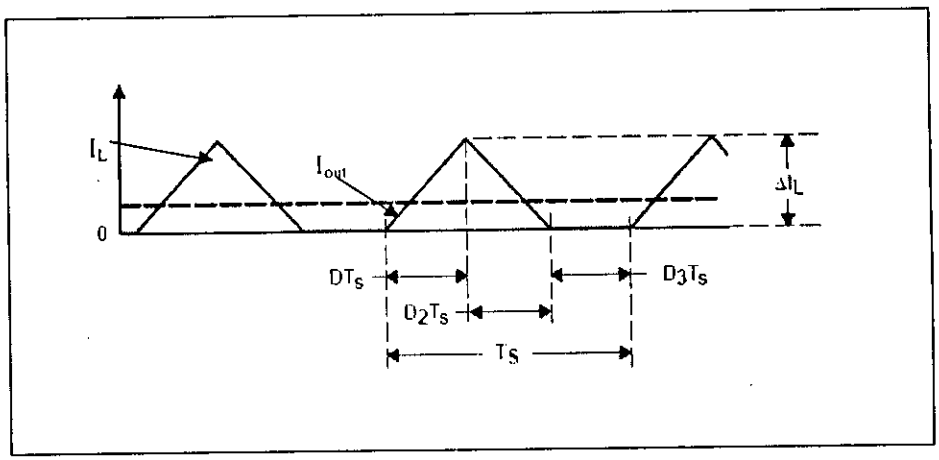

Fig 2.9: *Discontinuous conduction mode* [24]

2.5 PWM Switch Model in CCM:

The PWM switch model representing the dc and small-signal characteristics of the nonlinear part of the converter, has been illustrated in *[20]*. External circuit elements are connected to the switch in such a way as to satisfy the proper port conditions given in Fig 2.10, i.e. it is ensured that in any condition ports *a* and p do not get shorted and in one cycle *a* is connected to *c* and in the other cycle *p* is connected to *c* to have continuous current conducting condition in *a-c* and *c-p* paths

respectively. The dc and small-signal characteristics of a PWM converter are then obtained by replacing the PWM switch with its equivalent circuit model as shown in Fig 2.11.

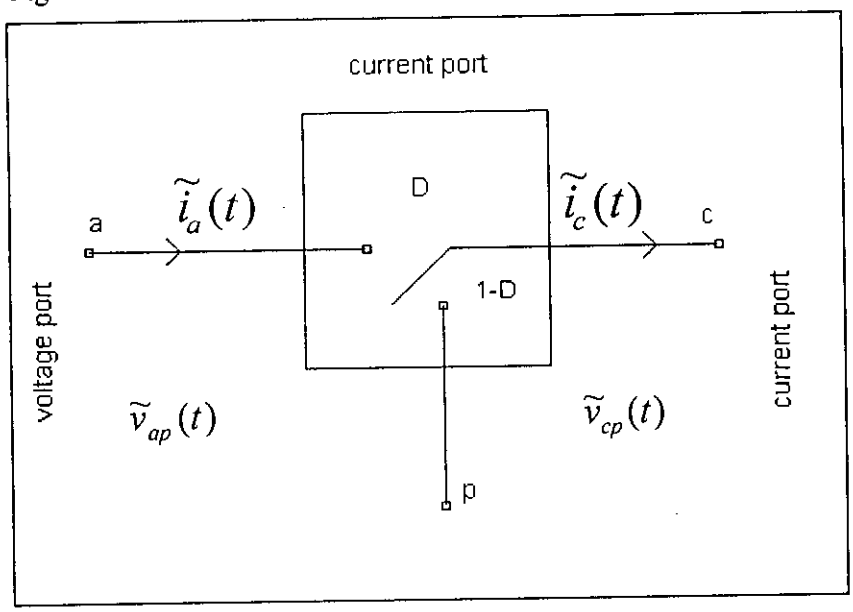

Fig 2.10: *The PWM switch*

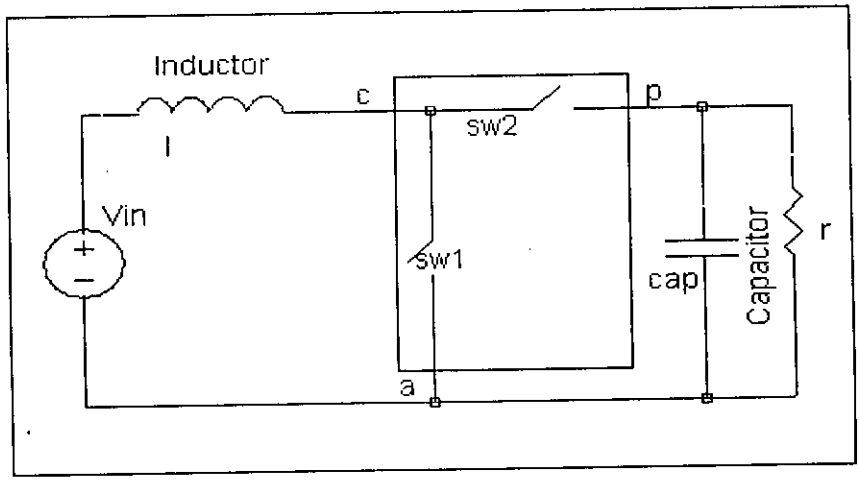

Fig 2.11: *Boost converter with PWM switch model.*

Now investigating the invariant relationships between the terminal currents and voltages of the PWM switch we have the following for the instantaneous quantities:

$$\tilde{i}_a(t) = \begin{cases} \tilde{i}_c(t), & 0 \le t \le DT_s \\ 0, & DT_s \le t \le T_s \end{cases} \tag{2.5}$$

$$\tilde{v}_{cp}(t) = \begin{cases} \tilde{v}_{ap}(t), & 0 \le t \le DT_s \\ 0, & DT_s \le t \le T_s \end{cases} \tag{2.6}$$

However, in dc-dc converters the average quantities are of greater importance and hence, for the average terminal quantities from the equations (2.5) and (2.6) are found as:

$$i_a = di_c \tag{2.7}$$

$$v_{cp} = dv_{ap} \tag{2.8}$$

Now, perturbing the equations (2.3) and (2.4) with respect to the variable quantities we have:

$$\hat{i}_a = D\hat{i}_c + I_c\hat{d} \tag{2.9}$$

$$\hat{v}_{cp} = D\hat{v}_{ap} + \hat{d}V_{ap}$$

$$\Rightarrow \hat{v}_{cp} = D(\hat{v}_{ap} + \frac{\hat{d}V_{ap}}{D}) \tag{2.10}$$

The equations (2.9) and (2.10) correspond to the dc and small-signal model of the PWM switch. The perturbed terminal quantities in the equations (2.9) and (2.10) can be arranged to satisfy the circuit configuration, illustrated in Fig 2.12.

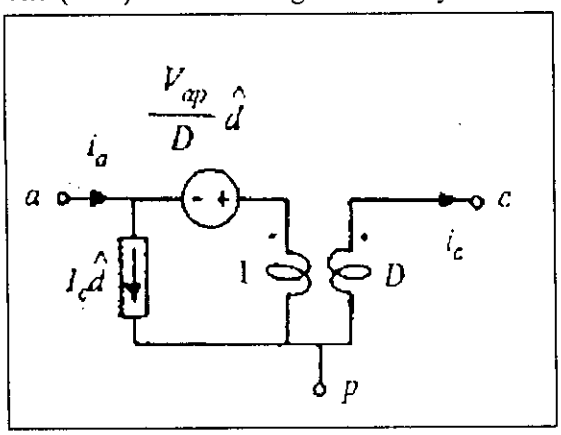

Fig 2.12: *DC and small signal model of PWM switch [20].*

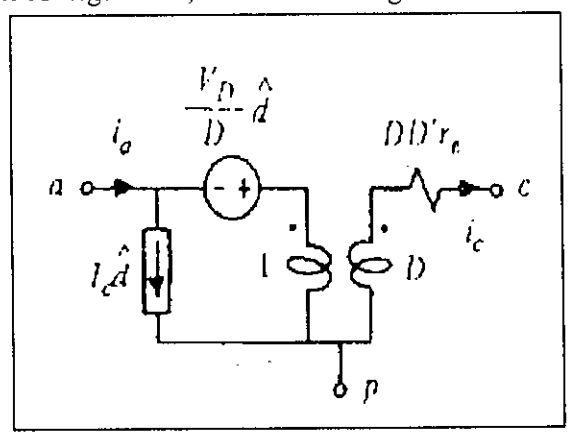

Fig 2.13: *DC and small signal model of PWM switch with ESR of the output capacitor [20].*

In deriving the equation (2.10), the Equivalent Series Resistance (ESR) of the output capacitor has been neglected; if it is intended to be included, equation (2.10) will be modified as:

$$\hat{v}_{ap} = \frac{\hat{v}_{cp}}{D} + \hat{i}_c r_e D' - V_D]\frac{\hat{d}}{D}$$

$$where, V_D = V_{ap} + I_c(D - D')r_e \tag{2.11}$$

The dc and small signal model of the PWM switch will then be represented as in Fig 2.13.

Chapter 3

The Proposed Converter

3.1 The Architecture of the Proposed Converter:

The functional block diagram in Fig 3.1 depicts the basic structure of the converter. The start-up oscillator starts the chip and raises the output voltage from zero to a certain level, where the actual PWM operation is initiated. The PWM operation of the chip is accomplished by two loops: one (current loop) functioning within the other (voltage loop). The current-sense amplifier, which senses the voltage across the PMOS switch, extracts the sensed current signal for the current loop, while the other amplifier taking REF and FB as inputs supplies the sensed voltage signal for the voltage loop. The current loop is embedded in the voltage loop, ensuring that sufficient response speed difference exists between the two loops. However, the loop is completed through a control block namely "Time Control Logic" where a time generator circuit provides a fixed ON time for a certain input voltage and a minimum OFF time. The bias select circuit selects the supply for all the circuitry of the converter either from the input or from the output voltage. The accessories for the proper, safe and efficient operation are thermal sensor, which protects the chip from thermal damage due to excessive rise of temperature within it; over-current limiter that checks the inrush of current from the source, feeding the converter; under voltage lockout block that prevents the logic blocks of the chip from malfunctioning because of low voltage; zero-crossing comparator that hinders the current through the inductor to reverse its polarity and thus back charging of the source from the load side ,when the output load is low, resulting in efficient operation during the light load condition; discharge switch which works to dampen the ringing of the inductor current and the body manage switch that manages the substrate diode of the PMOS switch by selecting the proper substrate bias from input and output voltages depending on the operation conditions. These accessories, however, perform their assigned tasks through a control block called "Gate Control Logic".

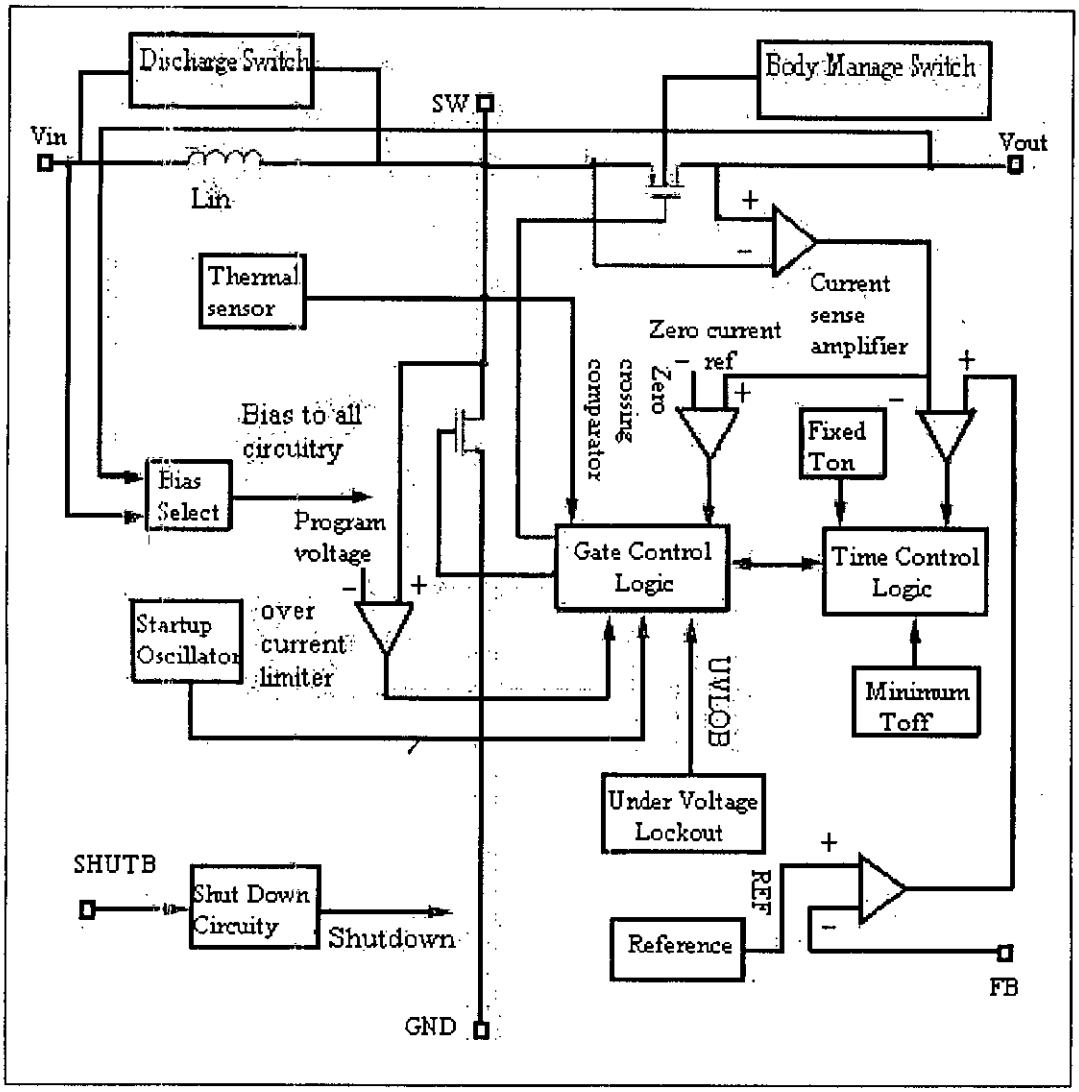

Fig 3.1: *The functional block diagram of the converter*

3.2 The Basic Operational Principle:

The proposed converter employs OFF time (Boost phase) modulation technique. The timing diagram in Fig 3.2 explains the operation principle of the loop. The ON time (Charge phase) is kept constant for a fixed input voltage V_{in} , in such a way that this ON time is inversely proportional to V_{in}. Each charge phase is initiated by an error amplifier which senses the valley current through the inductor as the current sense signal and takes the Band-gap reference and feedback voltage as its input signals.

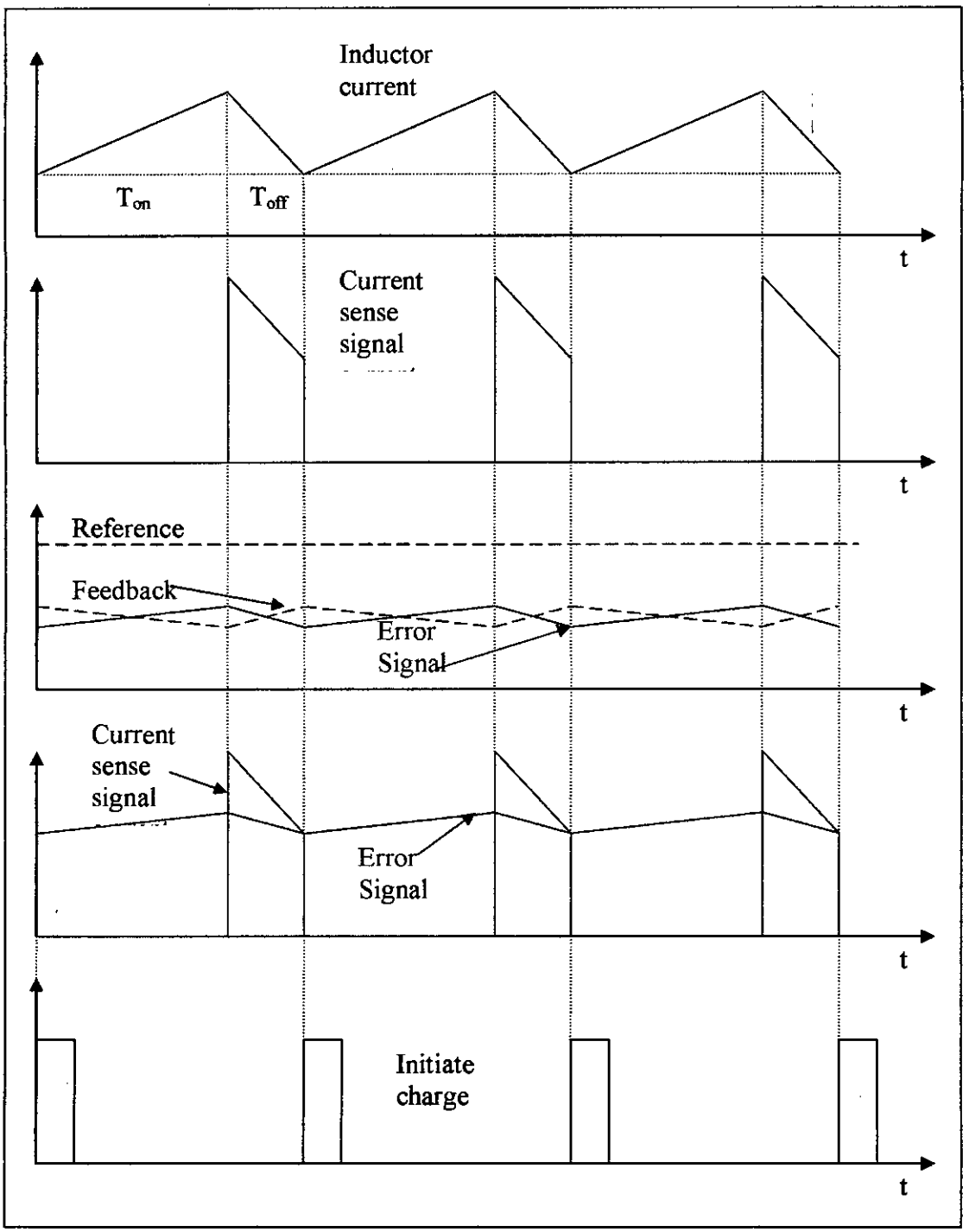

Fig 3.2: *The operational principle of the converter*

The charge phase, however, will be terminated by a time generator circuit, which generates the required ON time for a fixed input voltage. Referring to Fig 3.2, it is found that the current –sense signal is proportional to the inductor current of the time T_{off} (i.e. during the boost phase). Besides, the difference between the reference and feedback voltages constitutes the 'error signal'. The 'current sense

signal' and the 'error signal' are compared at their down slopes to yield the logic signal to initiate a charge phase. As the decision of the loop is being taken at the valley of the inductor current, this methodology is also known as 'valley current sense mode'. Here the current loop regulates the valley of the inductor current. The minimum T_{off} has been provided to have forceful boosting up of the output capacitor, when the loop is broken (e.g. during start-up condition, when a load step is applied etc.).

3.3 The Topological Impact on the Current Loop Oscillation:

This topology provides some inherent features, so that any sort of the current disturbances may die out within a cycle and does not grow any further. As a result, unlike the case that is in subsection 2.3 of chapter 2 the current disturbances will not aggravate. Fig 3.3 illustrates the fact.

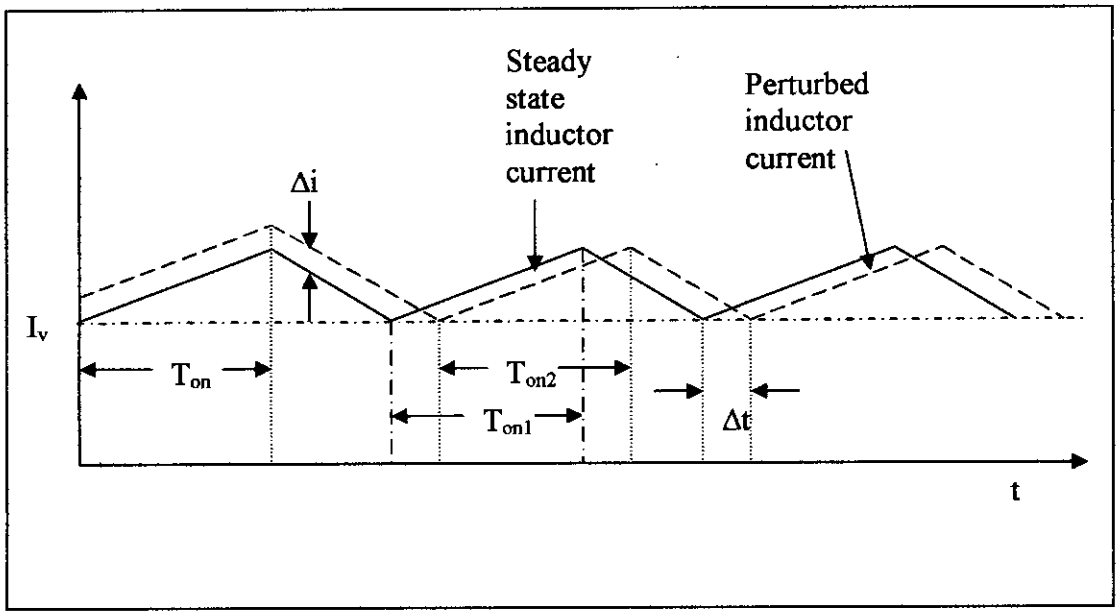

Fig 3.3: *Topological effect on current disturbances in the proposed topology of the converter.*

For some reasons, with a fixed input voltage i.e. V_{in}, a current disturbance Δi occurred (shown by dotted lines in Fig 3.3). As this is a valley current mode topology, the current loop will keep the valley of the inductor current constant (I_v in Fig 3.3). As a result, the next cycle will be initiated only if the perturbed inductor current reaches the valley at its down-slope. Moreover, ON time is constant for a fixed DC input voltage ($T_{on}=T_{on1}=T_{on2}$) for this topology and hence the charge phase of the next cycle will terminateat that fixed ON time. As a result, the perturbed

inductor current will just be a replica of the steady state inductor current with a Δt shift in time, in the next cycle. Thus the current disturbance that is got induced in the current loop is automatically eliminated by the topological features of the converter.

Following the approaches in *[25]*, let us examine the current loop of the converter in an alternative way to see the issues of current-loop oscillation and the way to compensate the loop to avoid the oscillation.

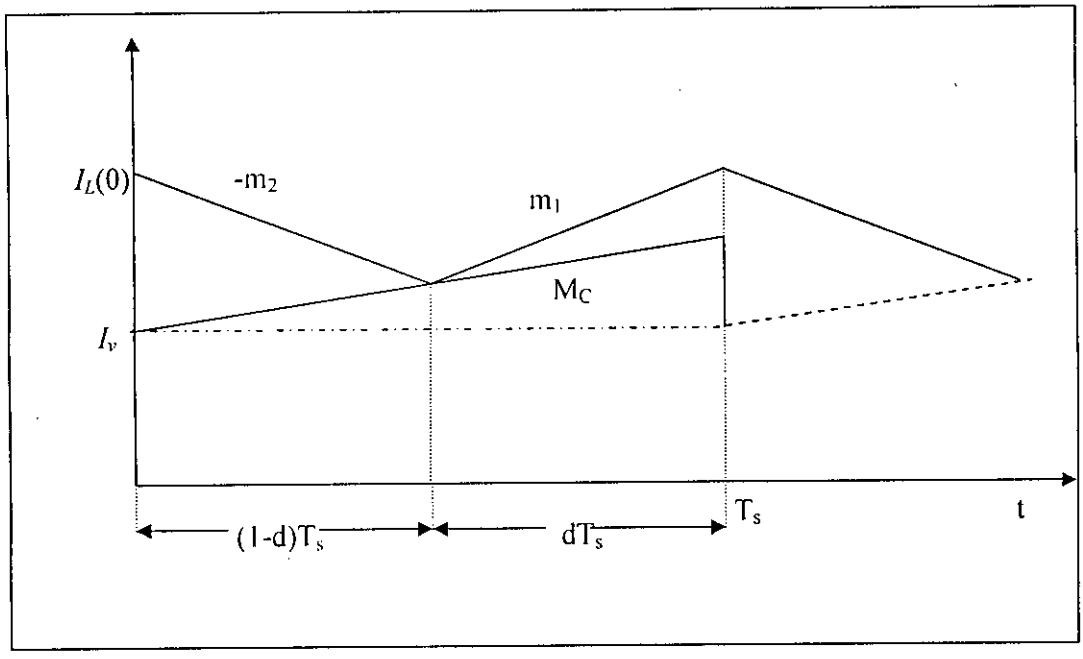

Fig 3.4: *The current loop with compensation in the proposed topology of the converter*

As mentioned earlier, this converter topology employs the valley-current mode technique, when the sensed current reaches the programmed current (illustrated by the dotted line), the boost phase terminates and the charge phase is initiated. Let's introduce a compensation ramp and as a result, the programmed current I_v will be perturbed with a slope of M_C. Now from the geometry, we have

$$\begin{aligned} & I_L(0) - m_2(1-d)T_s = I_v(T_s) + M_c(1-d)T_s \\ \Rightarrow\ & I_L(0) - m_2 T_s + m_2 dT_s = I_v(T_s) + M_c T_s - M_c dT_s \\ \Rightarrow\ & I_L(0) - m_2 T_s + m_2 T_{on} = I_v(T_s) + M_c T_s - M_c T_{on} \end{aligned} \qquad (3.1)$$

and,

$$\begin{aligned} & I_v(T_s) + m_1 dT_s - M_c dT_s = I_L(T_s) \\ \Rightarrow\ & I_v(T_s) + m_1 T_{on} - M_c T_{on} = I_L(T_s) \end{aligned} \qquad (3.2)$$

For this topology, T_{on} is fixed for a particular input voltage V_{in}. Taking this into consideration and perturbing the equations eq1 & eq2 we have

$$\hat{i}_L(0) = \hat{i}_v(T_s) \tag{3.3}$$

$$\hat{i}_v(T_s) = \hat{i}_L(T_s) \tag{3.4}$$

From the equations (3.3) and (3.4), we have $\hat{i}_L(0) = \hat{i}_L(T_s)$; hence $\Delta\hat{i}_L = 0$, i.e. any disturbance in the inductor current dies out within a cycle, it is does not aggravate in cycle by cycle basis. Moreover, if the compensating ramp is not used, we have $\hat{i}_v(T_s) = 0$ and again $\hat{i}_L(0) = \hat{i}_L(T_s)$ holds, which ensures that even if no compensation scheme is introduced, the current disturbances of the converter are eliminated by the current loop.

3.4 The Modulator Model:

As mentioned in *subsection 2.3* in the chapter 2, the actual task in modeling a converter has been reduced to the development of the model of the modulator. Following the steps in *[4]*, a unified modulator model has been derived here. Fig 3.5 shows inductor current waveforms in steady state, where m_1 is the upslope, $-m_2$ is the down-slope and M_c is the slope of the compensating ramp. The geometries of the waveforms provide fundamental information for derivation of a modulator model.

Finding the values of i_1 and i_2 at the respective middle points of the triangles we have:

$$i_1 = I_v + M_c dT_s + \frac{1}{2} m_1 dT_s \tag{3.5}$$

$$i_2 = I_v + M_c dT_s + \frac{1}{2} m_2 d'T_s \tag{3.6}$$

where, $d' = (1 - d)$ (3.7)

For a switch-mode converter, the effective voltage $\hat{v}_{eff}$ across the switches is found in terms of input terminal voltage $\hat{v}_i$ and the output terminal voltage $\hat{v}_o$, by the following expression [4]:

$$\hat{v}_{eff} = \alpha \hat{v}_i + \beta \hat{v}_o \tag{3.8}$$

Where, $\alpha, \beta \in \{0,1\}$.

For a boost converter, $\alpha = 0$ and $\beta = 1$ and hence from (3.8) we have,

$$\hat{v}_{eff} = \hat{v}_o \tag{3.9}$$

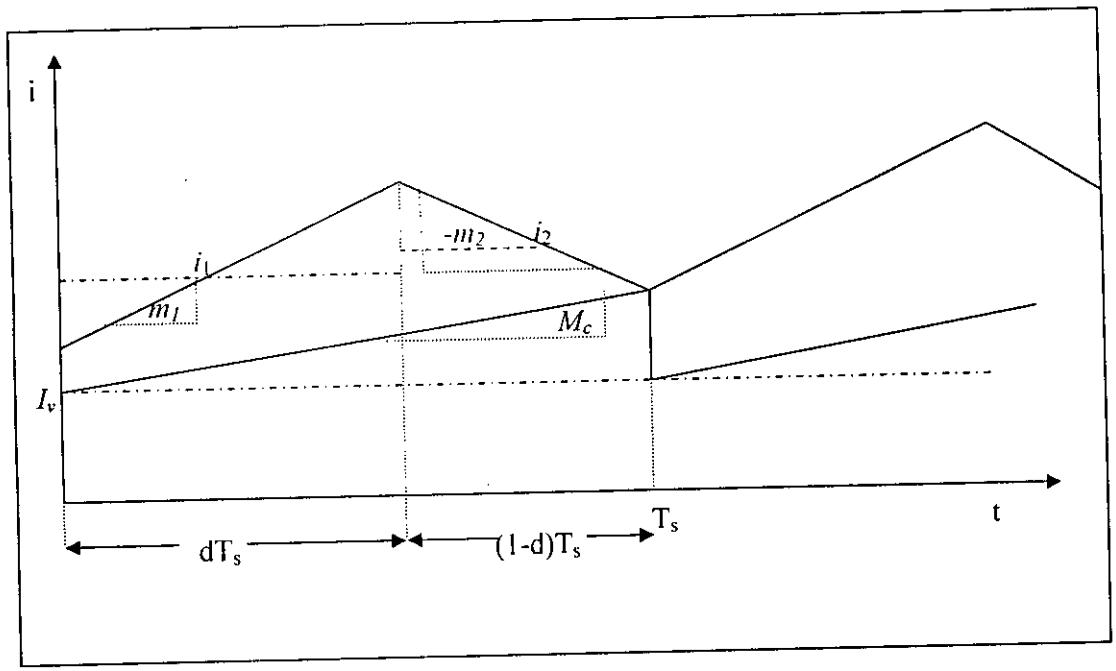

Fig 3.5: *Geometries of the inductor currents in steady states for obtaining the modulator model of the proposed converter.*

Again, the slope of the inductor current through an inductor of inductance L, during the charge cycle,

$$m_1 = \frac{v_i}{L} \tag{3.10}$$

And the input-output relationship of a boost converter operating in Continuous Conduction Mode at the duty cycle d,

$$v_o = \frac{v_i}{1-d} \tag{3.11}$$

From the equations (3.7), (3.9), (3.10) and (3.11) we have the following relationship:

$$m_1 = \frac{v_{eff} d'}{L} \tag{3.12}$$

Therefore, from (3.5) and (3.12) we have:

$$\begin{aligned} i_1 &= I_v + M_c dT_s + \frac{1}{2L}(dd'T_s)v_{eff} \\ &= I_v + KM_c + \frac{1}{2L}(Kd')v_{eff} \end{aligned} \tag{3.13}$$

Where K is a constant, as $dT_s = T_{on}$, which is a constant number for a fixed input voltage, in this topology.

Equation (3.13) is a unified large-signal expression which describes how a duty cycle d is determined. Small-signal information can be derived by its perturbation. Now differentiating the equation (3.13) partially, with respect to the variables, we have the following relationship:

$$\hat{i}_l = \hat{i}_v + KM_c + \frac{K}{2L}[D'\hat{v}_{eff} - \hat{d}V_{eff}]$$

$$\Rightarrow \frac{K}{2L}V_{eff}\hat{d} = (\hat{i}_v - \hat{i}_l) + \frac{K}{2L}D'\hat{v}_{eff} + KM_c$$

$$\therefore \hat{d} = \frac{1}{\frac{K}{2L}V_{eff}}[(\hat{i}_v - \hat{i}_l) + \frac{K}{2L}D'\hat{v}_{eff} + KM_c]$$

$$= F_m[(\hat{i}_v - \hat{i}_l) + K'\hat{v}_{eff} + K''] \qquad (3.14)$$

$$= F_m[(\hat{i}_v - \hat{i}_l) + K'\left(\hat{v}_{eff} + \frac{K''}{K'}\right)]$$

$$= F_m[(\hat{i}_v - \hat{i}_l) + K'(\hat{v}_{eff} + \gamma)] \qquad (3.15)$$

From the Equations (3.14) and (3.15) the following identification can be made in Fig 3.6.

$$F_m = \frac{1}{\frac{K}{2L}V_{eff}} \qquad (3.16)$$

$$K' = \frac{K}{2L}D' \qquad (3.17)$$

$$K'' = KM_c \qquad (3.18)$$

$$\gamma = \frac{K''}{K'} \qquad (3.19)$$

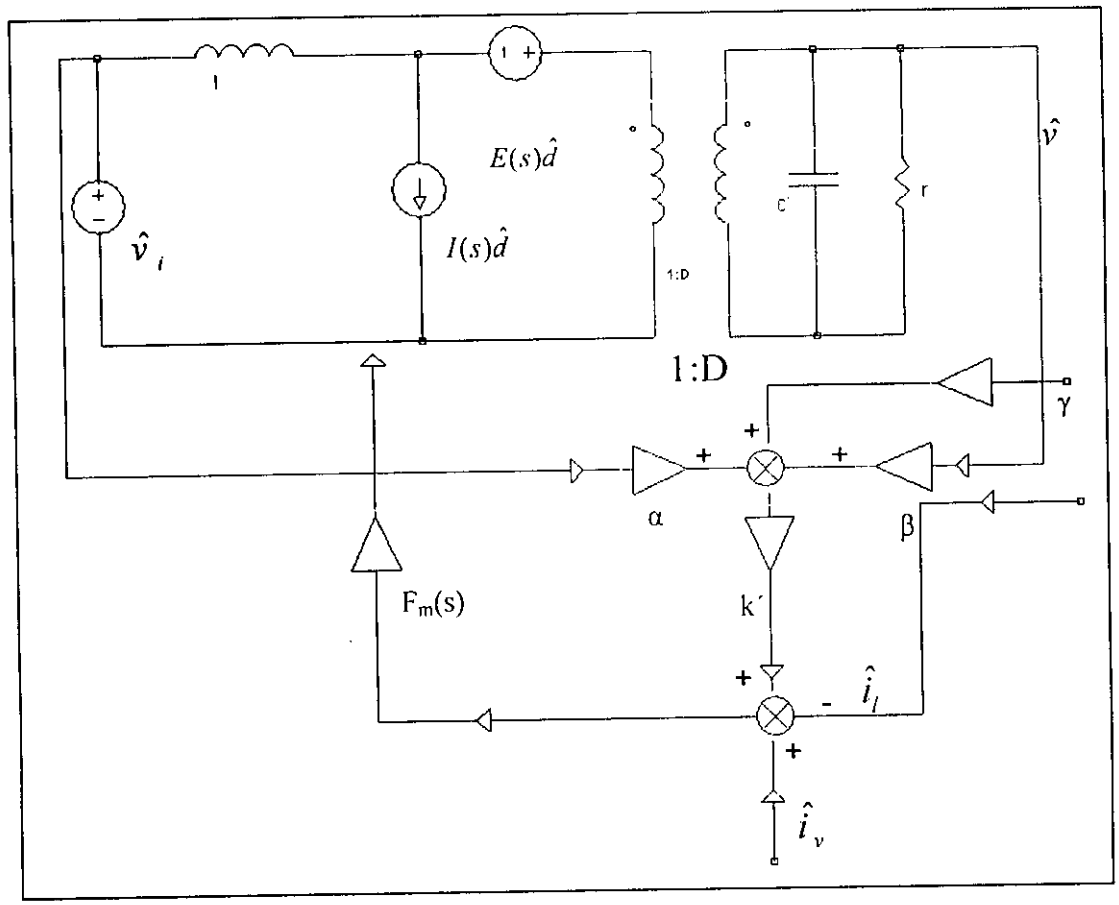

Fig 3.6: *The small signal low frequency model of the proposed converter.*

Hence unlike the modulator model that has been derived in [4], it is found that the gain of the modulator F_m is duty cycle independent. Again, if the slope signal is eliminated, we will have M_c=0 and hence from equations (3.15), (3.18) and (3.19) the following relationship is derived:

$$\therefore \hat{d} = F_m[(\hat{i}_v - \hat{i}_l) + K'\hat{v}_{eff}] \qquad (3.20)$$

Hence, from the equation (3.20), it is evident that the slope compensating signal does not affect the gain of the modulator, which, itself, is duty cycle independent. Moreover, inductor current averaging technique would not be applied here; rather, pulse-by-pulse decision of the current loop will be employed.

All active devices are built on-chip. The device needs only one power inductor and input-output capacitor as the external components.

3.5 Other Necessary Information:

This converter has been practically implemented using 0.5 um single poly double metal processes. The pin configuration and the typical application diagram of the converter have been mentioned in Fig 3.7:

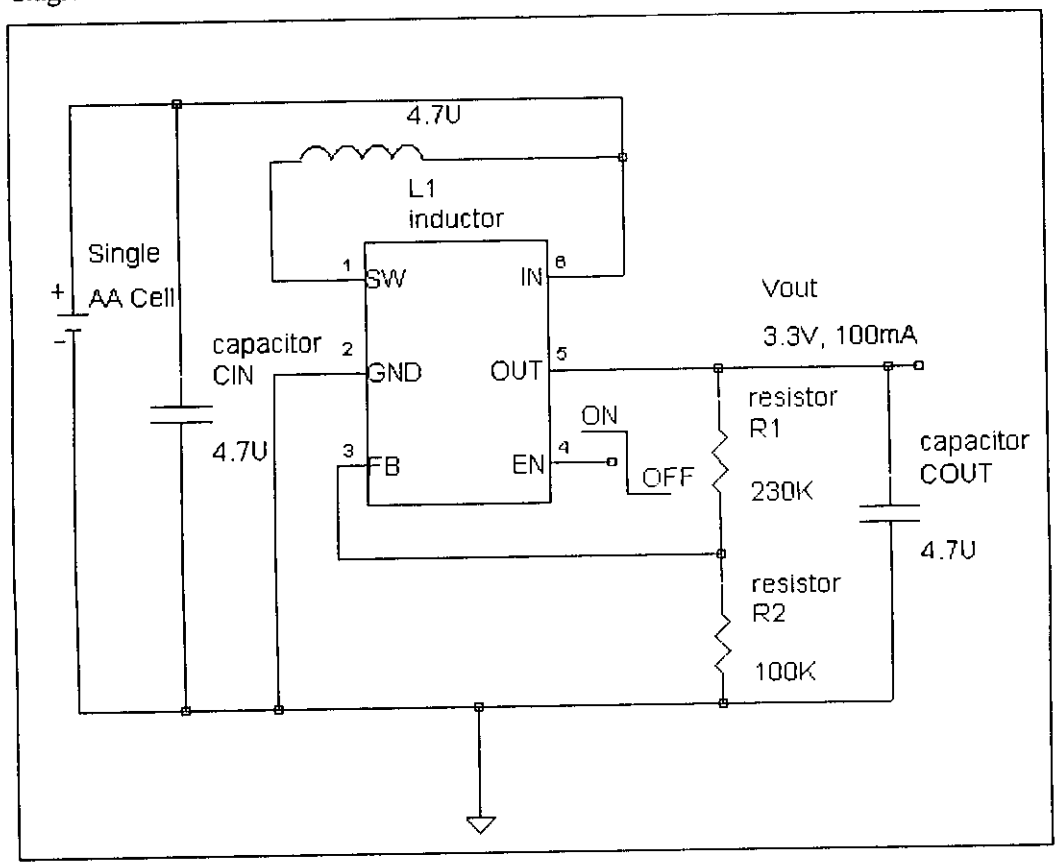

Fig 3.7: *The pin configuration & the typical application diagram of the converter*

Brief Pin Description:

Name	Pin	Type	Function
SW	1	Switch	Inductor is connected between SW and IN.
GND	2	Ground	Ground pin
FB	3	Feedback	Adjustable feedback input, resistor voltage divider is connected between FB & OUT, to have required output voltage.
EN	4	Enable	EN=High: normal operation.
OUT	5	Analog output.	Boost regulator output.
IN	6	Battery input.	Boost regulator input.

Chapter 4

Implementation of the Proposed Converter

The overall functional blocks can be grouped into the following categories:

1. Supply (bias currents and voltages) related blocks.
2. Loop-settling blocks.
3. Switches.
4. Performance enhancement and safety related blocks.
5. Start-up blocks.
6. Main Control Block.

Let's have a closer view of the above mentioned categories.

4.1Supply related blocks:

These blocks and sub-blocks are responsible for providing necessary bias voltages and currents to all other functional blocks. The supply related blocks are:

a) Reference:

Reference block is the heart of all the supply related blocks. This consists of a precise band-gap core. The principle of the band-gap core relies on two groups of transistors running at different emitter current densities. This difference in the current densities cause a difference between the base-emitter voltages, let's call it ΔV_{BE}.

From the large signal behavior of the bipolar transistor and neglecting the base current (for high β_F) of it, we have the following relationship

$$V_{BE1} = \left(\frac{KT}{q}\right)\ln\left(\frac{I_1}{I_{S1}}\right) \tag{4.1}$$

$$V_{BE2} = \left(\frac{KT}{q}\right)\ln\left(\frac{I_2}{I_{S2}}\right) \tag{4.2}$$

and $I_{S1} \alpha A_1$ & $I_{S2} \alpha A_2$ (4.3)

where, $I_1 = I_{C1} \cong I_{E1}$

& $I_2 = I_{C2} \cong I_{E2}$,

I_S => *saturation current*,

A => *base – emitter junction area of a bipolar transistor.*

$$\therefore \Delta V_{BE} = V_{BE2} - V_{BE1}$$

$$= (\frac{KT}{q}) \ln(\frac{A_1}{A_2})$$

$$= V_T \ln(\frac{A_1}{A_2}) \qquad (4.4)$$

For $I_1=I_2$, i.e in the balanced condition of the band-gap core.

$V_T=(\frac{KT}{q})$, is called thermal voltage.

The core, used in the design, has the emitter area ratio of 8:1, i.e. $A_1:A_2=8:1$ and it is shown in the Fig 4.1.

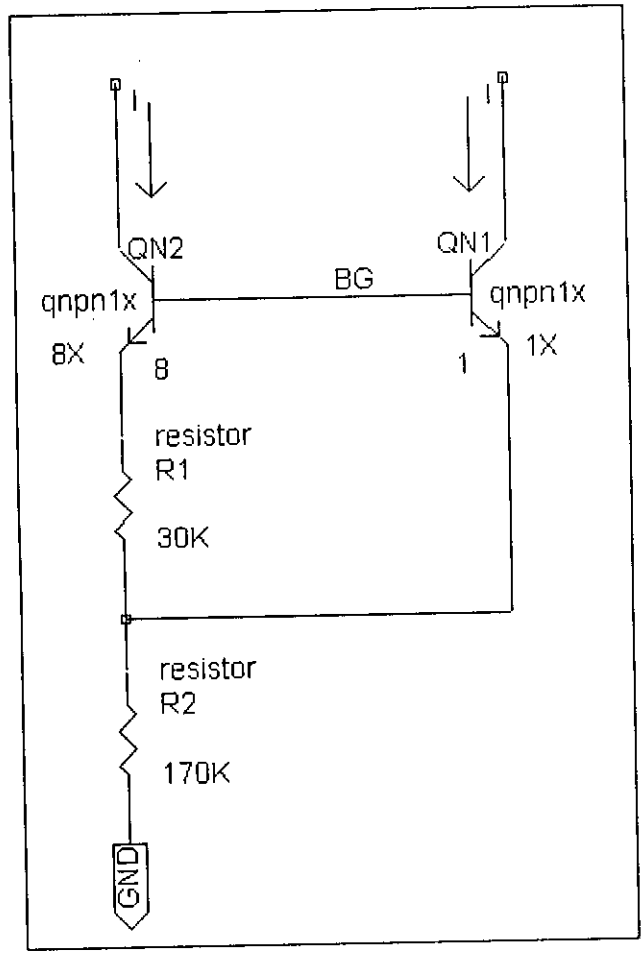

Fig 4.1: *The basic Band-gap core used in the converter.*

In the design, the rich transistor will runs at 8 times the density of the lean ones, and a factor of 8 will cause a 54 mv (i.e. 26mv*ln8) delta between the base-emitter voltages of the two groups. This delta voltage is usually amplified by a factor of about 10 and added to a V_{BE} voltage, i.e.

$$I = \frac{\Delta V_{BE}}{R1},$$

$$BG = 2IR2 + V_{BE}$$

$$= 2\Delta V_{BE}\frac{R2}{R1} + V_{BE}$$

$$\therefore BG = 2(54mv)\frac{170K}{30K} + 0.6$$

$$= 1.212V$$

The beauty of the band-gap reference is the weighted summation of the V_{BE} term, which decreases at the rate of about -2 m.v/°C, and the (delta-V_{BE} term) which grows at about + 2 m.v./°C, to achieve an overall Temperature Coefficient (Tempco) that is substantially zero. As a result, this band-gap voltage remains almost constant with the change in temperature.

Moreover, this circuit uses a feedback loop to establish an operating point in the circuit such that the output voltage is equal to a V_{BE} plus a voltage proportional to the difference between the two base-emitter voltages. If the special measures are not taken, the band-gap circuit halts to other of its two possible solutions i.e. 0 and V_{BE}. In Fig 4.2, the measures to get rid of those problems have been illustrated. At the beginning of the operation, when the 'SHUT' is released, emitters of I53, I54 and I55 remains at the same potential, as no voltage has been built up. A current (called initial current) set by the ON resistance of MP16, flows from the supply to the base of I53 and its operation is initiated. A 2X current of the initial one is drawn by I54 from the diode connected PMOS MP7. Again, this current of MP7 is amplified 40 times by MP8 and a portion of this huge current is injected to the band-gap core via I57 and thus the core comes out of the zero solution. Similarly, measures have been taken so that the band-gap voltage does not stop at V_{BE}. The simulation result of the temperature coefficient of the reference voltage has been illustrated in Fig 4.3, it is seen that, the variation of the band-gap voltage is very negligible over room temperature range (Fig 4.3).

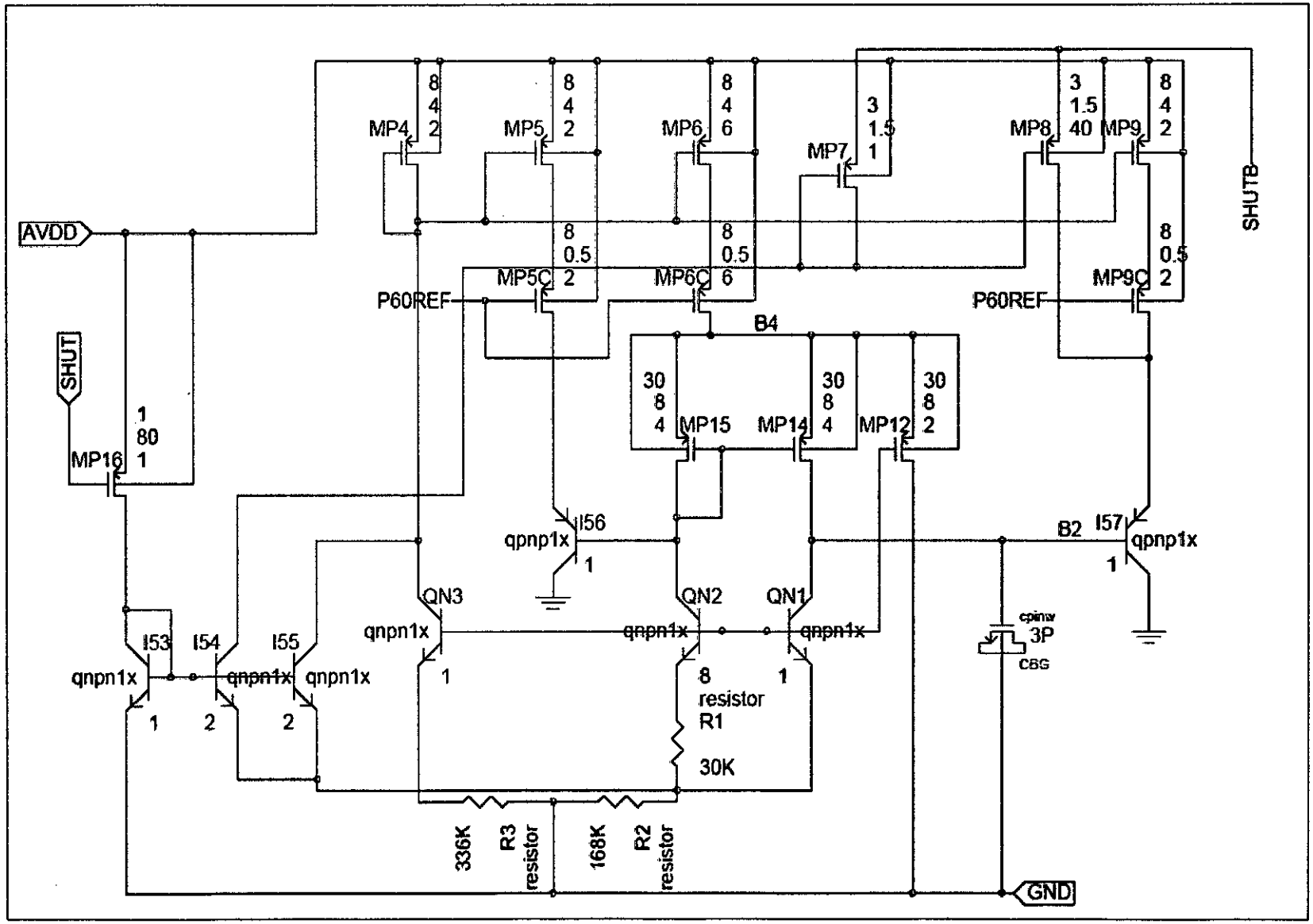

Fig 4.2: Techniques to avoid unexpected solutions of Band-gap in the converter

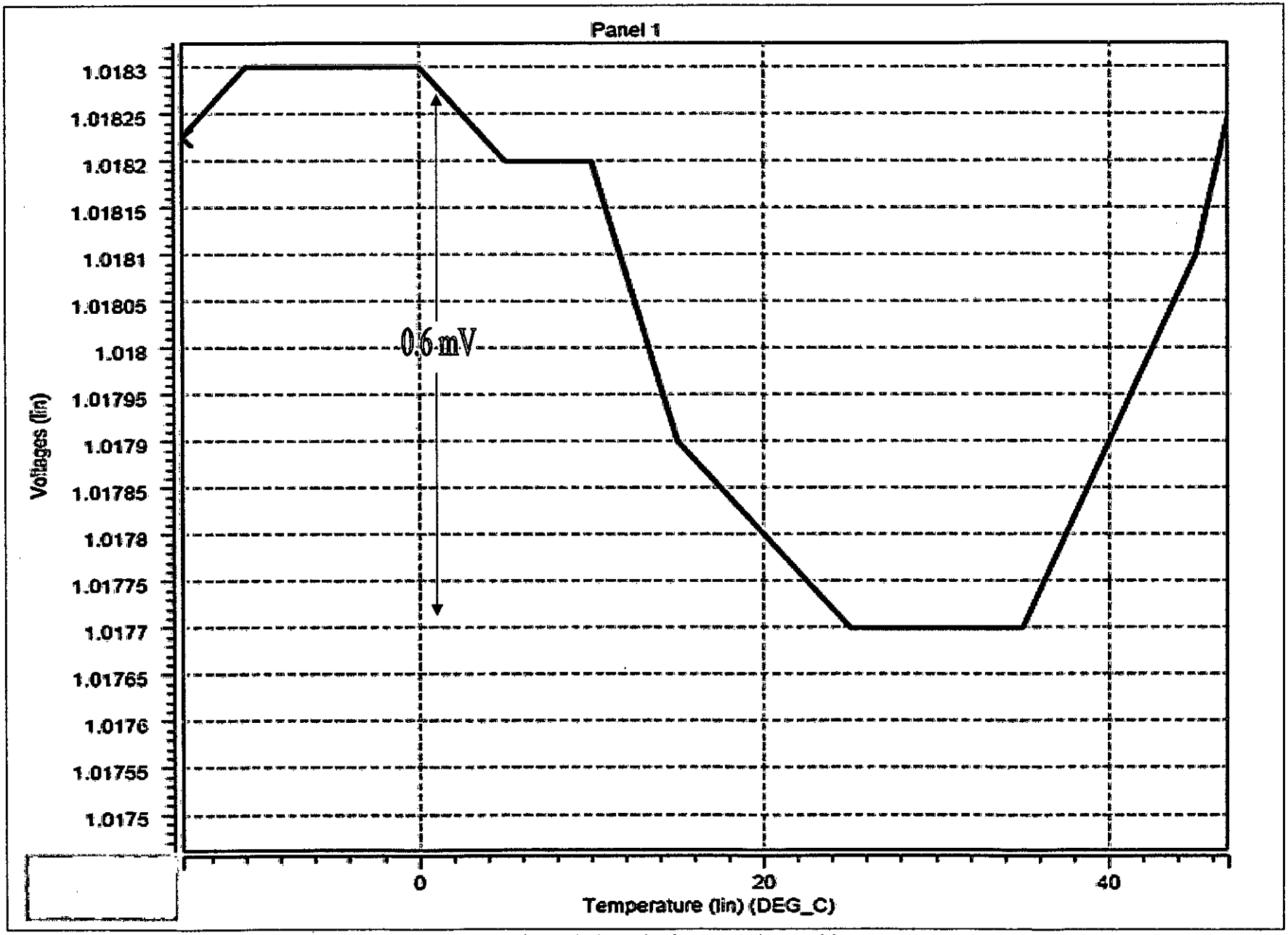

Fig 4.3: The variation of reference voltage with temperature

b) Bias Current Generating Block:

This block provides adjustable bias currents for various functional blocks of the converter based on the operating conditions; i.e. whether the converter is in the start-up mode or in the normal operational mode. The basic structure of the block has been illustrated in Fig 4.4. It also generates signal to indicate if the converter is in the start-up or normal operating-mode. In the start-up mode, a supply-based finely regulated current is provided by this block to have the blocks relevant to this mode to operate smoothly. There are two fail-safe signals available in the converter, one comes from the reference, the under-voltage lock-out signal, that points to the fact that the band-gap voltage is ready and the other comes from this Bias Current Generating Block that indicates if the supply reaches a certain safe limit. When both the conditions are true i.e. the band-gap voltage is ready and the supply has reached a certain safe limit, a logic signal is generated that makes all the operational blocks to take the bias current from the reference block rather than this bias current generating block.

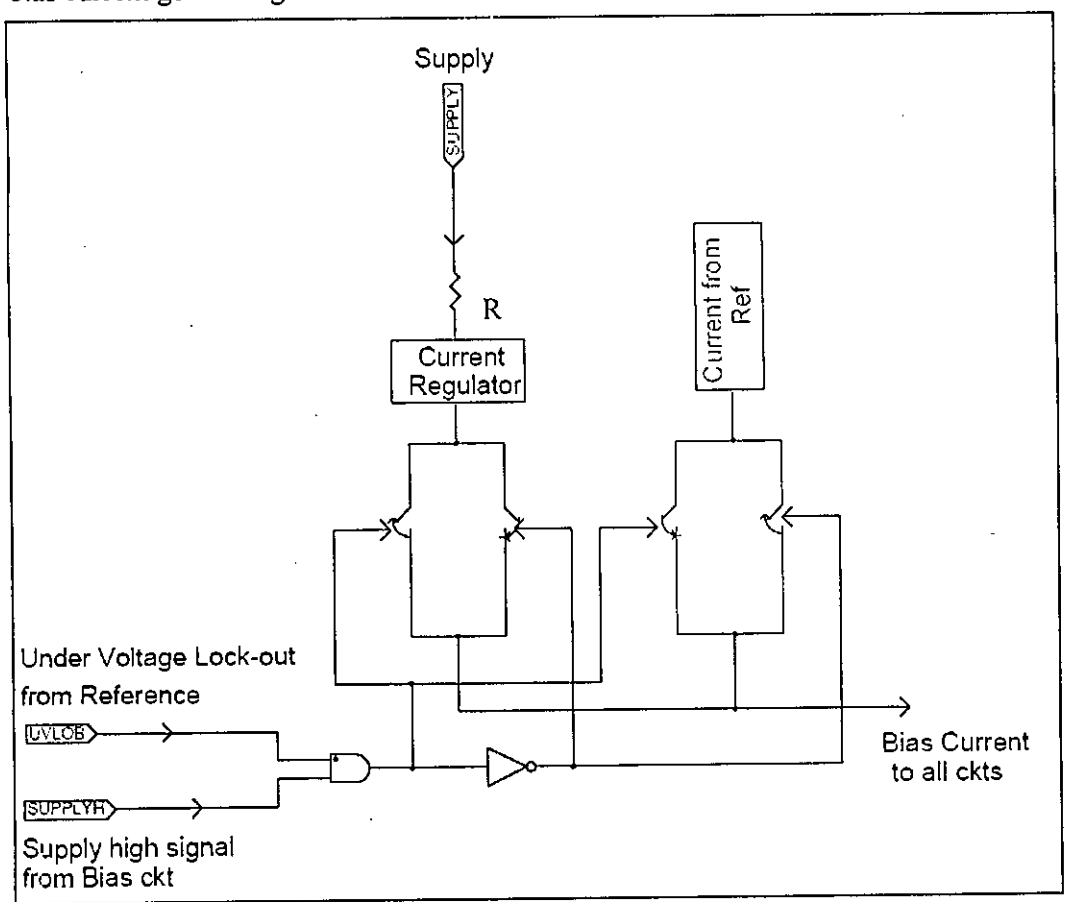

Fig 4.4: *Basic structure of the bias-current generating block of the converter.*

c) Supply Selector:

The bias to all the circuitry of the chip is supplied either from the input voltage or from the output voltage depending on the conditions of the two voltages. At the starting, when the output voltage level is building from zero, the bias to the circuitry is provided from the input voltage bus. Once the output voltage builds up enough to exceed the input level, the supply bus is switched to be fed from the output voltage. This facilitates some of the blocks like driver of the switches, error-amplifier etc. to have faster transient response. The aforesaid switching is accomplished by a block called 'Supply Selector'. This circuit is designed to work at the very low voltage level. As shown in Fig 4.5, a comparator checks the two voltage levels. In the beginning of the operation, input voltage is higher. Hence supply bus is fed from the input voltage through the switch sw2. As the output voltage builds and exceeds the input voltage, the comparator trips causing the switch sw2 to open and sw1 to close. Hence, the supply bus gets connected to the output pin and supply is provided from the output voltage.

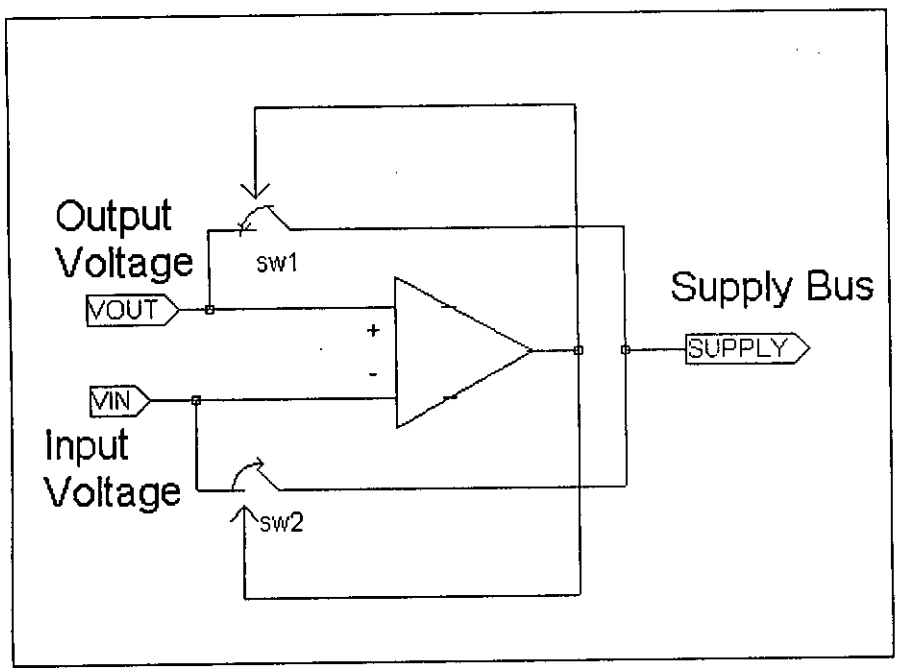

Fig 4.5: *Basic structure of the supply selector block of the converter.*

The comparator used for this purpose has been illustrated in Fig 4.6. A hysteresis has been added to the comparator such that output voltage needs to rise above the input voltage to some extent, to have the 'VOUP' signal of the comparator

'HIGH'. The trans- conductance, gm, of the device POUT is less than that of PIN. Hence the MOS POUT needs more source to gate voltage excursion than that of PIN to have the same Δi , and thus hysteresis is added.

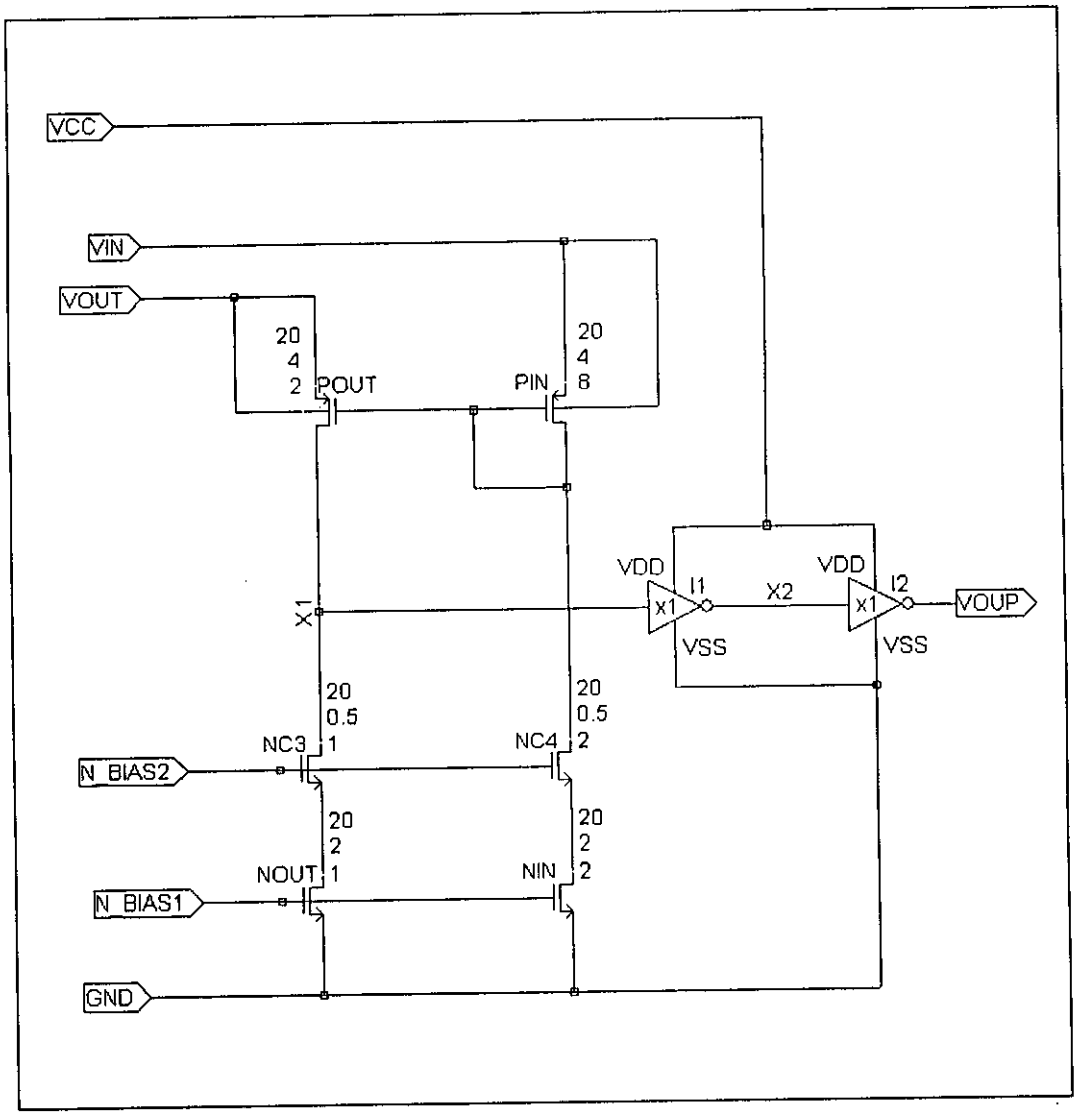

Fig 4.6: *The comparator used for the supply selector block of the converter.*

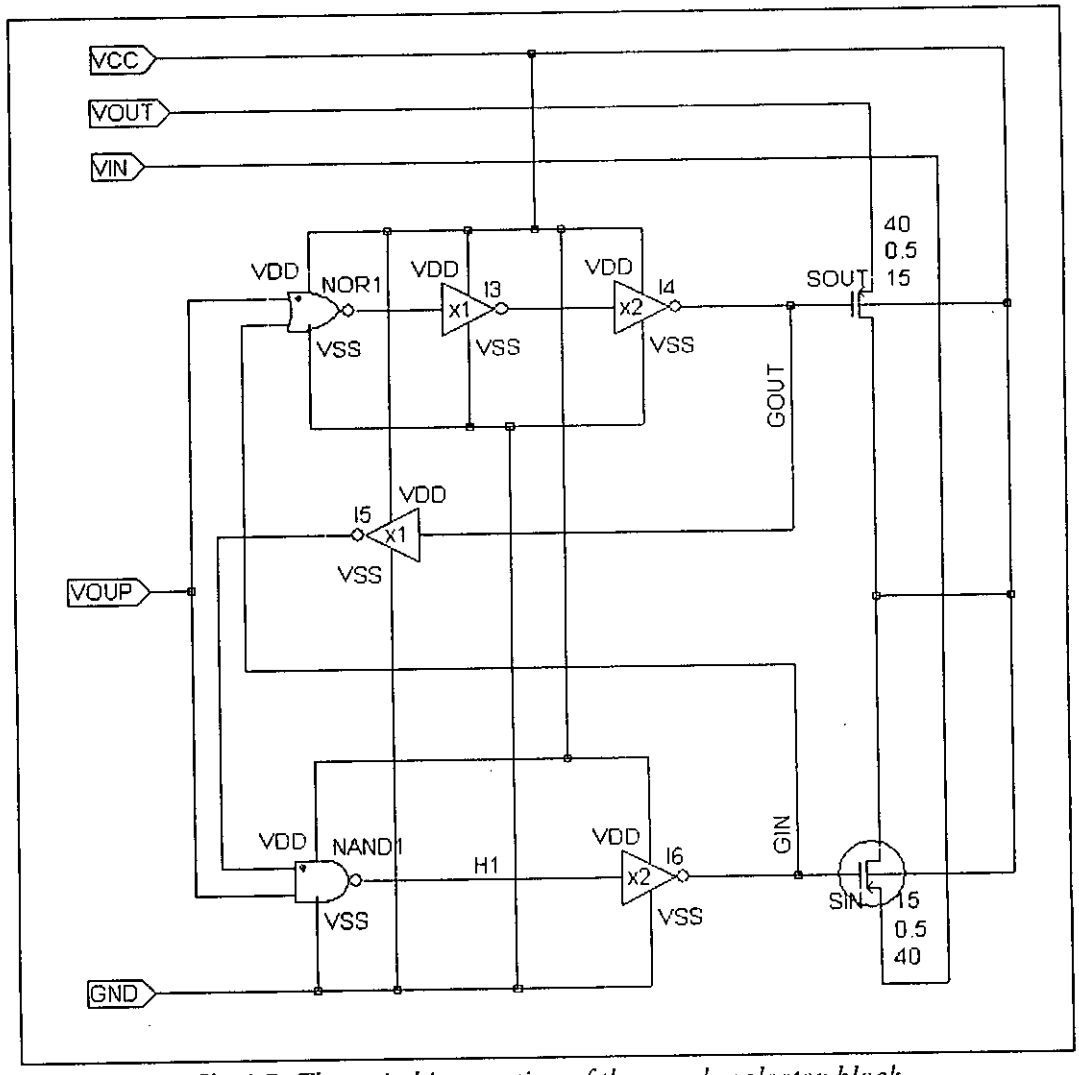

Fig 4.7: *The switching portion of the supply selector block of the converter.*

The basic switching portion of the block has been illustrated in Fig 4.7. Two MOS switches 'SOUT' and 'SIN' are there to connect VOUT and VIN bus to the VCC bus, based on the condition of the signal ('VOUP') derived from the comparator.

4.2 Loop-settling blocks:

The normal loop operation of the step-up regulator is performed by these blocks; an error amplifier and a time generating circuit fall into the category of the loop-settling blocks.

a) Error Amplifier:

The Error Amplifier block is in fact an open loop uncompensated comparator that takes the band-gap reference voltage, feedback voltage (portion of output voltage taken-off by a suitable resistive divider), the voltage at the switch pin and the output voltage as input signals. This amplifier yields a digital signal called 'charge' that initiates the charging cycle of the boost regulator. The basic structure of the error-amplifier has been illustrated in Fig 4.8. The input differential pair for

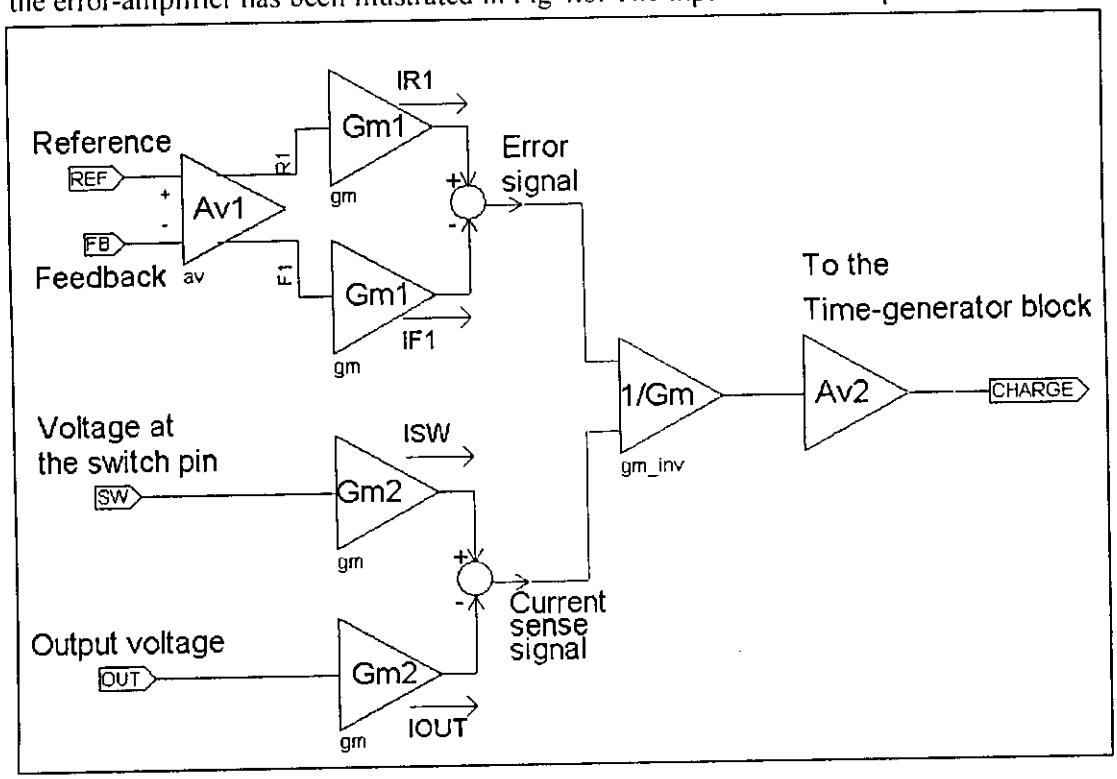

Fig 4.8: *The basic structure of the error-amplifier of the converter.*

REF and FB has been built with MOSFETs and stages of voltage gain have been applied to gain up the differential signal. Differential pairs with gate-drain connected

loads (as shown in Fig 4.9) have been used for the various gain stages in the Avl block in Fig 4.8.

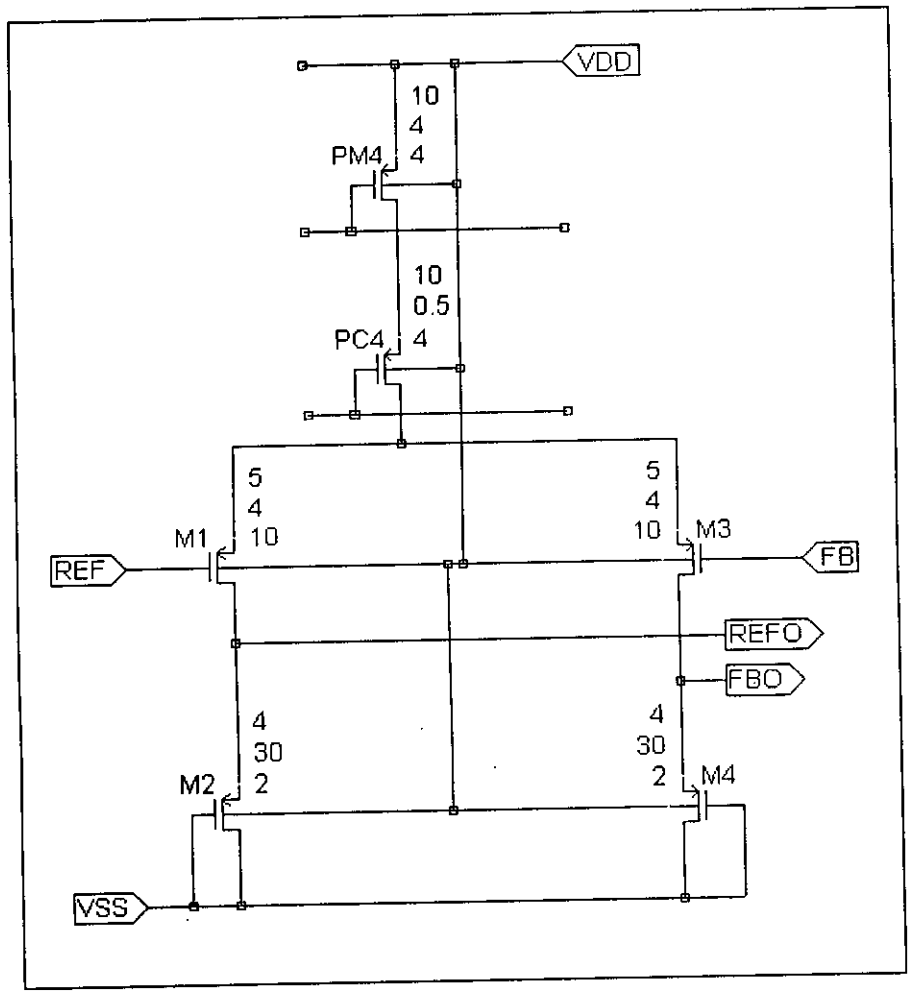

Fig 4.9: *A voltage gain stage used in the error-amplifier of the converter.*

The differential voltage gain of the pair shown in Fig 4.9 is calculated as following:

$$A_v = g_{m1} R_{out}$$

$$= g_{m1}\left(\frac{1}{g_{m2}}\right)$$

$$= \frac{\sqrt{2I_D\beta_1}}{\sqrt{2I_D\beta_2}}$$

Where, $\beta=\mu_p C_{ox}(W/L)$

$$= \sqrt{\frac{Z_1}{Z_2}}$$

$$= \sqrt{\frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}}}$$

$$= \sqrt{\frac{\frac{50}{4}}{\frac{4}{15}}}$$

$$= 6.85$$

Hence, if the difference between the signal REF and FB is 10mV, the difference between the signal REFO and FBO will be 68.5mV. Another stage cascaded with this stage, will further amplify the difference. In this way, the Av1 block will gain up the difference between the input signals. After amplification in the Av1 block, two more signals are found at R1 and F1 nodes and these node voltages are then converted into current signals by trans-conductance blocks, gm1 yielding IR1 and IF1 respectively. The difference between these two signals produces 'Error Signal'. The voltage signals at the SW and OUT pins are directly converted to current signals using similar trans-conductance blocks, without any sort of amplification. The difference between these two current signals will produce 'Current sense signal' (Fig 4.8). Before obtaining 'Error signal' the difference between the reference and feedback voltage has been amplified, whereas, the voltage at SW and OUT pins are directly converted to current signals. Hence, the 'Current sense signal' has more linearity than the 'Error signal'. Moreover, as the number of the stages from reference and feedback nodes to the summing node is larger than that from SW and OUT nodes to the same point, the response of the 'Current sense signal' is faster than that of the 'Error signal', on pulse by pulse basis. This ensures the path of the current signal to be faster than that of the voltage signal. This has been done intentionally, as it is one of the requirements for a loop, having another loop inside it, to be stable. The 'Current sense signal' and the 'Error signal' are then algebraically summed and the resultant signal is converted to a voltage signal by a 1/Gm block (as shown in Fig 4.8). As shown in Fig 4.10, the current signals have been added on the basis of the

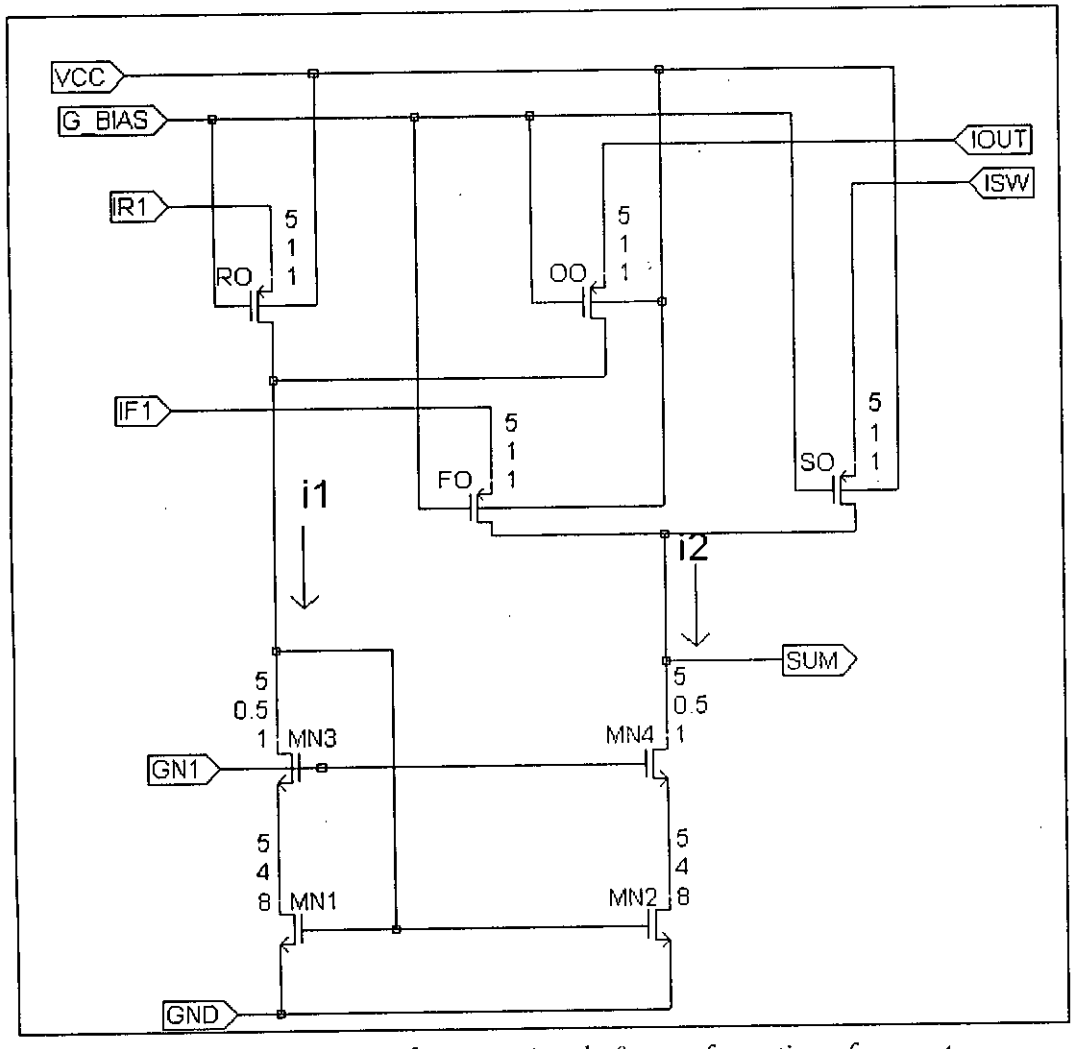

Fig 4.10: *Addition of current signals & transformation of current signals to a voltage signal in the error amplifier of the converter.*

required polarity of the signals corresponding to reference, feedback, switch and output voltages. The node 'SUM' is a high impedance node and therefore, a small difference between i1 and i2 will cause the node to move to a huge quantity, based on the polarity of the difference. And finally, the 'SUM' signal is gained up, using a single stage gain block, Av2, as shown in Fig 4.11. The single stage gain block is, in fact, a basic CMOS inverter, where one device serves as a common-source amplifier (NM2) and the other device acts as an active load (PM1). NC2 and PC1 are NMOS and PMOS cascode devices used to reduce the transient response time of the node 'PRELOGIC' by minimizing the effect of the parasitic gate-source and gate-drain capacitances associated with NM2 and PM1. Among these, the gate-drain capacitance is the most troublesome due to the Miller effect. Since the

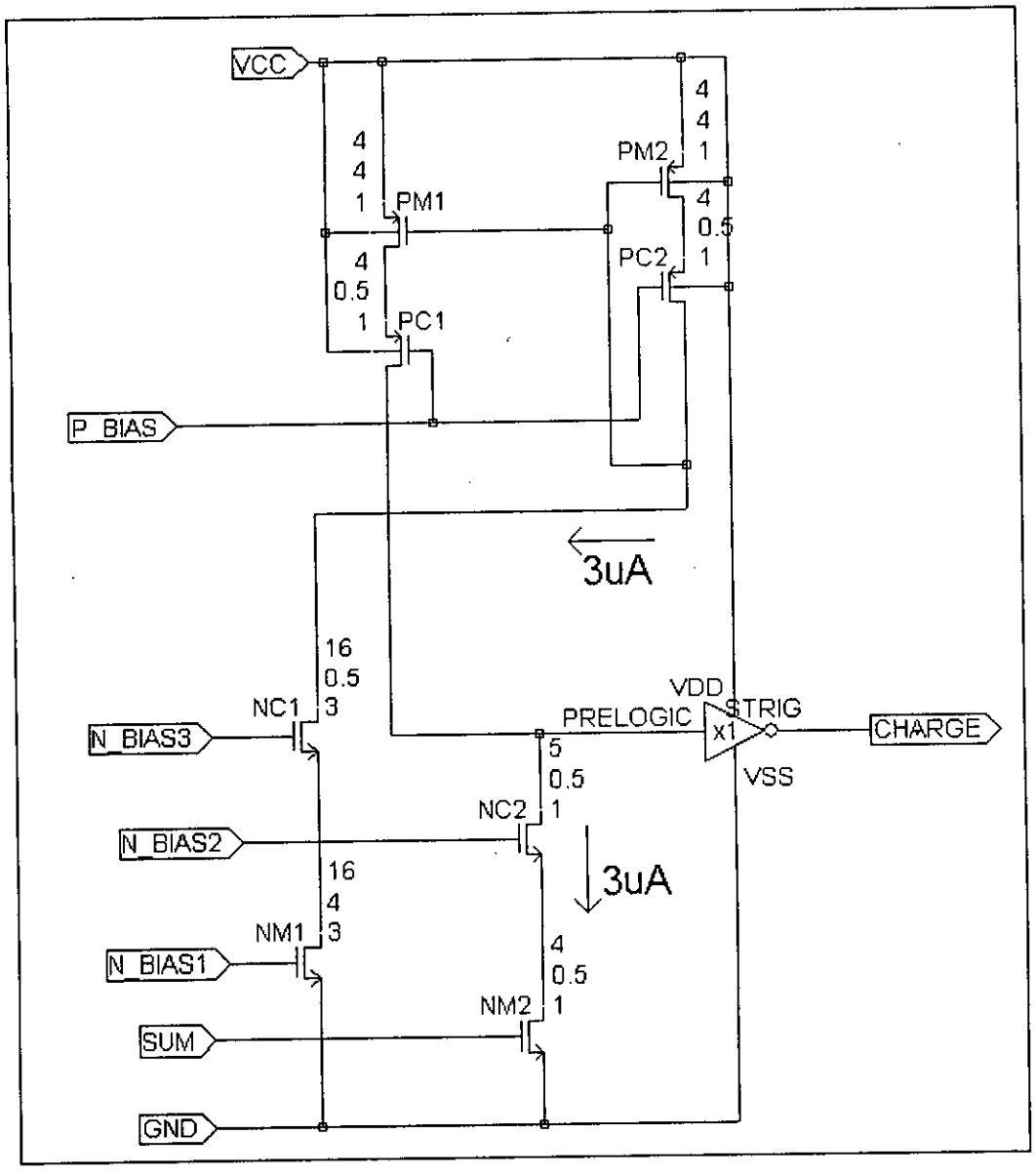

Fig 4.11: *The single stage gain block used in the error amplifier of the converter.*

Miller-effect capacitance reflected to the input depends on the voltage gain at the drain of NM2; it can be kept low by making $(W/L)_{nm2} \approx (W/L)_{nc2}$, as it is evident from the equation (4.5). Neglecting the body effect, the voltage gain from the point 'SUM' to the drain of NM2, in Fig 4.10, we have the following relationship:

$$A_{vd} \approx -\frac{gm_{nm2}}{gm_{nc2}} = -\sqrt{\frac{(W/L)_{nm2}}{(W/L)_{nc2}}} \qquad (4.5)$$

Moreover, the cascode connection increases the output impedance by a certain factor. Considering that, both NC2 and NM2 operate in active region, with I_D $=3uA$ and $V_A=50V$, we have the output resistance r_0 of each transistor given by,

$$\begin{aligned} r_0 &= \frac{V_A}{I_D} \\ &= \frac{50}{3\times10^{-6}} \\ &= 16.67\,M\Omega \end{aligned}$$

Now, if the resistance looking into the drain of NC2 is R_{02}, we have the following relationship:

$$R_{02} = r_{0nc2}(1 + gm_{nc2}r_{0nm2}) + r_{0nm2} \qquad (4.6)$$

Hence, using the values for the parameters, we 've from the equation (4.6),

$$\begin{aligned} R_{02} &= 16.67\times10^{6} \times \left(1 + \sqrt{(2\times3\times10^{-6}\times60\times10^{-6}\times10)} \times 16.67\times10^{6}\right) + 16.67\times10^{6} \\ &= 16.7\,G\Omega \end{aligned}$$

Hence voltage gain A_v from the node 'SUM' to 'PRELOGIC' is given by

$$\begin{aligned} A_v &= gm_{nm2} \times R_{02} \\ &= \sqrt{(2\times3\times10^{-6}\times60\times10^{-6}\times8)} \times 16.7\times10^{9} \\ &= 896.2 \end{aligned}$$

Therefore, a small excursion of the 'SUM' signal is gained up to the rail-to-rail excursion using this stage.

b) Time Generator:

Time generator generates the ON time that is inversely proportional to the input voltage and the minimum OFF time. Moreover, it controls the duration of the charge and the boost phases based on different conditions of the overall chip. Time generator can be divided into two parts; 1) Analog Part & 2) Logic Part.

The Analog Part has been shown in Fig 4.12. The basic principle of this time generation process depends on the well known property of a capacitor, being charged by a current source. We know, for a capacitor of capacitance C, being charged by a fixed current I, meets the following condition:

$$\frac{I}{C} = \frac{\Delta V}{\Delta t} \qquad (4.7)$$

Considering the generation of ON time, when CHR signal is TRUE (BST signal is FALSE, simultaneously) the switches SW1, SW2 & SW3 will be opened and the switch SW4 will be closed. As a result, the capacitor c(=3.6pf) will be charged by the constant current mI. A ramp, starting from 0, will be generated at the node B1. At that span of time, the node TON will be pulled to a high voltage (supply).When this ramp exceeds the base-emitter voltage of QON, it will turn ON and will pull down the node TON. Now ON time will be the span of time from the instant CHR signal becoming TRUE to the instant QON turning ON (as illustrated in the timing diagram in Fig 4.14). The current I is generated as:

$$I = \frac{V_{IN} - V_{BE}}{R_1} \qquad (4.8)$$

$$\Rightarrow I \alpha V_{IN} \qquad (4.9)$$

Again, rewriting equation (4.7), in terms of V_{BE} and T_{on}, we have

$$\frac{I}{C} = \frac{V_{BE}}{T_{on}}$$

$$\Rightarrow T_{on} = \frac{CV_{BE}}{I}$$

$$\Rightarrow T_{on} \alpha \frac{1}{I} \qquad (4.10)$$

Hence, from the equations (4.9) and (4.10) we have the following relationship:

$$T_{on} \alpha \frac{1}{V_{IN}} \qquad (4.11)$$

The relationship in equation (4.11) is one of the unique features of the loop in normal operation.

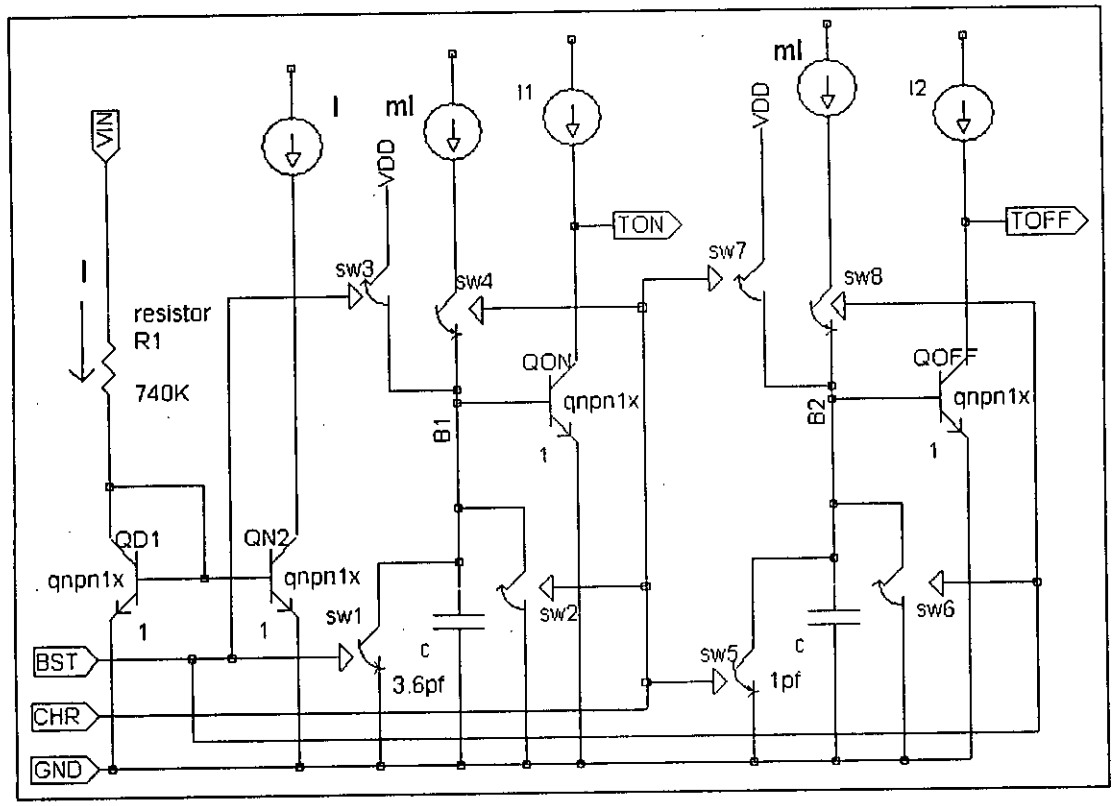

Fig 4.12: *The analog part of the time-generator block of the converter.*

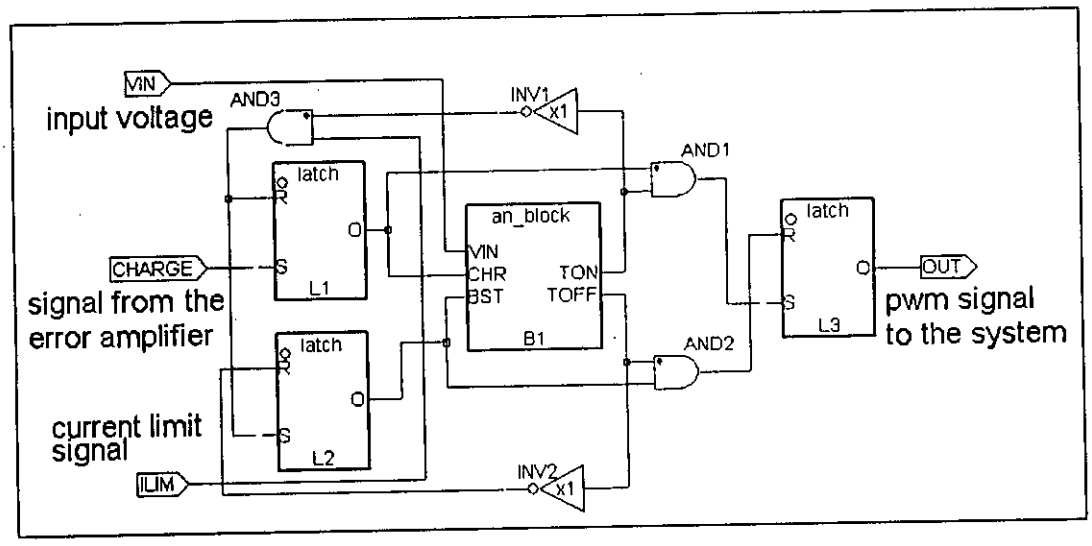

Fig 4.13: *The overall time-generator block of the converter.*

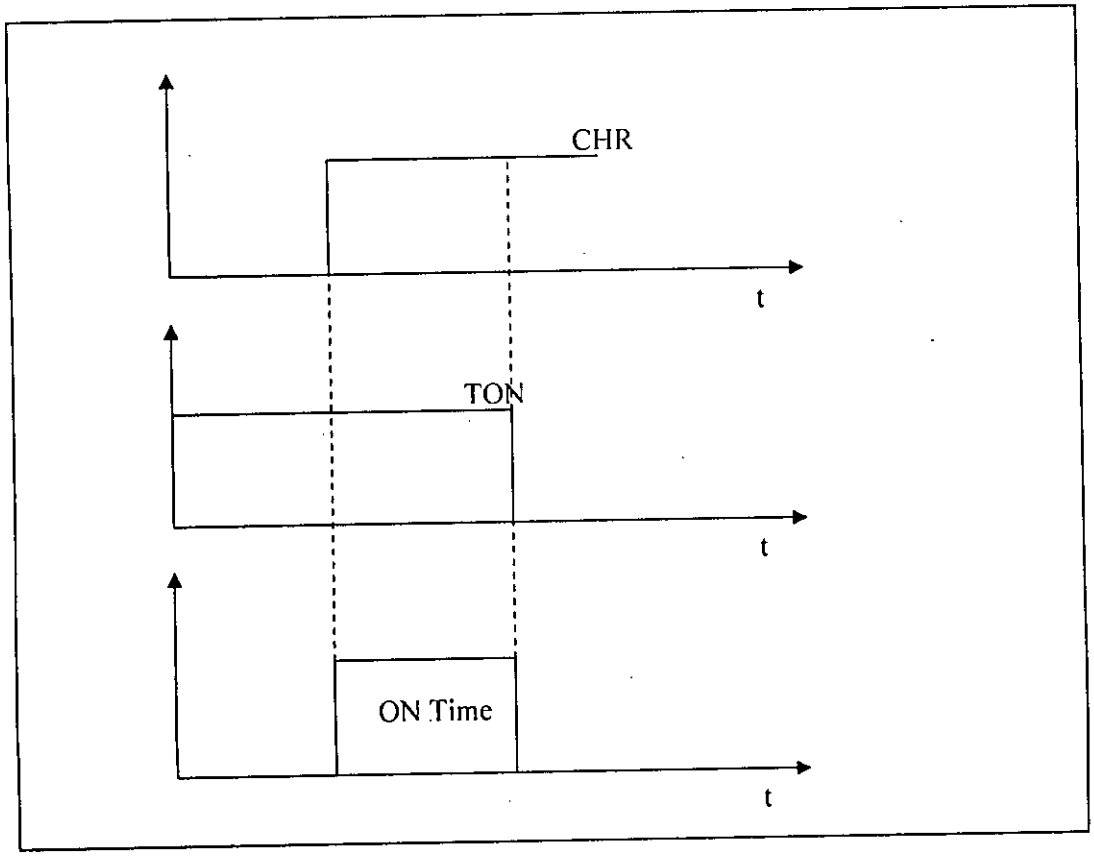

Fig 4.14: *The ON time to be extracted in time-generator block of the converter.*

On the other hand, the digital part, consisting of some asynchronous latches and logic gates, converts the signal, generated discretely on TON and TOFF nodes, to the PWM signal as required by the system depending on all the prevailing conditions, e.g. the conditions when the current-loop breaks or when the peak current through the inductor reaches the current limit or when the converter runs at the discontinuous conduction mode etc. The asynchronous latches are actually reset dominant flip-flops.

Depending upon the signal from the error-amplifier i.e. 'charge' in the Fig 4.13, the whole Time Generator block produces necessary signals for the system. Based on some conditions of the 'charge' signal, the results have been illustrated in the timing diagrams on Fig 4.15 & Fig 4.16.

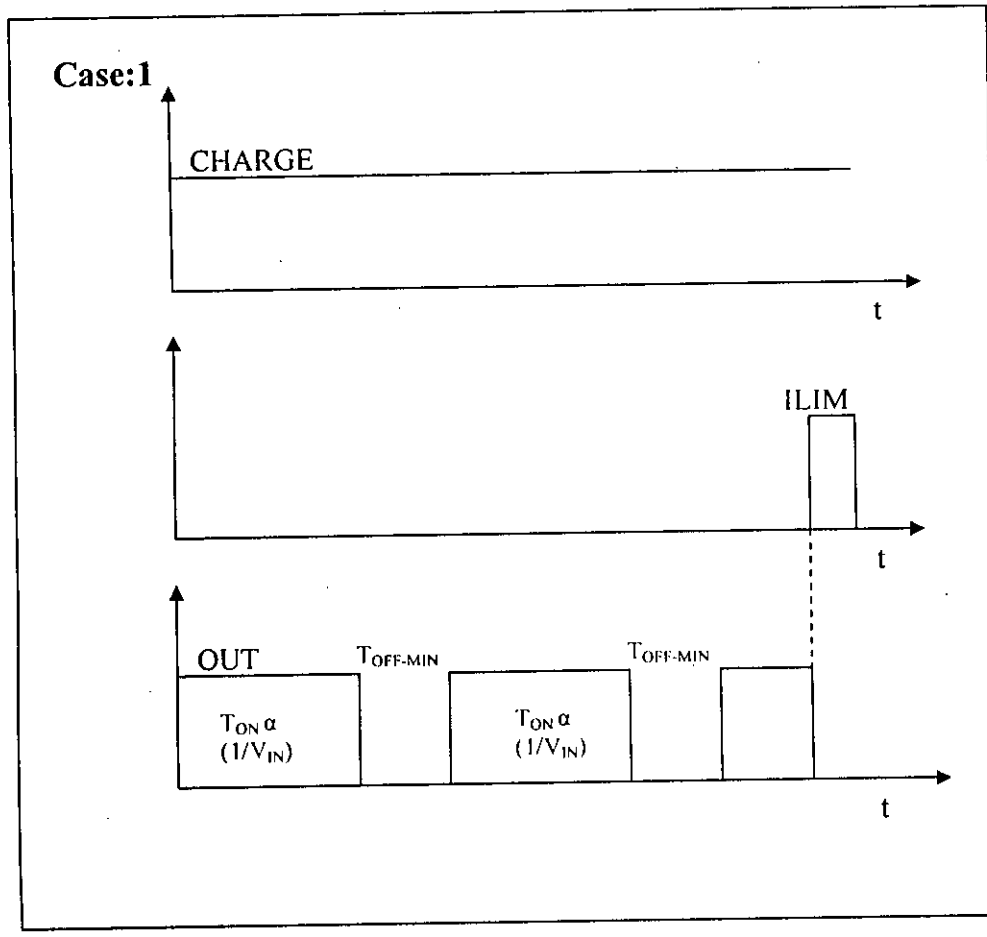

Fig 4.15: The *output signal, in time unit, for open loop operation of the time generator block of the converter.*

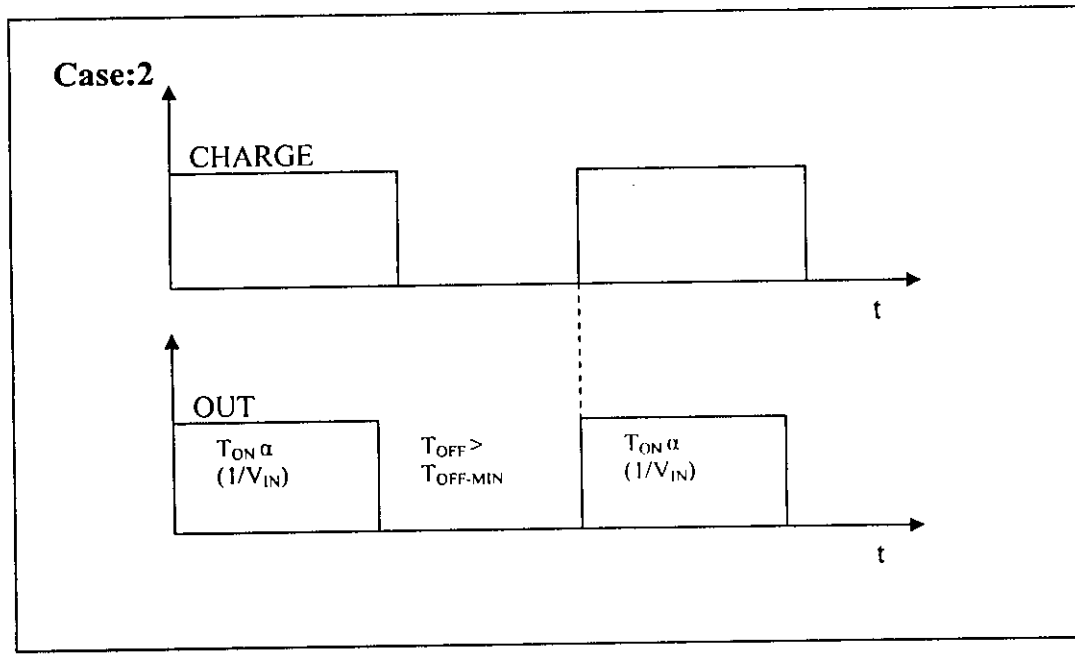

Fig 4.16: *The output signal, in time unit, for normal loop operation of time generator block of the converter.*

As shown in Fig 4.15, (case:1) the error-amplifier has produced a prolonged 'charge' signal, which takes place at the open-loop condition. As a result, the time-generator block is producing timing signal of ON time inversely proportional to the input voltage and OFF time equal to the minimum off time of the block. As soon as the current limit is hit, ON time terminates. In Fig 4.16 (case:2), the error-amplifier is producing regular signal, which is the case for normal loop operation. Hence, the time-generator block is producing timing signal of ON time inversely proportional to the input voltage but now OFF time is the required OFF time needed to have the expected duty cycle and of course, this OFF time is greater than the minimum OFF time of the block.

A real time transient simulation result has been shown in Fig 4.17. A prolonged 'Charge' signal has been applied and the input voltage has been swept from 1V to 4V. As a result, the Time Generator block will run at the minimum OFF time ($T_{off\text{-}min}$), which is invariant of the input voltage, and the ON time (T_{on}) will decrease with the increase of the input voltage.

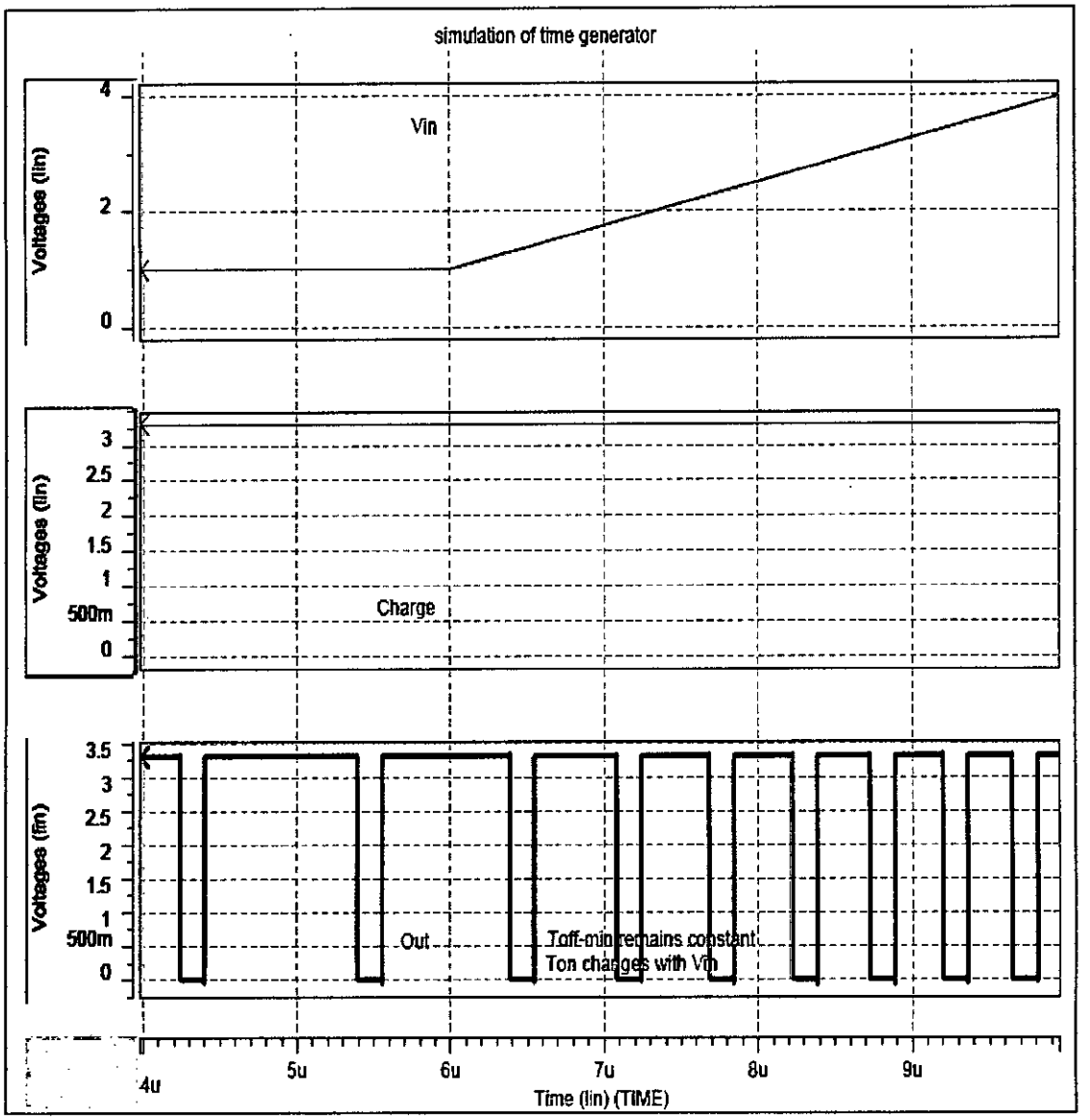

Fig 4.17: *Simulation result of the time generator with the change in input voltage*

From Fig 4.17, it is evident that the minimum OFF time is 150 nS and this time is retaining its value though the ON time is changing with the input voltage.

4.3 Switches:

This converter is a synchronous boost regulator. Hence two switches, namely NSW (NMOS switch) and PSW (PMOS switch), are switched alternately for the charge and the boost phase, respectively. Since most of the silicon area is used up for the two power devices, it is required to optimize the given silicon area for the efficient operation of the converter. In designing of the switches several factors are taken into account:

a). Total resistance,

b). the percentage of channel resistance in total resistance,

c). the current carrying capability of each segment of the switch.

In order to increase the efficiency of the converter, one of the requirements is to reduce the I^2R loss of the switches and for that purpose the total resistance of the switch needs to be reduced. Total resistance includes channel resistance, parasitic resistances of metal layers, metal to metal contact, metal to diffusion contact and diffusion resistance. However, this reduction, for a given silicon area, depends on some parameters like the aspect ratio of the switches, orientation of the switches, the pitch of the segments, the number of metal layers, the number of contacts among different metal layers or between metal layer and diffusion etc.

We want to have the total resistance dominated by the channel resistance, as it is the more predictable part than any other sorts of resistance of the switch. The channel resistance, as we know, is derived by the following relationship:

$$R_{ch} = \frac{1}{\beta(V_{gs}-V_t)}$$

To have the effect of the other resistances of the switch, minimized, several metal layers (at least 2) are used in parallel, number of metal to metal and metal to diffusion contacts etc. are increased.

Each type of metal has a safe current carrying capacity, above which there may have some destructive effect. Hence, while designing a switch, special care has to be taken in this respect.

Referring to Fig 4.18, a segment of switch with only 4 layers has been illustrated. Here metal layer is the top most layers, and then contact, then polysilicon and diffusion lies in the bottom most position.

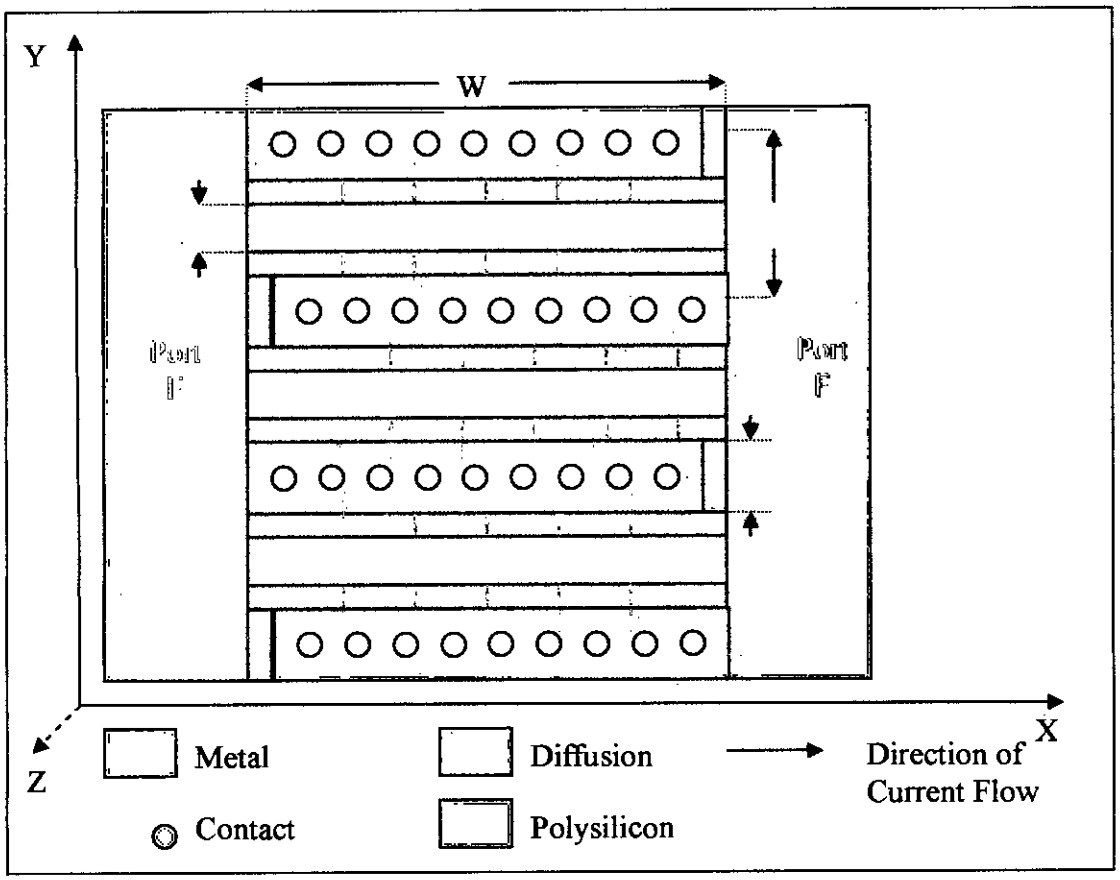

Fig 4.18: *A sample segment of a switch used in the converter.*

The switch segment shown in Fig 4.18, consists of four fingers of breadth B, two of which are connected to Port E and the remaining two connected to Port F. At first, the current enters the two fingers connected to port E, through the metal layer in the X direction. It then flows downward in the Z direction through the contacts to the diffusion and reaching the diffusion area it then flows in the Y direction through the channels in that plane, underneath the poysilicon gates, comes upward through the contacts to the metal layer of the fingers connected to Port F. Hence, for the channel resistance we have,

$$R_{ch}\alpha\frac{L}{W}$$

As W of each finger is increased or gate length L is decreased or both, the channel resistance is decreased and vice-versa. Again, for the parasitic resistance of metal and diffusion, we have,

$$R_x\alpha\frac{W}{B}$$

Hence, with W the parasitic resistance of the switch increases. Hence, to have total resistance minimized and the contribution of channel resistance to the total resistance, maximized, an optimization is needed. Moreover, for the same area, these two features will be changed with aspect ratio, orientation of the switch with respect to the direction of current flow etc. Besides, the breadth B of each finger has to be optimized for the maximum current density.

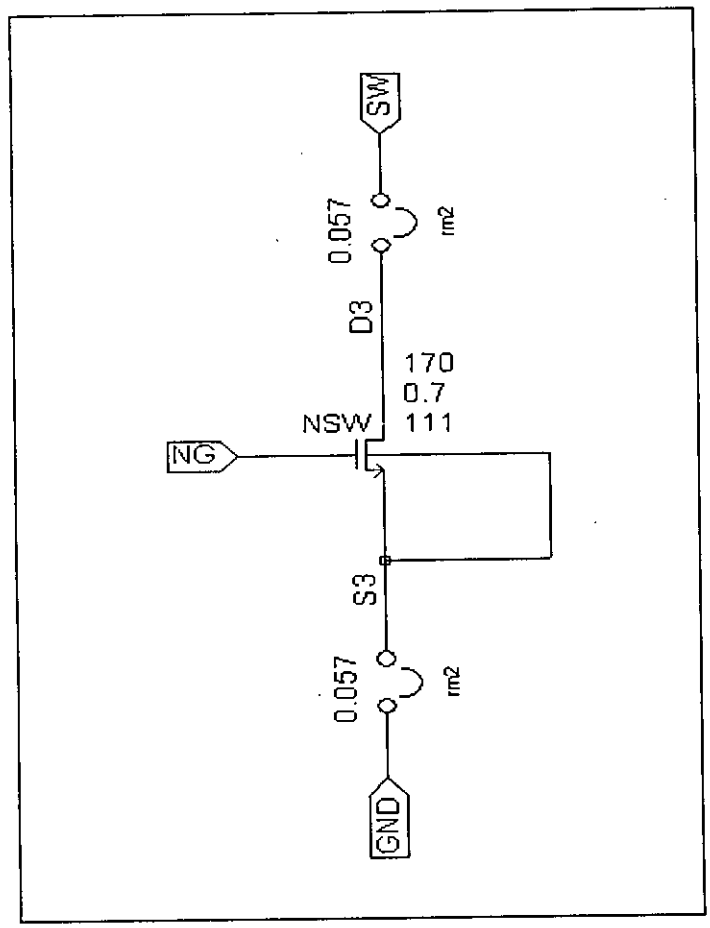

Fig 4.19: *The NSW, of the converter, for the simulation purpose*

For the simulation purpose, the switch is modeled as shown in Fig 4.19. Here a normal NMOS is used with its size calculated considering the required optimization of all the resistances for a given area. The channel resistance is calculated by SPICE from its information of size. The resistances for the parasitic elements are lumped in each side of the MOS, as shown.

4.4 Performance Enhancement and Safety Related Blocks:

Some of these blocks enhance the overall performance and ensure safe operation by providing enough drive to a huge gate , stopping the voltage across the PSW to go to zero and eventually becoming negative; again some blocks limits current through the inductor to go above a certain level, prevent the turning ON of the two switches simultaneously etc. The performance and safety related blocks are namely:

a. The Current Limiter:

The Current Limiter block senses the peak current through the inductor during the charge phase of it and limits that current to a safe level for that inductor. An inductor has a current bearing capability beyond which it may saturate and ceases to have its inductive effect or it may burn (as it is the case for an air-core inductor). The Current Limiter, used in the chip, is actually a comparator, which compares the peak inductor current during the charge phase to a programmed current level and

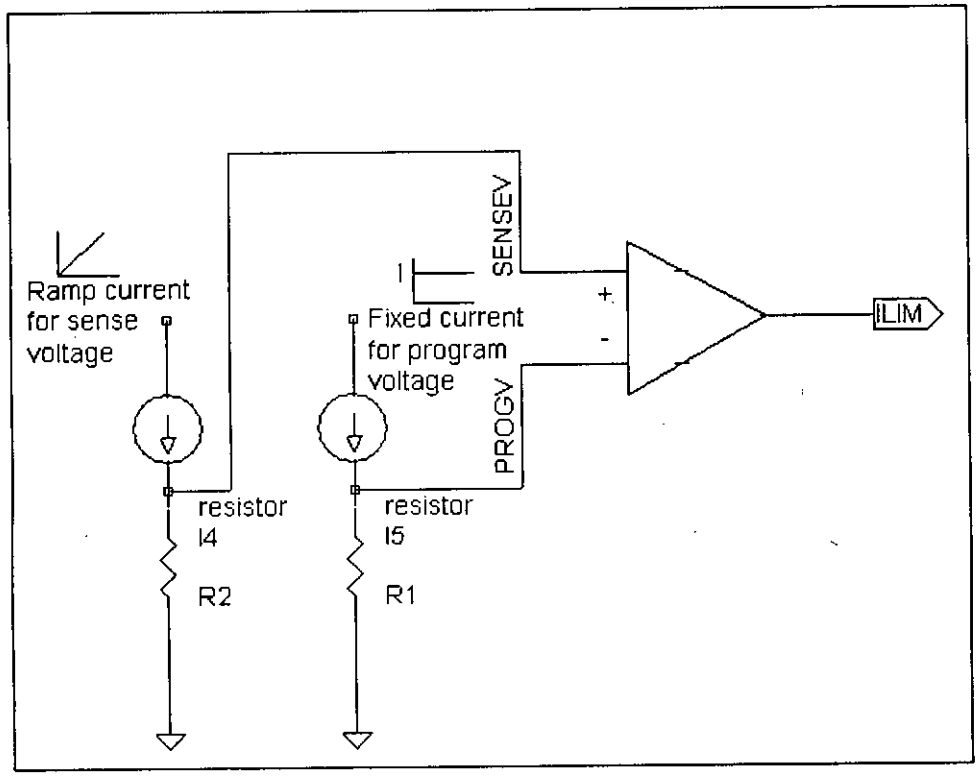

Fig 4.20: *The operational methodology of the current limiter of the converter*

trips when the aforesaid peak current exceeds that programmed level. The peak and programmed currents are, however, converted to voltage levels using resistors (Fig 4.20), before the comparison is accomplished. As shown in the Fig 4.21, 15uA current is passing through the program resistor R1 (R=8.222K) to have the program voltage at the node 'PROGV'=123mV. The node 'CS' is connected to the sense resistor, through which a portion of the inductor peak current flows. The portion of the current flowing through the resistor connected at the node 'CS' generates a sense voltage. In normal

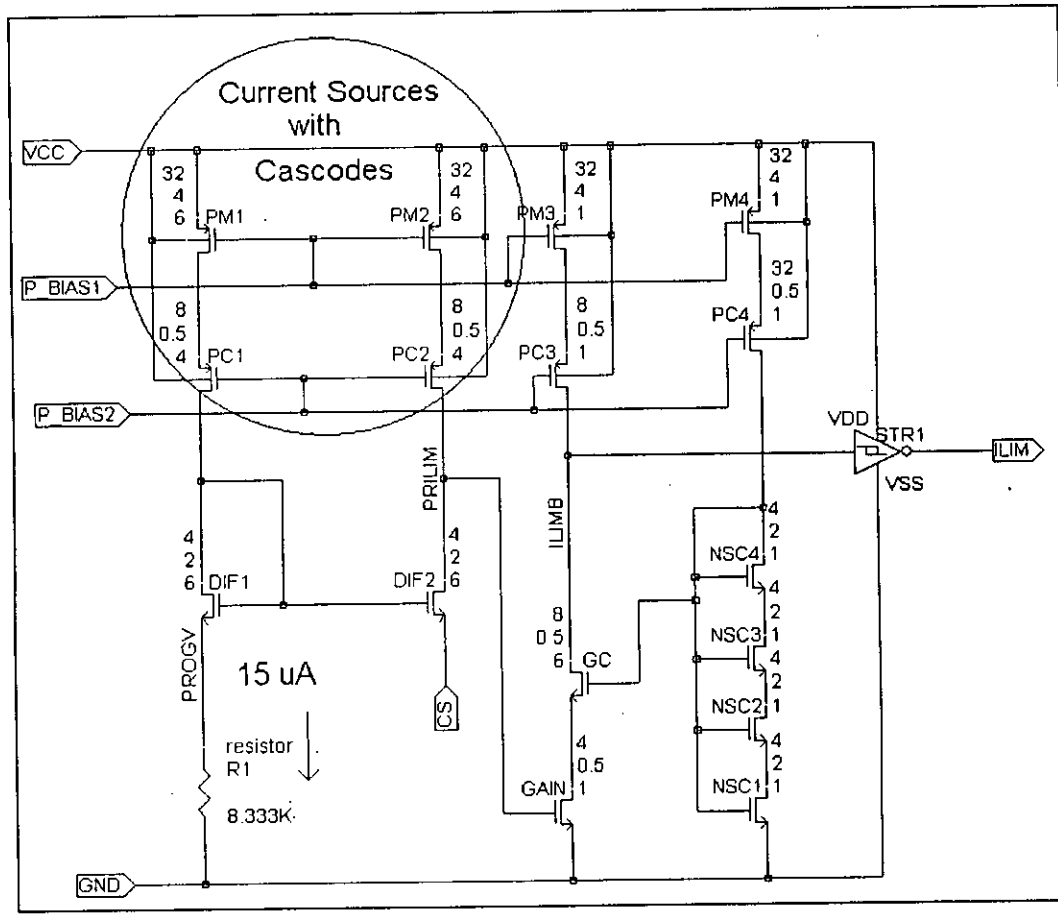

Fig 4.21: *The implementation of the current limiter of the converter*

operation, this sense voltage remains lower than the program voltage at 'PROGV', causing the drain-source voltage of DIF1 to be lower than that of DIF2, in Fig 4.21. As a result, the node 'PRILM' is pulled below the threshold voltage of the MOS 'GAIN', because of the higher strength of DIF2. When the peak current through the inductor exceeds the programmed limit, the voltage at the node 'CS' becomes higher than that at the node 'PROGV' causing the MOS DIF2 to squeeze in strength. As a result, the push current at the node 'PRILM' becomes higher than the pull current at

that node and the node is pulled above the threshold voltage of the MOS 'GAIN', causing it to operate as a gain element. Hence, 'ILIMB' is then pulled down to the ground rail causing the 'ILIM' signal to be TRUE.

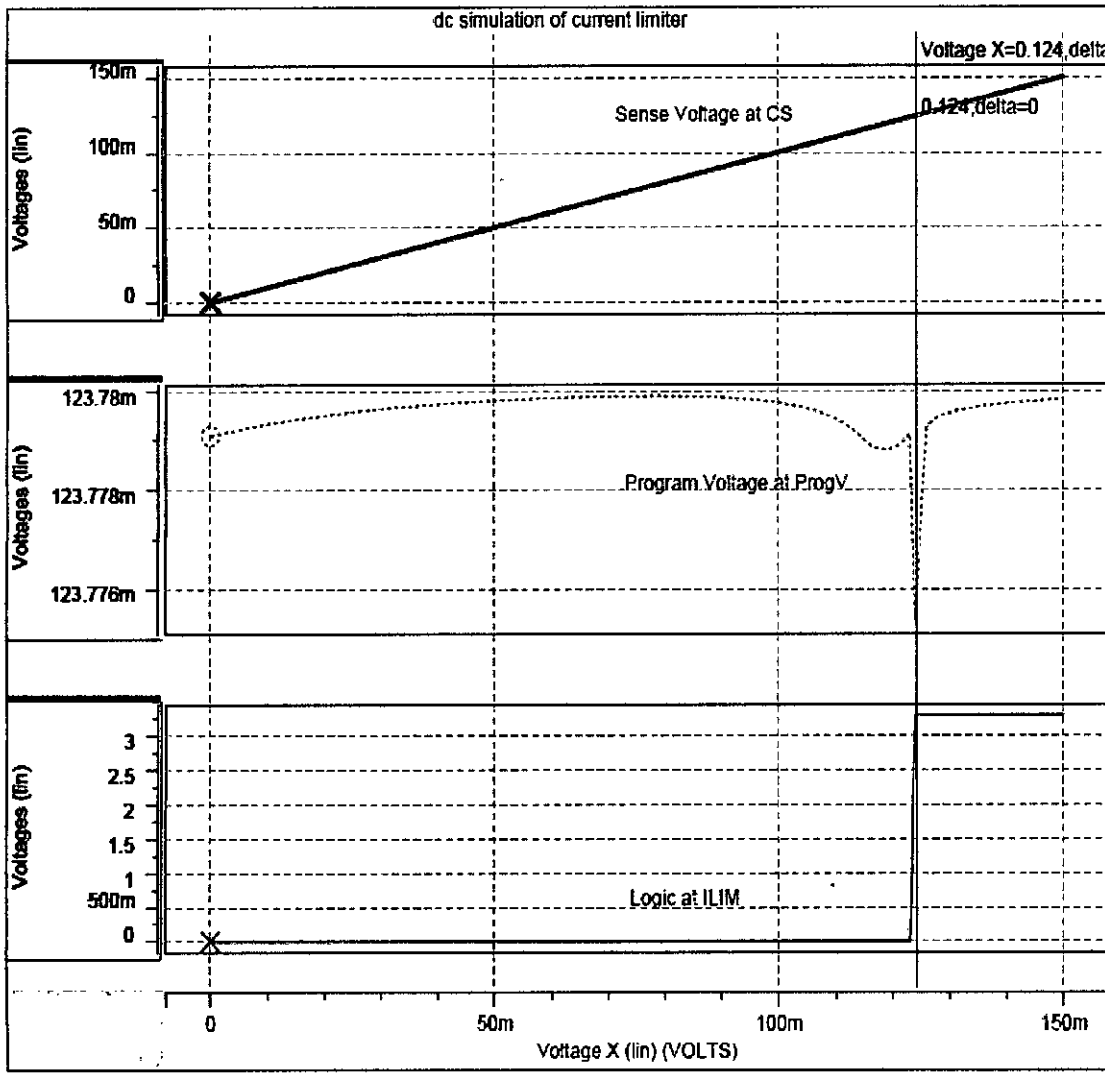

Fig 4.22: *The DC simulation of the current limiter of the converter*

The block level DC simulation result of the current limiter block has been shown in Fig 4.22. The sense voltage at CS is proportionate to the inductor current during the charge phase. Hence, the voltage at CS has been swept, maintaining all the conditions of the charge phase, for the simulation purpose. It is seen that as soon as the sense voltage at CS, reaches the program voltage level, the ILIM signal trips.

b. The Zero Current Comparator:

This chip has the provision to operate efficiently in the light load condition. When the output load of the converter becomes so low that the charge of the inductor is not fully replenished during the boost phase, the inductor needs to reverse the current flowing through it during that phase to conserve the volt-second across it. This reversal of the inductor current polarity causes back charge to the source and hence it affects the efficiency of the chip. Hence, to improve the efficiency, this back-charging needs to be stopped. The Zero Current Comparator senses the current through the P-switch during the boost phase and shuts the switch when the current through it tends to reverse its polarity. However, an offset has been added to this block (Fig 4.23), so that the comparator trips before the current through the P-switch goes to the zero. This offset has been added to account for the response delay of the comparator, i.e. it is provided so that the inductor current does not reverse its polarity by the time the comparator responds.

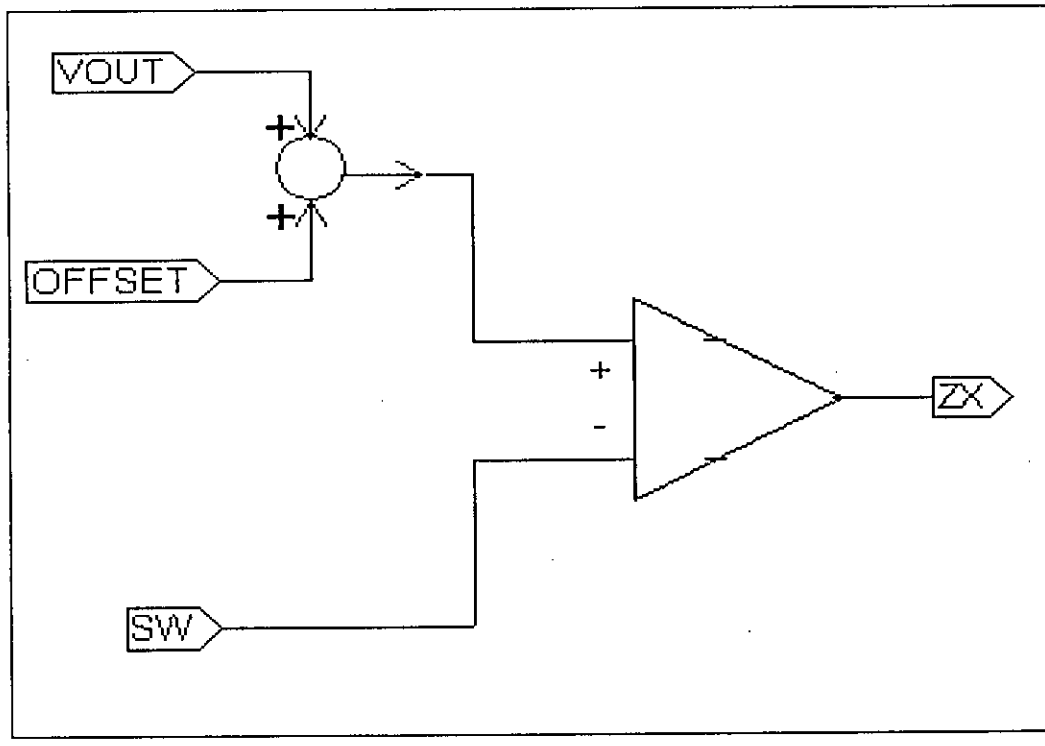

Fig 4.23: *The light load protection scheme of the converter*

As shown in Fig 4.24, the Zero Current Comparator consists of a differential pair with input devices at the common gate configuration. The offset has been provided in the required polarity with a MOS operating in the linear region. In

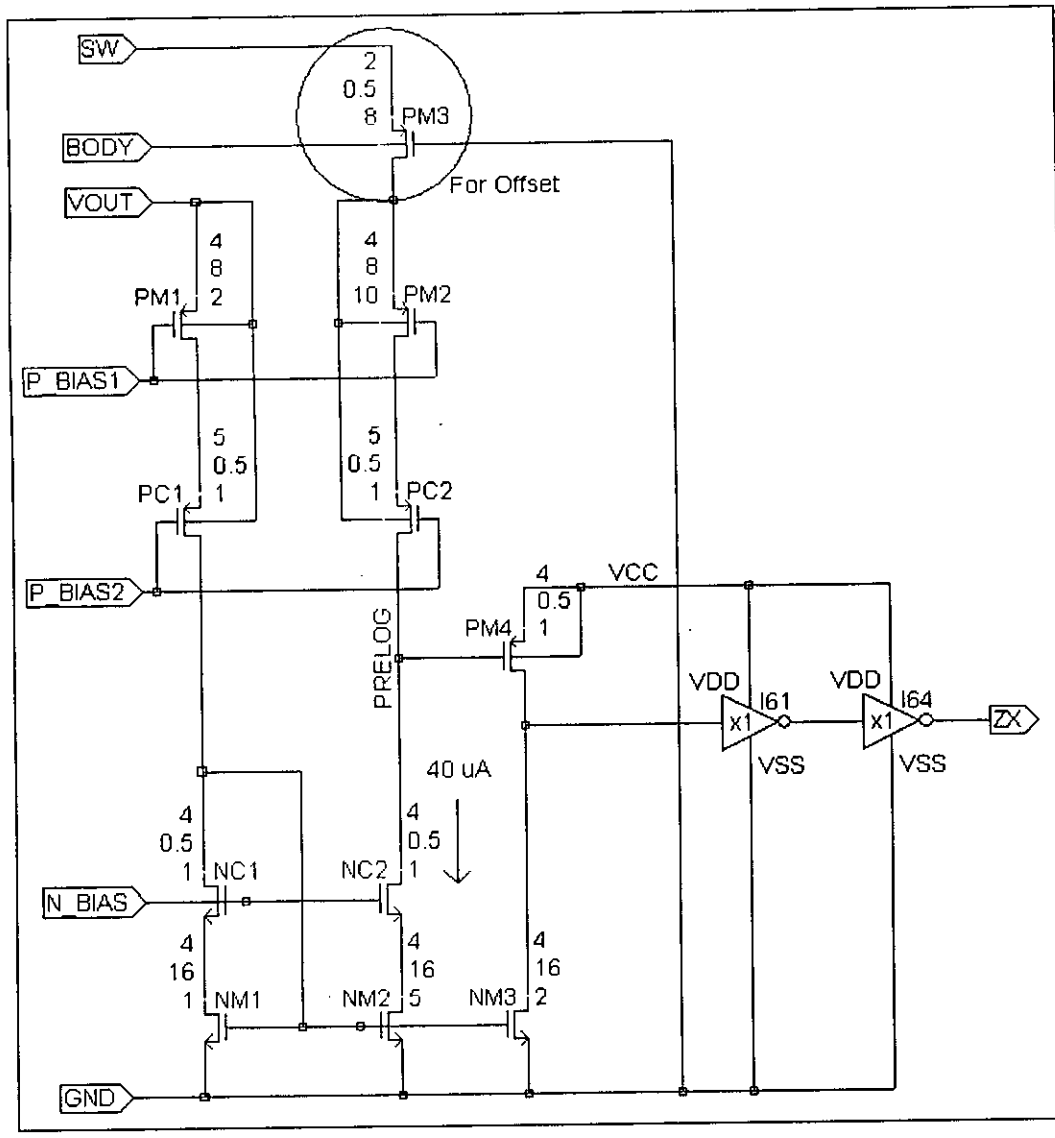

Fig 4.24: *Implementation of the light load protection scheme of the converter.*

the normal operating condition the voltage at the SW pin remains high enough than that at the VOUT pin, in the boost phase. But when the regulator runs in the light load condition, the voltage at the SW pin tends to be lower than that at the VOUT pin. Now the offset has been added in such an amount that in the normal operation, during the boost phase, $[V(SW)_{min}$ +offset] > V(VOUT). During the light load condition, when [V(SW) + offset] tries to be lower than V(VOUT), the node 'PRELOG' trips. However, by the time the comparator responds finally, the signal ZX transmits to the control block and the transmitted signal is processed to turn OFF the PSW, the voltage at the SW pin rolls down to a much lower level. But it is guaranteed for all the

possible voltage and temperature levels that the PSW is turned off at V(SW) > V(VOUT).

For 3.3V source-gate voltage of the MOS PM3 and taking K_p= 20×10^{-6} and V_{th}=0.8V, we have

$$R_{ds-on} = \frac{1}{\beta(V_{sg} - V_{th})}$$
$$= \frac{1}{20\times10^{-6}\times32\times(3.3-0.8)}$$
$$= 625\Omega$$
$$\therefore offset = (625\times40\times10^{-6})$$
$$= 25mV.$$

If the ON resistance of the PSW during the boost phase is 0.5Ω, neglecting the response delay of the comparator, the light load protection scheme will function when the current through the PSW during the boost phase falls down to *50ma*. However, this threshold of the light load protection scheme will change with the supply, as the response delay of the comparator depends greatly on that.

c. The Thermal Sensor:

The thermal sensor helps to limit the total power dissipation in the chip. When the junction temperature exceeds a certain limit, the thermal sensor generates logic to turn OFF the chip. The chip is again turned ON, when the temperature drops by a certain amount. The thermal sensor has been implemented using an NPN transistor, considering the dependence of the base-emitter voltage relationship with temperature.

As illustrated in Fig 4.25, the NPN transistor Q1 plays the main role in implementing the thermal sensor. In normal temperature Q1 is so biased that, it remains OFF. As the temperature within the chip started rising, the base-emitter voltage of Q1 falls gradually, as the base-emitter voltage has negative temperature dependence. At one point, when the temperature exceeds a certain limit, Q1 turns ON, for the given bias condition at 'BIAS_2', resulting in generation of the logic 'FAULT', which turns the chip OFF through the main control block. The simulation result of the thermal fault condition has been illustrated in Fig 4.26.

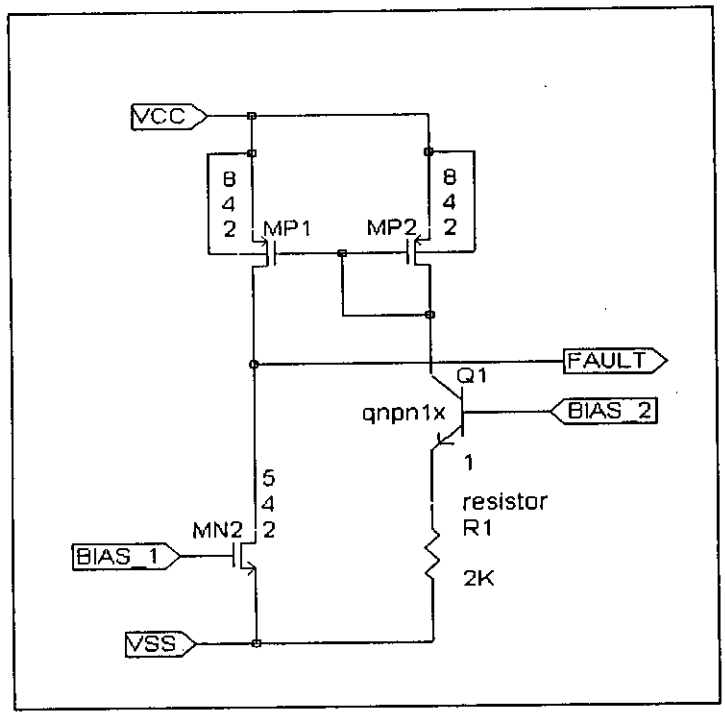

Fig 4.25: *Implementation of thermal sensor of the converter*

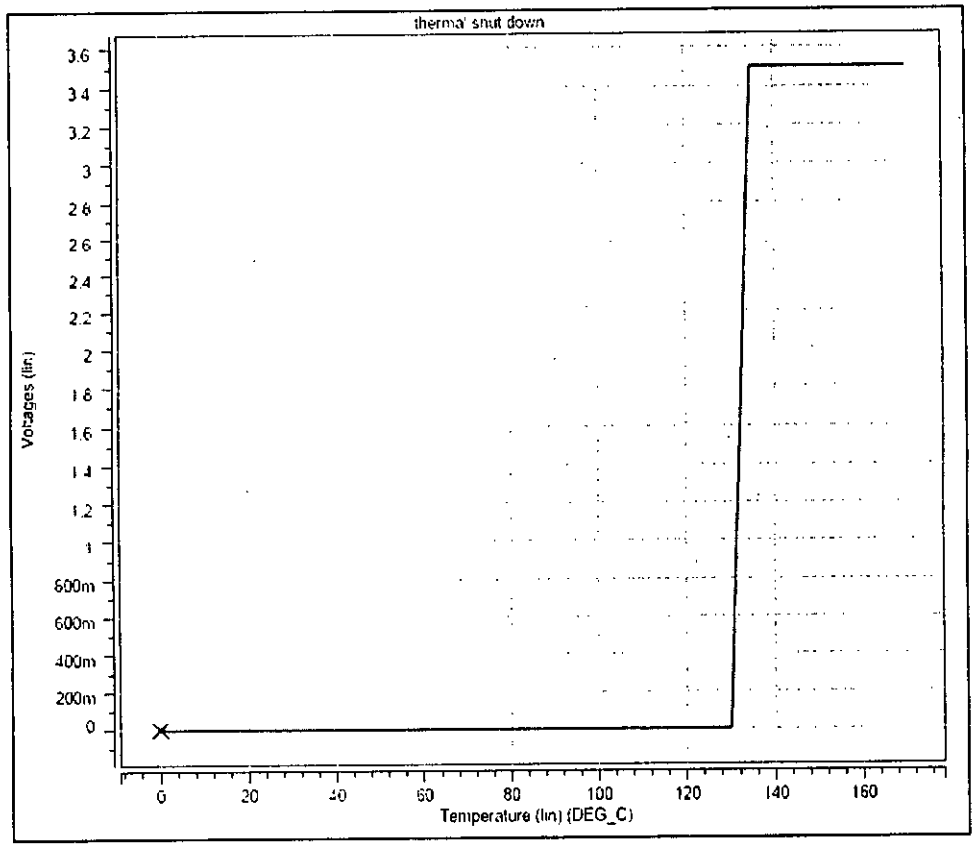

Fig 4.26: *The simulation result of the thermal fault condition of the converter.*

d. Switch Drivers with the Provision for Commutation:

The huge switches need enough gate drive to have efficient and fast switching. If devices of the minimum geometry want to drive a huge gate, the capacitance at the gate will affect the response time of it severely, as the transient drive to that gate will not be sufficient to charge that. Hence drive to a large gate has to be provided in stages, where devices of each of the stages are of higher geometry than the stages driving them. So, if the devices of a stage is 2X larger than those of the stage driving it, the inter-stage delay will be smaller than for the configuration where devices of a stage are of higher multiple (say 3X or 4X) than its pre-driving stage. But in the later case, the number of stages will be less than that in the former, which may result in less amount of overall response delay from the input node to the output node, though inter-stage delay in this respect is higher. Hence, an optimization, regarding the multiple of devices of the successive stages and the number of the stages are required to find out in order to minimize the overall response delay. Again, increasing the number of stages will increase the switching loss which will affect the efficiency of the chip. So, the optimized number of stages may not yield the required optimization regarding the efficiency of the converter. So, two-dimensional optimization is needed here. It is calculated that in order to minimize the response delay, the multiple of the successive stages should be set to 5, but in order to minimize the switching loss, the number of the stages has to be reduced and it is set that if multiple is set to 10, both the purposes are served. Besides, it has been guaranteed that both switches are not turned ON simultaneously, rather the switches are operated in the 'break then make' manner, i.e. before turning ON a switch, it is made sure that the other switch has been turned OFF. This prevents a huge inrush of current from the output node to the ground through the two switches.

As shown in Fig 4.27, skewed inverters have been used as pre-drivers of both the NSW and PSW. The skewed drivers are in a direction such that, in both the cases, the switches will need more time to turn ON than to turn OFF. Moreover, the skewed inverters in the feedback paths are so arranged that the command signals of turning OFF gates are passed slowly to the input of the pre-drivers of the complementary switches. This phenomenon ensures the total turn OFF of a gate before the turning ON of the complementary gate and thus makes the principle 'Break then make' for the switches, effective. The devices of the stages 'INV2' and 'INV4' are 10 times larger than those in the stages 'INV1' and 'INV3' respectively.

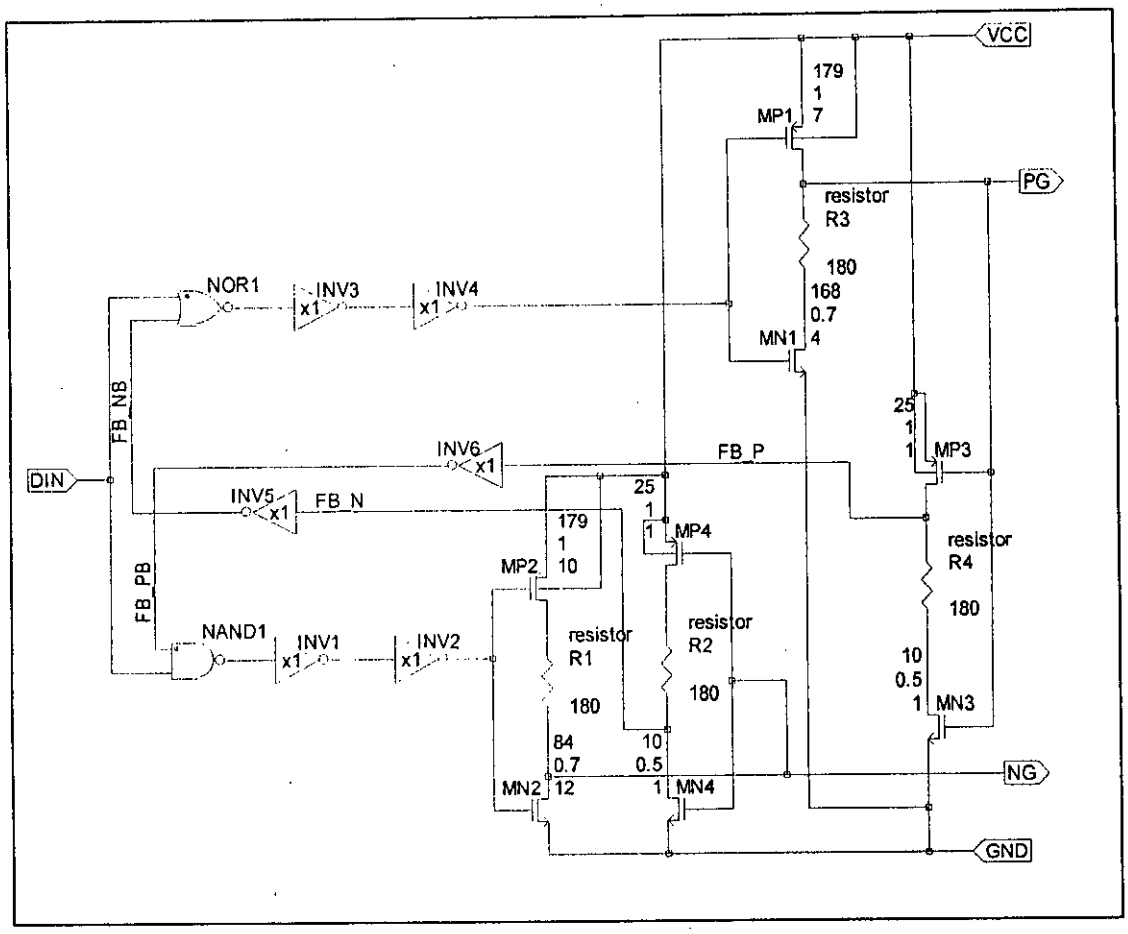

Fig 4.27: *Implementation of the switch drivers of the* converter.

Let the above statements be clarified more explicitly. When DIN is 'HIGH' the pre-driver stages wait for the feedback signal 'FB_PB' to be 'HIGH' from the 'PG' node to turn ON the NSW through the node 'NG'. When it gets that feedback signal, i.e. FB_PB is 'HIGH', the skewed pre-driver stage comprising of MP2 and MN2 turns ON the 'NG' node slowly. Again, when DIN goes 'LOW', the skewed pre-driver stage turns OFF the node 'NG' fast. The huge gate connected at 'NG' will need some time to turn OFF completely. To account for this delay, the signal at 'NG' at that time is transmitted slowly via feedback path to the PSW and this is accomplished by the skewed inverter comprising of MP4 and MN4. When 'NG' is LOW MP4 will pull up the node 'FB_N' slowly as the strength at that direction has been reduced by skewing the inverter with the resistor 'R2'. The same mechanism has been employed for driving the PSW. The simulation result has been illustrated in Fig 4.28. Moreover an example for driving a large NMOS gate by pre-driving stages of multiple 10 has been shown in Fig 4.29. The PMOS devices have been adjusted to have 2.5X higher geometry than that of NMOS devices for symmetry.

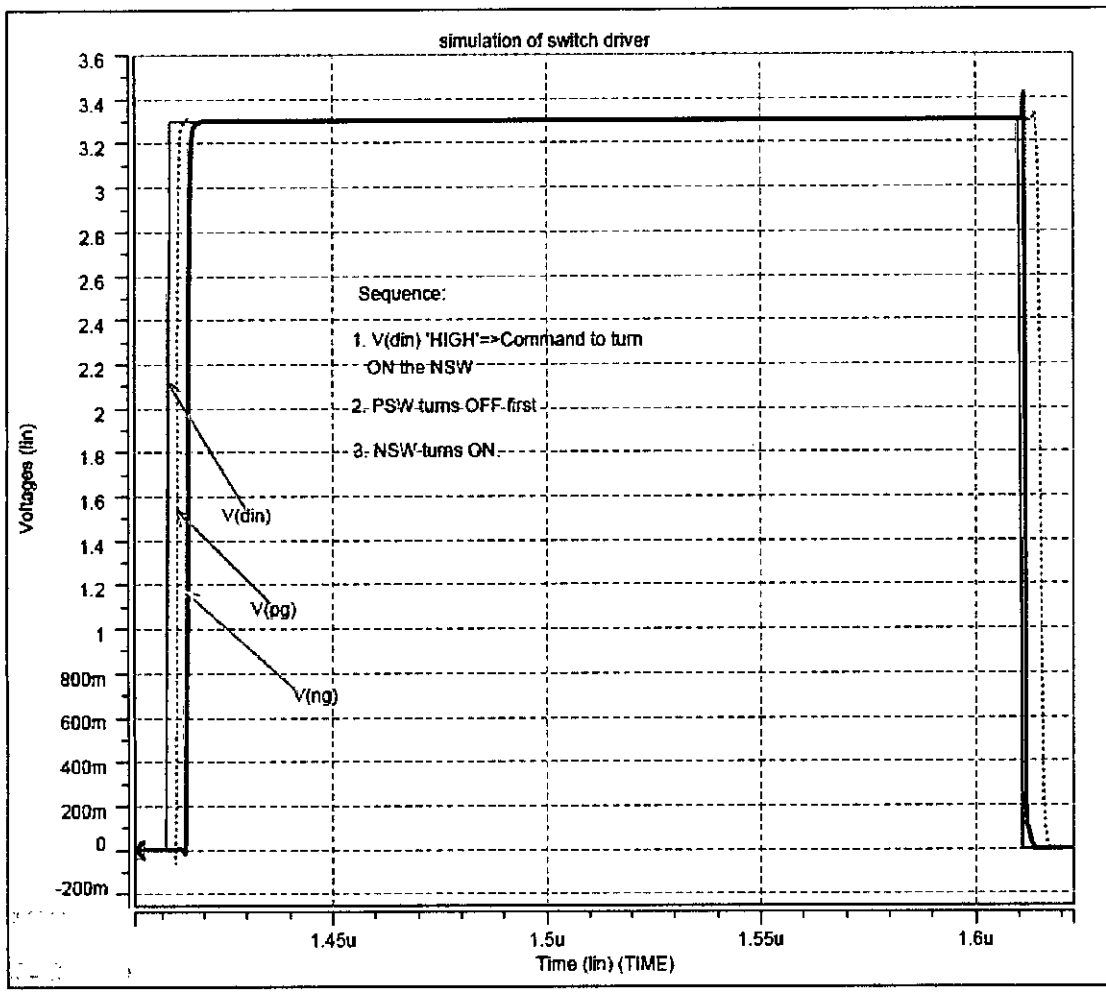

Fig 4.28: *The commutation of the switch driver of the converter*

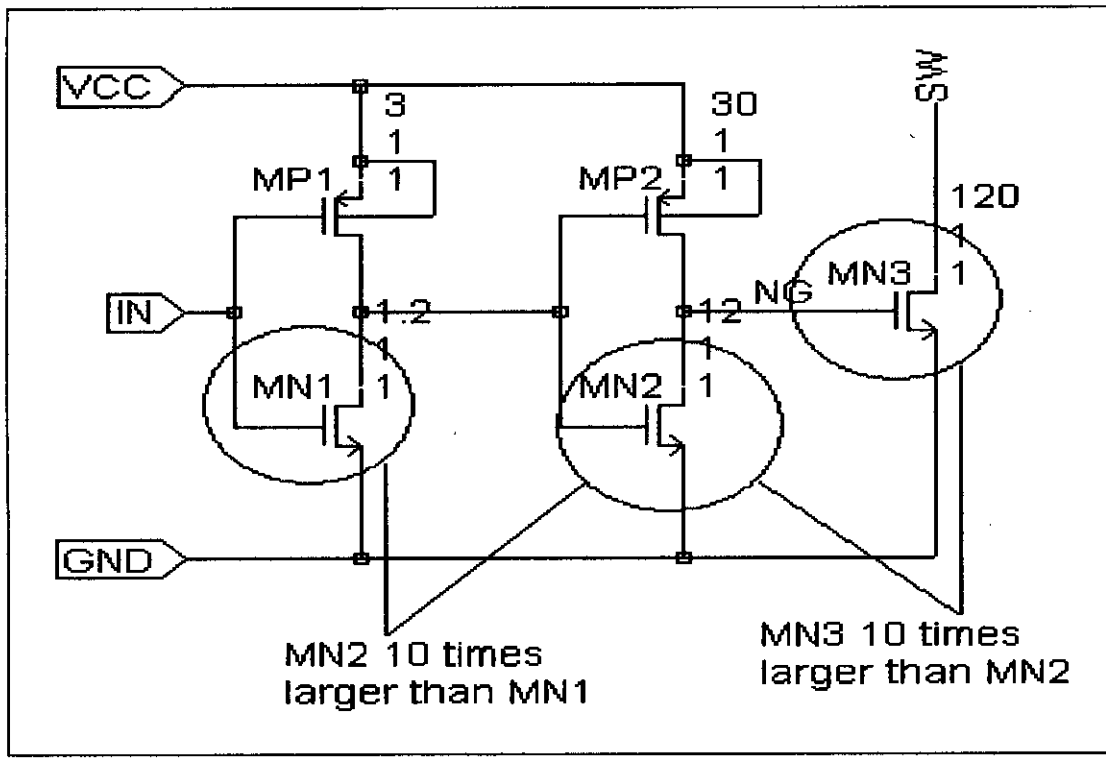

Fig 4.29: *Example of the way of staging of the driver of the switch of the converter.*

4.5 Start-up blocks:

There are some blocks and sub-blocks that enable the regulator to start its operation when it is powered up. These blocks are:

a. Oscillator:

The operation of the converter is initiated by an oscillator that is a one sort of ring-oscillator type. Fig 4.30 illustrates its functional structure. It runs at 66% duty cycle and this duty cycle is intended to guarantee the output voltage to be raised above a certain level (in this case, the level of voltage at which the reference comes out of the Under Voltage Lock-out state, i.e. 2.1V)

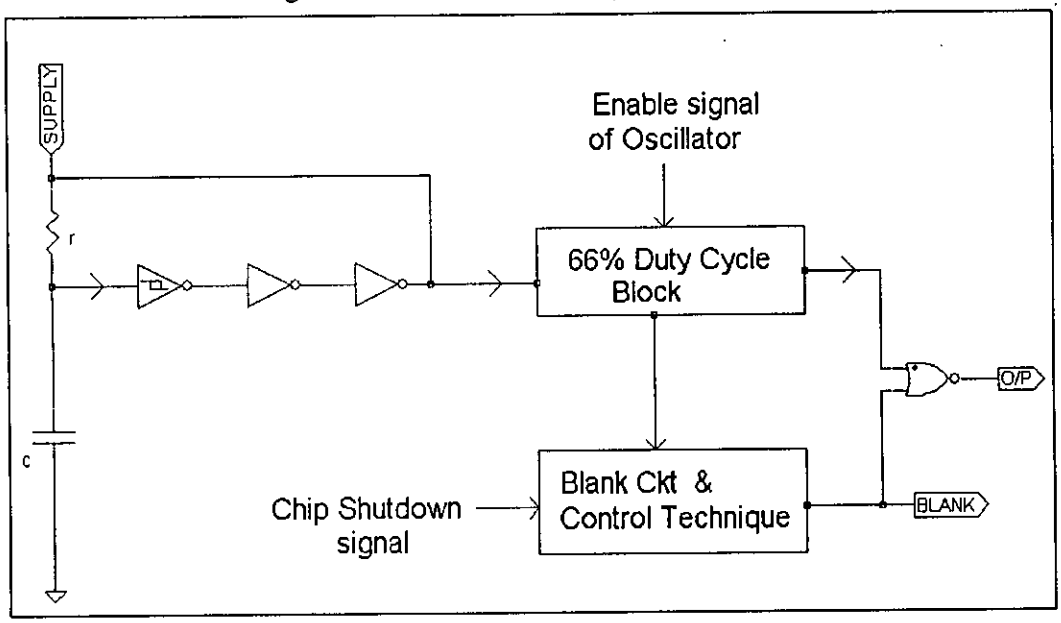

Fig 4.30: *The basic functional structure of the oscillator used in the converter*

from the minimum input voltage (typically 0.8V), satisfying all the process conditions and temperature levels. The bi-stable condition of the oscillator is set by an RC network, Schmitt-trigger and inverters and 66% duty cycle is set by D flip-flops. This oscillator is kept in the blank state, for a certain time, when the chip is powered up so that in the charging cycle the inductor peak current does not reach a destructive limit but the current limit block is not ready due to the response delay.

b. Block with the Start-up Logic:

The fixed frequency oscillator with 66% duty cycle plays the main role during the start-up condition. The logic block for the start-up condition is, therefore, simple. Only three conditions are watched during the start-up mode and these are:

a).whether current-limit is reached during the 66% ON time,

b).whether the output voltage exceeds the input voltage, and

c). whether the reference is ready.

If current limit is reached during the ON time, it is terminated. When the output voltage exceeds the input voltage, the supply to the whole chip is switched from the input bus to the output bus and when the reference is also ready, the start-up oscillator is stopped and the normal PWM operation is initiated.

4.6 The Main Control Block:

This block consists of logic gates and latches, and it integrates and manages all the digital signals generated from the analog blocks in a sequential and proper manner. The operation of this block has been summarized in the table below:

Case	Conditions	Actions
A	1. 'EN' => 'HIGH'=> (chip turns ON) 2. $V_{in}>V_{out}$ or $V_{out}=0$.	1. All the blocks of the converter turn ON. 2. Signal from the error-amplifier is blanked. 3. The supply of all the blocks=V_{in}. 4. The substrate of the PMOS switch gets connected to V_{in}. 5. The start-up fixed frequency oscillator (D=66%) starts running, with an initial blanking.
B	1. 'EN'=>'HIGH' 2. $V_{in}>V_{out}$. 3. UVLOB=> 'HIGH' (supply≥2.1).	1. The chip still runs at fixed frequency. 2. The supply of all the blocks=V_{in}.
C	1. All the conditions in B are TRUE.	1. Actions of B sustain. 2. The charge phase is terminated when

	2. ILIM=> HIGH (current limit is reached).	ILIM=> HIGH and the boost phase is initiated (D<66% for that cycle).
D	1. Conditions 1 & 3 of B =>TRUE. 2. $V_{in}<V_{out}$. 3. $V_{out}\leq V_{out\text{-}regn}$	1. The start-up oscillator stops running. 2. The blanking of the signal from the error-amplifier is removed. 3. The converter runs at maximum %D (at minimum T_{off}). 4. As 'ILIM' is reached while running at maximum %D, ON time terminates for that cycle. 5. The supply of all the blocks=V_{out}. 6. When the V_{out} reaches the regulation point, PWM operation is initiated.
E	1. ILOAD low, V(SW)≈0 during the boost phase.	2. PMOS switch is turned OFF. 3. The next charge phase is initiated when V_{out} falls below the regulation point.
F.	1. The output voltage is set in such a way that $V_{out\text{-}regn}<V_{in}$, =>set for abnormal boost converter operation.	1. The converter will run freely by the start-up oscillator. 2. V_{out} will grow and at one point it will exceed V_{in} and oscillator will be stopped. 3. But $V_{out}>V_{out\text{-}regn}$, so error-amplifier will not initiate a charge phase. 4. The V_{out} will decrease and when it will again fall below V_{in}, the oscillator will be enabled and V_{out} will grow again.

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G.	1. B, C or D is TRUE. 2. The temp of the chip or surrounding >150°C	1. The chip will shut and output will discharge to zero.

Chapter 5

Simulation and Results

5.1 Necessary Files and Tools:

The proposed chip is a synchronous step-up regulator. It can operate from a single cell battery (0.8V) and can supply 100 mA loads at the output voltage of even 5 Volts. Before going into the description of the functional stages, we need to be acquainted with the software tools for netlist generation, simulation and probing.

Purpose	Tools
Schematic Drawing & Netlist Generation	Cohesion Designer 5.11.
Simulation	Avanti Hspice 2001.4.
Probing	Avanwaves.

In order to do simulation by Avanti Hspice 2001.4, some files are needed and these are:

a). Netlist File:

It is the file having the description of all the devices and net connectivity of a circuit. It can be generated manually, but for a very large schematic, where numbers of hierarchies are present, this process is cumbersome. Hence, a tool like Cohesion Designer 5.11 has been used for the generation of netlist. The netlist file that the spice uses should be in *.spi* extension.

b). Stimulus File:

This file contains all the commands for bias, type of analyses (e.g. transient or dc or ac analysis), different tolerance limit (reltol, abstol etc.). Moreover, the netlist file and the file containing model libraries etc. are also called in this file. This file is directly executed in spice. Its extension is *.sp*.

c). Model Library:

A .txt file containing model libraries is also needed. That file contains different model parameters of devices like MOS (e.g. level 49 parameters), bipolar (e.g. level 1 parameters), and resistors, capacitors (e.g. sheet value, temperature coefficient, voltage coefficient) along with the skew parameters for different type of processes like typical, slow and fast processes.

The converter has different operational stages. In this chapter, a brief note of those stages has been illustrated through simulation.

5.2 The Start-up Mode:

The converter can start up typically at 0.8V i.e. from a single cell battery. When it is turned-on, it gets its start up bias from V_{in}. A start-up oscillator, which runs typically at 650 KHz, brings the output voltage high enough so that V_{out} exceeds V_{in}. Once V_{out} exceeds V_{in}, internal bias switches from Vin to V_{out} by an internal bias-select circuit. As shown in Fig 5.1, the converter started at V_{in}=1.5V and V_{out} was building by the start-up oscillator operating at 66% duty cycle. At that time the voltage level of the oscillator wave was equal to the input voltage i.e. =1.5V. When V_{out} exceeded V_{in}, the amplitude of the oscillator was seen changing gradually, which indicates that the internal bias select circuit was then taking the bias from V_{out}. Thus, once started (i.e. V_{out} exceeds V_{in}), internal circuit bias is completely independent of V_{in}. The start-up oscillator runs at 66% duty cycle around 650 KHz.

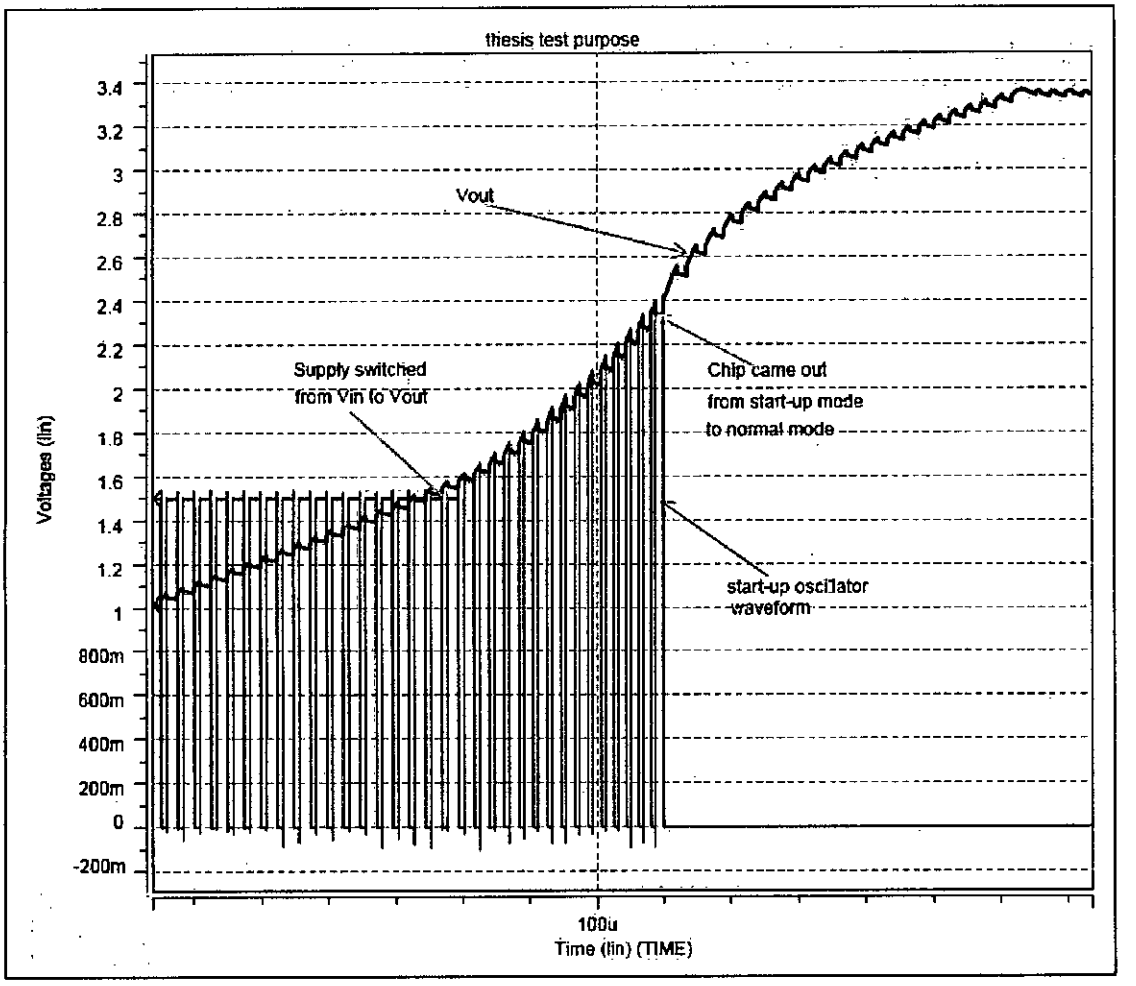

Fig 5.1: *The start-up mode of the converter*

Again when V_{out} exceeded V_{in} and the under voltage lock out threshold (typically 2.15V) of the REFERENCE block, the start-up oscillator is disabled and the normal fixed Ton PWM operation takes over. Before the loop comes to its normal operating mode from the start-up mode, the chip runs at the maximum duty cycle (set up by the minimum T_{off}) and the inductor current builds up continuously until it reaches its current limit (Fig 5.2). The higher the current limit of the chip is set, the lower will be its start-up time. Moreover, during the start-up phase, the output voltage is built up during the minimum off time set forcefully. This minimum off time also settles the start-up load of the converter, the higher the minimum off time, higher will be the start-up load but at the expense of the maximum attainable duty cycle, of course.

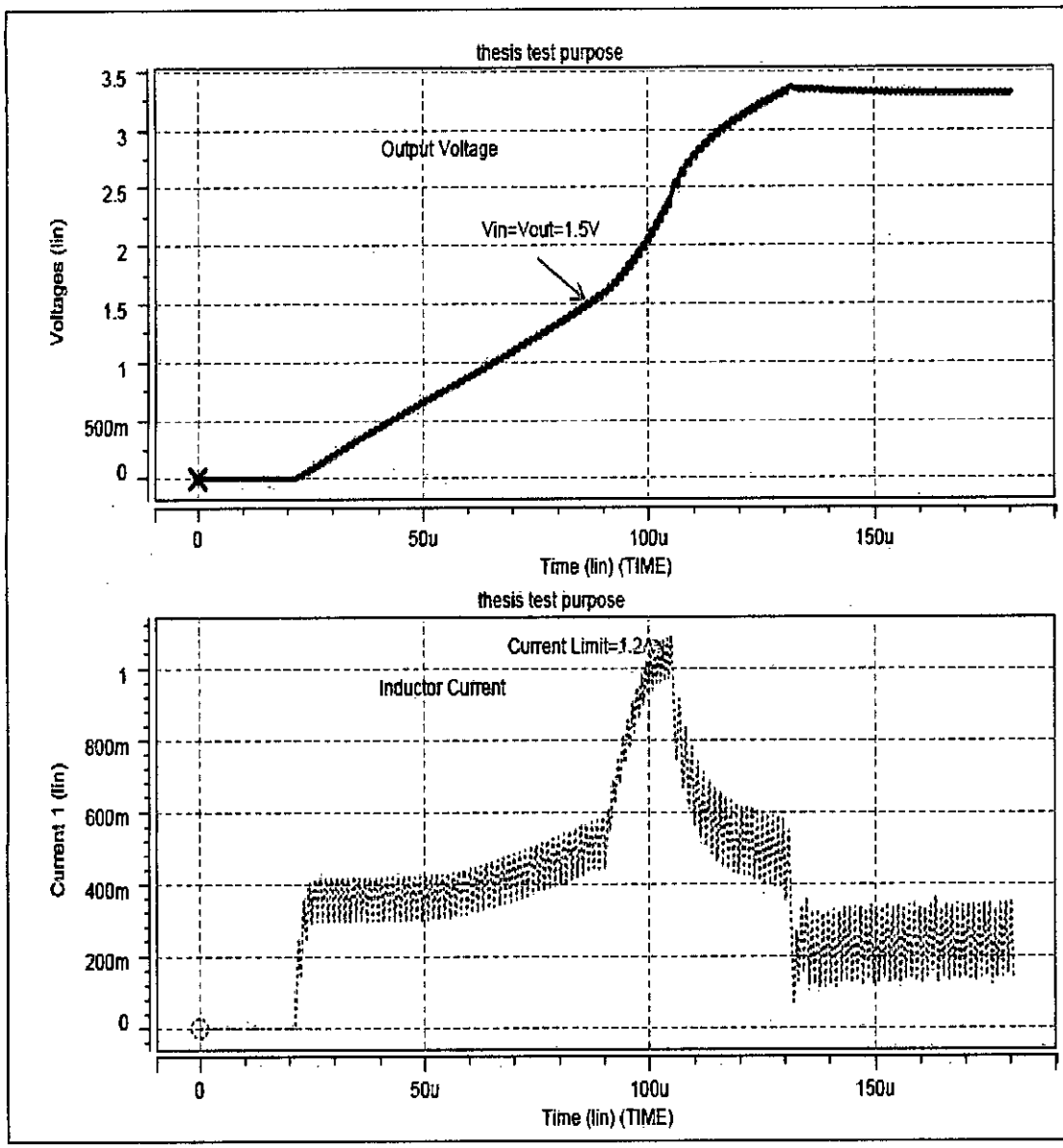

Fig 5.2: *Transition from the start-up mode to the regular mode of the converter.*

5.3 The Normal Operating Mode:

This converter employs OFF time modulation technique, where in each cycle, the charge phase is initiated by the error-amplifier. A steady state simulation result for V_{in}=1.5 and V_{out}=3.3 (D=55%), has been illustrated in Fig 5.3.

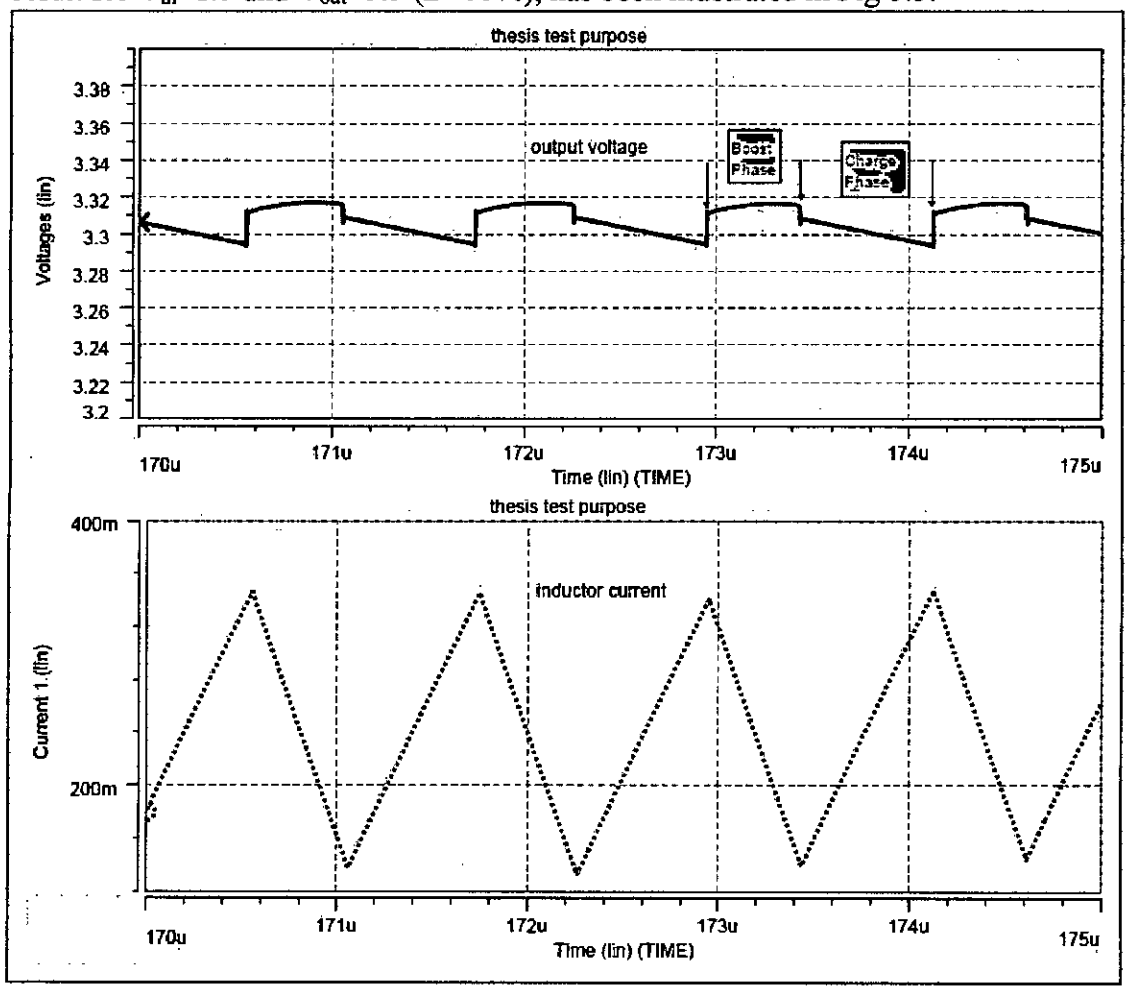

Fig 5.3: *Normal PWM operation for 55% duty cycle of the converter.*

The converter has settled for a fixed frequency in the steady state condition. The initial step jump in the output voltage, as shown in Fig 5.3, during the boost phase, is because of the potential drop at the Equivalent Series Resistance (ESR) of the output capacitor. A 50 $m\Omega$ ESR has been included in the simulation to replicate the real phenomenon.

5.4 Current Limit and Short Circuit Protection:

The chip includes a current limiter that monitors the peak inductor current through the NMOS switch NSW and turns the switch off when the inductor peak current exceeds the programmed current limit, 1.2A. Because of its true

shutdown feature, the IC is allowed to be short-circuited. The thermal shutdown turns off the regulator in case of excessive heating, when the die temperature reaches 145°C

5.5 The Light Load Operation:

In order to have improved light load efficiency, light load management scheme has been introduced in the converter. The internal zero current comparator monitors the inductor current to the load and shuts off the PMOS switch once this current reduces to some low value (30mA, typically). This prevents the inductor current from reversing its polarity, avoiding back-charging and thus improving efficiency at light load.

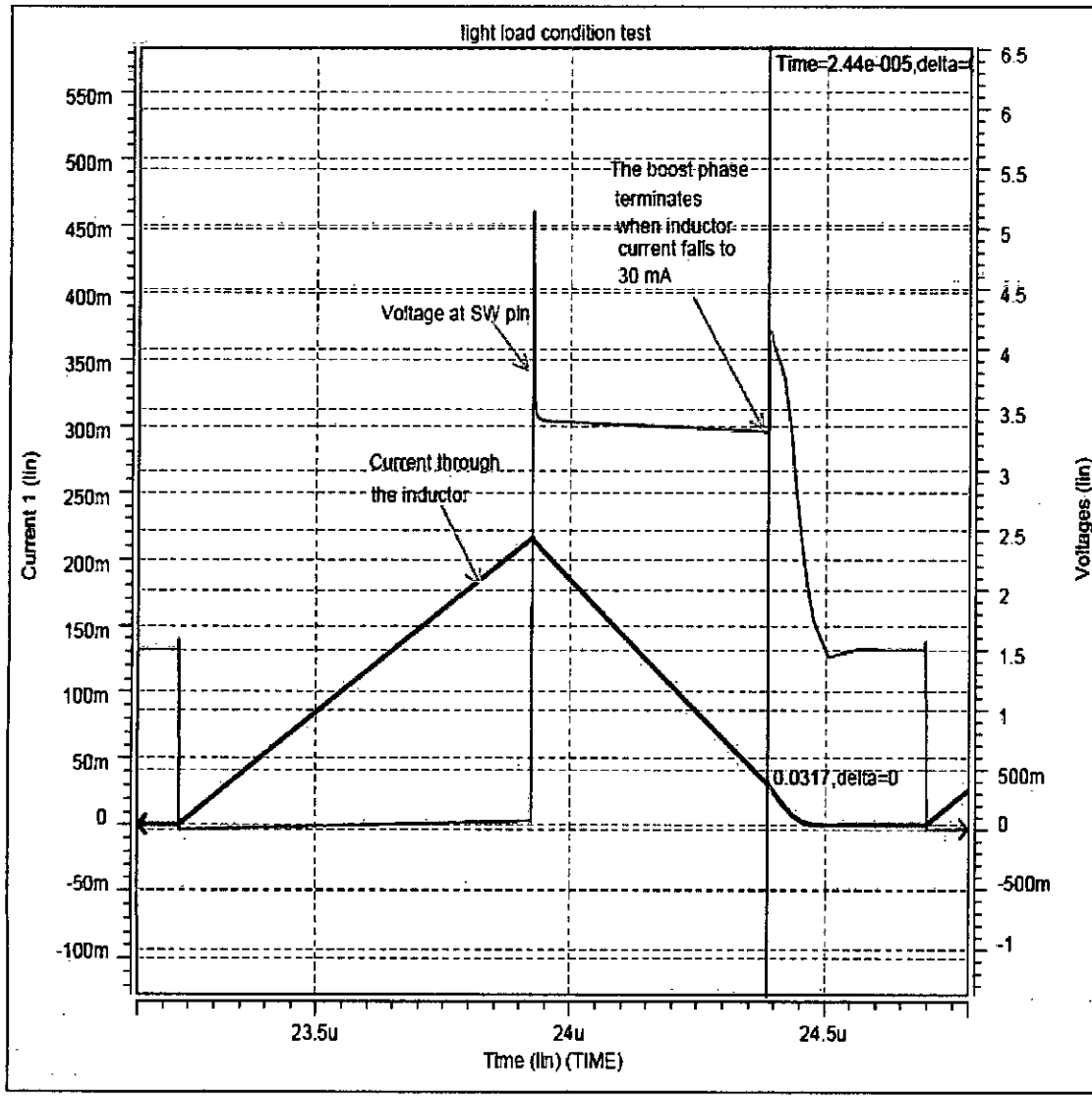

Fig 5.4: *The light load operation of the converter*

As shown in Fig 5.4, when the converter runs in the light load condition, the boost phase is terminated when the inductor current falls to a certain

low level (30mA for this converter). The SW pin is then connected to the input pin and hence voltage at the SW pin gradually discharges to the input voltage (1.5V for this purpose). During the light load condition, both the NMOS and PMOS switches remain off. However, normal operation starts again when the output voltage falls below the regulation point. The chip automatically skips pulses at light load, providing better efficiency.

5.6 Output Voltage Selection:

This chip is designed for the user adjustability of the output voltage, through an external feedback network. A voltage divider from V_{out} to *GND* (with R_1 from V_{out} to *FB* and R_2 from *FB* to *GND*) programs the output voltage via using the following equation:

$$V_{ref} = V_{out}\left(\frac{R_2}{R_1 + R_2}\right)$$

$$\Rightarrow V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$

5.7 Under Voltage Lockout Condition:

When the supply goes too low (below 2.0V typ), the chip produces an internal UVLO (under voltage lockout) signal that disables the normal PWM operation and enables the start-up oscillator to run at a fixed frequency. At that time, very few circuits are operational. When the oscillator raises the supply above 2.2V, UVLO signal is disabled and the normal PWM mode takes over the start-up oscillator operation. This mechanism protects the chip from producing false logic due to low input supply.

5.8 True Shutdown Mode:

The chip is designed to allow the true shutdown by managing the body diode of the PMOS switch. As the PMOS switch is turned off and there is no conductive path through the body of the PMOS, the output is allowed to go to zero during shutdown, drawing zero current from the input.

Chapter 6

Measured Data & Real Time Waves

6.1 Measured Data:

As mentioned earlier, the proposed converter has been fabricated with a standard BiCMOS process. The die area is about 1520 X 800 square microns. The converter was tested in the lab and was found that the performance is in good agreement with the simulated values. The following table shows the simulation and test data of various parameters of the chip:

Parameters	Test Conditions	Simulation Data	Measured Data
Start-up Frequency	V_{in}=1.5, T_A=27°C	680 KHz	710 KHz
Start-up Load	I_{load}=1mA, T_A=27°C	0.8 V	1.1V
ON time (T_{on})	V_{in}=0.8, T_A=27°C V_{fb}=0, SW OFF time is measured.	1 uS	812 nS
Min. OFF time ($T_{off\text{-}min}$)	T_A=27°C, V_{fb}=0, SW ON time is measured.	150 nS	130 nS
NSW resistance	V_{out}=3.3, T_A=27°C	0.35 Ω	0.425Ω
PSW resistance	V_{out}=3.3, T_A=27°C	0.45Ω	0.66Ω
Non-switching ground current.	V_{out}=3.3, T_A=27°C, V_{fb}=1.2, current at V_{out} is measured.	280 uA	400 uA
Reference Voltage	T_A=27°C	1 V	1.005 V
Current Limit	V_{out}=3.3, T_A=27°C	1.2 A	1.4 A
Zero-Current Threshold.	V_{out}=3.3, T_A=27°C	50 mA	45 mA
Load Regulation	V_{out}=3.3, T_A=27°C, I_{load}=0-100 mA	1.5%	1.6%

a). Start-up Load :

The amount of output load demand with which a boost converter can build up its output voltage is known as its start-up load. This mainly depends on start-up voltage (input voltage), the time provided in the system for forceful boost operation ($T_{off\text{-}min}$) and the ON resistance of the switch in the charging phase. For a fixed input voltage, the longer the $T_{off\text{-}min}$ and the smaller the switch resistance, the better will be the start-up load of the converter. Moreover, this start-up load giving

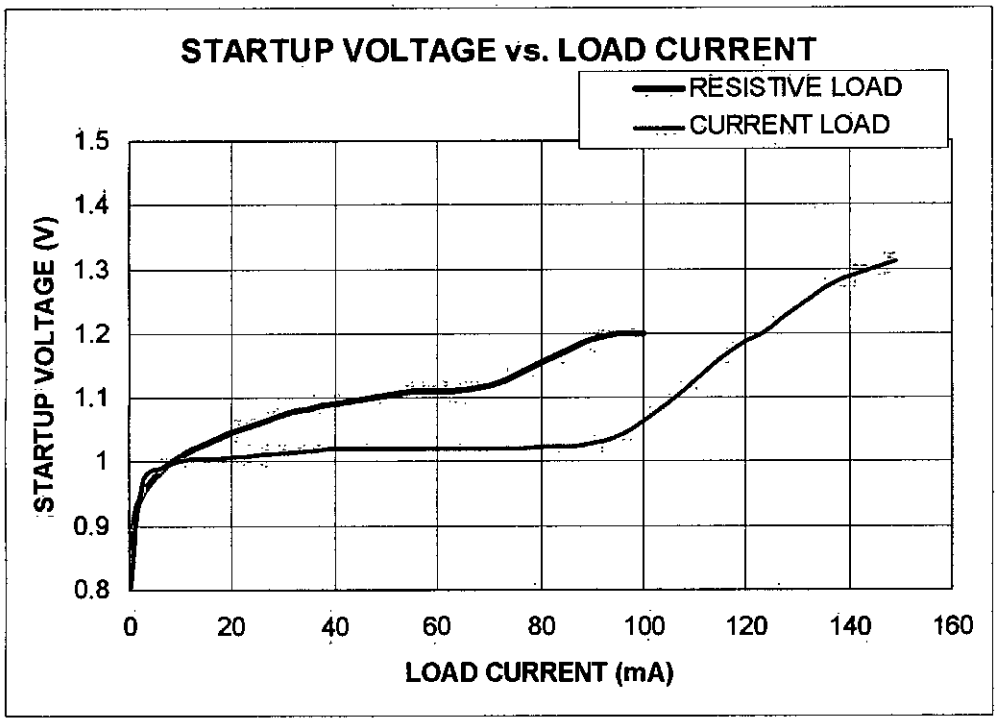

Fig 6.1: *Measured data of start-up load*

capacity increases with the start-up voltage, as with higher start-up voltage ,the ON resistance of the switch during the charge phase, will be smaller and the inductor will have higher effective volt-second across it. Fig 6.1 illustrates the relationship between the start-up load delivering capacity and start-up voltage. As it is evident, the load delivering capacity of the converter is very low until the start-up voltage is 0.9V. As the start-up voltage crosses that value, the start-up load capacity of the converter increases drastically. This is mainly due to the nature of the ON resistance of the switch, implemented by a MOS working in the resistive mode. Moreover, this load delivering capacity depends on the nature of load. Current load requires a certain voltage to demand a range of load. But, the resistive load is not like that. It demands the load based on V_{out}/R_{load}.

b). Variation of ON Time with Input Voltage:

The converter has been designed such that the charge time is inversely proportional to the input voltage. However, to prevent the ON time from becoming very long, the time generator circuit has been biased with a fixed current, which is always present in charging the capacitor. Another one is V_{in}/R based current. Fig 6.2 shows the relationship of ON time with the input voltage. When the input voltage is very low, V_{in}/R based current is insignificant compared to the fixed current, in charging the capacitor. Hence, the ON time remains fixed in the lower range of input voltage. As the input rises, V_{in}/R based current starts dominating the fixed current and then the ON time becomes inversely proportional to the input voltage. The $\frac{dt}{dv}$ slope

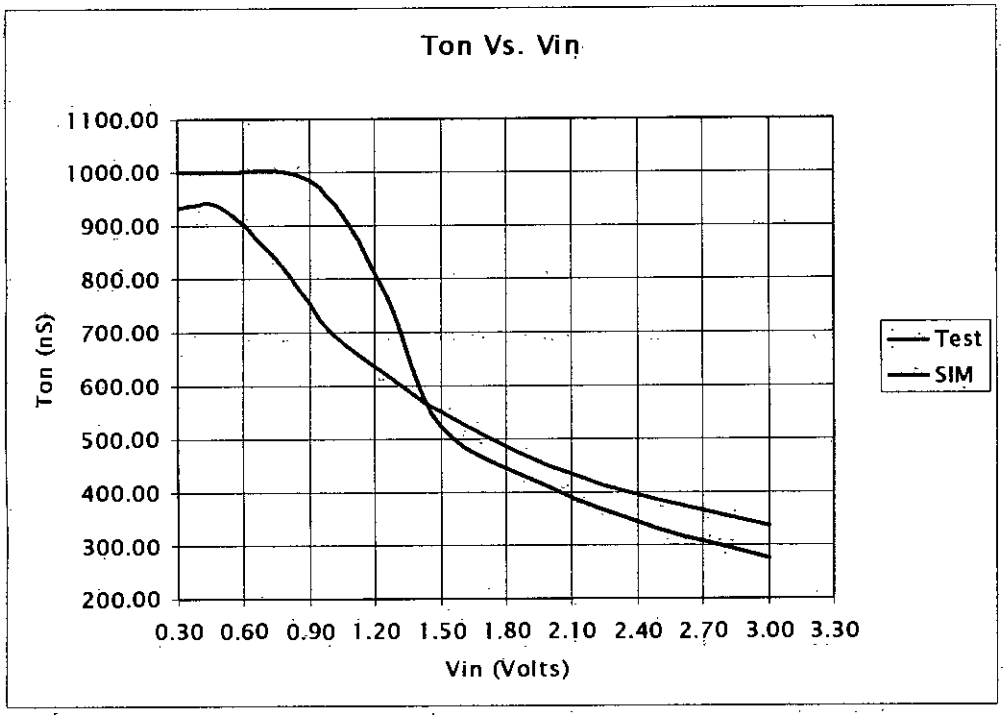

Fig 6.2: *Simulated & measured data of ON time (Ton) of the converter*

is steeper for lower range of input voltage, as it is evident from the relationship

$\frac{i}{C} = \frac{dv}{dt}$ *and* $i \alpha Vin$.

c). Single Cell Efficiency:

The efficiency of a converter for a single cell (battery) is an important performance parameter in commercial purposes. The main power loss occurs in the switch devices and the loss term consists mainly of the conduction loss (I^2R loss) and

the switching loss. The conduction loss dominates for higher load while the switching loss becomes significant in the lower load range. For a certain load, as shown in Fig 6.3, the efficiency of the converter becomes maximum (occurs at 100mA for V_{in}=1.5). That load is the optimum output load regarding the efficiency of the converter. In that load, the total loss becomes minimal.

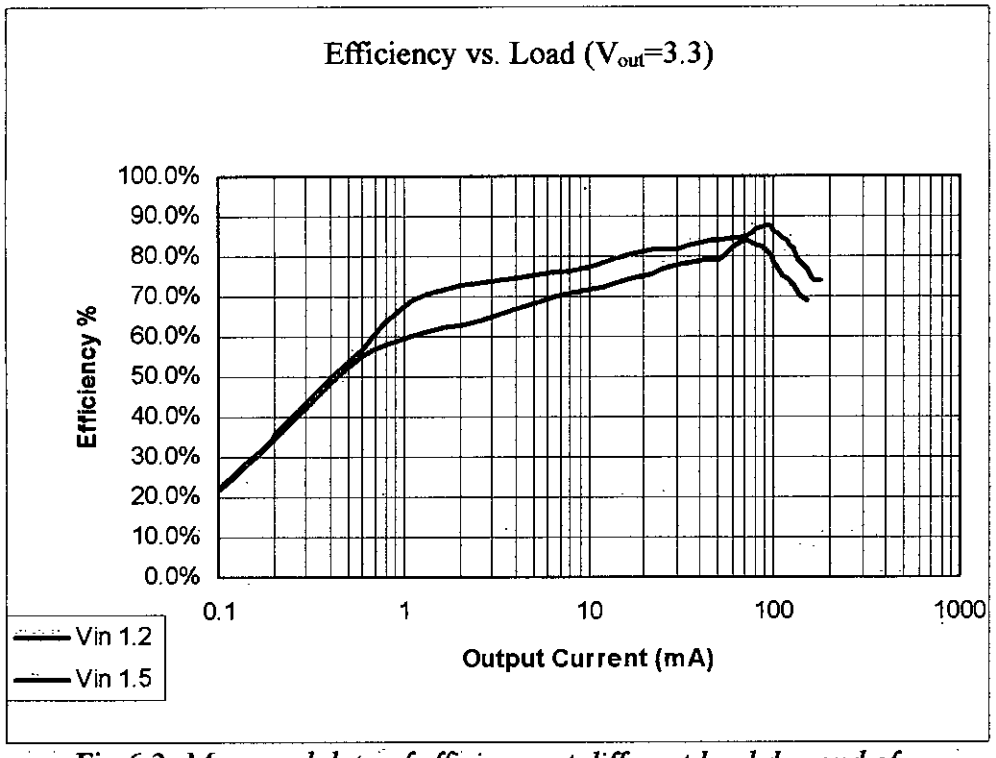

Fig 6.3: *Measured data of efficiency at different load demand of the converter.*

d). Variation of Output Voltage with Load:

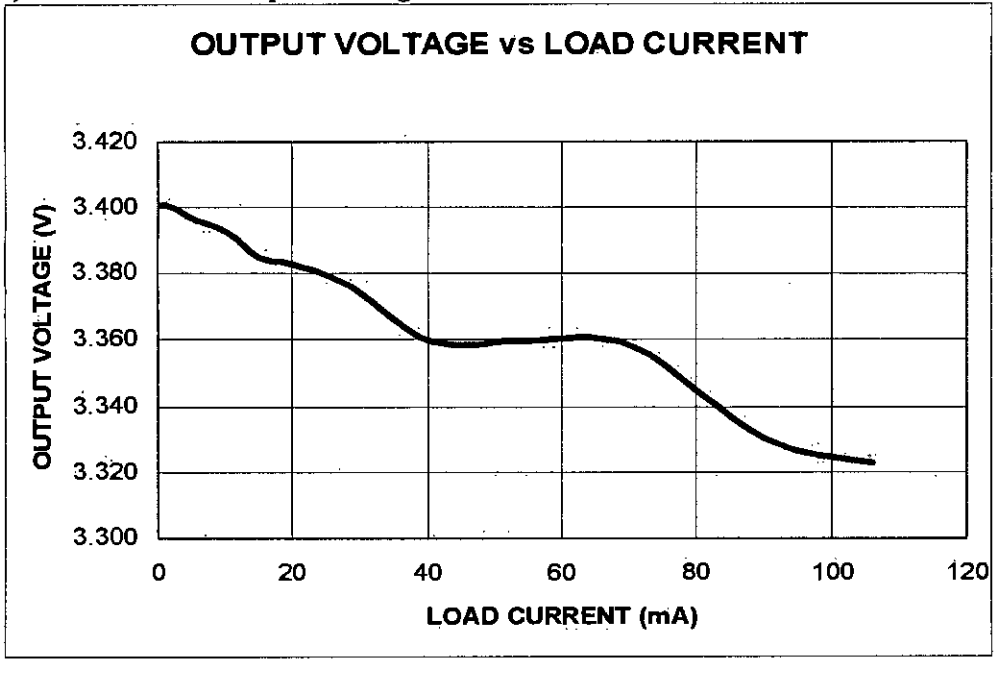

Fig 6.4: The *load regulation characteristics of the converter*

The converter has a very tight load regulation when it enters in the continuous conduction mode (40mA to 100mA range), as it is evident from Fig 6.4. Again, the change in output voltage from light load condition to continuous conduction mode is not much, it is only 20mV.

6.2 Real Time Waves:

All the waves have been recorded by digital memory oscilloscopes of model: TDS2014 and TDS3054B and a current probe of model: TCP202.

a).The Start-up of the Converter:

As mentioned earlier, the operation of the converter, when the output capacitor is at its complete discharged state, is initiated by a fixed frequency oscillator. The output builds up slowly until the condition $V_{out}=V_{in}$ is reached, as the stored charge in the inductor has to feed both the output capacitor and the load connected to the output node.

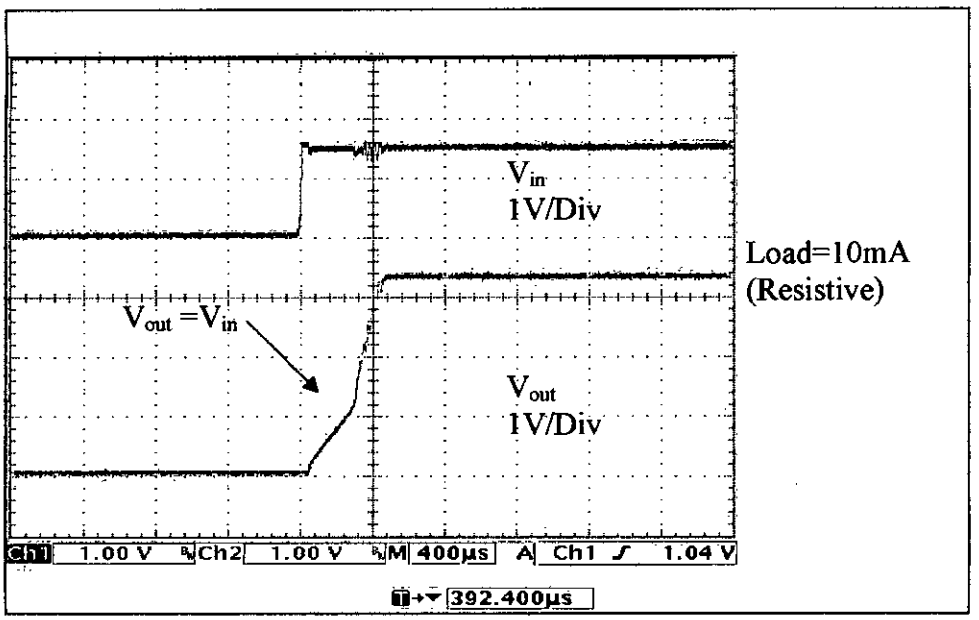

Fig 6.5: *The start-up waveform of the converter for V_{in}=1.5 & V_{out}=3.3 @ 10mA load.*

Then afterwards, output builds up rapidly and reaches the regulating point. This fact is illustrated in Fig 6.5; the voltage at the EN pin is recorded at Ch1 and the output voltage is plotted in Ch2, with a 10mA output load.

b).The Shut Cycle of the Converter:

One of the unique features of the converter is that, the output can be completely discharged to zero. The wave shapes in Fig 6.6, depict this fact. The converter has been turned ON just for the span of time, required to build output fully and then turned OFF. This cycle has been repeated at about 310 Hz and the wave shapes at EN and OUT pins have been recorded in CH2 and CH3 respectively. The

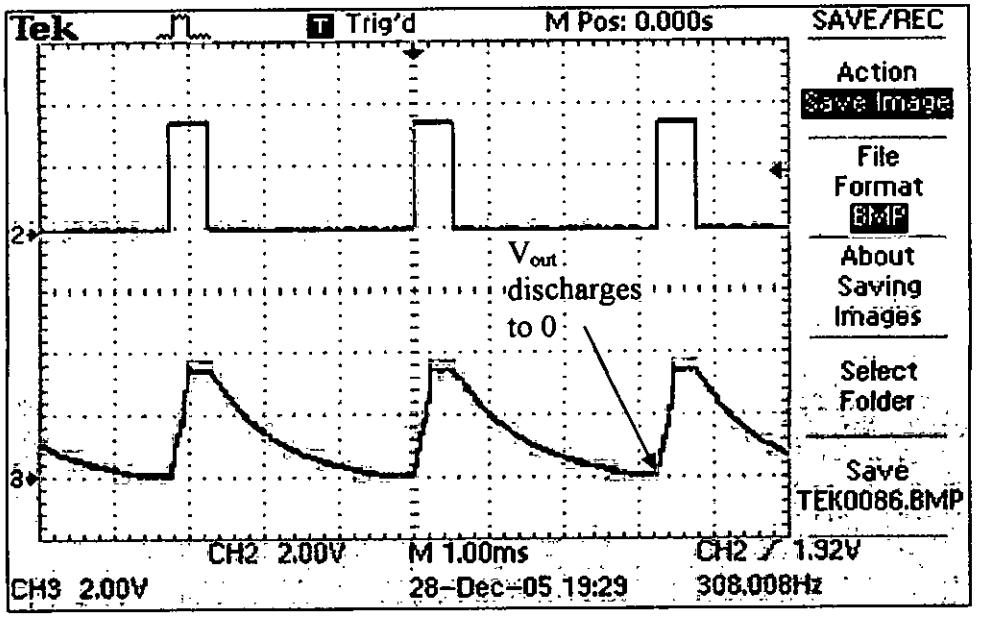

Fig 6.6: *The shut cycle of the converter*

frequency of the switching of the EN pin has been selected such that the output capacitor can discharge fully to zero before the converter is turned ON again.

c). Steady State Heavy Load Operation:

The steady state heavy load switching condition of the converter has been depicted in Fig 6.7. Signals at Ch1 and Ch2 have been AC coupled to record the ripples at the mv level of input and output voltages. Ch3 records the voltage at the SW pin and current through the inductor has been plotted by a current probe and recorded in Ch4. The chip has been set to supply a load of 100mA while boosting input voltage of 1.5V to 3.3V. Hence, the converter is running at 55% duty cycle, while supplying a load of 100mA.

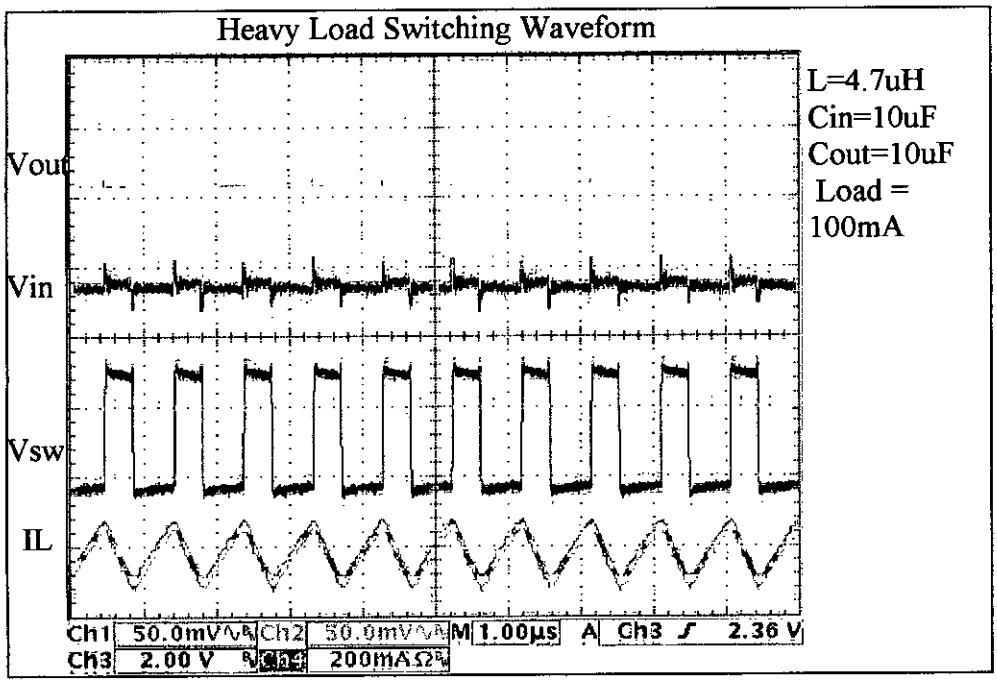

Fig 6.7: *Heavy load switching of the converter at D=55%*

d). Light Load Operation:

As mentioned earlier, the converter runs at the light load condition when the output load is very low. This fact has been illustrated in Fig 6.8. The signals have been recorded in different channels of the oscilloscope in the same manner and sequence as they have been done in the case of 'Steady State Heavy Load Condition'.

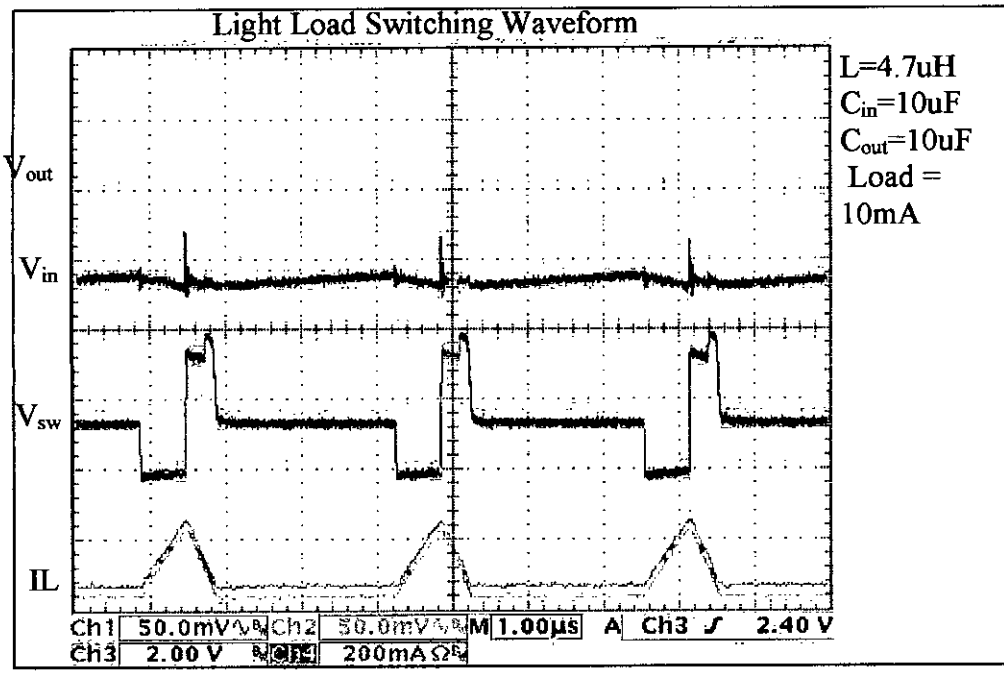

Fig 6.8: *The light load operation of the converter*

Examining the current through the inductor, we find that the converter is running in pulse skipping mode i.e. at first the inductor is charged at the upslope of the inductor current, the charge is replenished (boost phase) at the down slope of the current and then it remains at the zero level until the next charging phase is initiated

e). The Load Transient Response:

The load transient response is one of the performance measuring criteria of a loop. With a sudden abrupt change in load, the response of the converter is examined. Applying abrupt change in load is, in fact, examining the large signal phenomenon of the loop. The more stable a loop, the less the time it will take to damp down out the initial oscillation when such abrupt change in load is applied. Again,

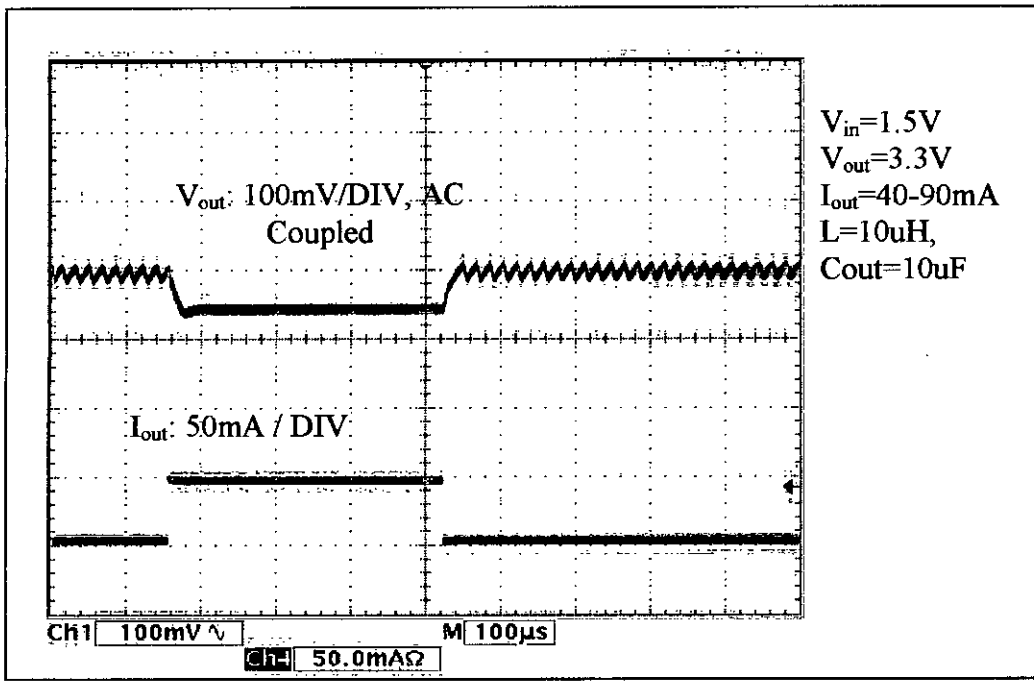

Fig 6.9: *The response of the converter output voltage for a step change in load.*

when the dc loop gain is high, the difference between the two DC levels of the output voltage (level at low load to the level at higher load) will be small. As such abrupt change is applied, the loop gets broken initially and it then settles down to another DC value by running in maximum duty cycle (i.e. in minimum T_{off}). As this minimum T_{off} is kept larger, more time will be provided to the loop to have forceful boost and it will settle quickly but at the cost of highest attainable duty cycle. The step change in output load and corresponding change in output voltage have been plotted in Ch4 and Ch1 respectively. As it is evident from Fig 6.9, for a change in load from 40mA to

90mA, only 50 mV change in output voltage occurred and output voltage settled to another DC level within 100nS, indicating a very good type of load transient response.

f). The Line Transient Response:

Another parameter to test the large signal phenomenon of the loop is to evaluate the line transient response of it. It is actually the response of the output voltage at the sudden abrupt (step) change in line quantity i.e. the input voltage. Any input voltage disturbance tends to propagate through to the output and affect it directly. However, the feedback topology of the loop attenuates this disturbance to a large extent. Hence, by examining the line transient response of the converter, it can be predicted, to what extent, the input disturbance would affect the output voltage. As

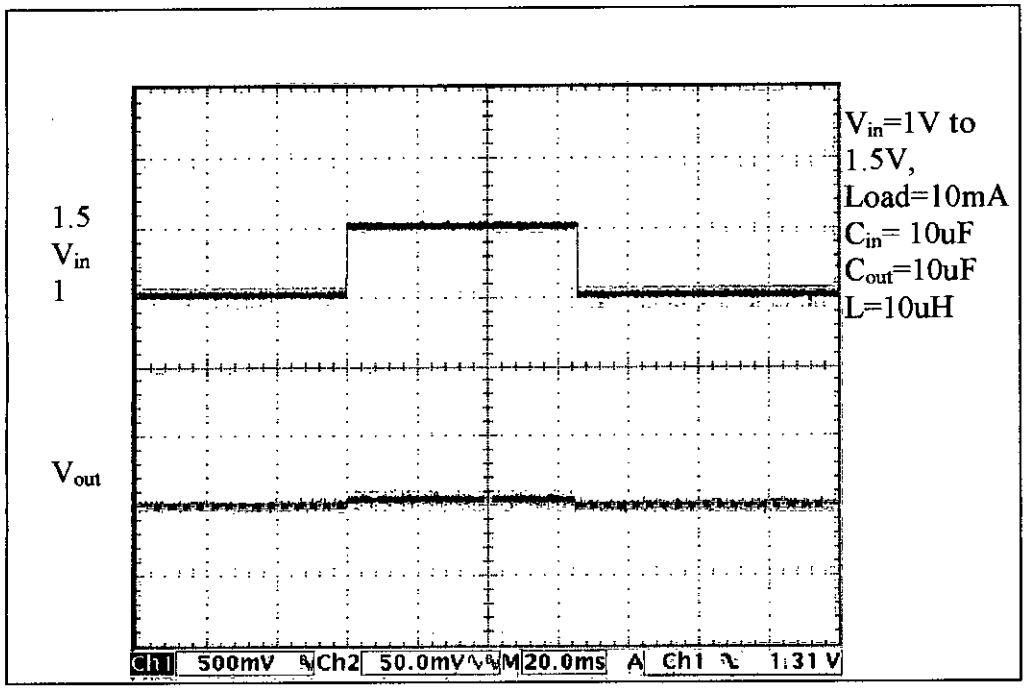

Fig 6.10: *The response of the converter output voltage for a step change in V_{in}*

shown in Fig 6.10, a step change of 500mV in input voltage could cause a 5mV change in output voltage.

g). High Duty Cycle Operation:

The converter can boost 1.5V up to 5V while supplying an output load of 15mA, running at 70% duty cycle. This condition has been illustrated in Fig 6.11. Inductor current and voltage at switch pin have been recorded in CH4 and CH2 respectively. It is to be noted that, the voltage at the switch pin=5V+diode drop.

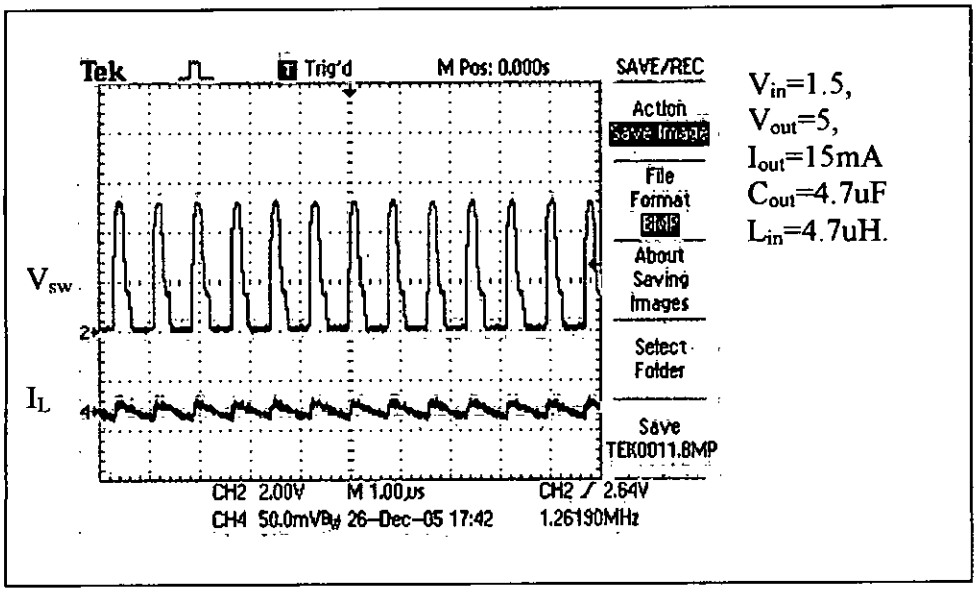

Fig 6.11: *Operation of the converter at D=70%*

h). Low Duty Cycle Operation:

The designed converter can operate at lower duty cycle without facing any type of response speed related problem. As shown in Fig 6.12, the converter is operating to have an output voltage of 3.3V from an input supply of 2.5V with a load

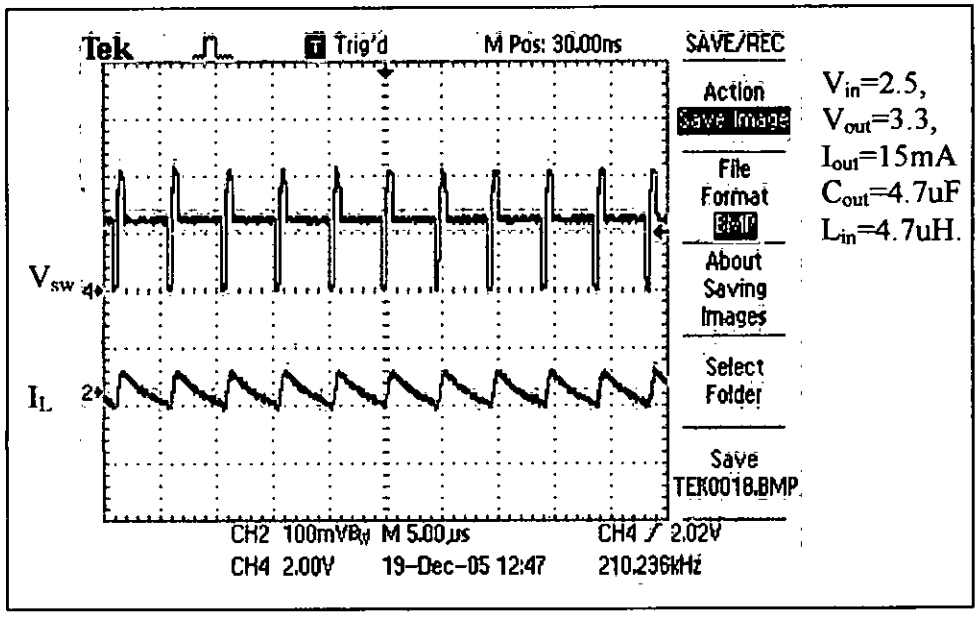

Fig 6.12: *Operation of the converter at D=24%*

of 15mA, i.e. it is operating at a duty cycle, as low as 24%.

Chapter 7

Conclusion & Future Work

7.1 Overview of the Whole Thesis:

In this thesis, a step-up converter of a new topology, with some unique features, has been developed. This converter is highly efficient over a large level of output load demand and very suitable for industrial purposes. A modulator model has been derived for this topology and based on both analytical approach and experimental verifications, it has been established that its loop stability is independent of duty cycle and any sort of external compensating network. Various critical issues relevant to the design and development of the chip have been discussed. Moreover, simulation results of various modes of the converter along with real time waves and data have been illustrated in the thesis.

7.2 Future Work on Model Related Issues:

AC analysis is one of the techniques used for determining open and closed loop gains, the relative positions of poles and zeros etc. for analyzing the loop dynamics of the linear circuits like OPAMP, LDO (Low Drop Out) regulator. Moreover, DC bias points' information can also be derived from such type of analysis. Such kinds of analyses are possible for the linear circuits because their states can be linearized. Switching regulators, on the other hand, have complicated loop dynamics and needs time domain analyses. As the behavior of such regulators, are non-linear, their states can't be linearized so easily and precisely like their linear counterparts. Various attempts have been taken and efforts have been made and now some works are being widely appreciated. Robert Sheehan has illustrated in *[14]*, some of the widely used techniques to model the current loop of the switching converters. Hence, following the steps of finding 'averaged model' or 'continuous-time model' or 'unified model' several parameters, for this topology, like Line to Output Gain, Audio Susceptibility Coefficient, Control to Output Gain, Current Loop Gain, and the Damping Coefficient Q_s etc. can be derived to analyze the loop dynamics more precisely.

7.3 Future Work on Implementation Related Issues:

Soft-start mechanism can be added to the main control block. This will prevent the huge inrush of current when the converter is turned ON. The huge inrush of current may cause a disaster, if the converter is connected to a supply bus and the under-shoot resulting from this inrush is latched. This may result in the hang up of the whole system or false logic generation.

To reduce the difference in average output voltage from the case of no-load to the case of full load, some steps may be taken. In full load condition, the control loop initiates the next cycle at the peak of the output voltage ripple, whereas, in the light load condition, this decision is taken at the valley of the output voltage ripple. Hence, naturally an error is introduced. Hence, to prevent this, the decision level for the converter to come out of the light load condition, can be increased.

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