AN ANALYTIC DESIGN MODEL FOR EPITAXIAL BIPOLAR POWER TRANSISTOR SWITCHES

BY

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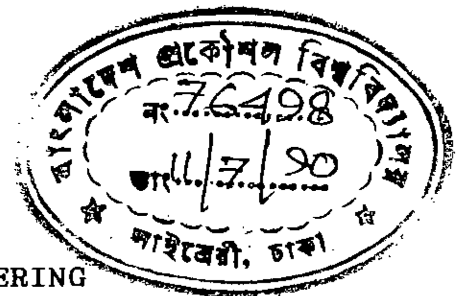

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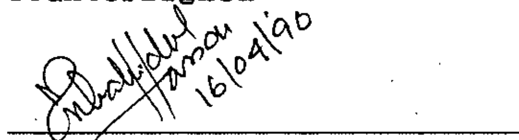

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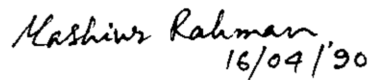

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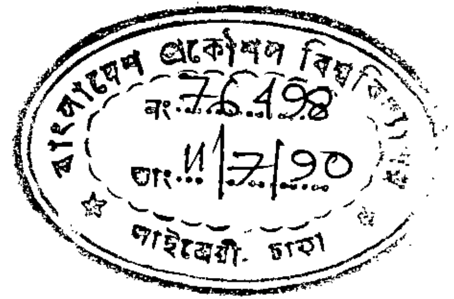

ABSTRACT

Continuous improvement in the field of technology and transistor physics have progressively opened up, to bipolar devices, the area of power applications upto 50 or 100 KVA. In particular the control of deep diffusion and thick epitaxies with low impurity concentrations had led to use $n^{+}pn^{-}n^{+}$ bipolar transistor as power switches. In this thesis an analytic design model is developed for epitaxial bipolar transistor switches where optimal calculations have been carried out for structural parameters which make it possible to comply in the best possible way with given specifications. All the numerical models follow a lengthy procedure and involes a large amount of computations. On the other hand this model is simple and straight forward and needs less computations. Results obtained by using this analytic model are compared with those evaluated numerically and are found in good agreement.

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CHAPTER 1

Introduction

1.1 Epitaxial Bipolar Transistor

The epitaxial technique consists of growing a thin, high-purity single-crystal layer of silicon or germanium on a heavily doped substrate of the same material. This augmented crystal forms the collector on which the base and emitter may be diffused through some standard processing. Epitaxial techniques are very much useful for manufacturing power transistors. For a power transistor switch, the desired features are current-handling capability in the on-state, blocking voltage in the off-state, switching times and losses. These features can be successfully achieved in an epitaxial transistor. A typical structure of an epitaxial bipolar $n^+pn^-n^+$ power transistor is shown in Fig.1.1a. A typical base-collector impurity concentration profile for an epitaxial transistor is shown in Fig.1.1b. The region adjacent to the base-collector junction is the most lightly doped and supports the reverse-biased collector-base voltage. Hence, this region essentially determines the breakdown voltage. To alter the breakdown voltage, the thickness and resistivity of the lightly doped collector region were changed.

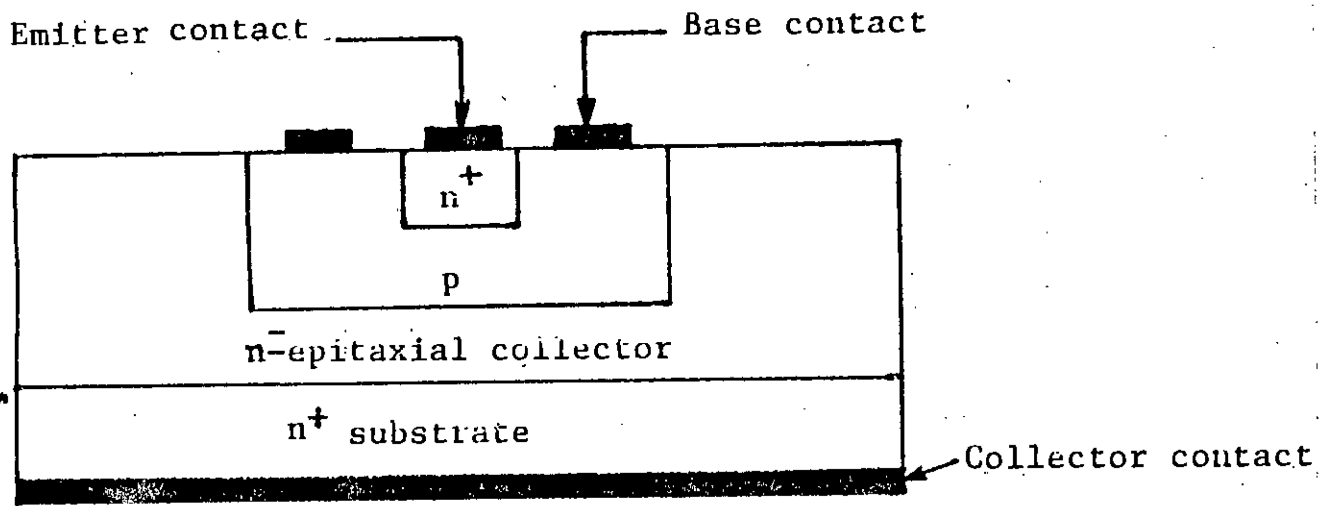

Fig. 1.1a Cross-section of an $n^{+}pn^{-}n^{+}$ epitaxial bipolar power transistor.

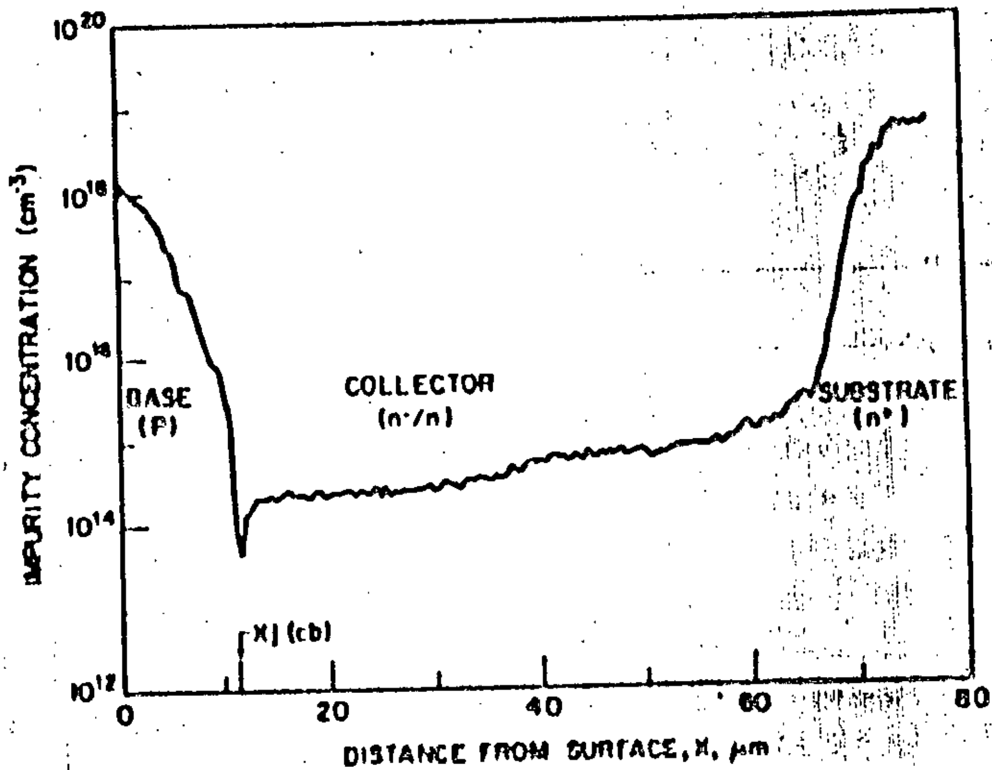

Fig. 1.1b Base-Collector impurity concentration profile showing the epitaxial collector and substrate region.

1.2 Transistor used as a Switch

An ideal switch should behave like a short circuit at the on state and like an open circuit at the off state. A transistor can approximate these behaviors of a switch. A switching transistor is designed to operate between the two regions i.e. the saturation region (on state) and the cutoff region(off state), of its output characteristic curve. It must switch between the two states in a very short time.

A simple switching circuit for a transistor in the common-emitter configuration is shown in figure 1.2 . In this figure the collector current i_C is controlled by the base current i_B over most of the family of characteristic curves. The load line specifies the locus of allowable (i_C,V_{CE}) points for the circuit. If the base current is zero or negative, the point C is reached at the bottom end of the load line,and the collector current is negligible. This is the 'off' state of the transistor and the device is said to be operating in the cut off regime. If the base current is positive and sufficiently large, the device is driven to the saturation regime, marked S. This is the "on" state of the transistor, in which a large value of i_C flows with only a very small voltage drop v_{CE}. In a typical switching operation the base current swings from

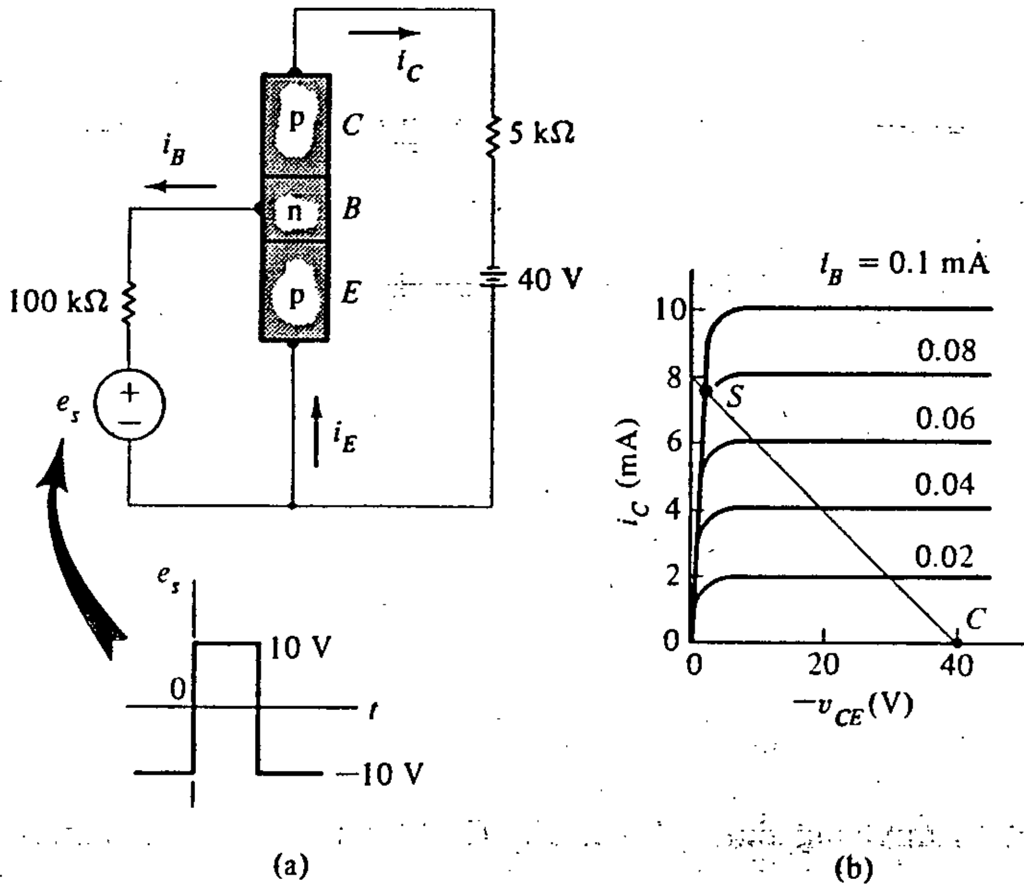

Fig. 1.2 Simple switching circuit for a transistor in the common-emitter configuration : (a) biasing circuit, (b) collector characteristics and load line for the circuit, with cutoff and saturation indicated.

positive to negative, thereby driving the device from saturation to cut-off, and vice versa.

1.3 Design Considerations

Designing a power transistor generally involves the development of a family of similar devices, each member of which possesses a different range of operating characteristics. To cover a wide spectrum of current-handling and voltage-blocking capabilities, changes are made in emitter area and in collector thickness and resistivity, respectively.

A switching epitaxial $n^+pn^-n^+$ power transistor must block a given voltage, it must carry a given current under the desired collector-emitter voltage V_{CE} and it must switch between the 'on' and 'off' states as quickly as possible [1]. In this work, a design model is developed for epitaxial bipolar power transistor switch, where optimal calculations are carried out for different structural parameters (i.e. doping concentration, layer thickness, geometrical dimensions etc.) which make it possible to comply with given specifications (i.e. BV_{CEO}, I_C, h_{FE} etc.) in the best possible way.

1.4 Summary of the Dissertation

The control of deep diffusions and thick epitaxies with low impurity concentrations has led to great improvements in structure design. Bipolar transistors have been preferred devices for a variety of applications. In this thesis we pursue the design of optimal parameters of power transistor switches.

In chapter 2, the avalanche breakdown voltages of an abrupt p^+n junction (base-collector) is numerically calculated. An empirical expression for breakdown voltage is established. The results are in good agreement with numerical values. In evaluation of Ionization integral, the most commonly used ionization rates given by Van Overstraeten and De Man [2] are used.

In chapter 3, breakdown voltage of an open-base transistor is calculated numerically. An analytical relationship between open-base and open-emitter breakdown voltage is established. This relationship is needed to obtain optimal values of collector parameters.

Chapter 4, deals with the derivations of mathematical expressions for optimal collector doping density and epitaxial layer thickness. Analytical expressions are derived by using the

method of Lagrange multipliers .

Chapter 5, deals with the design of epitaxial bipolar transistor switches. An optimization procedure is developed that completely specifies the parameters of the device with only two input data requirements - the collector-emitter sustaining voltage BV_{CEO} and the forced gain h_{FEF}. The analytical results are compared with numerical results of the other authors and are found in good agreement.

CHAPTER 2

Avalanche Breakdown voltages of Abrupt p^+n Junctions

2.1 Introduction

The breakdown voltage is one of the most important parameters in device design. In the evaluation of optimal parameters of collector doping density and collector width of a lightly doped collector, an analytic expression for open-emitter breakdown voltage BV_{CBO} for p^+n base-collector junctions given by Sze and Gibbons is often used. However, calculations based upon the ionization rates determined by Van Overstraeten and H. De Man [2] are shown to deviate substantially from the values obtained by Sze and Gibbons[3]. Reasons for discrepancies between ionization coefficients have been discussed in details by Van Overstraeten and De Man. In this chapter,the avalanche breakdown voltage V_B, is computed numerically for one-sided p^+n junctions based on the ionization rates of Van Overstraeten and De Man. Empirical expressions for breakdown voltage, maximum electric field and depletion layer width as a function of background doping N_B are then fitted to the numerical values. Empirical expression for breakdown voltage is used to calculate optimal values of collector parameters.

2.2 Avalanche Multiplication

Avalanche multiplication is the most important mechanism in junction breakdown, since the avalanche breakdown voltage imposes an upper limit on the reverse bias for most diodes, and on the collector voltage of bipolar transistors. Avalanche breakdown is caused by collisions between charge carriers and valence electrons in the reverse-biased depletion layers. As reverse bias voltage is increased, electron and/or holes (part of the reverse saturation current) achieve sufficient kinetic energies to generate hole-electron pairs when they collide with valence electrons. The new holes and electrons are accelerated by the electric field, achieving sufficient energy to generate more hole-electron pairs through collisions and so on. Thus each new carrier may, in turn, produce additional carriers through collision and the action of disrupting bonds. This cumulative process is referred to as avalanche multiplication. It results in large reverse currents, and the diode is said to be in the region of avalanche breakdown. The avalanche multiplication and breakdown processes are most probable in the lightly doped region of the depletion layer.

2.3 Ionization Integral

In the following section the basic ionization integral which determines the breakdown condition, is derived. Let us consider

the reverse biased junction, schematically shown in fig. 2.1. The origin of the x-axis is taken at the metallurgical junction. The boundaries of the depletion layer are respectively x_p and x_n. The total voltage across the junction is

$$V = V_a + V_d \qquad (2.1)$$

with V_a the external applied voltage and V_d the built-in potential. The sign convention for V_a used here, is that V_a is negative for reverse bias. The currents considered here to measure the multiplication factor, result from external excitation.

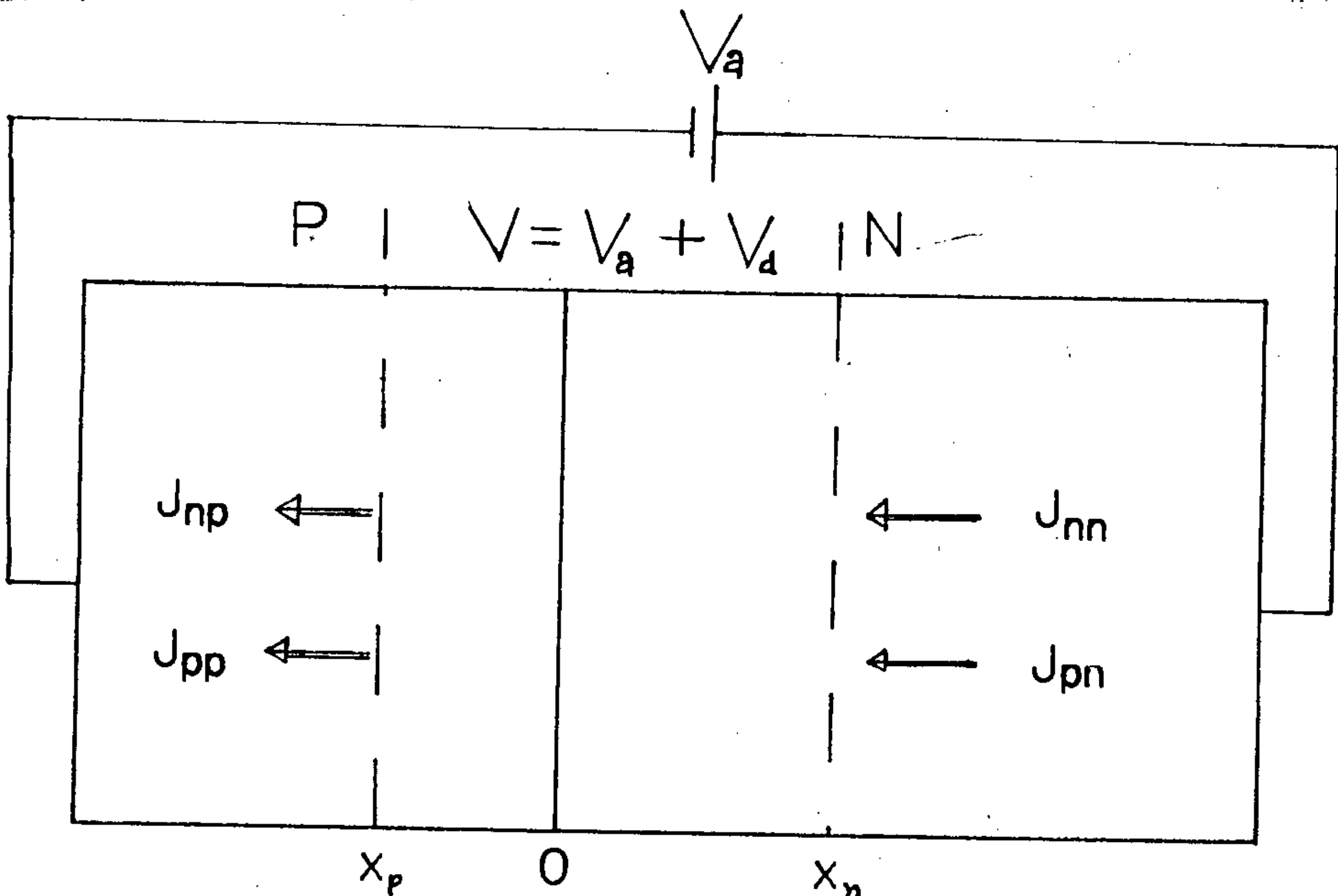

Fig. 2.1 A reverse biased p-n junction.

The minority carrier currents are referred to as J_{pn}, the hole current at x_n and J_{np}, the electron current at x_p respectively. For $qV = q(V_a+V_d)$ much larger than the threshold energy for ionization, the electrons and holes ionize, resulting in an increase of J_{pn} to J_{pp} at x_p and of J_{np} to J_{nn} at x_n. Since for $V_a = 0$ the total voltage across the junction corresponds to an energy qV_d, which is smaller than the threshold energy, there is no ionization. Consequently, the multiplication factor at a reverse voltage V may be defined and is calculated as [2]

$$M(V) = \frac{J(V)}{J(V_d)} = \frac{J_{nn} + J_{pn}}{J_{np} + J_{pn}} = \frac{J_{pp} + J_{np}}{J_{pn} + J_{np}} \qquad (2.2)$$

$$M(V) = \frac{\exp[-\int_{x_p}^{x_n}(\alpha_n - \alpha_p)dx] + k}{(1+k)\left(1 - \int_{x_p}^{x_n} \alpha_n \exp[-\int_{x_p}^{x}(\alpha_n - \alpha_p)dx]dx\right)} \qquad (2.3(a))$$

$$M(V) = \frac{k\exp[\int_{x_p}^{x_n}(\alpha_n - \alpha_p)dx] + 1}{(1+k)\left(1 - \int_{x_p}^{x_n} \alpha_p \exp[-\int_{x}^{x_n}(\alpha_p - \alpha_n)dx]dx\right)} \qquad (2.3(b))$$

with $k = J_{np}/J_{pn}$.

For an abrupt p^+n junction, the avalanche breakdown voltage is defined as the voltage at which the avalanche multiplication factor becomes infinite. For pure hole injection,

$k = 0$ ($J_{np} = 0$) and $M = \infty$

$$1 = \int_0^{W_c} \alpha_p \exp[-\int_x^{W_c} (\alpha_p - \alpha_n)dx]dx \qquad (2.5)$$

If x_p is taken as reference(0), then $x_n = W_c$. So the above equation becomes

$$\therefore \quad 1 = \int_{x_p}^{x_n} \alpha_p \exp[-\int_x^{x_n} (\alpha_p - \alpha_n)dx]dx \qquad (2.4)$$

where W_C is the thickness of the space-charge layer in the n-region at breakdown.

2.4 Numerically Calculated Breakdown Voltages

The threshold condition for avalanche breakdown in a one-sided p^+n junction where the avalanche multiplication is initiated by holes can by expressed by equation (2.5). The space-charge layer thickness in the heavily doped base (p^+) region is assumed to be negligible . The field dependence of the ionization rates α, can

be expressed by

$$\alpha = A \exp(-b/E(x)) \quad (2.6)$$

Therefore, for hole ionization

$$\alpha_p = A_p \exp(-b_p/E(x)) \quad (2.7)$$

and for electron ionization

$$\alpha_n = A_n \exp(-b_n/E(x)) \quad (2.8)$$

where the value of A and B are given by Van Overstraeten and De Man [2].

$A_p = 1.582 \times 10^6 \ cm^{-1}$

$b_p = 2.036 \times 10^6 \ V\ cm^{-1}$

$A_n = 7.03 \times 10^5 \ cm^{-1}$

$b_n = 1.211 \times 10^6 \ V\ cm^{-1}$.

Poisson's equation and other relevant equations used in solving the integral equation of (2.5) numerically are as follows:

$$\frac{dE}{dx} = \frac{q}{\epsilon}(p + N_B - n) \quad (2.9)$$

$$E_m = \frac{q}{\epsilon} N_B W_c \quad (2.10)$$

$$V_B = \frac{\epsilon E_m^2}{2qN_B} \quad (2.11)$$

where ϵ is the permittivity of silicon, q is the electronic

charge, and n and p are electron and hole densities, respectively. In carrying out the integration of (2.5), a powerful and efficient numerical technique , Romberg method, is used. The values of peak electric field E_m for given values of doping densities N_B are calculated numerically in such a way that equation (2.5) is satisfied. With known value of E_m, the breakdown voltage V_B can be obtained from (2.11).

The numerical results are plotted in Figs. 2.2-2.4. The breakdown condition for a one sided n^+p junction can be obtained by using J_{pn} = 0 and $K = \infty$. The breakdown field for this junction is slightly greater than that for P^+n junction. Because this difference is not significant and because mostly P^+n base-collector junction is used in epitaxial power transistor switch, the breakdown voltages for one-sided p^+n junction are carried out in this chapter.

2.5 Empirical Expression for Breakdown Voltages

With the help of numerical results obtained in the previous section, the empirical expression for V_B in terms of the doping density N_B is derived using the method of least square. Using this expression and equations (2.10) and (2.11) of previous section, the empirical expressions for E_m and W_c are derived in

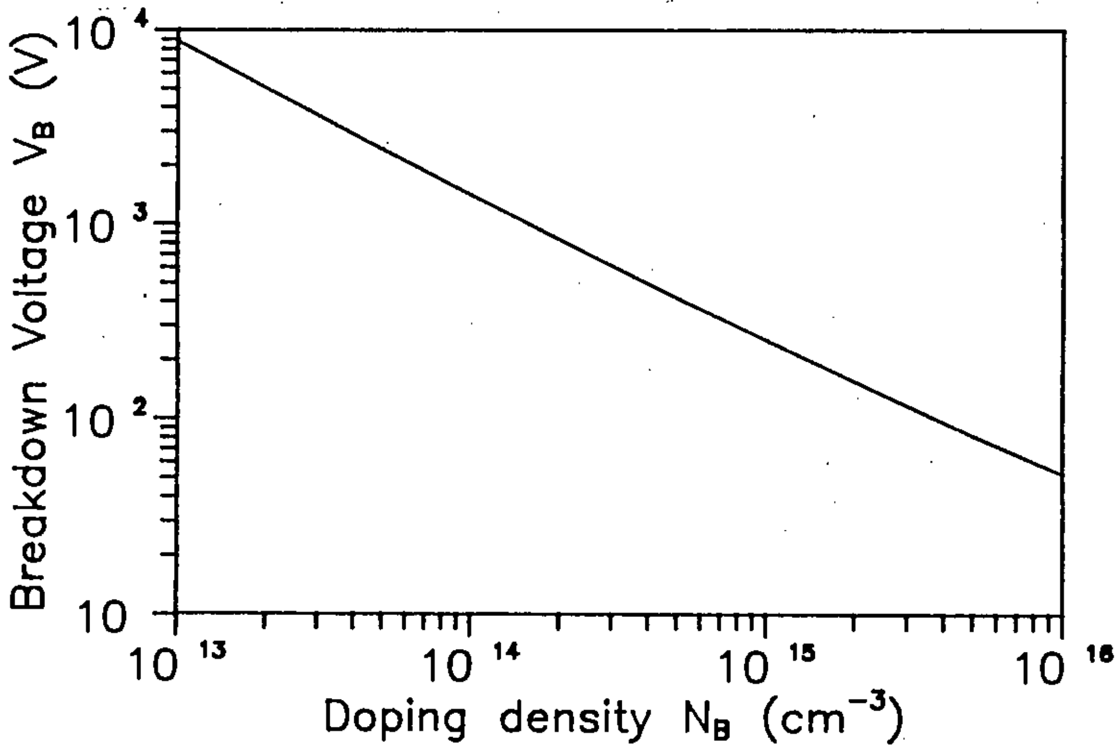

Fig. 2.2 Numerically obtained breakdown voltage as a function of doping density.

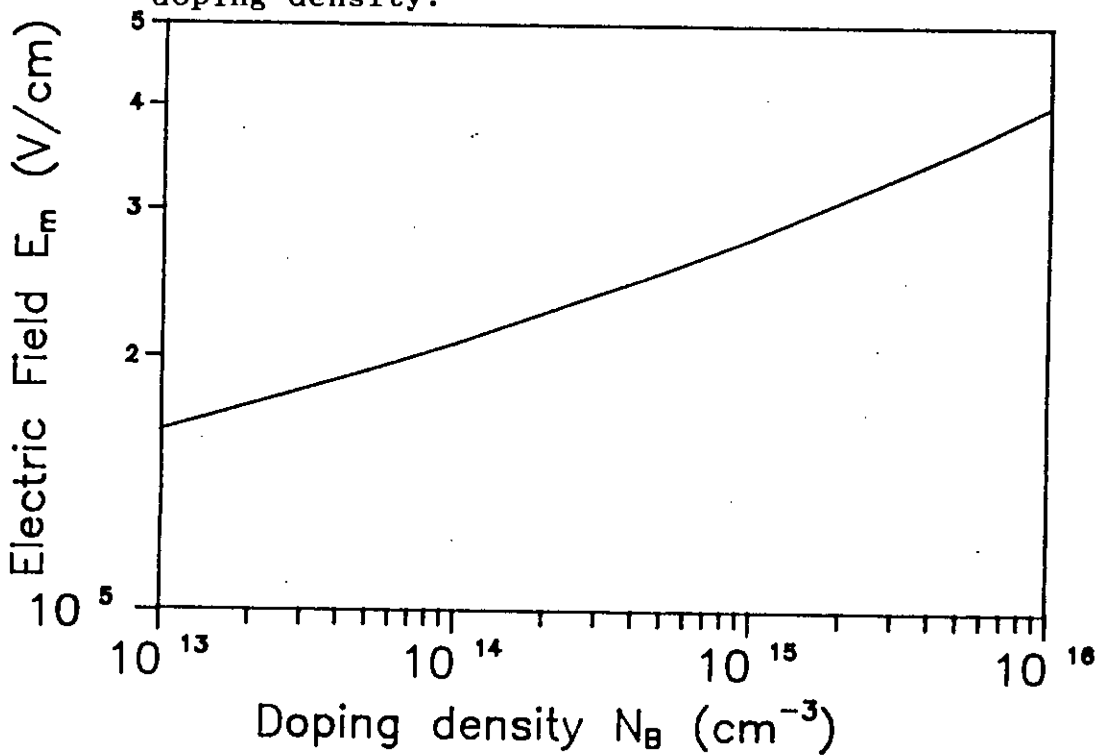

Fig. 2.3 Numerically obtained maximum electric field as a function of doping density.

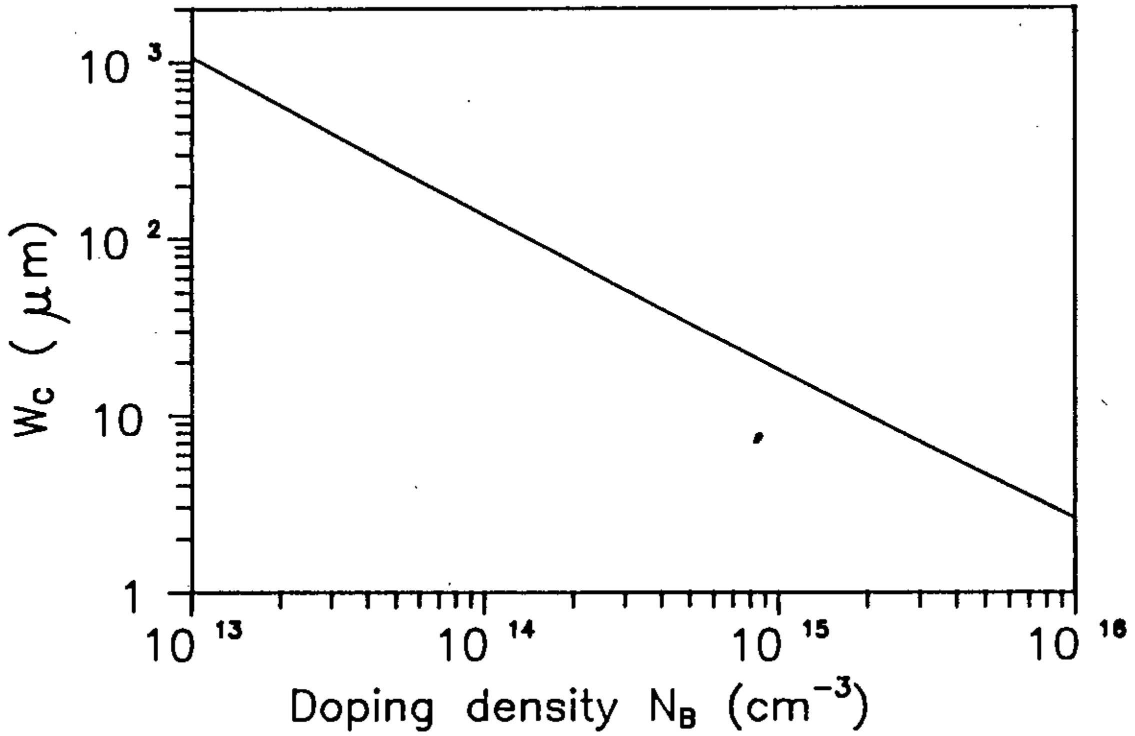

Fig. 2.4 Numerically obtained depletion layer width as a function of doping density.

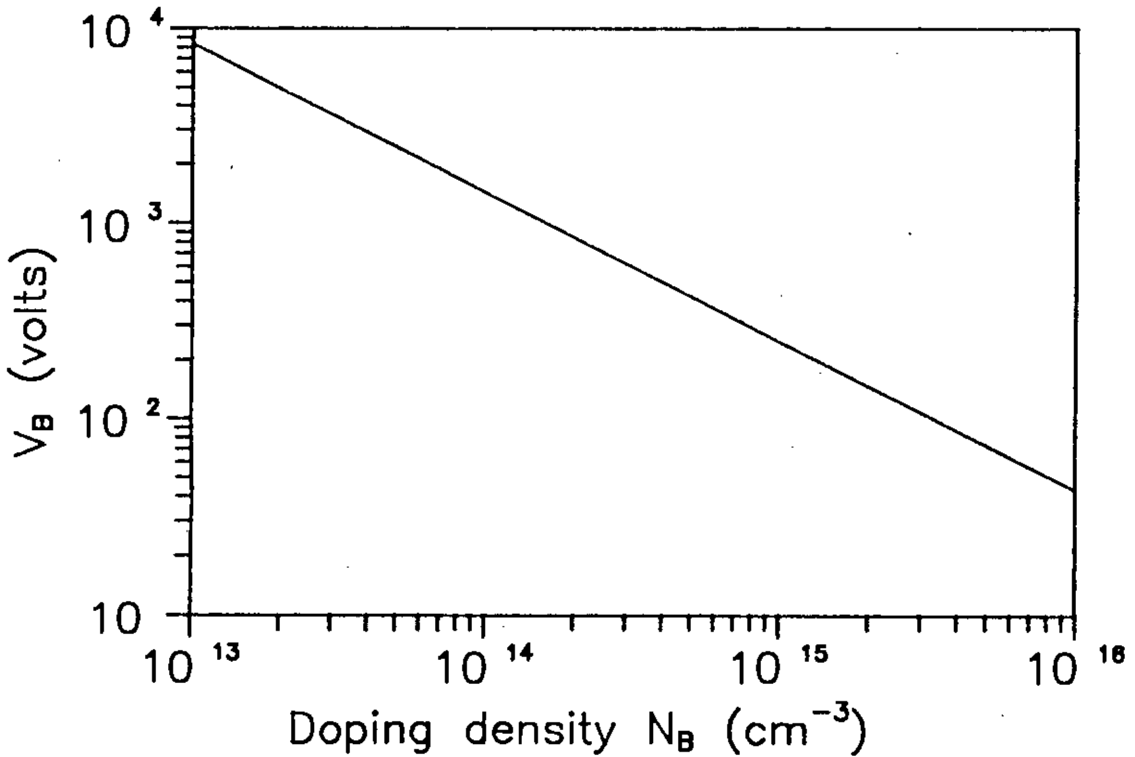

Fig. 2.5 Analytically obtained breakdown voltage as a function of doping density.

terms of N_B. They are given by

$$V_B = 6.31 \times 10^{13} N_B^{-0.76} \quad \text{volts} \qquad (2.12)$$

$$E_m = 4.41 \times 10^{3} N_B^{0.12} \quad \text{v/cm} \qquad (2.13)$$

$$W_c = 2.861 \times 10^{10} N_B^{-0.88} \quad \text{cm} \qquad (2.14)$$

Analytically calculated breakdown voltage V_B is shown in Fig. 2.5. The analytical results are in good agreement with numerical results.

2.6 Conclusions

Solving the ionization integral the avalanche breakdown voltage as a function of background doping for abrupt Si p^+n junction is calculated numerically based upon the ionization rates determined by Van Overstraeton and De Man[2]. An empirical expression for breakdown voltage is also derived. This analytical expression for bulk breakdown voltage can be used in the calculation of optimal parameters of the collector region of epitaxial power transistors.

CHAPTER 3

Breakdown Voltage of Open Base Transistor

3.1 Introduction

Designing a power transistor always involves optimal calculations of collector doping and collector width for desired values of blocking voltage specified either in terms of open base breakdown voltage or open emitter breakdown voltage. In the evaluation of optimal parameters, closed-from analytical expressions for collector doping density and collector width are often determined by using the relationship of open base breakdown voltage $BV_{CEO}*$ with maximum (low level) current gain h_{FEO} and open emitter breakdown voltage $BV_{CBO}*$ given by Miller [4]. In this chapter, both $BV_{CEO}*$ and $BV_{CBO}*$ are calculated numerically and then an empirical relationship is fitted to numerical values. These relationships are useful in obtaining analytical expressions for optimal parameters of collector region.

3.2 Numerical Solution

In the case of open emitter breakdown voltage $BV_{CBO}*$, equation (2.12) of chapter 2 can be used for an $n^+pn^-n^+$ transistor. For

convenience, the equation is rewritten here,

$$BV_{CBO}* = 6.31 \times 10^{13} \quad N_D^{-0.76} \quad \text{Volt} \tag{3.1}$$

where N_D is the doping density of the lightly doped n region. The breakdown condition for $BV_{CEO}*$ is given by $M\alpha = 1$, where α is the current transfer ratio. For $n^+pn^-n^+$ transistor, $K = I_{CO}/(\alpha I_B) = 1/h_{FEO}$ and $\alpha = h_{FEO}/(1+h_{FEO})$ then $M\alpha = M\, h_{FEO}/(1+h_{FEO})$, where I_{CO} is the collector saturation current with open emitter junction. Now with $M\alpha = 1$ equation (2.3(b)) of chapter 2 becomes

$$\frac{(1+h_{FEO})^2}{h_{FEO}} = \frac{\exp[-\int_0^{W_c}(\alpha_n - \alpha_p)dx] + h_{FEO}}{1 - \int_0^{W_c}\alpha_n \exp[-\int_x^{W_c}(\alpha_n - \alpha_p)dx]dx} \tag{3.2}$$

where the meaning of α_n and α_p have been described in the previous chapter.

The electric field and potential in the lightly doped collector space charge region of a transistor are determined from the solution of Poisson's equation. For a given h_{FEO}, the breakdown voltage is given by

$$BV_{CEO}* = 1/2\ (E_m W_C) = (\epsilon E_m^2)/(2q N_D) \quad V \tag{3.3}$$

where E_m is the maximum electric field, W_c is the space charge width, q is the electronic charge, ϵ is the dielectric constant of silicon and N_D is the collector doping density.

Now if equation (3.2) is numerically solved along with the equations (2.10) and (2.11) of chapter 2 and equation (3.2) of this chapter, then maximum electric field E_m and breakdown voltage BV_{CEO}* as a function of collector impurity density N_D for different values of current gain h_{FEO} are obtained. Plots of these numerically obtained data are shown in Figs. 3.1 and 3.2.

3.3 Empirical Expressions

From the numerical data obtained from the numerical solution in the previous section, curves of bulk breakdown voltage BV_{CEO}* versus the impurity concentration N_D can be plotted with h_{FEO} as a parameter. Now for fixed h_{FEO} empirical expressions of BV_{CEO}* as a function of N_D can easily be obtained following any one of the standard numerical techniques. Again from the BV_{CEO}* VS. N_D curves which were drawn for different values of h_{FEO}, variation of BV_{CEO}* with h_{FEO} for a fixed N_D can be read easily. Thus an empirical expression for BV_{CEO}* as a function of h_{FEO} can be obtained easily. Combining the two empirical expressions of BV_{CEO}* another empirical expression expressing

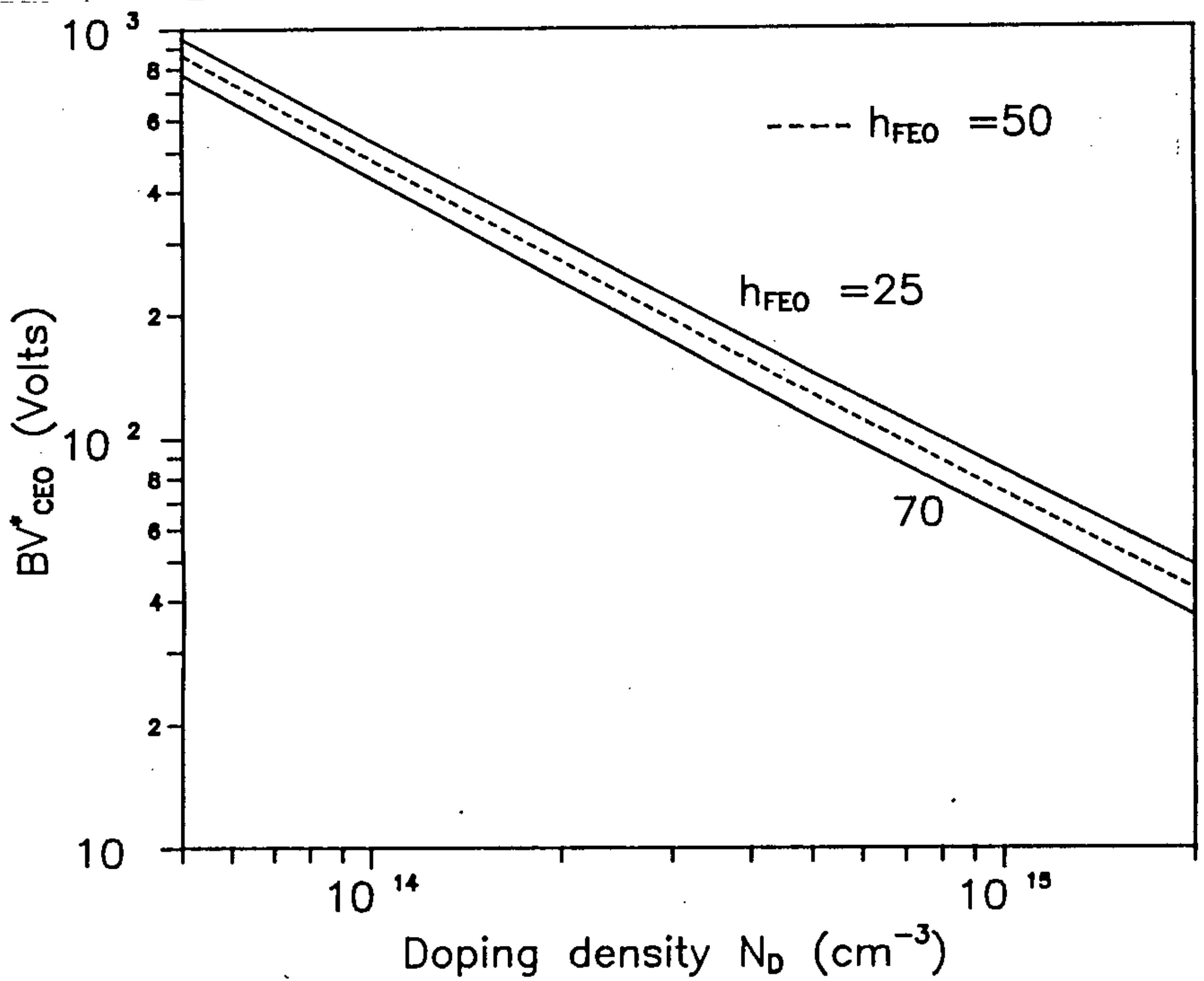

Fig. 3.1 Numerically obtained values of bulk breakdown voltage as a function of doping concentration for different values of current gain.

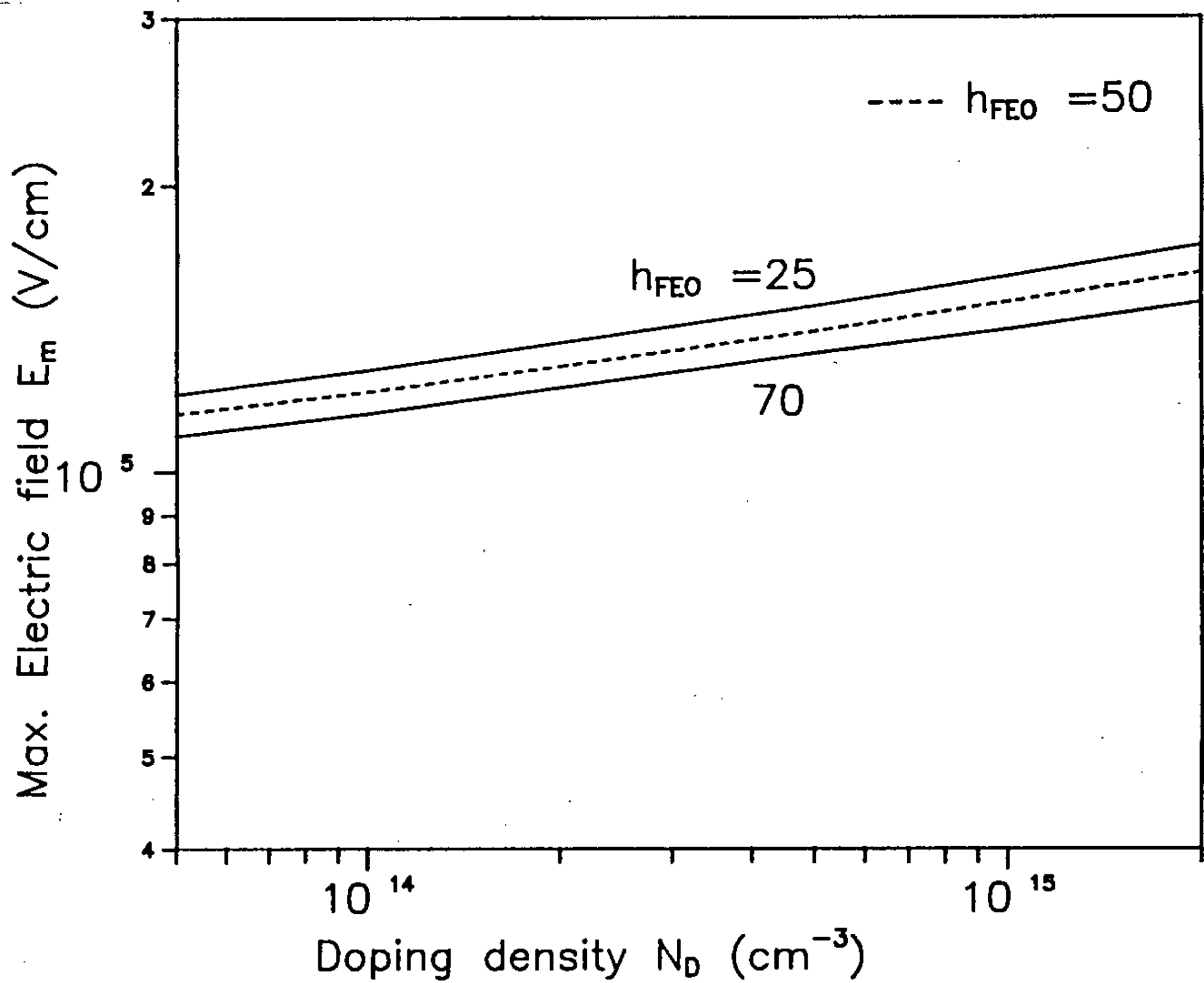

Fig. 3.2 Numerically obtained values of maximum electric field as a function of doping concentration for different values of current gain.

$BV_{CEO}*$ as a function of both h_{FEO} and N_D can be obtained. An empirical expression of maximum electric field E_m as a function of both h_{FEO} and N_D can be obtained by a similar process. The expressions are given below

$$BV_{CEO}* = 2.979 \times 10^{14} (1+h_{FEO})^{-0.183} N_D^{-0.82} \quad V \quad (3.4)$$

$$E_m = 9.55 \times 10^{3} (1+h_{FEO})^{-0.09} N_D^{0.09} \quad V/cm \quad (3.5)$$

A plot of $BV_{CEO}*$ as a function of N_D is shown in Fig. 3.3.

3.4 Relationship Between Open Emitter and Open Base Breakdown Voltages

The transistor is designed to block a specified voltage. This voltage is specified either in BV_{CEO} or in BV_{CBO}. Here a relation between bulk open-base and open-emitter voltages has been established on the basis of numerical results.
Equation(3.1) can be written as

$$N_D = [\ 6.31 \times 10^{13} (BV_{CBO}*)^{-1}]^{1/0.76}$$

$$\text{or, } N_D = 1.4385778 \times 10^{18} (BV_{CBO}*)^{-1/0.76} \quad cm^{-3} \quad (3.6)$$

Now, if the N_D of equation (3.4) is replaced with the above

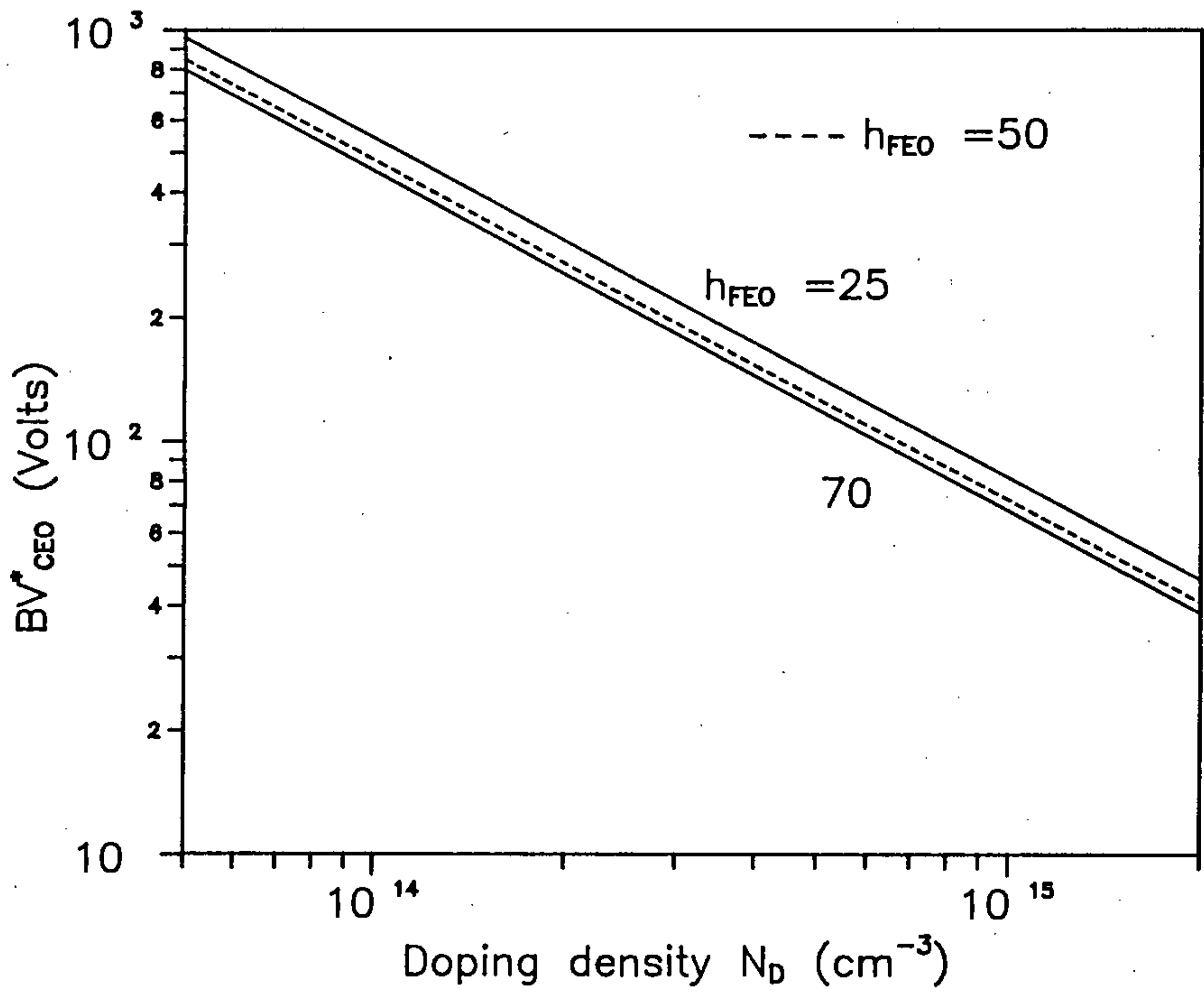

Fig. 3.3 Analytical plot of bulk breakdown voltage as a function of doping concentration.

expression of N_D, then the expression for $BV_{CEO}*$ becomes

$$BV_{CEO}* = 0.385(1 + h_{FEO})^{-0.183}\ BV_{CBO}*^{1.079}\ \text{V} \quad (3.7)$$

3.5 Conclusions

Open base breakdown voltage as a function of collector doping N_D and current gain h_{FEO} for npn transistor with lightly doped collector is calculated numerically based upon the most widely used ionization rates given by Van Overstraeten[2]. An empirical expression for breakdown voltage as a function of collector doping density and current gain is also established. Then an analytical expression relating open base breakdown voltage $BV_{CEO}*$ with open emitter breakdown voltage $BV_{CBO}*$ and current gain h_{FEO} is derived. By using the analytical expression for breakdown voltage $BV_{CEO}*$, more accurate optimal values of collector doping density and width under reach through condition can be obtained and will, therefore, be useful to the practical designers.

CHAPTER 4

Calculation of Optimal Values of Collector Parameters

4.1 Introduction

In designing a power transistor, determination of the optimal values of collector parameters is most important. In this chapter analytical expressions for two most important collector parameters i.e. the collector doping concentration N_C and the collector width W_C are determined. These two expressions give the optimal values of collector doping and collector width. In the determination of the expressions for optimal values of the colllector parameters, the wellknown method of Lagrange multipliers is used. These very important analytical expressions are used in the next chapter for designing the collector section of the transistor.

4.2 Breakdown Voltage under Reach Through Condition

With regard of W_C, the obvious choice would be to allow the depletion layer to spread freely in order to sustain the given

BV_{CEO}. However, a moderate reduction of W_C below the value W_{sc} corresponding to the free extent of the depletion layer (Fig.4.1) can lead to an advantageous rise in maximum on-state current I_{cmax} [5]. In order to avoid affecting the voltage-blocking capability, such a reduction must be accompanied by a decrease in collector impurity concentration N_C. This is quantitatively explained in Fig.4.1. Poisson's equation shows that the slope of E vs W curve is directly proportional to the the doping density N_C. Again the area under the E/W curve determines the blocking voltage BV_{CEO}. Now , if a reduced value of N_C and W_C is chosen in such a way that the required blocking voltage BV_{CEO} is supported then from Fig.4.1 the following expressions can be written.

The sustaining voltage $BV_{CEO}*$ which would be observed in case of free spreading (extent W_{sc}) of the depletion layer into the collector region, is given by

$$BV_{CEO}* = 1/2\ E_m\ W_{sc} \qquad (4.1)$$

and $$W_{sc} = \epsilon E_m/qN_C \qquad (4.2)$$

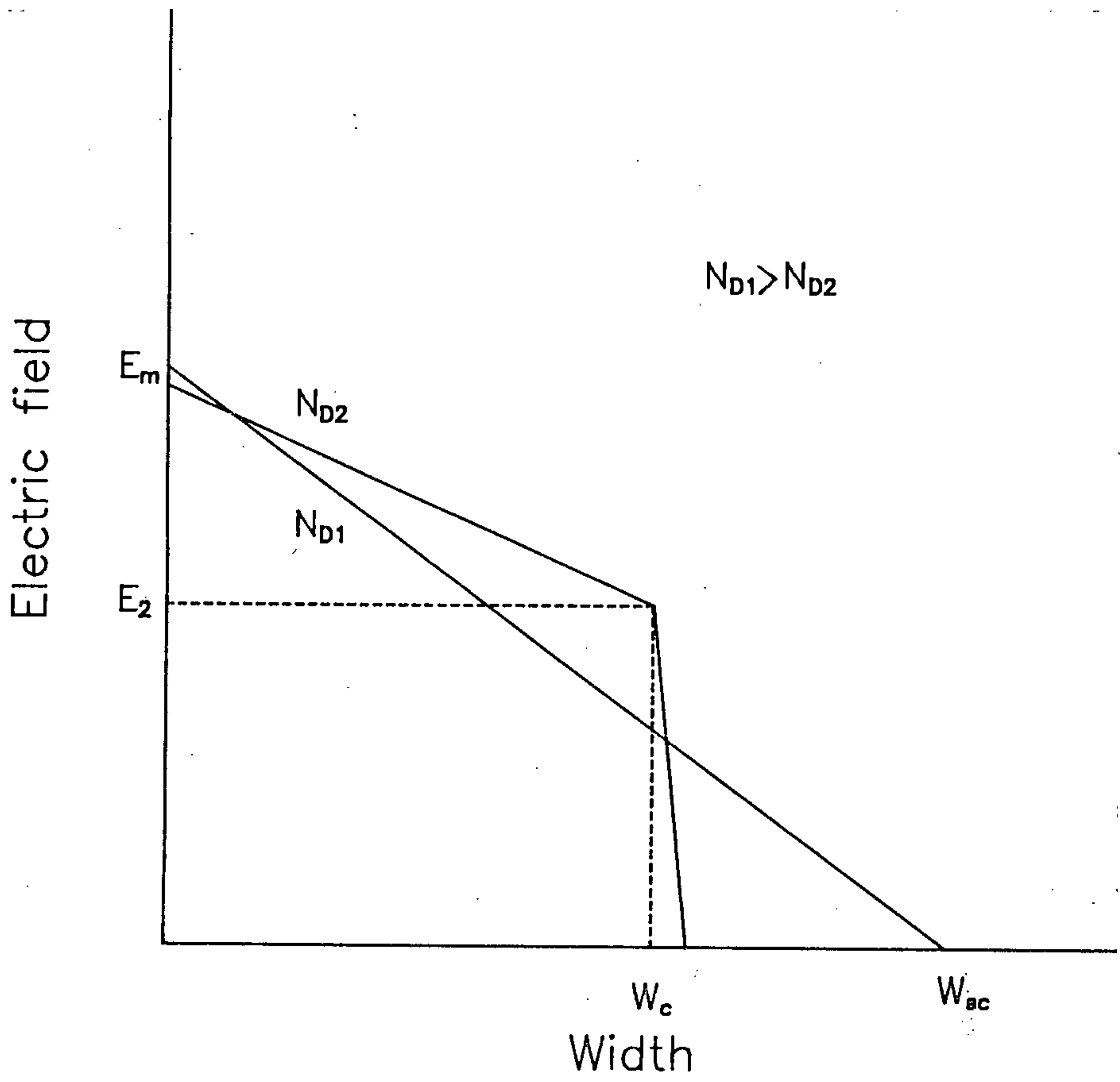

Fig. 4.1 Illustrating the (W_c, N_c) relationship for a given BV_{CEO}

The blocking voltage under reach-through condition BV_{CEO} is given by

$$BV_{CEO} = 1/2(E_m + E_2)W_c \qquad (4.3)$$

and $$E_m - E_2 = \frac{qN_cW_c}{\epsilon}$$

or $$E_m + E_2 = 2E_m - \frac{qN_cW_c}{\epsilon}$$

or $$E_m + E_2 = 2\left(\frac{2q}{\epsilon} N_cBV_{CEO}^*\right)^{1/2} - \frac{q}{\epsilon} N_cW_c \qquad (4.3a)$$

So, from (4.3) it can be written

$$BV_{CEO} = (2qN_cBV_{CEO}^*/\epsilon)^{1/2}W_c - \frac{qN_cW_c^2}{2\epsilon} \qquad (4.4)$$

4.3 Analytical Expressions for Doping Density and Width Under Reach Through Condition

In designing an epitaxial $n^+pn^-n^+$ power transistor switch it must be kept in mind that the transistor must block a given voltage, it must carry a given current under the desired collector-emitter voltage V_{CE}. In regard to collector width W_c, the obvious choice would be to allow the depletion layer to spread freely at the specified open base breakdown voltage

BV_{CEO}. However, in the previous section it is pointed out that a moderate reduction of W_C to some what less than the unbounded depletion layer width is advantageous. But a reduced W_C must be accompanied by a reduced collector impurity concentration N_C, in order to avoid affecting the voltage-blocking capability. Again, a decrease of N_C increases the collector resistance. Therefore, the best performance demands a combination of high doping levels and small epitaxial layers, while meeting the requirement of supporting the given BV_{CEO} voltage. Optimization of a collector layer in this respect leads to a reach-through condition at breakdown. To find the optimized values of N_C and W_C as a function of current gain h_{FEO} and sustaining voltage BV_{CEO} the method of Lagrange multipliers [6] is used.

In the previous section the mathematical expression for open-base breakdown voltage BV_{CEO} (N_C, W_C) due to reach -through in terms of bulk breakdown BV_{CEO}^* and doping concentration N_C is found , which is

$$BV_{CEO} = W_C(2qN_C BV_{CEO}^*/\epsilon)^{1/2} - (q/2\epsilon)W_C^2 N_C \quad (4.5)$$

The open-base bulk breakdown voltage is given by the expression [see section 3.3]

$$BV^{*}_{CEO} = B(1 + h_{FEO})^{-m_1} N_c^{-m_2} \qquad (4.6)$$

where B, m_1 and m_2 are constants. Their values are

B = 2.979 x 10^{14}

m_1 = 0.183

m_2 = 0.82

Using equations (4.5) and (4.6), one can write

$$BV_{CEO} = W_c(\frac{2q}{\epsilon}B)^{\frac{1}{2}}(1 + h_{FEO})^{-\frac{m_1}{2}} N_c^{\frac{1-m_2}{2}} - \frac{q}{2\epsilon}W_c^2 N_c \qquad (4.7)$$

The above equations for breakdown are derived on the assumption that the peak electric field at breakdown is insensitive to the epitaxial layer thickness (a premise based upon the very strong dependence of ionization rate on electric field strength). Eqn. (4.7) is a function of W_c and N_c. It can be written as

$$g = W_c(\frac{2q}{\epsilon}B)^{\frac{1}{2}}(1 + h_{FEO})^{-\frac{m_1}{2}} N_c^{\frac{1-m_2}{2}} - \frac{q}{2\epsilon}W_c^2 N_c - BV_{CEO} \qquad (4.8)$$

The resistance per unit area of the collector region is given by

$$R = \frac{W_c}{q\mu_n N_c} \tag{4.9}$$

where μ_n is the electron mobility. The minimum value of resistance R can be obtained by using Lagrange multipliers [6] with the constraint given by equation (4.7). Taking derivatives of R with respect to W_C and N_C we get

$$R_w = \frac{1}{q\mu_n N_c} \tag{4.10}$$

$$R_n = -\frac{W_c}{q\mu_n N_c^2} \tag{4.11}$$

Also the first derivatives of g (N_C, W_C) with respect to W_C and N_C result in

$$g_w = (\frac{2q}{\epsilon}B)^{\frac{1}{2}}(1 + h_{FEO})^{-\frac{m_1}{2}} N_c^{\frac{1-m_2}{2}} - \frac{q}{\epsilon}W_c N_c \tag{4.12}$$

$$g_n = W_C(2qB/\epsilon)^{1/2}((1-m_2)/2)(1+h_{FEO})^{-m_1/2} N_C^{-(1+m_2)/2} - qW_C^2/2\epsilon \tag{4.13}$$

From the method of Lagrange multipliers

$$R_w - \lambda g_w = 0 \tag{4.14}$$

$$R_n - \lambda g_n = 0 \tag{4.15}$$

where λ is a Lagrange multiplier. Solving equation (4.7), (4.14) and (4.15), we can write

$$N_c = K_1(1 + h_{FEO})^{-\frac{m_1}{m_2}} BV_{CEO}^{-\frac{1}{m_2}} \tag{4.16}$$

$$W_c = K_2(1 + h_{FEO})^{-\frac{m_1}{2m_2}} BV_{CEO}^{-\frac{1+m_2}{2m_2}} \tag{4.17}$$

where $$K_1 = \left(\frac{B}{9} \quad (9 - m_2)^2\right)^{\frac{1}{m_2}} \tag{4.18}$$

$$K_2 = \left(\frac{2\epsilon}{q}B\right)^{\frac{1}{2}}\left(\frac{3 - m_2}{3}\right)K_1^{-\frac{1+m_2}{2}} \tag{4.19}$$

are two purely numerical Coefficients. The values of K_1 and K_2 can be calculated as

$K_1 = 4.076 \times 10^{17}$ and $K_2 = 4.276 \times 10^{-6}$

4.4 Conclusions

Optimal values of collector parameters are very useful to the practical designer. In designing power transistor switches, the analytical expressions for N_C and W_C need to be used. With these optimal values, the other design parameter of a transistor switch can be obtained. The detail analysis is give in the next chapter.

CHAPTER 5

Optimal Values of Parameters of Power Transistor Switches

5.1 Introduction

Although the relationship between a transistor's operating characteristics and structural parameters have been known for a long time, designers often rely on cut-and-try methods for the development of their devices. This is probably due to the fact that technological difficulties did not permit them to take advantage of these relationships or even to establish their validity by experimental measurements. With the availability of advanced techniques in device fabrication and parameter measurements, manufacturers have now recognized the importance of design methods based upon detailed physical models. Designing a power transistor generally involves calculation of emitter area A_e, collector doping density N_C, collector width W_C and base doping concentration N_B for desired values of open base breakdown voltage BV_{CEO} and current gain h_{FE} at given collector current I_C and collector-emitter voltage V_{CE}.

In this work a design model is developed for uniformly doped epitaxial bipolar transistor switches, where optimal calculations have been carried out for structural parameters (i.e. doping concentrations, layer thicknesses, geometrical dimensions etc.) which make it possible to comply in the best possible way with given specifications. P.L. Hower in his paper [7] outlined a procedure for evaluation of minimum emitter area A_e meeting both h_{FE} and BV_{CEO} specifications. His proposed model is straight forward, but follows a lengthy procedure and involves more computational efforts than the model presented in this chapter. The present model is simple and needs less computations.

5.2 Design Criterion

5.2.1 Collector Region

In chapter 4 it has been pointed out that optimization of the collector layer width leads to a reach-through condition at breakdown, where the collector impurity density N_C is reduced to support the given BV_{CEO}. But with reduction of collector impurity density N_C, the resistivity of the collector region increases. Although, very high collector resistivities correspond to the lowest acceptable W_C values but it has the following major drawbacks: i) Intensified quasi-saturation

effects and ii) Increased liability to current-mode second breakdown [5]. Therefore, it is very important to choose a pair of values of N_C and W_C which minimizes the "collector resistance" W_C. In the previous chapter, optimum values of N_C and W_C have been determined using the method of Lagrange's multipliers. For convenience the expressions for optimum N_C and W_C are reproduced here.

$$N_C = K_1(1+h_{FEO})^{-m_1/m_2} BV_{CEO}^{-1/m_2} \quad (5.1)$$

$$W_C = K_2 (1+h_{FEO})^{m_1/2m_2} BV_{CEO}^{(1+m_2)/2m_2} \quad (5.2)$$

Analytical plots showing N_C and W_C as a function of maximum current gain h_{FEO} are shown in Figs. 5.1 and 5.2 for different values of BV_{CEO}.

5.2.2 Base Region

The impurity charge Q_B in the base region, which is the integral of the base impurity density over the base width, is the most influential parameter upon the maximum (low-level) value of current gain h_{FEO} in the case of a high carrier life time. P.L. Hower [7] derived an expression for the current gain h_{FE} of an $n^+pn^-n^+$ transistor on the basis of the Moll-Rose [8] and Gummel-Poon models [9].

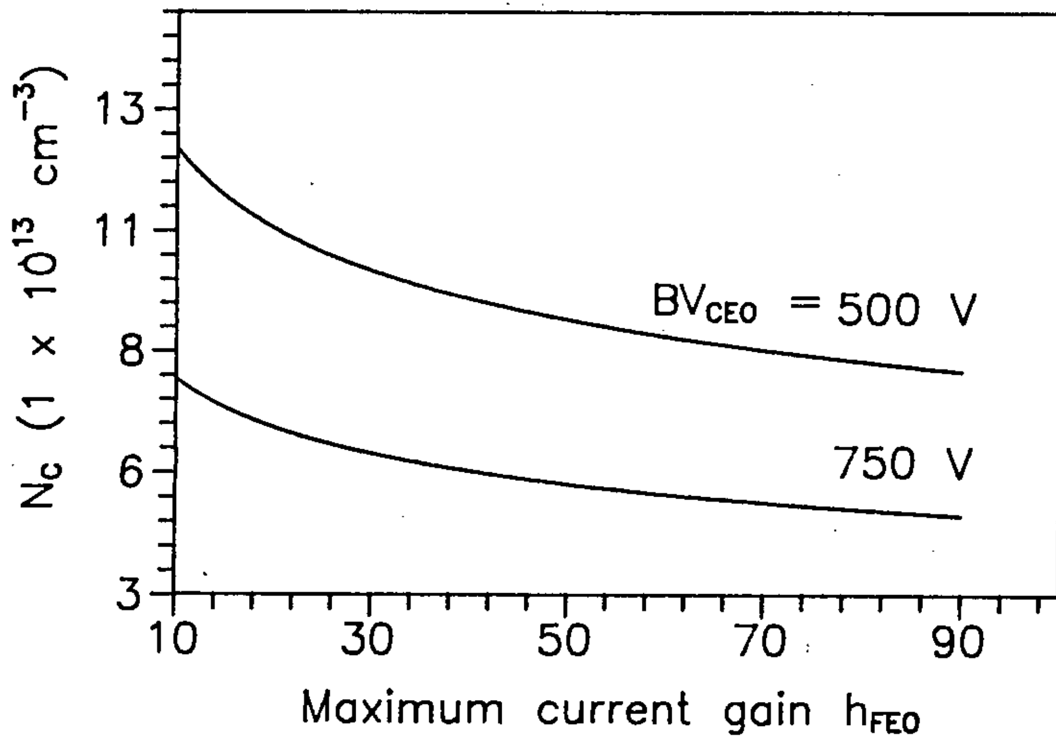

Fig. 5.1 Collector doping density as a function of maximum current gain for different values of BV_{CEO}.

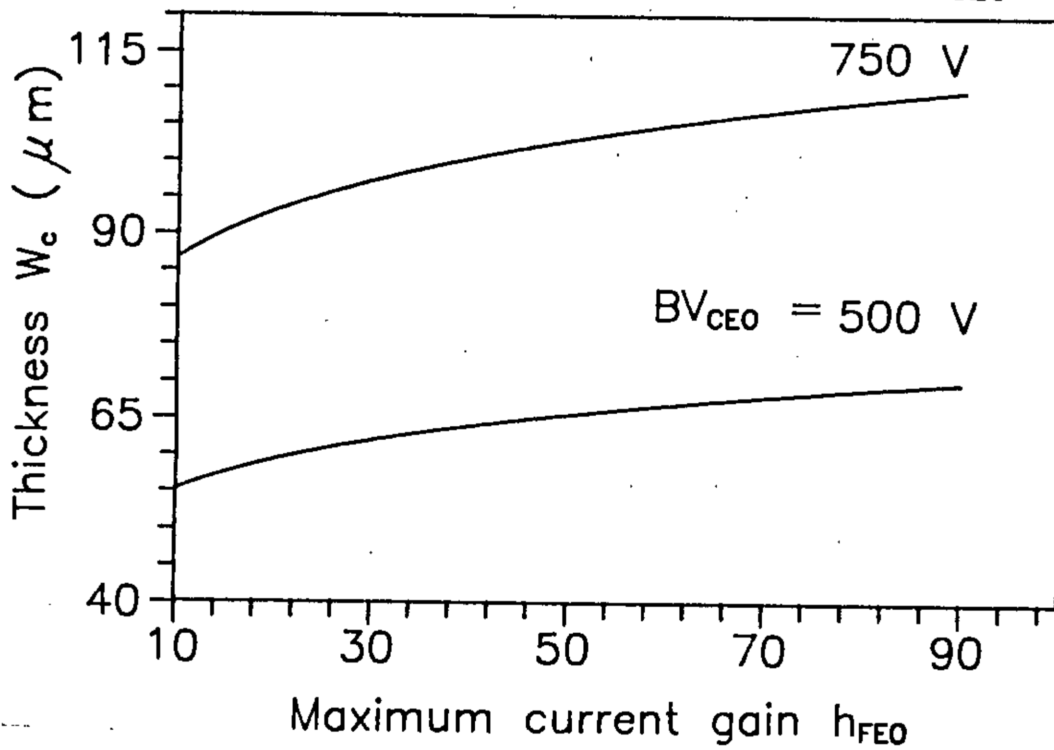

Fig. 5.2 Epitaxial layer thickness as a function of maximum current gain for different values of BV_{CEO}.

The expression is

$$h_{FE} = \frac{\frac{Q_E}{D_E}}{Q_B/D_B + \frac{I_c W_c^2}{4qD_B D_c A_e} + \frac{qA_e(\mu_n N_c V_{CB})^2}{4I_c D_B D_c} - \frac{V_{CB}}{2kT/q}\frac{N_c W_C}{D_B}} \quad (5.3)$$

where D_C (D_B) $= \mu_n KT/q$, is the diffusion co-efficient of electron in the collector (Base), μ_n is the mobility of electrons, I_C is the collector current, V_{CB} is the collector-base voltage and A_e is the effective emitter area. In the above derivation, the lifetimes in the base and collector are assumed to be large enough to permit the assumption of unity base transport factor. Also at the onset of base widening, the low-field approximation $I_O = q\mu_n N_C A_e V_{CB}/W_C$ for $V_{CB}/W_C < 3\times10^3$ V/cm is used for the critical current [9]. In absence of base widening, i.e. for $I_C < I_O$, all the terms except the first one (Q_B/D_B) in the denominator will be zero. For this case equation (5.3) becomes

$$h_{FEO} = \frac{Q_E/D_E}{Q_B/D_B} \quad (5.4)$$

For the case of zero bulk recombination and infinite velocity at the emitter contact, Q_E is simply the integral of emitter impurity density over the emitter width [8]. The value of Q_E/D_E is 4×10^{13} $cm^{-4}S$ for a wide range of emitter and base diffusion processes [7].

In the present analysis Q_E/D_E is assumed constant at this value.

The denominator of equation (5.3) contains the device variables Q_B, N_C and W_C, while Q_E/D_E appears only in the numerator . From the design point of view, it is desirable to have the model based on quantities that can be easily determined from simple measurements. The agreement between measured and theoretical values for h_{FE} calculated from equation (5.3) is quite satisfactory [7]. In this work, equation (5.3) is used to determine transistor parameters. Since V_{CE} is usually given, the collector-base voltage V_{CB} in equation (5.3) can be replaced by

$$V_{CB} = V_{CE} - V_{BE} \qquad (5.5)$$

In this work a fixed value for V_{BE} equal to 0.7V is used.

5.3 Optimum Emitter Area for Given BV_{CEO}, I_C and h_{FE}

For a given BV_{CEO}, I_C and h_{FE}, the parameter A_e can be calculated for any h_{FEO} from equations (5.1), (5.2), (5.3) and (5.4). With the help of equation (5.4), equation (5.3) can be

written as

$$A A_e^2 - B A_e + C = 0 \qquad (5.6)$$

where $A = (q D_C N_C V_{CB}/R)^2$ (5.7)

$$B = 4qD_B D_c I_c [4 \times 10^{13} \left(\frac{1}{h_{FE}} - \frac{1}{h_{FEO}} \right) + \frac{N_c W_c V_{CB}}{2RD_B}] \qquad (5.8)$$

$$C = W_C^2 \, I_C^2 \qquad (5.9)$$

$$R = 2K\,T/q$$

Now the above quadratic equation (5.6) can be solved for A_e with the help of equation (5.1) and (5.2) for any h_{FEO}. Fig. 5.3 shows A_e as a function of h_{FEO}. A_e goes through a minimum, giving a value of h_{FEO} that corresponds to the optimized value of A_e. For this particular value of A_e, the optimized values of N_C and W_C can be found from eqns (5.1) and (5.2). The collector doping density N_C as a function of h_{FEO} is shown in Fig. 5.1, while W_C is plotted as a function of h_{FEO} in Fig. 5.2. N_C decreases with increase of h_{FEO}, but W_C shows the opposite trend. Increasing h_{FEO} will increase W_C from the BV_{CEO} requirement, whereas an increase of W_C will decrease N_C for the same reason to meet the BV_{CEO} requirement. For each h_{FEO}, equation (5.1) and (5.2) give the optimized values of N_C and W_C

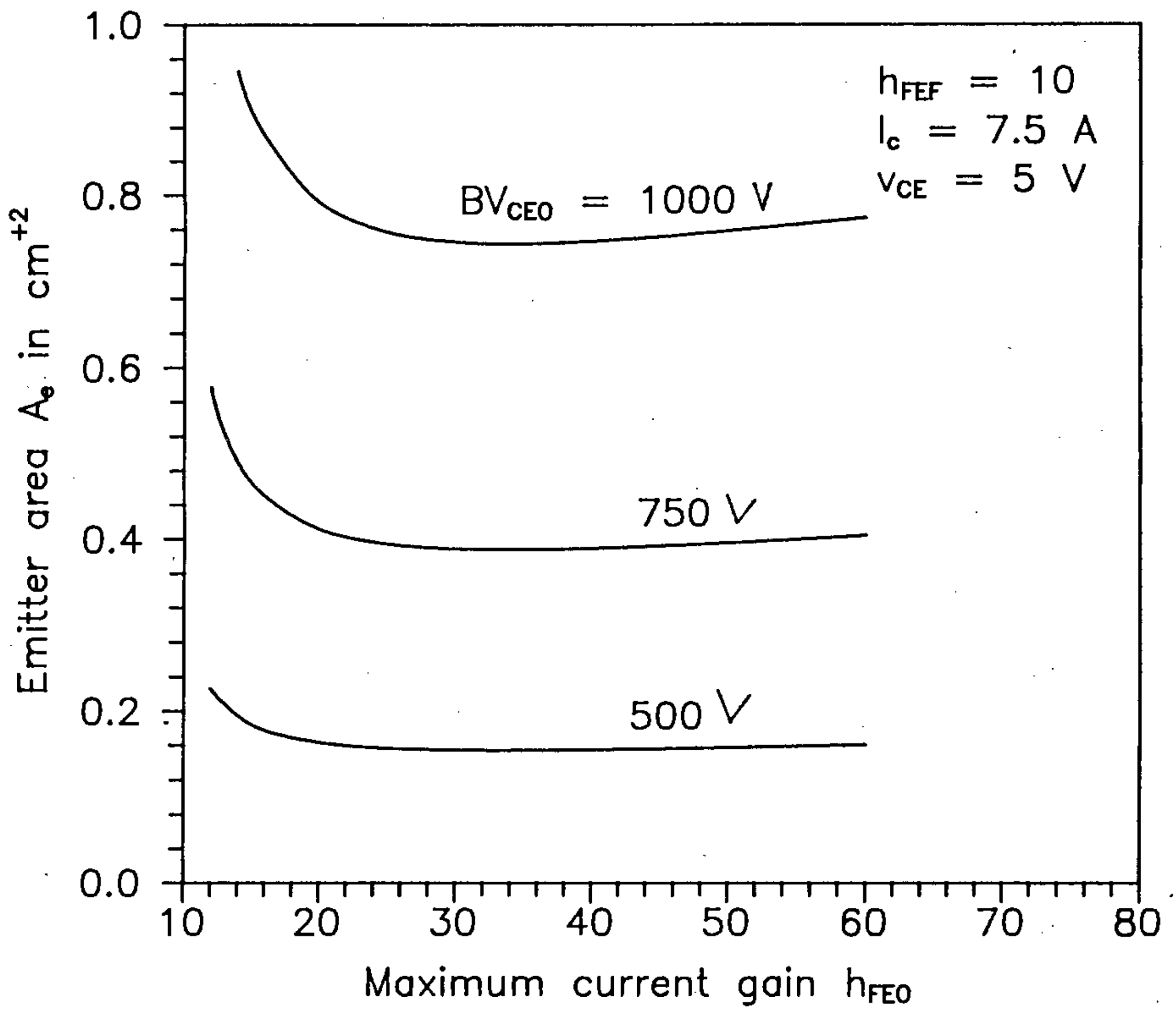

Fig. 5.3 Emitter area versus maximum current gain for different values of collector-emitter breakdown voltage.

at the given sustaining voltage BV_{CEO}. Therefore, the value of h_{FEO} which gives minimum A_e for a given I_C, h_{FE} and BV_{CEO}, also gives the optimized values of N_C and W_C at the desired BV_{CEO}.

5.4 Maximum Collector Current for given A_e, h_{FE} and BV_{CEO}

For maximum current solution, the emitter area A_e, h_{FE}, V_{CE} and BV_{CEO} are given. Equation (5.3) of section 5.2.2 can be written as a quadratic equation of I_C as follows:

$$A\ I_C^2 - B\ I_C + C = 0 \qquad (5.10)$$

where

$$A = W_C^2 \qquad (5.11)$$

$$B = 4qD_cA_e[N_cW_cV_{CB}/R + 4\times 10^{13}D_B\left(\frac{1}{h_{FE}} - \frac{1}{h_{FEO}}\right)] \qquad (5.12)$$

$$C = (2qA_eN_DV_{CB}D_C/R)^2 \qquad (5.13)$$

$$R = 2KT/q$$

Now equation (5.10) can be solved for I_C with fixed BV_{CEO} and different h_{FEO}. Plots of I_C Vs h_{FEO} for BV_{CEO} = 500 V, 750 V and 1000 V are given in Fig. 5.4. From the plots it is seen that the collector current goes through a relative maximum as the device variables, which can be related to the peak value of current gain h_{FEO}, cause h_{FEO} to be increased from the specified value of h_{FE} to larger values.

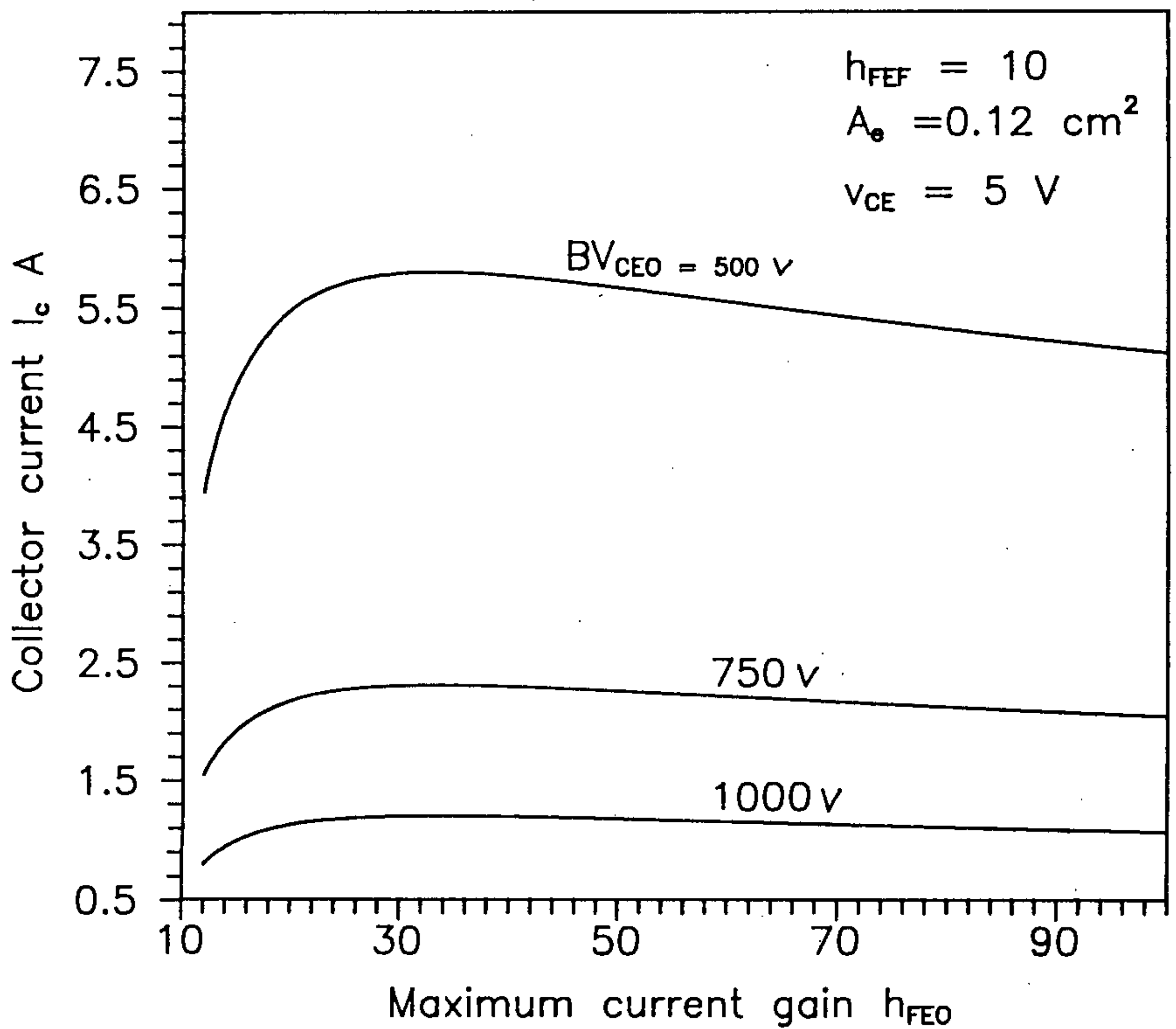

Fig. 5.4 Collector current as a function of h_{FEO} for different values of collector-emitter breakdown voltage with given emitter area.

5.5 Optimum Emitter Area as a Function of BV_{CEO} for Given Input Power

The optimum A_e can be easily calculated as a function of BV_{CEO} with constant power I_cBV_{CEO} with the help of equation (5.3) of section 5.2.2. For the optimum solution it turns out that the term containing $I_cW_c^2$ in the denominator of equation (5.3) is dominant and the product increases approximately in proportion to $BV_{CEO}^{2.22}$. W_c^2 is strongly dependent on BV_{CEO} and less sensitive to h_{FEO} (equation (5.2)). For constant I_cBV_{CEO} product, $I_cW_c^2$ increases with increase of BV_{CEO} even though I_c is decreasing .To determine A_e as a function of BV_{CEO} we first find optimum A_e as a function of h_{FEO} for fixed BV_{CEO} and power using equation(5.1), (5.2) (5.3) and (5.4) and the relation $I_c=P/BV_{CEO}$. Fig. 5.5 shows A_e as a function of BV_{CEO} for two different values of the I_cBV_{CEO} product. Computed results show that A_e is approximately proportional to $BV_{CEO}^{1.24}$.

5.6 Maximum Current Density Vs. Open Base Breakdown Voltage

The question that often arises is - how large does a device have to be if it turn on a certain collector current at a particular h_{FE} and block a certain voltage in the "off" state. This question can be answered by plotting I_c/A_e as a function of

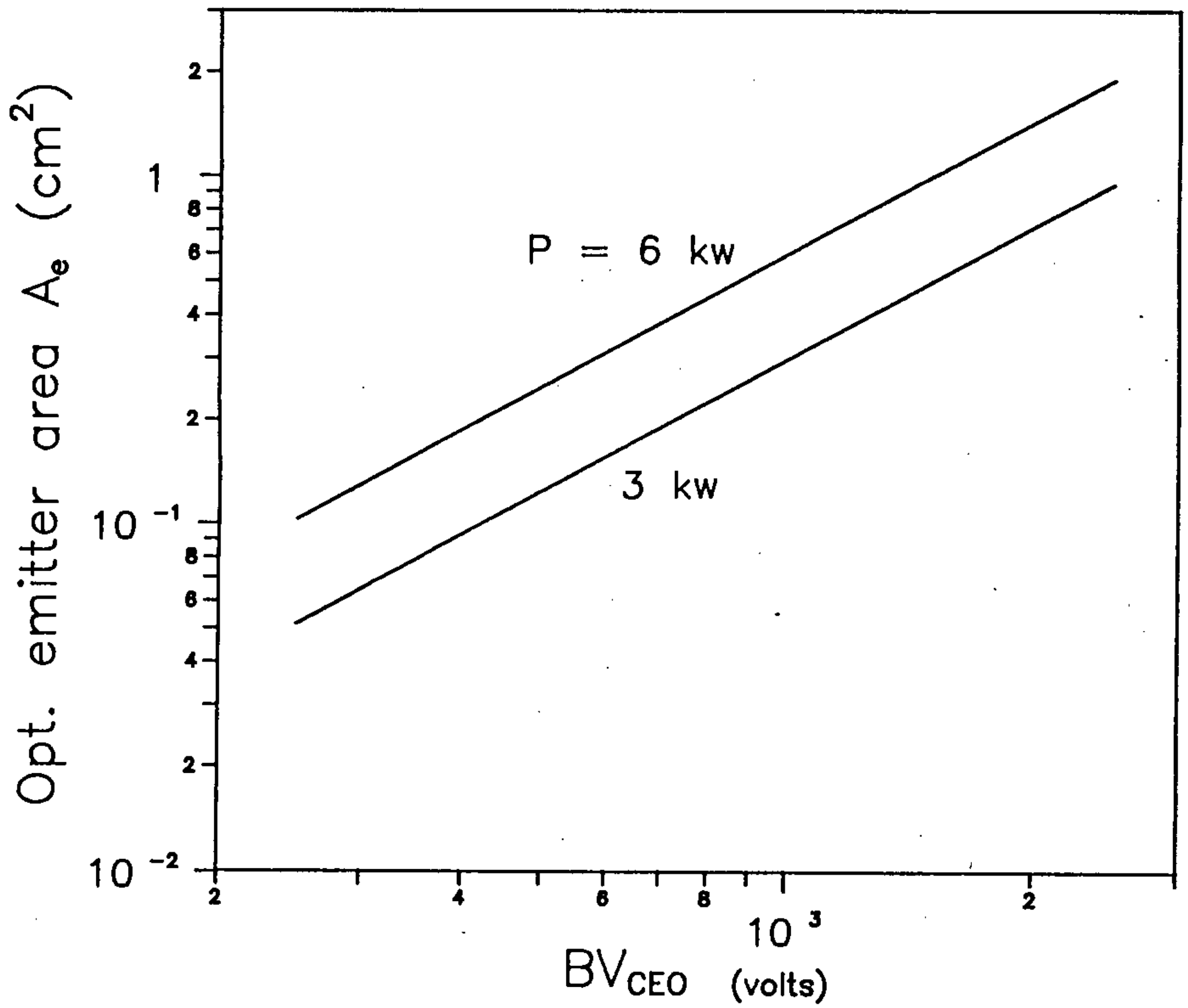

Fig. 5.5 Optimum emitter area as a function of collector-emitter breakdown voltage for different values of input power.

BV_{CEO} for different values of h_{FE}. The calculation is carried out for the case h_{FE} = 5, 10 and 15 the result is shown in Fig. 5.6.

This figure also shows that the current density falls off quite steeply as BV_{CEO} increases. This means that for a given $I_C BV_{CEO}$ product, the device will become more expensive as BV_{CEO} increases, simply because large values of A_e will be required to handle the same volt-ampere product.

The curves of Fig.5.6 can be used for values of h_{FE} other then h_{FE} = 5,10 and 15. For example, if BV_{CEO}=750 V and V_{CE} = 5V, the maximum I_C/A_e is 19.32 A/cm^2 with h_{FE}=10. If h_{FE} is reduced to, say to h_{FE}=5, then I_C/A_e will increase to 36.708

5.7 Comparison of the Results with Numerical Data

The optimal parameters obtained by this model for a given collector current are compared with numerical data and are found in good agreement. The results are tabulated in Table 5.1.

Also the results for a fixed emitter area are compared with numerical data and the comparison is shown in Table 5.2.

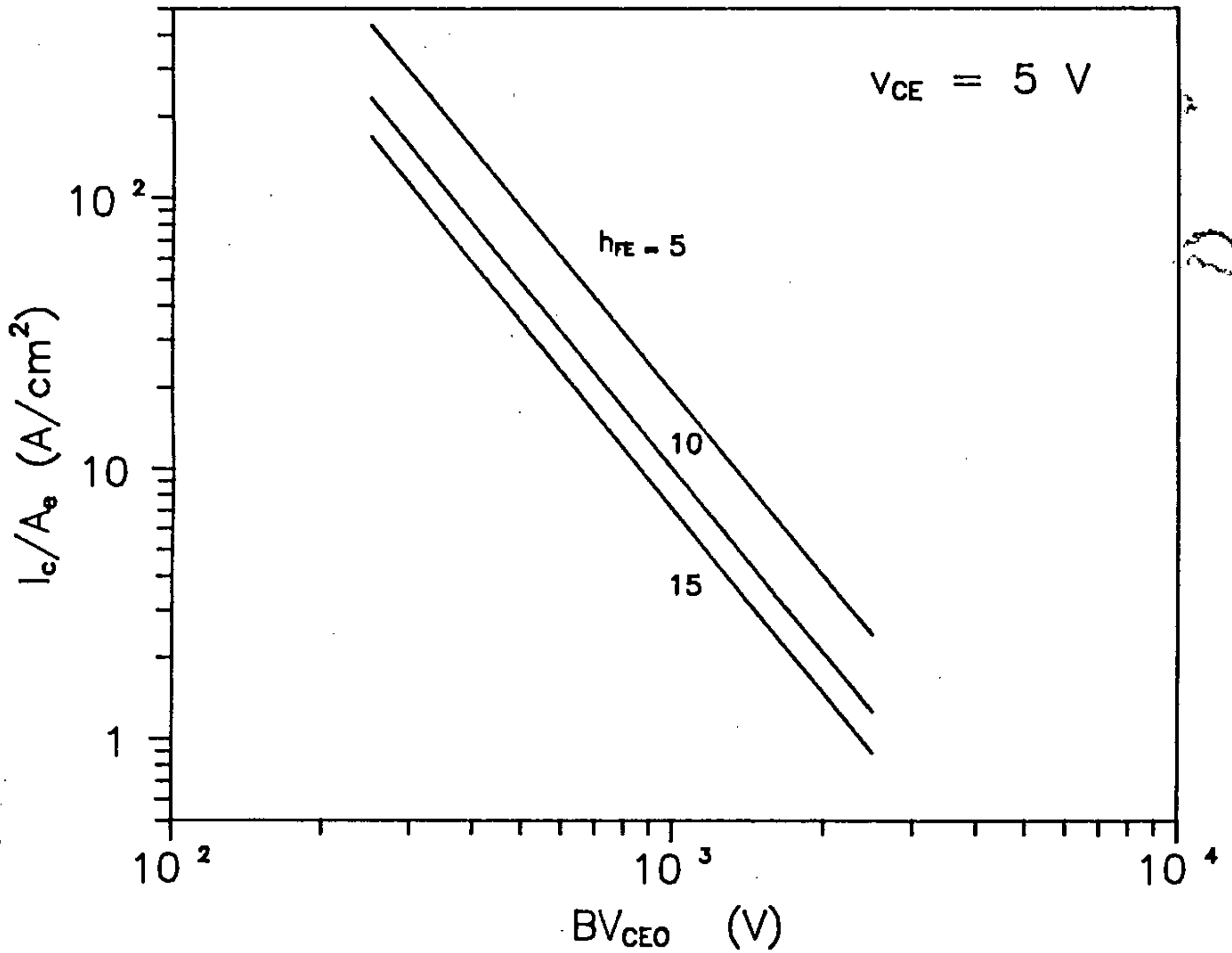

Fig. 5.6 Maximum controllable current density vs collector-emitter breakdown voltage for different values of h_{FE}.

Input data			*Optimum design results*			
constant	value	units	quantity	value [7]	value	units
B_1	1.0	–	A_e	0.0665	0.0666	cm^2
m_1	0.217	–	h_{FEO}	18	18	- -
B	2.694×10^{14}	$V^{4/5}cm^{-12/5}$	Q_B	4.7×10^{13}	4.7×10^{13}	cm^{-2}
m_2	0.8004	- -	N_C	2×10^{14}	2.2×10^{14}	cm^{-3}
Q_E/D_E	4×10^{13}	$cm^{-4} - sec$	W_C	41	44	μm
D_B	20	cm/sec	BV_{CBO}	760	760	V
Specifications						
h_{FE}	10.	–				
I_C	7.5	A				
V_{CE}	5.0	V				
BV_{CEO}	400	V				

Table 5.1. Optimized design parameters of a switch for a given collector current.

Input data(constants are same as in Table5.1)			*Optimum design results*			
Specifications						
constant	value	units	quantity	value[7]	value	units
A_e	0.12	cm^2	I_c	13.5	13.1	A
h_{FE}	10	–	h_{FEO}	20	19.5	–
V_{CE}	5	V	Q_B	4×10^{13}	4.1×10^{13}	cm^{-2}
B_{CEO}	400	V	N_D	2×10^{14}	2.5×10^{14}	cm^{-3}
			W_C	42	44.5	μm

Table 5.2. Optimized design parameters of a switch for a fixed emitter area.

5.8 Conclusions

The model presented in this work for designing power transistors is for a particular class of transistors, namely those with uniformly doped collectors. The method outlined here is found to be of considerable practical value in the design of high-voltage power switches. The model is simple and needs less computations for estimation of optimal values of different parameters of the device. In this work the procedure for designing a power transistor for optimum emitter area A_e with given BV_{CEO}, I_C and h_{FE} is shown and a design procedure for optimum collector current I_C with given BV_{CEO}, h_{FE} and A_e is also shown. Analysis also shows that an increase in the device area is the obvious choice for the achievement of higher power-handling capabilities.

CHAPTER 6

Conclusions

Although a truely comprehensive bipolar design theory is still not a reality, it is now possible to design devices "on paper" to meet the more important characteristics of high-voltage switching transistors. In this thesis an analytical model is developed for epitaxial bipolar transistor switches, where optimal calculations have been carried out for structural parameters which make it possible to comply in the best possible way with given specifications. The present model is simple and needs less computations.

Many effects of lesser importance have been ignored(among them the impurity mobility reduction by carrier-carrier scattering at high injection levels) and approximations have been tolarated in order to make the calculations easier. The effects of storage time and the current crowding are not included in this design model. By adding these effects with the present model an extended form of this model can be developed in future.

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c     Appendix   A
C
C     THIS COMPUTER PROGRAMME IS USED FOR SOLVING THE IONIZATION
C     INTEGRAL (EQUATION NO. 2.5).
C
C     THIS PROGRAM HAS BEEN DEVELOPED BY MASHIUR RAHMAN
C
      IMPLICIT REAL*8(A-H,O-Z)
      DIMENSION ATEMP(50)
      COMMON/blk/ XEM,XNO,XW
      Q=1.6D-19
      EPS=1.045D-12
      ERS=1.0D-04
      write(*,*) ' xno='
      read(*,*) xno
      write(*,*) 'xem='
      read(*,*) xem
   60 A=0.0
      I=1
      XW=(XEM*EPS)/(Q*XNO)
      VB=0.5*XEM*XW
      B=XW
      H=B-A
      ATEMP(1)=0.5*(F(A)+F(B))
```

```
      ZL=H
      POWER=1.0
      JJ=1
70    I=I+1
      ANS=ATEMP(1)
      TEMPL=ZL
      ZL=0.5*ZL
      POWER=0.5*POWER
      X=A+ZL
      SUM=0.0
      DO 10 JCOUNT=1,JJ
      SUM=SUM+F(X)
10    X=X+TEMPL
      ATEMP(I)=0.5*ATEMP(I-1)+SUM*POWER
      N=I
      R=1.0
      NM1=N-1
      DO 15 KOUNT=1,NM1
      KK=N-KOUNT
      R=R+R
      R=R+R
      ATEMP(KK)=ATEMP(KK+1)+(ATEMP(KK+1)-ATEMP(KK))/(R-1.0)
 15   CONTINUE
      DELTA=ABS((ATEMP(1)/ANS)-1.0)
      IF(DELTA-ERS) 40,40,30
```

```
   30  JJ=JJ+JJ
       GO TO 70
   40  ANS=ATEMP(1)*H
       write(*,*) 'ans = ',ans
  100  WRITE(*,*) 'ANS = ',ANS,'XEM = ',XEM,' XNO = ',XNO,'XW=',XW
       write(*,*) 'vb=', vb
       STOP
       END
C
       FUNCTION F(X)
       IMPLICIT REAL*8(A-H,O-Z)
       COMMON/blk/ XEM,XNO,XW
       AP=1.582D+06
       BP=2.036D+06
       Q =1.600D-19
       EPS=1.045D-12
       AA=XEM-Q*XNO*X/EPS
       IF(AA.LE.0.5D+05)THEN
       F=0.0
       ELSE
       BETAN=AP*EXP(-BP/AA)
       F=BETAN*G(X)
       ENDIF
       RETURN
       END
```

```
      FUNCTION G(X)
      IMPLICIT REAL*8(A-H,O-Z)
      G=EXP(-T(X))
      RETURN
      END
C
      FUNCTION T(X)
      IMPLICIT REAL*8(A-H,O-Z)
      DIMENSION TERM(30)
      COMMON/blk/ XEM,XNO,XW
      ERS = 1.d-04
      A=X
      II=1
      B=XW
      H=B-A
      TERM(1)=0.5*(S(A)+S(B))
      ZL=H
      POWER=1.0
      J=1
 170  II=II+1
      AWR=TERM(1)
      TEMPL=ZL
      ZL=0.5*ZL
      POWER=0.5*POWER
      Y=A+ZL
```

```
      SUM=0.0
      DO 12 JCNT=1,J
      SUM=SUM+S(Y)
 12   Y=Y+TEMPL
      TERM(II)=0.5*TERM(II-1)+SUM*POWER
      NN=II
      RP=1.0
      NM2=NN-1
      DO 14 KNT=1,NM2
      K=NN-KNT
      RP=RP+RP
      RP=RP+RP
      TERM(K)=TERM(K+1)+(TERM(K+1)-TERM(K))/(RP-1.0)
 14   CONTINUE
      DEL=ABS((TERM(1)/AWR)-1.0)
      if(del-ers) 62,62,66
 66   J=J+J
      go to 170
 62   T=TERM(1)*H
      RETURN
      END
C
C
C
C
```

```
C
      FUNCTION S(Y)
      IMPLICIT REAL*8(A-H,O-Z)
      COMMON/blk/ XEM,XNO,XW
      AP=1.582D+06
      AN=7.03D+05
      BP=2.036D+06
      BN=1.231d+06
      Q=1.6D-19
      EPS=1.045D-12
      BB=XEM-Q*XNO*Y/EPS
      IF(BB.LE.0.5D+05) THEN
      S=0.0
      ELSE
      PETA=AP*EXP(-BP/BB)
      BETA=AN*EXP(-BN/BB)
      SUBT=PETA-BETA
      S=SUBT
      ENDIF
      RETURN
      END

C     END OF THE PROGRAM
```

```
C       Appendix  B

c        THIS PROGRAM CALCULATES THE EMITTER AREA FOR DIFFERENT
C        VALUES OF CURRENT GAIN UNDER SATURATION CONDITION
C
C       PROGRAM STARTS HERE
C
        IMPLICIT REAL*8(A-H,O-Z)
        XM1 = 0.183
        XM2 = 0.82
        XK1 =4.076D17
        Q = 1.6D-19
        XK2 = 4.276D-6
        HFEF = 10.
        XIC = 7.5
C       FOR VCE = 5.0V, VCB=5-.7=4.3V
        VCB =4.3
        X1 =-XM1/XM2
        X2 = -1./XM2
        X3 = XM1/(2.*XM2)
        X4 = (XM2+1.)/(2.*XM2)
        WRITE(*,*) 'HFEO= '
        READ(*,*) HFEO
        WRITE(*,*) 'BVCEO= '
        READ(*,*) BVCEO
```

```
      XND = XK1*((1+HFEO)**X1)*BVCEO**X2
      WC = XK2*((1. + HFEO)**X3)*BVCEO**X4
C     KT/Q=0.0259,D/MU=.0259
      A = (Q**2)*(30./0.0259*XND*VCB)**2
C
      B=Q*30.*XIC*((77.22*XND*VCB*WC)+32.D14*(HFEO-HFEF)/(HFEO*HFEF))
C
      C = (WC**2)*(XIC**2)
      D =(B**2)-4*A*C
      IF(D) 20,30,40
 20   WRITE(*,*) 'ROOTS ARE IMMAGINARY'
      GO TO 50
 30   AE = B/(2*A)
      WRITE(*,*) 'AE = ',AE
      GO TO 50
  40  Y = SQRT(D)
      AE1 = B/(2.*A)+Y/(2.*A)
      AE2 =B/(2.*A)-Y/(2.*A)
      WRITE(*,*) 'AE1 = ',AE1,'AE2 =',AE2
  50  STOP
      END

C     END OF PROGRAM
```

```
c       Appendix  C
c
c        CALCULATION OF MAXIMUM COLLECTOR CURRENT FOR DIFFERENT
         VALUES OF CURRENT GAIN UNDER SATURATION CONDITION
C
C
        IMPLICIT REAL*8(A-H,O-Z)
        DC=30.0
        RT=2.*0.0259
        BK=1./RT
        DB=20.0
        PE= 4.0D13
        XM1 = 0.183
        XM2 = 0.82
        XK1 =4.076D17
        Q = 1.6D-19
        XK2 = 4.276D-6
        HFEF = 10.
C
C       FOR VCE = 5.0V, VCB=5-.7=4.3V
        VCB =4.3
        X1 =-XM1/XM2
        X2 = -1./XM2
        X3 = XM1/(2.*XM2)
        X4 = (XM2+1.)/(2.*XM2)
```

```
      WRITE(*,*) 'HFEO= '
      READ(*,*) HFEO
      WRITE(*,*) 'BVCEO= '
      READ(*,*) BVCEO
      WRITE(*,*) 'AE= '
      READ(*,*) AE
C
      XND = XK1*((1+HFEO)**X1)*BVCEO**X2
      WC = XK2*((1. + HFEO)**X3)*BVCEO**X4
C
C     KT/Q=0.0259,D/MU=.0259
      A = WC**2.
C
      B=4*Q*DC*AE*(BK*XND*WC*VCB+DB*PE*(HFEO-HFEF)/(HFEO*HFEF))
C
      C = (2*Q*AE*XND*VCB*DC*BK)**2
      D =(B**2)-4*A*C
      IF(D) 20,30,40
 20   WRITE(*,*) 'ROOTS ARE IMMAGINARY'
      GO TO 50
 30   XIC= B/(2*A)
      WRITE(*,*) 'IC= ',XIC
      GO TO 50
  40  Y = SQRT(D)
C
```

```
      XIC1= B/(2.*A)+Y/(2.*A)
      XIC2=B/(2.*A)-Y/(2.*A)
      WRITE(*,*) 'IC1 = ',XIC1,'IC2=',XIC2
   50 STOP
      END
C
C     END OF THE PROGRAM
```

```
C       Appendix  D
c
c       CALCULATION OF OPTIMUM EMITTER AREA AS A FUNCTION OF
C       COLLECTOR-EMITTER BREAKDOWN VOLTAGE FOR DIFFERENT VALUES
C       OF INPUT POWER UNDER SATURATION CONDITION.
C
        IMPLICIT REAL*8(A-H,O-Z)
        XM1 = 0.183
        XM2 = 0.82
        XK1 =4.076D17
        Q = 1.6D-19
        XK2 = 4.276D-6
        HFEF = 10.
C       XIC = 7.5
C       FOR VCE = 5.0V, VCB=5-.7=4.3V
        VCB =4.3
        X1 =-XM1/XM2
        X2 = -1./XM2
        X3 = XM1/(2.*XM2)
        X4 = (XM2+1.)/(2.*XM2)
        WRITE(*,*) 'HFEO= '
        READ(*,*) HFEO
        WRITE(*,*) 'BVCEO= '
        READ(*,*) BVCEO
        WRITE(*,*) 'POW='
```

```
      READ(*,*) POW
      XIC=POW/BVCEO
      XND = XK1*((1+HFEO)**X1)*BVCEO**X2
      WC = XK2*((1. + HFEO)**X3)*BVCEO**X4
C     KT/Q=0.0259,D/MU=.0259
      A = (Q**2)*(30./0.0259*XND*VCB)**2
C
      B=Q*30.*XIC*((77.22*XND*VCB*WC)+32.D14*(HFEO-HFEF)/(HFEO*HFEF))
C
      C = (WC**2)*(XIC**2)
      D =(B**2)-4*A*C
      IF(D) 20,30,40
 20   WRITE(*,*) 'ROOTS ARE IMMAGINARY'
      GO TO 50
 30   AE = B/(2*A)
      WRITE(*,*) 'AE = ',AE
      GO TO 50
 40   Y = SQRT(D)
      AE1 = B/(2.*A)+Y/(2.*A)
      AE2 =B/(2.*A)-Y/(2.*A)
      WRITE(*,*) 'AE1 = ',AE1,'AE2 =',AE2
 50   STOP
      END
C
C     END OF THE PROGRAM
```