DESIGN OF A CMOS RF WIDE BAND FREQUENCY SYNTHESIZER

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In Partial Fulfillment of the Requirement

For the Degree of

MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

by

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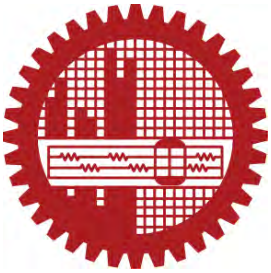

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The thesis titled **"DESIGN OF A CMOS RF WIDE BAND FREQUENCY SYNTHESIZER"** submitted by Abdullah Ibn Abbas, Student ID.: 0413062287 F, Session: April 2013 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on November 29, 2014.

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I, Abdullah Ibn Abbas, hereby declare that the thesis entitled "DESIGN OF A CMOS RF WIDE BAND FREQUENCY SYNTHESIZER" and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research and has not been submitted for higher degree to any other university or institution. I confirm that:

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- I have acknowledged all main sources of help.

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Dedication

To my Parents and Teachers

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Acknowledgment

All praises, prayers, glory, and gratitude belong to almighty Allah who is the gracious and the ever merciful.

This thesis is the outcome of the support from my beloved parents and teachers who encouraged me to carry out this work.

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I am thankful to my parents and sisters who are the ultimate source of my strength and the reason of my endeavor and without them I would not have achieved whatever I possess.

Abstract

The focus of this thesis is to design a silicon based RF frequency synthesizer in CMOS process that will generate frequency from the S band up to the X band (2 GHz -12 GHz). To achieve this target, an improved CMOS ring oscillator topology is proposed and is implemented in IBM 90nm RF CMOS process technology. The other building blocks of a frequency synthesizer, namely phase frequency detector (PFD), charge pump (CP), and divider circuits were also designed and implemented successfully to achieve the target. The proposed VCO can generate frequency from 2.51 GHz to 12.68 GHz with almost constant gain (Kvco) and low phase noise within the operating range. The performance of PFD has been boost up with proposed technique and an innovative idea in the design of CP has reduced the glitches in the charging and discharging current of the loop filter.

Each block of the proposed Phase-Locked Loop based Frequency Synthesizer is designed using Cadence Electronic Design Automation tools in IBM 90nm CMOS process technology. Virtuoso Schematic Editor tool is used for schematic design and all the simulation results are plotted in Cadence Spectre. Virtuoso Layout Editor (XL) tool is used for physical layout design whereas Assura DRC, LVS, and QRC tools are used for physical verification.

Simulation results are provided for the performance of VCO, PFD, CP and the PLL. Post-layout simulation including the parasitic is also provided to verify the functionality of the proposed circuit. Pre and post layout simulation results are compared and it is found that they meet our target and specification.

Finally, the results obtained for the designed circuits are compared with the literature works and is found that our proposed circuits are better in most of the performance parameters than those reported in literature works.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Over the last two decades, the continuous shrinking in the feature of MOSFETs has increasingly attracted the research and development of low-power radio frequency CMOS integrated circuits [1],[2]. For the modern transceiver architecture, a fully integrated frequency synthesizer with high frequency and low power voltage controlled oscillator (VCO) is always a topic of interest in research.

Phase-locked loops (PLLs) are widely used in radio frequency synthesis. The PLL based frequency synthesizer is one of the key building blocks of an RF front-end transceiver.

Fundamentally, no matter whether designed for digital or analog applications, a frequency synthesizer must ensure the devices are working at their designed operational speed. Furthermore, the frequency synthesizer requires their frequency to be tunable over a range of frequency bands. This requires the use of a voltage controlled oscillator (VCO) and the controllability requirement demands the utilization of the PLL. VCO is an integrated part of a frequency synthesizer. Recently, several CMOS voltage-controlled oscillators operating above 50 GHz have been demonstrated [3]-[5]. The existing phase-locked loops operating at frequencies above 50 GHz are usually based on III-V [6],[7] or SiGe HBT technologies [8]. Operating frequency around 12 GHz in silicon based CMOS process has not been reported till the present work.

Ring oscillator based voltage-controlled oscillators are attractive in terms of small area and frequency tuning range. Furthermore, they have the particularly desirable property that inductors can be dispensed with altogether, which makes ring-VCOs highly scalable. Unfortunately, their phase-noise performance is inferior to that of LC-VCOs with comparable power consumption. Nevertheless, a low-phase-noise ring VCO can be obtained if a noise-suppression mechanism can be included in the VCO.

Since its invention, the design of PLL has remained challenging because of the requirement of fast, low power consuming and less noisy electronic equipment. “Charge Pump” is an essential part of a PLL. Charge pump (CP) converts the phase or frequency difference information of two input signal into a voltage which is used to tune a VCO towards reference input frequency. Other elements of PLL are “Phase Frequency Detector (PFD)”, “Low Pass Filter (LPF)” and “VCO”. Implementation of LPF is very easy while PFD and VCO can be implemented in static CMOS logic. But being a current driven system, charge pump is found to be more challenging for implementation, since performance of CP directly affects the speed, power consumption and noise behaviour of PLL. Clock feed through, charge sharing, current mismatch are some of the challenges in design of CP.

1.2 Literature Review

The recent trend in the design of high frequency PLL based frequency synthesizer is to use LC oscillators [9] because of its low phase noise characteristics. These LC oscillator based frequency synthesizers on the other hand have narrow tuning range as compared to those frequency synthesizers which uses ring oscillators. Ring oscillators can be built in any standard CMOS process and may require less die area than LC designs. The design is straightforward, and ring architectures can be used to provide multiple output phases and wide tuning ranges. The literature works that uses sub-micron process technology fails to present ring oscillators that operate above 8 GHz and with a wide tuning range. Some literature works show that up to 6 GHz [10],[11] operating frequency have been achieved in recent technology process (0.18μm, 90nm etc.) but these technology are based on GaAs or SiGe HBT etc. but not silicon based CMOS process technology. A constant gain voltage-controlled oscillator within the full range of operating frequency has not been reported till date. Therefore, it is needed to design a wide tuning range ring oscillator that can operate at very high frequency for gigahertz application is needed to design in cheap silicon technology and which can have constant gain within the operating range. To design a frequency synthesizer which can operate at such a high frequency requires a phase frequency detector [12]-[14] which can stand this high frequency operation. The design of frequency synthesizer presented in this work can be successfully implemented in the area where on-chip high frequency and wide tuning range is desired.

1.3 Outline of the Thesis

This thesis consists of five chapters. Chapter 1 introduces the topic and the present state of the work.

Chapter 2 briefly describes the basics of PLL.

Chapter 3 builds the concepts of charge pump PLL and in the subsequent sections the building blocks of a PLL are discussed in brief.

The designed RF wide band frequency synthesizer is proposed in chapter 4. The proposed modified fast operating PFD with glitch suppressed and current matched CP is presented in section 4.1 and section 4.2. These sections also contain the simulation and verification results in addition to the layout drawn to estimate the area budget. The post simulation results are also provided to estimate the real performance of the circuit. The proposed VCO with improved topology is presented in section 4.3. Different properties of the VCO simulated are also shown along with the layout of the design and post layout simulated results. Finally, in section 4.4, the divider circuit designed to show the desired operation of the proposed RF frequency synthesizer is presented.

Chapter 5 concludes the thesis work highlighting the outcome of the proposed design and the future work on this topic to make the work more concrete.

CHAPTER 2

PHASE LOCKED LOOP FREQUENCY SYNTHESIZERS

In this Chapter, the fundamentals of frequency synthesizers are discussed. First we define the PLL frequency synthesizer. We then discuss the theory behind the phase locked loops (PLL) and the integer-N charge pump frequency synthesizer based PLL. Subsequently, all the building blocks of the frequency synthesizer such as phase frequency detector (PFD), charge pump (CP), Voltage controlled oscillator (VCO), divider and loop filter (LF) are discussed.

2.1 Basics of phase-locked loops (PLL)

A simple Phase Locked Loop (PLL) is a feedback system [15],[16] that compares the frequency and phase of the reference signal with that of the feedback signal coming from its output. The comparison is performed by a Phase Frequency Detector (PFD) which produces a voltage proportional to the phase difference. The output frequency of the PLL is in turn proportional to the voltage generated by the PFD. The earliest description of a PLL was provided by H. de Bellescize in 1932 and from then onwards the basic PLL has remained nearly the same but its implementation in different technologies and for different applications continues to challenge designers. Fig. 2.1 shows the basic block diagram of a PLL. Phase-locked loops are widely used in the design of frequency synthesizers of RF transceivers.

Before going into the detailed discussion of PLL, we first discuss the concept of phase locking. Phase locking means the phase difference between the two signals is constant with time and almost negligible. This means that once the loop achieves the locking, there is no frequency difference between the two signals which are compared. By using a feedback loop, a constant phase difference of two periodic signals is ensured when the loop reaches its steady state.

2.1.1 Operation of phase-locked loop

Fig. 2.1 shows the basic block diagram of a simple phase-locked loop. A PLL is a feedback system which minimizes the phase difference between the reference input f_{ref} and the feedback signal f_{div}. Here, a phase detector (PD) generates a phase error whose DC value is proportional to the difference between the phases of the reference and feedback signals. The

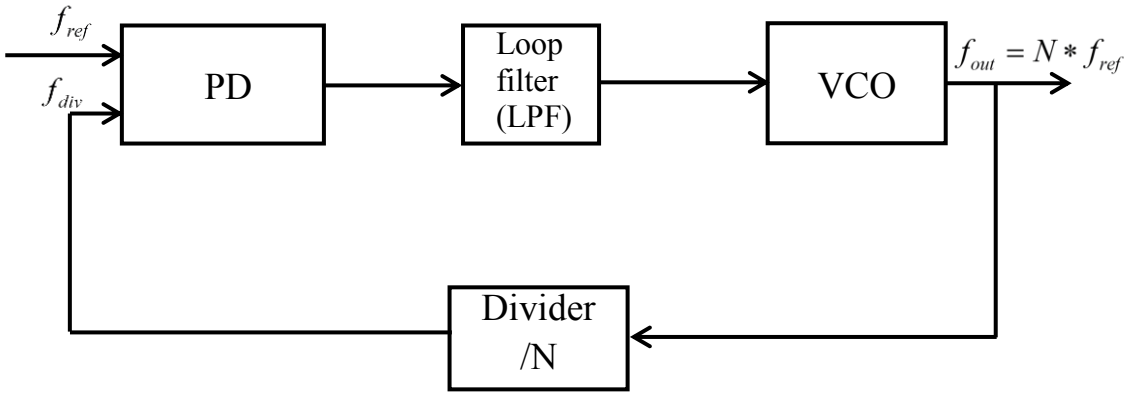


Fig. 2.1: Basic structure of a phase-locked loop

low pass filter (LPF) extracts the DC value and applies it to the voltage controlled oscillator (VCO), which changes the output frequency f_{out}. Since frequency synthesizer is required to produce a programmable output frequency, a frequency divider (FD) of programmable division ratio *N* is employed in the feedback path to divide down the VCO output frequency to the one comparable to the input reference frequency [17]-[19]. When the loop reaches steady state, the phase difference between the reference input f_{ref} and feedback signal f_{div} is constant over time and the relation $f_{out} = Nf_{ref}$ holds true. By changing the value of *N*, the VCO output frequency can be changed.

2.1.2 Terminology of PLL

1. Lock range:

The range of input signal frequencies over which the loop can maintain the lock is called as Lock Range or Tracking Range of PLL.

2. Capture range:

The range of input signal frequencies over which PLL can acquire a lock is called as Capture Range or Acquisition Range of PLL.

Capture range depends on the amount of the gain in a loop itself and the loop filter bandwidth. Reducing the loop filter bandwidth thus improves the rejection of the out of band signals, but at the same time the capture range decreases, pull in time becomes larger and phase margin becomes poor.

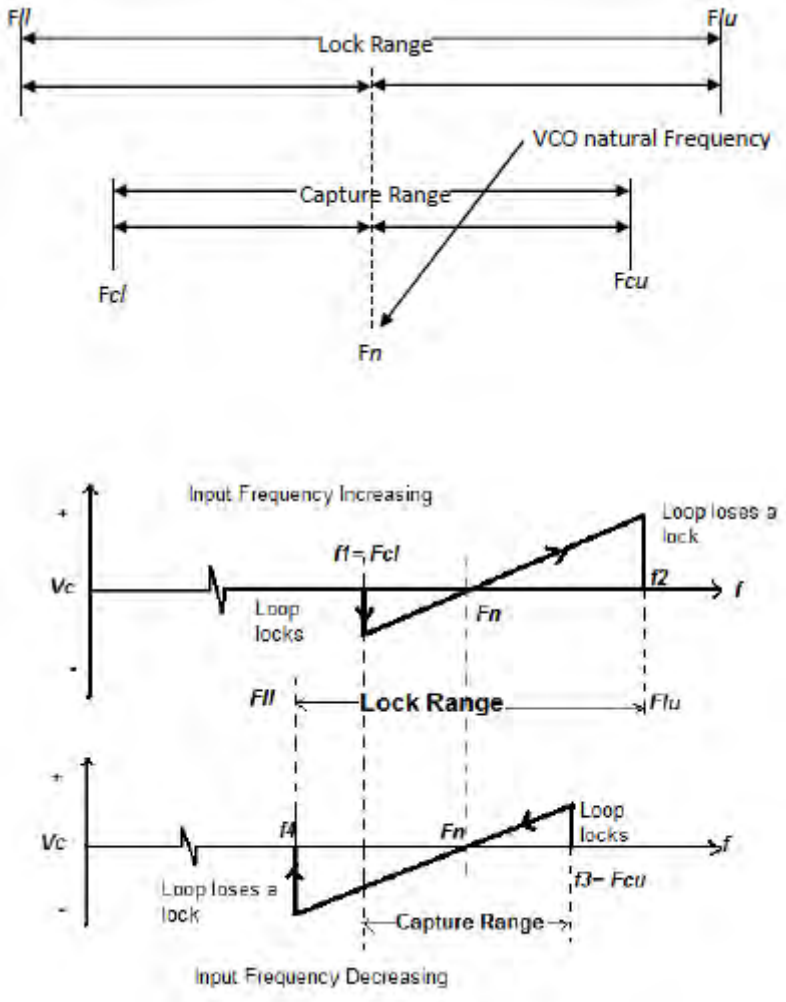


Fig. 2.2: Illustration of Terminologies of PLL

3. Pull in time:

The total time taken by the PLL to capture the signal (or to establish the lock) is called as Pull in Time of PLL. It is also called as Acquisition Time of PLL.

4. Band width of PLL

Bandwidth is the frequency at which the PLL begins to lose the lock with reference.

2.1.3 Dynamics of PLL

PLLs are classified according to the type of loop filter used in architecture. The order of loop filter is the type of PLL. For example, if 1st order loop filter is used, then it is called as type I PLL. If 2nd order filter is used, it is called as type II PLL and so on.

If PLL uses simple „Phase detector" in its architecture, it is called as simple PLL. But if PLL uses „Phase Frequency Detector" accompanied with „Charge Pump", it is called as "Charge Pump PLL".

2.1.3.a Dynamics of Type-I PLL

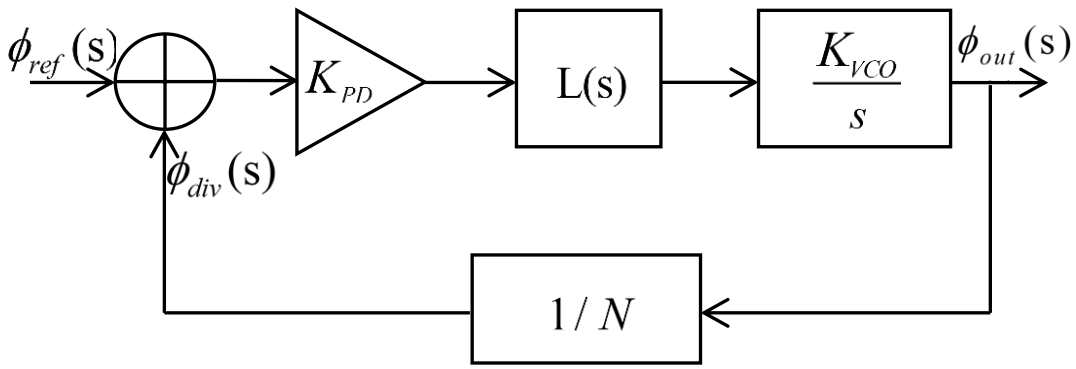


Fig. 2.3: Linear model of a type-I PLL

A simple PLL is analyzed by the phase transfer function as the PD compares the phase difference between the input $\phi_{ref}(s)$ and feedback signal $\phi_{div}(s)$. Fig.2.3 shows the linear model of a type-I PLL with the respective transfer functions of the building blocks. If the loop filter is a simple first order low pass filter (LPF), the transfer function is given by [19]

$$L(s) = \frac{1}{1 + s/\omega_{LPF}} \tag{2.1}$$

where ω_{LPF} denotes the -3 dB bandwidth. The open-loop transfer function is given by

$$H_o(s) = \frac{\phi_{out}}{\phi_{ref}}(s) = \frac{K_{PD}K_{VCO}}{N}\frac{1}{s(1+s/\omega_{LPF})} \tag{2.2}$$

Since open-loop transfer function contains only one pole at origin, this type of PLL is called type-I PLL. If the input phase varies slowly, owing to the pole at origin, the loop gain goes to infinity as *s* approaches zero. Thus, the PLL under locked condition ensures that the change in ϕ_{out} is exactly equal to the change in ϕ_{ref} as *s* goes to zero. The closed-loop transfer function is written as

$$H_C(s) = \frac{\phi_{out}}{\phi_{ref}}(s) = \frac{K_{PD}K_{VCO}}{s^2/\omega_{LPF} + s + K_{PD}K_{VCO}/N} \tag{2.3}$$

The second order closed-loop transfer function suggests the system can be over-damped, under-damped or critically damped. If we compare (2.3) with standard second order equation from control theory which is given by

$$H(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{2.4}$$

$$\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}} \tag{2.5}$$

$$\xi = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}} \tag{2.6}$$

where ξ is the damping ratio and ω_n is the natural frequency. The two poles of the closed-loop system are given by

$$S_{1,2} = \frac{1}{2}(\omega_{LPF} \pm \sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}}) \tag{2.7}$$

$$\xi\omega_n = \frac{1}{2}\omega_{LPF} \tag{2.8}$$

If $\omega_{LPF}^2 - 4K_{PD}K_{VCO}/N > 0$, the two poles are real and the transient step response is given by

$$\omega_{out}(t) = \left[\begin{array}{l} \dfrac{2K_{PD}K_{VCO}}{\sqrt{\omega_{LPF}^2 - \dfrac{4K_{PD}K_{VCO}}{N}}} \times \dfrac{1}{\omega_{LPF} - \sqrt{\omega_{LPF}^2 - \dfrac{4K_{PD}K_{VCO}}{N}}} \left[1 - e^{-\frac{1}{2}(\omega_{LPF} - \sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}})t} \right] \\ - \dfrac{1}{\omega_{LPF} + \sqrt{\omega_{LPF}^2 - \dfrac{4K_{PD}K_{VCO}}{N}}} \left[1 - e^{-\frac{1}{2}(\omega_{LPF} + \sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}})t} \right] \end{array} \right] u(t)\Delta\omega \tag{2.9}$$

(2.8) shows that the step response includes two exponential terms decaying with time constants τ_1 and τ_2 as

$$\tau_1 = \left[\frac{1}{2}(\omega_{LPF} - \sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}}) \right]^{-1} \tag{2.10}$$

$$\tau_2 = \left[\frac{1}{2}(\omega_{LPF} + \sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}}) \right]^{-1} \tag{2.11}$$

Since $\tau_1 > \tau_2$, the settling time is determined by τ_1, which decreases with the increase in $K_{PD}K_{VCO}/N$. But, having larger gain degrades the stability. Thus there is a trade-off between the settling time and stability for the type-I PLL. If $\omega_{LPF}^2 - 4K_{PD}K_{VCO}/N < 0$, the two poles are complex and the transient step response is given by

$$\omega_{out}(t) = \left[\begin{array}{l} 1 - e^{\frac{1}{2}\omega_{LPF}t} \cos(\sqrt{\dfrac{4K_{PD}K_{VCO}}{N} - \omega_{LPF}^2 t}) + \\ \dfrac{\omega_{LPF}}{\sqrt{\dfrac{4K_{PD}K_{VCO}}{N} - \omega_{LPF}^2 t}} \sin(\sqrt{\dfrac{4K_{PD}K_{VCO}}{N} - \omega_{LPF}^2 t}) \end{array} \right] Nu(t)\Delta\omega \tag{2.12}$$

If the damping factor is greater than one $(\xi > 1)$, the system is over-damped and from (2.12), the step response contains only one exponential term with the time constant equal to $2/\omega_{LPF}$, which is less than the time constant for real pole case. The larger is the bandwidth, the faster the settling time. In addition to the trade-off between settling time, phase error and bandwidth, type-I PLL suffers from the acquisition range. These problems are addressed by type-II PLL which is called charge pump PLL [20].

2.1.3.b Dynamics of Type-II PLL

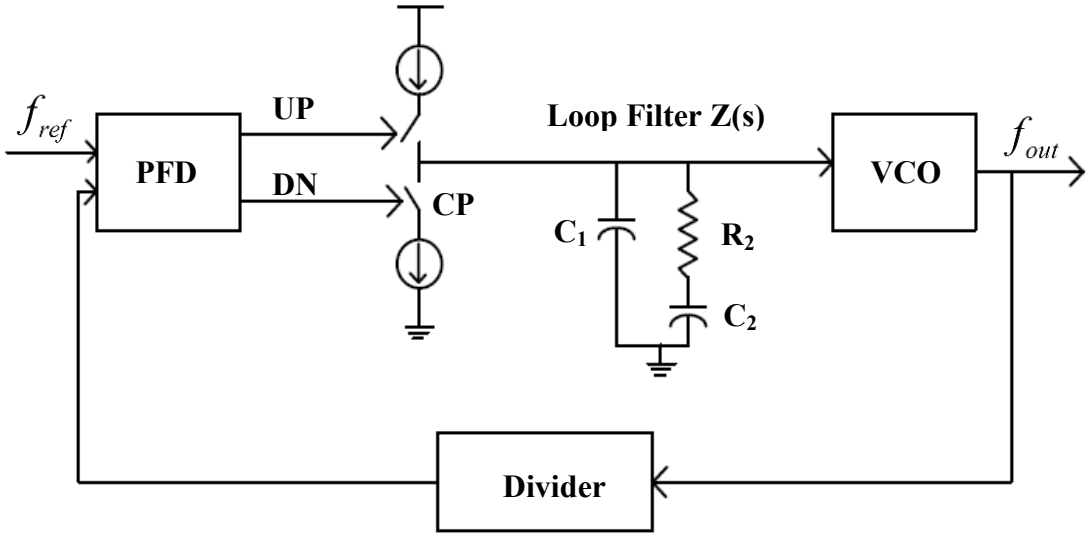


Fig. 2.4: Type-II charge pump PLL

Fig. 2.4 shows the typical type-II charge pump PLL with a 2nd order loop filter. In this architecture the charge pump is used to either sink or source a current with the help of the switches driven by the phase frequency detector (PFD). As a result, the PLL becomes a discrete system rather than a continuous system and strictly, the analysis cannot be performed in s-domain. However, Gardner [20] has proposed a limit that states, as long as the loop bandwidth is less than one-tenth of the reference frequency, the s-domain analysis holds true. Since the PD is replaced by the PFD, the locking range increases. Since the VCO acts as an integrator and the

combination of PFD with the charge pump and the LPF results in another integrator in the loop. Thus there exists two poles at the origin and this type of PLL is called as type-II PLL. Fig. 2.5 shows the linearized model of type-II PLL with their respective transfer functions.

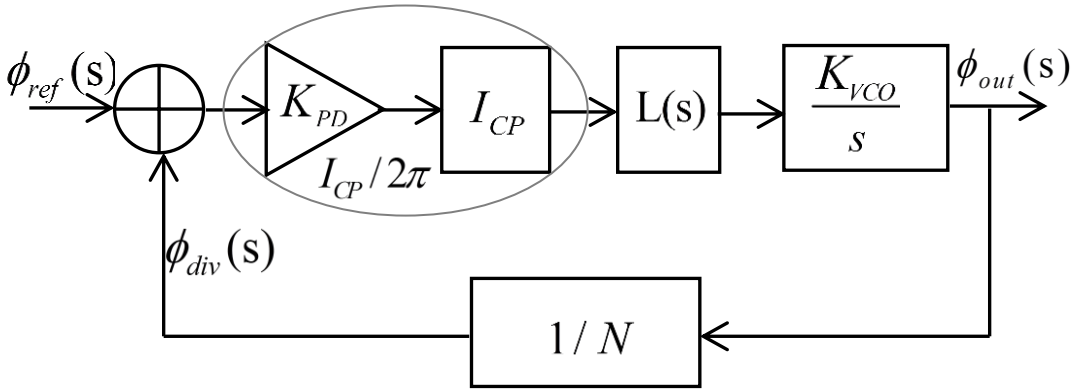


Fig. 2.5: Linear model of a type-II PLL

The open-loop transfer function is given by

$$H_O(s) = \frac{I_{CP}K_{VCO}}{2\pi N}\frac{L(s)}{s} \tag{2.13}$$

Where the transfer function of the 2nd order loop filter is given by

$$L(s) = \frac{1+sR_2C_2}{s^2R_2C_1C_2 + s(C_1+C_2)} \tag{2.14}$$

Here, C_2 together with charge pump generates a pole at the zero frequency while R_2 and C_2 generates a zero at the left half plane to stabilize the system. The location of the zero has to be less than the unity-gain frequency. The additional capacitor C_1 is introduced to generate a pole with R_2 to suppress high frequency components at the VCO control line. For stability, this pole has to be much larger than unity-gain frequency ω_c .The zero and pole frequencies are given by

$$\omega_{z1} = \frac{1}{R_2 C_2} = \frac{1}{T_2} \tag{2.15}$$

$$\omega_{p1} = \frac{C_2 + C_1}{R_2 C_2 C_1} = \frac{1}{T_1} \tag{2.16}$$

The closed-loop transfer function is given by

$$H(s) = \frac{I_{CP} K_{VCO}}{2\pi N(C_2 + C_1)} \frac{1 + sRC}{s^3 \frac{R_2 C_2 C_1}{C_2 + C_1} + s^2 + s \frac{I_{CP} K_{VCO} R_2 C_2}{2\pi N(C_2 + C_1)} + \frac{I_{CP} K_{VCO}}{2\pi N(C_2 + C_1)}} \frac{1}{2} \tag{2.17}$$

Since the pole ω_{p1} is far behind the unity gain frequency and $C_1 > C_2$, the closed loop transfer function can be re-written as

$$H_C(s) = \frac{I_{CP} K_{VCO}}{2\pi N C_2} \frac{1 + sR_2 C_2}{s^2 + s \frac{I_{CP} K_{VCO} R_2}{2\pi N} + \frac{I_{CP} K_{VCO}}{2\pi N C_2}} \tag{2.18}$$

This can be compared with the standard 2nd order negative feedback system from the control theory given by (2.4) and the critical loop parameters are obtained as,

$$\omega_n = \sqrt{\frac{I_{CP} K_{VCO}}{2\pi N C_2}} \tag{2.19}$$

$$\xi = \frac{R_2}{2} \sqrt{\frac{K_{VCO} I_{CP} C}{2\pi N}} \tag{2.20}$$

$$\phi_m = \tan^{-1}\left(\frac{\omega_C}{\omega_{z1}}\right) - \tan^{-1}\left(\frac{\omega_C}{\omega_{p1}}\right) \tag{2.21}$$

Here, ω_n is natural frequency, ω_c is loop bandwidth (unity-gain cross over frequency), ξ is the damping factor and ϕ_m is the phase margin. The poles of the closed-loop system are given by

$$S_{1,2} = \frac{1}{2}\left(-\frac{I_{CP}K_{VCO}R_2}{2\pi N} \pm \sqrt{\left(\frac{I_{CP}K_{VCO}R_2}{2\pi N}\right)^2 - \frac{4I_{CP}K_{VCO}}{2\pi NC_2}} \right) \tag{2.22}$$

Similar to type-I PLL, the system will have a higher settling time when the two poles are complex, which means

$$\left(\frac{I_{CP}K_{VCO}R_2}{2\pi N}\right)^2 - \frac{4I_{CP}K_{VCO}}{2\pi NC_2} < 0 \Rightarrow \frac{I_{CP}K_{VCO}}{2\pi N} < \frac{4}{R_2^2 C_2} \tag{2.23}$$

Based on this, the transient response for the system with complex poles is given by

$$\omega_{out}(t) = \left[1 - e^{\frac{1}{2}(\frac{I_{CP}K_{VCO}R_2}{2\pi N})t}\right] \left| \begin{array}{l} \cos\left(\sqrt{\frac{4I_{CP}K_{VCO}}{2\pi NC_2} - \left(\frac{I_{CP}K_{VCO}R_2}{2\pi N}\right)^2}\, t\right) + \\ \frac{R_2C_2}{2\sqrt{\frac{4I_{CP}K_{VCO}}{2\pi NC_2} - \left(\frac{I_{CP}K_{VCO}R_2}{2\pi N}\right)^2}} \sin\left(\sqrt{\frac{4I_{CP}K_{VCO}}{2\pi NC_2} - \left(\frac{I_{CP}K_{VCO}R_2}{2\pi N}\right)^2}\, t\right) \end{array} \right| Nu(t)\Delta\omega \tag{2.24}$$

The step response contains only one exponential term with the time constant τ expressed as,

$$\tau = \left(\frac{1}{2}\frac{I_{CP}K_{VCO}R_2}{2\pi N}\right)^{-1} \tag{2.25}$$

From the above study, the settling time is minimized by increasing $I_{CP}K_{VCO}$, thus there is no trade-off between critical specifications in the selection of $I_{CP}K_{VCO}$.

However, the increase of $I_{CP}K_{VCO}$ is bounded by the unity gain frequency, which is no more than one-tenth of the reference frequency as stated by the Gardner [20].

2.2 Types of PLL

Several types of PLL [21] architectures are available in market. The architectures broadly range according to the application. These different architectures of PLL can be considered as different types of PLL. Following types of PLL are classified according to their application.

1. Programmable PLL: This type of PLL can be programmed for wide range of signals.

2. Single and multi-phase PLL: These can control a single or many phases. They are used in digital clock networks.

3. Digital Phase Locked Loop: They are used digital input signals for application like Manchester coding.

4. PLL with lock detector: It uses a lock on one of the pins and is used in frequency modulation.

5. PLL frequency synthesizer: These are used to synthesize the frequency of different range and band.

6. PLL FM/AM demodulator: The FM/AM radio frequencies are modulated and demodulated using this type of PLL.

7. Single RF/ Multi RF PLL: It is used for controlling single or multiple radio frequencies.

8. Super PLL: It is used for frequency synthesizing of radios, networks of GSM, cordless phones, etc.

PLLs are also classified according to the type of loop filter used in architecture. The order of loop filter is the type of PLL. For example, if 1st order loop filter is used, then it is called as type I PLL. If 2nd order filter is used, it is called as type II PLL and so on.

If PLL uses simple „Phase detector" in its architecture, it is called as simple PLL. But if PLL uses „Phase Frequency Detector" accompanied with „Charge Pump", it is called as "Charge Pump PLL".

2.3 Types of Frequency Synthesizers

From the above study and analysis, the PLL output frequency could be programmed by setting frequency division ratio to different values. Indeed, the PLL based frequency synthesizer is the most widely used frequency synthesizer approach in modern wireless communications systems.

2.3.1 Integer-N Frequency Synthesizer

An integer-N frequency synthesizer consists of integer-N divider with integer division ratios. The advantage of this type of synthesizer is the robust design of the frequency dividers. The most commonly used integer-N divider is pulse-swallow divider as shown in Fig. 2.6.

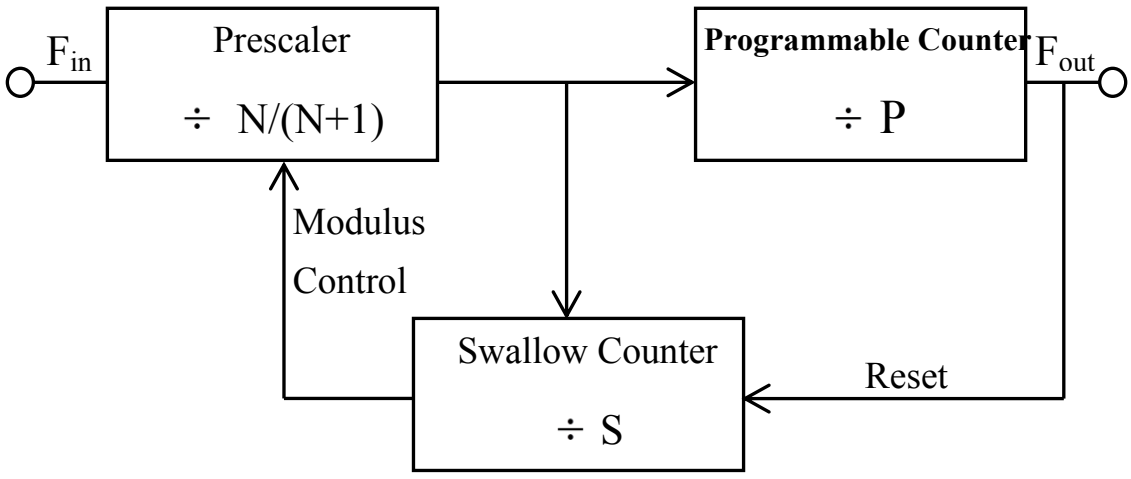


Fig. 2.6: Pulse-swallow frequency divider

Here, the PLL output is the integer multiple of the reference frequency and the finest PLL output frequency change equals to the reference frequency. Therefore, the required frequency spacing sets the upper-limit of the reference frequency. This results in the limited bandwidth, larger settling time and high close-in output phase noise.

2.3.2 Fractional-N Frequency Synthesizer

In a fractional-N frequency synthesizer [18], the smallest frequency step can be a fraction of the reference frequency. A simple fractional divider is shown in Fig. 2.7 which consists of a N/(N+1) dual-modulus divider and a modulus control unit. The modulus control unit sets the instantaneous division ratio to either N or N+ 1 ratio so that the division ratio is a fractional number between N and N+1. If the division ratio is N for P cycles of the output and N+1 for Q cycles of the output, the equivalent division ratio is equal to (PN+Q(N+1))/(P+Q).

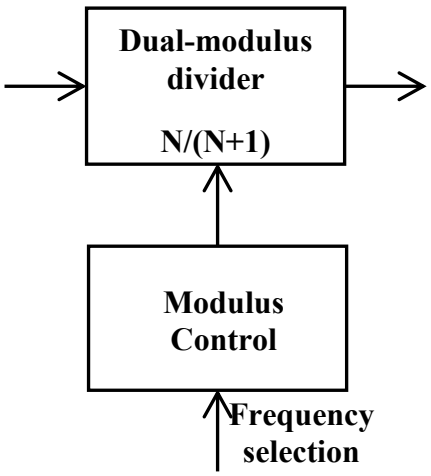


Fig. 2.7: A fractional frequency divider

Since the output is obtained by averaging instant ratios over time, the spectrum of divider output contains spurious tones called fractional spurs at the output of the PLL. The problem is severe when P and Q are constant over time. To address this issue, a delta-sigma modulator has introduced in place of modulus control unit which

transforms the fractional spurs to random noise. However, this approach increases the complexity and power consumption.

2.3.3 Direct Digital Synthesizer

A direct digital synthesizer (DDS) generates carrier frequency very fast by removing the feedback as shown in Fig.2.8. A DDS generates the signal in the digital domain through an accumulator and a read-only memory (ROM), which is converted to analog waveform by digital-to-analog converter (DAC). Spurious harmonics at the output of DAC are filtered out by low pass filter (LPF). Since this architecture employs no feedback, settling time is very fast. The main advantages of DDS are low phase noise, fine frequency steps and no stability issues.

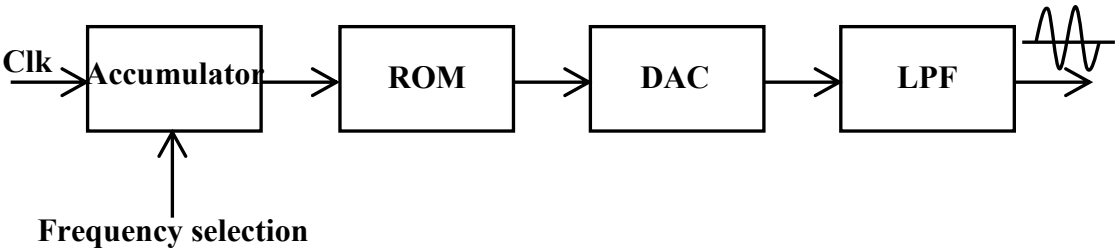


Fig. 2.8: A direct digital synthesizer

The main drawback of DDS is its low output frequency due to the practical speed limit of the DAC**.** To reconstruct the analog waveform correctly, the clock frequency has to be no less than twice of the output frequency (Nyquist‟s theorem). In RF applications, to have all the digital blocks of DDS work at least twice the carrier frequency is very difficult to achieve. The non-idealities of DAC are also major concerns.

2.4 Non Ideal Effects in PLL

So many imperfections always remain in practical PLL circuit. Ideally, the synthesized signal is a pure sinusoidal waveform. But in reality, its power spectrum features a peak at the desired frequency and tails on both sides. The uncertainty of a synthesizer‟s output is characterized by its phase noise (or spur level) at a certain frequency offset from the desired carrier frequency in unit of *dBc/Hz* (or *dBc).* The

unit of *dBc/Hz* measures the ratio (in *dB)* of the phase noise power in 1Hz bandwidth at a certain frequency offset to the carrier power. Similarly, the unit of *dBc* measures the ratio (in *dB)* of the spur (also known as tone) power at a certain frequency offset to the carrier power. These lead to high ripple on the control voltage even when the loop is locked. These ripples modulate the VCO frequency, which results in non-periodic waveform. This section considers these non-ideal effects in PLL [16],[22], [23].

2.4.1 Jitter in PLL

Timing jitter is the time domain characterization of the uncertainty of a synthesizer or oscillator‟s output. A jitter is the short-term variations of a signal with respect to its ideal position in time. This problem negatively impacts the data transmission quality. Deviation from the ideal position can occur on either leading edge or trailing edge of signal. Jitter may be induced and coupled onto a clock signal from several different sources and is not uniform over all frequencies. Denoting the period of the *n*th cycle of an oscillator‟s output as T_n and its average period is $\overline{T}$, there are basically three-types of jitters:

(1) The cycle jitter, or cycle-to-average jitter, is defined as:

$$\Delta T_{cn} = T_n - \overline{T} \tag{2.26}$$

(2) The cycle-to-cycle jitter is expressed as:

$$\Delta T_{ccn} = T_{n+1} - T_n \tag{2.27}$$

(3) The absolute jitter, also known as long-term jitter or accumulated jitter, of the N_{th} cycle can be described as:

$$\Delta T_{abs}(N) = \sum_{n=1}^{N} (T_n - \overline{T}) = \sum_{n=1}^{N} (\Delta T_{cn}) \tag{2.28}$$

The response of PLL to jitter is very important in most applications. Fig. 2.9 explains the jitter in PLL.

As shown in Fig. 2.9, a strictly periodic waveform, x1(t), contains zero crossings that are evenly spaced in time. Now consider nearly periodic signal x2(t),

whose period experiences a small changes, deviating the zero crossing from their ideal points. Hence we can say that x2(t) suffers from jitter. If the instantaneous frequency of signal varies slowly from one period to next period, then it is called as "slow jitter", and if the variation is fast, it is called as fast jitter.

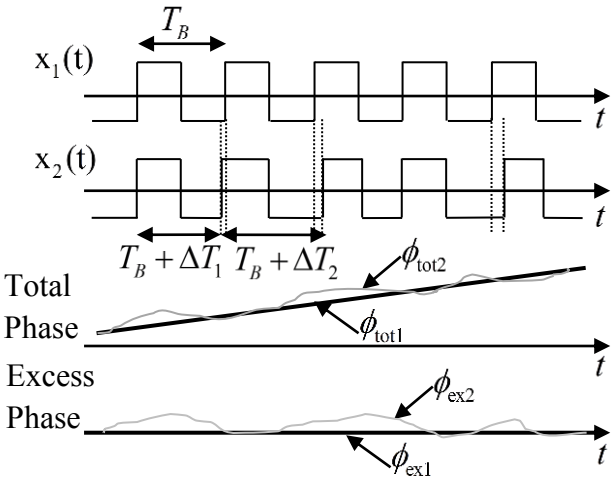


Fig. 2.9: Ideal and Jittery Waveforms

2.4.2 Phase Noise

Phase noise is random variation of phase of the signal. It is the frequency domain representation of rapid, short term fluctuations in the phase of the wave, caused by time domain instabilities ("jitter"). Generally the phase noise and jitter are closely related. Or more specifically, radio engineer call it as phase noise, but digital system engineer call it as jitter of the clock.

The ideal synthesizer produces a pure sinusoidal waveform

$$V(t) = V_0 \sin(2\pi f_0 t) \qquad ((2.29)$$

When amplitude and phase fluctuations are accounted, the waveform becomes

$$V(t) = (V_0 + v(t)) \sin(2\pi f_0 t + \phi(t)) \qquad (2.30)$$

where $V(t)$ and $\phi(t)$ represent amplitude and phase fluctuations, respectively. Here two types of phase fluctuations are considered, the periodic variation and the random variation [17]. In mathematical form, $\phi(t)$ can be written as:

$$\phi(t) = \Delta\phi \sin(2\pi f_m t) + \phi(t) \qquad (2.31)$$

The first term represents the periodic phase variation and it produces a spurious tone at an offset frequency of f_m from the carrier frequency f_0. The magnitude of the spurious tone can be derived as follows:

$$V(t) = V_0 \sin(2\pi f_0 t + \Delta\phi \sin(2\pi f_m t)) \tag{2.32}$$

$$= V_0[\sin(2\pi f_0 t)\cos(\Delta\phi \sin(2\pi f_m t)) + \cos(2\pi f_0 t)\sin(\Delta\phi \sin(2\pi f_m t))]$$

For very small phase modulation, i.e., $\Delta\phi << \pi / 2$

$$\cos(\Delta\phi \sin(2\pi f_m t)) \approx 1 \tag{2.33}$$

$$\sin(\Delta\phi \sin(2\pi f_m t)) \approx \Delta\phi \sin(2\pi f_m t) \tag{2.34}$$

Then (2.4) yields:

$$V(t) = V_0[\sin(2\pi f_0 t) + \Delta\phi \cos(2\pi f_0 t)\sin(2\pi f_m t)]$$

$$= V_0\left[\sin(2\pi f_0 t) - \frac{\Delta\phi}{2}\sin(2\pi(f_0 - f_m)) + \frac{\Delta\phi}{2}\sin(2\pi(f_0 + f_m)\right] \tag{2.35}$$

From (2.35) we observe that the two spurious tones at $f_0 + f_m$ and $f_0 - f_m$ are both $-20\log(\Delta\phi/2)dB$ below the carrier. The second term of $\phi(t)$ in (2.31) represents the random phase variation and it produces phase noise. The spectral density of phase variation is

$$S_\varphi(f) = \int_{-\infty}^{+\infty} R_\varphi(\tau) e^{-j2\pi f\tau} d\tau \tag{2.36}$$

where $R_\varphi(\tau)$ is the auto-correlation of the random phase variation $\varphi(t)$:

$$R_\varphi(\tau) = E[\varphi(t)\varphi(t-\tau)] \tag{2.37}$$

When the root-mean-square *(rms)* value of $\varphi(t)$ is much smaller than 1*radian,* the power spectrum density of $V(t)$ can be approximated as

$$S_V(f) = \frac{V_0^2}{2}[\delta(f - f_0) + S_\varphi(f - f_0)] \tag{2.38}$$

It consists of the carrier power at f_0 and the phase noise power at frequency offsets from f_0. The single-sideband (SSB) phase noise is defined as the ratio of noise power in $1Hz$ bandwidth at a certain frequency offset $\Delta f = f - f_0$ from the carrier to the carrier power. The unit is *dBc/Hz.*

$$N(\Delta f) = 10\log\frac{(\text{noise\_in\_}1Hz\ at\ f)}{P_{carrier}} = 10\log\frac{S_{\varphi}(\Delta f)}{2}\frac{1}{2} \qquad dBc/Hz$$

(2.39)

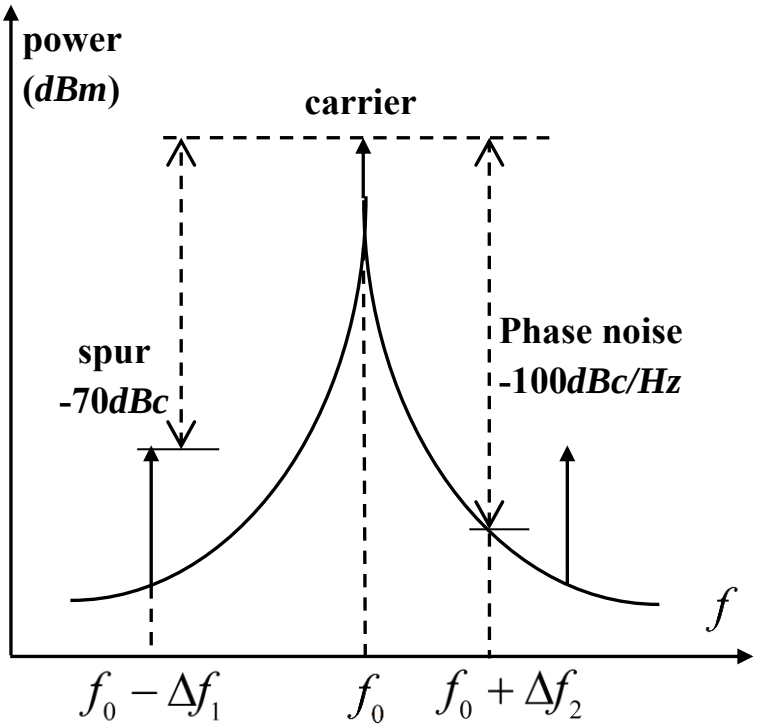


Fig. 2.10: Phase noise and spur

Therefore, the phase noise *dBc/Hz* value observed on the spectrum analyzer is numerically equivalent to $10\log[S_{\varphi}(\Delta f)] - 3$. Fig. 2.10 illustrates the phase noise and spurs of a synthesized signal of frequency f_0. The spur level at an offset frequency of $-\Delta f_1$ is *–70dBc,* and the phase noise at an offset frequency of Δf_2 is –100*dBc/Hz.*

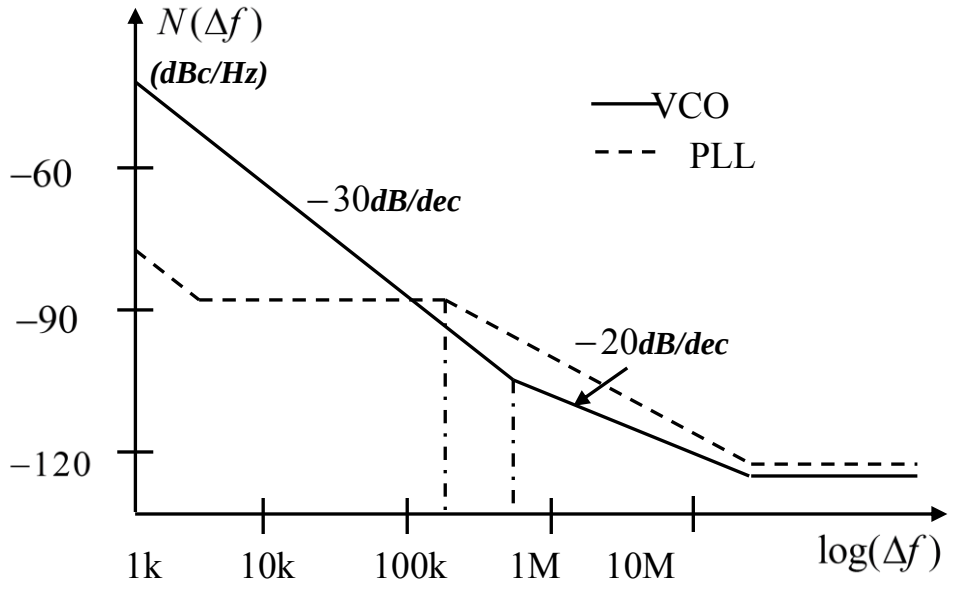


Fig. 2.11: Phase noise of VCO and PLL

Fig. 2.11 conceptually shows the phase noise of a voltage-controlled oscillator (VCO) and a phase-locked loop (PLL). The phase noise of a VCO demonstrates regions with slopes of –30*dBc/dec* and –20*dBc/dec,* and a flat region. A PLL‟s in-band phase noise is usually as flat as its reference input, while its out-band phase noise follows that of the VCO.

Phase noise is of very much concern in PLL, since it directly affects the entire performance of the system. Following are the common sources of phase noise in PLL.

i) **Oscillator noise**: There are two oscillators that contribute to the phase noise of the PLL. One is the reference oscillator and other is the VCO. Although both oscillators can be modeled similarly, their effects on the output noise are distinct just due to their position in the loop. Suppose a noiseless VCO is added with AWGN with DSPSD of *No*/2. Then the output power spectrum is given by *2KVCO*((*No*/*2)ω2*). Though it is very simplified equation, it clearly gives the idea of output noise of PLL in the presence of VCO noise. The reference oscillator is also assumed to have sufficient behavior with different constant of proportionality.

ii) **Frequency Divider noise**: The excess noise of a digital divider can be modeled as additive noise source at its output. In a PLL, this noise directly appears at the input of phase detector and experiences the same transfer function as the noise on the input terminal.

iii) **Phase detector noise**: Usually phase detectors are not major sources of noise in PLLs. As the work of PD is to detect the phase difference, any random variation in the phase of input signal makes the phase detector to produce wrong output, which is get transferred through filter and tunes the VCO wrongly.

2.4.3 Reference spur

Reference spurs are spurious emissions that occur from the carrier frequency at an offset equal to the channel spacing. These are usually caused by leakage and mismatch in charge pump of PLL. Though they occur outside the band of interest, they can enter the mixers and be translated back onto band of interest.

Reference spur mainly occurs in Charge Pump PLL. Though there is no phase difference between reference and feedback signal, in the locked state, the phase detector (or phase frequency detector) produces very narrow pulse width error voltage which drives the charge pump. Although these pulses have a very narrow width, the fact that they exist means that the dc voltage driving the VCO is modulated by a signal of frequency equal to input reference frequency. This produces **reference spurs** in the RF output occurring at offset frequencies that are integer multiples of input reference frequency. A spectrum analyzer can be used to detect reference spurs. Simply increase the span to greater than twice the reference frequency.

Let I_{cp} is charge pump current, I_{leak} is leakage current in CP then the phase offset is given by:

$$\Phi_{\in} = 2\pi.\frac{I_{leak}}{I_{cp}}\ [rad] \tag{2.40}$$

Now if f_{ref} is the input reference frequency, f_{BW} is loop bandwidth, f_{pl} is the frequency of pole in loop filter and N is the division value then the amount of reference spur in 3rd order PLL is given by:

$$P_r = 20\log\left(\frac{1}{\sqrt{2}}.\frac{f_{ref}}{f_{BW}}.N.\Phi_{\epsilon}\right) - 20\log\left(\frac{f_{ref}}{f_{pl}}\right)[dBc] \qquad (2.41)$$

If reference spur is not enough to meet the requirement, the loop bandwidth should be further narrowed or charge pump current should be increased. It is also helpful to reduce the division value to relax the charge pump design.

2.5 Applications of PLL

Since its invention, PLL continues to find new applications in electronics, communication and instrumentation. Examples include memories, microprocessors, hard disk drive electronics, RF and wireless transceivers, clock recovery circuits on microcontroller boards and optical fiber receivers. Some of the applications are as follows [16].

2.5.1 Frequency multiplication and synthesis

A PLL can be modified such that it multiplies its input frequency by factor of M . Fig. 2.12 shows basic frequency multiplication concept.

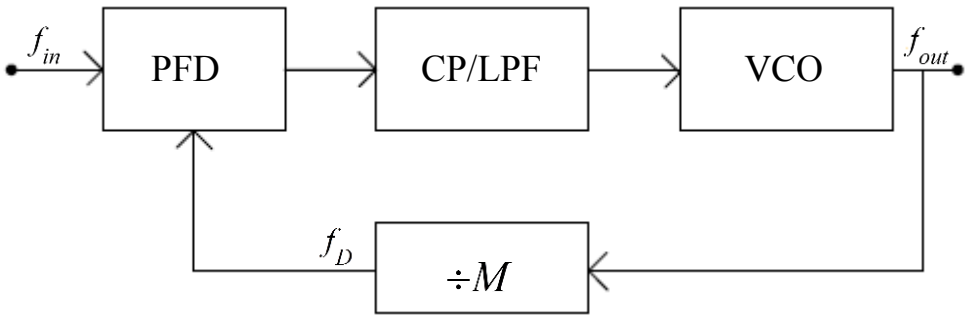


Fig. 2.12: Frequency Multiplication

Just like a voltage divider is used in feedback in voltage amplifier, as shown in Fig. 2.5, output frequency of PLL is divided by *M* and applied to the phase detector, we

get, $f_{out} = M.f_{in}$. Also, since fin and f_D must be equal, PLL multiplies f_{in} by M. Some systems require a periodic waveform whose frequency (a) must be very accurate and (b) can be varied in very fine stapes. Hence to synthesize a required frequency, a channel control word (digital) is applied to divider block in feedback that varies the value of M. Since $f_{out} = M.f_{in}$, the relative accuracy of f_{out} is equal to that of f_{ref}. It is also notable that f_{out} varies in stapes equal to f_{ref} if M changes by one each time.

2.5.2 Skew reduction

This is one of the very popular and earliest uses of PLL. Suppose synchronous pair of data and clock lines enter a large digital chip. Since clock typically drives a large number of transistors and logic interconnects, it is first applied to large buffer. Thus, the clock distributed on chip may suffer from substantial skew (delay due to buffer insertion) with respect to data. This is an undesirable effect which reduces the timing budget for on-chip operations.

Now consider the circuit as shown in Fig 2.13. Here input clock CK_{in} is applied to on chip PLL and buffer is placed inside the loop. Since PLL guarantees a nominally zero phase difference between CK_{in} and CK_B, the skew is eliminated. That is, the constant phase shift introduced by the buffer is divided by infinite loop gain of the feedback system. Alignment of V_{VCO} with CK_{in} is not important since V_{VCO} is not used.

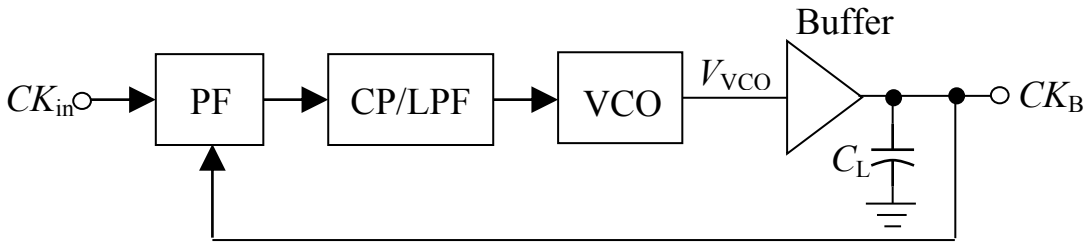


Fig. 2.13: Use of PLL to Eliminate Skew

CHAPTER 3

Frequency Synthesizer Building Blocks

3.1 Phase detector/Phase Frequency Detector (PD/PFD)

A phase detector (PD) [24]-[26] is a circuit whose average output voltage ($\overline{V_{out}}$) is linearly proportional to the phase difference ($\Delta\phi$) between its two inputs. In an ideal case, the relationship between $\overline{V_{out}}$ and $\Delta\phi$ is linear, crossing the origin for $\Delta\phi$=0 as shown in Fig. 3.1. The gain of the PD is K_{PD} expressed in V/rad.

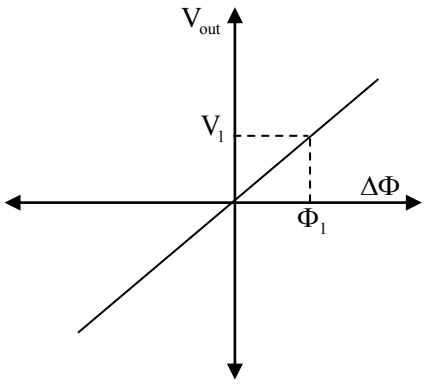


Fig. 3.1: Phase detector characteristics

A. XOR Based PD

A familiar example of phase detector is the exclusive OR (XOR) gate [19] as shown in Fig.3.2. As the phase difference between the inputs varies, so does the width of the output pulses, thereby providing a dc level proportional to $\Delta\phi$. The XOR PD produces error pulses on both rising and falling edges. Fig.3.2c shows the transfer characteristics of the XOR PD.

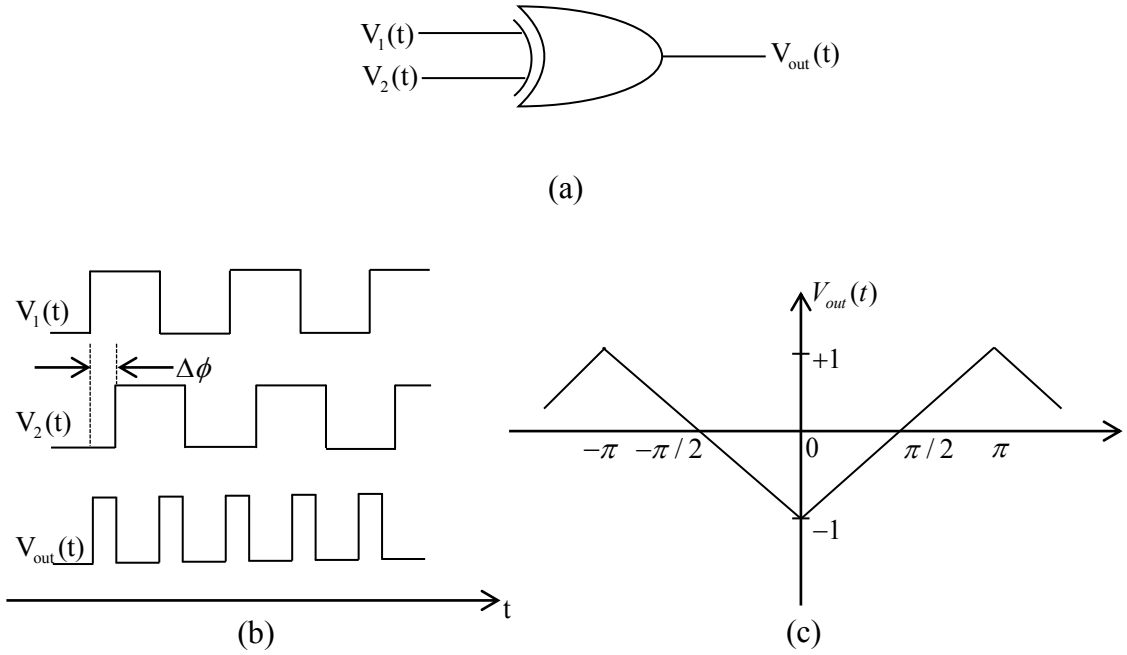


Fig. 3.2: XOR phase detector and phase characteristics

The major drawback of XOR PD is its inability to detect frequency difference. As any frequency difference exists, the phase difference would be accumulated either in a positive direction (reference frequency slower than divider frequency) or in a negative direction (reference frequency faster than divided frequency). As shown in Fig. 3.2c, the transfer function of PD is symmetrical over y-axis due to which it fails to differentiate the polarity of phase difference, and thus the frequency difference. The second issue is that, when the PLL is locked, the average of XOR PD output is zero. This zero voltage is averaged from a square wave of twice the reference frequency. Therefore, the pole of LPF has to be low enough to attenuate this reference spur. The XOR PD is sensitive to the duty cycle of the input signals.

B. D flip-flop Based PD

A simple D flip-flop (DFF) could also be used as a phase detector [27]. Here, the reference signal serves as a clock to sample the divided VCO signal. When reference leads the feedback divider signal, the output remains at logic „1" and if

the reference lags the feedback divider signal, the output switches to logic „0". Therefore, the DFF based PD operation is highly nonlinear and leads to the stability issue and phase error. This PD also fails to detect any frequency difference.

C. Tri-State Phase Frequency Detector (PFD)

The XOR and DFF based PD's fail to detect the frequency difference and are not suitable for PLL applications where initial VCO oscillation frequencies are far away from reference. A tri-state PFD [28] detects both phase and frequency difference. Fig.3.3 shows the implementation of the PFD.

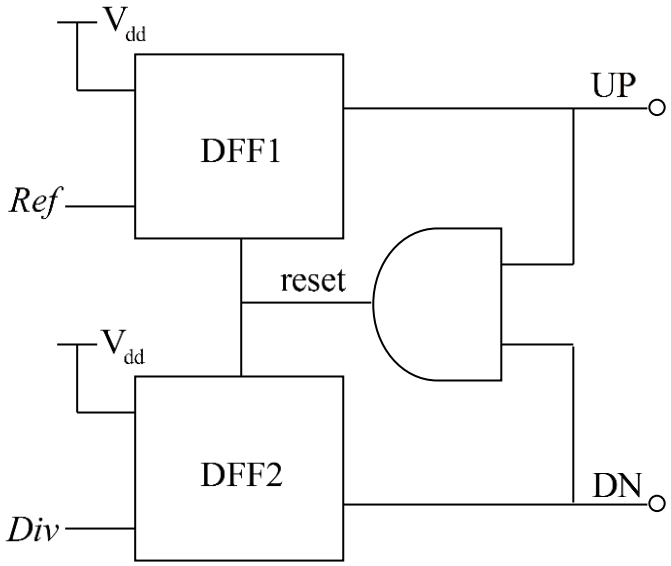


Fig. 3.3: Tri-state PFD implementation

Let *Ref* be the reference signal, and *Div* the divider output signal. If *Ref* leads *Div*, the rising edge of *Ref* triggers DFF1 and the UP signal is switched from 0 to 1 and DN signal remains at 0. The UP signal remains at 1 until the occurrence of rising edge of *Div* which triggers DFF2 and the UP signal is reset to 0 by the AND gate. A similar behavior happens when *Ref* lags *Div*. The phase difference between *Ref* and *Div* is indicated by the difference between UP and DN signals.

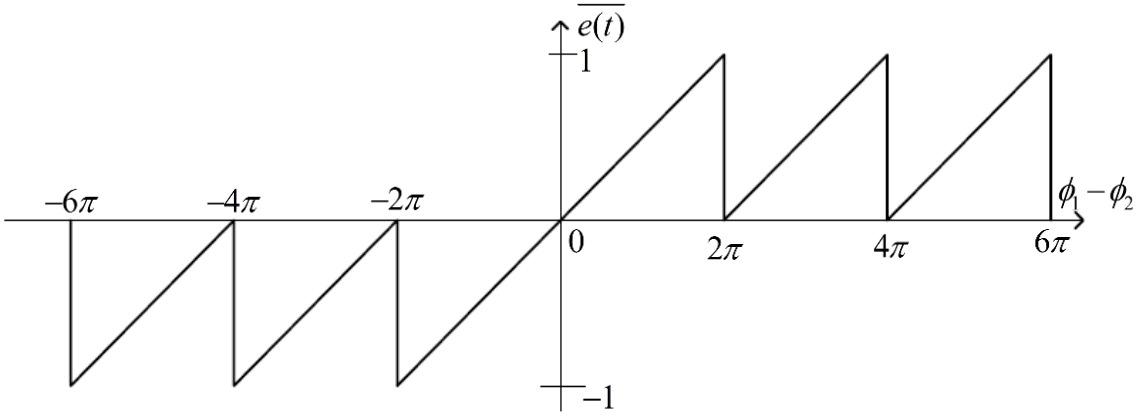


Fig. 3.4: Transfer characteristics of a tri-state PFD

Fig.3.4 shows the transfer characteristics of a tri-state PFD which is unsymmetrical over y-axis and the output has the same sign as that of the phase difference. Therefore, the output would be in opposite polarities between positive and negative frequency difference. When *Ref* leads *Div* ($f_{Ref} > f_{Div}$), the resulting positive pulses appear at *UP* while *DN* stays at 0. When *Ref* lags *Div* ($f_{Ref} < f_{Div}$), the resulting positive pulses appear at *DN* while *UP* stays at 0. Thus, the average of *UP-DN* suggests the frequency difference.

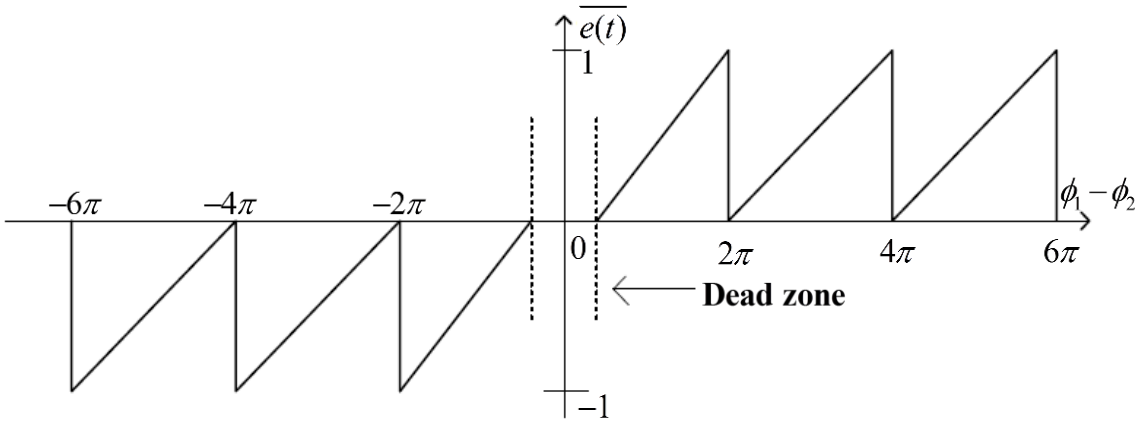


Fig. 3.5: Dead zone in tri-state PFD

However, tri-state PFD suffers from the "dead zone" problem [29]. The transfer function curve under the dead zone is given in Fig.3.5. When the phase difference between *Ref* and *Div* is close to zero, the width of the UP and DN pulses would approach to a minimal, which is set by the delay of the AND gate in the feedback path. However, the charge pump may not be to detect such narrow pulses, resulting

to no current injecting to the LPF, which is almost similar to the case of zero phase difference. As a result, the PFD gain is down to zero and the PLL loop would not function and there would be an unpredictable phase error between the two inputs so the jitter at output of the PLL accumulates. The dead zone in the PFD is avoided by introducing delay after the AND gate in the feedback path to increase the propagation delay as shown in Fig.3.6. However, this technique increase the charge pump mismatch current causing reference spurs.

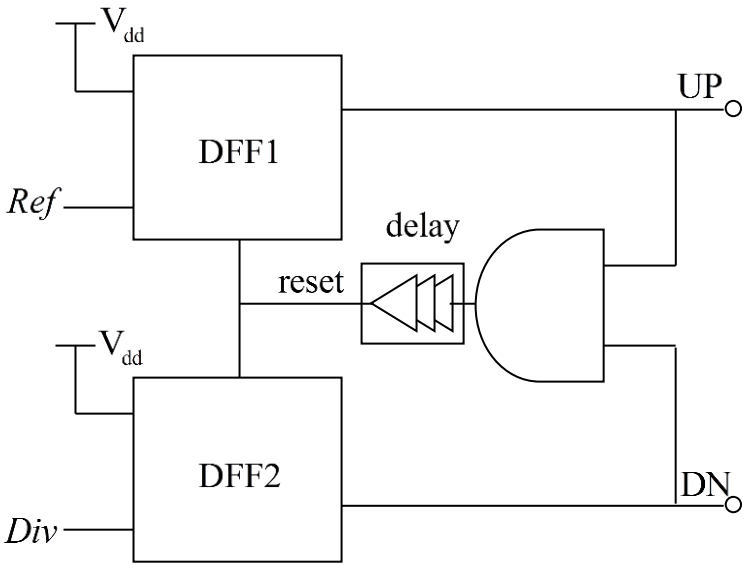


Fig. 3.6: Dead zone free PFD

3.2 Charge Pump

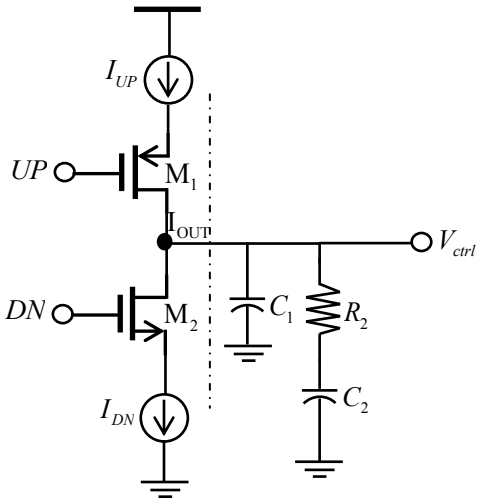


Fig. 3.7: Charge pump with loop filter

A charge pump [31] generally consists of two current sources that are switched on and off at the proper instance of time. When Ref leads Div ($f_{Ref}>f_{Div}$), the resulting positive pulses appear at UP while DN stays at 0. Under this condition, M1 is turned-on and M2 is turned-off such that the current I_{UP} charges the loop filter to pull-up the VCO frequency as shown in Fig.3.8a. When Ref lags Div ($f_{Ref} < f_{Div}$), the resulting positive pulses appear at DN while UP stays at 0. Under this condition, M1 is turned-off and M2 is turned-on such that the current I_{DN} discharges the loop filter to pull-down the VCO frequency as shown in Fig.3.8b. Under locked condition when Ref is equal to Div ($f_{Ref} = f_{Div}$), both switches M1 and M2 are on for a short period equal to the dead zone pulse width and net current flowing into the loop filter is negligible.

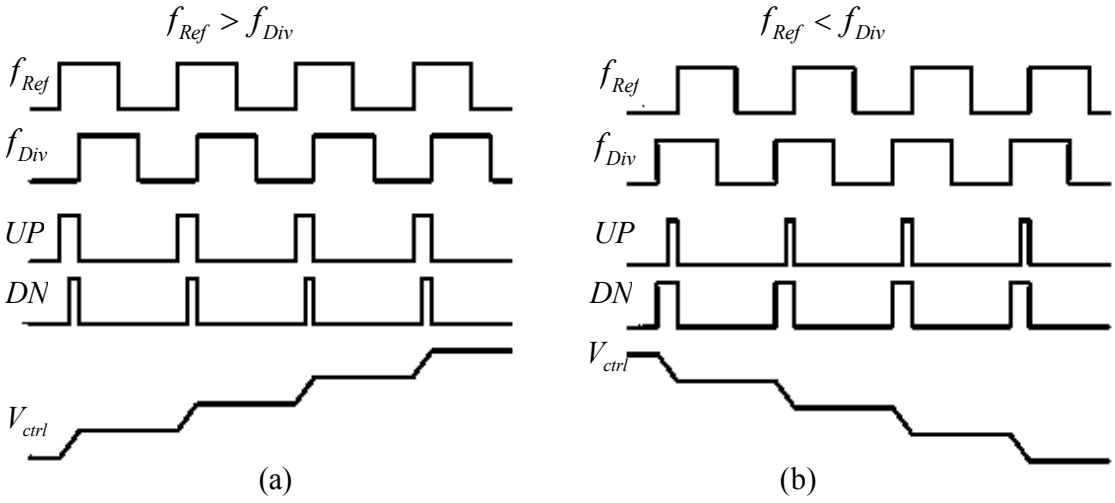


Fig. 3.8: Charge pump transient analysis a) *Ref* leads *Div* b) *Ref* lags *Div*

Charge pump suffers from non-ideal effects. Switches are constructed using PMOS and NMOS. The inherent mismatches between these two switches results in mismatch in charging and discharging current in addition to timing mismatch. Hence there is variation in control voltage at the output. In fact the W/L ratios are adjusted so as to have equal UP and DOWN currents. That means, since two current sources are themselves mismatched, the control voltage experiences the random changes in it. There is also problem of charge sharing between output node of charge pump (in

fact between filter capacitor) and the parasitic capacitances between drain and source of switch transistors. This results in sudden change in control voltage which may disturb the VCO. Another effect is clock feed through. The high frequency signal provided at the gate of switch transistor passes to the output node via gate to drain parasitic capacitor Cgd. This also results in jumps in control voltage. Since the VCO sensitivity is high, even a small jump in control voltage results a large jump in output frequency. Later on in chapter 4 we will use some techniques to overcome these non-idealities.

3.3 Voltage Controlled Oscillator (VCO)

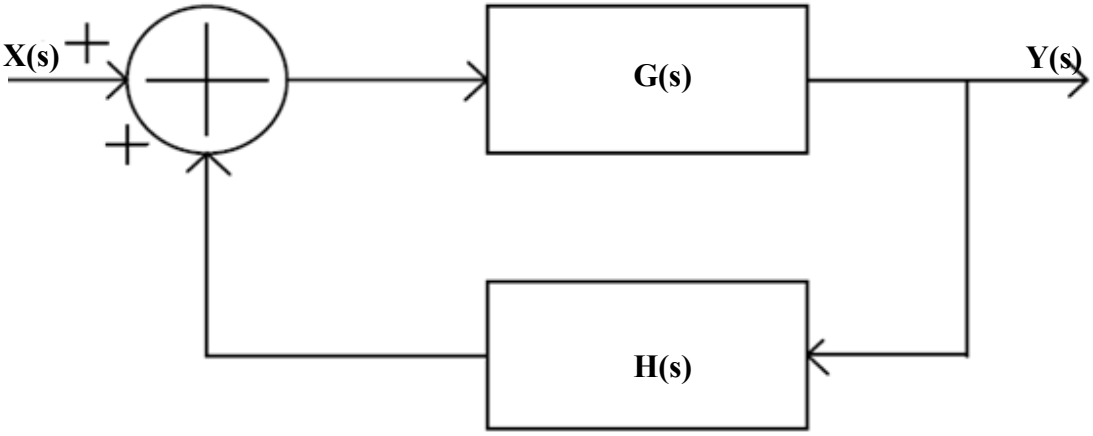


Fig. 3.9: Feedback oscillatory system

The voltage controlled oscillator (VCO) is an important building block of a PLL synthesizer which generates periodic signals. Consider a linear feedback system shown in Fig.3.9 and its transfer function is given by [19],

$$\frac{Y(s)}{X(s)} = \frac{G(s)}{1-G(s)H(s)} \quad (2.48)$$

Oscillation happens if a stable periodic signal is produced and in the steady state, Barkhausen‟s criteria must be satisfied at ω_0 [19]:

(1) The loop gain $\left|G(s)H(s)\right| \geq 1$

(2) The total phase shift around the loop, $\angle G(s)+H(s)=0°$ or $360°$

While Barkhausen's criteria explain the steady state of the VCO, it does not give hints on how the VCO converts its own noise in to periodic signal with certain amplitude. Actually, during oscillation start-up, the loop gain $\left|G(s)H(s)\right|$ must be larger than unity to amplify noise at ω_0. The nonlinearity of VCO would eventually limit the amplitude of the signal to a certain level, arriving at the steady state when the average loop gain is unity. Commonly, both ring oscillators and LC oscillators are used in GHz range applications [32],[33]. However, ring oscillators suffer from poor phase noise compared to that of LC oscillators [34],[35]. Ring oscillators are more attractive due to their smaller area compared to that of LC oscillators and are suitable for applications where such level of phase noise is acceptable.

3.4 Divider

The divider in the feedback path of the PLL determines the output frequency of the VCO in locked state. Typically the divider sees the full range of frequencies in the loop (from several hundred kHz to several GHz). The divider must be programmable to select different channels for the desired application. Due to different speed requirement, the divider is usually implemented by a combination of different logic family circuits. In the low speed part, the full swing conventional CMOS logic is used for its low static power consumption.

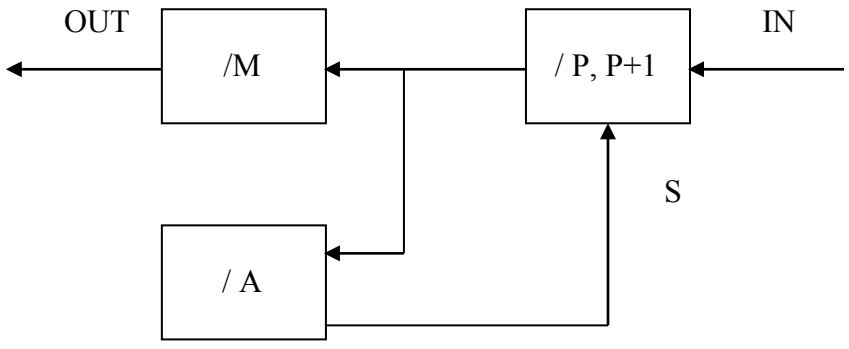


Fig. 3.10: Programmable divider

A programmable divider usually consists of a prescaler and two counters in a pulse swallow architecture [36], Fig. 3.10. The dual modulus prescaler divides the input frequency by either P or P+1 depending on the setting signal S. But in our design, we have purposely used static N divider which is explained in chapter 4. The output of the prescaler serves as the input of counter A and counter M. In our design we have omitted the A (swallow) counter. At the beginning, the prescaler is in the divide by P+1 mode. When counter A reaches zero, the setting signal S sets the prescaler in the divide by P mode. This mode continues until counter M reaches zero. For a complete cycle, it takes MP+A edges of the input to generate one edge at the divider output. This means that the divider divides the input by MP+A.

CHAPTER 4

CMOS RF Wide Band Frequency Synthesizer Design

4.1 Phase Frequency Detector Design

A Phase Frequency Detector (PFD) consists of two positive edge triggered D flip flop [37], which compares the reference and feedback clock continuously. The not gate and a delay buffer is used to reset the PFD when both the pulses go high, a state which we avoid to achieve. Since, when both the signals go high we don‟t want the PFD to keep working so we add a delay and then reset the D flip flops. To take a further look into what makes this D flip flop achieve its intended operation we will take a look at transistor level circuit diagram of the PFD.

The Phase Frequency Detector used in this design of PLL is similar to [38] with certain modification to achieve fast operation. According to [38], the Phase Frequency Detector consists of two D flip flops. Each D flip flop has 8 transistors and one extra CMOS inverter to get the positive output. The number of transistors has been reduced compared to [39] to further increase the operating frequency of the PFD. The two PMOS is connected to the VDD, the clocks and the reset pulse. When the Clock and Reset are both low then the PMOS turns “ON” and latches with the VDD and holds its value till the positive edge of the clocks. This is the basic idea of this flip flop. When the RESET turns high the PMOS is switched off and the node below PMOS is latched to ground via the 3 NMOS transistors. The transistor level circuit diagram of PFD in [38] is shown in Fig. 4.1. The UP and DN signals are obvious reference to slowing and speeding of the VCO.

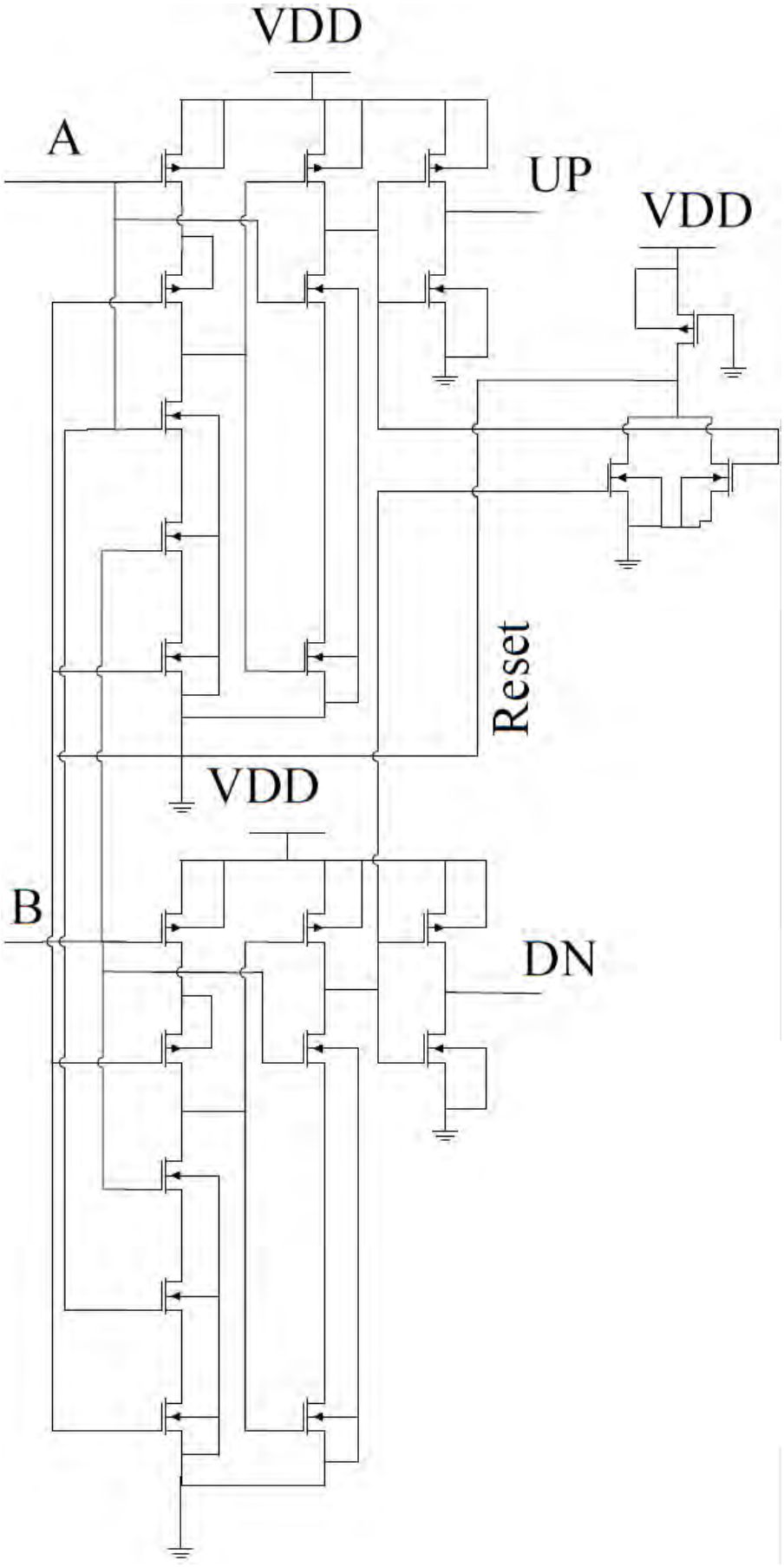


Fig. 4.1: Transistor Level PFD Circuit Diagram [38]

The following table and waveform in Fig. 4.2 explains the operating principle of Phase Frequency Detector.

TABLE 4.1

Operating principle of Phase Frequency Detector

UP	DN	Effect:
0	0	No Change
0	1	Slow Down
1	0	Speed Up
1	1	Avoid Dead-Zone

As it can be seen from the simulation in Fig. 4.2, when the rising edge of the clock A leads that of the clock B, UP goes high while the DN remain in the low position causing the DN to speed up. When B leads A, UP remains low while the DN goes high, causing the UP to speed up. The reset is activated when both the UP and DN line (outputs of the D flip flop) are both high.

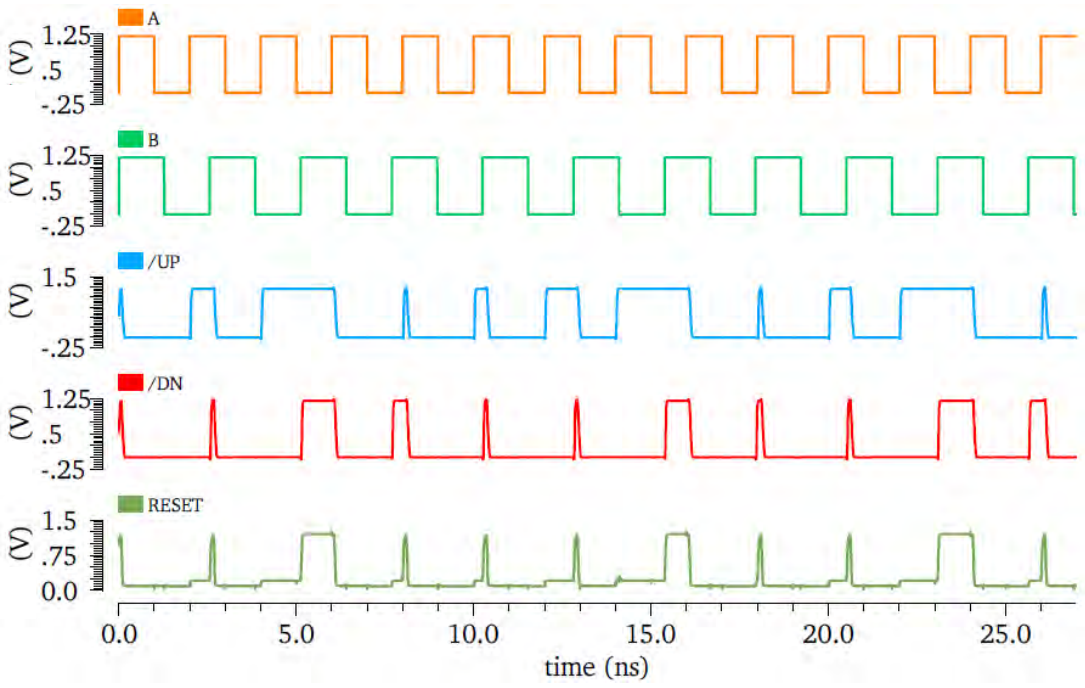


Fig. 4.2: Waveforms of PFD [38]

The UP and DN signals drive the charge pump which in turn charges and discharges the loop filter depending on the values of UP and DN signals. In the Fig. 4.2, the frequency of A is higher than that of B. Hence the charge pump must charge the loop filter to speed up the frequency of the oscillator. As it can be seen from the above figure that both UP and DN signals may simultaneously be high for a longer period of time irrespective of the frequencies of A and B and this increases the charging and discharging time of the loop filter by the charge pump. Ideally, if the frequency of A is higher than that of B, then DN signal must remain low or if the frequency of B is higher than that of A, then UP signal must remain low, otherwise it will take longer to charge and discharge as the case may be.

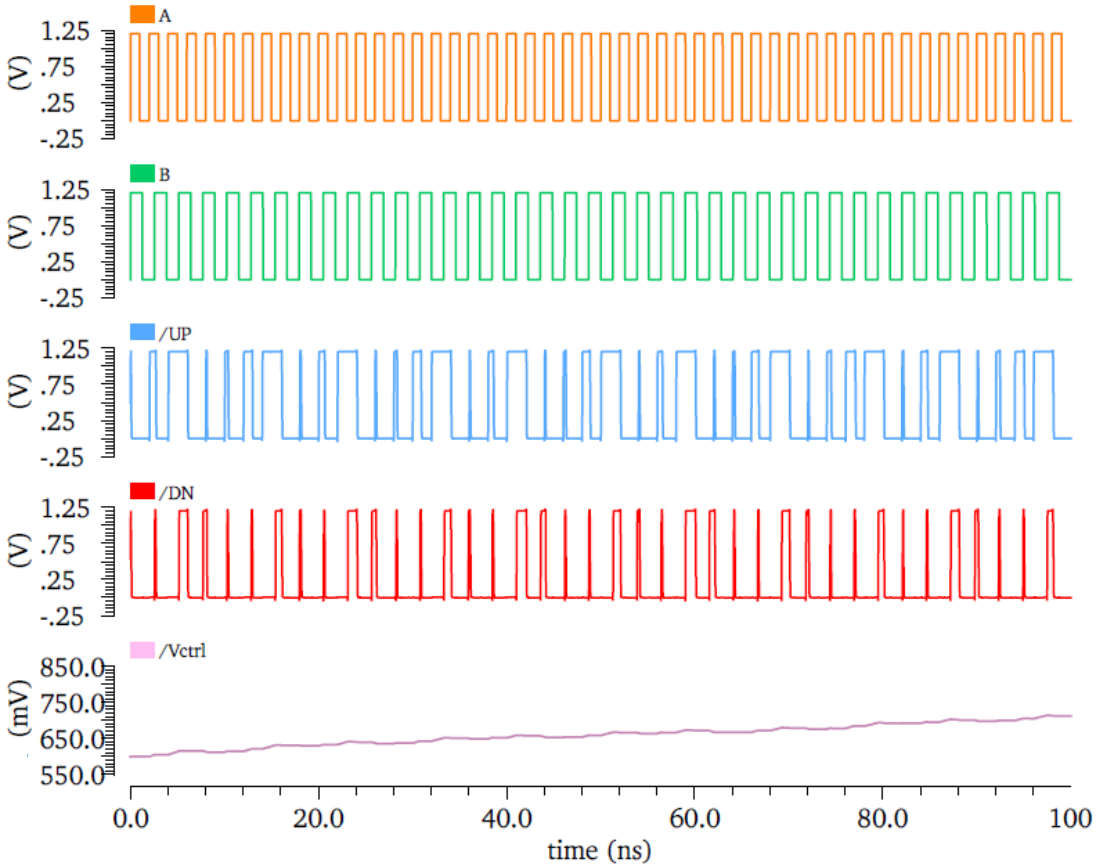


Fig. 4.3: Waveforms showing the UP, DN, and Charge Pump output signal where frequency of A is greater than that of B

In Fig. 4.3, A and B are the input signals of the two D flip flops used in the PFD and the frequency of A is higher than that of B. The UP signal remains high for longer period of time compared to the DN signal. The last waveform is of charge pump output which we will discuss in the next section in detail. It is clearly seen that the output of the charge pump is charged with the passage of time to boost up the

oscillator frequency. Fig. 4.4 explains the discharging phenomenon when the frequency of B is greater than that of A.

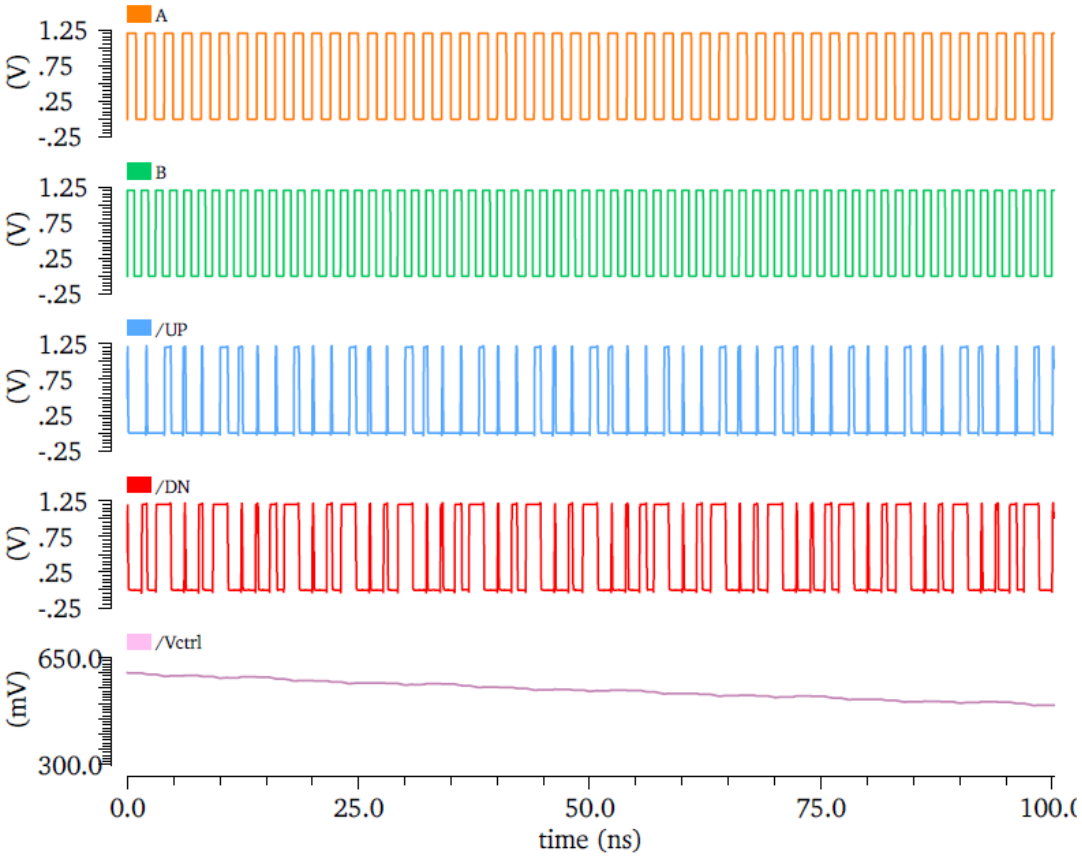


Fig. 4.4: Waveforms showing the UP, DN, and Charge Pump output signal where frequency of B is greater than that of A

To minimize the chances of UP and DN signal to be high simultaneously, the circuit which we name as "auxiliary circuit" in Fig. 4.5 is added to that in Fig. 4.1 and in the auxiliary circuit $\overline{U}$=UP and $\overline{D}$=DN. This auxiliary circuit speeds up the charging and discharging of the loop filter. The auxiliary circuit takes UP and DN as its inputs. Now the output of PFD is UPL and DNL instead of UP and DN. If we compare Fig. 4.3 with that of Fig. 4.6 and Fig. 4.4 with that of Fig. 4.7, it is clearly seen that in a given period of time, the loop filter charges and discharges fast with the addition of the auxiliary circuit. In figure 4.6 and figure 4.7, UPL and DNL are the up and down signals at the output of the auxiliary circuit.

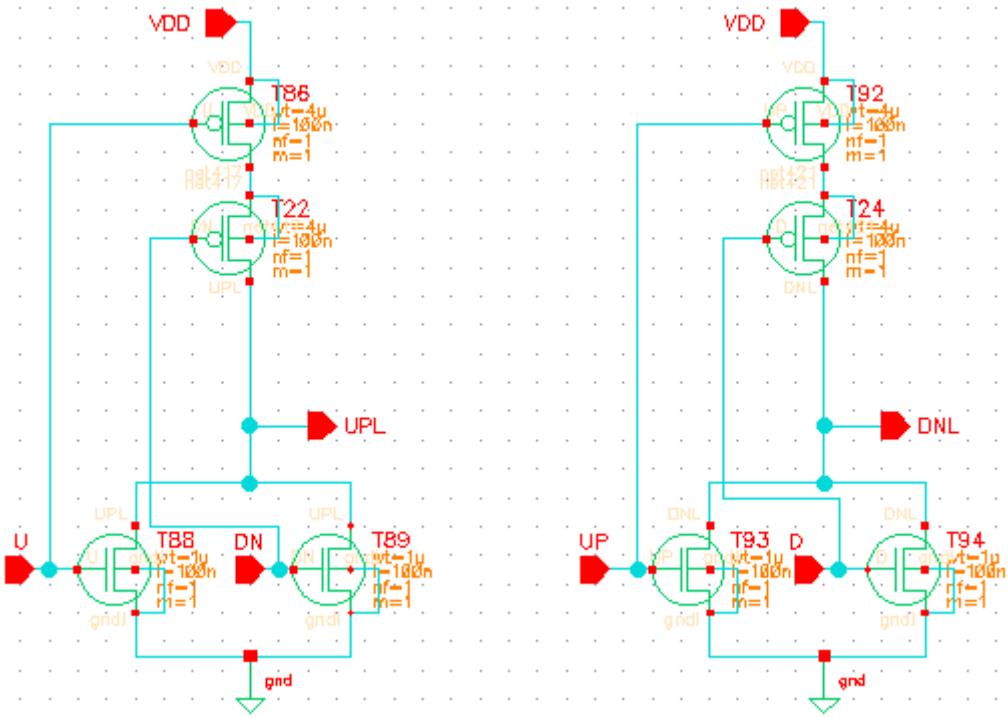


Fig. 4.5: IBM 90nm CMOS Process PFD Auxiliary Circuit Implementation

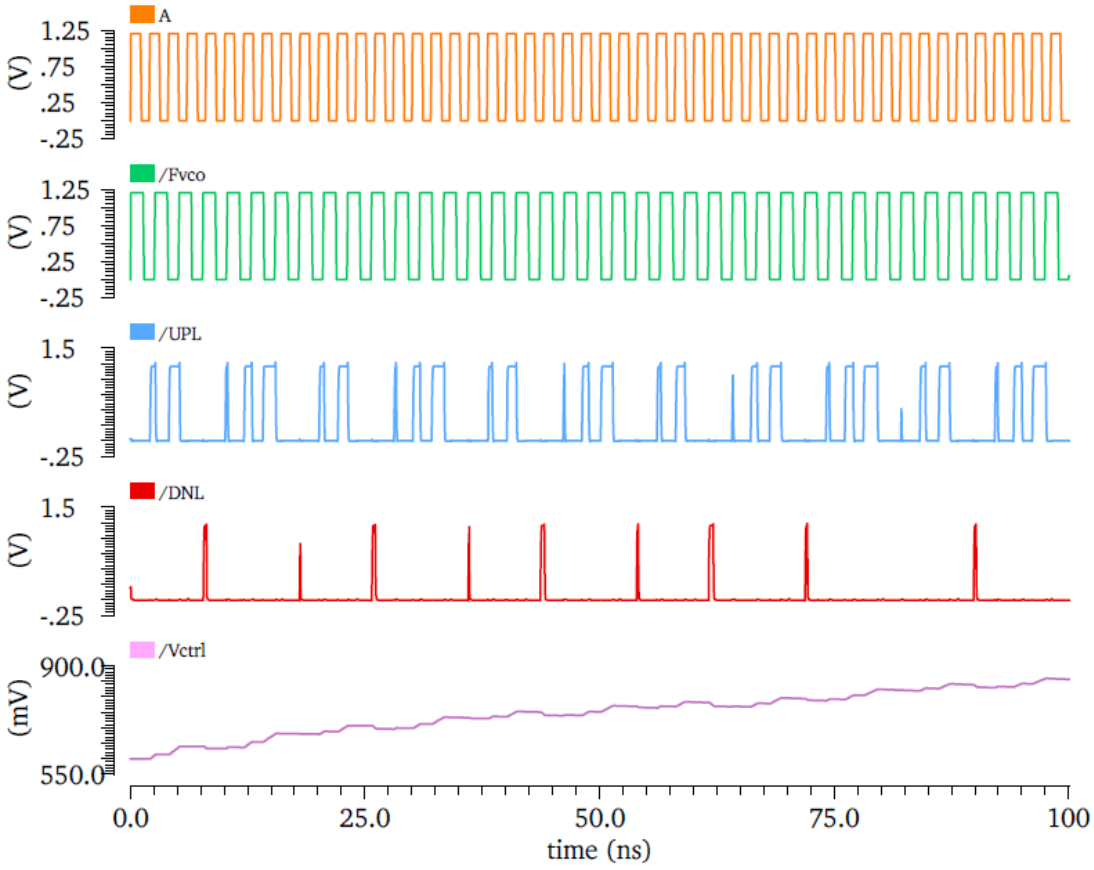


Fig. 4.6: Waveforms after addition of auxiliary circuit showing the UP, DN, and Charge Pump output signal where frequency of A is greater than that of B

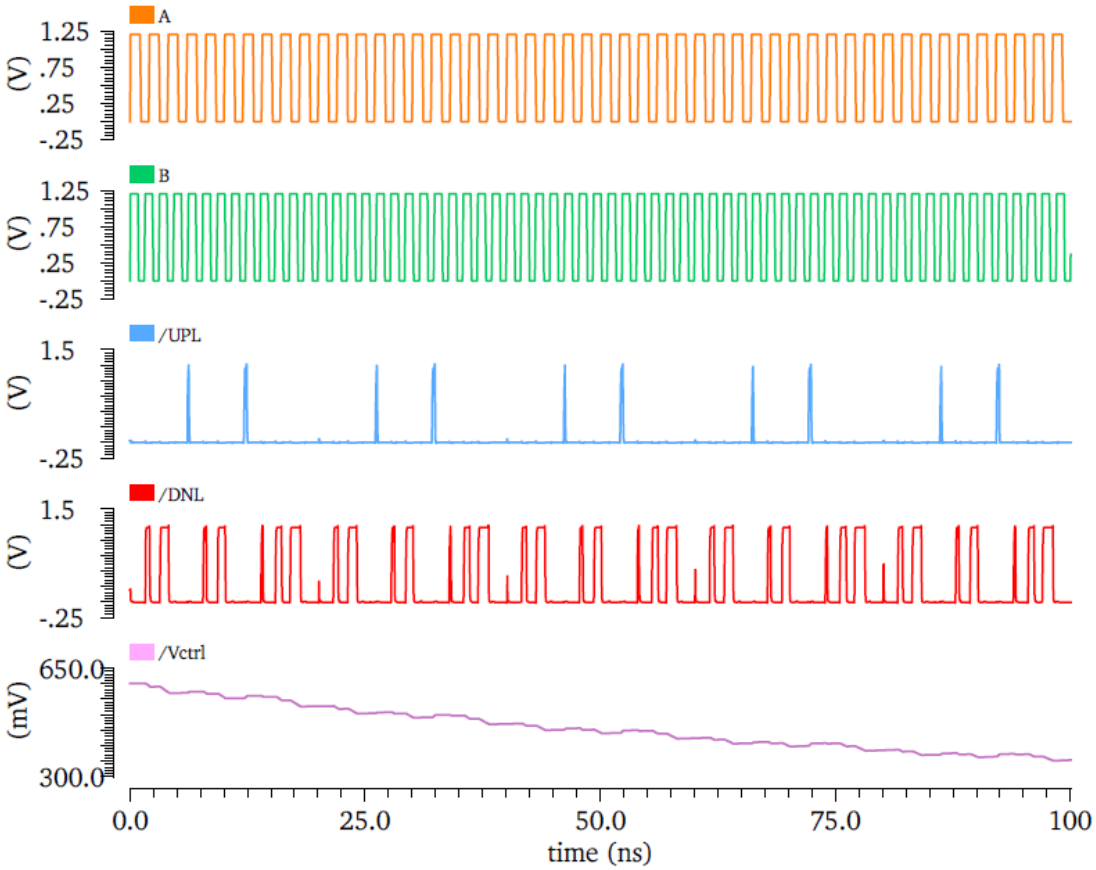


Fig. 4.7: Waveforms after addition of auxiliary circuit showing the UP, DN, and Charge Pump output signal where frequency of B is greater than that of A

4.2 Charge pump and Loop filter Design

The Charge Pump and Low Pass Filter govern the stability and smoothness of the PLL system. Generally the design of these block are overlooked but should be given considerable amount of time doing so. The Charge Pump (CP) takes the output of the PFD"s UP and DOWN pulses as its input. The Charge Pump then produces a single output depending on charging and discharging state of the Charge Capacitor (Cp). The Low Pass Filter takes the Charge Pump output, it integrates its output and low pass filters the ripples to bring it down to close to DC level. The more the ripple on the LPF output the more unstable will be the VCO. Therefore, we need to determine optimum LPF component parameter to meet both the criteria, i.e. low ripple on the V control and also close to DC level to stability purpose. We will

discuss the Charge Pump and Low Pass Filter now individually and in detail. The following diagram describes the basic block diagram of a Charge Pump.

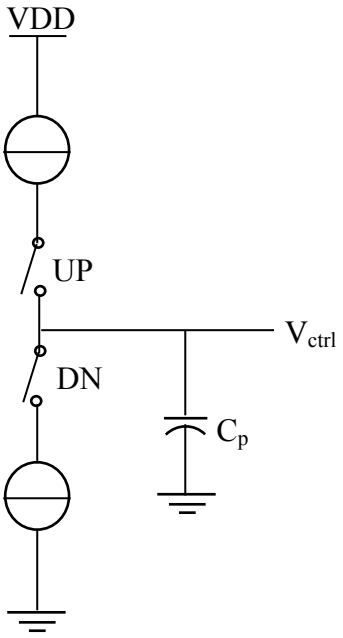


Fig. 4.8: Charge Pump Block Diagram

In the above diagram the output pulses of PFD charges or discharges the Cp capacitor via VDD and Ground. When the UP pulse is prominent the PMOS switch connected with VDD turns on and charges the Cp. The PMOS switch has an inverter connected to its input, so that to turn it "ON" when the UP is high, as PMOS turns on for logic 0. Similarly, the NMOS switch is turned "ON" when DN signal is prominent and discharges the Cp capacitor to ground. There are many non-idealities of conventional CP [40], such as current mismatch, charge share and charge injection, etc. Charge pump current mismatch due to finite output resistance of the MOS current sources is addressed in [41]. Any mismatch between the charging and discharging current can cause steady-state offset as well as dynamic jitter, known as reference spur in a PLL. Glitches [40] in the output current will increase the level of reference spurs in a PLL. It will also increase the level of jitter generation in clock and data recovery systems.

Various circuit techniques to reduce current mismatch have been reported in the literature [42]. A wide dynamic range of the charge pump is desired for the wide

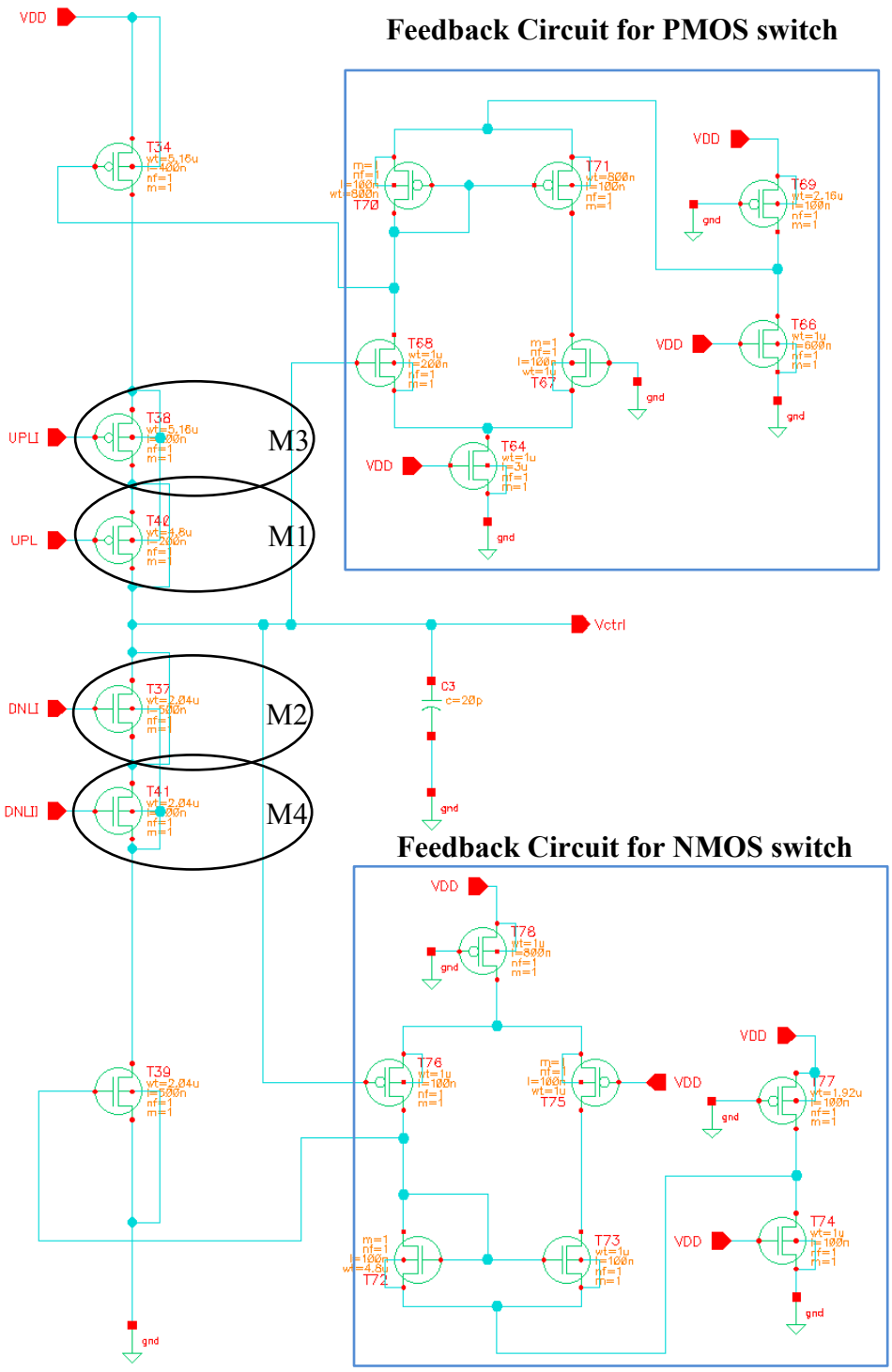


Fig. 4.9: Proposed Charge Pump Circuit (CP-1)

operating range of the PLL. To reduce the overall mismatch and the output current glitches significantly, different charge pump has been reported in [43].

The proposed CP circuit is depicted in Fig. 4.9 and we will name this CP circuit as CP-1. It uses the feedback circuit [44] to match the source and sinking current [45] with respect to the output voltage (V_{ctrl}). Fig. 4.10 shows the current variations against the output voltage variations of the charge pump circuit. For the proposed charge pump, the source/sinking current matching is nearly perfect. Moreover M1 and M2 are used to reduce the effect of charge injection [16] when the switches M3 and M4 turn off or turn on. The source and drain of M1 and M2 are shorted and is called "dummy" switch. Their gates are driven by the inverting signals on M3 and M4 respectively. They work in the manner that after M3 and M4 turns off, they turn on, the channel charge deposited by M3 and M4 are absorbed by M1 and M2 respectively.

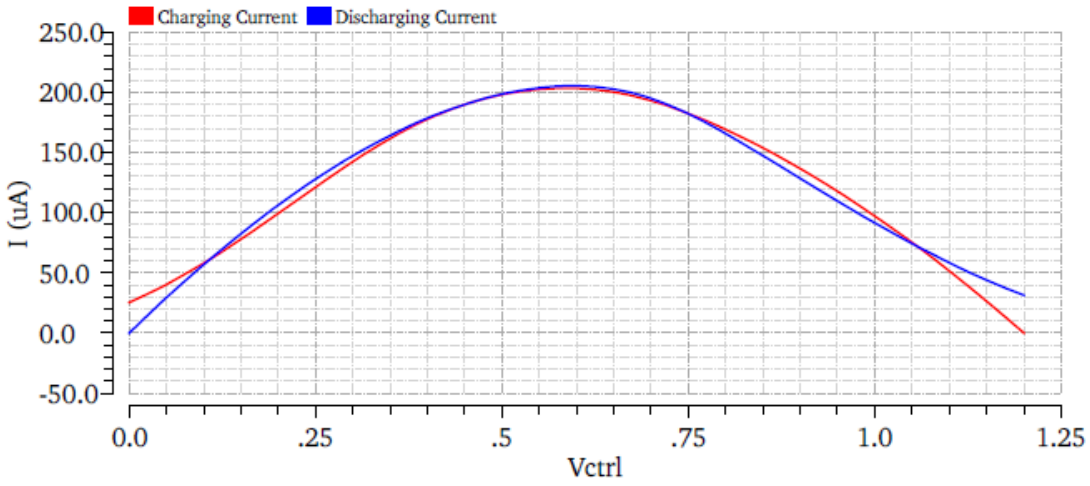


Fig. 4.10: Charge pump current matching characteristic

The low-pass filter is of second-order and the loop filter consists of two capacitors C_H and C_L and one resistor R [46]. Knowing the desired loop bandwidth, we can determine the RC parameters of the loop filter. The low pass filter as implemented is shown in the Fig. 4.11.

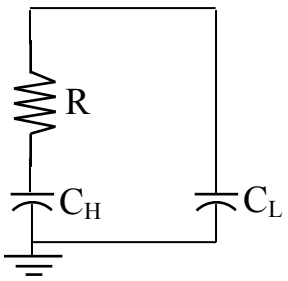


Fig. 4.11: Low Pass Filter (Loop Filter)

In our case we have assumed the following parameters for the calculation of C_H and C_L, and the resistor R:

Reference signal frequency F_{ref} = 500 MHz

Divide ratio = N

(This divide ratio depends on the desired output frequency of the frequency synthesizer. For the output frequency of 12GHz and F_{ref} = 500MHz, N=24. For 3GHz, N=6 and so on.)

The average charge pump current is assumed to be 200 μA.

Therefore, Icp = 200 μA

VCO gain is found to be

Kvco = 7.414 GHz/Volt

By the condition, the natural frequency ω_n is given by

$\omega_n = \sqrt{\frac{I_{cp}K_{VCO}}{2\pi NC_H}}$, also $\omega_n = \frac{16\pi}{T_s}$ where T_s is the Settling time or the Lock-in time.

From the above formula, we can calculate C_H as follows:

$$C = \frac{I_{CP}K_{VCO}}{2\pi N\omega_n^2}$$

From $\xi = \frac{\omega_n RC_H}{2}$, we get $R = \frac{2\xi}{\omega_n C_H}$ depending on the choice of ξ.

In this work, for the best performance of the system, we have selected the values of capacitors and resistor as follows:

C_H = 50 pf, C_L= 25 pf and R = 1 KΩ.

The two outputs from the proposed PFD are combined using a charge pump CP-1 and for convenience we will name the two input clocks of PFD as F_{ref} and F_{div} instead of A and B which were used in the previous section. Fig. 4.12 shows the UP and DN pulses for $F_{ref} > F_{div}$. The figure also shows the corresponding output current (charging or discharging). From the figure, it is noticed that the output current is accompanied by glitches which is undesirable as it will increase the level of

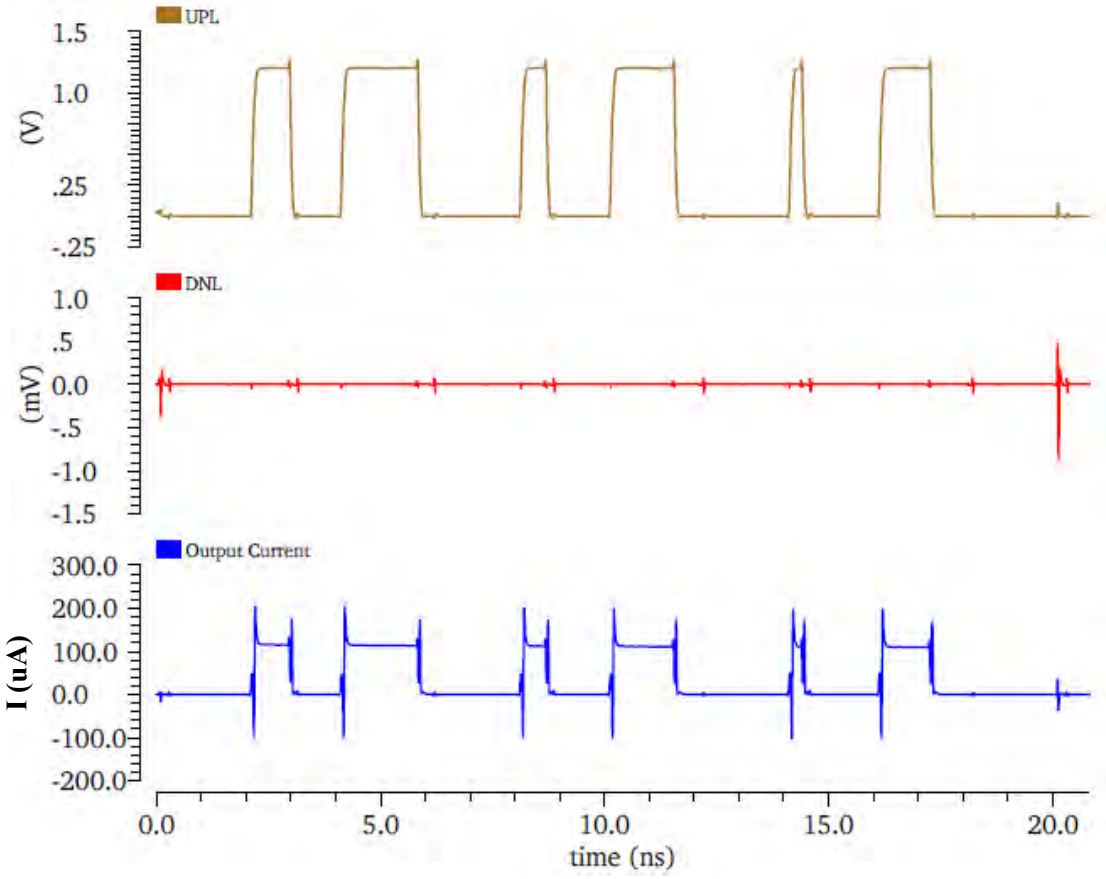


Fig. 4.12: Waveform for CP-1 ($F_{ref} > F_{div}$)

reference spurs in a PLL. In particular, two small resistances R1 and R2 and two capacitors C1 and C2 are added to the CP-1 circuit, which can suppress the output current glitches effectively. The addition of R1, R2 and C1, C2 also speeds up the charging and discharging phenomena by increasing the output current for the same biasing condition. Fig. 4.13 shows the modified charge pump and we will name this as CP-2. The corresponding waveforms and the output current are shown in Fig.

4.14. The output waveform clearly shows that the output current glitches have been effectively suppressed.

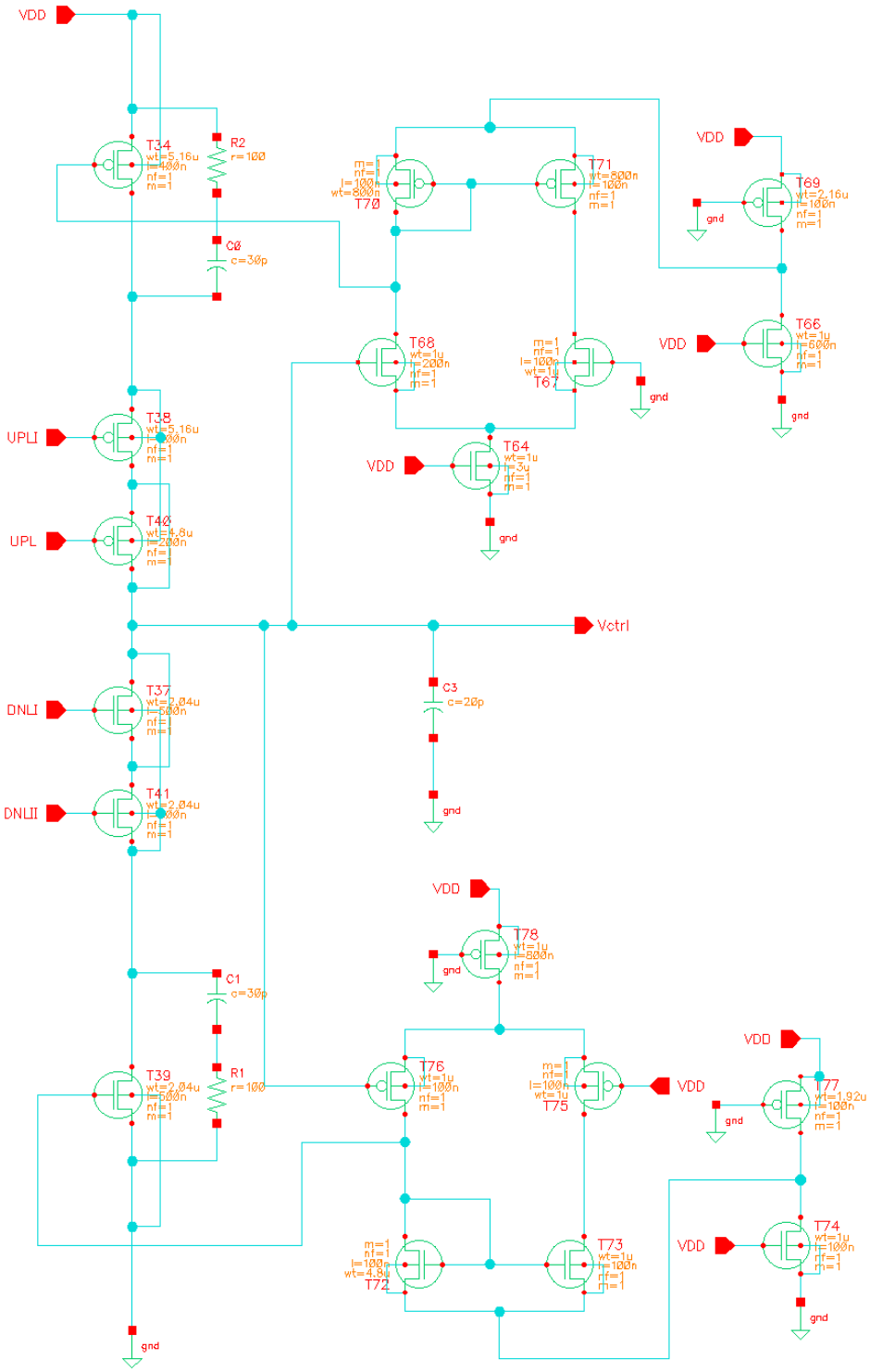


Fig. 4.13: Modified Proposed Charge Pump Circuit (CP-2)

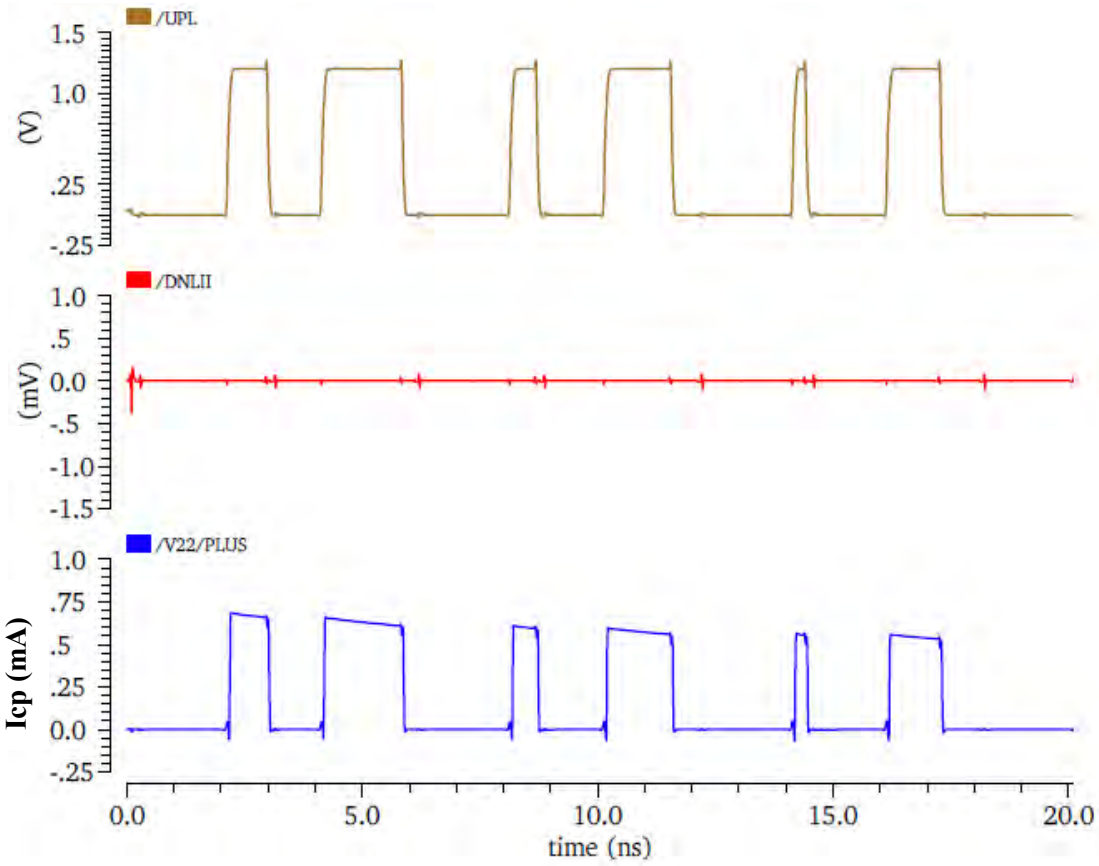
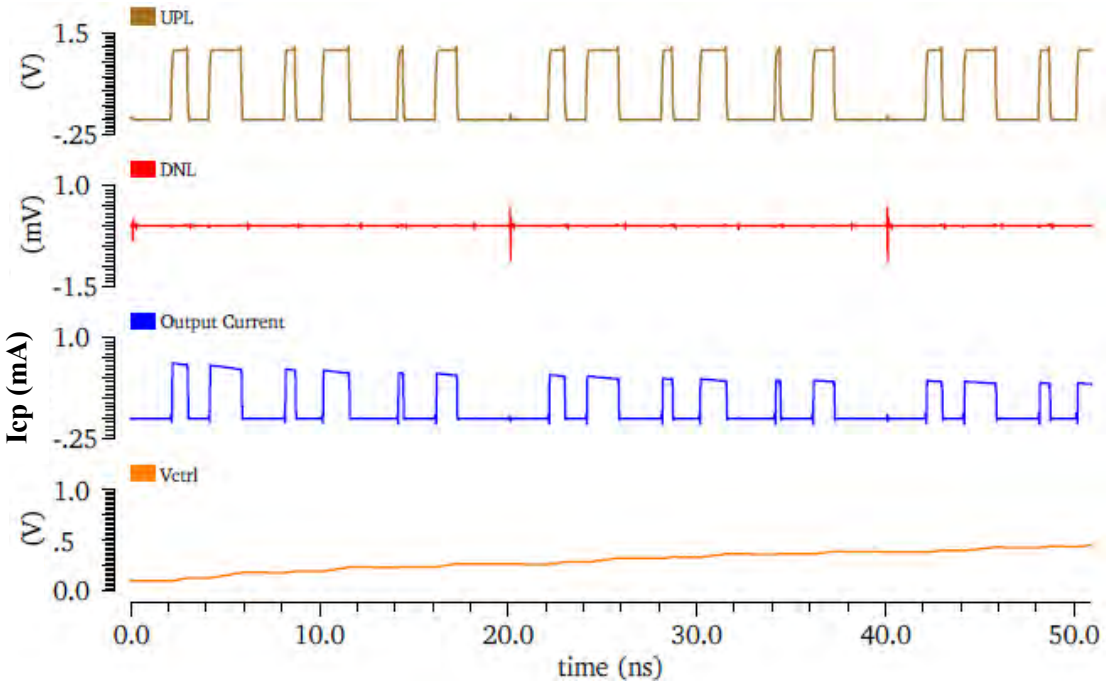
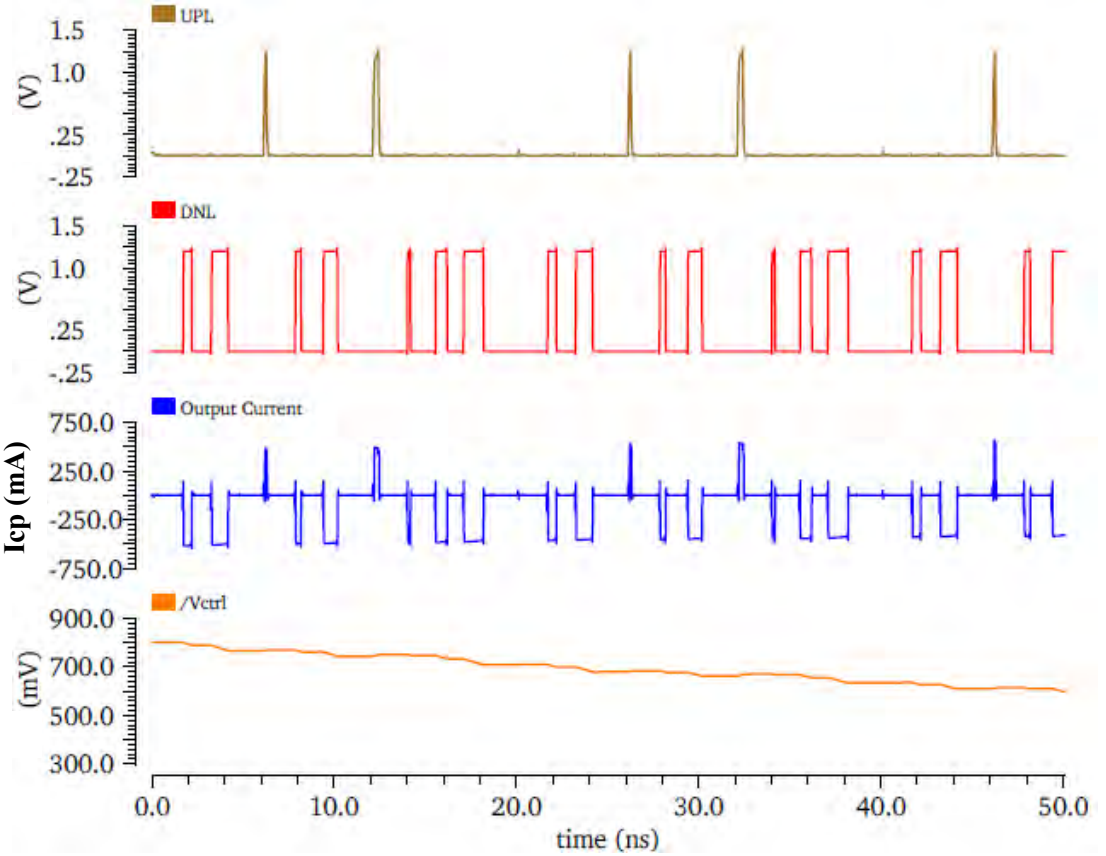


Fig. 4.14: Waveform showing no glitches in the output current for CP-2 ($F_{ref} > F_{div}$)

Fig. 4.15 clearly illustrates the charging and discharging phenomena. In Fig. 4.15 (a), Vctrl increases with time as Fref > Fdiv and the charging current is free from glitches since we have used the modified charge pump CP-2 and in Fig. 4.15 (b), Vctrl decreases over the time to show the discharging phenomena.



(a)



(b)

Fig. 4.15: Waveform for CP-2 (a): ($F_{ref} > F_{div}$) (b): ($F_{ref} < F_{div}$)

Due to the addition of extra resistances R1 and R2 in the proposed modified charge pump CP-2, one may conclude that this will increase the total phase noise of the circuit. But the simulation results obtained in Fig. 4.16 show that it has no deteriorating effect on the phase noise of the circuit. Rather it has somewhat improved its phase noise at 1 MHz offset frequency.

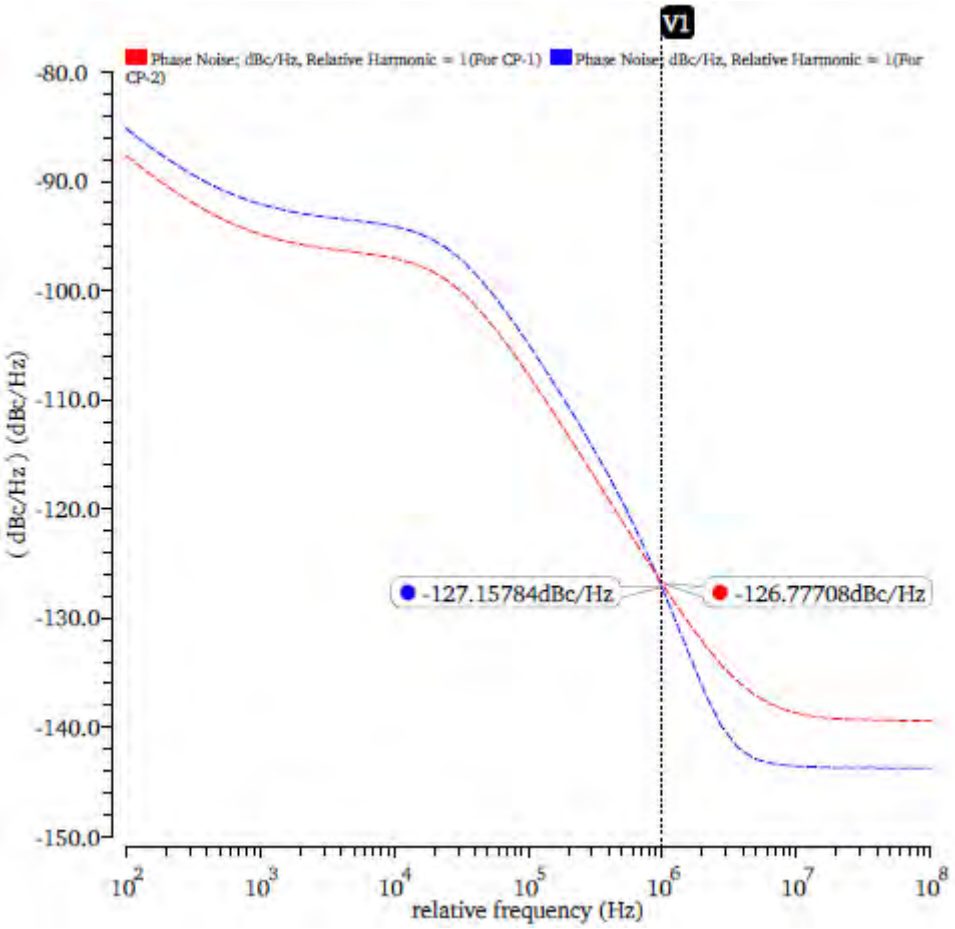


Fig. 4.16: Phase noise plot for PFD-CP-1 and PFD-CP-2

The plot of power dissipation for the circuit is shown in Fig. 4.17. The average power dissipated is calculated over a period of 100 ns and is found to be 1.717 mW.

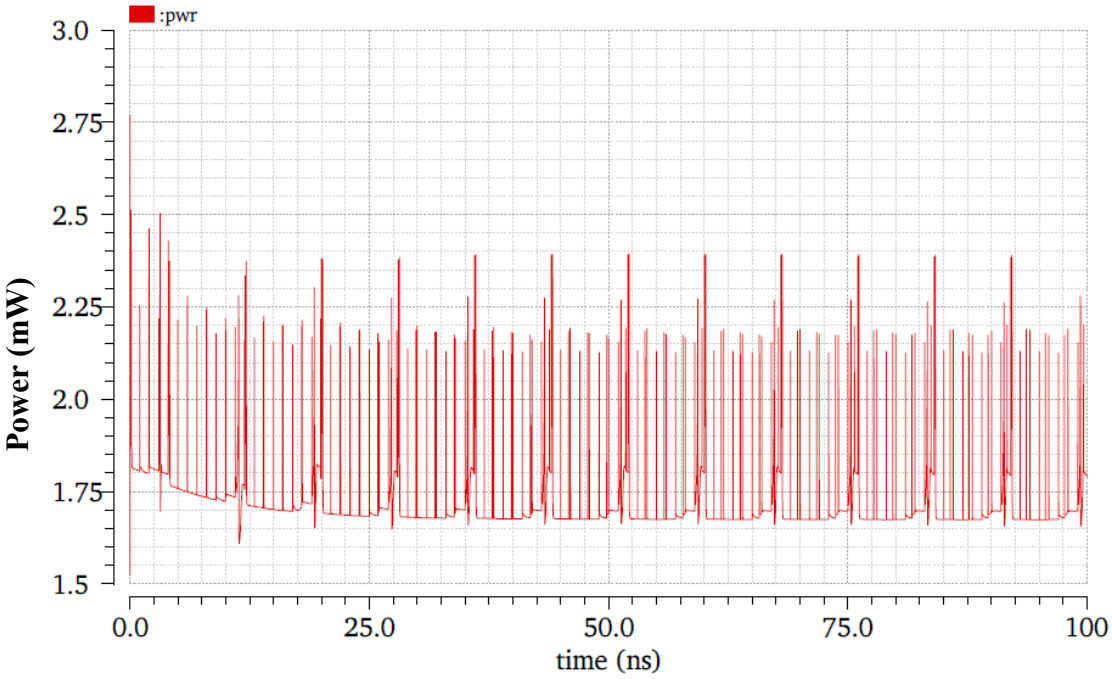


Fig. 4.17: Power Dissipation plot of the PFD-CP circuit

Fig. 4.18 shows the combined layout of the PFD and CP without resistor and capacitor added. It occupies an area of 74.22 µm×33 µm = .00244 mm^2.

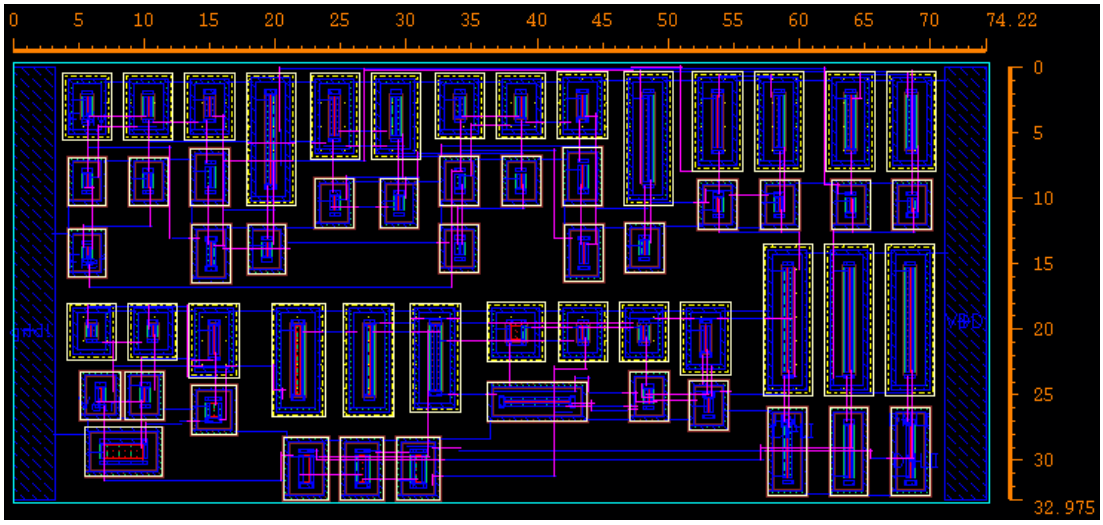


Fig. 4.18: PFD and CP Layout

The layout of PFD and CP including the Loop Filter and the added resistors and capacitors in the CP is shown in Fig. 4.19. A large area is occupied by the capacitor

as can be seen in the figure. The total area occupied by the circuit is 124.9 µm×106.85 µm = .01329 mm^2.

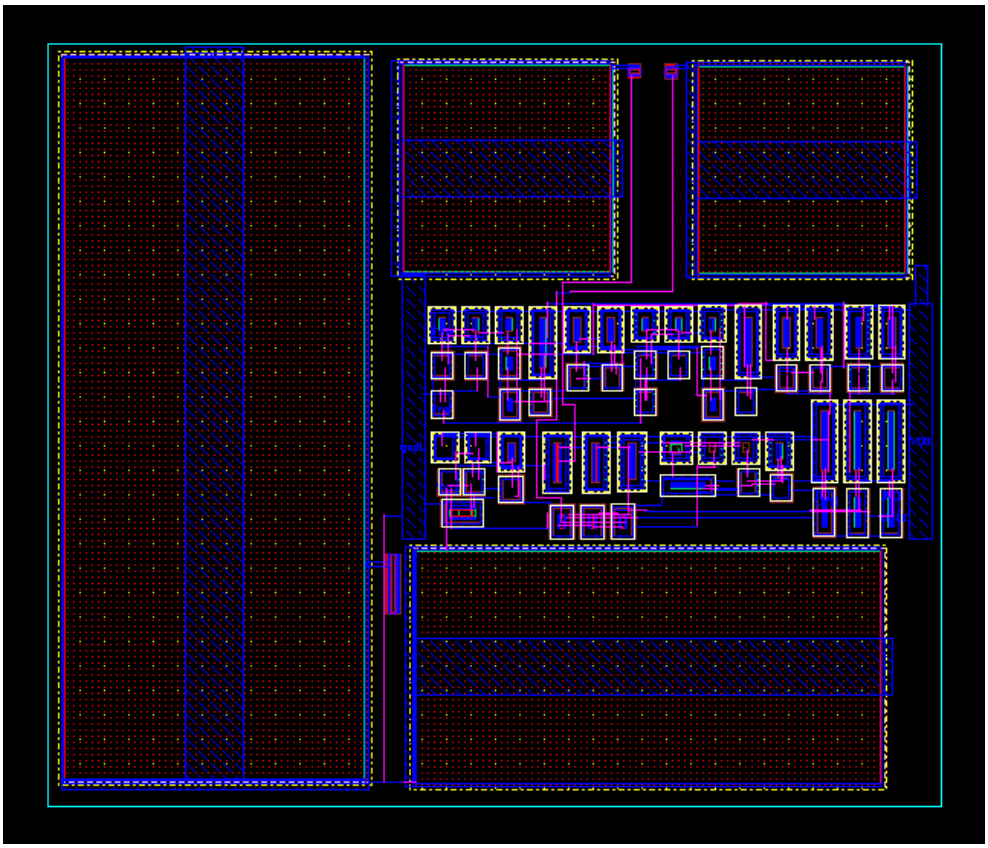


Fig. 4.19: PFD, CP and Loop Filter Layout

Post Layout Simulation

The post layout parasitic capacitance and resistance were extracted using Assura QRC in Cadence software. Fig. 4.20 sows the capture of the layout with

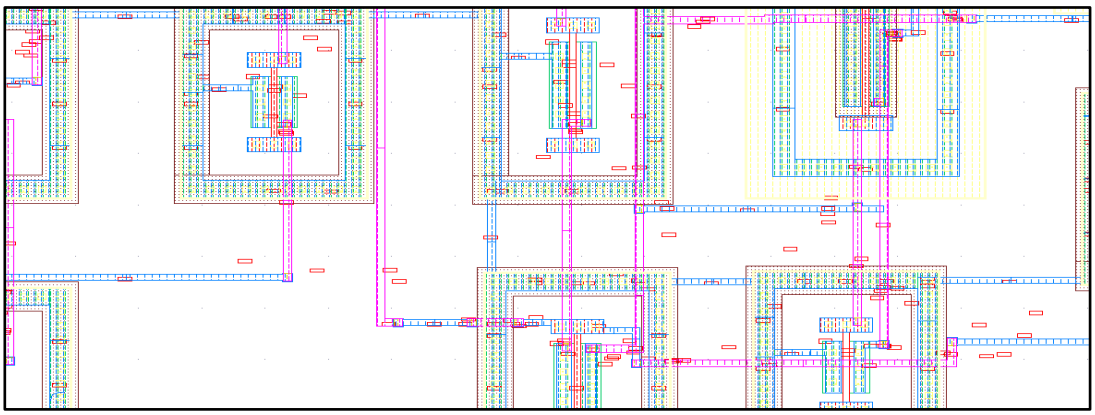


Fig. 4.20: PFD, CP and Loop Filter Layout showing Parasitic

parasitic capacitors and resistors. A closer view of these capacitors and resistors is depicted in Fig. 4.21. For this small circuit, the numbers of parasitic capacitors were found to be around 1650 but these capacitors are in the range of atto farad (aF) to femto farad (fF). The numbers of parasitic resistors were counted to be around 1150 and are within a value of 10 ohm.

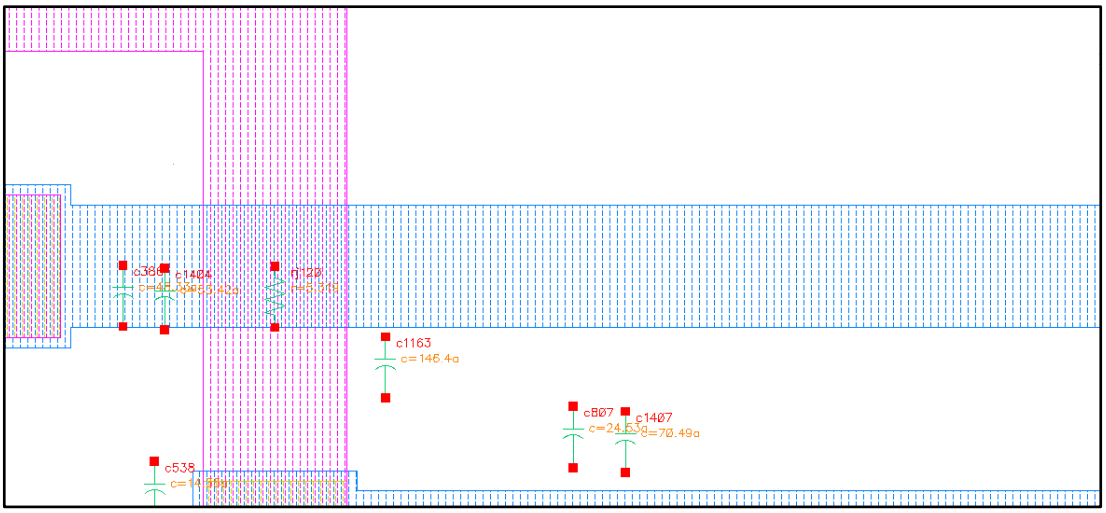


Fig. 4.21: Closer view of Fig. 4.20

	Numbers Counted	**Values**
Parasitic Capacitor	1641	aF-fF
Parasitic Resistor	1151	0.1-10 ohm

The addition of parasitics degrades the performance of the circuit and sometimes leads to undesirable results. As expected, in this circuit the performance has degraded in terms of speed but we have obtained satisfactory performance with respect to glitches in the output current and the up and down signals. Fig. 4.22 and Fig. 4.23 can be compared with that of Fig. 4.15(a) and Fig. 4.15(b) respectively. Fig. 4.24 shows the post-layout phase noise plot of the circuit. From the simulated result of the phase noise that remains unaffected at the offset frequency of 1 MHz.

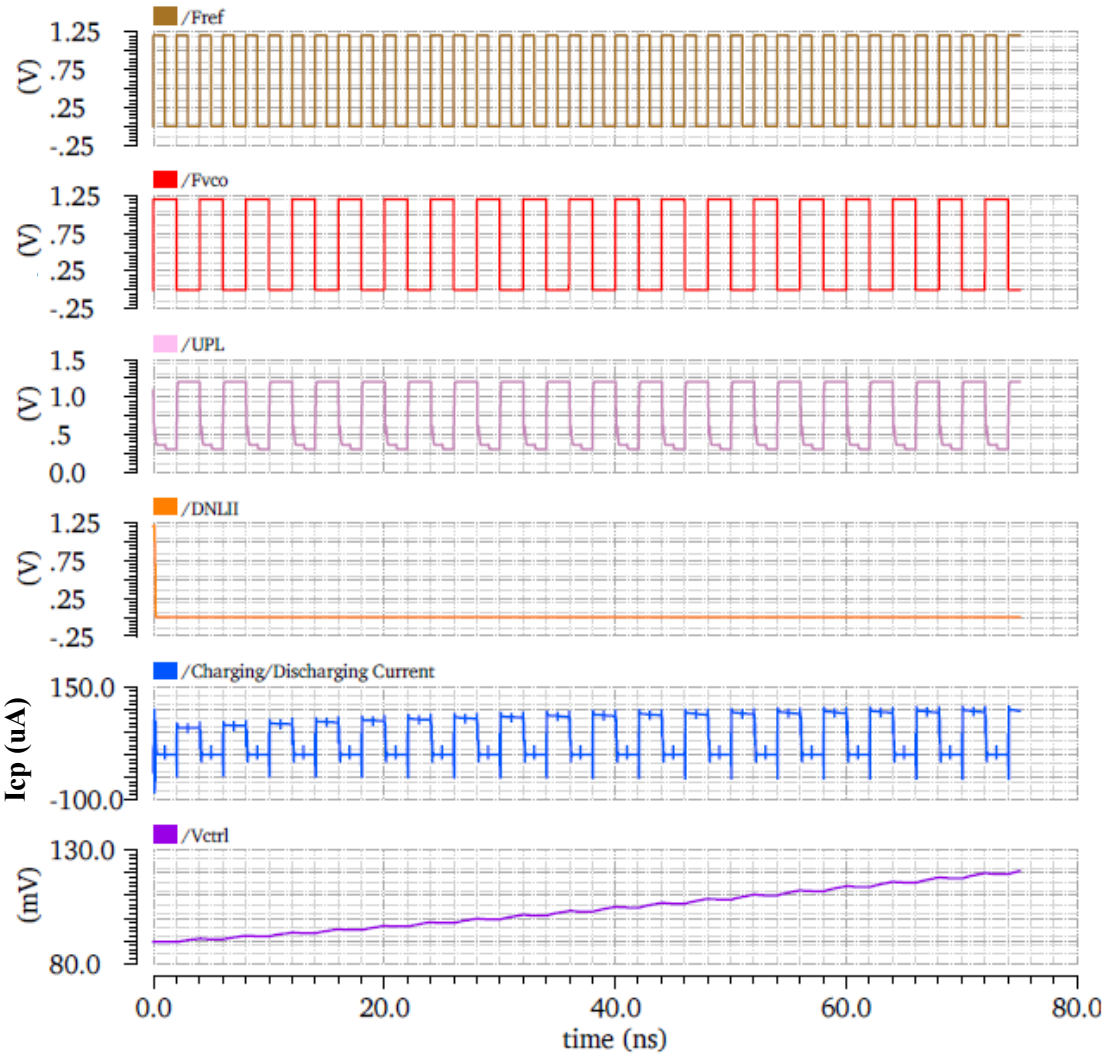


Fig. 4.22: Post Layout Waveforms showing the UP, DN, and Charge Pump output signal where frequency of F_{ref} is greater than that of F_{div}

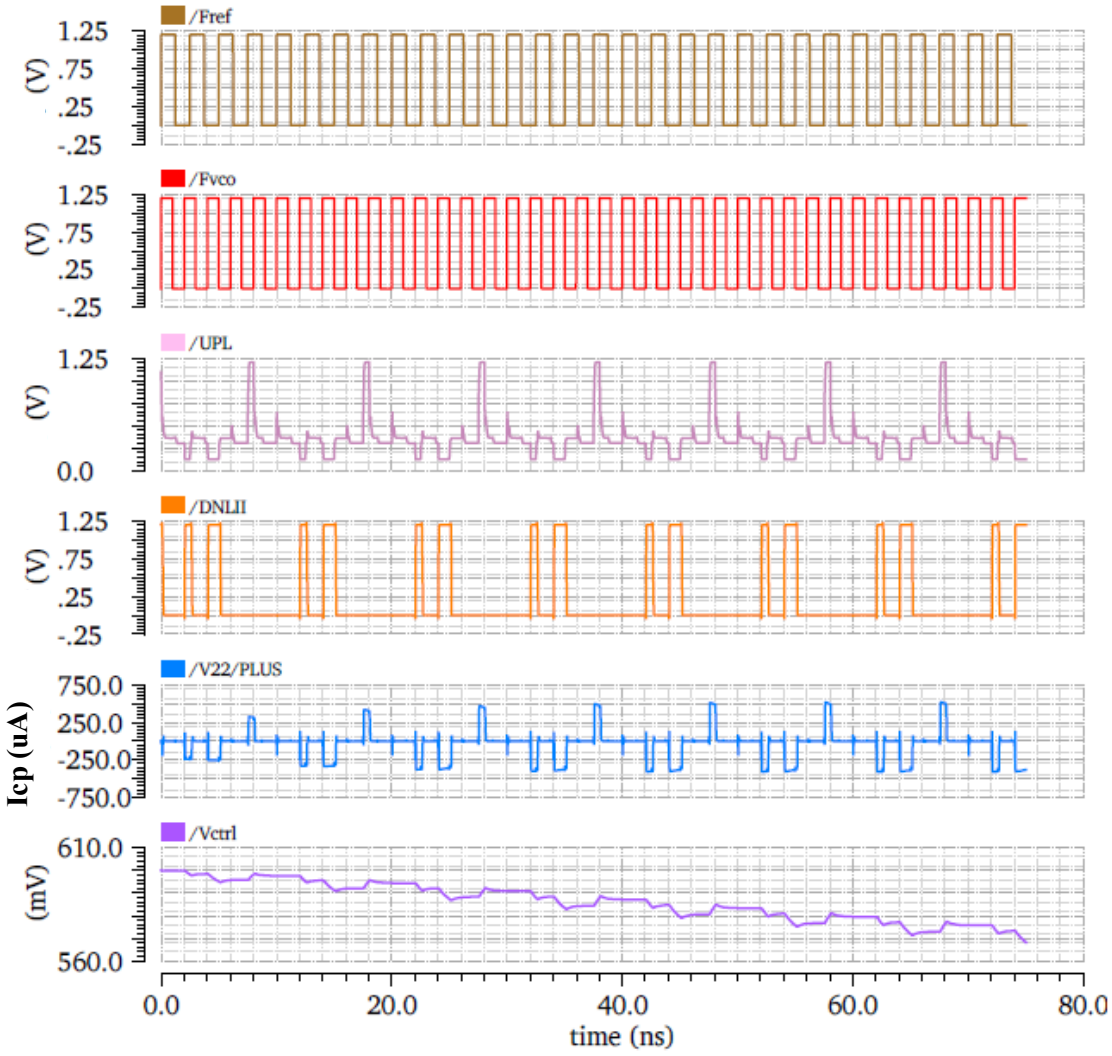


Fig. 4.23: Post Layout Waveforms showing the UP, DN, and Charge Pump output signal where frequency of F_{div} is greater than that of F_{ref}

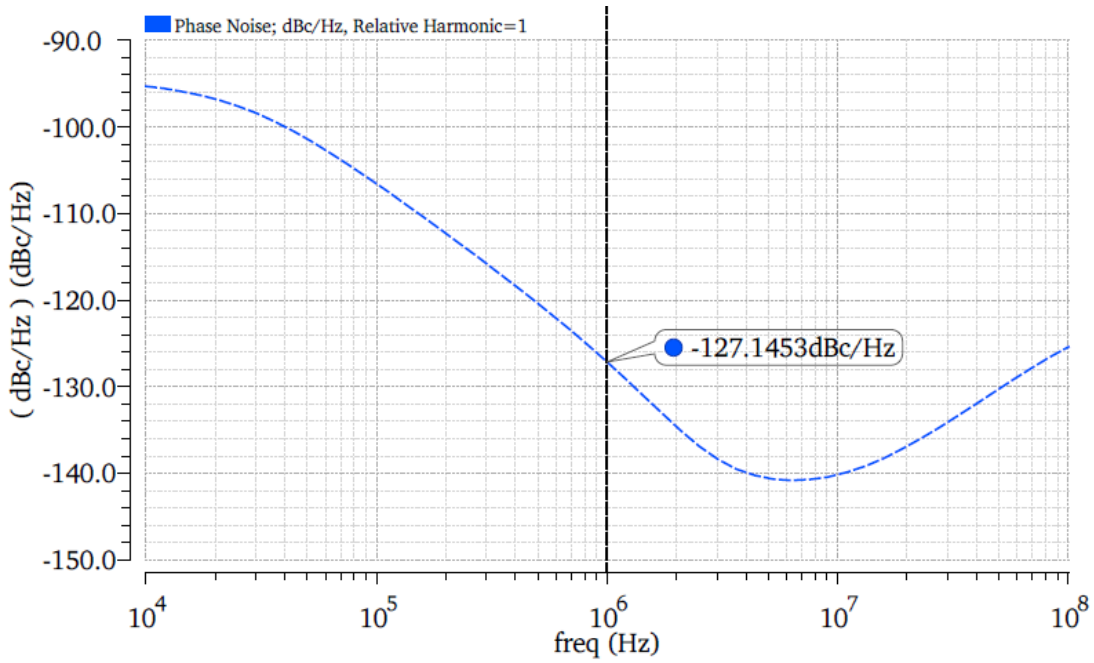


Fig. 4.24: Post-layout Phase noise plot for PFD-CP-2

4.3 Voltage Controlled Oscillator Design

A Voltage-Controlled Oscillator (VCO) is a circuit that provides a varying output signal whose frequency can be adjusted over a range controlled by a dc voltage. VCOs are important building blocks in PLLs. The design of complementary metal–oxide–semiconductor (CMOS) VCOs with low phase noise is a challenging research topic and has been studied extensively in recent years [47]–[50].Many traditional oscillators are based on LC resonators. Due to the difficulties in the implementation of on-chip inductors and the limited frequency tuning range, resonator-less VCOs have drawn significant attention for system-on-a-chip solutions[50]–[53]. Among many possible circuit topologies, ring oscillators are promising candidates due to their ease of implementation and wide frequency tuning range. They are compatible with digital CMOS technologies and occupy small chip area. The phase noises for ring oscillators have traditionally been much higher than that of resonator-based oscillators.

A ring VCO has been designed for our frequency synthesizer in a silicon CMOS 90nm technology and has been measured for its performance. The VCO provides a wide tuning range (2.51 GHz-12.68 GHz) and constant gain (Kvco) while

consuming maximum 1.96 mW for 12.68 GHz output frequency. The topology of the proposed delay cell is shown in Fig. 4.25. It contains a source coupled-differential pair and symmetric loads [54] which provide good control over delay and high dynamic supply noise rejection [55].

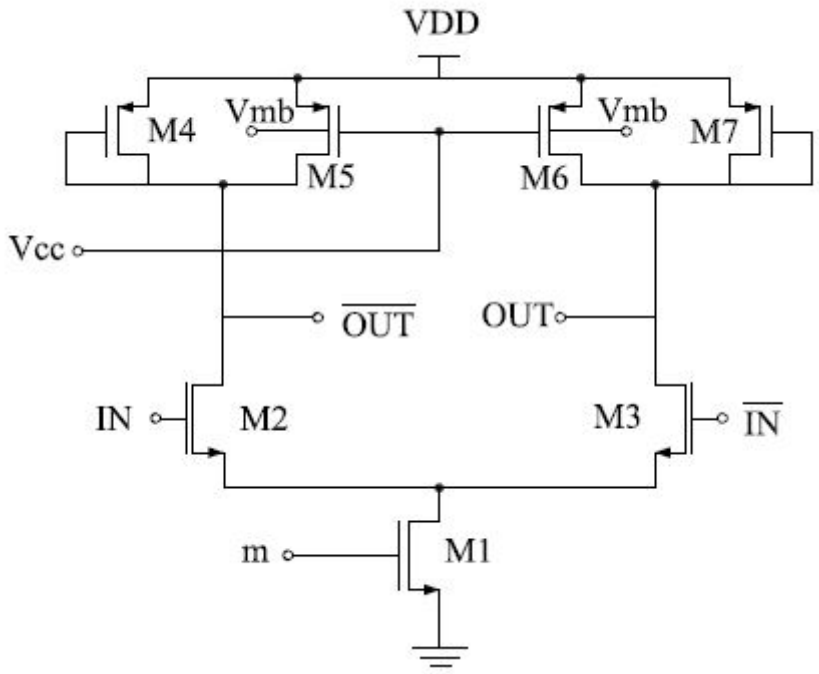


Fig. 4.25: Delay cell for the proposed ring oscillator with a source-coupled pair and symmetric loads

The proposed ring VCO is shown in Fig. 4.26. It is based on a four-stage differential ring oscillator [56]. To improve the load linearity [57] and to achieve higher operating frequency, the bulk of M5 and M6 are connected to Vmb where Vmb=0.5V. M4 and M7 are connected as diode. Fig. 4.27 shows both the bias circuit and the transistor level design of the proposed VCO.

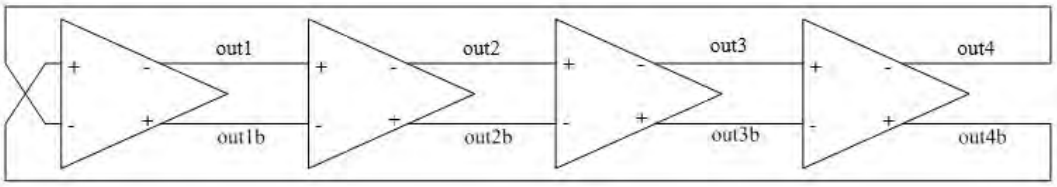


Fig. 4.26: Four-Stage Differential Ring VCO

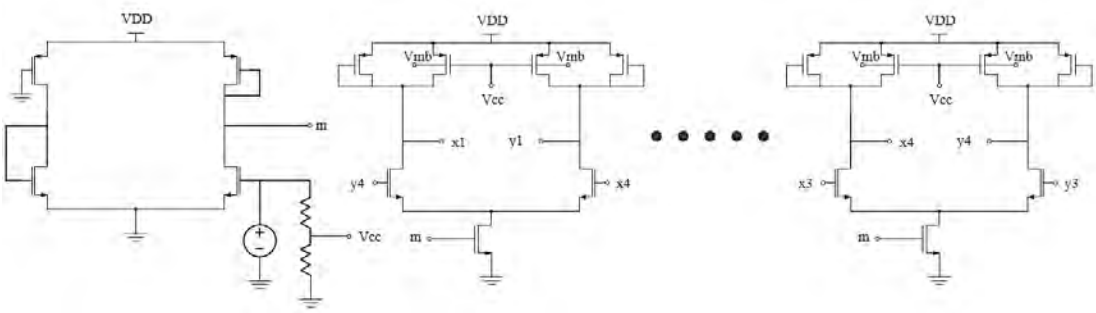


Fig. 4.27: Schematic of the proposed VCO

Design parameters of a VCO

Besides the oscillation frequency and phase noise, there are some other important performance parameters for a VCO such as tuning range, tuning linearity, output amplitude and power consumption.

Tuning Range

From the schematic level simulation when control voltage (Vctrl) is at 0.6 V, the oscillation frequency is 8.19 GHz. The tuning range property of this design is shown in Fig. 4.28. The maximum oscillation frequency is 12.68 GHz when Vctrl is at 1.2 V whereas the minimum oscillation frequency is 2.51 GHz.

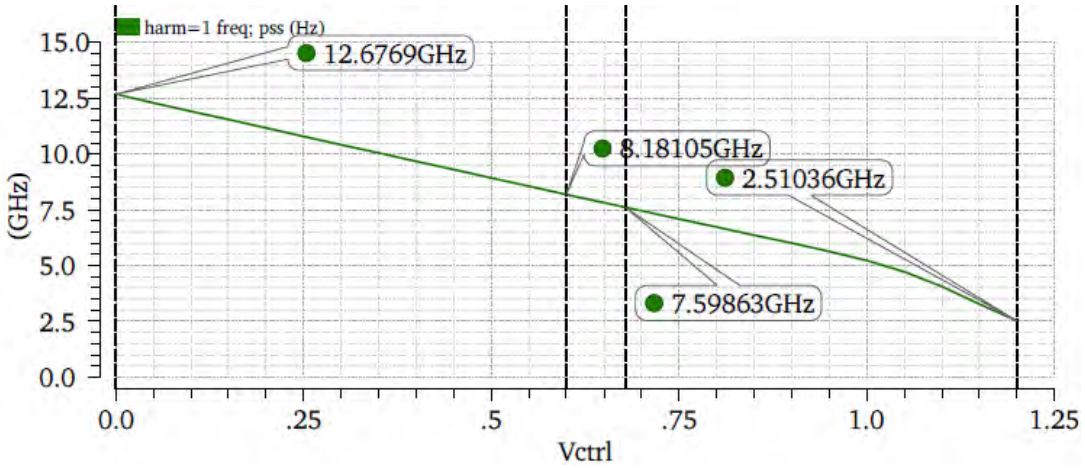


Fig. 4.28: Tuning range characteristic of the proposed VCO

A tuning range of 133.9% (Tuning range/ Centre frequency) [56] from 2.51 GHz to 12.68 GHz is achieved for the VCO as shown in the above figure. Frequency

Spectrum plot for the control voltage of 0 V and 1.2 V is presented in Fig. 4.29 and Fig. 4.30 respectively.

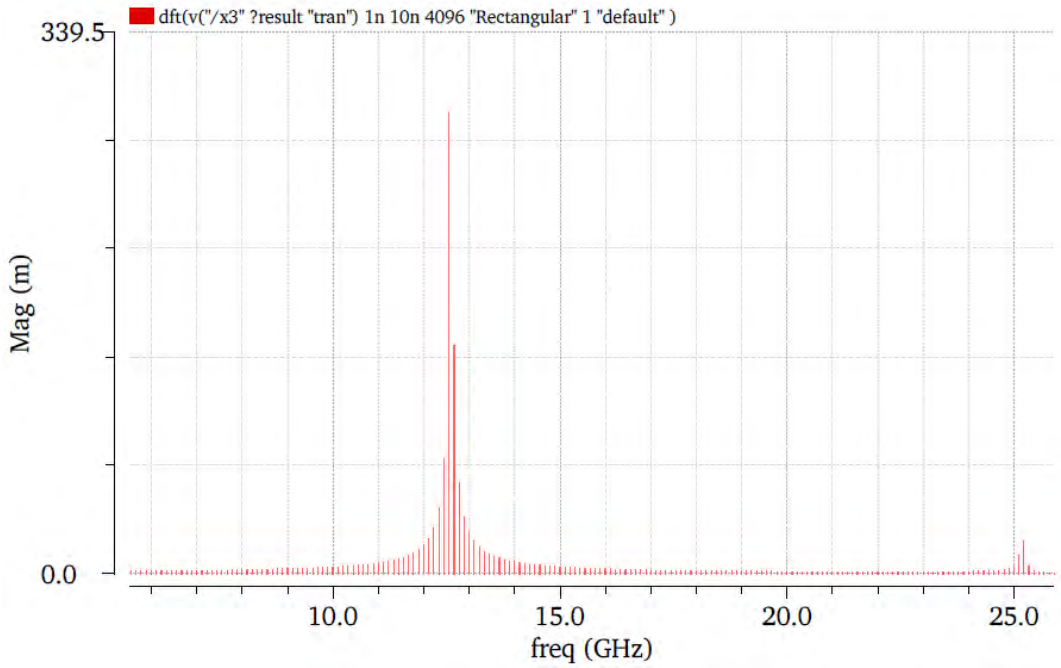


Fig. 4.29: Frequency Spectrum plot for Vctrl=0 V

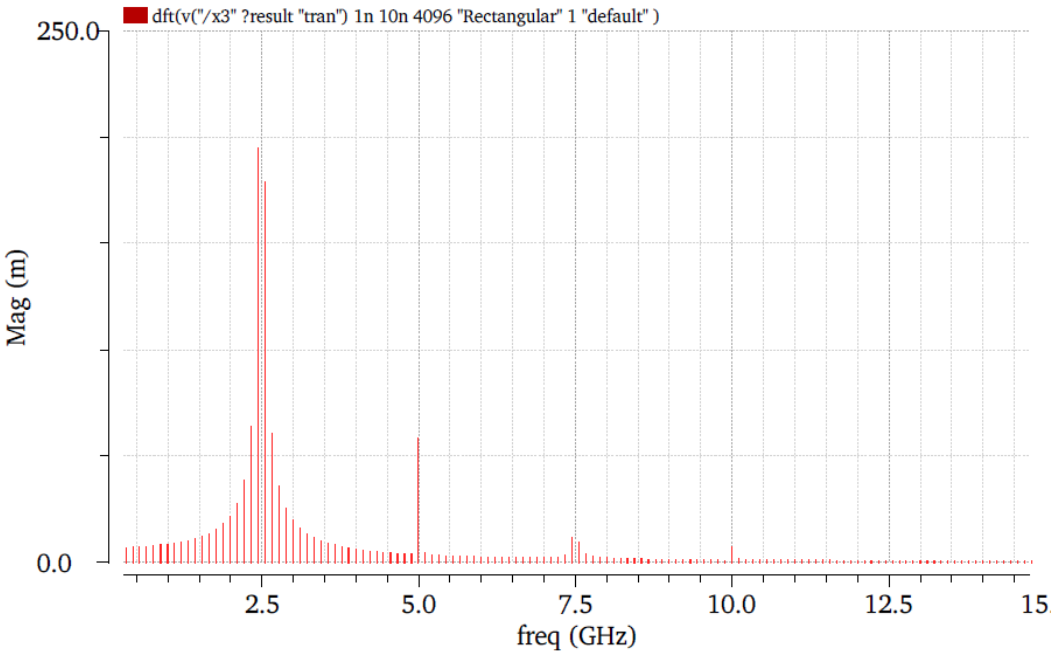


Fig. 4.30: Frequency Spectrum plot for Vctrl=1.2 V

Tuning Linearity/ Gain of VCO (K_{VCO})

When the tuning range is not linear then the VCO gain is an averaged value from the minimum to the maximum oscillation frequency as shown in Fig. 4.31 which shows much higher gain in the middle part of the tuning range than the two extremes. Then in that case the nonlinear behavior seriously degrades the settling behavior of PLL. In the proposed VCO, the nonlinearity has been minimized by properly configuring the VCO structure which is a challenge for high performance VCO design.

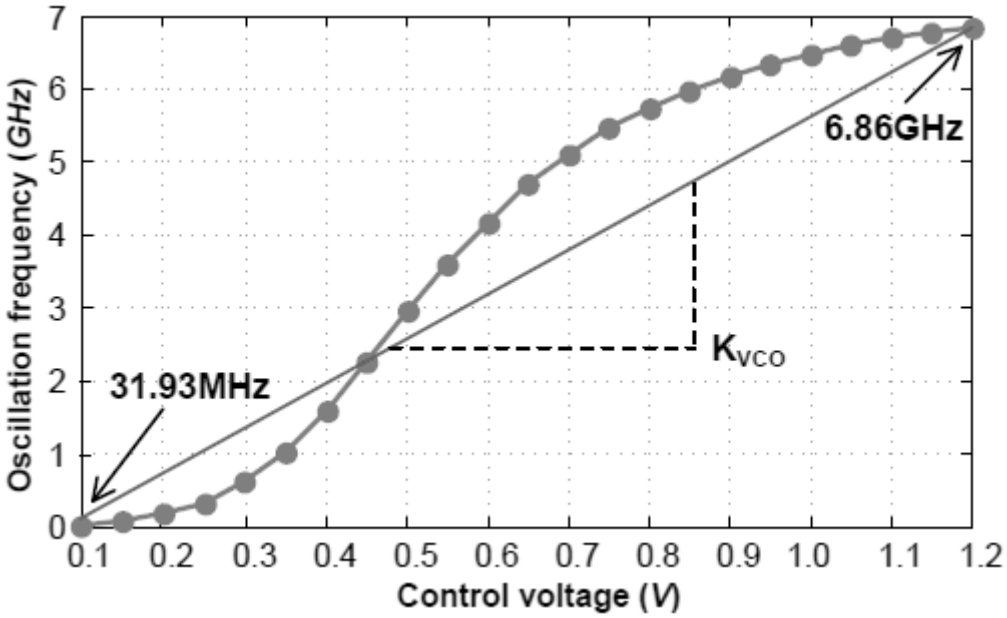


Fig. 4.31: Frequency of oscillation Vs Vctrl for non-linear tuning range

Fig. 4.32 shows the gain (K_{VCO}) of the proposed VCO and is found to be highly linear within the operating range and is the best reported in the literature.

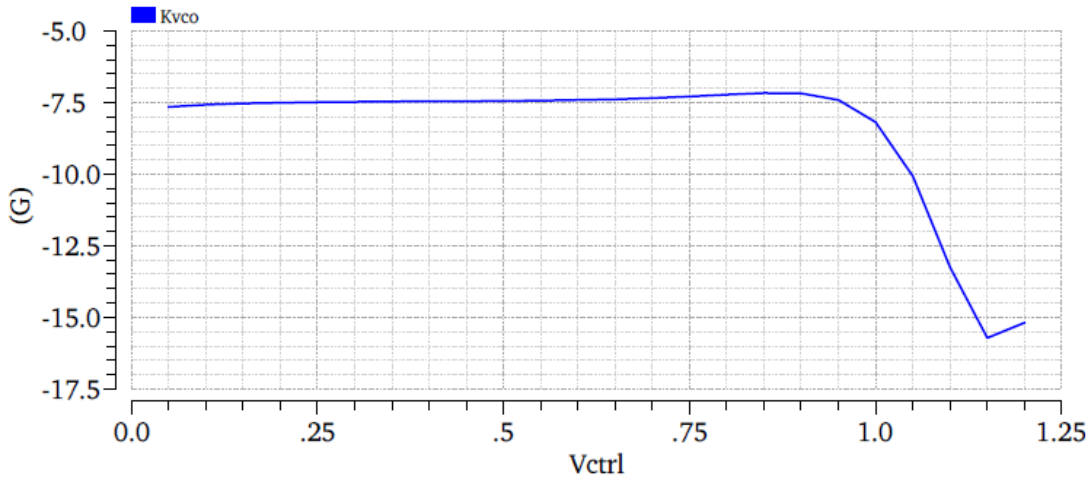


Fig. 4.32: Gain of the VCO (K_{VCO}) Vs Vctrl

Output Amplitude

It is desirable to maintain large output oscillation amplitude over the full frequency band, thus making the waveform less sensitive to noise and interference. However, in practice this is not always the case. Fig. 4.33 shows the output waveform for the proposed VCO with different control voltages and hence different oscillation frequencies.

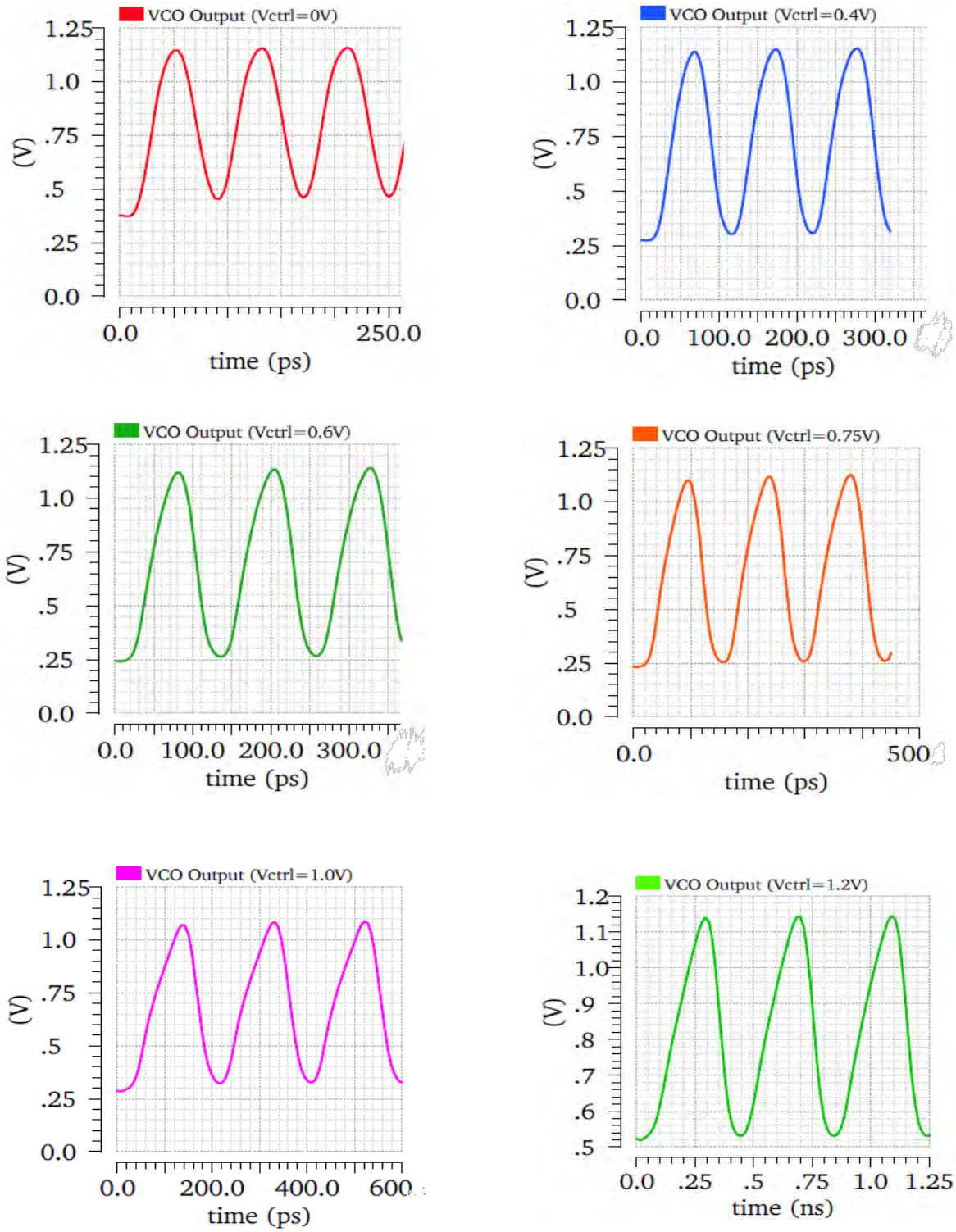


Fig. 4.33: Output Waveform of the proposed VCO for different values of Vctrl

Fig. 4.34 compares the output waveforms of the VCO and shows that the peak to peak voltage of oscillation is large in middle range of the tuning range than at the extremes.

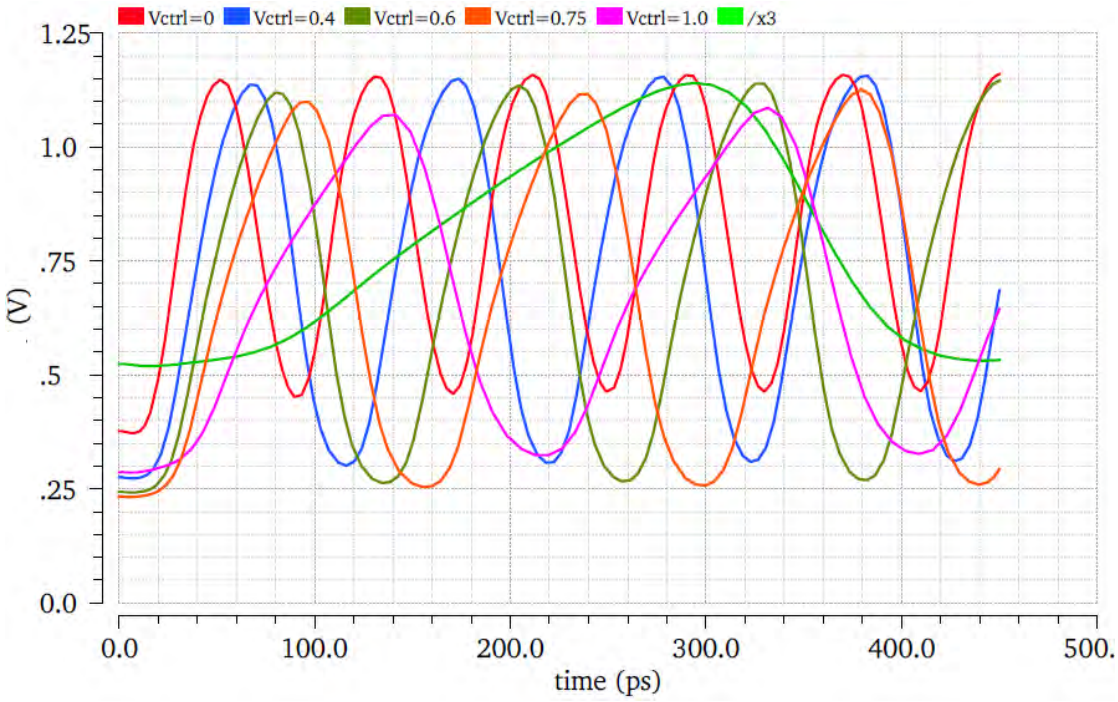
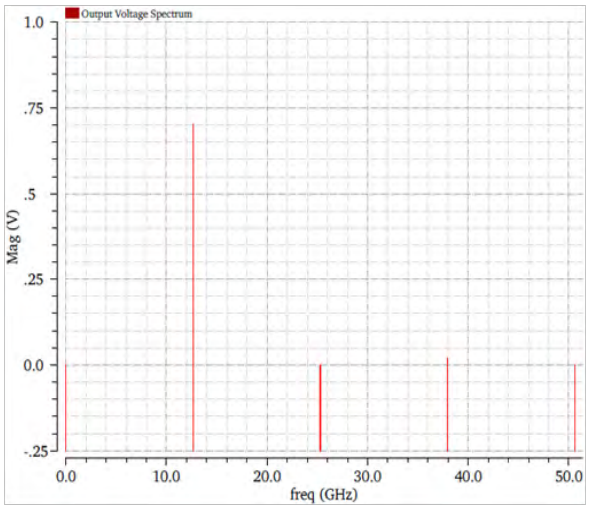
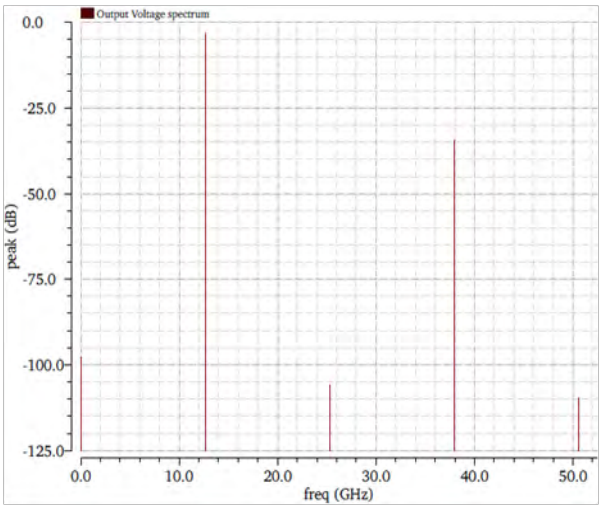


Fig. 4.34: Comparison of Output Waveforms of the proposed VCO for different values of Vctrl

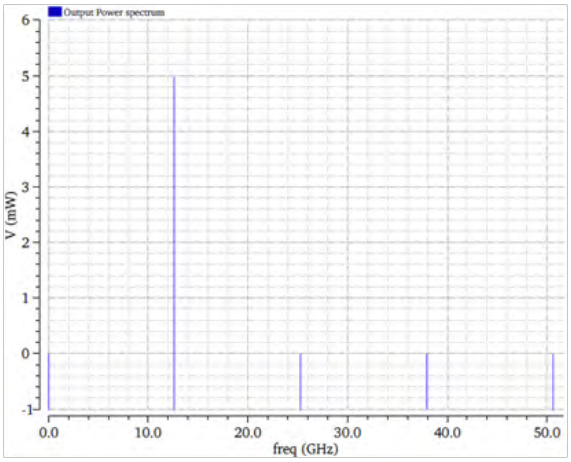
Output Power

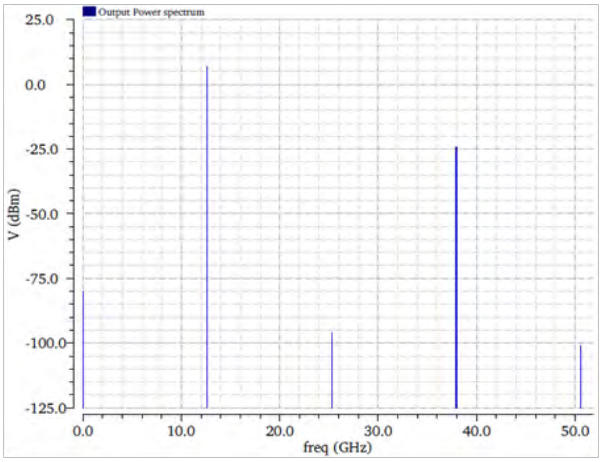
Differential output voltage and output power in magnitude, dB & dBm respectively (for output frequency of 12.68 GHz and 2.51 GHz) are plotted as shown in Fig. 4.35 and Fig. 4.36. Fig. 4.37 shows the output power of the VCO as the control voltage is varied (Frequency tuning). The output power is between 5 and 9 dBm over the entire tuning range.





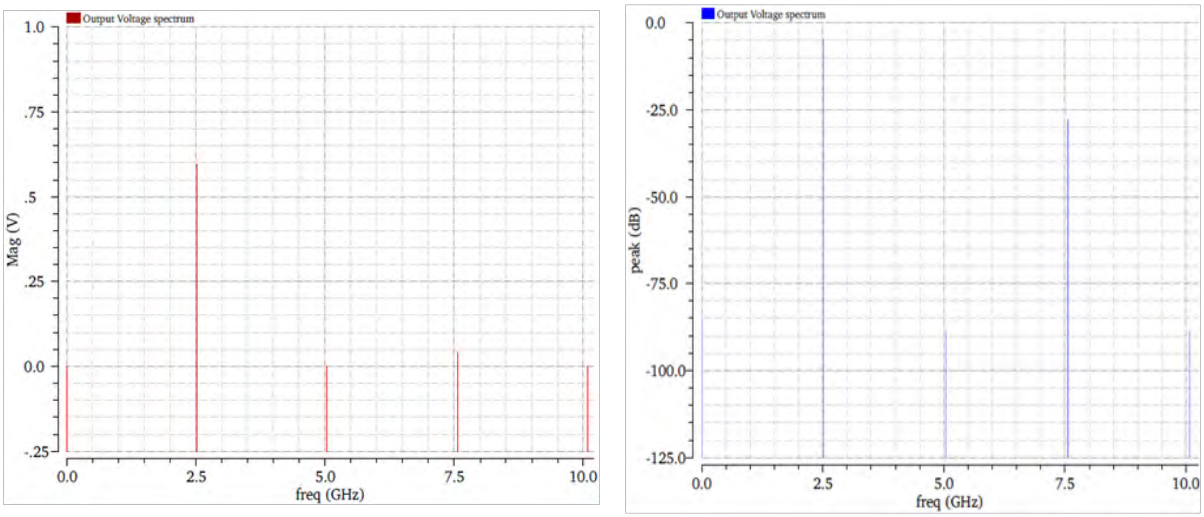
Output Voltage spectrum: Magnitude and dB plot



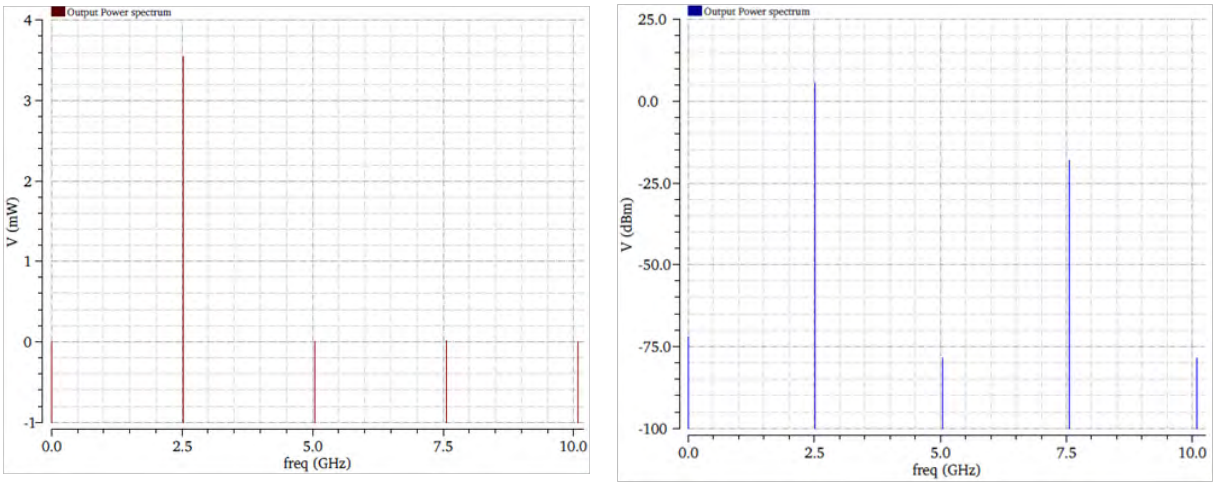


Output Power spectrum: Magnitude and dBm plot

Fig. 4.35: VCO Output Voltage and Power Spectrum at 12.68 GHz



Output Voltage spectrum: Magnitude and dB plot



Output Power spectrum: Magnitude and dBm plot

Fig. 4.36: VCO Output Voltage and Power Spectrum at 2.51 GHz

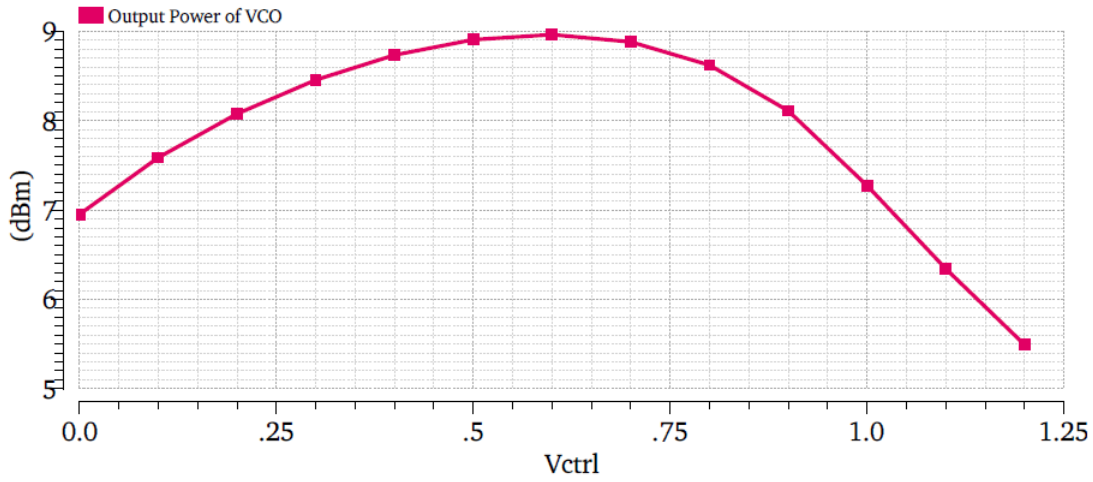


Fig. 4.37: Output power of the VCO

The output power of VCO is higher than 5 dBm over the entire tuning range

Power Dissipation

Power consumption is a critical issue for most modern IC designs. For oscillators, power dissipation is a trade-off between the oscillation frequency required and the phase noise. Fig. 4.38 shows the total power consuption of the VCO. (Average power= static+dynamic power) and it is found to be 1.96 mW for the maximum VCO output frequency. It is clear from the figure that for Vctrl=0 V, the oscillation frequency is higher than that for Vctrl=1.2 V and hence the power dissipation for higher frequency is higher.

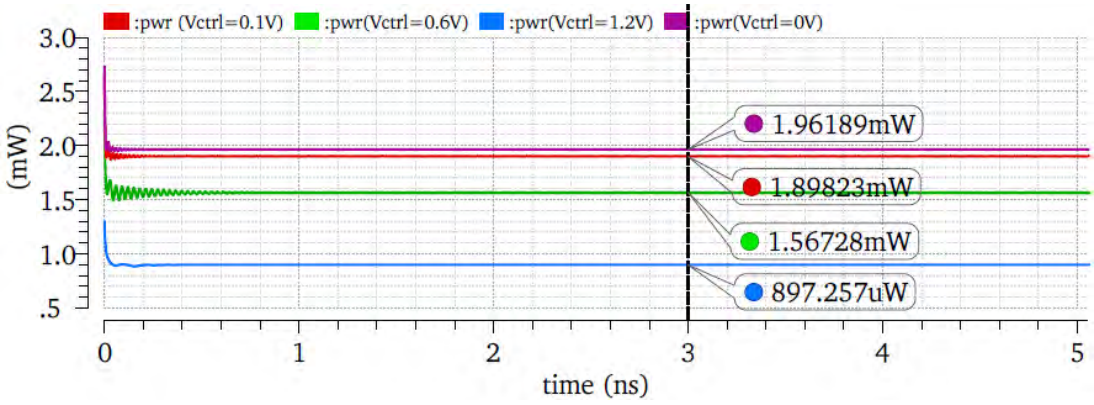


Fig. 4.38: Total power consumption of the VCO for different output frequencies

Phase Noise

Even with a constant, noise-less control voltage and constant power supply, the output waveform of a well-designed oscillator is not periodic. In fact, device noise sources and external interference can lead to tiny fluctuations in the output phase and frequency of the oscilltor. In the time domain, this fluctuation is quantified as "jitter" whereas in the frequency domain it is more commonly referred to and characterized as "phase noise" [58]. Fig. 4.39 shows the phase noise plot of the proposed VCO for an output frequency of 5.2 GHz. Since in our designed we have given emphasis to achieve higher frequency of operation with a wide tuning range and constant gain, we have over looked the technique to reduce the phase noise but still we have achived an appreciable phase noise of **-126.8 dBc/Hz** at an oscillation frequency of 5.2 GHz for Vctrl=1 V and **-123.8 dBc/Hz** at an oscillation frequency of 12.68 GHz for Vctrl=0 V. For future work, other techniques of reducing the phase noise of the ring VCO can be used for achieving much lower phase noise.

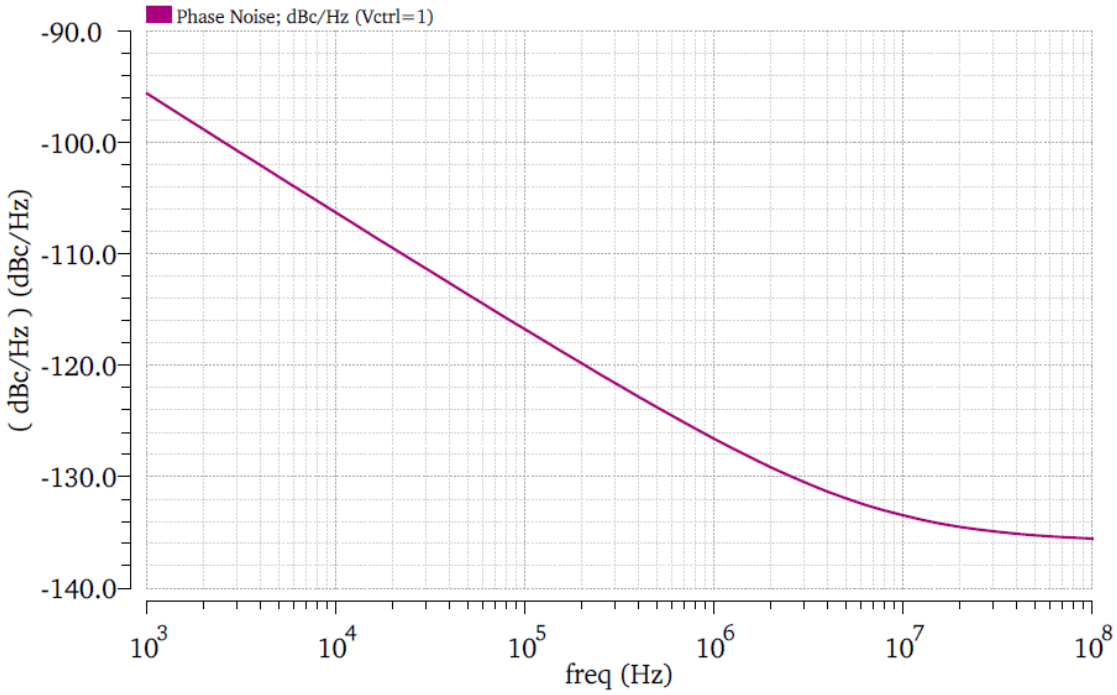


Fig. 4.39: Phase noise plot of the VCO at Vctrl=1V

Fig. 4.40 shows the phase noise plot for different frequency of oscillation of the VCO.

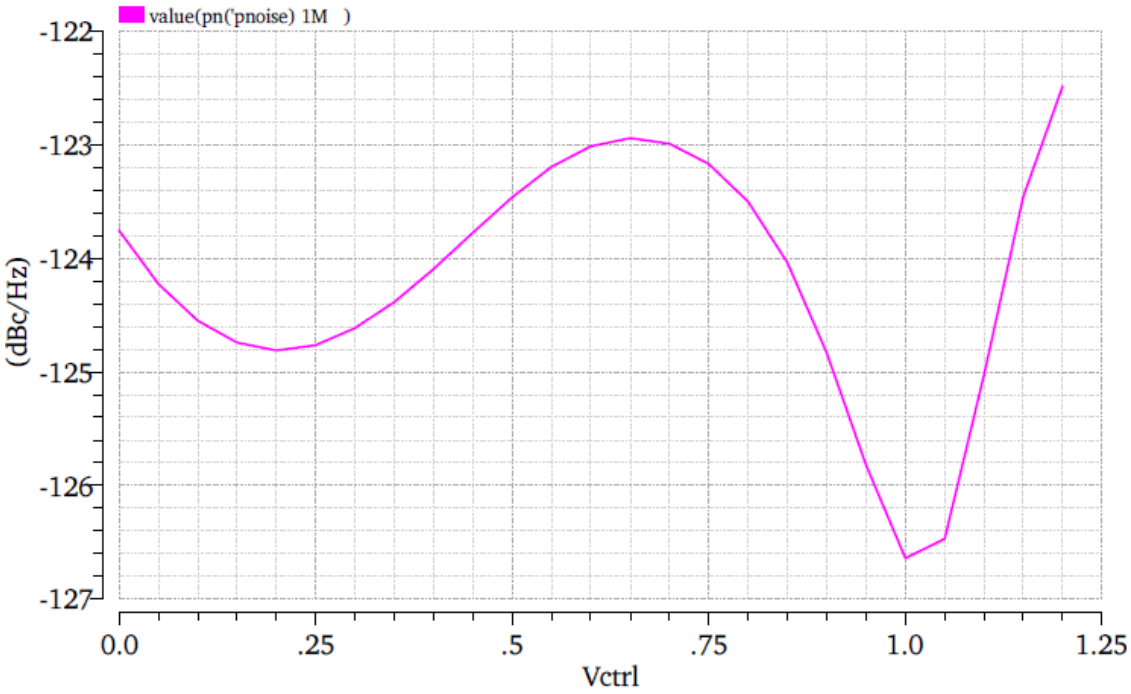


Fig. 4.40: Phase noise (at 1MHz offset) Vs Vctrl

The Figure of Merit (FOM) of the designed ring VCO is calculated by the equation given in [59]:

$$\text{FOM}=\text{PN}(f_{offset})-20\log\left(\frac{f_o}{f_{offset}}\right)+10\log\left(\frac{P_{DC}}{1\text{mw}}\right)$$

and is found to be -202.1.

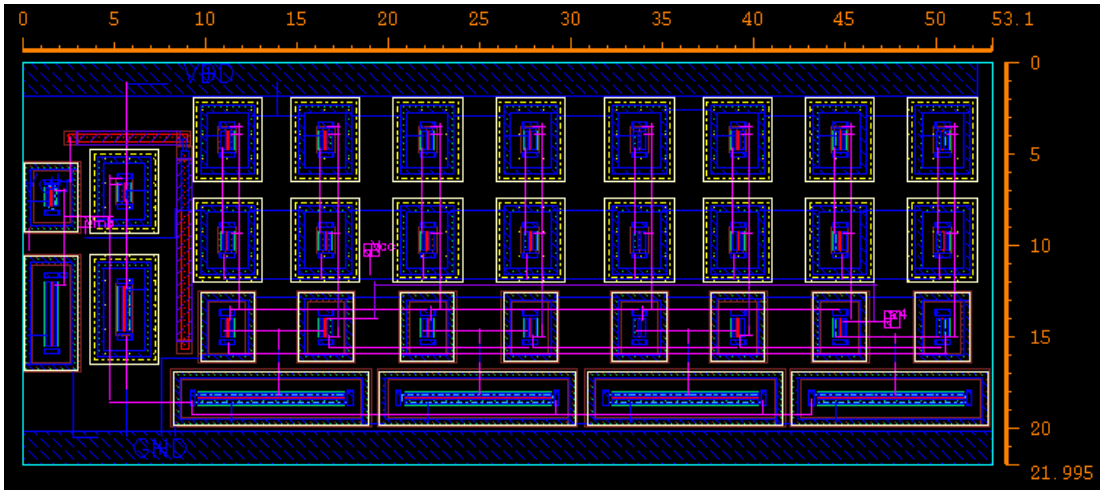


Fig. 4.41: Layout of the VCO

The final layout of the VCO is shown in Fig. 4.41. It occupies an appreciable small area of 53.1 μm×21.995 μm = .001 mm^2.

TABLE 4.2

SUMMARY OF VCO PERFORMANCES

Power Supply	1.2 V
Power Consumption	1.96 mW
Tuning Range	12.68 GHz ~ 2.51 GHz
Phase noise @ 1MHz offset	-123.8 dBc/Hz (12.68 GHz)
FOM	-202.1
Chip area	0.001 mm^2
Technology	90nm CMOS

TABLE 4.3

PERFORMANCE SUMMARY AND COMPARISON OF VCOs

Ref.	**Technology**	f_0 **[GHz]**	**FTR [%]**	**Phase Noise [dBc/Hz]**	**Offset [MHz]**	**Power [mW]**	**Area [mm^2]**
This Work	90nm	12.68	134	-123.8	1	1.96	.001
[60]	90nm	2.0	70	-120	0.2	13	0.008
[61]	90nm	0.8	143	-122	0.2	15	0.048
[56]	180nm	1.35	85	-120	1	41	0.014
[62]	180nm	1.92	75	-126	1	55	0.031

Post Layout Simulation

After the complete layout structure of the VCO in Virtuoso Layout Editor, we were in the position to extract the parasitic using Assura QRC. Fig. 4.42 sows the capture of the layout with parasitic capacitors and resistors.

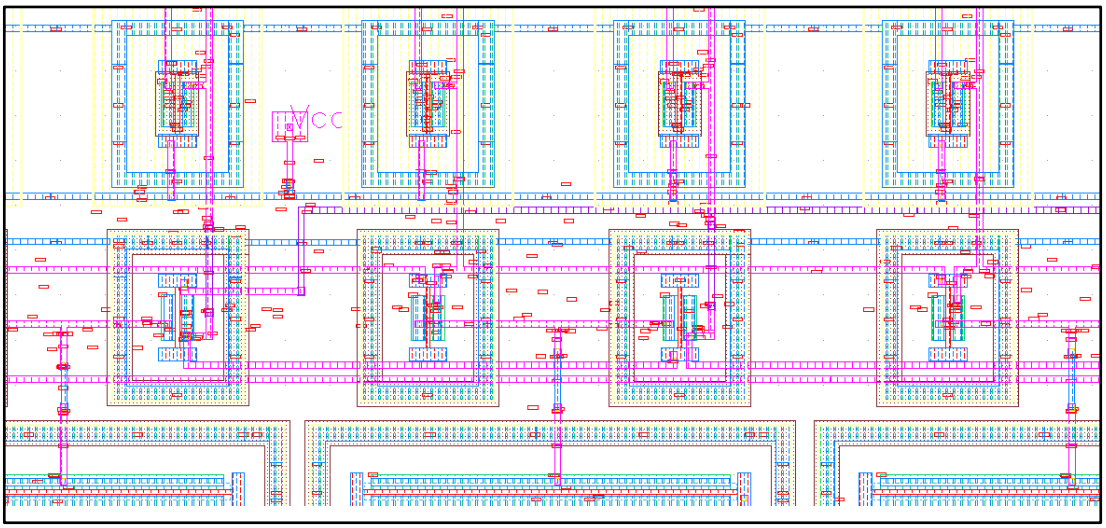


Fig. 4.42: VCO Layout showing Parasitic capacitors and resistors

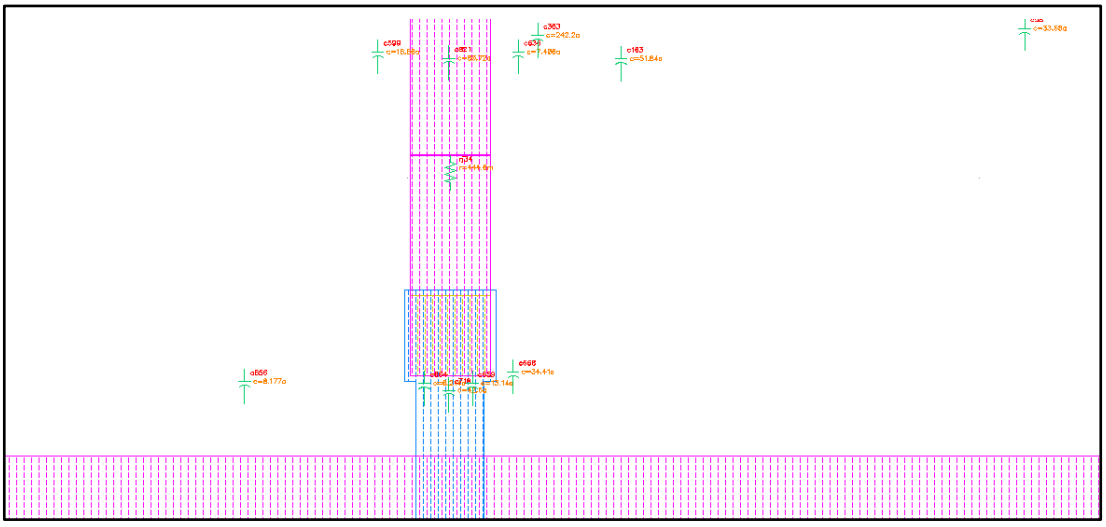


Fig. 4.43: Closer view of Fig. 4.42

A closer view of these capacitors and resistors is depicted in Fig. 4.43. For this circuit, the numbers of parasitic capacitors were found to be around 870 but these capacitors are in the range of atto farad (aF) to femto farad (fF). The numbers of parasitic resistors were counted to be around 560 and are within a value of 16 ohm.

	Numbers Counted	Values
Parasitic Capacitor	875	aF-fF
Parasitic Resistor	565	0.1-16 ohm

The post-layout tuning range characteristic presented in Fig. 4.44 indicates that maximum operating frequency that can be achieved after the additions of parasitic capacitance and resistance has come down to 12.13 GHz whereas the minimum achievable frequency is 2.42 GHz. The tuning range ratio almost remains the same. The post-layout Kvco plot is given in Fig. 4.45.

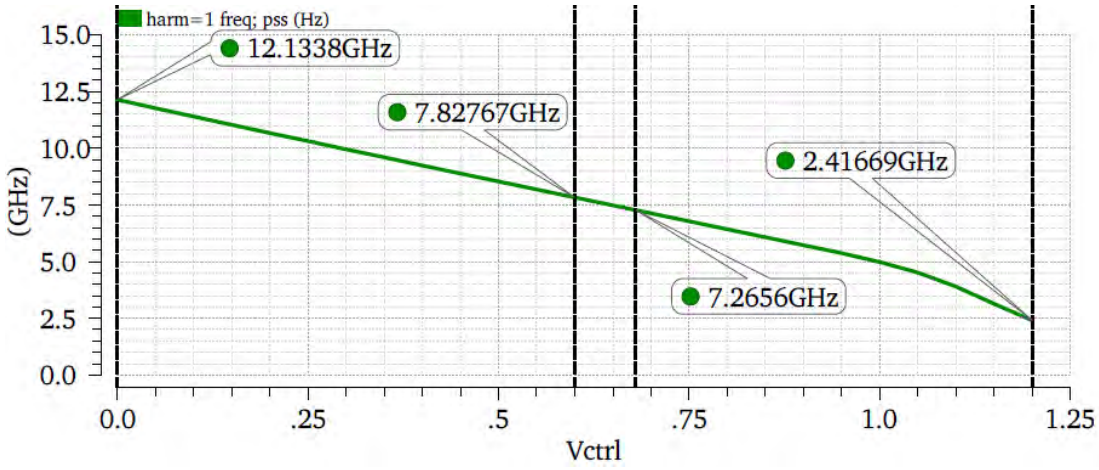


Fig. 4.44: Post-layout tuning range characteristic of the proposed VCO

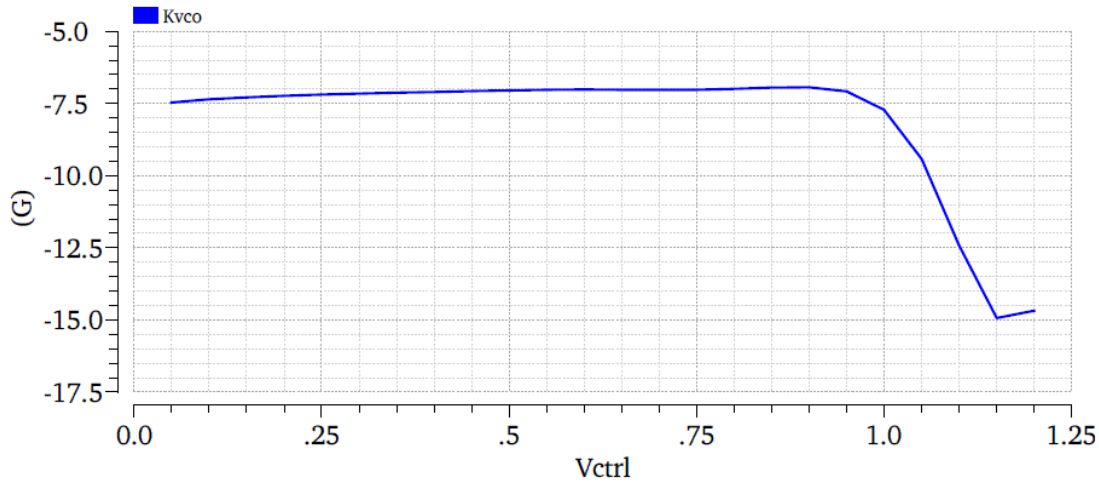


Fig. 4.45: Post-layout gain of the VCO (K_{VCO}) Vs Vctrl

The post layout output waveform for different control voltages and hence different oscillation frequencies is given in Fig.4.46.

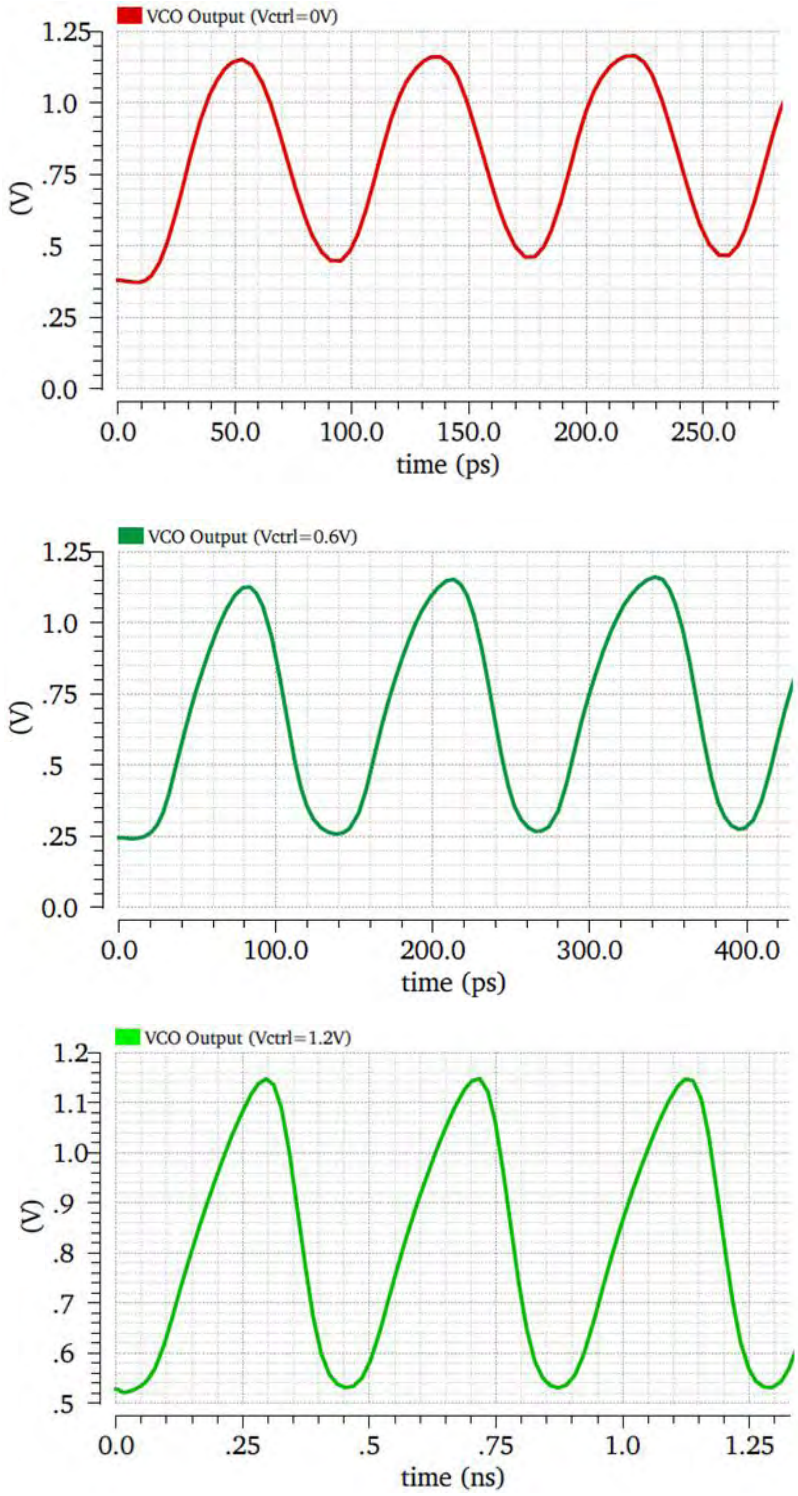


Fig. 4.46: Output Waveform of the proposed VCO for different values of Vctrl

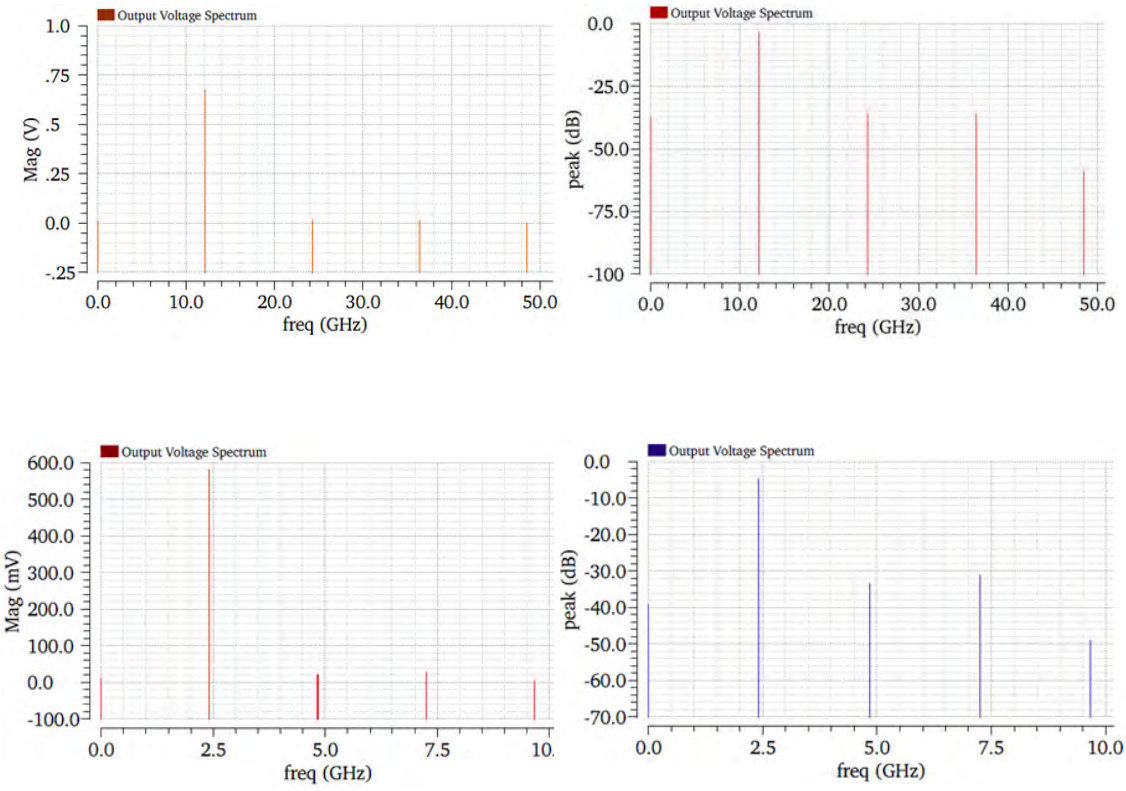


Fig. 4.47: Post layout VCO Output Voltage Spectrum (magnitude and dB) at Vctrl=0 V and 1.2 V

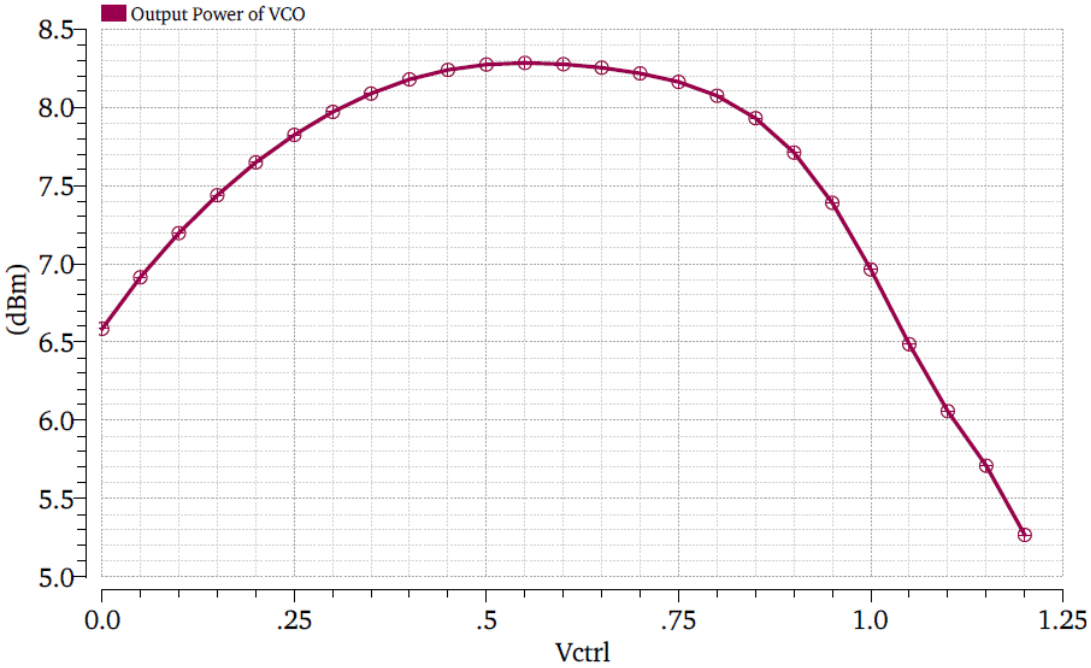


Fig. 4.48: Post layout output power of the VCO

The output power of VCO is higher than 5 dBm over the entire tuning range

Post layout output voltage spectrum is shown in Fig. 4.47 for the maximum and minimum frequency. Fig. 4.48 shows the output power of the VCO as the control voltage is varied (frequency tuning). The output power is between 5 and 8.5 dBm over the entire tuning range.

Fig. 4.49 shows the total power consuption of the VCO and it is found to be 1.9 mW for the maximum VCO output frequency. The power consumption for the minimum output frequency is found to be 1.02 mW.

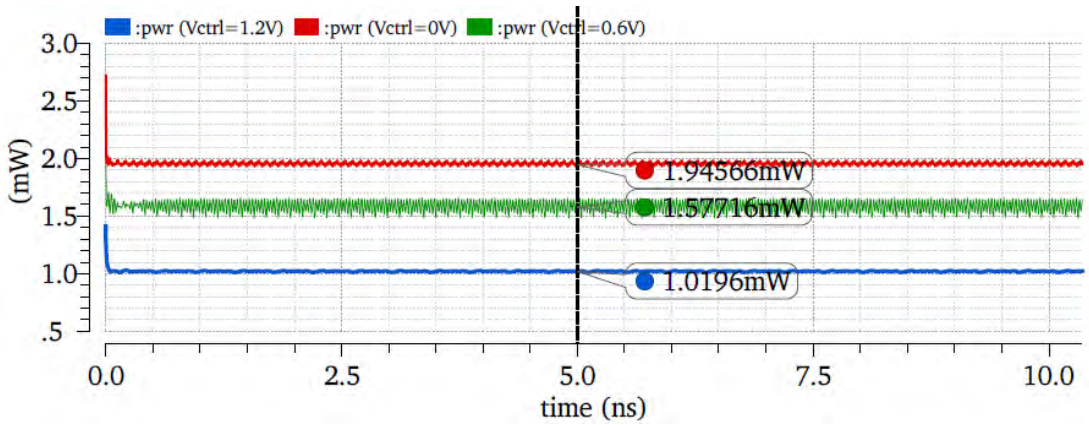


Fig. 4.49: Post layout total power consumption of the VCO for different output frequencies

Fig. 4.50 shows the post layout phase noise plot of the VCO for an output frequency of 2.42 GHz, 5 GHz, and 12.13 GHz. Post layout phase noise at an output frequency of 12.13 GHz is **-122.8 dBc/Hz** and is still acceptable and appreciable. Fig. 4.51 shows the phase noise plot for different frequency of oscillation of the VCO.

Therefore, after the post layout simulation of the desired properties of the proposed VCO, we conclude that we have successfully achieved our desired objective and have managed to obtain 12 GHz output frequency with low phase noise.

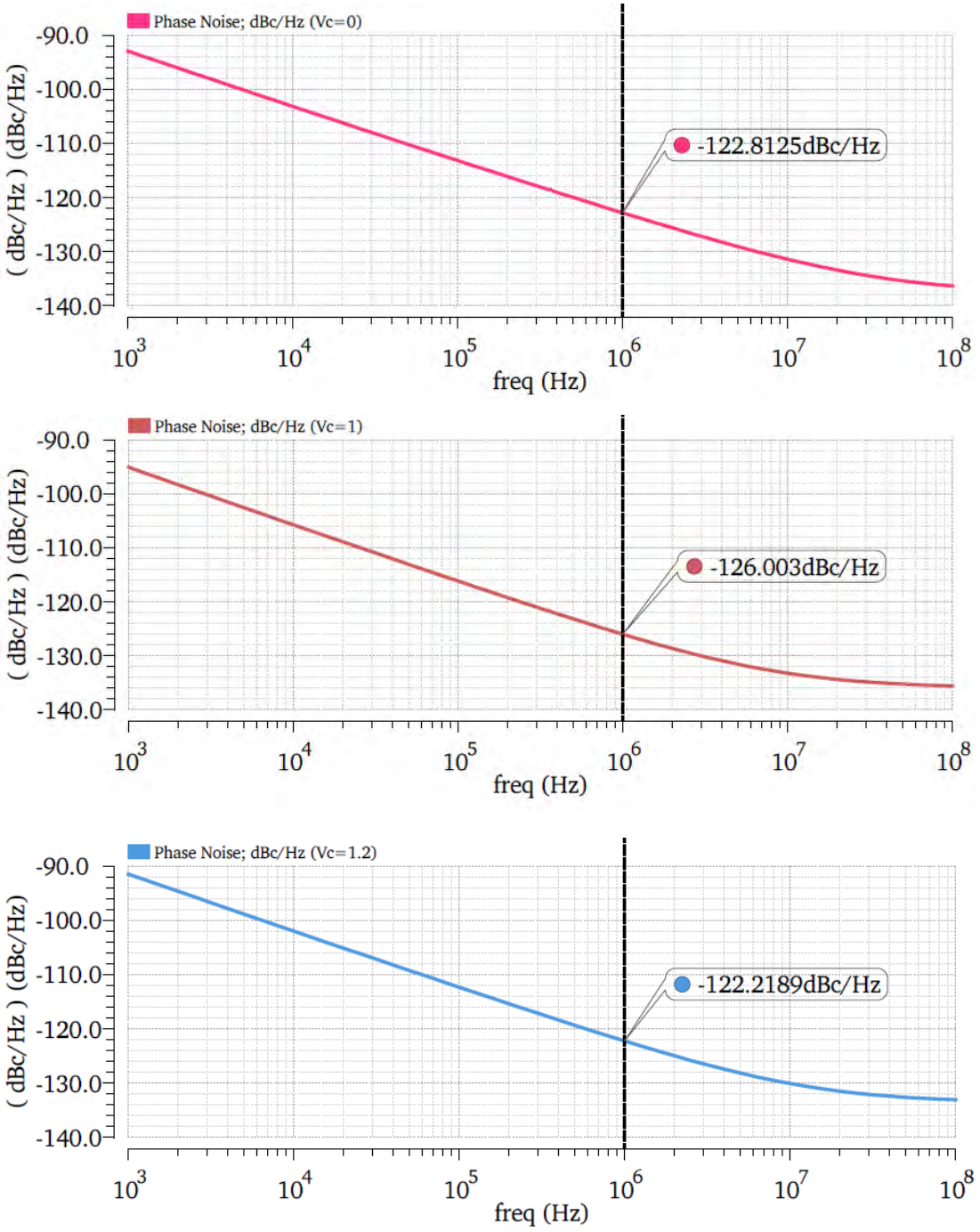


Fig. 4.50: Post layout phase noise plot of the VCO at Vctrl=0 V, 1 V, and 1.2 V

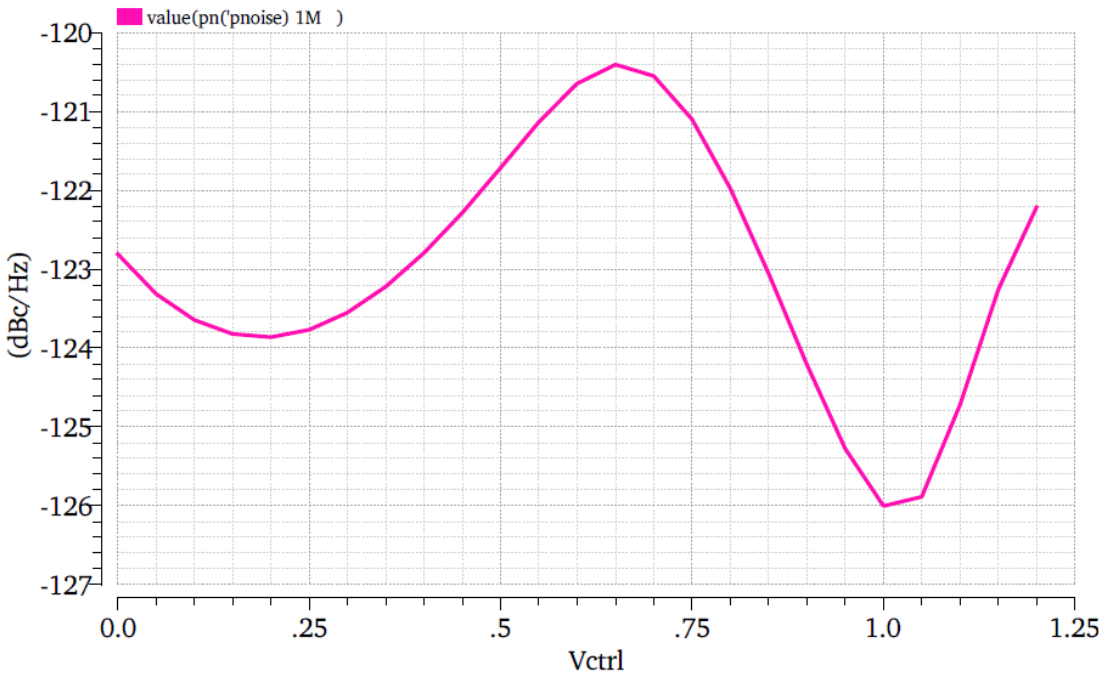


Fig. 4.51: Post layout Phase noise (at 1MHz offset) Vs Vctrl

4.4 Programmable Divider Design

In this work, for PLL frequency synthesizer operating between 2.5 GHz and 12 GHz with division ratios of 6-24 can be achieved with an N prescaler (N=2), a 2/3/4/5 divider, a 3 bit P- Counter and a multiplexer circuit. In this design we have not used the conventional method of designing the programmable counter because the division ratio is not too high. To show the functionality of the designed frequency synthesizer, the above mentioned components of the programmable divider is sufficient. Fig. 4.52 shows the block diagram of the programmable divider. The bits 2_4OR3_5, 2_3, 4_5, P0, P1, P2, and Select_P shown in the figure are used for programming the counter. Table 4.4 shows the programmable values of the divider.

4.4.1 Prescaler (*N*)

A divide by 2 prescaler is used in this work for the design of the fully programmable divider. The prescaler has been designed using the true single-phased clock (TSPC) D flip flop [63]-[65] with a slight modification given in [66]. The

designed prescaler operates up to a maximum operating frequency of 12.5 GHz. The output of the prescaler is fed to the input of 2/3/4/5 divider.

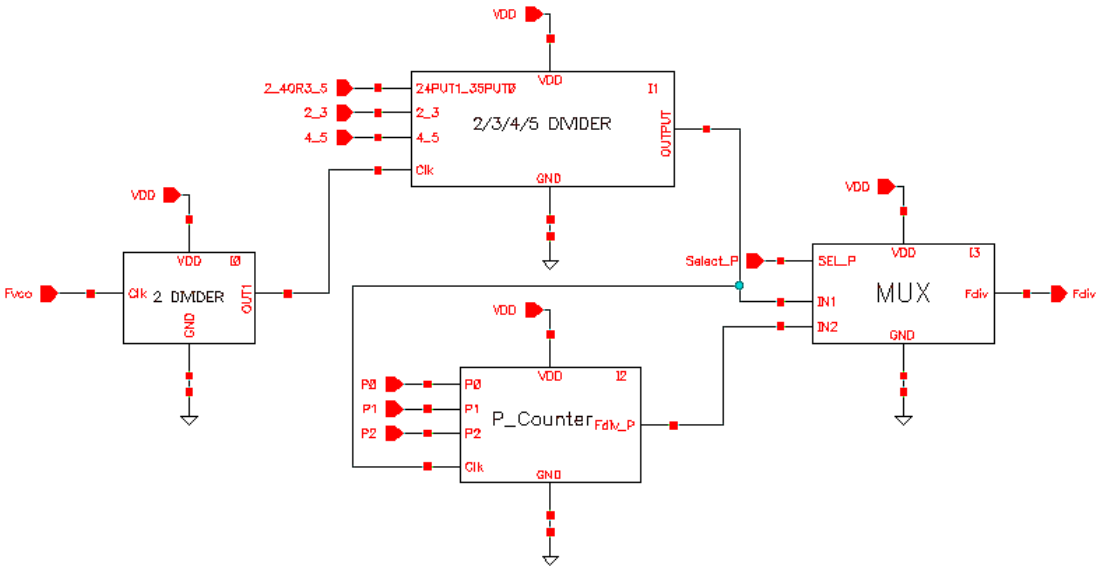


Fig. 4.52: Block Diagram of the programmable divider

4.4.2 2/3/4/5 Divider

The prescaler scales the input signal by a value of 2 such that the 2/3/4/5 Divider will be working in the frequency range of 1.25 -6 GHz. We have modified the 2/3 prescaler [67] and used three TSPC D flip flop to obtain the divider which divides the input frequency by 2 to 5 depending on the selection pin. Three selection pins have been used in this divider namely 2_4OR3_5, 2_3, and 4_5. To divide the frequency of the incoming signal by 2 or 4, logic „1" is placed at the 2_4OR3_5 pin and to divide it by 3 or 5, logic „0" is placed. If logic „1" is placed at the 2_4OR3_5 pin, then the divider is in a position to divide the frequency of the signal by 2 or 4. To divide the frequency by 2, we must provide logic „1" at the 2_3 pin and logic „0" at the 4_5 pin. We must provide the inverse logic to divide the frequency by 4.

4.4.3 P-Counter

The 2/3/4/5 divider scales its input signal by a minimum value of 2 and a maximum value of 5 such that the P-counter operates in the frequency range of 250

MHz-3 GHz. The given P-Counter can be programmed from a value of 3-8 with the help of the three programming pins P0, P1 and P2. The programmable P-Counter used in the design of the programmable divider is a 3-bit asynchronous down counter as shown in Fig.4.53. The P-Counter is designed with 3 reloadable TSPC D flip-flops (DFF) given in [67] and an end-of- count (EOC) detector which has reload circuit in it [68]. This reloadable DFF is similar to the original nine transistors TSPC DFF [69] with reloadable functions added to it. Since the counter is asynchronous, the complementary output of the first DFF is fed as clock to the input of next flip-flop. In the initial state, all the reloadable DFF are loaded by the programmable pins P0-P3. As the counter is triggered by the output of the prescaler, the P-counter starts down counting till the state "000" is reached. Once this state is detected by the EOC logic circuit, the load (LD) signal goes high to reset all reloadable DFF to the initial state.

The EOC logic circuit is used to detect when the P-Counter reaches the state "Q0Q1Q2=000", and preset the reloadable FF"s to the initial state so that P-Counter starts down counting again from the loaded value to the final state. The EOC logic circuit is built with a 2-input NOR, two 3-input NAND and an embedded NOR DFF.

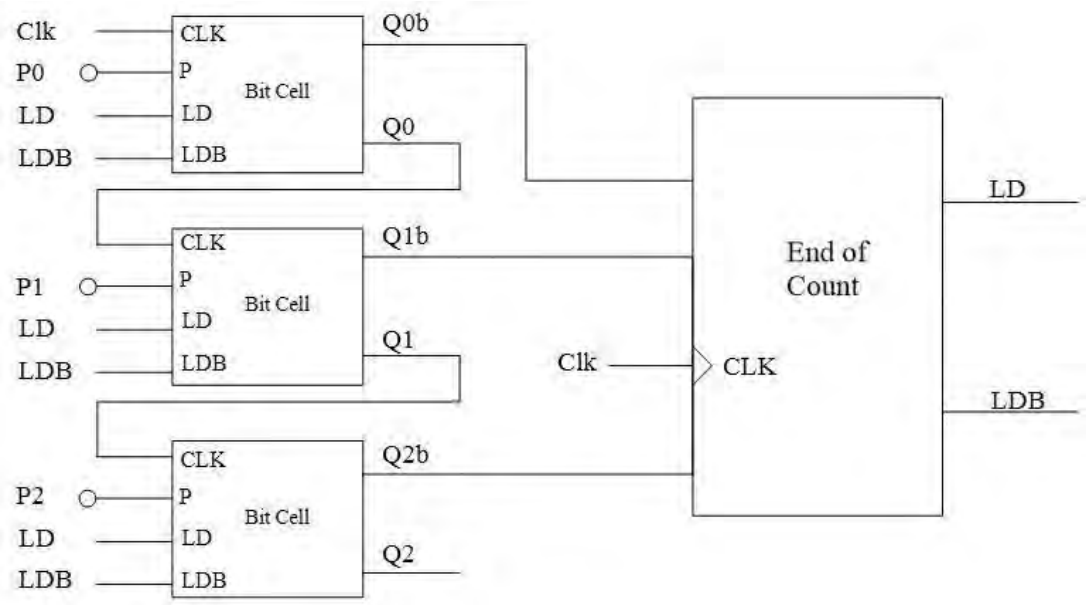


Fig. 4.53: Block diagram of the Programmable P-Counter

4.4.4 Multiplexer

In our design, a multiplexer circuit is needed to select either the output of the 2/3/4/5 divider or the output of the P-Counter. If the divide value needed is low then we bypass the further division by the P-Counter and takes the output of the 2/3/4/5 divider as F_{div}. The multiplexer circuit consists of an inverter, two AND gates and one NOR gate to perform the multiplexing operation.

The overall block diagram of the programmable divider used in this work is shown in Fig. 4.32. To show the functionality of the proposed frequency synthesizer, the different programmable values of the divider is shown in Table 4.4.

TABLE 4.4
PROGRAMMABLE VALUES OF THE DIVIDER

Output Frequency of PLL (F_{ref}=500 MHz)	Division ratio	Prescaler (N)	2/3/4/5 Divider	Programmable Counter (P)	Multiplexer (MUX) input
3	6	2	3	×	0
4	8	2	4	×	0
5	10	2	5	×	0
6	12	2	2	3	1
8	16	2	2	4	1
9	18	2	3	3	1
10	20	2	2	5	1
12	24	2	2/3/4	6/4/3	1

The layout of the full divider circuit is shown in Fig. 4.54. It occupies an area of 18.855 μm×18.36 μm = .000346 mm^2.

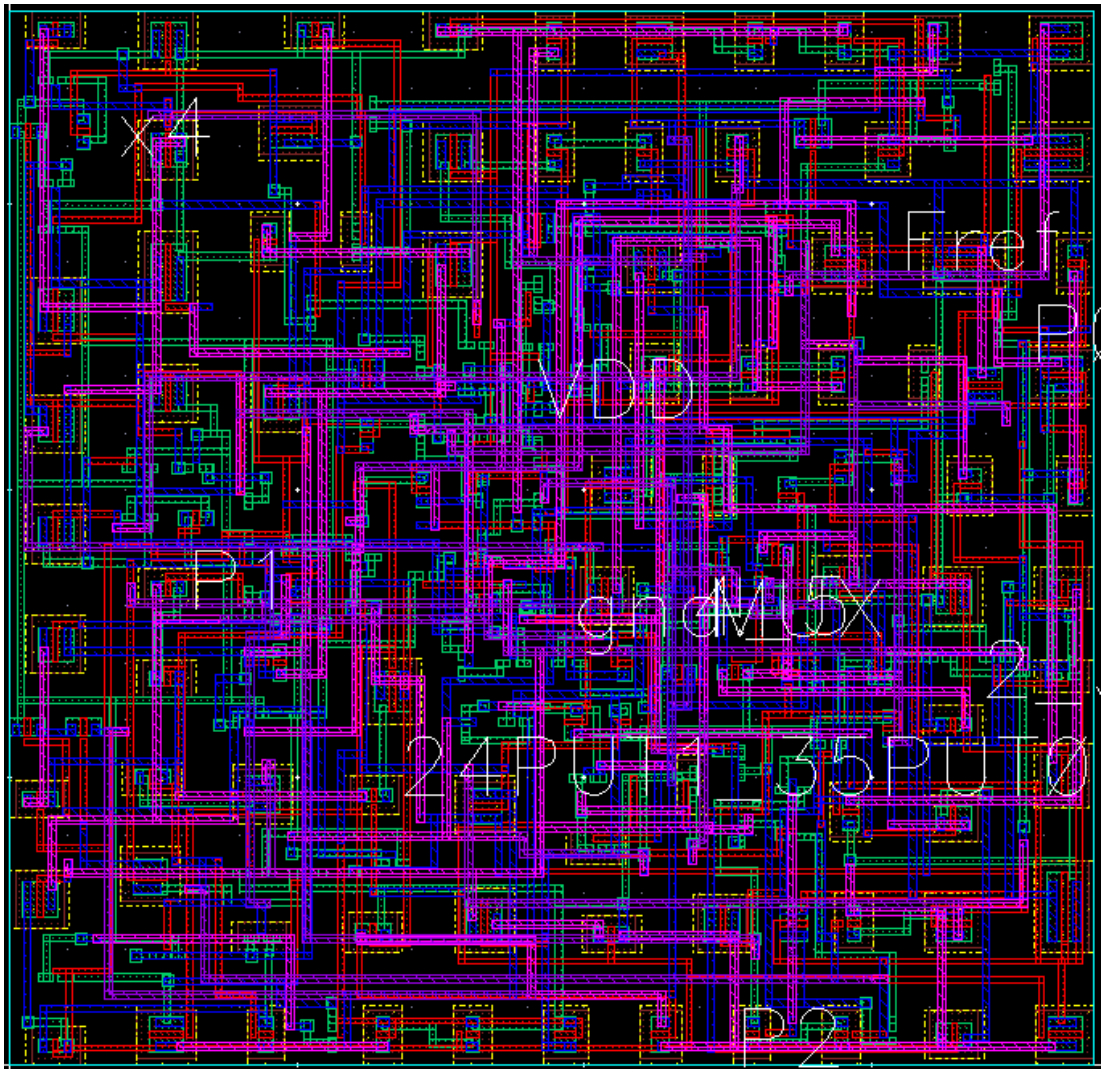


Fig. 4.54: Layout of the complete Divider Circuit

4.5 RF Frequency Synthesizer

After each component is designed and simulated, the next step is to implement the entire system. It is composed of a PFD, CP, Loop Filter, and a Divider. Since the design and layout of each component is already completed, the design and layout of the whole system is just the matter of connecting the design of each one.

The important performance analyses that need to be tested are the Lock-time, phase noise, and power dissipation.

It is known that the output frequency of the frequency synthesizer is not available immediately after the desired division value is applied to the programmable divider. It takes certain time to reach a steady state condition. The time taken to reach this steady state condition is known as the lock time. It varies with the value of the output frequency. Fig.4.55 shows the plot of the frequency and control voltage over time to achieve an output frequency of 12 GHz. From the figure it is found that the lock time is around 3 us.

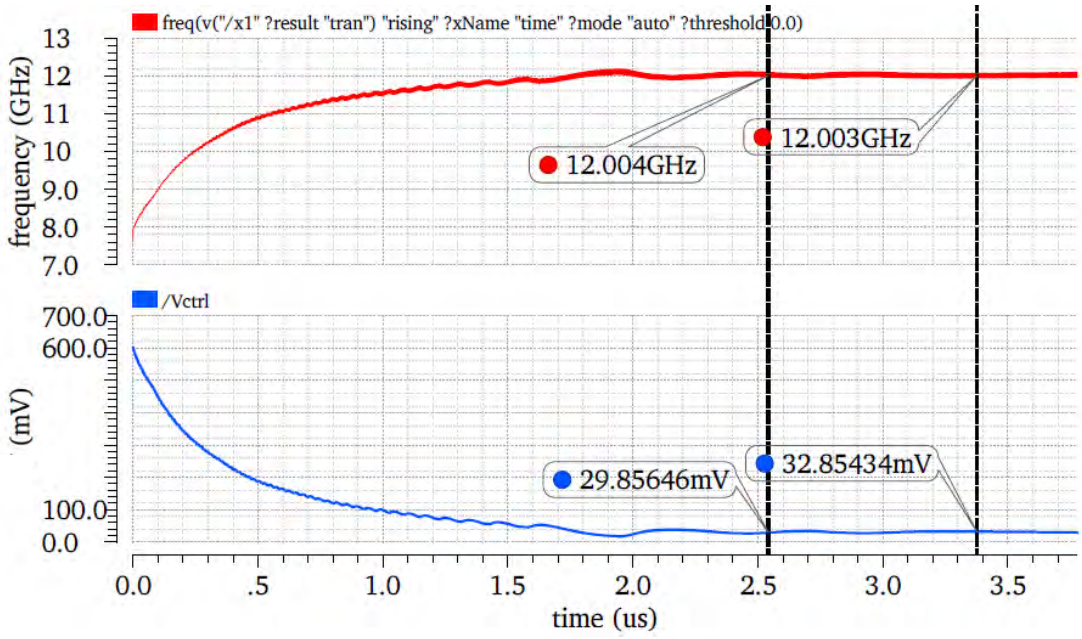


Fig. 4.55: Frequency and control voltage variation plot over time and lock-time required to achieve 12 GHz output frequency

Fig. 4.56 shows the different signals after the frequency synthesizer has reached the steady state and locked with the reference frequency.

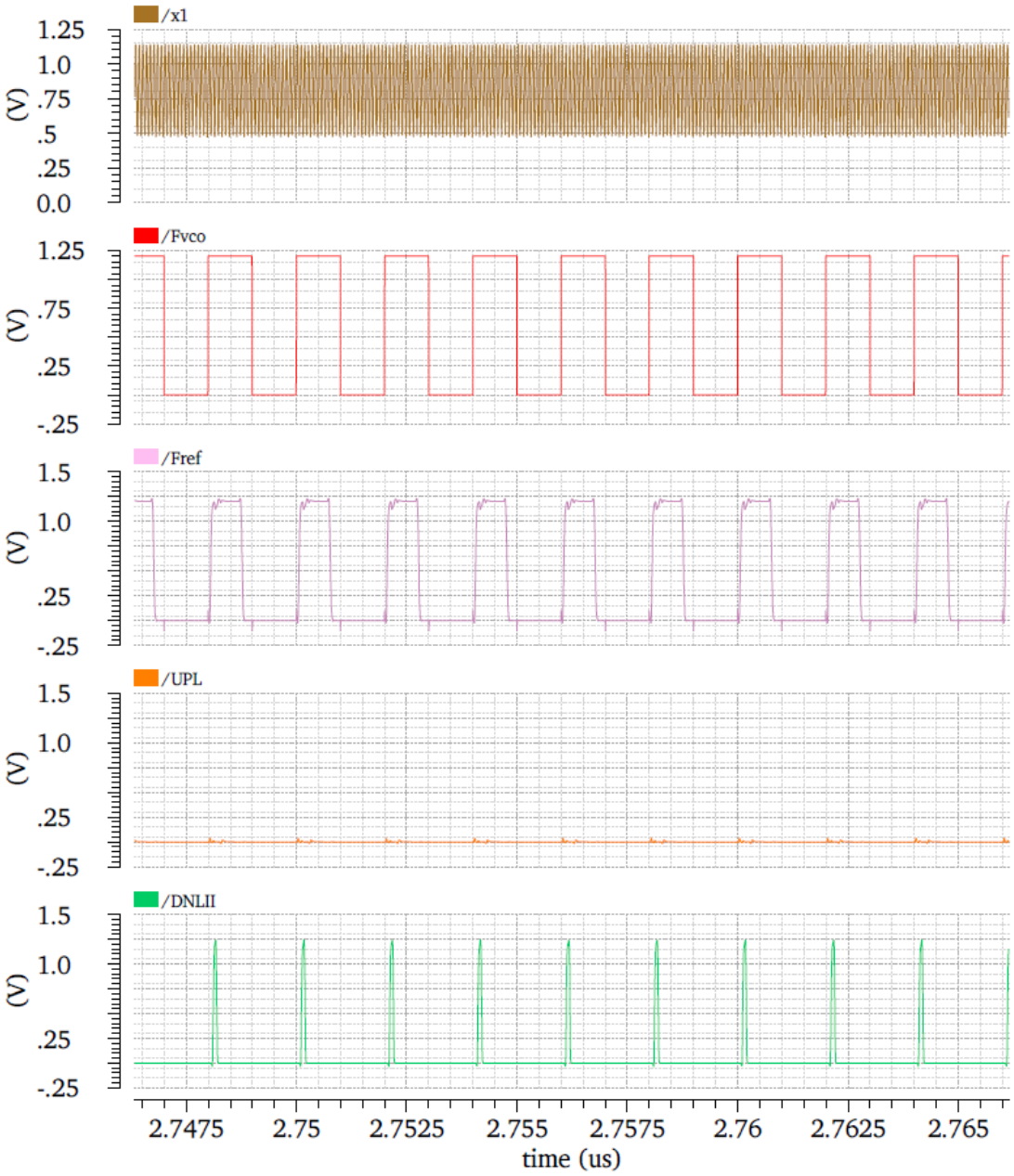


Fig. 4.56: Different signals of the frequency synthesizer in lock state at a frequency of 12 GHz

The frequency spectrum for an output frequency of 12 GHz is shown in Fig. 4.57. From the figure it is clearly seen that the spurious tones are at a frequency offset of 500 MHz which corresponds to the reference frequency. Fig. 4.58 shows the power dissipation of the frequency synthesizer over time at 12 GHz. The average power dissipation is calculated to be 3.074 mW.

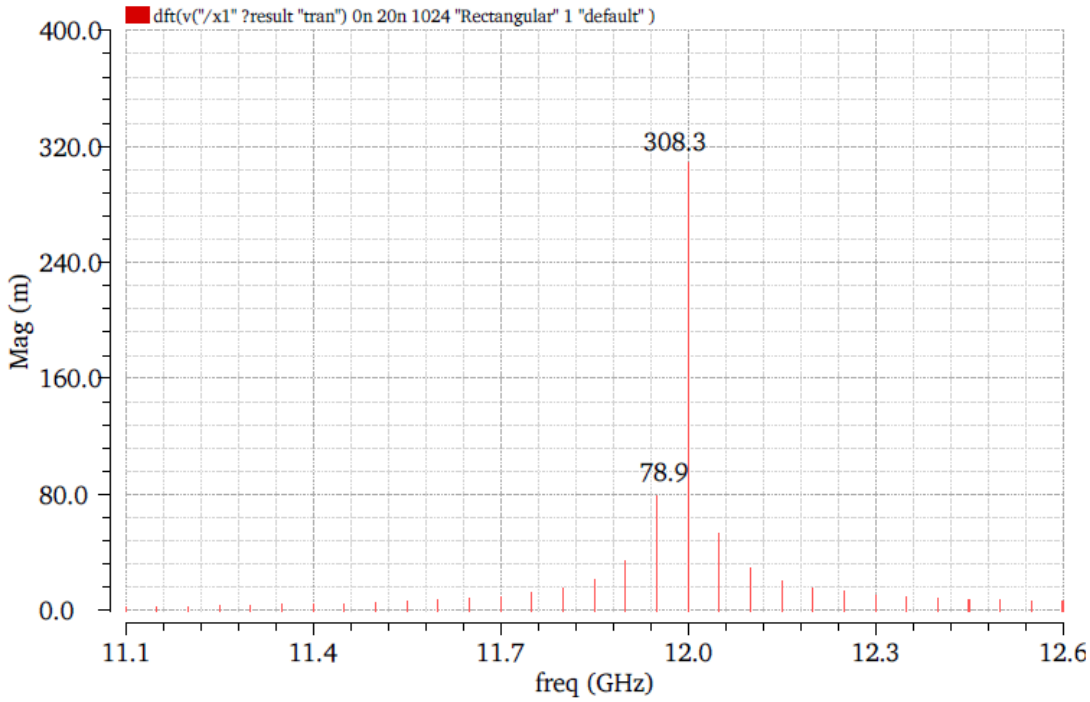


Fig. 4.57: Frequency Spectrum at an output frequency of 12 GHz

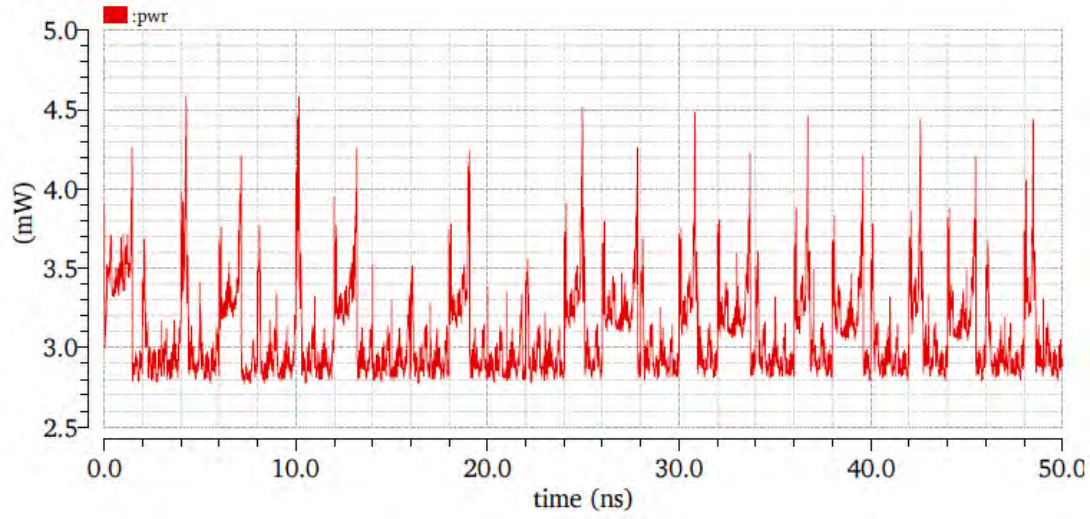


Fig. 4.58: Plot of power dissipation (at 12 GHz) over time

In Fig. 4.59, frequency and control voltage has been plotted over time and the corresponding various signals are shown in Fig. 4.60.

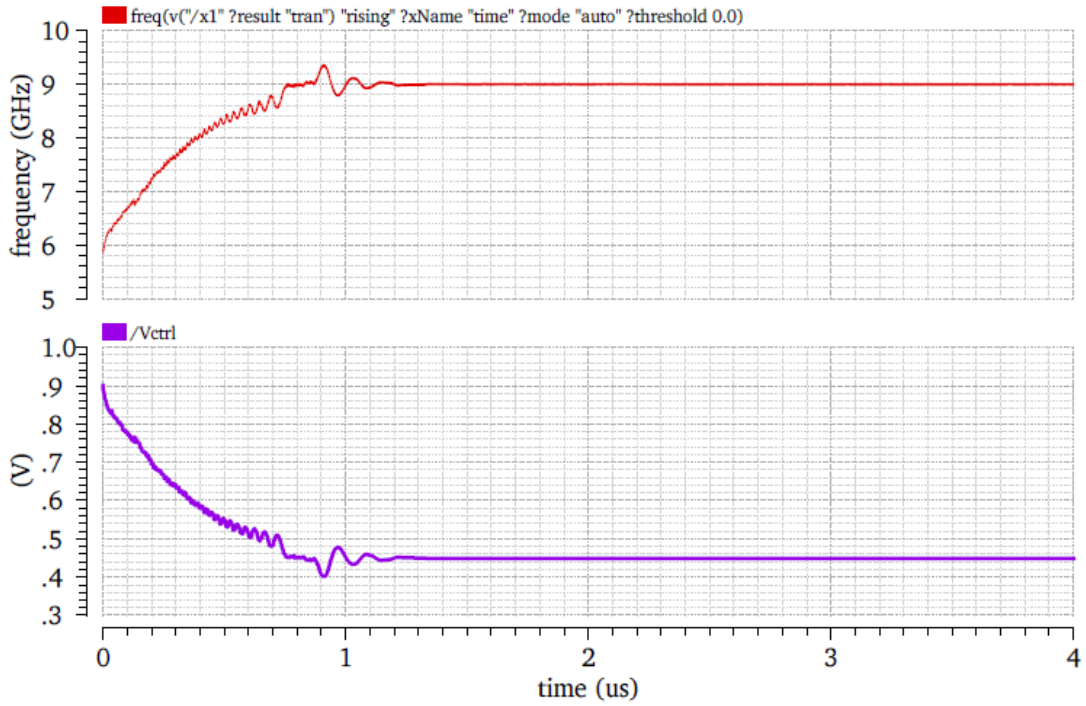


Fig. 4.59: Frequency and control voltage variation plot over time and lock-time required to achieve 9 GHz output frequency

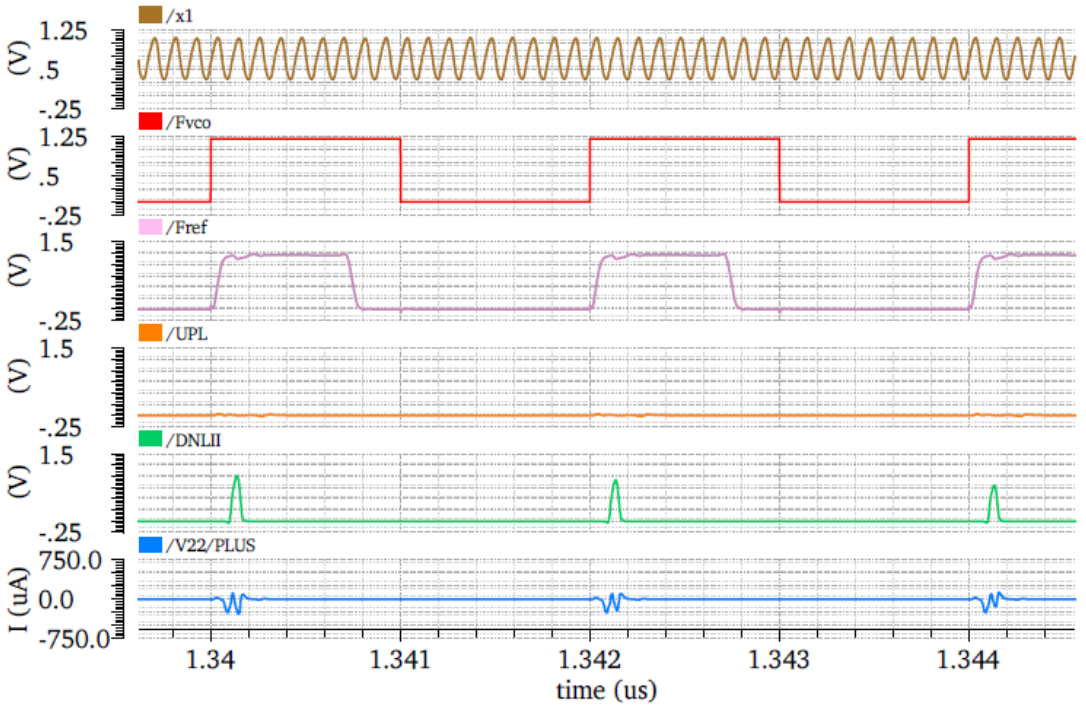


Fig. 4.60: Different signals of the frequency synthesizer in lock state at a frequency of 9 GHz

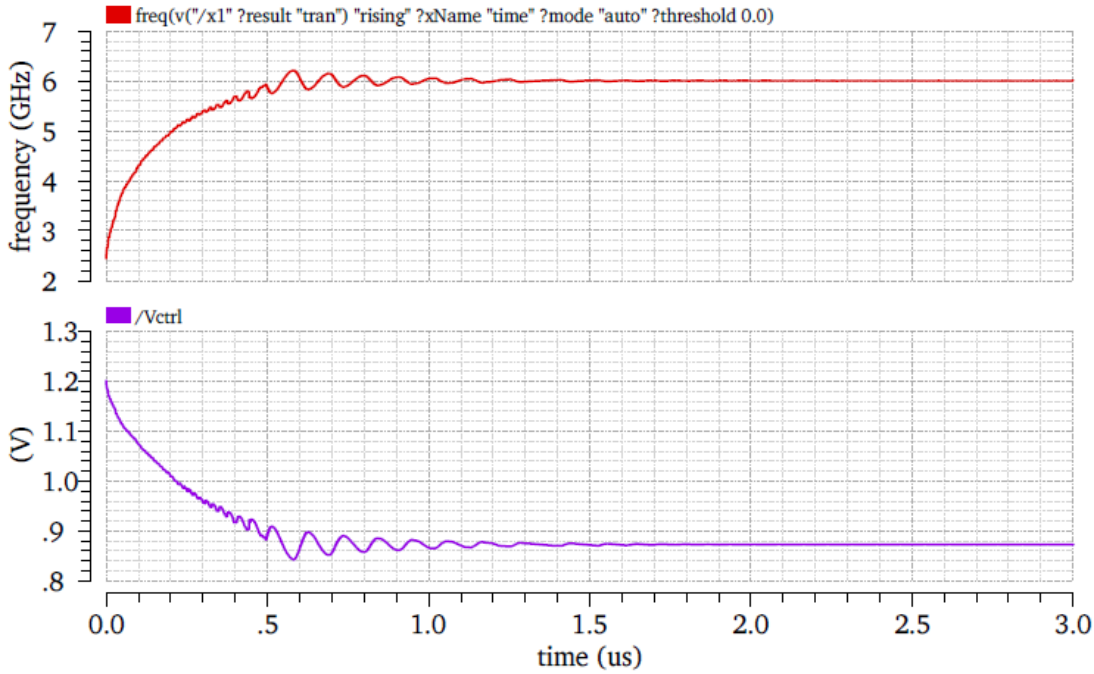


Fig. 4.61: Frequency and control voltage variation plot over time and lock-time required to achieve 6 GHz output frequency

Fig. 4.61 has been plotted for an output frequency of 6 GHz. From Fig. 4.62 we can see that the charging current is smooth and free from glitches.

Lastly we have the simulation output for an output frequency of 3 GHz which is depicted in Fig. 4.63. We could not achieve an output frequency of 2.5 GHz due to the limitations imposed by the loop filter as it could not be charged up to 1.2 V (which is required for an output frequency of 2.5 GHz) by the charge pump.

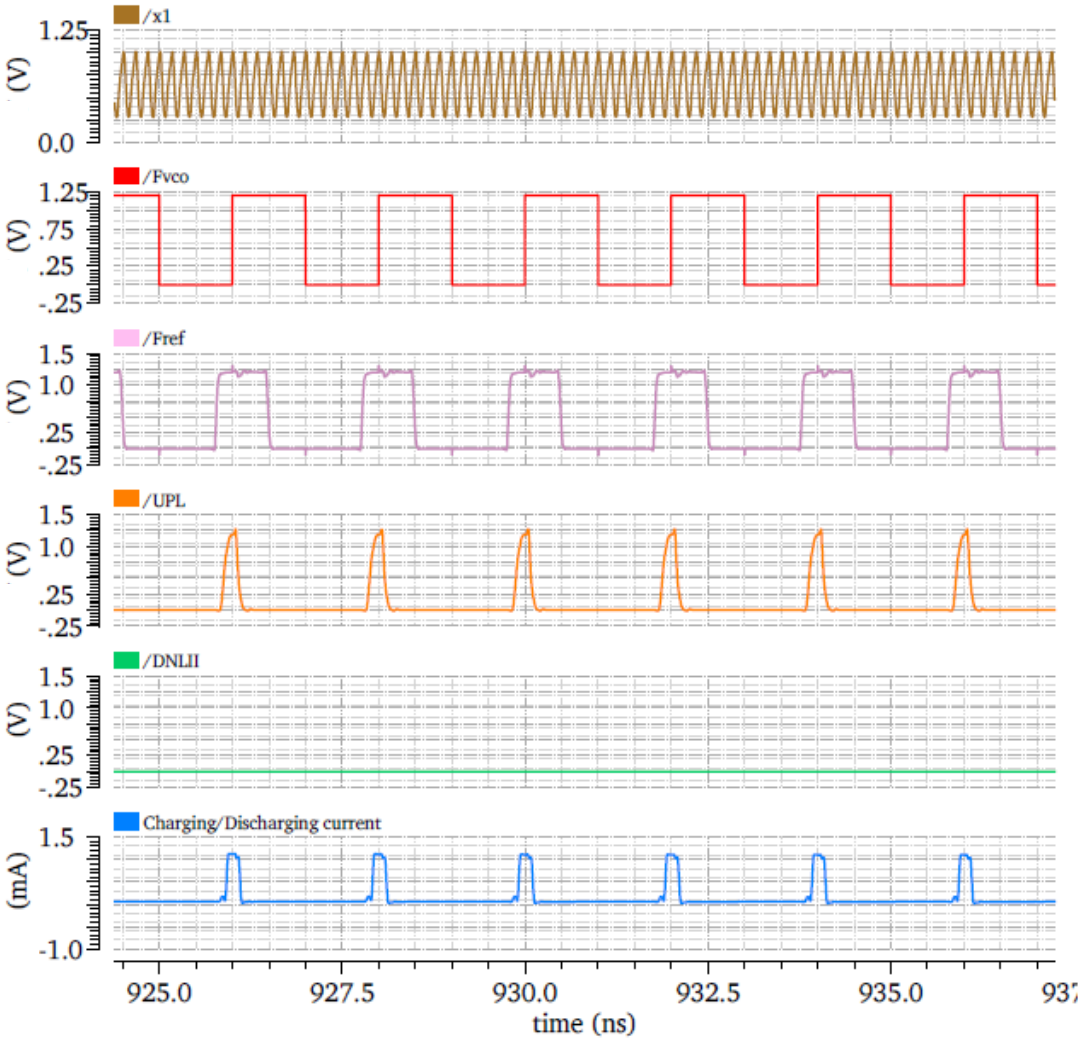


Fig. 4.62: Different signals of the frequency synthesizer in lock state at a frequency of 6 GHz

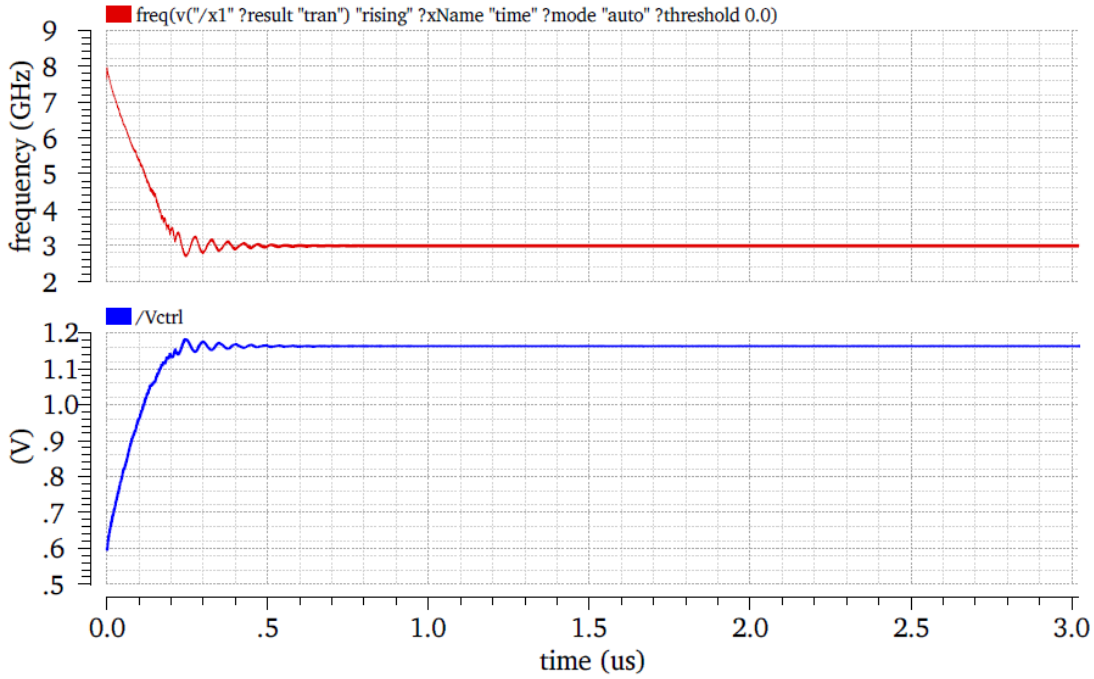


Fig. 4.63: Frequency and control voltage variation plot over time and lock-time required to achieve 3 GHz output frequency

One of the most important performance parameter of a frequency synthesizer is the phase noise. The phase noise plot is shown in Fig. 4.64. The overall phase noise of the designed frequency synthesizer operating at 12 GHz is found to be**-100.6 dBc/Hz** at an offset frequency of 1MHz without any additional means to reduce the phase noise.

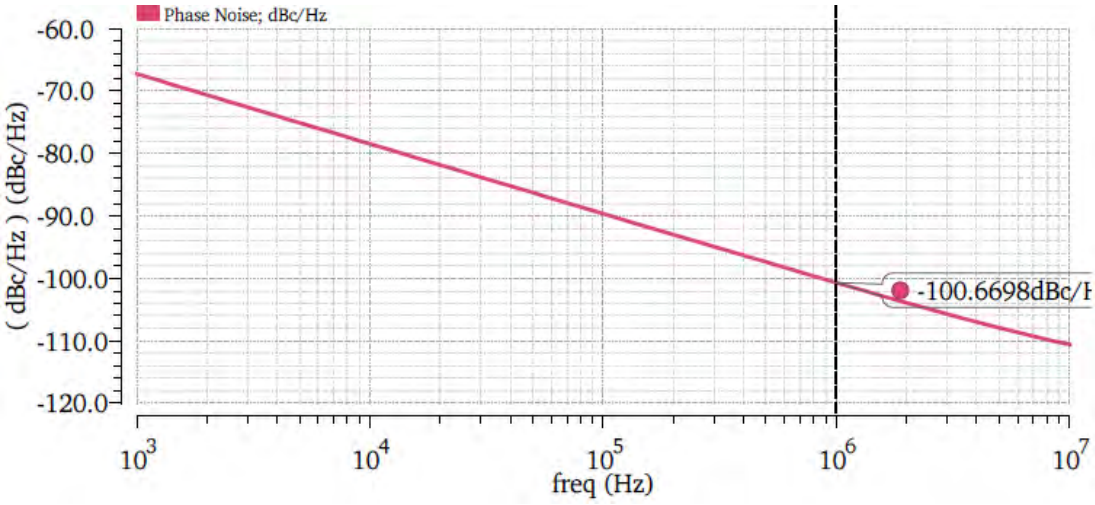


Fig. 4.64: Phase noise plot of the proposed frequency synthesizer operating at 12 GHz

The complete layout of the frequency synthesizer is shown in Fig. 4.65. It occupies an area of 148 µm ×107 µm =0.0158 mm^2.

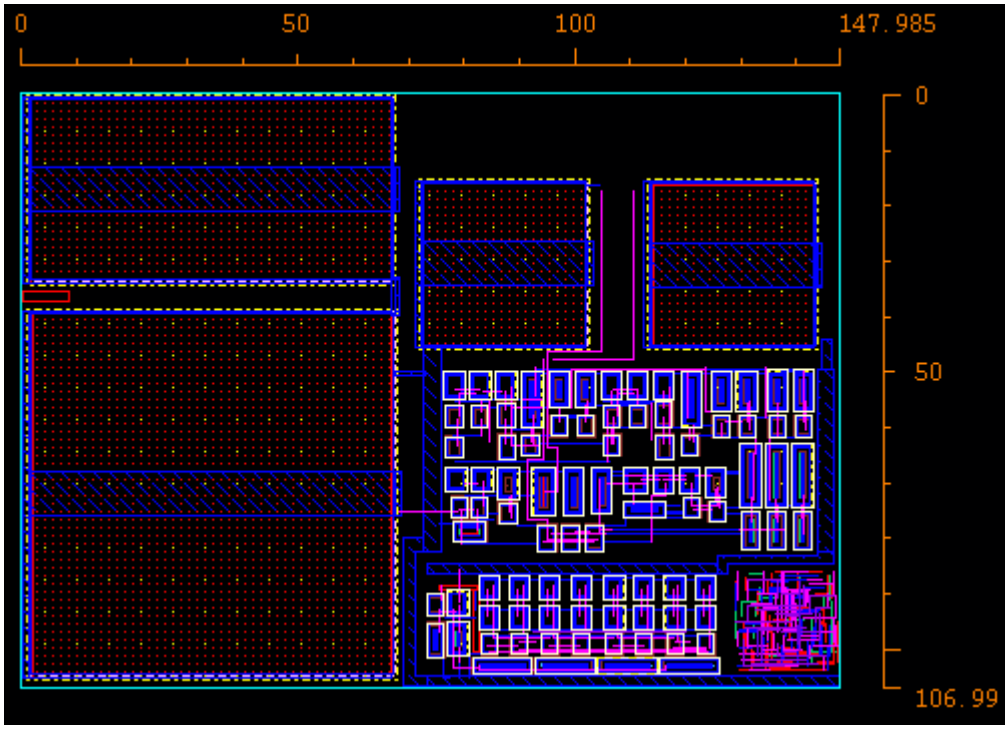


Fig. 4.65: Complete layout of the frequency synthesizer

The layout shown in Fig. 4.64 was accommodated in chip-edge with the dimension of 600 µm ×600 µm. The complete layout inside the chip-edge is shown in Fig. 4.66.

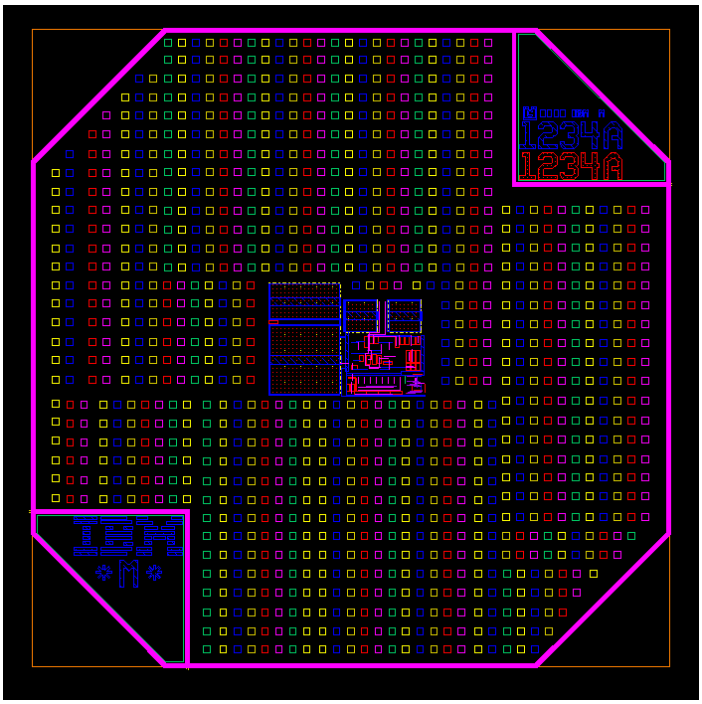


Fig. 4.66: Layout of the frequency synthesizer inside the chip-edge

Table 4.5 shows the comparison of performances of the designed frequency synthesizer with that presented in the literatures.

TABLE 4.5

PERFORMANCE SUMMARY AND COMPARISON OF FREQUENCY SYNTHESIZERS

Ref.	**Techno -logy**	**f_0 [GHz]**	**Range**	**Phase Noise [dBc/Hz]**	**Offset [MHz]**	**Power [mW]**	**Area [mm^2]**	**Type**
This Work	90 nm	12.0	3-12	-100.67	1	3.07	0.0158	Ring
[69]	90 nm	9.6	-	-93	1	27	0.11	Ring
[70]	90 nm	9.24	-	-97	0.2	56	0.09	Ring
[71]	90 nm	2.7	2.4-2.8	-121	1	23	0.014	Ring
[72]	90 nm	5.1	3.5-7.1	-105	1	29.64	0.121	Ring
[73]	90 nm (1.8 V)	1	-	-60	1	11.9	-	Ring
[74]	90 nm	0.432	0.35-0.7	-108	1	7	0.046	Ring

CHAPTER 5

Conclusions and future work

In this chapter we will summarize the outcome of our proposed Radio RF frequency synthesizer and discuss the future improvements or works to be done on this circuit.

5.1 Conclusions

Modern wireless communication systems operate in the GHz frequency range. Hence there is a necessity of a frequency synthesizer which must operate in the GHz range. The goal of this work is to design a frequency synthesizer which can generate frequency up to 12 GHz. We designed our frequency synthesizer using silicon (Si) CMOS process. A very few RF frequency synthesizer have been designed using Si process. Operating frequency around 12 GHz in Si based CMOS processes have not been reported till the present work.

To achieve the desired goal, it needs to first design a Voltage-controlled Oscillator (VCO) which can operate in the required frequency range. Then to design a Phase Frequency Detector (PFD) and Charge Pump (CP) that can fulfill the objective.

In this work a VCO has been designed which can operate from 2.51 GHz to 12.68 GHz with a constant gain and PFD-CP circuit for fast operation and glitch free charge pump output current. The proposed frequency synthesizer is designed using IBM 90nm process design kit in Cadence Electronic Design Automation tools. The schematic level design is drawn in Cadence Virtuoso Schematic Editor. The layout structure of the frequency synthesizer is drawn in Cadence Virtuoso Layout Editor. Finally from the simulation results we can conclude that our designed frequency synthesizer operate between 3 GHz and 12 GHz. The pre and post layout simulation results of each block of the frequency synthesizer are reported in this work. The pre and post layout simulation does not contradict much and satisfies our requirements.

5.2 Future work

In this work, we have not explicitly used the phase noise reduction technique. Phase noise can be further reduced by applying integral, half-integral injection

locking or phase alignment techniques. Charge pump is a significant source of phase noise in the circuit. This needs to be designed carefully. It can be further improved by reducing the current mismatch, charge share and charge injection. In this work we have not designed the divider circuit for a particular application but in general to show the functionality of the proposed frequency synthesizer. So, the divider circuit can be designed in such a way that it can be programmed according to the requirement of the application.

The proposed work is application oriented and any further improvement in this work will solidify its application.

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