CAPACITANCE-VOLTAGE CHARACTERISTICS OF ULTRATHIN MOS DEVICES WITH UNIAXIALLY STRAINED SILICON SUBSTRATE

A thesis submitted for the partial fulfillment of the requirement of the degree
of
Master of Science in Electrical and Electronic Engineering

By

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Contents

List of Figures

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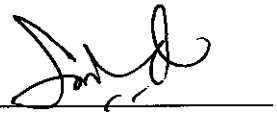

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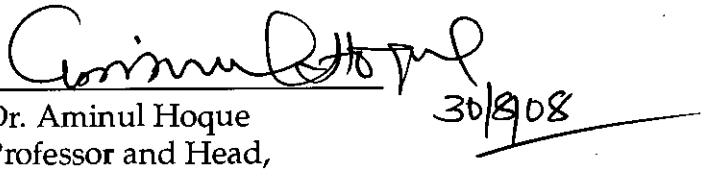

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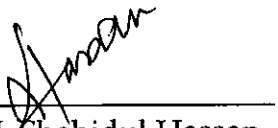

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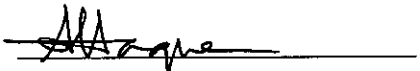

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Declaration

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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BUET, Dhaka,
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Dedication

To My Mother

Abstract

An accurate model to simulate gate capacitance versus voltage characteristics is developed for MOS devices with uniaxially strained silicon substrate. Strain is applied in <110> direction, most preferable direction of uniaxial strain for mobility enhancement. Tensile stress is applied for nMOS and compressive stress for pMOS devices. Proper energy profile correction for two conduction band valleys and effective mass change due to uniaxial strain are incorporated in the model. Significant amount of capacitance variation is obtained for stress levels varied up to 5 GPa, practical limit for uniaxial stress. It is observed that inversion region capacitance is varied in large proportion due to strain application. Change in effective mass in inversion region is found to be the dominant factor for the change of gate capacitance. It is also found that the capacitance corresponding to depletion region is less sensitive to strain. On the other hand accumulation C-V is less changed due to uniaxial strain. In accumulation region extended state charge increases with strain while accumulation charge decreases. Total charge is remained unaltered and this makes the capacitance value nearly independent of strain. Proper physical insights of all these changes are described.

Chapter 1

Introduction

Aggressive scaling of MOS devices in past decades has introduced the feature size to nanometer regime. A methodology has been given in [1] to show the scaling nature of MOS devices. As guided by the ITRS (International Technology Roadmap for Semiconductors), the scaling down has been accomplished by a decrease in gate-oxide thickness and increase in doping density. A complete scenario of scaling features of device size, oxide thickness and enhancement in doping concentration are given in ITRS [1].

Present day devices are produced in nanometer scale. In this small dimensions MOS device energy profiles for a particular operating voltage is no longer to be analyzed by semi-classical models [2, 3], instead quantum mechanical (QM) models must be used [4]. It is known that quantum confinement occurs in quantum wells of nanoscale devices and charges are quantized in several energy levels known as eigenenergies.

Device scaling has reached near saturation level and new alternative procedures are followed to increase device speed and other properties [5]. Straining is a technique that has been followed for mobility enhancement for quite a long time. Biaxial straining technique is used in different materials and its effects are also studied [6], [7]. Uniaxial straining process has recently been introduced [8], [9]. It has been found that mobility enhancement is more in case of uniaxial straining process than its biaxial counterpart [10]. Accurate

modeling of Capacitance-Voltage (C-V) is necessary for uniaxially strained Si devices for parameter extraction. In contrast to extensive study of biaxial straining [11], [12], uniaxial straining technique has been given less focus. In this work an accurate model is developed to simulate C-V characteristics for uniaxially strained devices with proper energy profile correction and effective mass change.

A number of self-consistent numerical simulators have been developed to simulate C-V characteristics accurately [13]. Wave function penetration effect occurs for nanometer scaled devices and when oxide thickness comes near 2 nm, its inclusion is a must for accurate modeling of C-V characteristics [14]. Extensive amount of work has been done to incorporate the wave function penetration effects on C-V characteristics of ultra-thin MOS devices [14], [15]. The simulator used for this work incorporates wave-function penetration effect.

1.1 Literature Review

Wave function penetration and quantization are the two most important phenomena for modeling ultrathin MOS devices. Extensive amount of study has been done on these two topics. Mudanai et al. [15] have shown a method to estimate capacitance voltage characteristics for nMOS devices incorporating wave function penetration. It has been seen that wave function penetration causes inversion charge distribution to shift toward the oxide-semiconductor interface and makes the capacitance value higher. For nanometer level oxide thickness this effect must be taken into account for accurate simulation of C-V.

Haque et al. [16] proposes a procedure to calculate normalized wave-functions in one dimensional well structure. Via this technique (i) the eigenenergies and the normalized eigenstates in quantum wells, (ii) the energy broadened spatially varying density-of-states in leaky quantum wells where the particle

lifetime is finite, and (iii) the energy position dependent density-of-states in quantum wells where phase-breaking and/or inelastic scattering processes are present, can be calculated. The method is based on the Green's function formalism.

Moglestue et al. [17] presented a self-consistent calculation for inversion region in both nMOS and pMOS devices where Schrödinger and Poisson's equations are solved to find the charge distribution. C-V results are compared with the one assuming triangular potential well. Necessity of wave function penetration for high-k gate dielectrics is discussed by Hakim et al. [18]. It was shown that without incorporating wave function penetration, C-V characteristics deviate from the original value.

Rahman et al. [19] showed broadening of quantized inversion layer states in deep submicron MOSFETs. This is needed for accurate modeling of ultrathin gate oxide dielectric C-V. Again Haque et al. [20] calculated the normalized electron wave functions in the inversion layers of nMOSFETs with ultra-thin gate oxides. Here an asymptotic boundary condition is taken that considers flat energy band profile deep inside the metal as well as deep inside the semiconductor. They showed that the use of the conventional boundary condition overestimates the distance of the carriers from the interface by a few angstroms. All these literatures are used to build self consistent model to simulate C-V characteristics incorporating wavefunction penetration.

Straining technique is used for quite a time for mobility enhancement. Biaxial straining process is well known for its application in MOS devices [11],[12], [21]. Uniaxial process has recently been introduced [8], [22]. Uniaxial process is used for its property to increase mobility than the biaxial process [10], [23], [24]. Uniaxial process is treated as the next generation technique for high speed devices but little concentration is given for accurate simulation of C-

V characteristics of MOS devices with uniaxially strained Si substrate. C-V simulation for biaxially strained device is studied in many literatures [25]. C-V characteristic is important for parameter extraction such as oxide thickness, doping density, flatband voltage etc. So accurate simulation of uniaxially strained devices is necessary for proper characterization.

Process of uniaxial strain is highlighted in [26],[27],[28]. Ranade et al. [29] describes 35 nm technology with uniaxial straining process. Thorough device physics study is done in [30],[31],[32]. Giusi [33] has studied the reliability of SiN capping layer which is used to introduce uniaxial strain. Zhao et al. [34] estimated drain current characteristics for uniaxially strained devices. But no literature has focused the study of C-V characteristics for uniaxially strained MOS devices.

Balslev [35] studied the effect of uniaxial strain on Si conduction band and valence band. He gave expressions of the net shift of energy profiles due to the application of strain. Laude [36] also gave this type of expressions but those are valid for low levels of stress. Strain causes curvature of the band structure to change. So variation of effective masses is expected. Dhar et al. [37] showed variation of effective masses with uniaxial <110> strain for two valleys of conduction bands. Incorporation of band diagram shift and effective mass change leads to develop C-V simulator for MOS devices with uniaxially strained silicon substrate for this work.

1.2 Objective of This Work

In this work, an accurate C-V simulator to simulate gate capacitance with uniaxial strain application is developed. The simulator is incorporated with wave function penetration consideration so that it can simulate C-V for ultrathin devices. Accurate band shifting along with effective mass change

from [35] and [37] are included so that devices under practical level of straining can be analyzed. Simulation is done with tensile stress for nMOS and compressive stress for pMOS. These are conventional stress types in CMOS technology. Stress level is varied up to 5 GPa, which is practical limit of stress application. Here stress is applied in <110>. Although stress can be given in other directions but for uniaxial straining process mobility enhancement occurs in maximum proportion if stress is applied in <110> direction. So <110> uniaxial strain is going to be studied in this work. Simulation of inversion and accumulation capacitance for electrons will be done. Physical insights of capacitance value changes will be discussed to understand the effect of strain.

1.3 Organization of The Thesis

In chapter 2 necessary theories to develop self-consistent model and strain effect on Si band structure and effective masses are discussed. Method of strain effect inclusion is presented. In chapter 3 simulated results are presented. Inversion and accumulation C-Vs are simulated for different stress conditions for electrons. Results are compared with relaxed C-V and percentage change is also given. Physical insight is discussed for C-V change due to strain application from total charge change. Simulations are also performed for different doping concentrations so that the effect of doping density on the C-V's strain effect can be analyzed. Finally complete flow chart of the simulator is given.

Chapter 2

Uniaxial Strain and Self-Consistent Model

This section describes uniaxial strain and self-consistent model. Complete analysis of uniaxial strain for MOS devices, as a parameter to alter band diagram as well as effective masses is given. The self-consistent model with wave function penetration consideration to generate C-V characteristics is also been presented.

2.1 MOS Structure

Metal-insulator-semiconductor (MIS) transistor is one of the most widely used electronic devices, particularly in digital integrated circuits. These types of devices are made using silicon as the semiconductor, SiO_2 as the insulator and metal or polysilicon as the gate electrode. The term metal oxide semiconductor field-effect transistor (MOSFET) or MOS devices is used to refer these devices.

Fig. 2.1 shows an n-channel enhancement-type MOS device. This device is fabricated on a p-type substrate which is a single-crystal silicon wafer that provides physical support for the device. Two heavily doped n-type regions termed as source and drain regions are created in the substrate. A thin layer of silicon dioxide (SiO_2) or any other material that is an excellent electrical insulator is grown on the surface of the substrate, covering the area between

the source and drain regions. Metal acts as the electrode for the device. Metal contacts are also brought out the source region, the drain region and the substrate also known as the body. Thus four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

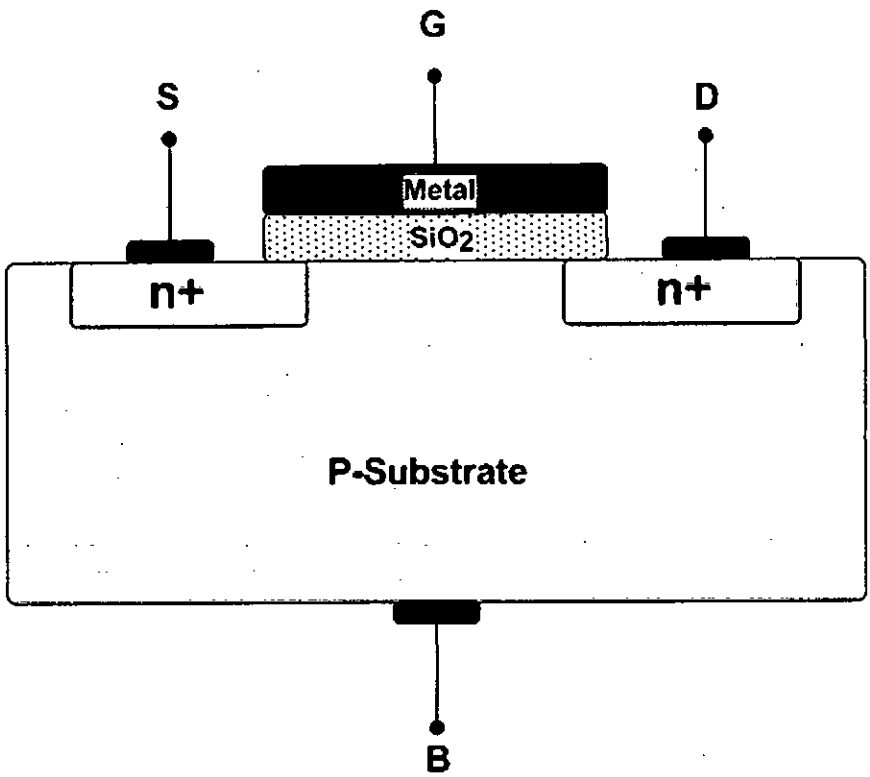

Fig. 2.1: Cross section of an enhancement-type n-MOSFET.

2.2 Gate Capacitance

The C-V characteristics of the MOS structure depends on whether the semiconductor surface is in accumulation, depletion or inversion. A typical C-V characteristics is shown in Fig. 2.2. The electrical equivalent of MOS capacitor is the series combination of a fixed voltage-independent gate insulator capacitance and a voltage-dependent semiconductor capacitance such that the overall MOS capacitance becomes voltage dependent.

The series capacitance in accumulation is basically the insulator capacitance,

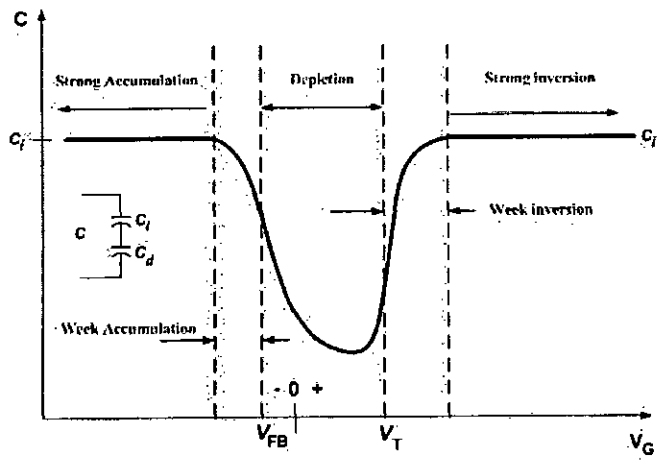

Fig. 2.2: Semi-classical C-V characteristics of an enhancement-type n-MOS.

C_{ox}. Since for negative voltage, holes are accumulated at the surface, the MOS structure appears almost like a parallel-plate capacitor dominated by the insulator properties. As the voltage becomes less negative, the semiconductor surface is depleted. The depletion layer capacitance C_d, added in series with C_{ox} to form the total capacitance. This value decreases until finally inversion is reached. After inversion is reached, the small signal capacitance depends on whether the measurements are made at high or low frequency. Here 'high' and 'low' are with respect to the generation-recombination rate of the minority carriers in the inversion layer. The charge in the inversion layer cannot change in response if the gate voltage is varied rapidly. Thus this does not contribute to the small signal a-c capacitance. Hence the semiconductor capacitance is at a minimum, corresponding to a minimum depletion width.

On the other hand if the gate bias is changed slowly, there is plenty of time for minority carriers to be generated in the bulk, drift across the depletion region to the inversion layer, or go back to the substrate and recombine. There is an increase in gate capacitance in inversion region as gate bias is increased. The low frequency MOS capacitance in strong inversion is basically C_{ox} once again. In accumulation we get a very high capacitance both at low and high frequencies because the majority carriers in the accumulation layer can respond

much faster than minority carriers.

2.3 Theory of Strain

Strain technique is widely used to enhance the performance of a MOS device. Present day MOS devices are strained in two ways, uniaxially and biaxially. Biaxial strain is quite familiar as it has been extensively studied [11],[12]. Uniaxial strain technique has been given less concentration and gate C-V characteristics study for MOS devices with uniaxially strained silicon substrate is absent in literatures. A complete theoretical insight of uniaxial straining process is given below.

2.3.1 Uniaxial Straining Process

Any straining technique is directly related to stress. A mechanical stress is applied to a device and it introduces strain in different directions. Biaxial straining is given by forming strained Si layer over a relaxed SiGe layer and vice versa. In this way lattice constant of Si is changed and specific change in properties such as band splitting and effective mass variation is observed. These effects lead to a change in C-V and other characteristics of MOS devices. Such changes are studied in [25].

Process of uniaxial strain is a little different from its biaxial counterpart. Two types of uniaxial strain is given. Tensile strain is given to nMOS devices and compressive strain to pMOS devices [38]. These are done as different straining process enhances mobility in different proportions in different devices. Usually SiGe is used in source and drain side or nitride capping layer is used on the gate for uniaxial straining process. Nitride capping layer can be used for both compressive and tensile stress. Both the processes introduces a stress in the channel region of the MOS device and as a result strain is introduced. Physical picture of uniaxial straining process is shown in Fig. 2.3 and Fig. 2.4.

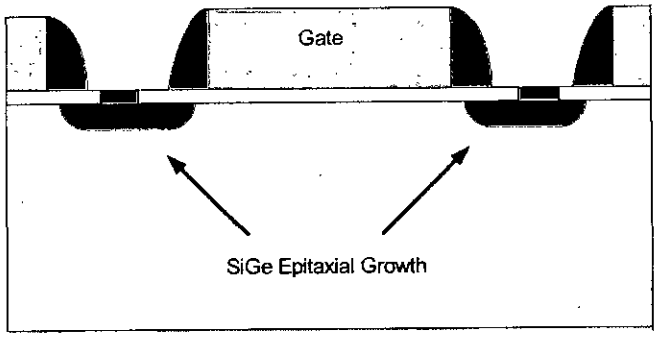

Fig. 2.3: Uniaxial straining process with SiGe layer in source and drain region.

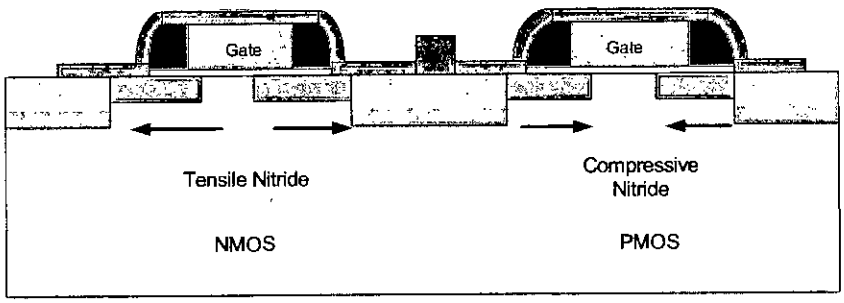

Fig. 2.4: Uniaxial straining process with nitride capping layer.

In Fig. 2.5 process of biaxial stress [9] is shown. Here a cubic crystal is in biaxial tensile stress. Application of the stress causes xy plane to remain as a square but x and yz plane are no longer square. They are now rectangular. In Fig. 2.6 cubic crystal under <110> uniaxial compressive stress is shown. Here x and yz planes become rectangles but xy plane becomes a rhombus. This introduces shear strain terms which is absent in biaxial strain. These shear terms make the characteristics of MOS devices to change from biaxial straining results.

Relationship between stress and strain can be shown by a matrix multiplication. It can be expressed as, $\epsilon = S.\sigma$. Elaborately it is shown as,

$$\begin{bmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \\ \epsilon_{yz} \\ \epsilon_{zx} \\ \epsilon_{xy} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{12} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44}/2 & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44}/2 & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44}/2 \end{bmatrix} \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{bmatrix} \tag{2.1}$$

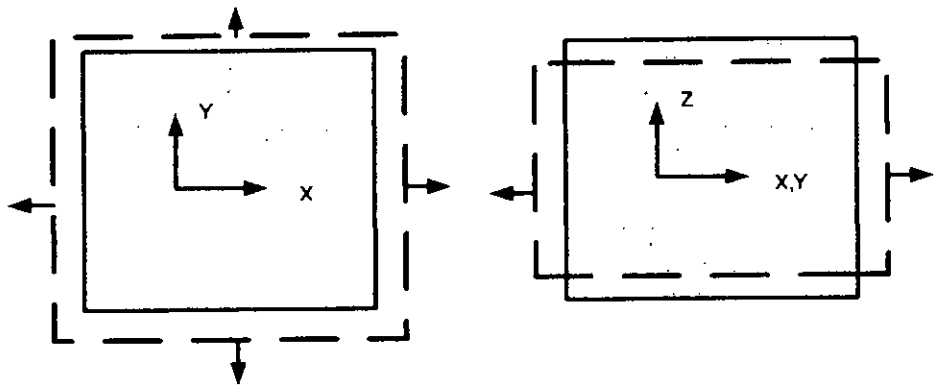

Fig. 2.5: Cubic crystal under in plane biaxial tensile stress.

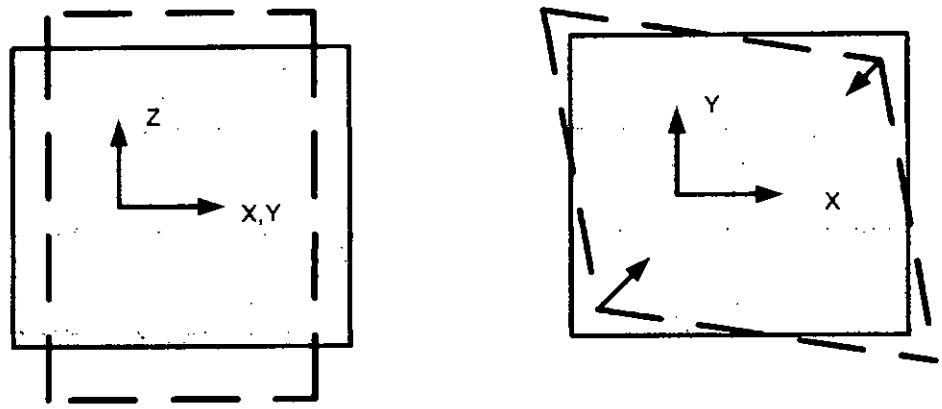

Fig. 2.6: Cubic crystal under uniaxial <110> compressive stress.

Here, x, y, z are directions of applied stress and resulted strain. S_{11}, S_{12}, S_{44} are conventional compliance coefficients. The values for Si are,

$S_{11} = 8.63 \times 10^{-12} N^{-1} m^2$

$S_{12} = -2.13 \times 10^{-12} N^{-1} m^2$

$S_{44} = 12.49 \times 10^{-12} N^{-1} m^2$

For <110> uniaxial stress σ is applied in three different directions. They are given as, $\sigma_{xx} = \sigma_{yy} = \sigma_{xy} = \sigma/2$. As there is σ_{xy}, shear strain terms are introduced which is completely absent in biaxial strain. This makes uniaxial straining technique favorable in terms of mobility enhancement and at the same time complex to evaluate the effect caused by it.

2.3.2 Band Splitting Due to Uniaxial Strain

Strain causes valley degeneracy to lift. So band structure does not remain same for strained and relaxed silicon. In relaxed silicon two conduction bands, Δ_2 and Δ_4 are at degenerate state. As strain is introduced degeneracy is lifted. For tensile stress Δ_4 band goes up and Δ_2 moves down. Opposite situation arises for compressive stress. Similarly for valence band, heavy hole and light hole (HH and LH) bands are at degenerate state for relaxed silicon. Strain lifts this degeneracy and for tensile stress LH band goes up and HH moves down. Due to the shift of the bands, band gap energy E_g also changes. All these changes are necessary to model strain effect in MOS devices correctly. In Fig. 2.7 conduction band and valence band change due to uniaxial tensile stress are shown.

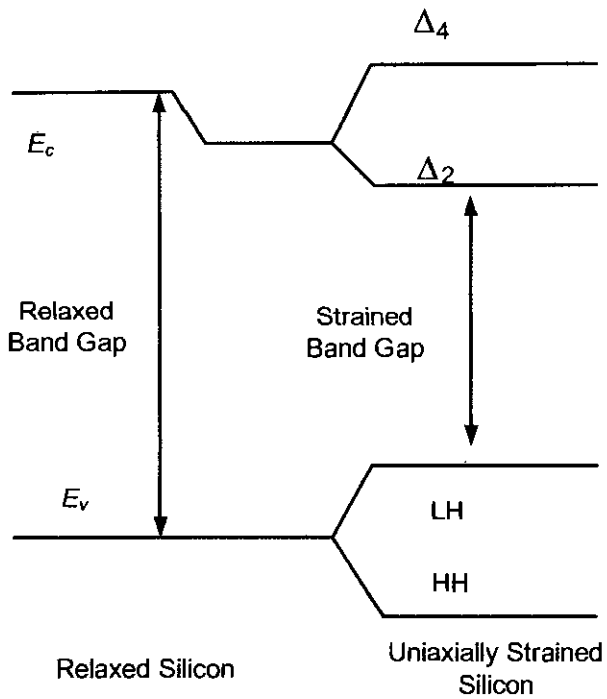

Fig. 2.7: Band splitting due to uniaxial tensile stress.

Expressions of band splitting as a function of strain is presented in many literatures. Laude et al. presented some equations in [36]. But these expressions are applicable for low stress levels. Hasegawa [39] also studied the valence band structure but no interrelation with the conduction band is given. Here

expressions by Balslev [35] are followed. According to Balslev, band splitting due to uniaxial <110> strain is,

$$\Delta E_c^2 - \Delta E_c^0 = -\frac{1}{3}(S_{11} - S_{12})\Xi_u P \tag{2.2}$$

$$\Delta E_c^4 - \Delta E_c^0 = \frac{1}{6}(S_{11} - S_{12})\Xi_u P \tag{2.3}$$

$$\Delta E_c^0 = \Delta E_{g0} - |E_{\epsilon\epsilon}| - \frac{1}{3}(S_{11} - S_{12})\Xi_u P \tag{2.4}$$

$$\Delta E_g^0 = (\Xi_d + \frac{1}{3}\Xi_u - a)(S_{11} + 2S_{12})\Xi_u P \tag{2.5}$$

$$|E_{\epsilon\epsilon}| = \frac{1}{2}[b^2(S_{11} - S_{12})^2 + 3(\frac{d}{2\sqrt{3}}S_{44})^2]^{\frac{1}{2}}|P| \tag{2.6}$$

Here, ΔE_c^0 = Hydrostatic band shifting of the conduction band

ΔE_c^i = Band splitting for the ith valley

ΔE_{g0} = Change in the energy band gap

P = Applied stress

Ξ_u = 8.6 eV

$\Xi_d + \frac{1}{3}\Xi_u - a$ = 3.8 eV

Eqn. 2.2 is the band splitting for Δ_2 conduction band valley, eqn. 2.3 is for Δ_4 conduction band valley with respect to the mean position of conduction band shift. Eqn. 2.4 represents hydrostatic shift of the mean position of the conduction band. Finally 2.6 is for valence band splitting. High amount of stress in GPa range can create significant amount of band splitting and this effect can cause change in the total charge distribution and as a consequence C-V characteristics. Change in two conduction band valleys, energy gap and valence band are shown in figs. 2.8 and 2.9. It is clear that strain causes considerable amount of band splitting and it has to be taken into account for the accurate simulation of electrostatic behavior of MOS devices with strained silicon substrate.

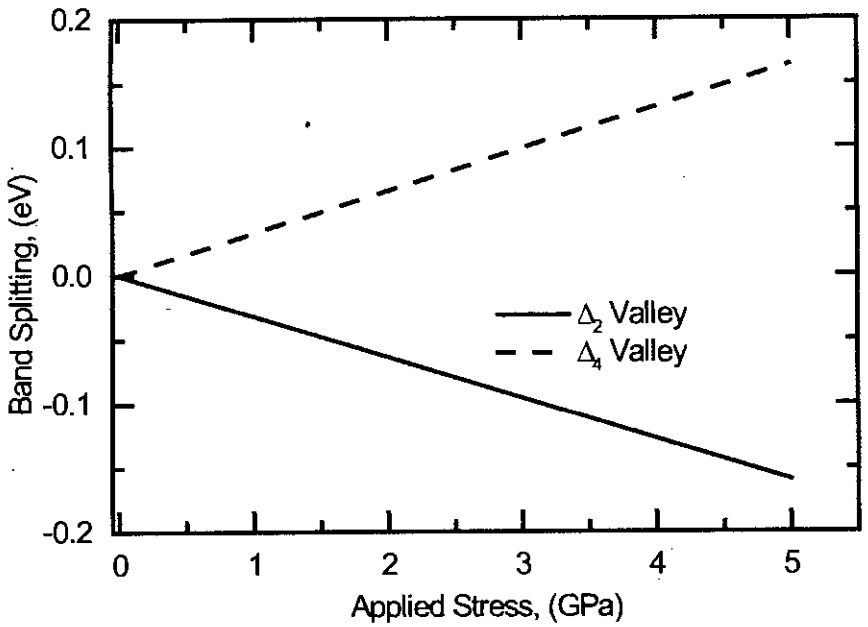

Fig. 2.8: Conduction band splitting due to uniaxial tensile stress.

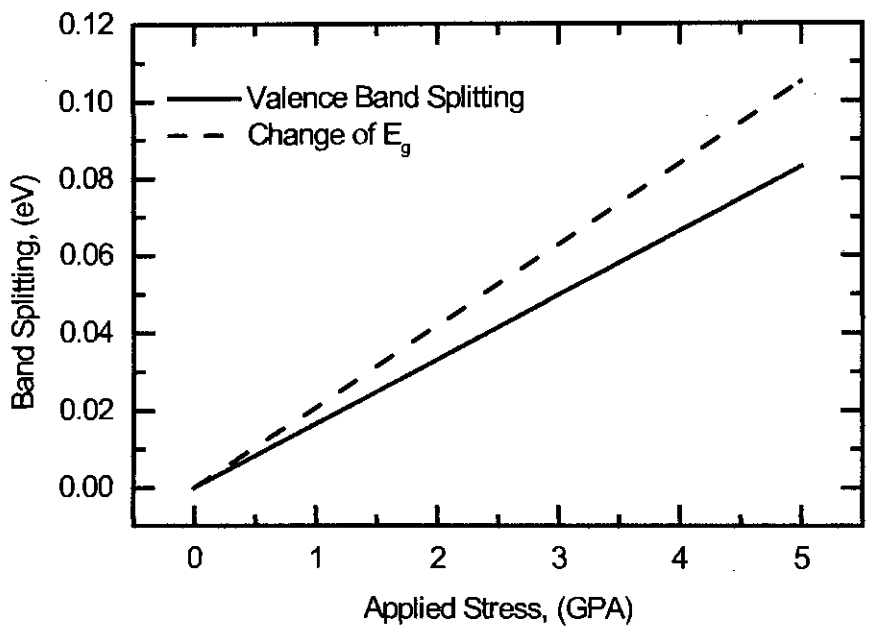

Fig. 2.9: Valence band splitting and change in energy gap due to uniaxial tensile stress.

2.3.3 Effective Mass Variation Due to Uniaxial Strain

Uniaxial strain causes the curvature of energy diagram to change from that of the relaxed condition. As effective masses are dependent on the curvature

of energy diagram, changes in all the effective masses (both quantization and density of state) for both the conduction bands are expected. Dhar et al. [37] showed the change in the effective mass in three different directions as a function of applied stress as,

$$m_x = 0.918 + 0.0236X^2 \tag{2.7}$$

$$m_y = 0.196 - 0.016X \tag{2.8}$$

$$m_z = 0.196 + 0.029X \tag{2.9}$$

Here, m_x, m_y and m_z are effective masses in three crystal directions, 100, 010, 001. From these expressions quantization and density of state effective masses are derived as,

$$m_{d1} = \sqrt{m_y m_z} \tag{2.10}$$

$$m_{z1} = m_x \tag{2.11}$$

$$m_{d2} = \sqrt{m_x m_y} \tag{2.12}$$

$$m_{z2} = m_z \tag{2.13}$$

Here, m_{z1} and m_{d1} are the quantization and density of states effective masses for the Δ_2 conduction band valley, m_{d2} and m_{z2} are same for the Δ_4 conduction band valley. Variation of these effective masses are shown in Fig. 2.10 and in Fig. 2.11.

Compressive strain is applied to pMOS devices so change in effective masses due the application of compressive stress is also important. Fig. 2.12 and 2.13 shows change in density of states and quantization effective masses due to

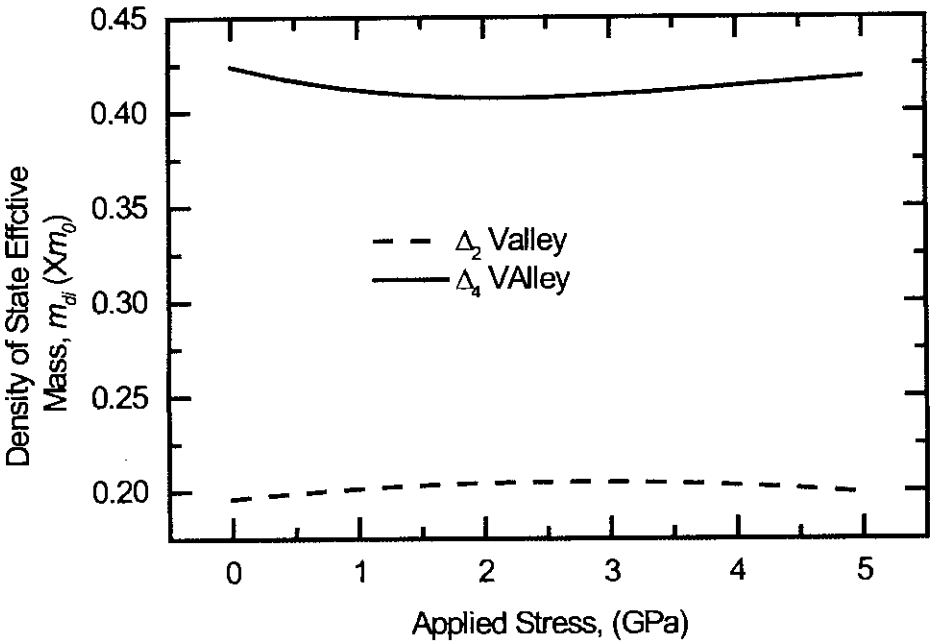

Fig. 2.10: Change in density of states effective masses with stress.

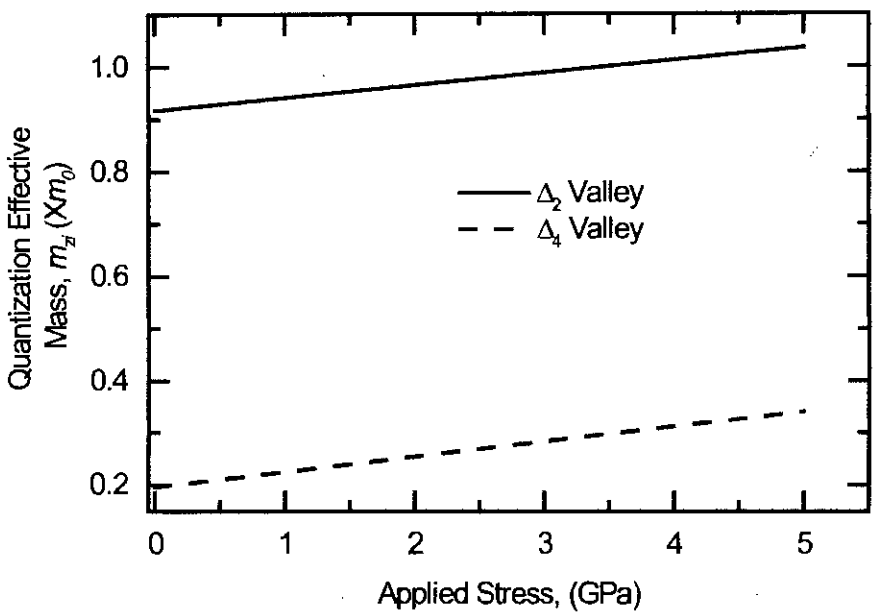

Fig. 2.11: Change in quantization effective masses with stress.

compressive stresses.

Effective masses play a vital role in charge calculation and calculation of

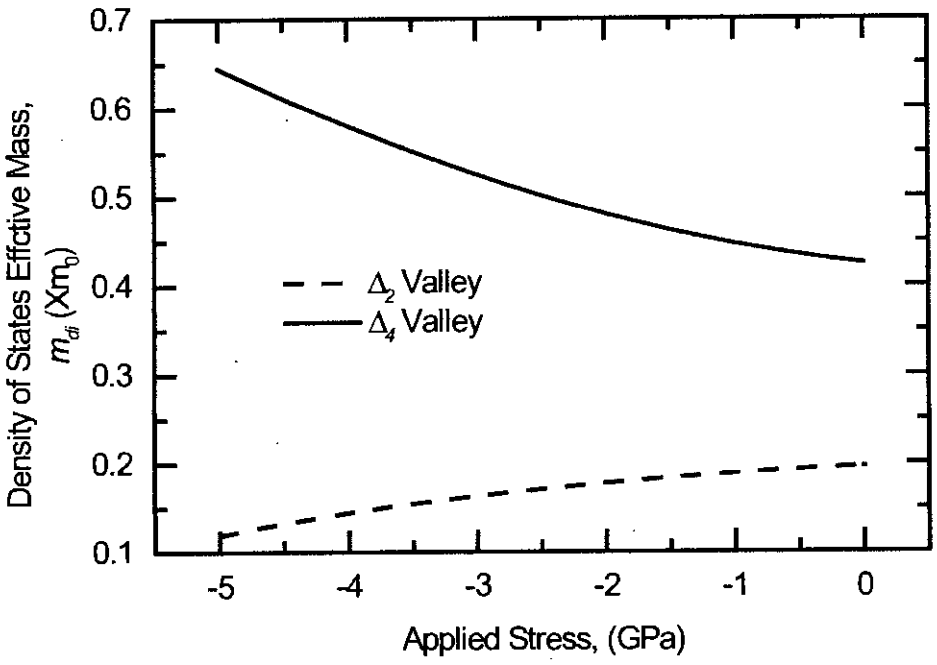

Fig. 2.12: Change in density of states effective masses with compressive stress.

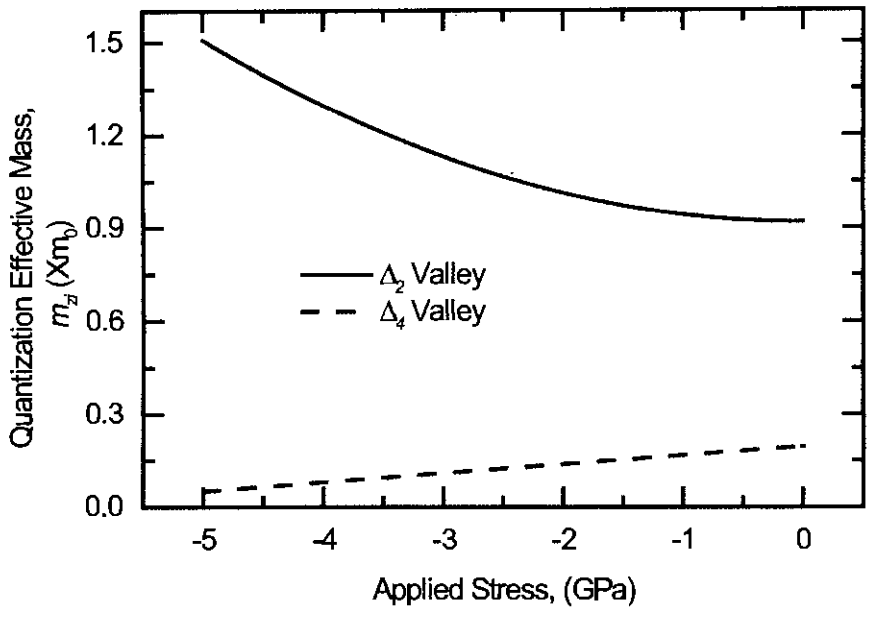

Fig. 2.13: Change in quantization effective masses with compressive stress.

eigenenergies. As seen from the figures strain causes large change in effective mass values. So it will also cause change in total charge distribution. These changes are to be incorporated in numerical calculations to generate accurate

C-V.

Both band splitting and effective mass variations are incorporated in this work with the expressions given above. Change in E_g causes the intrinsic carrier density to change from its relaxed value of $1.5 \times 10^{10} cm^{-3}$ as,

$$N_i = 1.5 \times 10^{10} cm^{-3} \times \exp \Delta E_g \tag{2.14}$$

2.4 Self Consistent Simulator

Self-consistent Schrödinger-Poisson solver is widely used for simulation of MOS devices. In this work the self consistent simulator used is based on Green's function formalization [14]. Detail of the calculations are given below.

2.4.1 Basic Model

Schrödinger solver

Stern [4] and Moglestue [17] described a self-consistent solution approach for the first time. Three major assumptions by Stern were,

(1) Effective mass approximation is valid. So periodic potential need not be taken into account.

(2) At the silicon surface envelop wavefunction vanishes.

(3) Surface states are neglected and any charge in the oxide near semiconductor body can be replaced by an electric field.

By the effective mass approximation, Schrödinger's equation for the wave function $\psi_{0_{ij}}$ can be written as,

$$[-\frac{1}{2}\hbar^2\nabla m^{*-1}\nabla + eV(z)]\psi_{0_{ij}} = E'_{ij}\psi_{0_{ij}} \tag{2.15}$$

Here, m^{*-1} is the effective mass tensor, $V(z)$ the electrostatic potential, e is electron charge magnitude and E'_{ij} is the energy. z is the direction in the MOSFET from gate to the bulk body.

Stern [4] showed that the electronic wavefunction $\psi_{0_{ij}}$ for the jth subband in the ith valley can be expressed in terms of Bloch function traveling parallel to the interface, constrained by an envelope function normal to it. This is represented as,

$$\psi_{0_{ij}}(x,y,z) = \psi_{ij}(z)e^{i\theta z}e^{ik_x x + ik_y y} \tag{2.16}$$

where, k_x and k_y represents the component of the wave vector k in x and y direction. θ depends on k_x and k_y. $\psi_{ij}(z)$ can be obtained from,

$$[-\frac{\hbar^2}{2m_{zi}}\frac{d^2}{dz^2} + eV(z)]\psi_{ij}(z) = E_{ij}\psi_{ij}(z) \tag{2.17}$$

where, m_{zi} is the quantization effective mass and E_{ij} is the eigenenergy of the jth subband in the ith valley in the perpendicular direction.

Here two boundary conditions are used for the solution of (2.17). They are,

- $\psi_{ij}(\infty) = 0$ deep inside the semiconductor
- $\psi_{ij}(0) = 0$ at the metal oxide interface.

Each eigenvalue E_{ij} found from the solution of Eq. (2.17) is the bottom of subband, with energy levels given by,

$$E'_{ij} = E_{ij} + \hbar^2 k_x^2/2m_x + \hbar^2 k_y^2/2m_y \tag{2.18}$$

here m_x and m_y are the effective masses in the transport plane. The conduction band of silicon has six ellipsoidal valleys along the 100 direction of the Brillouin zone. As a result there can be as many as three values of m_z depending on the surface orientation. From the effective mass approximation, the valleys are degenerated in pairs. So the solution of Eq. (2.17) gives the eigenenergy E_{ij} and the envelope function $\psi_{ij}(z)$.

2.4.2 Green's Function Formalism

The process of Schrödinger's equation solution as stated above is based on Green's function [19]. Green's function is a technique for calculating an effect at a certain point due to disturbance at any other point. In MOS devices retarded Green's function for the i'th valley at a distance z is given by,

$$[E + \frac{\hbar^2}{2m_{zi}}\frac{\partial^2}{\partial z^2} - eV(z) + i\epsilon]G_i^R(z, z^{'}; E) = \delta(z - z^{'}) \tag{2.19}$$

Here ϵ is an infinitesimally small positive energy. Its value is in 10^{-12} range. Retarded Green's function $G_i^R(z, z^{'}; E)$ is a wave function at z originated by an excitation at z'. An important fact here is this that Green's function is continuous at $z = z'$ and the derivative is discontinuous at z' by, $2m_{zi}/\hbar^2$.

One dimensional density of states, N_{1D}, eigenenergies E_{ij} and normalized wavefunctions, ψ_{ij} are calculated using the retarded Green's function. The logarithmic derivative of the retarded Green's function G^R is defined by,

$$Z_i(z, z'; E) = \frac{2\hbar}{im_{zi}}[\frac{\partial G_i^R(z, z^{'}; E)}{\partial z}/G_i^R(z, z^{'}; E)] \tag{2.20}$$

Two boundary conditions are needed to estimate $Z_i(z, z'; E)$ as $Z_i(z, z'; E)$ has a discontinuity at $z = z'$. Here we assume that potential profile is flat inside the semiconductor and inside the metal at a distance far from the oxide semiconductor interface. So if we have $V(\infty)$ is the constant potential at $z = \infty$

(deep inside the semiconductor) and if $V(-\infty)$ is the constant potential at $z = -\infty$ (deep inside the gate metal), Green's function may be expressed as,

$$G_i^R(z \longrightarrow \infty, z'; E) \sim e^{\gamma_i(\infty)(z-z')} \tag{2.21}$$

and

$$G_i^R(z \longrightarrow -\infty, z'; E) \sim e^{-\gamma_i(-\infty)(z-z')} \tag{2.22}$$

where, $\gamma_i(\pm\infty) = i\sqrt{(2m_{zi}/\hbar^2)(E - eV(\pm\infty) + i\epsilon)}$. The boundary conditions to estimate Z_i are determined from Eq. (2.21) and (2.22). These are,

$$Z_i(z \longrightarrow \infty, z'; E) = Z_{oi}(\infty), z > z' \tag{2.23}$$

and

$$Z_i(z \longrightarrow -\infty, z'; E) = Z_{oi}(-\infty), z < z' \tag{2.24}$$

where, $Z_{oi}(\pm\infty) = (2\hbar/im_{zi})\gamma_i(\pm\infty)$. From the properties of 1D Green's functions, it can be shown [16], for all $z > z'$:

$$Z_i(z, z'; E) = Z_i^+(z; E) \tag{2.25}$$

for all $z < z'$,

$$Z_i(z, z'; E) = Z_i^-(z; E) \tag{2.26}$$

here, $Z_i^+(Z_i^-)$ does not depend on z' as long as $z > z'$ ($z < z'$). To calculate, $Z_i^\pm$ method described by [40] is followed. Here microwave transmission line

analogy is used to find the eigenenergies for any quantum well. Use of this technique in MOS quantum wells is given in [20].

The normalized wave function is calculated from retarded Green's function. We have G_i^R expressed as a function of complete set of eigenfunctions,

$$G_i^R(z,z';E) = \sum_j \frac{\psi_{ij}(z)\psi_{ij}^*(z')}{E - E_{ij} + i\epsilon} \tag{2.27}$$

If $E_{i(j+1)} - E_{ij} >> \epsilon$ for all j, only one term dominates when $E \rightarrow E_{ij}$, as the discrete eigenenergies are degenerate. For the diagonal elements of G_i^R, we obtain

$$G_i^R(z,z';E \rightarrow E_{ij}) \cong \frac{|\psi_{ij}(z)|^2}{E - E_{ij} + i\epsilon} \tag{2.28}$$

Equating imaginary parts of (2.28) and putting $E = E_{ij}$,

$$|\psi_{ij}(z)|^2 = -\epsilon Im[G_i^R(z,z';E_{ij})] \tag{2.29}$$

It has been shown in [16] that,

$$-Im[G_i^R(z,z';E_{ij})] = \frac{4}{\hbar} Im(\frac{i}{Z_i^+(E_{ij}) - Z_i^-(z;E_{ij})}) \tag{2.30}$$

From (2.30) in (2.29),

$$|\psi_{ij}(z)|^2 = \frac{4\epsilon}{\hbar} Im(\frac{i}{Z_i^+(z;E_{ij}) - Z_i^-(z;E_{ij})}) \tag{2.31}$$

Again 1D state of density N_{1D} is related to the diagonal part of G^R. $N_{1D_i}(z;E)$, in terms of retarded Green's function, G_i^R is given by,

$$N_{1D_i}(z;E) = -\frac{1}{\pi} Im[G_i^R(z,z';E)] \tag{2.32}$$

When $\epsilon \rightarrow 0^+$, the density-of-states (DOS), $N_{1D_i}(z;E)$, becomes a delta function at the eigenenrgies, $E = E_{ij}$ in a bound system with the amplitude equal to the probability density at that energy, i.e.,

$$N_{1D_i}(z;E) = \sum_j |\psi_{ij}(z)|^2 \delta(E - E_{ij}) \tag{2.33}$$

Final expression of N_{1D_i} is given by,

$$N_{1D_i}(z;E) = \frac{V_i}{\pi} \frac{|\psi_{ij}(z)|^2}{(E - E_{ij})^2 + V_i^2} \tag{2.34}$$

Using Eq. (2.32), N_{1D} can be expressed in terms of the logarithmic $Z_i^{\pm}$ [16]:

$$N_{1D_i}(z;E) = \frac{4}{\pi\hbar} Im(\frac{i}{Z^+(z;E) - Z^-(z;E)}) \tag{2.35}$$

Poisson solver

Poisson solver is needed to obtain the potential profile $V(z)$. This is the starting phase of the self-consistent simulator. Here Poisson's equation is solved by finite difference method considering nonuniform grid spacing. Grid spacing is finer near oxide semiconductor interface.

$$\frac{d^2V(z)}{dz^2} = -\frac{[\rho_{depl}(z) + \rho_{inv}(z)]}{\epsilon_{si}\epsilon_0}, \quad for \quad z > Tox \tag{2.36}$$

$$\frac{d^2V(z)}{dz^2} = -\frac{[\rho_{inv}(z)]}{\epsilon_{ox}\epsilon_0}, \quad for \quad z \leq Tox \tag{2.37}$$

Here, ϵ_{si} is the dielectric constant of semiconductor, ϵ_{ox} is the dielectric constant of oxide, $\rho_{depl}(z)$ is the depletion charge and $\rho_{inv}(z)$ is the inversion charge distribution along z. Inversion charge is calculated with wave-function penetration effect consideration. Once proper charge distributions are known accurate determination of the potential profile is done. $\rho_{inv}(z)$ is calculated from eigenenergies and wave-function values. It is given by,

$$\rho_{inv} = \sum_{ij} N_{ij} |\psi_{ij}(z)|^2 \tag{2.38}$$

$$N_{ij} = \frac{n_{vi} m_{di} kT}{\pi \hbar^2} \ln[1 + \exp(\frac{E_F - E_{ij}}{kT})] \tag{2.39}$$

Here, n_{vi} is the valley degeneracy and m_{di} is the density of states effective mass of the ith valley as shown in the previous section. E_F is the Fermi level.

Depletion charge density $\rho_{depl}(z)$ is given by,

$$\rho_{depl}(z) = \begin{cases} -e(N_A - N_D), & 0 < z < z_d \\ 0, & z > z_d \end{cases} \tag{2.40}$$

here, z_d is the depletion layer thickness which is given by,

$$z_d = \sqrt{\frac{2\epsilon_{si}\epsilon_0 \Phi_d}{e(N_A - N_D)}} \tag{2.41}$$

where Φ_d is the depletion charge band bending. Φ_d is given by,

$$\Phi_d = \Phi_s - \frac{kT}{e} - \frac{eN_{inv} z_{avg}}{\epsilon_{si}\epsilon_0} \tag{2.42}$$

Here, Φ_s is the total band bending of the semiconductor. N_{inv} is the total inversion charges per unit area in the inversion layer. It is expressed as,

$$N_{inv} = \sum_{ij} N_{ij} \tag{2.43}$$

Again z_{avg} is the average distance of the inversion charge from the silicon-oxide interface and it is given by,

$$z_{avg} = (1/N_{inv}) \sum_{ij} N_{ij} \int z|\psi_{ij}|^2 dz \tag{2.44}$$

Boundary conditions are used for the solution of Eq. (2.36). These are,

- $V(z_d) = 0$
- $V(0) = V_g$, at the metal oxide interface. Here V_g acts as the gate voltage input.
- At the oxide semiconductor interface$F_s = F_{ox}$, where,

$$F_s = \frac{e(N_{inv} + N_{depl})}{\epsilon_{si}\epsilon_0} F_{ox} = \frac{e(N_{inv} + N_{depl})}{\epsilon_{ox}\epsilon_0} \tag{2.45}$$

are the surface electric fields and,

$$N_{depl} = z_d(N_A - N_D) \tag{2.46}$$

is the number of charge per unit area in the depletion layer.

2.4.3 Coupling Schrödinger and Poisson's Equation

Calculation for inversion

Self-consistent simulation is done for each gate bias for a MOS device. Here gate bias acts as the input. First for a particular gate bias Poissin's equation 2.36 is solved by finite difference method. According to finite difference method,

$$\frac{d^2V}{dz^2} = \frac{V_{n+2} - 2V_{n+1} + V_n}{\delta z^2} = -\rho_n/\epsilon \tag{2.47}$$

Here, n+2, n+1 and n are different grid space points. ρ_n is the value of total charge in space point n and ϵ is the dielectric constant for oxide or the semiconductor. Solving the Poisson's equation, voltage profile for a particular gate bias is gained. From it potential profile is estimated. Schrödinger's equation is solved by retarded Green's function to get the eigen states and from that inversion charges are calculated for each state and for each valley (2.39). From these charges ρ_{inv} is estimated. Taking the full charge profile, (ρ_{inv}, ρ_{depl}) Poisson's equation is solved again. A new potential profile is generated by taking 96% percent of the older profile and 4% of the newer profile. Whole calculation is done again. This procedure is repeated until error between the two successive profiles is less than 0.01%.

For higher gate voltages starting potential profile for the calculation is taken as the last converged profile of previous gate volteg.

Calculation for accumulation

Calculation for accumulation region is same as that of inversion region except the depletion charge absence. Here a new charge is introduces and that is the extended states charge. Though in inversion, extended state charges are also present, but it can be neglected due to the lower value of Fermi potential. But in accumulation region Fermi level is very close to the conduction band and this makes the extended state charges dominant. Extended state charges are calculated in the following way,

$$Q_{extnd} = \int_{E_c}^{\infty} f(E)g_c(E)dE \tag{2.48}$$

for conduction band

$$Q_{extnd} = \int_{-\infty}^{E_v} f(E) g_v(E) dE \tag{2.49}$$

for valence band

Here, $f(E)$ is the Fermi function given by,

$$f(E) = \frac{1}{1 + \exp^{E - E_F/kT}} \tag{2.50}$$

and, $g_{c,v}(E)$ is density of states as,

$$g_c(E) = \frac{m_n^* \sqrt{2m_n^*(E - E_c)}}{\pi^2 \hbar^3} \tag{2.51}$$

for conduction band

$$g_v(E) = \frac{m_p^* \sqrt{2m_p^*(E_v - E)}}{\pi^2 \hbar^3} \tag{2.52}$$

for valence band

Here, m_n^* and m_p^* are the conduction and valence band effective masses respectively.

Chapter 3

Simulations and Results

In this chapter simulations and physical explanation of the change in C-V are given. Inversion C-V for nMOS and accumulation C-V characteristics for pMOS are given with practical strain limit. Here all the simulations are done for <110> unixial strain. <110> direction is chosen for its wide practical use and the effect on mobility enhancement of electron [10]. Tensile stress is applied for nMOS and compressive stress is applied for pMOS. This is chosen as tensile stress introduces greater amount of mobility enhancement in nMOS and compressive stress does the same for pMOS. Different doping density is used to observe the doping density dependence of strain effect on the C-V characteristics.

3.1 Inversion Capacitance Change Due to Uniaxial Strain

Fig. 3.1 shows C-V characteristics for relaxed and strained silicon MOS devices. Here doping density $N_a = 10^{18} cm^{-3}$, oxide thickness T_{ox} = 2 nm, oxide material is SiO_2. Significant amount of change is observed in C-V for strained case with respect to relaxed Si case. C-V change is dominant in inversion region. There is insignificant amount of variation of C-V in depletion region due to strain. Strain causes inversion region to alter in more proportion than the depletion region.

Percentage change of C-V for strained Si devices is shown in Fig. 3.2. It can be seen that increase in strain increases the change in C-V. More strain causes more deviation for gate capacitance. Up to 5% of change is observed for X = 5 GPa of stress. This indicates significant amount of C-V variation due to uniaxial strain application.

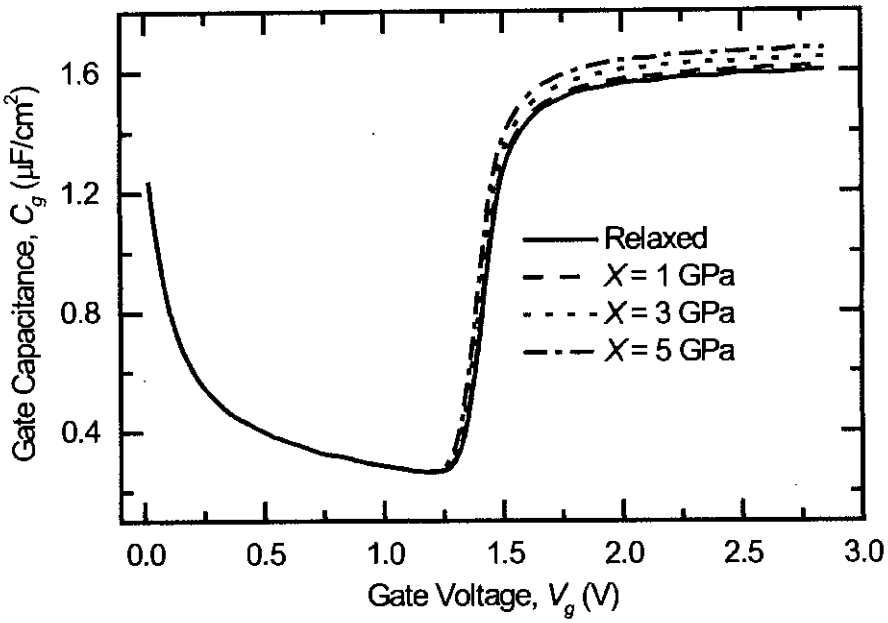

Fig. 3.1: Gate capacitance vs. gate voltage for relaxed and strained Si MOSFETs with $N_a = 10^{18} cm^{-3}$.

To understand the physical insight of the C-V change complete electrostatic study of strained device is done. Fig. 3.3 shows total charge vs. gate voltage characteristics of relaxed and strained Si devices. It is clearly seen that for low bias or in depletion region there are insignificant changes in charge, but for higher gate bias or in inversion region, we have considerable amount of charge change due to strain. As $C_g = \frac{dQ_{tot}}{dV_g}$, capacitance change is also observed in high bias region. Depletion band bending and depletion width for strained devices is shown in Figs. 3.4 and 3.5. It is clearly seen that strain has virtually no effect on these two characteristics and as a result no change in depletion layer charges is seen. This leads to no change in depletion capacitance. Fig. 3.6 shows change

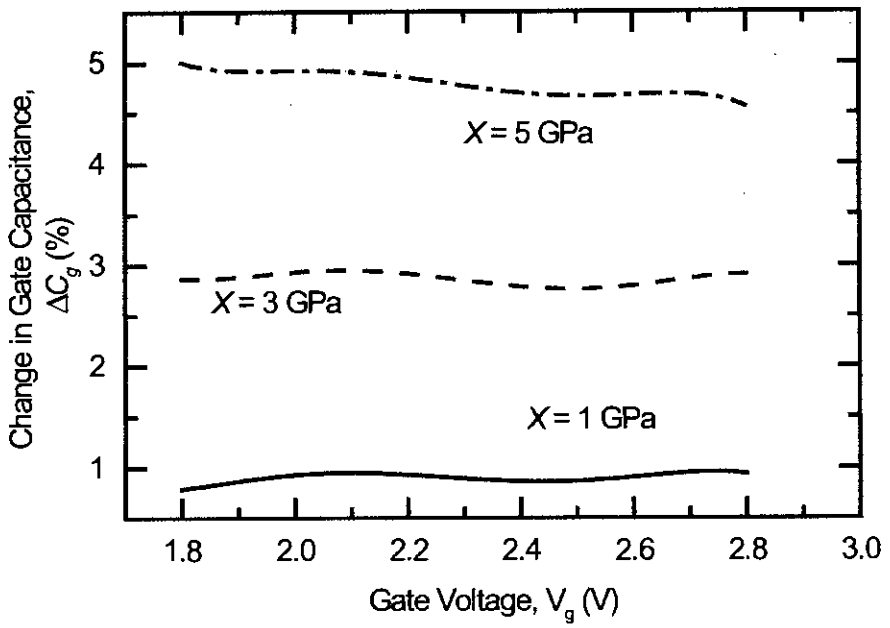

Fig. 3.2: Change in gate capacitance of strained Si MOSFETs with respect to relaxed Si MOSFET.

in inversion layer charges with strain. Inversion layer charges are changed with a great percentage due to application of strain.

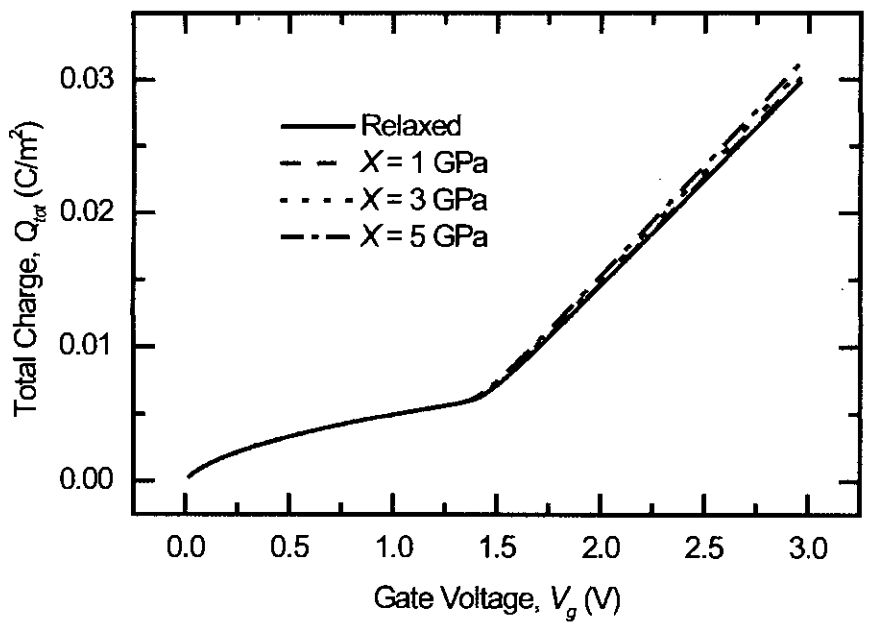

Fig. 3.3: Total charges of relaxed and strained Si MOSFETs.

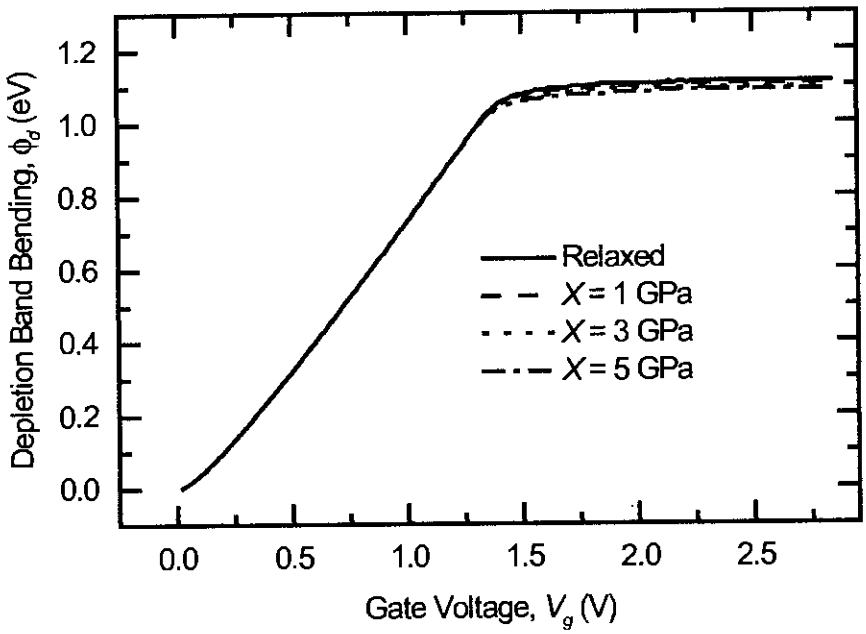

Fig. 3.4: Depletion band bending of relaxed and strained Si MOSFETs.

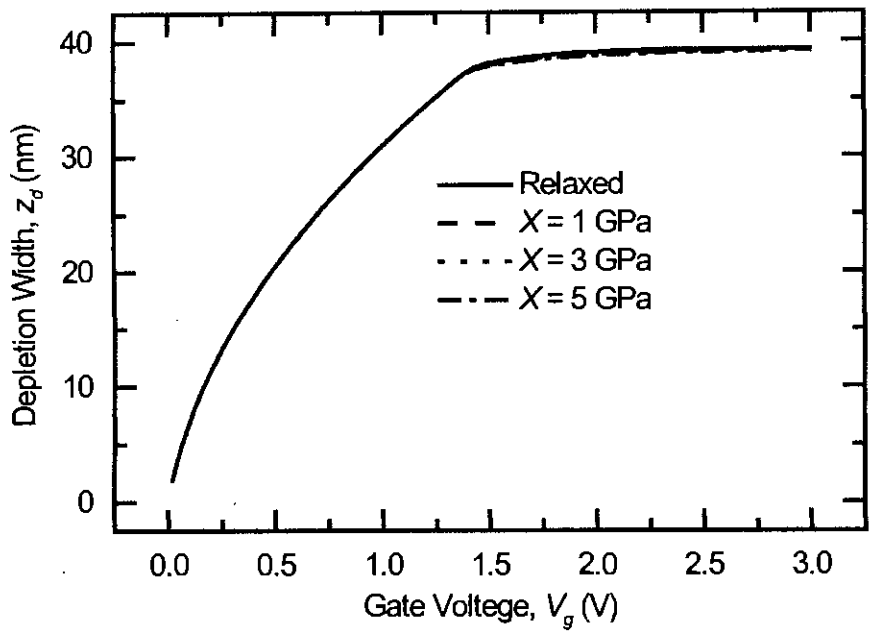

Fig. 3.5: Depletion width change of relaxed and strained Si MOSFETs.

As $C_{inv} = \frac{dQ_{inv}}{d\phi_s}$, change in the inversion charges leads to significant change in inversion capacitance. This change is shown in Fig. 3.7. Inversion capacitance change trend is identical to the change in gate capacitance confirming gate

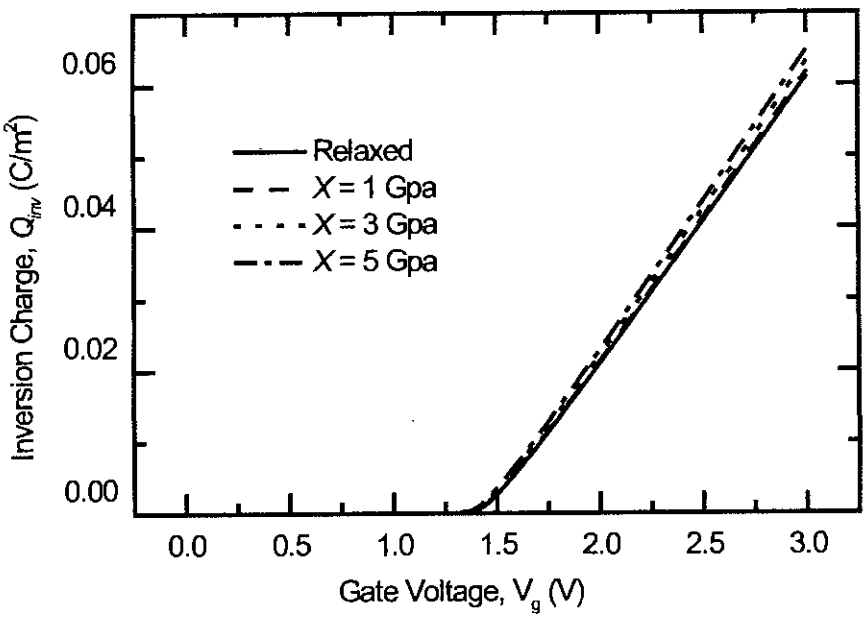

Fig. 3.6: Inversion charges of relaxed and strained Si MOSFETs.

capacitance changes mostly due to variation in inversion capacitance. Fig. 3.8 shows inversion charge distribution ρ_{inv} inside Si for relaxed and strained Si device at V_g = 1.4 V. Here z=0 is metal oxide interface. Strain causes ρ_{inv} to increase. Fig. 3.9 shows z_{avg} vs. gate voltage curve for relaxed and strained Si devices. z_{avg} is the average distance of the inversion charge density from oxide-semiconductor interface. Decrease in z_{avg} indicates increase in C_{inv}.

Now we find the reason for charge distribution change due to uniaxial strain application. Uniaxial strain causes both the energy band level and the effective mass to change. Both of these parameters make C-V characteristics to vary with strain. Fig. 3.10 shows two C-V characteristics compared with relaxed C-V. One is simulated with no effective mass correction and another one with both band level and effective mass correction. It is seen that band level plays a small role in C-V change due to strain. Effective mass plays a vital role. As can be seen from the theory section energy profiles are changed by small amounts for strain application. On the other hand effective masses change strongly with strain. Two effective masses are used in a Self-consistent simulator.

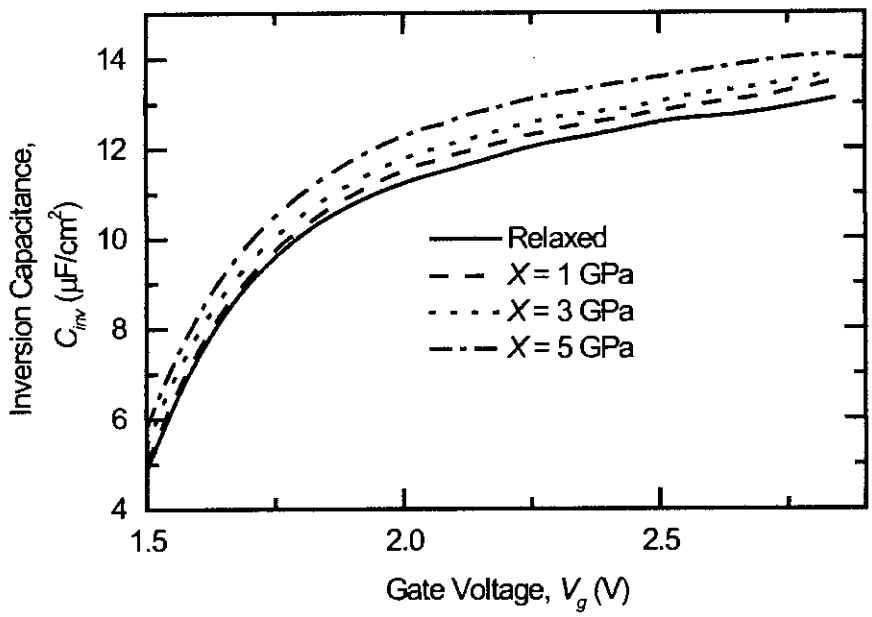

Fig. 3.7: Inversion capacitance of relaxed and strained Si MOSFETs.

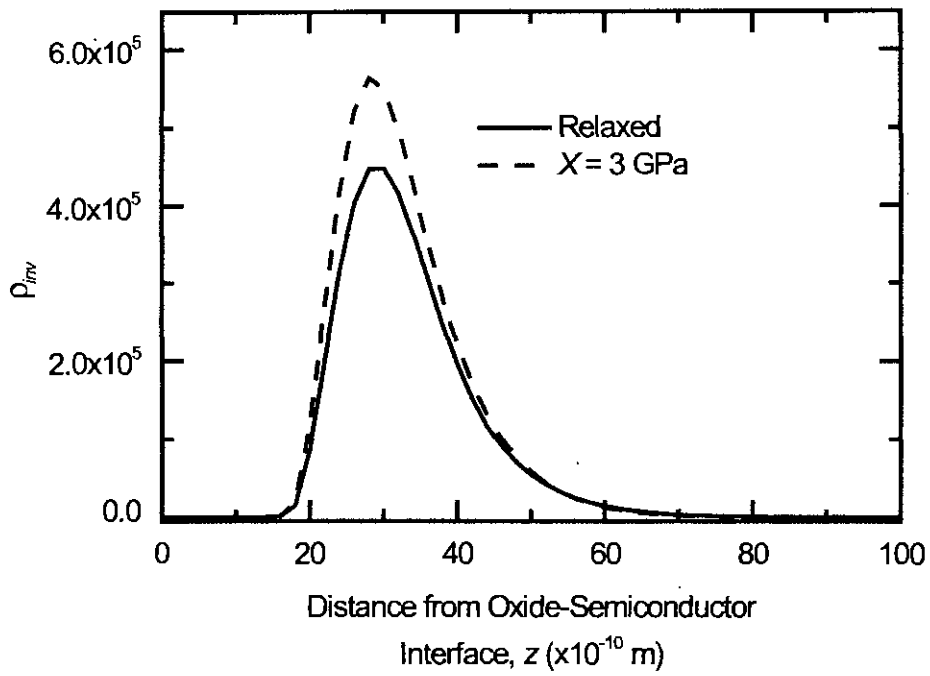

Fig. 3.8: Inversion charge distribution of relaxed and strained Si MOSFETs at V_g = 1.4 V.

Quantization effective masses are used to find the eigenenergies and density of states effective masses to find inversion charges in different energy levels. Increase in quantization effective mass lowers the eigenenergy values making

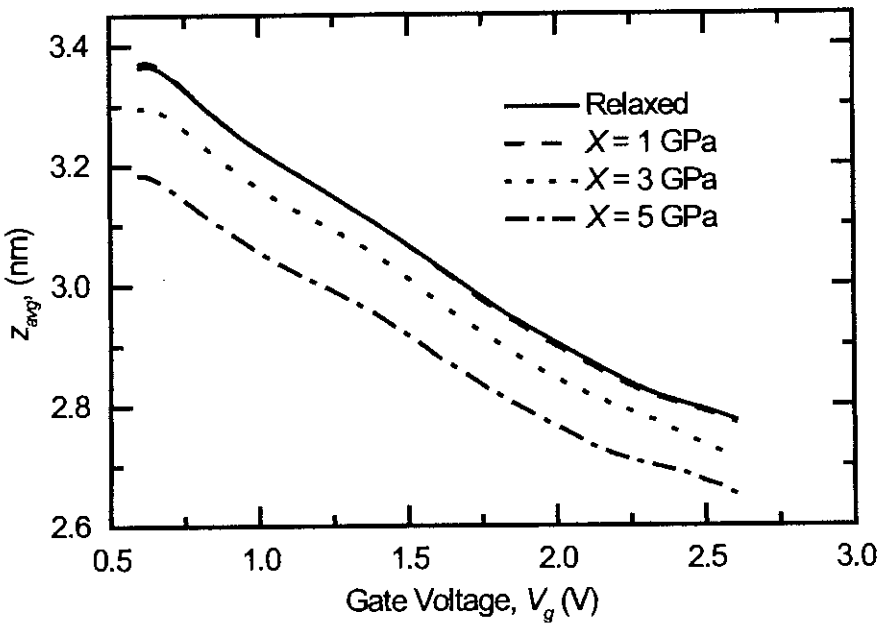

Fig. 3.9: z_{avg} of relaxed and strained Si MOSFETs.

the differences between eigenenergies and Fermi level decrease. This makes total inversion charge to increase. Inversion charges for different energy levels are directly proportional to the density of states effective masses. So change in density of states effective masses make total inversion charges to increase and as a result total charges to increase. Gate capacitance value is increased due to both the effective masses' change with uniaxial strain application for nMOS inversion region.

Another set of simulations with $N_a = 5 \times 10^{17} cm^{-3}$ is carried out. C-V characteristics and change in C-V for strained devices are shown in Fig. 3.11 and Fig. 3.12. It is seen that error levels are about same as that for $N_a = 10^{18} cm^{-3}$. This suggests that change in doping density does not make any significant variation over the strain effect of C-V characteristics.

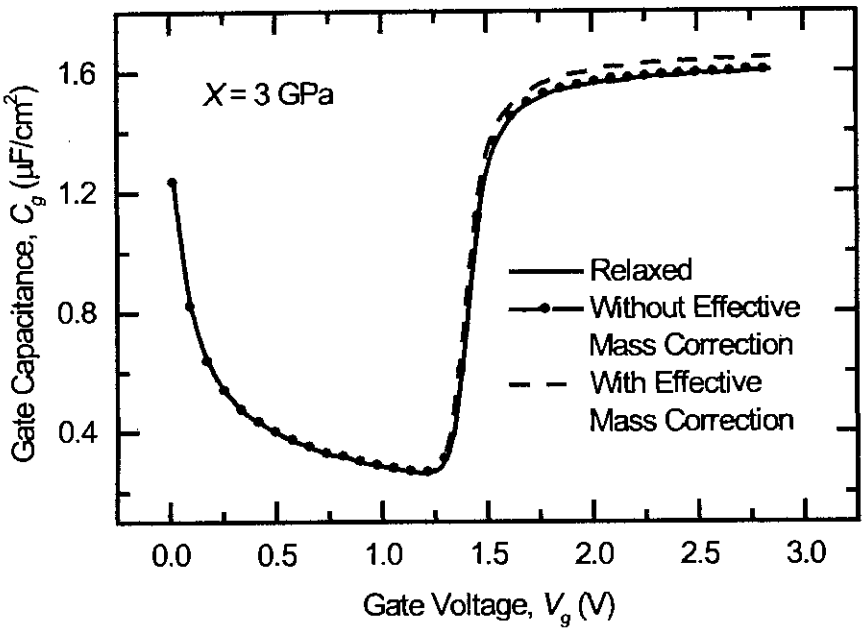

Fig. 3.10: Change in C-V with and without effective mass correction.

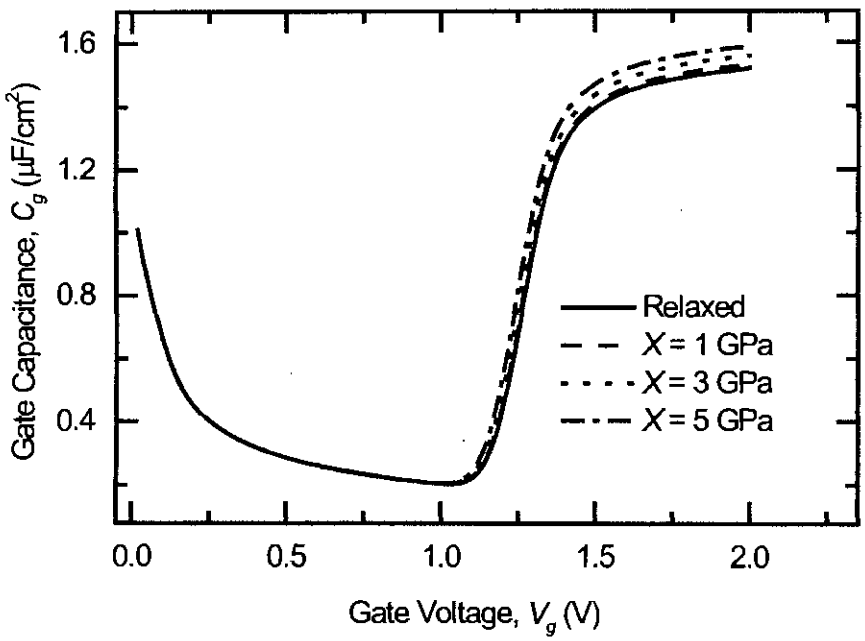

Fig. 3.11: Gate capacitance vs. gate voltage for relaxed and strained Si MOSFETs with $N_a = 5 \times 10^{17} cm^{-3}$.

3.2 Accumulation Capacitance Change Due to Uniaxial Strain

Change in accumulation C-V characteristics under compressive stress for doping density $N_d = 5 \times 10^{17} cm^{-3}$ is shown in Fig. 3.13. Here oxide thickness

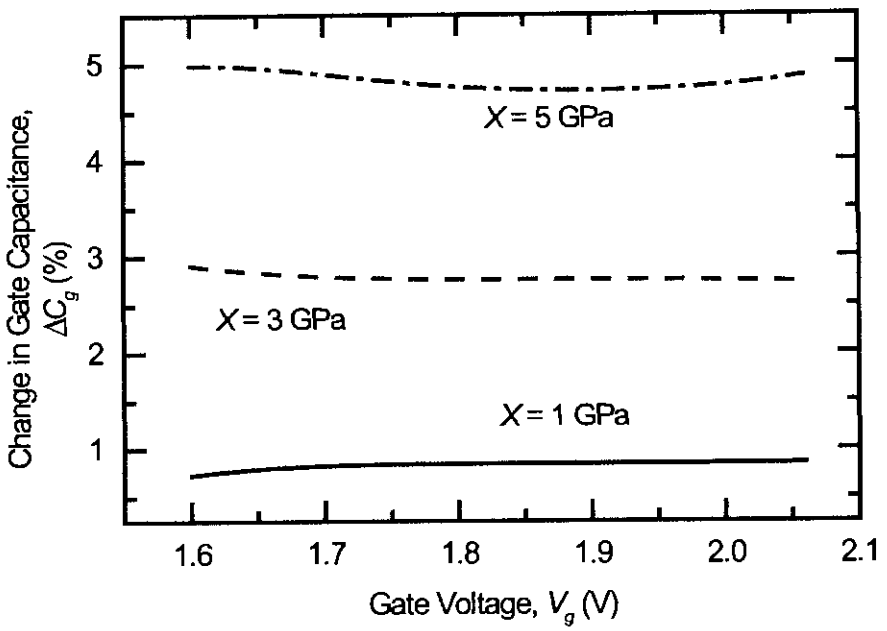

Fig. 3.12: Change in gate capacitance of strained Si MOSFETs with respect to relaxed Si MOSFET.

is 2 nm, oxide material is SiO_2. Clearly insignificant amount of change in capacitance value is observed for high gate bias. The percentage change is less in accumulation than in inversion region. Two different compressive stress levels are shown and it is observed that change in C-V increases with applied strain as in Fig. 3.14. Though comparatively high amount of change is seen in low gate bias region, this is not a considerable factor for this work. Conventionally MOS devices are not operated in low bias regions. And the observed change is due to numerical limitation of our simulator for high doping densities which is not seen for lower doping densities or higher gate biases. Physical explanation of capacitance value change in high bias region is explained below.

In accumulation region total charge to estimate capacitance is calculated from accumulation charge or bond charge and extended state charge. Though extended state charges exist in inversion, due to the lower position of the Fermi level, it is insignificant. In accumulation Fermi level is very close

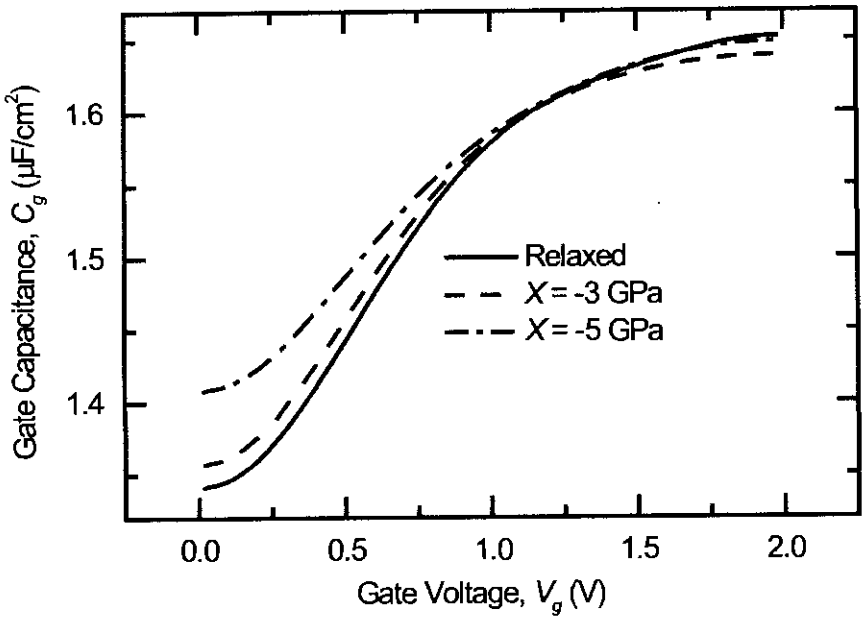

Fig. 3.13: Gate capacitance vs. gate voltage for relaxed and strained Si MOSFETs with $N_d = 5 \times 10^{17} cm^{-3}$.

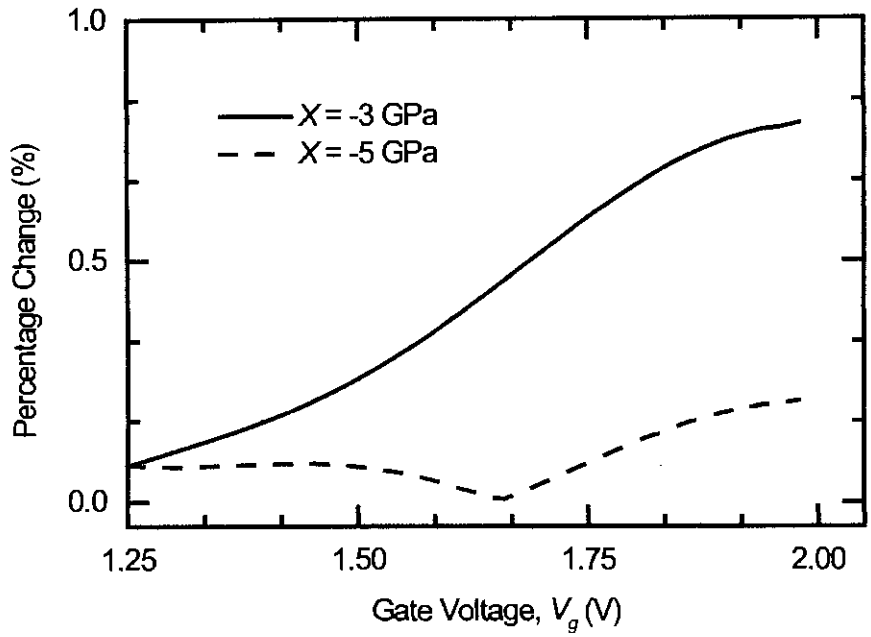

Fig. 3.14: Change in gate capacitance of strained Si devices for accumulation.

to the conduction band and exclusion of extended state charge will lead to underestimation of the total charges. Fig. 3.15 and 3.16 shows variation of two types of charges with uniaxial stress level. It is observed that they show

opposite tendency. Accumulation charges decreases and extended state charges increases with strain. Total charge remains almost the same for all levels of strain. This makes less change in capacitance value.

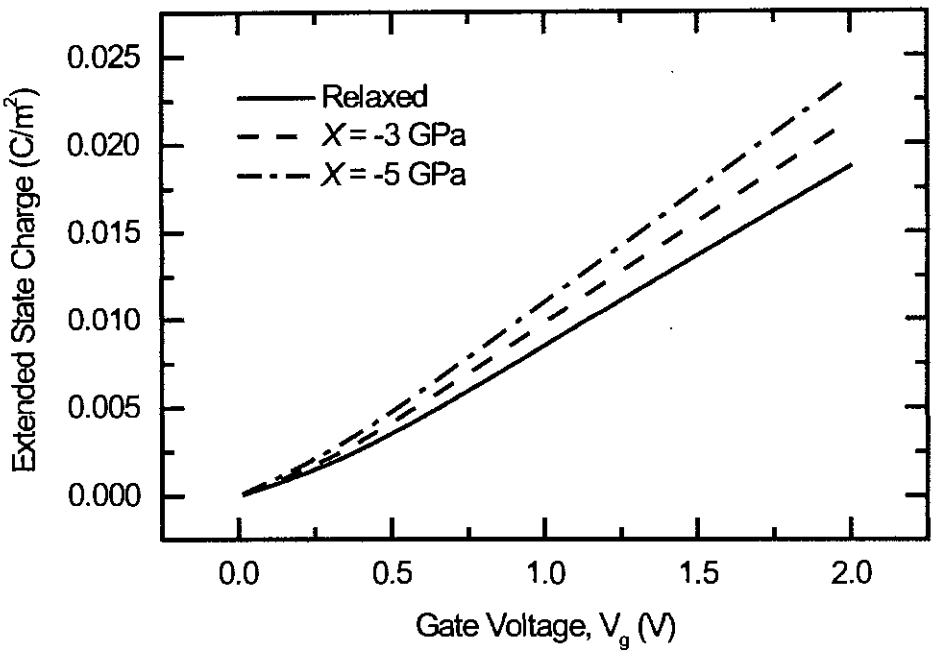

Fig. 3.15: Variation of extended state charge with strain.

Decrease in accumulation charge and increase in extended state charge occurs due to strong dependency of density of states effective masses and quantization effective masses of two conduction band valleys with compressive stress as shown in the theory section. Compressive stress increases density of states effective mass in Δ_2 band and decreases in Δ_4 band. Again Δ_4 band comes closer to the fermi level for compressive stress application. These effects increases the extended state charge for Δ_4 band and it dominates over Δ_2 band extended state charge. So total extended state charge increases. Again quantization effective mass is decreased for Δ_4 band while is increased for Δ_2 band. As increase in quantization effective mass means more eigenenergies in a quantum well, accumulation charges is to be increased. But decrease in density of states effective mass means less accumulation charges and density of states

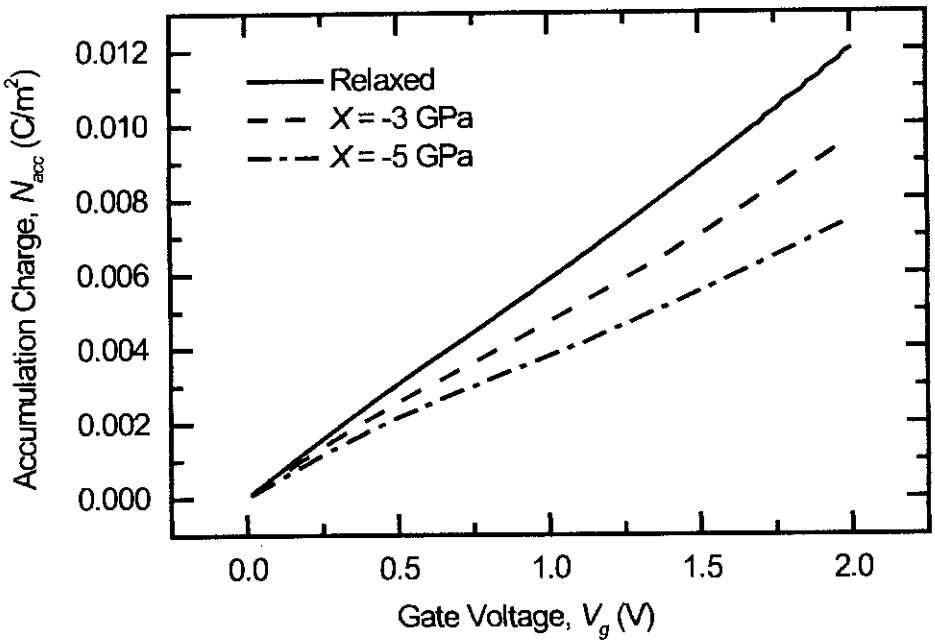

Fig. 3.16: Variation of accumulation charge with strain.

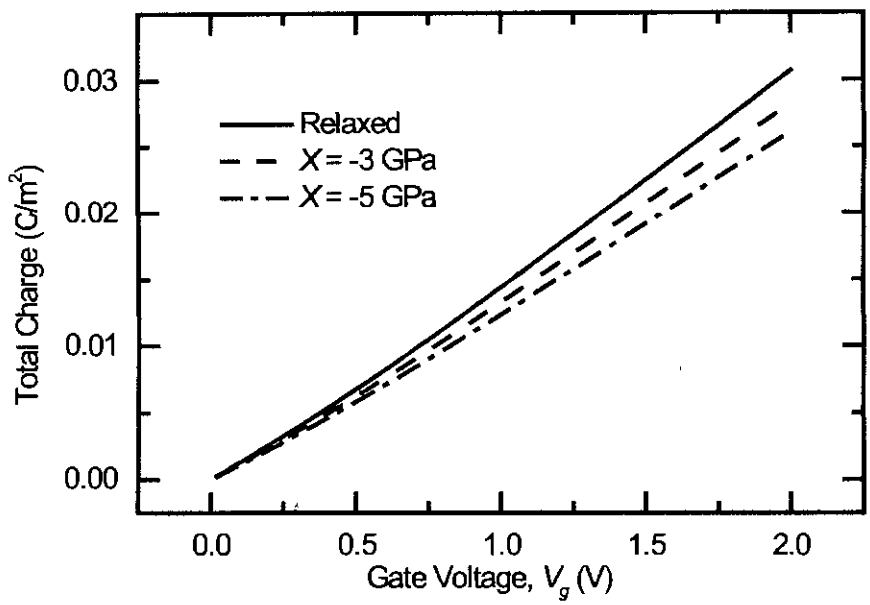

Fig. 3.17: Variation of total charge with strain.

effective masses show different direction of change with the compressive stress compared to quantization effective mass change. Due to two counter effects total accumulation charge decreases. Fig. 3.18 shows accumulation charge and

extended state charge distribution for $V_g = 0.1$ V for two levels of strain. It is clear that strain shifts the accumulation charges down but do the reverse for the extended state charge. Fig. 3.17 shows total charge as a function of the gate bias. As total charge is the summation of both the extended state charge and accumulation charge and it remains weakly dependent on strain.

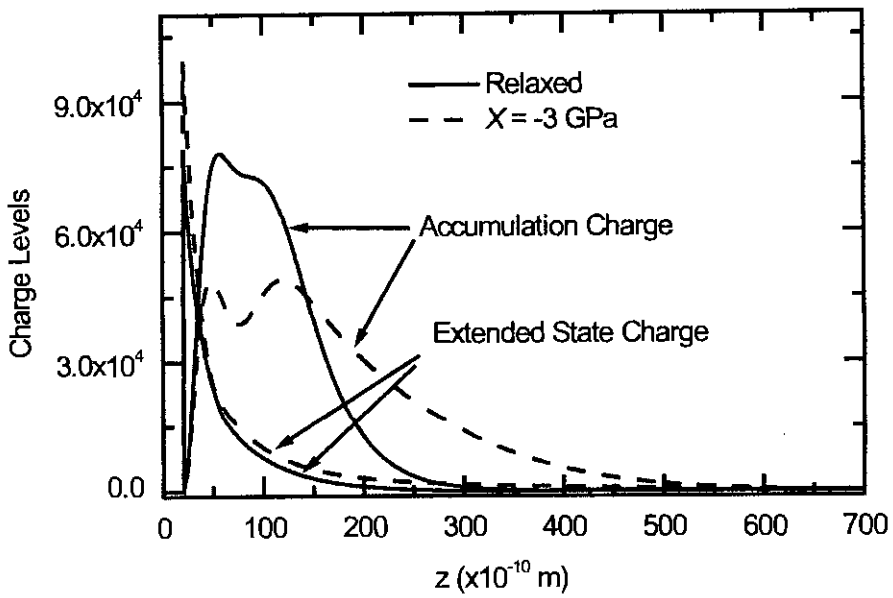

Fig. 3.18: Distribution of extended state and accumulation charges at V_g =0.1 V.

Two oppositely directed charges, extended state charge and accumulation charge make total capacitance in accumulation to be independent of strain. From the previous results it is clear that the strain shifts the inversion capacitance in more proportion than in accumulation.

Accumulation C-V for another doping density $N_d = 5 \times 10^{16} cm^{-3}$ is shown in Fig. 3.19. Again no significant amount of change in capacitance value due to strain is observed. Extended state charge and accumulation charge per m^2 is shown in Fig. 3.20. Extended state charges are increasing with strain. Fig. 3.21 shows accumulation charges are decreasing with strain. As the total charge is the summation of these two charges, it remains nearly same for all values

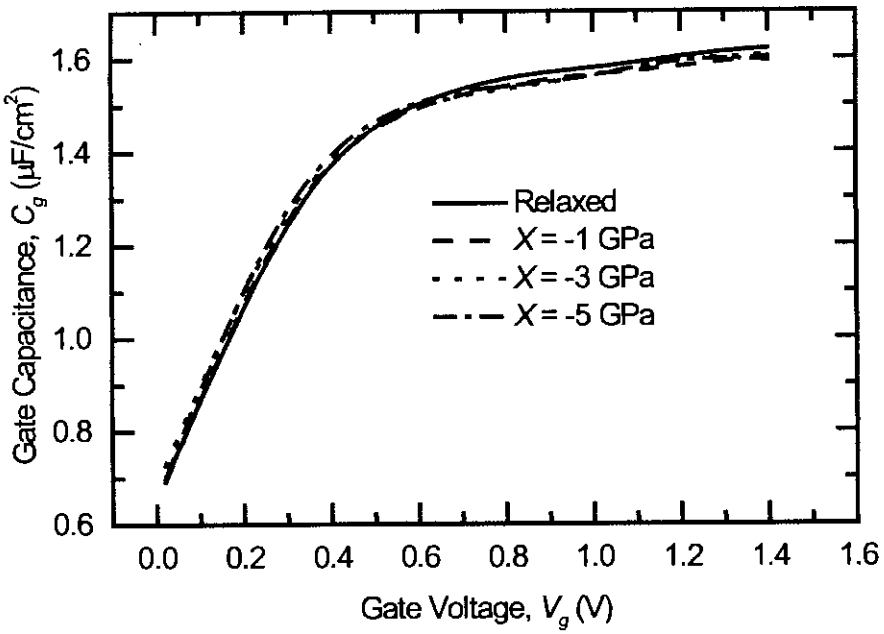

Fig. 3.19: Gate capacitance vs. gate voltage for relaxed and strained Si MOSFETs with $N_d = 5 \times 10^{16} cm^{-3}$.

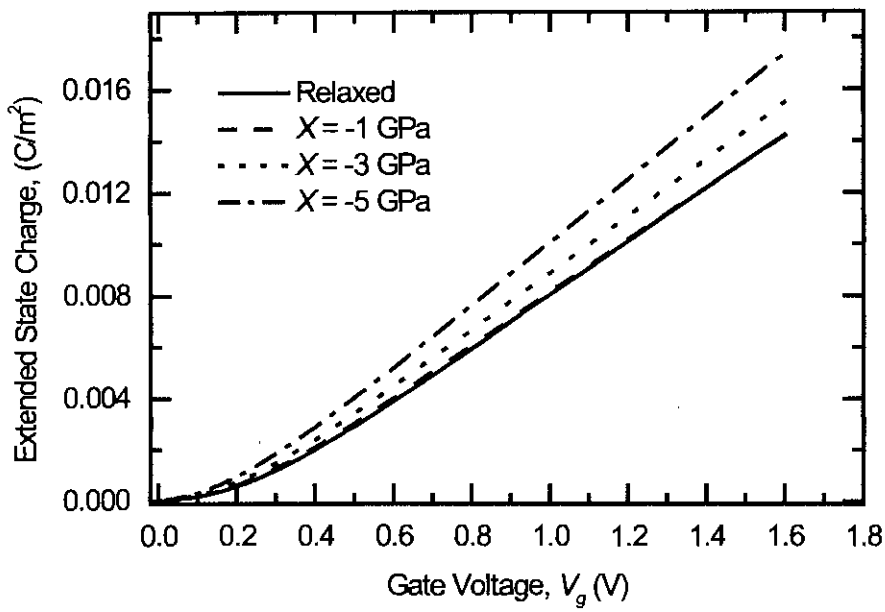

Fig. 3.20: Variation of extended state charge with strain.

of strain. This makes capacitance value to change in insignificant proportion due to strain application. Fig. 3.22 shows total charge for three different stress levels. Total accumulation charge and extended state charge are obtained by

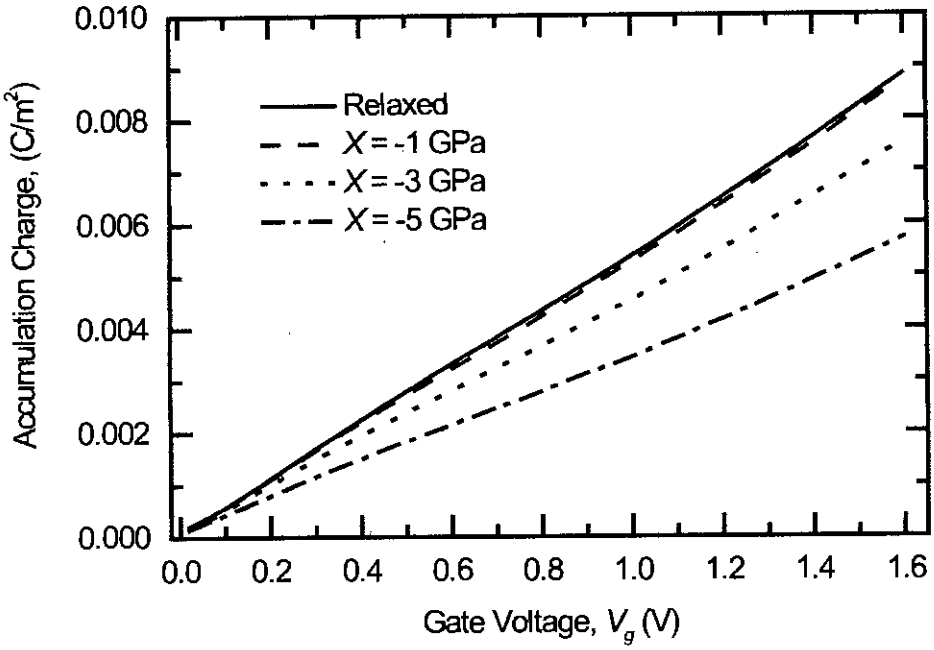

Fig. 3.21: Variation of accumulation charge with strain.

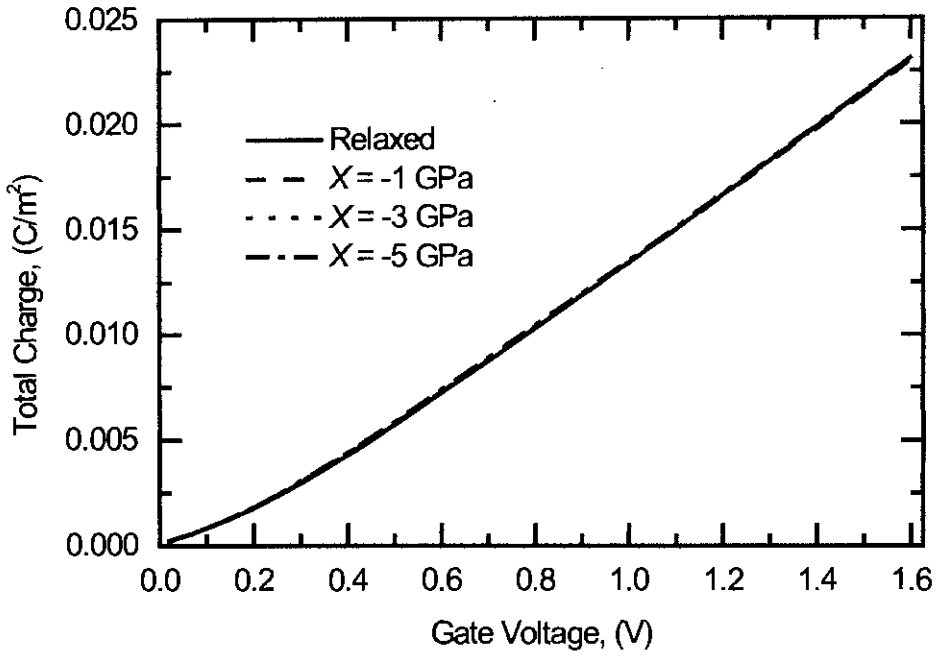

Fig. 3.22: Variation of total charge with strain.

integrating the area of the distribution. Here results are quite similar as the previous doping density. Doping density variation does not introduce any

change in the trend of C-V for strained MOS devices in accumulation region. This is similar to our conclusion for inversion region.

Chapter 4

Conclusion

4.1 Summary

An accurate self consistent model is developed to simulate C-V characteristics for uniaxilly strained MOS devices incorporating wave function penetration and necessary band splitting and effective mass change. C-V characteristics are simulated for inversion and accumulation regions. The results are compared with relaxed C-V and percentage changes of C-Vs of strained devices with relaxed device are given.

Uniaxial straining technique is recently been introduced to enhance mobility of the carriers in more extent than other conventional techniques. C-V modeling of uniaxial devices is necessary for parameter extraction. Accurate modeling of C-V is possible with the given simulator for any stress level up to 5 GPa, practical limit for uniaxial stress. A detail physical insight is given regarding the change of C-V due to strain. It has been seen that strain causes inversion region capacitance to change and depletion region capacitance remains unaltered. Strain causes no change in depletion width or depletion band bending. But significant amount of change is seen in the inversion charges. This causes C-V to change in more percentage in inversion region. It is observed that effective mass change plays the main role in C-V change in inversion region. Doping density variation does not affect the variation of C-V due to uniaxial strain application. On the other hand accumulation C-V is less changed by uniaxial

strain than inversion C-V. Variation of extended state charge and accumulation charge in different directions is found to be responsible for this. Extended state charges are increased while accumulation charges are decreased with uniaxial strain. These changes make total charge to be independent of strain. Thus capacitance values are also independent of strain. Doping density change does not play any role to affect the variation of C-V change with uniaxial strain.

4.2 Suggestion for Future Works

In this work only inversion and accumulation C-Vs for electrons are discussed. Similarly C-Vs for holes can also be simulated. For Si valence band structure is more complex than the conduction band. But accurate determination of band splitting and effective mass change for heavy hole, light hole and split-off hole can lead to simulation of hole C-Vs for different strain values.

Other than single gate MOS devices, that is used in this work, double gate MOS devices are also emerging for integrated chips. This simulator can be extended to double gate MOS devices, to simulate gate C-V characteristics due to uniaxial strain application. On the other hand drain current is another important characteristics for MOS devices. This one dimensional simulator can be extended to two dimensional one to calculate drain current for different strain conditions.

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Appendix A

Flow Chart for Self-Consistent Simulator

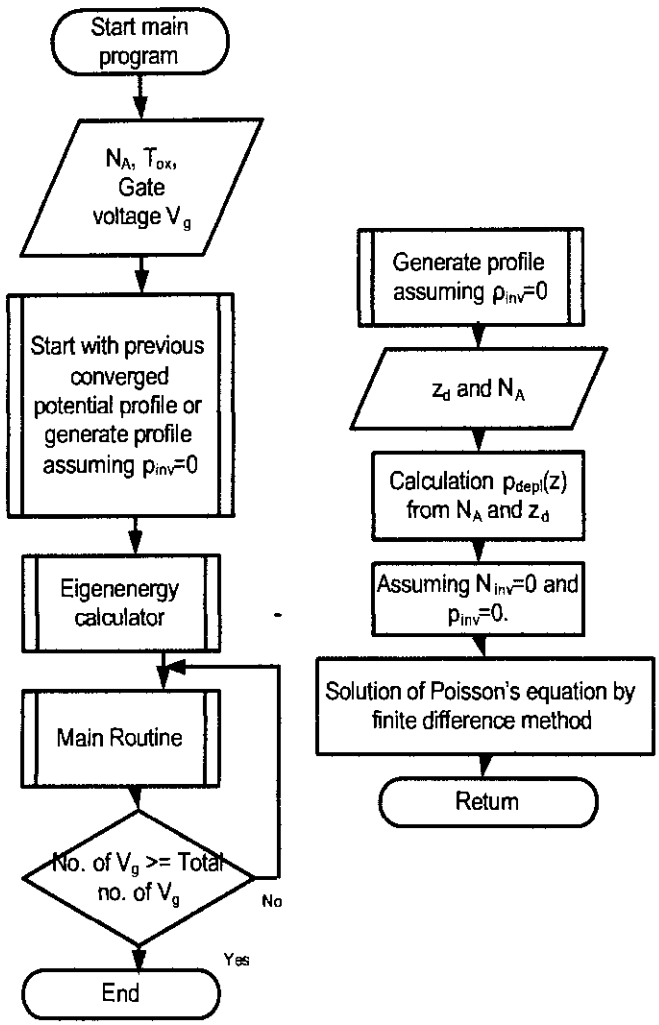

Fig. A.1: Flowchart.

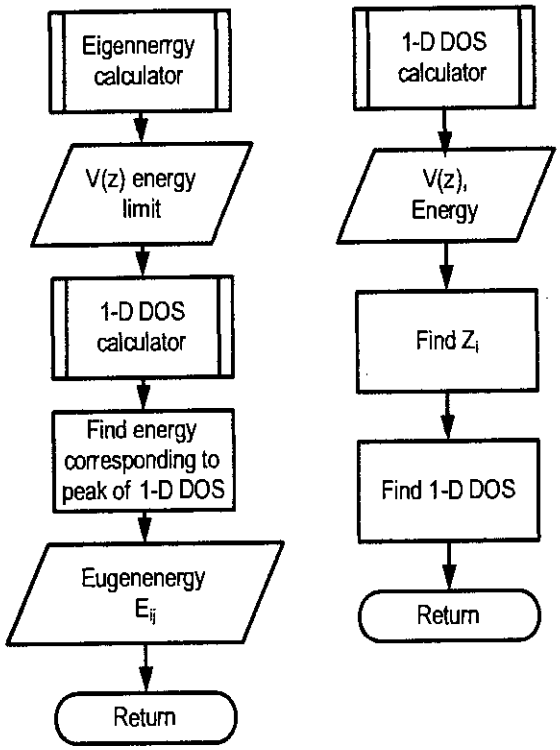

Fig. A.2: Flowchart.

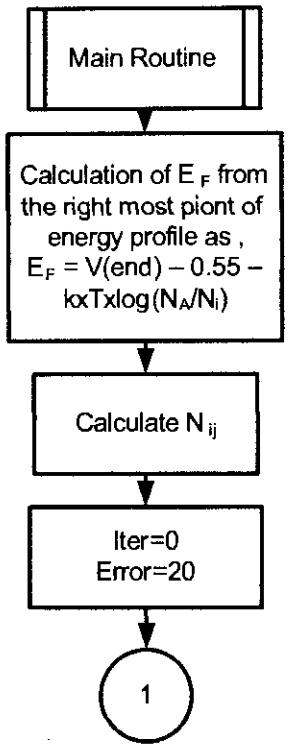

Fig. A.3: Flowchart.

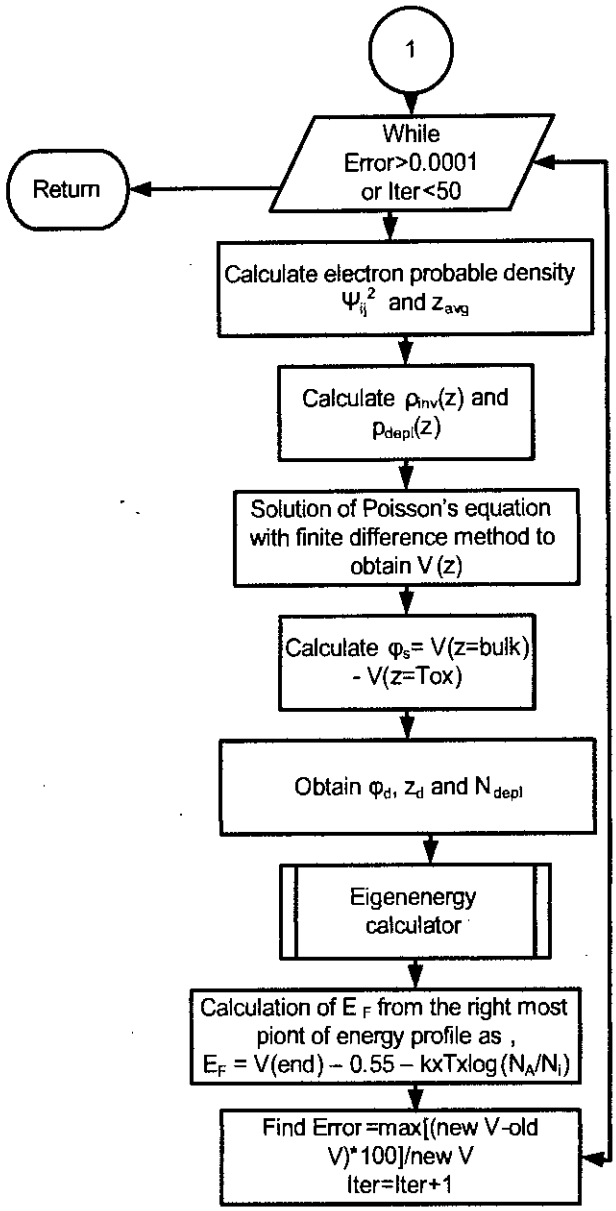

Fig. A.4: Flowchart.