DESIGN AND ANALYSIS OF A RF FRONT END LOW NOISE AMPLIFIER BASED ON IBM 0.13μm CMOS TECHNOLOGY

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MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

By,

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BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY

August’ 2014
DECLARATION

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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(Md. Sariful Islam)
APPROVAL CERTIFICATE

The thesis titled “DESIGN AND ANALYSIS OF A RF FRONT END LOW NOISE AMPLIFIER BASED ON IBM 0.13µm CMOS TECHNOLOGY” submitted by Md. Sariful Islam, Student ID: 0412062217, Session: April 2012 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on 13th August, 2014.

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<th>Description</th>
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<tr>
<td>CMOS</td>
<td>Complimentary Metal Oxide Semiconductor</td>
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<tr>
<td>UWB</td>
<td>Ultra Wide Band</td>
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<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>MMIC</td>
<td>Monolithic Microwave Integrated Circuit</td>
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<td>NF</td>
<td>Noise Figure</td>
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<td>ICP</td>
<td>Input Compression Point</td>
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<td>IIP3</td>
<td>Input Referred Third Order Intercept</td>
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<td>IIP2</td>
<td>Input Referred Second Order Intercept</td>
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<td>S-parameter</td>
<td>Scattering Parameter</td>
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<tr>
<td>IBM</td>
<td>International Business Machines Inc.</td>
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<tr>
<td>VSWR</td>
<td>Voltage Standing Wave Ratio</td>
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<td>GP</td>
<td>Average Power Gain</td>
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<tr>
<td>GT</td>
<td>Transducer Power Gain</td>
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<tr>
<td>GA</td>
<td>Available Power Gain</td>
</tr>
<tr>
<td>VGA</td>
<td>Variable Gain Amplifier</td>
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<tr>
<td>SiGe</td>
<td>Silicon Germanium</td>
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<tr>
<td>CNM</td>
<td>Classical Noise Matching</td>
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<tr>
<td>SNIM</td>
<td>Simultaneous Noise and Input Matching</td>
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<td>PCNO</td>
<td>Power Constrained Noise Optimization</td>
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ABSTRACT

Design and analysis of a RF front end low noise amplifier (LNA) is presented here. The RF front end LNA is designed for 15-22GHz of K-band and Ku-band. The designed LNA can be used for short distance communication like on-chip wireless communication as well as in data communication. The proposed circuit of LNA uses CS-CG topology with a three sections chebyshev filter at input, a coupling inductor in between diode connected MOS and main MOS and an inductive load at output. The proposed architecture uses inductively source degenerated topology and is designed in IBM 0.13Î¼m CMOS process. The simulation is done both in Hspice RF and Cadence Spectre. Response of the input network is observed from Hspice and parameters values are selected. Coupling inductor is used to compensate the effect of the parasitic capacitances (gate-drain capacitance of main MOS, gate-source capacitance of diode connected MOS) and finally to increase the bandwidth. The proposed design shows a forward gain of 10.14dB at center frequency 17.56GHz with a -3dB bandwidth of 6.2GHz. The input and output reflection co-efficient are below -10dB within the band of interest. The output matching parameter is -25dB at center frequency. The circuit shows average noise figure of 3.74dB. Linearity of the circuit is also simulated and IIP3 and 1-dB compression point found -5dBm and -9.38dBm respectively. All the transistors are biased within the circuit and by the same supply source. The overall power consumption including bias circuit is 10.91mW when powered up by a 1.2V source.
CHAPTER ONE

INTRODUCTION

Communication technology is moving toward a major milestone. The explosive growth of the wireless industry, global access to the internet, and the ever increasing demand for high speed data communication are spurring us toward rapid developments in communication technology.

Wireless communication plays an essential role in this transformation to the next generation of communication systems. Cellular phones, pagers, wireless local area networks (WLAN), global positioning system (GPS) handhelds, and short-range data communication devices employing Bluetooth and ultra-wideband (UWB) technologies are all examples of portable wireless communication devices. Nowadays, driven by the insatiable commercial demand for low-cost and low-power multi-standard portable devices, RF designers are urged to develop new methodologies that allow the design of such products. These all devices are operated below 5GHz frequency.

While 3-10GHz frequency band is mostly explored by the researcher for Ultra-Wide-Band communication, Ku-band and K-band are not explored that much. The rapid development of wireless communication systems in recent years, various wireless communication products have been integrated into the life and become a common electronic product, and K-band and Ku-band application (15-22GHz) is more and more extensive. These bands have many applications like the NHK television is expected to use 21GHz band satellite broadcast transmission in order to offer the higher quality factor for Super Hi-Vision TV service than Hi-definite TV (HDTV) in 2025 [1] and Taiwan NCC is planning to use 21GHz for Hi-definite satellite broadcasting [2]. Ku-band is widely used in traditional geosynchronous earth orbit (GEO) and video broadcasting systems for telephone communications and analog television distribution. 15GHz-18GHz band of Ku-band is used for Radio astronomy, Aeronautical, fixed satellite and Mobile Communication. On the other hand, the delay due to the parasitic effect of the interconnecting wires limits the intra-chip and inter-chip communication speed of modern CMOS ICs [3-4]. On chip wireless interconnections with integrated antenna might be one of the approaches to overcome this limitation [5]. High frequency UWB communication would be a
wise choice in this respect because it provides benefits like multiple access capabilities, high data transmission rate, reduced antenna size, low power consumption and reduced interference [5].

Ultra wideband (UWB) systems are a new wireless technology capable of transmitting data over a wide spectrum of frequency bands. The benefits that UWB technology can provide, includes low power, high data rate, low cost, and reduced interference, all of which are crucial for applications such as wireless video conferencing, wireless projector, and multimedia content downloading [6]. To support the high end of the data rates, the radio frontend must be able to provide a simple and cost effective solution to cover a wide bandwidth. Uniform performance specifications must be satisfied across a large bandwidth. Due to many possible mobile UWB applications, low power consumption is also highly desirable. The amplifier must meet several stringent requirements, such as broad-band input matching to minimize the return loss, sufficient gain to suppress the noise of a mixer, low noise figure (NF) to enhance receiver sensitivity, low power consumption to increase battery life, and small die area to reduce the cost.

A UWB receiver, diagrammed in Fig. 1 will feature a low-noise amplifier (LNA) followed by a correlator that removes the carrier (or the pseudo-carrier) from the received radio frequency (RF) signal. Analog-to-digital conversion will then allow for digital signal processing aimed at recovering the information data. In this context, it is clear that, regardless of what the future standard will be, a wideband LNA operating over the entire band of operation is required.

![Fig. 1.1 Block diagram of a UWB receiver. The dashed box represents the subsystem that brings the RF signal to baseband in order to recover the information signal [6]](image)

Most of the designs of LNA in recent times are based on SiGe technology and Monolithic Microwave Integrated Circuit (MMIC) process because of restriction of high frequency
application of standard CMOS technology due to various reasons. One of the reasons is poor quality of on-chip passive element. But proper designing of these elements can help to overcome this problem and thus enabling the application of LNA for high frequency in standard CMOS process.

Recently, there has been a tremendous effort to develop wireless devices that integrate multiple applications (phone, video-game console, navigator, digital camera, web browser, etc.) on a single chip. The growing number of these wireless communication standards promotes the need for a multi-standard transceiver. The RF front-end of such a receiver has to cover a wide range of different carrier frequencies. To achieve this goal, wideband performance of the receiver front-end is desired. A variety of architectures have been proposed to fulfill this requirement. One approach is to use a parallel combination of several tuned narrowband LNAs. This solution, although straightforward, is power hungry and area inefficient. Therefore, it is not particularly suitable for low-cost portable systems. Two other LNA architectures that can be used for multi-standard signal reception are concurrent LNA [7] and tuneable LNA [8]. The former technique is applicable when the frequency bands of desired standards are well separated, while the latter design approach is complicated if a wideband tuning-range is desired [9]. An alternative solution is to design a single wideband LNA covering the entire band of interest, which is the subject of this research.

Currently, most commercial RF transceivers are implemented as multi-chip modules (MCMs) or system in packages (SiPs), using various technologies [10]. Base-band and mixed-signal components (e.g., DAC, ADC, and DSP) are mainly implemented in complementary metal-oxide semiconductor (CMOS) technology, while RF and analog sections are typically implemented in silicon-germanium (SiGe) or gallium-arsenide (GaAs) technologies. High quality passive filters are mostly realized as discrete components. MCM and SiP approaches suffer from many shortcomings, such as large size, high power consumption, and high integration cost. The aforementioned problems account for the global trend toward a single technology that can support a commercially viable single chip RF transceiver.

Historically, CMOS technology was not considered a good candidate for analog and RF applications. Relatively small transconductance, low drive capability, and poor quality of on-chip passive elements are among the several limitations of this technology. However, the incredible
growth of the digital industry due to the continuous scaling in CMOS technology has motivated designers to develop analog and RF CMOS circuits that can be integrated along with the digital circuitry. This has led to the tremendous research and development in implementing single chip systems. Furthermore, the transit frequency ($f_t$) of MOS devices has recently increased due to the evolution of CMOS into deep-sub-micron (DSM) technologies ($f_t$’s exceeding 100GHz have been recently reported [11]). This greatly improves the performance of integrated RF CMOS circuits.

To summarize, despite the inferior performance of RF CMOS circuits compared to their SiGe and GaAs counterparts, the dominance of CMOS in the digital world, combined with the feasibility of integrating digital/RF/analog circuits on a single chip and the potential cost and power advantage of this integration, provide reasonable motives to adopt CMOS over other technologies.

1.1 **Objectives of This Work**

The objective of this work is to design an UWB Low Noise Amplifier (LNA) for Ku-band and K-band application using IBM 0.13µm. In order to accomplish this task, an inductively degenerated LNA architecture will be used with a three section chebyshev filter at input section. The effect of coupling inductor in between main MOS and cascode MOS is observed. After analyzing the circuit fully, this design will be simulated in Hspice RF using model files of IBM 0.13µm. After that the circuit will be simulated in Cadence spectre.

The objectives of this work are:

i) To design a Low Noise Amplifier (LNA) to cover a 15-22GHz band using IBM 0.130µm CMOS technology.

ii) To design the UWB LNA using HSpice RF software and investigate the effect of different circuit parameters on the performance of UWB LNA.

iii) To study, investigate and improve the performance parameters of UWB LNA.
iv) To design this UWB LNA using Cadence Virtuoso Simulation Tool and investigate the effect of parasitic capacitance on performance of the UWB LNA.

Possible outcome of this work results an UWB Low Noise Amplifier which can be used in RF receiver for several applications such as Mobile, Satellite, Inter satellite, Space communication, on chip wireless interconnect communication on a single chip.

1.2 THESIS OUTLINE

The thesis is organized as follows-

Chapter One introduces the topic of the thesis. The motivation behind this thesis work is written in this chapter. An outline of the specific objectives of the project is also included.

Chapter Two presents the theoretical aspects of microwave communication which are relevant to the UWB communication scheme. The parameters which need to know to understand the basic of a LNA and on which the performance of the LNA depends are explained. The design parameters that are considered as figures of merit of wireless receivers are defined and their influence on the performance of the UWB system is illustrated.

Chapter Three illustrates the existing topologies with relative advantages and disadvantages. This chapter explains the architecture of the proposed LNA. Circuit level analysis of the amplifier also presented. Input matching, output matching, noise analysis, voltage gain are analyzed in this chapter.

Chapter Four presents the simulated performance of the proposed amplifier, the summary of the amplifier and comparison of performance with other published LNA.

Chapter Five provides the design insight for considering the fabrication of the proposed design in IBM 130nm CMOS RF technology.

Chapter Six briefly summarize the overall research work and the suggestion of future work.
CHAPTER TWO

BACKGROUND

In a receiver chain, LNA is usually the first active signal-processing block after the antenna. The amplitude of the received signal at the input of LNA may vary from few nV (less than -130dBm for GPS signals) to tens of mV (e.g., large interferers accompanying the signal). The LNA should be capable of amplifying all these signals without causing any significant distortion. Furthermore, the sensitivity of LNA determines the sensitivity of the overall receiver. This requires that very little noise from the LNA be introduced to the entire receiver [12]. Another major requirement of the LNA is to provide a large gain to suppress the noise of subsequent blocks.

LNAs are usually preceded and followed by passive filters for out-of-band rejections and channel selection. The transfer function of such filters is usually a function of their termination impedance. This imposes the requirement of certain input and output impedances, such as 50Ω, on the LNA. On the other hand, as will be shown in the following sections, the amount of noise introduced by the LNA is also a function of source impedance. The optimum source impedance, which results in the minimum noise figure of the LNA, may not be equal to that required by the preceding stage, e.g., 50Ω. This may result in an LNA having a good input matching and a poor noise figure or vice versa. The design of an LNA satisfying all these requirements in a wide bandwidth is even more challenging and needs a careful study of the different parameters affecting noise, gain, and linearity. To achieve this goal one needs to develop an accurate mathematical model for the LNA and find the analytical expressions for noise, gain, and linearity.

2.1 NOISE

In communication systems, any signal other than the desired signal is called noise and will reduce the sensitivity of the overall system. Different sources of noise with different noise generation mechanisms exist. The dominant sources of noise in integrated circuits are shot noise, flicker noise, and thermal noise. Shot noise is mainly caused by the hopping of electric charges
over a potential barrier and is specific to nonlinear devices such as diodes and transistors. In MOS devices, which are the subject of this work, the only source of shot noise is the DC gate leakage current, and hence it is not considered a major problem [12]. This is in contrast to bipolar transistors in which base and collector shot noise may significantly degrade the performance of the overall receiver.

2.1.1 Flicker Noise

Flicker noise, also known as pink noise, occurs due to the trapping of charges in the defects and impurities of the channel region in MOS devices [12]. As a general rule, larger MOS devices experience less flicker noise. The spectral density of this noise is given by:

\[ \frac{I_{fn}}{f} = \frac{K_{g_m}^2}{fWL\varepsilon_{ox}} \]

where \( K \) is a device-specific constant, \( g_m \) is the transconductance of the MOS device, \( f \) is the operating frequency, \( \varepsilon_{ox} \) is the gate-oxide capacitance per unit area, and \( W \) and \( L \) are the width and length of the MOS device, respectively.

As can be seen from spectral density equation, the amount of flicker noise is inversely proportional to the frequency of operation. Therefore, flicker noise can be a dominant noise source at very low frequencies. In LNAs where the frequency of the received signal is about several GHz, flicker noise does not play an important role and is usually ignored. It is worth mentioning that in other receiver stages such as mixers or voltage controlled oscillators (VCO), flicker noise can be a major problem.

2.1.2 Thermal Noise

Thermal noise is the noise caused by the agitation of carriers in a conductor, and its spectrum density is given by the following quantity known as available noise power [12].

\[ P_N = K T A f \]
where \( k \) is the Boltzman constant \((\approx 1.38 \times 10^{23} \text{ J/K})\), \( T \) is the absolute temperature in Kelvins, and \( \Delta f \) is the bandwidth of the noise measured in Hz. The value of this quantity for 1Hz of noise bandwidth at room temperature (290K) is \(-174\text{dBm}\) and is often called the noise floor of the system. The noise floor is an important quantity in determining the sensitivity of the receiver [13]. The available noise power is the maximum power delivered to a load from a noise source.

On the basis of this definition, the thermal noise of each passive or active element can be modeled with an equivalent voltage or current noise source.

Therefore, the mean square noise voltage over a noisy resistor is \( 4kT\Delta f \). As a reference point, the rms voltage noise of a 50Ω resistor is equal to 1nV/ Hz.

### 2.2 Noise Sources in a MOS Transistor

MOS devices act like a trans-conductance in the saturation region, and like a resistance in the triode region. So, one should expect a thermal noise associated with the carriers in the channel similar to the noise of carriers in a conductor. In [14] Van der Ziel has derived the expression for the drain current noise of MOS devices, also known as channel thermal noise [14]:

\[
\bar{i}_{nd}^2 = 4kT\gamma g_{d0} \Delta f
\]

Where \( g_{d0} \) is the drain conductance for zero drain-source voltage and \( \gamma \) is a technology-dependent parameter and has a value of around 2/3 for long-channel devices in saturation (in short channel devices \( \gamma \) is larger and its value is between 2 and 3) [15].

A careful examination of noise characteristics in a MOS device reveals that channel thermal noise does not fully take into account all the noise associated with a MOS device [16]. The extra noise can be modeled by introducing a frequency-dependent gate conductance [12]:

\[
g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}
\]
and an equivalent gate current noise of [12]:

\[ \overline{i}_{ng}^2 = 4KT\delta_{g}g\Delta f \]

where \( \delta \) is the gate noise coefficient and is also a technology-dependent parameter. Its value is 4/3 for long channel devices and is augmented by a factor of 2 in short channel devices. Note that the gate current noise is partially correlated with the channel thermal noise.

\[ c = \frac{i_{nd}i_{ng}}{\sqrt{i_{nd}^{2}i_{ng}^{2}}} \]

where \( c \) is a complex number and its value is theoretically computed to be around \(-0.395j\) for long channel devices [3]. This value is higher for short channel MOS and an experimental value of \(-0.5j\) is usually assumed for noise calculations. The exact value of \( \gamma \) and \( \delta \) depends on the technology and, unless provided by the foundry, is cumbersome to measure. However, it can be shown that the noise behavior of an LNA depends on the ratio of these two numbers and not their exact value. Fortunately, this ratio is almost a constant (\( \delta/\gamma \approx 2 \)) regardless of whether we use long channel or short channel devices. Hence, one can determine the characteristics of an LNA without knowing the exact values of these parameters.

### 2.3 Noise Figure

Noise figure (NF) is a measure of signal-to-noise ratio (SNR) degradation as the signal traverses the receiver front-end. Mathematically, NF is defined as the ratio of the input SNR to the output SNR of the system.

\[ NF = \frac{Output\ Noise\ Power}{Output\ Noise\ Power\ due\ to\ source} \]

NF may be defined for each block as well as the entire receiver. NF\textsuperscript{LNA}, for instance, determines the inherent noise of the LNA, which is added to the signal through the amplification process.
With the use of the classical two-port network theory, it can be shown that the NF of a noisy two-port network is given by [12] –

\[
NF = NF_{\text{min}} + \frac{R_n}{G_S} \left[ \left( G_S - G_{\text{opt}} \right)^2 + \left( B_S - B_{\text{opt}} \right)^2 \right]
\]

where \( NF_{\text{min}} \) is the minimum achievable NF, \( B_{\text{opt}} \) and \( G_{\text{opt}} \) are the optimum source susceptance and conductance corresponding to \( NF_{\text{min}} \), and \( R_n \) is an equivalent noise resistance, which quantifies the sensitivity of NF to departure from optimum conditions. Note that NF is a function of source admittance seen from the input terminal of the two-port network. To achieve the \( NF_{\text{min}} \), optimum impedance, namely \( Z_{\text{opt}} \), should be introduced to the network. The expressions for \( NF_{\text{min}} \) and \( Z_{\text{opt}} \) can be derived for a MOS device by considering a two-port network model for the MOS device. In this model the gate-source terminal is the input port and the drain-source terminal is the output port.

### 2.4 Input Impedance Matching

To deliver the maximum power from the antenna to the LNA, matching to the impedance of antenna, e.g., 50Ω, is required at the input port of the LNA. For wideband applications, this impedance matching should be obtained over a wide frequency range at the input port of the LNA and is usually a major challenge considering the noise and power consumption requirements.

To quantify the impedance matching, VSWR (Voltage Standing Wave Ratio) needs to be introduced. VSWR is defined as the ratio of maximum voltage to the minimum voltage of the standing wave. Reflection coefficient is defined as the ratio of the incident voltage to the reflected voltage.

\[
VSWR = \frac{1+|\Gamma|}{1-|\Gamma|}
\]

where \( \Gamma \) is the reflection coefficient and can also be defined as:

\[
\Gamma = \frac{Z - Z_0}{Z + Z_0}
\]
where $Z$ is the input impedance and $Z_0$ is the characteristic impedance which is usually equal to 50Ω. Perfect matching ($Z=Z_0$) results in $\Gamma=0 (\sim \infty \, \text{dB})$ and equivalently VSWR=1. However, for practical purpose VSWR under 2 is sufficient to meet practical purpose. Reflection coefficient is the same as $S_{11}$. To specify practical application, $S_{11}$ has to be less than -10dB.

Several topologies exist for input impedance matching. Fig. 2.1 shows some topologies of input impedance matching.

![Fig. 2.1: Input matching (a) resistive termination (b) $1/g_m$ termination (c) inductive degeneration](image)

Resistive termination uses a resistance between gate to source to match the source impedance. But this topology suffers from relatively high noise figure (NF) due to thermal noise of resistance. This condition becomes worse at high frequency because of parasitic capacitance effect. Another shortcoming of the resistive termination is that the input power is attenuated by
the resistive divider before reaching the MOS device, and this will reduce the maximum power gain.

An alternative approach to achieve input matching is to use the source of a MOS device as the input termination, symbolically depicted in Fig. 2.1 (b). In common-gate architecture, the impedance looking into the source terminal of active device is $1/g_m$. Therefore, proper bias and sizing of the LNA will result in $1/g_m=50$ and satisfies the matching requirement. However, there still exists the problem of high NF with this architecture. The impedance matching at the input port yields the following lower bound on the NF of common gate LNA [17]-

$$NF > = 1 + \frac{\gamma}{\alpha}$$

This will force a lower limit of around 4.7dB ($\gamma/\alpha \approx 2$) in short-channel devices, which is not an acceptable value for applications such as GPS receivers [17].

The most popular topology is inductively source degenerated topology because of its low noise, low power consumption features. Input impedance of this topology is-

$$z_{in} = j\omega(L_g + L_s) + \omega_L L_s + \frac{1}{j\omega C_{gs}}$$

$\omega_L$ is the transit frequency for the MOS device. Real part in the equation does not have any resistive part for which there will be no thermal noise. The value of source inductance needed to satisfy the input matching, i.e. $\omega_L L_s=50\Omega$, is usually very small (e.g., a few nH). This small inductance is usually realized using bond-wires with high quality factors and hence negligible loss and noise.

Due to the superior performance of L-deg LNA in terms of NF and power consumption, this architecture has found many applications in industry. In the last few years, several design techniques have been developed to satisfy the noise, gain, and power requirements of L-deg LNA for different applications. However, due to the narrowband nature, none of these approaches are suitable for broadband applications.
2.5 SCATTERING PARAMETERS

The short circuit admittance, open circuit impedance, hybrid h–, and hybrid g–parameters are commonly used to formulate two port circuit models that macroscopically inter-relate the driving point input and output impedance and forward and reverse transfer characteristics of relatively complex linear networks. These models are simple architectures in that they embody only four electrical parameters whose measurement or calculation exploit the electrical implications of short or open circuits imposed at the input and output ports of the network undergoing study. Although the parameterization of these conventional two port models can generally be executed straightforwardly and accurately at relatively low signal frequencies, high signal processing frequencies present at least two challenges in broadband electronics. The first of these challenges is that the unavoidable parasitic inductance implicit to circuit interconnects renders perfect short circuits an impossibility at very high signal frequencies. Moreover, very low impedance paths at either the input or the output port of electronic circuits may force embedded active devices to function nonlinearly or even to fail because of excessive current conduction. Second, the inherent potential instability of most high frequency or broadband electronic networks is exacerbated when these networks are constrained to operate with open circuited input or output ports. For example, attempts to measure the open circuit impedance parameters of a broadband electronic circuit are invariably disturbed by parasitic network oscillations incurred by the action of opening either an input or an output network port.

The daunting, if not impossible, challenge posed by the measurement of conventional two port parameters motivates the scattering, or S–parameter characterization of linear two port systems. In contrast to the impedance, admittance, and hybrid parameters, the scattering parameters of linear electrical or electronic networks are measured without need of short circuiting or open circuiting input and output ports. Instead, these ports are terminated in fixed and known characteristic impedances that are often similar or even identical to the terminating impedances incorporated in the design.

Fig. 2.2 depicts the linear two port network where voltage \( V_{s1} \) and \( V_{s2} \) are applied at input and output port. The indicated port voltages, \( V_1 \), and \( V_2 \), which are established in response to the
applied test signals, $V_{s1}$ and $V_{s2}$, can be viewed respectively as a superposition of incident and reflected components.

\[ V_{1} = V_{1i} + V_{1r} \]
\[ V_{2} = V_{2i} + V_{2r} \]

Where $V_{1i}$ is the incident voltage and $V_{1r}$ is the reflected voltage from port 1 and same analogy is applicable for port 2. Maximum energy will be transferred from source to port 1 if the impedance looking from the port 1 is equal to the source impedance ($R_0$). $a_1$ represents the maximum energy that can be transferred from the source. But the transferred energy will be less than this as there will be discrepancy between impedance of port 1 and source. So, some energy will be reflected from the input port.
\[ a_1 = \frac{V_{1i}}{\sqrt{R_0}} \]
\[ a_2 = \frac{V_{2i}}{\sqrt{R_0}} \]
\[ b_1 = \frac{V_{1r}}{\sqrt{R_0}} \]
\[ b_2 = \frac{V_{2r}}{\sqrt{R_0}} \]

Now, the scattering parameter matrix relates this \( b \) and \( a \) parameter.

\[
\begin{bmatrix}
   b_1 \\
   b_2
\end{bmatrix}
= \begin{bmatrix}
   S_{11} & S_{12} \\
   S_{21} & S_{22}
\end{bmatrix}
\begin{bmatrix}
   a_1 \\
   a_2
\end{bmatrix}
\]

If the output port incidence voltage is zero, then \( a_2 \) will be zero. Another, explanation is that if the output port is terminated by characteristic impedance then no energy will be reflected back to the input port. That means perfect matching at output port and \( a_2 \) will be zero. Under this condition,

\[
S_{11} = \frac{b_1}{a_1} \quad S_{21} = \frac{b_2}{a_1}
\]

\( S_{11} \) means the reflected coefficient at input port and \( S_{21} \) is the transmitted energy from input port to the output port when the output port is terminated by the characteristic impedance. Now, if the input port is terminated by the characteristic impedance and voltage is incident on the output port. Then \( a_1 \) will be zero.

\[
S_{12} = \frac{b_1}{a_2} \quad S_{22} = \frac{b_2}{a_2}
\]

\( S_{22} \) is the output port reflection coefficient and measure the output matching. \( S_{22} \) denotes the amount of energy reflected back from output port to input port. \( S_{12} \) is the reverse gain of the two port network. That means if we interchange the input port and output port, the amount of gain
we will find is the reverse gain. But it is required to have isolation between input port and output port.

Using these definitions, we can predict that a good amplifier should possess a large $S_{21}$ to achieve high gain, small $S_{11}$ and $S_{22}$ to possess good input and output matching, and very small $s_{12}$ to ensure stability and reverse isolation. The typical values of $S$ parameters for an LNA are $S_{11}$ and $S_{22}<-10\text{dB}$, $S_{21}>10\text{dB}$, and $S_{12}<-40\text{dB}$, which may vary according to the application.

### 2.6 Linearity

The dynamic range (DR) is usually defined as the ratio of the maximum input signal that the circuit can tolerate to the minimum input signal that provides adequate signal quality. The LNA should possess a large DR to guarantee that it remains linear when receiving weak signals in the presence of strong interferers. The upper limit of DR in low-frequency applications is usually defined as the maximum input power that the circuit can handle without going into saturation. However, in high-frequency applications, non-linear effects such as inter-modulation distortion or signal compression may be prominent and limit this upper bound.

Active RF devices are ultimately non-linear in operation. When driven with a large enough RF signal the device will always generate undesirable spurious signals. How much spurious effect will be generated by the device is dependent on its linearity characteristics. The linearity of a microwave circuit is defined in terms of a total of two parameters –

- 1-dB compression point
- Third order intercept point

The input 1-dB compression point is usually defined as the amplitude of the input signal at which small-signal gain drops 1dB below its nominal value (Fig. 2.3). Input signals above the compression point are usually clipped or saturated at the output; therefore, the compression point is considered an upper bound on the dynamic range of the LNA.
In telecommunications, a third-order intercept point (IP, IP3 or TOI) is a measure of linearity for systems and devices, for example receivers, linear amplifiers and mixers. The third-order intercept point relates nonlinear products caused by the 3rd order term in the nonlinearity to the linearly amplified signal.

The intercept point is a purely mathematical concept and does not correspond to a practically occurring physical power level. In many cases, it lies beyond the damage threshold of the device.

Two different definitions for intercept points are currently in use:

- **Based on a single input tone:** The device is tested using a single input tone. The nonlinear products caused by n-th order nonlinearity appear at n times the frequency of the input tone.

- **Based on inter-modulation products:** The device is fed with two sine tones with a small frequency difference. The n-th order inter-modulation products then appear at n times the frequency spacing of the input tones. This two-tone approach has the advantage that it is not restricted to broadband devices and is commonly used for radio receivers.
The intercept point is obtained graphically by plotting the output power versus the input power both on logarithmic scales. Two curves are drawn; one for the linearly amplified signal at an input tone frequency, one for a nonlinear product. On a logarithmic scale, the function \( x^n \) translates into a straight line with slope of \( n \). Therefore, the linearly amplified signal will exhibit a slope of 1. A third order nonlinear product will increase by 3 dB in power when the input power is raised by 1 dB.

Both curves are extended with straight lines of slope 1 and \( n \) (3 for a 3rd order intercept point). The point where the curves intersect is the intercept point (see figure 2.4). It can be read off from the input or output power axis, leading to input or output referred intercept points respectively (IIP3/OIP3). Input and output referred intercept points differ by the small signal gain of the device.

Fig. 2.4: Third Order Intercept Point

2.7 POWER GAIN

The power gain of an electrical network is the ratio of the output power to the input power. Three important parameters are defined in relation to the power gain of a circuit, namely average power gain, transducer power gain and available power gain [18].

The average power gain of a two-port network, \( G_P \), is defined as:
\[ GP = \frac{P_{\text{load}}}{P_{\text{input}}} \]

where \( P_{\text{load}} \) is the average power delivered to the load and \( P_{\text{input}} \) is the average power entering the network.

The transducer power gain of a two-port network, \( G_T \), is defined as:

\[ G_T = \frac{P_{\text{load}}}{P_{\text{source,max}}} \]

where \( P_{\text{load}} \) is the average power delivered to the load and \( P_{\text{source,max}} \) is the maximum average power available at the source. \( P_{\text{source,max}} \) may only be obtained from the source when the load impedance connected to it is the complex conjugate of the source impedance, a consequence of the maximum power theorem.

The available power gain of a two-port network, \( G_A \), is defined as:

\[ G_A = \frac{P_{\text{load,max}}}{P_{\text{source,max}}} \]

where \( P_{\text{load,max}} \) is the maximum average power available at the load and \( P_{\text{source,max}} \) is the maximum average power available at the source. Similarly, \( P_{\text{load,max}} \) may only be obtained when the load impedance is the complex conjugate of the output impedance of the network.

The parameters which are associated with the design of UWB LNA explained in this chapter. Several topologies are shown for input matching. These are the basic topologies exist in the literature. Among the above parameters, S-parameters are associated with input matching and output matching. Forward gain as high as possible is needed and input and output matching as low as possible are expected. Requirement of linearity of the LNA depends on the application in where it will be used.
CHAPTER 3

CIRCUIT ANALYSIS AND DESIGN CHALLENGES

The ultra-wideband LNA serves as an important building block for the ultra-wideband receiver. Flat and large gain, lower noise figure (NF), good linearity and lower power consumptions are needed for this type of LNA. But LNA’s behave differently at high frequency. At high frequency gain degrades, noise figure increases and parasitic capacitances become more dominant. So, many things need to be considered to design high frequency LNA. To address these challenges in the design of a wideband LNA, several topologies and circuit techniques have been proposed in the literature. In this section, some of the popular wideband architectures and with their advantages and disadvantages will be introduced.

3.1 NEGATIVE FEEDBACK LNA

One implementation of a negative feedback amplifier is shown in Fig. 3.1. In this circuit [19] the input stage is a common source amplifier and the feedback stage is a common drain amplifier. A simple analysis of this circuit shows that $g_{m,M2}$ of the common drain stage controls the input impedance, while $g_{m,M1}$ of the common source amplifier contributes to the gain and NF of the overall LNA. This is in contrast to the $1/g_m$ termination architecture where the $g_m$ of the input transistor is set by the input matching requirements and leaves no freedom for NF optimization. The main disadvantage of this architecture is the relatively high power consumption due to the addition of the feedback stage.
In another work, negative feedback is employed to realize a UWB LNA covering a 7GHz bandwidth (2 – 9 GHz) [20]. The schematic of this LNA is shown in Fig. 3.2. The input stage adopts a shunt-series feedback structure to satisfy the wideband input matching. The inverter configuration at the input is to increase the total trans-conductance \((g_{m1}+g_{m2})\), and hence the open-loop voltage gain for a fixed power consumption. The increase in the total trans-conductance also allows for a higher shunt resistor for a given 3dB bandwidth. This increase in the value of shunt resistance will lend itself to a lower total NF. Two degeneration inductances \(L_{s1}\) and \(L_{s2}\) are used to partially cancel the parasitic capacitances at the input of the LNA, which would otherwise devastate the impedance matching at high frequencies. The second stage is a simple cascode amplifier with a shunt-peaking load that provides the required gain of the entire LNA.
Negative feedback amplifiers may also be used as the second stage of wideband amplifiers. One example is the work in [21] that combines the benefits of $1/g_m$ termination with those of the negative feedback amplifier. Fig 3.3 depicts the schematic of this architecture. The input stage uses a common-gate amplifier to achieve 50Ω impedance matching. However, this matching sets the value of $g_m,M_1$, and another stage is required to provide sufficient gain over the entire bandwidth. This second stage is realized by employing $M_2$ in a shunt-feedback configuration. One drawback of this feedback is that the degradation of forward gain at high frequencies causes a positive feedback through $R_f$, thus leading to oscillation at the output. To alleviate this problem, $L_f$ is connected in series with the shunt resistor, $R_f$. This will reduce the feedback at high frequencies and also improve the gain flatness. $L_{d1}$ and $L_{d2}$ are inductive loads to compensate the gain degradation at high frequencies.
3.2 THERMAL-NOISE-CANCELLED WIDEBAND LNA

Feedback amplifiers, as discussed earlier, typically require two stages of amplification in order to provide sufficient gain and thus dissipate a large amount of power. Also note that the input impedance in a feedback amplifier is a function of the amplifier gain. However, this dependency is not straightforward, and the impedance matching is susceptible to the variations of the gain. To overcome these shortcomings, [22] suggests the use of a noise-cancelling feed-forward technique that decouples noise and input matching requirements. The conceptual schematic of this LNA is shown in Fig. 3.4. The noise current of the amplifier, $I_{n,i}$, flows out of the MOS device and passes through $R$ and $R_s$. Therefore, the instant noise voltages at nodes X and Y have the same polarity. Conversely, the signals at X and Y are of opposite polarities, simply due to the negative gain of the amplifier. This difference between the sign of signal and noise suggest the possibility of cancelling the noise while boosting the signal up.
To do so, another gain stage is inserted between the first stage and the output. The voltage at node Y (signal plus noise) is added with the properly scaled negative replica of the voltage at node X (the block shown by $-A_v$ generates this replica) [23]. By the proper choice of $A_v$, the noise contribution of the MOS device becomes equal to zero, and a low NF can be obtained over a wide range of frequency. The analysis in [23] derives the appropriate value of $A_v$ in terms of circuit elements $R$ and $R_s$:

$$A_v = 1 + \frac{R}{R_s}$$

It is also shown that, under these conditions, the noise contribution of different components is as follows:

$$NF_{LNA} = 1 + EF_{MOS} + EF_R + EF_A$$
\[ EF_{MOS} = 0 \]
\[ EF_R = \frac{R_s}{R} \]
\[ EF_A = \frac{\gamma g_m d_0}{g_{m2}} \left( \frac{1}{R_s} + \frac{3}{R} + \frac{2R_s}{R^2} \right) \]

where the excess noise factor, EF, is used to quantify the contribution of different noise sources to the NF_{LNA}. Also note that the impedance of the LNA equals \(1/g_{m1}\). Since the term \(g_{m1}\) is not present in the NF_{LNA} expressions, NF optimization and input matching can be done separately.

The idea of noise cancellation can be extended to any type of amplifier that has 1) a stage of impedance matching, 2) an auxiliary amplifier for sensing the voltage across a real input source, and 3) a circuit to combine the output of two amplifiers to cancel out the noise of the impedance matching stage. Some implementations of this idea are proposed in [23].

Despite all these benefits, the dominant pole at the input (node X) may limit the bandwidth at high frequencies. Furthermore, due to the existence of the parasitic capacitances, NF increases quadratically with the frequency. These effects, along with the high power consumption required by the two amplifiers, may limit the applications of this architecture.

### 3.3 Balanced Amplifier

A typical block diagram of a balanced amplifier [24-25] is shown in Fig. 3.5. It consists of two amplifiers in parallel and two 3dB Lange or hybrid couplers. The basic operation is as follows:

![Fig. 3.5: Schematic of balanced amplifier](image-url)
The input signal is split into two quadrature components (equal but with a 90° phase shift) by the input hybrid coupler. The two quadrature signals are then amplified using two identical LNAs. The output coupler combines the output signals of the two amplifiers by introducing an additional 90° phase shift, thus bringing them in phase again [26]. Denoting the S parameters of two amplifiers by \( S_{ij}^A \) and \( S_{ij}^B \), one can relate the S parameters of the entire amplifier to that of individual branches as follows:

\[
|S_{11}| = \frac{1}{2} |S_{11}^A - S_{11}^B| \\
|S_{22}| = \frac{1}{2} |S_{22}^A - S_{22}^B| \\
|S_{21}| = \frac{1}{2} |S_{21}^A + S_{21}^B| \\
|S_{12}| = \frac{1}{2} |S_{12}^A + S_{12}^B|
\]

The advantage of this architecture is that it possesses a very good matching at the input and output ports and continues to operate even if one of the amplifiers fails to function. However, this architecture suffers from the increased power consumption of two amplifiers, increased circuit size, and the bandwidth reduction caused by the couplers.

### 3.4 Distributed Amplifier

Distributed amplifiers (DA) (also known as travelling wave amplifiers) employ an architecture in which several active devices are connected in parallel [27]. A basic distributed amplifier is shown in Fig. 3.6. The output current of individual amplifiers combine in an additive fashion, and this dictates a relatively low gain for this architecture. The advantage of this architecture comes from the fact that the input capacitances of these amplifiers are distributed in an LC network which allows for the realization of amplifiers with large bandwidths. In fact, the series inductive elements and capacitances of MOS devices form an artificial transmission line, which allows the flow of the signal to the end of the gate line. The signal fed to the gate of the MOS device is transferred to the drain line through the trans-conductance \( g_m \) of the device. If the phase velocity on the gate and drain lines are identical, then the signals at the output add in the
forward direction as they arrive at the output. Many wideband LNAs in CMOS have been realized using DA architectures [28-29]. However, the large power consumption of this architecture is a major drawback and makes it unsuitable for low-power portable systems.

![Schematics of Distributed Amplifier](image)

These architectures are most well-known for ultra-wideband LNA design. Though these are successfully used in several applications, there are still several things needs to be addressed.

Large chip size, bandwidth limitation and large power consumption are the main problems of these structures. So, a well-established methodology is needed for designing low power LNA. The inductively degenerated LNA (L-deg LNA for short) satisfies the input matching requirement without introducing the additional noise attributed to a real resistor. In addition, compared to other architectures, L-deg LNAs consume less power and therefore are especially suitable for low-power applications.
The design of L-deg LNA involves many trade-offs among gain, NF, power consumption, matching, and linearity. Several design techniques have been proposed to satisfy these requirements for different applications. The classical noise matching (CNM) technique [30], simultaneous noise and input matching (SNIM) technique [31], power constrained noise optimization (PCNO) technique [32], and power-constrained simultaneous noise and input matching (PCSNIM) technique [33-34] are among the many design procedures developed for this architecture.

All these design techniques have been developed based on the assumption of narrowband input signal; i.e., the bandwidth of the input signal to be amplified is much smaller than the center frequency.

However, low power consumption and the low NF capabilities of L-deg LNAs have motivated us to develop a new methodology for Ultra-Wide-Band (UWB) applications.

### 3.5 Proposed Circuit

The proposed design is shown in Fig. 3.7 for 15-22GHz, an inductively source degenerated common source amplifier which is commonly used in narrowband LNA design [35]. This design ensures wideband matching by employing a three section chebyshev filter at the input of inductively source degenerated amplifier and coupling inductor at output of the main MOS. The overall input reactance will be on resonance over the band of interest for wideband application. In this structure two cascoding common source amplifier share the same supply, ‘ current reuse topology [36] ’ to reduce the power consumption and also to boost the gain by the multiplication of the trans-conductances of the two cascoding stages. The bandwidth can be increased by reducing the parasitic capacitances $C_{gs2}$ and $C_{gd1}$ by introducing inductor in the system. This inductor provides an inter-stage matching and simultaneously reduces the effect of parasitic gate to source capacitance ($C_{gs2}$) of cascoded MOS transistor on top & gate to drain capacitance ($C_{gd1}$) of MOS transistor at bottom. $L_c$, $C_{gd1}$ and $C_{gs2}$ form a broadband $\pi$-LC filter [37]. An output capacitor is placed before the output to increase the gain by creating resonance at center frequency with the load inductance. But generally this resonance is occurred outside the band.
The input network is intended to match with 50 ohm impedance and also the output impedance is matched with 50 ohm. Others parameters $R_s$, $R_l$, $R_d$ are the source resistance, load resistance and bias resistance, respectively.

Fig. 3.7: Schematic of the proposed LNA

### 3.5.1 Input Matching

To ensure maximum power transfer from source to the amplifier impedance matching is necessary. Input network provide that matching with the source over the band and also ensure flat gain. Input impedance is calculated from the small signal model shown in Fig. 3.8.
Fig. 3.8: Small signal model of input matching network

\[
v_{in} = sLg i_{in} + \frac{1}{sC_{gs}} i_{in} + \left(\frac{g_m}{sC_{gs}} i_{in} + i_{in}\right) sL_S = sLg i_{in} + \frac{1}{sC_{gs}} i_{in} + \frac{g_m L_s}{C_{gs}} i_{in} + sL_S i_{in}
\]

\[
Z_{in} = s(Lg + L_S) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}}
\]

Real part:

\[
R_{in} = \frac{g_m L_s}{C_{gs}}
\]

Reactive part:

\[
s(Lg + L_S) + \frac{1}{sC_{gs}} \Rightarrow \omega_0 = \frac{1}{\sqrt{(Lg + L_S)C_{gs}}}
\]

This input impedance of the cascode device is incorporated with the three section T-network chebyshev filter to match source impedance in a wider band shown in Fig. 3.9 Real part is the termination of the chebyshev filter. It shows good performance while dissipating small amounts of DC power. For this portion, power comes from radiation greater than 10µW and \(R_s = R_{in}\) ensures maximum power transferred to the input.
The response of the chebyshev filter is shown in figure 3.10. We know that at maximum power transfer load voltage is half of the source voltage. But here the maximum voltage due to 1V ac voltage at the termination resistance is 0.47V.

The function of the T-network is to match the source impedance, $R_s$ equals to the $R_{in}$ for the
whole band of interest. $C_{gs}$ depends on the width of $M_1$ transistor. $L_g + L_s$ is chosen as to make series resonance at center of the band. $C_1$ is used to block DC and should be large enough so that it doesn’t alter series resonance of the network. But the series resonance changes due to the parasitic gate-drain capacitance $C_{gd1}$ of the main transistor, gate-source capacitance $C_{gs2}$ of cascaded MOS and coupling inductor $L_c$. Others parameters depend on the band of interest but it also changes due to the parasitic capacitances.

Another choice for the wideband impedance matching is butterworth filter. Three section butterworth filter uses less number of inductors and capacitors than three section chebyshev filter. But butterworth filter does not ensure constant gain in the whole band of interest. But chebyshev filter provides constant gain over the desired band. Due to constant gain characteristic of chebyshev filter, chebyshev filter is used in this work for impedance matching.

The picture described so far is complicated by the presence of the gate–drain capacitance $C_{gd1}$ of $M_1$. The real part of $Z_{in}$ from what we have shown in 3.9. The desired branch series resonance is determined by the resonance of $L_g$ and the parallel combination of $C_{gd}$ and the equivalent capacitance due to the series combination of $C_{gs}$ and $L_s$, i.e., $C_{gs}/(1-\omega^2 L_s C_{gs})$. $C_{gd}$ also introduces one more parallel resonance and one more series resonance. The parallel resonance essentially occurs between $C_{gd}$ and $L_g$. The second series resonance, on the other hand, occurs between $L_g$ and the equivalent capacitance resulting from the parallel combination of $C_{gd}$ and $L_s$ at frequencies higher than the parallel resonance.

![Schematic of the input network of the LNA including parasitic capacitance](image_url)
3.5.2 Output Impedance Matching

Once the input impedance is matched, output impedance matching has to be done to achieve maximum power gain at the output. The load at output node is designed to achieve flat and considerably high gain over the band of interest. The output of the LNA is generally characterized with the behavior of the output node to a 50Ω resistive termination. Generally, both high gain and wide bandwidth are required for UWB system. And surprisingly, gain and bandwidth is inversely proportional to each other. That’s why gain is sacrificed for higher bandwidth or bandwidth is sacrificed for higher gain. Output is drawn by a capacitor which is seen from the fig 3.7. Bandwidth and gain of the LNA depends on the quality factor of the output load inductance. A resistance is inserted in series with the load inductance to control the quality factor (Q) of the $L_L$. Quality factor of the $L_L$ is, $Q = \frac{\omega L_L}{R_L}$. Increasing the value of resistance decreases the quality factor and finally increases bandwidth. For large $R_L$, noise contribution will be large by the resistance. So, we need to choose optimum resistance for both bandwidth and noise contribution.

For mathematical demonstration of gain-bandwidth dependence on quality factor, the $Z_{load}$ is drawn on figure in 3.12 (a) where $C_{gd2}$ is the gate-drain capacitance of the cascode MOS transistor.

![Load Impedance](image1.png)

(a)

![Approximation Circuit](image2.png)

(b)

Fig. 3.12: (a) Load impedance (b) approximation circuit of load impedance
\[ Z_{\text{load}}(s) = \frac{R_L + sL_L}{1 + s^2L_LC_{gd2} + sR_LC_{gd2}} \approx \frac{sL_L}{s^2L_LC_{gd2} + sR_LC_{gd2} + 1} \]

Calculating for the approximation figure, \( Z_{\text{load}}(s) = \frac{sL_L}{s^2L_LC_{gd2} + sL_L/ R_{\text{load}} + 1} \)

By comparing equations,

\[ \frac{L_L}{R_{\text{load}}} = R_LC_{gd2} \]
\[ \Rightarrow R_{\text{load}} = \frac{L_L}{R_LC_{gd2}} \]

\[ \Rightarrow R_{\text{load}} = R_L \frac{L_L^2}{R_L^2} \frac{1}{L_LC_{gd2}} \]
\[ \Rightarrow R_{\text{load}} = \frac{\omega_c^2 L_L^2}{R_L^2} R_L = Q_L^2 R_L \]

Where, \( \omega_c = \frac{1}{\sqrt{C_{gd2}L_L}} \), \( Q_L \) is the quality factor.

For perfect output matching, \( \text{Im}\{Z_{\text{out}}\} = 0 \) and the gain of the amplifier solely depends on the real part of the \( \text{Re}\{Z_{\text{out}}\} = R_{\text{load}} \). But as \( R_L \) increases \( R_{\text{load}} \) decreases and finally gain decreases. But the bandwidth increases as the -3dB point moves away from the center frequency. Maximum Gain and minimum BW is achieved when \( R_L = 0 \). Increasing \( R_L \) increases the BW, reducing the gain, thus keeping the Gain-Bandwidth product constant. So, Gain-Bandwidth can be adjusted by simply choosing a suitable value of \( R_L \). Of course, NF will degrade slightly if \( R_L \) is increased.
The magnitude of $R_L$ and $C_{out}$ plays an important role. Due to $R_L$, a zero is introduced in the system which increases the bandwidth and as $R_L$ increases bandwidth also increases. $C_{out}$ creates a resonance at center frequency with inductive load and finally increases the gain of the system.

$L_L$ increases gain by creating resonance at center frequency. In addition, $L_L$ also provides an additional level of highly desirable band pass filtering. $C_{out}$ capacitor with overall load impedance will provide matching close to the output impedance and also blocks DC voltage [38].

### 3.5.3 Voltage Gain Analysis

To derive the voltage gain of the amplifier, first need to analyze the input section of the proposed design. The input network of the proposed design is the three sections band-pass chebyshev filter. The function of this filter is to match input impedance over the whole bandwidth.

Transfer function of the chebyshev filter in band is unity and where out of band is zero ideally. So, voltage at output of the chebyshev filter will be same as input voltage of the chebyshev filter and input point is indicated in fig. 3.13.

![Fig. 3.13: Schematic of input network](image)

So, the current flowing into the gate of the main MOS transistor is, $i_{in} = \frac{v_{in}}{R_s}$, So voltage across the gate to source, $v_{gs} = i_{in} / sC_{gs} = \frac{v_{in}}{sC_{gs}R_s}$. Current through both $M_1$ & $M_2$ is same.
for ideal cascode configuration. The output voltage $v_d$ calculating from the small signal model of fig. 3.14 is shown below.

$$v_d = -g_m Z_d v_{gs}$$

$$Z_d = (R_L + sL_L) \frac{1}{(1/sC_d)}$$

$$= \frac{R_L + sL_L}{1 + s^2 L_L C_d + sR_L C_d}$$

$$= \frac{R_L (1 + \frac{SL_L}{R_L})}{1 + s^2 L_L C_d + sR_L C_d}$$

Fig. 3.14: Overall small signal model

There are two poles exist on this system. Here, $L_L$ introduces a zero in the system. Inductor compensates the roll-off by introducing that zero.
\[
\frac{v_d}{v_{in}} = -g_m \frac{1}{sC_{gs}R_s} \frac{R_L}{1 + \frac{sL}{R_L}} \left(1 + s^2L_LC_d + sR_LC_d\right)
\]

But the parasitic capacitances $C_{sb1}$, $C_{gs2}$ and $C_{db1}$ have detrimental effect on the amplifier gain. The $C_{db1}$, $C_{gs2}$ introduces pole on the system. Introduction of pole on the system means bandwidth reduction of the system.

To reduce the effect of $C_{sb1}$, body of the main transistor is connected with source of $M_1$. An inductor is placed between $C_{gs2}$, $C_{gd2}$. $L_C$ introduces a zero in the system and form a $\pi$-LC bandpass filter. As an effect, it reduces the gain roll-off and increases the bandwidth of the system.

The effect of the $C_{gs2}$ is shown on the analysis given below-

![Overall small signal model including parasitic gate to source capacitance](image)

**Fig. 3.15:** Overall small signal model including parasitic gate to source capacitance
\[ v_{in} = sLg_{in} + v_{gs1} + (i_{in} + g_{ml}v_{gs1})sL_s \]
\[ v_{gs1} + \frac{i_{in}}{sC_{gs1}} \]

\[ = \left( s^2C_{gs1}L_g + 1 + s^2L_sC_{gs1} + sg_{ml}L_s \right) v_{gs1} \]

\[ g_{m2}v_{gs2} - i_1 = g_{ml}v_{gs1} \]

\[ \Rightarrow g_{m2}v_{gs2} + v_{gs2}^{-} + s_{gs2}C_{gs2} = g_{m1}v_{gs1} \]

\[ \Rightarrow v_{gs2} = \frac{g_{m1}}{(g_{m2} + sC_{gs2})} v_{gs1} \]

\[ v_d = -g_{m2}Z_d v_{gs2} \]

\[ = g_{m2} \frac{g_{m1}}{g_{m2} + sC_{gs2}} \cdot \frac{v_{in}}{s^2C_{gs1}L_g + 1 + s^2L_sC_{gs1} + sg_{ml}L_s} \cdot Z_d \]

\[ \frac{v_d}{v_{in}} = \frac{g_{m1}}{g_{m2} + sC_{gs2}} \cdot \frac{1}{s^2C_{gs1}L_g + 1 + s^2L_sC_{gs1} + sg_{ml}L_s} \cdot Z_d \]

From the above equation it is evident that, gate to source capacitance of diode connected MOS introduces a pole in the system. A pole in a system reduces the bandwidth of the system. Also the gain will be decreased by the introduction of the parasitic capacitance. The calculation will be more complicated if we introduce gate-drain parasitic capacitance in the system. Effect of pole of this system is reduced by the coupling inductor which will increase bandwidth along with gain of the system.

3.5.4 Noise Optimization

There are 4 techniques of optimizing noise of a circuit. Noise optimization is needed for the better noise performance of the circuit.
3.5.4.1 CLASSICAL NOISE MATCHING (CNM) TECHNIQUE

In this technique, the LNA is designed for minimum noise figure $NF_{\text{min}}$ by presenting the optimum noise impedance $Z_{\text{opt}}$ to the given amplifier, which is typically implemented by adding a matching circuit between the source and the input of the amplifier. By using this technique, the LNA can be designed to achieve NF equal to $NF_{\text{min}}$ of transistor, the lowest NF that can be obtained with given technology. However, due to the inherent mismatch between $Z_{\text{opt}}$ and $Z_{\text{in}}^*$ (where $\text{in}^*$ is the complex conjugate of the $Z_{\text{in}}^*$ amplifier input impedance), the amplifier can experience a significant gain mismatch at the input. Therefore, the CNM technique typically requires compromise between the gain and noise performance.

Fig. 3.16 (a) shows a cascode-type LNA topology, which is one of the most popular topology due to its wide bandwidth, high gain, and high reverse isolation. In the given example, the selection of the cascode topology simplifies the analysis, and the gate-drain capacitance can be neglected.

Fig. 3.16 (b) shows the simplified small-signal equivalent circuit of the cascode amplifier for the noise analysis including the intrinsic transistor noise model. In Fig. 3.16-(b), the effects of the common-gate transistor $M_2$ on the noise and frequency response are neglected [30] as well as the parasitic resistances of gate, body, source, and drain terminal.
Fig. 3.16: The schematic of a cascode LNA topology adopted to apply the CNM technique (a) and its small-signal equivalent circuit (b)

The noise parameters for this amplifier are:

\[ R_n^o = \frac{\gamma'}{\alpha} \cdot \frac{1}{g_m} \]

\[ Y_{opt}^o = \alpha \omega C_{gs} \sqrt{\frac{\delta}{5\gamma}} \left( 1 - |c|^2 \right) + sC_{gr} \left( 1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right) \]

\[ F_{min}^o = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma \delta (1 - |c|^2)} \]

where \( R_n^o \) represents the noise resistance, the optimum noise admittance \( Y_{opt}^o \), \( F_{min}^o \) the minimum noise figure, respectively.

The cutoff frequency \( \omega_T \) is equal to \( g_m/C_{gs} \), and \( \alpha = g_m/g_{do} \) is unity for long-channel devices and decreases as channel length scales down. Note that, from Fig. 3.16-(b), the input admittance is purely capacitive, i.e. \( j\omega C_{gs} \). By comparing the complex conjugate of \( Y_{in} \) with optimum noise admittance, \( Y_{opt}^o \), it can be seen that the optimum source admittance for input matching is inherently different from that of the noise matching in both real and imaginary parts. Thus, with the given example, one cannot obtain both input matching and minimum noise figure simultaneously. This is the main limitation of the CNM technique when applied to the LNA topology shown in Fig. 3.16-(a). Note that the imaginary component of optimum noise
admittance is inductive, but the frequency response is like that of a capacitor. Hence, there is a fundamental limitation in achieving a broadband noise matching.

3.5.4.2 Simultaneous Noise and Input Matching (SNIM) Technique

Feedback techniques are often adopted in designing low noise amplifiers in order to shift the optimum noise impedance $Z_{opt}$ to the desired point. Parallel feedback has been applied for wideband and better input/output matching. Series feedback has been preferred to obtain simultaneous noise and input matching without the degradation of NF [39-42]. Especially, the series feedback with inductive source degeneration, which is applied to the common-source or cascode topology, is widely used for narrow band applications [43-49].

Fig. 3.17 (a) and (b) show a cascode LNA with inductive source degeneration and the simplified small-signal equivalent circuit.

![Diagram](image)

(a)

![Diagram](image)

(b)

Fig. 3.17: The schematic of a cascode LNA topology adopted to apply the SNIM technique (a) and its small-signal equivalent circuit (b)
Noise parameters using this technique for the inductively degenerated LNA circuit are –

\[
F = 1 + \frac{1}{g_m^2 R_s} \left\{ \gamma d_0 \left[ 1 + s^2 C_{gs} \left( L_s + L_c \right) \left( 1 + |e| |a| \sqrt{\frac{\delta}{5\gamma}} \right) \right] - \left( s C_{gs} R_s \right)^2 \left( 1 + |e| |a| \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\} - \frac{a\delta}{5} \left( 1 - |e|^2 \right) g_m \left( s C_{gs} \right)^2 \left( R_s^2 - sL_g^2 \right)
\]

\[
R_n = R_n^\alpha = \frac{\gamma}{\alpha g_m}
\]

\[
Z_{opt} = Z_{opt}^\alpha - sL_s
\]

\[
F_{min} = F_{min}^\alpha = 1 + \frac{2}{\omega/\omega_c} \sqrt{\gamma\delta (1 - |e|^2)}
\]

The noise parameters with superscripted zeros are those of the cascode amplifier with no degeneration. \( Z_{opt}^\alpha \) is given by

\[
Z_{opt} = \frac{\alpha \sqrt{\frac{\delta}{5\gamma (1 - |e|^2)}} + j \left( 1 + |e| |a| \sqrt{\frac{\delta}{5\gamma}} \right)}{\omega C_{gs} \left\{ \frac{\alpha^2 \delta}{5\gamma (1 - |e|^2)} + \left( 1 + |e| |a| \sqrt{\frac{\delta}{5\gamma}} \right) \right\}}
\]

So only \( Z_{opt} \) shifted and no change in \( R_n \) and \( F_{min} \). The input impedance of the LNA is -

\[
Z_{in} = s(L_s + L_c) + \frac{1}{s C_{gs}} + \frac{g_m L_s}{C_{gs}}
\]

From the above equation it is found that real part is introduced in the input impedance equation and it was not for non-degenerated LNA. This is important because there is no real part in the \( Z_{in} \) without degeneration while there is in the \( Z_{opt} \). Therefore \( L_s \) helps to reduce the discrepancy between the real parts of the \( Z_{opt} \) and the \( Z_{in} \) of LNA. Furthermore the imaginary part of \( Z_{in} \) is changed by \( sL_s \), and this is followed by the same change in \( Z_{opt} \). Therefore it can be said that
inductive source degeneration helps to bring $Z_{\text{opt}}$ close to the input impedance complex conjugate point without degrading $R_n$ and $F_{\text{min}}$.

The noise performance is related to the input impedance, $Z_{\text{in}}$, source impedance, $Z_s$ and optimum impedance, $Z_{\text{opt}}$. To obtain the wideband noise and input matching, the source impedance seen from the gate of the input transistor should be the complex conjugate of the input impedance, $Z_{\text{in}}$ to deliver the maximum power and at the same time is equal to $Z_{\text{opt}}$ to achieve $NF_{\text{min}}$. Thus the following four conditions should hold over the entire frequency band of interest:

\[
\begin{align*}
\text{Re}\{Z_{\text{opt}}\} &= \text{Re}\{Z_s\} \\
\text{Im}\{Z_{\text{opt}}\} &= \text{Im}\{Z_s\} \\
\text{Re}\{Z_{\text{in}}\} &= \text{Re}\{Z_s\} \\
\text{Im}\{Z_{\text{in}}\} &= \text{Im}\{Z_s\}
\end{align*}
\]

Combining the above criteria, simultaneous noise and input matching are achieved when,

\[Z_{\text{in}} = Z_{\text{opt}}^*\]

The proposed circuit used SNIM technique for noise optimization. These four conditions of SNIM technique need to be hold for this circuit to achieve minimum noise figure and simultaneously maximum power transfer.

The value of $Z_{\text{in}}$ is analyzed in input matching section and $Z_{\text{opt}}$ in noise contribution section. If they become equal, then the noise can be optimized. But due to inductive terms in aforementioned equations, the inductive reactance fades the effect of capacitance at high frequencies, further improving the noise performance.

The matching of $\text{Re}\{Z_{\text{opt}}\}$ and $\text{Re}\{Z_{\text{in}}\}$ in a wide frequency range is very challenging. This is due to the fact that $\text{Re}\{Z_{\text{opt}}\}$ is frequency-dependant while $\text{Re}\{Z_{\text{in}}\}$ is constant and bias dependant. $\text{Re}\{Z_{\text{in}}\}$ is also a function of $L_s$ and by the proper choice of this inductance we can optimize the circuit for wideband operation. SNIM is not optimized for low power consumption circuit because lower size MOS results higher source inductor value. As the proposed circuit consumes small power so there is some mismatch between $NF$ and $NF_{\text{min}}$. 
3.5.5 Noise Contribution

The noise performance of the proposed topology is determined by two main contributors: the losses of the input network and the noise of the amplifying device. The noise contribution of the input network is due to the limited quality factor of the integrated inductors. Its optimization relies on achieving the highest for a given inductance value. The optimization of the noise contribution from relies instead on the choice of its width for a given bias current. Optimum device width has been fully discussed in the literature in the case of narrow-band LNA design [35]. We extend the analysis to the wideband case, i.e., we investigate the amplifier noise behavior over a wide range of frequencies. Optimization is performed on the in-band average NF, as opposed to the spot NF (i.e., NF at a single frequency), used in the narrow-band case. The analysis follows the guidelines of [6] in a dual fashion and with the difference that the loading effect of the local feedback inductor is taken into account.

The noise sources are drain-induced noise current and gate-induced noise current. Gate-induced noise current is correlated with drain-induced noise current. The equivalent current and thevenin noise voltage is shown in Fig. 3.18. Input referred noise current \( i_n \) and voltage \( v_n \) are -

\[
i_n = i_{ng} + \left( i_{nd}/g_m \right) sC_{gs}
\]

\[
v_n = i_{nd}/g_m + sL_i i_n
\]

Spectral density of \( i_{nd} \) & \( i_{ng} \):

\[
S_{i_{nd}}(\omega) = i_{nd}^2 = 4Kg_d
\]

\[
S_{i_{ng}}(\omega) = i_{ng}^2 = 4Kg_g
\]

\[
g_g = \frac{\omega^2 C_{gs}}{5g_d}
\]
The noise voltage can be expressed as the sum of two components, one fully correlated, and the other, uncorrelated to the noise current as follows:

\[ e_n = e_{nc} + e_{nu} \]

Carrying out the calculations, the correlation impedance is written as [details in Appendix]:

\[
Z_c = \frac{1 - \omega^2 L^S C_w \left[ 1 + 2 \left| c \right| a + a^2 \chi \right]}{j \omega C_{gs} \left[ 1 + 2 \left| c \right| a + a^2 \chi \right]}
\]

Where, \( \chi = \sqrt{\frac{\delta}{5\gamma}} \), \( \alpha \leq 1 \). \( \frac{i_{ng} \gamma_{nd}}{\sqrt{i_{ng}^2 + i_{nd}^2}} \) is the co-efficient factor between gate-induced noise current and drain induced-noise current. For MOS devices the value of \( c \) is \( j0.4 \) [50]. \( \alpha = \frac{g_m}{g_{d0}} \)

is account for the short channel effects. It describes the transconductance reduction due to velocity saturation and mobility decreases due to vertical electric field [35], [51].

The two uncorrelated noise sources, \( e_{nu} \) and \( i_n \) are described by the following parameters:

\[
R_u = \frac{\gamma}{\alpha^2 g_{d0} \left[ 1 + 2 \left| c \right| a + a^2 \chi \right]} \cdot \frac{a^2 \chi^2 (1 - \left| c \right|^2)}{1 + 2 \left| c \right| a + a^2 \chi^2}
\]
\[ G_n = \frac{\gamma}{\alpha^2 g_{d0}} \omega^2 C_{gs} \left(1 + 2|c|\alpha\chi + \alpha^2\chi^2 \right) \]

By introducing the noise parameters, NF can be expressed as:

\[ F = 1 + R_u + \frac{|Z_c + Z_s|^2}{R_s} G_n \]

Where \( Z_s = R_s + jX_s \);

Classic noise optimization theory [52], [6] shows that the minimum NF is achieved if the source impedance \( Z_s = Z_{opt} = R_{opt} + jX_{opt} \) is chosen such that,

\[ R_{opt} = \sqrt{\frac{R_u}{G_n}} = \frac{\alpha\chi(1-|c|^2)}{\omega C_{gs} \left(1 + 2|c|\alpha\chi + \alpha^2\chi^2 \right)} \]

But here, \( R_c = 0 \) and \( X_{opt} = -X_c \). Optimum source impedance is roughly equal to that at which the \( C_{gs} \) & \( L_s \) resonates. As a consequence nearly \( \text{min} \) NF is achieved by using the input network proposed here over the whole bandwidth.

Overall noise figure of the main MOS transistor can be calculated as [6]-

\[ F(\omega) = 1 + \frac{R_u}{R_s} + G_n R_s = 1 + \frac{P(\omega)}{g_m R_s} \frac{\gamma}{\alpha} \]

\[ P(\omega) = \frac{\alpha^2\chi^2(1-|c|^2)}{1+2|c|\alpha\chi + \alpha^2\chi^2} + \omega^2 C_{gs} 2 R_s(1+2|c|\alpha\chi + \alpha^2\chi^2) \]

From the above equations, using a smaller width transistor for a given transconductance \( (g_m) \) drawing more current is preferable. Moreover, increasing the \( g_m \) by keeping all others parameters as it is also decreases the noise figure. Above noise analysis showed that noise figure (NF) mainly depends on bias current \( (I_D) \), width \( (W) \), overdrive voltage \( (V_{ov}) \) and frequency \( (\omega) \). Increasing width deteriorates noise figure due to higher gate-source capacitance, \( C_{gs} \). Higher bias current improves the noise performance at the cost of higher power consumption. For each value of bias current the device width can be chosen to minimize the NF [50]. If better noise
performance is required, the design can be improved by raising bias current from the original value.

Others sources of noise in this proposed design are load resistance ($R_L$), cascode MOS ($M_2$) itself and input matching network inductors, coupling inductor & load inductor due to their finite quality factor. But input network noise contribution is optimized by choosing highest Q-factor for a specific inductance value and same work is done for coupling inductor ($L_c$) & load inductor ($L_L$). Load resistance noise contribution negligible as a very small resistance is used at load. As the bias current of the proposed topology is fixed by the main transistor ($M_1$), smaller width is chosen for cascode MOS ($M_2$). Due to smaller width noise contribution will be less from this transistor.

3.5.6 Cascode Structure

Isolation is very important for high frequency amplifier design. Otherwise, power will reflect back to the input port from the output port. So, $S_{12}$ has to be highly negative. There are several configurations for making reverse isolation better as CS-CG [6], CG-CS [53] and CS-CS [54].

CG-CS structure takes input in CG configuration and fed the output to a CS amplifier. Impedance matching is easier in CG structure. This configuration has a very low noise figure. But the problem is that gain is also low for this configuration. Input impedance depends on the biasing of the MOS.

In this work, CS-CG in fig. 3.19(b) structure is used for better isolation than the other mentioned design. A CG is connected at the output of CS structure. CG just passes the output of the main MOS and amplification is done in the first stage. CG is also provides output matching along with load and output capacitor. CS-CG structure has the better reverse isolation but the problem is that it consumes more power than the other cascode structures.

CS-CS in fig. 3.19 (a) structure two CS MOS amplifier and amplify the signal two times. Output of the first CS amplifier is fed to the gate of the second CS amplifier by a coupling capacitor. This structure shows a very high voltage gain because the overall transconductance is the multiplication of transconductances of two MOS transistor. Main problem of this structure is larger chip area because of many inductors and capacitors.
3.5.7 **POWER CONSUMPTION**

Nowadays major concern of RF low noise circuit design is power consumption. Low power analog circuit is highly desired. Linearity, input impedance, noise figure, voltage gain, power gain depends on $g_m$ of the circuit and related with each other by $g_m$. $g_m$ depends on biasing of the MOS, width of the MOS and as a whole on power dissipation.

Input impedance of a source degenerated LNA is $g_mL_s/C_{gs}$. To tune input impedance needs to change bias and width of the transistor. So, matching of input impedance also depends on power dissipation.

![Fig. 3.19: Demonstrating (a) CS-CS cascode (b) CS-CG cascode and (c) CG-CS cascode structures](image)

From noise contribution section, it is seen that NF of this proposed circuit relies on tranconductance, frequency, and width of the transistor. NF decreases as $g_m$ increases. So, higher power consumption means higher bias current which subsequently reduces the NF of the LNA. Width (W), bias current ($I_D$) and overdrive voltage ($V_{ov}$) are selected as a compromise between NF and power consumption of the circuit.
In this chapter, design of the proposed amplifiers with different parasitic effect has shown. Different types of optimization techniques, different cascode configuration with their relative merits and demerits have also shown in this chapter. The adopted technique has explained from the perspective of the proposed LNA.
CHAPTER FOUR
RESULTS AND DISCUSSION

4.1 SIMULATION

Circuit’s components values are needed to perform the simulation. The parameters values are chosen in such a way that meets the design requirement. The input network component is selected such that input reflection should be less than -10dB for the entire band of interest (15GHz-22GHz) and minima very close to the center frequency 17.56GHz. Chebyshev filter at input is of three sections uses T-network as a compromise between complexity and components value because two sections require very high value of capacitor. This would require an extremely high \( g_m \) to ensure adequate gain and noise performance.

The width of \( M_1 \) is chosen as 150\( \mu \)m which is optimized for noise. It is sized for a given current budget so that both thermal noise and induced gate noise are balanced. The gate-drain capacitance decreases the real part of the input impedance, \( g_m L_s/C_{gs} \). So, that \( L_s \) should be larger than the calculated value in the simulation \( L_s > C_{gs} R_s/g_m \). Center frequency is set by the series resonance of \( L_g + L_s \) and \( C_{gs} \). But it also depends on \( C_{gd1}, C_{gs2}, \) & \( L_c \). Finally, the chosen values of the input network are \( L_g=0.045nH, \) \( L_s=0.222nH, \) \( L_p=0.238nH, \) \( C_1=180fF, \) \( C_p=85fF \) and \( L_1=0.265nH \), respectively.

The cascode MOS is used for the isolation between input and output node. But this device also contributes to the overall noise figure. So, the MOS is selected as small as possible to reduce the parasitic capacitance and noise contribution. Width of \( M_2 \) is selected to be 125\( \mu \)m.

The load, output capacitor and the coupling inductor are designed in such a way to achieve flat and considerably high gain over the whole bandwidth of the amplifier. The choice of \( L_L \) is determined by two opposite requirements: must be large to have large gain, and it must be small so that it resonances out-of-band. \( R_L \) must be chosen in such a way so that zero frequency \( \omega_z = \frac{R_L}{L_L} \) as close as possible to the lower band edge to increase gain. Upper limit is set by the voltage head room of the cascode MOS transistor. Another requirement is to make the output...
reflection parameter less than -10dB at center frequency. The values for the load components are, \( R_L = 4.53\Omega \), \( L_L = 0.427\text{nH} \), \( C_{out} = 80\text{fF} \) and \( L_c = 0.3\text{nH} \), respectively.

For biasing a current mirror topology is used. A saturated MOS with a resistance at drain is used for this purpose. The length and width of the biasing MOS is fixed to 0.6 (W/L). Long channel devices have lower noise than short channel device [17]. Biasing network shouldn’t have any effect on input network. That’s why the MOS is chosen in such a way so that its parasitic has no effect on input impedance and operating frequency.

### 4.2 Results

The circuit is simulated using IBM 0.13\( \mu \text{m} \) CMOS 8RF process and the simulated response found from Cadence Spectre is exhibited in this section. However, first the circuit was simulated in Hspice RF to see the effect of the design.

The results of the Hspice RF simulation are given below in the Fig. 4.1. Center frequency is 20GHz and bandwidth of 8.4GHz. Reverse isolation is below -25dB. \( S_{11} \) is below -10dB for the entire band.

![Fig. 4.1: S-parameter as a function of frequency in Hspice](image-url)
But due to parasitic capacitance in Cadence Spectre, simulated bandwidth decreases to 6GHz and gain also decreases. The maximum forward gain $S_{21}$ is 10.1dB at 17.56GHz with 3dB bandwidth 6.4GHz from 15.2GHz-21.6GHz as shown in Fig. 4.2. So, center frequency shifted from 20GHz. Reverse isolation $S_{12}$ is -22dB at 17.56GHz which shows the effectiveness of cascode configuration in Fig. 4.3. Reverse isolation is -29dB at lower band edge and -20dB at upper band edge. Input and output matching parameters are shown in Fig. 4.4. $S_{11}$ is less than -10dB for the entire band of operation. -10dB generally means perfect input match which ensures maximum power transfer from antenna to the amplifier in this band. To make reflection parameter, $\Gamma = 0$ $S_{11}$ has to be $-\infty \text{dB}$. But practically $S_{11}$ less than -10dB means perfect match. $S_{11}$ minima are -30dB at 16GHz and it is -12dB at center frequency. Real part of input impedance lies in between 45$\Omega$ to 60$\Omega$ shown in fig. 4.5 in the operating band. That’s why input reflection parameter is below -10dB for the entire band. Input impedance is perfectly matched near 16GHz. Output matching parameter $S_{22}$ is -25dB at center frequency, 17.56GHz. $S_{22}$ is less than -10dB from 16.4GHz to 18.8GHz where -10dB effective bandwidth is 2.4GHz.

Fig. 4.2: Forward gain, $S_{21}$ as a function of frequency

But without the coupling inductor, $L_C$ this design would have a lesser bandwidth and lower gain. This inductor provides a bandpass filtering and reduces the parasitic capacitances effect ($C_{gd1}$
and $C_{gs2}$) by forming pi-LC filter. The forward gain with and without $L_C$ is shown in fig. 4.6. Without coupling inductor gain is 9.6dB and bandwidth 5GHz which are lower than with $L_C$ design. But the circuit without $L_C$ ensures higher $S_{11}$ which means input impedance deviates from $Z_{opt}$. As a result NF increases for without $L_C$ design. Input and output matching parameter without $L_C$ is in fig. 4.7 and NF is in fig. 4.8. Output matching parameter is greater than -10dB for the whole band.

Fig. 4.3: Input, $S_{11}$ and Output reflection, $S_{22}$ parameters as a function of frequency

Fig 4.4: Reverse isolation, $S_{12}$ parameter as a function of frequency
Though proposed design performs better, it will require larger chip area than the without \( L_c \) design. The proposed design is unique because no one used chebyshev filter at input and coupling inductor in between main MOS and diode connected MOS.

![Input impedance (real part) as a function of frequency](image1)

**Fig. 4.5:** Input impedance (real part) as a function of frequency

![Forward gain of with and without coupling inductor design as a function of frequency](image2)

**Fig. 4.6:** Forward gain of with and without coupling inductor design as a function of frequency
Fig. 4.7: Input and output reflection parameter without coupling inductor

Fig. 4.8: NF as a function of frequency without $L_c$
Noise should be as low as possible for RF circuit design. To limit the noise contribution, the outer dimension, metal spacing and turns ratio of the inductors were selected to peak Q near operating frequency during simulation. To make the noise figure lower, $Z_{in}$ is compromised between maximum power transfer condition and minimum noise figure condition. Noise contribution from the inductors is optimized by choosing higher Q-factor and cascode MOS is selected as small as possible. Main contribution is by the thermal noise of the circuit. Noise figure (NF) is proportional to the square of the frequency for this proposed design. So, NF for this proposed circuit will be higher than lower operating frequency design. NF and $NF_{min}$ are plotted in the Fig. 4.9. NF is 3.7dB at center frequency and less than 4dB for the entire band of operation. $NF_{min}$ is 3.35dB at center frequency. There is a discrepancy between NF and $NF_{min}$. To coincide NF and $NF_{min}$, $Z_{in}$ needs to be changed from the current value. If we change $Z_{in}$, it will degrade input matching parameter from the current value. For UWB application average NF is a better figure of merit than spot NF. The average NF for this UWB structure is 3.74dB. NF can be improved by using higher $g_m$ of the MOS transistors which will effectively increase the power consumption of the circuit also. Noise factor for $V_{dd} = 1.5V$ is shown in fig. 4.10. $NF_{min}$ is 3.3dB at center frequency. Average NF is 3.68dB. So, increasing supply voltage reduces the NF. NF can also be reduced further by increasing width of the MOS device.

![Noise Factor as a function of frequency (Vdd = 1.2V)](image)

Fig. 4.9: Noise Factor as a function of frequency ($V_{dd} = 1.2V$)
Fig 4.10: Noise factor as a function of frequency ($V_{dd}=1.5V$)

The transducer gain, $G_T$, available gain, $G_A$ and power gain, $G_P$ are shown in the fig. 4.11. All the gain curves demonstrate quasi-flat response within operational band yielding the performance of the proposed LNA. The values of the three plots coincide at the center frequency which indicates good matching for the design.

Fig. 4.11: $G_A$, $G_P$ and $G_T$ as a function of frequency
VSWR1 and VSWR2 are 1.69 and 1.12 respectively at the center frequency and. If VSWR is under 2, antenna match is very good. Input reflection parameter is at minimum at VSWR 1.06 at 16GHz. VSWR1 is under 2 for the whole band of operation.

1-dB compression is the measure of the linearity of LNA. 1dB compression point is used as linearity measure for single tone application. Input and output power relationship is depicted in fig. 4.12. Input referred 1-dB compression point of the LNA is -9.38dBm as indicated in Fig. 4.10 and the LNA delivers -1.14dBm power to a matched load at this point. So, the LNA can handle 115µW without any compression effect. Compression point depends on the voltage headroom of the MOS. In order to increase the compression point, it is needed to increase the supply voltage of the amplifier. But the device is intended to use for mobile communication back-haul or inter-chip wireless communication where the maximum radiation power can be of 50µW. So, this amplifier can work without any compression effect for these applications.

Another linearity parameter is the IIP3 which is useful for multi-tone application. So, in UWB structure IIP3 is more important than 1-dB compression point. Two tone test is performed to
measure third order intercept point at 16GHz where the spacing is 40MHz. So, the third order intermodulation products are at 15.6GHz and 16.8GHz. Input referred third order intercept point was found about -5.013dBm and LNA delivers +2dBm output at this point which is illustrated in fig. 4.13. So, OIP3 is +2dBm and the extrapolation point for this simulation is -25dBm. The upper edge of dynamic range is 316μW.

![Fig. 4.13: Third Order Intercept Point, IP3](image)

The circuit should compress the intermodulation products that mean both second order and third order intercept should be as high as possible. Second order intermodulation was also simulated using two tone test at 16GHz and spacing is 400MHz. The second order products are at 400MHz and 32.4GHz. Input referred second order point is +58dBm which is quite high for LNA design as in fig. 4.14.

To test the linearity of the proposed amplifier over the band of performance, IIP2 & IIP3 are determined for the whole band of interest. As the operating frequency increases, IIP3 & OIP3 both increases because gain decreases. IIP3 & OIP3 at different frequencies are shown in Fig. 4.15. IIP2 is found +57dBm, +73dBm, +61dBm, +57dBm, +55dBm, +56dBm at 17-22 GHz, respectively. In total, the circuit demonstrates better performance in terms of IIP2 and OIP2.
The circuit is simulated to find the linearity parameter at higher supply voltage ($V_{dd}=1.5$V). If the supply voltage is increased to 1.5V, this would result in better IIP3 but higher power consumption. Figure 4.16 shows the linearity performance at 1.5V supply voltage.

**Fig. 4.14:** Input referred second order intercept point, IIP2

**Fig. 4.15:** Variation of IIP3 and OIP3 with frequency
Generally systems are designed to operate at nominal voltage but this voltage varies due to various reasons. This proposed design is simulated for ±10% variation in supply voltage and the effect of this variation in proposed amplifier’s gain is shown in Fig. 4.17. It is evident from the figure that peak gain is almost insensitive to the variation of the supply voltage & maximum variation for supply voltage is about 2%.

The conditional stability factor ($K_f$) is shown in fig. 4.18 for the whole band of interest. $K_f$ has to be greater than 1 for the entire band to ensure stability. If $K_f$ is below 1 then there will be problem in using it. $K_f$ is defined as

$$K_f = \frac{1-|S_{11}|^2-|S_{22}|^2+\Delta^2}{2|S_{12}|}$$

where $\Delta$ is defined as $S_{11}S_{22}-S_{12}S_{21}$.

From the figure it is visible that $K_f$ is greater than 1 for the entire band. So the LNA is not prone to oscillate due to white noise which may be present in the circuit during power up.
Fig. 4.17: Peak gain as a function of supply voltage

Fig. 4.18: Conditional stability factor, $K_f$, as a function of frequency
Different performance parameters for all process corners are simulated for the proposed circuit. The collective effects of process and environmental variation can be lumped into their effect on transistors: (called Slow, Fast or Typical). Fig. 4.19 shows the forward gain at different process corners. As there are only NFET in the design, so FF and FS corners results are same. On the same way SF and SS are same. For SS and SF condition center frequency shifted a small portion in the direction of lower frequency. Gain is almost same for all process corners. For slow n-MOS transistor, threshold voltage is higher and for faster n-MOS threshold voltage is lower. As a result transconductance, \( g_m \) is higher for Fast n-MOS and lower for slow n-MOS. Forward gain will be around 10dB and BW will be around 6GHz irrespective of the process variation.

Input matching parameter, \( S_{11} \) for all the extreme corners is illustrated in fig. 4.20. For all the corners point \( S_{11} \) is less than -10dB in the operating band. FF and FS shows better input matching than SS and SF. But SS and SF shows better input matching at lower edge of the band. But the major goal is to make \( S_{11} \) less than -10dB for irrespective of the process variation, which is achieved in the proposed circuit.

![Forward Gain, \( S_{21} \) at different process corners as a function of frequency](image)

**Fig. 4.19:** Forward gain, \( S_{21} \) at different process corners as a function of frequency
NF is proportional to the square of the operating frequency and inversely proportional to $g_m$. SS and SF yields the same results as the proposed circuit contains only n-MOS transistor. SS corner has higher NF than FF corner simulation as in fig. 4.21. But still the NF is below 4.5dB for the designed circuit which is quite low for high frequency LNA circuit. So, NF can be as low as 3.2dB and as high as 4.5dB in the operating band.

This circuit is also simulated to find the response at extreme case of corner points. Means SS process corner is combined with minimum temperature (-55°C, military application) and maximum temperature (85°C, industrial application). At lower temperature drain current will be higher than normal room temperature condition because at low temperature scattering will be very low. Thermal noise contribution is negligible at -55°C. Due to higher drain current, forward gain is found to be 12dB at center frequency shown in fig. 4.22. The performance for FF corner combining with highest commercial application temperature is tabulated in Table 4-I. At high temperature transconductance will be decreased and gain will be lower than 10dB.
Fig. 4.21: NF as a function of frequency at different process corners

Fig. 4.22: Performance of LNA for SS process corner at -55°C
Table 4-I

Performance of LNA at FF corner for 85°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward gain, $S_{21}$</td>
<td>8.5dB</td>
</tr>
<tr>
<td>Input reflection, $S_{11}$</td>
<td>-20dB (&lt;-10dB for whole band)</td>
</tr>
<tr>
<td>NF</td>
<td>4.47dB (5.5dB-4.17dB)</td>
</tr>
<tr>
<td>$N_{F_{min}}$</td>
<td>4dB</td>
</tr>
</tbody>
</table>

The linearity of the amplifier at this extreme case of FF process corner is illustrated in fig. 4.23. The ICP and IIP3 are -11.5dBm and -6dBm respectively at this condition. The extrapolation point is -25dBm. So, LNA can handle 70µW for single tone application and 250 µW for multi-tone application. Simulation is also done to find out the linearity of the LNA at -55°C. ICP and

![Fig. 4.23: Linearity at 85°C for FF corner](image-url)
IP3 both are shown in fig. 4.24. Here the simulation is done at 17.5GHz and spacing between the tone is 50MHz. So the 3rd order intermodulation products are 17.6GHz and 17.45GHz. ICP and IIP3 both at this extreme case are -15dBm and -8.65dBm respectively.

The target applications of the proposed amplifier are mobile communication, satellite application and on chip wireless communication where the temperature can be as high as 100°C. So, the LNA performance needs to be satisfactory at this temperature. The considered transistors are typical which mean no process variation. The forward gain is in between 8dB~6dB in the operating band as shown in fig. 4.25 which is acceptable at such a high temperature. Thermal noise is the main contributor of NF. Thermal noise is proportional to the temperature. So, it would be definitely higher than room temperature NF. The NF at room temperature and 100°C is shown in fig. 4.26. But it is still less than 5dB for the whole band of operation.

![Graph showing linearity at SS corner for -55°C](image)

**Fig. 4.24**: Linearity at SS corner for -55°C
Fig. 4.25: $S_{21}$ and $S_{11}$ at 100°C for typical MOS transistor

Fig. 4.26: NF @room temperature and @ 100°C
The fig. 4.27 depicts the time domain response of the proposed LNA to a series of UWB pulses. From the output, it can easily be realized that for both positive and negative Gaussian monocycle pulses, the LNA produces distinct response.

The major concern of recent LNA design is power consumption. The proposed circuit is a low power design as it consumes less amount of power including its bias circuitry. This LNA consumes 10.91mW power including bias circuit when powered up by 1.2V supply.

![Time domain response of the LNA](image)

Fig. 4.27: Time domain response of the LNA

The performance of the designed LNA is illustrated in Table 4-II. The comparison of this work with other published works is given in Table 4-III in section 4.3.
### Table 4-II Tabulated response of the LNA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>IBM 130nm CMOS</td>
</tr>
<tr>
<td>Forward gain, $S_{21}$</td>
<td>10.1 dB</td>
</tr>
<tr>
<td>Input matching parameter, $S_{11}$</td>
<td>$&lt;-12$ dB</td>
</tr>
<tr>
<td>Output matching parameter, $S_{22}$</td>
<td>$&lt;-10$ dB</td>
</tr>
<tr>
<td>Reverse isolation, $S_{12}$</td>
<td>$&lt;-20$ dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>6.2GHz (15.2-21.6GHz)</td>
</tr>
<tr>
<td>NF average</td>
<td>3.74 dB</td>
</tr>
<tr>
<td>NF$_{\min}$</td>
<td>3.36dB</td>
</tr>
<tr>
<td>Input impedance</td>
<td>50$\Omega$ @ 15.8GHz and 17.8GHz</td>
</tr>
<tr>
<td></td>
<td>Remain 40-60 Ohm in the band</td>
</tr>
<tr>
<td>Output impedance</td>
<td>50$\Omega$ @ center frequency</td>
</tr>
<tr>
<td>ICP @ center frequency</td>
<td>-9.38dB</td>
</tr>
<tr>
<td>IIP3</td>
<td>-5.013dB</td>
</tr>
<tr>
<td>OIP3</td>
<td>+2dBm</td>
</tr>
<tr>
<td>$P_{\text{diss}}$</td>
<td>10.91mW</td>
</tr>
<tr>
<td>Conditional Stability Factor, $K_f$</td>
<td>$&gt;1.2$</td>
</tr>
</tbody>
</table>

### 4.3 Comparison With Other Published UWB LNAs

The performance of the proposed LNA is compared with some published results in Table 4-III. 3-10 GHz band LNAs in [37], and [6] has higher noise figure 4.6dB and 5.3dB where the designed LNA shows average NF below 3.8dB. [37] and [6] both have lower power consumption but linearity ICP and IIP3 of those circuits are less than -18dBm and -8dBm. The circuit proposed here consumes 10.91mW and have a very good linearity of -9.38dBm ICP and -5dBm IIP3. [53] and [54] designed in the 3GHz band and have a lower average noise figure than proposed circuit. But these designs [53] and [54] have lower BW (less than 2GHz), higher power consumption and poor input-output matching than the designed circuit. [55] and [56] are designed for higher operating frequency (Ku-Band and K-Band), but these circuits have very
high power consumption, higher noise figure and less forward gain compared to the circuit proposed here. Designed circuits bandwidth (6.4GHz) is comparable to the lower frequency designs [37], [6], and [56] but it is higher than K-band LNA (6GHz) [55]. Operating frequency FOM (Figure of Merit) defined as $S_{21} (dB) * f(GHz) / P(mW) * NF$ of this work is 4.36 which is higher than [6] and [53-56]. Circuit of [19] has higher FOM but it uses more inductors than this design so the chip area requirement is higher for [19].
Table 4-III

Comparison of this work with Other UWB LNAs

<table>
<thead>
<tr>
<th>Specification</th>
<th>This Work</th>
<th>[37]</th>
<th>[53]</th>
<th>[54]</th>
<th>[6]</th>
<th>[55]</th>
<th>[56]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
<td>Simulated</td>
<td>Simulated</td>
<td>Simulated</td>
<td>Simulated</td>
<td>Measured</td>
<td>Measured</td>
<td>Measured</td>
</tr>
<tr>
<td>CMOS Process(µm)</td>
<td>0.13</td>
<td>0.18</td>
<td>0.18</td>
<td>0.13</td>
<td>0.18</td>
<td>0.18</td>
<td>0.13, SiGe</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1.2</td>
<td>0.6</td>
<td>0.9</td>
<td>1.5</td>
<td>1.8</td>
<td>1.8</td>
<td>2.2</td>
</tr>
<tr>
<td>BW (GHz)</td>
<td>6.4</td>
<td>7</td>
<td>2</td>
<td>1.3</td>
<td>7.1</td>
<td>6</td>
<td>10</td>
</tr>
<tr>
<td>$S_{21}$(dB)</td>
<td>10.1</td>
<td>14.6</td>
<td>16</td>
<td>12</td>
<td>10.4</td>
<td>9.3</td>
<td>20</td>
</tr>
<tr>
<td>$S_{11}$(dB)</td>
<td>-11~-30</td>
<td>-9.6</td>
<td>&lt;5</td>
<td>&lt;8.5</td>
<td>&lt;9.4</td>
<td>-13~-20</td>
<td>&lt;8.5</td>
</tr>
<tr>
<td>$S_{22}$(dB)</td>
<td>-25</td>
<td>-10</td>
<td>&gt;-8</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>$NF_{ave}$ (dB)</td>
<td>3.74</td>
<td>4.6</td>
<td>3.2</td>
<td>2.2</td>
<td>5.3</td>
<td>5.5</td>
<td>7.2</td>
</tr>
<tr>
<td>ICP (dBm)</td>
<td>-9.38</td>
<td>&lt;20</td>
<td>&lt;15</td>
<td>N/A</td>
<td>-18</td>
<td>-14</td>
<td>N/A</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>-5.013</td>
<td>-13.19</td>
<td>-4</td>
<td>16</td>
<td>-8.8</td>
<td>-4</td>
<td>N/A</td>
</tr>
<tr>
<td>$P_{diss}$(mW)</td>
<td>10.91</td>
<td>3.1</td>
<td>13</td>
<td>17.4</td>
<td>9</td>
<td>27</td>
<td>180</td>
</tr>
<tr>
<td>Stage</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Operating Range(GHz)</td>
<td>15.2-21.6</td>
<td>3.1-10.6</td>
<td>3-5</td>
<td>0.8-2.1</td>
<td>2.1-9.5</td>
<td>21-27</td>
<td>8-18</td>
</tr>
<tr>
<td>FOM</td>
<td>4.36</td>
<td>5.11</td>
<td>2.34</td>
<td>0.47</td>
<td>1.22</td>
<td>1.96</td>
<td>0.216</td>
</tr>
</tbody>
</table>
CHAPTER SIX

CONCLUSION

6.1 CONCLUSION

Design and analysis of a UWB LNA have been demonstrated in this work. The simulated response of the proposed design is also demonstrated in the result section. Circuit analysis of input matching, output matching, voltage gain analysis and noise figure analysis is shown in this work. The performance of the LNA found satisfactory for UWB communication. To test the performance of the designed amplifier under different process variations, the circuit is simulated for all the process corners at worst case condition. The results found input matching below -10dB for whole band of interest, forward gain around 10dB, -3dB bandwidth above 6.2GHz and average noise figure in between 2.5dB~3.9dB for all process corner point simulation. The simulation results show that compared to other LNA this design has the advantages of less complexity, low power dissipation (10.91mW), lower noise figure (3.74dB), higher linearity (-9.38dBm) and higher operating frequency (15.2-21.6GHz). The proposed LNA architecture is suitable for low power; low noise and high frequency UWB applications like satellite TV, mobile communication, fixed satellite etc.

6.2 SCOPE FOR FUTURE WORK

The designed amplifiers schematic is simulated in Cadence Spectre and Hspice RF using IBM 0.13µm CMOS process. But to include the parasitic of the components placement and all other parasitic capacitance of routing, parasitic extraction has to be done. To do this, layout design and simulation of layout should be done. But layout design was not the scope of this thesis work. To consider the fabrication of the designed amplifier, the circuit designs are need to be optimized up to post layout simulation level and the architecture is yet to be evaluated in terms of parasitic extraction.

The topology which is adopted in this work can be used to design UWB LNA for operating frequency greater than 25GHz by changing the parameters values. The average noise figure will be very low as SNIM technique is adopted for this design.
The next stages of the receiver like mixer, delay element, ADC can be designed and this LNA circuit can be incorporated to design a whole receiver circuit in one chip.
REFERENCES

http://techon.nikkeibp.co.jp/articleINews/2005052611051241

http://www.motc.gov.tw/motchypage/deptl782/1485_chapter6-MHz.html


APPENDIX A

Noise figure calculation of an inductively degenerated MOS

Thevenin equivalent noise voltage and noise current, (Noise model shown in Noise calculation section of chapter three)

\[ i_n = i_{ng} + \frac{i_{nd}}{g_m} sC_{gs} \]

\[ e_n = \frac{i_{nd}}{g_m} + sL_s i_n \]

\( i_{ng} \) is the gate induced noise current, \( i_{nd} \) is the drain induced noise current.

Spectral density of the noise current, \( S_{in} = 4KT \frac{\delta \omega C_{gs}^2}{5g_{d0}} \), \( S_{ind} = 4KT \frac{\gamma g_{d0}}{2} \)

\[ S_{in} = \left( i_{ng} + \frac{j \omega C_{gs}}{g_m} i_{nd} \right) \left( i_{ng}^* - \frac{j \omega C_{gs}}{g_m} i_{nd}^* \right) \]

\[ = i_{ng}^2 + \frac{\omega C_{gs}^2}{g_m^2} i_{nd}^2 + \frac{2j \omega C_{gs}}{g_m} \left( i_{ng} i_{nd}^* + i_{ng}^* i_{nd} \right) \]

\[ = 4KT \left( \frac{\delta \omega C_{gs}^2}{5g_{d0}} + \frac{\omega C_{gs}^2}{g_m^2} \frac{\gamma g_{d0}}{2} + \frac{2\omega C_{gs}}{g_m} \frac{\gamma g_{d0}}{2} \right) \]

\[ G_n = \frac{1}{R_n} = \frac{\gamma^2}{4KT} = \frac{\omega^2 C_{gs}^2}{\alpha^2 g_{d0}} \frac{1 + \alpha^2 \chi^2 + 2|\chi|\alpha\chi}{\gamma} \]

Here, \( \alpha = \frac{g_m}{g_{d0}} \), \( \chi = \sqrt{\frac{\delta}{5\gamma}} \), \( \delta, \gamma \) process parameter, \( g_{d0} \) is the zero drain voltage trans-conductance, \( c \) is the coupling co-efficient.

\[ Z_c = \frac{i_{nd}^* i_n}{g_m} = 4KT \left( \frac{j \omega C_{gs}}{g_m} \sqrt{\frac{\delta}{5}} + \frac{j \omega C_{gs}}{g_m} g_{d0} \right) \]

\[ Z_c = -jX_c \]
The input noise current can be divided into two components. One is correlated component and another one is uncorrelated component.

\[
\overline{i_n^2} = \overline{i_c^2} + \overline{i_u^2} = \overline{i_n^2} |c|^2 + \overline{i_n^2} (1-|c|^2)
\]

Resistance due to uncorrelated noise current-

\[
R_u = \frac{\overline{i_n^2} (1-|c|^2)}{4KT} = \frac{\alpha^2\chi^2 (1-|c|^2)}{a^2 g_d (1+a^2 \chi^2 + 2 |c|\alpha \chi)}
\]

\[
R_{opt} = \sqrt{\frac{R_u}{G_n}} + R_c = \sqrt{\frac{R_u}{G_n}} [R_c = 0, X_{opt} = X_c]
\]

Overall noise figure-

\[
F = 1 + \frac{R_u + |Z_c + Z_s|^2 G_n}{R_s} = 1 + \frac{R_u + |X_c + R_s + X_s|^2}{R_s} = 1 + \frac{R_u}{R_s} + R_s G_n \quad \text{[Minimum noise figure when } X_c = X_s]\]

\[
= 1 + \frac{\gamma}{\alpha} \frac{1}{g_m R_s} \left( \frac{\alpha^2 \chi^2 (1-|c|^2)}{1+a^2 \chi^2 + 2 |c|\alpha \chi} \right) + \omega^2 C_{gs}^2 R_s^2 \left( 1+a^2 \chi^2 + 2 |c|\alpha \chi \right)
\]
APPENDIX B

HSPICE CODES

Code for s-parameter simulation

.options post=2
.options tnom=25
.LIB 'skew.file' stats
.INCLUDE 'nfet.inc'
.INCLUDE 'fixed_corner'
.INCLUDE 'hspice.param'
.INCLUDE 'oprrpres.inc'
.include 'ind.inc'
.include 'indstack.inc'
.include 'mimcap.inc'
*.param l1=0.05p
.param gnd=0 w1=30u g11=8

Xmnt n4 n5 n6 n6 nfet l=130.0n w=180.00000u nf=1 m=1 par=1
   +ngcon=1 ad=9.9e-11 as=9.9e-11 pd=361.1u ps=361.1u nrd=0.0011
   +nrs=0.0011 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1
   +lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p
   +panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
   +sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0 *200u

Xmnd nd nvdd nc nc nfet l=130.0n w=170.00000u nf=1 m=1 par=1
+ngcon=1  ad=9.35e-11  as=9.35e-11  pd=341.1u  ps=341.1u  nrd=0.0012
+nrs=0.0012  rf_rsub=1  plnest=-1  plorient=-1  pld200=-1  pwd100=-1
+lstis=1  lnows=0  rgatemod=0  rbodymod=0  panw1=0p  panw2=0p  panw3=0p
+panw4=0p  panw5=0p  panw6=0p  panw7=0p  panw8=0p  panw9=0p  panw10=0p
+sa=5.5e-07  sb=5.5e-07  sd=0u  dtemp=0  *150

xll1  n2  n5  gnd  ind  x=100u  w=17.0u  wu=15.0u  s=5u  n=1  bp=2  tlev1=3  tlev2=2  dtemp=0
xll2  n2  n5  gnd  ind  x=100.00000u  w=17.0u  wu=15.0u  s=5u  n=1  bp=2  tlev1=3  tlev2=2  dtemp=0
xll3  n2  n5  gnd  ind  x=100.00000u  w=17.0u  wu=15.0u  s=5u  n=1  bp=2  tlev1=4  tlev2=1  dtemp=0
xllp  n2  nbias  gnd  ind  x=120.00000u  w=13.0u  wu=15.0u  s=5u  n=1  bp=2  tlev1=4  tlev2=1  dtemp=0
xllg  nin  n1  gnd  ind  x=120.00000u  w=15.0u  wu=15.0u  s=5u  n=1.25  bp=2  tlev1=3  tlev2=2  dtemp=0
xlls  n6  0  gnd  ind  x=120.00000u  w=16.0u  wu=15.0u  s=5u  n=1.5  bp=2  tlev1=3  tlev2=2  dtemp=0
xllc  n4  nc  gnd  ind  x=110.00000u  w=16.0u  wu=15.0u  s=5u  n=1.5  bp=2  tlev1=3  tlev2=2  dtemp=0

Xcc1  n1  n2  0  mimcap  l=8.5u  w=15.8u  c=282.9452f  m=1  par=1  est=1  tlev1=3  tlev2=2  bp=3  setind=-2  rsx=50  dtemp=0
Xccp  n2  nbias  0  mimcap  l=7u  w=5.31u  c=80.06384f  m=1  par=1  est=1  tlev1=3  tlev2=2  bp=3  setind=-2  rsx=50  dtemp=0
Xcco  nd  nout  0  mimcap  l=7u  w=5.31u  c=80.06384f  m=1  par=1  est=1  tlev1=3  tlev2=2  bp=3  setind=-2  rsx=50  dtemp=0
Code for power calculation

A single stage LNA

Code for power calculation

A single stage LNA
.INCLUDE 'hspice.param'

.include 'ind.inc'

.include 'indstack.inc'

.include 'mimcap.inc'

.param gnd=0  w1=30u  g11=8

.Xmnt  n4  n5  n6  n6 nfet l=130.0n  w=150.00000u  nf=1  m=1  par=1
  +ngcon=1  ad=9.9e-11  as=9.9e-11  pd=361.1u  ps=361.1u  nrd=0.0011
  +nrs=0.0011  rf_rsub=1  phnest=-1  plorient=-1  pld200=-1  pwd100=-1
  +lstis=1  lnws=0  rgatemod=0  rbodymod=0  panw1=0p  panw2=0p  panw3=0p
  +panw4=0p  panw5=0p  panw6=0p  panw7=0p  panw8=0p  panw9=0p  panw10=0p
  +sa=5.5e-07  sb=5.5e-07  sd=0u  dtemp=0  *200u

.Xmnd  nd  nvdd  nc  nc  nfet l=130.0n  w=125.00000u  nf=1  m=1  par=1
  +ngcon=1  ad=9.35e-11  as=9.35e-11  pd=341.1u  ps=341.1u  nrd=0.0012
  +nrs=0.0012  rf_rsub=1  phnest=-1  plorient=-1  pld200=-1  pwd100=-1
  +lstis=1  lnws=0  rgatemod=0  rbodymod=0  panw1=0p  panw2=0p  panw3=0p
  +panw4=0p  panw5=0p  panw6=0p  panw7=0p  panw8=0p  panw9=0p  panw10=0p
  +sa=5.5e-07  sb=5.5e-07  sd=0u  dtemp=0  *150

.xll1  n2  n5  gnd  ind  x=110.00000u  w=17.0u  wu=15.0u  s=5u  n=1  bp=2  tlev1=3  tlev2=2  dtemp=0

.xll2  n2  n5  gnd  ind  x=110.00000u  w=17.0u  wu=15.0u  s=5u  n=1  bp=2  tlev1=3  tlev2=2  dtemp=0

.xll3  n2  n5  gnd  ind  x=120.00000u  w=13.0u  wu=15.0u  s=5u  n=1  bp=2  tlev1=4  tlev2=1  dtemp=0

.xllp  n2  nbias  gnd  ind  x=120.00000u  w=13.0u  wu=15.0u  s=5u  n=1  bp=2  tlev1=4  tlev2=1  dtemp=0
xllg n1 n2 gnd
  ind x=100.0000u w=15.0u s=5u n=1.25 bp=2
dtemp=0
dtemp=0

xlls n6 0 gnd
  ind x=120.00000u w=16.0u s=5u n=1.25 bp=2
dtemp=0
dtemp=0

xld nd nvd gnd
  ind x=200.0000u w=25.0u s=5u n=1.5 bp=2
dtemp=0
dtemp=0

xlc n4 nc gnd
  ind x=110.00000u w=10u s=5u n=1.5 bp=2
dtemp=0
dtemp=0

Xcc1 n1 n2 0 mimcap
  l=8.5u w=15.8u c=282.9452f m=1 par=1 est=1
tlev1=3 tlev2=2
bp=3 setind=-2 rsx=50
dtemp=0

Xccp n2 nbias 0 mimcap
  l=7u w=5.31u c=80.06384f m=1 par=1 est=1
tlev1=3 tlev2=2
bp=3 setind=-2 rsx=50
dtemp=0

Xcco nd nout 0 mimcap
  l=7u w=5.31u c=80.06384f m=1 par=1 est=1
tlev1=3 tlev2=2
setind=-2 rsx=50
dtemp=0

rrout nout 0 100000

rrd nvd nvdd g11

rd nbias nvdd 20000

Xmn2 nbias nbias 0 0 nfet
  l=50u w=30u nf=1 m=1 par=1 ngcon=1
  ad=1.65e-11
  +as=1.65e-11
  +pd=61.1u ps=61.1u nr=0.0073
  +rs=0.0073 rf_rsub=1
  +plnest=-1 plorient=-1 pld200=-1 pwd100=-1
  +lstis=1 lnws=0
  +rgatemod=0 rbbodymod=0
  +panw1=0 panw2=0 panw3=0 panw4=0 panw5=0
  +panw6=0 panw7=0 panw8=0 panw9=0 panw10=0
  +sa=5.5e-07
  +sb=5.5e-07 sd=0u dtemp=0
  *40u

vdd nvdd 0 1.2

vin nin 0 dc 0 ac 1m sin (0 15m 17.56g 0 0)
.ac lin 1000 12g 23g *sweep g11 2122
.ac lin 1000 12g 23g *sweep g11 2122

.end