Modeling of Subthreshold Characteristics of Non-Planar Multi-Gate InGaAs Quantum Well Field Effect Transistor

by

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Signature of the Candidate

____

Urmita Sikder

Dedication

To my mom.

Acknowledgment

First of all, I would like to thank God for giving me the strength to complete this thesis.

This thesis would not be possible without the help and support of a number of people to whom I am very grateful. I want to thank my supervisor, Prof. Quazi Deen Mohd Khosru for his continuous guidance and support. Whenever I faced problems and did not know how to proceed, he pointed me to the right direction. I am grateful to him for his kind words and encouragement.

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ABSTRACT

In this work, a physically based analytical model for the threshold voltage and subthreshold swing of non-planar trigate InGaAs quantum well field effect transistor (QWFET) has been developed. The model is derived from the analytical solution of the 3D Poisson's equation including the electron concentrations. Based on the subthreshold electrostatic potential obtained from the solution of the Poisson's equation, the threshold voltage and the subthreshold swing are obtained by considering the changes at the top of the barrier at the leakiest channel path. The results from the proposed model are compared to the results from numerical simulator (NEGF mode-space solver) for a wide range of gate length and lateral dimensions of the channel; hence good agreement between the analytical model and the numerical model is observed. Applying the developed model, the sensitivities of threshold voltage and subthreshold swing to channel length, fin height, fin width and donor layer thickness are investigated. The subthreshold characteristics of the planar single-gate and double-gate QWFET devices are also modeled; and they are compared to the non-planar trigate QWFET in terms of performance. The non-planar structure is found to provide better subthreshold swing and stronger enhancement mode operation than its planar counterpart. Short-channel effects of the trigate QWFET can be reasonably controlled by reducing either the fin height or fin width. The aggressively scaled non-planar trigate QWFET proves to be the better option for short channel operation.

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CHAPTER 1
INTRODUCTION

1.1 Preface

For the last five decades, the semiconductor industry has been characterized by the improvement trends in terms of integration level, cost, speed, power, compactness and functionality. Most of these trends are the direct outcome of exponential decrease in the minimum feature sizes used to fabricate integrated circuits through aggressive scaling trend. Due to the rapid advancement of the semiconductor device fabrication technology, devices have approached the deep submicron regime. In order to control the gate leakage through ultra-scaled gate oxide layer, high- κ gate stacks are explored for silicon CMOS technology. Threshold-voltage tuning and control high- κ gate stacks have proven to be challenging, especially for low-threshold-voltages as the supply voltage continues to go down. New device architecture such as multiple-gate MOSFETs (e.g., FinFETs) and ultra-thin body FD-SOI are being explored to overcome this challenge. To attain adequate drive current for the highly scaled MOSFETs, materials with light effective masses are greatly beneficial in quasi-ballistic operation with enhanced thermal velocity and injection at the source end.

III-V materials provide an attractive option for continuing transistor scaling according to the Moore's Law because of their high mobility, although growing high quality oxides on III-V materials are posing a difficult challenge. High-κ metal gate dielectric with low interface trap density (DIT), low bulk traps and leakage, unpinned Fermi level and low ohmic contact resistances are major challenges too. III-V Materials providing high mobility for both electrons and holes are also being researched. Moreover, the integration of high-mobility materials in the well developed Silicon CMOS technology is another important issue. According to International Technology Roadmap for Semiconductors (ITRS) 2013 Edition, in 2021-2028 the transistor gate length is projected to scale below 10 nm and ultra-thin body multi-gate MOSFETs with lightly doped channels are expected to be utilized to effectively scale the device and control short-channel effects [1].

As Si CMOS technology approaches the end of ITRS roadmap, high mobility channel materials, such as germanium and III-V materials have been considered as or replacement for Si channel for CMOS logic applications [2]-[4]. The experimental research focused on various high-mobility materials as candidates for high-speed low-power nanoscale devices is extremely vast. Germanium has emerged as a promising material for high mobility channels, especially for p-MOSFETS [5]-[6]. High mobility compound semiconductor materials, such as InGaAs, InAlAs, InAs, InSb and GaAs exhibit excellent transport properties, therefore they have much potential for being used in high-speed and high-frequency systems [4],[8]. Among these materials, InAs and InGaAs have attracted much attention recently [9]-[18]. InGaAs is a very promising candidate for future high electron mobility devices because it allows for a very good tradeoff between the excellent transport properties of InAs and the low leakage of GaAs [19]-[20].

As the device dimensions are scaled, the gate leakage for Schottky gated HEMT and QWFET devices becomes particularly dominant. High-κ gate dielectric material is a solution to solve the problem of high gate leakage current, since the gate leakage current density corresponding to a given EOT is much smaller for high-κ than for conventional oxy-nitride gate dielectric. The tunneling current through the gate is found to be significantly reduced with the inclusion of a high-κ dielectric below the gate [21]. Integration of high-mobility materials with high-κ dielectric has recently emerged as a leading candidate for next-generation technology on and beyond 16nm node. Al_2O_3 gate oxides grown via Atomic Layer Deposition (ALD) is the most promising gate dielectric for InGaAs devices and this technique is widely used in InGaAs MOSFETs, FinFETs and Gate-All-Around nanowire transistors [22]-[29]. In the recents years, the non-planar device technology has been implemented for InGaAs QWFET devices with undoped channel [30]-[31]. This device aims to combine the superior gate control of the non-planar technology with the high electron mobility in modulation doped InGaAs channel and the reduced gate leakage through Al_2O_3 gate dielectric. As continuous scaling has brought Si CMOS technology into its fundamental limits, the non-planar InGaAs QWFET is one of the most promising candidates for continuing the historic progress in semiconductor industry.

1.2 Literature Review

In recent years, a number of research works have focused on prediction of performance for small dimension QWFET devices in order to guide experimentalists in the process of scaling the device dimensions [32]-[36]. These simulation based studies demonstrate nearly ballistic operation in short-gate length devices. Moreover, the non-planar multi-gate device is found to provide better enhancement mode operation and higher mobility and drive current than their planar counterpart [32].

Analytical modeling of hetero-junction devices has received considerable attention in literature as they provide fast computation and physical insights into the device operation. Models for planar HEMT devices have been developed using a variety of approaches. Sheet carrier based models [37]-[38] and physics based compact models [39]-[40] of long channel HEMT devices have shown good consistency with experimental results. Gupta et. al. have developed several HEMT models taking into account short channel effects [41]-[42]. Multi-gate HEMT structure models have also been developed [42]-[43].

Analytical models have also been developed for undoped FinFET devices. Three dimensional analytical models of FinFET structures have been reported in literature [44]-[46]. The non-planar structure of multi-gate FinFET requires solution of 3D Poisson's equation. Such models accurately describe the subthreshold characteristics of the devices.

A considerable amount of experimental works have been focused on QWFET devices. Experiments have shown that QWFETs demonstrate improved electrostatic characteristics [12] as well as improved high frequency characteristics [15]. Multi-gate non-planar QWFET structure allows better enhanced mode operations. Despite large number of reported experimental works, to the best of our knowledge, analytic modeling of non-planar QWFET has not been reported in literature yet. This work takes the modeling techniques used in HEMT and SOI FinFET devices to model the QWFET device.

1.3 Thesis Objectives

In the recent years, the non-planar structure of QWFET devices has gained attention due to improved electrostatics and superior performance. Although a large number of research work have been focused on the analytical modeling of subthreshold characteristics of undoped non-planar SOI devices, no such model has been reported yet for the non-planar QWFET devices. Hence this work aims to introduce an analytic model for the subthreshold characteristics of non-planar trigate InGaAs Quantum Well FET with Al_2O_3 gate dielectric. The primary objectives of this thesis are:

- Modeling 3D electrostatics of the non-planar QWFET in the subthreshold and near-threshold regime
- Introducing a threshold voltage model using the potential distribution of the QWFET
- Developing a subthreshold swing model considering the effective conduction path
- Comparing low dimension non-planar and planar structures in terms of subthreshold swing, threshold voltage and drain induced barrier lowering
- Analyzing the effects of various devices parameters on the subthreshold characteristics

1.4 Thesis Organization

Chapter 1 contains an introductory discussion on the recent trends in semiconductor industry and the background of research on III-V QWFET devices. It also describes the motivation behind this work and the objectives of this thesis. The thesis is also outlines in this chapter.

Chapter 2 provides a description of the structures of QWFET devices used in this work with illustrations. Chapter 3 describes the analytical approach used in this works to extract the subthreshold characteristics of a device. The potential distribution of different types of QWFET structures, i.e. single-gate, double-gate and tri-gate are modeled in this chapter. Using the modeled potential distribution in Chapter 3, a threshold voltage model

and a subthreshold swing model are developed in Chapter 4. In Chapter 5 the planar and non-planar structures are compared according to their subthreshold performance. The threshold voltage, subthreshold swing and drain induced barrier lowering effect is observed for several structures and comparisons are made. The effect of changing indium concentration in the InGaAs channel is also discussed. Chapter 6 draws the conclusion to this work. It provides the summary of the significant results and observations. The scope of future work is also discussed in this chapter.

CHAPTER 2
DEVICE DESCRIPTION

2.1 Introduction

The device under investigation is a high-mobility III-V quantum well Field Effect Transistor (QWFET) with high high-κ gate dielectric. This QWFET device has an undoped InGaAs channel between InAlAs barriers and Al_2O_3 as gate dielectric. Both the planar and non-planar varieties of the QWFET structure have been studied in this work.

2.2 Planar QWFET

Two types of planar structures are studied in this work:

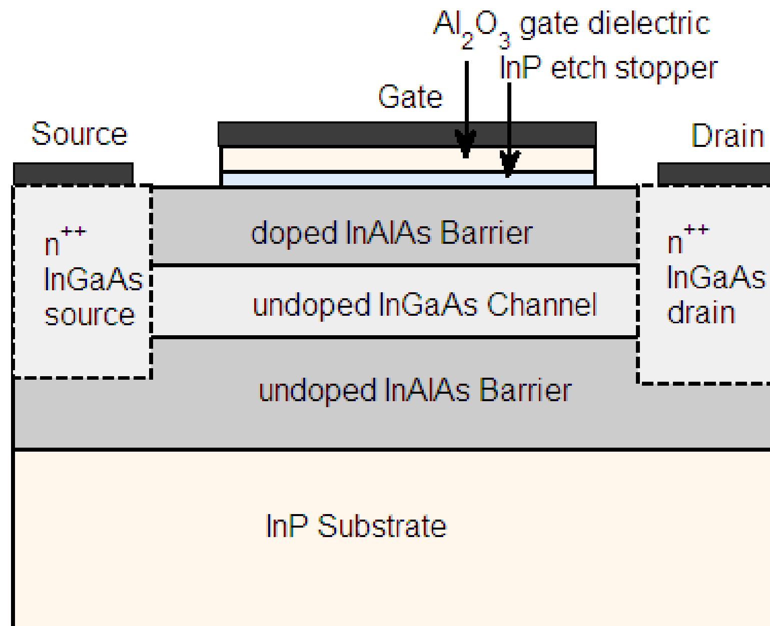
i) Single-gate QWFET

ii) Symmetric Double Gate QWFET

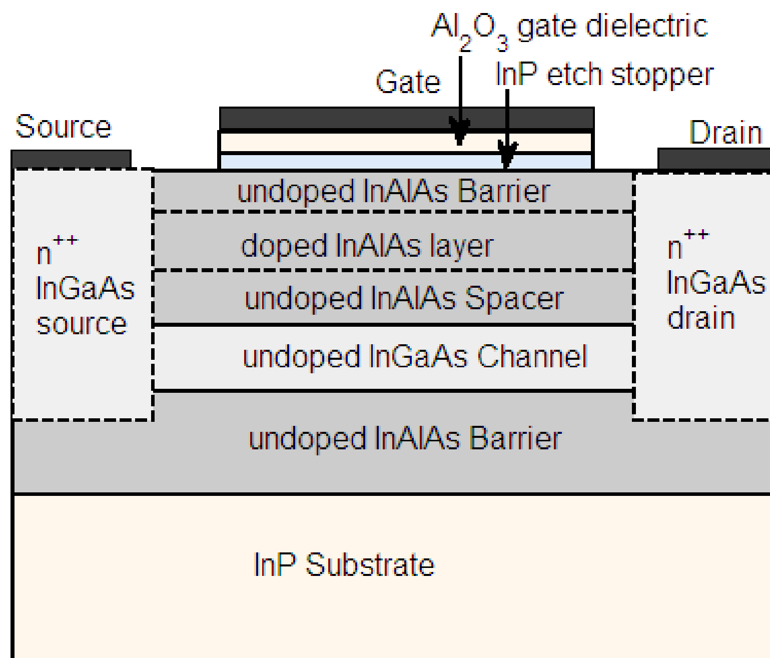
2.2.1 Single-gate QWFET

The planar single-gate device has an undoped InGaAs quantum well as the channel region, while the barriers are composed of InAlAs. A 5nm Al_2O_3 layer is grown by atomic layer deposition (ALD) to act as the gate dielectric, which helps to reduce the gate leakage current of the device. An InP layer of 1nm thickness is used as the etch-stopper layer. The InAlAs layer between the gate dielectric and the channel acts as the upper barrier. The channel layer is modulation doped via the doping of the upper barrier layer. The channel carriers are thus spatially separated from the doped region which results in higher mobility since the channel carriers do not experience any ionized impurity scattering. The barrier is either uniformly doped or pulse-doped to supply conduction electrons to the channel. In case of uniform doping, the channel electrons at the channel-barrier hetero-junction face some scattering due to the ionized impurities at the channel surface. The pulse-doped structure has an InAlAs spacer layer between the doped layer and the channel that prevents the impurity scattering at the channel surface. The upper and lower barriers are made of wide-bandgap InAlAs, confining the electrons in the quantum well created in the InGaAs region. A cross-section of the planar QWFET with

uniform doping is schematically shown in Figure 2.1(a) while a similar structure with pulsed doping is shown in Figure 2.1 (b).



(a)



(b)

Figure 2.1: InGaAs/InAlAs QWFET with (a) uniform doping and (b) pulsed doping

2.2.2 Symmetric double gate QWFET

The Symmetric Double Gate QWFET has the undoped InGaAs channel layer sandwiched between two exactly similar layers of InAlAs barriers.

The carriers in the channel layer are controlled by the gate bias applied through the Al_2O_3 gate dielectric, InP etch stopper and InAlAs barrier. In the device structure shown in Figure 2.2, the InAlAs barrier is pulse-doped to supply conduction electrons to the channel.

The study on the QWFET structure is done for both $In_{0.53}Ga_{0.47}As$ and $In_{0.75}Ga_{0.25}As$ channels epitaxially grown on an InP substrate. $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ layers are lattice-matched to the InP substrate. However, $In_{0.75}Ga_{0.25}As$ has a different (larger) lattice constant than the substrate and barrier layers, which gives rise to a biaxial compressive strain in the $In_{0.75}Ga_{0.25}As$ channel region. Biaxial compressive strain induced in the $In_{0.75}Ga_{0.25}As$ channel shrinks the in-plane lattice dimensions to take the lattice constant of the substrate while the perpendicular lattice dimension grows. Such biaxial compressive strain alters the band gap and effective mass of electrons of the $In_{0.75}Ga_{0.25}As$ QW.

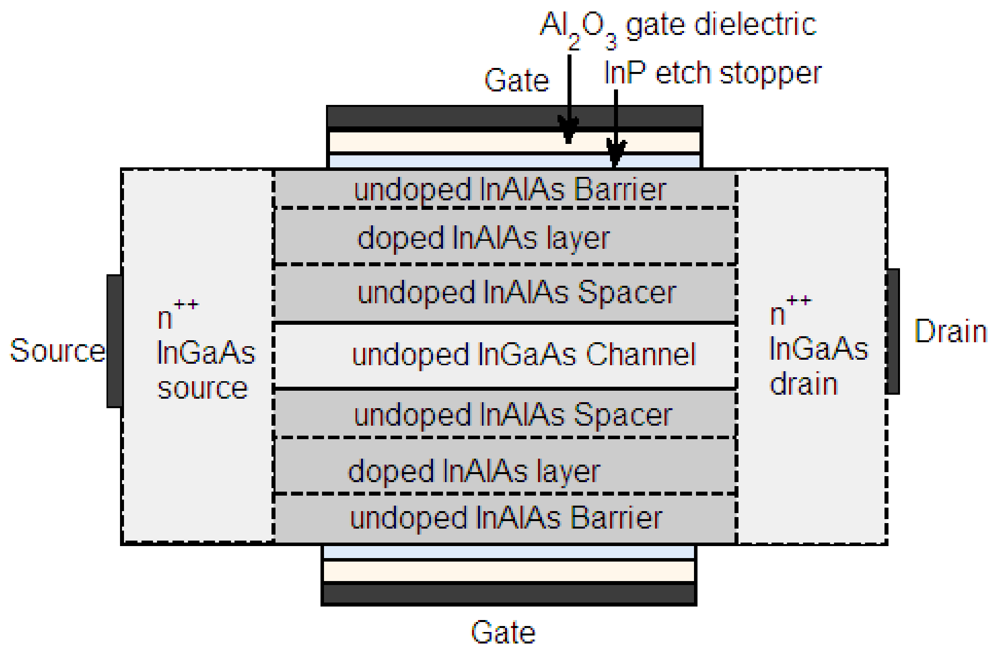


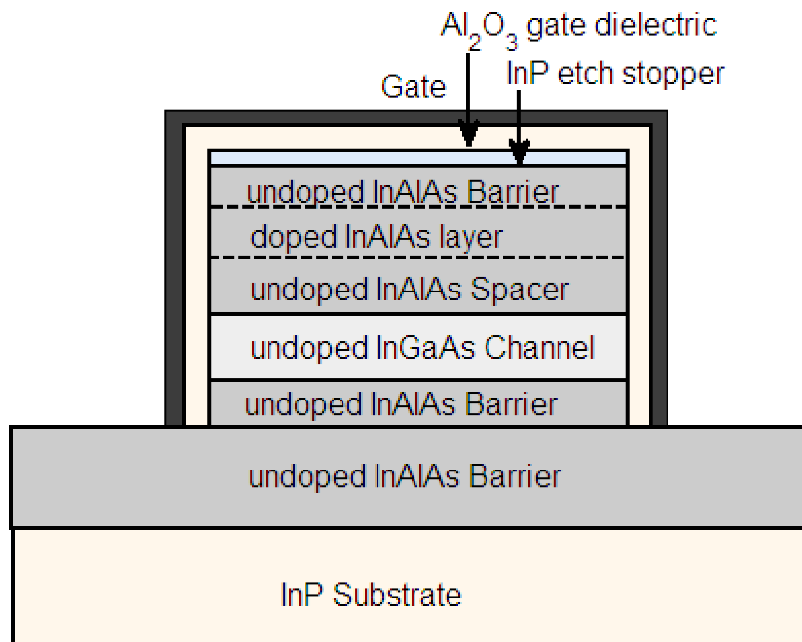
Figure 2.2: Symmetric Double Gate QWFET with pulse-doped InAlAs barrier layers

2.3. Non-planar QWFET

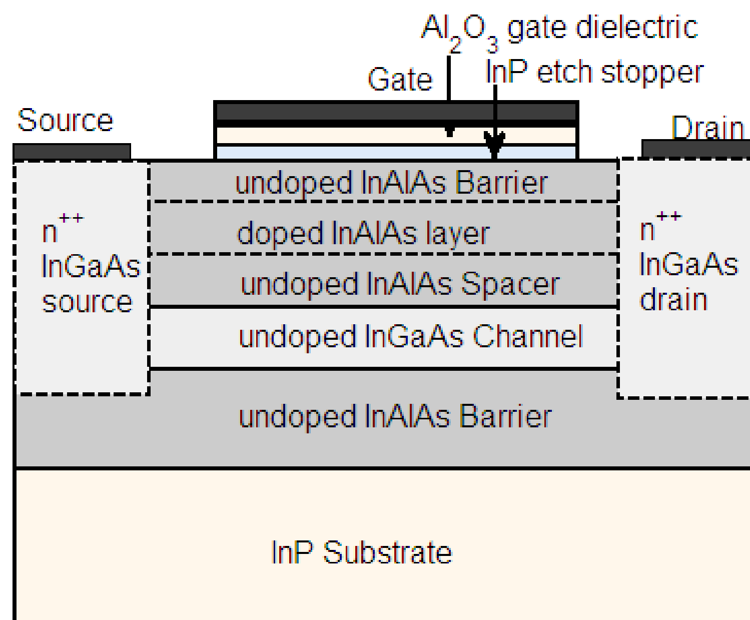
Non-planar, multi-gate QWFET devices are used to achieve stronger gate control over the InGaAs channel carriers due to higher carrier confinement in the channel. Consequently, the non-planar device can provide significantly improved electrostatics even when the transistor gate length is aggressively scaled. Moreover, more enhancement-mode threshold voltage is obtained by the non-planar structure.

The QWFET described in this section is a trigate structure. Two types of trigate QWFET structures are studied in this work. The cross sections of a trigate QWFET with gated InGaAs fin with InAlAs barrier with pulse-doped donor layer is shown in Figure 2.3. Figure 2.3(a) illustrates the cross section perpendicular to the channel length, while Figure 2.3(b) shows the cross section along the direction of the channel length.

Similarly Figure 2.4 (a) and (b) shows the cross sections of a trigate structure without the doped InAlAs top barrier. This alternate structure is reported to be obtained by simplifying a recessed-gate QWFET structure by removing the thick barriers and doped layers under the source/drain region, which enables scaling of the source/drain contact area with small resistance [30]. Good transport characteristics along with subthreshold characteristics are also reported for this structure. This structure is similar to a FinFET with gated InGaAs fin on a semi-insulating InAlAs layer. Both the structures shown in Figure 2.3 and 2.4 are epitaxially grown on an InP substrate.

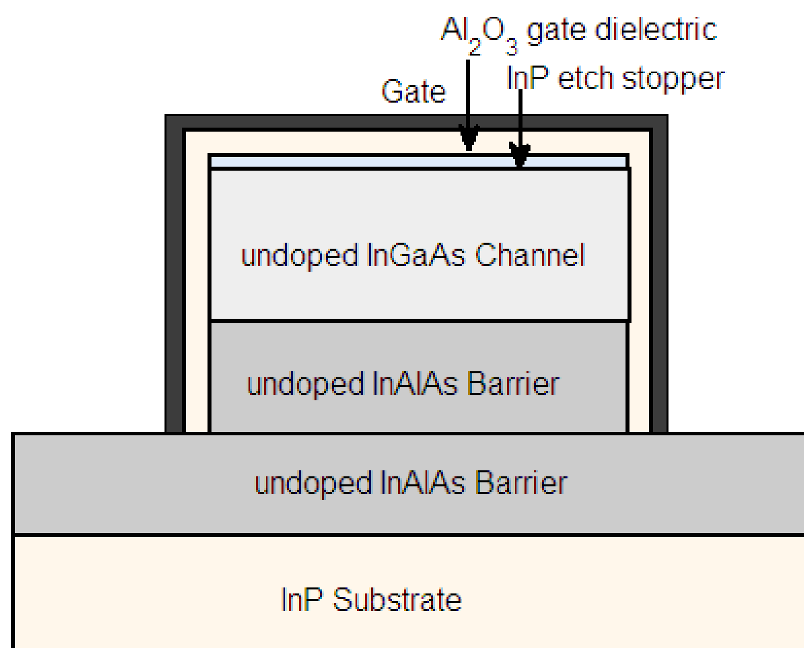


(a)

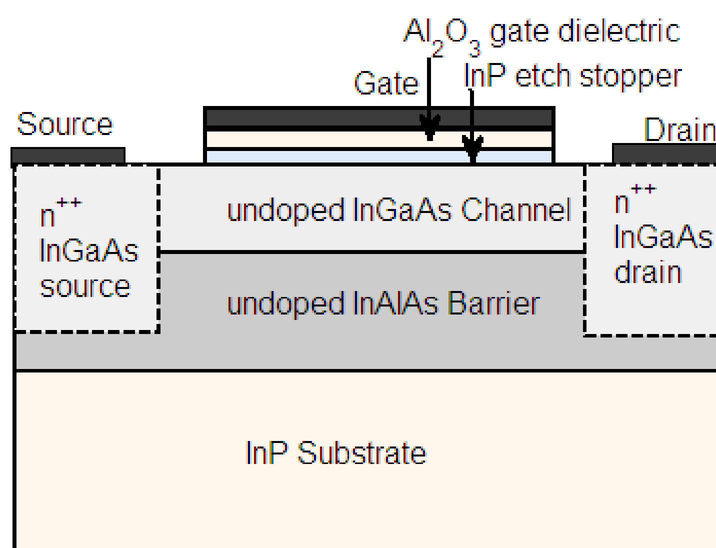


(b)

Figure 2.3: Cross sections (a) perpendicular to the channel length and (b) along the direction of channel length of a trigate QWFET with pulse-doped InAlAs barrier layer



(a)



(b)

Figure 2.4: Cross sections (a) perpendicular to the channel length and (b) along the direction of channel length of a trigate QWFET without InAlAs top barrier.

2.4. Conclusion

This chapter describes several QWFET geometries which are studied in this work. Both planar and non-planar structures have been described. The following chapter describes the mathematical modeling of the channel potential of these device geometries. The threshold voltage model and subthreshold swing model, along with the subthreshold characteristics of the device structures are described in the subsequent chapters.

CHAPTER 3
ANALYTICAL MODELING OF SUBTHRESHOLD POTENTIAL

3.1 Introduction

In this chapter, an analytic model of the channel potential in the subthreshold regime is developed for non-planar InGaAs QWFETs with Al_2O_3 gate dielectric and InGaAs/InAlAs heterostructure system. The subthreshold potential distributions of the devices under investigation are obtained from the solution of Poisson's equation with proper boundary conditions. At first, the analytical expression of potential distribution for the single-gate QWFET is derived under subthreshold conditions. Subsequently, the analysis is extended to double-gate and tri-gate device structures. The potential distribution of the QWFET channel is used to determine the threshold voltage, subthreshold slope and drain induced barrier lowering in the next chapter.

3.2 Device Parameter Extraction

$In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ are ternary III-V materials. Parameters of ternary III-V materials are conveniently predicted by interpolating the data of corresponding binary components. Experimentally determined parameters of GaAs, AlAs and InAs are used to estimate the parameters of $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ needed for the simulation employing the following formula:

$$\begin{aligned} T_{InGaAs} &= xT_{InAs} + (1-x)T_{GaAs} - x(1-x)C_{InGaAs} \\ T_{InAlAs} &= xT_{InAs} + (1-x)T_{AlAs} - x(1-x)C_{InAlAs} \end{aligned} \tag{3.1}$$

C_{InGaAs} and C_{InAlAs} are empirical bowing parameters. Bowing is considered negligible for lattice constant and effective mass while other parameters (i.e. band gap) exhibit strong bowing. Table 3.1 provides the expressions of several material parameters used in the modeling process.

Table 3.1: Parameters of $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ [48], [49]

Parameters	$In_xGa_{1-x}As$	$In_xAl_{1-x}As$
Lattice constant, a_0 (Å)	6.06x+5.65(1-x)	6.06x+5.66(1-x)
Band gap, E_g (eV)	0.348x+1.426(1-x)-0.477x(1-x)	0.348x+2.155(1-x)-0.7x(1-x)
Electron Affinity (ev)	4.9x-4.07(1-x)+0.1908x(1-x)	4.9x-3.85(1-x)-0.49x(1-x)
Permittivity, ε_r	15.15x+12.91(1-x)	15.15x+10.06(1-x)
Electron effective mass/m_0 (Γ)	0.026x+0.067(1-x)	0.026x+0.15(1-x)

When $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$ are chosen as barrier/channel materials, all the layers are lattice matched to the InP substrate. On the other hand, In-rich channel layer, such as $In_{0.65}Ga_{0.35}As$ or $In_{0.75}Ga_{0.25}As$ layers grown on undoped $In_{0.52}Al_{0.48}As$ has a larger lattice constant than the substrate layer. Biaxial compressive strain induced in the channel the shrinks in-plane lattice dimensions (a_{xx} and a_{zz}) to take the lattice constant of the substrate while the perpendicular lattice dimension (a_{yy}) grows. The relative changes of lattice periods in x- and z-direction are:

$$\varepsilon_{xx} = \varepsilon_{zz} = \frac{a_{st} - a_0}{a_0} < 0 \tag{3.2}$$

where a_{st} and a_0 are the lattice constants of the strained and unstrained channel materials respectively. The relative change of perpendicular lattice period, ε_{yy} is related to ε_{xx} by elastic stiffness constants C_{11} and C_{12}.

$$\varepsilon_{yy} = -2\frac{C_{12}}{C_{11}}\varepsilon_{xx} > 0 \tag{3.3}$$

The $In_{0.65}Ga_{0.35}As$ channel is subjected to 0.8% compressive strain while 1.5% compressive strain is induced in the $In_{0.75}Ga_{0.25}As$ channel. The effects of strain are modeled in this section by determining the shifts conduction and valence band edges and changes the effective masses.

InAs, InAl and GaAs are indirect materials with zinc-blende (cubic) structure. In unstrained cubic semiconductors heavy-hole (HH) and light-hole (LH) bands usually

overlap at the Γ-point. The spin-orbit (SO) split-off valence band is separated by the split-off energy, Δ_0. In unstrained $In_{0.52}Al_{0.48}A$ and $In_{0.53}Ga_{0.47}As$, the band edges at zone centre are given by:

$$E_{hh}(0) = E_{lh}(0) = E_v^0 \tag{3.4}$$

$$E_{so}(0) = E_v^0 - \Delta_0 \tag{3.5}$$

$$E_c(0) = E_v^0 + E_g \tag{3.6}$$

However, strain splits the valence band degeneracy at zone center and shifts the spin-orbit band. Considering strain effects, the band edges of $In_{>0.53}Ga_{<0.47}As$ at the Γ-point are found from:

$$E_{hh}(0) = E_v^0 - P_\varepsilon - Q_\varepsilon \tag{3.7}$$

$$E_{lh}(0) = E_v^0 - P_\varepsilon + \frac{1}{2}[Q_\varepsilon - \Delta_0 + \sqrt{\Delta_0^2 + 9Q_\varepsilon^2 + 2Q_\varepsilon\Delta_0}] \tag{3.8}$$

$$E_{so}(0) = E_v^0 - P_\varepsilon + \frac{1}{2}[Q_\varepsilon - \Delta_0 - \sqrt{\Delta_0^2 + 9Q_\varepsilon^2 + 2Q_\varepsilon\Delta_0}] \tag{3.9}$$

$$E_c(0) = E_v^0 + E_g + a_c(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \tag{3.10}$$

where P_ε and Q_ε are defined as:

$$P_\varepsilon = -a_v(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \tag{3.11}$$

$$Q_\varepsilon = -\frac{b}{2}(\varepsilon_{xx} + \varepsilon_{yy} - 2\varepsilon_{zz}) \tag{3.12}$$

Factors a_c and a_v are hydrostatic deformation potentials in conduction band and valence band respectively; while *b* is the shear deformation potential.

The conduction band offset ΔE_c and valence band offset ΔE_v are estimated according to model-solid theory [49]. The concept of average valence band energy, $E_{v,av}^0$ is employed in this theory to obtain a reference for the energy bands. The $E_{v,av}^0$ parameters of GaAs, AlAs and InAs obtained from model-solid theory are used to estimate $E_{v,av}^0$ for $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ where the effects of change in the lattice constant (a) are encompassed by a bowing parameter:

$$C_{InGaAs}(E_{v,av}^0) = 3[a_v(InAs) - a_v(GaAs)]\,\frac{a(InAs)-a(GaAs)}{a(In_xGa_{1-x}As)}$$

$$C_{InAlAs}(E_{v,av}^0) = 3[a_v(InAs) - a_v(AlAs)]\,\frac{a(InAs)-a(AlAs)}{a(In_xAl_{1-x}As)} \tag{3.13}$$

For the unstrained $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$ the conduction band edge at Γ-point is given by:

$$E_c^0 = E_v^0 + E_g = E_{v,av}^0 + \frac{\Delta_0}{3} + E_g \tag{3.14}$$

where,

$$E_v^0 = E_{v,av}^0 + \frac{\Delta_0}{3} \tag{3.15}$$

In strained $In_{>0.53}Ga_{<0.47}As$ the band energies can be calculated from:

$$E_c^0 = E_v^0 + E_g = E_{v,av} + \frac{\Delta_0}{3} + E_g \tag{3.16}$$

$$E_{v,av} = E_{v,av}^0 - P_\varepsilon \tag{3.17}$$

Band offset between the channel and barrier layer is illustrated in Fig. 3.1 for two different In-concentrations in the channel.

The electron affinity (χ) of the intermediate $In_{0.53}Ga_{0.47}As$ layer is determined using bowing parameter C(χ):

$$C(\chi) = -C(E_g)(\chi(InAs) - \chi(AlAs))/(E_g(InAs) - E_g(AlAs))$$

$$C(\chi) = -C(E_g)(\chi(InAs) - \chi(GaAs))/(E_g(InAs) - E_g(GaAs)) \tag{3.17}$$

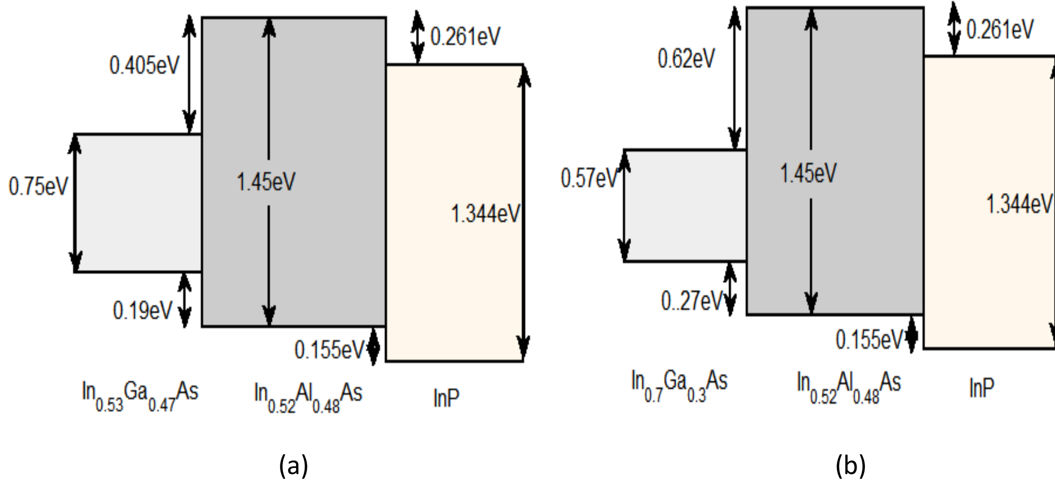


Figure 3.1: Band offsets in InGaAs and InAlAs heterostructure system for (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.75}Ga_{0.25}As$

From electrical characteristics and HR-XPS studies a band gap of 6.65±0.11 eV and an electron affinity of 2.58±0.09 eV for ALD Al_2O_3 have been extracted [50]. We take the band gap and electron affinity to be 6.73eV and 2.5eV respectively.

For the unstrained $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$, the electron and hole effective masses are determined from the effective masses of GaAs, AlAs and InAs. Biaxial compressive strain causes the curvatures of the energy band structures to change and consequently induces change in effective masses.

3.3 Modeling Potential Distribution

In the device structures considered in this work, the channel material is undoped, while the source and drain regions are abrupt and densely doped. All the calculations are done at room temperature. Since the conduction current is small at the subthreshold region, the electrostatics can be assumed to be governed by Poisson's equation only. The potential distribution of the Quantum Well Field Effect Transistor at the subthreshold region can be obtained by solving the Poisson's equation including only the mobile charge (electrons) term under gradual channel approximation. In this section, the subthreshold potentials of single-gate, double-gate and tri-gate QWFET devices are modeled.

3.3.1 Single-gate QWFET potential

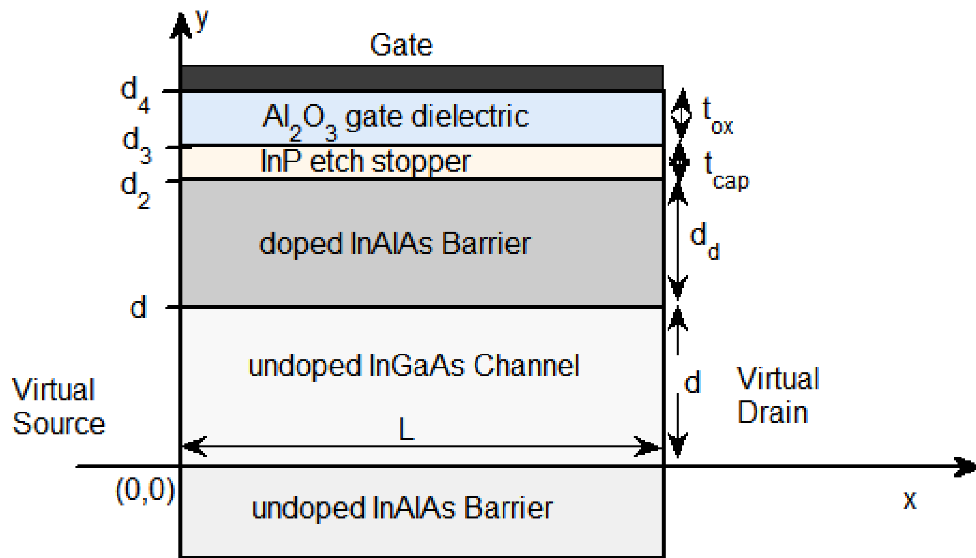
The single-gate structure used in this analysis is shown in Figure 3.2. At the subthreshold condition, the two dimensional electron gas (2DEG) is absent in the channel. So the 2D Poisson's equation for threshold region with the mobile charge term can be approximated by

$$\nabla^2\varphi(x,y) = \frac{q}{\varepsilon_c} n_i \exp\left((\varphi - \varphi_F)/V_T\right) \tag{3.18}$$

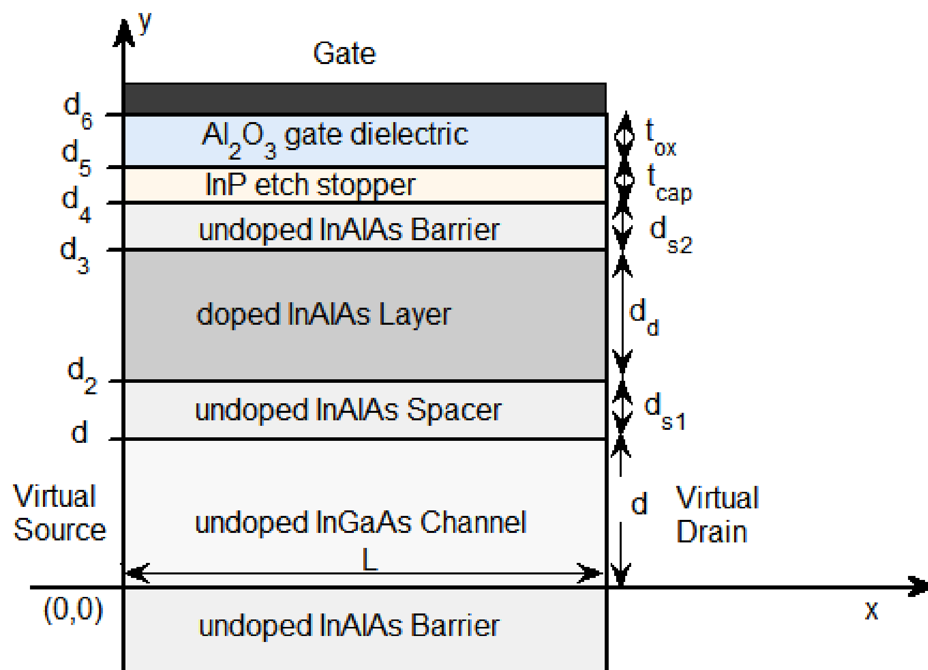
where q is the electronic charge, ε_c and n_i are the permittivity and intrinsic carrier concentration of InGaAs respectively, V_T is the thermal voltage at room temperature, φ is the electrostatic potential and φ_F is the electron quasi-Fermi potential referenced to the Fermi level in the source, which is constant in the x-direction. Here $q(\varphi - \varphi_F/kT >> 1$, so the hole density is considered negligible. The 2D Poisson's equation has to be solved satisfying the following boundary conditions for the electron quasi-Fermi potential:

$$\varphi_F(0,y) = 0 \tag{3.19}$$

$$\varphi_F(L,y) = V_{DS} \tag{3.20}$$



(a)



(b)

Figure 3.2: Device geometry for single-gate QWFET with

(a) uniformly doped barrier and (b) pulse-doped barrier

where V_{DS} is the drain to source voltage and L is the channel length. The boundary conditions for φ are given as

$$\varphi(0, y) = V_{bi} \quad (3.21)$$

$$\varphi(L, y) = V_{bi} + V_{DS} \quad (3.22)$$

$$\frac{\partial\varphi}{\partial y}|_{y=0} = 0 \quad (3.23)$$

$$\varepsilon_c \frac{\partial\varphi}{\partial y}|_{y=d-} = \varepsilon_d \frac{\partial\varphi}{\partial y}|_{y=d+} \quad (3.24)$$

where, V_{bi} is the built-in voltage, d is the thickness of the InGaAs channel and ε_d is the permittivity of InAlAs. The boundary condition imposed in Eq. (3.23) considers all the mobile charge to be confined in the channel, while the boundary condition of Eq. (3.24) signifies constant electric flux at the channel/barrier interface. The potential $\varphi(x, y)$ as the sum of two terms: $\varphi_0(y)$, which is the solution of the 1-D Poisson's equation in the direction perpendicular to the channel, and $\varphi_1(x, y)$, which is the solution of the residual 2-D differential equation:

$$\varphi(0, y) = \varphi_0(y) + \varphi_1(x, y) \quad (3.25)$$

$\varphi_0(y)$ is the solution to the one dimensional Poisson's equation given by

$$\frac{\partial^2}{\partial y^2}\varphi_0(y) = \frac{q}{\varepsilon_c} n_i \exp\,(\varphi_0/V_T) \quad (3.26)$$

which satisfies the boundary conditions:

$$\frac{\partial\varphi_0}{\partial y}|_{y=0} = 0 \quad (3.27)$$

$$\varepsilon_c \frac{\partial\varphi_0}{\partial y}|_{y=d-} = \varepsilon_d \frac{\partial\varphi_0}{\partial y}|_{y=d+} \quad (3.28)$$

The residual differential equation for $\varphi_1(x, y)$ can be written as

$$\nabla^2\varphi_1(x, y) = \frac{q}{\varepsilon_c} \exp\left(\frac{\varphi_0}{V_T}\right) n_i \left[\exp\left(\frac{\varphi_1 - \varphi_F}{V_T}\right) - 1\right] \quad (3.29)$$

Assuming that $(\varphi_1 - \varphi_F)/V_T$ is small, Eq. (3.29) can be reduced to be a Laplace equation. This is equivalent to use the superposition of a 1D solution of the Poisson's equation assuming a 1D distribution of the mobile charge and a 2D solution of Laplace's equation [51].

The solution of the 1D Poisson's equation, $\varphi_0(y)$ is given by [52]:

$$\varphi_0(y) = V_T In\left[\frac{2V_T B^2 \varepsilon_c}{n_i q} sec^2(By)\right] \quad (3.33)$$

Here B is a constant whose value depends on the boundary condition and device parameters. The value of B should fall in range: $0 < B < \frac{\pi}{2d}$. In the following subsections, the value of B is determined; hence the 1D potential distribution and band diagram are modeled for both the structures shown in Figure 3.2.

3.3.1.1. With uniform doping

In the case of uniform doping of the InAlAs barrier, the y-component of the electric field is considered to be constant in the oxide layer and InP cap layer, while the field is considered to be zero in the InAlAs lower barrier. The y-component of the electric field for different regions of QWFET device is given by

$$E_y(y) = \begin{cases} -2V_T B tan(By), & \text{for } 0 < y \leq d \\ E_1 + \frac{qN_d}{\varepsilon_d}(y-d), & \text{for } d < y \leq d_2 \\ E_{cap}, & \text{for } d_2 < y \leq d_3 \\ E_{ox}, & \text{for } d_3 < y \leq d_4 \end{cases} \tag{3.34}$$

Here N_d is the donor doping density of the InAlAs barrier. At the interfaces, the electric fields in different regions are related by

$$-\varepsilon_c \frac{\partial \varphi_0}{\partial y}|_{y=d} = E_1 \varepsilon_d \tag{3.35}$$

$$E_2 = E_1 + \frac{qN_d}{\varepsilon_d} d_d \tag{3.36}$$

$$\varepsilon_d E_2 = \varepsilon_{cap} E_{cap} \tag{3.37}$$

$$\varepsilon_{cap} E_{cap} = \varepsilon_{ox} E_{ox} \tag{3.38}$$

where d_d is the barrier thickness, ε_{cap} and ε_{ox} are the permittivity of InP and Al_2O_3 respectively.

The potential of the InGaAs channel at *y=d* satisfies the following relation:

$$\varphi_0(d) = V_{GS} - \varphi_{ms} + V_{ox} + V_{cap} + \frac{qN_d(d_d - d'^2)}{2\varepsilon_d} - \frac{qN_d d'^2}{2\varepsilon_d} \tag{3.39}$$

Here it is assumed that the maximum potential occurs at y=$(d + d')$. Putting $V_{ox} = E_{ox} t_{ox}$ and $V_{cap} = E_{cap} t_{cap}$ in Eq. (3.39) and using Eqs. (3.35)-(3.38), we obtain,

$$\varphi_0(d) = V_{GS} - \varphi_{ms} + \frac{\varepsilon_{cap}}{\varepsilon_{ox}} E_{cap} t_{ox} + E_{cap} t_{cap} + \frac{qN_d d_d^2}{2\varepsilon_d} - \frac{qN_d d_d d'}{2\varepsilon_d}$$

or, $$\varphi_0(d) = V_{GS} - \varphi_{ms} + \frac{\varepsilon_d}{\varepsilon_{ox}} E_2 t_{ox} + \frac{\varepsilon_d}{\varepsilon_{cap}} E_2 t_{cap} + \frac{qN_d d_d^2}{2\varepsilon_d} - \frac{qN_d d_d d'}{2\varepsilon_d}$$

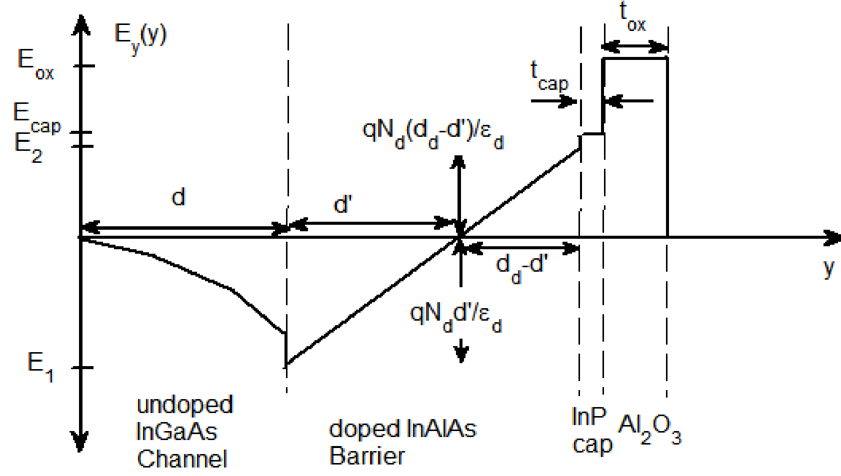


Figure 3.3: Illustration of the y-component of electric field, $E_y(y)$

or, $\varphi_0(d) = V_{GS} - \varphi_{ms} + (\frac{\varepsilon_d}{\varepsilon_{ox}}t_{ox} + \frac{\varepsilon_d}{\varepsilon_{cap}}t_{cap})(E_1 + \frac{qN_d}{\varepsilon_d}d_d) + \frac{qN_d d_d{}^2}{2\varepsilon_d} - \frac{qN_d d_d d'}{2\varepsilon_d}$

or,$\varphi_0(d) = V_{GS} - \varphi_{ms} + (\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}})(-\varepsilon_c \frac{\partial \varphi_0}{\partial y}|_{y=d} + qN_d d_d) + \frac{qN_d d_d{}^2}{2\varepsilon_d} - \frac{qN_d d_d d'}{2\varepsilon_d}$

We can express E_1 as $qN_d d^{'}/\varepsilon_d$ using Figure 3.3, which leads to

$$\varphi_0(d) = V_{GS} - \varphi_{ms} + qN_d d_d\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d}{2\varepsilon_d}\right) - \varepsilon_c\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d}{\varepsilon_d}\right)\frac{\partial \varphi_0}{\partial y}|_{y=d} \quad (3.40)$$

Substituting the expression of Eq. 3.33 into Eq. 3.40 and simplifying, we get

$$V_{GS}^{'} - 2\varepsilon_c V_T B tan(Bd)\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d}{\varepsilon_d}\right) - V_T In\left[\frac{2V_T B^2 \varepsilon_c}{n_i q} sec^2(Bd)\right] = 0 \quad (3.41)$$

where, $$V_{GS}^{'} = V_{GS} - \varphi_{ms} + qN_d d_d\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d}{2\varepsilon_d}\right) \quad (3.42)$$

The value of B is obtained by solving Eq. (3.41). According to analytical approach, the solution of the 1D Poisson's equation, $\varphi_0(y)$ can be expressed as

$$\varphi_0(y) = \begin{cases} V_T In\left[\frac{2V_T B^2 \varepsilon_c}{n_i q} sec^2(By)\right], & \text{for } 0 < y \le d \\ -\frac{qN_d(y-d)^2}{2\varepsilon_d} - E_1(y-d) + \varphi_0(d), & \text{for } d < y \le d_2 \\ -E_{cap}(y-d_2) + \varphi_0(d_2), & \text{for } d_2 < y \le d_3 \\ -E_{ox}(y-d_3) + \varphi_0(d_3), & \text{for } d_3 < y \le d_4 \end{cases} \quad (3.42)$$

Figure 3.4 demonstrates the potential distribution, $\varphi_0(y)$, while the corresponding band diagram is shown in Figure 3.5.

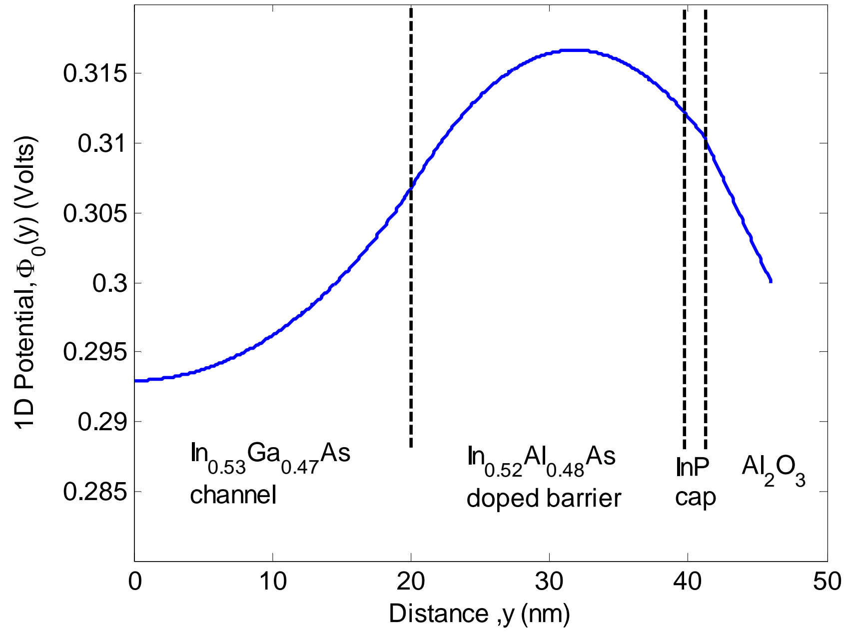


Figure 3.4: Potential distribution in the y-direction for single-gate QWFET with uniform doping. $V_{GS} = 0.5V$, $\varphi_{ms} = 0.2V$, $N_d = 10^{17}cm^{-3}$, $d = 20nm$, $d_d = 20nm$, $t_{cap} = 1nm$ and $t_{ox} = 5nm$.

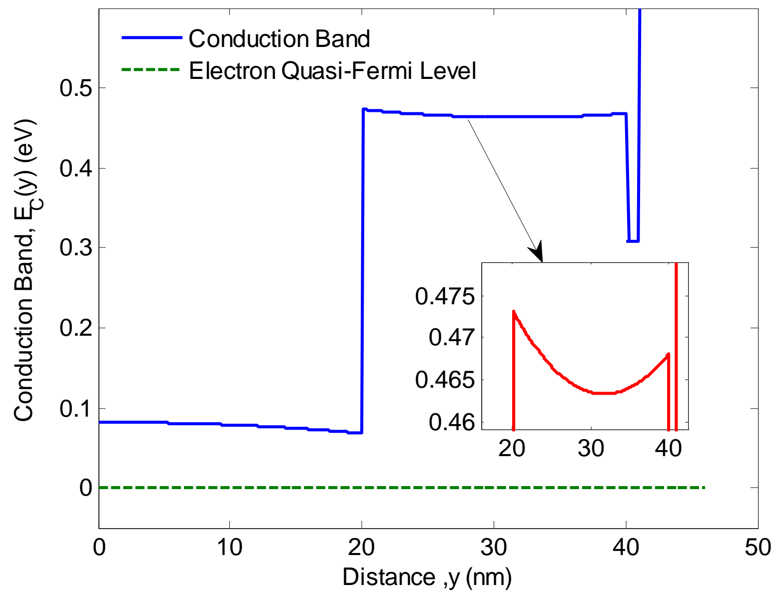


Figure 3.5: Conduction band diagram and electron quasi-Fermi level for single-gate QWFET with uniform doping. $V_{GS} = 0.5V$, $\varphi_{ms} = 0.2V$, $N_d = 10^{17}cm^{-3}$, $d = 20nm$, $d_d = 20nm$, $t_{cap} = 1nm$ and $t_{ox} = 5nm$.

3.3.1.2. With pulsed doping

In this subsection, the expression of $\varphi_0(y)$ is derived considering pulse-doped InAlAs barrier, where d_{s1}, d_d and d_{s2} are the thicknesses of undoped InAlAs barrier layer, donor layer and undoped InAlAs spacer layer respectively. For this structure, the y-component of the electric field for different regions can be expressed as

$$E_y(y) = \begin{cases} -2V_T B tan(By), & \text{for } 0 < y \leq d \\ E_1 & \text{for } d < y \leq d_2 \\ E_1 + \frac{qN_d}{\varepsilon_d}(y - d_2), & \text{for } d_2 < y \leq d_3 \\ E_1 + \frac{qN_d}{\varepsilon_d} d_d, & \text{for } d_3 < y \leq d_4 \\ E_{cap}, & \text{for } d_4 < y \leq d_5 \\ E_{ox}, & \text{for } d_5 < y \leq d_6 \end{cases} \tag{3.43}$$

where, the electric fields the interfaces are related by Eqs. (3.35)-(3.38). Solving for $\varphi_0(y)$, we obtain the expression

$$\varphi_0(y) = \begin{cases} V_T In\left[\frac{2V_T B^2 \varepsilon_c}{n_i q} sec^2(By)\right], & \text{for } 0 < y \leq d \\ -E_1(y - d) + \varphi_0(d) & \text{for } d < y \leq d_2 \\ -\frac{qN_d(y-d_2)^2}{2\varepsilon_d} - E_1(y - d_2 + d_{s2}) + \varphi_0(d), & \text{for } d_2 < y \leq d_3 \\ -E_2(y - d_3) + \varphi_0(d_3), & \text{for } d_3 < y \leq d_4 \\ -E_{cap}(y - d_4) + \varphi_0(d_4), & \text{for } d_4 < y \leq d_5 \\ -E_{ox}(y - d_5) + \varphi_0(d_5), & \text{for } d_5 < y \leq d_6 \end{cases} \tag{3.44}$$

The value of B is obtained according to the previous subsection using the boundary condition

$$\begin{aligned} \varphi_0(d) = V_{GS} - \varphi_{ms} + qN_d d_d\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d}{2\varepsilon_d} + \frac{d_{s1}}{\varepsilon_d}\right) \\ -\varepsilon_c\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d+d_{s1}+d_{s2}}{\varepsilon_d}\right)\frac{\partial\varphi_0}{\partial y}\Big|_{y=d} \end{aligned} \tag{3.45}$$

which leads to

$$V_{GS}^{'} - 2\varepsilon_c V_T B tan(Bd)\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d+d_{s1}+d_{s2}}{\varepsilon_d}\right) - V_T In\left[\frac{2V_T B^2 \varepsilon_c}{n_i q} sec^2(Bd)\right] = 0 \tag{3.46}$$

where,
$$V_{GS}^{'} = V_{GS} - \varphi_{ms} + qN_d d_d\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d}{2\varepsilon_d} + \frac{d_{s1}}{\varepsilon_d}\right) \tag{3.47}$$

The potential distribution, $\varphi_0(y)$ and the corresponding band diagram for the single-gate pulse doped structure are shown in Figure 3.6 and Figure 3.7 respectively.

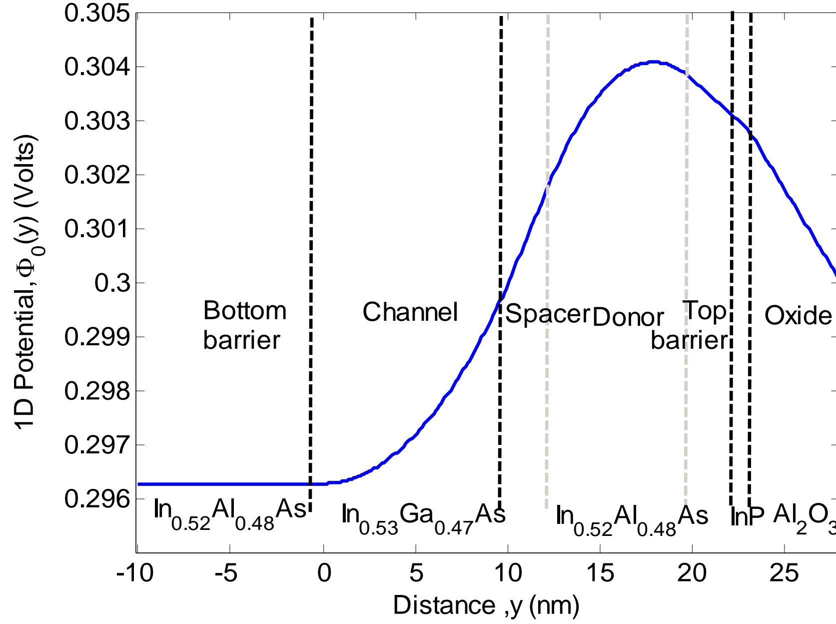


Figure 3.6: Potential distribution in the y-direction for single-gate QWFET with pulse doping. $V_{GS} = 0.5V$, $\varphi_{ms} = 0.2V$, $N_d = 10^{17} cm^{-3}$, $d = 10nm$, $d_d = 8nm$, $d_{s1} = 2nm$, $d_{s2} = 2nm$, $t_{cap} = 1nm$ and $t_{ox} = 5nm$.

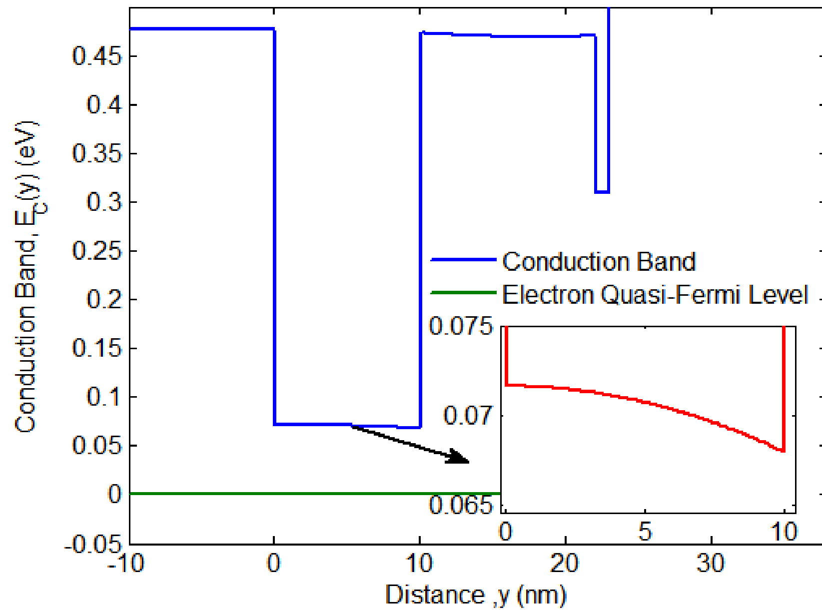


Figure 3.7: Conduction band diagram in the y-direction for single-gate QWFET with pulse doping. $V_{GS} = 0.5V$, $\varphi_{ms} = 0.2V$, $N_d = 10^{17} cm^{-3}$, $d = 10nm$, $d_d = 8nm$, $d_{s1} = 2nm$, $d_{s2} = 2nm$, $t_{cap} = 1nm$ and $t_{ox} = 5nm$.

3.3.1.3. Two-dimensional potential distribution

Since the two-dimensional potential, $\varphi(x,y)$ can be derived by adding 2D potential component, $\varphi_1(x,y)$ to the 1D potential, $\varphi_0(y)$, the residual Poisson's Equation in Eq. (3.29) has to be solved for $\varphi_1(x,y)$, which can be simplified to

$$\frac{\partial^2}{\partial x^2}\varphi_1(x,y)+\frac{\partial^2}{\partial y^2}\varphi_1(x,y)=0 \tag{3.48}$$

Using Eq. (3.25), the boundary conditions can be derived from the Dirichlet boundary conditions in Eqs. (3.21)-(3.23):

$$\varphi_1(0,y)=V_{bi}-\varphi_0(y) \tag{3.49}$$

$$\varphi_1(L,y)=V_{bi}+V_{DS}-\varphi_0(y) \tag{3.50}$$

$$\frac{\partial\varphi_1}{\partial y}|_{y=0}=0 \tag{3.51}$$

The remaining boundary condition can be simplified into

$$\varphi_1(x,d)=-\sigma\frac{\partial\varphi_1}{\partial y}|_{y=d} \tag{3.52}$$

which is derived from Eqs. (3.40) and (3.45)

where,
$$\sigma=\begin{cases}\varepsilon_C\left(\frac{t_{ox}}{\varepsilon_{ox}}+\frac{t_{cap}}{\varepsilon_{cap}}+\frac{d_d}{\varepsilon_d}\right), & \text{for uniform doping}\\ \varepsilon_C\left(\frac{t_{ox}}{\varepsilon_{ox}}+\frac{t_{cap}}{\varepsilon_{cap}}+\frac{d_d+d_{s1}+d_{s2}}{\varepsilon_d}\right), & \text{for pulse doping}\end{cases} \tag{3.53}$$

Eq (3.48) is solved using variable separation technique, i.e.

$$\varphi_1(x,y)=f(x)g(y) \tag{3.54}$$

Substituting the expression of $\varphi_1(x,y)$ in Eq. (3.48) and rearranging, we obtain,

$$\frac{f''(x)}{f(x)}+\frac{g''(y)}{g(y)}=0 \tag{3.55}$$

Choosing $\frac{f''(x)}{f(x)}=\lambda^2$ and $\frac{g''(y)}{g(y)}=-\lambda^2$, the following solutions are obtained for $f(x)$ and $g(y)$:

$$f(x)=A\exp(\lambda x)+B\exp(-\lambda x) \tag{3.56}$$

$$g(y)=C\cos(\lambda y)+D\sin(\lambda y) \tag{3.57}$$

D is found to be 0 from the boundary condition in Eq. (3.51), while the Eq. (3.52) gives the equation to find the value of λ:

$$\lambda\tan(\lambda d)=1/\sigma \tag{3.58}$$

Now $\varphi_1(x,y)$ can be expressed as

$$\varphi_1(x,y) = [C_0\exp(\lambda x) + C_1\exp(-\lambda x)]\cos(\lambda y) \tag{3.59}$$

C_0 and C_1 are solved using the Dirichlet boundary conditions in Eqs. (3.49) and (3.50):

$$C_0 = \frac{[V_{bi}-\varphi_0(d/2)][1-\exp(-\lambda L)]+V_{DS}}{[\exp(\lambda L)-\exp(-\lambda L)]\cos(\lambda d)} \tag{3.60}$$

$$C_1 = \frac{[V_{bi}-\varphi_0(d/2)][\exp(\lambda L)-1]-V_{DS}}{[\exp(\lambda L)-\exp(-\lambda L)]\cos(\lambda d)} \tag{3.61}$$

So the 2D potential distribution for the channel is given by:

$$\varphi(x,y) = V_T In\left[\frac{2V_T B^2 \varepsilon_c}{n_i q} sec^2(By)\right] + [C_0\exp(\lambda x) + C_1\exp(-\lambda x)]\cos(\lambda y) \tag{3.62}$$

The potential distribution of the channel region is shown in Figure 3.8 for the pulsed doped structure.

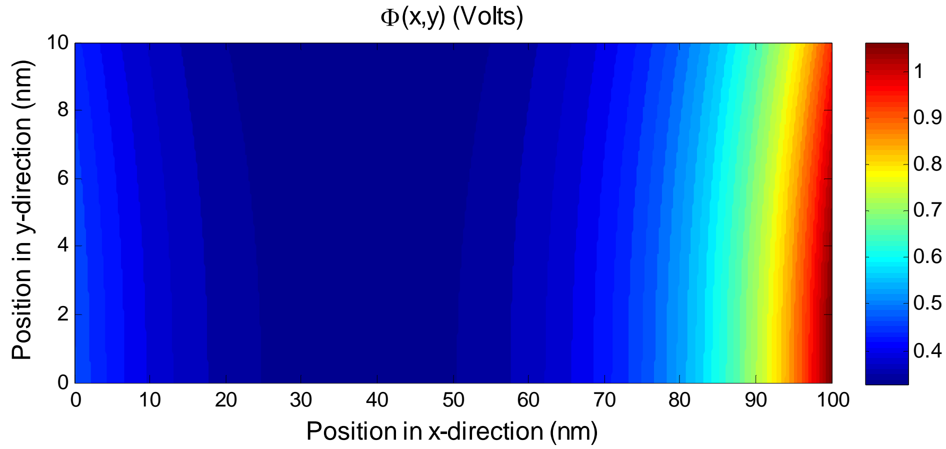


Figure 3.8: Channel potential for the pulsed doped QWFET, where $V_{GS} = 0.5V$ $V_{DS} = 0.5V$, $V_{bi} = 0.5V$ and $L = 100nm$. The other parameters are repeated from the corresponding single-gate structure.

3.3.2 Symmetric double-gate QWFET potential

The two-dimensional potential of the Symmetric Double-gate QWFET is derived in this subsection by solving the 2D Poisson's equation with the mobile charge term. Figure 3.9 shows the structure used in this analysis. The electron quasi-Fermi level satisfies the boundary conditions described in Eqs. (3.19) -(3.20). The boundary conditions for φ are similar to the conditions for the single gate structure

$$\varphi(0,y) = V_{bi} \tag{3.63}$$

$$\varphi(L, y) = V_{bi} + V_{DS} \tag{3.64}$$

$$\varphi\left(x, \frac{d}{2}\right) = \varphi\left(x, -\frac{d}{2}\right) \tag{3.65}$$

$$\varepsilon_c \frac{\partial\varphi}{\partial y}|_{y=d-/_2} = \varepsilon_d \frac{\partial\varphi}{\partial y}|_{y=d+/_2} \tag{3.66}$$

The boundary condition stated in Eq. (3.65) arises due to the symmetry of the structure under investigation. This condition is only valid for a symmetrical structure with respect to the channel centre and equal voltages applied to the top gate and bottom gate. It leads to a similar equation to the single-gate structure, i.e.

$$\frac{\partial\varphi}{\partial y}|_{y=0} = 0 \tag{3.67}$$

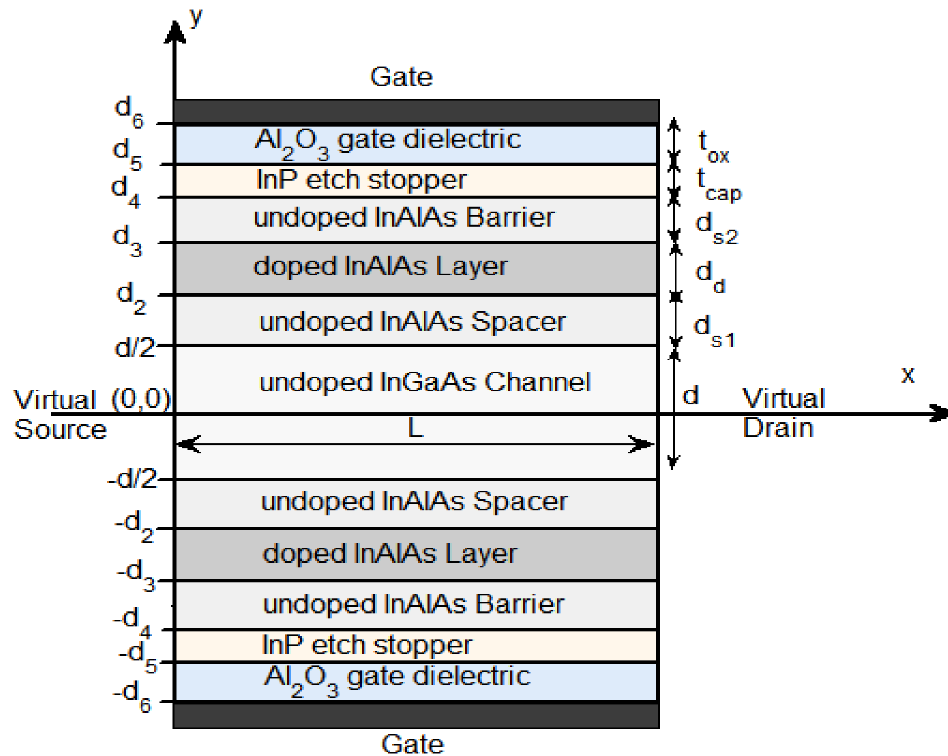


Figure 3.9: Device geometry of double-gate QWFET

Since these equations resembles the single-gate equations, the potential $\varphi(x, y)$ is obtained in a similar manner, assuming $\varphi(x, y)$ to be the summation of the solution of 1D Poisson's equation in the direction perpendicular to the channel and the solution of the 2D Laplace equation.

3.3.2.1 With pulse-doped barrier

The solution to the 1D Poisson's equation is given by

$$\varphi_0(y) = V_T In\left[\frac{2V_T B^2 \varepsilon_c}{n_i q} sec^2(By)\right], \qquad \text{for } -\frac{d}{2} \leq y \leq \frac{d}{2} \tag{3.68}$$

For a DG-QWFET with pulse-doped barrier, B can be obtained by solving

$$V_{GS}^{'} - 2\varepsilon_c V_T Btan\left(\frac{Bd}{2}\right)\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d + d_{s1} + d_{s2}}{\varepsilon_d}\right) - V_T In\left[\frac{2V_T B^2 \varepsilon_c}{n_i q} sec^2(\frac{Bd}{2})\right] = 0 \tag{3.69}$$

where $V_{GS}^{'}$ is given in Eq. (3.47).

The 1D potential for the double-gate QWFET is plotted in Figure 3.10, while the conduction band diagram is demonstrated in Figure 3.11.

The solution to the Laplace equation, $\varphi_1(x, y)$ is expressed as

$$\varphi_1(x, y) = [C_0 \exp(\lambda x) + C_1 \exp(-\lambda x)] \cos(\lambda y) \tag{3.70}$$

where the value of C_0 and C_1 are given by

$$C_0 = \frac{[V_{bi} - \varphi_0(d/4)][1 - \exp(-\lambda L)] + V_{DS}}{[\exp(\lambda L) - \exp(-\lambda L)]\cos(\lambda d)} \tag{3.71}$$

$$C_1 = \frac{[V_{bi} - \varphi_0(d/4)][\exp(\lambda L) - 1] - V_{DS}}{[\exp(\lambda L) + \exp(-\lambda L)]\cos(\lambda d)} \tag{3.72}$$

The two-dimensional potential distribution of the symmetric double-gate QWFET is shown in Figure 3.12.

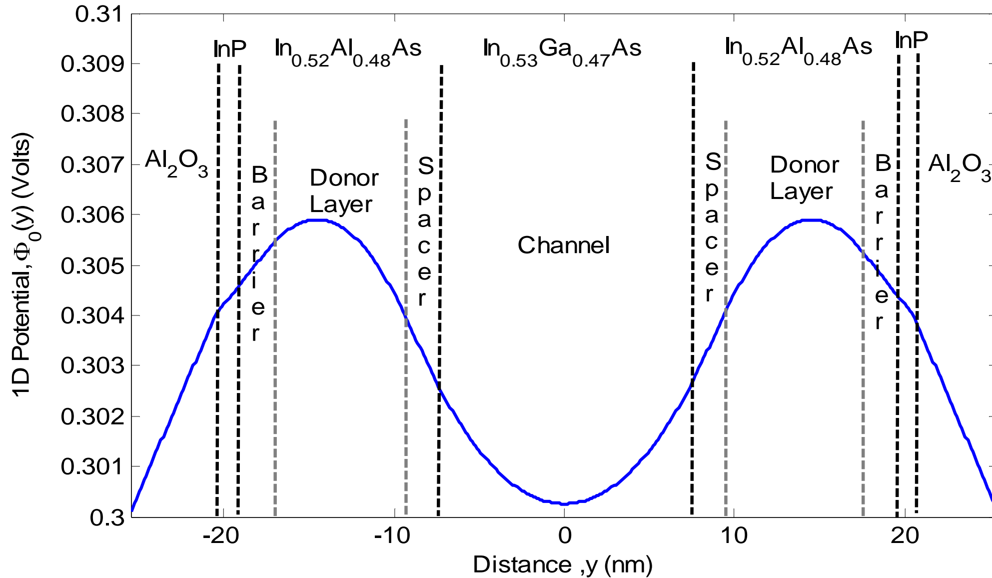


Figure 3.10: Potential distribution in the y-direction for double-gate QWFET with pulse doping, where $V_{GS} = 0.5V$ and $d = 15nm$.

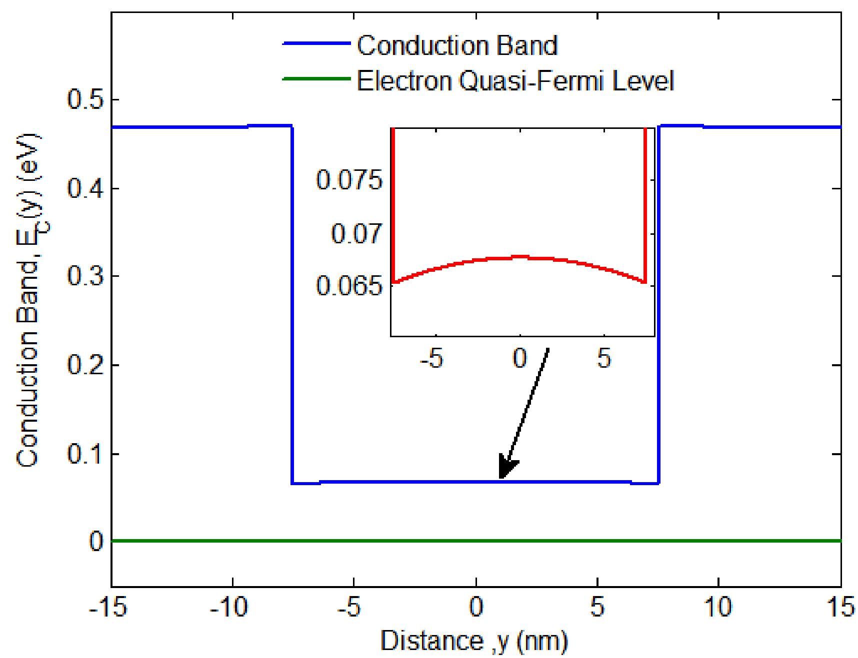


Figure 3.11: Conduction band diagram in the y-direction for double-gate QWFET with pulse doping, where $V_{GS} = 0.5V$ and $d = 15nm$.

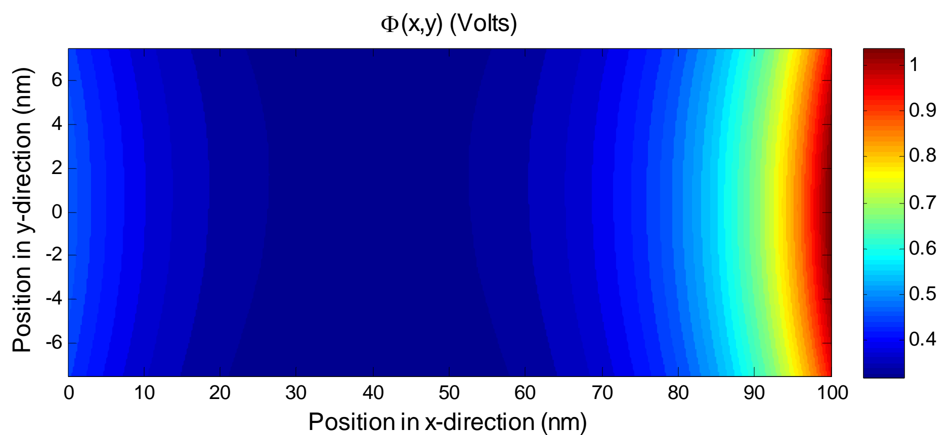


Figure 3.12: Channel potential for the pulsed doped DG QWFET, where $V_{GS} = 0.5V$ $V_{DS} = 0.5V$, $V_{bi} = 0.5V$ and $L = 100nm$. The other parameters are repeated from the corresponding single gate structure.

3.3.3 Non-planar QWFET potential

In this subsection, the subthreshold potential distribution will be derived for the non-planar trigate QWFET, with the aid of the analysis done for the single-gate and the double-gate structures. Since the structure is non-planar, the solution requires three-dimensional analysis. Accordingly, the 3D Poisson's equation with the mobile charge term is solved with the appropriate boundary conditions. Figure 3.13 shows the geometry of the structure used in this analysis. While the boundary conditions for electron quasi-Fermi level remains the same as (3.19) -(3.20), the boundary conditions for φ are given by

For the source end:

$$\varphi(0, y, z) = V_{bi} \tag{3.73}$$

For the drain end:

$$\varphi(L, y, z) = V_{bi} + V_{DS} \tag{3.74}$$

For the top gate:

$$\begin{aligned} V_{GS} - \varphi_{ms} + qN_d d_d \left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d}{2\varepsilon_d} + \frac{d_{s1}}{\varepsilon_d}\right) - \varphi(x, h, z) \\ -\varepsilon_c \left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d + d_{s1} + d_{s2}}{\varepsilon_d}\right) \frac{\partial \varphi}{\partial y}\Big|_{(x,h,z)} = 0 \end{aligned} \tag{3.75}$$

For the bottom barrier:

$$\frac{\partial \varphi}{\partial y}\Big|_{(x,0,z)} = 0 \tag{3.76}$$

For the right gate:

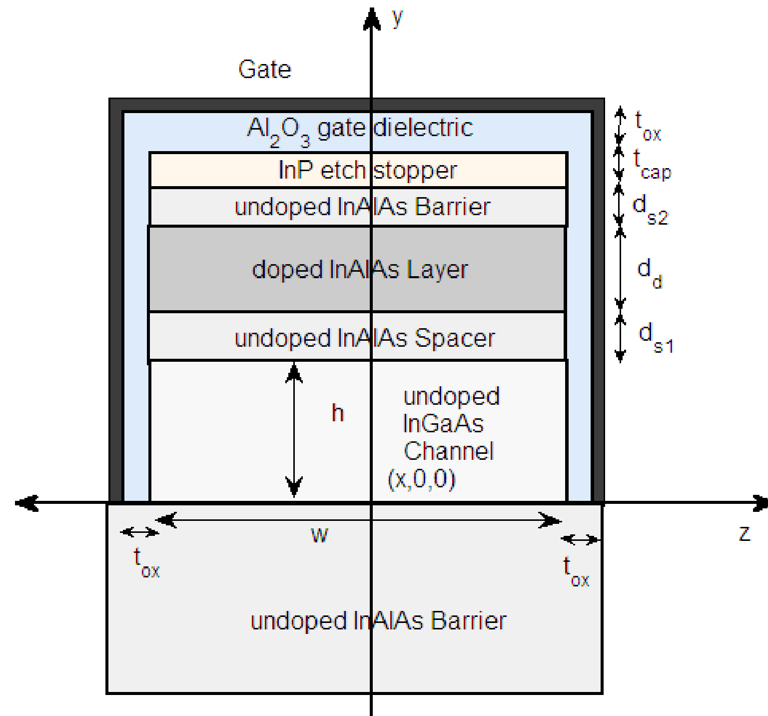
$$V_{GS} - \varphi_{ms} - \varphi(x, y, w/2) - \varepsilon_c \left(\frac{t_{ox}}{\varepsilon_{ox}}\right) \frac{\partial \varphi}{\partial z}\Big|_{(x,y,w/2)} = 0 \tag{3.77}$$

For the left gate:

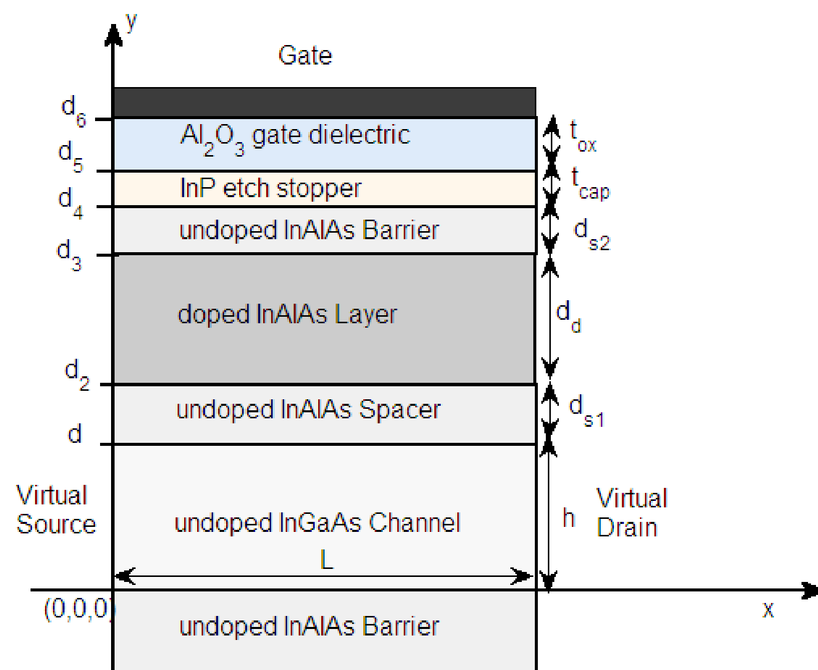
$$V_{GS} - \varphi_{ms} - \varphi(x, y, -w/2) + \varepsilon_c \left(\frac{t_{ox}}{\varepsilon_{ox}}\right) \frac{\partial \varphi}{\partial z}\Big|_{(x,y,-w/2)} = 0 \tag{3.78}$$

Since the potential is symmetric with respect to the z-axis, the Eq (3.77) and Eq (3.78) lead to

$$\frac{\partial \varphi}{\partial z}\Big|_{(x,y,0)} = 0 \tag{3.79}$$



(a)



(b)

Figure 3.13: Cross section of the non-planar trigate QWFET in (a) the yz plane (perpendicular to the channel direction) and (b) the xy plane (along the channel direction)

where w is the fin width, while h is the fin height. The potential $\varphi(x,y,z)$ will be represented as the sum of two terms: $\varphi_{2D}(y,z)$, which is the solution of the 2D Poisson's equation for the cross-section of the channel, and $\varphi_{3D}(x,y)$, which is the solution of the Laplace equation along the length of the channel:

$$\varphi(x,y,z) = \varphi_{2D}(y,z) + \varphi_{3D}(x,y,z) \tag{3.80}$$

$\varphi_{2D}(y,z)$ is the solution to the 2D Poisson's equation for the device cross-section:

$$\nabla^2 \varphi_{2D}(y,z) = \frac{q}{\varepsilon_c} n_i \exp\left(\varphi_{2D}(y,z)/V_T\right) \tag{3.81}$$

where $\varphi_{2D}(y,z)$ is sum of the solution of 1D Poisson's equation in the y direction, $\varphi_y(y)$ and the solution of 2D residual Poisson's equation, $\varphi_{yz}(y,z)$, i.e.

$$\varphi_{2D}(y,z) = \varphi_y(y) + \varphi_{yz}(y,z) \tag{3.82}$$

where $\varphi_y(y)$ is the solution of

$$\frac{\partial^2}{\partial y^2}\varphi_y(y) = \frac{q}{\varepsilon_c} n_i \exp\left(\varphi_y(y)/V_T\right) \tag{3.83}$$

with the following boundary conditions

$$\frac{\partial \varphi_y}{\partial y}\Big|_{y=0} = 0 \tag{3.84}$$

$$V_{GS} - \varphi_{ms} + qN_d d_d\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d}{2\varepsilon_d} + \frac{d_{s1}}{\varepsilon_d}\right) - \varphi_y(h,z)$$
$$-\varepsilon_c\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d + d_{s1} + d_{s2}}{\varepsilon_d}\right)\frac{\partial \varphi_y}{\partial y}\Big|_{(h,z)} = 0 \tag{3.85}$$

The solution to Eq. (3.83) can be expressed as

$$\varphi_y(y) = V_T In\left[\frac{2V_T B^2 \varepsilon_c}{n_i q} sec^2(By)\right] \tag{3.86}$$

where B is given by

$$V_{GS}' - 2\varepsilon_c V_T B tan(Bh)\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d + d_{s1} + d_{s2}}{\varepsilon_d}\right) - V_T In\left[\frac{2V_T B^2 \varepsilon_c}{n_i q} sec^2(Bh)\right] = 0$$

(3.87)

where, $$V_{GS}' = V_{GS} - \varphi_{ms} + qN_d d_d\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d}{2\varepsilon_d} + \frac{d_{s1}}{\varepsilon_d}\right) \tag{3.88}$$

$\varphi_{yz}(y,z)$ is the solution of residual Poisson's equation

$$\frac{\partial^2}{\partial y^2}\varphi_{yz} + \frac{\partial^2}{\partial z^2}\varphi_{yz} = \frac{q}{\varepsilon_c} n_i \exp\left(\frac{\varphi_y}{V_T}\right)\left[\exp\left(\frac{\varphi_{yz}}{V_T}\right) - 1\right] \tag{3.89}$$

Considering the $\frac{\varphi_{yz}}{V_T}$ to be small and expanding exp $(\frac{\varphi_{yz}}{V_T})$ by Taylor's expansion, Eq. (3.89) can be simplified into

$$\frac{\partial^2}{\partial y^2}\varphi_{yz} + \frac{\partial^2}{\partial z^2}\varphi_{yz} \approx 2B^2 sec^2(By)\varphi_{yz} \tag{3.90}$$

Using separation of variable method, $\varphi_{yz}\,(y,z)$ can be expressed as $f(y)g(z)$, where $f(y)$ and $g(z)$ can be found by solving the equations:

$$\frac{f''(y)}{f(y)} = 2B^2 sec^2(By) - m^2 \tag{3.91}$$

$$\frac{g''(z)}{g(z)} = m^2 \tag{3.92}$$

where *m* is the separation factor, i.e. the eigen value. After some mathematical manipulation, $f(y)$ and $g(z)$ can be expressed as [53]

$$f(y) = cos^2(By) \tag{3.93}$$

$$g(z) = C[\exp(mz) + \exp(-mz)] \tag{3.94}$$

Here the eigen value, *m* is approximated to be equal to $2B$. Hence $\varphi_{yz}\,(y,z)$ can be written as

$$\varphi_{yz}\,(y,z) \;= C[\exp(2Bz) + \exp(-2Bz)]cos^2(By) \tag{3.95}$$

where *C* is derived from boundary conditions in Eqs. (3.77) and (3.78):

$$C = \frac{V_{GS}-\varphi_{ms}}{\exp(Bw)\left[1+2B\frac{\varepsilon_c t_{ox}}{\varepsilon_{ox}}\right]cos^2(Bh)+\exp(-Bw)\left[1-2B\frac{\varepsilon_c t_{ox}}{\varepsilon_{ox}}\right]cos^2(Bh)} \tag{3.96}$$

Hence $\varphi_{2D}\,(y,z)$ is obtained by adding $\varphi_{yz}\,(y,z)$ and $\varphi_y\,(y)$. The potential distribution of the cross section of the non-planar QWFET, $\varphi_{2D}\,(y,z)$ is shown in Figure 3.14. Now the solution to the 3D Laplace equation has to be obtained with the following boundary conditions:

$$\varphi_{3D}\,(0,y,z) = V_{bi} - \varphi_{2D}\,(y,z) \tag{3.97}$$

$$\varphi_{3D}\,(0,y,z) = V_{bi} + V_{DS} - \varphi_{2D}\,(y,z) \tag{3.98}$$

$$-\varphi_{3D}\,(x,h,z) - \varepsilon_c\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d+d_{s1}+d_{s2}}{\varepsilon_d}\right)\frac{\partial\varphi_{3D}}{\partial y}\Big|_{(x,h,z)} = 0 \tag{3.99}$$

$$\frac{\partial\varphi_{3D}}{\partial y}\Big|_{(x,0,z)} = 0 \tag{3.100}$$

$$-\varphi_{3D}\,(x,y,w/2) - \varepsilon_c\left(\frac{t_{ox}}{\varepsilon_{ox}}\right)\frac{\partial\varphi_{3D}}{\partial z}\Big|_{(x,y,w/2)} = 0 \tag{3.101}$$

$$\frac{\partial\varphi_{3D}}{\partial z}\Big|_{(x,y,0)} = 0 \tag{3.102}$$

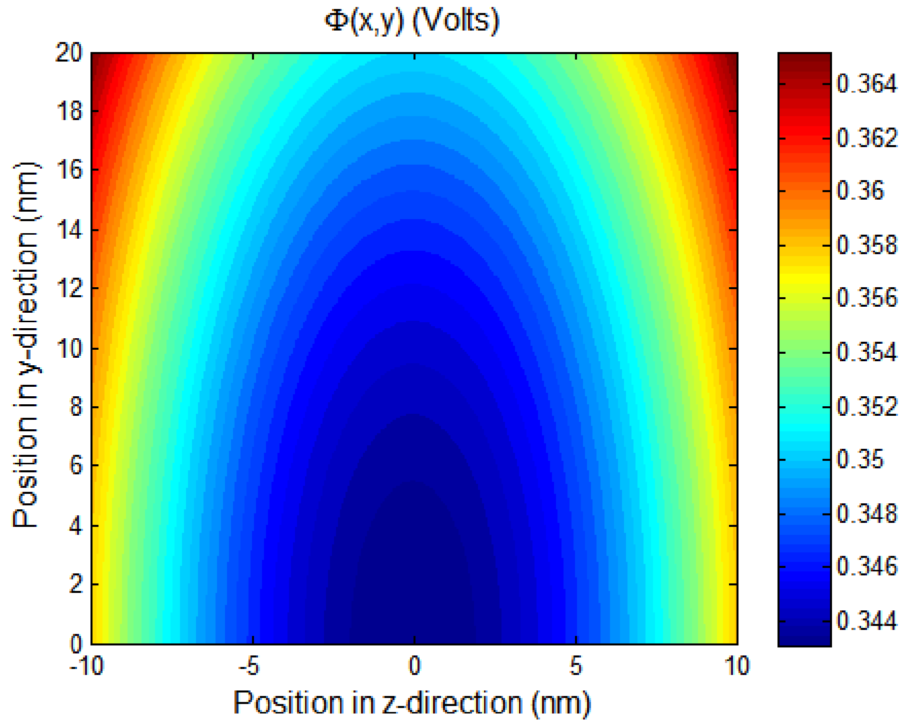


Figure 3.14: 2D potential distribution for trigate QWFET at the yz plane normal to the channel direction, where $V_{GS} = 0.4V$, $h = 20nm$ and $d = 20nm$.

$\varphi_{3D}\,(x, y, z)$ is obtained using variable separation technique, i.e.

$$\varphi_{3D}\,(x, y, z) = u(x)v(y)w(z) \tag{3.103}$$

Substituting the expression of φ_{3D} in the Laplace equation and rearranging, we obtain,

$$\frac{u''(x)}{u(x)} + \frac{v''(y)}{v(y)} + \frac{w''(z)}{w(z)} = 0 \tag{3.104}$$

Choosing $\frac{u''(x)}{u(x)} = \lambda^2$, $\frac{v''(y)}{v(y)} = -{\lambda_y}^2$ and $\frac{w''(z)}{w(z)} = -{\lambda_z}^2$, the following solutions are obtained for $u(x)$, $v(y)$ and $w(z)$:

$$u(x) = A\exp(\lambda x) + B\exp\,(-\lambda x) \tag{3.105}$$

$$v(y) = C\cos(\lambda_y y) \tag{3.106}$$

$$w(z) = E\cos(\lambda_z z) \tag{3.107}$$

While the boundary conditions provide the values of λ, λ_y and λ_z :

$$\lambda_y \tan(\lambda_y h) = \left[\varepsilon_c\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d + d_{s1} + d_{s2}}{\varepsilon_d}\right)\right]^{-1} \tag{3.108}$$

$$\lambda_z \tan(\lambda_z h) = \left[\varepsilon_c\left(\frac{t_{ox}}{\varepsilon_{ox}}\right)\right]^{-1} \tag{3.109}$$

$$\lambda^2 = {\lambda_y}^2 + {\lambda_z}^2 \tag{3.110}$$

Hence $\varphi_{3D}\,(x, y, z)$ is given by

$$\varphi_{3D}(x, y, z) = [C_0 \exp(\lambda x) + C_1 \exp\,(-\lambda x)] \cos(\lambda_y y) \cos(\lambda_z z) \tag{3.111}$$

C_0 and C_1 are solved using the Dirichlet boundary conditions in Eqs. (3.49) and (3.50):

$$C_0 = \frac{[V_{bi} - \varphi_{2D}(h, w/2)][1 - \exp(-\lambda L)] + V_{DS}}{[\exp(\lambda L) - \exp(-\lambda L)] \cos\,(\lambda_y h) \cos\,(\lambda_z w/2)} \tag{3.112}$$

$$C_1 = \frac{[V_{bi} - \varphi_{2D}(h, w/2)][\exp(\lambda L) - 1] - V_{DS}}{[\exp(\lambda L) - \exp(-\lambda L)] \cos\,(\lambda_y h) \cos\,(\lambda_z w/2)} \tag{3.113}$$

Now $\varphi_{2D}\,(y, z)$ and $\varphi_{3D}\,(x, y, z)$ are added to obtain the 3D potential for non-planar QWFET in the subthreshold region. The potential distribution, $\varphi(x, y, z)$ is plotted in Figure 3.15 for the xy-plane at the channel center.

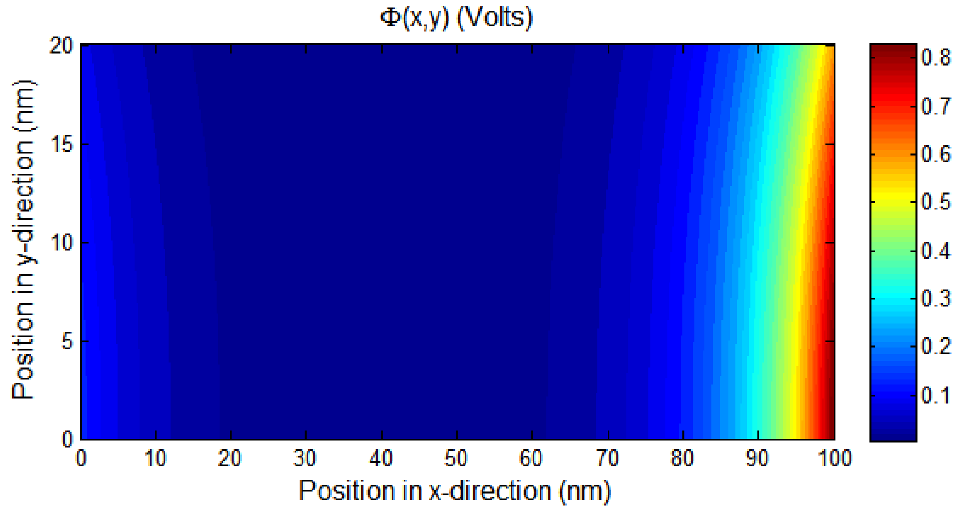


Figure 3.15: 2D potential distribution for trigate QWFET at the xy-plane along the channel direction, where $V_{GS} = 0.4V$, $h = 20nm$, $d = 20nm$, $V_{DS} = 0.5V$, $V_{bi} = 0.5V$ and $L = 100nm$..

3.4 Conclusion

The mathematical models for the channel potentials of multiple QWFET structures are developed in this chapter. In the following chapter, the expressions of the potential distribution are used to model subthreshold swing, threshold voltage and drain induced barrier lowering of the QWFET structures.

CHAPTER 4
MODELS FOR THRESHOLD VOLTAGE AND SUBTHRESHOLD SWING

4.1 Introduction

In this chapter, models for threshold voltage and subthreshold swing are developed for both planar and non-planar InGaAs QWFETs with Al_2O_3 gate dielectric. The potential distribution model described in the previous chapter is employed to develop these models.

4.2 Design Trade-Off

The threshold voltage can be defined by the *maximum transconductance method* [54]. According to this method, threshold voltage can be determined by drawing a tangent to the I_D–V_{GS} characteristics at the point of peak transconductance and finding the voltage where the tangent line intercepts the V_{GS}-axis. As the gate voltage drops below the threshold value, i.e. at the subthreshold region the logarithm of the drain current decreases with the decreasing gate voltage at an almost constant rate. The inverse of the $log(I_D)$ vs. V_{DS} curve at the subthreshold region is defined as the subthreshold swing (*SS*), which signifies the rate at which the drain current diminishes below threshold. The value of drain current at zero gate voltage is denoted as the off-state leakage current, I_{OFF} and it is directly related to the value of subthreshold swing. In order to minimize the off-state power consumption, the leakage current has to be minimized. It can be seen from Figure 4.1 (a) that the lower subthreshold swing implies lower subthreshold leakage current.

However, as the power supply voltage (V_{DD}) is being scaled, the threshold voltage (V_{TH}) has to be lower in order to facilitate a sufficiently high drain current, since it is directly related to the V_{DD}-V_{TH}. On the other hand, a lower threshold voltage invariably leads to a higher off-state leakage current if the subthreshold swing remains the same, as seen from Figure 4.1 (b). Since the subthreshold leakage current prevents the downscaling of threshold voltage, the supply voltage is more difficult to scale than the other device

parameters. According to ITRS Reports 2013 Edition, the power supply scaling remains as one of the most crucial long-term challenges, which requires scaling of power supply while supplying sufficient drive current and maintaining a low subthreshold current or subthreshold swing [1].

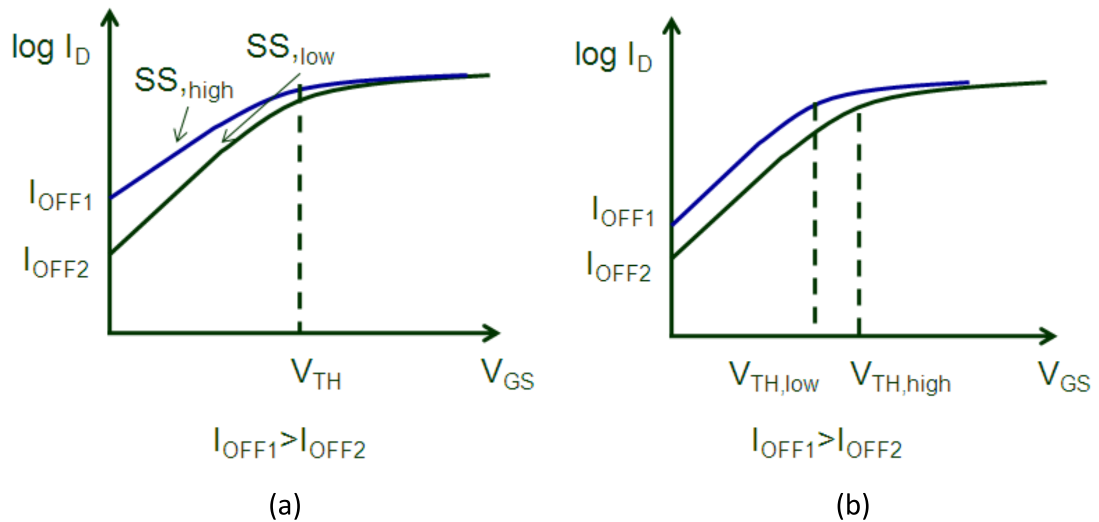


Figure 4.1 : Relations between off-state leakage current, threshold voltage and subthreshold swing

It can be observed from the scaling trends of supply voltage, that it has not been aggressively scaled due to these trade-offs. ITRS predicts that the supply voltage will approach the regime of 0.6 V within a few years as shown in Figure 4.2. This fact along with the continuing increase of current density (per area) causes the dynamic power density to climb with scaling and to approach an unacceptable level. Alternate high-mobility channel materials like InGaAs can provide some solution to this problem by allowing more aggressive V_{DD} scaling via smaller subthreshold swing. Hence, the modeling of subthreshold characteristics of the high-mobility material devices is very important to understand their prospect in future technologies.

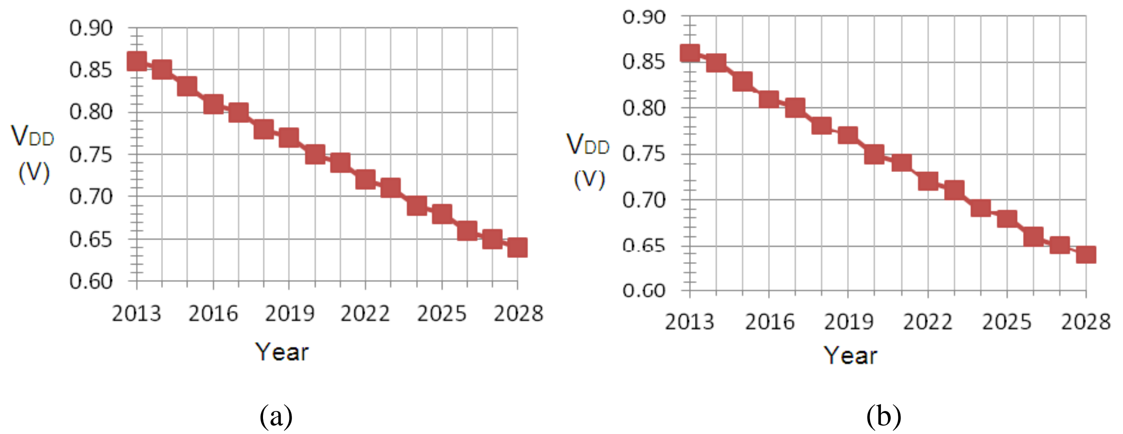


Figure 4.2: Predicted scaling trend of supply voltage for (a) logic high performance transistors and (b) logic low power transistors

4.3 Subthreshold Swing Model

Subthreshold current can be characterized by the amount of carriers traveling in the channel over the potential barrier between the source and drain when the gate voltage is below the threshold value. Hence the number of electrons at the top of the barrier i.e. at the location of the minimum channel potential can be used to define the subthreshold swing. The location of the minimum potential in the channel-length direction is described as the "*virtual cathode*", which is of particular interest in device modeling. This location corresponds to the maximum potential barrier faced by the electrons traveling from source to drain. Figure 4.3 shows the process of subthreshold leakage over the barrier.

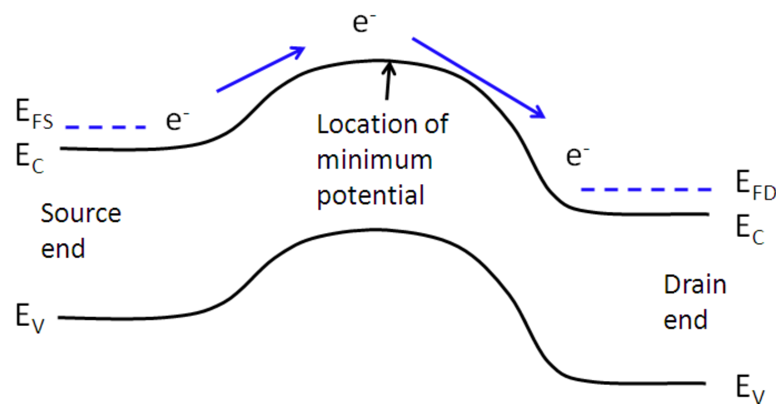


Figure 4.3: Injection of carrier from the source to the drain over the potential barrier

We can obtain the location of the *virtual cathode* by solving the equation

$$\frac{\partial \varphi}{\partial x} = 0 \quad (4.1)$$

where, x_{min} is the location of virtual cathode in the channel direction, which is given by

$$x_{min} = \frac{1}{2\lambda} In(\frac{C_1}{C_0}) \quad (4.2)$$

The subthreshold drain current, I_D is proportional to the total amount of free electrons diffusing over the virtual cathode, i.e.

Non-planar structure: $$I_D \propto \int_{y=0}^{h} \int_{z=-w/2}^{w/2} n_i \exp\,(\frac{\varphi_{min}(y,z)}{V_T})\, dydz \quad (4.3)$$

Planar structure: $$I_D \propto \int_{y=0}^{h} n_i \exp\,(\frac{\varphi_{min}(y)}{V_T})\, dy \quad (4.4)$$

So the subthreshold swing, $SS = \frac{\partial V_{GS}}{\partial log I_D}$ can be expressed as

Non-planar structure: $$SS = V_T In(10) \left[\frac{\int_{y=0}^{h} \int_{z=-w/2}^{w/2} n_i \exp\,(\frac{\varphi_{min}}{V_T}) \frac{\partial \varphi_{min}}{\partial V_{GS}} dydz}{\int_{y=0}^{h} \int_{z=-w/2}^{w/2} n_i \exp\,(\frac{\varphi_{min}}{V_T}) dydz} \right]^{-1} \quad (4.5)$$

Planar structure: $$SS = V_T In(10) \left[\frac{\int_{y=0}^{h} n_i \exp\,(\frac{\varphi_{min}}{V_T}) \frac{\partial \varphi_{min}}{\partial V_{GS}} dy}{\int_{y=0}^{h} n_i \exp\,(\frac{\varphi_{min}}{V_T}) dy} \right]^{-1} \quad (4.6)$$

The expressions of subthreshold swing can be simplified by considering the value of the integrals fixed at the *effective conduction path*. Hence the subthreshold swing can be expressed as

$$SS = \begin{cases} 2.3 V_T\, \eta(y_C,\ z_C), & \text{for non-planar structure} \\ 2.3 V_T\, \eta(y_C), & \text{for planar structure} \end{cases} \quad (4.7)$$

where η is known as the subthreshold slope factor. For bulk devices, η is calculated from the inverse slope of the surface potential versus gate voltage characteristics, since most of the carriers are accumulated at the surface. However, in the case of undoped small-dimension QW channels, the conduction electrons could spread all over the channel. So the *effective conduction path* could be away from the surface in undoped devices [45]-[46]. It was reported that for trigate FinFET devices, the *effective conduction path* is very close to $y = h$ and $z = w/4$ [45]. It is observed that for the trigate QWFET, good results can be obtained by considering $y_C = h$ and $z_C = w/4$. In case of the single-gate and

double-gate devices the *effective conduction path* can be defined as: $y_C = d/2$ and $y_C = d/4$ respectively. So the subthreshold slope factor can be expressed as

$$\eta = \left(\frac{\partial \varphi_{min}}{\partial V_{GS}}\right)^{-1} \tag{4.8}$$

where φ_{min} is the potential at x_{min} and at effective conduction path.

4.3.1 Planar structure

For planar structures, $\frac{\partial \varphi_{min}}{\partial V_{GS}}$ can be expressed as

$$\frac{\partial \varphi_{min}}{\partial V_{GS}} = \frac{\partial \varphi(x_{min}, y_C)}{\partial \varphi_0(y_C)} \times \frac{\partial \varphi_0(y_C)}{\partial V_{GS}} \tag{4.9}$$

Similar expressions can be obtained for the SS of single-gate and double-gate QWFET by determining the derivatives from Eq. (4.9).

4.3.1.1 Single-gate QWFET

Using Eqs. (3.59)-(3.61) φ_{min} can be written as

$$\varphi_{min} = \varphi_0\left(\frac{d}{2}\right) + \left[\left[\alpha - \beta\varphi_0\left(\frac{d}{2}\right)\right]\exp(\lambda x_{min}) + \left[\gamma - \delta\varphi_0\left(\frac{d}{2}\right)\right]\exp(-\lambda x_{min})\right]\cos\left(\frac{\lambda d}{2}\right) \tag{4.10}$$

where,

$$\begin{aligned} \alpha &= \frac{V_{bi}[1-\exp(-\lambda L)]+V_{DS}}{[\exp(\lambda L)-\exp(-\lambda L)]\cos\left(\frac{\lambda d}{2}\right)} \\ \beta &= \frac{1-\exp(-\lambda L)}{[\exp(\lambda L)-\exp(-\lambda L)]\cos\left(\frac{\lambda d}{2}\right)} \\ \gamma &= \frac{V_{bi}[\exp(\lambda L)-1]-V_{DS}}{[\exp(\lambda L)-\exp(-\lambda L)]\cos\left(\frac{\lambda d}{2}\right)} \\ \delta &= \frac{\exp(\lambda L)-1}{[\exp(\lambda L)-\exp(-\lambda L)]\cos\left(\frac{\lambda d}{2}\right)} \end{aligned} \tag{4.11}$$

Rearranging Eq. 4.10 and setting $y_C = d/2$ we get can obtain

$$\frac{\partial \varphi(x_{min}, y_C)}{\partial \varphi_0(y_C)} = 1 - [\beta\exp(\lambda x_{min}) + \delta\exp(-\lambda x_{min})]\cos\left(\frac{\lambda d}{2}\right) \tag{4.12}$$

where

$$x_{min} = \frac{1}{2\lambda} In\left(\frac{\alpha - \beta\varphi_0^m}{\gamma - \delta\varphi_0^m}\right) \tag{4.13}$$

and

$$\varphi_0^m = \frac{\varphi_{sub_th} - [\alpha\exp(\lambda L/2) + \gamma\exp(-\lambda L/2)]\cos\left(\frac{\lambda d}{2}\right)}{1 - [\beta\exp(\lambda L/2) + \delta\exp(-\lambda L/2)]\cos\left(\frac{\lambda d}{2}\right)} \tag{4.14}$$

In this work, φ_{sub_th} is chosen to be 0.05V below the threshold potential at the *effective conduction path*, which is determined via numerical simulations. It is to be noted that the

value of φ_{sub_th} does not significantly alter the results as long as its value is in the subthreshold region.

Now $\frac{\partial\varphi_0(y_C)}{\partial V_{GS}}$ can be expressed as

$$\frac{\partial\varphi_0(y_C)}{\partial V_{GS}} = \frac{\partial\varphi_0(d/2)}{\partial B} / \frac{\partial V_{GS}}{\partial B} \tag{4.15}$$

where

$$\frac{\partial\varphi_0(d/2)}{\partial B} = \frac{2V_T}{B} + 2V_T\frac{d}{2}\tan\left(\frac{Bd}{2}\right) \tag{4.16}$$

$$\frac{\partial V_{GS}}{\partial B} = 2V_T\tan(Bd) + 2V_T\varepsilon_c Bd sec^2(Bd)\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d+d_{s1}+d_{s2}}{\varepsilon_d}\right) \tag{4.17}$$

B can be obtained by solving

$$\varphi_0^m = V_T In\left[\frac{2V_T B^2\varepsilon_c}{n_i q} sec^2\left(\frac{Bd}{2}\right)\right] \tag{4.18}$$

Since the value of $\frac{\partial\varphi_0(y_C)}{\partial V_{GS}}$ is close to one, the value of subthreshold swing can be approximated using Eqs. (4.7) and (4.8):

$$SS \approx \frac{2.3V_T}{1-[\beta\exp(\lambda x_{min})+\delta\exp(-\lambda x_{min})]\cos\left(\frac{\lambda d}{2}\right)} \tag{4.19}$$

4.3.1.2 Double-gate QWFET

Using a similar analysis, the expression of subthreshold-swing of double-gate can be derived:

$$SS \approx \frac{2.3V_T}{1-[\beta\exp(\lambda x_{min})+\delta\exp(-\lambda x_{min})]\cos\left(\frac{\lambda d}{4}\right)} \tag{4.20}$$

where

$$\beta = \frac{1-\exp(-\lambda L)}{[\exp(\lambda L)-\exp(-\lambda L)]\cos\left(\frac{\lambda d}{4}\right)}$$
$$\delta = \frac{\exp(\lambda L)-1}{[\exp(\lambda L)-\exp(-\lambda L)]\cos\left(\frac{\lambda d}{4}\right)} \tag{4.21}$$

and x_{min} can be obtained by substituting $y_C = d/4$ in Eqs. (4.13)-(4.14).

4.3.2 Non-planar structure

In case of non-planar structures, $\frac{\partial\varphi_{min}}{\partial V_{GS}}$ can be expressed as

$$\frac{\partial\varphi_{min}}{\partial V_{GS}} = \frac{\partial\varphi(x_{min}, y_C, z_C)}{\partial\varphi_{2D}(y_C, z_C)} \times \frac{\partial\varphi_{2D}(y_C, z_C)}{\partial V_{GS}} \tag{4.20}$$

where $\varphi_{2D}(y,z)$ is the 2D potential given by Eq. (3.82). Following the steps described in subsection 4.3.1, the expression for $\frac{\partial\varphi(x_{min}, y_C, z_C)}{\partial\varphi_{2D}(y_C, z_C)}$ can be obtained

$$\frac{\partial\varphi(x_{min}, y_C, z_C)}{\partial\varphi_{2D}(y_C, z_C)} = 1 - [\beta \exp(\lambda x_{min}) + \delta \exp(-\lambda x_{min})] \cos(\lambda_y h) \cos\left(\frac{\lambda_z w}{4}\right) \quad (4.21)$$

where

$$\alpha = \frac{V_{bi}[1-\exp(-\lambda L)]+V_{DS}}{[\exp(\lambda L)-\exp(-\lambda L)]\cos(\lambda_y h)\cos\left(\frac{\lambda_z w}{4}\right)}$$
$$\beta = \frac{1-\exp(-\lambda L)}{[\exp(\lambda L)-\exp(-\lambda L)]\cos(\lambda_y h)\cos\left(\frac{\lambda_z w}{4}\right)}$$
$$\gamma = \frac{V_{bi}[\exp(\lambda L)-1]-V_{DS}}{[\exp(\lambda L)-\exp(-\lambda L)]\cos(\lambda_y h)\cos\left(\frac{\lambda_z w}{4}\right)} \quad (4.22)$$
$$\delta = \frac{\exp(\lambda L)-1}{[\exp(\lambda L)-\exp(-\lambda L)]\cos(\lambda_y h)\cos\left(\frac{\lambda_z w}{4}\right)}$$

The location of minimum potential, x_{min} is given by Eq. (4.13) where φ_0^m is modified for non-planar structure:

$$\varphi_0^m = \frac{\varphi_{sub_th}-[\alpha\exp(\lambda L/2)+\gamma\exp(-\lambda L/2)]\cos(\lambda_y h)\cos\left(\frac{\lambda_z w}{4}\right)}{1-[\beta\exp(\lambda L/2)+\delta\exp(-\lambda L/2)]\cos(\lambda_y h)\cos\left(\frac{\lambda_z w}{4}\right)} \quad (4.23)$$

Considering the value of $\frac{\partial\varphi_{2D}(y_C, z_C)}{\partial V_{GS}}$ is close to one, the approximate value of subthreshold swing can be obtained from Eqs.(4.7)-(4.8):

$$SS \approx \frac{2.3V_T}{1-[\beta\exp(\lambda x_{min})+\delta\exp(-\lambda x_{min})]\cos(\lambda_y h)\cos\left(\frac{\lambda_z w}{4}\right)} \quad (4.24)$$

4.4 Threshold Voltage Model

In a QWFET device, the threshold voltage can be found numerically by the *maximum transconductance method*. Analytically, the threshold condition could be defined by the potential of the effective conduction path at the top of the drain-source. At threshold condition, this potential (φ_{TH}) is extracted by simulation. The threshold voltage, V_{TH} is modeled using the value of φ_{TH}.

4.4.1 Planar structure

In the planar structure, at threshold condition occurs when

$$\varphi(x_{min}, y_C) = \varphi_{TH} \quad (4.25)$$

The potential $\varphi(x, y)$ of a planar QWFET consists of two terms: a one-dimensional potential and a two-dimensional potential term. Since the 1D potential is a function gate voltage (V_{GS}), it is necessary to extract the 1D potential at the *effective conduction path* in the threshold condition (φ_{TH_1D}). Using Eqs. (3.59)-(3.61), φ_{TH} and φ_{TH_1D} can be related by the equation:

$$\varphi_{TH} = \varphi_{TH_1D} + \left[[\alpha - \beta\varphi_{TH_1D}]\exp(\lambda x_{min}) + [\gamma - \delta\varphi_{TH_1D}]\exp(-\lambda x_{min})\right]\cos(\lambda y_C) \quad (4.26)$$

where α, β, γ and δ are parameters defined in section 4.3.

$$\varphi_{TH_1D} = \frac{\varphi_{TH}-[\alpha\exp(\lambda x_{min})+\gamma\exp(-\lambda x_{min})]\cos(\lambda y_C)}{1-[\beta\exp(\lambda x_{min})+\delta\exp(-\lambda x_{min})]\cos(\lambda y_C)} \quad (4.27)$$

The value of x_{min} is found by Eq. (4.13). The threshold value of the parameter, B is denoted as B_{TH}, which is extracted from the equation:

$$\varphi_{TH_1D} = V_T In\left[\frac{2V_T {B_{TH}}^2\varepsilon_c}{n_i q}sec^2(B_{TH}y_C)\right] \quad (4.28)$$

The value of B_{TH} is used to find the threshold voltage, V_{TH} with the aid of Eq. (3.46) (for single-gate structure) or Eq. (3.69) (for double-gate structure). The threshold voltage is given by

$$V_{TH} = \varphi_{ms} - qN_d d_d\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d}{2\varepsilon_d} + \frac{d_{s1}}{\varepsilon_d}\right) + 2\varepsilon_c V_T B_{TH} tan(2B_{TH}y_C)\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d+d_{s1}+d_{s2}}{\varepsilon_d}\right) + V_T In\left[\frac{2V_T {B_{TH}}^2\varepsilon_c}{n_i q}sec^2(2B_{TH}y_C)\right] \quad (4.29)$$

4.4.2 Non-planar structure

For the non-planar structure, the threshold condition is defined by

$$\varphi(x_{min}, y_C, z_C) = \varphi_{TH} \quad (4.30)$$

Since the potential of the non-planar structure contains a 2D potential term and a 3D potential term, the value of the 2D potential at *effective conduction path* is extracted by

$$\varphi_{TH_2D} = \frac{\varphi_{TH}-[\alpha\exp(\lambda x_{min})+\gamma\exp(-\lambda x_{min})]\cos(\lambda_y h)\cos\left(\frac{\lambda_z w}{4}\right)}{1-[\beta\exp(\lambda x_{min})+\delta\exp(-\lambda x_{min})]\cos(\lambda_y h)\cos\left(\frac{\lambda_z w}{4}\right)} \quad (4.31)$$

The values of α, β, γ and δ can be found from subsection 4.3.2.

So the threshold condition occurs when

$$\varphi_{TH_2D} = \varphi_{2D}(y_C, z_C) \quad (4.32)$$

With the aid of Eq. (3.86) and Eq. (3.95), $\varphi_{2D}(y_C, z_C)$ can be expressed as

$$\varphi_{TH_2D} = C\left[\exp\left(\frac{B_{TH}w}{2}\right) + \exp\left(-\frac{B_{TH}w}{2}\right)\right]cos^2(B_{TH}h) + V_T In\left[\frac{2V_T {B_{TH}}^2\varepsilon_c}{n_i q}sec^2(B_{TH}h)\right] \quad (4.33)$$

where *C* is found by mathematical manipulation of Eqs. (3.85) and (3.96):

$$C = \left[-qN_d d_d \left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d}{2\varepsilon_d} + \frac{d_{s1}}{\varepsilon_d} \right) + 2\varepsilon_c V_T B_{TH} tan(B_{TH} h) \left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{cap}}{\varepsilon_{cap}} + \frac{d_d + d_{s1} + d_{s2}}{\varepsilon_d} \right) + V_T In \left[\frac{2V_T B_{TH}{}^2 \varepsilon_c}{n_i q} sec^2(B_{TH} h) \right] \right] / \left[\exp(B_{TH} w) \left[1 + 2B_{TH} \frac{\varepsilon_c t_{ox}}{\varepsilon_{ox}} \right] cos^2(B_{TH} h) + \exp(-B_{TH} w) \left[1 - 2B_{TH} \frac{\varepsilon_c t_{ox}}{\varepsilon_{ox}} \right] cos^2(B_{TH} h) \right] \quad (4.34)$$

Now Eq. (4.33) is numerically solved to find the value of B_{TH}. This value is substituted in the following equation to obtain the value of threshold voltage, V_{TH}.

$$V_{TH} = \varphi_{ms} + 2B_{TH} C \varepsilon_c \frac{t_{ox}}{\varepsilon_{ox}} [\exp(B_{TH} w) + \exp(-B_{TH} w)] cos^2(B_{TH} h) + C[\exp(B_{TH} w) + \exp(-B_{TH} w)] cos^2(B_{TH} h) + V_T In \left[\frac{2V_T B_{TH}{}^2 \varepsilon_c}{n_i q} sec^2(B_{TH} h) \right] \quad (4.35)$$

4.5 Drain-Induced Barrier Lowering

As the channel length is aggressively scaled, the potential barrier between the source and the drain is lowered. This effect is more pronounced at higher drain voltages as seen from the plot of mid-channel potential in Figure 4.4.

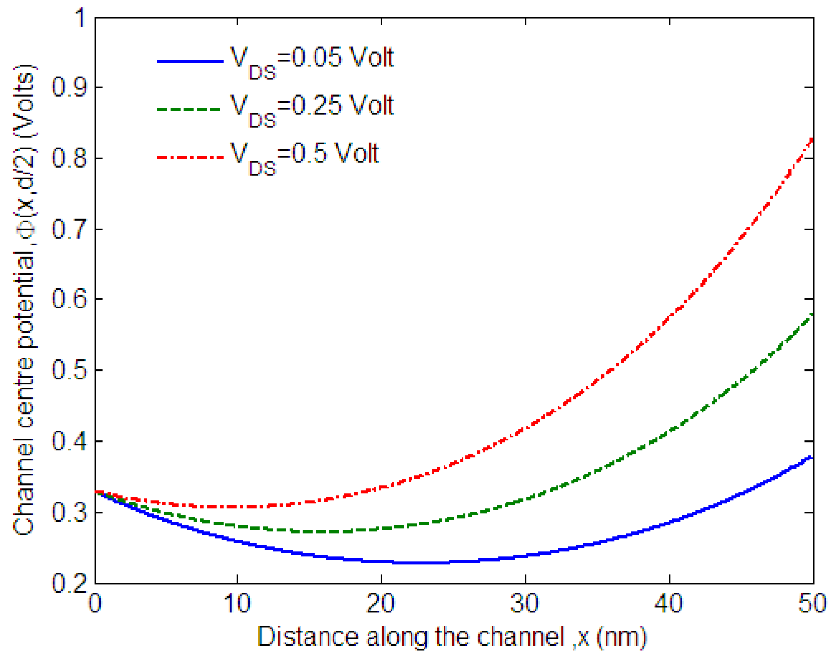


Figure 4.4: Effect of drain voltage on the channel potential and location of minimum potential for channel length, L=50 nm.

It can be observed that the higher the drain voltage, the higher is the value of minimum channel potential. The minimum channel potential corresponds to the top of the barrier between the source and the drain. The higher drain voltage raises the potential of the channel, i.e. the energy required for an electron to reach the top of the barrier gets lowered. Moreover, the location of minimum channel potential shifts towards the source end as the drain voltage is increased. The lowering of barrier due to drain voltage, i.e the *drain-induced barrier lowering effect* is more dominant in short channel devices. Figure 4.5 shows the mid-channel potential for different gate-lengths. The longer gate length has stronger control over the channel potential, so the drain-induced barrier lowering effect is less pronounced in long channel devices. However, in short-channel devices the drain voltage increases the minimum potential and lowers the threshold voltage. Hence it is important to characterize the drain-induced barrier lowering effect in short channel devices. The drain-induced barrier lowering (*DIBL*) parameter is defined as the change in threshold voltage with respect to the change in drain voltage.

$$DIBL = \frac{|V_{TH}(V_{DS,high}) - V_{TH}(V_{DS,low})|}{V_{DS,high} - V_{DS,low}} \qquad (4.36)$$

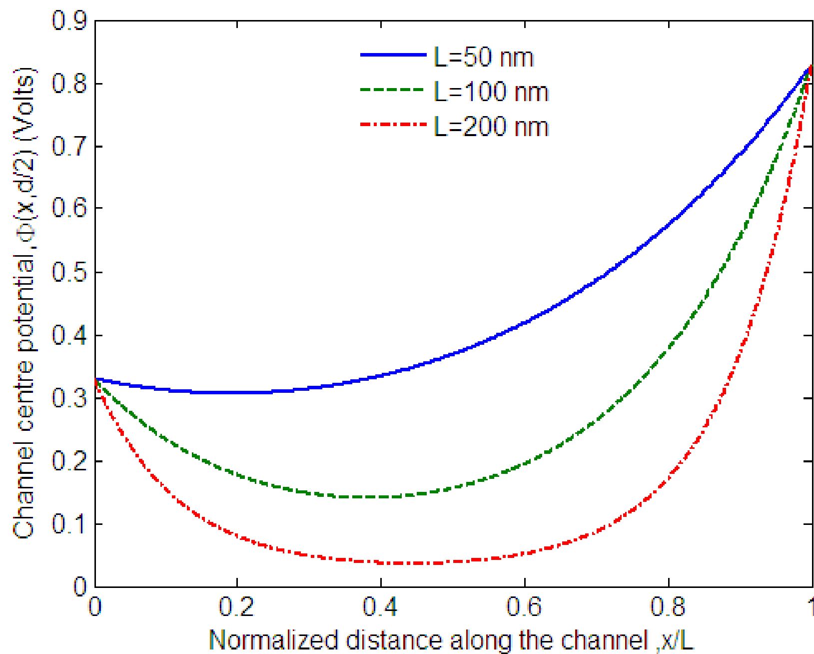


Figure 4.5: Effect of gate length on the channel potential and location of minimum potential for V_{DS}=0.5V

The lower *DIBL* signifies better performance of the device. In this work, DIBL is calculated considering $V_{DS,high}$ and $V_{DS,low}$ to be 0.5V and 50mV respectively.

4.6 Conclusion

In this chapter, models are proposed for extracting the threshold voltage and the subthreshold swing of QWFET devices. In the next chapter, the results obtained from these models are used to compare different QWFET structures in terms of threshold voltage, subthreshold swing and drain-induced barrier lowering.

CHAPTER 5
RESULTS AND DISCUSSIONS

5.1 Introduction

According to the analytical model proposed in the previous chapter, the subthreshold characteristics of the InGaAs QWFET device are defined and the corresponding results are presented in this chapter. Several parameters defining the subthreshold characteristics, i.e. subthreshold swing, threshold voltage and drain induced barrier lowering are extracted and illustrated here. Using the subthreshold swing model described in Section 4.3, the subthreshold swings of both planar and non-planar QWFET are obtained, while the threshold voltages are extracted for the same structures using the model introduced in Section 4.4. The results from the proposed model are compared with the device characteristics obtained from Silvaco ATLAS [55]. The default simulation parameters are shown in Table 5.1.

Table 5.1: Default device parameters used in analysis

Parameter	**Symbol**	**Values**
Channel length	L	100nm
Channel thickness (Planar)	d	15nm
Fin height	h	15nm
Fin width	w	15nm
Drain voltage	V_{DS}	0.5V
Donor layer thickness	d_d	8nm
Upper Barrier thickness	d_{s1}	2nm
Spacer thickness	d_{s2}	2nm
Doping of donor layer	N_d	10^{16}cm^{-3}
Gate dielectric thickness	t_{ox}	5nm
Cap layer thickness	t_{cap}	1nm
Metal-semiconductor work function	φ_{ms}	0.03V

5.2 Channel Length Variation

In this section, the effect of channel length variation are observed on the single-gate, double-gate and trigate QWFET structures, hence the short channel effects are observed. A comparative analysis is made on the performance of all three types of structures.

5.2.1 Effects on threshold voltage

The variation of threshold voltage with channel length for single-gate, double-gate and trigate QWFET structures are shown in Figure 5.1, Figure 5.2 and Figure 5.3 respectively. It can be observed from the figures, that the developed model shows good agreement with simulation results. However, the results from the model are found to deviate from the ATLAS simulation results when channel length is very small. It is to be noted that the variation of charge distribution due to the potential variation in the channel length direction was ignored while solving the Poisson's equation, i.e. the residual Poisson's equation was simplified to Laplace equation. While this simplification has negligible effects on the accuracy of long channel devices, the same assumption is not valid for the devices with strong short channel effects, which is the reason behind the discrepancies between analytical model and simulation results at short channel length and higher drain voltage.

Figure 5.4 compares threshold characteristics for single-gate, double-gate and trigate structure. At short channel length, the trigate QWFET has the largest threshold voltage among the three structures, which exhibits stronger enhancement mode operation. The larger threshold voltage is achieved by the superior gate control of the non-planar structure. Between the planar structures, the double-gate structure has the larger threshold voltage compared to the single-gate structure. It can be observed that the trigate structure is less sensitive to gate length scaling compared to its planar counterparts.

Figure 5.5 shows a comparison of the three structures of QWFET devices in terms of drain induced barrier lowering (DIBL), which demonstrates that the trigate device threshold voltage is more immune to changes in drain voltage.

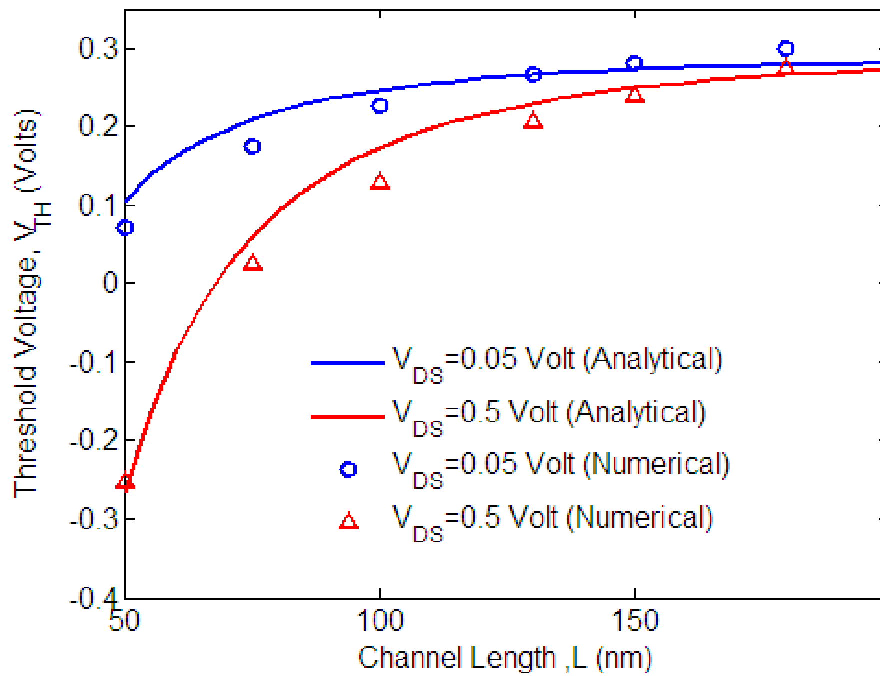


Figure 5.1: Variation of threshold voltage, V_{TH} with channel length, L for single-gate modulation doped QWFET.

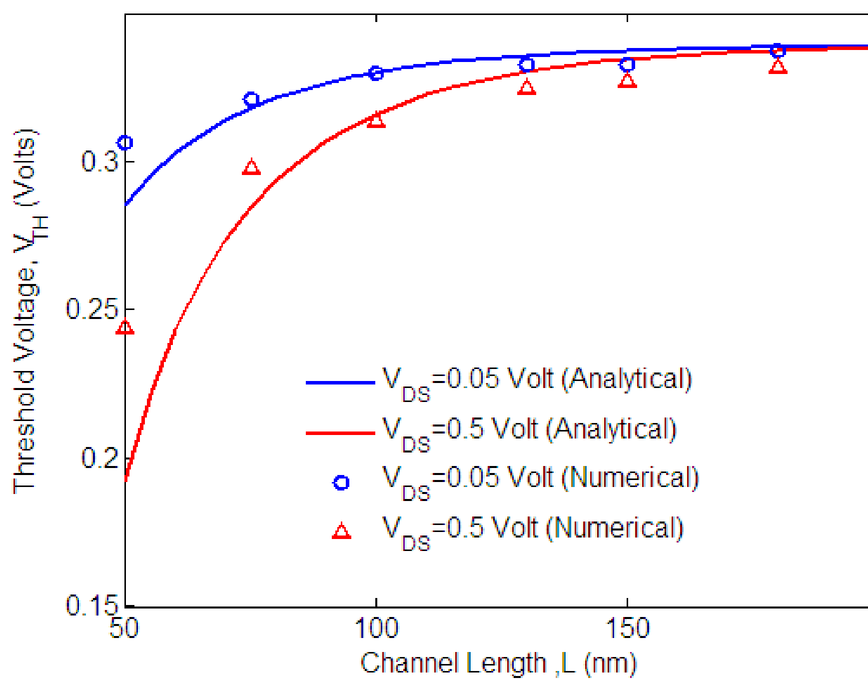


Figure 5.2: Variation of threshold voltage, V_{TH} with channel length, L for double-gate modulation doped QWFET.

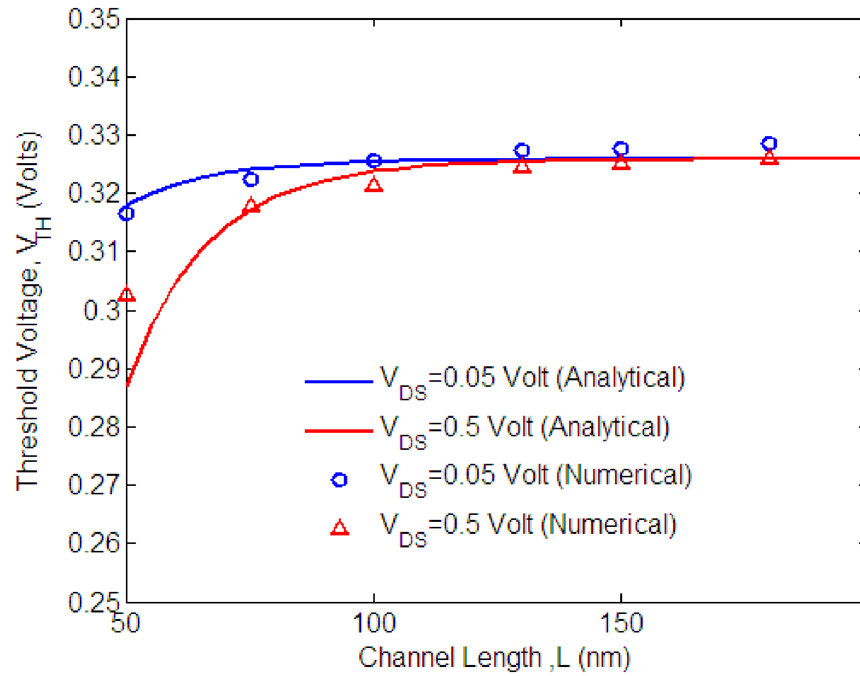


Figure 5.3: Variation of threshold voltage, V_{TH} with channel length, L for non-planar trigate modulation doped QWFET.

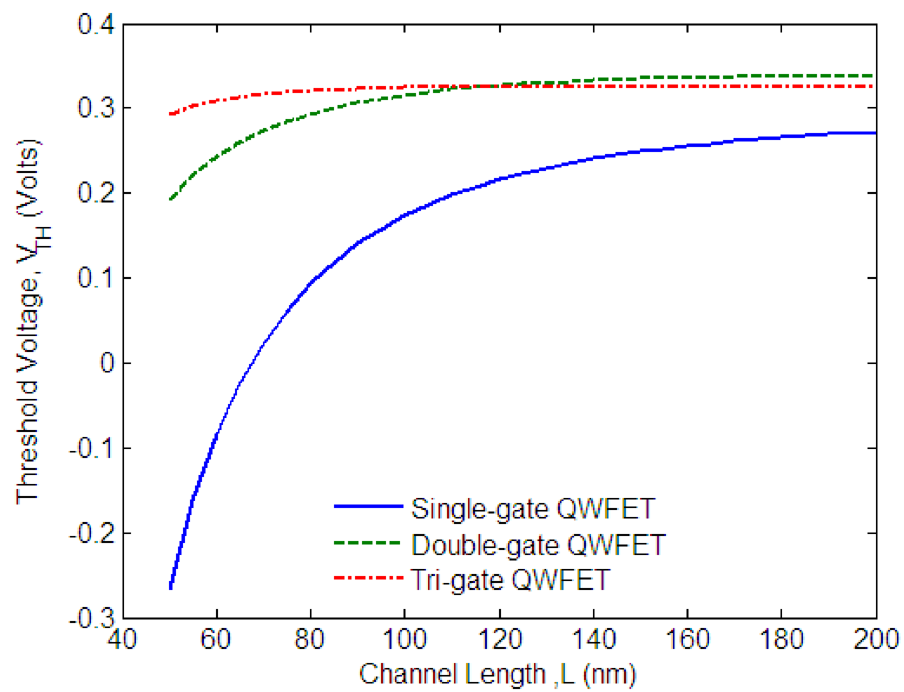


Figure 5.4: Effect of change in channel length, L on threshold voltage, V_{TH} for different configurations of QWFET (V_{DS} = 0.5V).

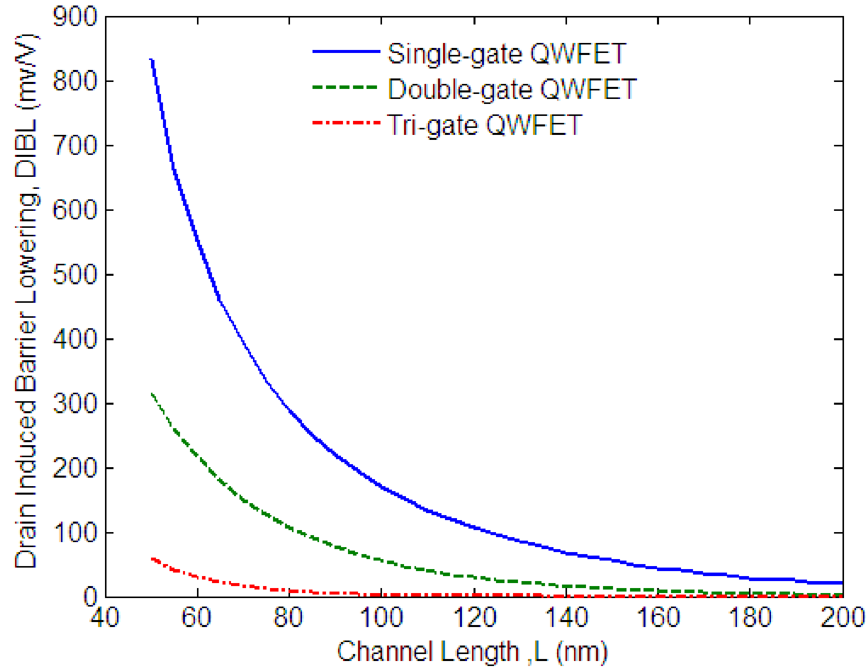


Figure 5.5: Effect of change in channel length, *L* on drain induced barrier lowering, *DIBL* for different configurations of QWFET.

5.2.2 Effects on subthreshold swing

The variation of subthreshold swing with channel length for single-gate, double-gate and trigate QWFET structures are shown in Figure 5.6, Figure 5.7 and Figure 5.8 respectively. The developed model shows good agreement with simulation results for small values of V_{DS}. The double-gate and the trigate structure models deviate from simulation results when V_{DS} values are large. However, the deviations are small. It can be observed that short channel devices have higher subthreshold swing values.

Subthreshold swing characteristics of single-gate, double-gate and trigate QWFET structures are compared in Figure 5.9. It is noted that the trigate structure has the smallest subthreshold swing value for any channel length and it approaches the 60mv/Dec limit for long channels and smaller drain voltages.

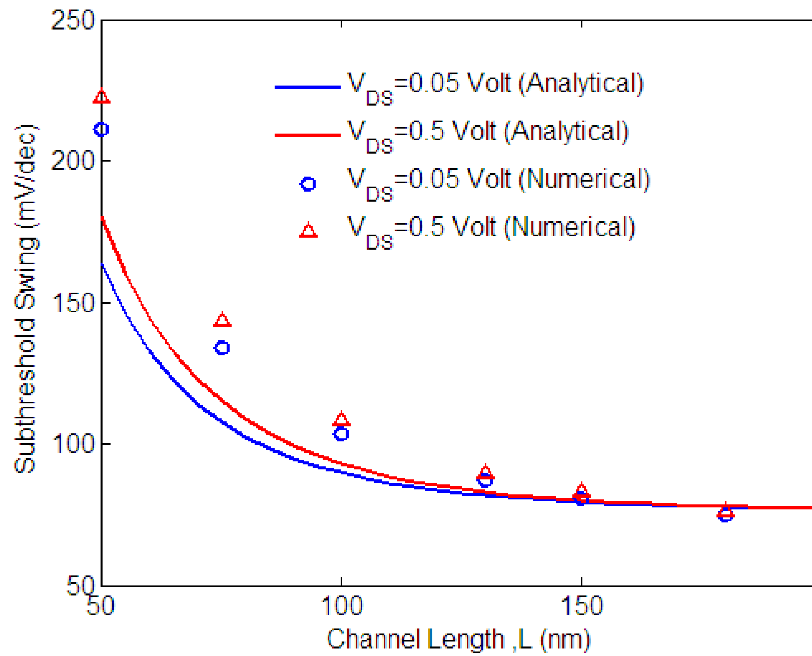


Figure 5.6: Variation of subthreshold swing, *SS* with channel length, *L* for single-gate modulation doped QWFET.

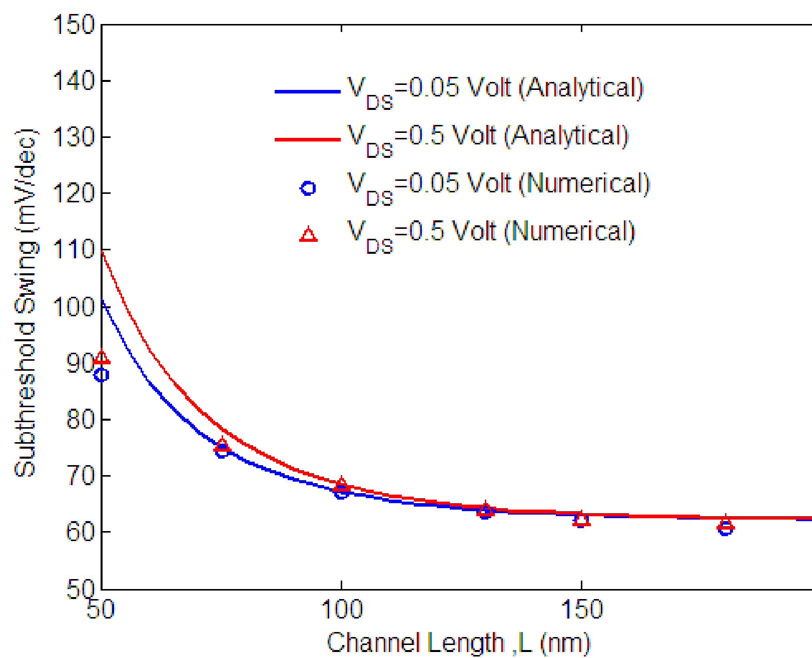


Figure 5.7: Variation of subthreshold swing, *SS* with channel length, *L* for double-gate modulation doped QWFET.

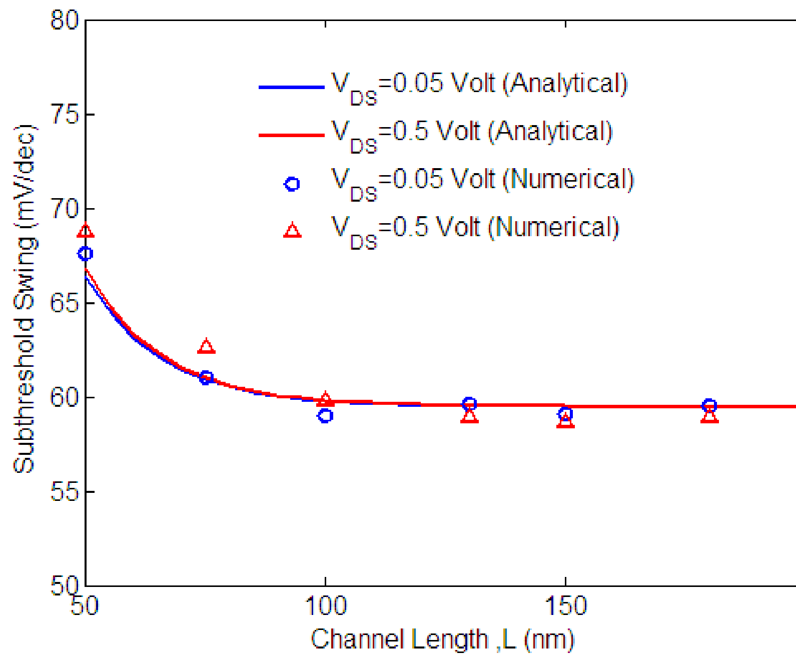


Figure 5.8: Variation of subthreshold swing, *SS* with channel length, *L* for trigate non-planar modulation doped QWFET.

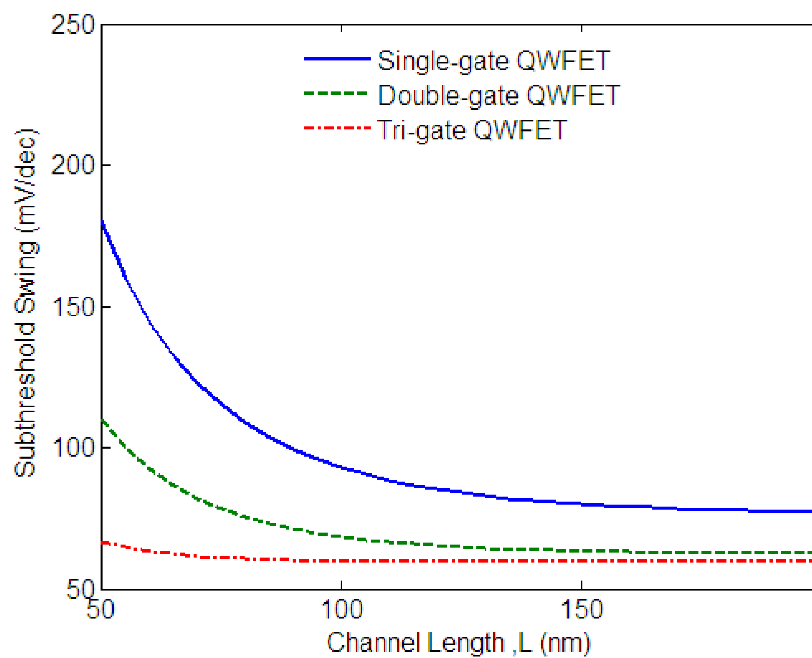


Figure 5.9: Effect of change in channel length, *L* on subthreshold swing, *SS* for different configurations of QWFET (V_{DS} = 0.5V).

5.3 Variation in Lateral Channel Dimensions

The effect of lateral channel dimensions on the threshold voltage and subthreshold swing of different QWFET structures are discussed in this section.

5.3.1 Effects on threshold voltage

Figure 5.10 and Figure 5.11 shows the effect of channel thickness on the threshold voltage of single-gate and double-gate QWFET structures respectively, while the effects of scaling the channel fin of non-planar trigate QWFET can be observed in Figure 5.12. The model shows satisfactory agreement with simulation results. It can be noted from the figures, that the threshold voltage becomes less immune to drain induced barrier lowering as the lateral dimensions are scaled for all the devices. Moreover, the drain voltage has least effect on the trigate QWFET. Additionally, the threshold voltage of the trigate QWFET can be adjusted by scaling either the fin height or the fin width, which provides further design flexibility.

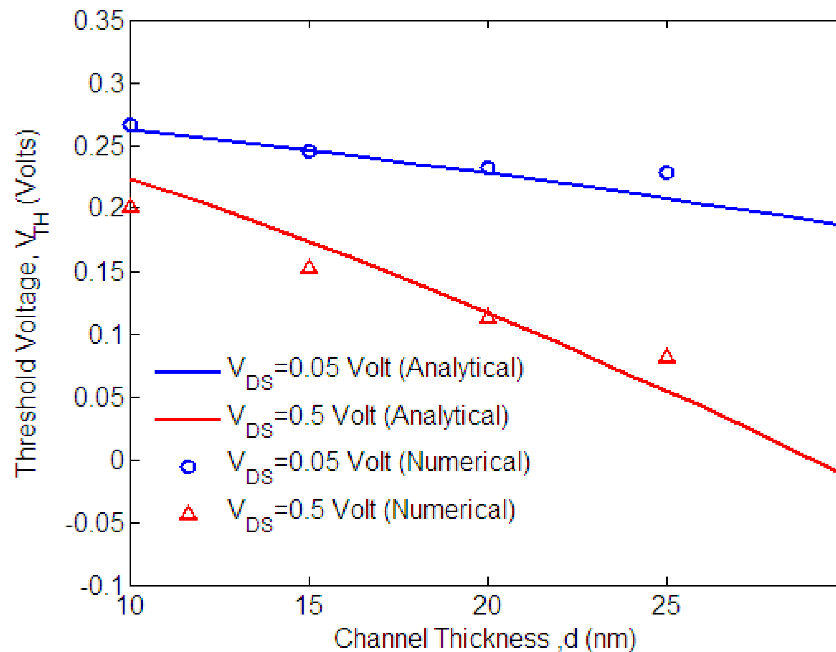


Figure 5.10: Variation of threshold voltage, V_{TH} with channel thickness, d for single-gate modulation doped QWFET .

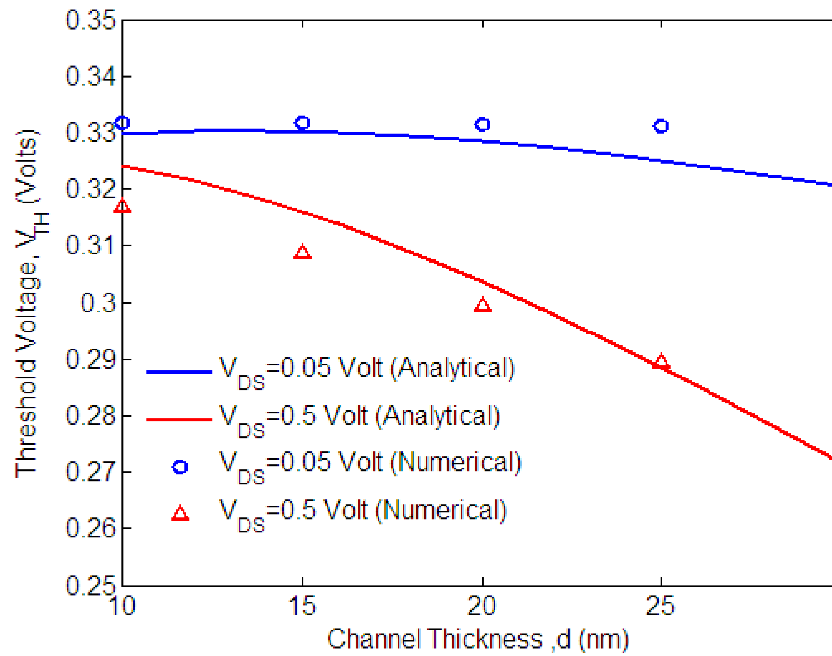


Figure 5.11: Variation of threshold voltage, V_{TH} with channel thickness, *d* for double-gate modulation doped QWFET.

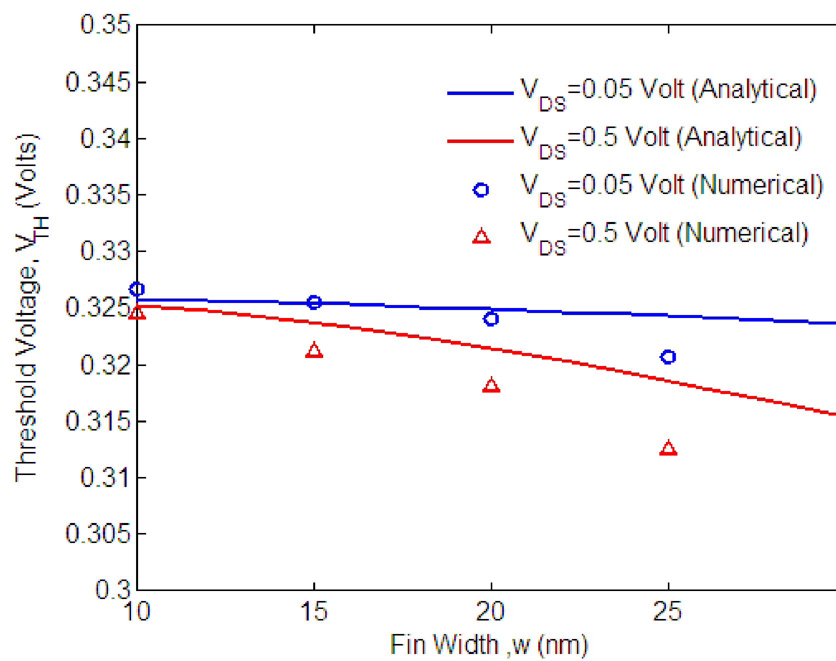


Figure 5.12: Variation of threshold voltage, V_{TH} with fin thickness, *w* for trigate non-planar modulation doped QWFET.

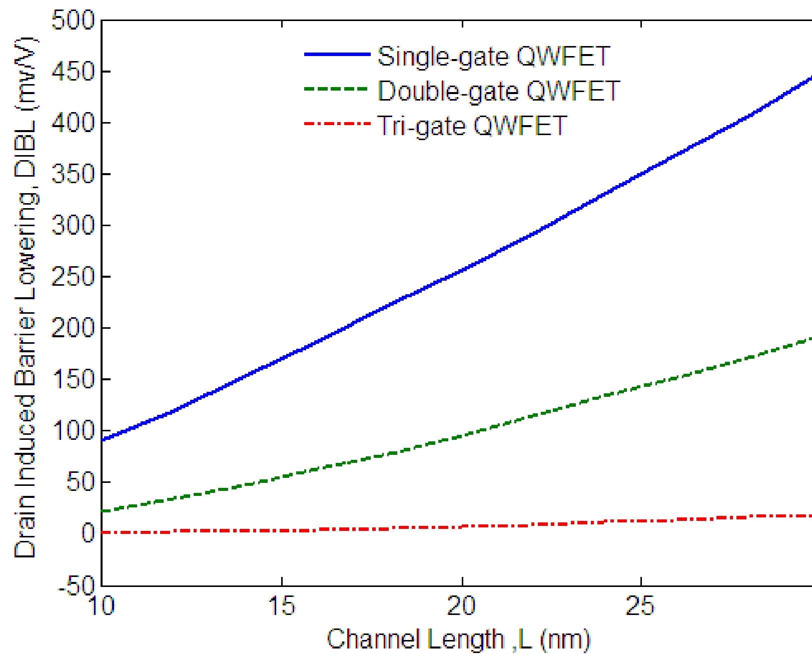


Figure 5.13: Effect of change in channel or fin thickness on drain induced barrier lowering, *DIBL* for different configurations of QWFET.

5.3.2 Effects on subthreshold swing

Figure 5.14 and Figure 5.15 show the effect of scaling channel thickness on the subthreshold swing of single-gate and double-gate QWFET devices. As the dimensions become smaller, the devices show smaller subthreshold swing. Between the two planar structures, the double gate QWFET has the better subthreshold value. Similar effects are observed in Figure 5.16 and Figure 5.17 for the scaling of fin height and fin width in the non-planar structure. For all three structures, increasing channel thickness results in increase in subthreshold swing. The single-gate and double-gate structure shows almost linear characteristics. For the trigate structure, the effect of channel thickness on subthreshold swing saturates at high channel thickness values. Results from the analytical model and simulation match closely for the single-gate and double-gate structure. The analytical model and simulation results vary slightly for the trigate structure. Figure 5.18 shows that subthreshold swing increases with the increase of fin thickness. The deviation is more pronounced for smaller dimensions due to neglecting some of the quantum mechanical effects.

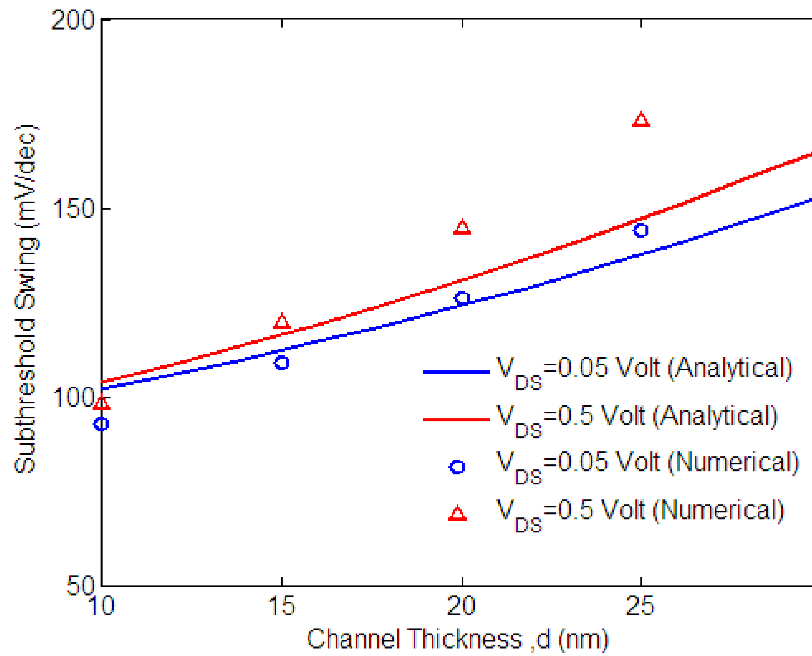


Figure 5.14: Variation of subthreshold swing, *SS* with channel thickness, *d* for single-gate modulation doped QWFET.

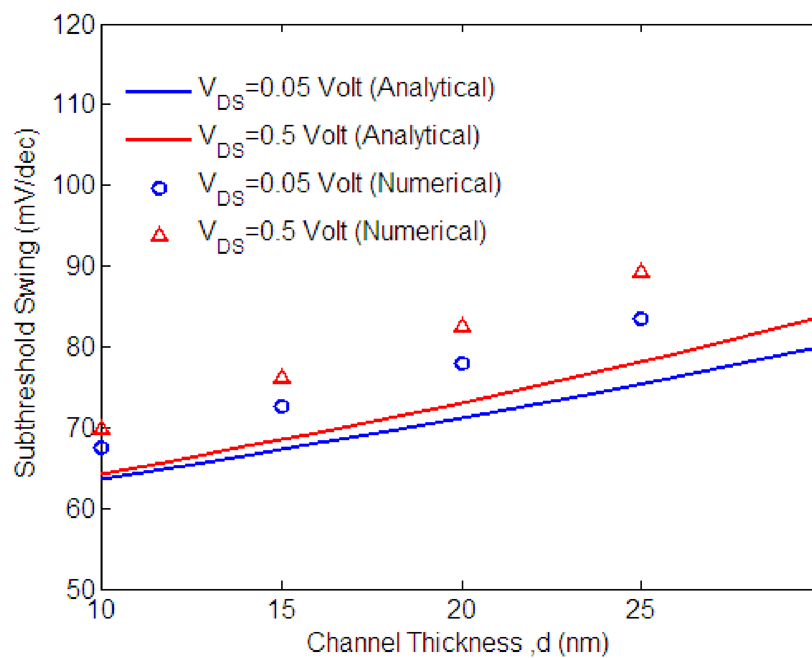


Figure 5.15: Variation of subthreshold swing, *SS* with channel thickness, *d* for double-gate modulation doped QWFET.

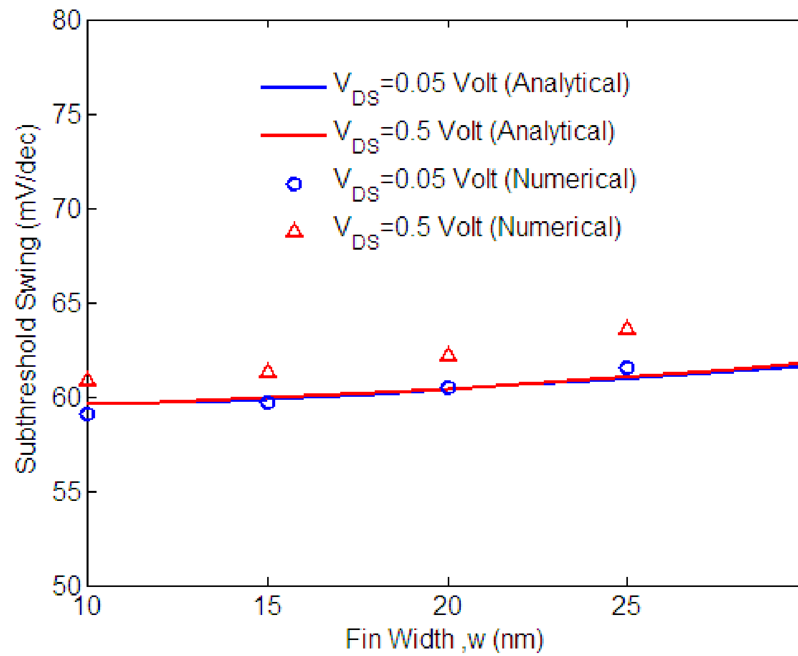


Figure 5.16: Variation of subthreshold swing, *SS* with fin height, *h* for trigate modulation doped QWFET.

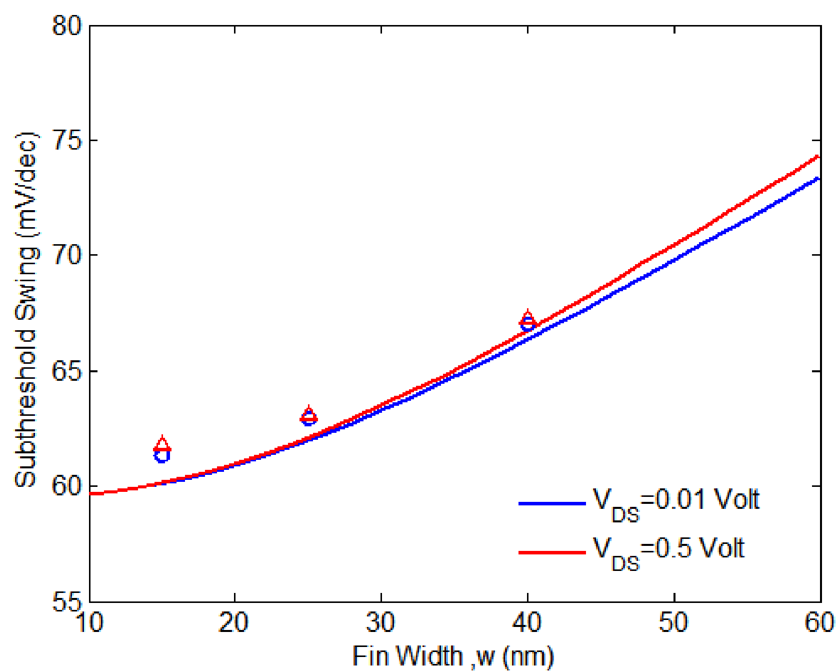


Figure 5.17: Variation of subthreshold swing, *SS* with fin thickness, *w* for trigate non-planar modulation doped QWFET.

5.4 Effect of Indium Concentration

The effects of indium concentration on the threshold voltage and subthreshold swing of non-planar trigate QWFET structure is discussed in this section. Figure 5.18 shows that the device with $In_{0.7}Ga_{0.3}As$ channel has a lower threshold voltage than the $In_{0.53}$ $Ga_{0.47}As$ device; i.e. higher indium concentration results in lower threshold voltage. Since the higher indium concentration increases the intrinsic carrier concentration and decreases the bandgap of InGaAs, the electron concentration is significantly larger in the In-rich channel for the same gate voltage. This results in a lower threshold voltage in channels with higher indium concentration. Figure 5.19 depicts that the subthreshold swing is slightly larger for the indium-rich QWFET. Since at the subthreshold region of trigate QWFET, the change in minimum potential in the effective conduction path with respect to the gate voltage is a weak function of intrinsic carrier concentration, the subthreshold swings are found to be similar for both materials.

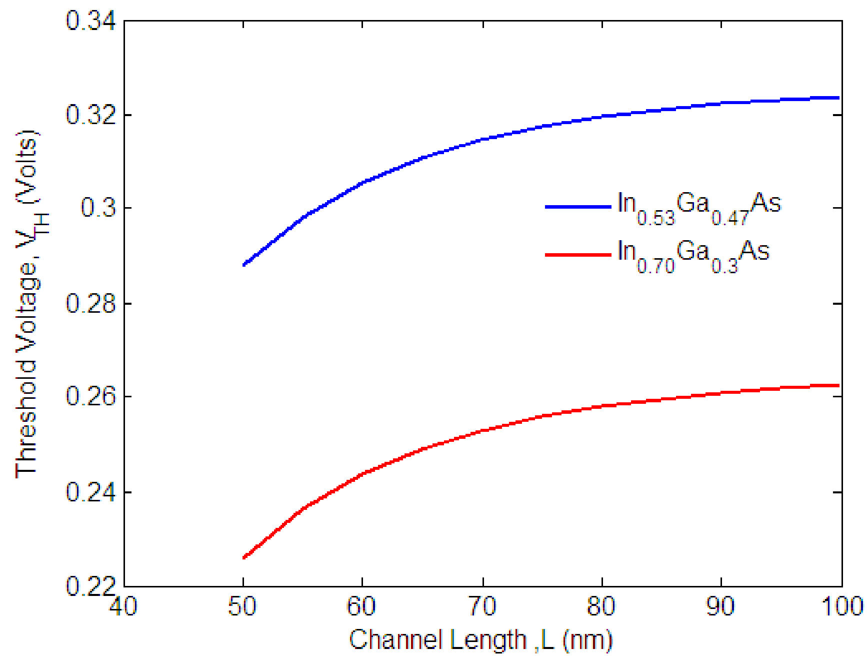


Figure 5.18: Effect of change in indium content in the channel of trigate non-planar modulation doped QWFET on threshold voltage, V_{TH} (V_{DS} = 0.5V).

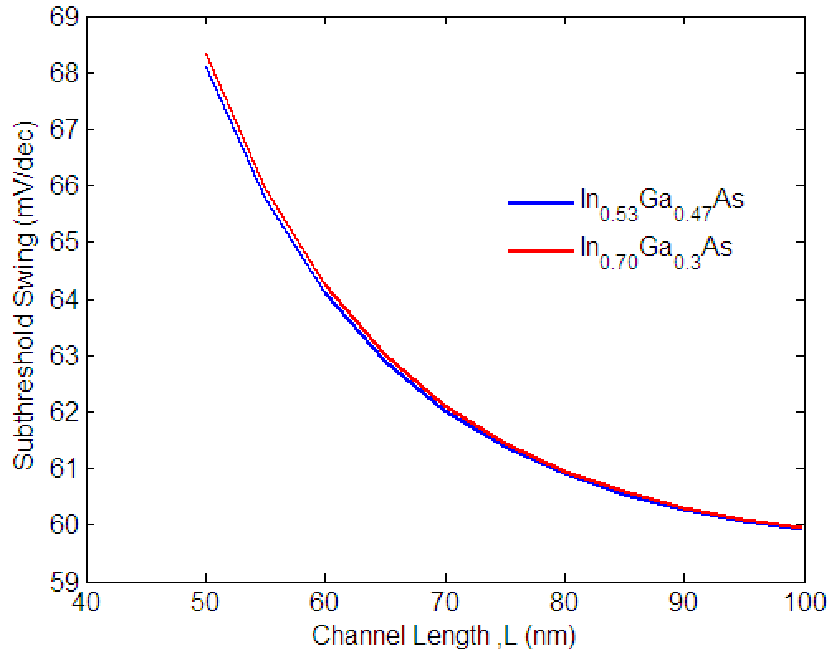


Figure 5.19: Effect of change in indium content in the channel of trigate non-planar modulation doped QWFET on subthreshold swing, SS ($V_{DS} = 0.5$V).

5.5 Effect of Donor Layer Parameters

The effects of donor layer thickness on the subthreshold characteristics of the non-planar trigate QWFET structures are observed for multiple doping concentrations.

Figure 5.20 shows that the threshold voltage decreases with the increase in donor layer thickness, since a thicker donor layer can supply more conduction electrons to the channel at a certain gate voltage. Higher doping concentrations also results in smaller values of threshold voltage, since the availability of electrons in the channel is directly dependent of the availability of donors in the InAlAs barrier layer.

Figure 5.21 shows that the subthreshold swing increases with donor layer thickness, although the effects are negligible. Moreover, the doping concentration has no effect on the subthreshold swing value, since the doping concentration does not affect the change of minimum potential in effective conduction path with respect to the change of gate voltage. The thicker donor layer increases the distance between the top gate and the

channel, resulting in poorer top gate control. However, the subthreshold swing in trigate QWFET is immune to the changes in donor layer thickness because the thicker donor layer only reduces the control of the top gate over the channel carriers, whereas the control of the other two gates remains unchanged. Hence the subthreshold leakage is not affected by the poor control of the top gate.

For the sake of comparison, the effect of donor layer thickness is observed on the subthreshold swing for the single-gate QWFET in Figure 5.22. Since there are no other gates to control the source-drain subthreshold leakage in the single-gate structure, the effect of poorer gate control demonstrates itself in drastically increasing subthreshold swing.

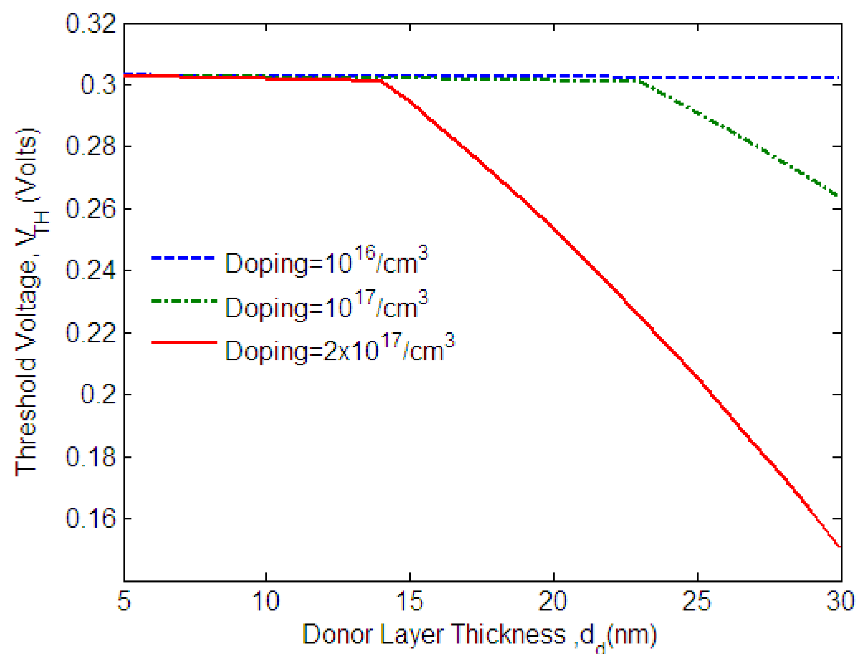


Figure 5.20: Variation of threshold voltage, V_{TH} with donor layer thickness, d_d trigate non-planar modulation doped QWFET ($V_{DS} = 0.5$V).

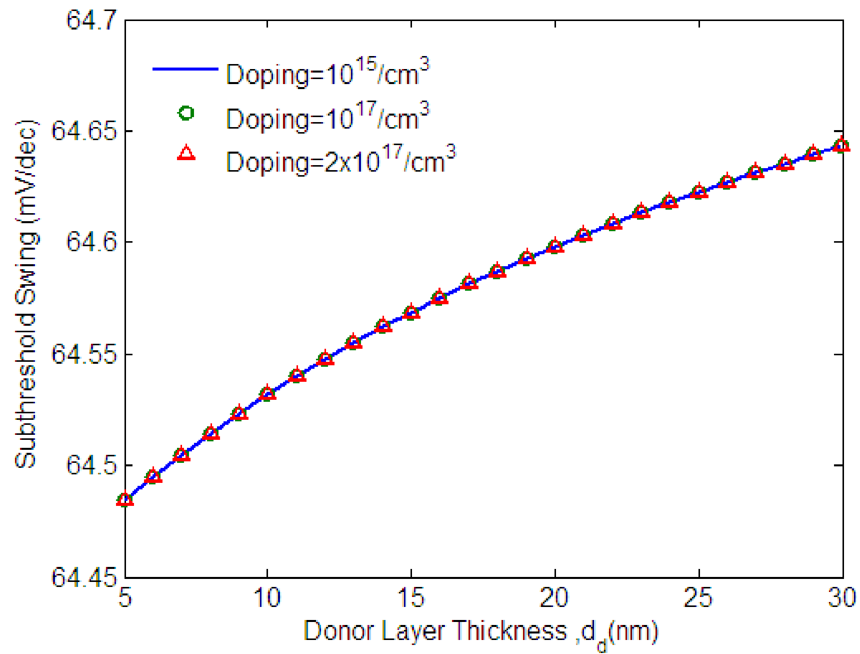


Figure 5.21: Variation of subthreshold swing, *SS* with donor layer thickness, d_d trigate non-planar modulation doped QWFET (V_{DS} = 0.5V).

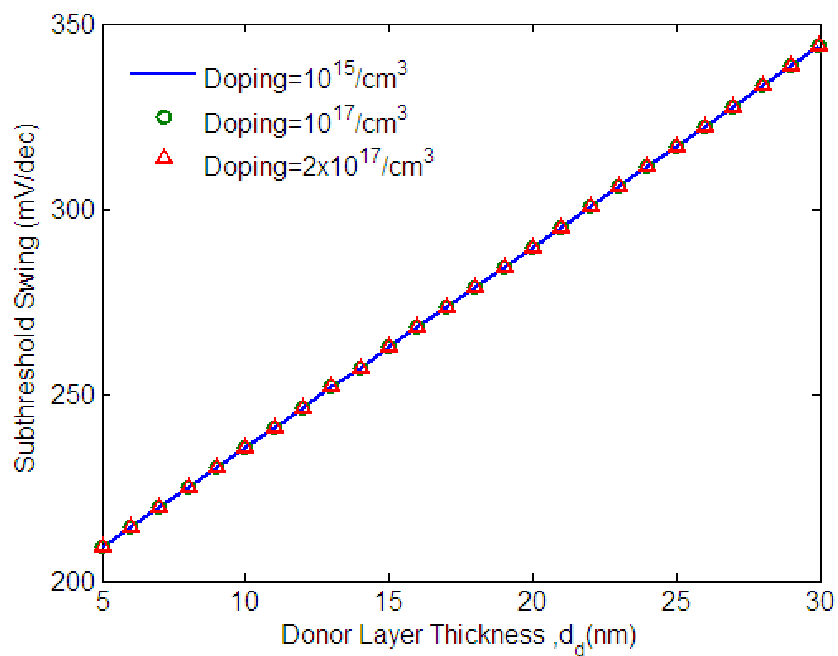


Figure 5.22: Variation of subthreshold swing, *SS* with donor layer thickness, d_d single-gate planar modulation doped QWFET (V_{DS} = 0.5V).

5.6 Modulation-Doped QWFET and Undoped QWFET

The threshold and subthreshold characteristics of doped QWFET and undoped QWFET is compared in this section. Figure 5.23 shows that the modulation doped QWFET has lower threshold voltage compared to an undoped device. Since there is no donor layer in the undoped device to supply electrons to the channel, higher gate voltage is required to draw out electrons from the n^{++} InGaAs cap at the source, which results in a higher threshold voltage value.

As seen in the previous section, the donor layer has little effect on the subthreshold swing of the trigate QWFET devices due to its superior gate control. So removing the donor layer of the trigate QWFET does not significantly improve the subthreshold swing. Figure 5.24 shows that the subthreshold swing of modulation-doped device is slightly larger than that of an undoped device. However, this effect can only be observed for short channel devices. For longer channel lengths the difference between the subthreshold swing of the doped and undoped devices starts to diminish.

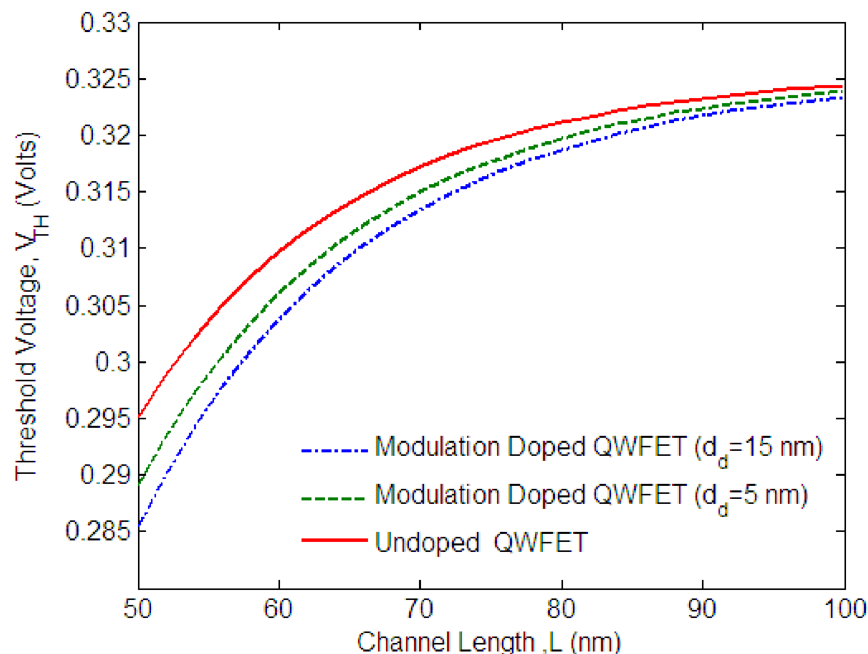


Figure 5.23: Threshold voltage, V_{TH} vs. channel length, L for non-planar modulation doped QWFET and undoped QWFET.

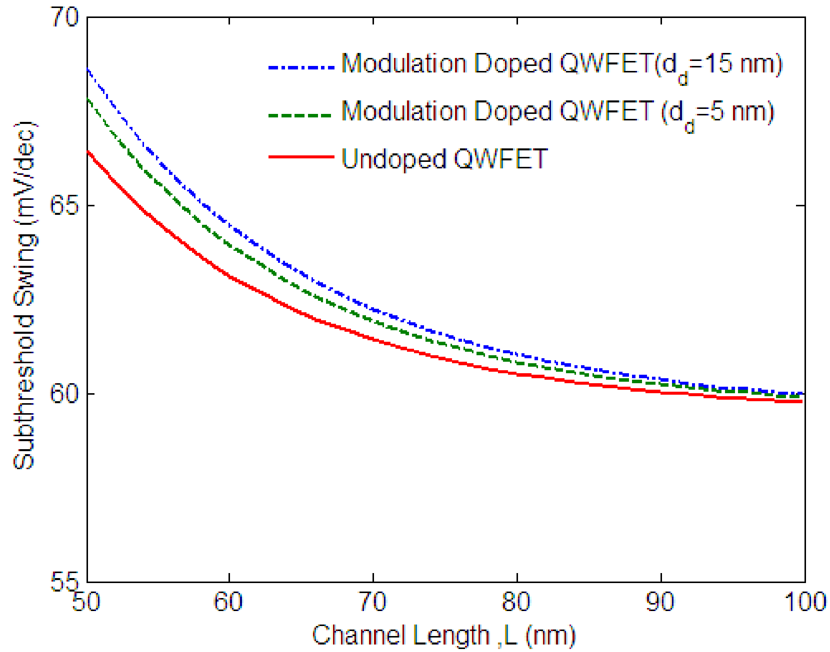


Figure 5.24: Subthreshold swing, *SS* vs. channel length, *L* for non-planar modulation doped QWFET and undoped QWFET.

5.7 Conclusion

Effect of different device parameters on the threshold and subthreshold characteristics of single-gate, double-gate and trigate QWFET structures are shown in this chapter. The results obtained from the analytical model are compared with results from ATLAS simulations, and they are found to be in good agreement. A comparative analysis of the performances of single-gate, double-gate and trigate structures is made in terms of subthreshold characteristics.

CHAPTER 6
CONCLUSION

6.1 Summary

The work presented in this thesis concentrates on analytic modeling of threshold and sub-threshold characteristic of QWFETs. The analysis is done for both planar and non-planar structures of QWFET. For the planar configuration, two dimensional Poisson's equation is analytically solved to formulate the potential distribution. The planar variety includes both single-gate and double gate QWFETs. On the other hand, the solution to three-dimensional Poisson's equation is obtained for modeling of the non-planar configuration, i.e. the trigate QWFET. A threshold voltage and subthreshold swing model is proposed using the channel potential distribution obtained from the mathematical model. The obtained results from the analytic model are compared with simulation results. The results are found to be in good agreement with each other, thus verifying the proposed model.

The analytical model is used to observe the effect of device dimensions on device characteristics. Short channel effects on device performance are highlighted, hence the non-planar structure is found to perform better compared to the planar structures. The short channel non-planar structure is also less sensitive to drain induced barrier lowering than its planar counterparts. For low drain voltages, the short channel trigate QWFET provides subthreshold swing very close to the 60mv/Dec limit. However, the discrepancies between the analytical model and the numerical results are amplified as the channel length approaches the value of the channel thickness. This is a direct consequence of ignoring the charge variation due to the channel length dimension while solving the 3D Poisson's equation. Two types of planar structures are considered in this analysis i.e. single-gate and double-gate QWFETs. Between these two structures, the double-gate provides better performance at short channel lengths and higher drain voltages.

The effects of scaling the lateral dimensions of the channel are also observed for different configurations of QWFET devices. When the channel thickness is scaled in the planar structure, the device provides stronger enhancement mode operation, i.e. the threshold voltage is found to increase. In the non-planar device, scaling the fin height and width has a similar effect. Scaling of lateral dimension is found to improve the subthreshold swing in all three types of structures, although the trigate structure is found to perform yield the lowest value of swing. In the trigate structure the subthreshold swing value approaches 60mV/Dec limit for ultra-scaled device dimensions even for small length of channels, while the planar structures produce higher value of SS for similar cases. The accuracy of the proposed model deteriorates when the lateral dimensions are scaled, since all the quantum mechanical (QM) effects could not be included while solving the 3D Poisson's equation.

The effects of scaling the dimension and changing the doping concentration of the donor layer were also observed for the trigate device. The threshold voltage increase when the donor layer is thinner or donor concentration decreases, since the amount of conduction electron provided by the donor layer decreases in these cases. These properties can be used to adjust the threshold voltage in QWFET structures. On the other hand, the subthreshold swing increases for thicker donor layer, although the doping concentration has no discernible effect on the subthreshold swing.

6.2 Scope for Future Work

In this work, the threshold and subthreshold characteristics are derived from the Poisson's equation including the semi-classical mobile charge terms. The accuracy of the proposed model can be increased for short channel and small lateral dimensions by including the quantum mechanical (QM) effects. The QM effects can be included by adding a correction term with the threshold voltage that can provide sufficient accuracy for small dimensions.

Moreover, a similar analysis can be applied to the gate-all-around and pi-gate structure to derive the subthreshold characteristics.

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