DESIGN AND ANALYSIS OF INTEGRATED ANTENNA ON Si FOR ON-CHIP WIRELESS INTERCONNECT

A Dissertation submitted to the
Department of Electrical and Electronic Engineering
of
Bangladesh University of Engineering and Technology

in partial fulfillment of the Requirement
for the Degree of

MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

By

NASRIN SULTANA
STUDENT ID-040406219P

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
2006

The thesis titled "**Design and Analysis of Integrated Antenna on Si for On-chip Wireless Interconnect**" submitted by Nasrin Sultana, Roll No.: 040406219P, Session: April 2004 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on 17.10.2006

BOARD OF EXAMINERS

1.1 _____ **Chairman**

Dr. A.B.M. Harun Ur-Rashid (Supervisor)
Professor
Department of Electrical and Electronic Engineering
BUET, Dhaka-1000, Bangladesh.

2.1 _____ **Member**

Dr. Satya Prasad Majumder (Ex-officio)
Professor and Head
Department of Electrical and Electronic Engineering
BUET, Dhaka-1000, Bangladesh.

3.1 _____ **Member**

Dr. Pran Kanai Saha
Professor
Department of Electrical and Electronic Engineering
BUET, Dhaka-1000, Bangladesh.

4.1 _____ **Member**

Dr. Jiban Podder (External)
Professor
Department of Physics
BUET, Dhaka-1000, Bangladesh.

DECLARATION

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

Signature of the student

Nasrin Sultana

(Nasrin Sultana)

DEDICATION

To my parents.

CONTENTS

CHAPTER 4 RESULTS AND DISCUSSIONS.....42

LIST OF FIGURES

ACKNOWLEDGEMENT

At first, all thanks goes to almighty Allah to make me capable both physically and mentally to finish my thesis work.

I would like to express my sincere gratitude and heartiest respect to my supervisor, Dr. A. B. M. Harun Ur-Rashid. He supported me all through my work and tried to make me self motivated. I have been strongly impressed by his passion to academic professionalism and integrity, and those virtues will be one of important goal I hope to pursue in my career. Also I really appreciate his dedication to my research to the end of my study, not withstanding his tight schedule.

I am thankful to Dr. Rezwan Khan, Professor and Vice-chancellor, United International University and former Professor of dept. of EEE, BUET for his time, kind attention, fruitful discussion and collaborations. The interaction with him was one of the most valuable experiences of my life.

I would like to express my deepest gratitude to my parents for their unconditional love and devoted support. Their endless encouragement is unforgettable.

ABSTRACT

Dipole antenna is commonly used for Wireless Interconnect on chip. In this thesis, the characteristics of Integrated Dipole Antenna in Si substrate have been investigated by simulation and this simulation has been explained by theoretical derivation. The effect of upper metal layer above the antenna in a multilayer metal process has been simulated using ANSOFT HFSS and explained analytically for the first time in this work. It has been seen that the second metal layer effects significantly on the Forward Transmission Co- efficient— presence of the upper metal layer reduces the gain of the antenna structure. Also, the effect of changing resistivity of the Si substrate, i.e., the transmitting medium and effect of changing the inter antenna distance on the forward transmission Co-efficient has been simulated and explained by theoretical analysis. The comparison between the simulated data and analytical values shows good agreement in each case. At last, Monopole Antenna has been introduced to improve the performance of the antenna in case of the presence of upper metal layer. Monopole antenna preserves the gain of the antenna both in presence of upper metal layer and also without this layer. The analytical explanation of this observation has also been provided here. Monopole antenna with vertical excitation has been proved itself as more efficient than dipole antenna in multilayer metal processes. But the recent works has proposed to use dipole antenna for on-chip wireless interconnect.

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND:

The electronics industry has achieved a phenomenal growth over the last 50 years, mainly due to the invention of Integrated Circuit (IC) in early 1960. Improvement in the processing technique in subsequent years has resulted in a steady increasing chip area and a progressively reducing feature size. This has allowed a complexity increase of approximately one hundred every ten years [1]. Technically speaking, the history of Very Large Scale Integration (VLSI) is a history of miniaturization. This miniaturization is backed by the scaling theory, which states that a MOSFET operates at higher speed without any degradation of reliability when the device size is scaled by a factor of k and at the same time, the operating voltage is scaled by a factor of k. The circuit cost per function is also decreased by miniaturization. Thus, the cost-performance is rapidly improved as devices are scaled down. That is why miniaturization has been pursued so persistently for the last thirty years and will continue to be pursued in the future. Recently, however, undesirable side effects of scaling have become noticeable. These unwanted effects have arrived as challenges to the researchers. To enhance the circuit and system performance, recent studies are focusing on and trying to mitigate these problems [2].

1.2 INTERCONNECT PROBLEM:

Despite remarkable experimental results for transistor scaling well below 100nm design rule, there are growing challenges to our ability to effectively stay on the technology roadmap [3]. One such prime challenge is "Interconnect Problem".

In microelectronic circuits, the transistors and other devices are often connected by the metallic interconnects. Formation of digital nanocomputers that promise

dramatically increased computational speed and density requires the successful formation of molecular-scale devices. Even after the challenges of fabricating the molecular devices are successfully overcome, the problem of connecting these devices in a circuit to carry the information from the output of one device to the input of the next device sustains. This problem is usually referred to as the "Interconnect Problem" [4].

The quintessential purpose of an interconnect is to communicate. To give a more complete definition, it is communication between distant points with small latency. Reducing the distributed resistance– capacitance product provides smaller latency for a given interconnect length [5]. However, during the past four decades interconnect scaling has increased the distributed resistance– capacitance product, demanding larger latency for a given interconnect length. In stark contrast, scaling of transistors reduces the power–delay product or switching energy of a binary transition, to reduce simultaneously both average power transfer and delay.

Scaling of transistors reduces their cost, intrinsic switching delay, and energy dissipation per binary transition. Scaling of interconnects serves to reduce cost but increases latency or time delay and energy dissipation relative to that of transistors. These increase result from relatively larger average interconnect lengths and larger die sizes for successive generations. Therefore, interconnects have become the primary limit on both the performance and the energy dissipation of future Ultra Large Scale Integration (ULSI).

1.3 IMPACT OF INTERCONNECT PROBLEM:

According to the simple scaling rule, when the devices and interconnects are scaled down in all three dimensions by a factor of S, the intrinsic gate delay is reduced by a factor of S, the delay of local interconnects (such as connections between adjacent gates) remains the same, but the delay of global interconnects increases by a factor of S^2 [5-9]. As a result, the interconnect delay has become the dominating factor in determining system performance. Interconnect problem is the most prevailing one. In many systems designed today, as much as 50% to 70% of clock cycle is consumed by

interconnect delays. This percentage will continue to rise as the feature size decreases further.

Repeater insertion is generally used to reduce the delay of long global interconnects [10]. The delay can be reduced up to a certain extent by this technique, but the power consumption increases by about 70% due to the inserted buffers, which will be described in more detail below. Another way to decrease the interconnect delay without increasing the power is to use a thicker and wider metal layer. However, with consistent scaling of global interconnect dimensions to meet the increased connectivity demands in a high performance system-on-a-chip (SoC), the interconnect delay per unit length of optimally buffered minimum sized global wires is also increasing with technology scaling [11]. Therefore, global interconnects tend to limit the performance of high-performance SoCs. In order to achieve improvement in performance, designers tend to use wires, which are wider than minimum-sized global interconnects prescribed by the technology. Increasing the width of the interconnect proportionally reduces its resistance per unit length and also increases the line capacitance per unit length. However, for global interconnects in nanometer technologies, where the aspect ratio of wires is approximately 2–2.5, the increase in width results in a reduction in the resistance–capacitance (RC) time constant of the line and therefore improves delay per unit length [12]. However, these "fat" wires take up a lot of routing resources and using fat wires can adversely affect the wireability of the chip, like signal integrity problems such as high crosstalk noise and large delay fluctuation due to capacitive coupling among adjacent lines. The higher speed causes inductance-related issues and electromagnetic interference problems. For further improvement in performance, the spacing of global interconnects can also be increased which, to some extent, offsets the increase in line capacitance due to increasing line width. On the other hand, this increase in spacing will further degrade the wireability of the chip. Therefore, in determining the wire width at the global tier, the number of interconnects per unit chip edge should also be taken into account along with the delay per unit length.

1.4 EVOLUTION OF INTERCONNECT TECHNOLOGIES:

The semiconductor technology is moving quickly towards applications requiring operating frequencies of the order of tens and hundreds of GHz, as have been predicted in fig.1.1. Also, this is fuelling the demand for scaling the VLSI integration down to the deep sub-micron level with an astonishing pace, i.e., toward ULSI. Along with the transistor scaling, wire width and wire spaces have been scaled down together. Metal routing pitches have also been scaled down and the number of metal layers has been increased. This increasing level of integration is the main route to achieve ever-higher computing speed. But, the main concern toward high-speed operation of ULSIs is the interconnect delay due to the parasitic resistance and capacitance [13]. The scaled chip interconnects suffer from increased resistance due to a decrease in conductor cross-sectional area and increased capacitance for reduced spacing and an increase in conductor height. Thus, Interconnect delay exceeds the gate delay at present technology, as shown in fig. 1.2 [14]. Therefore, the parasitic R and C will remain the primary obstacle to increase clock frequency in future ULSI. Therefore, now-a-days, one of the most urgent needs concerns the development of new interconnect technologies for systems on chip.

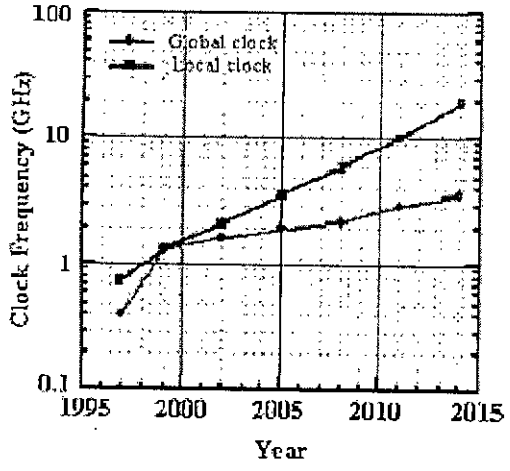

Fig. 1.1: Projected Clock Frequency

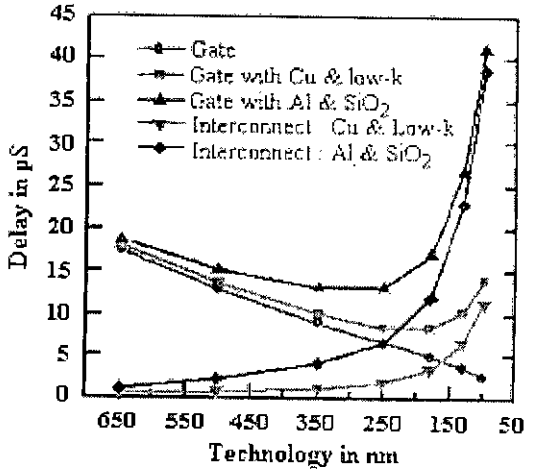

Fig. 1.2: Comparison between Gate delay and Interconnect delay

1.5 DIFFERENT SOLUTIONS OF INTERCONNECTION PROBLEMS— THE WIRING BOTTLENECK:

Due to continually shrinking feature sizes, higher clock frequencies, and the simultaneous growth in complexity, the role of interconnect as a dominant factor in determining circuit performance is growing in importance. For the past few decades, a great deal of work has been focused on improving the conventional interconnect technology. If all these solutions are enlisted chronologically, then we get the following approaches —

1.5.1 Multi layer Interconnects:

In the 80's, advances in VLSI and electronic product performance were driven by silicon technologies. The main driver was transistor scaling which was propelled by advances in lithography and gate dielectrics. Thus, the smaller the feature size is, the faster the transistors become. In the '90s, multilayer interconnection on VLSI became a common technology driven by advances in metallization. An extremely large number of interconnects are needed not just for connecting the devices in a circuit but also for connecting the circuits together. The results show that multilayer interconnects show similar capacitance behavior as do the corresponding single path interconnects. However, the current carrying capability of a multilayer interconnection is expected to be much higher. Therefore it could be beneficial to use multilayer interconnects since more current could be carried by the interconnect in relation to the amount of additional capacitance that the interconnect adds to the circuit [15]. Thus, this advance, in turn, hastened VLSI integration. While this advance is impressive, it is increasingly apparent that such high levels of integration and performance place significant demands on VLSI interconnections. It is evident that VLSI circuit speed is now dominated by the interconnection. In order to mitigate this limitation, modern VLSI interconnection strategies were driven mostly by adding more metal layers. However, due to the increase of interconnect resistance and intra-layer capacitance, multilayer capacitance failed to meet the speed demand of new generation chip.

1.5.2 Cu Interconnect:

The introduction of copper metallization, along with the imminent introduction of low-dielectric-constant insulating materials, indicates an accelerating pace of innovation.

Cu has been seriously evaluated as an interconnection material due to its high electrical conductivity and relatively high melting temperature. Al, on the other hand, had been the interconnection material for about 30 years. The restriction was due to two limiting behaviors of Al.

The first one is related to interconnection failures associated with electromigration [16]. The phenomenon of electromigration occurs when the conductor is subjected to high current density at operating conditions where atomic drifting is severe, leading to mass transports associated with atomic flux divergence. The enhanced and directional mobility of atoms are caused by the direct influence of the electric field on the ionized atoms and the collision of electrons with atoms, leading to momentum transfers and atomic movements. Table 1.1 compares the electromigration parameters of Al and Cu as calculated for the bulk large-grained metals, where Z* is effective valence, ρ is the electrical resistivity, Q is the activation energy of diffusivity, and Do is the pre-exponential constant. Cu is the more resistant against electromigration.

Metal	$-Z^*$	ρ(μΩ-cm)	Diffusion parameters		$Z^*\rho D$ at 100°C
			Q(eV)	D_0 (cm^2/s)	
Al	6.5-16.4	2.65	1.71	2.1×10^{-20}	$3.62\text{-}9.12\times10^{-19}$
Cu	3.7-4.3	1.67	0.78	2.1×10^{-30}	$1.3\text{-}1.5\times10^{-29}$

Table 1.1: Comparison of electromigration parameters for bulk materials.

The second limiting property of Al is its resistivity. For pure Al, the resistivity is 2.7 μΩ-cm, which is considerably higher than that of pure Cu (1.7 μΩ-cm). Making the situation worse, pure Al is not used as the interconnection metal. To bolster its electromigration resistance and minimize its reactivity with silicon substrate, actual Al

interconnections are alloys containing Cu and Si, which increase the resistivity to 3 to 3.5 mW-cm or higher.

As the channel length of a MOS transistor decreases, the carrier transit time across the length of the channel also decreases, making the transistor a faster device. However, the signal propagation in between the devices must occur through interconnections. The interconnection is surrounded by insulating dielectrics. One can approximate the RC delay by multiplying R with a simple plate capacitance C, leading to an expression—

$$RC = \frac{\rho}{t_M} \frac{L^2 \varepsilon_{ILD}}{t_{ILD}} \tag{1.1}$$

where ρ, t_M and L are the resistivity, thickness, and length of the interconnection respectively. ε_{ILD} and t_{ILD} are interlayer dielectric (ILD) permittivity and thickness of the dielectric respectively. One can substitute ρ/t_M with the sheet resistance R_s given in units of ohms per square. A reduction in t_M or t_{ILD} will increase the RC. For a given t_M and t_{ILD}, however, RC delay depends only on R_s, L, and ε_{ILD} and is independent of the width of the interconnection. This dependency implies that, to the first order, reducing the line width does not affect the RC. Indirectly, this is a disadvantage because the RC time constant can offset the speed advantage of device miniaturization.

More rigorous calculations of the RC time constant that includes the effect of fringing capacitances will show that at smaller dimensions, the total circuit delay is a composite of the intrinsic device delay associated with the transistor and the interconnection delay [17]. Therefore, by changing the interconnection material from Al to Cu, number of metal layer, power consumption, and RC delay can be significantly improved as shown in Fig. 1.3.

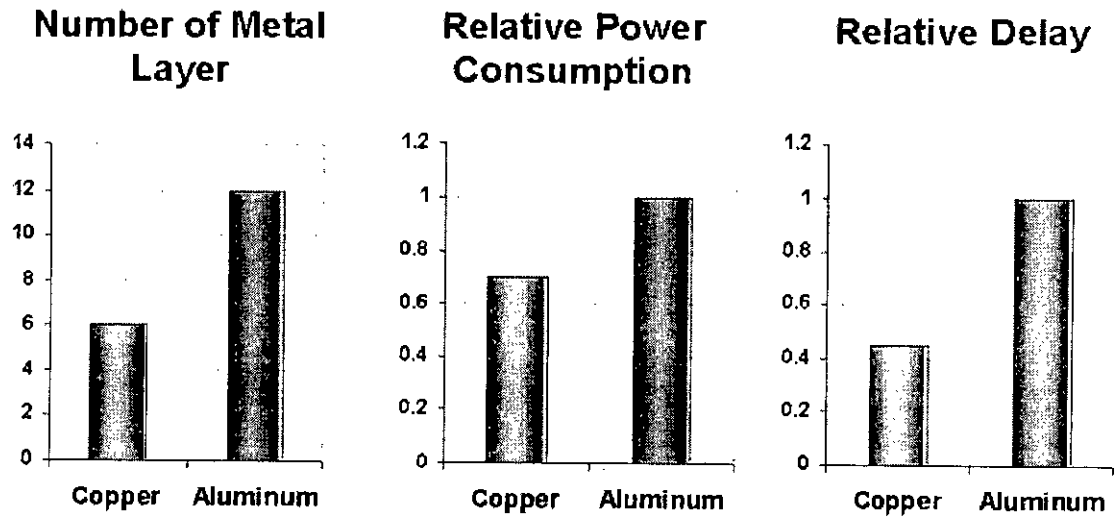

Fig. 1.3: Superiority of Cu/low-k interconnection over Al/ SiO_2 interconnection.

1.6 REVOLUTIONARY TECHNIQUES-PREDICTED "END OF THE ROAD" FOR METALLIC INTERCONNECT:

At 250-nm technology node, copper (Cu) with low- dielectric was introduced to alleviate the adverse effect of increasing interconnect delay [18]. However, as shown in Fig. 1.4, below 130-nm technology node, substantial interconnect delays will result in spite of introducing these new materials, which in turn will severely limit the chip performance. Further reduction in interconnect delay cannot be achieved by introducing any new materials.

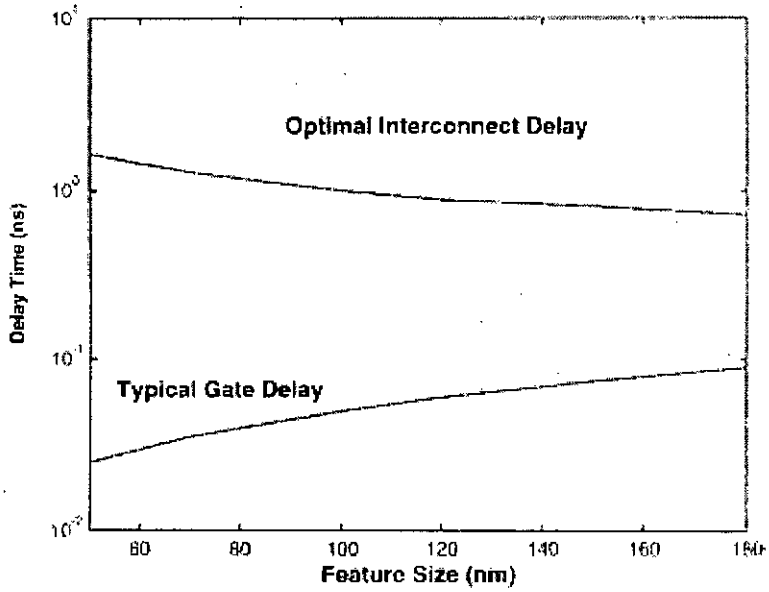

Fig. 1.4: Typical gate and interconnect delays as a function of feature sizes. The interconnect delay assumes an optimally repeated line and includes the delay due to the repeaters.

Again, the global clock skew can limit the high-speed operation of microprocessors, even when using the state-of-the-art copper and low-κ interconnect technology [19]. Worse than this, typical systemic clock skew solutions involve use of H-tree circuitry, taking up a large area and requiring symmetry [20]. What this means in terms of clock delivery is that as the chip size and clock frequency are increased each passing year, the clock skew becomes harder to equalize across the chip, and the total area used in clock delivery increases. This problem is one of the grand challenges facing the semiconductor industry, which could place serious limitations on the growth of the industry.

The problem facing us then is that evolutionary solutions will not be sufficient to meet the performance roadmap. To tackle the issues developed above, radically different interconnect approaches displaying a highly improved data-rate to power ratio must be developed. At present, the most prominent ideas are

- 3D (non-planar) integration [21],
- Optical interconnects [22] and
- Integrated radio frequency or microwave interconnects [23].

1.6.1 3-D integration:

Three-dimensional integration (schematically illustrated in Fig. 1.5) to create multilayer Si ICs is a concept that can significantly improve deep-submicrometer interconnect performance, increase transistor packing density, and reduce chip area and power dissipation [24]. In the 3-D design architecture, an entire (2-D) chip is divided into a number of blocks, and each block is placed on a separate layer of Si that is stacked on top of each other. Each Si layer in the 3-D structure can have multiple layers of interconnect. These layers are connected together by vertical interlayer interconnects (VILICs) and common global interconnects as shown in Fig. 1.5 [21].

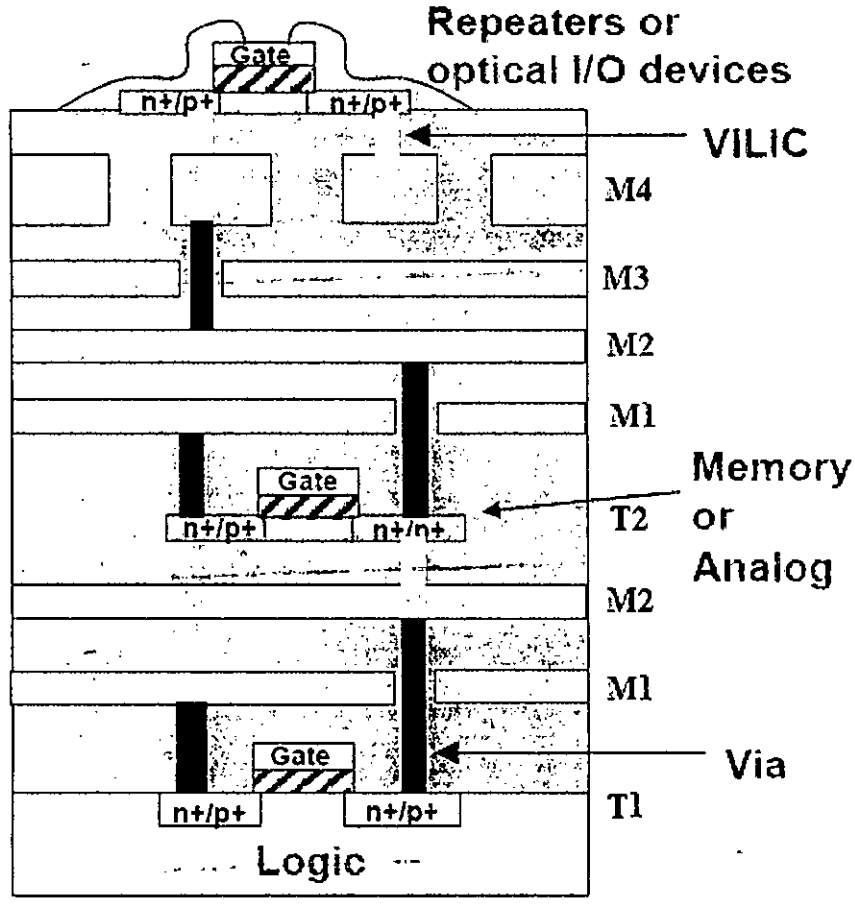

Fig. 1.5: Schematic representation of 3-D integration with multilevel wiring network and VILICs. T1: first active layer device, T2: second active layer device, Optical I/O device: third active layer I/O device. M'1 and M'2 are for T1, M1 and M2 are for T2. M3 and M4 are shared by T1, T2, and the I/O device.

3-D integration offers some attractive **advantages** related to system performance and enabling of new system architectures.

First, the 3-D architecture offers extra flexibility in system design, placement, and routing. For instance, logie gates on a critical path can be placed very close to each other using multiple active layers. This would result in a significant reduction in RC delay and ean greatly enhance the performance of logic circuits.

Second, the negative impact of deep-submicrometer interconnects on VLSI design can be reduced significantly by eliminating the long *global wires* that realize the interblock communications by vertical placement of logie blocks connected by short vertical interlayer interconnects.

Third, the 3-D chip design technology can be exploited to build SoCs by placing circuits with different voltage and performance requirements in different layers.

Fourth, three-dimensional integration can reduce the wiring, thereby reducing the capacitance, power dissipation, and chip area and therefore improve chip performance.

Fifth, the digital and analog components in the mixed-signal systems can be placed on different Si layers thereby achieving better noise performance due to lower electromagnetic interference between such circuit blocks.

However, there are several **critical challenges** on the way to use this technique.

- Difficult technological barriers are opposed to the use of this technique. Heterogeneous integration is still a long way from reaching the status of mature technology.
- It also appears rather clear that physical problems must be solved, such as the evacuation of thermal energy and the necessarily higher reliability of the components, which must survive the longer and more intricate fabrication process.
- Even if these issues are resolved, it is also necessary to question the long-term validity of the approach. Indeed, when communication frequency increases, the communication distance decreases at constant power budget. The surface of each layer must thus decrease, which results in a quadratic increase in the number of layers and in the vertical communication distance.

- Thus it is not obvious that all technological problems will be solved before this technique becomes obsolete compared to bandwidth requirements.

The active interconnect layer is a variant on the general vertical integration technique, specific to the interconnect problem. This solution will not solve the problems inherent to metallic interconnect, but it offsets them for a while. The idea is to graft a layer of active buffers above the last metal layer and use these buffers (which can be arranged in a matrix formation or as a "sea" of buffers) solely as repeaters for long interconnect. This approach frees up active silicon area for computing functions rather than for interconnects. It also reduces congestion by replacing the via stacks (necessary between the last metal layer and the active silicon layer), by single vias going vertically upwards from the last metal layer to the vertically adjacent buffer layer. Power may be marginally reduced (as the via stack contribution to line load is removed). Crosstalk or any disturbance on victim lines should be reduced. As with 3D, doubts can be expressed as to how long this approach could be viable.

1.6.2 Optical interconnects:

Optics is arguably a very interesting and different physical approach to interconnection that can in principle address most, if not all, of the problems encountered in electrical interconnections. [22]. Fig. 1.6 shows a typical view of an optical interconnect system. Proposed optical approaches can be grouped into **guided wave** and **free space** [25], as shown in fig. 1.7. Guided wave optics involves the use of waveguides to contain the optical signals within a board, package, or on a chip. Free-space optics utilizes diffractive optics and conventional lenses or microlens arrays to guide single or multiple parallel optical beams in free space.

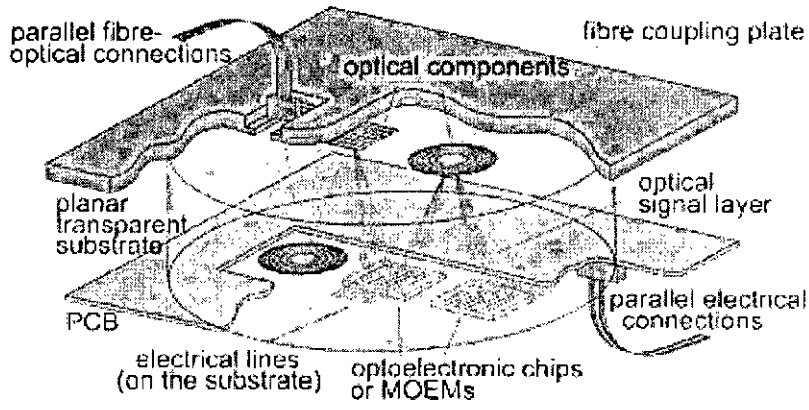

Fig. 1.6: Optical Interconnect Technology on Si

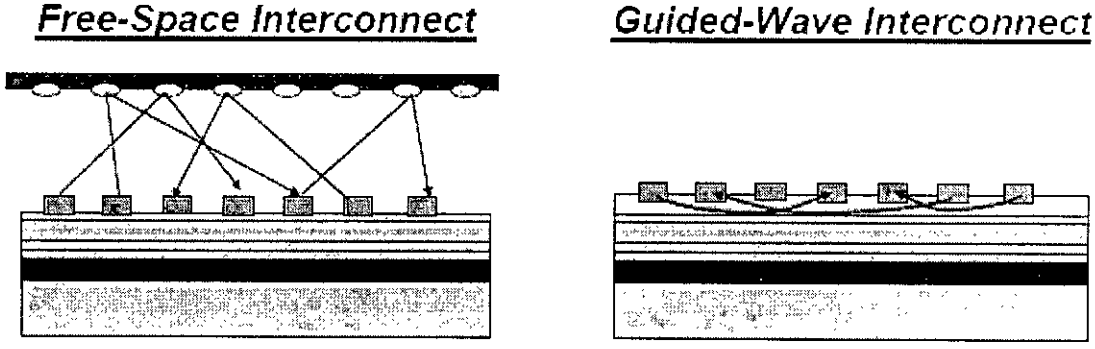

Fig. 1.7: Proposed two groups of Optical Interconnect.

Compared to electrical wires, optical technology offers fundamental advantages to global interconnects, given that the technology can be realized in a simple, cost effective implementation.

- The bandwidth of electrical interconnects is $\sim A/l^2$, where A is the cross section area of the Interconnect and l is the length. Optical interconnects, however, are not bandwidth limited in this way, although they are limited by the propagation delays of optoelectronic components such as transmitters, modulators, and receivers.
- The signal propagation velocity of electrical interconnects tends to be 10%–30% of the speed of light, c, whereas the optical propagation velocity for guided waves tends to be ~ (l/3)c.

- Optical interconnects used for off-chip and on-chip clock and signal distribution have similar bandwidths and latency, and they, therefore, eliminate the hierarchical constraints imposed by off-chip electrical interconnects, i.e., the lower bandwidth and longer delay times. .

Optical interconnects must overcome some rather difficult fundamental and technological challenges before they will find application even in off-chip applications. The technical challenges this interconnect is facing includes

- The decisions on which signals to include in optical communications and which remain in conventional metal dielectric, and the choice of on-chip optical emitters, are significant. In the case of optical interconnects, it is easy to assume that this solution will meet speed requirements because the signal travels at "the speed of light." However, to define the total interconnect system for this approach it is necessary to consider the delays associated with rise and fall times of optical emitters and detectors, the speed of light in the transmitting medium, losses in the optical waveguides (if used), the signal noise due to coupling between waveguides, and a myriad of other details.
- Guided wave optical interconnects may require separate active layers in the vertical dimension with via interconnect to the functional blocks to support the required optoelectronic components.
- An on-chip optical interconnect technology may require either impractical high levels of optical signal power or area intensive error correction circuits. The latter, again, can be achieved perhaps in a separate set of active interconnect layers.
- The additional disadvantages include Power dissipation for receivers, and, to a lesser extent, transmitters can be prohibitively large.
- Other issues with optical interconnects are the technologies for fabricating III–V devices on silicon. Heteroepitaxial growth of III–V vertical-cavity surface-emitting lasers (VCSELs) on silicon CMOS circuits is a very difficult technology limited by reliability concerns.

Much sophisticated optical and optoelectronic technology has been developed for long-distance communications, but the requirements of dense interconnects are substantially different. Low power dissipation, small latency, small physical size, and the

ability to integrate with mainstream silicon electronics in large numbers are all required for dense interconnects at the chip-to-chip or on-chip level. Existing optical telecommunications applications do not require any of these constraints, and the technologies developed do not satisfy them. Additionally, the discrete approaches used for long distances are likely not to be viable for dense interconnects. However, other opportunities in optical and optoelectronic technology have been researched over the last several years that are apparently capable of operating at the densities needed, though the technologies are often quite different from those of long-distance communications and are much less mature.

1.6.3 RF/Wireless Interconnect:

A relatively radical alternative to the usual metal/dielectric interconnects is to use transmission of signals from one part of a chip to another via RF or microwaves. Recently, this technology has been considered as a viable candidate to replace metal/dielectric global wires. In general, RF signals can be transmitted through free space or waveguide mediums. At chip scale, the free space transmission is not possible. On the other hand, guided transmission (by MTL (Microstrip transmission line) or CPW (Coplanar waveguide)) can be carried out with attenuation lower than 2dB/cm up to 200GHz. A wireless LAN type interconnect architecture (Fig. 1.8) can exploit this high bandwidth by associating IP blocks, RF transceivers, capacitive couplers as near-field antennas and MTL/CPW as shared RF communication channel [23].

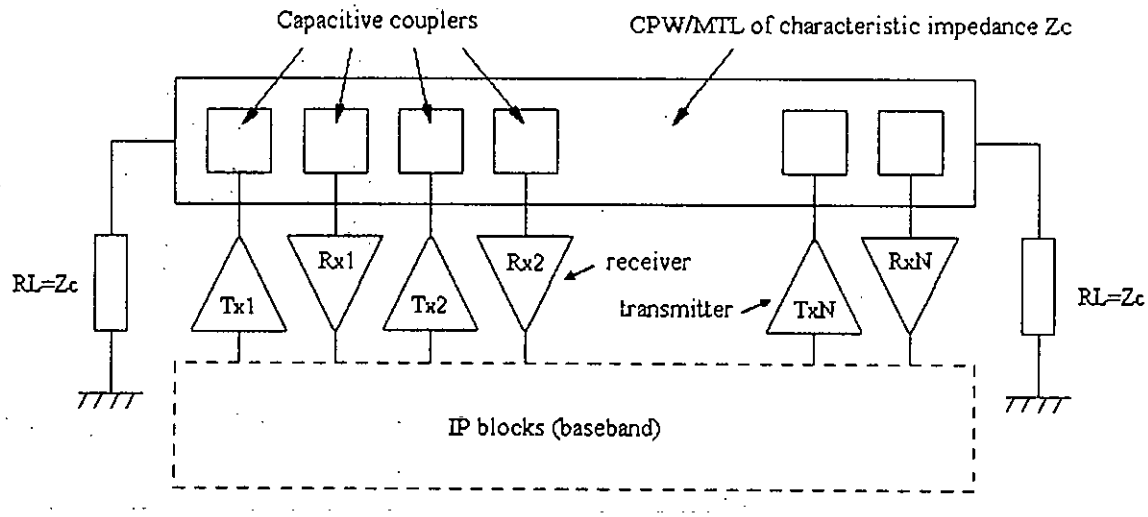

Fig. 1.8 Integrated RF interconnect channel concept

RF interconnects are a very new approach for intrachip and interchip interconnects. This approach has become possible because of the confluence of wireless technologies for communications applications with high-frequency silicon technologies. This approach can be used for both clock and data signals. They have been demonstrated recently for clock distribution at 7.4 GHz and 15 GHz in 0.25-μm and 0.18-μm technologies respectively. They have also received attention for data communication [26].

The use of code division multiple access (CDMA) and frequency division multiple access (FDMA) to obtain up to 100 channels in a 100-GHz carrier connecting multiple transmitting and receiving nodes is the special and novel feature of this wireless approach. Using local area network (LAN) communication techniques applied to microsystems applications, this micro-LAN (M-LAN) approach will provide high-speed, low-loss intrachip clock/signal distribution among multiple block functions on a chip, or, more likely, among multiple chips in a package.

Compared to global electrical wires, RF interconnects potentially offer several advantages.

- Circuits can be synchronized over much larger areas because wireless approach transmit signals three to ten compared to global wires.

- In addition, the bandwidth of the RF approaches is only limited by the bandwidths of the transmitting and receiving components, and not by the transmission medium, as is the case for global wires.
- The crosstalk between channels should be much improved, particularly for the approach using FDMA and CDMA communication techniques.
- The signal multiplexing capability of the M-LAN approach should reduce the actual number of I/O ports going off-chip and the M-LAN communications techniques can provide new flexibility to reconfigure the interconnect system simply by changing the CDMA codes.
- RF interconnects are a very new approach for intrachip and interchip interconnects, although the techniques proposed are well developed for wireless communications applications.

RF interconnect has to overcome some difficult challenges before becoming a viable candidate to replace global wires. First, for package applications, the RF implementation must be cost competitive with conventional interconnect systems. Further, the power dissipated by RF interconnect support circuits must be equal to or less than the power dissipated by the global interconnect wires, and the silicon area consumed by these RF circuits must only be a small fraction of the chip size. Also, the RF power dissipation cannot add a significant amount of heat to an already heavy thermal load. Finally, similar to optical interconnects, RF interconnect systems will likely require adaptation of new system architectures to fully exploit the capabilities of RF interconnects.

1.7 ADVANTAGES OF WIRELESS INTERCONNECT OVER OPTICAL INTERCONNECT:

Though both optical and wireless interconnect schemes are simultaneously evaluated as a new technology solution for the future ULSI, the later shows a number of promising advantages.

- The advantage of RF technique lies primarily in the possibility of offering several IP blocks access to a broadband communication channel through a single physical channel, without major process modifications. Whereas

optical interconnect, traditionally considered as a specialized technique, raises design questions that industrial IC designers are not equipped to answer. Difficulties expected are obtaining a large enough optical-electrical conversion efficiency.

- Optical devices are fabricated using III-V group which are not compatible with existing Si technology and hence costly to implement. On the other hand, wireless interconnects provide completely CMOS compatible architecture.
- The relative size of optical components (particularly waveguides and photo-receiver circuits) compared to chip circuitry is a critical design constraint. That is why, optical interconnects may require separate active layers in the vertical dimension with via interconnect to the functional blocks to support the required optoelectronic components. To the contrary, no special guided wave mechanism is required for on-chip wireless interconnect hence it reduces the electronic overhead on the existing circuit components.
- WDM (Wavelength Division Multiplexing) is the only technique that makes possible to increase the aggregate data rate of the optical link. RF interconnect exploits CDMA (Code Division Multiple access) or FDMA (Frequency Division Multiple access) encoding techniques, managed by the transceivers, which are not only the most common and easy techniques, but also increase data rate and reduce any interchannel interference. CDMA and FDMA are compatible to other communication systems also.

1.8 RESEARCH OUTLINE:

The ultimate goal of this work is to develop an efficient system of On-chip integrated antenna on Si for Wireless Interconnect. A model of on chip integrated antenna on Si substrate will also be developed. The outcomes while delving through the work are asserted below—

- The effect of multi layer interconnect scheme on forward transmission co-efficient of dipole antenna.
- Analytical explanation of the simulation of dipole antenna excited horizontally.
- The effect of Si resistivity on transmission co-efficient of dipole antenna at different frequencies.
- The effect of distance between the antennas on transmission co-efficient of dipole antenna at different frequencies.
- The efficient way of providing excitation to the antenna in integrated circuit fabricated with planar IC technology.
- Analytical explanation of the simulation of antenna excited in vertical direction.

The complete system was simulated in ANSOFT and the calculation was done by MATLAB. Optimistic results from these simulations and theoretical studies took us a way forward to achieve the overall goal of finding the circuit parameters of the transmitting and receiver antenna and also the transmission medium.

1.9 THESIS LAYOUT:

This thesis comprises of seven chapters.

In **chapter 1,** we first highlighted the interconnect problem of today's small scale ICs as a prime challenge to meet the projected overall technology requirements. There are several new techniques to overcome this interconnect problem. Different types of Interconnect schemes have been delineated in details starting with the definition of interconnect. The problem of using metallic interconnect irrespective of the material has been also depicted in this chapter. Consequently, the importance of revolutionary interconnect schemes has aroused and all this new techniques has been sketched. It has been shown that the wireless interconnect scheme using Si integrated antenna has some superfluous advantages above the others. At last, a detailed outline of the research has been sketched.

In **chapter 2**, the definitions and theories that have been used in this work has been described elaborately. At first the characteristics of dipole and monopole antennas has been recited with the help of electromagnetic theory. Then the definition of scattering matrix of a microwave network has been depicted and at last the Friis transmission formula, which is the backbone of the work, has been derived.

In **chapter 3,** the detail of the analytical part of the research has been enumerated. At first an analytical model of dipole antenna under study has been formed on the basis of Friis transmission formula. The Forward transmission Co-efficient (S_{21}) of a dipole has been developed from this Formula. Then equation of S_{21} at different conditions, like without any metal layer on the top of the dipole antenna, with metal layer on the top has been derived and the explanation is given for the first time in this work. The effect of change in resistivity of Si substrate and variation in distance between the transmitting and receiving antenna on S_{21} has been also incorporated in case of dipole antenna without any metal layer. Dipole antenna without any metal layer on the top has been analyzed as it is the most conventional and efficient way of using integrated antenna in VLSI. In this same chapter, the same antenna structure has been modeled as a two port microwave T network. The circuit parameters of each of the T model element have been further derived. Then the problem in using the dipole antenna in presence of upper metal layer has been described and a novel approach of applying vertical excitation to the antenna has been proposed here.

In **chapter 4,** the simulation procedure has been described and comparison between the theoretical data and simulation results has been also shown. The simulation result has been extracted in the form of Forward Transmission Co-efficient (S_{21}) and Z-matrix of the antennas. All the theoretical data that have been acquired from the theory described in chapter3, has been juxtaposed with the simulated one at different situations and cases. The comparison showed good agreement between the simulated and modeled data.

In **chapter 5,** the thesis has come to its end with the summary of the research and with some suggestions to move toward the future of this work.

CHAPTER 2

GENERAL THEORY OF DIPOLE ANTENNA

In our thesis, we propose an efficient design of Integrated Dipole antennas on Si for on-chip wireless interconnects in Multi layer metal process. Therefore, we need to define some of the terms of our work. The definitions are described below—

2.1 BASIC ANTENNA THEORY:

Every structure carrying RF current generates an electromagnetic field and can radiate RF power to some extent and likewise an external RF field can introduce currents in the structure. This means that theoretically any metallic structure can be used as an antenna. However, some structures are more efficient in radiating and receiving RF power than others. The following set of examples explains this concept.

Transmission lines (striplines, coaxial lines etc.) are designed to transport RF power with as little radiation loss as possible because these structures are designed to contain the electromagnetic fields. To obtain any appreciable radiation from such a structure, requires excessively high RF currents which causes low efficiency due to high losses. Likewise, the ability to introduce RF currents into the structure is of importance, described by the feed point impedance. If the feed point impedance is very high, low, and/or highly complex, it is difficult to introduce RF current with good efficiency.

The antenna structure should be of reasonable size compared to the wavelength of the RF field. A natural size is half a wavelength, which corresponds to approximately 6 cm at the 2.4 GHz band. This size is effective because when fed with RF power at the center point, the structure is resonant at the half wave frequency. Reducing the size below 6cm tends to make the antenna less visible to the RF field and not resonant that causes low efficiency. Not all structures make an efficient antenna.

Numerous structures have been devised that provide good efficiency and impedance match, but most of these are derived from a few basic structures. Of the variations that exist, the following sections highlight the most common.

2.1.1 Dipole Antenna:

The dipole is one of the most basic antennas. The dipole is a straight piece of wire cut in the center and fed with a balanced generator or transmission line. As previously stated, this structure is resonant, or non-reactive, at the frequency where the conductor length is 1/2 wavelength. For the ISM band, this length is approximately 6 cm or about 2 ½ inches. At this length, the dipole shows resonance, the feed impedance is resistive, and is close to 73 Ohms. This also holds true for a very thin wire in free space.

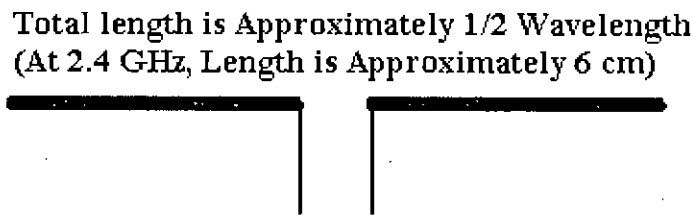

Fig 2.1: Basic Dipole

A practical dipole of some thickness, loaded with different dielectric materials (PCB etc.), and perhaps relatively close to ground, shows resonance at a slightly shorter length than calculated, and the radiation resistance drops somewhat. For dipoles not too close to ground, the shorting factor is typically in the range of 5-20%, the shorter being more heavily dielectric loaded, and radiation resistance is in the range of 35-65 Ohms. This dipole setup exhibits a relatively good match to a 50 Ohm generator, but the feed is differential.

2.1.2 Monopole Antenna:

If one part of a dipole antenna is removed and replaced by an infinite ground plane, the remaining half of the dipole "mirrors" itself in the ground plane, much in the same way that one sees their own reflection in water.

For all practical purposes, the monopole behaves as a "half" dipole. That is, it has the same doughnut shaped radiation pattern; the radiation resistance is half that of the

dipole (37 Ohm), and the same loading and feeding techniques can be applied. However, one very important difference remains in that the antenna feed point is not balanced, but single ended. Because of this and because most RF circuits are of the unbalanced type, this antenna type has been immensely popular and a lot of variations of the monopole theme exist, most designed to match 50 Ohms.

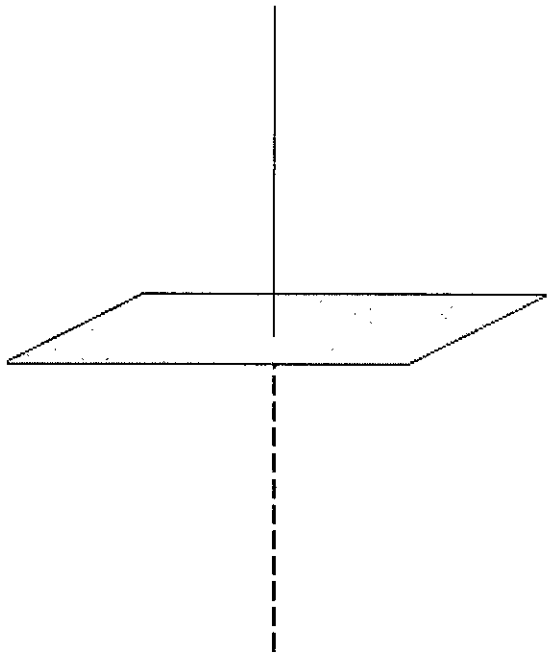

Fig. 2.2: Monopole above a ground plane, showing the "Mirror" Antenna

In a practical application, the ground plane of monopole antenna is often made up of the remainder of the PCB (ground and supply planes, traces, and components). The ground plane should be a reasonably sized area compared to the antenna, and should be reasonably continuous. If a monopole is used on a very small PCB, perhaps even with only a small area of copper, efficiency suffers, and the antenna is difficult to tune. Components and tracks introduce additional losses and affect the feed point impedance.

As for the dipole, resonance is obtained at a length slightly shorter than one quarter wavelength, typically 5-15% shorter. Typical lengths are slightly more than an inch or two or 3 to 5 cm.

2.1.3 Radiation Patterns:

The radiation or antenna pattern describes the relative strength of the radiated field in various directions from the antenna, at a fixed or constant distance. The radiation pattern is a "reception pattern" as well, since it also describes the receiving properties of the antenna. The radiation pattern is three-dimensional, but as shown in the fig. 2.3 it is difficult to display the three-dimensional radiation pattern in a meaningful manner, it is also time consuming to measure a three-dimensional radiation pattern.

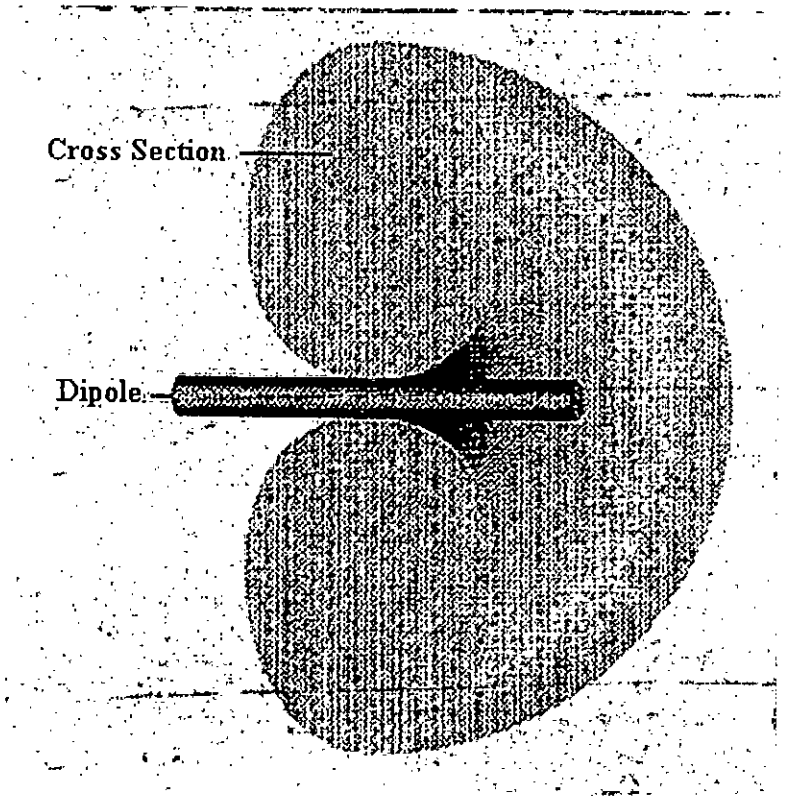

Fig. 2.3: Radiation Pattern of Horizontal Half-Wave Dipole (3 dimensional sketch).

Often radiation patterns are measured that are a slice of the three-dimensional pattern, which is of course a two-dimensional radiation pattern that can be displayed easily on a screen or piece of paper. These pattern measurements are presented in either a rectangular or a polar format (The co-ordinate system is shown in figure 2.4). Two-

dimensional radiation patterns of Dipole and Monopole antenna are shown in fig 2.5, 2.6 and 2.7.

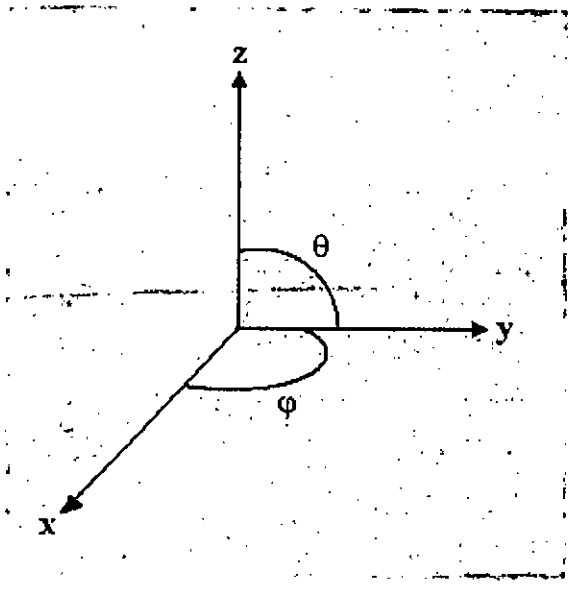

Fig. 2.4: Three dimensional Co-ordinate System

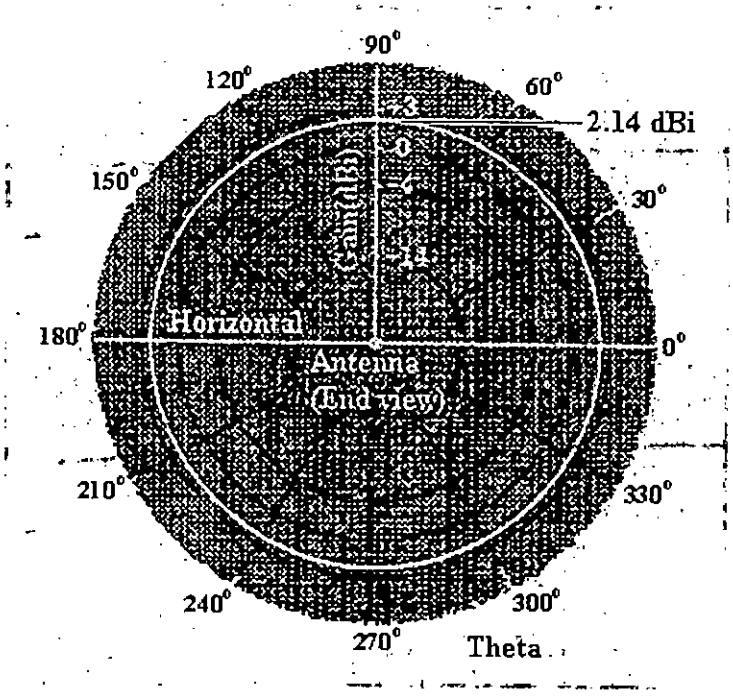

Fig. 2.5: Radiation Pattern of Horizontal Half-Wave Dipole (Vertical Plane).

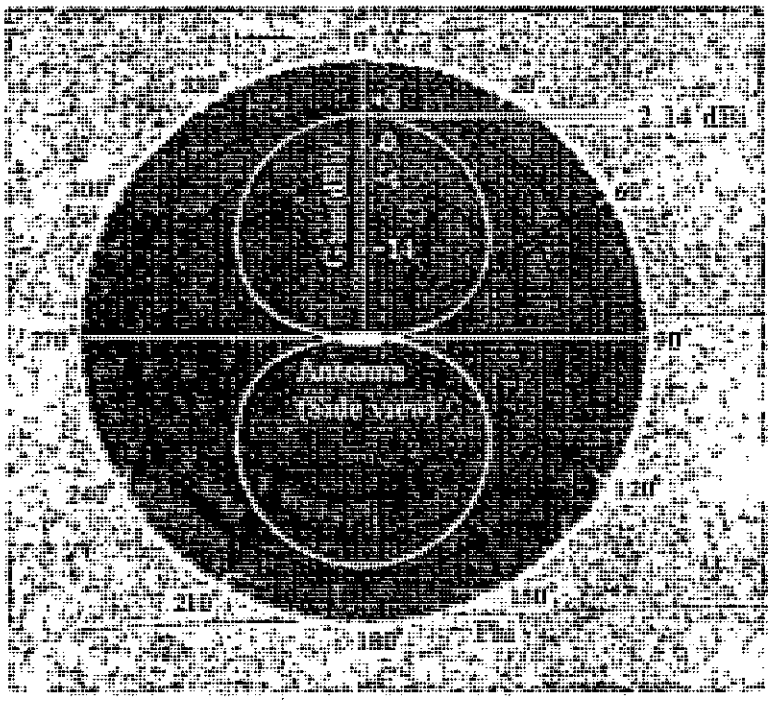

Fig. 2.6: Radiation Pattern of Horizontal Half-Wave Dipole (Horizontal Plane).

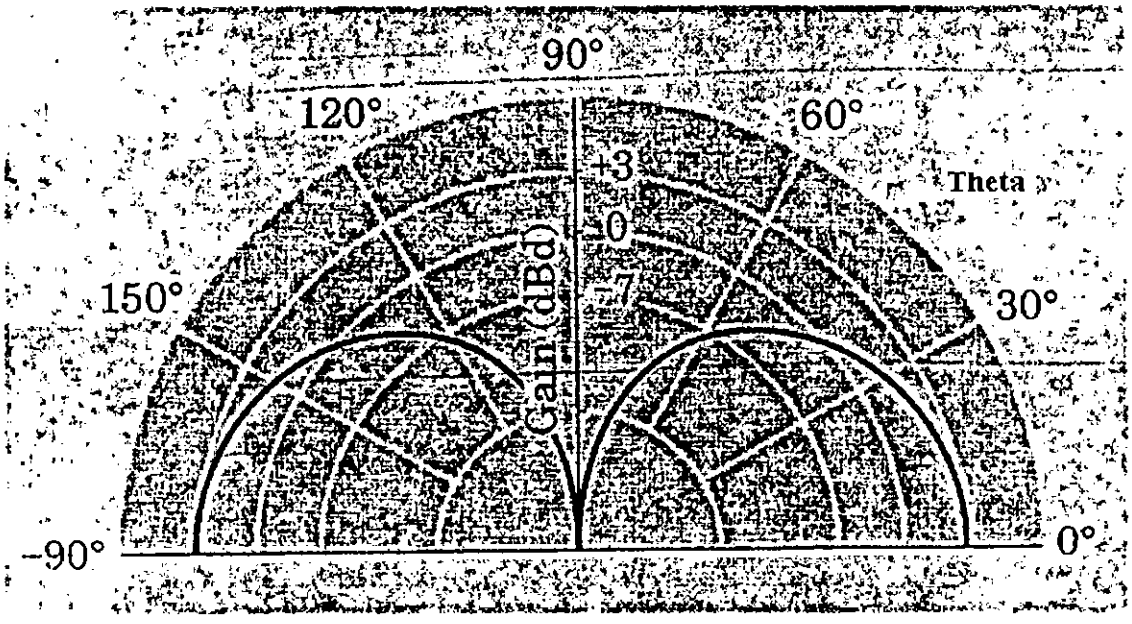

Fig. 2.7: Radiation Pattern of Vertical Monopole Antenna.

2.2 THE SCATTERING MATRIX:

In microwave networks, a practical problem exists when trying to measure voltages and currents because direct measurements usually involve the magnitude (inferred from power) and phase of a wave traveling in a given direction or, of a standing wave. Thus, equivalent voltages and currents, and the related impedance and admittance matrices, become somewhat of an abstraction when dealing with high-frequency networks. A representation more in accord with direct measurements, and with the ideas of incident, reflected, and transmitted waves, is given by the scattering matrix.

The scattering matrix provides complete description of an N-port network as seen at its N ports. This matrix relates the voltage waves incident on the ports to those reflected from the ports. For some components and circuits, the scattering parameters can be calculated using network analysis techniques. Otherwise, the scattering parameters can be measured directly with a vector network analyzer. Once the scattering parameters of the network are known, conversion to other matrix parameters can be performed, if needed.

Consider the N-port network shown in Figure 2.8, where V_n^+ is the amplitude of the voltage wave incident on port n, and V_n^- is the amplitude of the voltage wave reflected from port n. The scattering matrix, or [S] matrix, is defined in relation to these incident and reflected voltage waves as

$$\begin{bmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_N^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdots & S_{1N} \\ S_{21} & S_{22} & \cdots & \vdots \\ \vdots & & & \vdots \\ S_{N1} & \cdots & \cdots & S_{NN} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_N^+ \end{bmatrix}$$

$$or \qquad [V^-] = [S][V^+]$$

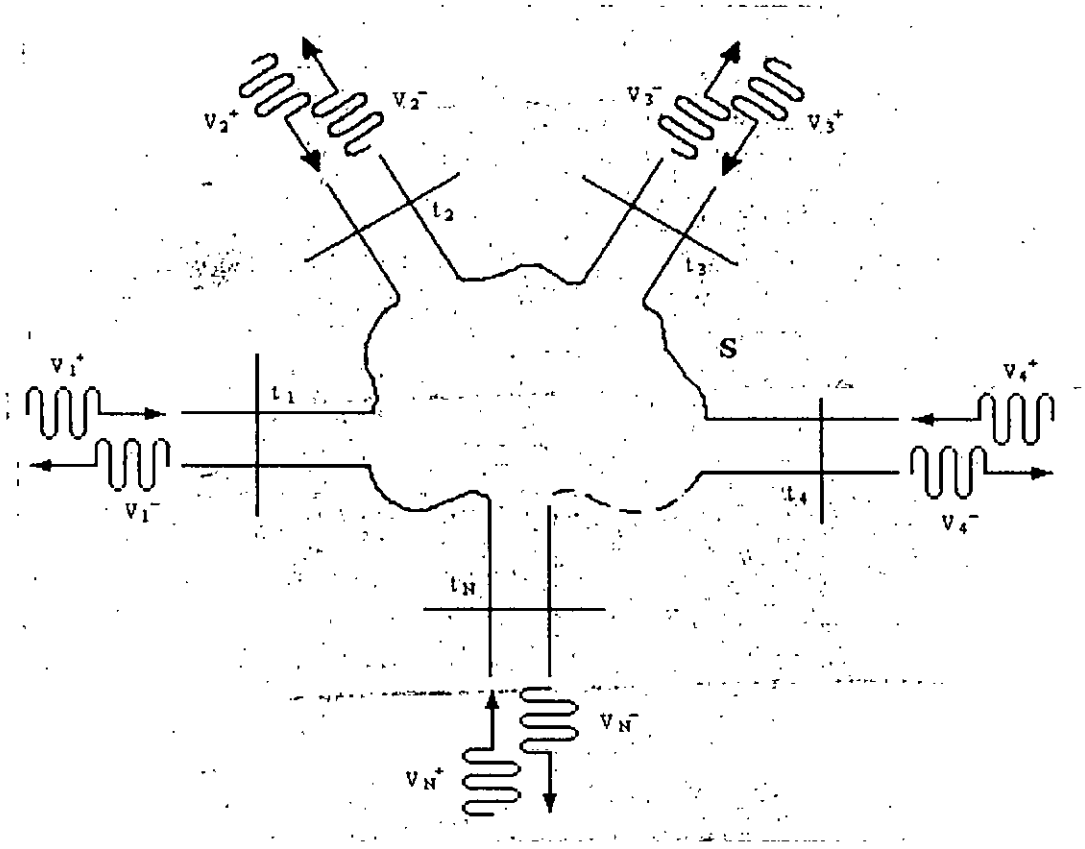

Fig 2.8: An arbitrary N-port microwave network

A specific element of the [S] matrix can be determined as

$$S_{ij} = \left.\frac{V_i^-}{V_j^+}\right|_{V_k^+=0 \text{ for } k\neq j}$$

In words, the above equation says that S_{ij} is found by driving port j with an incident wave or voltage V_j^+ and measuring the reflected wave amplitude, V_i^- coming out of port i. The incident waves on all ports except the jth port are set to zero, which means that all ports should be terminated in matched loads to avoid reflections. Thus, S_{ij} is the reflection coefficient seen looking into port i when all other ports are terminated in matched loads, and S_{ij} the transmission coefficient from port j to port i when all other ports are terminated in matched loads.

2.3 FRIIS TRANSMISSION FORMULA:

Friss Transmission formula is derived by Harad T. Friis in 1946. This formula gives the power received over a radio communication link.

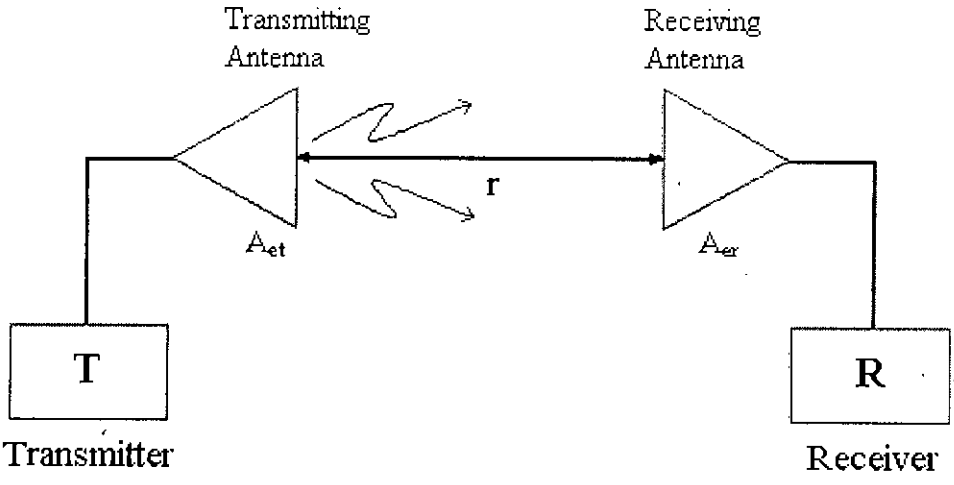

Fig. 2.9: The Radio Communication Link describing Friis Transmission Formula

Referring to fig. 2.9, let the transmitter feed a power P_t to a tramsmitting antenna of effective Aperture A_{et}. The antennas are assumed to be lossless and matched. At a distance r, a receiving antenna of effective aperture A_{er} intercepts some of the power radiated by the transmitting antenna and delivers it to the receiver R. Assuming for the moment that the transmitting antenna is isotropic, the power per unit area available at the receiving antenna is –

$$S_r = \frac{P_t}{4\pi r^2} \quad (W) \tag{2.1}$$

If the antenna has gain G_t, the power per unit area available at the receiver antenna will be increased in proportion as given by—

$$S_r = \frac{P_t G_t}{4\pi r^2} \quad (W) \tag{2.2}$$

Now the power collected by he lossless, matched receiving antenna of effective aperture A_{er} is—

$$P_r = S_r A_{er} = \frac{P_t G_t A_{er}}{4\pi r^2} \tag{2.3}$$

The gain of the transmitting antenna can be expressed as—

$$G_t = \frac{4\pi A_{et}}{\lambda^2} \tag{2.4}$$

Substituting this in (2.3) yields the **Friis Transmission Formula**—

$$\frac{P_r}{P_t} = \frac{A_{er} A_{et}}{r^2 \lambda^2} \quad (Dimensionless) \tag{2.5}$$

CHAPTER 3

THEORETICAL ANALYSIS OF THE WORK

3.1 WORK OUTLINE:

As discussed in chapter 1, the speed limitations of conventional interconnect metal lines have led to the concept of on-chip wireless interconnections using integrated antennas on Si. Microwave clock distribution using integrated antennas can reduce the chip area used in interconnection and also reduces the clock skew and dispersion, allowing a higher clock frequency for a given chip size. The reported studies of wireless interconnects using integrated antennas have focused on dipole antennas with field excitation along the plane of the antenna. We call this horizontal excitation in this work, and it is thus far the most convenient way of exciting the antennas in chips fabricated with planar IC technology. Different analytical derivations have been developed in this chapter to explain the behavior of the integrated dipole antenna at different situation under study. The effect of upper metal layer on the transmission gain of the dipole antenna has been investigated for the first time in this dissertation. The derived equation shows that the gain is lowered significantly if a metal layer is present above the antennas. This work also presents a novel approach of evaluating an equivalent two port T-modeled microwave circuit of a system-on-chip consisting of transmitting and receiving dipole antennas on Si wafer. Each component of the T-model represents a physical quantity, like the transmission antenna, receiving antenna and the medium. Finally, a new approach of exciting the antenna has been described. Since all practical IC fabrication processes involve multiple metal layers to reduce chip size due to wiring, it is important that an antenna structure is devised such that the affect of other metal layers on the signal propagated through the Si substrate is minimized. The analytical expression derived in this work has shown that the excited field mode propagates through the silicon substrate with constant antenna gain in presence of upper metal layers.

3.2 Theoretical Gain of a Dipole Antenna:

The performance of the dipole antenna can be explained analytically by using the Friis Transmission Formula, described in chapter 2. The cross sectional diagram of the structure under study has been shown in fig. 3.1.

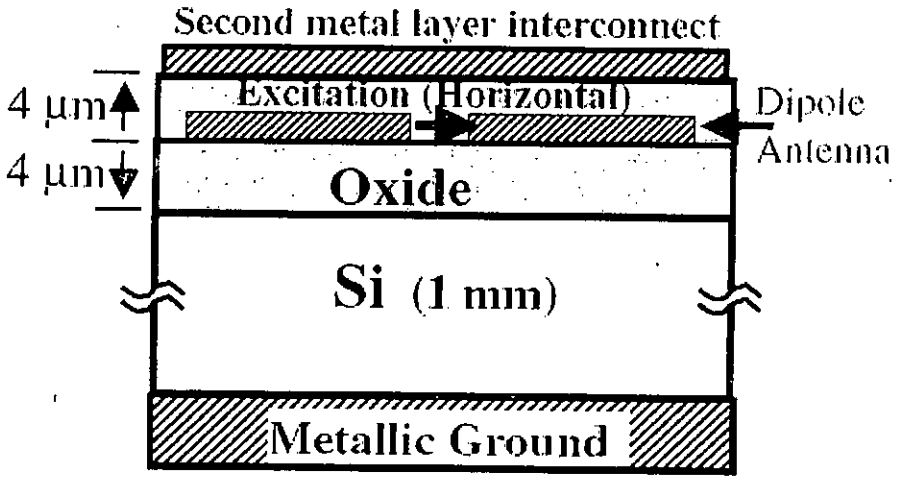

Fig. 3.1: Cross-sectional diagram of a dipole antenna excited horizontally.

According to this formula, the gain of the the antenna can be calculated from the equation—

$$\frac{P_r}{P_t} = \frac{A_{er}\, A_{et}}{r^2 \lambda^2} \qquad (3.1)$$

where,

P_r = received power in W,

P_t = transmitted power in W,

A_{et} = effective aperture of the transmitting antenna in m^2,

A_{er} = effective aperture of the receiving antenna in m^2,

r = distance between the transmitting and receiving antennas in m and

λ = wavelength in m.

In the entire work, the transmitting and the receiving antenna has been taken as identical. So, in the above equation, A_{et} becomes equal to A_{er} and taking $A_{er} = A_{er} = A$, equation (3.1) reduces to—

$$\frac{P_r}{P_t} = \frac{A^2}{r^2 \lambda^2} \tag{3.2}$$

However, when the second metal layer placed above the first metal layer, the second metal layer can be effectively considered as a metal plate and it serves as a mirror for the transmitting antenna. So, a mirror image of the transmitting antenna appears above it at a distance of d, as shown in fig.3.2.

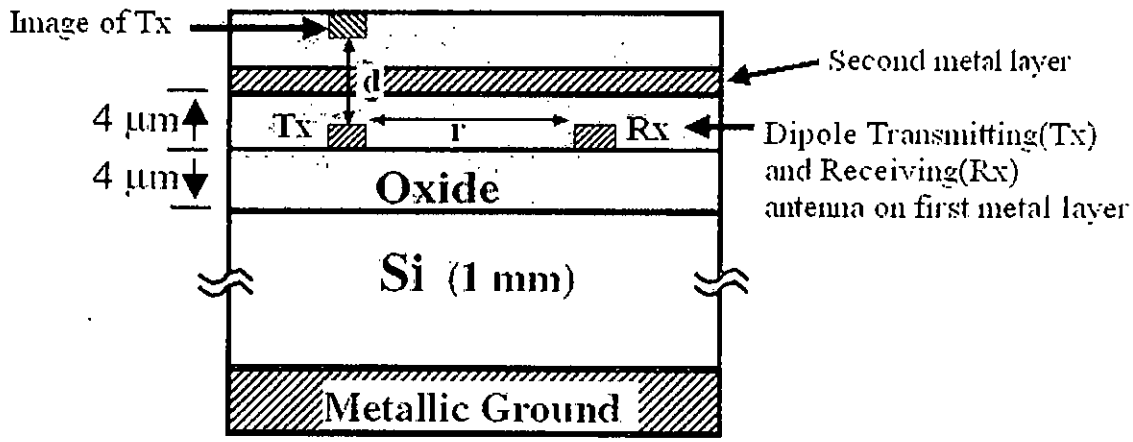

Fig. 3.2: Conceptual Diagram of the structure explaining the image theory when the antenna is excited horizontally.

The distance of the upper metal plate from the antenna is equal to the inter-layer metal distance which is $\frac{d}{2}$, as seen in the figure. Hence, the distance between the mirror transmitter and the receiver becomes $\sqrt{\left(r^2 + d^2\right)}$. The Si substrate is thick enough. So, the bottom plate can be considered to be relatively far away from the antennas. Thus, ignoring the contribution of the bottom plate at the receiving antenna, the gain of the receiving antenna in presence of the second metal layer can be written as—

$$\left(\frac{P_r}{P_t}\right)_m = \frac{A^2}{r^2\lambda^2} - \frac{A^2}{\left(r^2+d^2\right)\lambda^2} \tag{3.3}$$

In this case, λ is the wavelength in the Si substrate.

3.3 Effect of Variation of Resistivity and Antenna Distance on the Analytical Gain of the Antenna:

The work so far has been delineated without the effect of variation of resistivity [27,37]. As the gain of an antenna exponentially decreases with distance, equation (3.2) can be rewritten as—

$$\frac{P_r}{P_t} = \frac{A^2}{r^2\lambda^2} e^{-2\alpha r} \tag{3.4}$$

where,

α = Real part of $\left[j\omega\sqrt{\mu_{Si}\varepsilon_{Si}\left(1-j\frac{\sigma}{\varepsilon_0\omega}\right)} \right]$ = Attenuation Constant

$\omega = 2\pi f$, f is the operating frequency,

μ_{Si} = Silicon permeability,

ε_{Si} = Silicon permittivity,

σ = Conductivity of Si substrate.

Hence the effect of the resistivity is incorporated in this model. The equation (3.4) can be rearranged as follows –

$$\frac{P_r}{P_t} = \frac{A^2}{\left(re^{ar}\right)^2\lambda^2} = \frac{A^2}{r_{eff}^{\ 2}\lambda^2} \tag{3.5}$$

where, $r_{eff} = re^{ar}$ = Effective inter antenna distance.

This effective distance r_{eff} changes with both distance and the resistivity. So, this model can now explain the behavior of the integrated antenna at different distances as well as different resistivities. Hence, the parameter A can be again used as a frequency

dependent fitting parameter in this work using equation (3.5) which results an array of values at different frequencies.

3.4 DESCRIPTION OF THE ANALYTICAL MODEL:

The entire system of wireless transmission using the dipole antennas has been delineated as a two port T-modelled microwave circuit as shown in the fig. 3.3 [28].

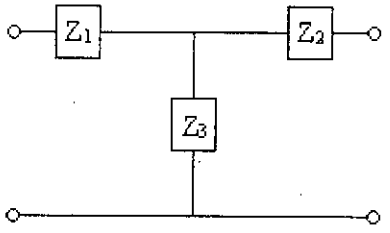

Fig. 3.3: The estimated T-model of the Antenna structure

The Z_1 has been considered as the transmitting antenna, Z_2 has been considered as the receiving antenna and Z_3 has been deemed as the transmitting medium. Then each of the elements of the model has been separately modeled. The total procedure can be described in the following steps —

3.4.1 Estimation of the entire system as T-Model:

The T-model has been derived from the Z-matrix obtained from the simulation. On the way to the model, the Z-matrix has been converted in the transmission (ABCD) matrix using the following formulae [28] —

$$A = \frac{Z_{11}}{Z_{21}} \tag{3.6}$$

$$B = \frac{Z_{11}Z_{22} - Z_{12}Z_{21}}{Z_{21}} \tag{3.7}$$

$$C = \frac{1}{Z_{21}} \tag{3.8}$$

$$D = \frac{Z_{22}}{Z_{21}} \tag{3.9}$$

Then the equivalent circuit parameters, Z_1, Z_2 and Z_3 have been calculated using the following equations –

$$Z_3 = \frac{1}{C} \tag{3.10}$$

$$Z_1 = Z_3(A-1) \tag{3.11}$$

$$Z_2 = Z_3(D-1) \tag{3.12}$$

The reciprocity of the system has been maintained in the proposed model as well as in the simulated structure.

3.4.2 Antenna Modeling:

The antenna has been modeled with the concept of ElectroMagnetic (EM) theory. As we know that antenna impedance depends upon the ratio of θ- component of the Elecrical field (E_θ) and φ-component of the magnetic field (H_φ), the equation of the impedance of any dipole antenna will be proportional to the following $\left(\frac{E_\theta}{H_\varphi}\right)$ term [29]—

$$\left(\frac{E_\theta}{H_\varphi}\right) = \frac{\frac{j\omega\mu}{r} + \frac{1}{j\omega\varepsilon r^3} + \frac{\eta}{r^2}}{\frac{jk}{r} + \frac{1}{r^2}} \tag{3.13}$$

where,

r is the distance between the transmitting and receiving antenna,

ω is the angular frequency and is equal to 2πf, f is the frequency of operation,

μ is the Permeability of the Si wafer,

ε is the Permittivity of the Si wafer,

η is the Intrinsic impedance of the Si wafer,

k is the wave number and is equal to $\omega\sqrt{\mu\varepsilon}$ *or* $2\pi f\sqrt{\mu\varepsilon}$

Equation (3.14) can be transform to a binomial series of the variable $(kr)^2$, like—

$$\left(\frac{E_\theta}{H_\varphi}\right)=\eta\left[1+\frac{1}{(kr)^2}\right]^{-1}-j\frac{1}{\omega^3\mu\varepsilon r^3}\left[1+\frac{1}{(kr)^2}\right]^{-1} \tag{3.15}$$

The real part of the modeled antenna, R should be proportional to the real part of equation (3.15) and the imaginary part of the same, X should be proportional to the imaginary part of equation (3.15). So, R and X can be written as—

$$R \propto \textit{real part of}\left(\frac{E_\theta}{H_\varphi}\right) \propto \eta\left[1+\frac{1}{(kr)^2}\right]^{-1} \quad \text{and}$$

$$X \propto \textit{imaginary part of}\left(\frac{E_\theta}{H_\varphi}\right) \propto \left[-j\frac{1}{\omega^3\mu\varepsilon r^3}\left[1+\frac{1}{(kr)^2}\right]^{-1}\right]$$

As $k=2\pi f\sqrt{\mu\varepsilon}$, then we can write the equation of R at a particular distance between the antennas as follows—

$$R=a_1-a_2f^{-2}+a_3f^{-4}-a_4f^{-6}+\cdots\cdots \tag{3.16}$$

$$X=-b_1f^{-3}+b_2f^{-5}-b_3f^{-7}+b_4f^{-9}+\cdots\cdots \tag{3.17}$$

where, a_1, a_2, a_3,..... and b_1, b_2, b_3,..... etc. are the constants for a particular r. Though the series is an infinite one, first 12 terms are sufficient for the best fit of the equation with the simulated data. The first term of the R is a frequency independent term representing the resistance of the Antenna element and the first term of X represents the dominance of the capacitive quality of the antenna in transmitting a signal.

As the transmitting and the receiving antenna impedance are same due to the reciprocity of the system, the model of the antenna satisfies both Z_1 and Z_2.

3.4.3 Transmission Medium Modeling:

The transmission line modeling has been done using the circuit theory. Z_3 of the proposed T-model represents the tranmission line or medium. The transmission medium has been assumed to be a circuit consisting of one resistance, one capacitance and one inductance each being parallel with others. The admittance of Z_3, Y_3 has been used to determine the parameters. At resonance point, the magnitude of Y_3 has been inverted to find the resistive value of the transmission line. The positive maximum value of the imaginary part of Y_3 gives the capacitive susceptance and the negative maximum value of the imaginary part of Y_3 gives the inductive susceptance of the medium. From these values, transmission line inductance and capacitance can be determined. Thus the RLC modeling of the transmission medium has been done.

The entire estimated system has been shown in fig. 3.4.

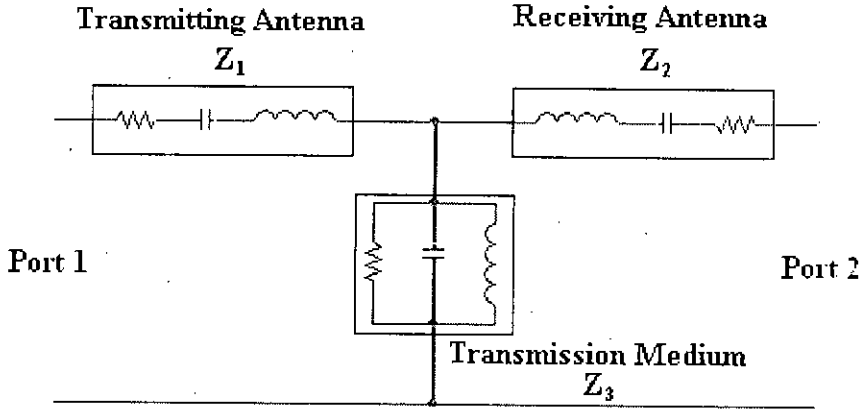

Fig. 3.4: The estimated T-modeled circuit in detail.

3.5 THE PROBLEMS IN USING DIPOLE ANTENNA WITH UPPER METAL LAYER:

The gain of the dipole antenna clearly indicates that upper metal layers contribute to the reduction of the dipole antenna gain at the entire frequency range of examination. Hence, in multilayer metal process, using a dipole antenna with horizontal excitation is not a preferable and appropriate decision.

Again, recent sucessful fabrication of an interated low noise amplifier (LNA) has been reported in the GHz frequency range [30]. This LNA has more than 40 dB voltage gain. For the efficient use of the integrated dipole antenna along with this LNA in on chip wireless interconnect system, the gain of the dipole antenna needs to be more than -50dB. This implies that dipole antenna with horizontal excitation can not be used efficiently in multi-layer processes. Therefore integrated antenna structure in Si which can overcome the effect of second and upper metal layer for wireless interconnect has become an exigency.

3.6 THE IMPROVED INTEGRATED ANTENNA— MONOPOLE:

In order to improve the performance of the integrated antenna, monopole antenna can be a better substitute of the dipole antenna. In case of monopole, the excitaion is given vertically through the Si substrate. The structure has been shown in fig. 3.5.

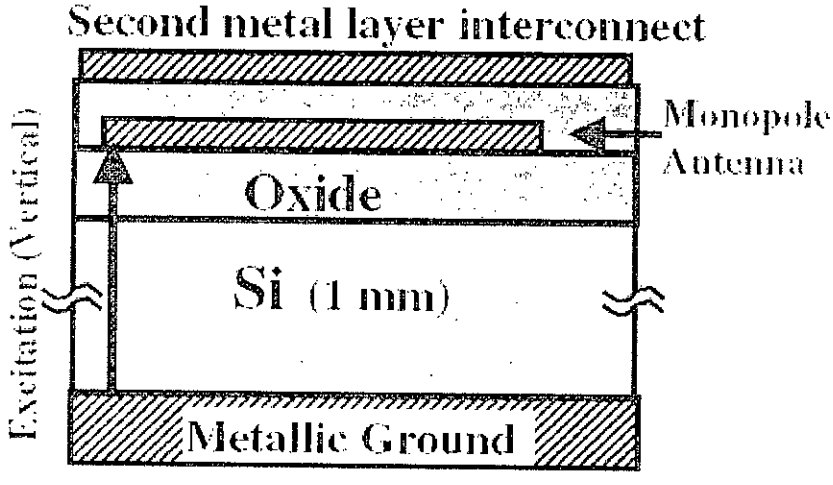

Fig. 3.5: Cross-sectional diagram of a monopole antenna excited vertically through the Si layer.

3.7 Analytical Gain of Monopole Antenna:

The transmission of power from the transmitting monopole antenna to the receiving antenna can be explained by dielectric waveguide concept. Without the presence of the upper metal layer, the oxide layer and the metallic ground of the structure create a waveguide for the propagation of energy. On the other hand, when the second metal layer is present, the dielctric waveguide becomes parallel plate waveguide and the energy propagation remains almost uneffected and unchanged.

The radiation intensity, I, in terms of transmitting power, can be written as—

$$I = \frac{P_t G_t}{r} \tag{3.18}$$

where,

P_t = total power transmitted by the antenna,
G_t = antenna gain,
r = the distance between transmitting and receiving antenna.

Again, if A is the effective area of the antenna, then the power received by the receiving antenna is given by—

$$P_r = I.A \tag{3.19}$$

Hence, the gain of the receiving antenna becomes—

$$\frac{P_r}{P_t} = \frac{AG_t}{r} = \frac{K}{r} \tag{3.20}$$

The parameter K can be assumed to be independent of frequency as the length of the antennas are much smaller than the wavelength. So, equation (3.20) represents the gain of a monopole antenna to be constant with the variation of frequency for a fixed distance.

3.8 DISCUSSION:

The theories that are developed in this work explain the characteristics of the dipole antenna and model the entire dipole antenna structure. The work also focuses on the problem of the performance using a dipole antenna in a multilayer process and proposes a new antenna structure i.e., monopole antenna with vertical excitation to overcome this problem. The support of simulation results by matching the simulation values with the values developed theoretically (shown in the next chapter) can confirm the ground of the theory emerged here.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 WORK SUMMARY:

The effect of the other metal layers on the transmission gain of the antenna has not been studied before; it has been done for the first time in this thesis. In this work, we report that the forward transmission coefficient of the transmitting antenna is drastically reduced in a multi-layer metal interconnect scheme when a second metal layer is placed above the antenna at the usual inter-layer metal distance. Therefore, further investigation in this work has been made on the dipole antenna without any layer on top. This work also demonstrates the change in forward transmission gain of the dipole antenna with the change in resistivity of the medium, Si substrate in this case, as well as the change in inter antenna distance. Here it has been seen that the forward transmission gain becomes saturated with the increase in resistivity and distance. Simulations have been carried out using the ANSOFT high frequency structure simulator (HFSS) program employing three dimensional (3-D) finite element method. A simplified analytical model has also been developed that explains the drastic reduction in antenna transmission co-efficient in the presence of neighboring metal layers in a multi-layer process and also the effect of Si resistivity and inter antenna distance. The same structure has been used for the simulation in case of the modeling. The simulation of the antennas has been done with horizontal excitation without any second metal layer, because this excitation is mostly used in the conventional VLSI circuits. The impedance matrix of the system has been extracted from the simulation. Then, Transmission (ABCD) matrix has been determined using this Impedance[Z] matrix.

All the above discussions have focused on the dipole antenna as the most conventional way of utilizing antennas on chip. Here, we have shown that the adverse effect of a neighboring metal layer in a multi-layer metal process of dipole antenna can be avoided by designing it with the first metal layer and exciting it vertically through the

Si substrate. In this case, the excited field mode propagates through the silicon substrate without any reduction in the power transmission of the antenna due to the presence of upper metal layers.

4.2 SIMULATED DEVICE STRUCTURE:

Fig. 4.1 shows the structure of the antennas used for the simulation. The excitation has been given horizontally through the plane of antenna.

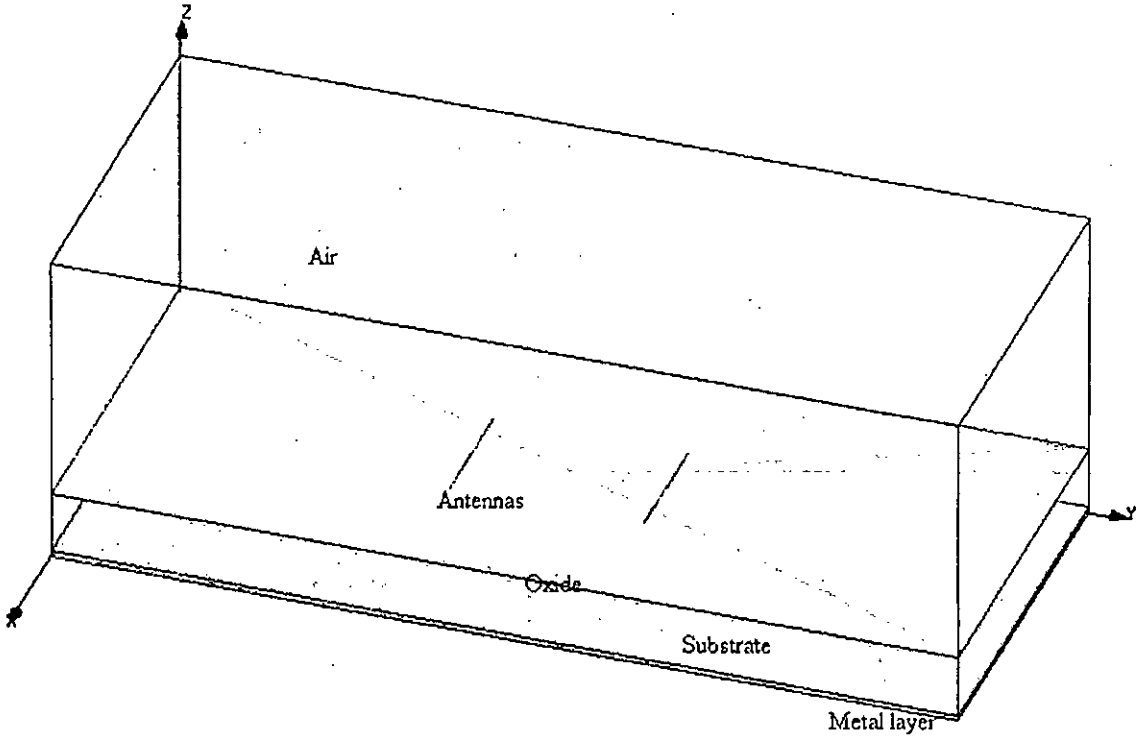

Fig. 4.1: The structure used in the simulation.

The structure was grown on a thick metallic ground placed at the bottom. The substrate, 1 mm thick Si layer, was on the metallic ground. The antennas were formed using first metal layer, which is 1μm thick Aluminium(Al). The substrate and the metal is separated by an insulator— 4 μm thick SiO_2 layer. The permittivity of Si and SiO_2 was taken as 11.9 and 4 respectfully and the conductivity of the Al is 3.5×10^7 mho/m.

4.2.1 Dipole antenna— s-matrix data extraction:

The cross sectional diagram of the structure used for simulation has been shown in fig. 4.2.

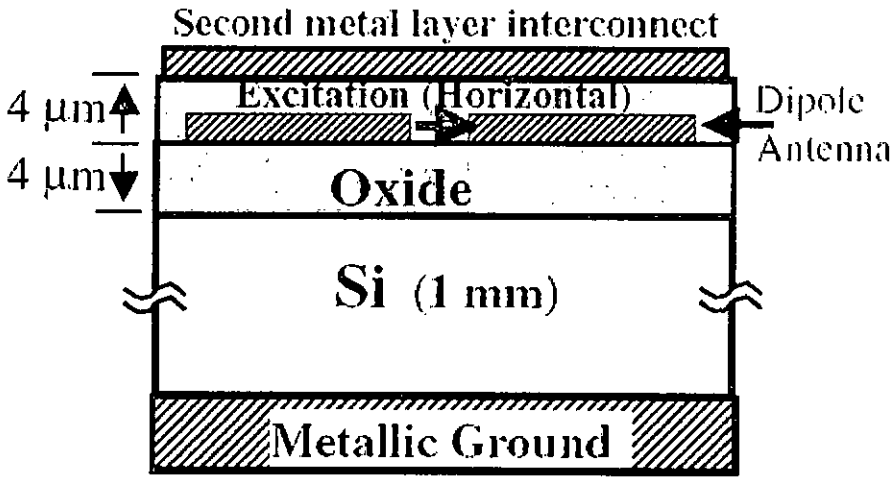

Fig. 4.2: Cross-sectional diagram of a dipole antenna excited horizontally. Simulation was carried out with and with out the second metal layer.

The variations in the s-parameter between the transmitting and receiving antennas, in different situations, was analyzed in this work. The variations are as belows—

- With and without the second metal layer. The space between the first and second metal layers was filled with SiO_2.
- By varying the frequency from 1GHz to 30 GHz with 1 GHz step.
- By changing the resistivity of Si substrate from 10Ω-cm and 1000Ω-cm.
- By varying the inter antenna distance from 3mm to 10mm.

The effect of placing metal layers above the antenna was examined. For this, a second metal layer was placed above the antenna. The layer consists of 1 μm thick Al and was at a 4 μm distance.

4.2.2 Dipole antenna— Z-matrix data extraction:

In this case, there was no upper metal placed above the dipole antennas. The Z matrix of the system during the transmission of the signal has been extracted using the simulation. The input port of the system, i.e., the input terminals of the transmitting antenna has been considered as port 1 and the output terminals of the receiving antenna is said to be port 2.

The Z matrix was collected at different situations of dipole antenna, like—

- At several frequencies starting from 5GHz to 30GHz with 1GHz step.
- At different distances between transmitting and receiving antenna. The distance was varied from 3mm to 5mm with 1mm step.

Each simulation was done at each resistivity of Si substrate at a perticular distance between the antennas. Then all the four components of the Z matrix was collected at different frequencies— Input impedances (Z_{11}, Z_{22}) and the transfer impedances (Z_{12}, Z_{21}). These impedances has been used for the further analysis and system modeling.

4.2.3 Monopole antenna— s-matrix data extraction:

In order to improve the performance of the integrated antenna, monopole antenna can be a better substitute of the dipole antenna. In case of monopole, the excitaion is given vertically through the Si substrate. The structure has been shown in fig. 4.3.

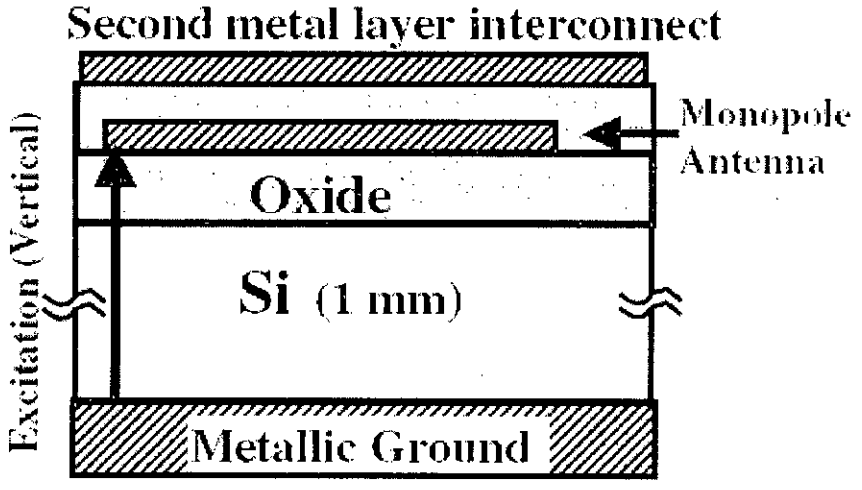

Fig. 4.3: Cross-sectional diagram of a monopole antenna excited vertically through the Si layer. Simulation was carried out with and with out the second metal layer.

As shown in the figure, the structure is same as in case of dipole antenna, the only difference is in the direction of the excitation. The variation of forward transmission gain (S_{21}) with frequency has been investigated for this excitation.

4.3 SIMULATION METHOD:

The simulation of the structure was executed by using the ANSOFT high frequency structure simulation (HFSS) program. It is a three-dimensional full-wave finite element electromagnetic simulator. In this software, the simulation region is divided into a large number of tetrahedral — a single tetrahedral is basically a four-sided pyramid. HFSS stores the components of the H-field or E-field that are tangential to the three edges of the tetrahedron at each vertex of the tetrahedron.

In addition, the system can store the component of the vector field at the midpoint of selected edges that is tangential to a face and normal to the edge (Fig. 4.4). The field inside each tetrahedron is interpolated from these nodal values. By representing field quantities in this way, the system can transform Maxwell's equations into matrix equations that are solved using traditional numerical methods.

In the simulation, adaptive mesh was used. In adaptive mesh, the simulated structure is initially divided into a coarse number of finite elements of tetrahedral shape. The number of tetrahedrons is gradually increased by 20% between each successive simulation until the simulated s-parameter show a 99.9% match between two successive simulations at every vertex of every tetrahedron in the entire simulated structure. The result of the simulation was stored as the variation of the forward transmission co-efficient (S_{21}) with the frequency of the antenna at different situations.

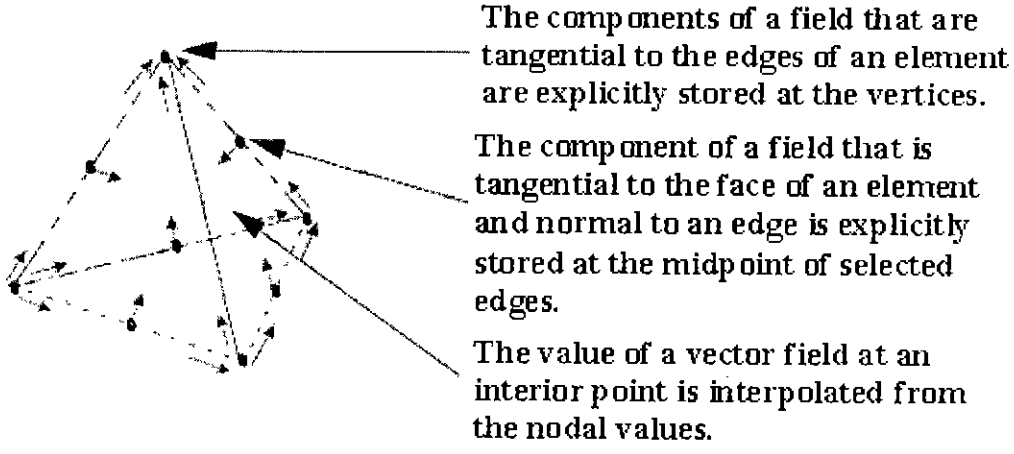

Fig. 4.4: Three Dimensional finite element (Tetrahedron)

4.4 COMPARISON BETWEEN THE SIMULATION RESULTS AND ANALYTICAL DATA OF S_{21}—WITH AND WITHOUT UPPER METAL LAYER IN CASE OF DIPOLE ANTENNA:

The simulation results were saved as the transmission gains of the dipole antenna. The graph of forward transmisison gain (S_{21}) vs. frequency of the dipole antenna excited horizontally is shown in fig. 4.5. In this case, the length of the dipole antenna was 2mm, the transmitter and the receiver were separated by a distance of 3mm and Si resistivity was set to be 1000 Ω-cm.

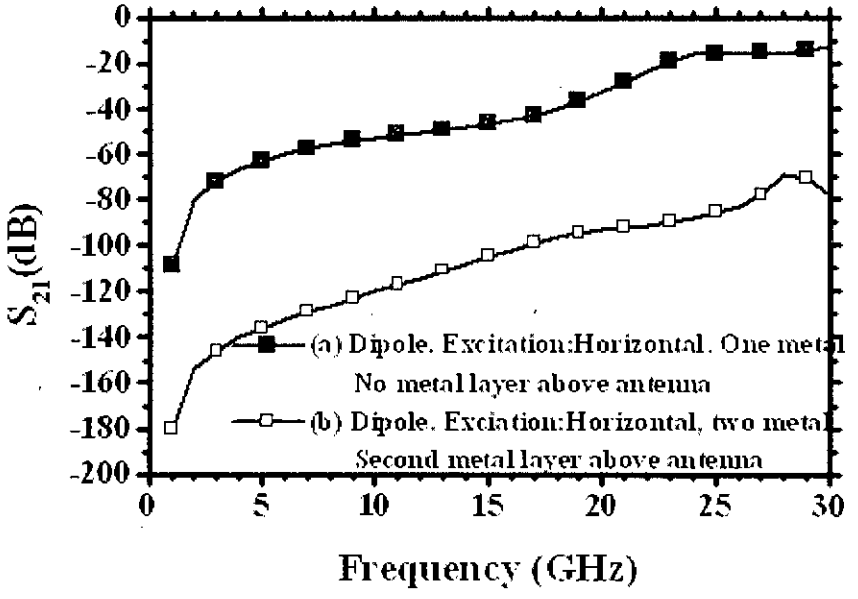

Fig. 4.5: Simulation result: Variation of the Forward transmission coefficient (S_{21}) with frequency for a horizontally excited Dipole antenna.

The graph clearly shows and indicates the effect of placing the metal layers at the top of the first metal layer. In case of one metal layer, as shown in curve (a) of the figure, the transmission gain is lower value at low frequency and then starts to increase with the increase of frequency. The presence of a second metal layer on the top of the first metal layer shows same pattern of variation transmission gain (S_{21}) with frequency but the transmision gain decreases significantly at each frequencies. For example, the gain deceases from -52.9 dB to -120 dB at 10 GHz and from -32 dB to -93.4 dB at 20 GHz. Second metal layer was placed at a distance of 4 μm above the transmitting antenna, which is the usual metal layer distance of VLSI circuits. This close proximity of the metal layers results the zero boundary condition for the electric field on the metal surface and prevents the transmitting antenna from effective radiation.

In theoretical analysis, A has been taken as the frequency dependent fitting parameter. At first, the equation (3.2) was used for the best fit between the analytical gain of the receiving antenna and the simulated gain of the receiving antenna without the presence of any upper metal layer. These values of A at different frequencies obtained from the above fitting has been used in equation (3.3) to determine the analytical gain of

the receiving antenna in the presence of the upper second metal layer. The resultant curves of the analytical gain (S_{21}) have been shown in fig. 4.6. In the same figure, the simulated gain (S_{21}) has also been plotted for comparison. And it can be seen that the analytical and the simulated data has similar tendency and affinity. So, from the figure, it is apparent that the presence of upper layer drastically reduces the gain of the receiver, which can be explained by the mirror image of the transmitting antenna formed in presence of the upper metal layer.

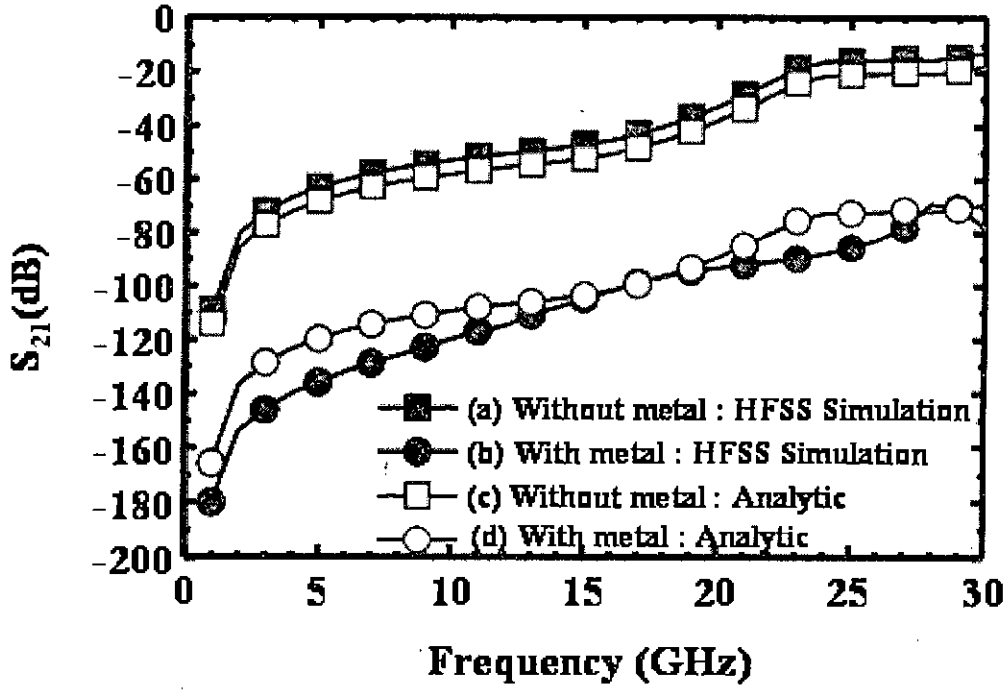

Fig. 4.6: Comparison of antenna transmission gain of dipole antenna between simulated data and analytically calculated values using HFSS.

4.5 THE EFFECT OF VARIATION IN RESISTIVITY ON S_{21} OF THE DIPOLE ANTENNAS— COMPARISON BETWEEN SIMULATED AND ANALYTICAL DATA:

As already mentioned, for a given distance, A has been used as the fitting parameter to match one curve of the analytic gain with HFSS results. This A, being an array at different frequencies, has been used as frequency dependent fitting parameter in this work, using equation (3.5) which includes the effect of resistivity as well as inter

antenna distance. A is determined from the simulated result in case of the resistivity 1000 ohm-cm and inter antenna distance of 3mm, as the gain gets saturated beyond this value of resistivity. This A has been used for the other different resistivities and distances under study. Fig. 4.7 shows the Forward Transmission Co-efficient (S_{21}) versus frequency curve at different resistivities at an inter antenna distance of 3 mm. The simulated and analytical results in case of 1000 ohm-cm have been the same as this curve has been used for determining the array of A. One noticeable point is that the results are well matched in higher frequencies rather than the lower frequencies in case of 10 ohm-cm. Friis Transmission formula is more appropriate for the far field of an antenna. It does not include the effect of the reactive field. As a result, the analytical curve shows clear difference with the simulated one for 10 ohm-cm as it does not include the gain due to the reactive field at low frequencies.

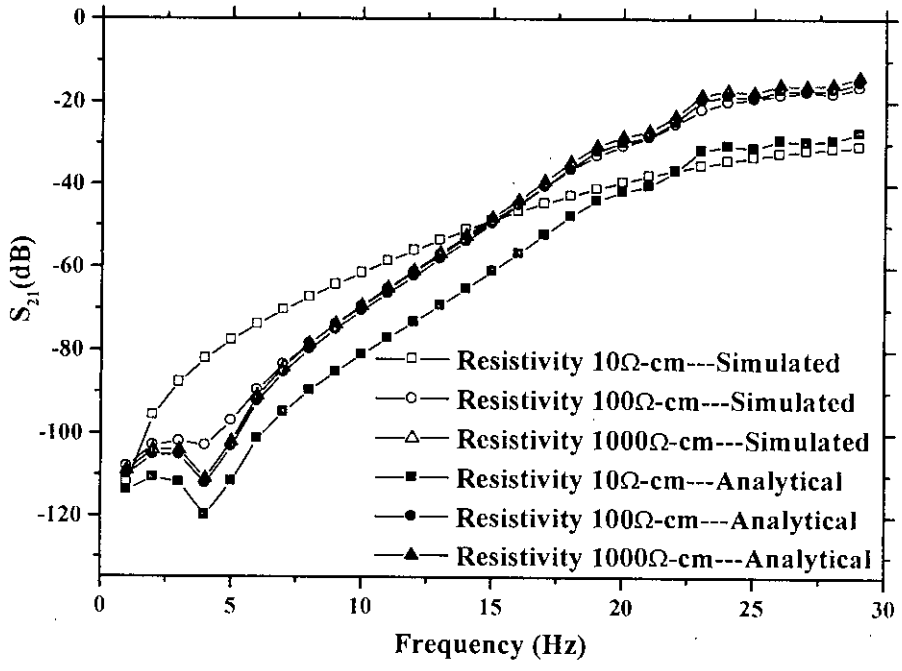

Fig. 4.7: Comparison between the simulated and analytical Forward Transmission Co-efficient (S_{21}) of the structure under study at different resistivity. The plot is a semi log one, i.e., S_{21} values are in dB.

For example, for 10 ohm-cm, the difference between analytical and simulated S_{21} are 19.6585dB and 2.1771dB at 10GHz and 25GHz, respectively. In case of 100 ohm-cm,

the effective distance becomes sufficient for the field to be far. So, the analytical curve is in well harmony with the simulated one. For example, at 25GHz, the difference between analytical and simulated S_{21} are 2.1771dB and 0.2201dB for 10 ohm-cm and 100ohm-cm, respectively. As seen in the figure, the gain increases with the frequency, but gets saturated at higher frequency irrespective of the value of resistivity.

4.6 THE EFFECT OF VARIATION IN DISTANCE BETWEEN THE DIPOLE ANTENNAS ON S_{21} — COMPARISON BETWEEN SIMULATED AND ANALYTICAL DATA:

The same array of A, mentioned in case of variation in resistivity, has been used to determine S_{21} for different distances. Fig. 4.8 shows the forward transmission co-efficient (S_{21}) versus frequency at different distances between the antennas having the resistivity of Si substrate 1000 ohm-cm. This curve also shows the saturation of S_{21} in higher frequencies at each distance between the antennas. The same dissimilarity of the curves is seen at the lower frequencies, the differences between the analytical and simulated values are noticeable in case of both 7mm and 10mm. The reason is again the reactive field effect at low frequencies. The values match well at high frequencies.

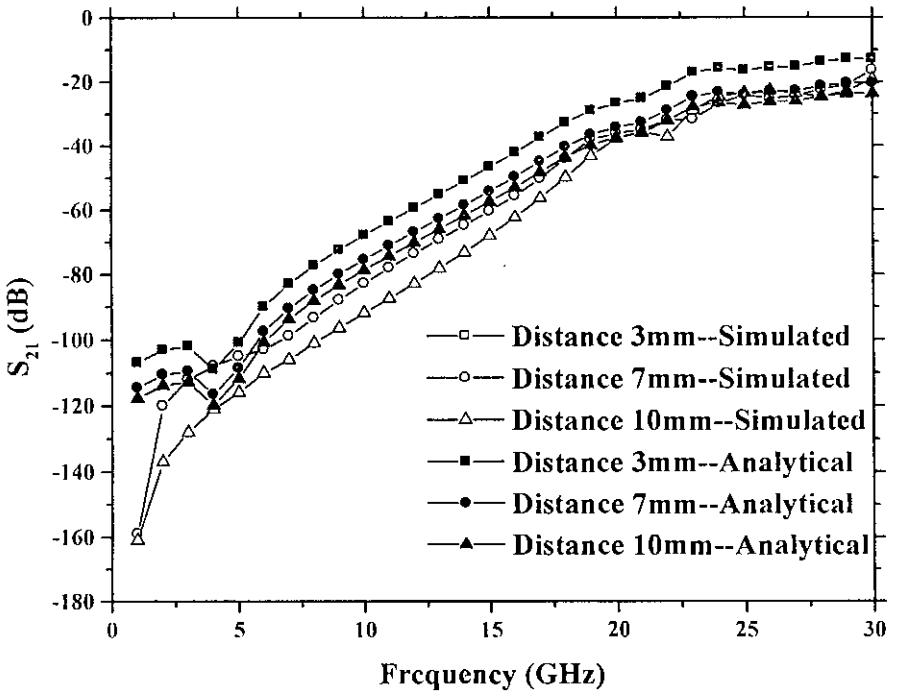

Fig. 4.8: Comparison between the simulated and analytical Forward Transmission Co-efficient (S_{21}) of the structure under study at different inter antenna distances. The plot is a semi log one, i.e., S_{21} values are in dB.

As shown in the figure, for 7mm distance, the differences between S_{21} are 7.3515dB and 0.1515dB at 10GHz and 25GHz, respectively. And for 10mm distance, the differences between S_{21} are 13.2118dB and 3.7882dB at 10GHz and 25GHz, respectively.

4.7 COMPARISON BETWEEN THE SIMULATED CIRCUIT PARAMETERS AND THE ANALYTICAL PARAMETERS OF THE ANTENNA MODEL:

The antenna has been modeled to be a series circuit having both Resistive and Reactive part. The equation (3.16) and (3.17) has been used for the real and imaginary part of the impedance respectively. Fig. 4.9 [(a) is for the Resistive part, (b) is for Reactive part of the antenna and (c) is for Impedance part of the antenna] shows the

comparison between the Simulated and Modeled antenna impedance. The distance between the antennas was 3mm in this case and the resistivity of the Si substrate was 10Ω-cm As can be seen from the figure, impedance of the modeled antenna is in good harmony with the simulated one.

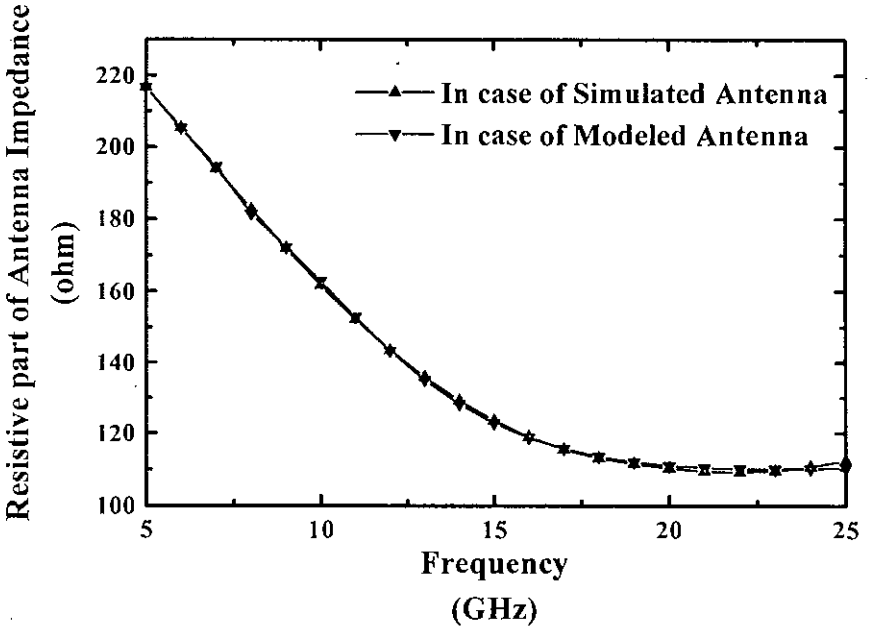

Fig. 4.9(a): The comparison of the Transmitting or Receiving Antenna resistance between simulated data and analytically calculated values of the estimated model.

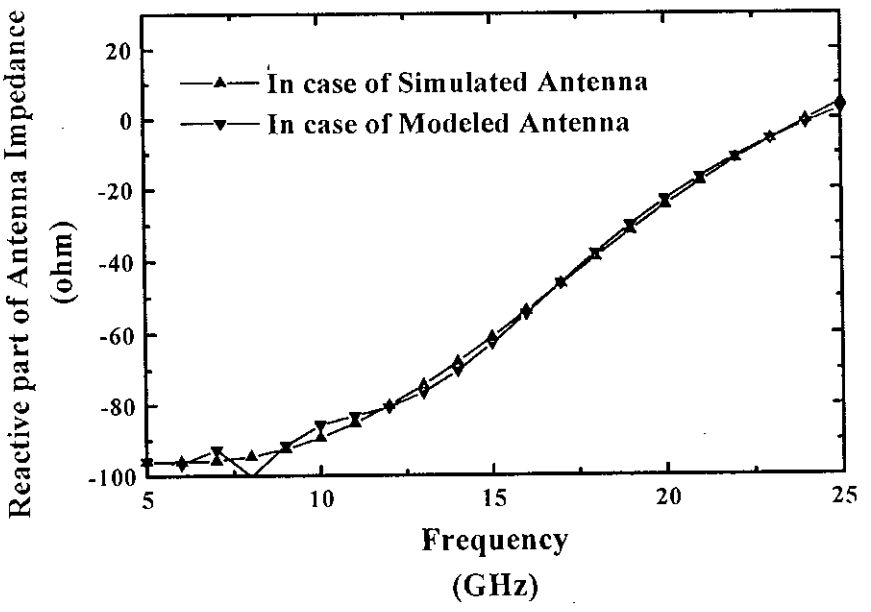

Fig. 4.9(b): The comparison of the Antenna Reactance between simulated data and analytically calculated values of the estimated model.

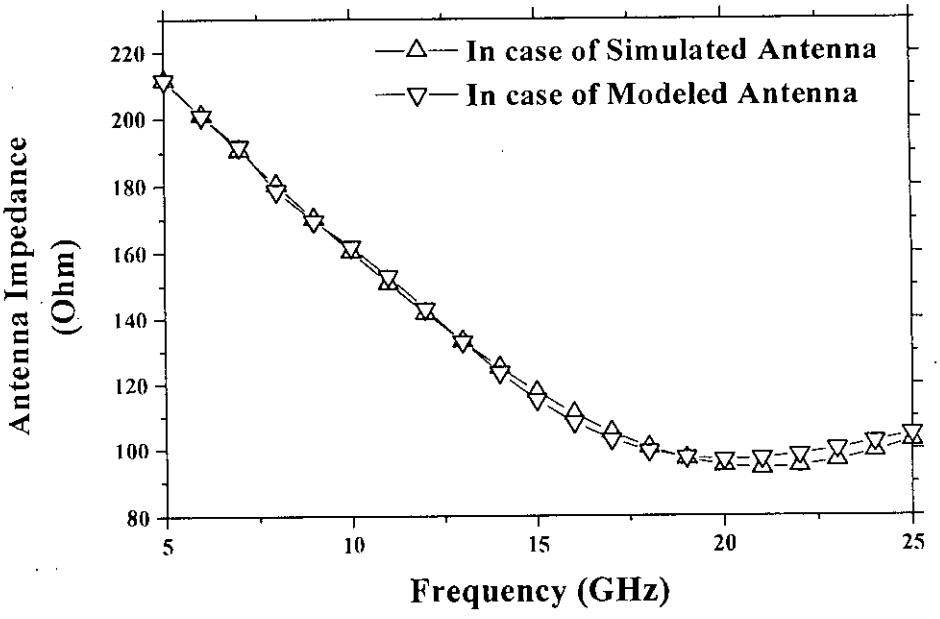

Fig. 4.9(c): The comparison of the Antenna Impedance between simulated data and analytically calculated values of the estimated model.

4.8 DIPOLE ANTENNA MODEL AT DIFFERENT DISTANCE:

The characteristics of any antenna do not change with the inter antenna distance. The proposed antenna model has been determined individually at each distance, and then compared to each other. The comparison has been shown in fig. 4.10. The distance between the antennas has been varied from 3mm to 6mm with 1mm step. As seen in the figure, the impedances are not exactly equal to each other. In addition, the variations of the real and imaginary parts of the impedances of antennas at different distances are not in the same order. These two effects have changed the phase of the impedances as well. The differences among the values are not ignorable though unexpected. The reason for these differences can be explained by the effect of circulating current in the Si wafer due to the electromagnetic induction and effect of the reactive field between the antennas.

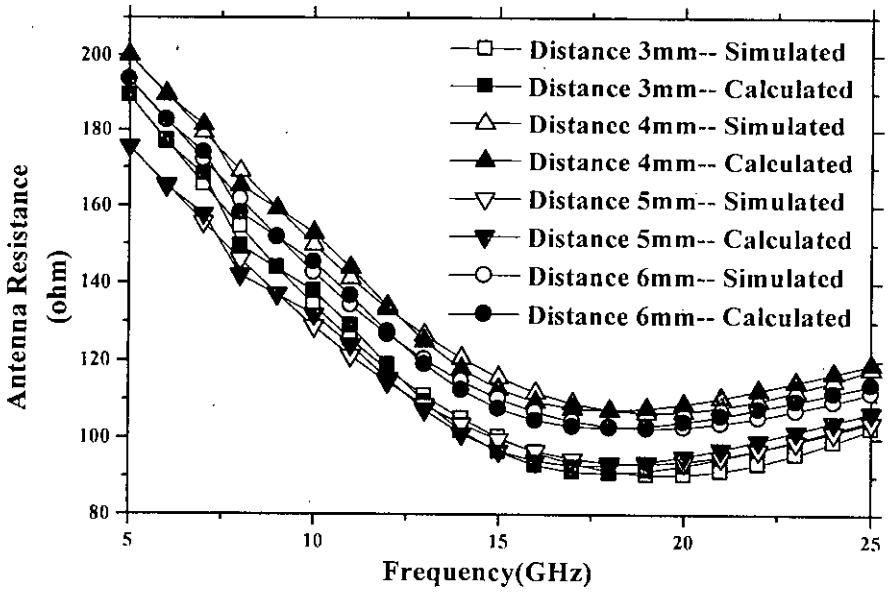

Fig. 4.10(a): Antenna Resistances at different inter antenna distances— the simulated data and calculated values from the estimated model and comparisons among them.

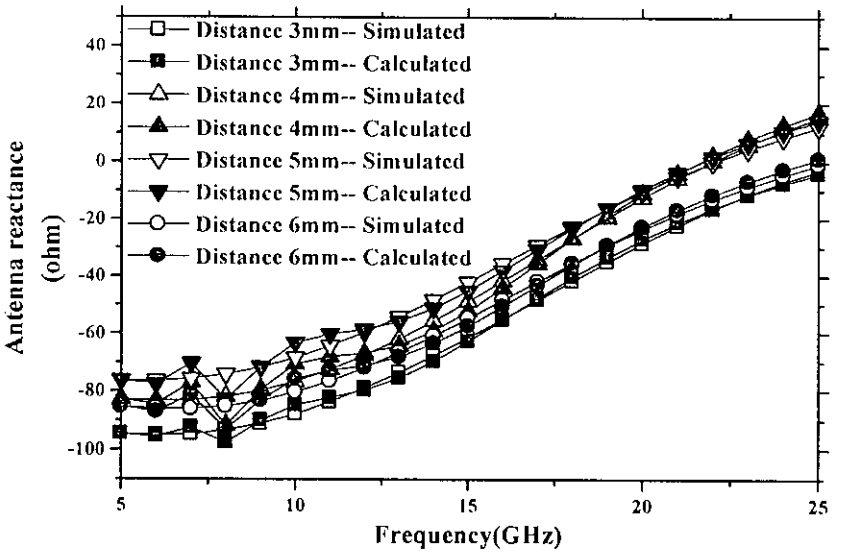

Fig. 4.10(b) Reactances of the Antennas at different inter antenna distances— Comaprisons among the simulatcd values and calculated data.

4.9 TRANSMISSION LINE MODEL OF Si SUBSTRATE AT DIFFERENT DISTANCE:

The characteristics of the transmission line should change with the inter antenna distance. As the transmission line has been modeled as circuit consisting of resistance, capacitance and inductance in parallel, the parameters have been shown in terms of admittance instead of impedance. In the fig. 4.11, the real and imaginary part of the estimated transmission line model and the simulation structure data have been plotted for comparison. As seen in the fig. 4.11(a), the real part of the transmission line admittance of the simulation structure has a variation with frequency with even negative value. This variation reflects the problem of simulation spurious, as the deviation of the conductance values are not of wide range. So, the conductance of the proposed transmission line model has been estimated to be the mean value of all the simulated data. The simulation spurious also affected the susceptance of the transmission line, as can be seen from the figure 4.11(b).

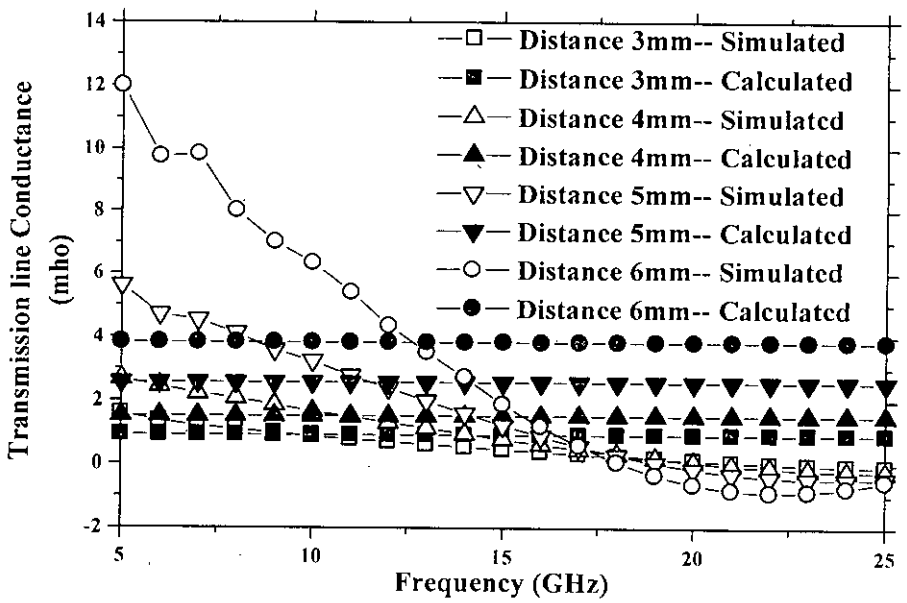

Fig. 4.11(a): Comparison among the calculated and the estimated Transmission Line Conductances at different frequencies.

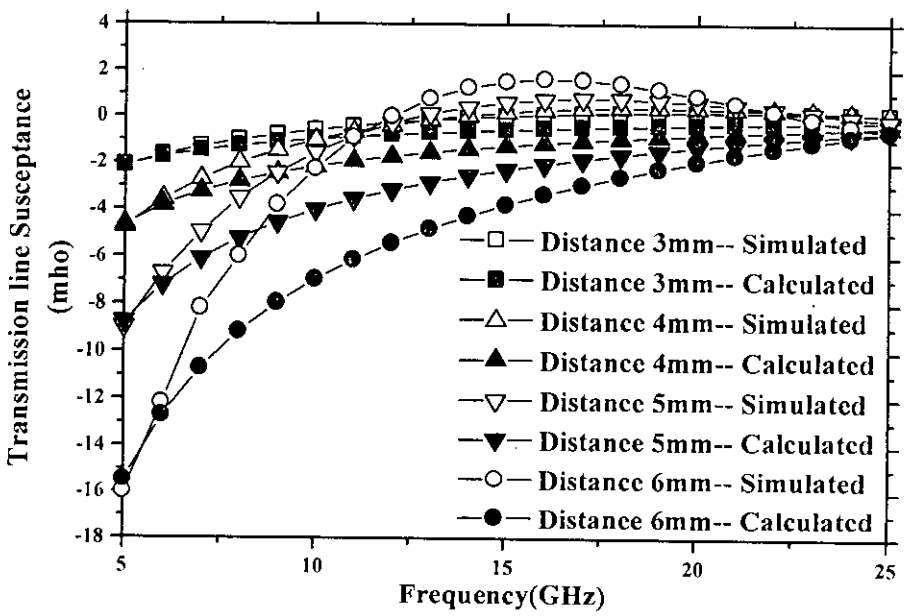

Fig. 4.11(b): Comparison among the calculated and the estimated Transmission Line Susceptances at different frequencies.

4.10 COMPARISON BETWEEN THE SIMULATION S-MATRIX AND S- MATRIX OF THE PROPOSED MODEL:

The ultimate aim of this work is to determine the Forward Transmission Co-efficient of the proposed model. The Reflection co-efficient S_{11} and Forward Transmission co-efficient S_{12} of the dipole antenna in case of different distances has been shown in fig. 4.12. At each distance, calculated co-efficients have been compared with the simulated data. The discrepancies between the data are due to the problem in transmission line modeling which occurred in the simulation. Though this probelem exists, the simulated data and the calculated values are in good agreement. The co-efficients are in log scale.

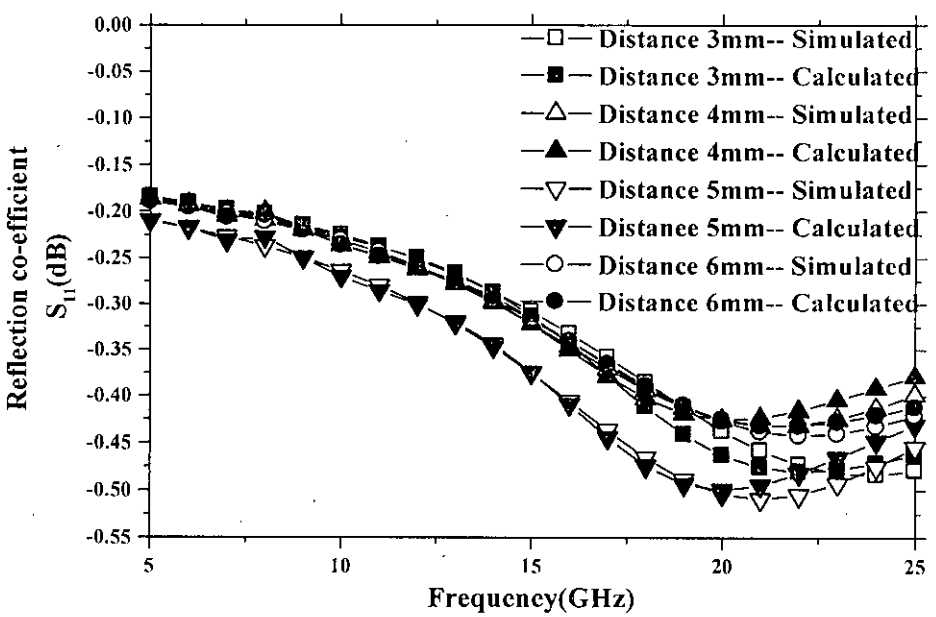

Fig. 4.12(a): Comparison among the calculated and the estimated Reflection Co-efficient (S_{11}) at different frequencies.

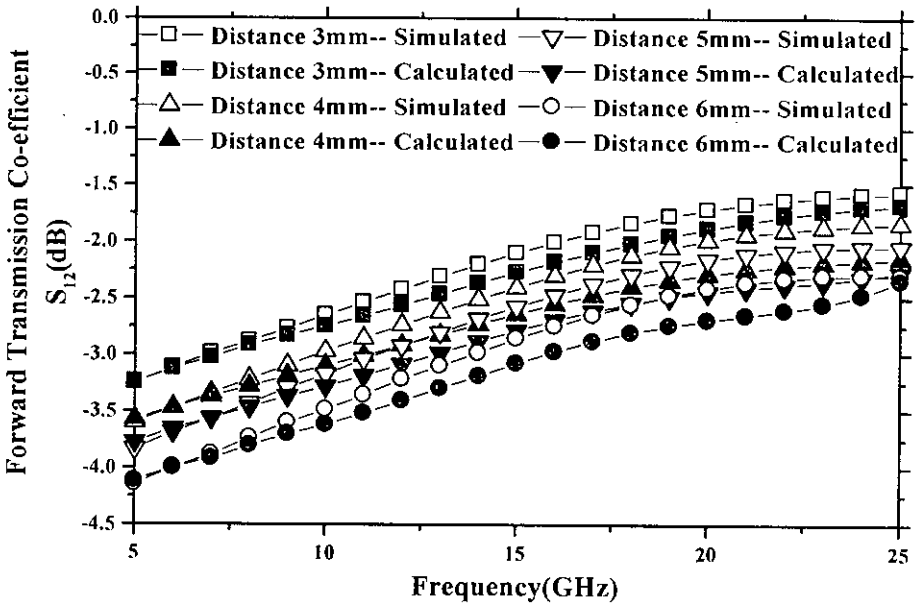

Fig. 4.12(b): Comparison among the calculated and the estimated Forward Transmission Co-efficient (S_{12}) at different frequencies.

4.11 COMPARISON BETWEEN THE SIMULATION RESULTS AND ANALYTICAL DATA OF S_{21}—WITH AND WITHOUT UPPER METAL LAYER IN CASE OF MONOPOLE ANTENNA:

As indicated earlier, the structure of the monopole antenna is same as that of dipole antenna, the only difference is in the direction of the excitation. The excitation is in vertical direction to make the antennas monopole. The variation of forward transmission gain (S_{21}) with frequency for monopole is shown in the fig. 4.13.

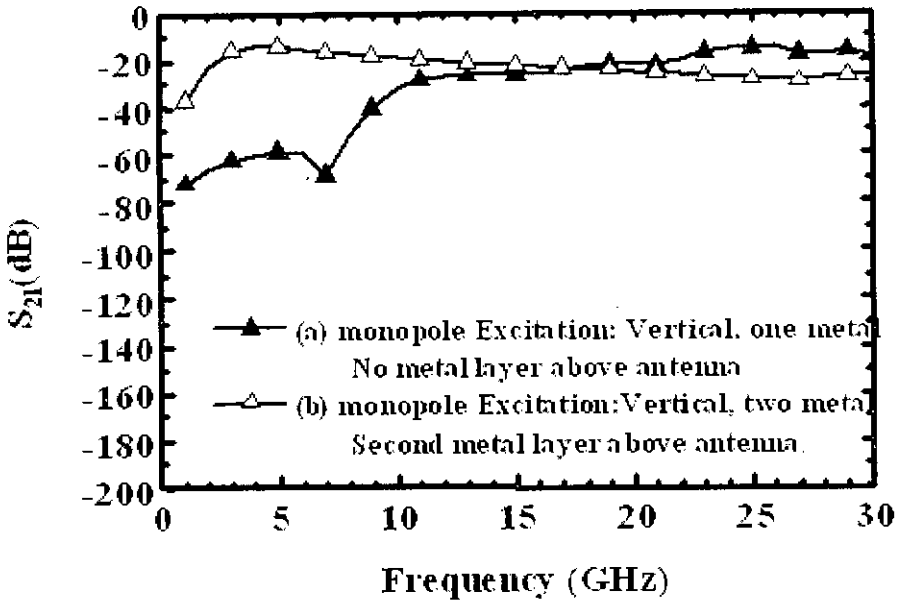

Fig. 4.13: Simulation result: Variation of the Forward transmission coefficient (S_{21}) with frequency for a vertically excited Monopole antenna.

From the curves of the Forward transmission co-efficient in case of with or without upper metal, it is clear that there is almost no effect of upper metal layers on the transmission co-efficient in case of monopole antenna excited vertically. The trend of the S_{21} curve has also been changed – it has become almost constant with the variation of frequency as well as the presence of metal layer. Moreover, the gain at low frequencies has been increased than that of the dipole.

K has been used as a fitting parameter in case of monopole antenna and the equaiton (6.20) has been fitted with the HFSS simulation data. The analytical result along with the simulation data has been shown in the fig. 4.14.

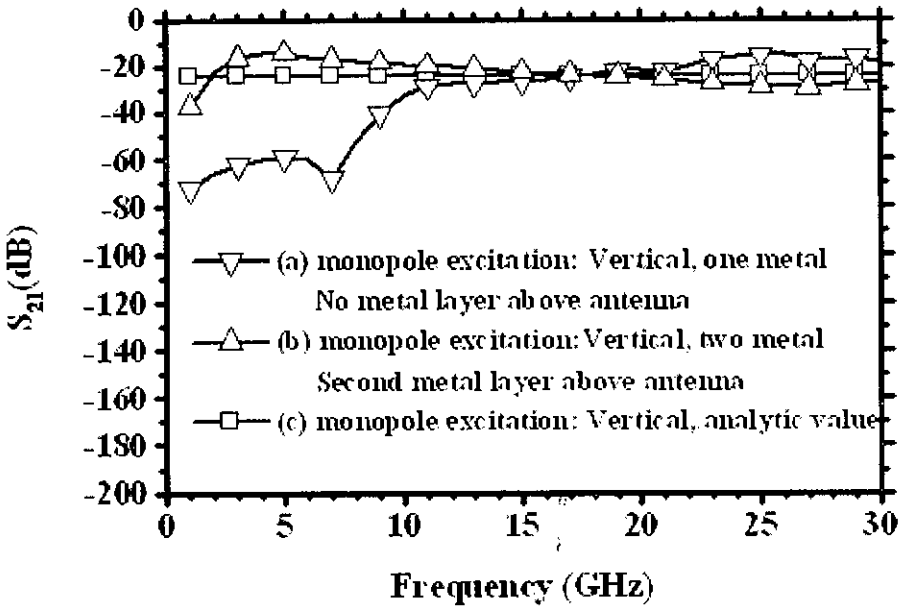

Fig. 4.14: Comparison of antenna transmission gain of monopole antenna between simulated data and analytically calculated values using HFSS.

As seen from the figure, the pattern of the forward transmission gain is flat over the examined frequency range. The performance of monopole antenna with vertical excitation not only eliminates the problem of dipole antenna but also transforms those disadvantages into advantages. For example, the gain of the monopole antenna remains unchanged when upper metals are placed. So, this monopole antenna can be easily utilized in multilayer systems with LNA, meeting the requirement of at least -50dB gain. Monopole antenna gives additional advantage of having same higher gain at lower frequencies also, whereas, Dipole has lower gain at lower frequencies.

4.12 CONCLUSION:

Integrated antenna can be widely utilized to produce Ultra Wideband (UWB) ultra short pulse, which is essential for the UWB transmitter circuit [31]. The effect of any top or bottom metal layer in a multilayer metal process on the transmission characteristics of an integrated antenna has been investigated here. If we approximate the interconnect metal layers as a solid metal plate, the simulation shows that a very small amount of

power propagates when the dipole antenna is excited horizontally parallel to the plane of the Si substrate in the presence of a second metal layer interconnect above the antenna [27]. The drastic reduction in transmitted power can be explained using the Friis transmission formula and image theory.

The effect of resistivity and distance between the antennas has also been examined in this work. Both simulation and analytical analysis show that the transmission gets maximum and saturated in higher frequencies and higher resistivity. From the curves, we can see that simulated S_{21} is higher than the analytical one in the lower frequencies. But at high frequencies, the simulated antenna gains are in good harmony with the analytical one. As the RF antennas generally used in the high frequencies, the result is quite agreeable.

This work also delineates a novel model of the structure of the dipole antenna on chip under investigation. The performance of the model is quite satisfactory.

This thesis also depicts that if we excite a monopole antenna vertically through the Si substrate, the excited mode propagates through the Si substrate, and any metal layers on top of the antenna do not hinder the field propagation. For integrated antenna system in a multi level metal process, the system is expected to perform better if the antenna on the first metal layer is excited vertically through the Si substrate to achieve a higher transmission coefficient.

CHAPTER 5

CONCLUSION

5.1 SUMMERY OF THE WORK:

This thesis has investigated effects of variation of different system parameters in the characteristics of the Integrated Dipole Antenna on Si for On-chip Wireless Interconnects and modeling of the entire structure consisting of the transmitting antenna, receiving antenna and the medium, which is Si substrate in this case. A new method of applying excitation has also been proposed to retain the power during transmission through wireless interconnect. The different features and outcomes from this work can be summerized as follows—

- The transmission gain of an integrated dipole antenna on a Si chip used for an on-chip wireless interconnect is drastically reduced in a multi-layer metal interconnect scheme when a second metal layer is placed above the antenna at the usual interlayer metal distance. If we approximate the interconnect metal layers as a solid metal plate, the simulation shows that a very small amount of power propagates when the dipole antenna is excited horizontally parallel to the plane of the Si substrate in the presence of a second metal layer interconnect above the antenna.
- The drastic reduction in transmitted power can be explained using the Friis transmission formula and image theory.
- The transmission co-efficients of dipole antennas increases and gets saturated with the increase in frequency with the variation in the resistivity of the Si substrate, as well as inter antenna distance.
- The modeling of the structure of the wireless interconnect system has been rendered for dipole antenna. Successful separation and modeling of the tranmitting and receiving antenna has been completed with the help of

electromagnetic theory. The transmission line parameters has been determined using circuit theory.

- The best way to preserve high gain of the integrated antenna in such a multi-layer metal process is to design an antenna with excitation vertically through the Si substrate. If the monopole antenna is excited vertically, the excited mode propagates through the Si substrate, and any metal layers on top of the antenna do not hinder the field propagation.

5.2 FUTURE WORK:

Though the research has been done quite successfully, some amelioration can be still be done for the completeness of the discussion of the characteristics and modeling of the wireless interconnect system toward the end, like—

- Derive a successful derivation of equivalent circuit of monopole antenna.
- The effect of change in resistivity of Si substrate and inter antenna distance can be simulated and theoretically explained in case of monopole antenna.
- The effect of changing the thickness of the Si substrate can be investigated and theoretical explanation can be developed for the clarification in case.
- The effect of inter antenna distance, resistivity and thickness of the Si substrate in presence of the upper metal layer and explain these effects theoretically.

Favorable outcomes from the investigation of the above topics may lead toward the end of the full elucidation of Wireless Inter connect system using Integrated Antenna on Chip for future utilization.

REFERENCE:

1. http://lsiwww.epfl.ch/LSI2001/teaching/webcourse/ch01/ch01.html#1.1
2. Takayasu Sakurai, "Past, present and future VLSIs in the year 2010 and beyond-from a designer's point of view", JSAP Interational Nn. 3 (January 2001).
3. The National Technology Roadmap for Semiconductors, 1997 Edition, Semiconductor Industry Association, San Jose, CA, November 1997. http://notes.sematech.orgi97pelec.htm.
4. A.K. Goel and N.R. Eady, "Characterization of "Multipath Interconnects for Microelectronic and Nanotechnology Circuits", Nanotech 2002 Vol. 1, pp.632-635.
5. H. B. Bakoglu, Circuits, Interconnections, and Packaging for VLSI, Addison-Wesley, 1990.
6. International Technology Roadmap for Semiconductors (ITRS), 2001.
7. W. J. Dally, "Interconnect-limited VLSI architecture," in Proc. IEEE Int. Conf. Interconnect Technology, 1999, pp. 15–17.
8. M. T. Bohr, "Interconnect scaling—the real limiter to high performance ULSI," in IEDM Tech. Dig., 1995, pp. 241–244.
9. J. D. Meindl, "Beyond moore's law: The interconnect era," Comput. Sci. Eng., pp. 20–24, 2003.
10. R. H. J. M. Otten and R. K. Brayton, "Planning for performance," in Proc. Design Automation Conf., 1998, pp. 122–127.
11. K. Banerjee and A. Mehrotra, "Inductance aware interconnect scaling," in Proc. Int. Symp. Quality Electronic Design, 2002, pp. 43–47.
12. C.K. Cheng, J. Lillis, S. Lin, and N. Chang, Interconnect Analysis and Synthesis. New York: Wiley, 1999.
13. M. T. Bohr and Y. A. El-Mansy: IEEE Trans. Electron Devices 45(1998) 620.
14. S.P. Jeng, M.C. Chang, and R.H. Havemann, "Process integration and manufacturing issues for high performance interconnect," in MRS Symp. Proc. Adv. Metallization for Devices and Circuits, 1994, pp. 25-31.
15. A. K. Goel, "Nanotechnology Circuit Design: The Interconnect Problem," *Proc. IEEE NANO-2001*, Maui, Hawaii, October 27-30, 2001, pp. 123-127.
16. S. P. Murarka, *Proc. Int. Conf. Adv. Microelectronic Devices and Processing*, pp. 321 (1994).
17. A. K. Sinha, J. A. Cooper, H. J. Levinstein, "Speed limitations due to interconnect time constants in VLSI integrated circuits", *Electron, Dev. Lett.*, vol. 3, 90 (1982).
18. B. Zhao et al., "A Cu/low-k dual damascene interconnect for high performance and low cost integrated circuits," in Symp. VLSI Technology, Tech. Dig., 1998, pp. 28–29.
19. B. A. Floyd, "A CMOS Wireless Interconnect System for Multigigahertz clock distribution," Ph.D. Dissertation, University of Florida, Gainesville, FL, 2001.
20. J. M. Rabaey, Digital Integrated Circuits: a Design Perspective, New Jersy: Prentice Hall, 1996.

21. K. Banerjee; S.J. Souri; P. Kapur; and Krishna, C. S., "3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration", *Proc. IEEE*, Vol. 89, 602, 2001.
22. D.A.B. Miller, "Rationale and challenges for optical interconnects to electronic chips," *Proc. IEEE*, Vol. 88, No. 6, June 2000.
23. M.F. Chang et al., RF/wireless interconnect for inter- and intra-chip communications, *Proc. IEEE*, 89(4), 456, 2001.
24. S. J. Souri, K. Banerjee, A. Mehrotra, and K. C. Saraswat, "Multiple Si layer ICs: Motivation, performance analysis, and design implications," *Proc. 37th ACM Design Automation Conf.*, 2000, pp. 873–880.
25. R.H. Havemann; J.A. Hutchby, "High-performance interconnects: an integration overview", Proceedings of the IEEE Volume 89, Issue 5, May 2001, pp.586-601.
26. K.K. O; K. Kim; B. Floyd; J. Mehta; H. Yoon; C.M. Hung; D. Bravo; T. Dickson; X. Guo; R. Li; N. Trichy; J. Caserta; W. Bomstad; J. Branch; D.J. Yang; J. Bohorquez; L. Gao; A. Sugavanam; J. J. Lin; J. Chen; F. Martin; J. Brewer, "Wireless communications using integrated antennas," Interconnect Technology Conference, 2003. Proceedings of the IEEE 2003 International 2-4 June 2003, pp.111-113
27. A. B. M. H. Rashid, Nasrin Sultana, M. Rezwan Khan and T. Kikkawa, "Efficient Design of Integrated Antennas on Si for On-Chip Wireless Interconnects in Multi-Layer Metal Process", Japanese Journal of Applied Physics, Vol. 44, No. 4B, pp. 2756–2760, 2005.
28. David M. Pozar, Microwave Engineering, John Wiley & Sons, 2001, 2nd Edition.
29. Simon Ramo, John R. Whinnery, Theodore Van Duzer, Fields and Waves in Communication Electronics, John Wiley & Sons, 1997, 3rd Edition.
30. F. Svelto, S. Deantoni, G. Montagna and R. Castello: IEEE Trans. Very Large Scale Integr. Syst. 9 (2001) 100.
31. A.B.M.H. Rashid, Md. Ariful Hoque, Nayan Abdullah, Md. Zahidul Islam, Nasrin Sultana and M. Rezwan Khan, "Integrated antenna on Si for on chip wireless interconnect using UWB transmission", 3rd International Conference on Electrical & Computer Engineering ICECE 2004, 28-30 December 2004, Dhaka, Bangladesh. pp. 80-83.