INVESTIGATION INTO THE PERFORMANCE AND TESTABILITY OF BiCMOS LOGIC CIRCUITS

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Abstract

CMOS logic is now being extensively used for VLSI circuits because of its extremely low static power dissipation, high noise immunity and high packing density. However, standard CMOS circuits are still slower than its bipolar counterpart. BiCMOS logic circuits have been introduced to increase the output drive capability and speed of CMOS circuits. In order to justify the additional complexity of fabricating both MOS and bipolar devices in BiCMOS logic circuits, it is necessary to ascertain their relative advantages and disadvantages compared to standard CMOS. This thesis examines the performance and testability of two classes of BiCMOS circuits, namely, basic BiCMOS and full-swing BiCMOS circuits. Although some work has been carried out on basic BiCMOS circuits, to the best of our knowledge none has been reported so far on full-swing BiCMOS circuits.

Investigation is carried out on the speed, static power dissipation and noise immunity of the BiCMOS circuits. The results indicate that the two types of BiCMOS circuits are much faster than standard CMOS. The noise immunity of basic BiCMOS circuits is lower than standard CMOS while that of full-swing BiCMOS circuits is the same as that of standard CMOS. The static power dissipation of both classes of BiCMOS circuits are higher than that of standard CMOS.

Some new interesting results have been obtained from the investigations on the behavior of BiCMOS circuits under various single faults. Unlike standard CMOS circuits, the stuck open faults in the pull-down bipolar drivers of the full-swing BiCMOS circuits have been found to be undetectable. The behavior of both types of BiCMOS circuits under other stuck open faults are the same as that of standard CMOS circuits. All stuck on faults in both classes of BiCMOS circuits can be detected by current monitoring. The order of increment in power supply current when these faults are sensitized is almost the same as that in standard CMOS circuits. The results presented in this thesis would provide useful guidelines for designing testable BiCMOS logic circuits.

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List of Abbreviations and Symbols

cq_1: Collector of bipolar transistor q_1 open (transistor q_1 stuck-open fault)

DCVS: Differential Cascode Voltage Switch (logic)

DSL: Differential Split-Level (logic)

dsm_4: Drain and Source of MOSFET m_4 shorted (MOSFET m_4 stuck- on fault)

V_{BE}: Base-Emitter junction voltage of a bipolar transistor

$V_{BE.ON}$: Base-Emitter voltage when a (bipolar) transistor is turned ON

$V_{CE.ON}$: Collector-Emitter voltage when a (bipolar) transistor is turned ON

V_{DD}: Power supply voltage

V_{REF}: Reference voltage

V_{tpo}: Zero bias threshold voltage of p-transistor

τ_{df}: Propagation delay through a gate when output falls

τ_{dr}: Propagation delay through a gate when output rises

V_{TN}: Threshold voltage of n transistor

Chapter 1

Introduction

1.1 Aims:

Recently CMOS is considered the mainstream technology for VLSI applications because of its low static power dissipation and high packing density [1]. But it demonstrates lower speed than other technologies such as Silicon Bipolar technology or Gallium-Arsenide technology [2]. The demand for superior performance, which has motivated the relentless search and development of new technologies, eventually lead the way towards the emergence of BiCMOS technology. It is the technology which merges old rivals, namely, CMOS and bipolar to complement each other, so that the strength of one covers the weakness of other. Today BiCMOS technology is one of the leading candidate technologies for future generations of high speed VLSI circuits. However the cost of BiCMOS processes, due to added complexity of merging CMOS and bipolar devices together, prevents this technology from being widely used in place of existing CMOS

together, prevents this technology from being widely used in place of existing CMOS processes. Moreover the complex failure modes of various BiCMOS circuits speaks against it. Thus it is of great importance to study the effect of physical failures on BiCMOS logic circuits and the effect of these failures on the testing techniques currently employed for MOS and bipolar technologies. The objective of this research is to observe the behavior of different BiCMOS circuits under various faults. The impact of each possible single defect on the behavior of the circuits is analyzed by simulation. The research provides the results of a simulation based fault characterization study of BiCMOS logic circuits. Based on these results this research also aims at a comparative study of BiCMOS circuits with conventional CMOS logic circuits subjected to same faults, with a view to determine the suitability of these circuits for VLSI design. The performance of BiCMOS logic circuits in terms of speed, static power dissipation and propagation delay are also compared with the conventional CMOS logic circuits.

1.2 Literature Review:

The main advantages of BiCMOS technology over CMOS technology are its high current driving capability and high speed [3],[4]. There are two main BiCMOS logic families. The first one is the conventional (Pull-up/Pull-down) family which uses a CMOS structure to implement the logic, followed by a bipolar output stage for high driving capability [4]. The second family uses a differential-mode logic whose operation is based on switching a fixed bias current between two branches [5], [6]. Introduction of bipolar drivers at the output stages of conventional CMOS logic gates significantly increases the gates' speed [3], [4]. However, to overcome the long turn-off time of bipolar transistors

bleeding elements are added to speed the discharging of base charge [4], [7]. But conventional BiCMOS logic gates do not exhibit full logic swing. As a result they loose the performance leverage over CMOS circuits in the reduced voltage environment [8]. The emergence of emitter follower driver configuration with full swing techniques overcomes this problem. Full swing is achieved by shunting base and emitter of the complementary emitter follower driver with MOS diodes [4], [9], [10]. BiCMOS logic family using differential mode logic operates at high a speed in reduced supply voltage environment. High transconductance of bipolar devices is used in the evolution of BiCMOS DCVSL gates. It consists of a bipolar differential pair combined with the existing differential n-channel MOSFET logic tree of CMOS DCVSL technique [5]. Merged CMOS/Bipolar current switch logic is another structure of differential BiCMOS logic family which have several potential application in high speed VLSI circuits to shorten delay times through critical paths of complex circuits [6].

Most of the work reported in the literature to-date on the testability of BiCMOS circuits has concentrated on fault characterization of the conventional family [11]-[15]. Different testing methods are also presented on the conventional BiCMOS gates [5], [6], [11], [16]. A design for testability (DFT) technique for detecting short and bridging fault in CMOS/BiCMOS logic circuits has been presented in [17]. The DFT technique applies for detecting the defects which causes an excessive increase in power supply current (I_{DDQ} fault). It has been claimed that about 67% of all possible shorts and bridging faults are detectable with this technique. However conventional BiCMOS circuits under stuck-open fault demand further investigation. A few work has also been done on the fault characterization and testing methods of differential BiCMOS logic circuits [12], [16], [18].

The topic of studying the effect of physical failures on basic BiCMOS circuits and the effect of these failures on the testing techniques currently employed for MOS and bipolar technologies is also attended in [11]. But the behavior of full swing BiCMOS circuits under various physical failures is the least attended topic.

1.3 Organization of the thesis:

Chapter two introduces the various BiCMOS logic families. Also a brief introduction to CMOS logic circuits are presented in that chapter. In chapter three the performance of various BiCMOS circuits are investigated and compared to that of standard CMOS circuits. A detailed investigation into the behavior of various BiCMOS circuits under different single faults is carried out in chapter four. The results presented in this chapter are then compared with those of standard CMOS to asses their testability. Chapter five concludes this thesis with some recommendations for future work.

Chapter 2

CMOS/BiCMOS Logic Families and Faults

2.1 Introduction :

This chapter introduces various CMOS/BiCMOS logic circuits. The principles of operation of conventional static CMOS, Differential CMOS, conventional BiCMOS and full swing BiCMOS circuits are described in detail. The chapter also focuses on the various faults that occur in integrated circuits and the fault models used to analyze the behavior of the faulty circuits.

2.2 Various CMOS Circuit Techniques :

Recently CMOS has been accepted as the most widely used technology in VLSI applications. In this section conventional static CMOS and two different types of differential CMOS circuits: Differential Cascode Voltage Switch (DCVS) logic and Differential Split Level (DSL) CMOS logic are described.

2.2.1 Conventional Static CMOS :

The structure of a conventional static CMOS logic gate consists of a driver network comprising only nMOS transistors and a load network comprising only pMOS transistors, where all MOSFETs are of enhancement mode [1]. The load network is connected between power supply V_{DD} and the output node. The driver network is connected between the output node and ground. The load and driver networks are never ON simultaneously rather they operate in antiphase. As a result, the output logic levels are independent of the sizes of load and driver networks. This is why CMOS circuits are referred to as "ratioless" circuits. When no input changes, then ideally there should be no current through the load and driver network.

Fig. 2.1 depicts the circuit diagram of a conventional CMOS NAND gate. It consists of enhancement mode nMOS transistors n_1 and n_2 as the driver network and enhancement pMOS transistors p_1 and p_2 as the load network. When both the inputs are raised to logic high level of 5 volts (which is much greater than the threshold voltage [1] of nMOS transistors), both nMOS transistors conduct and output node V_{OUT} is pulled down to ground (logic 0). For any other input vector either one or both the transistors in the load network conduct and output is pulled up to V_{DD} (logic 1). With such inputs no conducting path exists between V_{OUT} and ground due to OFF state of one or both the pMOS transistors [1].

2.2.2 Differential Cascode Voltage Switch (DCVS) Logic :

Differential CMOS logic was introduced for speed improvement in CMOS logic circuits while maintaining the low quiescent power characteristics of CMOS circuitry [19],

[20]. Fig. 2.2 shows the basic logic gate using DCVS logic. In larger gates, the transistors m_3 and m_4 represent complimentary nMOS combinational logic trees for intended functions. Depending on the differential inputs D and $\bar{D}$, either the node Y or the node $\bar{Y}$ is pulled down. Regenerative action sets the cross-coupled pMOS latch to static outputs Y and $\bar{Y}$ having full differential high and ground logic levels. The logic trees do not draw direct current from the power supply after the circuit latches. Since the inputs drive only the nMOS devices, input gate capacitance loading is typically three times smaller than fully complementary CMOS circuits that require complementary nMOS and pMOS transistors to be driven[19]. Performance of the circuit is limited by the set time of the pMOS latch [19]. However "Clocked DCVS logic" overcomes the problems of long output settling time of pMOS latch of static DCVS logic [19].

2.2.3 Differential Split-Level CMOS Logic :

The load and tree arrangement of DSL CMOS logic circuit is shown in Fig. 2.3. Here the load circuit consists of cross coupled current controlled cascode n and p transistors. This load is similar to that of DCVS circuit in Fig. 2.2. except two extra nMOS transistors m_5 and m_6 driven by a reference voltage V_{REF} have been introduced in the load. Let V_{REF} is set to $(V_{DD}/2 + V_{TN})$. If D is high (5v) and $\bar{D}$ is low (0v), then m_3 is ON and m_4 is OFF. Then node $\bar{A}$ has logic low level and node A has logic high level of V_{DD}. Node $\bar{Y}$ is also pulled down to logic 0 through m_3. This turns m_2 hard ON. The reference voltage determines the logic high level at node Y to be $V_{DD}/2$. For V_{DD} = 5v and V_{TN} = 1v, the voltage at Y is approximately 2.5 volts. Therefore, m_1 is moderately conducting. This

causes a large leakage current and a voltage drop between nodes $\bar{Y}$ and ground. The magnitude of this drop depends upon the number of n-transistors in series in the pull down path as well as their aspect ratios (W/L) [23]. If the inputs D and $\bar{D}$ are now switched then m_3 turns ON and m_4 turns ON. The half V_{DD} level at Y discharges immediately and m_1 turns more ON to its high drive state. At the same time node $\bar{A}$ and $\bar{Y}$ start rising because m_1 was already partly ON, causing m_2 to switch faster to its low drive state than in the DCVS gate of Fig. 2.2. Because of the reduced voltage swing at the nodes $\bar{Y}$ and Y, the delay due to wiring capacitance can be reduced by using them as the I/O nodes. The speed of operation of DSL circuit is maximum when the reference voltage is close to ($V_{DD}/2$ + V_{TN}) [23]. If V_{REF} is increased further, the logic high level at Y (when D=5v and $\bar{D}$ =0v) increases. As a result m_1 becomes less conducting, reducing the amount of leakage current which in turn reduces the voltage drop between $\bar{Y}$ and ground. The leakage current at $V_{REF}=V_{DD}$ is negligible. However, as V_{REF} is increased from the optimum value, the speed of operation reduces.

2.3 BiCMOS Logic Circuits :

CMOS and bipolar technologies have their weak and strong points. CMOS has qualified to be the most appropriate choice for VLSI applications because of its low DC power dissipation and its high packing density, yet its speed is limited by the capacitive loading. On the other hand , bipolar digital circuits outperforms CMOS in terms of speed, but are power consuming. Thus a performance gap exists between CMOS and bipolar and neither of them have the flexibility required to cover the gap. This can only be achieved by

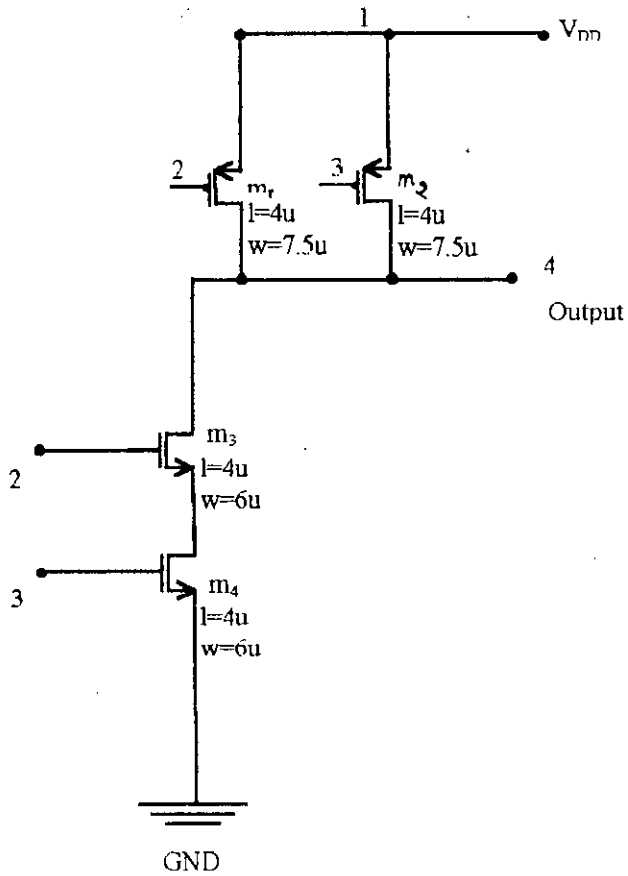

Fig: 2.1 CMOS NAND gate

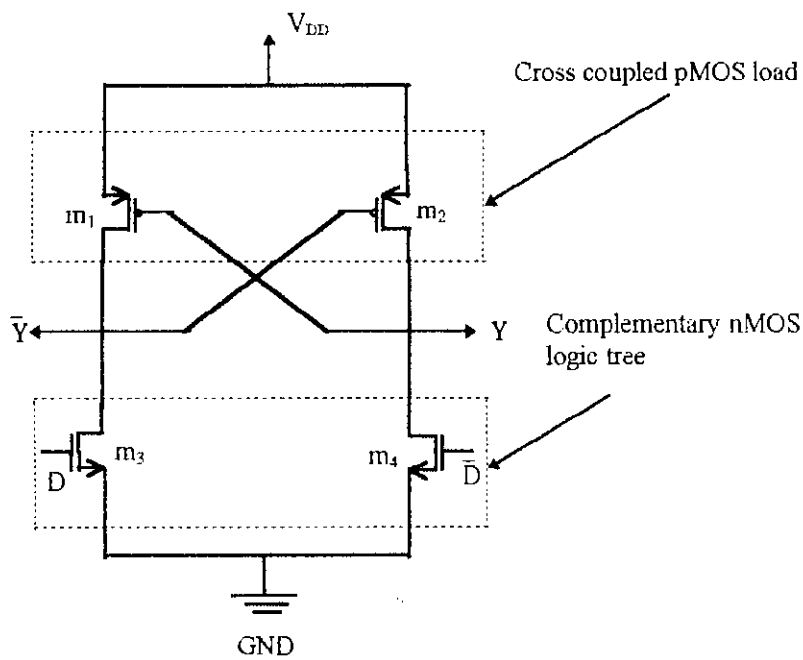

Fig: 2.2 Basic logic gate in DCVS logic

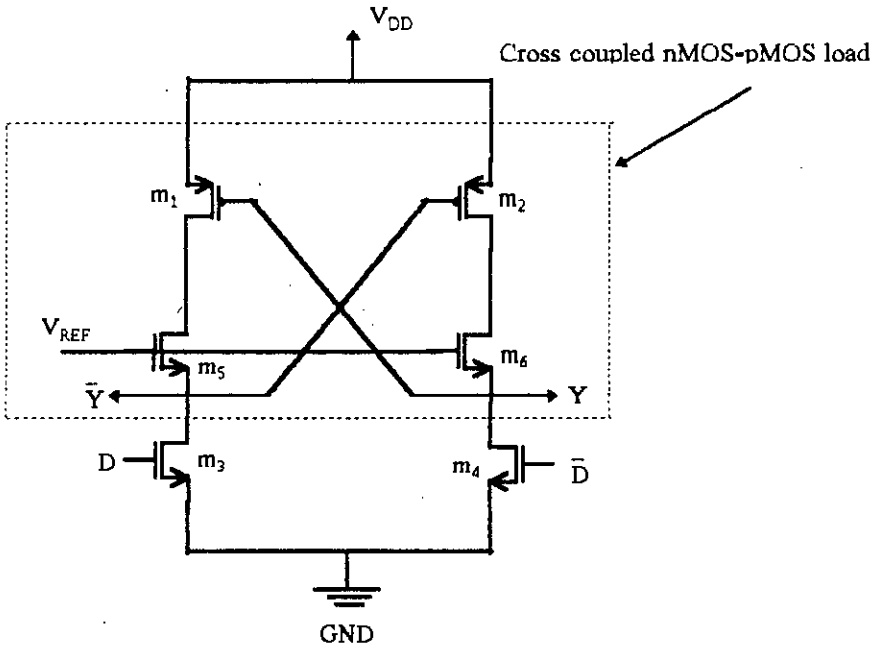

Fig: 2.3 DSL CMOS logic principle

a technology such as BiCMOS. Introducing bipolar drivers at the output stage of CMOS gate, significantly increases the gate's driving capability and hence its speed [3]. The objective of the synergy of bipolar and CMOS is to exploit the advantages of both at the circuit and system levels. In this section various BiCMOS circuits are introduced. The principles of operation of conventional BiCMOS logic gate as well as different full-swing BiCMOS gates are described.

2.3.1 Conventional BiCMOS Logic :

Fig. 2.4(b) shows the early version of a BiCMOS inverter deduced from a basic CMOS inverter of Fig.2.4(a). Here the transconductance of both the p and n transistors of Fig. 2.4(a) are increased by adding a bipolar transistor at the output stage of each MOS device. The operation of BiCMOS inverter is similar to CMOS inverter. When the input is low (0v), pMOS is ON and its drain current turns the transistor Q_1 ON. The collector current of Q_1 charges the output load capacitance. As the output reaches $V_{DD} - V_{BEon}$, Q_1 gradually turns OFF. The HIGH DC level output is hence $V_{DD} - V_{BEon}$. If the input is high, transistor N is turned ON causing Q_2 to turn ON to discharge the output node. As the output voltage reaches V_{BEon}, transistor Q_2 turns OFF and the DC LOW level stays at V_{BEon}. The speed of this circuit is limited because of the long turn OFF time of the bipolar transistors. Therefore bleeding elements are added to speed the discharging of the base charge when the BJTs are turning OFF [4]. Fig. 2.5 shows a conventional BiCMOS inverter with N_{d1} and N_{d2} as the bleeder. The path between base of the bipolar and ground is created only when the bipolar transistor is to be turned OFF. Fig. 2.6 shows a basic

BiCMOS NAND gate. Transistors m_1, m_2, m_3 and m_4 implements the logic. m_7 is ON during the pull-up stage and bleeds the base charge of Q_2.

2.3.2 Full Swing BiCMOS Logic:

Recently, comparison of generic BiCMOS drivers have shown that the emitter follower driver configuration with full-swing techniques may extend the leverage of BiCMOS for scaled technologies [8]. Various full-swing BiCMOS logic circuits with the complementary emitter-follower driver configuration have been fabricated in a fully complementary BiCMOS technology [9], [10].

2.3.2.1 Full-swing BiCMOS Logic using clamping diode :

Fig. 2.7 shows the basic full-swing complementary MOS/bipolar logic circuit realizing a two-input NAND function [10]. Logic is implemented in the CMOS stage (mn_1, mn_2, mp_1 and mp_2) and output is driven by the push pull complementary emitter follower (qn_1 and qp_1). Two base nodes (4 and 7) of the emitter follower are clamped to ensure that qn_1 and qp_1 are never turned ON simultaneously but biased near the edge of turn off in steady states. The clamping device is a CMOS diode which is a parallel pair of nMOS diode mn_4 and pMOS diode mp_4. Full swing is achieved by the CMOS positive feedback network that shunts the base and emitter of qn_1 and qp_1 in a controlled manner. Gate terminals of the shunting devices (mp_3 and mn_3) are driven by the CMOS inverter (mn_5, mp_5 pair)that inverts the output signal and delays turn-on of mp_3 (or mn_3) during pull-up (or pull-down) until the output changes its logical state.

Initially when both the inputs are high (5v), node 7 is fully discharged to ground and, if mn_3 were OFF, output node 5 would stay at $V_{BEp,on}$ which is the turn-on voltage of qp_1. This low voltage is inverted by the output inverter and node 6 becomes high. This turns mn_3 fully ON, shorting output to GND and turning qp_1 OFF. In this state qp_1 is clamped off because mn_4 holds node 4 at V_{tno}, which is the zero bias threshold voltage of mn_4 assumed to be smaller than $V_{BEn,on}$ of qn_1. mp_4 is OFF due to the body effect and mp_3 is OFF. When input A falls to zero, mp_2 turns ON and its drain current charges up node 4 as well as node 7 through mn_4. Because mp_3 remains OFF until the output crosses inverter logic threshold voltage, most of the current flows into the base of qn_1, turning it ON. The output is then pulled up by a large emitter current of qn_1. Since mn_3 is ON and mn_4 clamps the voltage between base nodes 4 and 7, qp_1 is held OFF and there is no crossover current through qp_1.

When output (node 5) rises above the logic threshold voltage, voltage at node 6 falls falls to GND and mn_3 will be OFF immediately. At this point, since V_4 ($=V_5 + V_{BEn,on}$) will be greater than $|V_{tp}|$, mp_3 turns ON bypassing a fraction of the qn_1 base current to the output. Although this causes the final output transient to be slower, because the output has already changed its logical state, the circuit speed will not be degraded. Finally when $V_4=V_7$ the threshold voltages of mp_3 and mp_4 return to V_{tpo}. Then mp_3 strongly discharges the base-emitter junction of qn_1, pulling up the output to V_{DD} and turning qn_1 OFF. The diode mp_4 clamps V_7 at $V_{DD} - |V_{tpo}|$ preventing qp_1 from turning ON. If the input A is changed back to logic high, the circuit operates in a complementary way. Because the output level of this circuit reaches the full supply rails after the feedback inverter changes its logical state minimum operation voltage of this circuit is the larger of $V_{BEn,on} + V_{LT}$ or

($V_{BEp,on}$ + V_{DD} - V_{LT}) where V_{LT} is the logic threshold voltage of the feedback inverter. For a symmetric case minimum V_{DD} is $2V_{BE,on}$.

Performance of this type of circuit mainly depend on parasitic capacitances at nodes 4 and 7, current voltage characteristics of the clamping diode and details of the full swing circuitry. Reduction of parasitic capacitances (by reducing W/Ls of mn_3 and mp_3) at these prevent excessive base current bypassing and premature cutoff of qn_1 and qp_1 during active periods and essentially improve the speed.

2.3.2.2 Low capacitance variation of Full-swing BiCMOS Logic :

The parasitic capacitances at nodes 4 and 7 of Fig. 2.7 can be reduced by modifying the CMOS diode as in Fig. 2.8. Comparing the two the drain terminals of mn_4 and mp_4 are connected to the output node in this circuit, instead of nodes 4 and 7 respectively. So this circuit has less parasitic at nodes 4 and 7 by as much as the drain junction capacitances of mn_4 and mp_4 [9]. However this CMOS diode operates differently and has a higher clamping voltage because of the body effect. When both inputs are ONE base node 7 and output node 5 are shorted to GND. Thus mp_4 functions as a MOSFET diode biasing node 4 at $|V_{tp}|$ [9]. For qn_1 to be clamped OFF, this bias voltage $|V_{tp}|$ must be smaller than $V_{BEn,on}$. Therefore a zero bias threshold voltage much smaller than the BJT turn-on voltage is required for mp_4. This requirement also applies to mn_4 due to complementary nature if so mn_4 is ON providing an additional shunt path between node 7 and output node 5 because its gate-source bias is larger than its threshold voltage. During pull-up transient, node 7 is clamped by mn_4 operating in source follower mode. Since the voltage between nodes 4 and 7 is close to $V_{BEn,on}$, a small fraction of base current for qn_1

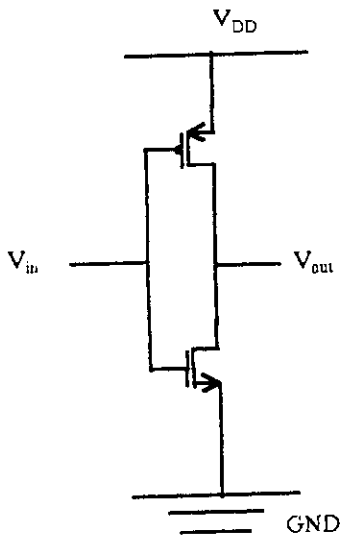

Fig: 2.4 (a) CMOS inverter

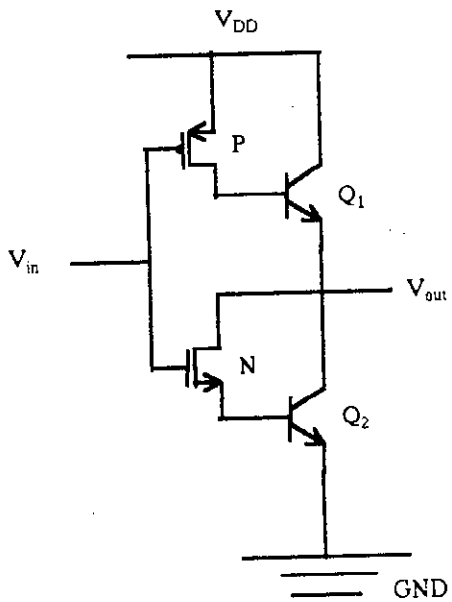

Fig: 2.4 (b) BiCMOS inverter

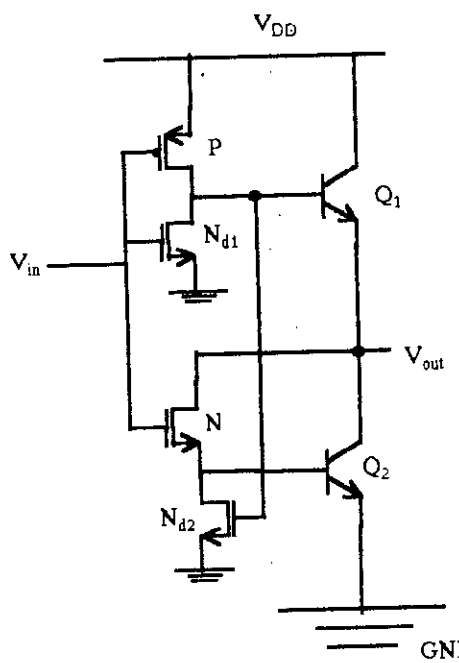

Fig: 2.5 Conventional BiCMOS inverter

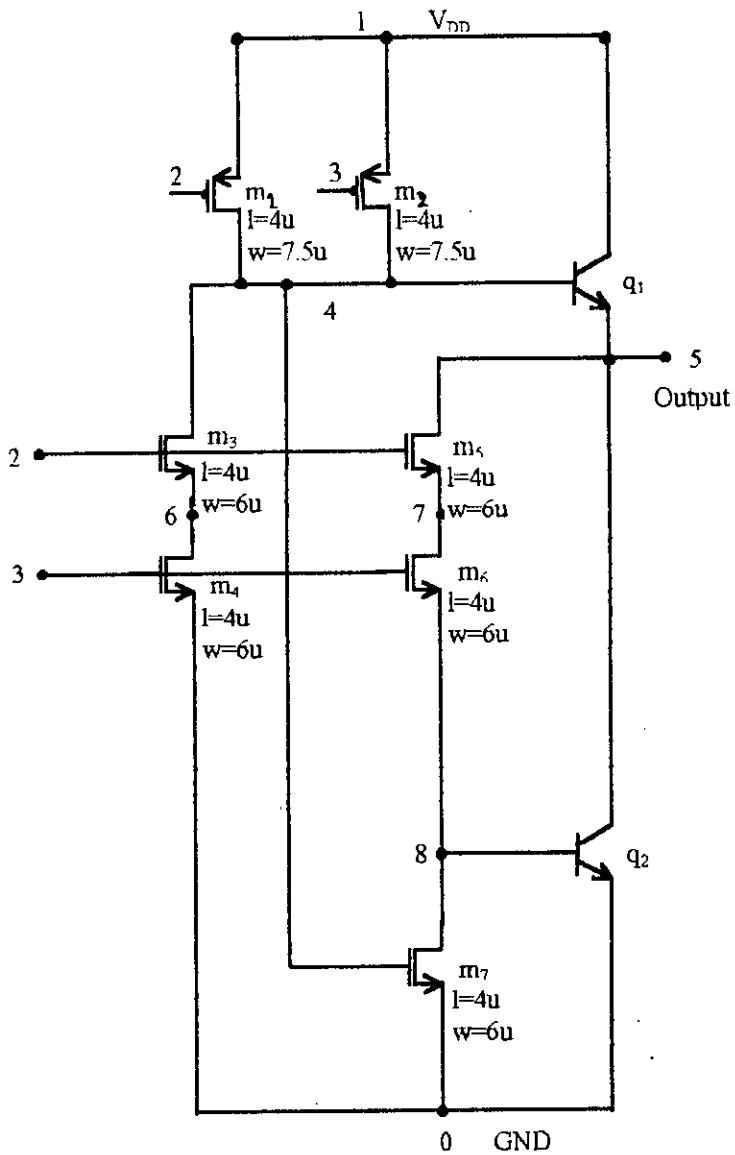

Fig. 2.6 Basic BiCMOS NAND gate

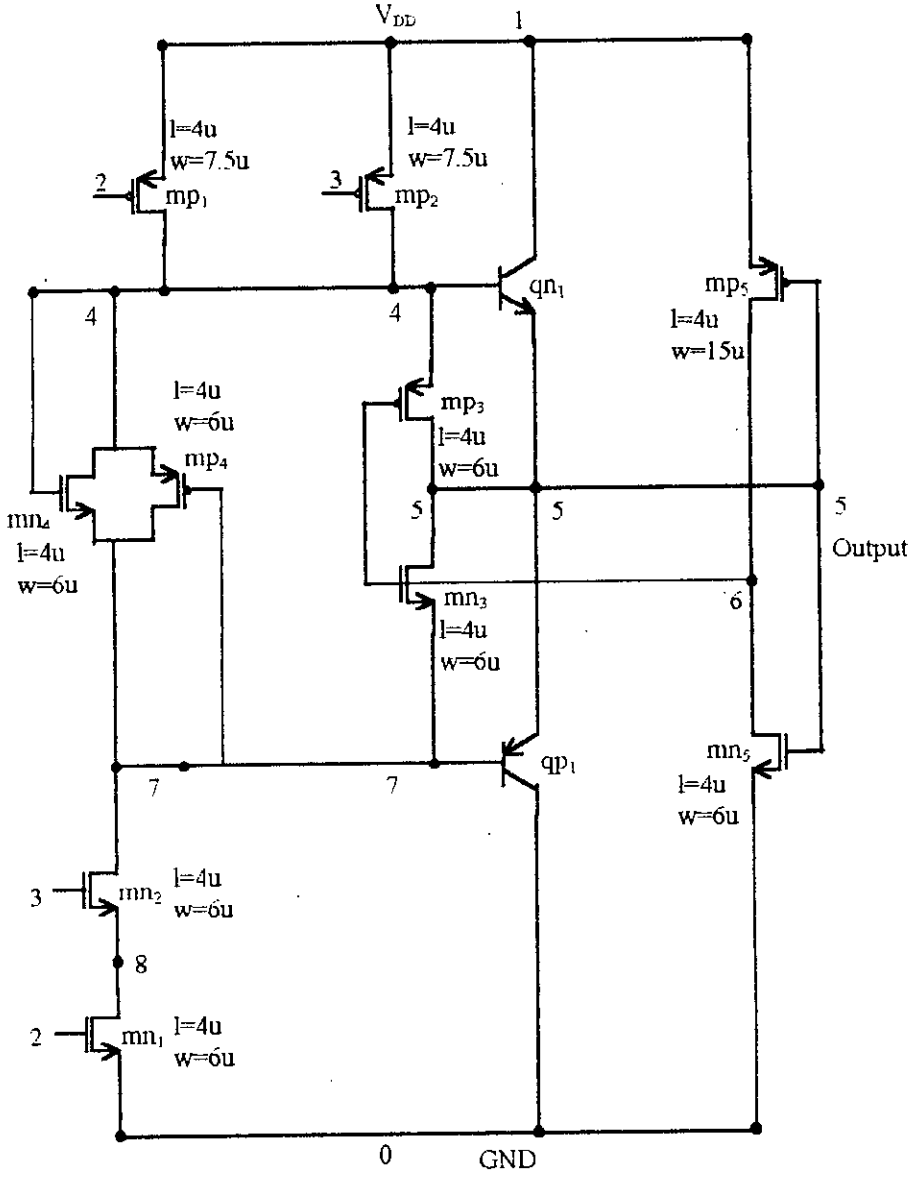

Fig: 2.7 Basic Full-Swing BiCMOS NAND gate

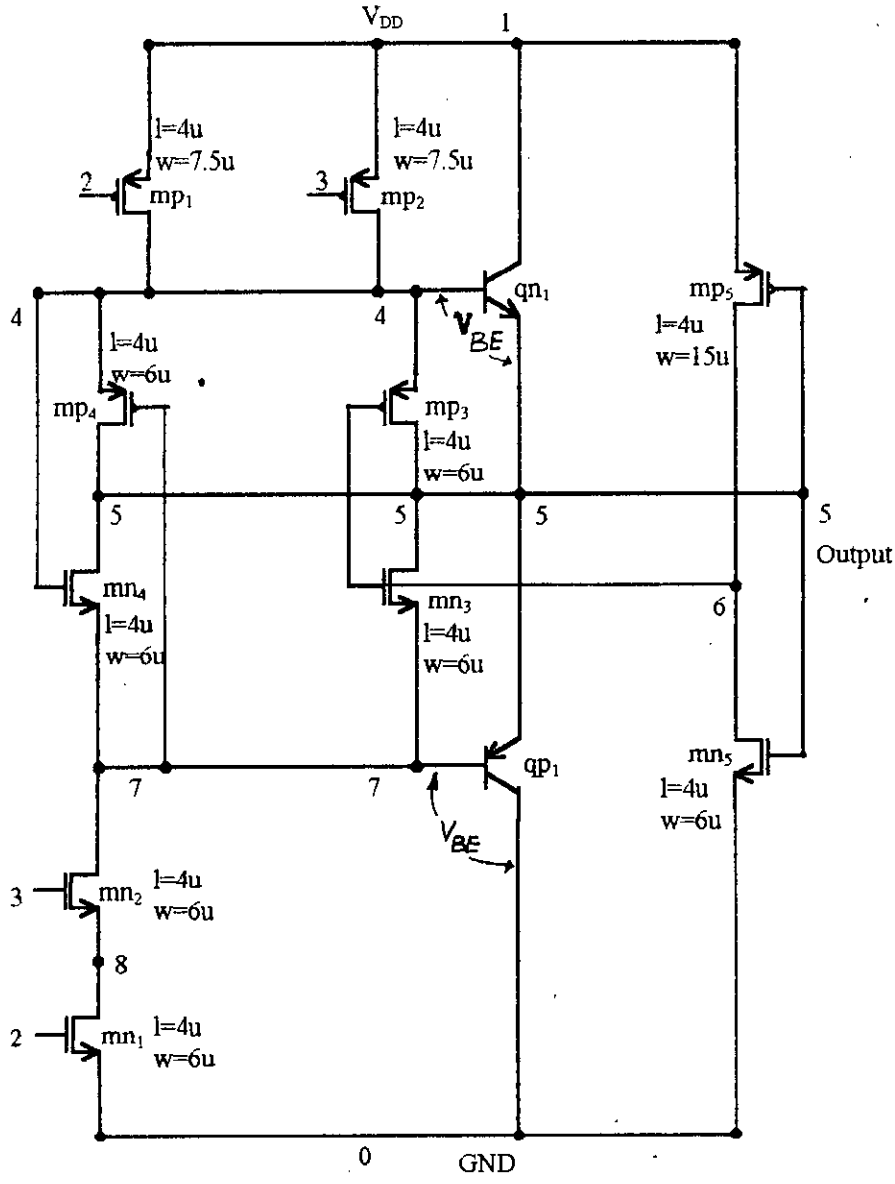

Fig: 2.8 Low-capacitance full-Swing BiCMOS NAND gate

leaks through mp_4 to the output. As the output is pilled up, mn_4 gets weaker but mp_4 becomes stronger because of the body effect. When the output is high, mn_4 clamps node 7 at V_{DD} - V_{tn} and prevents qp_1 from turning ON as long as V_{tn} is smaller than $V_{BEp.on}$ of qp_1. Similarly during pull down , node 4 is clamped by mp_4 operating in a source follower mode [9], [10].

2.4 Physical failures in ICs :

Various physical failures can occur in ICs [11], [22]. Physical defects can occur during the fabrication of an IC or during its use. A defect that causes a change of the logical function of the circuit can be represented by a logical abstraction known as logical fault. Similarly a defect that causes a change in a continuous parameter of the circuit can be represented by an abstraction called a parametric fault.

BiCMOS devices are subjected to most of the defects which occurs in each of the CMOS and bipolar technologies. The most prevalent failures in bipolar technology are [11]: (1) open connections, (2) shorts between connections, (3) "piped" transistors with excessive emitter to collector leakage current. Similarly the defects which can be found in MOS ICs are: (1) shorts (e.g., gate oxide shorts), (2) opens (e.g., intragate breaks), and (3) circuit degradation (e.g., threshold voltage variations).

When a vector is applied to a faulty device which produces an incorrect response, an error is said to have occurred. However, if we try to derive test vectors for every possible physical failure in a VLSI chip, the problem would soon become unmanageable. In order to successfully tackle the problem, physical failures in a chip are represented with the help of a fault model.

2.4.1 Stuck-at Fault Model :

In stuck-at fault model it is assumed that the fault causes a line in the circuit to behave as if it is permanently at logic 0 or logic 1 [22]. If the line is permanently at logic 0 it is said to stuck-at 0, otherwise if the line is permanently at logic 1 it is said to be stuck-at 1.

2.4.2 Stuck-on Fault Model :

If a fault causes a transistor to conduct continuously, the transistor is said to be stuck-on [11], [22]. When a defect causes a bipolar to become permanently ON it is assumed in this model that the bipolar's collector and emitter terminals are shorted through a fault resistance whose value depends upon the fault strength. Similarly, stuck-on fault in MOS devices are modeled by shorting its source and drain nodes through the fault resistance.

2.4.3 Stuck-open Fault Model :

When a transistor is rendered non-conducting by a faulty it is said to be stuck-open. A stuck-open fault may force a combinational CMOS circuit to behave in a sequential fashion. Thus in order to detect a stuck-open fault, a sequence of vectors is required. To model an open fault of a device terminal, a large resistance is inserted between the device terminal and the circuit node to which the terminal would otherwise be connected.

Chapter 3

Performance of BiCMOS Logic Circuits

3.1 Introduction:

BiCMOS as an emerging technology has faced fierce opposition due to the increased cost of adding BJTs to a conventional CMOS process. Nevertheless BiCMOS has been widely accepted due to their high performance and high speed. This chapter aims at a detailed analysis of the performance of BiCMOS circuits. Basic BiCMOS as well as full swing BiCMOS circuits are analyzed. These circuits are simulated to determine the propagation delay, static power dissipation and output logic low and high voltage level. Propagation delays are measured with additional loading. Their performances are then compared with the performance of conventional static CMOS circuits.

3.2 Test Arrangement:

To analyze and compare the performance of various BiCMOS circuits, a cascaded chain of three two-input NAND gates are used as shown in Fig. 3.1. One of the inputs of each NAND

gate is tied internally to a logic high level of 5 volts. The other input is connected to the output of the preceding gate. Additional capacitive load is placed at the output of each gate.

A structured approach is adopted for simulation of the cascaded chain of Fig. 3.1. Description of only one NAND gate of Fig. 3.1 is written using the subcircuit function of SPICE [25]. Then the whole cascaded chain is modeled in a main SPICE program by making three references to the subcircuit. Propagation delay between the input and output of the second stage is measured. Static power dissipation is measured for all the three gates.

3.3 Spice Simulation Results:

As mentioned earlier cascaded chain of Fig. 3.1 has been simulated using three types of NAND gates: (i) Basic BiCMOS, (ii) Full-Swing BICMOS and (iii) Conventional CMOS. The circuit diagrams of these NAND gates are shown in Figures 3.2, 3.3 and 3.4 respectively. Width and length of the MOS devices shown in the figures are used for simulating the circuits. Table 3.1 presents the SPICE simulation results on cascaded chain of NAND gates.

Table 3.1: SPICE simulation results showing output Logic levels and Power dissipation

Circuit	Logic Level (volts)		Static Power Dissipation (nw)
	V_{LOW}	V_{HIGH}	
Conventional CMOS NAND gate	0	5	2.42×10^{-1}
Basic BiCMOS gate	0.263	4.675	$7.18 \times 10^{+4}$
Full swing BiCMOS gate	0	5	$3.51 \times 10^{+1}$

Regarding output logic level, the full swing BiCMOS circuit of Fig. 3.3 achieves the same rail to rail swing as the conventional CMOS circuit of Fig. 3.4. Depending on the inputs, in a

conventional CMOS gate, either the driver or the load network are active and thereby connects output to either ground or V_{DD} respectively. Thus, the circuit achieves full voltage swing (refer to section 2.2.1). As for the full swing BiCMOS gate (Fig. 3.3), after initial pull up through the bipolar qn_1 to (V_{DD} - $V_{BE,on}$), rail to rail swing is achieved by the shunting MOS device mp_3. During pull down, mn_3 operates to achieve logic low level of 0 volt. This phenomenon was described in section 2.3.2.2.

For the basic BiCMOS gate of Fig. 3.2, output achieves partial swing. Bipolar drivers prevents the output from attaining full V_{DD} swing since they remain at the edge of turning ON after the output is pulled up or pulled down to a certain extent. The behavior of this circuit was described in section 2.3.1.

It is found in Table 3.1 that the static power dissipation in basic BiCMOS circuit is approximately 10^5 orders of magnitude higher than that in conventional CMOS circuit. However, the power dissipation in full-swing BiCMOS circuit is about 10^2 order of magnitude higher than conventional CMOS circuits. Thus, full-swing BiCMOS is advantageous compared to basic BiCMOS in terms of static power dissipation.

Table 3.2: SPICE simulation results showing propagation delay

Output Capacitance (pF)	Conventional CMOS gate		Basic BiCMOS gate		Full Swing BiCMOS gate	
	τ_{df} (ns)	τ_{dr} (ns)	τ_{df} (ns)	τ_{dr} (ns)	τ_{df} (ns)	τ_{dr} (ns)
0.1	1.66	1.23	0.35	00.17	1.02	0.26
1	17.05	12.25	0.78	0.33	1.1	0.46
2.5	42.75	30.78	1.33	0.60	1.42	0.37
4	68.18	49.2	1.88	0.90	1.86	0.61
5	85.29	61.03	2.21	1.05	2.14	0.78

Table 3.2 presents the propagation delays of the NAND gates obtained from SPICE simulation on the three types of logic circuits under consideration. The results confirm the advantage of BiCMOS circuits over conventional CMOS circuits with speed as the criterion of comparison. The propagation delays of various gates are plotted as a function of load capacitance in Fig. 3.5. The figure shows that the delays for basic BiCMOS and full-swing BiCMOS gates are very close for various loading conditions. However, when the propagation delays of the BiCMOS gates are plotted on an expanded time scale as in Fig. 3.6, the full-swing BiCMOS is found to be slightly faster than basic BiCMOS at small load. With increased capacitive loading, the delays of two types of BiCMOS gates are found to be almost the same. Delays in BiCMOS circuits are considerably small as compared to the delays in conventional CMOS circuits due to the high current driving capability of bipolar drivers at the output stages of BiCMOS gates. However, as can be seen from Table 3.2, the propagation delay when the output rises (τ_{dr}) is much lower than the delay when the output falls (τ_{df}) for both types of BiCMOS gates. Since the sources of the load network (m_1 and m_2) are connected to the power supply voltage V_{DD}, body effect cannot adversely affect the operation of these transistors. As a result, when input to m_1 or m_2 falls to ($V_{DD} - |V_{tpo}|$) the respective transistor turns fully ON and connects base of q_1 to V_{DD}. The large emitter current of q_1 then charges the output towards high logic level. During the falling transition, body effect adversely affects the turning ON of the n-MOS transistors m_3, m_5 and m_6 since their source nodes are not grounded. Also, m_7 remains ON until node 4 is pulled down below V_{tn} and bypasses a fraction of base current for q_2 from the output. Consequently its emitter current is not as large as the current during pull up transient. This causes output transition from logic high to logic low level slower than the transition from low to high level.

3.4 Comparison:

The SPICE simulation results presented in the last section have been analyzed. A comparison of these results for the various types of circuits leads to the following conclusions:

- BiCMOS circuits are much faster than conventional CMOS circuits at nominal loading conditions. The speed advantage of BiCMOS circuits become more and more prominent with increasing capacitive load.
- The speed of basic and full-swing BiCMOS circuits are very close for various capacitive loads except at small load when the later shows slight speed advantage over the former.
- While conventional CMOS and full-swing BiCMOS circuits have full output logic swing, the basic BiCMOS circuit has a reduced output swing. Thus, basic BiCMOS circuits have a lower noise immunity compared to other two classes of circuits under consideration.
- Power dissipation in BiCMOS circuits are higher than that in conventional CMOS circuits. Full-swing BiCMOS circuits have much lower static power dissipation than basic BiCMOS circuits.

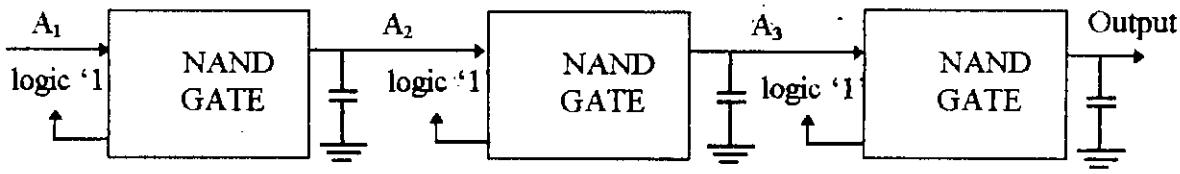

Fig: 3.1 Cascaded chain of three two-input NAND gates

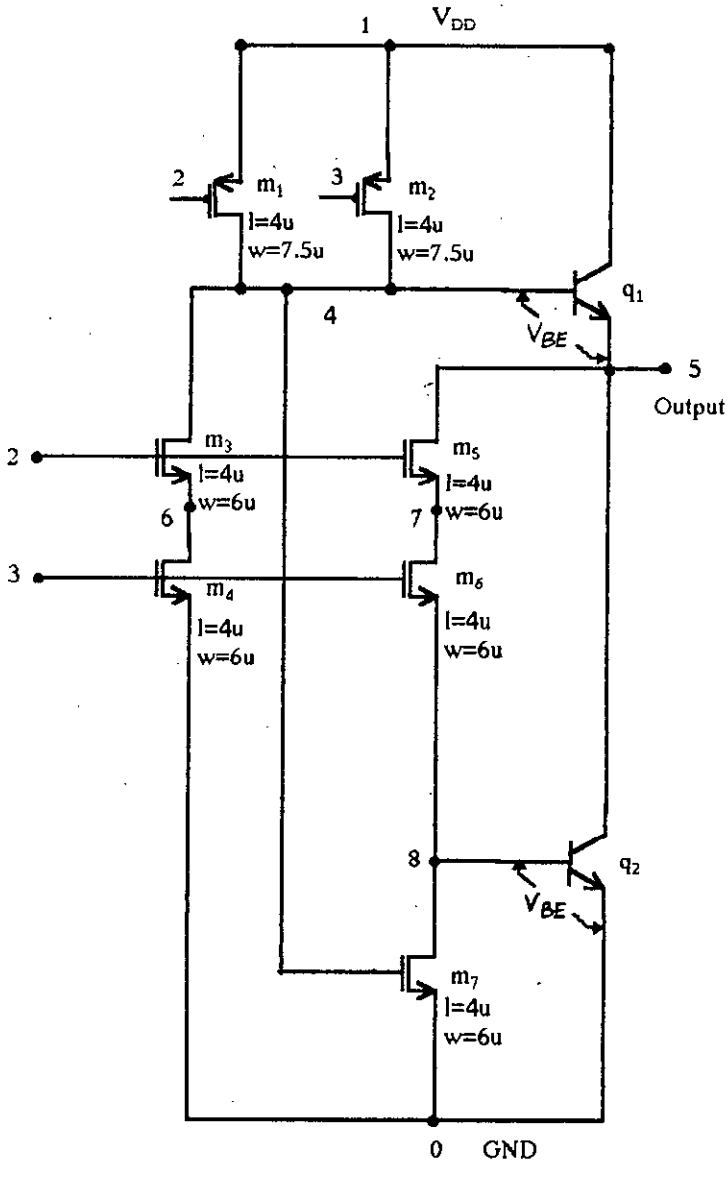

Fig: 3.2 Basic BiCMOS NAND gate

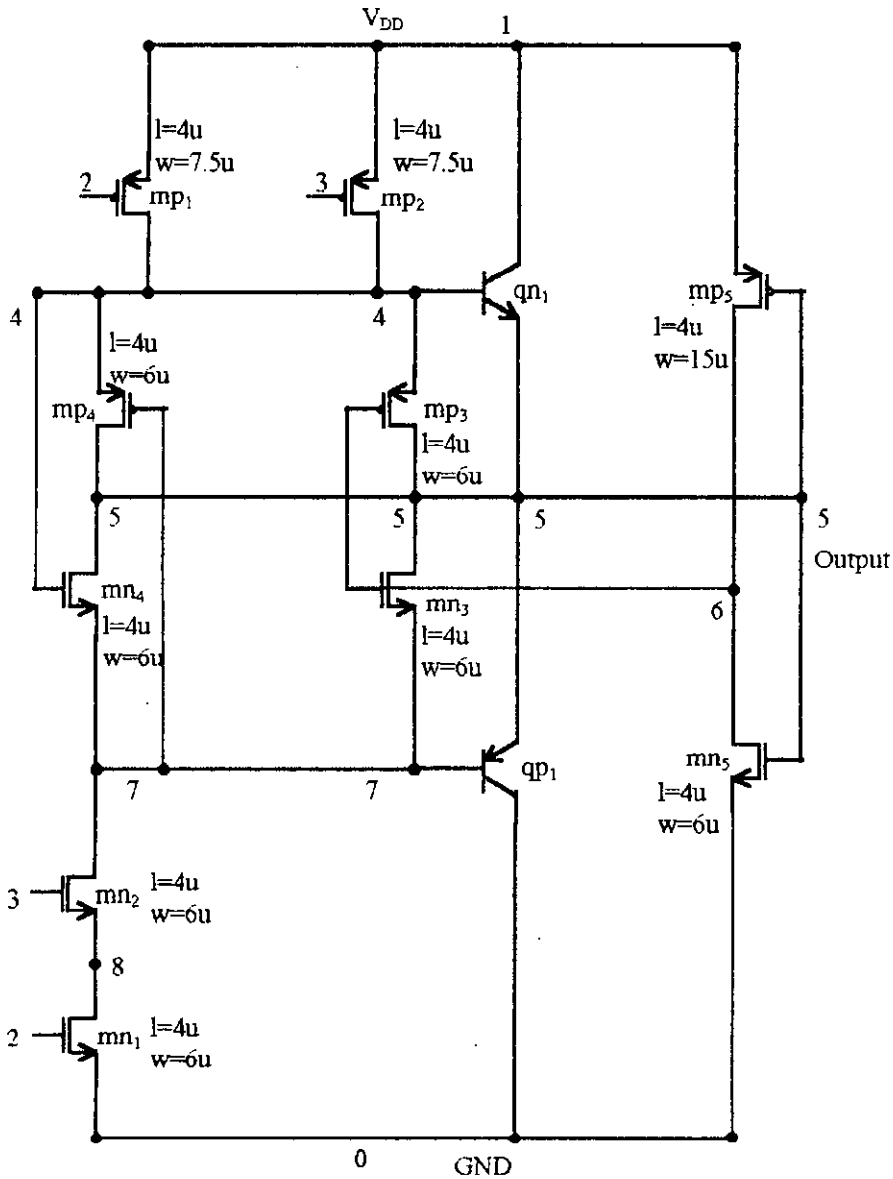

Fig: 3.3 Full-Swing BiCMOS NAND gate

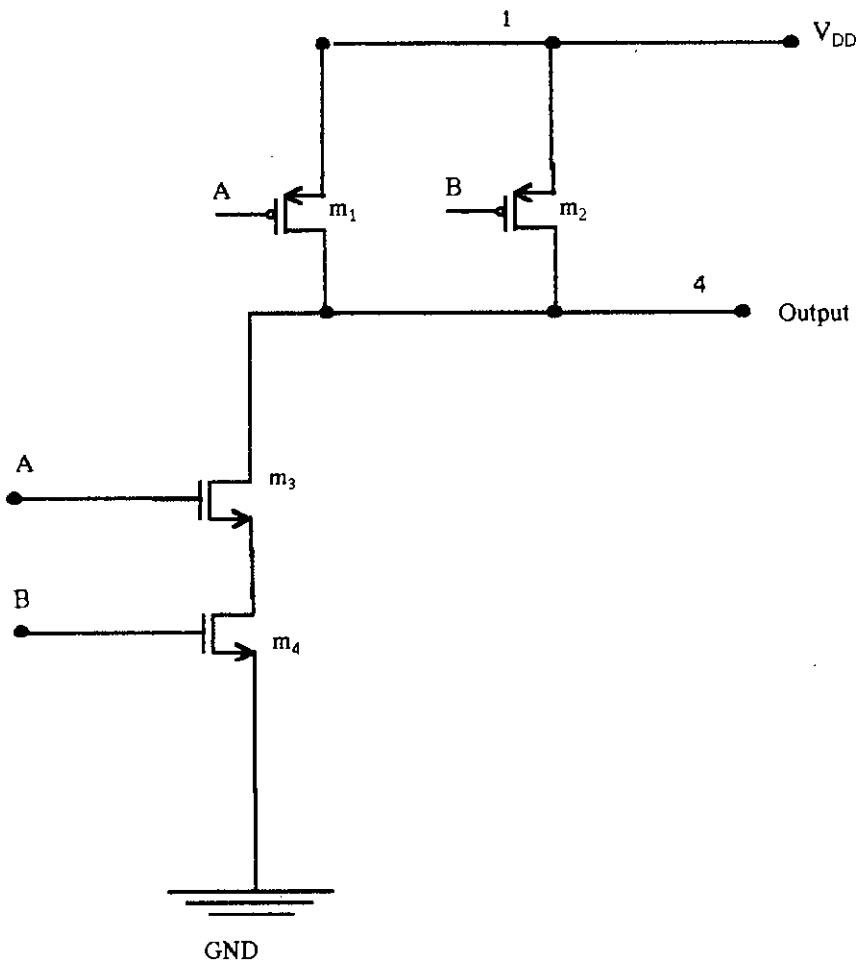

Fig: 3.4 CMOS NAND gate (conventional)

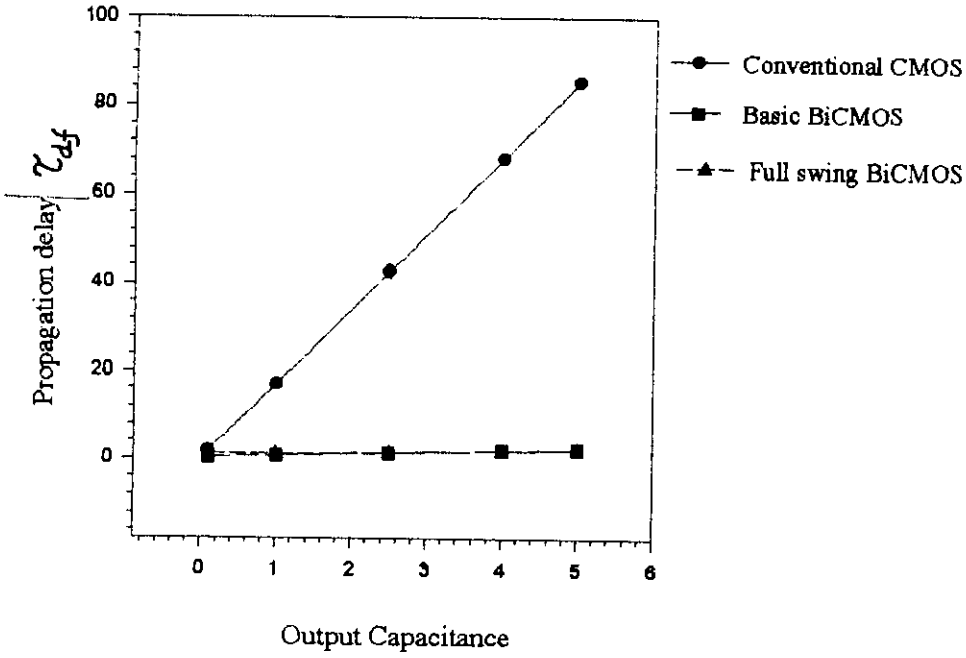

Fig: 3.5 Propagation delay vs. output capacitance

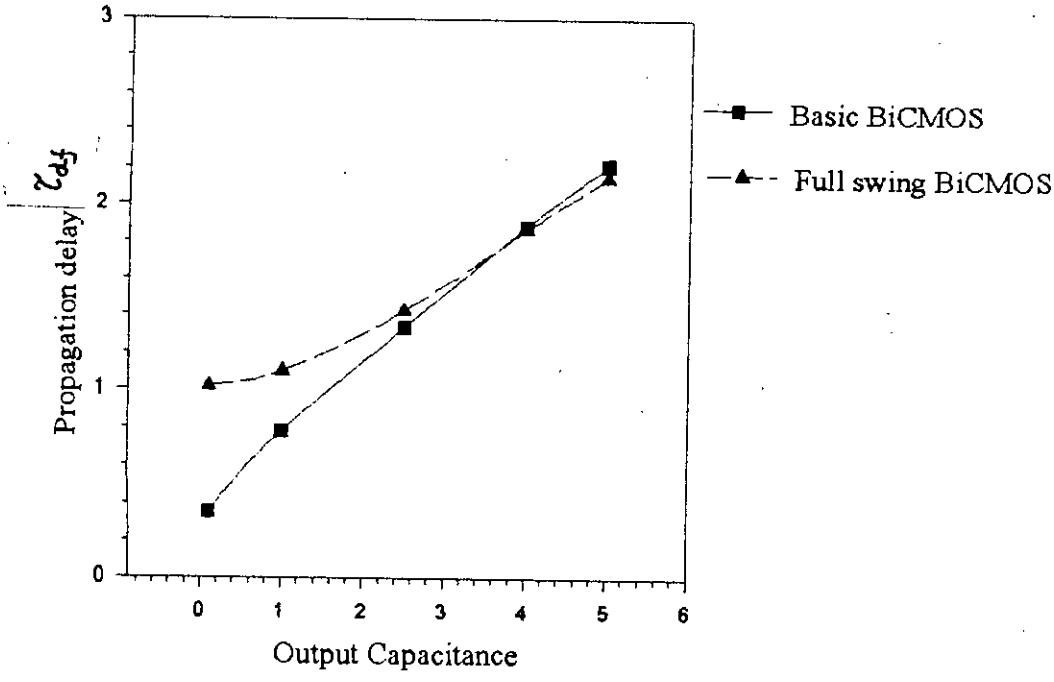

Fig: 3.6 Propagation delay vs. output capacitance for BiCMOS circuits

Chapter 4

Fault Characterization of BiCMOS Logic Circuits

4.1 Introduction:

The behavior of different BiCMOS logic circuits under various faults are investigated in this chapter. Various modes of failure can occur in VLSI circuits resulting in stuck-at, stuck-on, stuck-open, bridging faults etc. To avoid the complexity of dealing with multiple defect case, it is assumed in this chapter that not more than one defect can occur at a time. Single stuck-on and single stuck-open faults in MOS logic transistors and bipolar transistors are considered. Multiple faults are clearly possible but it seems reasonable to suppose that a circuit with two faults will still fail test programs. Of course there may be fault masking but very few researchers believe that this is a significant problem in practice [22]. Another reason to support single stuck fault model is that due to exponential rise of multiple fault conditions with the number of nodes, it may not be

feasible to consider all the possibilities [22]. The results of extensive SPICE simulation using various fault models are presented in this chapter.

4.2 Fault Modeling:

Physical defects in VLSI circuits can be modeled as opens or shorts in switch level representation [11], [22]. For a more realistic modeling the possibility of a short between two terminals (collector-emitter for bipolar and drain-source for MOS) of a transistor as well as an open in one transistor node (collector or emitter for bipolar and drain or source for MOS) are considered. Shorts are modeled as a small resistor between two nodes. Open circuits are modeled as a large resistor inserted between the affected node and the node to which it would normally have been connected. The values of the resistors, modeling shorts and opens, are varied in a wide range to take into account faults of various strengths.

The following nomenclatures are used to represent various faults in a circuit:

If a fault is caused by a short between two nodes of a transistor, it is referred to by the first letters of those nodes, followed by the name of the transistor; e.g., a fault caused by a short between drain and source of MOS m_2 will be referred to as dsm_2 . This fault is also referred to as a transistor stuck-on fault. Stuck-on fault in an active device means that the device is permanently ON even in the absence of an input excitation. An open fault at a transistor node will be referred to by the first letter of that node, followed by the name of the transistor; e.g., an open in the collector of q_1 will be denoted by cq_1. This fault can also be defined as transistor stuck-open fault. With this fault an active device remains permanently OFF even in the absence of any input excitation.

Figures 4.1 and 4.2 shows how these two types of faults are modeled.

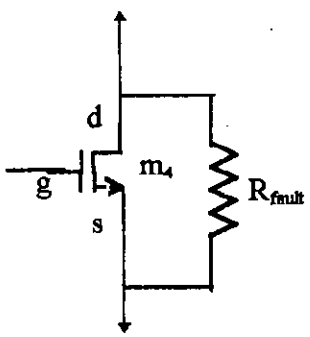

Fig. 4.1 Stuck-on fault model for MOS m_4

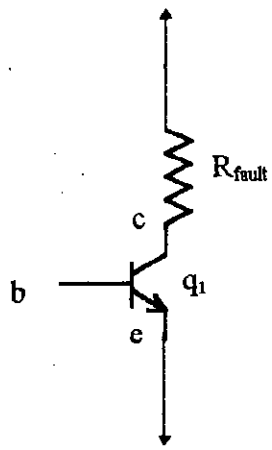

Fig. 4.2 Stuck-open fault model for bipolar q_1

4.3 Behavior Of BiCMOS Circuits Under Single Stuck Faults:

The behavior of BiCMOS circuits under single stuck-on and single stuck-open fault in MOS and bipolar parts are analyzed in this section. Both the basic BiCMOS and full-swing low-capacitance BiCMOS circuits are considered. The two input NAND gates shown in Figures 4.3 and 4.4 for the basic and full-swing BiCMOS case are used in this analysis.

4.3.1 Stuck-on Faults:

dsm_4: (Stuck-on fault in m_4 of Fig. 4.3)

Referred to Fig. 4.3 physical defects may cause m_4 to be permanently ON, thus causing a stuck-on fault. The fault is sensitized when V_2 = 5v and V_3 = 0v are applied. In a fault free circuit these vectors would have pulled the output node 5 to a high level of (V_{DD} - V_{BE}). The input vectors causes m_3 and m_2 to turn on. With dsm_4 , m_4 is also ON and a low resistance path is thus

established from V_{DD} to ground. This causes supply current to increase. The amount of current depends on the resistances of the ON transistors (m_2 and m_3) and the fault strength at m_4. The voltage at the internal node 4 also depends on the ON resistances of m_2 and m_3, and on the fault strength. Since the ON resistance of a transistor depends on its geometry, therefore for a particular value of fault resistance, the voltage V_4 is independent of the sizes of transistors m_2 and m_3. That is when the circuit is sensitized for dsm_4 then the voltage V_4 varies with device geometry and fault strength. Therefore V_4 can have any value between 0 and 5v depending on device geometry and fault strength. Consequently the output voltage at node 5 may have any value between logic low to logic high level with it's value less than V_4 by V_{BE}. Under the fault sensitized condition m_6 remains OFF thus no base current for q_2 and it remains OFF. Thus, the fault dsm_4 is not detectable by logic monitoring. However, it may be detected by the increase in power supply current.

$dsmn_1$: (Stuck-on fault in mn_1 of Fig. 4.4)

For a stuck-on fault in the full swing BiCMOS NAND gate (referred to Fig. 4.4), behavior is almost the same as that of the basic BiCMOS gate described above. This fault is sensitized when V_2 = 0v and V_3 = 5v are applied. Therefore mp_1 is turned ON thus pulling V_4 to a high value, turning qn_1 ON, and consequently charging the output node 5. However, as mn_2 is ON (V_3 = 5v) and mn_1 is also ON due to fault, node 7 has a low resistance path to ground. Then due to high output node, $|V_{BE}| > |V_{BEon}|$ for qp_1. The output discharges through qp_1 and at the same time it is charged up through qn_1, thereby causing large supply current. Again due to lower V_7, V_{GS} for mn_4 is greater than V_{tn} and $|V_{GS}|$ for mp_4 is greater than $|V_{tp}|$, so these transistors are also ON, providing another current path from V_{DD} to ground. The current is constant for a

particular device geometry. The node voltage V_4 depends on the ON resistances and thus on the device geometry of mp_1, mp_4, mn_4, mn_2, as well as on the fault strength at mn_1. Therefore, V_4 may have any value between 0v and V_{DD}. As a result output at node 5 under fault is indeterminate. Hence, in similarity with dsm_4, this fault cannot be detected by logic monitoring. However, it may be detected by current monitoring.

dsm_1: (Stuck-on fault in m_1 of Fig. 4.3)

When m_1 is permanently ON, the fault is sensitized by applying V_2=V_3=5v. Thus m_3 and m_4 are ON. Due to faulty m_1 a low resistance path is established between V_{DD} and ground. Consequently there is a large power supply current when the fault is sensitized. The voltage at node 4 then depends on the resistances (thus on device geometry) of m_3 and m_4 and on the fault strength at m_1. If m_1 is very strongly ON then the voltage drop across m_1 may be so small that V_4 may have a high logic level. This causes q_1 to turn ON thereby charging output node #5. High V_4 also causes m_7 to turn ON. As m_5 and m_6 are ON due to the input vectors, q_2 turns on. The output tends to discharge through q_2 and at the same time it is charged up by q_1. Therefore, there would be large increment in supply current when the fault dsm_1 is sensitized. However, the output logic level is unpredictable.

If m_1 is very poorly ON, V_4 may have a much lower voltage level turning q_1 either very weakly ON or OFF. Consequently V_5 will have a much lower voltage level than for the case discussed above (when m_1 was assumed strongly ON).

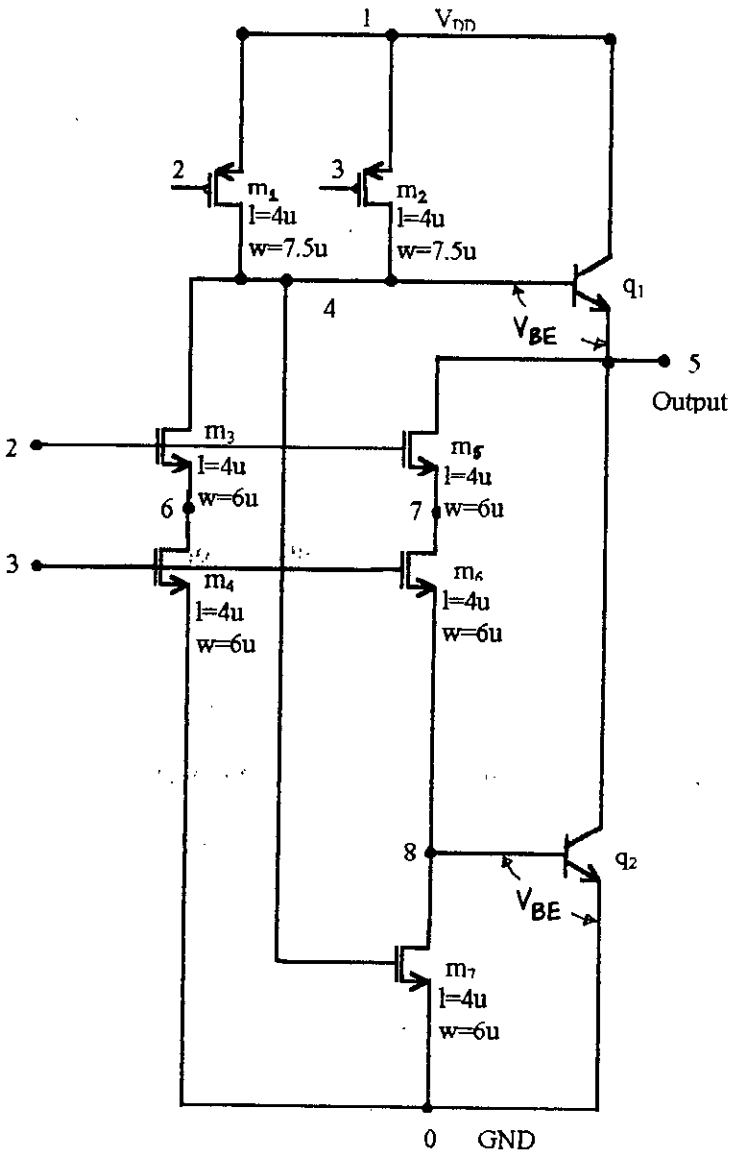

Fig: 4.3 Basic BiCMOS NAND gate

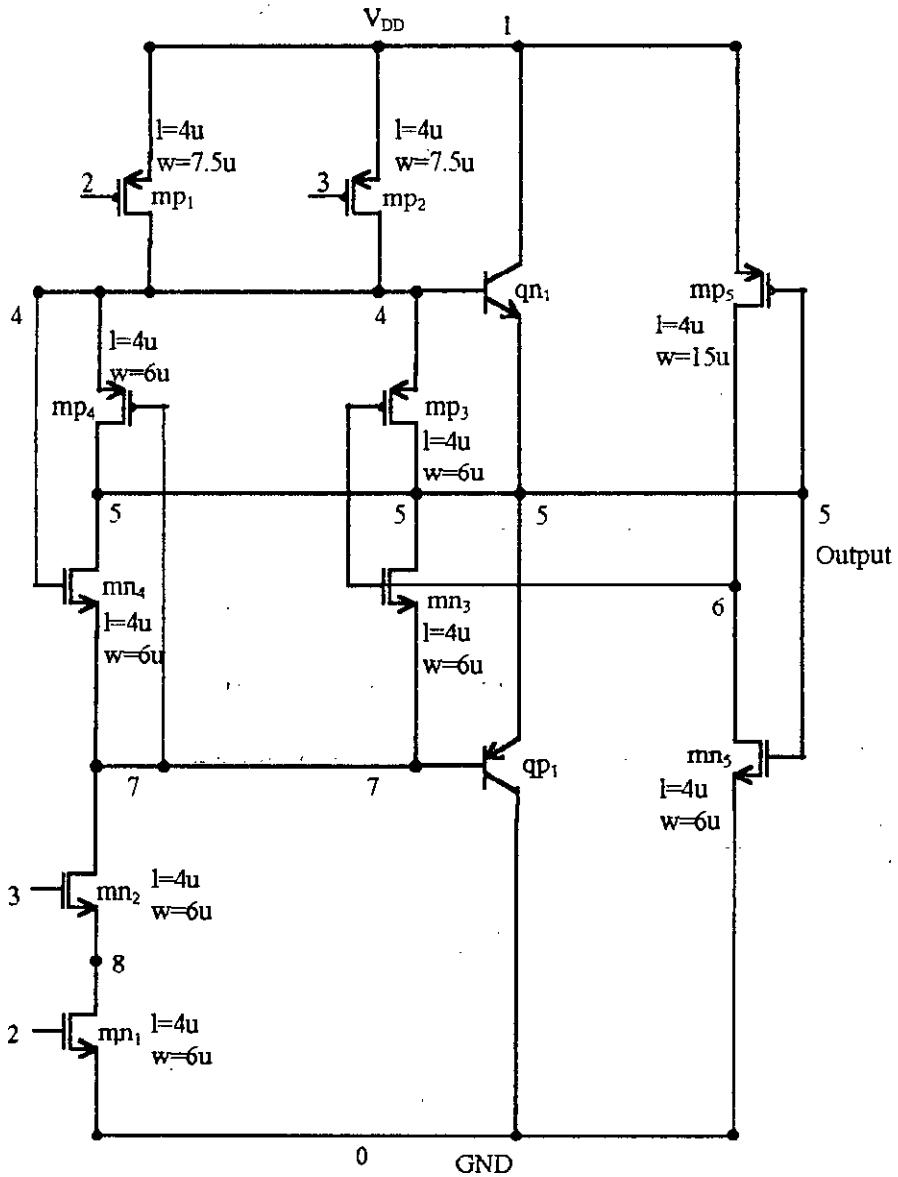

Fig: 4.4 Full-Swing BiCMOS NAND gate

dsmp$_1$: (Stuck-on fault in mp$_1$ of Fig. 4.3)

Fault sensitizing vector is the same as dsm$_1$, i.e., V_2=V_3= 5v. Faulty mp$_1$ causes node 4 to be charged up. If V_4 is a reasonably high voltage then qn$_1$ turns on and output node 5 charges up towards (V_4 - V_{BE}). High inputs connect node 7 to ground. As a result qp$_1$ turns on and large power supply current flows as in the case of dsm$_1$. Output logic is unpredictable as well. Low V_7 also causes mp$_4$ to turn ON and high V_4 causes mn$_4$ to turn ON. Thus another conducting path is established from V_{DD} to ground through faulty mp$_1$, and mp$_4$, mn$_4$, mn$_2$ and mn$_1$. If mp$_1$ is weakly ON due to the fault then the voltages at node 4 and node 5 may be much lower than the case when mp$_1$ is strongly ON.

ceq$_1$: (Stuck-on fault in q$_1$ of Fig. 4.3)

The fault is sensitized by applying V_2 = V_3 = 5v. In a fault free circuit the output would have been pulled down to logic low level. However, due to the fault the output node 5 is always connected to V_{DD} through q$_1$. Due to the input vectors m$_5$ and m$_6$ are ON and connect the base of q$_2$ to the output node 5 thus turning it ON. This causes a large increment in power supply current when the fault is sensitized. This current depends on the fault strength. Also, the output voltage level at node 5 is unpredictable and depends on how hard q$_1$ is ON. Therefore, the stuck-on fault in q$_1$ can not be detected by logic monitoring. However, it may be detected by current monitoring

ceqn$_1$: (Stuck-on fault in qn$_1$ of Fig. 4.4)

The behavior of the circuit under ceqn$_1$ fault is little more complicated than the corresponding fault in the basic BiCMOS gate. The fault ceqn$_1$ in Fig. 4.4 is sensitized by the

application of $V_2 = V_3 = 5v$. For these inputs, the output V_5 in a fault free gate would be low. However, due to the fault output node 5 is always connected to V_{DD} through the permanently ON transistor qn_1. Thus, output node 5 may attain a high voltage level. High output causes V_6 to become low. Depending on the previous states of the inputs, low V_6 may cause mp_3 to turn ON. Also, due to ON states of mn_1 and mn_2, node 7 is connected to ground and mp_4 will be ON. Thus node 4 is charged by the output current through mp_4 and mp_3 and V_4 becomes equal to the output voltage. The rise in V_4 causes mn_4 to turn ON and offers output current a parallel path through mn_4, mn_2 and mn_1. Thus voltage at node 7 is clamped by mn_4 at $(V_4 - V_{tn})$.

For a poorly ON transistor (qn_1) output may assume low state (1v to 2v). Depending on the aspect ratio (W/L) of output inverter, V_6 may be high enough so that mp_3 remains in the OFF state. This high V_6 will then cause mn_3 to turn ON and provide an additional path for the output current to pass through mn_1 and mn_2. However, mp_4 will still be ON due to ON states of mn_1 and mn_2 causing node 4 to charge up until V_4 equals V_5. Then mn_4 turns ON and clamps V_7 at $(V_4 - V_{tn})$. It is clear that there will be a significant increment in power current when the fault $ceqn_1$ is sensitized. However, the output logic level is unpredictable.

ceq_2: (Stuck-on fault in q_2 of Fig. 4.3)

The fault is sensitized when one (or both) of the input line is grounded. Thus node 4 is pulled up to logic high state and q_1 turns ON. Due to faulty q_2 a low resistance path is established between V_{DD} and ground. The voltage V_{DD} is divided between the transistors q_1 and q_2 according to the ratio of their ON resistances. As q_1 operates in the linear region, a constant current flows through q_1 and q_2 depending on the fault strength at q_2. When fault resistance is low the current is

high and the output node 5 may remain at a logic low level. However, for a very large fault resistance at q_2, the output may attain a logic high level.

ceqp$_1$: (Stuck-on fault in qp_1 of Fig. 4.4)

The behavior of the full swing BiCMOS circuit under this fault is similar to the fault ceq_1 in the basic BiCMOS NAND gate. Depending on the fault strength output logic level may be at any state between 0v to 5v. Fault sensitizing pattern (one or both of the input grounded) turns qn_1 ON. Thus V_{DD} is connected to ground through qn_1 and the faulty qp_1. As a result, power supply current increases. Low fault resistance causes output to remain at logic low level. Then V_6 is high which causes mn_3 to turn ON and pulling node 7 to output voltage level. As a result $|V_{BE}|$ for qp_1 is zero and it is clamped OFF. With increasing fault resistance output increases to logic high level. V_4 is always greater than output level by V_{BE}. High V_4 causes mn_4 to turn ON and node 7 is pulled to the output level.

4. 3. 2 Spice Simulation Results For Stuck-On Faults:

This section summarizes the SPICE simulation results for a single stuck-on fault in both the MOS and bipolar sections of the basic BiCMOS NAND gate as well as the full swing BiCMOS NAND gate. Length of all the MOS devices are taken as 4μm and SPICE Level-2 mode parameters are used for simulating the circuits.

Table 4.1: SPICE simulation results for stuck-on fault in nMOS transistor m_4 in the basic BiCMOS NAND gate of Fig 4.3

Fault	Fault Resistance Ohms	Transistor Size W_P/W_N	Input Logic V_1	V_2	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-4} A
dsm_4	1	7.5/24	5	0	0.828	0.335	4.55
dsm_4	10	7.5/24	5	0	0.833	0.340	4.55
dsm_4	100	7.5/24	5	0	0.879	0.385	4.54
dsm_4	1K	7.5/24	5	0	1.317	0.823	4.36
dsm_4	1	7.5/6	5	0	2.913	2.418	3.09
dsm_4	10	7.5/6	5	0	2.915	2.420	3.09
dsm_4	100	7.5/6	5	0	2.940	2.444	3.06
dsm_4	1K	7.5/6	5	0	3.151	2.813	2.82
dsm_4	1	24/6	5	0	4.342	4.369	3.68
dsm_4	10	24/6	5	0	4.343	4.371	3.67
dsm_4	100	24/6	5	0	4.352	4.570	3.63
dsm_4	1K	24/6	5	0	4.428	3.934	3.23

** Normal operating current is about 30 pA.

Table 4.2: SPICE simulation results for stuck-on fault in nMOS transistor mn_1 in the full-swing BiCMOS NAND gate of Fig 4.4

Fault	Fault Resistance Ohms	Transistor Size W_P/W_N	Input Logic V_2	V_3	V_7 Volts	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-2} A
$dsmn_1$	1	7.5/24	5	0	0.743	2.472	1.608	3.35
$dsmn_1$	10	7.5/24	5	0	0.746	2.476	1.611	3.351
$dsmn_1$	100	7.5/24	5	0	0.781	2.510	1.646	3.319
$dsmn_1$	1K	7.5/24	5	0	0.8	2.54	1.66	3.25
$dsmn_1$	1	7.5/6	5	0	1.764	3.467	2.616	1.99
$dsmn_1$	10	7.5/6	5	0	1.765	3.468	2.617	1.98
$dsmn_1$	100	7.5/6	5	0	1.775	3.477	2.626	1.96
$dsmn_1$	1K	7.5/6	5	0	1.867	3.564	2.716	1.79
$dsmn_1$	1	24/6	5	0	2.652	4.370	3.511	2.73
$dsmn_1$	10	24/6	5	0	2.654	4.372	3.513	2.72
$dsmn_1$	100	24/6	5	0	2.656	4.374	3.516	2.72
$dsmn_1$	1K	24/6	5	0	2.66	4.377	3.518	2.69

** Normal operating current is about 60 pA.

Table 4.3: SPICE simulation results for stuck-on fault in pMOS transistor m_1 in the basic BiCMOS NAND gate of Fig 4.3

Fault	Fault Resistance Ohms	Transistor Size W_P/W_N	Input Logic V_1	V_2	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-3} A
dsm_1	1	7.5/24	5	5	4.999	4.215	2.21
dsm_1	10	7.5/24	5	5	4.992	4.208	2.21
dsm_1	100	7.5/24	5	5	4.923	4.138	2.25
dsm_1	1K	7.5/24	5	5	4.25	3.462	2.43
dsm_1	10K	7.5/24	5	5	1.395	0.738	0.37
dsm_1	1	7.5/6	5	5	4.999	4.216	1.64
dsm_1	10	7.5/6	5	5	4.997	4.214	1.65
dsm_1	100	7.5/6	5	5	4.979	4.195	1.66
dsm_1	1K	7.5/6	5	5	4.797	4.011	1.75
dsm_1	10K	7.5/6	5	5	3.232	2.451	1.44

** Normal operating current is about 30 pA.

Table 4.4: SPICE simulation results for stuck-on fault in pMOS transistor mp_1 in the full-swing BiCMOS NAND gate of Fig 4.4

Fault	Fault Resistance Ohms	Transistor Size W_P/W_N	Input Logic V_2	V_3	V_7 Volts	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-2} A
$dsmp_1$	1	7.5/6	5	5	3.313	4.999	4.156	1.46
$dsmp_1$	10	7.5/6	5	5	3.311	4.997	4.154	1.46
$dsmp_1$	100	7.5/6	5	5	3.289	4.975	4.132	1.45
$dsmp_1$	1K	7.5/6	5	5	3.085	4.769	3.927	1.40
$dsmp_1$	10K	7.5/6	5	5	2.192	3.855	3.023	0.95
$dsmp_1$	1	7.5/24	5	5	3.236	4.999	4.117	6.4
$dsmp_1$	100	7.5/24	5	5	3.165	4.927	4.046	6.32
$dsmp_1$	1K	7.5/24	5	5	2.603	4.360	3.482	5.60
$dsmp_1$	10K	7.5/24	5	5	1.044	2.748	1.896	2.06

** Normal operating current is about 60 pA.

Table 4.5: SPICE simulation results for stuck-on fault in bipolar driver qn_1 in the basic BiCMOS NAND gate of Fig 4.3

Fault	Fault Resistance Ohms	Transistor Size W_P/W_N	Input Logic V_1	V_2	V_4 Volts*10^{-7}	Output V_5 Volts	Power Supply Current I (V_{DD}) *10^{-3} A
ceq_1	1	7.5/6	5	5	2.52	4.991	8.78
ceq_1	10	7.5/6	5	5	2.52	4.912	8.77
ceq_1	100	7.5/6	5	5	2.52	4.157	8.42
ceq_1	1K	7.5/6	5	5	2.51	1.679	3.32

** Normal operating current is about 30 pA.

Table 4.6: SPICE simulation results for stuck-on fault in bipolar driver qn_1 in the full-swing BiCMOS NAND gate of Fig 4.4

Fault	Fault Resistance Ohms	Transistor Size W_P/W_N	Input Logic V_2	V_3	V_7 Volts	V_4 Volts	Output V_5 Volts	Power Supply Current I (V_{DD}) *10^{-2} A
$ceqn_1$	1	7.5/6	5	5	4.134	4.982	4.982	1.76
$ceqn_1$	10	7.5/6	5	5	3.977	4.825	4.825	1.74
$ceqn_1$	100	7.5/6	5	5	2.726	3.568	3.568	1.43
$ceqn_1$	1K	7.5/6	5	5	1.186	1.988	1.988	0.30
$ceqn_1$	1	7.5/24	5	5	4.043	4.927	4.927	7.21
$ceqn_1$	10	7.5/24	5	5	3.441	4.323	4.323	6.76
$ceqn_1$	100	7.5/24	5	5	1.266	2.127	2.127	2.87
$ceqn_1$	1K	7.5/24	5	5	0.376	1.184	1.184	0.38

** Normal operating current is about 60 pA.

Table 4.7: Spice simulation results for stuck-on fault in bipolar driver q_2 in the basic BiCMOS NAND gate of Fig 4.3

Fault	Fault Resistance Ohms	Transistor Size W_P/W_N	Input Logic V_1	V_2	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-2} A
ceq_2	1	7.5/6	0	0	0.981	0.091	9.10
ceq_2	10	7.5/6	0	0	1.722	0.834	8.34
ceq_2	100	7.5/6	0	0	4.067	3.203	3.20
ceq_2	1K	7.5/6	0	0	4.891	4.080	0.40
ceq_2	1	24/6	0	0	1.205	0.285	28.5
ceq_2	10	24/6	0	0	2.912	2.001	20.01
ceq_2	100	24/6	0	0	4.675	3.807	3.80
ceq_2	1K	24/6	0	0	4.965	4.154	0.41

** Normal operating current is about 30 pA.

Table 4.8: Spice simulation results for stuck-on fault in bipolar driver qp_1 in the full-swing BiCMOS NAND gate of Fig 4.4

Fault	Fault Resistance Ohms	Transistor Size W_P/W_N	Input Logic V_2	V_3	V_7 Volts	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-2} A
$ceqp_1$	1	7.5/6	0	0	0.0902	0.980	0.0902	9.02
$ceqp_1$	10	7.5/6	0	0	0.827	1.715	0.827	8.27
$ceqp_1$	100	7.5/6	0	0	3.065	3.928	3.065	3.06
$ceqp_1$	1K	7.5/6	0	0	3.886	4.694	3.886	0.38
$ceqp_1$	1	24/6	0	0	0.284	1.204	0.284	28.4
$ceqp_1$	10	24/6	0	0	1.996	2.907	1.996	19.97
$ceqp_1$	100	24/6	0	0	3.745	4.613	3.745	3.74
$ceqp_1$	1K	24/6	0	0	4.093	4.903	4.093	0.41

** Normal operating current is about 60 pA.

4. 3. 3 Effects of Device Geometry:

When stuck-on fault in nMOS transistors occurs, i.e., **dsm_4** in the basic BiCMOS NAND gate of Fig. 4.3 or **$dsmn_1$** in the full swing BiCMOS NAND gate of Fig. 4.4, the effect of device geometry on the output voltage and power supply current is very prominent as can be seen from Tables 4.1 and 4.2 respectively. When the width of logic implementing pMOS transistors (m_1 and m_2 in Fig. 4.3 and mp_1 and mp_2 in Fig 4.4) are increased, their ON resistances decrease. As described in Art. 4.3, fault sensitizing pattern activates one pMOS and a direct path from V_{DD} to ground is established. Now, due to decreased ON resistance of the active pMOS devices the voltage at the internal node 4 increases and consequently the output voltage increases. On the contrary, when width of the nMOS devices (m_3 and m_4 in Fig. 4.3 and mn_1 and mn_2 in Fig 4.4) increases, voltage at node 4 decreases. As a result output voltage also decreases. Thus with varying device geometry, output voltage varies from a very low to a very high level [~ 1.5v to 3.6v, referred to Tables 4.1 and 4.2]. This effect is depicted in Fig. 4.5, Fig. 4.6, Fig. 4.7 and Fig. 4.8. For a particular device geometry when fault resistance is varied, the power supply current also varies slightly.

It is seen from Tables 4.3 and 4.4 that the MOS device sizes have negligible effect on the output voltage level when there is single stuck-on faults in the pMOS devices of the NAND gate circuits (Figures 4.3 and 4.4). Application of the fault sensitizing pattern turns the series nMOS devices (m_3, m_4 in Fig 4.3 and mn_1, mn_2 in Fig. 4.4) ON. If their total (series) ON resistance is large compared to the resistance of the faulty p-device then changing the sizes of series nMOS devices have negligible effect on the voltage at node 4 in both circuits. Figures 4.9 and 4.10

illustrates this phenomenon for fault resistance equal to 1 Kohm. However, if the faulty p-device is weakly ON then its ON resistance is much higher, e.g., 10KΩ, and becomes comparable to the ON resistance of the series nMOS devices. In such case, increasing the width of nMOS devices causes the output (V_5 in Fig. 4.3 OR V_7 in Fig. 4.4) to decrease due to the decreased voltage level at node 4. This is illustrated in Figures 4.11 and 4.12 for the basic BiCMOS and the full-swing BiCMOS NAND gate respectively.

It is clear from Table 4.5 that change in MOS device geometry have no effect on the output voltage when stuck-on fault occurs in bipolar driver q_1 of basic BiCMOS gate (Fig. 4.3) because, the output gets directly connected to V_{DD} through the faulty device q_1. As a result, output depends only on the fault resistance. Output reduces with increased fault resistance due to increased voltage drop across the resistance. This phenomenon is depicted in Fig. 4.13. However, it is seen from Table 4.6 that in case of $ceqn_1$ fault in the full swing BiCMOS gate of Fig 4.4, output voltage drops slightly with increased width of the nMOS devices mn_1 and mn_2. These devices are in the ON state due to fault sensitizing pattern (5, 5) and therefore connect node 7 to ground. The output node 5 gets connected to node 7 through mn_4. As a result increased width of mn_1 and mn_2 causes the output to decrease for the same fault strength.

Tables 4.7 and 4.8 show that change in the MOS device sizes have no effect on output voltage when the faults ceq_2 in Fig 4.3 or the fault $ceqp_1$ fault in Fig 4.4 are sensitized. In this case output gets connected to ground through the faulty devices in both circuits. Power supply current depends on the fault resistance. Output voltage increases with increased fault resistance and the power supply current decreases. The effect of fault strength on the output as well as on internal node 4 are illustrated in Figures 4.14 and 4.15.

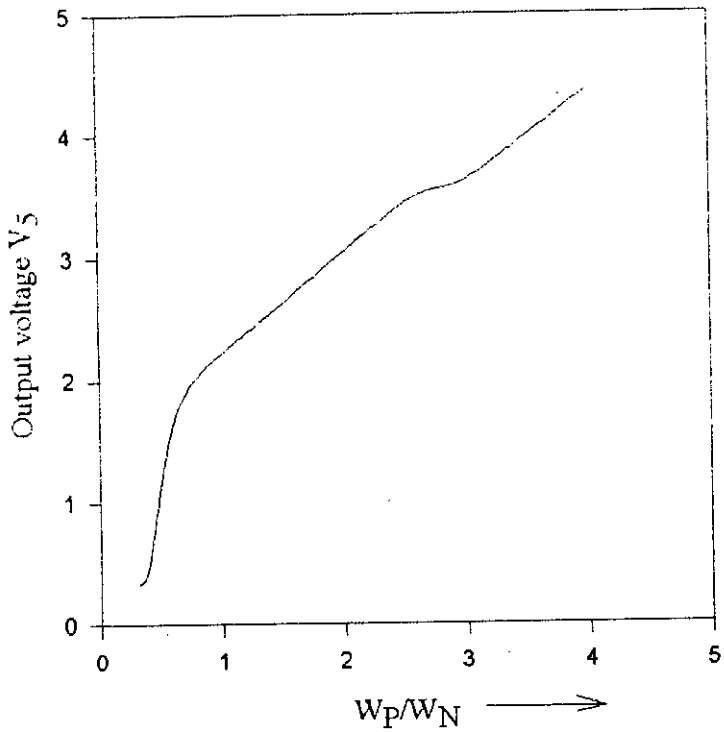

Fig. 4.5 Variation of output with device parameter for dsm_4 fault in Fig. 4.3 (fault resistance is 1 ohm).

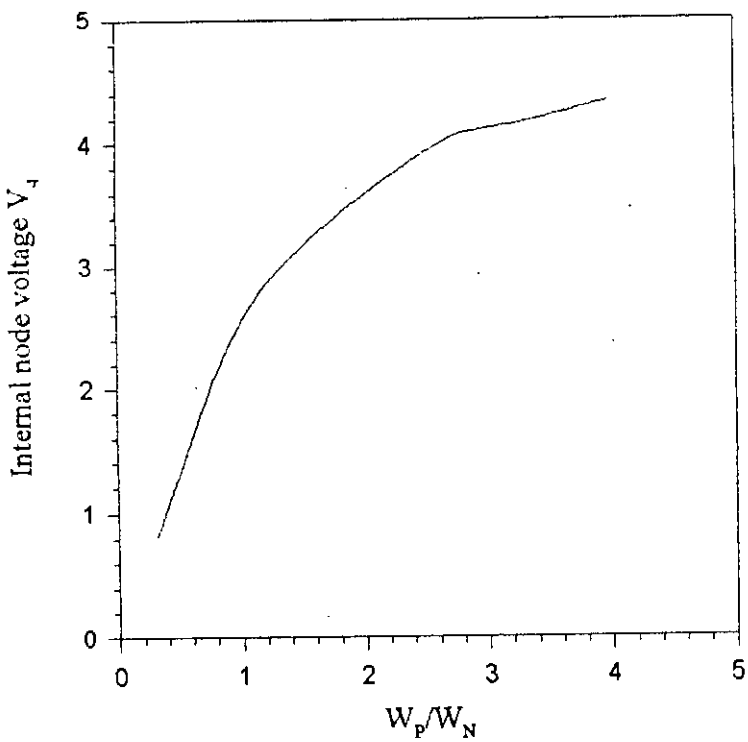

Fig. 4.6 Variation of V_4 with device parameter for dsm_4 fault in Fig. 4.3 (fault resistance is 1 ohm).

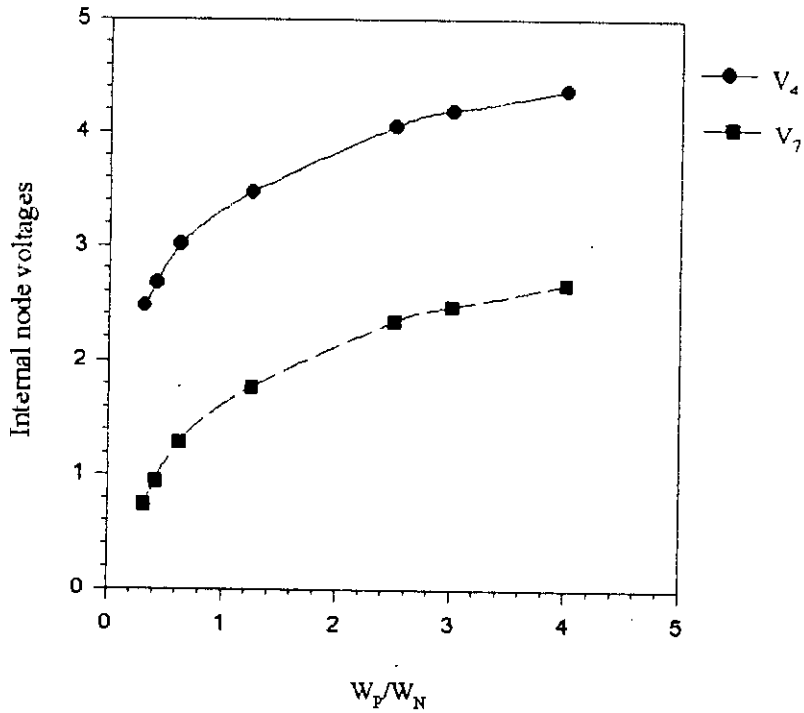

Fig. 4.7 Internal node voltages (V_4 & V_7) vs device parameter for $dsmn_1$ fault in Fig. 4.4

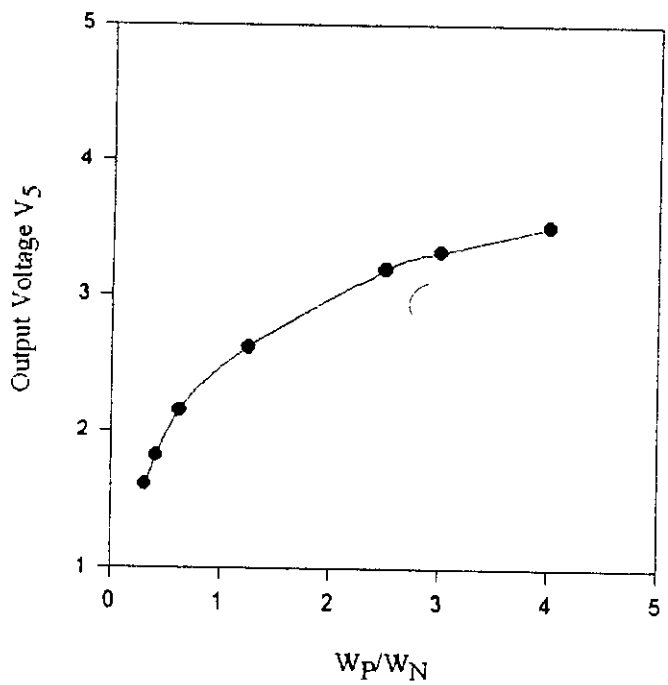

Fig. 4.8 Output voltage V_5 vs. width ratio (W_P/W_N) for $dsmn_1$ fault of Fig. 4.4

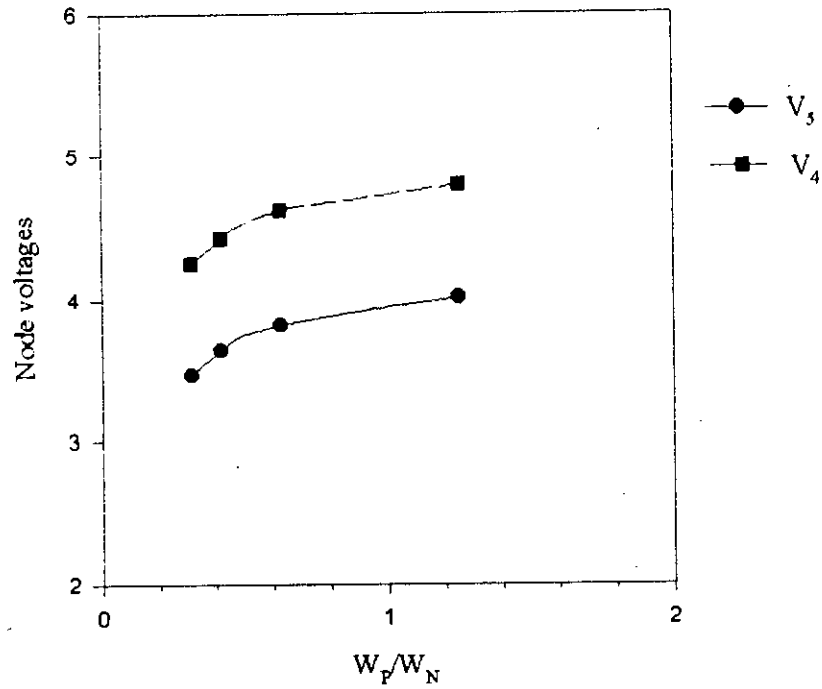

Fig. 4.9 Node voltages vs. device geometry for dsm_1 fault in Fig. 4.3 (fault resistance is 1K ohms).

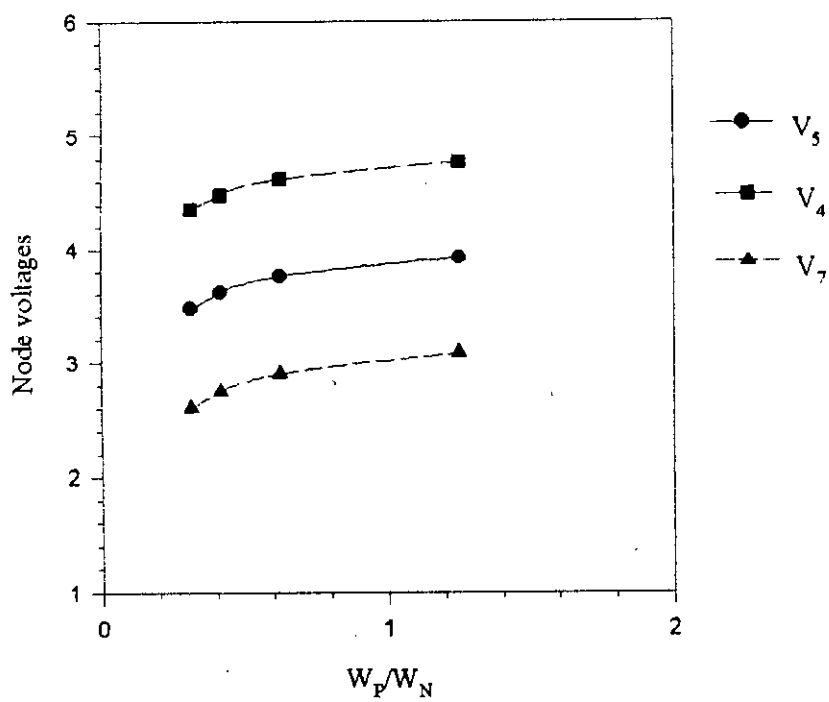

Fig. 4.10 Node voltages vs. device parameters for $dsmp_1$ fault in Fig. 4.4 (fault resistance is 1K ohms).

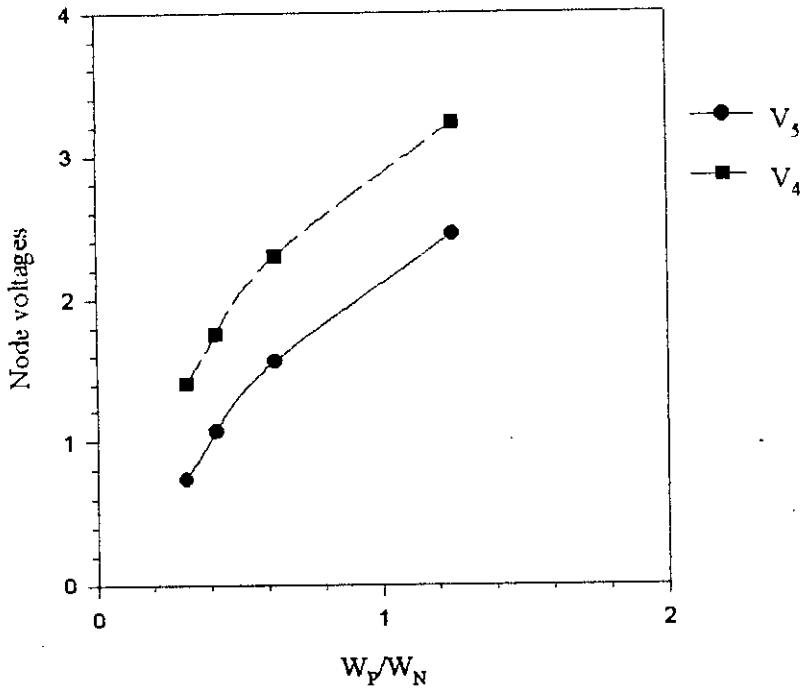

Fig. 4.11 Node voltages vs. device geometry for dsm_1 fault in Fig. 4.3 (fault resistance is 10K ohms) .

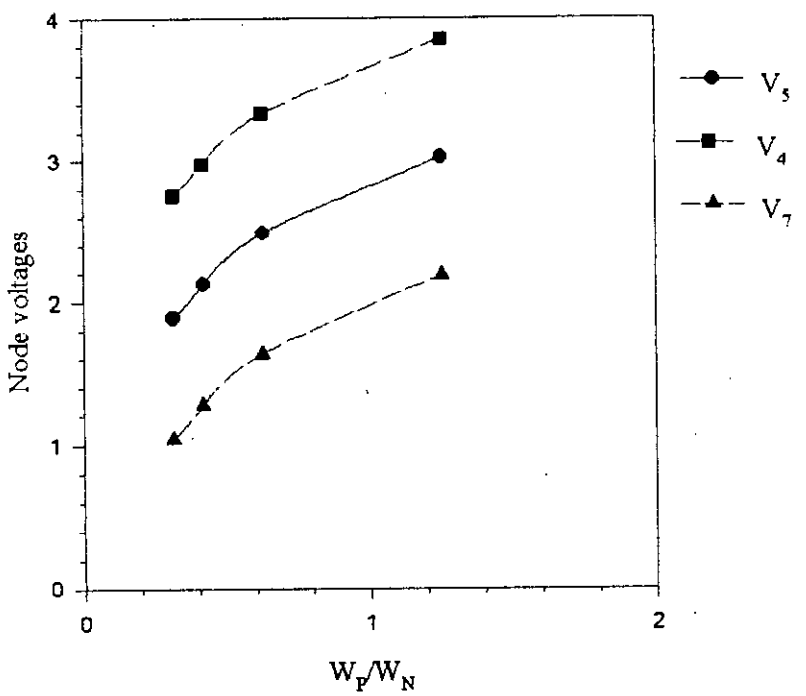

Fig. 4.12 Node voltages vs. device parameters for $dsmp_1$ fault in Fig. 4.4 (fault resistance is 10K ohms) .

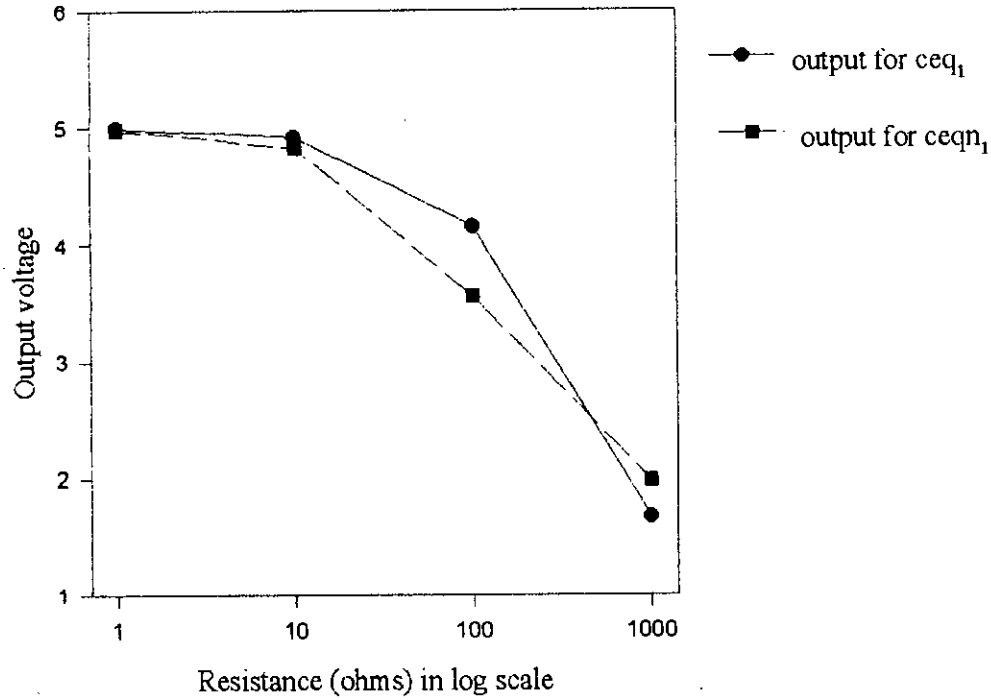

Fig. 4.13 Output voltage level vs. fault resistance for ceq_1 and $ceqn_1$ fault in figures 4.3 and 4.4 respectively

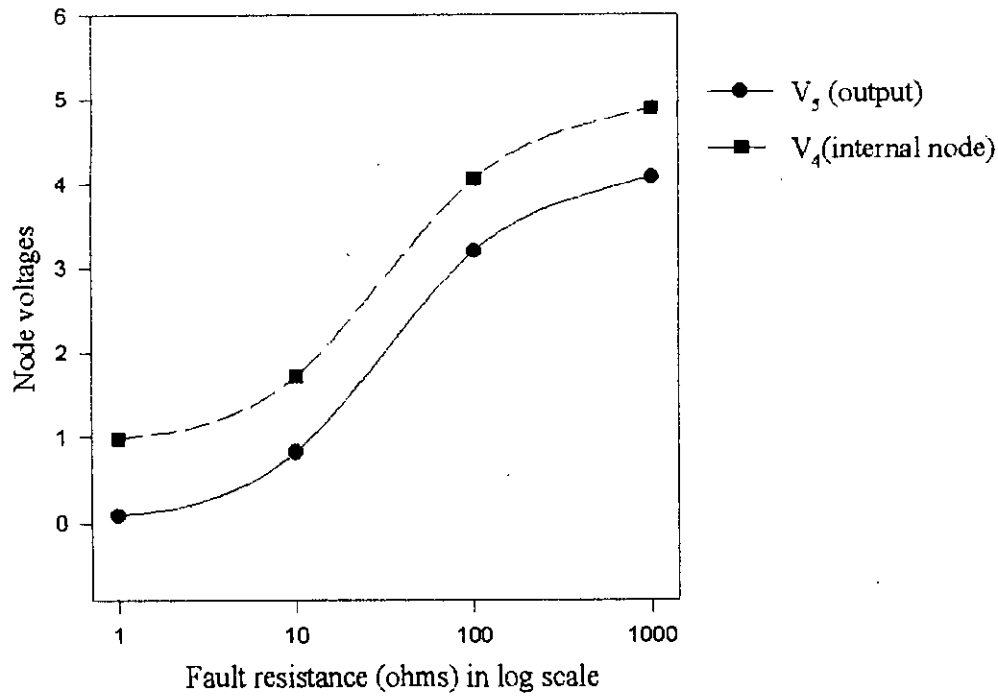

Fig. 4.14 Node voltages vs. fault resistance for ceq_2 fault in Fig. 4.3

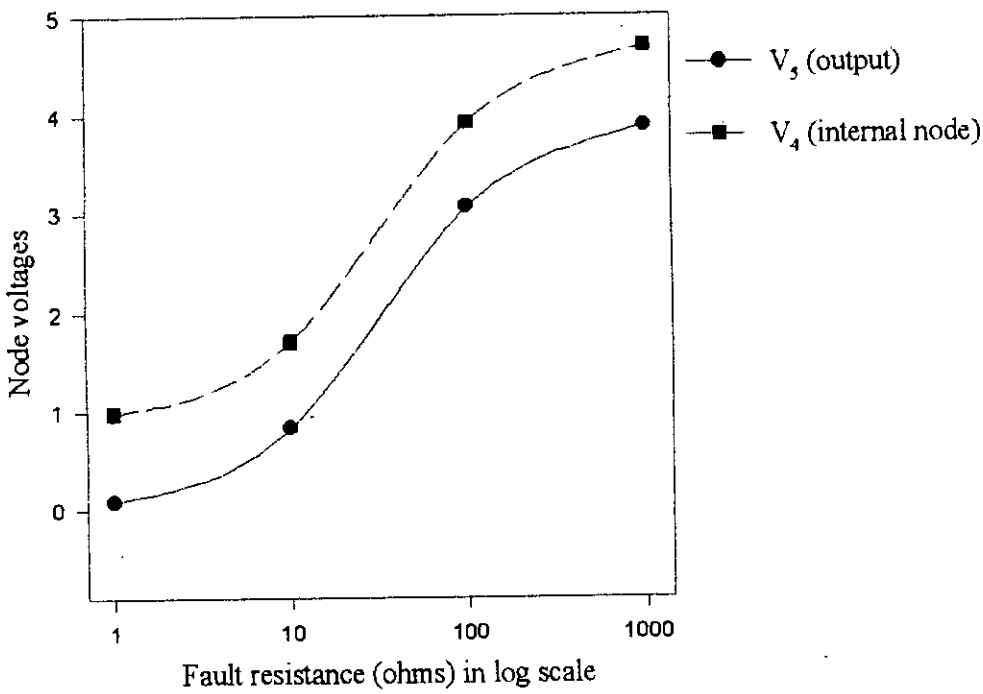

Fig. 4.15 Node voltages vs. fault resistance for $ceqp_1$ fault in Fig. 4.4

4. 3. 4 Comparison with Standard CMOS:

Behavior of BiCMOS circuits under single stuck-on faults are similar with the behavior of conventional CMOS circuits under the same fault. When a stuck-on fault occurs in MOS section of the BiCMOS NAND gate, change in device geometry as well as change in fault resistance affect the output logic level in much the same way as they affect the output of a faulty standard CMOS gate. It is seen from Tables 4.1 through 4.8 that the increment in power supply current when a single stuck-on fault in BiCMOS circuits is sensitized varies approximately between 10^8 and 10^9. In a static CMOS circuit, the order of magnitude difference between the fault current and normal leakage current can be as high as 9 [25], [26]. Therefore the increment in power supply current in BiCMOS circuits under single stuck-on faults is of the same order of magnitude as that in standard CMOS providing almost the same levels of device integration.

4.4 Stuck Open Faults:

Physical defects may cause a transistor to become permanently open and insensitive to it's input signal. The transistor is then said to be stuck open. The affected transistor then inserts a very high resistance (>10Meg ohms) between its drain and source terminals (for MOS) or collector and emitter terminals (for BJT). The effects of a single stuck-open faults in both MOS and bipolar sections of the basic BiCMOS NAND gate as well as the full swing BiCMOS gate will be considered next.

sm_4 : (Stuck-open fault in m_4 of Fig. 4.3)

Two pattern test is used to detect the stuck-open fault in MOS m_4 of Fig. 4.3. First, one of the input is grounded so that internal node #4 and output node #5 goes high. Then both of the inputs are raised to logic high level (V_2=V_3=5v). A fault free circuit would have produced low output. But since m_4 is permanently open due to the fault, node 4 can not discharge quickly. Due to very large resistance from source to ground of m_4, time constant for V_4 to discharge through m_3 and m_4 may be very large. As a result V_4 as well as V_5 remain at high state. However high V_4 keeps m_7 in the ON state. Also the fault sensitizing vectors (V_2 = V_3 = 5v) keeps m_5 and m_6 ON, and provides the base bias for q_2. Therefore q_2 turns ON and the output node 5 tends to discharge through two parallel paths : one through m_3, m_5 and m_7 while the other through q_2. But as soon as the output node 5 starts discharging, V_{BE} of q_1 increases, sourcing more current to charge up the output node. The voltage at the output node will be less than V_4 by V_{BE}. A large power supply current will flow due to ON states of q_1, q_2, m_3, m_5 and m_7. Unlike standard CMOS, the stuck open fault in m_4 of Fig. 4.3 can not be detected by logic monitoring. However, this fault may be detected by current monitoring.

smn_1: (Stuck-open fault in n-MOS mn_1 of Fig. 4.4)

The behavior of the full swing circuit under dmn_1 fault is the same as that described above for sm_4 fault in the basic BiCMOS NAND gate. Two pattern test is again used to detect the fault. First, the output node 5 is made high by grounding one of the inputs. Then high logic is applied to both the inputs (V_2 = V_3 =5v) . Due to high resistance from source to ground of faulty mn_1, node 7 can not discharge to the ground level. As a result qp_1 can not turn ON and output remains in the high state. Due to high V_7, mp_4 and mn_4 also can not turn fully ON and node 4

also remains at high state. As a result circuit remembers it's previous state. Therefore this fault may be detected by logic monitoring

dm_1: (Stuck-open fault in MOS m_1 of Fig. 4.3)

Two pattern test is applied to detect the fault. First, both the inputs are raised to high logic level ($V_2 = V_3 = 5v$) so that the output node 5 reaches logic low level. Now the input corresponding to the faulty is lowered to ground level ($V_2 = 0v$). A fault free circuit would have raised the output to logic high level. But the faulty transistor m_1 shows a very high resistance (>10 Meg ohms) between its drain node to V_{DD}. This high resistance together with the parasitic capacitance at node 4 prevents V_4 from charging up to high logic level. Thus q_1 can not turn ON and output remains at logic low level. Therefore, this open fault in the basic BiCMOS NAND gate causes the circuit to behave as a sequential one as in conventional CMOS gate, e.g., it retains it's previous state at the output.

dmp_1: (Stuck open fault in pMOS mp_1 of Fig. 4.4)

Two pattern test is again applied here. First the output is made to assume logic low state by making both the inputs high ($V_2 = V_3 = 5v$). Then the input to mp_1 is grounded ($V_2 = 0v$). But due to its high drain to source resistance node 4 can not charge up to high logic level and q_1 still remains OFF. Thus the output node 5 retains its previous logic low state. This fault can therefore be detected by the two pattern tests using logic monitoring.

eq_2: (Stuck-open fault in bipolar driver q_2 of Fig. 4.3)

Two pattern test is applied to detect the fault. First, one of the inputs is grounded so that output node 5 becomes high. Then high logic level is applied to both the inputs ($V_2 = V_3 = 5v$). This causes node 4 to discharge quickly to ground level through the ON transistors m_3 and m_4. So, q_1 is its previous state.

eqp_1: (Stuck-open fault in bipolar driver qp_1 of Fig. 4.4)

In a full swing BiCMOS NAND gate this fault (emitter of qp_1 open) is masked by the auxiliary circuitry required to attain full swing. Two pattern test is also applied here to detect the fault. First, the output is raised to logic high level. Then as logic (5, 5) is applied at the inputs. Due to high collector resistance qp_1 cannot turn ON even though node 7 is connected to ground through ON transistors mn_1 and mn_2. Thus mp_4 turns ON. Considering previous input state V_4 still remains high and causes mn_4 to remain ON. As a result node 4 discharges through mp_4, mn_4, mn_2, and mn_1. At the same time output also discharges through mn_4, mn_2 and mn_1. When output changes logic level, V_6 becomes high enough to turn mn_3 strongly ON and thus provides additional path for the output to discharge. No significant change in power supply current occurs. So, the fault is completely masked by the additional MOS devices required to attain full swing. However, since BJTs are not involved during output transition from high logic to low logic level, speed is relatively low as compared to a fault free circuit. Therefore this fault can not be detected by either logic or current monitoring.

eq_1 : (Stuck-open fault in bipolar driver q_1)

With emitter of q_1 open in the basic BiCMOS NAND gate, the circuit behaves as a sequential one. Two pattern test is applied to detect the fault. First pattern pulls the output down to logic low state. Then one or both the inputs are grounded. A fault free circuit would have produced logic high output. But due to high emitter resistance, q_1 cannot turn ON even though its base node is charged to high logic level (5v) through ON transistors m_1 or m_2 or both (dcpending on the inputs). As a result output remembers its previous state of logic low level. Consequently power supply current remains at about he same value as in a fault free circuit. Thus this type of fault can only be detected by logic monitoring.

cqn_1: (Stuck-open fault in bipolar driver qn_1)

This type of fault is masked by shunting MOS transistors and clamping MOS devices of full swing circuit. Two pattern test is also applied here to find out whether the circuit behaves as the basic BiCMOS circuit. The first pattern (5,5) causes output to assume low state. Now as one or both the inputs are grounded node 4 charges up to high logic level. Due to high collector resistance qn_1 cannot turn ON. But mn_4 and mp_4 turns ON as V_7 remains at logic low level due to previous inputs (5, 5). Thus the output is charged up through mp_4. Depending on the inverter's (mp_5 and mn_5) output characteristics as output rises to a certain level (2 to 3 volts), mp_3 turns ON and provides parallel charging path for the output to rise towards logic high (5v) level. However, since bipolars are not involved the transition from logic low level to logic high level is

slow as compared to the speed of a fault free circuit. This fault thus can not be detected by either logic or current monitoring.

4. 4. 1. SPICE Simulation Results for Stuck-Open Faults

This section summarizes the spice simulation results for a single stuck-open fault in both the MOS and bipolar section of the basic BiCMOS NAND gate as well as full swing BiCMOS NAND gate. Length of the MOS devices being taken as 4μ and default Level-2 parameters are taken for simulating the circuits.

Table 4.9: SPICE simulation results for stuck-open fault in MOS m_4 of Fig 4.3

Fault	Fault Resistance Ohms	Width Ratio W_P/W_N	Input Logic V_1	V_2	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-3} A
sm_4	10Mega	7.5/6	5	0	5	4.675	4.95×10^{-8}
sm_4	10Mega	7.5/6	5	5	4.518	3.731	1.65
sm_4	100Mega	7.5/6	5	5	4.504	3.717	1.65
sm_4	10Mega	7.5/6	5	5	2.133	1.406	0.158
sm_4	100Mega	7.5/6	5	5	2.156	1.427	0.158

** Normal operating current is about 30 pA.

Table 4.10: SPICE simulation results for stuck-open fault in MOS mp_1 of Fig 4.4

Fault	Fault Resistance Ohms	Width Ratio W_P/W_N	Input Logic V_2	V_3	V_7 Volts	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-6} A
dmp_1	10Mega	7.5/6	5	5	6.87×10^{-7}	1.8×10^{-3}	1.2×10^{-6}	5.85×10^{-5}
dmp_1	10Mega	7.5/6	5	0	0.313	0.524	0.313	1.43
dmp_1	100Mega	7.5/6	5	0	0.033	0.103	0.033	0.06

** Normal operating current is about 60 pA.

Table 4.11: SPICE simulation results for stuck-open fault in MOS m_1 of Fig 4.3

Fault	Fault Resistance MΩ	Width Ratio W_P/W_N	Input Logic V_1	V_2	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-3} A
dm_1	10	7.5/6	5	5	2.51 e-7	0.263	2.36×10^{-8}
dm_1	10	7.5/6	0	5	0.126	0.263	4.87
dm_1	100	7.5/6	0	5	0.015	0.263	0.49

** Normal operating current is about 30 pA.

Table 4.12: SPICE simulation results for stuck-open fault in MOS mn_1 of Fig 4.4

Fault	Fault Resistance MΩ	Width Ratio W_P/W_N	Input Logic V_2	V_3	V_7 Volts	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-7} A
dmn_1	10	7.5/6	5	0	4.998	5	4.999	6.54×10^{-4}
dmn_1	10	7.5/6	5	5	4.478	4.689	4.689	9.66
dmn_1	100	7.5/6	5	5	4.896	4.966	4.966	0.11

** Normal operating current is about 60 pA.

Table 4.13: SPICE simulation results for stuck-open fault in bipolar driver q_1 of Fig 4.3

Fault	Fault Resistance MΩ	Width Ratio W_P/W_N	Input Logic V_1	V_2	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-7} A
eq_1	10	7.5/6	5	5	8.38×10^{-8}	0.263	2.36×10^{-4}
eq_1	10	7.5/6	0	0	4.999	0.5	3.89
eq_1	100	7.5/6	0	0	4.999	0.23	0.42

** Normal operating current is about 30 pA.

Table 4.14: SPICE simulation results for stuck-open fault in bipolar driver qn_1 of Fig 4.4

Fault	Fault Resistance MΩ	Width Ratio W_P/W_N	Input Logic V_2	V_3	V_7 Volts	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-7} A
cqn_1	10	7.5/6	5	5				
cqn_1	10	7.5/6	5	0	4.88	4.999	4.997	1.45
cqn_1	100	7.5/6	5	0	4.88	4.999	4.997	1.43

** Normal operating current is about 60 pA.

Table 4.15: SPICE simulation results for stuck-open fault in bipolar driver q_2 of Fig 4.3

Fault	Fault Resistance MΩ	Width Ratio W_P/W_N	Input Logic V_1	V_2	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-11} A
eq_2	10	7.5/6	5	0	4	4.675	4.95
eq_2	10	7.5/6	5	5	8.4×10^{-8}	4.675	1.96
eq_2	100	7.5/6	5	5	8.4×10^{-8}	4.415	1.94

** Normal operating current is about 30 pA.

Table 4.16: SPICE simulation results for stuck-open fault in bipolar driver qp_1 of Fig 4.4

Fault	Fault Resistance MΩ	Width Ratio W_P/W_N	Input Logic V_2	V_3	V_7 Volts	V_4 Volts	Output V_5 Volts	Power Supply Current $I(V_{DD})$ *10^{-10} A
cqp_1	10	7.5/6	5	0	4.998	5	4.999	0.654
cqp_1	10	7.5/6	5	5	4.2×10^{-3}	0.176	7.15×10^{-3}	8.26
cqp_1	100	7.5/6	5	5	4.2×10^{-3}	0.176	7.15×10^{-3}	8.25

** Normal operating current is about 60 pA.

4. 4. 2 Effects of Device Geometry and Fault Strength:

Change in device geometry has no effect on the output voltage when BiCMOS NAND gates (basic and full swing) are subjected to stuck-open faults in both MOS and bipolar sections of the gates. Fault sensitizing pattern tries to activate only the faulty transistor. But due to fault a very large resistance, compared to it's ON resistance, is inserted between it's faulty node and the node to which it would normally have been connected. As a result change in it's ON resistance due to change in the device geometry can not appreciably change the total circuit resistance and output remains constant.

4.4.3 Comparison with Standard CMOS:

When stuck-open fault in both MOS and bipolar sections of the basic BiCMOS gate (Fig. 4.3) occurs, the circuit shows similar behavior as a faulty conventional CMOS gate. The detection of a single stuck-open fault requires two pattern test and both the circuits behave as a sequential circuit remembering its previous state. However, significant difference is observed when stuck-open fault in bipolar driver of a full swing BiCMOS NAND gate occurs as compared to a stuck-open fault in standard CMOS gate. The auxiliary MOS transistors required to obtain full logic swing than the basic BiCMOS gate completely mask the fault and fault sensitizing pattern produces an output which is same as the output of a fault free circuit.

Chapter 5

Conclusions and Recommendations

5.1 Conclusions

This thesis has examined in detail the performance and testability of BiCMOS logic circuits. Two classes of BiCMOS circuits have been investigated: (i) conventional (or basic) BiCMOS circuits and (ii) low capacitance full-swing BiCMOS circuits.

It has been shown that the BiCMOS circuits in general are much faster than standard CMOS circuits. The speed of basic and full-swing BiCMOS circuits are almost same under various loads except at small loads when the later is slightly faster than the former. The performance figures on full-swing BiCMOS circuits presented in this thesis have not been found in the literature available so far.

Full-swing BiCMOS circuits have a logic swing of full V_{DD} where as the output high logic level in basic BiCMOS circuits can only rise up to (V_{DD} - V_{BE}). Thus, basic BiCMOS circuits suffer from the disadvantage of lower noise immunity compared to standard CMOS. However, the full-swing BiCMOS circuits have the same noise immunity

standard CMOS. However, the full-swing BiCMOS circuits have the same noise immunity as that of standard CMOS. Thus, full-swing BiCMOS circuits would be the best choice compared to basic BiCMOS and standard CMOS circuits as far as speed and noise immunity are concerned. However, both classes of BiCMOS circuits have a higher static power dissipation than standard CMOS. Also, for BiCMOS circuits, the need to fabricate MOS as well as bipolar devices in the same process makes their fabrication more complicated and costlierthan standard CMOS.

The investigations carried out on the behavior of BiCMOS circuits under various single faults have yielded some interesting new results. Although the two classes of BiCMOS circuits considered behave in much the same way as the standard CMOS circuits under single stuck-on faults, their behavior differ under certain single stuck-open faults.

As in standard CMOS, no single stuck-on fault in BiCMOS circuits can be detected by logic monitoring. However, the presence of the fault may be detected by current monitoring. The increment in power supply current in BiCMOS circuits under single stuck-on faults is approximately of the same order as that in standard CMOS.

Most single stuck-open faults in both types of BiCMOS circuits can be detected by logic monitoring using two pattern tests as in standard CMOS. However, in full-swing BiCMOS circuits, the single stuck-open faults in the bipolar drivers are undetectable. When these faults are sensitized the output shows correct logic level due to fault masking

by the MOS devices. Also, the power supply current do not increase. These results indicate that further research is essential to make the full swing BiCMOS circuits testable for all single device faults.

5.2 Recommendations for future work.

As mentioned in the previous section, the stuck-open faults in the bipolar drivers in full-swing BiCMOS circuits are undetectable. It would be a challenging work to modify or redesign the full-swing BiCMOS circuit topology so that the presence of all faults can be detected. That is, designing fully testable BiCMOS logic circuits would be an important direction for future research. Also for detecting the presence of stuck-on faults in BiCMOS circuits through current monitoring, research work can be undertaken toward the design of Built-In Current Sensors (BICS) [27]. Bipolar devices can be used as the current sensors. In a CMOS process, these devices can be laid out as lateral NPN or PNP transistors [27].

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