CALCULATION OF TRAPPED CHARGE IN THE SILICON DIOXIDE LAYER OF AN ENHANCEMENT TYPE MOSFET USING IMPURITY TRAP LEVELS

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(Electrical and Electronic)

by

Syed Saiful Islam

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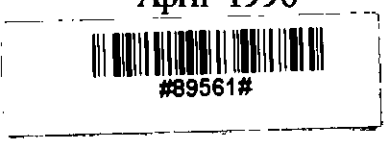

The thesis "CALCULATION OF TRAPPED CHARGE IN THE SILICON DIOXIDE LAYER OF AN ENHANCEMENT TYPE MOSFET USING IMPURITY TRAP LEVELS" submitted by Syed Saiful Islam , Roll No. 921312P, Registration No. 86207, Session 1990-91-92 to the Electrical and Electronic Engineering Department of BUET has been accepted as satisfactory for partial fulfillment of the requirements for the degree of Master of Science in Engineering (Electrical and Electronic).

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CONTENTS

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ABSTRACT

Gate current and trapped charge inside oxide layer of an enhancement type MOSFET are calculated in this work using quantum mechanical analysis. Quantum analysis is important for MOSFETs as their future size shrinks to nanometer range. The effects of the traps due to impurity atoms inside oxide layer on gate current and trapped charge are studied by simulating them with rectangular potential wells and traps are considered to be uniformly distributed. These impurity traps are considered to be vigorous inelastic scatterers and any incident electron is assumed to be inelastically scattered and completely trapped inside a trap-well and then tunnel out to the adjacent traps through the oxide potential barriers. In this thesis the calculation of gate current and trapped charge inside oxide layer are carried out for various MOSFET parameters. The calculations show that both gate current and trapped charge increase with increasing trap density and oxide field. With decreasing energy levels of the trap-wells the trapped charge increases with decreasing gate current. Trapped charge distribution inside various trap-wells are calculated from probability density function. It is found that most of the trapped charge are residing inside trap-wells near the channel. A comparison between calculated and experimentally measured results are presented and they are found to be in good agreement.

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 Background of the thesis

Metal-oxide-semiconductor field-effect transistors (MOSFET) are widely used in very large scale integrated (VLSI) circuit design, where high density and high speed performance are required. This led to a continual device miniaturization [1]. As a result the oxide layer (SiO_2) of the MOSFET became very thin (less than 100 A°). Through this thin oxide layer, tunneling of carriers take place between the semiconductor channel and the metal contact at the gate of the MOSFET [2]. The presence of the impurity atoms in the SiO_2 layer act as a trapping centre for the carriers and therefore affect the tunneling. Due to tunneling, MOSFETs have gate current and charge is trapped inside the thin SiO_2 layer, when switching takes place between ON and OFF states. Therefore the switching speed is reduced and the performance of MOSFETs is degraded. From another point of view, the presence of trapped charge in the gate region gives a new idea of non-volatile memory and multi-stage logic design using MOSFET. As a result the calculation of gate current and trapped charge in the SiO_2 layer have become important to evaluate the performance of MOSFETs.

1.2 General review

In the late 1970s and early 1980s, trap creation inside the thin amorphous film of silicon dioxide has received much attention because of their important effects on carrier tunneling through the oxide layer. In 1976, Woods and Williams [3] measured the properties of trapped holes in the SiO_2 layer by the application of large electric field. They also measured the trapped hole density and their distribution in a SiO_2 layer of thickness 1000-1250 A° neglecting traps due to the impurity atoms. They suggested that traps are created due to the electron missing from the covalent bonds of SiO_2. Later, a theoretical treatments on the process of hot-electron emission from silicon into silicon dioxide was carried out by Ning [4]. He considered avalanche and nonavalanche injection mechanism to calculate emission probability of the carriers at Si-SiO_2 interface. Yambae and Miura [5] observed experimentally the flat-band voltage shift, because of the generation of interface states due to the electron trapping in the SiO_2 film. They suggested that the interface states, where electrons can be trapped, are generated due to the collisions of electrons at the Si-SiO_2 interface.

Trap creation was observed in several experiments during tunneling of carriers through the SiO_2 layer [6,7,8]. Di Maria [6] observed the trap creation in thin films of SiO_2 follows the electron heating characteristics of the material. He observed the generation of electron traps in SiO_2 at fields above 1.5 MV/cm due to the electron heating. In another investigation [8], Di Maria suggested that electrons can travel without scattering through thin (<100A°) oxide layer and traps are not produced unless injected electrons acquire more than 2eV of kinetic energy from the applied electric field. Miki and others [7] observed higher trap density in ultra-dry oxide films than that in wet-oxide films. They suggested the presence of impurity atoms such as Sodium and heavy metals in the oxide films act as trap-states for the tunneling carriers. In an experiment Farmers, and others [9] suggested that the trap creation in SiO_2 due to electron heating is suppressed below 150° K.

Recently Khosru and others [10, 11] found the non uniform distribution of hole traps inside SiO_2 layer. They suggested [10] that most of the trapped holes exist between 2-6 nm from the SiO_2/Si interface. In another investigation [11] they observed that holes are created by ionizing radiation which produce new electronic states at the SiO_2-Si interface resulting in the formation of interface traps. They also found a threshold voltage shift due to the trapping of carriers inside the SiO_2 layer.

In a classical approach Depas and others [2] showed that the direct tunneling current in poly Si/SiO_2 /Si structures with ultra thin gate oxide can be explained by using the effective mass of the tunneling electron. They also measured the gate current density for different oxide layer thickness at different oxide electric field. They found a higher gate current density for thinner oxide layer at low ($\leq$ 8 MV/cm) electric field. In a theoretical approach Mingzhen and others [12] proposed a model based on current continuity concept, for studying the rate of change of inversion layer charge related with tunneling current. They neglected any oxide trap generation at low injected carrier density.

In a recent approach, Kuei-Shan Wen and others [13] proposed a two-dimensional numerical simulation technique to study the effects of hot-electrons on short n-channel MOSFETs. They showed that the generated electron traps at the Si-SiO_2 interface enhance the degradation of MOSFET characteristics but retard the injection probability of hot-electrons into gate oxide. They experimentally measured the gate current at various gate voltage. For a particular gate voltage, they observed different gate current at different drain voltage. Leong and others [14] observed that the high frequency measurement of gate current is different from the low frequency measurement. They also explained the necessity of the high frequency measurement.

1.3 Scope of the work

The effects of impurity atoms inside the SiO_2 layer which act as a trapping centre [7,17] for the tunneling carriers have overlooked in most of the works. But traps due to impurity atoms plays an important role during tunneling. Their property and quantity depend on conditions of the oxidation process, especially on the moisture content in the oxidizing atmosphere. Carrier tunneling through the thin SiO_2 layer with impurity traps are discussed in the present work. Each impurity trap is simulated by a rectangular trap-well inside the SiO_2 layer. Vigorous inelastic scattering is considered and sequential tunneling is assumed from one trap to another. Quantum mechanical analysis is used instead of existing classical and semiclassical analysis for better accuracy. The calculations are based on quantum mechanical wave impedance concept developed by Khondker et al. [18]. Wave functions are calculated inside trap-wells and in the semiconductor channel using S-matrix. Gate current and trapped charge in the SiO_2 layer are then calculated from wave functions.

1.4 Summary of the thesis

In this thesis, the inversion well at the Si-SiO_2 interface is assumed to be triangular at strong inversion. The confinement of the carriers inside this potential well is considered to form a two-dimensional electron-gas (2DEG). The resulting eigen states due to the split of conduction band are calculated using quantum mechanical impedance concept. This is described in chapter-2. An analytical model to calculate transmission coefficient is also developed here.

The analytical expression for gate current and trapped charge are presented in chapter-3. Chapter-3 also contains the calculated gate current and trapped charge for

various MOSFET parameters. A comparison between calculated and experimentally measured gate current is also presented here.

The concluding remarks and recommendations for future work are included in chapter-4 of the thesis.

CHAPTER 2

BASIC MOS STRUCTURE AND QUANTUM EFFECT

2.1 Basic structure of a MOSFET

The basic structure of an n-channel enhancement type metal-oxide-semiconductor field-effect transistor (MOSFET) is illustrated in Fig.2.1. In this device two highly doped n^+ source and drain regions are diffused or implanted into a relatively lightly doped p-type substrate. A thin SiO_2 layer separates the metal gate from the Si surface. Drain current (I_D) -voltage (V_D) characteristics of the device as a function of gate voltage (V_G) [15] of the device is shown in Fig.2.2. No current flows from drain to source without a conducting n-channel between them as the drain-substrate-source combination induces oppositely directed p-n junctions in series. When a positive voltage is applied to the gate with respect to substrate, positive charges are deposited on the gate metal. In response, negative charges are induced in the underlying Si by the formation of depletion region and then the thin surface region contain mobile electrons. This induced negative charges form the channel of the device allow the current to flow from drain to source. With higher gate voltage, the induced electrons in the channel are increased which increases channel conductivity and allows more current for a particular drain voltage.

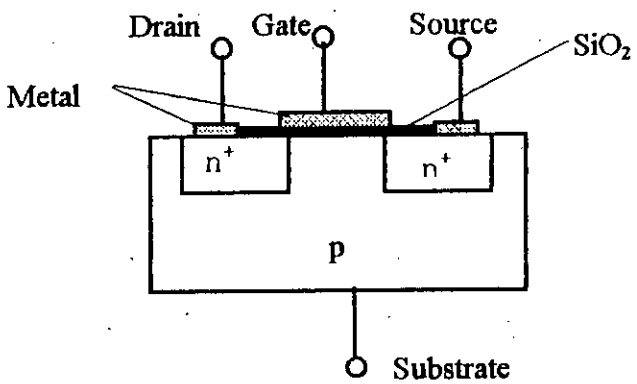

Fig.2.1. An enhancement-type n-channel MOS transistor.

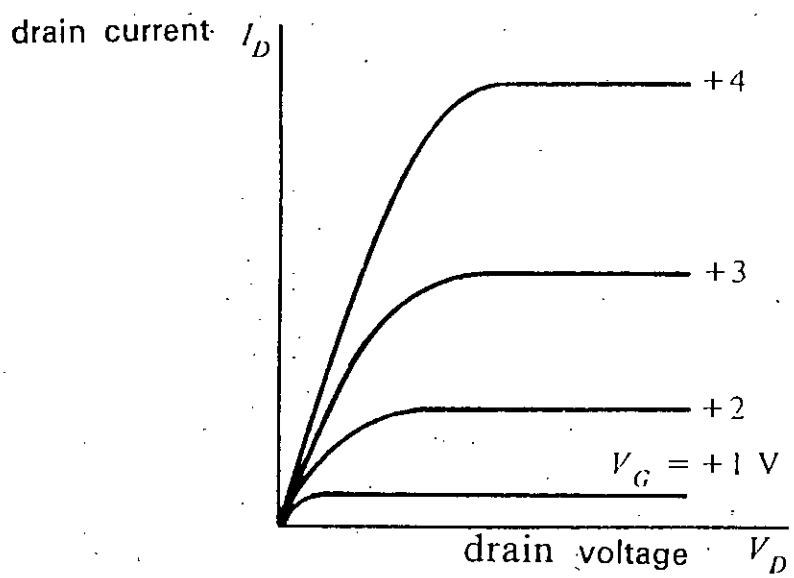

Fig.2.2. Drain current-voltage characteristic as a function of gate voltage of a MOSFET [15].

The energy band diagram of an ideal MOS structure with p-type substrate at equilibrium for zero gate voltage is shown in Fig.2.3. The energy required to move an electron from metal Fermi level to SiO_2 conduction band is the work function for metal-SiO_2 interface ϕ_m and is measured from the metal Fermi level to the SiO_2 conduction band. Similarly, ϕ_S is the work function of SiO_2-Si interface and is measured from the semiconductor Fermi level to the SiO_2 conduction band. In this idealized case, there is no difference between these two work functions that is $\phi_m = \phi_S$, as there is no flow of carriers between metal and semiconductor through the SiO_2 region [15]. The potential ϕ_B measures the position of the semiconductor Fermi level E_F below intrinsic Fermi level E_i and indicates how strongly the semiconductor is doped with p-type impurities. The energy band diagram for n-type substrate under zero gate voltage is shown in Fig. 2.4.

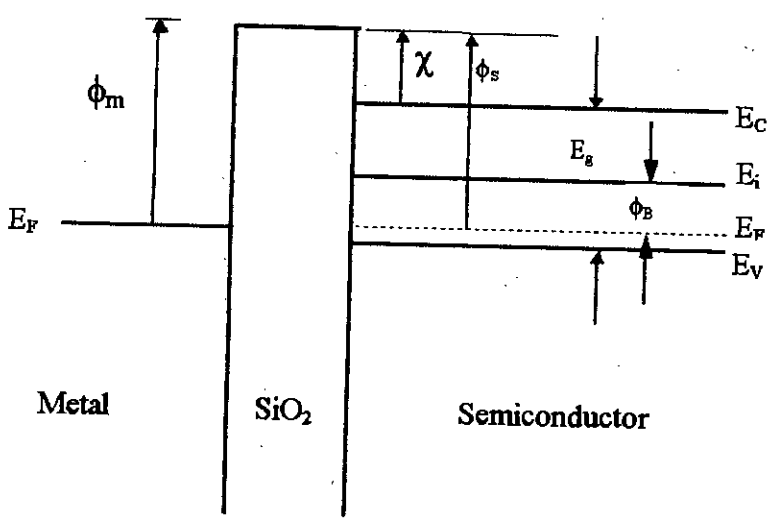

Fig. 2.3. Band diagram with zero gate voltage for p-type substrate.

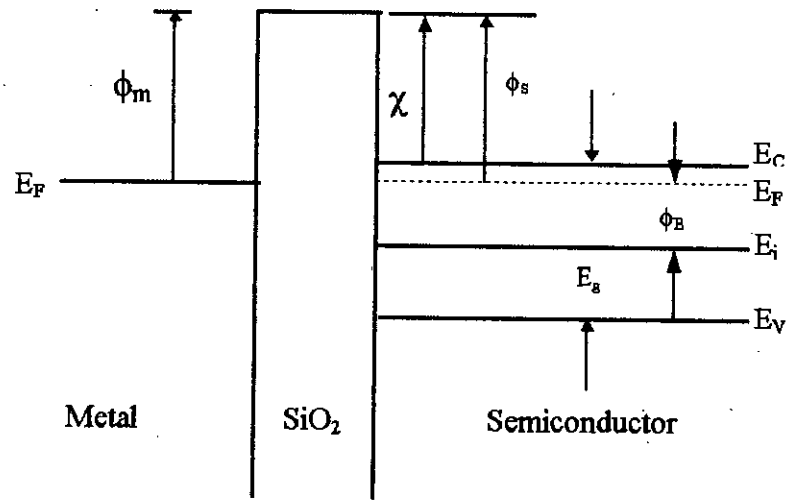

Fig. 2.4. Band diagram with zero gate voltage for n-type substrate.

From above figures, it can be written[16]-

$$\phi_{ms} = \phi_m - \phi_s = \phi_m - (\chi + \frac{E_g}{2} + \phi_B) = 0, \quad \text{for p-type substrate} \tag{2.1}$$

$$\phi_{ms} = \phi_m - \phi_s = \phi_m - (\chi + \frac{E_g}{2} - \phi_B) = 0, \quad \text{for n-type substrate} \tag{2.2}$$

where χ is the semiconductor electron affinity and is measured from semiconductor conduction band to SiO_2 conduction band. E_F, E_c and E_v are Fermi level, conduction band and valence band respectively.

Let us consider an enhancement type MOSFET with p-type semiconductor as substrate as shown in Fig 2.1. When a small positive voltage V is applied to the gate, then the potential of the metal is increased which lowers the metal Fermi level by an amount V

relative to its equilibrium position of Fig.2.3. As a result, oxide conduction band is tilted [15] as shown in Fig.2.5.

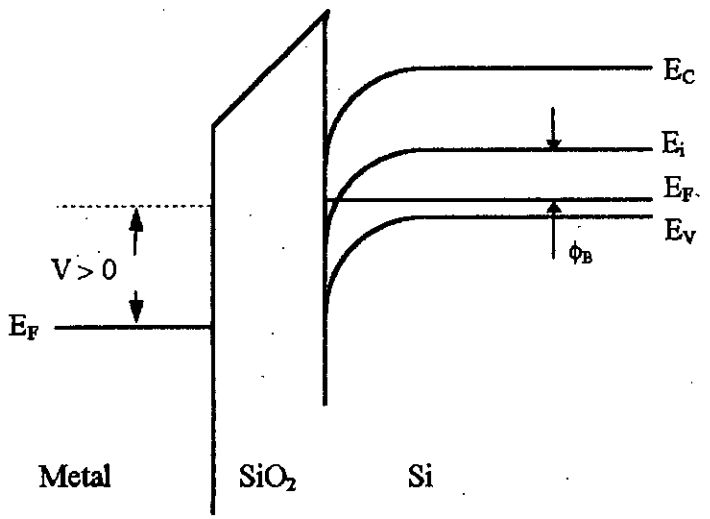

Fig.2.5. Inversion in a MOS structure.

The electron and hole concentration in the semiconductor is given [15] by using Fermi-Dirac distribution function under the assumption-

$$\exp[(E_C - E_F)/kT] >> 1 \quad \text{and} \quad \exp[(E_V - E_F)/kT] << 1 .$$

$$n_p = n_i \exp\{(E_F - E_i)/kT\} \tag{2.3}$$

$$p_p = n_i \exp\{(E_i - E_F)/kT\} \tag{2.4}$$

where n_i is the intrinsic electron concentration , k is the Boltzman's constant and T is the absolute temperature.

The positive gate voltage deposits positive charges on the metal which calls for a corresponding negative charge on the semiconductor surface. Such a negative charge arises from the depletion of the holes from the regions near the surface. As a result, the hole concentration decreases in the depletion region, moving E_i closer to E_F as required by equation (2.4). Therefore E_i band bends downward near the semiconductor surface as shown in Fig. 2.5.

If we continue to increase the positive voltage at the gate, the bands at the semiconductor surface bend more strongly. At a certain gate voltage E_i crosses E_F and this implies that there present a large electron concentration in the semiconductor conduction band, as described in equation (2.3). In this case, the region near the semiconductor surface has conduction properties of n type material. Thus the inversion layer of original p-type semiconductor (substrate) is achieved by the application of positive gate voltage.

The band diagram for Si under strong inversion is shown in Fig.2.6. If we define a potential ψ to give the extent of band bending which is the bending of E_i from its equilibrium of position as shown in Fig.2.6.

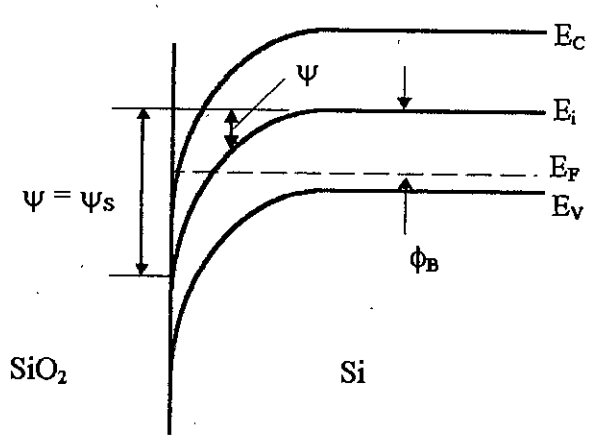

Fig.2.6. Silicon band diagram in a MOS structure under strong inversion.

From equations (2.3) and (2.4) electron and hole concentration in terms of ψ can be written as-

$$n_p = n_{po} e^{\frac{q\psi}{kT}} \tag{2.5}$$

$$p_p = p_{po} e^{-\frac{q\psi}{kT}} \tag{2.6}$$

where n_{po} and p_{po} are the equilibrium electron and hole concentration respectively and ψ is considered positive when bands bend downward. At the Si-SiO_2 interface $\psi = \psi_s$, where ψ_S is the surface potential and strong inversion is defined [15] as $\psi_S = 2.\phi_B$. Then from equations (2.5) and (2.6) electron and hole concentrations at the surface can be written as-

$$n_S = n_{po} e^{\frac{q\psi_s}{kT}} \tag{2.7}$$

$$p_S = p_{po} e^{-\frac{q\psi_s}{kT}} \tag{2.8}$$

2.2 Importance of quantum analysis

Application of positive gate voltage to a n-channel MOSFET, causes band bending and at strong inversion a large number of carriers (electrons for this case) exist inside the channel at Si-SiO_2 interface. Classical and semiclassical analyses are meaningful only at device dimension $\geq 1\mu m$ [23]. But the miniaturization of the electronic devices has resulted

the MOS dimensions of the order of nanometer. As a result oxide layer becomes very thin. So classical or semiclassical analysis does not provide the correct mechanism of gate conduction and the results are not very accurate. In this work, for better accuracy quantum mechanical analysis is used to study the tunneling of the carriers from semiconductor channel to the metal gate through the oxide layer.

2.3 Quantum effects on inversion layer carriers

When a voltage V_g is applied to the gate of an enhancement type MOSFET, partial voltage drop occurs across the insulator, V_i and partially appears as the surface potential ψ_S at the SiO_2-Si interface which causes band bending. Again at zero gate voltage, the metal work function is not exactly equal to that of the semiconductor, therefore a voltage drop is present due to this, which is known as flat-band voltage V_{FB}. Also we have to include the various oxide and interface (SiO_2-Si) charges in an effective positive charges Q_i. The effect of this charge is to induce an equivalent negative charge in the semiconductor. Thus another additional term must be considered in the flat-band voltage [15]. Therefore we can write-

$$V_g = V_i + \psi_S + V_{FB} - \frac{Q_i}{C_i} \tag{2.9}$$

where C_i is the insulator capacitance. With increasing gate voltage both V_i and ψ_S are increased. Higher V_i causes the SiO_2 conduction band to be more tilted and higher ψ_S results further semiconductor band bending and more induced carriers inside the channel.

Strong inversion occurs at $\psi_s \geq 2.\phi_B$ [15] and the resultant band diagram at this condition is shown in Fig.2.6. The combination of higher doping levels and thinner oxide layer increases the electric field at the SiO_2-Si interface to a level such that the energy band bending at the SiO_2-Si interface under strong inversion is very steep. The confinement of the carriers in this potential well leads to a two dimensional electron gas (2DEG) system. As a result, the bulk conduction energy band splits into discrete sub-bands (eigen states) inside the inversion well, with the lowest sub-band shifted substantially above the conduction band minimum. This is illustrated in Fig. 2.7. With increasing gate voltage, surface potential increases and conduction band tip shifts further downward as a result eigen states are also shifted.

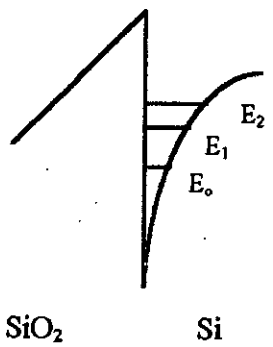

Fig. 2.7. Quantum mechanical effects on inversion layer charge.

2.4 Impurity traps and their simulation using rectangular trap-wells

The presence of impurity atoms in the SiO_2 layer affects the transmission of carriers from the semiconductor channel to the metal. It is seen that many impurities have energy

level close to the SiO_2 conduction band. These impurities form the traps as they serve as an efficient trapping centre for the tunneling carriers [17]. Traps inside thin amorphous films of SiO_2 is currently receiving much attention as it causes performance degradation of MOSFETs in memory and logic circuits. Trap states in SiO_2 films thermally grown on Si substrates have found to be classified by the following three types with respect to their origin: 1) extrinsic trap states related to impurities such as Sodium and heavy metals 2) semi-intrinsic trap states generated by water or Hydrogen related species and 3) intrinsic trap states induced in Si-Si stretched bonds or Oxygen vacancy in SiO_2 [7].

The potential well can affect the transmission and reflection of a carrier in the same way as done by the impurity atoms in the SiO_2 layer. For analysis the effects of a trap on the freedom of motion of the carrier, each impurity atom is simulated with a rectangular potential well as shown in Fig.2.8.

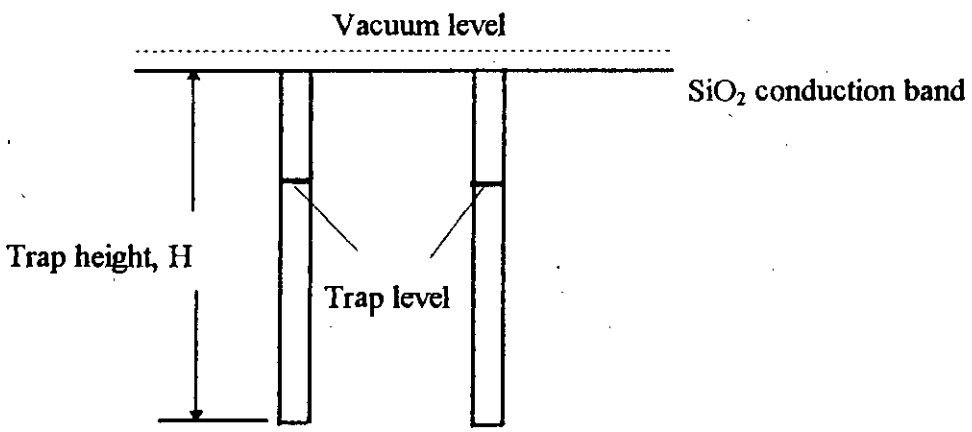

Fig. 2.8. Silicon dioxide layer with rectangular trap-wells.

For SiO_2, band-gap is found to be 8eV and the electron affinity is 0.9eV. Trap level ranges from 1.5eV to 2.5eV below the SiO_2 conduction band [16]. The height of the potential well, H can be calculated by-

$$H = \frac{\pi^2 \hbar^2}{2m^* L^2} + (\text{trap level below } SiO_2 \text{ conduction band}) \qquad (2.10)$$

where m^* is the carriers effective mass and $\hbar$ is the modified Plnak's constant and L is the width of the potential well which is approximately equal to the diameter of the impurity atoms. The diameter of the impurity atoms are of the order of 1-2 A°. In this work, L is considered 2 A°.

The traps are assumed to be vigorous inelastic scatterers and any incident electron is completely trapped inside the well. They then tunnel out to the adjacent traps through the potential barriers.

2.5 Exact solution of Schrodinger's equation: the generalized impedance concept

There exists an analogy between the plane wave and evanescent wave solutions of Schrodinger's equation in a region of constant potential and the waves along a uniform transmission line. Based on this analogy, Khondker et al. [18] have developed a simple and straight forward method of solving the time independent Schrodinger's equation. A quantum mechanical impedance analogous to the impedance in a transmission line has been defined to make use of the well developed theories of transmission line to calculate quantum mechanical transmission probability across an arbitrary potential structure.

The time-independent one-dimensional Schrodinger's equation is given by-

$$\frac{\hbar^2}{2m^*}\frac{d^2\psi}{dx^2} + (E - V)\psi = 0 \qquad (2.11)$$

where ψ is the wave function at any position x, m^* is the effective mass, V is the potential energy at that position and E is the kinetic energy. To put the concept of wave impedance in analytical term let us consider a potential step as shown in Fig.2.9.

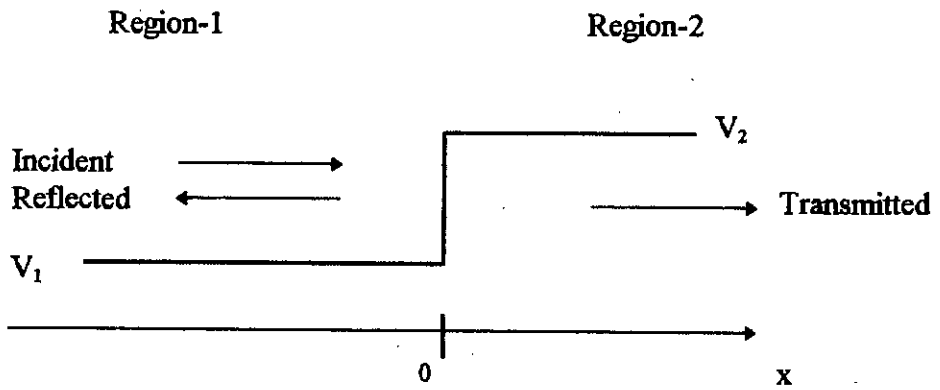

Fig.2.9. Transmission and reflection of electrons from a potential barrier.

Let us assume an electron having an energy E is incident normally from x<0 on the step. Then the wave function ψ of the electron in either region can be written ingeneral as-

$$\psi(x) = A^+[\exp(\gamma x) - \rho \exp(-\gamma x)] \qquad (2.12)$$

where A^+ is the amplitude of the incident wave, ρ is the wave-amplitude reflection coefficient and γ is the propagation constant of the region under consideration. γ for a particular region can be written as-

$$\gamma = \alpha + j\beta = j\sqrt{\frac{2m^*(E - V)}{\hbar^2}} \tag{2.13}$$

where α is the attenuation constant, β is the phase constant, m^* is the effective mass of electrons, V is the potential energy of the region and $\hbar$ is the modified Plank's constant. Region-2 ($x > 0$) is of infinite extent, so there is no reflected wave in this region as shown in the figure and to write the wave function in this region from equation (2.12) second term of the right hand side should be neglected.

Let us now introduce a new function $\phi(x)$, which is obtained from equation (2.12) when differentiated with respect to x and multiplied on both sides by $\frac{2\hbar}{jm^*}$.

$$\phi(x) = \frac{2\hbar}{jm^*}\frac{d\psi}{dx} = A^+ Z_o[\exp(\gamma x) + \rho\exp(-\gamma x)] \tag{2.14}$$

where-

$$Z_o = \frac{2\hbar\gamma}{jm^*} \tag{2.15}$$

The equation for current (I) and voltage (V) in a uniform transmission line with distributed impedance [19] have the form-

$$I(x) = I^+[\exp(\gamma_t x) - \rho_t\exp(-\gamma_t x)] \tag{2.16}$$

and

$$V(x) = I^+ Z_\alpha[\exp(\gamma_t x) + \rho_t\exp(-\gamma_t x)] \tag{2.17}$$

where γ_t is the propagation constant and ρ_t is the wave amplitude reflection coefficient for transmission line. ρ_t is expressed as-

$$\rho_t = \frac{Z_{Lt} - Z_{ot}}{Z_{Lt} + Z_{ot}} \tag{2.18}$$

here Z_{Lt} and Z_{ot} are the load and characteristic impedances of the line [20]. Comparison of equations (2.12) and (2.14) with equations (2.16) and (2.17) shows that ψ and ϕ are analogous to current I and voltage V of a transmission line respectively. Thus Z_o expressed by equation (2.15) can be regarded as a characteristic wave impedance of either region.

To complete the analogy, we must consider the continuity conditions between two regions. At the interface, particle conservation requires the continuity of ψ while the continuity of particle current demands the continuity of $\frac{1}{m^*}\frac{d\psi}{dx}$. These conditions are in direct correspondence to those of transmission lines which require that the total current and voltage must be continuous at any junction between two transmission lines. Again if we apply this boundary conditions to the wave functions in region-1 and region-2 of Fig.2.9. and solve for ρ we get-

$$\rho = \frac{\frac{\gamma_2}{m_2^*} - \frac{\gamma_1}{m_1^*}}{\frac{\gamma_2}{m_2^*} + \frac{\gamma_1}{m_1^*}} \tag{2.19}$$

where γ_1 and γ_2 are the propagation constants, m_1^* and m_2^* are the effective carrier masses in region-1 and region-2 respectively. This equation is analogous to the wave amplitude reflection coefficient of a transmission line expressed in equation (2.18).

To exploit this analogy further, the ratio of ϕ and ψ is considered analogous to the ratio of voltage and current which is the impedance. Therefore at any position x, the quantum mechanical wave impedance is defined as-

$$Z(x) = \frac{\phi(x)}{\psi(x)} \tag{2.20}$$

Once the quantum mechanical wave impedance is defined, the transmission line impedance transformation equation can be used in quantum mechanical problems. Thus the input value of quantum mechanical wave impedance Z_i at a distance $x = -l$ inside region-1 of Fig.2.9 is expressed in terms of quantum mechanical load impedance Z_L of region-1 as-

$$Z_i = Z(-l) = \frac{\phi(-l)}{\psi(-l)} = Z_o \frac{Z_L \cosh(\gamma l) - Z_o \sinh(\gamma l)}{Z_o \cosh(\gamma l) - Z_L \sinh(\gamma l)} \tag{2.21}$$

The load impedance Z_L seen from the first region of Fig.2.9 at $x = 0$ is the input impedance of region-2 at $x = 0$. Therefore Z_L can be expressed using the equation for an infinitely long transmission line-

$$Z_L = \frac{2\gamma\hbar}{jm^*} \tag{2.22}$$

2.6 Calculation of eigen energies of the semiconductor well at strong inversion

The band diagram at strong inversion for an enhancement type MOSFET with p-type substrate is shown in Fig.2.6. The condition for eigen state inside the well can be expressed [21] in terms of quantum mechanical wave impedance by-

$$Z_+ = Z_- \tag{2.23}$$

where Z_- is the impedance seen from the SiO_2-Si interface toward SiO_2 and Z_+ is the impedance at the same position but looking toward substrate.

To calculate eigen states of the well, Z_+ and Z_- are calculated for various electron energies and then compared. At eigen energies these impedances are equal as required by equation (2.23). In this work, the well is assumed to be a triangular one as shown in Fig.2.10 for simple analysis.

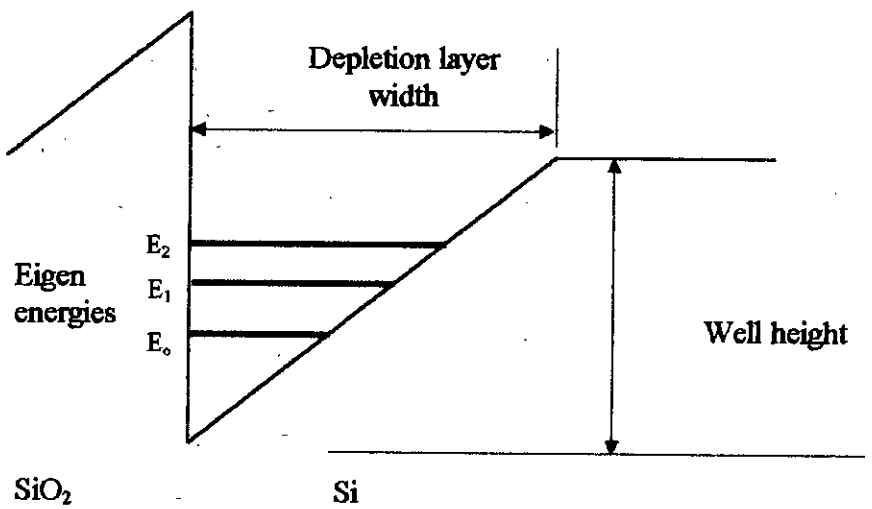

Fig.2.10. Triangular well approximation of the semiconductor well at strong inversion.

Z_+ is then calculated by stepwise approximation of the triangular well as shown in Fig.2.11. Calculation is started from the maximum depletion width and then advanced toward the Si-SiO_2 interface.

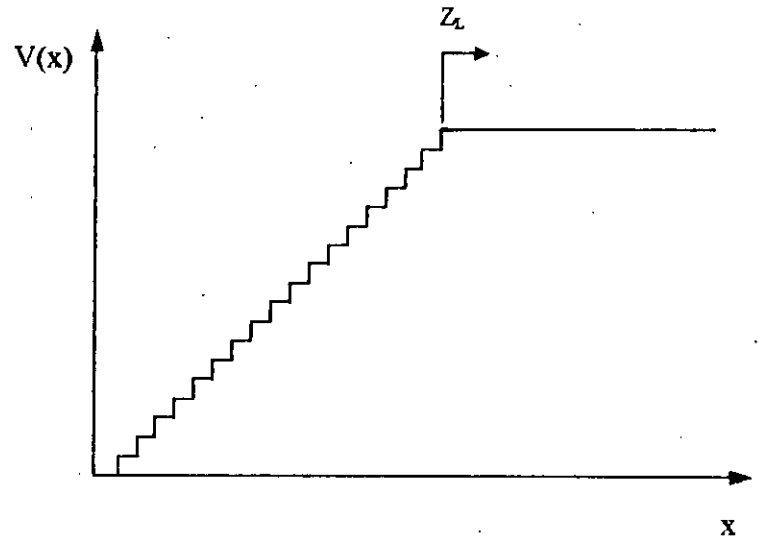

Fig.2.11. Stepwise approximation of the triangular well

Let Z_L be the impedance at the top of the well looking toward substrate for an electron energy E. Using quantum mechanical wave impedance concept which is illustrated in article 2.5, Z_L can be written as-

$$Z_L = \frac{2\gamma\hbar}{jm^*} \tag{2.24}$$

where m^* is the effective carrier mass, $\hbar$ is the modified Plank's constant and γ is the propagation constant, which is expressed as-

$$\gamma = j\sqrt{\frac{2m^*(E - V)}{\hbar^2}} \tag{2.25}$$

where V is the potential energy corresponding to the bulk conduction band. Z_L is assumed as the load impedance of the first step. The input impedance Z_i at the other end of this step is calculated by using the impedance transformation equation which is given by-

$$Z_i = Z_o \frac{Z_L \cosh(\gamma L) - Z_o \sinh(\gamma L)}{Z_o \cosh(\gamma L) - Z_L \sinh(\gamma L)} \tag{2.26}$$

where L is the step length, Z_o is the characteristic impedance and γ is the propagation constant of the step. Both Z_o and γ are calculated from equations (2.24) and (2.25) using potential energy corresponding to the step. Z_i is the load impedance for the second step. Proceeding in this way toward the Si-SiO_2 interface, Z_+ which is the input impedance of the last step is calculated. For the same electron energy, Z_- is calculated from equations (2.24) and (2.25) for a potential energy corresponding to the SiO_2 conduction band at the interface. If Z_+ and Z_- are equal, then E is an eigen energy.

For a depletion layer width of 200 A° with a height of 1eV first, second and third eigen states are found at 0.237eV, 0.41eV and 0.551eV above the channel tip.

2.7 Calculation of current transmission coefficient of the SiO_2 layer with traps

The carrier transport mechanism from the semiconductor channel to the metal gate is illustrated in Fig.2.12. The trap potentials are assumed to be perfectly rectangular. The traps are considered to be vigorous scatterers and inelastically scatter all the incoming electrons. The electrons scattered by the traps are assumed to suffer a transition to the minimum energy level of the trap-well irrespective of the energy of the incoming electrons, but in the actual tunneling not all the electrons do so. The second energy state of the trap-well corresponding to an energy four times greater than the lowest therefore according to the Fermi-Dirac statistics second and other higher states have a negligible probability of being occupied by the tunneling electrons. The trapped electrons from the first trap-well are transmitted to the lower most energy state of the adjacent trap-well and then

sequentially move from one trap-well to another. In this way electrons tunnel toward the metal. At the metal, as its Fermi level is far below the SiO_2 conduction band, the tunneling of electrons from metal toward SiO_2 is neglected.

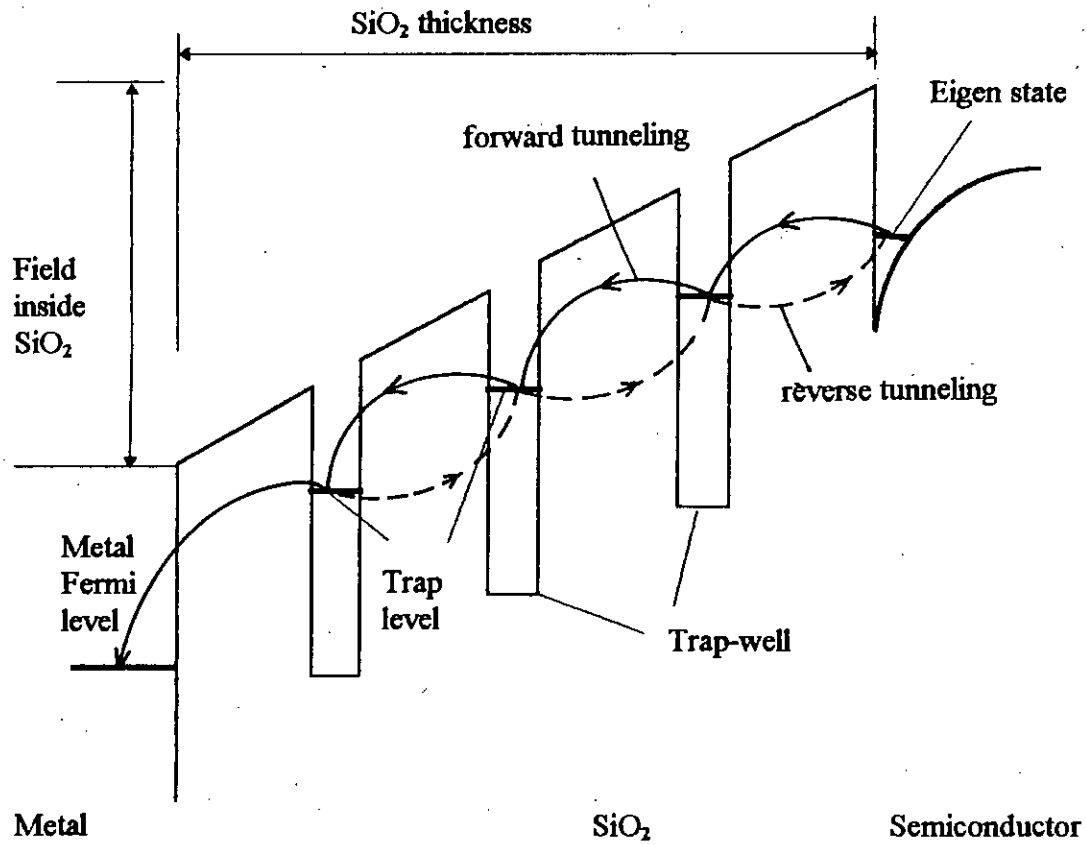

Fig.2.12. Carrier tunneling mechanism through the SiO_2 layer.

For the sake of simplicity let us consider a total number of N traps are uniformly distributed in the SiO_2 region. Therefore electrons have to tunnel through (N+1) SiO_2 barriers between channel and gate. Let us consider a single SiO_2 barrier between trap-well

A and B as shown in Fig.2.13. Let τ be the current transmission coefficient and ρ is the reflection coefficient of the barrier.

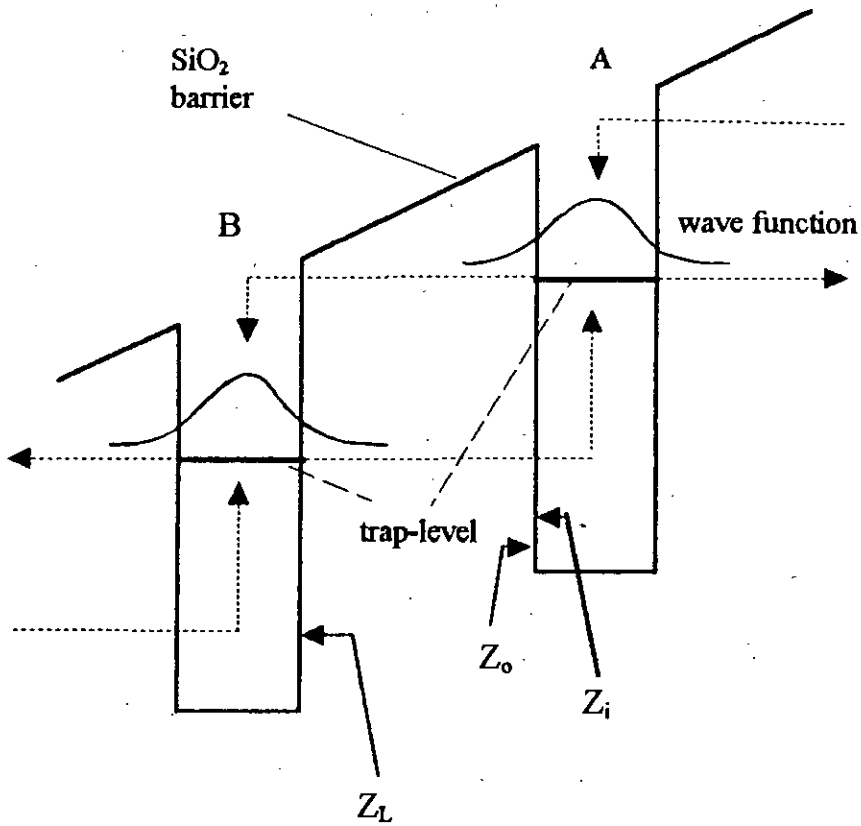

Fig.2.13. A single SiO_2 barrier.

Quantum mechanical wave impedance concept described in article 2.5 can be used to calculate reflection and transmission coefficient. The wave function of an electron inside a trap-well tunnels to the adjacent traps through the SiO_2 barrier on both sides. So there exist both forward and reverse tunneling of electrons between trap-well A and trap-well B through the same SiO_2 barrier. During tunneling from a particular trap-well electrons see the adjacent SiO_2 barrier only. For instance, the forward tunneling of electrons from trap-

well A to trap-well B is not affected by the traps and SiO_2 barriers following trap-well B. Let us consider, during this forward tunneling when an electron cross right side wall of trap-well B from the SiO_2 barrier of Fig.2.13, it passes through an wave impedance Z_L, which is calculated at that position looking toward trap-well B for a potential energy corresponding to the bottom of the trap-well as shown in the figure. Then Z_L can be written as-

$$Z_L = \frac{2\gamma_B \hbar}{jm^*} \tag{2.27}$$

where γ_B is the propagation constant inside trap-well B which can be written as-

$$\gamma_B = j\sqrt{\frac{2m^*(E_{tA} - V_B)}{\hbar^2}} \tag{2.28}$$

here E_{tA} is the energy corresponding to the trap level below SiO_2 conduction band of trap-well A and V_B is the potential energy at the bottom of that trap.

The input impedance Z_i at the other end of the SiO_2 barrier looking toward the barrier from trap-well A can be calculated by considering step approximation of the barrier and then calculating input impedance of each step. Let Z_L is the load impedance of the first step. Then input impedance for any nth step can be written as-

$$Z_{in} = Z_{on}\frac{Z_{Ln}\cosh(\gamma_n L) - Z_{on}\sinh(\gamma_n L)}{Z_{on}\cosh(\gamma_n L) - Z_{Ln}\sinh(\gamma_n L)} \tag{2.29}$$

where Z_{on} is the characteristic impedance, Z_{Ln} is the load impedance and γ_n is the propagation constant of nth step. Characteristic impedance and propagation constant for a particular step can be calculated by using equations (2.27) and (2.28) with V_B replaced by

V_n which is the potential energy of the corresponding step. The input impedance of a particular step is the load impedance for the next step. Proceeding in this way toward the other end of the barrier at trap-well A, Z_i which is the input impedance of the last step can be calculated. Let Z_o is the impedance at the boundary between SiO_2 barrier and trap-well A looking toward the trap for a potential energy corresponding to the bottom of trap-well A as shown in Fig.2.13. Z_o can also be calculated from equations (2.27) and (2.28) using V_A for V_B, where V_A is the potential at the bottom of trap-well A. Then the reflection coefficient of the barrier can be given by-

$$\rho = \frac{Z_i - Z_o}{Z_i + Z_o} \tag{2.30}$$

Therefore the current transmission coefficient can be written as-

$$\tau = 1 - |\rho|^2 \tag{2.31}$$

Finally total current transmission coefficient of the SiO_2 region can be calculated by multiplying transmission coefficients for each SiO_2 barrier between channel and gate.

Considering a 100 A° SiO_2 layer with 1.5 eV of trap levels below SiO_2 conduction band, current transmission coefficient was found to be of the order of 10^{-3}, where the channel eigen energy was taken to 0.237 eV.

CHAPTER 3

CALCULATION OF GATE CURRENT AND TRAPPED CHARGE INSIDE SILICON DIOXIDE LAYER

3.1 Introduction

Wave function at any point inside SiO_2 layer gives the probability of finding carriers at that point. In this work, wave functions are calculated inside each trap-well using S-matrix, assuming vigorous inelastic carrier scattering and a sequential carrier tunneling from one trap-well to another. Gate current and trapped charge inside the SiO_2 layer is then calculated from the wave function. To calculate the carrier concentration inside the channel, two-dimensional density of states (DOS) associated with each eigen state in the semiconductor well at strong inversion is calculated.

In this chapter analytical expression for gate current and trapped charge inside SiO_2 layer is presented. This chapter also contains the calculated gate current and trapped charge for different oxide layer thickness, applied electric field and trap level potentials. A

comparison between calculated and experimentally measured gate current is also presented here.

3.2 Density of states (DOS) for a two dimensional electron gas (2 DEG) system

The confinement of the carriers inside the channel at strong inversion, leads to a two-dimensional electron gas system (2 DEG). As a result, the bulk conduction energy band splits into discrete sub-bands in the semiconductor well. To calculate the carrier concentration of each eigen state using Fermi-Dirac statistics, it is necessary to calculate the density of states associated with each energy state.

Assuming the energy of the bottom of the conduction band to be zero, if $n(\varepsilon)d\varepsilon$ is the number of carriers and $g(\varepsilon)d\varepsilon$ is the number of states whose energy lie between ε and $\varepsilon+d\varepsilon$ then-

$$n(\varepsilon)d\varepsilon = g(\varepsilon)d\varepsilon\, f(\varepsilon) \tag{3.1}$$

where $f(\varepsilon)$ is the Fermi-Dirac distribution function which is given by-

$$f(\varepsilon) = \frac{1}{1+\exp[(\varepsilon-\varepsilon_F)/kT]} \tag{3.2}$$

here ε_F is the Fermi energy, k is the Boltzman's constant and T is the absolute temperature. Then for a two dimensional electron gas system total number of states per unit volume with resultant momentum between p_t and p_t+dp_t is given by-

$$g(p_t)dp_t = \frac{2\pi p_t\, dp_t}{h^2} \tag{3.3}$$

For a carrier with effective mass m* the relation between momentum p_t and energy ε is given by-

$$p_t = \sqrt{2m^*\varepsilon} \tag{3.4}$$

Using equation (3.4), equation (3.3) can be modified as-

$$g(\varepsilon)\,d\varepsilon = \frac{2\pi m^{*}\,d\varepsilon}{h^2} \tag{3.5}$$

Substituting Plank's constant h by modified Plank's constant $\hbar$, where $\hbar = \frac{h}{2\pi}$, in equation (3.5), the expression for density of states can be written as-

$$g(\varepsilon)d\varepsilon = \frac{m^{*}}{2\pi\hbar^2}\,d\varepsilon \tag{3.6}$$

3.3 Probability current density

To illustrate the concept of probability current density associated with tunneling carriers let us consider an one dimensional potential step as shown in Fig.3.1. The carriers incident from region-1 toward region-2 are partially reflected from the interface of the two regions. Region-2 is of infinite extent, so there is no reflected carriers in this region.

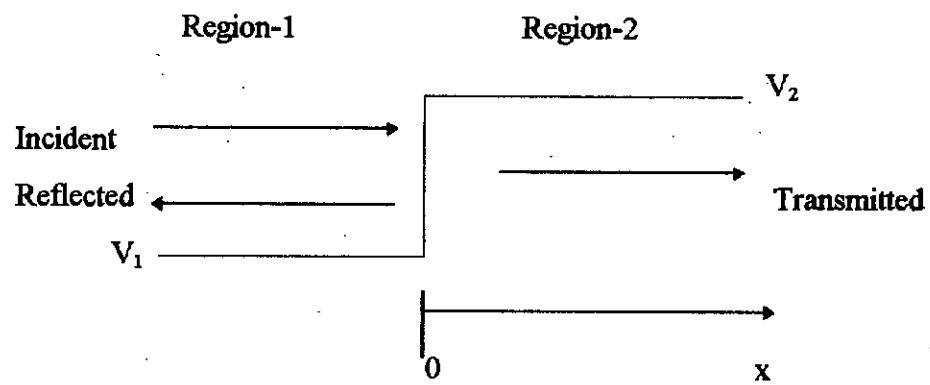

Fig. 3.1. One dimensional potential step.

The wave functions in region-1 and region-2 can be written as-

$$\psi_1(x) = A_1(e^{jk_1x} - \rho e^{-jk_1x}), \quad x<0 \tag{3.7}$$

and

$$\psi_2(x) = A_2 e^{jk_2x}, \quad x>0 \tag{3.8}$$

where A_1 and A_2 are the amplitudes of the incident and transmitted wave in the positive x direction in region-1 and region-2 respectively, ρ is the wave amplitude reflection coefficient at the interface and k_1 , k_2 are the phase constants in region-1 and region-2 respectively. k_1 and k_2 can be expressed as-

$$k_i = \sqrt{\frac{2m_i^*(E - V_i)}{\hbar^2}} \tag{3.9}$$

where m_i^* and V_i (i=1,2) are effective carrier mass and potentials for ith region. Then flow of probability current density [22] is given by-

$$S = \frac{\hbar}{2jm^*}\left[\psi^* \frac{\delta\psi}{\delta x} - \psi\frac{\delta\psi^*}{\delta x}\right] \tag{3.10}$$

where ψ^* is the complex conjugate of ψ. Using plane wave solutions[22] we get-

$$S = \psi(x)\psi^*(x)\frac{k\hbar}{m^*} \tag{3.11}$$

In the above equation $\psi(x)\psi^*(x)$ represents the electron density and $\hbar k$ represents the momentum of the particle. By current continuity relation, the current densities inside region-1 region-2 are equal. These are expressed as-

$$S_1 = |A_1|^2 \frac{\hbar k_1}{m^*}\left[1-|\rho|^2\right], \qquad x<0$$

$$= |A_2|^2 \frac{\hbar k_2}{m^*}, \qquad x>0 \tag{3.12}$$

3.4 Gate current

The carrier transport mechanism from the semiconductor channel to the metal gate and is illustrated in the chapter-2. Various currents due to the tunneling of electrons from channel to the gate with vigorous inelastic scattering inside trap-wells are illustrated in Fig.3.2.

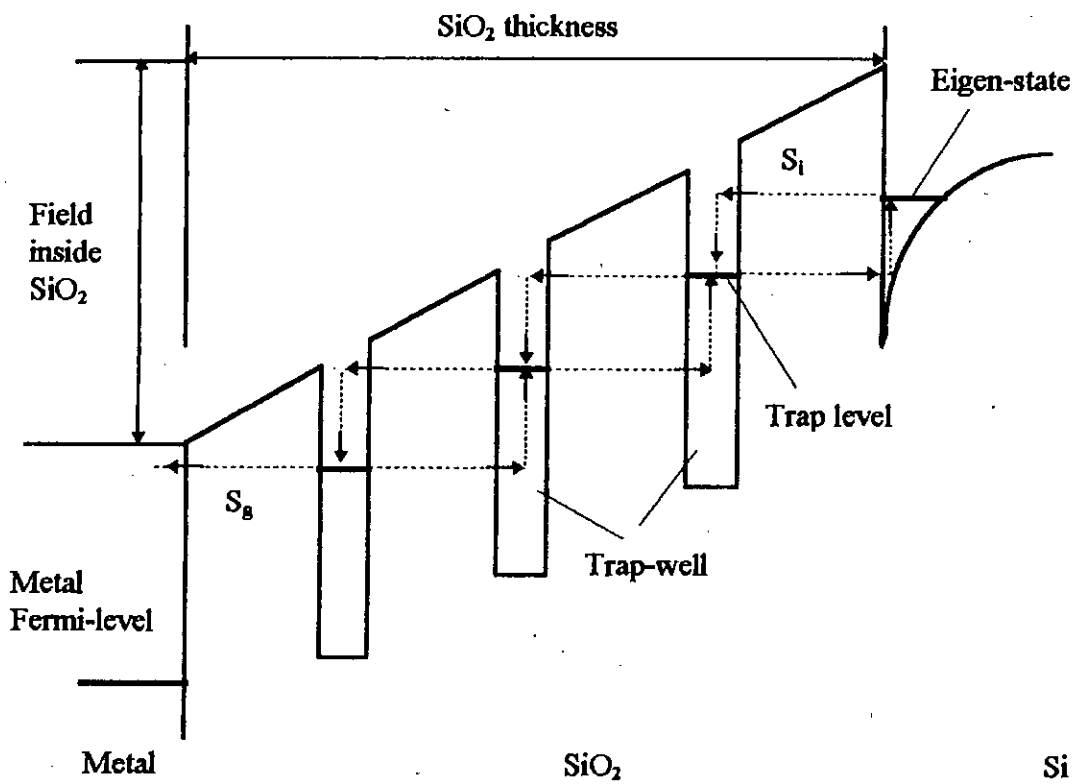

Fig.3.2. Current conduction through SiO_2 region.

Electrons tunneling from channel to the nearest trap-well through the adjacent SiO_2 barrier, suffer a transition to the lower most energy state of that trap-well. The current density due to this forward tunneling is represented by S_l. The wave function of an electron inside a trap-well tunnels in both forward and reverse direction through the adjacent SiO_2 barriers. Therefore there are both forward and reverse current through each SiO_2 barrier. Due to forward tunneling, electrons move sequentially from one trap-well to another and finally reaches the metal gate. As the metal Fermi level is far below the SiO_2 conduction band, the reverse tunneling through last SiO_2 barrier at SiO_2-metal interface is neglected. Therefore in the barrier adjacent to gate metallization, there is no reverse current. The forward current density at the gate is represented by S_g. For the purpose of analysis, let us consider any nth trap-well as shown in Fig.3.3 having wave function ψ_n toward metal and ψ_n' toward semiconductor.

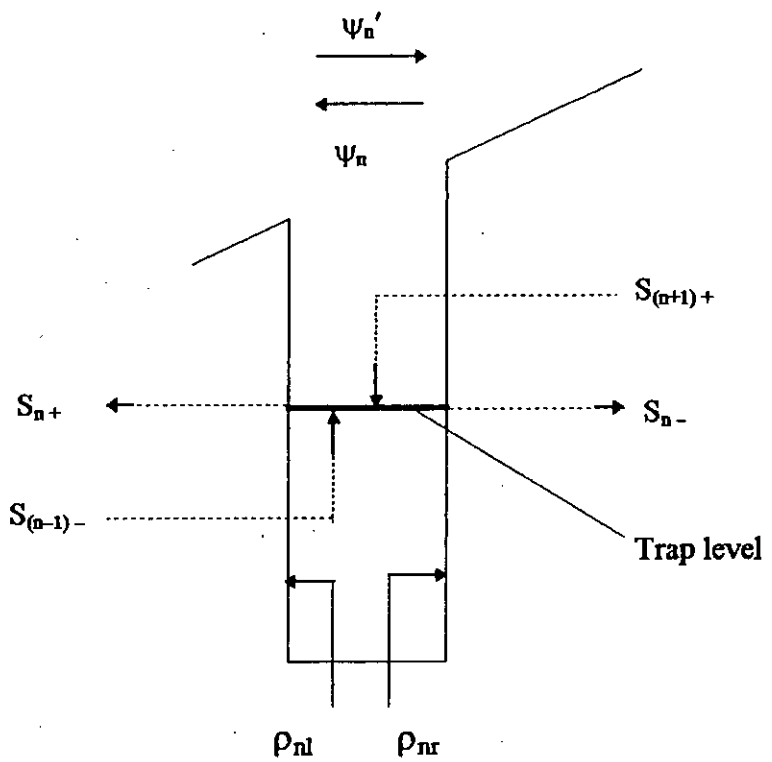

Fig.3.3. Forward and reverse currents associated with a trap-well.

In this analysis, the gate current is calculated from wave function inside trap-wells, which is calculated by using S-matrix. To calculate wave functions, let us start from the trap-well nearest to the metal-gate and then proceed toward the channel. By current continuity relation, in each SiO_2 barrier the algebraic sum of the forward and reverse current is equal to the gate current density, S_g. Therefore from Fig.3.3. we can write-

$$S_g = S_{n+} - S_{(n-1)-} \tag{3.13}$$

Using equation (3.12) we can write-

$$S_g = |\psi_n|^2 \frac{k_n \hbar}{m^*}\left(1-|\rho_{nl}|^2\right) - \left|\psi'_{(n-1)}\right|^2 \frac{k_{(n-1)}\hbar}{m^*}\left(1-|\rho_{(n-1)r}|^2\right) \tag{3.14}$$

solving for $|\psi_n|^2$ we can write-

$$|\psi_n|^2 = S_g \frac{m^*}{k_n \hbar}\frac{1}{\left(1-|\rho_{nl}|^2\right)} + \left|\psi'_{(n-1)r}\right|^2 \frac{k_{(n-1)}}{k_n}\frac{\left(1-|\rho_{(n-1)r}|^2\right)}{\left(1-|\rho_{nl}|^2\right)} \tag{3.15}$$

Now inside nth trap-well current toward semiconductor is equal to the sum of the current due to ψ_n and the reverse current coming from the previous trap-well. Therefore we can write-

$$|\psi'_n|^2 \frac{k_n \hbar}{m^*} = |\psi_n|^2 \frac{k_n \hbar}{m^*}|\rho_{nl}|^2 + \left|\psi'_{(n-1)}\right|^2 \frac{k_{(n-1)}\hbar}{m^*}\left(1-|\rho_{(n-1)r}|^2\right) \tag{3.16}$$

solving for $|\psi_n'|^2$ we can write-

$$|\psi_n'|^2 = |\rho_{nl}|^2 |\psi_n|^2 + |\psi_{(n-1)}'|^2 \frac{k_{(n-1)}}{k_n}\left(1-|\rho_{(n-1)r}|^2\right) \tag{3.17}$$

To calculate actual gate current density, let us first calculate the forward current density S_i at Si-SiO_2 interface from channel to the nearest trap-well for S_g=1.0 using wave functions. Then actual gate current can be calculated by taking ratio with actual S_i which is calculated from the inversion layer electron concentration tunneling toward the SiO_2 region. Inside first trap-well (n=1) which is the nearest of the metal gate, we can calculate both $|\psi_1|^2$ and $|\psi_1'|^2$ for S_g=1.0 from equations (3.15) and (3.17) respectively by using n=1 and neglecting second term of the right hand side of both equations as there is no reverse current in the SiO_2 barrier between the trap-well and the metal gate. Using these values, wave functions inside the following trap-wells are calculated for unit gate current density. Let N is the total number of traps inside SiO_2 layer. Then inside the last trap-well which is nearest to the channel, wave function toward gate is ψ_N and toward channel is ψ_N'. Then S_i for S_g=1.0 can be written as-

$$S_i = 1.0 + |\psi_N'|^2 \frac{\hbar k_N}{m^*}\left(1-|\rho_{Nr}|^2\right) \tag{3.18}$$

where k_N is the propagation constant inside last trap-well and ρ_{Nr} is the reflection coefficient of the SiO_2 barrier at the channel seen from that trap-well. To calculate actual gate current density, let us now calculate actual value of S_i by using concentration of tunneling carriers from channel to the SiO_2 region.

For a particular eigen energy E_o in the channel, electrons move with a velocity corresponds to an energy from E_o to infinity. The electron concentration N_{inv} for the eigen energy E_o, is given by Fermi-Dirac statistics using density of states associated with the eigen state as follows-

$$N_{inv} = \int_{E_o}^{\infty} \frac{m^*}{2\pi\hbar^2} \frac{dE}{1+\exp\{(E-E_F)\,q/kT\}} \tag{3.19}$$

where E_F is the Fermi energy, k is the Boltzman's constant, q is the electronic charge and T is the absolute temperature. Applying easily verifiable formula-

$$\int \frac{dx}{1+\exp(x)} = -\ln\{1+\exp(-x)\} \tag{3.20}$$

we get from equation (3.19)-

$$N_{inv} = \frac{m^*}{2\pi\hbar^2} kT \ln\left[1+\exp\{(E_F-E_o)q/kT\}\right] \tag{3.21}$$

Assuming 50% of the inversion layer electrons tend to move toward the gate, then the actual value of S_i is given by-

$$S_{i(actual)} = \frac{1}{2} N_{inv} \frac{\hbar k}{m^*} \tau \tag{3.22}$$

where τ is the current transmission coefficient of the SiO_2 layer and $\frac{\hbar k}{m^*}$ is the velocity of the electrons. Then the actual gate current density is given by-

$$S_g = \frac{S_{i\,(actual)}}{S_{i\,(for\ S_g=1.0)}} \tag{3.23}$$

which when multiplied by effective gate area gives the actual gate current.

3.5 Trapped charge in SiO_2 layer

Tunneling of electrons from semiconductor channel to the metal gate is described chapter 2. During tunneling, electrons move sequentially from one trap-well to another inside SiO_2 layer. When the device switches to the OFF state, electrons are trapped inside the SiO_2 region. In this calculation of trapped charge, electrons are assumed to be completely trapped inside trap-wells not any other region of the SiO_2 layer. Wave function of an electron inside each trap-well for unit gate current density which is calculated in article 3.4. is used to calculate trapped charge.

Let ψ_n be the wave function of an electron inside any nth trap-well for unit gate current density, L be the trap-well width and x is measured along the width then the integration, $\int_0^L |\psi_n|^2 dx$ gives the probability of finding the electron inside that trap-well. As the electrons are completely trapped inside trap-wells, so the probability of the electron to be trapped inside SiO_2 region when the device switches to the OFF state is given by-

$$\sum_{n=1}^{N} \int_0^L |\psi_n|^2 dx = \sum_{n=1}^{N} |\psi_n|^2 . L \qquad (3.24)$$

where N is the total number of traps and the variation of wave function with x inside a particular trap-well is neglected.

Now let us consider ψ is the wave function of an electron inside channel for unit gate current density, which is calculated from equation (3.12) using current density from channel toward first trap-well as calculated in article 3.4, propagation constant inside

channel for eigen energy E_o, effective mass of electron inside semiconductor and reflection coefficient of the SiO_2 layer looking from channel. Then the probability of finding the electron inside channel is given by-

$$\int_0^w |\psi|^2 . dx$$

where w is the channel width at eigen energy E_o and x is measured along the width. The variation of $|\psi|^2$ at different position of the channel is shown in Fig.3.4.

Thus we have calculated the probability of an electron to be found inside channel and to be trapped inside SiO_2 layer. Therefore the trapped charge density in the SiO_2 layer is given by-

$$Q_t = \frac{\left[\sum_{n=1}^{N} |\psi_n|^2 . L\right] . q . N_{inv}}{\int_0^w |\psi|^2 . dx} \qquad (3.25)$$

where q is the electronic charge and N_{inv} is the inversion layer carrier concentration associated with eigen energy E_o which is calculated in article 3.4.

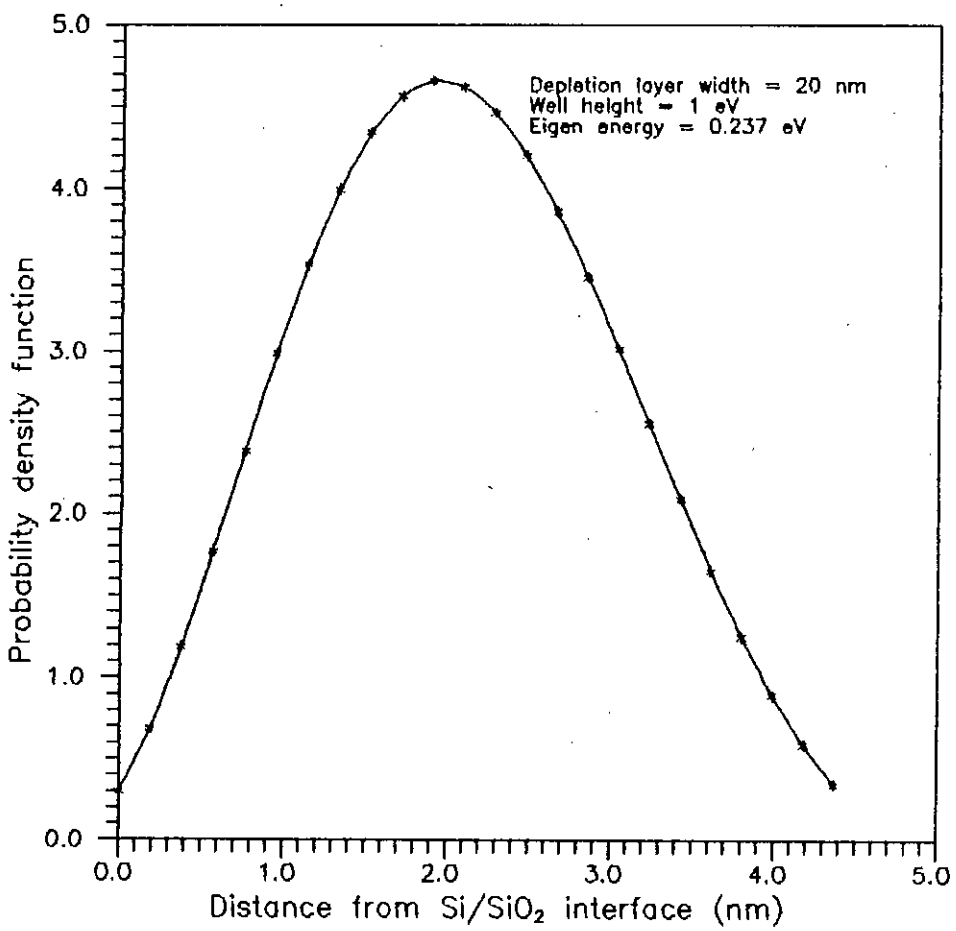

Fig.3.4. Distribution of probability density function at different position inside channel.

3.6 Calculation of gate current and trapped charge inside SiO_2 layer

3.6.1 Effect of trap density variation

Calculation of gate current and trapped charge inside SiO_2 layer for various impurity trap densities are illustrated in figures 3.5, 3.7 and 3.8. In this calculation SiO_2 layer thickness is 10.4nm, effective gate area is $50x10^{-12}$ square metre, field inside SiO_2 is $4.8x10^8$ V/m and trap level is 1.5eV below the SiO_2 conduction band.

The calculated values of gate current are presented in Fig.3.5 which are found of the same order, when compared with the experimentally measured results [12] shown in Fig.3.6 for the same effective gate area. The variation in trapped charge density is shown in Fig.3.7. From these graphs it is seen that with increasing trap density both gate current and trapped charge density increase. With increased trap density, overall inelastic scattering increases and makes the transmission coefficient of the SiO_2 layer higher. Hence both gate current and trapped charge inside SiO_2 layer are increased.

The variation of the probability density function $|\psi|^2$ inside channel and various trap-wells is shown in Fig.3.8. For a given trap density, $|\psi|^2$ inside a particular trap-well is of higher magnitude than that inside adjacent trap-well toward gate. This result is expected as the electrons from channel have to tunnel through a number of potential barriers to reach the metal gate. With increasing trap density, the transmission coefficient of the SiO_2 layer increases and more electrons tunnel through the region and get trapped inside trap-wells. Inside the channel, $|\psi|^2$ is then found to be lower than the corresponding values inside adjacent trap-wells. With lower trap density, $|\psi|^2$ inside channel is higher than that inside trap-wells as the transmission coefficient of the SiO_2 layer then reduced and permits a few electrons to enter from channel.

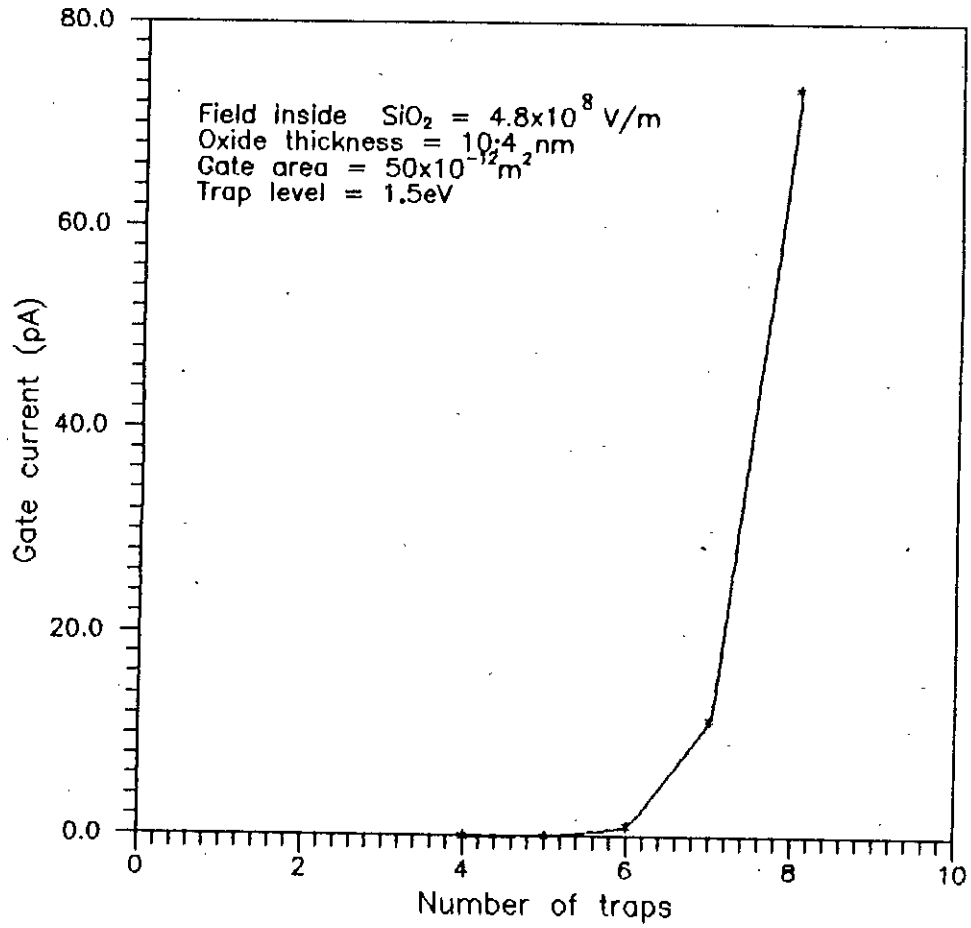

Fig.3.5. Effect of impurity trap density on gate current.

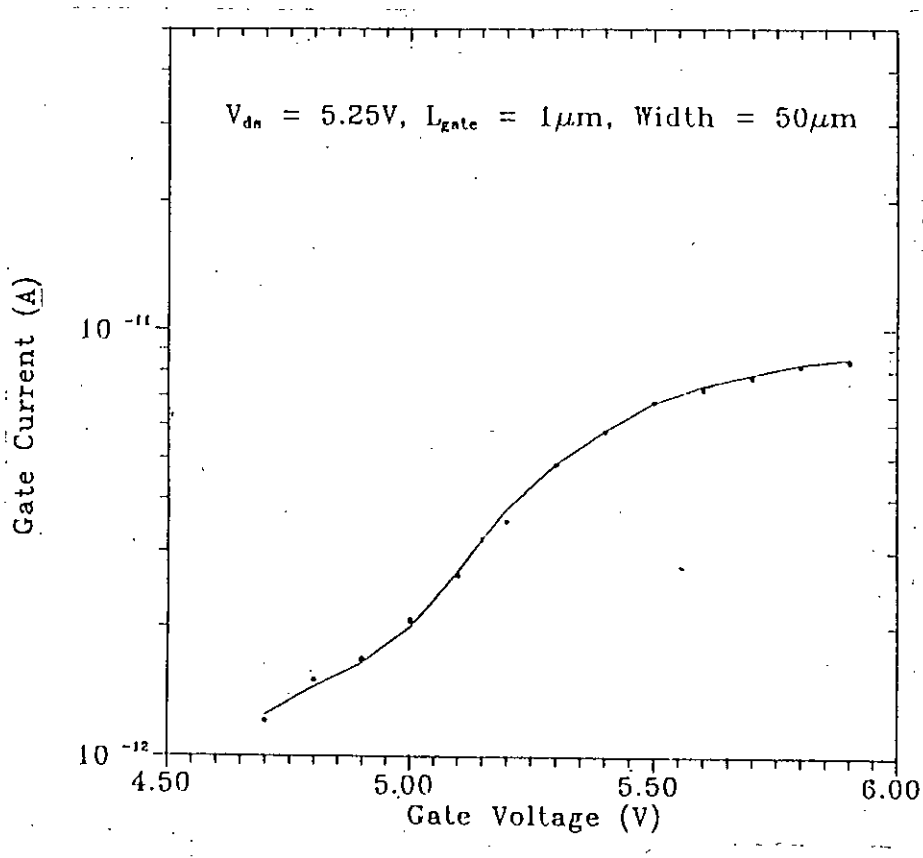

Fig. 3.6. Experimentally measured gate current [12].

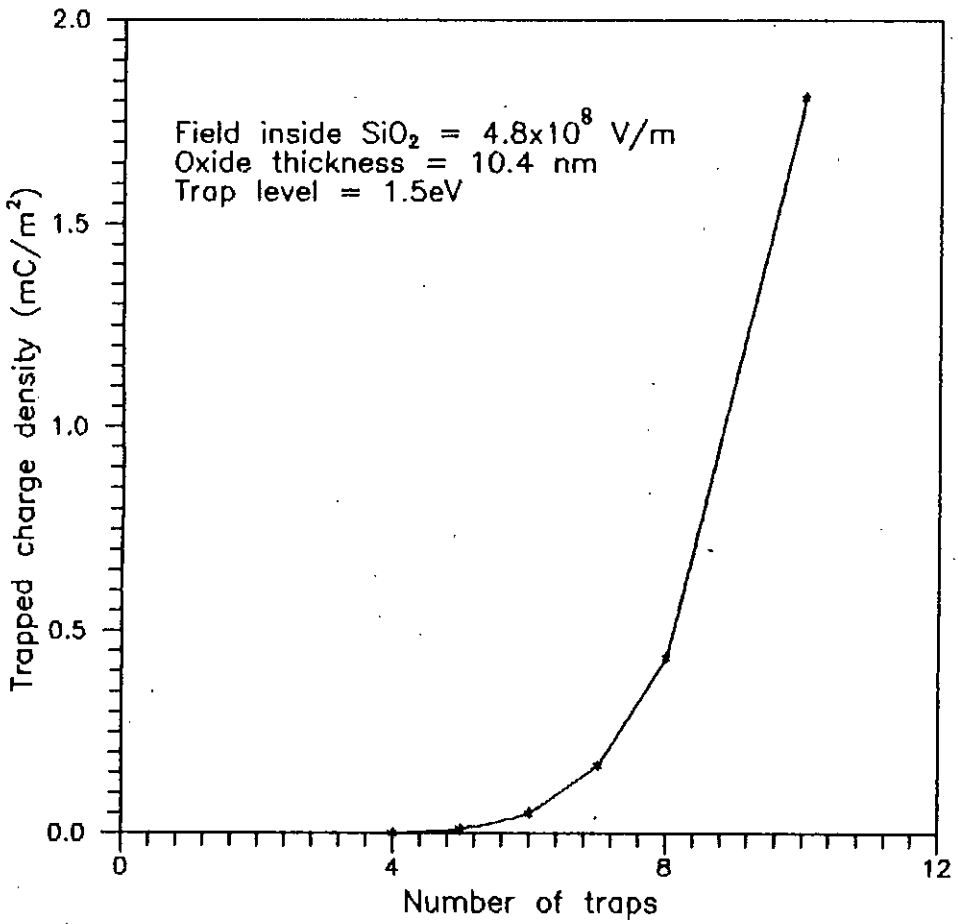

Fig.3.7. Effect of impurity trap density on trapped charge inside SiO_2 layer.

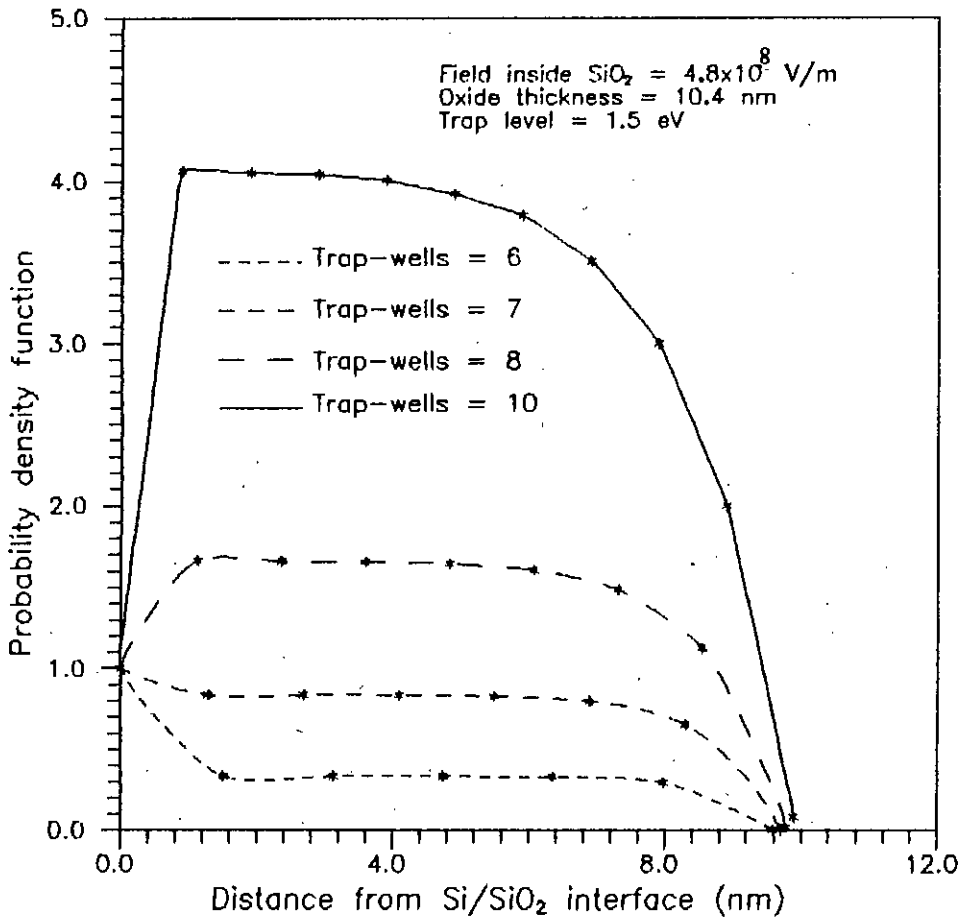

Fig.3.8. Variation of probability density function inside trap-wells and channel with the variation of impurity trap density.

3.6.2 Effect of SiO_2 layer thickness variation

The transmission coefficient of the SiO_2 layer increases when its thickness is reduced. Therefore both the gate current and the trapped charge inside SiO_2 layer increases with reduced SiO_2 thickness. These are observed from their calculated results illustrated in figures 3.9 and 3.10. Here effective gate area is $50x10^{-12}$ square metre, total number of trap-wells inside oxide layer is 8, field inside SiO_2 layer is $4.8x10^8$ V/m and trap level is 1.5eV below SiO_2 conduction band.

The variation of probability density function $|\psi|^2$ inside various trap-wells and channel is shown in Fig.3.11 for various SiO_2 thickness. With reduced thickness, the transmission coefficient of the SiO_2 layer increases and more number of inversion layer electrons enter into the oxide layer and increases the value of $|\psi|^2$ inside the nearest trap-wells. With increasing oxide layer thickness less electrons can enter into the oxide layer and fewer electrons are trapped inside a particular trap-well, indicated by lower values of $|\psi|^2$.

3.6.3 Effect of oxide field variation

Figures 3.12, 3.13 and 3.14 illustrate the results of the calculation of gate current and trapped charge inside SiO_2 layer for various oxide fields. In this calculation, oxide layer thickness is 10.4nm, total number of trap-wells inside oxide layer is 8 and trap level is 1.5eV below SiO_2 conduction band.

Fig.3.12 shows the variation of gate current, for an effective gate area of $50x10^{-12}$ square metre. The variation of trapped charge density is presented in Fig.3.13. With increased field inside oxide layer the slope of the conduction band bending become higher, which increases the transmission coefficient of the SiO_2 layer. As a result, both gate current and trapped charge are increased.

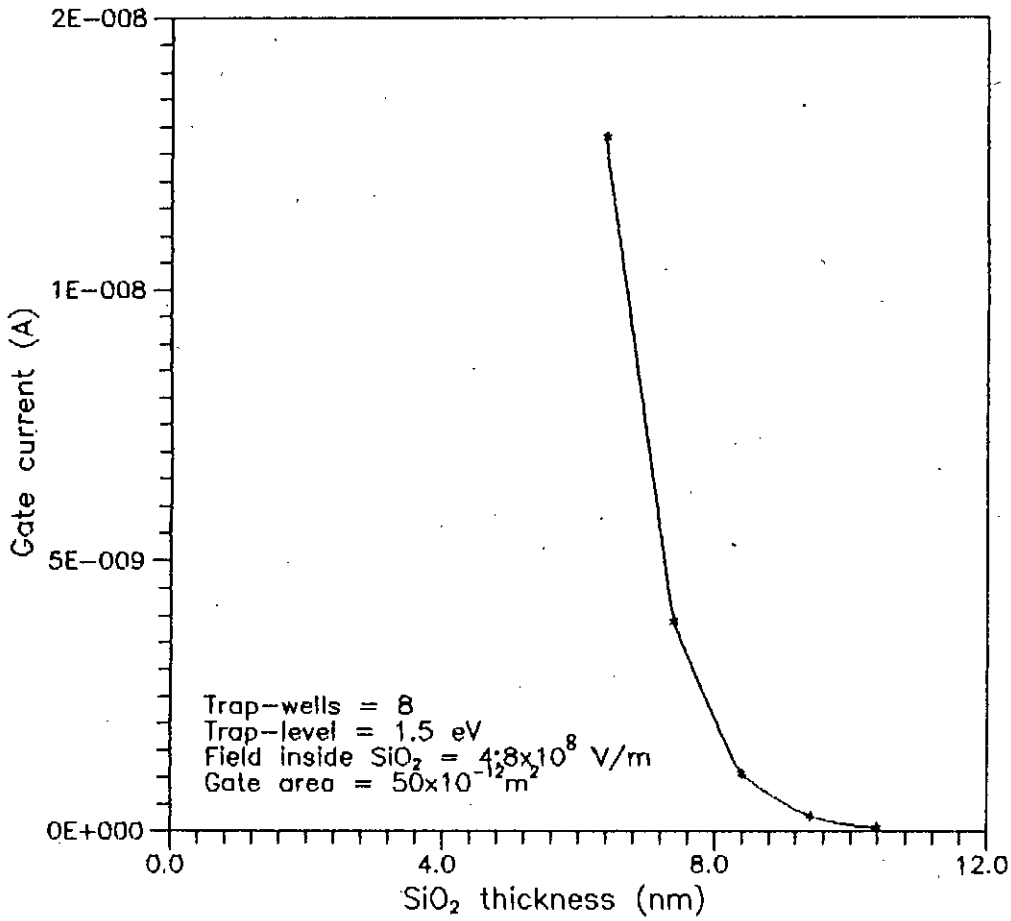

Fig.3.9. Effect of SiO_2 thickness variation on gate current.

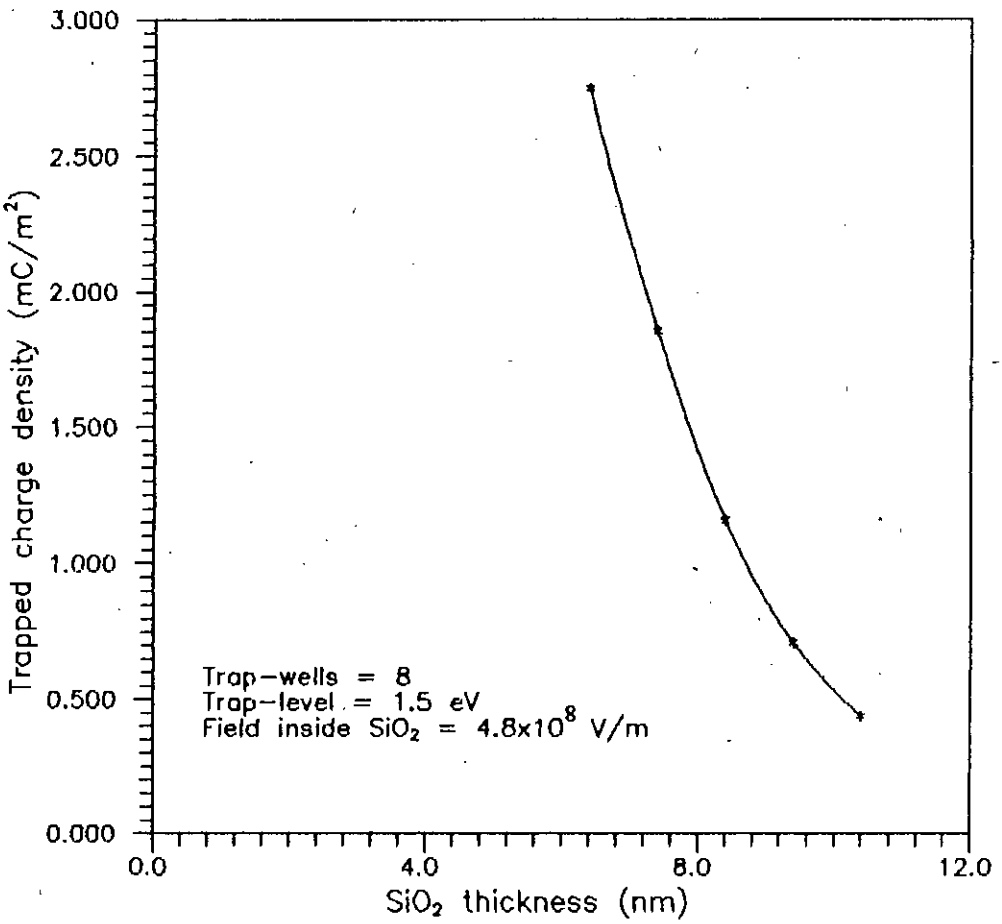

Fig.3.10. Effect of SiO_2 thickness variation on trapped charge.

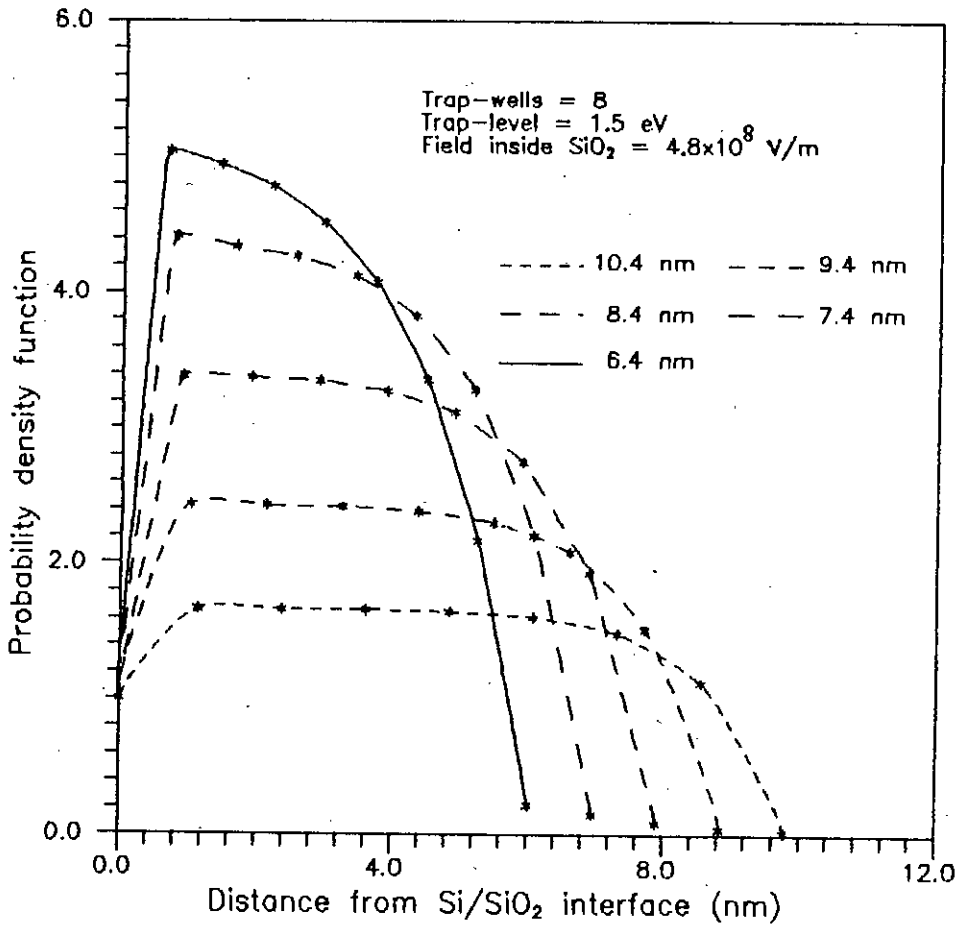

Fig.3.11. Variation of probability density function inside channel and trap–wells with SiO_2 thickness.

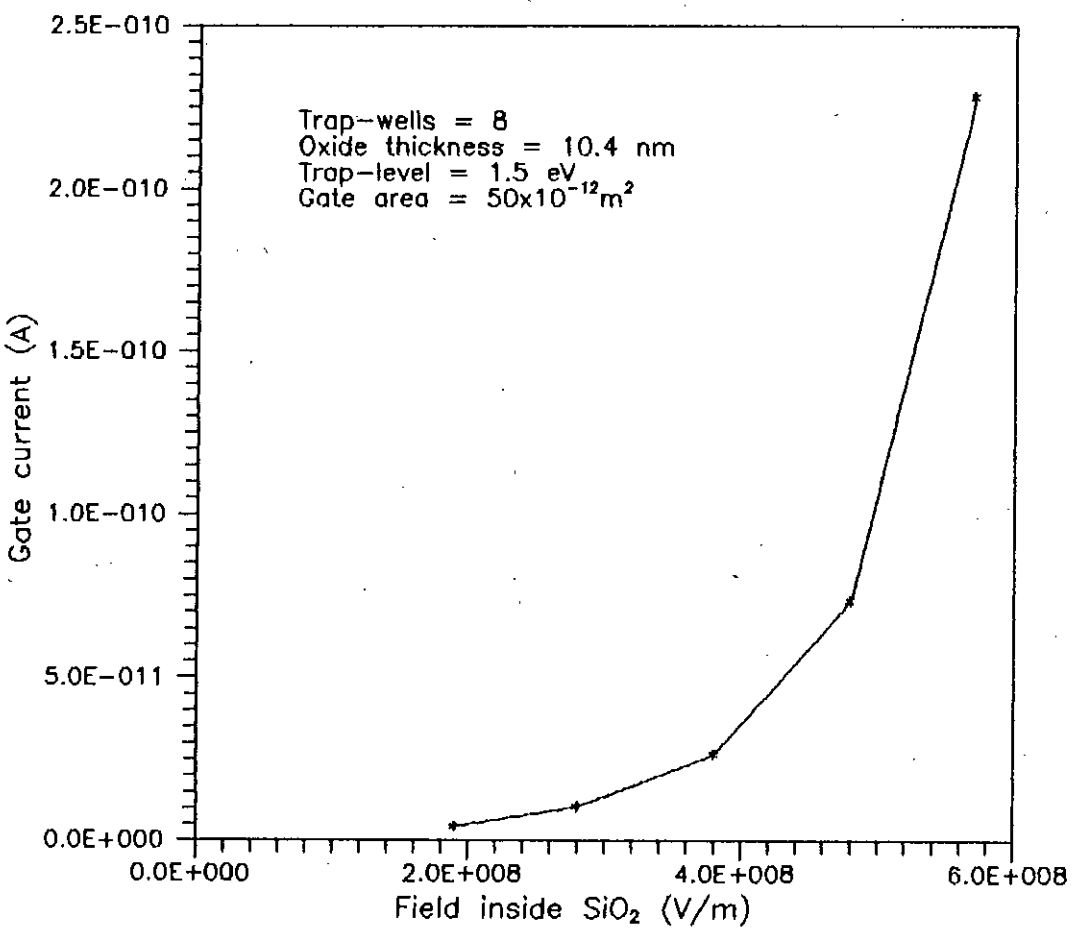

Fig.3.12. Effect of oxide field variation on gate current.

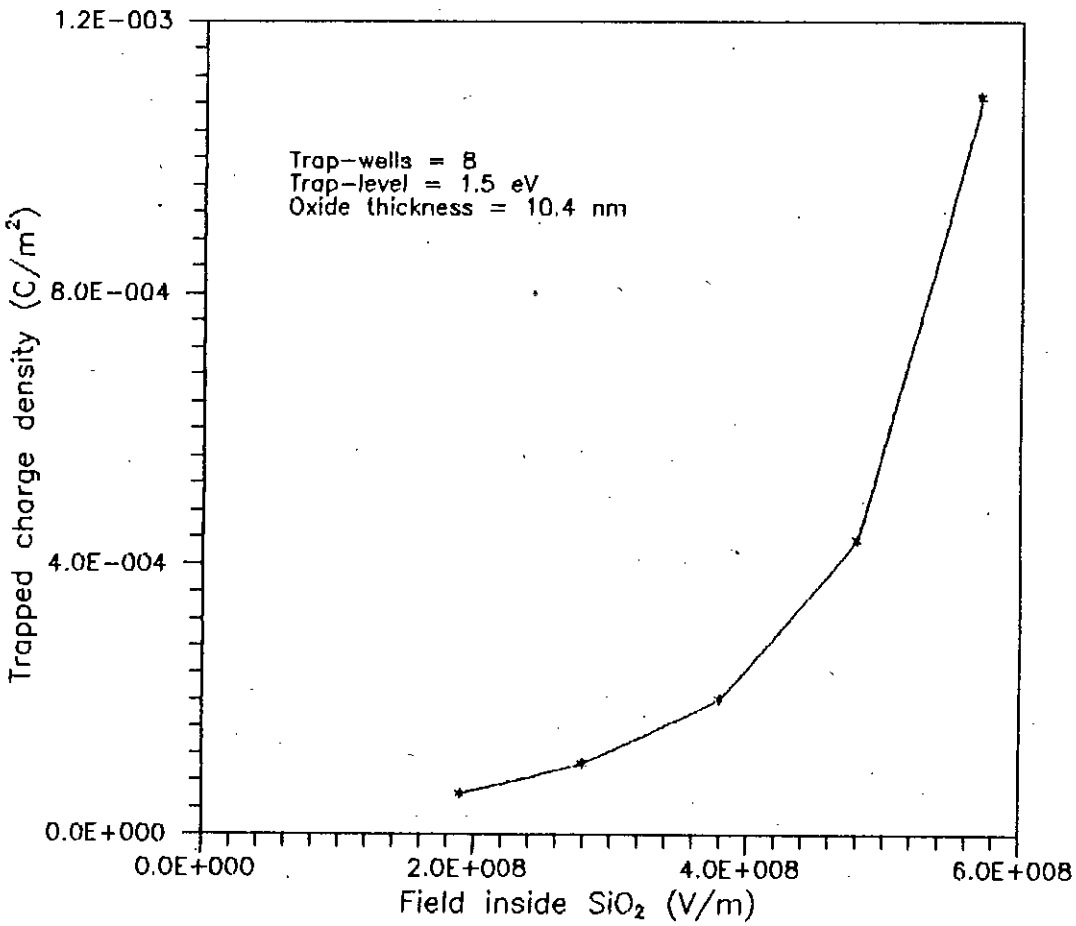

Fig.3.13. Effect of oxide field variation on trapped charge.

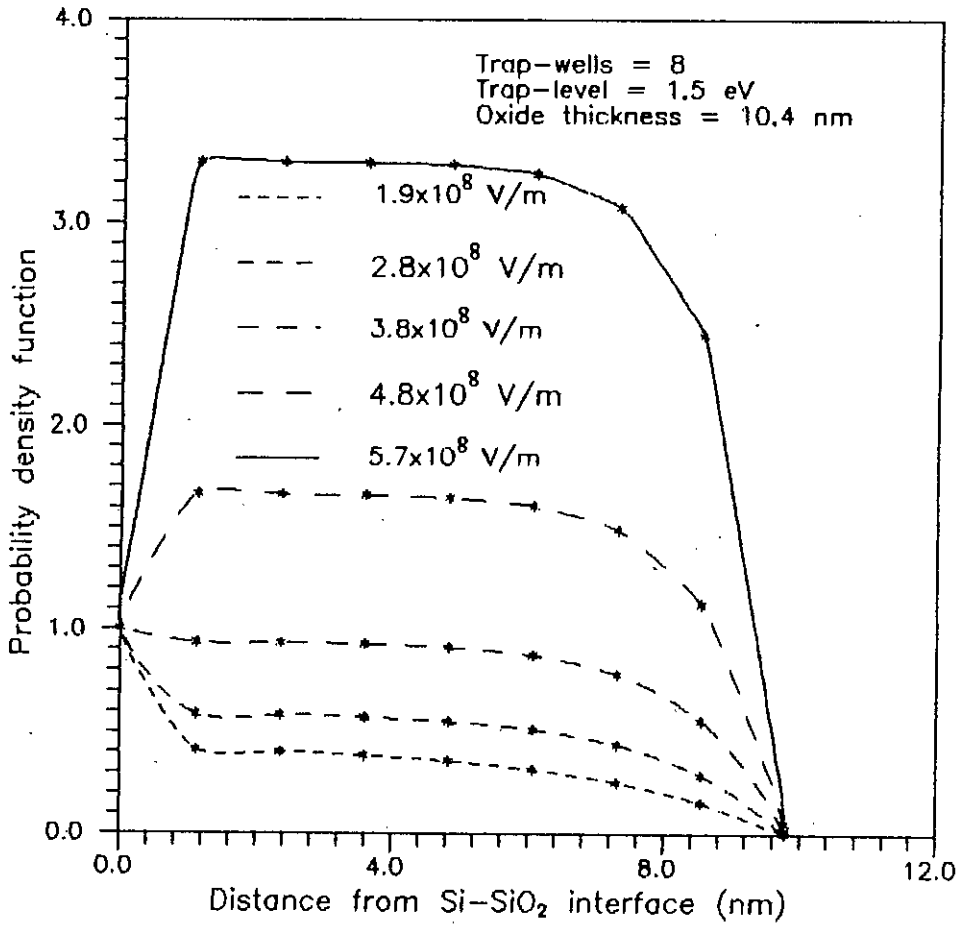

Fig.3.14. Variation of probability density function inside channel and trap-wells with the voriation of field inside SiO_2.

Fig.3.14 shows the variation of probability density function $|\psi|^2$ inside channel and various trap-wells, for different oxide fields. For lower oxide fields, transmission coefficient of the SiO_2 layer decreases and most of the electrons are residing inside the channel instead of tunneling through the oxide layer to the gate. Therefore $|\psi|^2$ inside channel is higher than that inside trap-wells. But with higher fields, $|\psi|^2$ inside adjacent trap-wells increase due to the increased transmission coefficient of the oxide layer. Hence, more electrons are trapped inside the trap-wells.

3.6.4 Effect of trap level variation

The effects of the variation of trap level below SiO_2 conduction band on the results of the calculation of gate current and trapped charge are illustrated in figures 3.15, 3.16 and 3.17. The calculation is carried out for a MOSFET with effective gate area of $50x10^{-12}$ square metre, oxide layer thickness of 10.4nm, total number of trap-wells inside oxide layer of 8 and for a field inside SiO_2 layer of $4.8x10^8$ V/m.

With decreasing trap levels transmission coefficient of the SiO_2 barriers in between trap-wells is decreased. Therefore the inversion layer electrons, entering the oxide layer on its way to the gate, have to tunnel through a number of SiO_2 barriers in between trap-wells with lower transmission coefficient. As a result, the trapped charge density is then increasing with decreased gate current, as seen from graphs shown in figures 3.15 and 3.16.

The variation of probability density function $|\psi|^2$ inside various trap-wells and channel is shown in Fig.3.17. With decreased trap level, electrons inside a particular trap-well have to tunnel through the adjacent SiO_2 barriers with lower transmission coefficient and reside for a longer time inside the trap-well. Therefore more carriers are trapped inside trap-wells resulting higher trapped charge density and increased $|\psi|^2$ inside trap-wells.

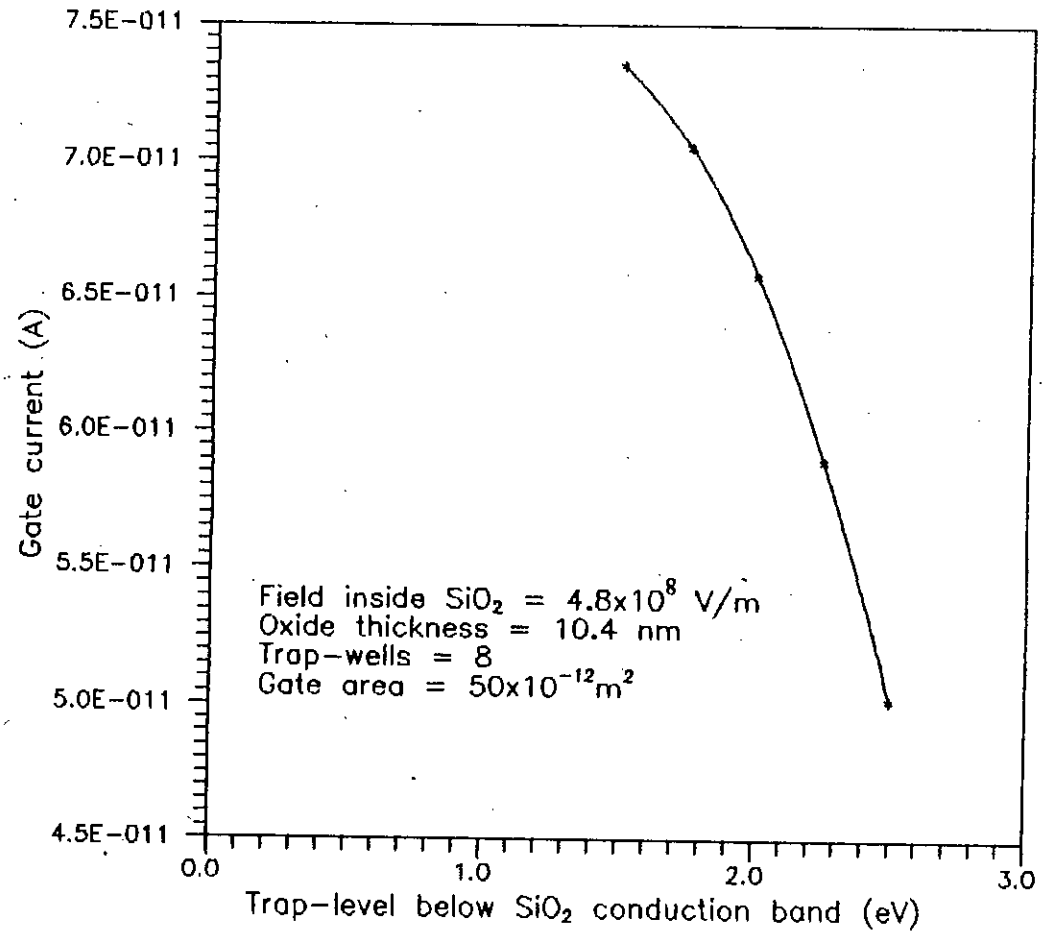

Fig.3.15. Effect of trap level variation on gate current.

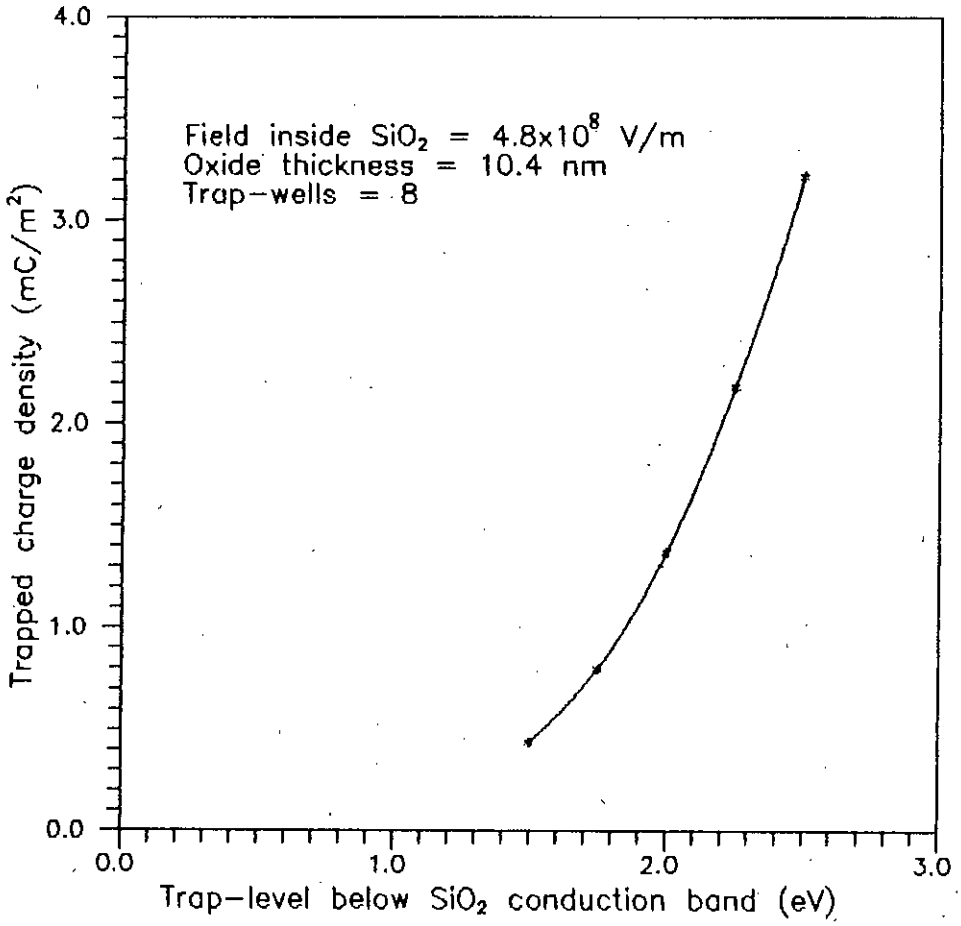

Fig.3.16. Effect of trap level variation on trapped charge.

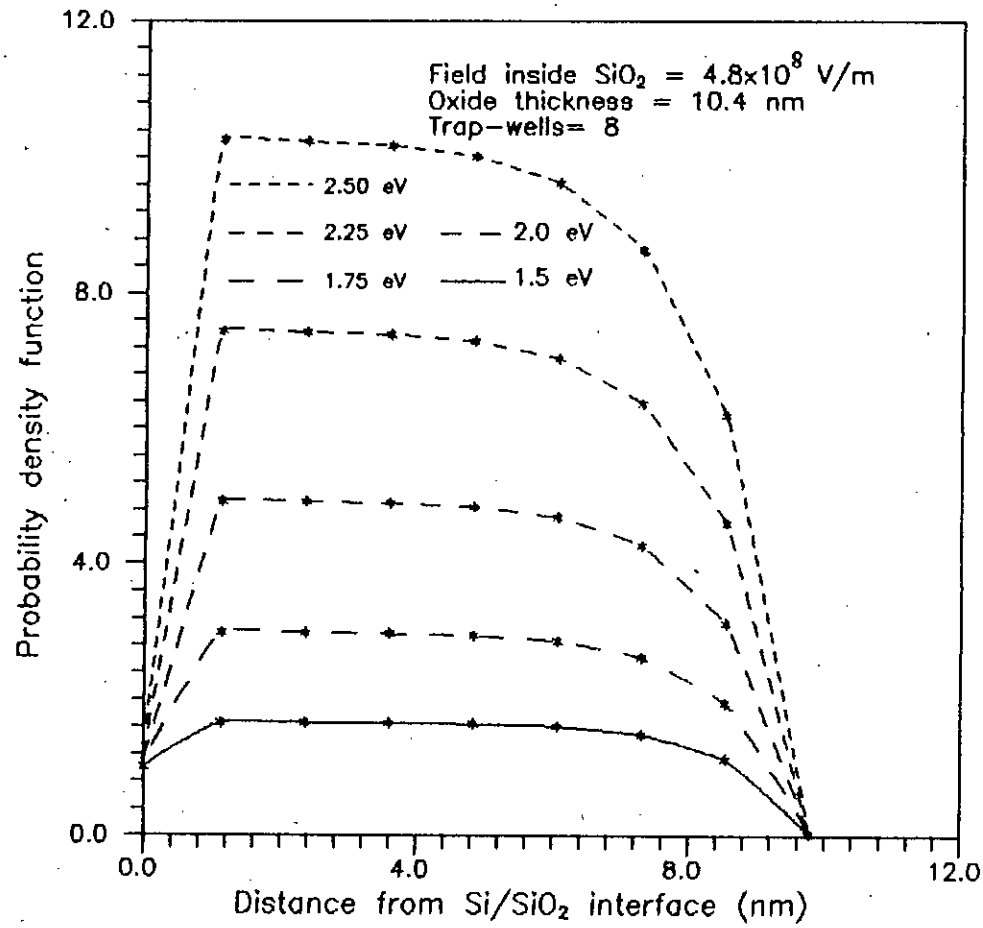

Fig.3.17. Variation of probability density function inside channel and trap-wells with the variation of trap-level below SiO_2 conduction band.

CHAPTER 4

CONCLUSION

4.1 Discussion

The calculation of gate current and trapped charge inside SiO_2 layer of a low dimensional enhancement type MOSFET based on quantum-mechanical analysis is presented in this work. The quantum mechanical analysis is used for better accuracy over classical and semiclassical analysis for decreased device dimensions. The presence of the impurity atoms inside SiO_2 layer, which is neglected in most of the previous work, is considered in this work. The effects of the impurity atoms on the tunneling electrons are studied by simulating them with rectangular potential wells. The traps due to impurity atoms are assumed to be uniformly distributed inside SiO_2 region. In this work traps are considered as vigorous inelastic scatterers and any incident electron inside a trap-well is assumed to suffer a transition in energy corresponding to the lower most energy state of the trap-well. Furthermore any incident electron is assumed to be completely trapped inside a trap-well and then tunnel out to the adjacent traps through the SiO_2 barriers. Eigen energies inside semiconductor channel at strong inversion are calculated by considering it a triangular well.

With this assumptions gate current and trapped charge inside SiO_2 layer are calculated for various MOSFET parameters. The effects of the variation of oxide field,

impurity trap density, SiO_2 thickness and trap level are presented graphically. With increasing trap density or oxide field, transmission coefficient of the SiO_2 layer increases and both gate current and trapped charge are increased. Similar results are obtained with decreasing SiO_2 thickness. The probability density function inside trap-wells and channel are calculated, from which the distribution of trapped charge inside various traps are found. Most of the trapped charge are observed inside trap-wells near the channel. The results of the calculations are found of the same order as the experimentally measured values for similar device dimensions.

4.2 Limitations

In the present analysis rectangular trap-wells are assumed. Hence, this is not the exact potential distribution of a trap. Instead, the potential distribution is much more complicated which makes mathematical calculations more difficult. Again traps due to impurity atoms are randomly distributed inside oxide layer instead of being uniformly distributed which is assumed in this work. Another limitation is the assumption of vigorous scattering of the electrons inside trap-wells. The scattering is assumed to be extremely vigorous so that no electron can get through a trap without changing its energy state. These assumptions were made to make the analysis simple, which can give a quick insight to the actual mechanism of electron transport inside SiO_2.

4.3 Suggestions for future work

Traps are to be simulated by actual trap-wells, which can represent the actual potential distribution of the impurity atoms. Then the mathematical calculations will

become more complicated, but we can expect more accurate results. Gate current and trapped charge can be calculated for actual distribution of the trap-wells by using statistical analysis. In this analysis, calculations will be done for a number of times. In each time the positions of the trap-wells will be randomly generated. Then actual results are to be obtained by taking statistical average of the calculated values. The limitations due to the assumption of vigorous scattering of the tunneling electrons can be solved by using imaginary potentials inside the oxide layer. The limitation of using imaginary potentials is that then the wave function will be dissipating in nature. But, more accurate results are then expected with less mathematical complications.

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