A Quantum Mechanical Modeling of Post Soft Breakdown Conduction Through Ultrathin Gate Oxide MOS Devices

by

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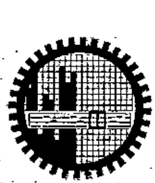

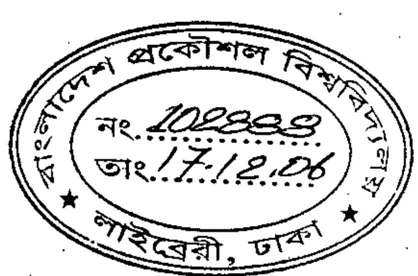

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The thesis titled "**A Quantum Mechanical Modeling of Post Soft Breakdown Conduction Through Ultrathin Gate Oxide MOS Devices**", submitted by Muhammad Qazi, Roll No: 040406215 P, Session: April 2004 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of Master of Science in Electrical and Electronic Engineering on July 30, 2006.

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DEDICATION

To my Parents

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ABBREVIATIONS

DT	Direct Tunneling
FN	Fowler-Nordheim
HBD	Hard Break Down
MOSFET	Metal Oxide Field Effect Transistor
QBD	Quasi Break Down
QMTC	Quantum Mechanical Transmission Co-efficient
QMWI	Quantum Mechanical Wave Impedance
QPC	Quantum Point Contact
RTS	Random Telegraph Signal
SBD	Soft Break Down
SHEI	Substrate Hot Electron Injection
TAT	Trap Assisted Tunneling
TDDB	Time Dependent Dielectric Breakdown
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration
VRH	Variable Range Hopping
WKB	Wentzel-Kramer-Brillouin

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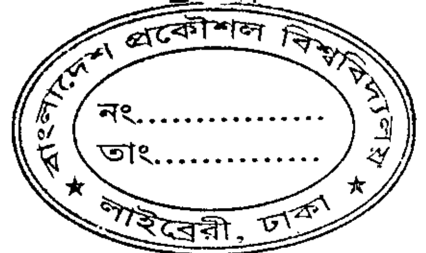
ABSTRACT

The apparently never ending progress of VLSI technology has scaled the MOS devices down to limiting sizes and reduced the gate oxide thickness to tunneling regime. For such thickness reliability of oxide has become a major concern. Recently a new failure mode of ultra-thin oxide, called Soft Breakdown (SBD), has drawn much attention. Despite extensive research in recent years, the mechanism of the SBD phenomena is still controversial in literature, leaving scopes for further investigation into the matter.

In this work we proposed a new and simple model for describing the post Soft Breakdown conduction mechanism for ultrathin gate oxides using Quantum Mechanical Wave Impedance method. The model handles the potential profile of the non-transparent Soft Breakdown spot as a lowered barrier in comparison to that of the remaining unaffected oxide area. In this work, a Soft Breakdown spot is characterized in terms of its barrier height, effective thickness, spot area, electron effective mass, imaginary potential etc. Variation of these parameters is considered to obtain experimental fit between the experimental and theoretical SBD current. It has been observed that a lowered but non-zero oxide barrier remains existent in an SBD spot. It has also been found that the effective oxide thickness and the electron effective mass remains unchanged in comparison to the remaining oxide. Variation of various parameters, such as SBD spot area (used in this work), is taken from the literature. The post SBD currents thus calculated using the proposed model reveal good agreement with the reported experimental results.

CHAPTER 1

INTRODUCTION



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1.1 GENERAL OVERVIEW

Aggressive scaling in microelectronics to achieve higher performance and circuit density necessitates the thinning of the SiO_2 gate dielectric [1]. With the advent of ULSI (Ultra Large Scale Integrated) circuit technology, MOS transistors featuring gate oxide of sub-1.5 nm have already been fabricated [2],[3]. However, the electronic structure at the atomic scale seems to limit practical oxide thicknesses to 0.7–1.2 nm [4]. This is a fundamental limit which cannot be overcome by technological advancements. In this ultrathin (<3nm) gate oxide regime, the reliability has become one of the most important concerns. The degradation and breakdown problem of SiO_2 have been extensively studied for more than fifty years. Much has been learnt about how to grow good quality oxide; however a definitive picture of the microscopic mechanism which finally causes oxide breakdown is still missing. With the increased degradation, the increased gate current adversely affects MOS device performance and greatly increases the standby power consumption of highly integrated chips. Moreover, gate current in small dimension MOS transistors has substantial effect on appropriate modeling of the devices.

In recent years, a new failure mechanism, called Soft Breakdown (SBD), mainly detected in ultrathin oxides (<5 nm), has received much attention for it has important consequences in the evaluation of the reliability of MOS devices [5],[6]. Since the occurrence of this failure event, it is identified as an abrupt change in the oxide conductance, which is several orders larger than that of the Hard Breakdown (HBD). Though in most of the SBD events the device remains functional [7], a large current flows through the damaged oxide. In such cases, accurate modeling of SBD current, along with the understanding of the parameters of a SBD path is extremely essential.

1.2 LITERATURE REVIEW

Since its use as gate insulator in 1957 [8], the degradation of thin silicon dioxide films was observed over three decades ago [9]-[12]. Several physical mechanisms have been identified as the most probable in causing defect generation in thin SiO_2 films. First, an empirical model for breakdown was developed by observing the electric field dependence of TDDB (Time Dependent Dielectric Breakdown) data [13]-[15]. The logarithm of the time-to-failure shows a linear relation with the applied electric field. Later a physical model known as Thermochemical model (or E model) was proposed by McPherson *et al.* [16]. According to that model, the applied electric field eventually breaks the weak bond and creates a permanent defect or trap. Chen *et al.* [17] proposed another model which shows that a positive feedback process causing current runaway, leads to breakdown. The feedback process is initiated when electron injected into the oxide transfers energy to the holes which eventually leads to additional electron injection. However, the above mentioned models were subject to debate as simply observing an empirical dependence of breakdown time on electric field is not a conclusive evidence for a particular physical model [1].

The validity of an electric field driven model becomes questionable after the observation of results from substrate hot electron injection (SHEI) experiments performed by DiMaria [18]. The important results indicate that the time to breakdown is proportional to the inverse of the injected current density, in other words tunneling electrons. In the 90s, DiMaria demonstrated the degradation of oxide due to Anode Hole Injection (AHI) [19],[20] which is initiated by high energy carriers even at low voltage. A critical hole fluence (Qp) is needed for oxide breakdown [17]. Later, Schuegraf *et al.* [21] added that this Q_p decreases for decreasing oxide thickness. Contemporary works by DiMaria and Stasiak [22] showed that there is evidence for a defect generation mechanism involving the release of atomic hydrogen from the anode by energetic tunneling electrons. However, despite the existence of these models, there is still controversy concerning the physical model of breakdown in SiO_2. It is not known definitively whether

released species like hydrogen or injected holes causes the defect that eventually leads to breakdown.

To demonstrate the breakdown statistics, Weibull statistics is widely accepted as it fits data over a wide range of samples [23]. Weibull statistics can incorporate the oxide thickness and also the number of defects at breakdown, N_{BD}. Sune *et al.* [24] first formulated a statistical model and described oxide breakdown and defect generation via a Poisson process. Dumin *et al.* [25] incorporated the model to describe failure distributions in thin oxides. Degraeve *et al.* [26] later used percolation theory to describe the statistical process of breakdown. The parameters used to fit experimental data are the trap radius and the fraction of defects effective in initiating breakdown. Stathis [27] used a computer simulation to demonstrate the thickness dependence of using percolation theory.

In the early 80s, Maserjian *et al.* [28] observed that thin oxides that had been stressed at high voltages had increased low-level pre-tunneling leakage currents through the oxides, the current that is presently known as SILC (Stress Induced Leakage Current). From the experimental point of view, this effect was first studied in details by Olivo *et al.* [29]. At present, there is wide agreement in considering SILC as being related to a trap-assisted tunneling (TAT) mechanism occurring more or less uniformly throughout the structure area [30], [31].

In 1994, a new failure mechanism, mainly detected in ultrathin oxides (<5 nm), has been reported by Lee *et al* [32]. The new failure event is identified by an abrupt change in the oxide conductance, which is several orders of magnitude smaller than that associated with the HBD; the conduction mode has been named Quasi-Breakdown [32] (later Soft Breakdown, SBD). The main two features of this mode are a huge leakage current in the Direct Tunneling (DT) voltage range that shares some major aspects with the BD mode, and a significant increase of the noise level, sometimes in the form of large multilevel current fluctuations with respect to time. Because of the low-field leakage associated with SBD, the terminology B-mode stress-induced leakage current (SILC) has also been used in the literature [33]. To demonstrate the fluctuation of current, Depas *et al.* [5] explained it as multiple

tunneling via electron traps after critical density of traps developed to trigger breakdown. Farmer *et al.* [34] explained the fluctuations as a result of trap–trap transport of electrons.

An elaborate review of different models regarding SBD conduction has been presented by Miranda *et al.* [35]. The foremost models for the SBD conduction were based on the tunneling mechanism. Lee *et al.* [32] proposed that SBD takes place when the injected electrons travel the oxide conduction band ballistically causing a localized physical damage in the vicinity of the anode interface. The damaged region was then modeled as a resistance in series with a trapezoidal potential barrier of reduced thickness (1.8 nm for a 4 nm oxide). According to Okada *et al.* [36], Lee's model fails to reproduce the SBD for bias below 2.5 V. On the same line of thought, Yoshida *et al.* [37] also considered a trapezoidal barrier of reduced thickness (1.6 nm for a 4 nm oxide). In this latter case, the series resistance was simply eliminated. These authors concluded that the length of the conducting filament (the damaged region in the former context) never exceeds 3 nm for all the measured oxides.

Another model based on the tunneling mechanism was proposed by Goguenheim *et al.* [38], who reported that the SBD-curves can be fitted by a simple exponential law (DT related) and suggested that SBD could result from a local reduction of the oxide thickness caused by a sudden metal/insulator transition in a localized region near to the anode interface. Halimaoui *et al.* [39] simulated the SBD current by a superposition of FN and DT currents through a locally modified oxide barrier. Although they found a good agreement in the entire voltage range, the values of the physical parameters used to fit the experimental data were qualified by themselves as questionable: a trapezoidal potential barrier as high as 6 eV with a tunneling thickness of 0.9 nm for a 4.5-nm thick oxide. In summary, all these models share the idea that SBD is caused by an oxide unilateral damaging or thinning, ranging the thickness of this modified zone from 2 to 4 nm. Analyzing the SBD temperature dependence, Okada *et al.* [36] proposed variable range hopping (VRH) as the conduction mechanism for temperatures higher than 125K, however, whether such model is valid for a 3-nm thick oxide is still questionable. It is worth mentioning that VRH predicts for the current an exponential dependence on the oxide thickness.

Recently, an alternative mechanism based on the percolation theory of nonlinear conductor networks has been proposed by Houssa *et al.* [40], which gathered much interest. In this model, it is assumed that two nearest-neighbor trap sites are connected by nonlinear resistors developed through percolation. Post SBD current versus voltage curves have been successfully fitted by Sune *et al.* [41], using Quantum Point Contact (QPC), which represents a conducting filament that has developed as a result of the percolation of defects. Here two parameters are used for fitting- the barrier height of the SBD spot and α, which is used to correlated to the shape or thickness of the contact.

A model was also developed by Alam *et al.* [42] which explains that soft breakdown is the result of limited power dissipation available at the instance of dielectric breakdown. As the oxide ages under constant voltage stress, traps are generated via a percolation process. Current begins to flow through the path and localized joule heating may result in permanent structural damage if the local power dissipation is high enough. Alam also established the connection between the statistical distribution of the theoretically predicted percolation conductance and the distribution of experimentally measured conductance after soft breakdown [43] and explained the thickness, voltage, stress, and circuit configuration dependence of soft and hard breakdown [44].

With the growing controversy whether SBD and HBD resulted from same physical origin, Sune *et al.* [45] showed through statistical analysis that both hard and soft breakdown share a similar origin. The study indicated that soft breakdown was not a pre-cursor to hard breakdown since the hard breakdown conduction spot usually appeared in a different spatial location.

1.3 SCOPE OF THE WORK

Quantum mechanical approach in extracting the parameters of an SBD spot is overlooked in most of the previous works. It is reported that the SBD path is the consequence of the percolation path between different traps [40]. However, the relation between the energy levels of traps with that of an SBD spot is absent. The various physics based parameters, such as SBD effective barrier height, electron effective mass inside the SBD spot, SBD damage area etc are discussed in this work. To extract these various parameters the simulated current through an SBD damaged oxide is related to the previously reported experimental work [46]. The gate current was calculated using the Tsu-Esaki expression [47]. The transmission co-efficient was calculated using Quantum Mechanical Wave Impedance (QMWI) method [48].

1.4 THESIS LAYOUT

This thesis consists of five chapters of which chapter one gives an introduction followed by literature review and objective of this study.

Chapter 2 deals with brief description of MOSFET fundamentals and gate tunneling currents. It also contains a brief description of the origin of traps creation, oxide degradation and an overview of Soft Breakdown phenomenon.

In Chapter 3, the quantum mechanical calculations and the current expression for MOS capacitors are discussed.

The simulation results are presented in Chapter 4 based on the expressions developed in Chapter 3.

Conclusive remarks and discussions are given in chapter 5 with a recommendation for further works.

CHAPTER 2

REVIEW OF MOS STRUCTURES AND OXIDE DEGRADATION DUE TO ELECTRICAL STRESS

2.1 INTRODUCTION

Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), briefly termed as MOS, is the building block of the complex Integrated Circuits (IC), such as microprocessors, graphics, and Digital Signal Processing (DSP) chips. Each IC packs more than 100 million MOS transistors on a single chip. Integration of one billion transistors into a single chip will become a reality before 2010.

The basic operation of a MOS is analogous to that of a capacitor. Here, one plate acts as conducting channel between two ohmic contacts (termed as the Drain and the Source) and the other (called the Gate) controls the charge inducted in the channel. An ideal insulator is placed between the gate and the channel to prevent the flow of any current flow. This research is focused on the reliability of this gate insulator. If a conducting channel is induced by the gate then this type of structure is called enhancement type MOSFET. On the other hand, if the conducting channel is diffused during fabrication the device is called depletion type MOSFET. Enhancement type MOSFET is the most popular used MOSFET. Each MOSFET has an *n* and *p* sub-type depending on the type of carriers (electrons and holes) contributing the current. In this chapter, we focus on the MOSFET structure, operation, its history and the degradation of the Gate of MOSFET.

2.2 A BRIEF HISTORY OF MOSFET

The operating principle of the MOSFET transistor was first described in Lilienfield's historical patent issued in 1926. It took another 34 years before Dawon Kahng and Martin Atalla successfully built a working MOSFET in 1960.

For the past 40 years, the semiconductor industry and academia have relentlessly pushed transistor scaling. Along with scaling, the MOSFET transistor evolved from the p-MOSFET in the 1960's to the n-MOSFET in the 1970's. A good understanding of gate oxide quality, such as interface traps, fixed and mobile charges, and a good control of gate oxide quality in a manufacturing environment enabled industry to make the transition from PMOS technology to a higher-performing NMOS technology in 1970's.

2.3 THE MOSFET STRUCTURE AND OPERATION

The structure of an n-channel enhancement type MOSFET, shown in the figure consists of a moderately doped p-type silicon substrate into which two heavily doped n+ regions, the source and the drain are diffused. Between these two regions there is a narrow region called the channel. A layer of SiO_2 insulator is sandwiched between the channel and the gate made of poly crystalline silicon.

When a positive voltage is applied across the gate and substrate, positive charges are accumulated on the gate. Consequently electrons drift towards the insulator in the region between the drain and source. An increasing gate voltage changes the channel to a conductive path between the drain and source. When, a voltage is applied between drain and source, electrons move from the source to the drain creating an electric current.

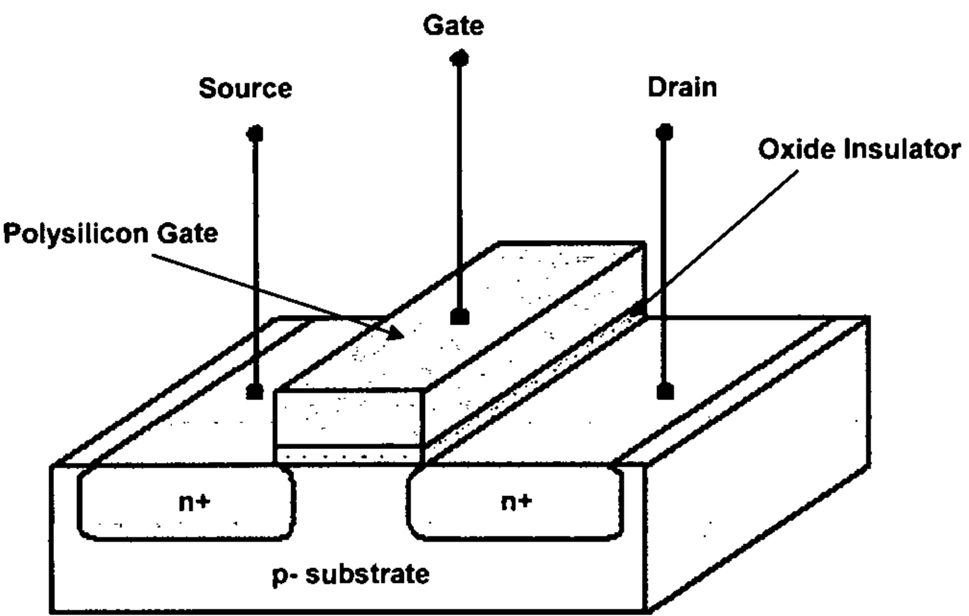

Fig. 2.1: A basic n-channel MOSFET structure.

2.4 MOSFET SCALING AND RECENT TRENDS

Over the past decades, the MOSFET has continually been scaled down in size to achieve lower switching time, reduces cost and lower power consumption. Typical MOSFET channel lengths were once several micrometres, but modern integrated circuits are incorporating MOSFETs with channel lengths of less than a tenth of a micrometre long. Indeed Intel will begin production of a process featuring a 65nm channel length in early 2006. Until the late 1990s, this size reduction resulted in great improvement to MOSFET operation with no deleterious consequences.

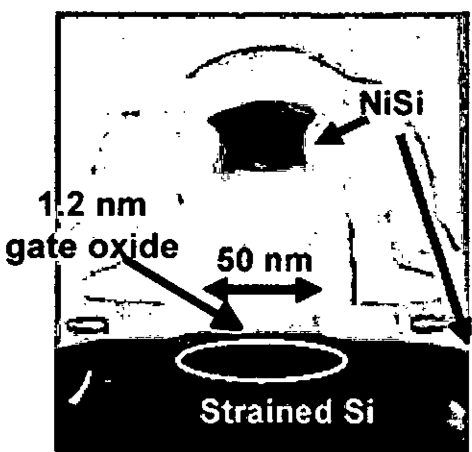

Fig. 2.2: 45-nm transistor presented in IEDM 2003 (Ref. [3]).

The most advanced MOS transistors used in volume production today are probably those of Intel's used in their 130nm logic technology with transistor gate length and gate oxide thickness are 60nm and 1.5nm, respectively. At IEDM 2003 [3], Intel presented a manufacturing-ready 90nm technology, with transistor gate length 50nm and gate oxide thickness 1.2nm. As of 2nd half of 2004, 90nm technology is at the beginning of manufacturing life cycle at a very limited number of top semiconductor manufacturers. For majority of IC manufacturers, 90nm technology is in the qualification stage or in the middle of development.

2.5 MOSFET ENERGY BAND DIAGRAM

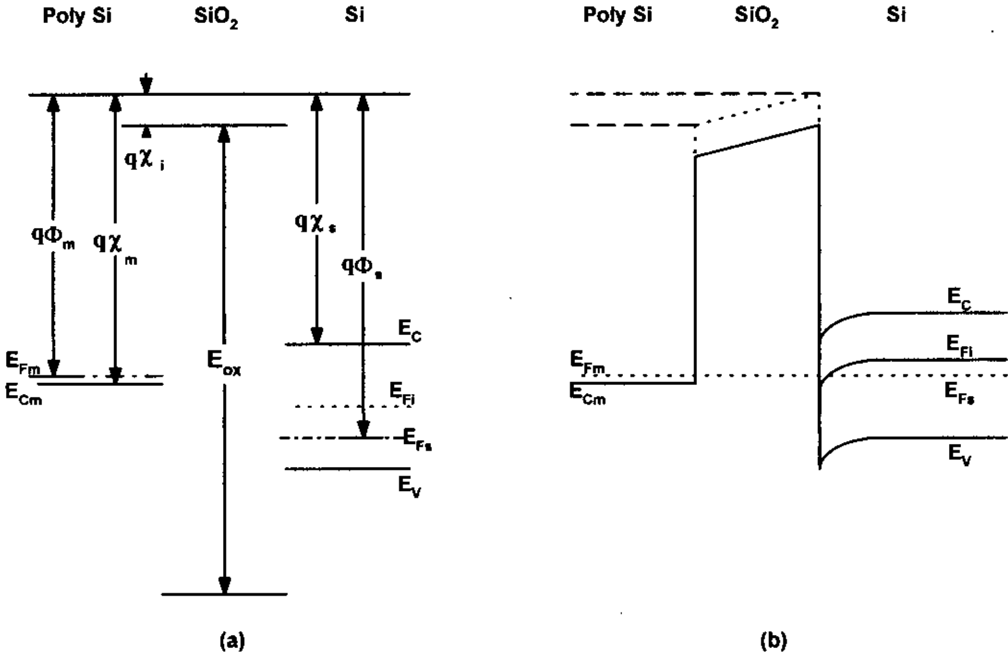

Fig. 2.3: Energy Band diagram of a p type MOS capacitor, (a) Before contact (b) After contact.

For a material, work function ϕ_m is defined as the potential needed to inject an electron from the Fermi level of the material to the vacuum. On the other hand, electron affinity is the potential needed to inject an electron from the conduction band of the material to the vacuum. The work function difference of metal (or poly Silicon) and semiconductor is given by [49],

For p-type substrate,

$$\phi_{ms} = \left[\phi_m - \left(\chi_m + \frac{E_g}{2q} + \phi_{fp}\right)\right] \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.1)$$

For n-type substrate,

$$\phi_{ms} = \left[\phi_m - \left(\chi_m + \frac{E_g}{2q} - \phi_{fn}\right)\right] \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.2)$$

Here, E_g is the band gap of the semiconductor substrate material. ϕ_{fp} and ϕ_{fn} are the potential difference between the extrinsic and intrinsic Fermi Level for p-substrate and n-substrate respectively. As shown in the Fig. 2.3, after contact there is a band bending of the energy bands that introduce a potential difference between the conduction band at the interface and that of the bulk. This voltage is termed as *Surface Potential* (ψ_S). This bending can be eliminated by applying Flat Band Voltage (V_{FB}) which is given by the following relation,

$$V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C_{ox}} \quad \ldots \ldots \ldots \ldots \ldots \ldots \ldots (2.3)$$

Where, Q_{ss} is the interface trap charge or surface state trap charge per unit area and C_{ox} is the capacitance per unit area of the gate oxide. The channel can become a depletion, inversion, strong inversion or accumulation depending upon the surface potential. The depletion layer width W and the charges per unit area in the depletion region is given by [50],

$$W = \sqrt{\frac{2\varepsilon_s \psi_s}{qN_A}} \quad \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (2.4)$$

and, $$Q_B = -qN_A W \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (2.5)$$

here, ε_s is the permittivity of Si, N_A is the doping concentration of the substrate

The relation between the applied voltage and the surface potential is given by [50],

$$V_G = V_{FB} + \psi_s \pm \gamma \sqrt{\psi_s \left(1 - e^{\frac{-2\varphi_F}{\varphi_t}}\right) + \varphi_t \left\{ e^{\frac{-\psi_s}{\varphi_t}} + e^{\frac{(\psi_s - 2\varphi_F)}{\varphi_t}} - e^{\frac{-2\varphi_F}{\varphi_t}} - 1 \right\}} \ldots \ldots \ldots (2.6)$$

here, body effect parameter, $$\gamma = \left(\frac{\sqrt{2q\varepsilon_s N_A}}{C_{ox}} \right) \quad \ldots \ldots \ldots \ldots \ldots \ldots (2.7)$$

and, oxide capacitor per unit area, $$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (2.8)$$

here, ε_{ox} is the permittivity of the oxide; t_{ox} is the thickness of the oxide

2.6 THE GATE AND GATE OXIDE

Early MOSFET used metal (such as aluminum) as a gate electrode, hence the name MOSFET was came. However, in fabrication processes high temperature causes metal to melt. Moreover, MOSFETs with metal gates have higher threshold voltage. Thus poly-crystalline silicon was preferable to metal as gate material as it has higher melting point. However, polysilicon is highly resistive (approximately 1000 times more resistive than metal) which reduces the signal propagation speed through the material. To lower the resistivity, dopants are added to the polysilicon. Sometimes additionally, high temperature metal such as Nickel layered onto the top of the polysilicon which decreases the resistivity. Such a blended material is called silicide. The silicide-polysilicon combination has better electrical properties than polysilicon alone and still does not melt in subsequent processing. Also the threshold voltage is not significantly higher than polysilicon alone, because the silicide material is not near the channel.

In case of the Gate Oxide, the insulator should be of high insulating property to resist leakage current from gate to the channel. As the device is scaled down, the tunneling phenomena becomes prominent leading to an increased power consumption. (The various degradation of oxide are discussed in the following sections). Insulators that have a larger dielectric constant than SiO_2, such as group IV(B) metal silicates e.g. Hafnium and Zirconium Silicates and Oxides, are now being researched to reduce the gate leakage. Increasing the dielectric constant of the gate oxide material allows a thicker layer while maintaining a high capacitance. The higher thickness reduces the tunneling current between the gate and the channel. An important consideration is the barrier height of the new gate oxide; the difference in conduction band energy between the semiconductor and the oxide will also affect the leakage current level. For the traditional gate oxide, silicon dioxide, the former barrier is approximately 3 eV. For many alternative dielectrics the value is significantly lower, somewhat negating the advantage of higher dielectric constant.

2.7 GATE OXIDE TUNNELING

According to quantum physics electrons behave both like particles and like waves and are described by the solutions of Schrödinger equation. These waves can penetrate a potential barrier that would be a forbidden area if the particle was considered in the classical way. The term tunneling phenomenon refers to this property-the particle "tunnels" through the forbidden area.

2.7.1 Interband Tunneling

The interband tunneling occurs because of the finiteness of the height and width of the oxide barrier. It can be either direct (DT) or Fowler-Nordheim (FN) tunneling depending upon the magnitude and polarity of the applied gate voltage. The mechanisms are governed by the shape of the tunneling barrier. If the oxide barrier is trapezoidal and the electrons do not transit through the conduction band states of the barrier, then that is called Direct Tunneling (Fig. 2.4 (a)[i]). If the tunneling barrier is triangular and the transported electrons partly transit through the conduction band states of the barrier, then FN tunneling (Fig. 2.4 (a)[ii]) occurs [52],[53].

2.7.2 Trap-Assisted Tunneling

With advent of modern ULSI (Ultra Large Scale Integrated) technology, the grown SiO_2 has reached a satisfactory purity level. However, still the SiO_2 is not devoid of impurities. Such impurities and oxide defects are modeled as oxide traps which in turns lead to additional leakage current. Detailed description is presented in the subsequent sections.

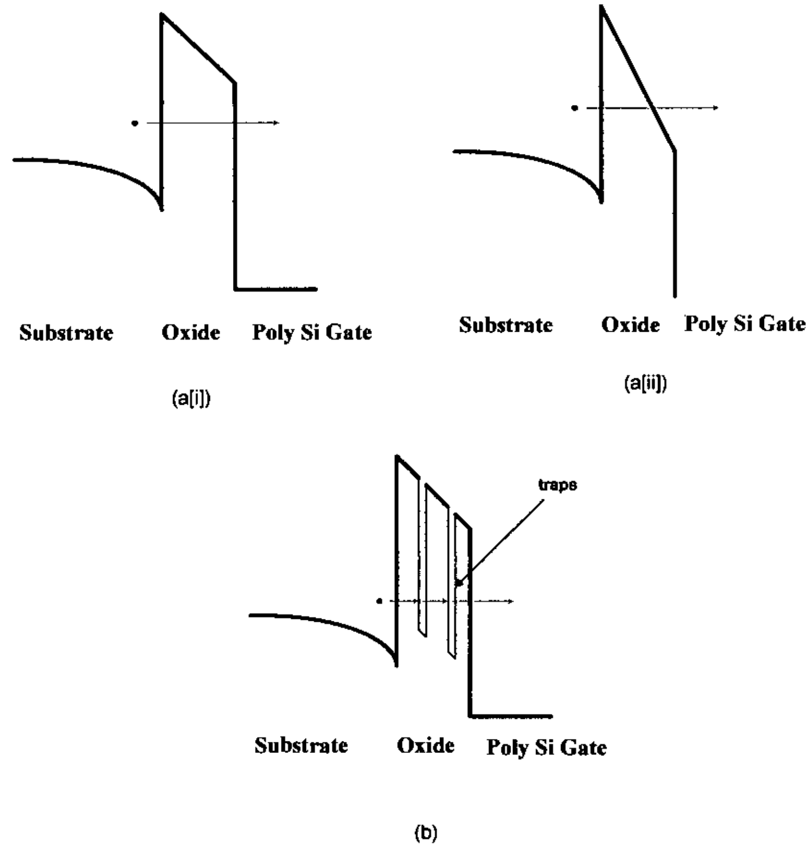

Fig. 2.4: (a) Energy band diagram of two types of Interband tunneling- [i] Direct Tunneling (DT), [ii] Fowler-Nordheim (FN) Tunneling, (b) Trap Assisted Tunneling (TAT).

2.7 GATE OXIDE DEGRADATION

Although the exact physical mechanism responsible for wear-out and eventual breakdown is still an open question, it is generally assumed that a driving force such as the applied voltage or the resulting tunneling electrons create defects in the volume of the oxide film. The defects accumulate with time and eventually reach a critical density triggering a sudden loss of dielectric properties. A surge of current produces a large localized rise in temperature leading to permanent structural damage in the silicon-oxide film [1].

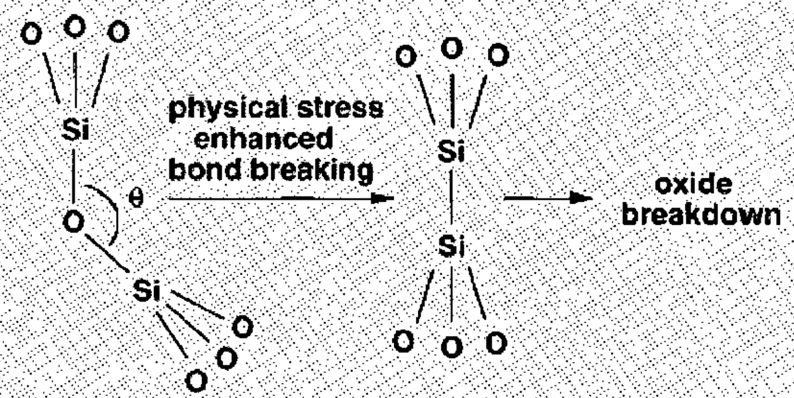

Fig. 2.5: Proposed physical stress-enhanced bond breaking mechanism [51]. For the oxide breakdown to occur, the Si–O–Si bonds in SiO_2 break and are replaced by the Si–Si bonds, and this process is strongly dependent on the physical stress in the thin oxide films.

The electron traps can be of two types depending upon their origin- i) traps during formation or the 'as grown' traps and ii) traps due to the applied electrical stress. Traps formed during the fabrication steps are intrinsic oxide traps, intrinsic interface traps and impurities.

To demonstrate the oxide degradation process and trap generation during stress, Yang and Saraswat [51] assumed that the Si-O-Si bond is broken and replaced by the Si-Si bond during an oxide breakdown. As to the missing oxygen atom after the formation of the Si-Si bond, the following process was proposed because it is not easy for the oxygen atoms to dissociate out of oxides:

$$2(\equiv \mathrm{Si}-\mathrm{O}-\mathrm{Si}\equiv) \leftrightarrow \equiv \mathrm{Si}-\mathrm{Si}\equiv + \equiv \mathrm{Si}-\mathrm{O}-\mathrm{O}-\mathrm{Si}\equiv$$

This Si-Si bond is very weak and it can be either an electron trap or a hole trap.

In the past, many studies have been published that suggest that there are perhaps four regimes in which the relationship between the generation of defects and the electron energy during transport is well understood. The regime is where the electron energy is greater than 9 eV, the bandgap of SiO_2, *Impact Ionization* [54] occurs.

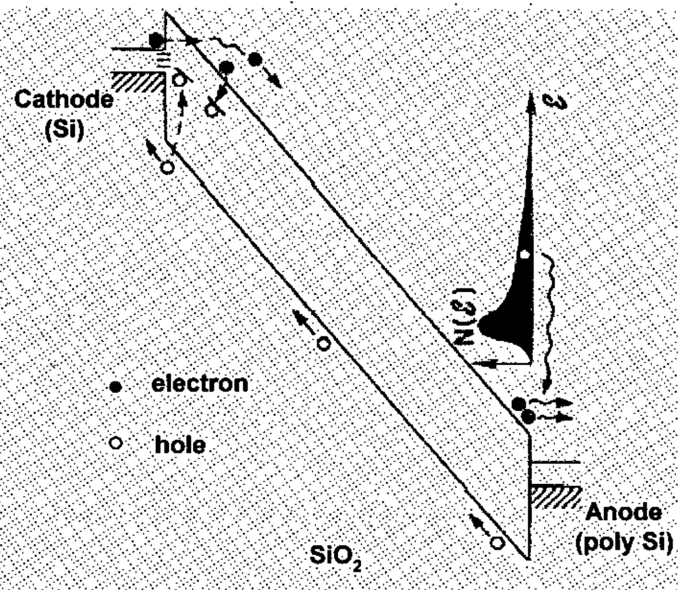

Fig. 2.6: Schematic energy-band diagram showing defect generation near the cathode caused by free-electron/trapped-hole recombination where holes were generated in the oxide bulk by impact ionization [54]. Density of states N(ℰ) as a function of electron energy is also shown here.

Generally this occurs only in relatively thick films and extremely high electric fields, in which case electron-hole pairs are created. The subsequent trapping of holes and electrons, and the recombination of electrons on trapped hole sites, generate defects in the form of electron traps and interface states.

In the second regime, for a bias condition in which the electron energy is less than the SiO_2 bandgap, holes may still be created in the anode of a MOS device. Some of these holes may be injected back into the oxide film, where they can be trapped and create defects. This mechanism of creating defects is usually referred to as *Anode Hole Injection* (AHI) [19]. The exact mechanism for the production of holes is still under some debate, but it is accepted that the injection of these holes back into the oxide film leads to trapped holes and the production of interface states. Anode hole injection usually occurs in relatively thick films (~10nm) if the electric field across the oxide is greater than 5 MV/cm. Anode hole injection can also occur in thin films independent of the oxide field, but only if the applied bias is greater than ~7-8V.

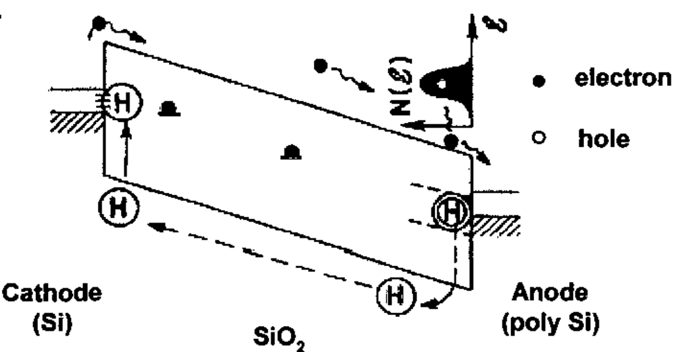

Fig. 2.7: Schematic energy-band diagram showing trap creation near the cathode caused by mobile hydrogen release from decorated sites near the anode for electron energy >2eV [54]

In the ultra-thin-oxide regime, the transport of the electrons is approximately ballistic. The term '*ballistic*' is meant to refer to the fact that electrons traverse the film without losing energy. For an applied bias, $5<V_{applied}<7$ V (for a poly-Si/SiO_2/Si structure), where the transported electrons have an energy at least 2 eV above the SiO_2 conduction band edge, only electrons, not holes, are present in the dielectric. These hot electrons create damage in the form of electron traps and interface states.

In the fourth regime, defect generation occurs below a bias voltage of 5V. The actual mechanism of the creation of defects in this regime is yet to be clearly understood.

2.8 SOFT BREAKDOWN PHENOMENA OF GATE OXIDE

In 1994, a new failure mechanism was identified by Lee *et al.* [32] in ultra-thin oxide. This new phenomenon is identified as an abrupt change in the oxide conductance, which is several orders of magnitude smaller than that associated with the HBD-the conduction mode initially has been named Quasi Breakdown (QBD). This failure mode was also known as B-mode SILC [55]. (The conventional Stress Induced Leakage Current, SILC was named A-mode SILC). However, at present this mode is widely known as *Soft Breakdown* [5].

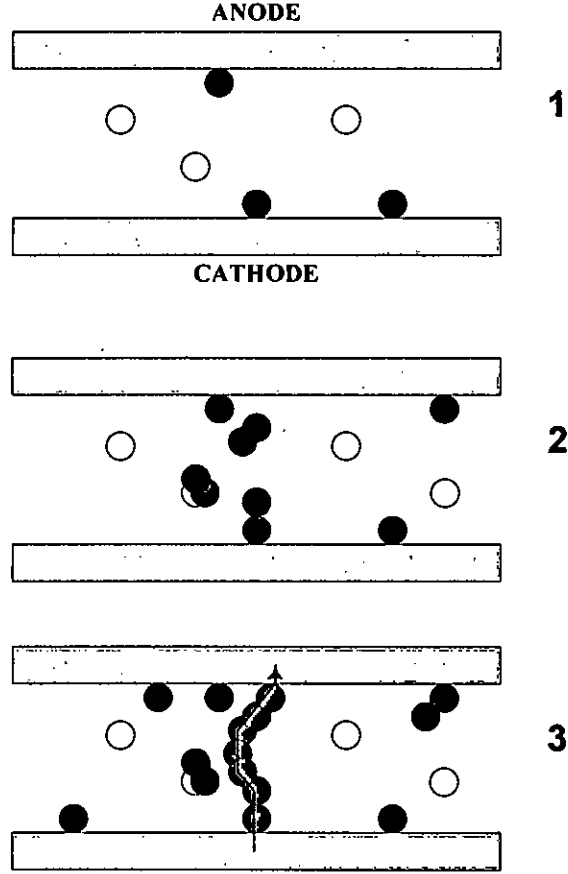

Fig. 2.8: Series of schematics illustrating the percolation of defects and ultimate breakdown in ultra-thin gate oxides. Oxide traps (circles) are generated randomly throughout the volume of the dielectric in step 1. If two neighboring traps overlap or are in contact with one of the electrodes conduction is possible (shaded circles shown in step 2. Breakdown occurs when a conducting path is created from one interface to another shown in step 3. [1]

Two main features of this Soft Breakdown can be highlighted: i) during a high-field stress, several SBD events can occur in a single sample and this causes an apparent increase of the area involved in the conduction [56] and ii) the application of a low voltage after the occurrence of SBD events leads to the observation of large current fluctuations which have the appearance of a random telegraph signal (RTS) [56].

Soft Breakdown path is proposed to be created due to the creation of percolation path between adjacent traps [46]. The connecting path between two traps behaves like nonlinear conductors. The area of the breakdown spot depends on the

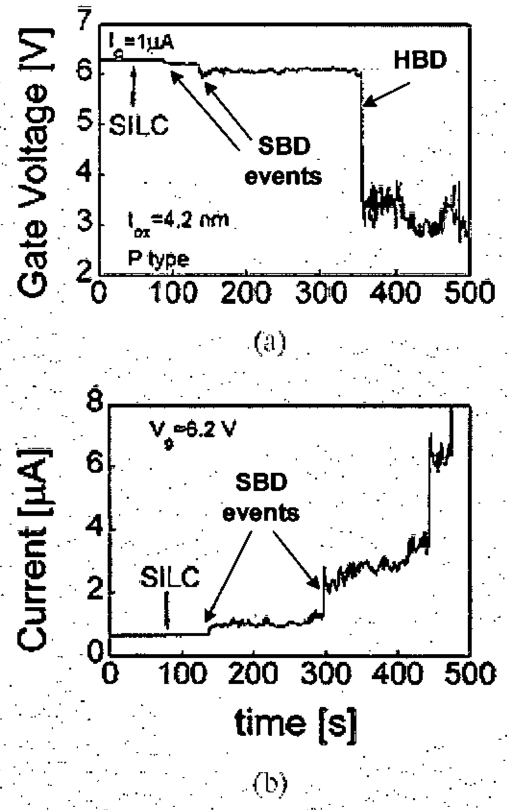

Fig. 2.9: Experimental observation of SBD [35]. Temporal evolution of (a) gate voltage and (b) current under constant stress. The oxide thickness is 4.2 nm, the capacitor area is 1.96×10^{-5} cm^2, and the substrate is p-type.

breakdown current runaway and for both SBD and HBD it has been estimated to be of atomic dimensions (in the 10^{-14}-10^{-12} cm^2) [45],[57]. According to circuit point of view the device may still remain functional after going through SBD [7], however, recent research reveal that device failure can also occur due to further degradation of SBD spot [58].

CHAPTER 3

CALCULATION OF QUANTUM MECHANICAL TUNNELING PARAMETERS IN MOS STRUCTURES

3.1 INTRODUCTION

In order to calculate the current density through an oxide barrier and to understand the resonant tunneling process, an estimation of quantum mechanical transmission co-efficient (QMTC) is across the oxide potential barrier and quantum well structure is needed. The transport properties of tunnel structures may be analyzed by solving the one-electron, one-dimensional, time-independent Schrödinger equation with scattering wave conditions.

The conventional method for determining the QMTC has been the Wentzel-Kramer-Brillouin (WKB) approximation [59],[60]. Although conceptually elegant, it is an approximation that does not take into account the detailed structure of a given potential below the penetrating electron energy level. Furthermore, it predicts incorrect resonant energies of a resonant system [61]. The WKB method is a quasi-classical approximation and is valid when the De-Broglie wavelengths of electrons are small compared to the distance over which the potential changes appreciably.

Chandra and Eastman [62] calculated the QMTC for a triangular barrier via the numerical method using Taylor series expansions for the wavefunction and its derivative. Although this method can be extended to include arbitrary structures, large number of grid-points may very often be necessary, which is computationally inefficient. There are other methods, but all of them require extensive matrix manipulation.

A simple method of calculating the QMTC of tunnel structures is presented in Sec 3.2; this method was formulated by Khondker *et al.* [48].

3.2 QUANTUM MECHANICAL CALCULATIONS FOR POTENTIAL BARRIERS

The calculation of Quantum Mechanical Transmission Co-efficient (QMTC) is necessary for analyzing the current–voltage (I-V) characteristics of resonant tunneling and quantum size devices [63]. In this work the QMTC is calculated by Quantum Mechanical Wave Impedance (QMWI) method formulated by Khondker *et al.* [48].

Using the effective mass approximation the one dimensional Schrödinger Equation is written as

$$-\frac{\hbar^2}{2}\frac{d}{dx}\left(\frac{1}{m^*(x)}\frac{d\psi}{dx}\right)+\left[V(x)-E\right]\psi(x)=0 \qquad \text{(3.1)}$$

where, $\psi(x)$ is the envelope wave function, E is the energy of incident electron and V(x) is the potential energy. Here, $m^*(x)$ is the effective mass and $\hbar$ is the reduced Planck's constant. If we consider constant effective mass and potential constant then the Schrödinger equation reduces to,

$$\frac{d^2\psi}{dx^2}+\frac{2m^*}{\hbar^2}\left[E-V(x)\right]\psi(x)=0 \qquad \text{(3.2)}$$

and the solution of the Eqn. (3.2) is,

$$\psi(x)=A^+\left(e^{\gamma x}-pe^{-\gamma x}\right) \qquad \text{(3.3)}$$

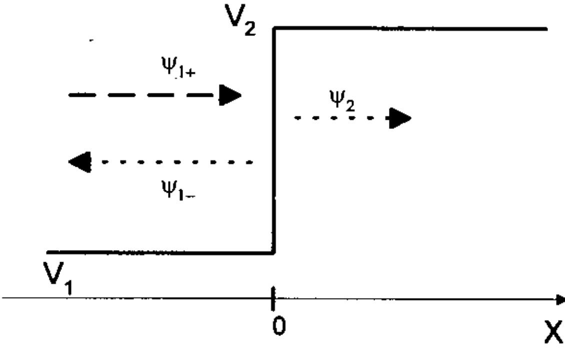

Fig. 3.1: A step potential barrier with potential height of (V_2-V_1).

where, the propagation constant, γ is given by

$$\gamma = \alpha + j\beta = j\sqrt{\frac{2m^*[E - V(x)]}{\hbar}} \qquad \dots\dots\dots\dots\dots\dots(3.4)$$

In Fig. 3.1, the wave function $\psi(x)$ in the region where $x<0$, can be defined as the superposition of two waves – one the incident wave ψ_+ and another is the reflected wave ψ_- that is reflected from the potential discontinuity at $x=0$.

3.2.1 Calculation of QMTC

Now, differentiating Eqn. (3.3) w.r.t. *x* and multiplying on both sides by factor ($\hbar/jm^*$) we get,

$$\Phi(x) = A^+ Z_0 \left(e^{\gamma x} + \rho e^{-\gamma x}\right) \qquad \dots\dots\dots\dots\dots\dots\dots(3.5)$$

where,

$$Z_0 = \gamma\hbar \big/ jm^* \qquad \dots\dots\dots\dots\dots\dots\dots(3.6)$$

According to Khondker *et al.* [48] the terms $\psi(x)$ and $\phi(x)$ are analogous to the distributed parameters I(x) and V(x) of transmission lines respectively. The term Z_0 is regarded as characteristic impedance of the region with potential V(x) that is analogous to the characteristic impedance of transmission line. The new parameter introduced by Khondker *et al.* [48] is Quantum Mechanical Wave Impedance, which is defined as [48],

$$Z(x) = \frac{\Phi(x)}{\psi(x)} = R(x) + jX(x) \qquad \dots\dots\dots\dots\dots\dots\dots(3.7)$$

where, R(x) and X(x) are the real and imaginary parts of the QMWI at any point.

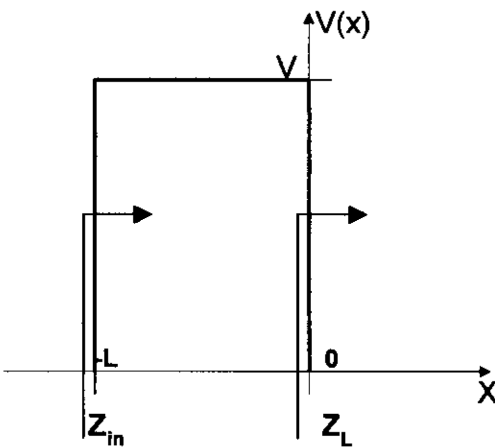

Fig. 3.2: Calculation of QMWI for a potential barrier of length L.

Fig. 3.2 illustrates the calculation of Z(x) using simple formula. If the load impedance at point x=0 is Z_L, then the input impedance at point x=-L will be $Z(x)=Z_{in}$ (Fig. 3.2).
Here,

$$Z_{in} = Z_0 \frac{Z_L \cosh\gamma L - Z_0 \sinh\gamma L}{Z_0 \cosh\gamma L - Z_L \sinh\gamma L} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3.8)$$

In similar way, the QMWI can be determined at the potential boundaries. Such method can also be applied for potential profiles that vary continuously with x. In such case, the potential profile is approximated as multistep functions with a sequence of N segments each having a length of L.

Here, the QMWI of the segment 1 at the boundary is considered Z_L (or Z_1) looking to the right. By using Eqn. (3.8) we determine the input QMWI of segment 1 (or Z_2). This input impedance serves as the load QMWI for segment 2. In this way, the input QMWI of N-th segment can be determined, which is the input QMWI of the whole potential profile.

Now, after determining the QMWI of the whole potential structure, the amplitude reflection co-efficient is calculated by,

$$\rho(E) = \frac{Z_L - Z_0}{Z_L + Z_0} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3.9)$$

The Quantum Mechanical Transmission Co-efficient (QMTC) will be determined by,

$$T(E) = 1 - |\rho(E)|^2 \quad \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (3.10)$$

The next section will be dedicated to a detailed numeric example for calculating QMWI and QMTC.

3.2.2 A Numeric Example for Calculating QMTC

Let us consider a simplified Si-Oxide-Poly Si structure, where the band bending effects are ignored. The specifications for this potential barrier without any applied voltage are as follows:

Barrier Length	= 4.2 nm
Si Conduction Band Energy, V_1	= 0 eV
Oxide barrier height, V_{ox}	= 3.15 eV
Poly Si conduction band energy, V_3	= -0.5 eV
Electron effective mass in Si and Poly Si,	= $1.0\times m^*$
Electron effective mass in Oxide,	= $0.5\times m^*$
Electron energy,	= 0.1 eV

The QMTC is to be calculated when a voltage of 1.0 V is applied.

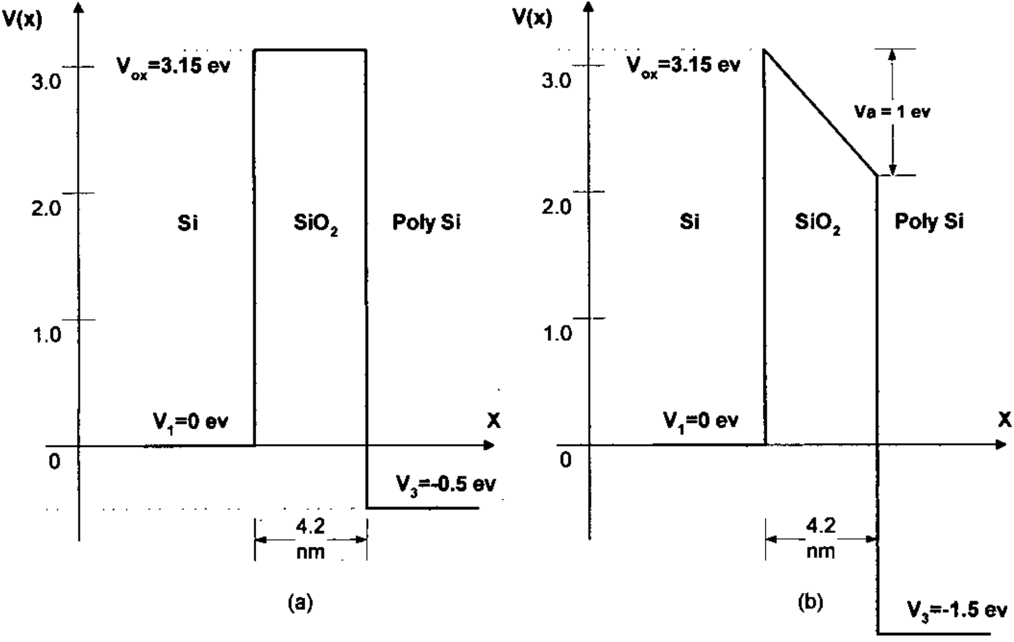

Fig. 3.3: The energy band diagram of the numeric example presented in section 3.2.2, (a) Before applying voltage, (b) After applying voltage.

The effective mass is considered constant throughout the oxide barrier. After the application of voltage the potential is varying with distance (Fig. 3.3). The values of the step potentials can be determined by,

$$V(x) = V_i = \frac{V(x_i) + V(x_{i+1})}{2} \qquad \text{... ... ...(3.11)}$$

where, i= 1, 2, 3, ... N. In this example we considered N=4 for reducing complexity. However, the accuracy of the calculated values increases if N is changed to a large value.

Fig. 3.4 shows the calculated potential values of the multisteps and the corresponding magnitudes of γ and the characteristic impedance Z_0.

Fig. 3.5 shows the values of Z_{in} and the final amplitude reflection co-efficient ρ and the QMTC, T(E).

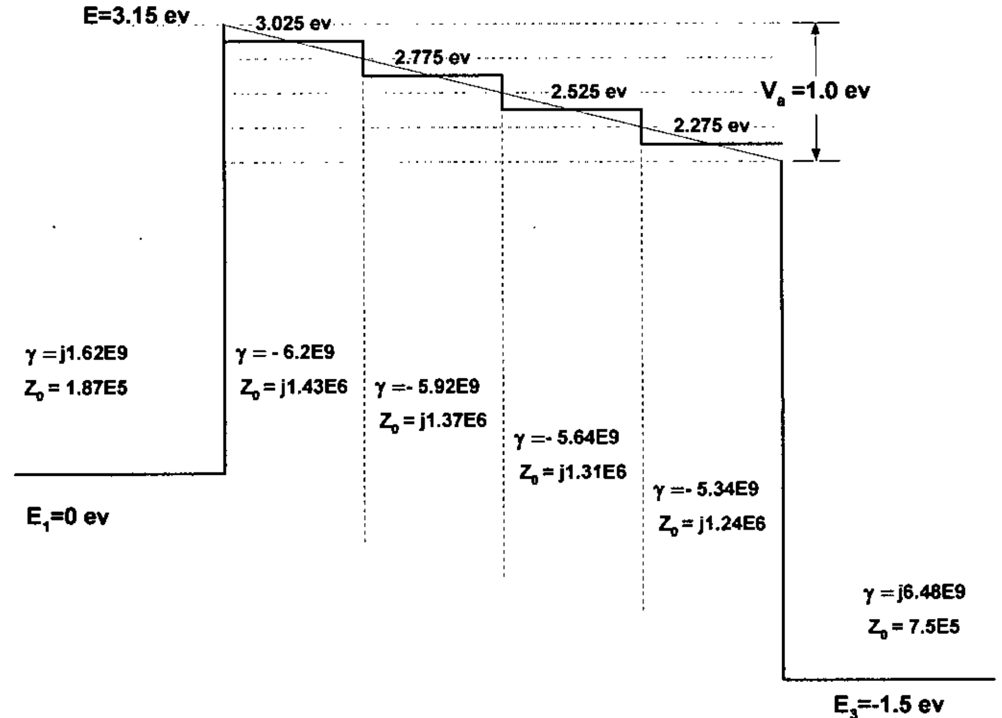

Fig. 3.4: Calculated potential values of the multisteps and the corresponding magnitudes of γ and the characteristic impedance Z_0.

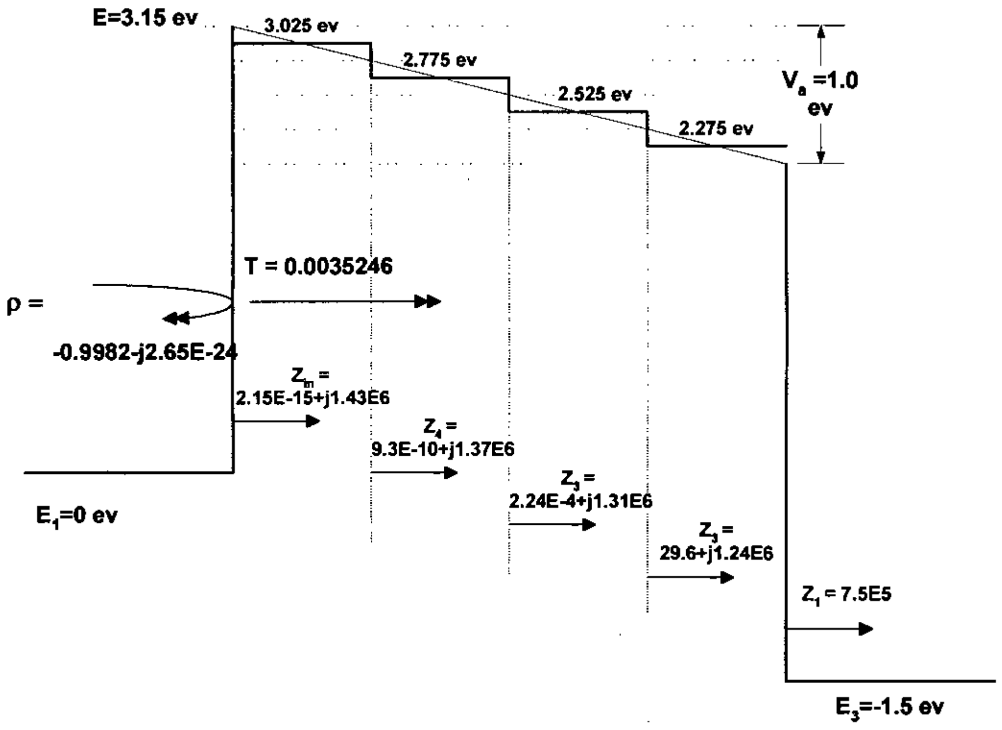

Fig. 3.5: Values of Z_{in} and the final amplitude reflection co-efficient ρ and the QMTC, T(E).

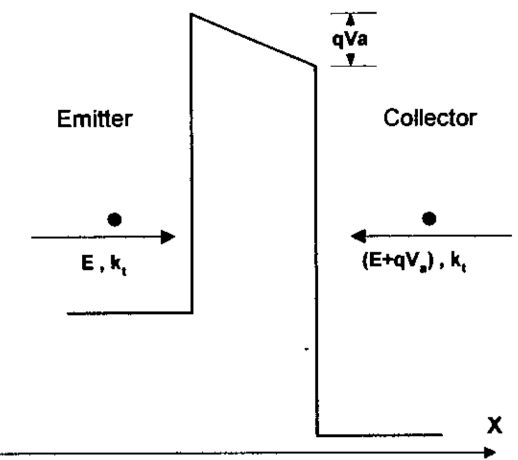

Fig. 3.6: A schematic representation of a potential energy profile employed in the derivation of the current density expression.

3.3 CURRENT DENSITY FORMULA

The nonzero probability for tunneling of electrons through potential barrier offers the possibility of measurable currents. A typical situation is shown in Fig. 3.6 where an electron plane wave is specified by a total energy E and a transverse wave vector k_t.

For arbitrary potential barrier, electrons incident upon the potential from both the electrodes will contribute to the total current. First, let us consider the contribution from electrons incident from the emitter. Since electrons are fermions, these electrons will contribute to the total current only if there are corresponding empty states on the side to which the electrons can tunnel. Assuming conservation of total energy and transverse momentum [47], the tunneling current density $J_{E\text{-}C}$ from a unit volume of k-space is [61].

$$J_{E-C} = \frac{q}{\hbar}\left(\frac{\partial E}{\partial k_x}\right)_E g(k) f_E(E)\left[1 - f_C(E + qV_a)\right] T(E, k_t) \quad \ldots\ldots\ldots\ldots\ldots(3.12)$$

where, f_E (E) and f_C (E) are the Fermi-Dirac electron distribution function at the emitter and collector electrode respectively. g(k) is the density of states per unit volume of k-space.

A similar analysis can be used to obtain the contribution from electrons of energy ($E+qV_a$) incident from the collector. Since the tunneling probability is equal for both directions, the tunneling current density J_{C-E} from the collector to the empty states of the emitter is given by,

$$j_{C-E} = \frac{q}{\hbar}\left(\frac{\partial E}{\partial k_x}\right)_{(E+qV_a)} g(k) f_C(E+qV_a)[1-f_E(E)]T(E,k_t) \quad \ldots\ldots\ldots\ldots\ldots(3.13)$$

The net tunneling current density per unit volume of k-space is,

$$J_t = J_{E-C} - J_{C-E} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3.14)$$

The density of states per unit volume of k-space is evaluated to be [64]

$$g(k) = \frac{2}{(2\pi)^3} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3.15)$$

The Fermi-Dirac electron distribution function is given by,

$$f(E) = \frac{1}{1+\exp\left(\frac{E-E_F}{k_B T}\right)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3.16)$$

where, E_F is the Fermi energy, k_B Boltzman's constant and T is the absolute temperature.

To simplify the analysis, we neglect the velocity difference between the electrons of emitter and collector and evaluate the derivative in Eqn. (3.13) at E instead of at ($E+qV_a$). The assumption of parabolic energy momentum relationship for states describing the contacts reduces Eqn. (3.14) to,

$$J_t = \frac{2}{(2\pi)^3}\frac{q\hbar k_x}{m^*}[f_E(E) - f_C(E+qV_a)]T(E,k_t) \quad \ldots\ldots\ldots\ldots\ldots\ldots(3.17)$$

The electron effective masses for the two electrodes are assumed to be equal. Integrating J_t over the entire k-space the total current density can be obtained

$$J = \frac{2}{(2\pi)^3}\frac{q\hbar}{m^*}\int_0^\infty\int_0^\infty k_x T(E,k_t)[f_E(E) - f_C(E+qV_a)]2\pi k_t\, dk_t dk_x \quad \text{......... ...(3.18)}$$

$$\therefore J = \frac{2qm^*}{(2\pi)^2\hbar^3}\int_0^\infty\int_0^\infty T(E,k_t)[f_E(E) - f_C(E+qV_a)]dE_t dE_x \quad \text{......... ...(3.19)}$$

where,

$$E = \frac{\hbar^2 k_t^2}{2m^*} + E_x \quad \text{..................... ...(3.20)}$$

The effect of mass variation on the transverse motion can be neglected, as done by several authors [47],[61],[63]. This makes the transmission coefficient dependent only on the longitudinal energy E_x=E-E_t. The E_t integral can now be performed giving the usual Tsu-Esaki expression [47]:

$$\therefore J = \frac{qm^* k_B T}{2\pi^2\hbar^3}\int_0^\infty T(E_x)\ln\left[\frac{1+\exp\left\{\frac{(E_{F_E} - E_x)}{k_B T}\right\}}{1+\exp\left\{\frac{(E_{F_C} - E_x - qV_a)}{k_B T}\right\}}\right]dE_x \quad \text{...... ...(3.21)}$$

The spatial dependence of effective mass is however taken into account to calculate $T(E_x)$ in Eqn. (3.21).

In the derivation of tunnel current expression the velocity of an electron of energy ($E+qV_a$) incident from the collector is assumed to be equal to that of an electron of energy E incident from the emitter. Collins *et al.* [61] found the contribution to J due to the velocity difference to be less than 10% for physically relevant tunneling systems. This is conceivable, since at low voltages the velocity difference is small, while at higher voltages the contribution from the collector is insignificant.

3.4 CONCLUSION

Following Khondker *et al.* [48], a simple but exact method of solving the Schrödinger equation for a piecewise constant potential has been presented. Since any potential function can be approximated to arbitrary accuracy using a piecewise constant function, the Schrödinger equation can be solved to any degree of accuracy for various potential barriers and wells including continuous variations of potential and effective mass. In addition to this it can be noted here that the surface potential for the Si substrate is kept constant and its variation with the applied voltage is ignored. The quantized energy levels inside the potential well of inversion region are also neglected here.

CHAPTER 4

RESULTS

4.1 INTRODUCTION

In this chapter, the simulated results using the expressions summarized in the previous chapter are presented in details. The aim of this work is to find out the parameters of a Soft Breakdown (SBD) path from the I-V characteristics of gate oxide after a single SBD event. The current density of a fresh oxide (SiO_2 is considered here) is presented at first. The variations of the current density for fresh oxide with gate oxide thickness, substrate Fermi level, oxide effective mass, imaginary potential inside the oxide, oxide barrier height are also analyzed. Then the I-V characteristic of an oxide that has undergone SBD is presented.

4.2 SIMULATED OXIDE CURRENT DENSITY

The simulations here are performed for a MOS capacitor, with SiO_2 grown on n-Si substrate (100) with $N_D=10^{15}$ cm^{-3}. The gate is made of poly Silicon with n-type doping. The effective mass of electrons in Si is taken as $m^* = 0.98m_0$ as done by early researchers. Fig. 4.1 shows the band diagram of Si-SiO_2-poly Si structure for none bias condition. Here, the band tilting inside SiO_2 is neglected.

The height from the conduction band edge of Si to that of SiO_2 is considered to be 3.15 eV [65]. In fact this barrier height differs in literature and varies between 2.3 eV and 5 eV [66]. The band gap of SiO_2 and poly Si varies from 9 eV to 10 eV and from 1.5 eV to 1.8 eV respectively. Consequently the energy difference between the conduction band of SiO_2 and poly Si varies between 4 eV and 6 eV. Here, the value is taken to be 3.65 eV.

The use of doped poly Si as a gate material introduces a thin space charge layer at the SiO_2-poly Si interface which acts to retard the applied field. This effect is termed as poly Si depletion effect which is generally considered as thickening of gate oxide

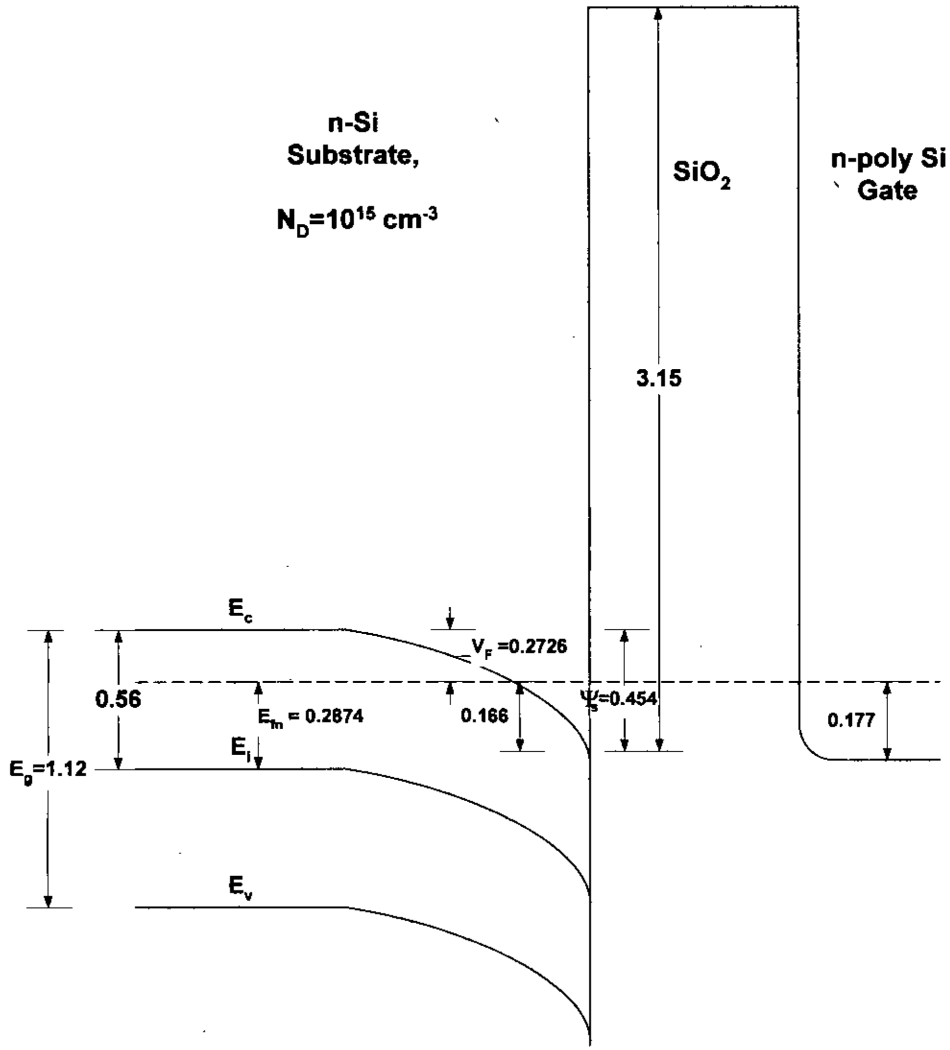

Fig. 4.1: The energy band diagram of an n-Si–SiO_2-n-poly Si structure and the corresponding values of energies.

thickness by constant amount [50]. But such consideration can bring about overestimated results [67]. Hence this effect is ignored in this work.

Though the E-k relation is important for modeling the electron tunneling through the oxide, experiment or calculations of band dispersion is virtually non-existent. For this work parabolic E-k diagram is assumed. The effective mass inside oxide, which depends upon the fabrication process, growth and condition of the amorphous oxide

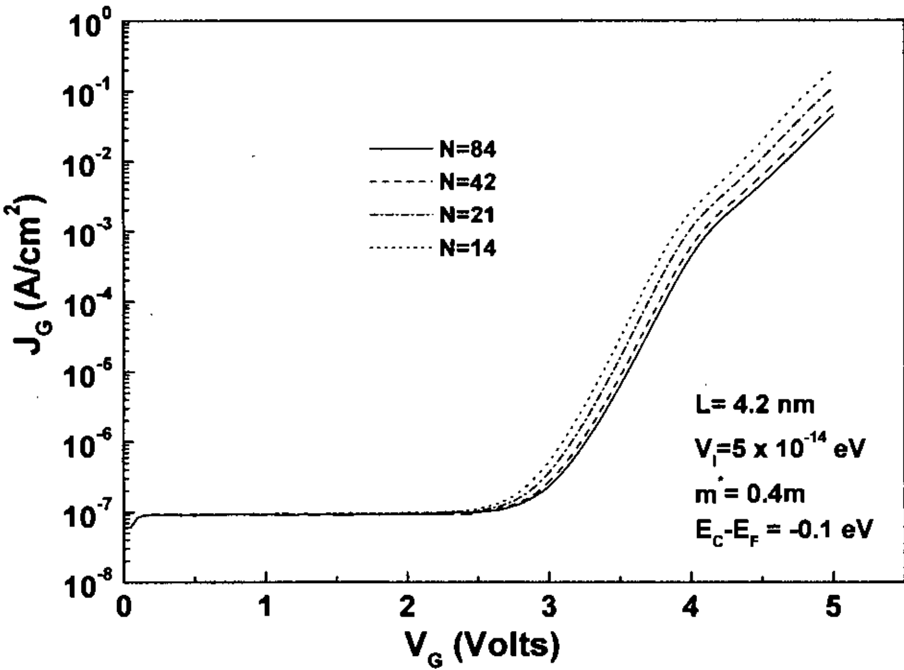

Fig. 4.2: Current density as a function of applied voltage with the oxide segment numbers as a parameter.

layer, varies between $0.25m_0$ and $1.03m_0$, as used by previous researchers [68],[69]. In this work the effective mass of electron inside SiO_2 is taken as $0.42m_0$.

In determining the oxide current density, Tsu-Esaki expression (Eq 3.21) is used. However, for estimating the current density, the variation of surface potential with the applied voltage is ignored. Such assumption has been made because in accumulation region the variation of the surface potential is less and a certain value of surface potential is attained for a small increase in applied voltage. The value of surface potential is comparatively small in his region, hence the quantization of electron energy is sufficiently less to ignore it keeping considerable amount of accuracy.

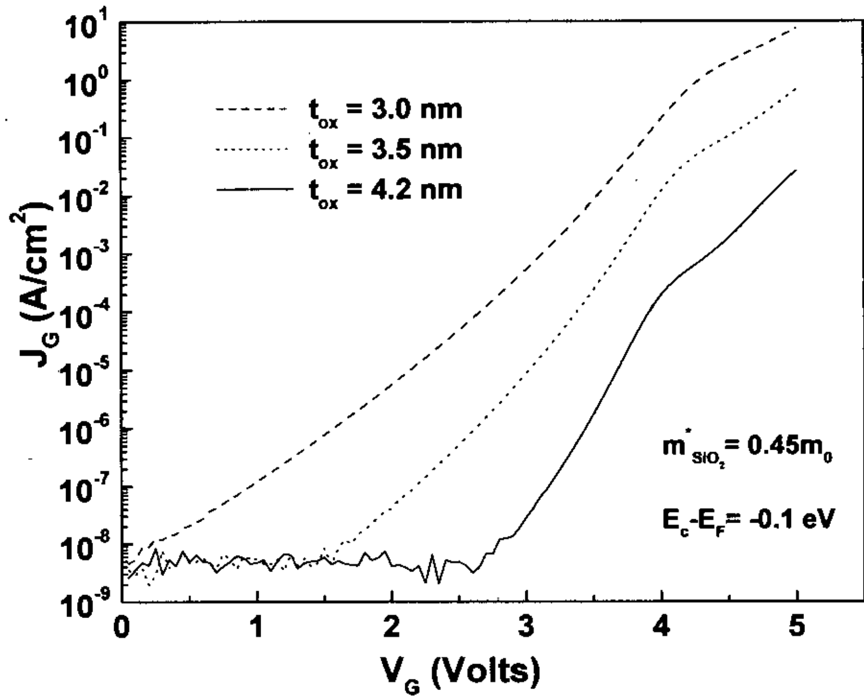

Fig. 4.3: Current density as a function of applied voltage with the oxide thickness as a parameter.

The current density through a 4.2 nm fresh gate oxide with the variation of applied voltage is presented in Fig. 4.2. The accuracy of the simulated results increases with the increase in oxide segment number. To keep sufficient accuracy and considerable computational time we took the oxide segment number, N=42 (ie. segment length l=0.2 nm).

The gate current shows different characteristics in two different regimes; the direct tunneling (DT) regime and the Fowler-Nordheim (FN) regime. In case of 4.2 nm gate oxides the direct tunneling current exhibits fluctuations (Fig. 4.3) when the applied voltage is less than 3V. However, the current rises sharply with the increase in the applied voltage as it enters the FN tunneling regime. In this regime the gate current shows an oscillating behavior [68] (the oscillations are absent in the results presented here as the gate voltage is limited to 5V).

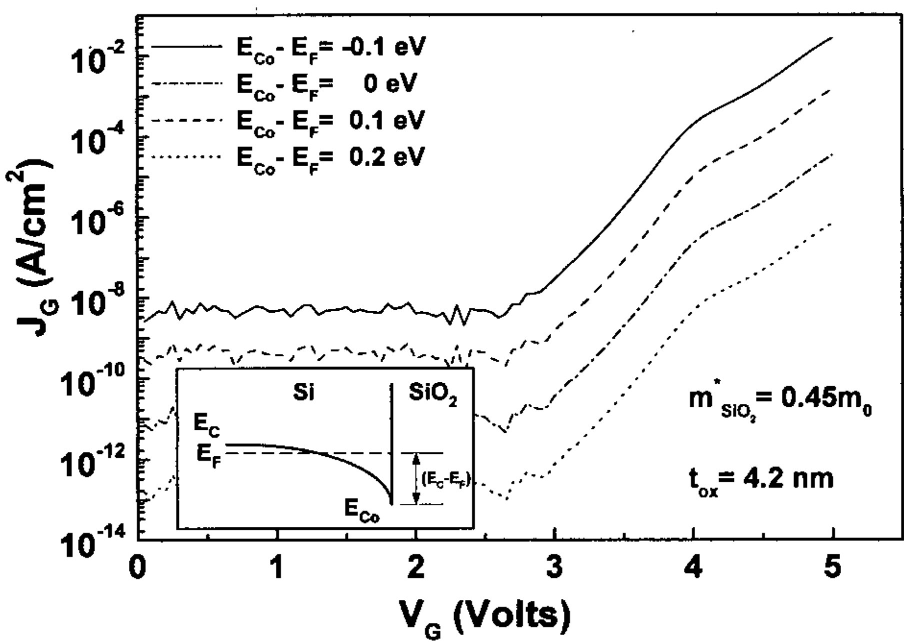

Fig. 4.4: Current density as a function of applied voltage for different values of the difference of the conduction band edge at the Si-SiO_2 interface and the Fermi energy inside Si.

Figure 4.3 reveals that the gate current is strong function of the oxide thickness and it increases exponentially as the gate oxide thickness is reduced [67]. For very thin oxides, especially below 3 nm there is a large increase in the direct tunneling current, where the electrons can tunnel from the inversion layer through the gate oxide into the positively biased gate.

If we consider the change in surface potential with variation of applied voltage, it is necessary to incorporate the change in the energy difference between the energy of the conduction band edge at the Si-SiO_2 interface (at x=0) and the Fermi energy (E_{Co}-E_F). Fig. 4.4 shows almost parallel shift of the I-V characteristics with variation of (E_{Co}-E_F).

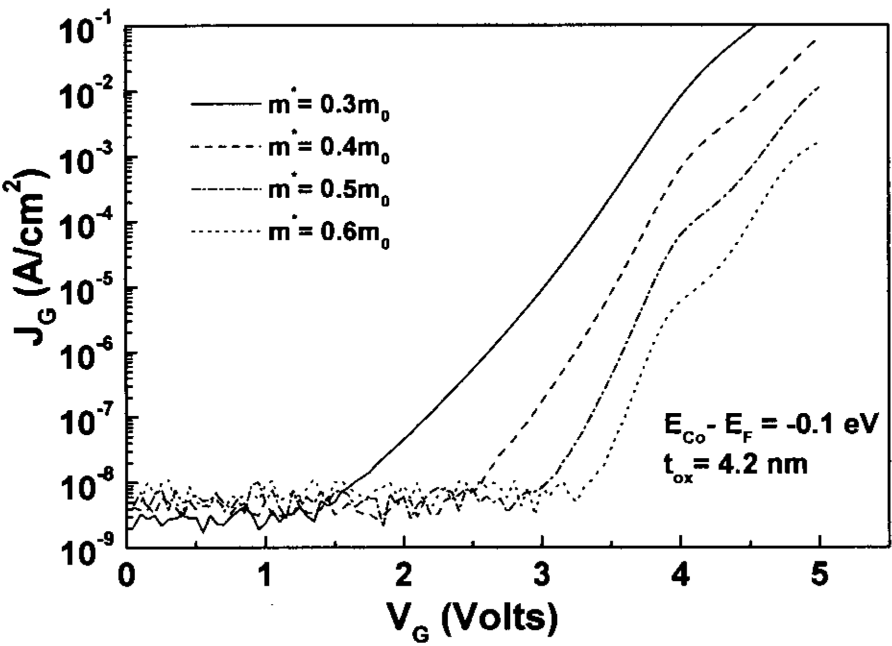

Fig. 4.5: Current density as a function of applied voltage for different electron effective mass.

In case of the electron effective mass inside the oxide, previous researchers [68],[69] used the values between $0.25m_0$ and $1.03m_0$. We used $0.42m_0$ in order to attain good match with the previously reported experimental data [46].The variation of the I-V characteristics with the electron effective mass is shown in Fig. 4.5. To incorporate the scattering effect in the oxide, complex potential, $V(x)=V_r(x)-iV_i(x)$ profile is introduced inside the oxide. The imaginary potential is related to the particle scattering lifetime, τ as $V_i = \hbar/2\tau$ [70]. For 4.2 nm thick oxide, change of V_i within small range causes noticeable change in current density for low voltage range which is shown in Fig. 4.6. The current density has a strong dependence on the potential barrier height of the oxide. Figure 4.7 shows that the barrier height lowering creates significant increase in the gate current.

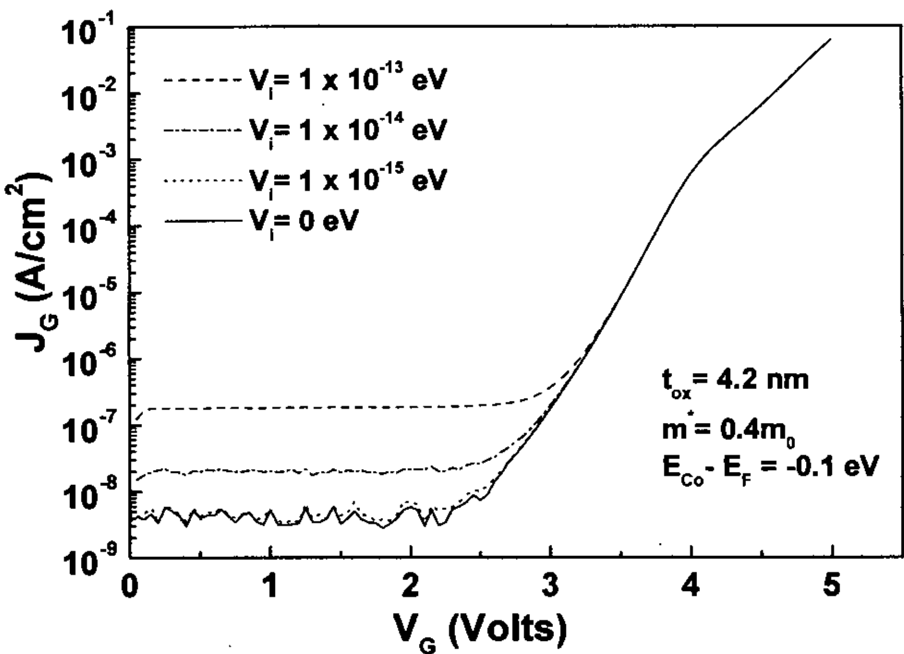

Fig. 4.6: Current density as a function of applied voltage- imaginary potential inside SiO_2 as a parameter.

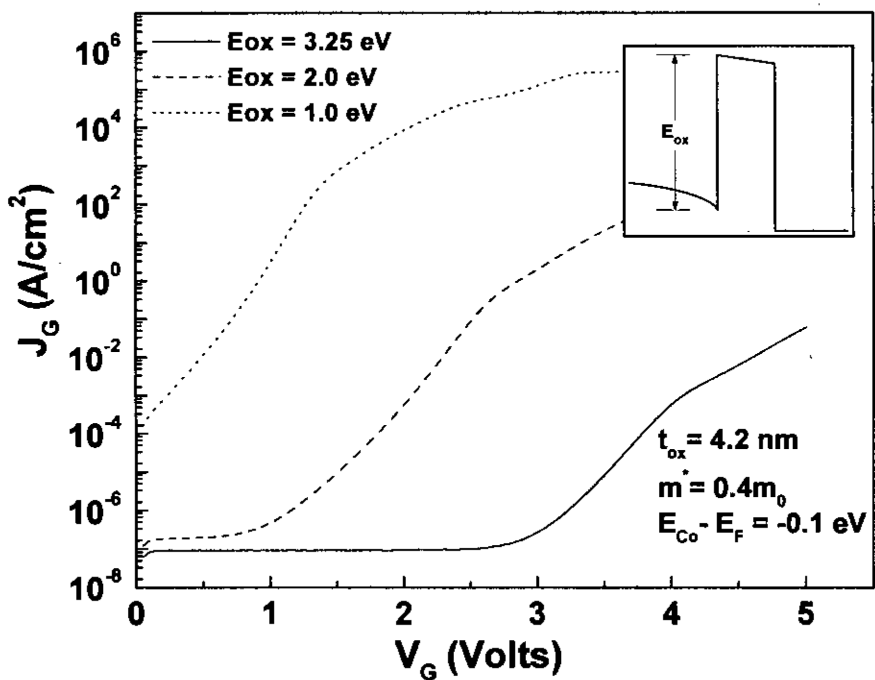

Fig. 4.7: Current density as a function of applied voltage-the height of the conduction band of oxide from the conduction band of Si at the interface as a parameter.

4.3 CHARACTERIZING THE SOFT BREAKDOWN SPOT

In section 2.8, the literature of Soft Breakdown Phenomena is discussed in details. Soft Breakdown spot is an extremely localized damage in the oxide [45]; however its conduction level is several orders lower than that of Hard Breakdown. It is proposed that the SBD path is created when a percolation path of non-linear resistors is created between adjacent traps [46].

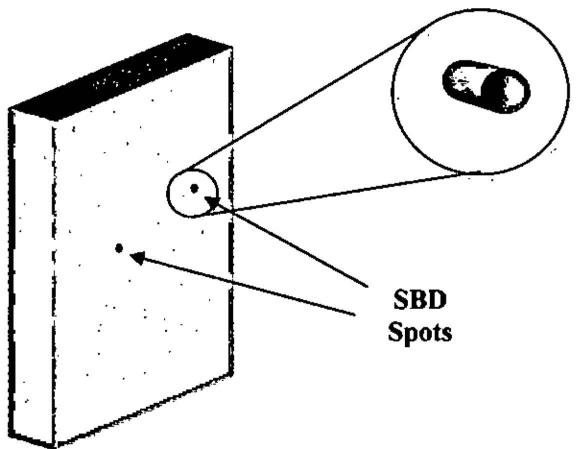

Fig. 4.8: Schematic representation of a degraded oxide with SBD spot. The SBD spot is assumed cylindrical.

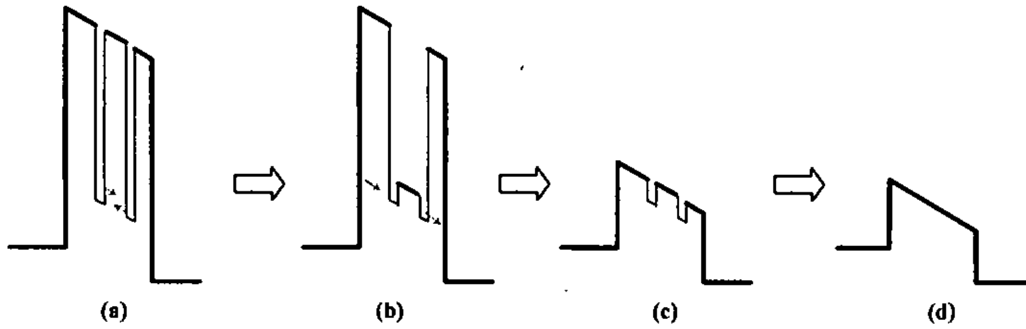

Fig. 4.9: Creation of a SBD path-its energy band diagram. (a) Initial trap generation, (b) Further degradation and creation of percolation path between adjacent traps, (c) Percolation path created between the two electrodes through the traps, (d) Representation of an SBD spot by lowered oxide barrier.

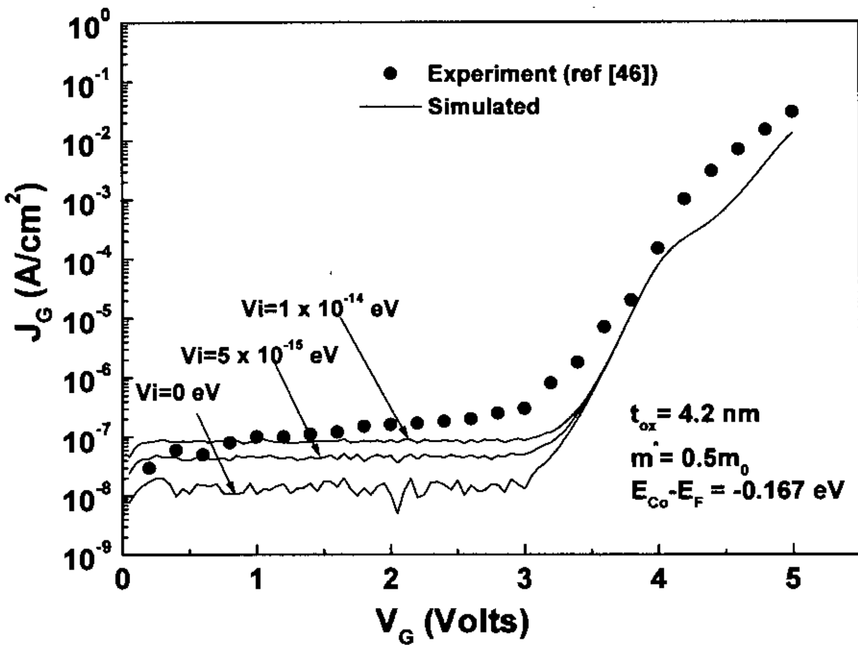

Fig. 4.10: Simulated Current density versus applied voltage curves for fresh oxide. Fitting the experimental data [46] by varying V_i.

During electrical stressing of MOS capacitor, electron traps are created in the SiO_2 and at the Si/SiO_2 interface [54]. Electron traps are found to be distributed throughout the upper SiO_2 energy gap between 0 to at least 3.0 eV below the conduction band edge [71].

As the SBD is the consequence of the percolation connection of these traps we propose that the SBD path has an effective barrier height whose conduction band edge is 0-3 eV below that of the unaffected barrier. Therefore, in this work the SBD spot is characterized as the barrier lowering. The SBD spot is assumed to be cylindrical.

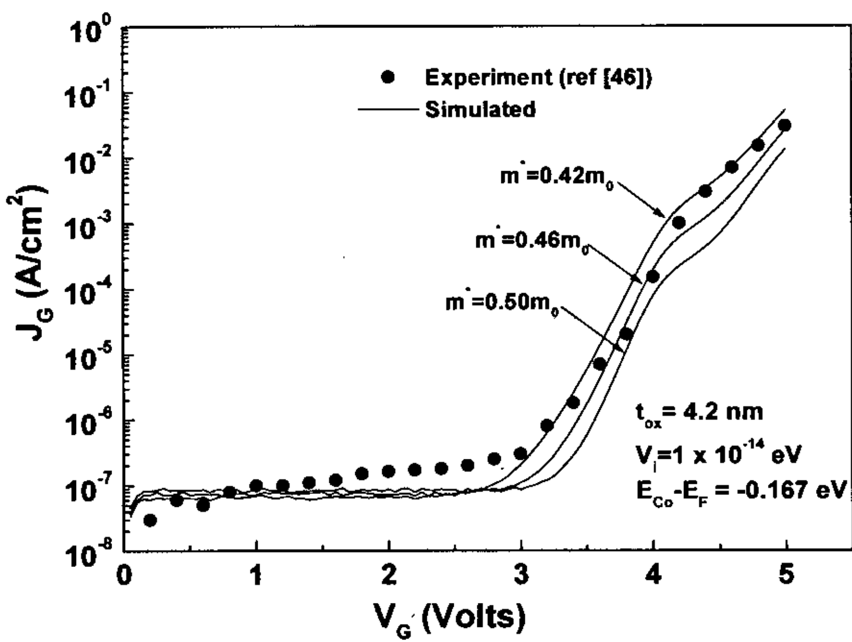

Fig. 4.11: Simulated Current density versus applied voltage curves for fresh oxide. Fitting the experimental data [46] by varying m^*.

The total current density is obtained using superposition of the current through the SBD spot and the current through the remaining area. Here, the remaining oxide other than that of the SBD spot is assumed to be unaffected. In reality, when electrical stress is applied the degradation occurs almost in the whole oxide area [25]. However, the SBD current is several orders larger than that of a non-SBD but degraded oxide. So, such assumption can be safely incorporated.

Fig. 4.10 and 4.11 show the simulated gate oxide current using the Tsu-Esaki relation. The imaginary potential and the effective mass of electron inside the oxide were varied to achieve better agreement with the experimental data. For obtaining better fit the imaginary potential and the effective mass is considered 10^{-14} eV and $0.42m_0$ respectively.

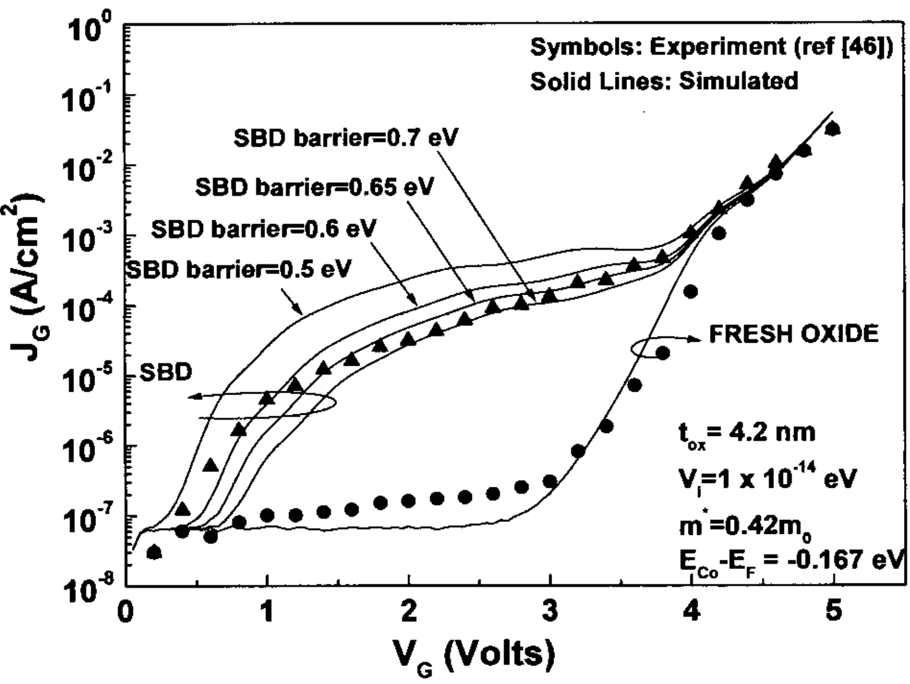

Fig. 4.12: Simulated SBD Current density- variation with the effective barrier height of the SBD spot. The oxide area is 3.14×10^{-4} cm^2. Effective mass of the electron is same throughout the specimen. SBD area was taken to be 10^{-14} cm^2 for simulation.

Lowering the barrier introduces a huge current in the low voltage region which closely matches the experimental data [46]. Current density with various SBD barrier heights was observed (Fig. 4.12). The SBD barrier height was measured from the conduction edge of Si at the Si/SiO_2 interface. Potential barriers with lower height achieve FN tunneling at lower applied voltage (Fig. 4.12). With the decrease in SBD barrier height, an increase in the current level is observable. However, this increase is more in lower voltage region than that in the higher voltage region.

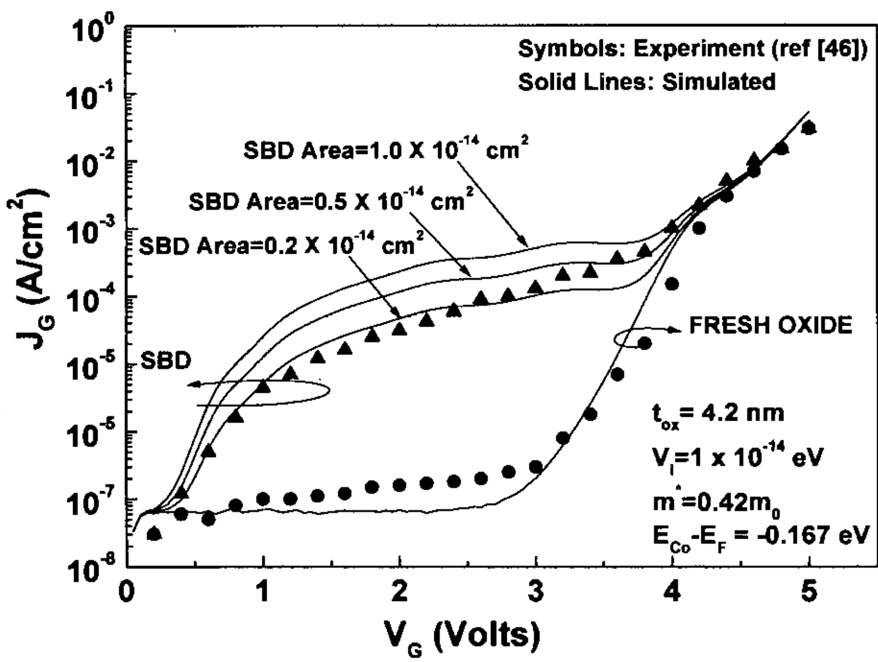

Fig. 4.13: Simulated SBD Current density- variation with area of the SBD spot. The oxide area is 3.14×10^{-4} cm^{-2} and the SBD barrier height here is 0.5 eV.

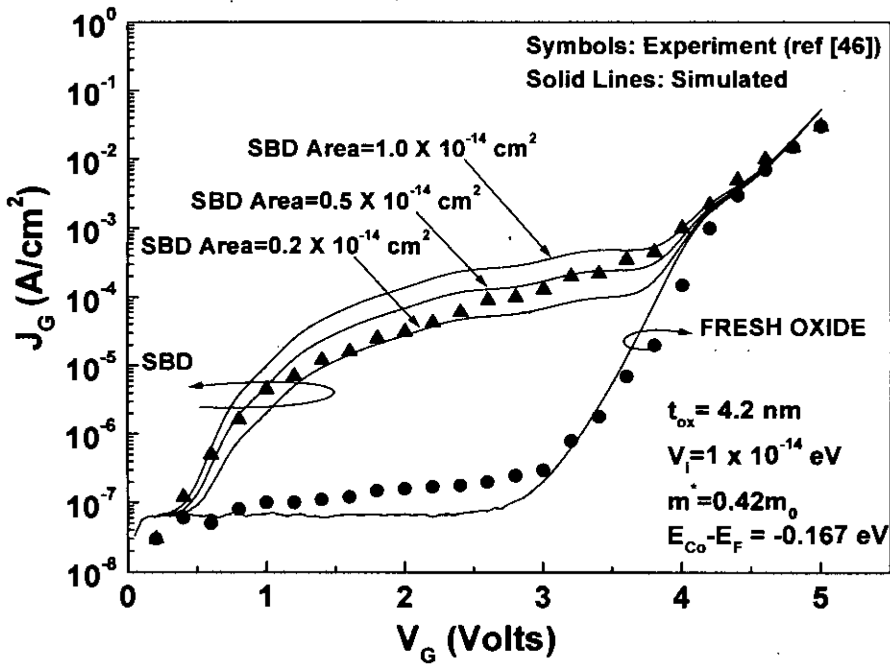

Fig. 4.14: Simulated SBD Current density- variation with area of the SBD spot. The oxide area is 3.14×10^{-4} cm^{2} and the SBD barrier height here is 0.55 eV.

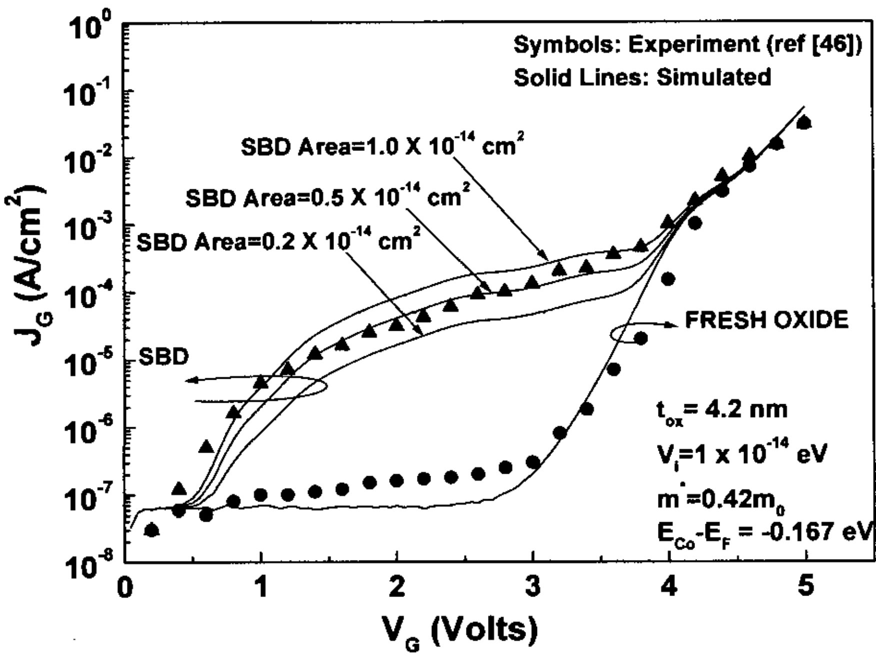

Fig. 4.15: Simulated SBD Current density-variation with area of the SBD spot. The oxide area is 3.14×10^{-4} cm^2 and the SBD barrier height here is 0.6 eV.

Moreover, these shapes exhibit oscillations that are due to the FN tunneling current. At higher voltage (>4V) the FN current of the fresh oxide suppresses the SBD current. Here, the SBD path is assumed to be 10^{-14} cm^2 [45]. However, we also simulated the SBD current density with the variation of SBD area.

Figures 4.13-4.15 show the current density through a Soft Broken down oxide with the variation of SBD spot area for three SBD barrier heights (0.5 eV, 0.55 eV and 0.6 eV). SBD barrier height with 0.6 eV and the spot area 0.5×10^{-14} cm^2 gives the best result so far. The curves exhibit slight oscillatory nature (a characteristic of FN current) for the electron effective mass less than $0.4m_0$ and greater than $0.5m_0$ (Fig. 4.16). Therefore, for the remaining simulations the effective mass of electron for the SBD spot is considered the same as that of the remaining oxide.

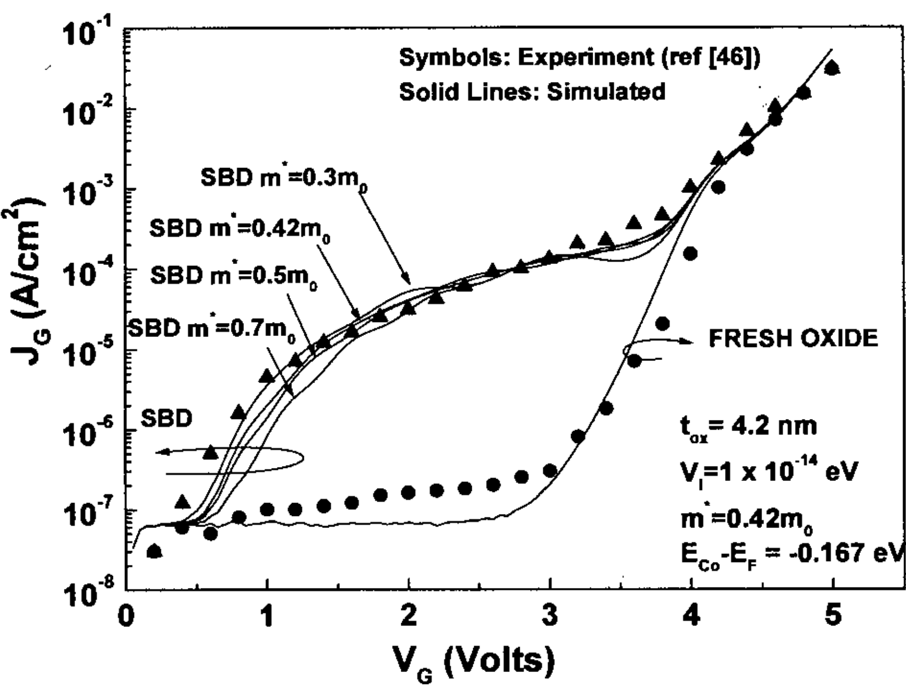

Fig. 4.16: Simulated SBD Current density- variation with the electron effective mass of the SBD spot. The oxide area is 3.14×10^{-4} cm^{-2} and the SBD barrier height here is 0.6 eV.

Though the SBD current exhibits close match when the SBD spot barrier height is 0.6 eV and the area is 0.5×10^{-14} cm^2, there is obvious discrepancy in the lower voltage region and in the higher voltage region (between 3.5V and 4V) before the FN current suppresses the SBD current. The discrepancy in the lower voltage region may have occurred because we did not consider the surface potential change with the variation of applied voltage. Also, to reduce simulation time we ignored the energy quantization.

In the process of simulating the SBD current we assumed that the remaining oxide other than the SBD spot is unaffected, however in reality the remaining oxide should have certain amount of degradation [25]. The degraded oxide will contribute oxide leakage current but this current is negligible compared to that of the SBD current for 4.2 nm oxides in the low voltage regime. However, in the higher voltage regime, the current is significant enough to cause an increasing I-V characteristic. This may be

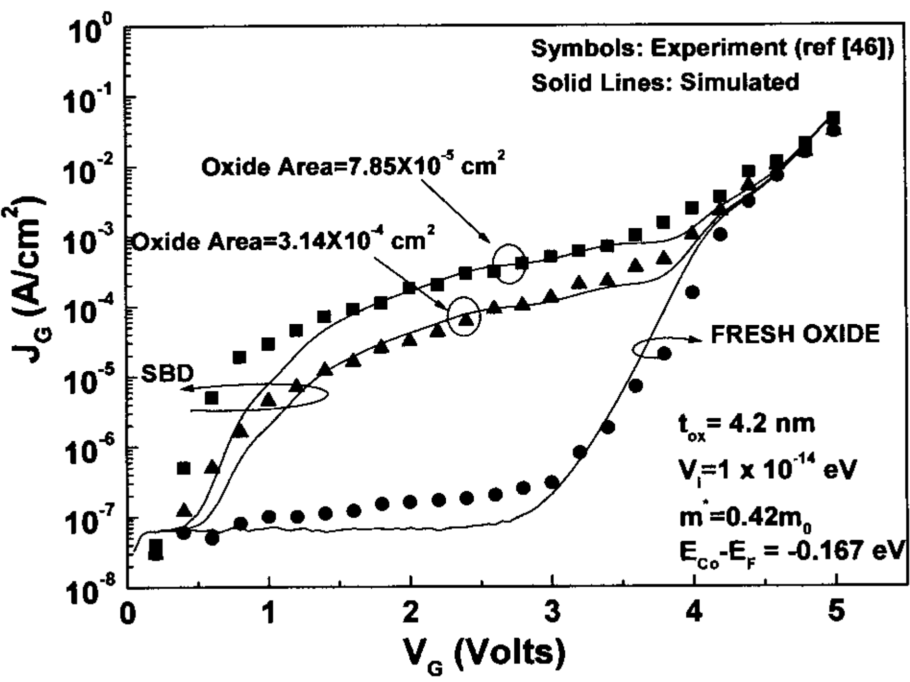

Fig. 4.17: Simulated SBD Current density for different oxide specimens. The SBD barrier height here is 0.6 eV.

the reason why there is a discrepancy in the higher voltage region between 3.5V and 4V. In Fig. 4.17, SBD current density for oxide specimens of different areas are simulated. As the oxide area decreases, the SBD current level will increase if we consider fixed SBD spot area (ie 0.5×10^{-14} cm^2). However, the SBD current is also dependent on the current stresses applied to create SBD.

CHAPTER 5

CONCLUSION

5.1 SUMMARY

In this study, post soft breakdown gate current is modeled using a quantum mechanical approach. This gate current was developed using the Tsu-Esaki expression, whereas the transmission co-efficient of electrons through arbitrary potential barriers was determined using generalized wave impedance method. The model is free from the rigorous simulations to evaluate the eigen energy state; however, it incorporates the physics based approach to characterize the properties of a Soft Breakdown spot.

The main objective of this study was to extract the properties of a Soft Breakdown spot of a degraded oxide specimen. It has been shown that the effective barrier height for a SBD spot becomes lowered significantly in comparison to the remaining oxide. The simulations show good agreement with reported experimental data [46]. The simulations were performed for an oxide thickness of 4.2 nm in the gate voltage range of 0-5 V.

It has been reported that the oxide traps are located 0-3 eV below the conduction band edge of the oxide [71]. As the SBD spot is created due to percolation path connection between adjacent traps, we propose that the SBD path should have a lowered barrier. In such case, as the SBD current is several orders lower than that of the Hard Breakdown, we assume that the barrier height inside the SBD spot is not totally eliminated. We proposed that the barrier height is 2.55 eV below the conduction band edge. The effective length and the effective mass of the SBD spot is assumed unaffected. The area of the SBD spot is taken to be 0.5×10^{-14} cm^2. A good agreement between the simulated results and reported experimental data was achieved.

5.2 SUGGESTION FOR FUTURE WORK

In this study, while determining the gate current, we ignore the energy quantization in the potential well at the Si-SiO_2 interface. 2-D Electron Gas model can be applied to increase the accuracy of the gate current simulation.

SBD pot is considered a lower barrier potential profile and the remaining oxide is considered unaffected. The degradation can be considered for the remaining oxide using the trap distribution throughout the oxide. Also the dependency of the degradation on the applied electrical stress can be considered for better results. An oxide specimen that has undergone SBD, may have further degradation while going through the experiments of I-V characteristic. So, the degradation of the SBD spot also can be made dependent on the applied electrical stress.

Our study is totally devoid of any time dependent property changes. The time dependent current fluctuations and the conductions are not considered here. A quantum mechanical model can also be formulated for a time dependent SBD damage.

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