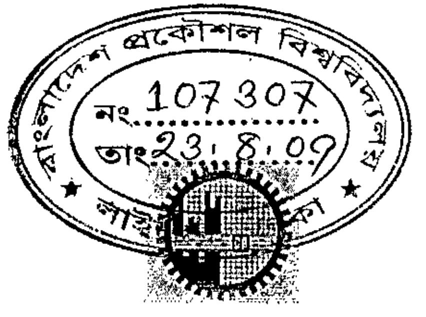
EFFECTS OF DYNAMIC STRESS INDUCED CHARGE TRAPPING IN STACK GATE DIELECTRICS OF SCALED MOS DEVICES

Sonia Ahsan

A thesis submitted to
The Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology, Dhaka, Bangladesh
in partial fulfillment of the requirements for the degree of
MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING



DEPT. OF ELECTRICAL AND ELECTRONIC ENGINEERING (EEE)
BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
(BUET)

August, 2009

The thesis titled "**EFFECTS OF DYNAMIC STRESS INDUCED CHARGE TRAPPING IN STACK GATE DIELECTRICS OF SCALED MOS DEVICES.**", submitted by Sonia Ahsan, Roll No: 100606230P, Session: October 2006 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of Master of Science in Electrical and Electronic Engineering on August 11, 2009.

BOARD OF EXAMINERS:

1. ______________________________

Dr. Quazi Deen Mohd Khosru — **Chairman** (Supervisor)
Professor
Department of Electrical and Electronic Engineering
BUET, Dhaka 1000, Bangladesh

2. ______________________________ 11/8/09

Dr. Aminul Hoque — **Member** (Ex-officio)
Professor and Head
Department of Electrical and Electronic Engineering
BUET, Dhaka 1000, Bangladesh

3. ______________________________ 11/08/2009

Dr. Md. Shafiqul Islam — **Member**
Professor
Department of Electrical and Electronic Engineering
BUET, Dhaka 1000, Bangladesh

4. ______________________________ 11/8/2009

Dr. Khairul Alam — **Member** (External)
Assistant Professor
Department of Electrical and Electronic Engineering
East west university, Dhaka 1212, Bangladesh

DECLARATION

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

Signature of the Candidate

SONIA AHSAN

ACKNOWLEDGMENT

First of all, the author would like to pay her gratitude to Almighty Allah for the successful completion of the work. The author expresses sincere gratitude and respect to her supervisor Dr. Quazi Deen Mohd Khosru, Professor, Department of EEE, BUET for his sincere guidance and supervision throughout the work. She is also thankful to Dr. Aminul Haque, Professor, Head, Dept. of EEE, BUET for his support and kind co-operation.

The author likes to express her gratitude to her siblings and parents for their selfless inspiration and encouragement throughout the progress of the work. She would like to express her profound gratitude to her husband, Farhan Shahil for his guidance and inspiration. The author likes to pay her gratitude to her in-laws and Athena who were also her source of inspiration.

Finally, the author reminds with gratitude the names of all those who were directly or indirectly involved with this work.

DEDICATION

To my Family

TABLE OF CONTENTS

Declaration iii

Acknowledgements iv

Dedication v

List of Figures ix

Abbreviations xii

Abstract xiii

CHAPTER 1 INTRODUCTION

1.1 General Overview 2

1.2 Literature Review 3

1.3 Scope of the Work 5

1.4 Thesis Layout 6

CHAPTER 2 HIGH-K GATE STACKS AND ITS IMPLICATION ON DEVICE CHARACTERISTICS

2.1 Introduction and Motivation 7

2.2 Background of MOSFETT 7

2.3 MOS Structure and Operation 8

2.4 MOSFET Scaling and Recent Trends 10

2.5 Quantum Confinement in MOS Structures 12

2.6 The Gate and Gate Dielectrics 14

2.7 Choice Of Hfo_2 as Gate Dielectrics 15

2.8 Electrical Characteristics of High-K Dielectrics 18

2.9 New Challenges for Hafnium Based Dielectrics 20

2.9.1 *Mobility degradation* 20

2.9.2 *Chare trapping/detrapping phenomena in gate dielectrics* 23
2.9.3 *Threshold Voltage (Vth) instability and reliability* 24

2.10 Conclusion 24

CHAPTER 3 CALCULATION OF TRAP ASSISTED LEAKAGE CURRENT DENSITY, DISSIPATED POWER DENSITY AND CHANNEL MOBILITY DEGRADATION

3.1 Introduction 26
3.2 Self-Consistent Model 27
3.3 Charge Trap Model 29
3.4 Trap Assisted Leakage Current Density and Dissipated Power Density 30
3.5 Mobility Calculation 32
3.6 Conclusion 37

CHAPTER 4 RESULTS

4.1 Introduction 38
4.2 Potential Profile of NMOS Structure 39
4.3 Threshold Voltage Shift 40
4.3.1 Threshold Voltage Shift vs Gate voltage as a function of Defect level
4.3.2 Polaron effect
4.3.3 Threshold Voltage Shift vs stress time as a function of gate Voltage
4.3.4 Threshold Voltage Shift vs Effective Oxide Thickness (EOT)
4.3.5 Threshold Voltage Shift under dynamic stress at different Gate voltage

4.3.6 Threshold Voltage Shift vs frequency

4.4 Trap Assisted Leakage Current Density (TALC) vs Gate Voltage 47

4.5 TALC vs HfO_2 Thickness At Different Bulk Trap Density 48

4.6 TALC vs Inversion Carrier Density 49

4.7 Comparison of TALC With Direct Tunneling Current (DTC) 50

4.8 Power Calculation 51

4.8.1 Dissipated Power density vs Gate voltage as a function of oxide thickness

4.8.2 Power density vs HfO_2 thickness at different bulk trap density

4.8.3 Power density vs Frequency at different oxide thickness

4.9 Mobility Calculation 55

4.9.1 Mobility vs Electric field

4.9.2 Mobility vs Electric field varying interfacial oxide thickness

4.10 Conclusion 56

CHAPTER 5 CONCLUSION

5.1 Summary 57

5.2 Suggestion for future work 58

References 59

LIST OF FIGURES

Figure 2.1 N-channel_enhancement-type_MOSFET. 9

Figure 2.2 Technology node and transistor physical gate length in Intel processors. 11

Figure 2.3 Potential well formed at oxide semiconductor interface. 12

Figure 2.4 Potential well formed at the oxide semiconductor interface. Horizontal lines represent the subbands. 13

Figure 2.5 Classical and quantum mechanical charge distribution inside semiconductor. 13

Figure 2.6 Various gate dielectrics and their dielectric constants, and concerns for the application into gate dielectrics. 16

Figure 2.7 Band offset of gate dielectric candidates with conduction band edge and valence band edge of Si substrate. 17

Figure 2.8 Schematic carrier mobility vs. vertical field in FETs in the universal mobility model, showing the mechanisms which limit the mobility, and their temperature dependences . 21

Figure 2.9 Carrier mobility of n-type Si, for various gate oxides, after Gusev et al. 22

Figure 4.1 Potential profile of a multi-stack (Si/SiO_2 /HfO_2/poly-Si) containing empty defect level and occupied defect level in the HfO_2 layer at positive gate bias. 39

Figure 4.2 Threshold-voltage shift as a function of gate voltage taking two empty defect levels and same occupied defect level. 40

Figure 4.3 Polaron effect is shown by taking $E_t = E^*_t$ = -0.4 eV in the simulation. 41

Figure 4.4 Threshold-voltage shift versus stress time for HfO_2/ poly-SiO_2 gate under constant voltage stress. 42

Figure 4.5 Threshold-voltage shift versus varying effective oxide thickness at a gate voltage of 2.5V. 43

Figure 4.6 Simulated threshold-voltage shift as a function of time during on and off stress at V = 2.0 V and 2.5 V. 44

Figure 4.7 Simulated threshold-voltage shift as a function of time during on and off stress at V = 2.5 V and five pulses. 45

Figure 4.8 Simulated threshold-voltage shift as a function of frequency at V = 1.5V. 46

Figure 4.9 TALC versus gate voltage at different oxide thickness. Here substrate doping density. 47

Figure 4.10 TALC versus gate voltage at different oxide thickness. 48

Figure 4.11 TALC versus inversion carrier density at different oxide thickness. 49

Figure 4.12 Comparison of TALC with DTC at different oxide thickness. 50

Figure 4.13 Simulated dissipated power density versus gate voltage with different oxide thickness. 51

Figure 4.14 Simulated dissipated power density versus gate voltage with different oxide thickness. 52

Figure 4.15 Dissipated power density as a function of frequency considering Vg = 1.8V considering thickness as a parameter. 53

Figure 4.16 Simulated mobility profile inside the channel. 54

Figure 4.17 Simulated mobility profile inside the channel with 1.67 nm EOT and 1.1 nm EOT. 56

ABBREVIATIONS

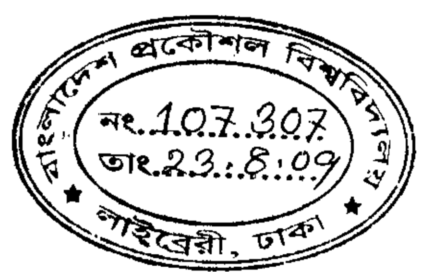
DTC	Direct Tunneling Current
FN	Fowler-Nordheim
EOT	Effective Oxide Thickness
MOSFET	Metal Oxide Field Effect Transistor
QMTC	Quantum Mechanical Transmission Co-efficient
QMWI	Quantum Mechanical Wave Impedance
QPC	Quantum Point Contact
TAT	Trap Assisted Tunneling
TDDB	Time Dependent Dielectric Breakdown
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration
TALC	Trap Assisted Leakage Current
WKB	Wentzel-Kramer-Brillouin

ABSTRACT

Charge trapping dynamics in hafnium based dielectric stacks and their impact on various device performances of scaled MOS devices is studied A theoretical model has been presented to incorporate the charge trapping/detrapping mechanism in hafnium based dielectric stacks followed by studying the properties of carriers in inversion layers solving coupled Schrödinger's and Poisson's equations self consistently. Several important characteristics of device such as power dissipation, effect of dynamic stress, trap assisted leakage current density, threshold voltage instability, polaron effect and channel mobility degradation are investigated with decreasing effective oxide thickness as well as increasing gate voltage. Then the simulated results are compared with the reported experimental results.

CHAPTER 1

INTRODUCTION



1.1 GENERAL OVERVIEW

In order to provide better performance and higher packing density on the limited space, scaling down of the channel length is essential in ULSI fabrication technologies. Although the thermally grown or rapid thermally grown oxynitride with Effective Oxide Thickness (EOT) of 18~25Å has been introduced in the manufacturing area for the replacement of SiO_2 to further scale technology, the technology for beyond that still needs further thickness scaling of SiO_2 or oxynitride and is approaching the scaling limits. Therefore, new materials such as high-k dielectrics and metal gate electrodes have been investigated in order to ensure continued scaling of the technology. Among multiple candidates such as Ta_2O_5, TiO_2, Al_2O_3, Y_2O_3, La_2O_3, ZrO_2, the HfO_2-based material has been presently considered the most attractive candidate for the gate dielectric application due to its high k value, better device performance and thermal stability, etc. However, various challenges for high-k devices implementation include low mobility and threshold voltage instability, which can be affected by the quality of the interfacial oxide and charge trapping. In particular, transient charge trapping was proposed to be one of the main resources for mobility reduction. Even though several process modifications, such as nitridation and silicate formation, suggest the ways for improvement of high-k dielectrics device performance, the effect of these changes has not been yet studied systematically. The reliability issues of the hafnium-based dielectrics, such as Time Dependent Dielectrric Breakdown (TDDB), bias temperature instabilities, and hot carrier stability, needs to be addressed in order to introduce high-k technology in 45 nm technology node. Metallic impurity such as Hf and Ta could penetrate through dielectric layer resulting in degraded bulk minority carrier lifetime and inversion carrier mobility.

To minimize transient charging behavior in high-k devices, pulsed I-V measurement has been proposed. Using pulsed I-V measurement technique, the effects of interface treatment and dielectric stacks on transient characteristics of high-k transistors were studied. The results based on varying pulse frequency and t_{rise} & t_{fall} supported that bulk traps appeared to be a main factor for threshold voltage shift. The results of bias instability suggested that the stress induced mobility degradation was primarily related with interface degradation.

From the study of transient charge trapping/detrapping characteristics in high-k n/pMOSFETs, transient charge trapping has been found to be an interface thickness limited phenomenon. Additionally, transient electron trapping/detrapping was dominant even in pMOSFETs.

High-k ring oscillator circuit study suggested that high-k device would operate in close to intrinsic mode in the actual circuit operation. At high Vdd regime, the propagation delay for high-k devices was shorter than that of SiO_2. However, in the lower Vdd regime, high-k device showed slower circuit performance due to charge trapping.

Using ultra-short pulse measurement technique, we could get near intrinsic I-V curves of high-k devices. Mobility degradation was still observed even though negligible charge trapping takes place during ultra-short pulse measurement. Remote charge scattering appeared to be the main cause of intrinsic mobility degradation. Again, it was confirmed that trapped charges appear to locate in the bulk high-k layer rather than at the interfacial layer.

1.2 LITERATURE REVIEW

Aggressive scaling down of MOSFETs continues to reduce the feature sizes into deep submicron regime. The continuous scaling of MOSFETs, as outlined in International Technological Roadmap for Semiconductor Devices [1], requires that the Equivalent Oxide Thickness (EOT) to become as thin as 0.5 nm in some cases in the next 10 years. However such thin SiO_2 suffers due to excessive direct tunneling current (DTC) and reliability problems. To overcome these problems, SiO_2 should be replaced by suitable high-k materials as gate insulators [1]. Using high-k (dielectric constant) material, both thicker physical thickness and several orders of magnitude lower gate leakage current can be achieved with similar oxide capacitance. While high-k materials can help to solve gate leakage problems, high densities of traps within high-k gate dielectrics adversely affect the device performance [2] in different ways. Trapping of charges in the preexisting bulk trap center inside high-k materials arises some important issues such as threshold voltage instability, dissipated power density and higher trap assisted leakage current density. Charge trapping dynamics in Hafnium based dielectric stacks and their impact on

the threshold voltage instability was studied by several researchers [3], [4], [5]. But the last two unnoticed issues (dissipated power density and higher trap assisted leakage current density) must be studied before using high-k material as a gate dielectric material. With further thinning of the gate oxide thickness, these trapped charges may detrapped through the oxide/gate interface. In paper [6], Farhan et al investigated the effect of detrapped charges from the oxide trap centers to the gate electrode on the threshold voltage shift. Such detrapping would reduce the amount of charges trapped in the dielectric, resulting in a reduction of the threshold voltage shift [6]. Garross et al [7] have also incorporated this detrapping term in their model but found the effect almost negligible during negative half of the ac cycle. In our paper [6], we concluded that the impact of these two simultaneous processes on device performance during positive half of the ac cycle should be studied. Also some other issues such as dissipated power density trap assisted leakage current density should be studied before neglecting these detrapped charges with farther scaling.

Over the last 10 years the power dissipation in the lead microprocessor has increased by a factor of 2.5 per generation, saturating at about 100 W levels [8]. Not only that, in present technologies that as SiO2 as the gate dielectric (90, 65 and some of 45 nm), there is a significant contribution of increasing gate leakage current. In contrast to the past researcher [9] this trend may be continued, with the introduction of high-k dielectrics having high bulk trap density. The mechanism will rapidly increase in severity as scaling proceeds. Various types of power dissipation and the details of these effects along with other scaling issues have been described by frank [10]. In case of using high-k materials having high bulk trap density such as HfO_2, ZrO_2; Al_2O_3 as a gate dielectric dissipated power density should be re-calculated incorporating this detrapping mechanism.

Moreover gate leakage current density should also be recalculated incorporating trap assisted leakage current density with further thinning of oxide thickness. Scaling down allows the same performance with reduced voltage, leading to low power. As devices shrink to sub-micron dimensions, the supply voltage must be reduced to avoid damaging electric fields. This development, in turn, requires a reduced threshold voltage. On the other hand, for a given voltage, leakage current increases exponentially with a decrease in V_{th}. Further, leakage occurs as long as power flows

through the circuit. This constant current can produce an increase in the chip temperature, which in turn causes an increase in the thermal voltage, leading to a further increase in leakage current. In some cases, this circle results in unconstrained thermal runaway. Also the poor future power scaling, combined with previously applied aggressive performance scaling techniques has made power the number one problem in modern chip design since high performance circuit will dissipate too much power.

Fully understanding the charge trapping/detrapping mechanism is the key to understanding device related issues associated with the high-k dielectrics. These detrapped charges may affect the device performances answering the question how far scaling can go with high-k dielectric materials having large bulk trap density. In this connection, here we study the leakage current density contributed by these detrapped charges and the dissipated power density associated with them.

1.3 SCOPE OF THE WORK

With the advent of high-k dielectrics gate oxide can be scaled below keeping the gate leakage current density lower. But due to excessive bulk trap density of high-k dielectric, we believe, further scaling may be prohibited due increasing leakage current density as well as dissipated power density and these terms should be further studied for successful high-k integration into the Si CMOS technology. As systems became more power constrained, optimizing the power became more critical, viewing power reduction from an optimization perspective provides valuable insights. So Charge trapping /detrapping phenomena has become a decisive criterion as it makes the threshold voltage unstable. However, before their final integration in industry, significant issues remain to be overcome as there are mobility degradation, metal gate incompatibility and threshold voltage instability. To address this last issue it becomes important to know the trapping/detrapping mechanisms in pre-existing defects. Although these models are useful for providing qualitative explanations, a device-level numerical model is nonetheless necessary to

quantitatively analyze the origin and impact of the electrical instability in such multi stack systems.

1.4 THESIS LAYOUT

This thesis consists of five chapters of which chapter one gives an introduction followed by literature review and objective of this study.

Chapter 2 deals with brief description of MOSFET fundamentals and charge trap behavior and gate current. It also contains a brief description of the origin of traps creation, oxide degradation and an overview of charge trapping phenomenon.

In Chapter 3, threshold voltage calculation, dissipated power density, mobility degradation and the trap assisted discharged current density expression for MOS capacitors are discussed.

The simulation results are presented in Chapter 4 based on the expressions developed in Chapter 3. Conclusive remarks and discussions are given in chapter 5.

CHAPTER 2

HIGH-K GATE STACKS AND ITS IMPLICATION ON DEVICE CHARACTERISTICS

2.1 INTRODUCTION AND MOTIVATION

The MOSFET (Metal-Oxide-Silicon Field-Effect- Transistor) or MOS Transistor (MOST) is a three dimensional electronic device. It operates on the conductivity modulation principle in a thin semiconductor layer by a controlling electric field to give amplifying and switching functions between three electrical terminals (input, output and common) connected to the film.

It is the building block of the complex Integrated Circuits (IC), such as microprocessors, graphics, and Digital Signal Processing (DSP) chips. Each IC packs more than 100 million MOS transistors on a single chip. Integration of one billion transistors into a single chip will become a reality before 2010.

2.2 BACKGROUND OF MOSFET

A conceptually similar structure was first proposed and patented by Lilienfeld and Heil in 1930, but was not successfully demonstrated until 1960. The main technological problem was the control and reduction of the surface states at the interface between the oxide and the semiconductor. The operating principle of the MOSFET transistor was first described in Lilienfield's historical patent issued in 1926. It took another 34 years before Dawon Kahng and Martin Atalla successfully built a working MOSFET in 1960.

For the past 40 years, the semiconductor industry and academia have relentlessly pushed transistor scaling. Along with scaling, the MOSFET transistor evolved from the p-MOSFET in the 1960's to the n-MOSFET in the 1970's. A good understanding of gate oxide quality, such as interface traps, fixed and mobile charges, and a good control of gate oxide quality in a manufacturing environment enabled industry to make the transition from PMOS technology to a higher-performing NMOS technology in 1970's. Initially it was only possible to deplete an existing n-type channel by applying a negative voltage to the gate. Such devices have a conducting channel between source and drain even when no gate voltage is applied and are called "depletion-mode" devices.

A reduction of the surface states enabled the fabrication of devices which do not have a conducting channel unless a positive voltage is applied. Such devices are refered to as "enhancement-mode" devices. The electrons at the oxide-semiconductor interface are concentrated in a thin (~10 nm thick) "inversion" layer. By now, most MOSFETs are "enhancement-mode" devices.

2.3 MOS STRUCTURE AND OPERATION

A traditional metal–oxide–semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO_2) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon (the latter is commonly used). As the silicon dioxide is a dielectric material, its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor.

When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor. If we consider a P-type semiconductor (with N_A the density of acceptors, p the density of holes; $p = N_A$ in neutral bulk), a positive voltage, V_G, from gate to body (Figure 2.1) creates a depletion layer by forcing the positively charged holes away from the gate-insulator/semiconductor interface, leaving exposed a carrier-free region of immobile, negatively charged acceptor ions . If V_G is high enough, a high concentration of negative charge carriers forms in an inversion layer located in a thin layer next to the interface between the semiconductor and the insulator (unlike the MOSFET where the inversion layer electrons are supplied rapidly from the source/drain electrodes, in the MOS capacitor they are produced much more slowly by thermal generation through carrier generation and recombination centers in the depletion region). Conventionally, the gate voltage at which the volume density of electrons in the inversion layer is the same as the volume density of holes in the body is called the threshold voltage.

This structure with P-type body is the basis of the N-type MOSFET, which requires the addition of an N-type source and drain regions.

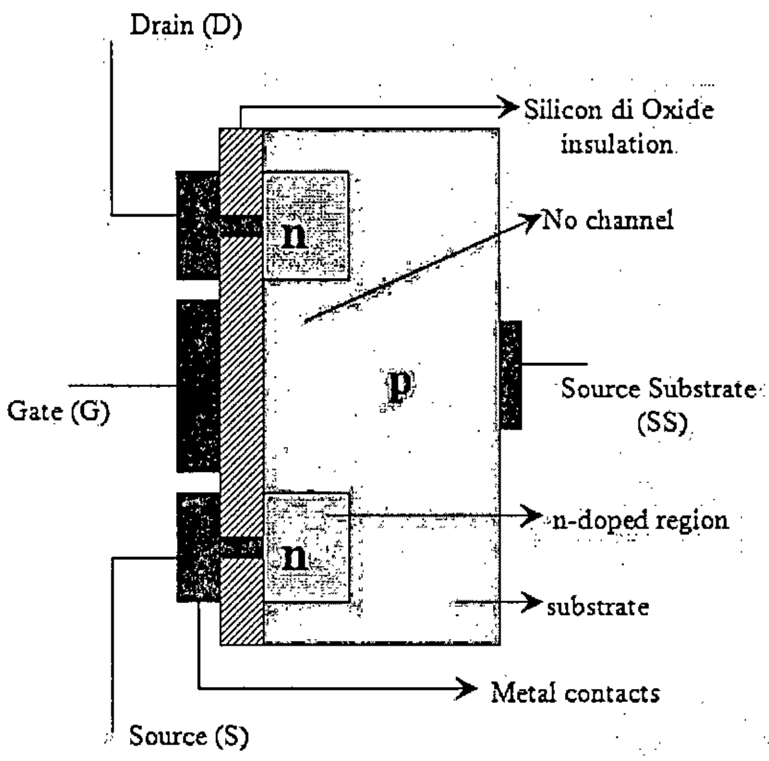


Fig. 2.1: N-channel_enhancement-type_MOSFET [11]

A metal–oxide–semiconductor field-effect transistor (MOSFET) is based on the modulation of charge concentration by a MOS capacitance between a body electrode and a gate electrode located above the body and insulated from all other device regions by a gate dielectric layer which in the case of a MOSFET is an oxide, such as silicon dioxide. If dielectrics other than an oxide such as silicon dioxide (often referred to as oxide) are employed the device may be referred to as a metal–insulator–semiconductor FET (MISFET). The MOSFET includes two additional terminals (source and drain), each connected to individual highly doped regions that are separated by the body region. These regions can be either p or n type, but they must both be of the same type, and of opposite type to the body region. The source and drain (unlike the body) are highly doped as signified by a '+' sign after the type of doping.

If the MOSFET is an n-channel or nMOS FET, then the source and drain are 'n+' regions and the body is a 'p' region. As described above, with sufficient gate voltage,

above a threshold voltage value, electrons from the source (and possibly also the drain) enter the inversion layer or n-channel at the interface between the p region and the oxide. This conducting channel extends between the source and the drain, and current is conducted through it when a voltage is applied between source and drain. For gate voltages below the threshold value, the channel is lightly populated, and only a very small subthreshold leakage current can flow between the source and the drain.

If the MOSFET is a p-channel or pMOS FET, then the source and drain are 'p+' regions and the body is a 'n' region. When a negative gate-source voltage (positive source-gate) is applied, it creates a p-channel at the surface of the n region, analogous to the n-channel case, but with opposite polarities of charges and voltages. When a voltage less negative than the threshold value (a negative voltage for p-channel) is applied between gate and source, the channel disappears and only a very small subthreshold current can flow between the source and the drain.

The source is so named because it is the source of the charge carriers (electrons for n-channel, holes for p-channel) that flow through the channel; similarly, the drain is where the charge carriers leave the channel.

The device may comprise a Silicon On Insulator (SOI) device in which a Buried Oxide (BOX) is formed below a thin semiconductor layer. If the channel region between the gate dielectric and a Buried Oxide (BOX) region is very thin, the very thin channel region is referred to as an Ultra Thin Channel (UTC) region with the source and drain regions formed on either side thereof in and/or above the thin semiconductor layer. Alternatively, the device may comprise a SEMiconductor On Insulator (SEMOI) device in which other semiconductors than silicon are employed. Many alternative semicondutor materials may be employed.

2.4 MOSFET SCALING AND RECENT TRENDS

Over the past decades, the MOSFET has continually been scaled down in size to achieve lower switching time, reduces cost and lower power consumption. Typical MOSFET channel lengths were once several micrometres, but modern integrated circuits are incorporating MOSFETs with channel lengths of less than a tenth of a micrometre long. Indeed Intel will begin production of a process featuring a 65nm

channel length in early 2006. Until the late 1990s, this size reduction resulted in great improvement to MOSFET operation with no deleterious consequences.
In order to increase circuit functionality and performance at lower cost, the scaling of integration technology was always one of the top priorities for semiconductor business and has aggressively driven that the semiconductor research became the quintessence of the technology and science in present-day.
Fig 2.1 shows how the technology node and transistor physical gate length in Intel processors has changed [12].

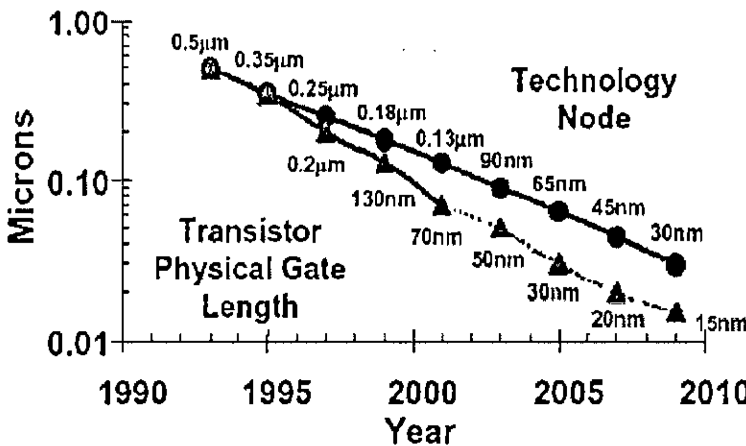


Fig. 2.2 Technology node and transistor physical gate length in Intel processors [2].

For the last four decades, the improvement of speed and shrinkage of chip area of integrated circuits were achieved by scaling down of physical thickness of the SiO_2 gate dielectrics and gate length (L). When the dimensions of a MOSFET are scaled down, both the voltage level and the gate-oxide thickness must also be reduced [13]. However, beyond the 100 nm node technology, SiO_2 has reached its physical limitations: higher leakage current and reliability concerns. Continuing scaling down of the MOSFET device with the minimum feature size of 90 nm and below requires EOT (Equivalent Oxide Thickness) less than 15 Å. A 10-15Å-thick SiO_2 layer corresponds to only around 3-4 mono-layers of SiO_2. In this thinner EOT range, SiO_2 suffers from leakage current too high to be used (particularly) for low power operation due to the direct tunneling of electrons.

The most advanced MOS transistors used in volume production today are probably those of Intel's used in their 130nm logic technology with transistor gate length and gate oxide thickness are 60nm and 1.5nm, respectively. At IEDM 2003 [14], Intel presented a manufacturing-ready 90nm technology, with transistor gate length 50nm and gate oxide thickness 1.2nm. As of 2nd half of 2004, 90nm technology is at the beginning of manufacturing life cycle at a very limited number of top semiconductor manufacturers. For majority of IC manufacturers, 90nm technology is in the qualification stage or in the middle of development.

2.5 QUANTUN CONFINEMENT IN MOS STRUCTURE

It has been well known since the late sixties, that for a better description of the MOS structure, the conventional semi-classical approach is not very adequate. In the semi-classical approach, the density of states above the conduction band is assumed to be continuous, and using this continuous density of states model and the Fermi function, the classical description of the electron concentration can be obtained. This approach works well if the bands are slowly varying compared to the electron's deBroglie wavelength. However, in case of an MOS C, Fig. 2.3 shows that the band bending near the surface can form a quantum well, which introduces energy quantization. So the semi-classical approach does not work well for these problems, and for a precise description a quantum mechanical approach has to be used.

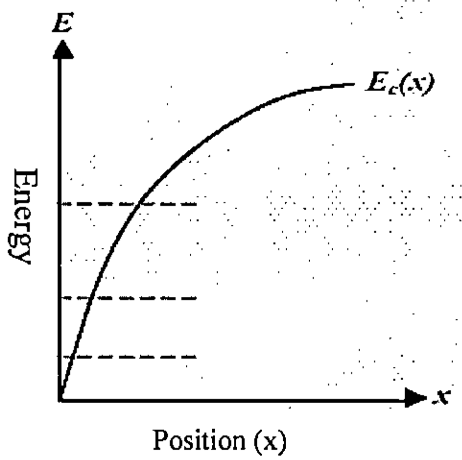


Fig. 2.3: Potential well formed at oxide semiconductor interface.

So far we have outlined the mechanics of the quantum mechanical calculation for MOS structures. What we understood is: why we need quantum approach and how we solve the problem quantum mechanically. But, we may want to know how these quantum results differ from the semi-classical result. There are actually two key effects. To see this let us consider Fig. 2.4 and 2.5. Figure 2.4, shows one of the effects, that is the quantization of the energies above conduction band, which is assumed to be continuous in classical model. The direct effect of these on MOS capacitors or on MOSFETs is an increase of threshold voltage, because the threshold voltage is approximately the gate voltage for which, the conduction band goes below the Fermi level. However, due to the energy quantization, the lowest level that electrons occupy is not the bottom of conduction band, rather it is the first energy level, which is little higher than the conduction band edge. So to bend this band below the Fermi level, a little more gate voltage is needed. This gives rise to a threshold voltage rise in MOSFETs.

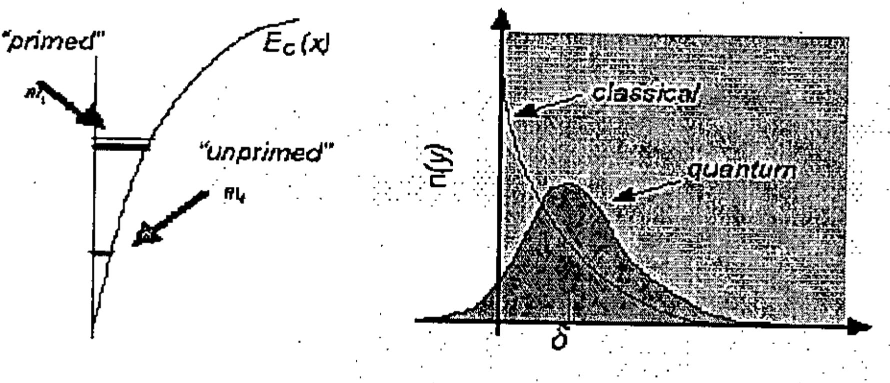


Fig. 2.4: Potential well formed at the oxide semiconductor interface. Horizontal lines represent the subbands.

Fig. 2.5: Classical and quantum mechanical charge distribution inside semiconductor.

Another effect comes from the spatial distribution of inversion charge. Both the classical and the quantum distribution of inversion charge along the depth of the device (x direction) are shown in Fig. 2.4. The classical distribution shows a peak at the oxide semiconductor interface while the quantum mechanical distribution is totally different from that and shows a peak inside. The net effect is that the actual profile (quantum mechanical) has an average distance from the surface that is larger

than that predicted by the classical calculations. As we know, the average carrier distance has the effect of increasing the effective oxide thickness. Thus the quantum mechanical calculation predicts a larger effective oxide thickness, which means a lower gate capacitance. Thus for a certain gate voltage, the amount of inversion charge will be somewhat smaller than that, predicted by the classical analysis. This is more important as the oxide thickness becomes smaller with each technology generation.

2.6 THE GATE AND GATE DIELECTRICS

Early MOSFET used metal (such as aluminum) as a gate electrode; hence the name MOSFET was came. However, in fabrication processes high temperature causes metal to melt. Moreover, MOSFETs with metal gates have higher threshold voltage. Thus poly-crystalline silicon was preferable to metal as gate material as it has higher melting point. However, polysilicon is highly resistive (approximately 1000 times more resistive than metal) which reduces the signal propagation speed through the material. To lower the resistivity, dopants are added to the polysilicon. Sometimes additionally, high temperature metal such as Nickel layered onto the top of the polysilicon which decreases the resistivity. Such a blended material is called silicide. The silicide-polysilicon combination has better electrical properties than polysilicon alone and still does not melt in subsequent processing. Also the threshold voltage is not significantly higher than polysilicon alone, because the silicide material is not near the channel.

In case of the Gate Oxide, the insulator should be of high insulating property to resist leakage current from gate to the channel. As the device is scaled down, the tunneling phenomena becomes prominent leading to an increased power consumption. (The various degradation of oxide are discussed in the following sections). Insulators that have a larger dielectric constant than SiO_2, such as group IV(B) metal silicates e.g. Hafnium and Zirconium Silicates and Oxides, are now being researched to reduce the gate leakage. Increasing the dielectric constant of the gate oxide material allows a thicker layer while maintaining a high capacitance. The higher thickness reduces the tunneling current between the gate and the channel. An

important consideration is the barrier height of the new gate oxide; the difference in conduction band energy between the semiconductor and the oxide will also affect the leakage current level. For the traditional gate oxide, silicon dioxide, the former barrier is approximately 3 eV. For many alternative dielectrics the value is significantly lower, somewhat negating the advantage of higher dielectric constant.

2.7 CHOICE OF HfO_2 AS GATE DIELECTRIC

High-k gate dielectrics have been studied as alternative gate dielectrics for the 70 nm technology node and beyond to replace conventional SiO_2 or silicon oxynitrides (SiOxNy).

Principal requirements for high-k dielectric applications are

- high dielectric constant
- high band offset with electrodes (i.e. barrier height) to suppress leakage current thermally and chemically stable in contact with Si substrate.
- It must have a high enough K that it will be used for a reasonable number of years of scaling.
- The oxide is in direct contact with the Si channel, so it must be thermodynamically stable with it.
- It must be kinetically stable, and be compatible with processing to 1000 °C for 5 seconds.
- It must act as an insulator, by having band offsets with Si of over 1 eV to minimise carrier injection into its bands.
- It must form a good electrical interface with Si.
- It must have few bulk electrically active defects.

In Fig. 2.6, dielectric constants of high-k candidates were summarized. TiO2 and barium strontium titanate (BST) showing profoundly higher k in Fig. 2.6, were reported not to be thermally stable with silicon substrates [15]. It is worth mentioning that high-k dielectrics such as BST with a too high dielectric constant (>100) does not seem to be appropriate since the high dielectric constant causes field

induced barrier lowering (FIBL) which degrade short channel effects of MOSFETs [16].

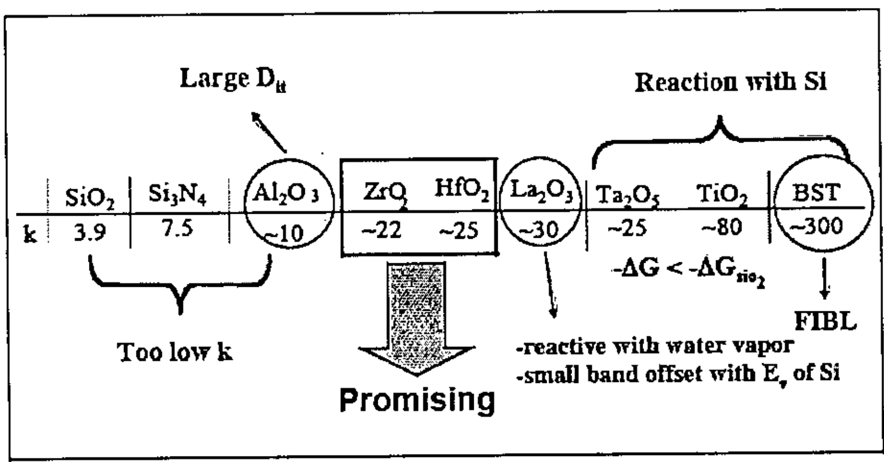


Fig. 2.6 Various gate dielectrics and their dielectric constants, and concerns for the application into gate dielectrics [17].

According to a report [18], band offset less than 1.0 eV may lead to an unacceptably large leakage current. Based on the band offset in Fig. 2.7, Ta_2O_5, which has been studied widely for the application in DRAM storage capacitors appears to be inappropriate for the gate electrode application. Al_2O_3 and Si_3N_4 have too low k to be used for several generations as shown in Fig.2.7. Among these materials, HfO_2 has been shown to be compatible with poly-silicon gate , poly-SiGe , and TaN gates. In contrast, ZrO_2 has been reported that it was not compatible with poly-Si gate due to the reaction of Zr with poly-Si gate.

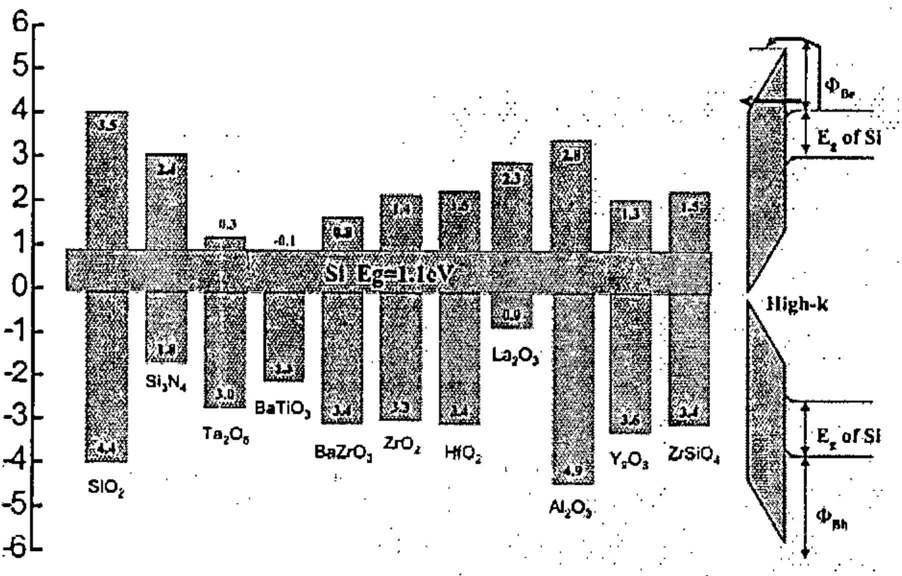


Fig. 2.7 Band offset of gate dielectric candidates with conduction band edge and valence band edge of Si substrate [19].

MOSFETs with HfO_2 dielectrics and TaN gate showed very low EOT (~10-12Å) and low leakage current even after the conventional CMOS process flow [10]. Considering the cost of development and implementation, HfO_2 gate dielectric needs to span two or three generations from the 75 nm to the 35 nm design rule. To meet the requirements for these generations, EOT should be scaled down to less than 10 Å while suppressing leakage current to below 1 A/cm^2 [20].

Among the high-k dielectrics being studied, HfO_2 appears promising due to its relatively high dielectric constant (25) as compared to Si_3N_4 and Al_2O_3 [21], its relatively high free energy of reaction with Si (47.6 Kcal/mole at 727 C) as compared to TiO_2 and Ta_2O_5, and its relatively large bandgap (5.8 eV). Although there has been some recent work done on HfO_2 and its MOS capacitors [22], [23], the charge-trapping properties of this material are still unclear. In this thesis, the effects of stress voltage, trapping time, backward detrapping, and gate electrode on charge trapping in HfO_2 are reported.

One problem with high K oxides is that they contain much higher defect concentrations than SiO_2. The SiO_2 possessed such a low concentration of defects for three reasons. First, its high heat of formation means that offstoichiometry defects such as O vacancies are costly and so are rare. The second is that SiO_2 has covalent bonding with a low coordination. The covalent bonding means that the main defects are dangling bonds, and the low coordination allows the SiO_2 network to relax to remove any dangling bonds by rebonding the network. This occurs in particular for defects at the Si: SiO_2 interface. The high K oxides differ in that their bonding is ionic, and they have higher coordination number. The greater ionic character of the bonding and the higher coordination numbers mean that the high K oxides are poorer glass formers. The effect of poor glass forming ability and high coordination is that the oxides have higher defect concentrations. The oxides have very high heats of formation, so the equilibrium concentration of non-stoichiometric defects should be low (except where mixed valence is possible, such as TiO_2). However, the non-equilibrium concentration of defects is high, because the oxide network is less able to relax, to rebond and remove defects.

2.8 ELECTRICAL CHARACTERISTICS OF HIGH-K DIELECTRICS

Currently Hf based material has been extensively investigated in order to overcome the intrinsic disadvantages of HfO_2 such as lower crystallization temperature, formation of interfacial oxide layer with Si substrate, low channel mobility, etc. Nitrogen8 incorporation into dielectric and Si surface nitridation by NH3 has proved that these fabrication techniques are effective to reduce EOT [22, 23]. Si or N incorporation has shown the improvement of thermal budget before the crystallization of dielectric, which resulted in leakage current reduction. Also optimization of annealing condition with forming gas or deuterium has demonstrated the improvement of electrical characteristics, particularly channel electron mobility [24, 25]. However, there are still lots of issues to be concerned. Due to the significant preexisting traps and fast transient charge trapping/detrapping, it is not easy to understand the electrical characteristics of high-k device using the conventional characterization technique for SiO_2 based devices [26, 27]. Reduced transistor performance in high-k dielectric such as reduced carrier mobility,

saturation current, and hysteresis was addressed that trapped charges during the conventional measurement were the primary reason. These trapped charges have very small time constant. Therefore, these easily jump up to the trap sites in dielectric layer and go back to substrate during very short characterization time. To characterize these transient charges, transient measurement technique has been proposed for high-k devices [28, 29].

For mobility characterization, the most important parameter is inversion charge density. The electron mobility was usually calculated from drain current-gate bias (Id- Vg) curve and gate to channel capacitance (Cgs) vs. Vg curves of the MOSFETs using a well-known equations (1) ~ (3).

Effective mobility of carrier can be expressed by a simple equation (1),

$$\mu_{eff}(V_g) = \frac{I_d/V_d}{(W/L)Q_{inv}(V_g)} \tag{2.1}$$

where $\mu_{eff}(Vg)$ and $Q_{inv}(Vg)$ represent effective mobility and inversion charge density as a function of gate voltage, respectively. If gate to channel capacitance (Cgs) is measured as a function of gate voltage, then $Q_{inv}(Vg)$ is calculated from an integration of the Cgs for Vg from accumulation regions to V_g by equation (2). In addition, effective field E_{eff} is a function of inversion charge and depletion charge (Q_D) with a relationship of equation (3).

$$Q_{inv}(V_g) = \int_{-\infty}^{V_g} C_{gc}(V_g)dV_g \tag{2.2}$$

$$E_{eff} = \frac{(0.5Q_{inv} + Q_D)}{\varepsilon_{Si}} \tag{2.3}$$

Some researchers reported that the reduced carrier mobility came from the under or overestimation of the inversion charge density using conventional capacitor-voltage measurement [30, 31]. They proposed the inversion charge extraction method using

ideal C-V correction technique and modified charge pumping technique. Interface formation on silicon surface that affect increasing of EOT and pinning effect with gate electrode is one of the biggest issues in high-k research and its effects on device characteristics is under investigation. Even though various attempts have been proposed, charge trapping characteristics of high-k devices has not fully understood yet. Therefore, it is worth further systematic studying on the transient characteristics of Hf-based dielectric device.

2.9 NEW CHALLENGES FOR HAFNIUM BASED DIELECTRICS

2.9.1 Mobility degradation

In the several years study, hafnium based dielectric transistors were suffering from severe mobility degradation and poor interface state quality due to low-quality sub-oxide formation from high-k dielectric during and after annealing processes. Charge trapping and phonon scattering were proposed to be the main cause of mobility degradation. The mobility issue is complicated by the fact that mobility values demonstrate dependence on the gate stack EOT. Therefore, different process solutions may be needed for high performance (small EOT) and low power (greater EOT) applications. Process solutions yielding ~80% universal SiO_2 mobility have been reported only for EOT ~ 15 Å, while the high performance EOT range has not yet been addressed. Recently it was suggested that thinning HfO_2 could improve mobility. However, thin film quality at the scaling limit is often poor, making it difficult to simultaneously achieve mobility, EOT and Jg targets. Obtaining more than 90% universal SiO_2 mobility value is required to make use of high-k device in future technology.

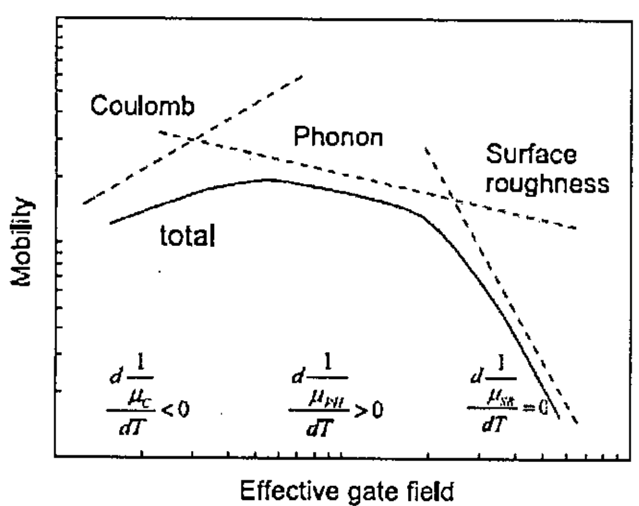


Fig. 2.8. Schematic carrier mobility vs. vertical field in FETs in the universal mobility model, showing the mechanisms which limit the mobility, and their temperature dependences .

The objective of device scaling is to create smaller, faster devices. Speed follows source-drain drive current, which in turn depends on the carrier mobility. Carriers in the FET behave like a two-dimensional electron gas. The carrier density is determined by the vertical gate field which induces them, by Poisson's equation. The carrier mobility in 2D gases is found to depend in a universal way on this gate field, according to the so-called universal mobility model. This idea developed from observations by Sah, Plummer [32] and others. The most recent version is by Takagi et al. [33] in which the mobility of electrons and holes depends only on the effective gate field and the Si face, [100], [110] or [111]. The individual components of mobility add according to Matthiessen's rule,

$$\frac{1}{\mu} = \frac{1}{\mu_C} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}}. \tag{2.4}$$

The mobility is limited by different mechanisms at different fields, as each obeys a different power law with field, see Figure 2.8. At low fields, mobility is limited by Coulombic scattering (C) by trapped charges in the oxide and/or channel and/or the gate electrode interface; at moderate field it is limited by phonon scattering (PH),

and at high fields by scattering by surface roughness (SR). CMOS devices with a SiO_2 gate oxide have mobility close to the universal limit. The mobility is limited mainly by interface roughness over the range of interest. The mobilities in devices with high K gate oxides presently lie well below the universal curve. This is particularly true of NMOS devices. The reduction in mobility for PMOS devices is fractionally less. Figure 2.9 shows typical examples.

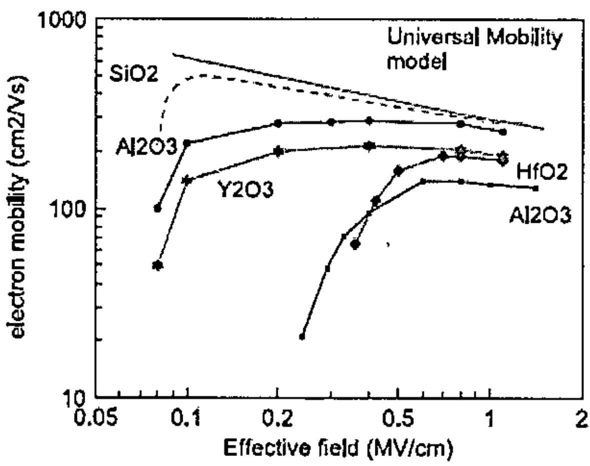


Fig. 2.9. Carrier mobility of n-type Si, for various gate oxides, after Gusev et al. [32].

A major objective of present research is to understand the cause of this lowered mobility and to try to correct it. The cause is presently not well understood. There are two likely causes. First, there could be scattering by excessive amounts of trapped charge and interface states [34]. This is clearly true as other measurements show that high K oxides have much more trapped charge than SiO_2. Secondly, there is the possibility of remote scattering by low lying polar phonon modes, as noted by Fischetti et al. [35]. The two contributions can be distinguished by their temperature and by their thickness dependence. It is also possible that the reduced mobility is due to a reduced induced channel carrier density in inversion, due to the filling of interface traps. This effect has been analyzed in detail by Ma et al. [36]. It can be excluded by direct measurements of Hall effect mobility which also shows a reduction.

2.9.2 Charc trapping/dctrapping phcnomcna in gatc diclcctrics

We have already noted that high-K oxides possess a larger bulk density of defects and trapped charge than SiO_2 [37]. It is now well known that the channel mobility in a high-k gated MOSFET is typically much lower than its SiO_2-gated counterpart. Since it is also well known that high-k gated MOSFET tends to have more oxide charge and interface traps than its SiO_2-gated counterpart. It should be noted that trapping/detrapping time constants for some of the high-k gate dielectrics, including HfO_2 and Al_2O_3, are much shorter than those for SiO_2 [38], and therefore the DC measurement methodology commonly used for MOS devices with SiO_2 gate dielectric will likely to miss these traps. A transient (pulsed) measurement methodology has been introduced to reveal more fully the traps in high-k gate dielectrics [38]. Charge trapping leads to instability in the flat band voltage and gate threshold voltage. It is seen as hysteresis on a drive current vs. gate voltage plot. The effect can be demonstrated by charge pumping experiments. It is notable that HfSiOx gate oxides have less hysteresis than HfO_2 and also that nitrogen addition reduces it below 70 meV. The amount of trapped charge can be reduced by various annealing cycles and by design of the oxide. It would also be helped by a clearer understanding of its origin. The origin of this trapped charge is becoming clearer. The first source is intrinsic defects in the oxide and interface traps. Zafar et al. [39] showed that trapping in HfO_2 and Al_2O_3 occurs by the filling of existing defect levels rather than the creation of new defects. This indicates that bulk defects in high K oxides are a serious problem. Kumar [40] showed that hot carriers can create additional defects, but this is an additional effect. The trapped charge can be reduced by annealing. This can be carried out in forming gas (N_2/H_2 mixture), or other nitrogen containing gases such as ammonia.

The detrapping process can originate from three possible mechanisms. The first may be due to a back tunnelling of electron from traps to substrate and the second, resulting from a Poole–Frenkel-like electrons conduction from traps to traps toward the gate electrode, which we have neglected . And the third mechanism is tunneling of electrons from channel to poly-silicon gate.

2.9.3 Threshold Voltage (V_{th}) instability and reliability

One of main issues for high-k gate stack is the charge trapping characteristics during reliability test. Initial observation of instability was studied through capacitance-voltage (CV) characteristics in flat-band voltage change and current-voltage (IV) change. Since electrons can be trapped and detrapped in the high-k dielectrics with a minimal residual damage to its atomic structure, a threshold voltage instability associated with electron trapping/detrapping in high-k layer can significantly affect the transistor parameters and complicate the evaluation of the effects of stress-induced defect generation phenomenon on the high-k gate stacks, which typically is not an issue in the case of SiO2 dielectrics. Pulsed based Id-Vg technique is proposed to monitor charge trapping characteristics. However origin of the charge trapping have not been clearly understood yet. Intrinsic properties of high-k film have been refocused based on pulse measurement. Since those charge trapping affect significantly on Vth measurement and reliability characteristics, comprehensive study is required to detail understand and find the solution for high-k/metal gate stack.

2.10 CONCLUSION

Here in this chapter the choice of high-k dielectrics as a replacement of conventional SiO_2 is described. But due to higher bulk trap in HfO_2 another problem arises which is threshold voltage instability. In this dissertation effect of trapped charges on mobility degradation has been discussed. Another noticeable phenomena is with the further shrinking (EOT<2nm) of oxide thickness charges get detrapped through the gate oxide interfaces increasing dissipated power density which has been considering as a major disadvantages to take high-k dielectric instead of conventional SiO_2

CHAPTER 3

CALCULATION OF TRAP ASSISTED LEAKAGE CURRENT DENSITY, DISSIPATED POWER DENSITY AND CHANNEL MOBILITY DEGRADATION

3.1 INTRODUCTION

Over the past decades, the MOSFET has continually been scaled down in size to achieve lower switching time, reduces cost and lower power consumption The scaling trend for gate dielectric is such that for sub-100 nm generation devices an equivalent gate oxide thickness of less than 2 nm will be required. In order to meet the requirement, the conventional gate oxide dielectric will need to be replaced by higher dielectric constant materials. Hafnium based dielectrics are being widely investigated as a potential replacement for the silicon oxi-nitride. However, before the final integration in to the industry, several important issues, such as mobility degradation, metal gate incompatibility and threshold voltage instability is needed to be considered. As high k oxides posses a large bulk density of defects, charge trapping leads to instability in the gate threshold voltage. Although there is some recent work done on HfO_2 and its MOS capacitor, the effect of charge trapping needs further investigation to ascertain the quality of performance.

The Physical limitations of the conventional silicon dioxide as gate dielectric has reached the point where films thickness are only a few atomic layers thick [41]. This results in high leakage current and degrades the device performance. To get around this critical problem, high-k dielectrics such as hafnium, zirconium, aluminum oxides [42] have been introduced. In fact, while keeping the EOT constant high-k dielectrics allow us to increase the physical thickness of the gate stack. Hence, the gate leakage is found to be reduced by 2 to 3 orders of magnitude. Despite extensive investigation on the use of high-k dielectrics, many critical problems still remain which are yet to be explored. These problems include defects in the dielectrics which can lead to mobility degradation, metal gate incompatibility, power consumption and threshold voltage instability. As high-k dielectrics posses a large bulk density of defects, charge trapping leads to instability in the gate threshold voltage. Charge trapping dynamics in hafnium based dielectric stacks and their impact on the threshold voltage instability was studied by several researchers [3-5, 39,43]. Effect of charge trapping on threshold voltage instability has also been modeled recently [5, 6]. Before using high-k materials as a potential replacement of SiO_2 several issues such as dissipated power density, mobility degradation, capacitance etc. should be considered. To address these issues not only high quality

films need to be deposited but also excellent electrical characteristics need to be obtained before high-k materials can be integrated into standard CMOS technology [44].

In this work, these issues are investigated incorporating both forward and backward detrapping. A model is developed to explain the mechanism of trapping detrapping phenomena in high-k stack gate dielectrics. Several important characteristics of device such as power dissipation, capacitance, threshold voltage instability, effect of stress voltage and stress time and channel mobility degradation are investigated.

3.2 SELF-CONSISTENT MODEL

External electric fields can change the properties of semiconductor surfaces significantly, and the consequences of such changes have been systemically explored for many years. More recently there has been considerable work on the quantum effects that arise when band bending confines the carriers to a narrow surface channel. To model the effects of quantum confinement, quantum allows the self-consistent solution of the Schrödinger equation with Poisson's equation. Properties of carriers in MOS inversion layers are studied by solving coupled Schrödinger's and Poisson's equations self-consistently within the effective-mass approximation.

The 1D Schrödinger Equation is given by

$$\left[-\frac{\hbar^2}{2m_{Zi}}\frac{d^2}{dz^2}+eV(z)\right]\psi_{ij}(z)=E_{ij}\psi_{ij}(z) \tag{3.1}$$

Here m_{Zi} is the effective-mass perpendicular to the interface in the ith valley, V (z) is the electrostatic potential and E_{ij} and Ψ_{ij} are the eigenenergy and the wave function corresponding to the jth subband in the ith valley.

The potential is calculated from Poisson's equation which is as follows

$$\epsilon_0 \epsilon_r \frac{d^2 V(z)}{dz^2} = -[\rho_{dep}(z) - en(z)] \tag{3.2}$$

Where n(z) represents the total inversion electron density. The inversion layer electron can exist only at eigen energies and their spatial distribution in described by the respective wave function. Under such conditions, n(z) is calculated from

$$n(z) = \sum_{ij} (n_{vi} m_{di} k_B T / \pi\hbar^2) \ln\left(1 + \exp\left(\frac{E_F - E_{ij}}{k_B T}\right)\right) \times \left|\psi_{ij}\right|^2 \tag{3.3}$$

Where n_{vi} and m_{di} are the velley degeneracy and the density of states effective mass for the ith valley, respectively.

The boundary conditions commonly used to solve Schrödinger's equation are that the wave function goes to zero at z = 0 and at z = 1 where z = 0 is at the silicon-oxide interface and z = 1 is deep inside silicon [45].

In this thesis, we use a technique, based on Green's function formalism, to solve Schrödinger's equation with wave function penetration. This technique is described in detail in [46], [47]. Open boundary conditions are used, which are based on the assumption that the potential profile is flat at deep inside the gate metal as well as at deep inside the bulk semiconductor. Our assumption implies that the wave function deep inside the semiconductor is exponentially decaying and deep inside the gate metal, the wave function is a plane wave.

The eigenenergies of the quasi-bound states are calculated by locating the peaks of the one-dimensional (1-D) density-of-states [47]. The corresponding wave functions including penetration can easily be obtained using the relationships described in [48]. Once the eigen-energies and the wave functions are calculated, the self-consistent formulation is applied with appropriate modifications to include penetration effects also in the solution of Poisson's equation. Since a fraction of inversion charge resides within the gate-oxide due to wave function penetration,

Poisson's equation is solved for the combined oxide and semiconductor regions with the boundary conditions applied at the gate metal-oxide interface

3.3 CHARGE TRAP MODEL

A rate equation [3.4] for the distributed trapped electrons incorporating detrapping of electrons to the gate is developed as follows

$$\frac{dn_t}{dt}=\frac{n}{N_O}\cdot\frac{N_t-n_t}{\tau^*}\left[\frac{1}{1+\exp((E_t^*-E_f)/kT)}\right]-\frac{n}{N_O}\cdot\frac{n_t}{\tau_1}\left[1-\frac{1}{1+\exp((E_t-E_f)/kT)}\right]$$
$$-\frac{n_g}{N_{og}}\cdot\frac{n_t}{\tau_2}\left[1-\frac{1}{1+\exp((E_t-E_{fm})/kT)}\right] \tag{3.4}$$

where n_t is the trapped electron density, N_t the density of the uniform bulk traps in HfO_2, n the electron concentration in the channel, N_0 a unit normalization factor, E^*_t the empty defect level, E_t the occupied defect level, E_f the channel electron quasi-Fermi level. In this model, the tunneling of trapped electrons to the gate has been neglected, due to lowering of charged trap levels.

The equation basically consists of three terms, the first term represents the charge trapping rate from the channel and the second term accounts for the detrapping of the trapped charges back to the channel and the third term of the Eqn.3.4 incorporates the detrapping of electrons to the poly-silicon gate, where E_{fm} is the poly-silicon gate Fermi level, τ^* is the tunneling time constant for the forward trapping process from channels to trap. τ_1 is the tunneling time constant for the detrapping process from occupied defect state to the channel and τ_2 is the tunneling time constant for the detrapping process from occupied defect states to the gate. All these time constants are obtained using WKB approximation [49]. For the forward tunneling process from channel to traps, it is given by

$$\tau^*=\tau_O\exp\left[\frac{4\sqrt{2m^*m_O}}{3\hbar qE}\times\left(\left(E_C^{OX}-E_t^*-qEx\right)^{\frac{3}{2}}-\left(E_C^{OX}-E_t^*\right)^{3/2}\right)\right] \tag{3.5}$$

Considering the fact that, trap level in the oxide layer is at a high energy level from the Fermi level of the gate, trapping from the gate side is neglected.

The detrapping time constant from occupied defect states to the gate for any position y inside the high-k dielectric is expressed as

$$\tau_2 = \tau_o \exp\left(\frac{4\sqrt{2m^*}}{3\hbar qE} \times \left(\left(E_c^{ox} - E_t + qEy\right)^{\frac{3}{2}} - \left(E_c^{ox} - E_t\right)^{\frac{3}{2}}\right)\right) \tag{3.6}$$

For calculating the detrapping time constant from occupied defect states to the channel, x is replaced by y, where x is the depth of the trap into the dielectric from SiO_2/Si interface.

The electron-trap centers are distributed in the HfO_2 bulk region as well as in the HfO_2/SiO_2 interface [25]. Liu et al. [3] have characterized the hysteresis phenomena on samples with different HfO_2 thickness. Their results suggest that trapping occurs mostly in the bulk on high-k materials rather than only at the interface. We also make the following assumptions:

1) The electrons tunnel from the channel to the empty defect states. While detrapping, trapped charges tunnel both to the channel and gate electrode.

2) Here we neglect the detrapping resulting from a Pool-Frenkel-like electrons [41] conduction from traps to traps. So we have adopted a general approach originally proposed for Schottky barrier tunneling [51] to model trapping/detrapping process.

3.4 TRAP ASSISTED LEAKAGE CURRENT DENSITY AND DISSIPATED POWER DENSITY

We calculate the power dissipation associated with the detrapped charges through the gate electrode/ oxide interfaces.

To calculate dissipated power density, we have used the detrapping part of Eqn. 3.4 The leakage current density associated with the detrapped charges termed as "Trap Assisted Leakage Current density (TALC)", J_{TALC} has been calculated for an entire pulse width using the following equation.

$$J_{TALC} = \frac{1}{T}\int_0^T J_d\, dt \tag{3.7}$$

Where J_d has been calculated using the third term of Eq. 3.4.

$$J_d = q \times \sum \frac{n_g}{N_{0g}} \frac{n_t}{\tau_2} \{1 - F(E_t, E_{fg})\} \tag{3.8}$$

Where $F(E_t, E_{fg})$ is given by

$$F(E_t, E_{fg}) = \frac{1}{1 + e^{\frac{E_t - E_{fg}}{kT}}} \tag{3.9}$$

Here we calculate *TALC* for a given instant time of the pulse width summing up all the current components associated with the detrapped charges form the electron-trap centers which are distributed in the high-k bulk region as well as in the high-k dielectric/SiO_2 interface. We neglect the off-state dissipated power density as the gate voltage is zero and the average dissipated power density for an entire time period has been calculated using the Eq. 3.9.

$$P_{dissipation} = \frac{1}{2} V_g J_{TALC} \tag{3.10}$$

Where T is the total time period having duty cycle 50%.

To compare the J_{DTC} density with the direct tunneling current (DTC) density we have also calculated J_{DTC} through the oxide barrier by summing up the contribution from all subbands current density arising from the i-th subband j-th valley as a function of gate voltage and the expression as

$$J_{DTC} = \sum q v_g \left|\psi_{ij}\right|^2 N_{ij} \quad (3.11)$$

3.5 MOBILITY CALCULATION

Modeling of MOS devices requires a mobility model which can accurately capture the dependence of effective mobility on Effective field in the inversion layer. We have calculated the mobility based on Darwish mobility model [52] and Klaassen model [53]. Here the functional dependence of surface roughness limited mobility on the inversion charge density, in addition to accounting for the coulomb screening effect in the bulk limited mobility [53] is taken into consideration

To evaluate the carrier mobility the Mathiessen rule has been used that approximates the local mobility, $\mu_0(\vec{r})$, at low longitudinal field as the sum of three terms [54]

$$\frac{1}{\mu_0(\vec{r})} = \frac{1}{\mu_b(\vec{r})} + \frac{1}{\mu_{ac}(\vec{r})} + \frac{1}{\mu_{sc}(\vec{r})} \quad (3.12)$$

where $\mu_b(\vec{r})$ is the carrier mobility in the bulk, $\mu_{ac}(\vec{r})$ is the carrier mobility limited by surface acoustic phonon scattering, and $\mu_{sr}(\vec{r})$ is the carrier mobility limited by surface roughness. To emphasize the local nature of this model, we will use the variable $(\vec{r})$ to designate spatial dependence.

The bulk mobility term , $\mu_b(\vec{r})$, uses the Klaassen model [53], which takes into account coulomb screening effects, separately models majority and minority carrier mobilities, and includes temperature dependence

$$\frac{1}{\mu_b(\vec{r})} = \frac{1}{\mu_L} + \frac{1}{\mu_I(\vec{r})} \quad (3.13)$$

where

$$\mu_L = \mu_{\max}(\frac{300}{T})^{\theta_n} \tag{3.14}$$

$$\mu_I(\vec{r}) = \mu_N(\frac{N_I(\vec{r})}{N_{Ieff}(\vec{r})})(\frac{N_{ref1}}{N_I(\vec{r})})^{\alpha 1} + \mu_c(\frac{n(\vec{r})}{N_{Ieff}(\vec{r})}) \tag{3.15}$$

$$\mu_N = \frac{\mu_{\max}^2}{\mu_{\max} - \mu_{\min}}(\frac{300}{T})^{3\alpha_1 - 1.5} \tag{3.16}$$

$$\mu_c = \frac{\mu_{\min}\mu_{\max}}{\mu_{\max} - \mu_{\min}}(\frac{300}{T})^{0.5} \tag{3.17}$$

where $n(\vec{r})$ is the total carrier concentration (n+p) and $N_1(\vec{r}) = N_A(\vec{r}) + N_D(\vec{r})$. For electrons, $N_{Ieff}(\vec{r}) = G(P_e)N_A(\vec{r}) + N_D(\vec{r})$, where $G(P_e)$ is the ratio between collision cross sections of repulsive and attractive screened coulomb potentials for electrons and is a function of the local carrier concentration, $n(\vec{r})$.

In the low transverse field regions of the device, away from the inversion layer, this bulk mobility term dominates the carrier mobility, as given by (3.13). In the high inversion layer of an MOS device, this same bulk mobility term is used in (3.13), along with the other terms that now play a term is used in (3.13), along with the other terms that now play a model applicable throughout the device. The second term in (3.13) is due to surface acoustic phonon scattering, which influences the inversion layer mobility at high transverse fields. This is taken into account here by adopting a similar formulation to that of Lombardi [54], which follows the approximation suggested by Schwarz and Russek [55]. Therefore

$$\mu_{ac}(\vec{r}) = (\frac{BT'}{E_\perp(\vec{r})} + \frac{CN_I^{\tau}(\vec{r})}{E_\perp^{\frac{1}{3}}(\vec{r})})(\frac{1}{T'}) \tag{3.18}$$

Where $E_{\perp}(\vec{r})$ is the local field component normal to the direction of current flow. The initial values of B and C are based on physically derived quantities, as explained in [54] , [55]. However, it should be pointed out that because of the difficulty in implementing a local formulation of the mobility degradation due to fixed interface charge, we followed the same approach of [56] by allowing C to be weakly dependent on the impurity concentration. Therefore, $\mu_b(\vec{r})$ with the parameters given in [53] could be still used in the interface region. As in the case of [54], it is recognized that this model will not be able to describe mobility degradation due to unusually large fixed interface charge. $T' = (\frac{T}{300})^k$, where k is the temperature dependence of the probability of surface phonon scattering, as discussed in [55], and is an empirical parameter fit to measurements [54].

At very high transverse electric field, surface roughness scattering has a significant effect on the inversion layer mobility. In previously published local mobility model [54], [56], [57] the dependence on the transverse field has the form

$$\mu_{sr}(\vec{r}) = \frac{\delta}{E_{\perp}^{\gamma}(\vec{r})} \tag{3.19}$$

Where δ is a constant that depends on the details of the technology, such as oxide growth conditions. The exponent of the transverse electric field, γ, has previously been held constant and set to a value between 2.0 and 2.9 [57].

Earlier experimental investigation [58] of mobility limited by surface roughness scattering at low temperature indicated that the field exponent remains approximately 2.0, even at high inversion charge and field. Early theoretical calculations of surface roughness scattering [59] showed that the exponent should decrease at high fields because of screening of surface roughness by the increase in surface carriers. But it was later shown that, as the transverse field and inversion charge increase, higher subbands in the quantum well of the inversion layer begin to become occupied, and multi-subband transport between levels separated in energy results in an enhanced decrease in mobility as the transverse field increases .

In the present model, the field exponent in (3.17) is expressed to be a function of the local inversion charge. This results in a surface roughness limited mobility that increases with distance from the surface, as physically expected. The following formula is proposed for γ:

$$\gamma = \mathrm{A} + \frac{\alpha n(\vec{r})}{N_I^{\eta}(\vec{r})} \tag{3.20}$$

where A, α and η are fitting parameters. This formulation accounts for the increase in the rate of falloff of μ_{eff} with E_{eff} that is seen in measurements at very high fields, due to the increase in carrier density [60]. It also accounts for the invariability of μ_{eff} with substrate bias that is seen experimentally. As the substrate bias increases, the carrier concentration in the inversion layer is reduced for the same value of E_{eff}. This results in a decrease in $\mu_b(\vec{r})$ because of the reduction in impurity screening, and hence a dependence of the total mobility on substrate bias. In our model, this reduction in $\mu_b(\vec{r})$ is compensated by an increase in $\mu_{sr}(\vec{r})$ when the carrier concentration reduces. Therefore, the dependence of effective mobility on substrate bias is minimized. The inclusion of a weak dependence on $N_I(\vec{r})$ in (3.18) was found to be necessary for an agreement between measured and calculated μ_{eff}. This effectively eliminates the weak dependence of $n(\vec{r})$ on $N_I(\vec{r})$ and results in γ that is independent of substrate doping.

Table-I

Mobility Model Parameters

Parameters	Electrons	Holes	Units
B	3.61×10^{7}	1.51×10^{7}	Cm/sec
C	1.70×10^{4}	4.18×10^{3}	$(cm^2/Vsec)(V/cm)^{\frac{1}{3}}.cm^{3\tau}$
τ	0.0233	0.0119	-
δ	3.58×10^{18}	4.10×10^{15}	V/sec
A	2.58	2.18	-
α	6.85×10^{-21}	7.82×10^{-21}	-
η	0.0767	0.123	-
K	1.7	0.9	-

An optimized set of values for the fitting parameters in the acoustic phonon and surface roughness mobility terms are shown in Table I for both electrons and holes. $E_{\perp}(\vec{r})$ in (3.18)-(3.19) is in V/cm, and $n(\vec{r})$ on $N_I(\vec{r})$ are in cm^{-3} , and T is in ^{0}K. The values of B and C in the table compare favorably to the physically derived values, and to those extracted by Lombardi [54] when normalized for temperature. The parameter τ in the acoustic phonon scattering term in Lombardi's model has a value of 0.125 for electrons and 0.0317 for holes. However, because screening of ionized impurities at higher carrier concentration is now taken into account in the bulk mobility term, the value of τ in this model is greatly reduced to 0.0233 for electrons and 0.0119 for holes. The value of the parameter A is 2.58 and 2.18 for electrons and holes, respectively.

3.6 CONCLUSION

A quantum mechanical charge trapping model is developed by modifying the rate equation proposed by [6]. Using high-k materials having high bulk trap density as a gate dielectric several device parameters has been taken into consideration. Here the current contributed and dissipated power density by these charges has been calculated in chapter 4. Also the mobility degradation due to bulk trap has been discussed. The threshold voltage shift with stressing time and effective oxide thickness has been investigated. Then the simulated results are compared with the, reported experimental results.

CHAPTER 4

RESULTS and DISCUSSION

4.1 INTRODUCTION

In this chapter, the simulated results using the expressions summarized in the previous chapters are presented in details. We focus various device characteristics such as channel mobility degradation, threshold voltage shift with stress time, trap-energy level shift due to the polaron effect and reduction of mobility degradation due to oxide thickness. Simulated data has been compared with available experimental results.

We have divided our whole work into four parts

i. threshold voltage shift varying different parameters such as stress/relaxation time, Effective oxide thickness (EOT), pulse width (trapping time), occupied and empty defect level
ii. Dissipated power density calculation
iii. Trap assisted leakage current density (TALC),
iv. Channel mobility degradation and effect of interface oxide thickness.

4.2 POTENTIAL PROFILE OF NMOS STRUCTURE

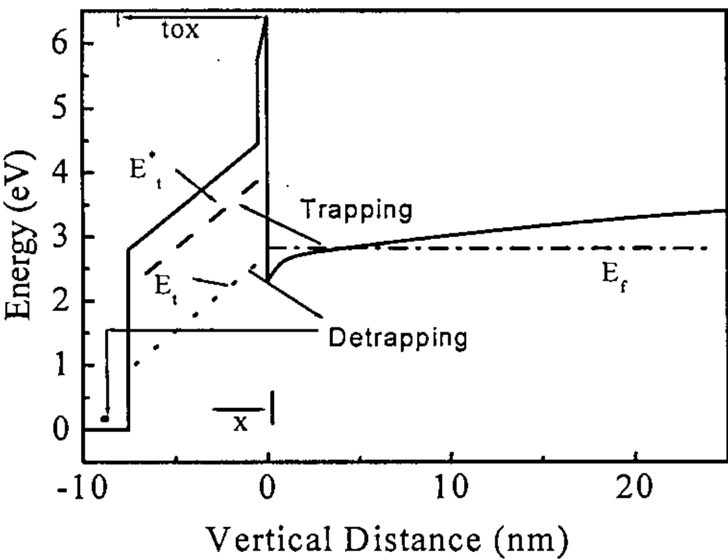


Fig. 4.1 Potential profile of a multi-stack (Si/SiO_2 /HfO_2/poly-Si) containing empty defect level and occupied defect level in the HfO_2 layer at positive gate bias consisting of 0.5 nm SiO_2 and 7.05 nm of HfO_2. Here substrate doping density, $Na=5\times10^{17}$ cm^{-3}.

Fig 4.1 shows a potential profile of a multi-stack MOS structures. The HfO_2 oxide thickness is taken as 7.05 nm with a 0.5 nm interfacial thickness layer of SiO_2 according to the experiments [5]. We conducted transient simulations with trapezoidal pulses applied at the gate. The pulse width is 0.2 ms. The potential profile of Si inversion layer has been shown with two defect level, empty defect level (E_t^*) and occupied defect level (E_t) which are set to 0.4 ev and 1.4 ev below the CBM, respectively [6]. A fixed interface charge density 3×10^{12} cm^{-2} is considered. Both the trapping and detrapping process are shown in the figure. Relative dielectric constant of HfO_2 = 25, Relative dielectric constant of SiO_2 = 3.9, Unit normalization factor $N_0 = 10^{19}/cm^3$ .Here electrons trap to the empty defect level from the channel and detrap to the channel and also to the gate electrode.

4.3 THRESHOLD VOLTAGE SHIFT

4.3.1 Threshold Voltage Shift vs Gate voltage as a function of defect level

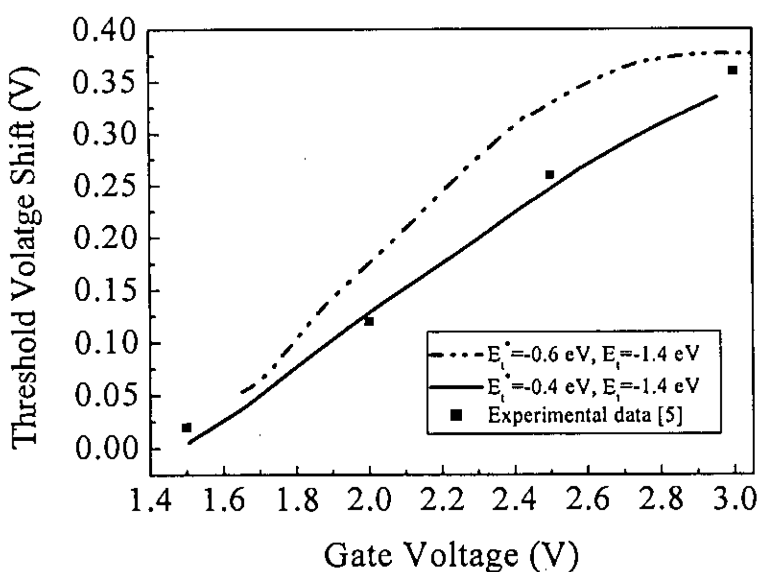


Fig. 4.2 Threshold-voltage shift as a function of gate voltage taking two empty defect levels and same occupied defect level. Here HfO_2 oxide thickness is taken as 10.25 nm with 0.5 nm interfacial SiO_2 thickness.

The effect of empty trap level on threshold voltage shift is shown in Fig. 4.2. We show the threshold voltage shift verses gate voltage (*Vg*) at different empty and occupied trap energy levels. We consider two empty defect levet E_t^{*} = -0.4 eV, -0.6eV for E_t =-1.4 eV with respect to HfO_2 CBM. For E_t^{*} = -0.4 eV, we obtain a reasonable match to validated our model with experimental result reported by Shanwar et al [5]. It is found that more severe V_t shifts are found for lower E_t^{*} levels because of larger trap occupation factors. The pulse width is 0.2 ms. From the ratc equation, we also observe, as E_t^{*} is lowered, the tunneling probability of electrons from channel to the empty defect

level increases and more electrons get trapped to the empty states of the oxide region with an increase of threshold voltage shift.

4.3.2 Polaron effect

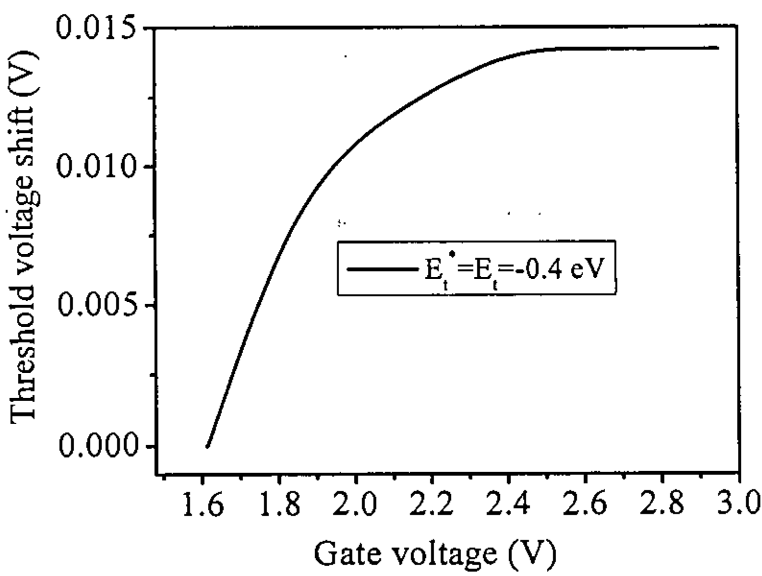


Fig. 4.3 Polaron effect is shown by taking $E_t^* = E_t$ = -0.4 eV in the simulation. Here HfO_2 oxide thickness is taken as 10.25 nm with 0.5 nm interfacial SiO_2 thickness.

The polaron effect is evidenced by setting $E_t^* = E_t$ in the simulation as shown in Fig 4.3. Here, the simulated V_{th} shift is significantly reduced and it has a much weaker dependence on Vg. This is because, without considering the occupied defect energy level shift, the detrapping process would cause significant tunneling of trapped electrons back into the channel and gate during the pulse falling edge. Therefore, to observe the dependency of Vg with V_{th} the polaron effect should be taken into account. The more the difference between empty and occupied defect level is reduced the less dependency will be observed for the threshold voltage shift on gate voltage.

4.3.3 Threshold Voltage Shift vs stress time as a function of gate voltage

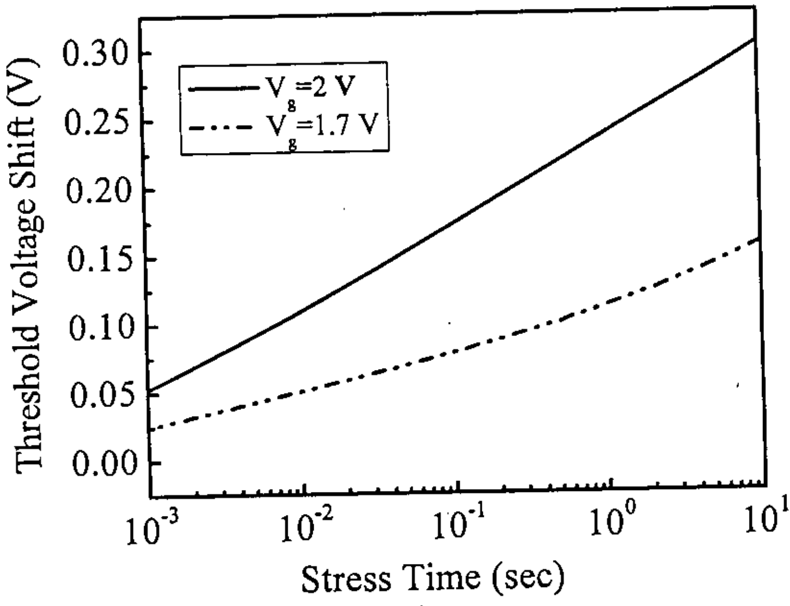


Fig. 4.4 Threshold-voltage shift versus stress time for HfO_2 / poly-SiO_2 gate under constant voltage stress. The oxide thickness is taken as 5.3 nm.

We simulated our model for 5.3 nm oxide thickness (consisting of 0.8 nm SiO_2 and 4.5 nm of HfO_2) and show the dependence of the threshold voltage shift on stress time under constant gate voltage. In the measurements, the single-pulse technique is used for stress times up to 10 s. A logarithmic stress-time dependence of the V_T shift can be seen for several decades with only moderate saturation at the very long stress times. This trend agrees well with the experimental data [4] strongly suggesting the dependence of threshold voltage shift on trapping time.

4.3.4 Threshold Voltage Shift vs Effective Oxide Thickness (EOT)

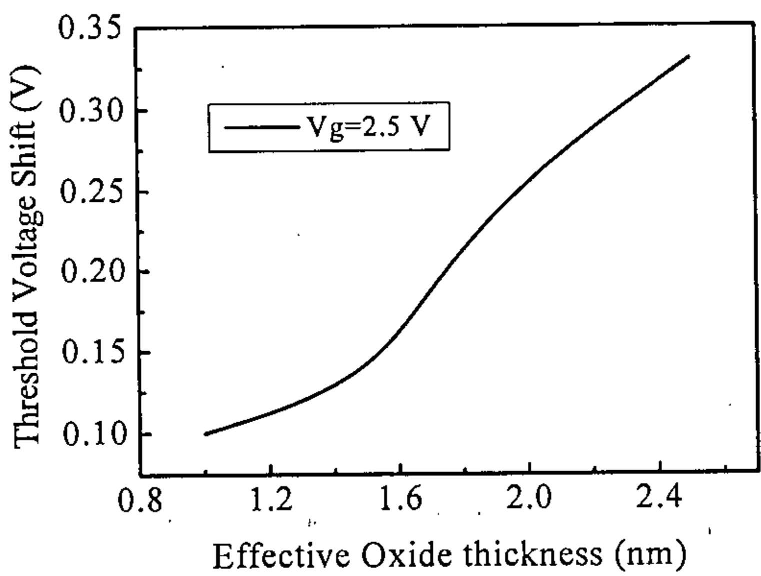


Fig. 4.5 Threshold-voltage shift versus varying effective oxide thickness at a gate voltage of 2.5V.

Fig. 4.5 shows threshold voltage shift variation with different gate effective oxide thickness. Here the interfacial SiO_2 oxide thickness has been kept at 0.5 nm and the gate voltage is 2.5 V. The pulse width is 0.2 ms. At lower regime (below EOT 1.4 nm) of the curve threshold voltage shift is as low as charge does not get enough defect states to get trapped while at the mid region of the curve the threshold voltage shift increases rapidly with EOT as charge get sufficient defect states to get trapped. Another observation is upper portion the curve, again V_{th} does not increase as that of the middle region as the charge trapping dynamics becomes more stable for that gate voltage.

4.3.5 Threshold Voltage Shift under dynamic stress at different gate voltage

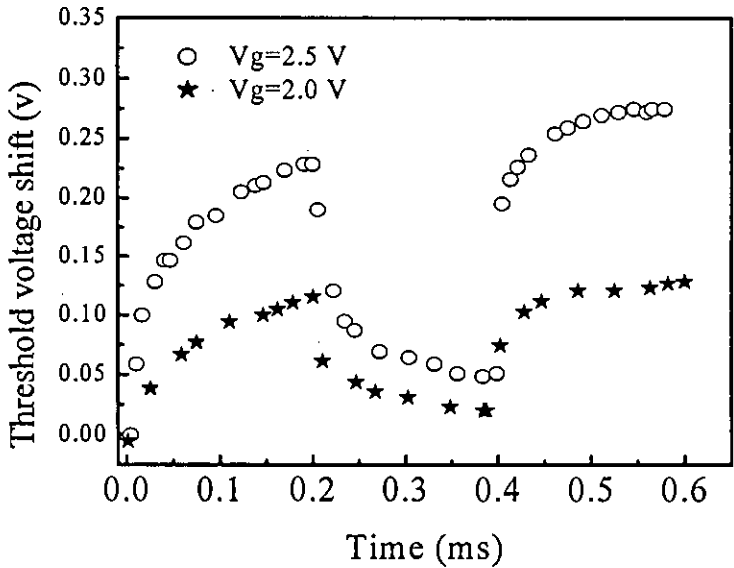


Fig. 4.6 Simulated threshold-voltage shift as a function of time during on and off stress at Vg = 2.0 V and 2.5 V stress condition and three pulses using an HfO_2 thickness of 10.25 nm and the SiO_2 thickness is set to be 0.5 nm .

We have investigated the dynamic bias stress-induced charge trapping and detrapping phenomenon in Polysilicon-HfO_2-Si oxide thin film transistors. Figure 4.6 shows the time evolution of the threshold voltage shift (ΔV_{th}) under dynamic stresses. During the stress phase (on stage), the gate electrode was forced to *Vg*, and during the relax phase (off stage) the gate electrode was fixed at 0V. Here we take two different gate voltage of 2.0 v and 2.5 V. Effective oxide thickness is taken as 1.6 nm (SiO_2 thickness = 0.5 nm and HfO_2 physical thickness= 10.25 nm), ΔV_{th} is shifted significantly at the beginning of the stress phase, and as the stress continues, ΔV_{th} approaches a saturation value. In the recovery phase, keeping gate voltage at zero potential, threshold voltage decreases by the electron detrapping from the interface or bulk dielectric layers to the gate and channel, but the original ΔV_{th} is not fully recovered. This is because trapped

charges cannot be fully recovered during relaxation time and the remaining charges are responsible for the hysteresis behavior (C_v vs V_g, I_d vs V_g) of MOS structures. Similar to the stress phase, ΔV_{th} post stress relaxation demonstrates saturation-like behavior after the initial rapid decrease. This repetitive and reversible ΔV_{th} behavior indicates that the relaxation behavior is associated with the partial detrapping of the previously trapped charges [6].

During our simulation dynamic Stress (multiple pulses applied) was applied. Applying the multipulse we observe the variation of threshold voltage. During the stress time (0 to 0.2 ms) duration, threshold voltage shift increases. Now for the next two seconds, pulse have been removed (relax/off stage). But afterwards the rate of increasing threshold voltage shift decays. If further pulses are applied threshold voltage shift at one point will be saturate as all the defects will be occupied by electrons.

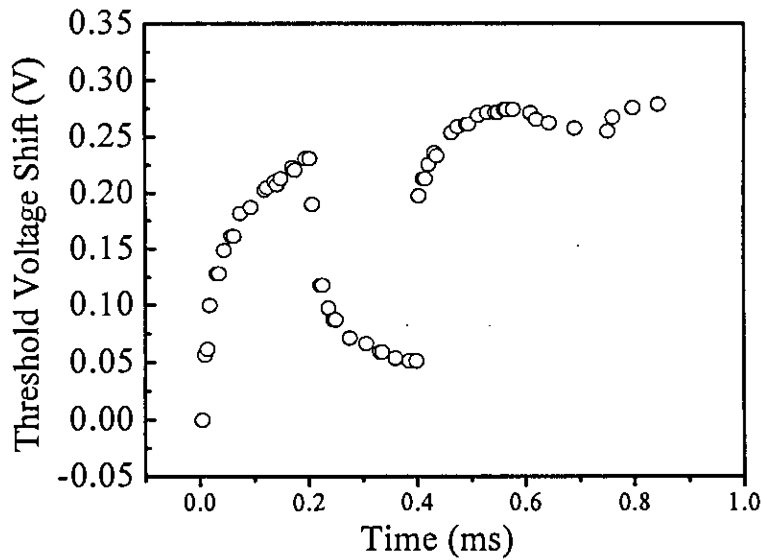


Fig. 4.7 Simulated threshold-voltage shift as a function of time during on and off stress at V = 2.5 V stress condition and five pulses using an EOT of 1.6nm and the SiO_2 thickness is set to be 0.5 nm .

To observe the saturation in threshold voltage shift we put additional couple of pulses. In Fig 4.7 we have simulated the threshold voltage shift for 5 pulse (stress and relaxation time consequently). During the 4th cycle (2nd relaxation cycle) the threshold voltage shift almost reaches at a saturation level. This is because of the defect levels being filled by pre-occupied trapped charges. During the last two cycles the threshold voltage shows less dynamics rather than reach saturation.

4.3.6 Threshold Voltage Shift vs frequency

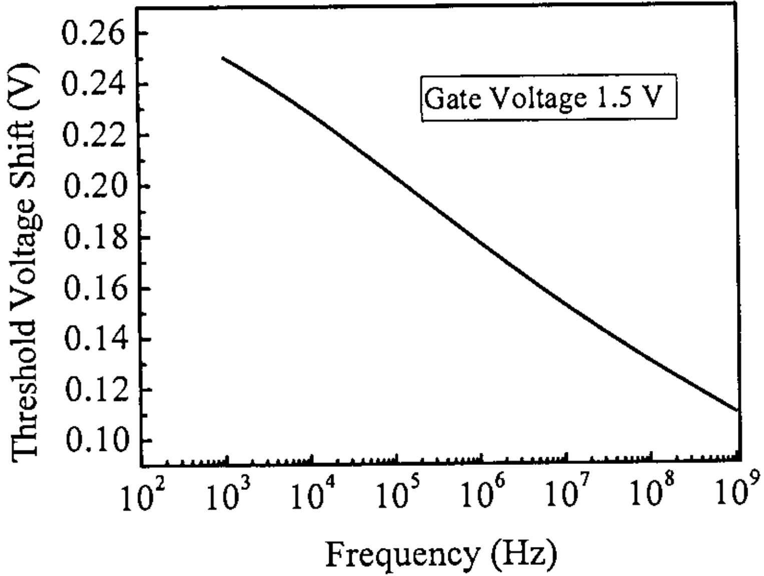


Fig. 4.8 Simulated threshold-voltage shift as a function of frequency at V = 1.5V using HfO_2 thickness of 3.0 nm and the SiO_2 thickness is set to be 0.8 nm.

Fig. 4.8 depicts the variation of threshold voltage shift with frequency. The curve clearly reveals the effect of frequency variation on the threshold voltage shift. We find that at around 10^4 Hz the threshold voltage shift is high (~0.23 volt) as charge gets enough time to get trapped while at high frequency charge does not get sufficient time to get trapped.

4.4 TRAP ASSISTED LEAKAGE CURRENT DENSITY (TALC) VS GATE VOLTAGE

Since charges detrap through the gate/oxide region so time has come to calculate the current contributed by those charges as it will become an additive quantity with the gate current. Here we calculate this current termed as "TALC" by summing up all the current component of each detrapped charge using Eqn. 3.17

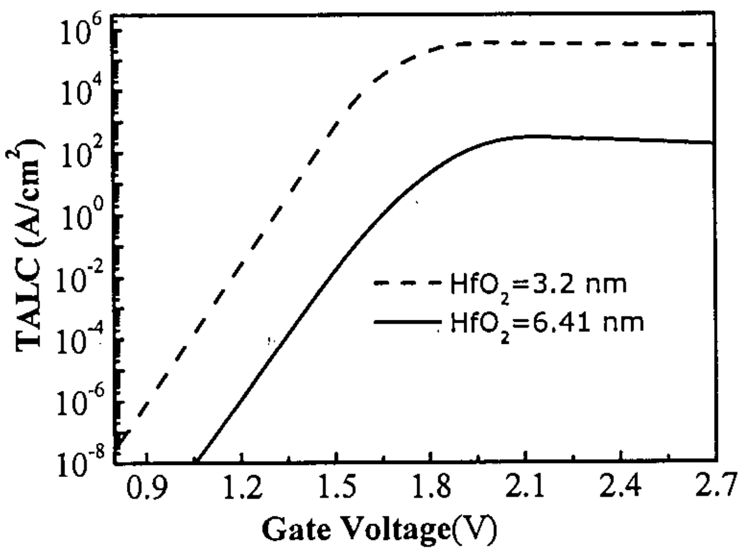


Fig. 4.9 *TALC* versus gate voltage at different oxide thickness. Here substrate doping density $5\times10^{17}cm^{-3}$

The *TALC* has been calculated and shown in Fig. 4.9. And this discharged current is higher to a great extent at lower EOT. For an oxide thickness of 1 nm (consisting of 0.5 nm SiO_2 and 3.2 nm of HfO_2), this current density is ~10^4 A/cm^2 at a gate voltage of 2.5 V and the calculated total gate current will be underestimated as this current is an additive component with the gate current.

4.5 TALC vs HfO_2 Thickness at different bulk trap density

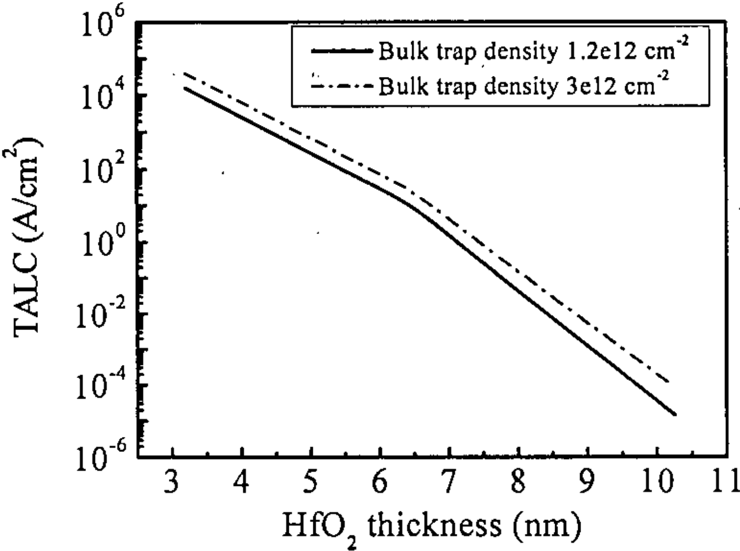


Fig. 4.10 *TALC* versus gate voltage at different oxide thickness. Here substrate doping density $5\times10^{17}cm^{-3}$

In fig 4.10 TALC has been calculated with different HfO_2 oxide thick ness keeping SiO_2 thickness as 0.5 nm. Simulation has been done at a Inversion carrier density of 2e13 cm^{-2} with two different bulk trap density. Around EOT of 1 nm (HfO2=3.2 nm and SiO2 0.5 nm) the TALC due to detrapped charges is 1.56×10^{4} W/cm^{2} at a bulk trap density of 1.2e14 cm^{-2} and this current decreases with increase of HfO_2 thick ness as expected. Also the TALC has been calculated with a higher bulk trap density of 3e12 cm^{-2}. Here the leakage current increases as charger get more trapped due to higher trap center.

4.6 TALC vs INVERSION CARRIER DENSITY

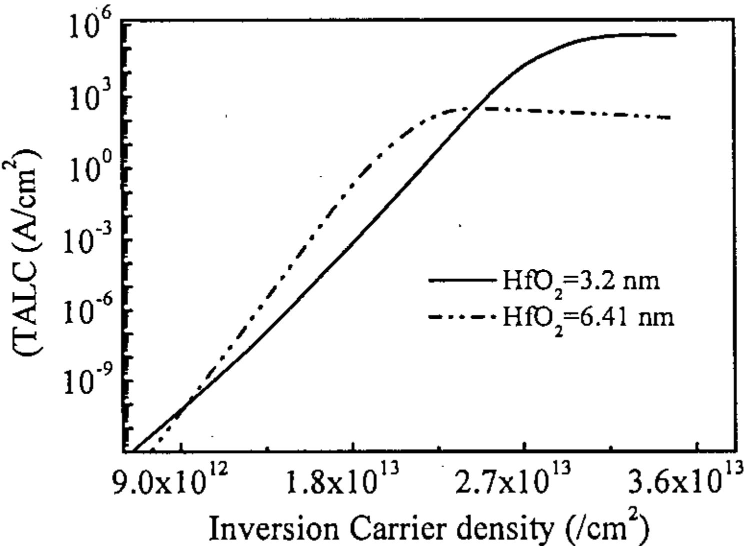


Fig. 4.11 *TALC* versus inversion carrier density at different oxide thickness. Here substrate doping density, Na=5e17 cm^{-3}

This *TALC* is shown as a function of inversion carrier density in Fig. 4.11 Here at lower inversion charge discharged current increases with lower EOT. Then opposite characteristic has been found but for higher inversion charge again *TALC* increases with lower EOT. This phenomenon has been observed due to oxide-electric field variation caused by trapped charge in the HfO_2. For an oxide thickness of 1 nm (consisting of 0.5 nm SiO_2 and 3.2 nm of HfO_2).This discharged current is high enough to limit further oxide thickness scaling. So this effect is no longer negligible as *TALC* increases with decreasing oxide thickness.

4.7 Comparison of TALC with direct tunneling current (DTC)

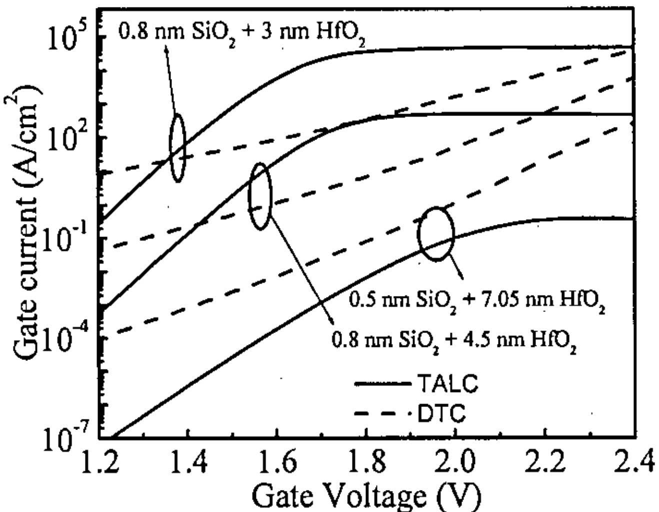


Fig. 4.12 Comparison of TALC with DTC at different oxide thickness.

In Fig. 4.12, we calculate *TALC* and compare with Direct Tunneling Current *(DTC)* calculated using Eq. 3.10. This *TALC* is higher to a great extent at lower oxide thickness. The calculated *TALC* can be neglected for the oxide thickness (0.5 nm SiO_2 + 7.05 nm HfO_2) as shown in the figure but reduced oxide thickness makes this term significant and dominating over the *DTC*. For an oxide thickness of 3.8 nm (0.8 nm SiO_2 + 3 nm HfO_2) this discharged current density is 10^4 A/cm^2 at a gate voltage of 1.8 V which is almost 100 times larger than the calculated *DTC*. Applying high-k gate dielectric, several orders of magnitude lowered *DTC* can be achieved but another current component, *TALC* increases due to high bulk trap density.

4.8 POWER CALCULATION

4.8.1 Dissipated Power density vs Gate voltage as a function of oxide thickness

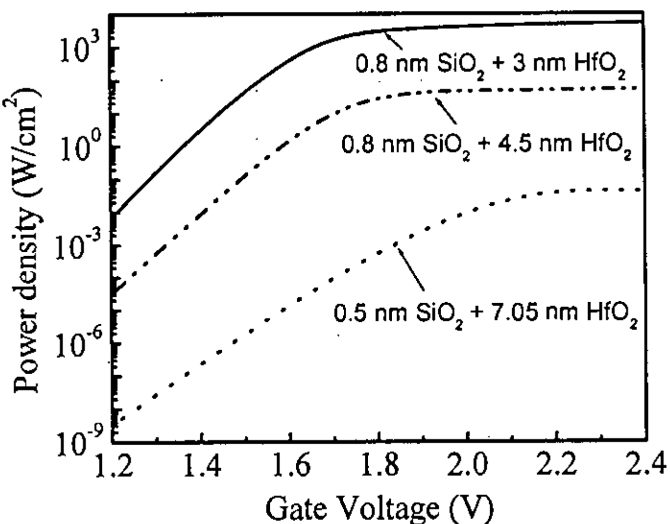


Fig. 4.13 Simulated dissipated power density versus gate voltage with different oxide thickness.

In Fig. 4.13 we show variation of dissipated power density for trap assisted leakage electrons with gate voltage at different oxide thickness. The curve clearly reveals the effect of further scaling on the dissipated power. At an oxide thickness of 3.8 nm (0.8 nm SiO_2 + 3 nm HfO_2) we find that the dissipated power density is around 2×10^3 W/cm^2 at a gate voltage of 1.8 V. This extra dissipated power can be cooled using reasonable technology, but raises the economic question that may limit the further scaling as described in [7]. By scaling MOS devices we can reduce V_{th}. Here we can hit the point where we can no longer reduce the Vth. Reduction in V_{th} have made leakage power large enough that it needs to be considered in the power budget. To minimize this dissipated power density we need to set the V_{th} not only by technology scaling. To continue with the scaling trend as forecasted in [1] high-k materials having low bulk trap density need to be chosen to minimize the dissipated power density and leakage current.

4.8.2 Power density vs HfO_2 thickness at different bulk trap density

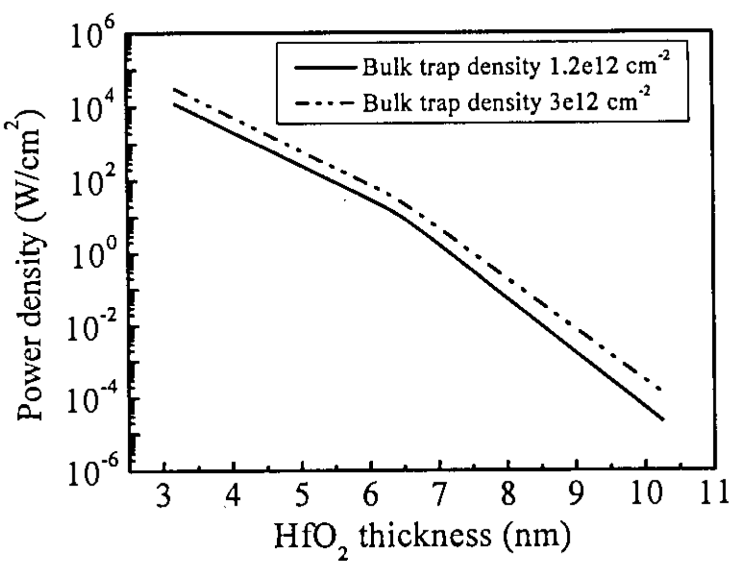


Fig. 4.14 Simulated dissipated power density versus gate voltage with different oxide thickness.

In Fig 4.14 Power density has been shown with different HfO_2 oxide thick ness keeping SiO_2 thickness as 0.5 nm. Simulation has been done at a Inversion carrier density of 2e13 cm^{-2}. Around EOT of 1 nm (HfO_2=3.2 nm and SiO_2 0.5 nm) the dissipated power density due to detrapped charges is 1.2×10^4 W/cm^2 (bulk trap density= 1.2e12 cm^{-2}) which decreases with increase of HfO_2 thick ness as expected. Also similar simulation for dissipated power density has been carried out increasing bulk trap density. Dissipated power density incraeases, as expected, due to higher trap centers as more charges get trapped.

4.8.3 Power density vs Frequency at different oxide thickness

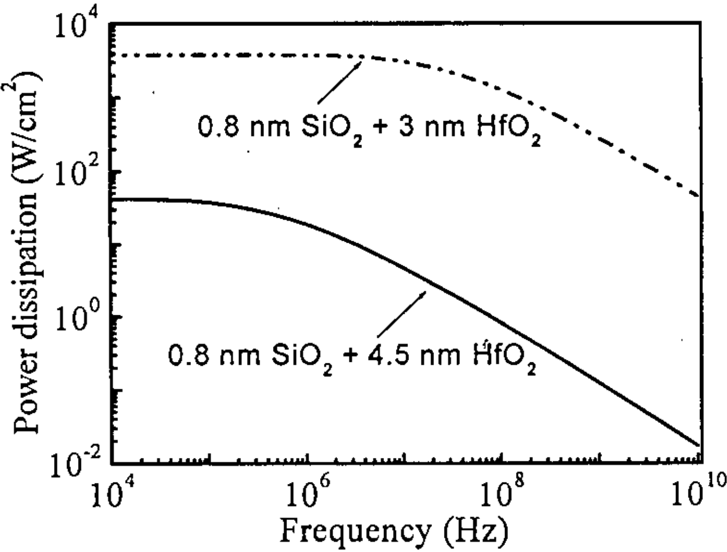


Fig. 4.15 Dissipated power density as a function of frequency considering Vg = 1.8 V considering thickness as a parameter.

In Fig. 4.15 we show the frequency response of power dissipation density. The trend of the curve shows that dissipated power density remains constant up to a certain frequency and then gradually decreases. Because at higher frequency, trapped charges as well as detrapped charges decreases due to lower pulse width (trapping time). For an oxide thickness of 5.3 nm (0.8 nm SiO_2 + 4.5 nm HfO_2) this rolling off occurs after 0.1 MHz but for an oxide thickness of 3.8 nm (0.8 nm SiO_2 + 3 nm HfO_2), dissipated power density remains high up to 10 MHz and then rolling off occurs. Dissipated power density will be less at high frequency operation but consequently present scaling trend will increase the dissipated power density which may set a constraint to the scaling roadmap [7].

4.9 MOBILITY CALCULATION

4.9.1 Mobility vs Electric field

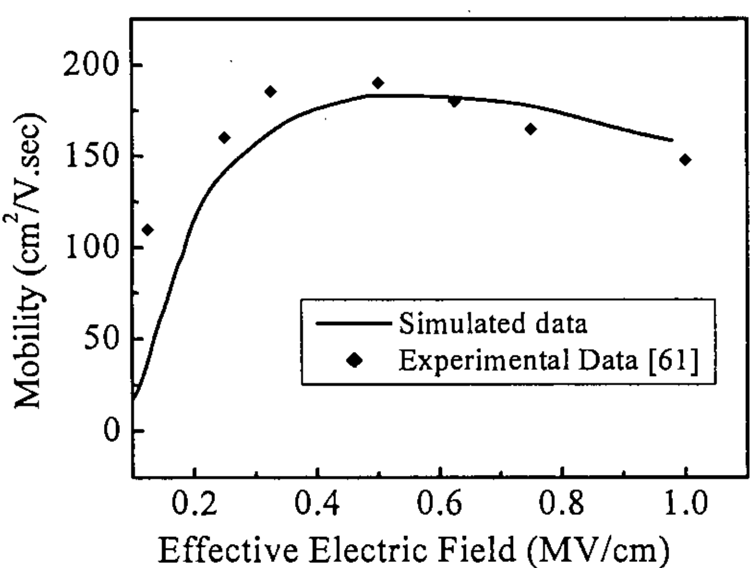


Fig. 4.16 Simulated mobility profile inside the channel. EOT = 2 nm (SiO_2 = 0.8nm, HfO_2 =7.69 nm).

Degradation mechanism of the channel mobility for MOSFETs with HfO_2 as the gate dielectric has been shown in Fig 4.16. An effective oxide thick of 2 nm has been taken (0.8 nm SiO_2 and 7.69 nm HfO_2). Experimental data has been taken from [61] and a good agreement with our simulated results has been obtained. Here using HfO_2 as a gate dielectric, the channel mobility is reduced to ~145 cm^2/V-sec at an electric field of 0.5 MV/cm. But a high mobility of ~400 cm^2/V-sec is found while taking SiO_2 as an insulator at the same electric field as shown in [61]. Trapping by high densities of interface traps (and/or border traps) could lead to a significant underestimate of the channel mobility. Our results suggest that Coulomb scattering due to interface traps and oxide charge in HfO_2 is a major cause for mobility degradation.

4.9.2 Mobility vs Electric field varying interfacial oxidc thickness

Mobility degradation can still be observed by varying the interfacial layer thickness. It is known that the mobility degradation in high-k is attributed to trapped charges. With an increase of the interfacial layer thickness, charge trapping efficiency was dramatically decreased, which in turn reduced the mobility difference. Also the interface state density decreased with increasing interfacial layer thickness. In addition, the interface states also were also decreased. These results suggest that the remote scattering center is located in the middle of bulk high-k layer. Thus with thicker interface layer, the screening field for carrier scattering is reduced because the centroid of remote scattering is moved away from the channel region, which led to the mobility improvement. And as the high-k layer thickness increases with the fixed bottom interfacial layer, the scattering centroid also was moved away from the inversion layer and the screening field was decreased. However, the area density of trapped charges was increased as well. Therefore, these two effects compensated each other and led to the similar intrinsic mobility [62].

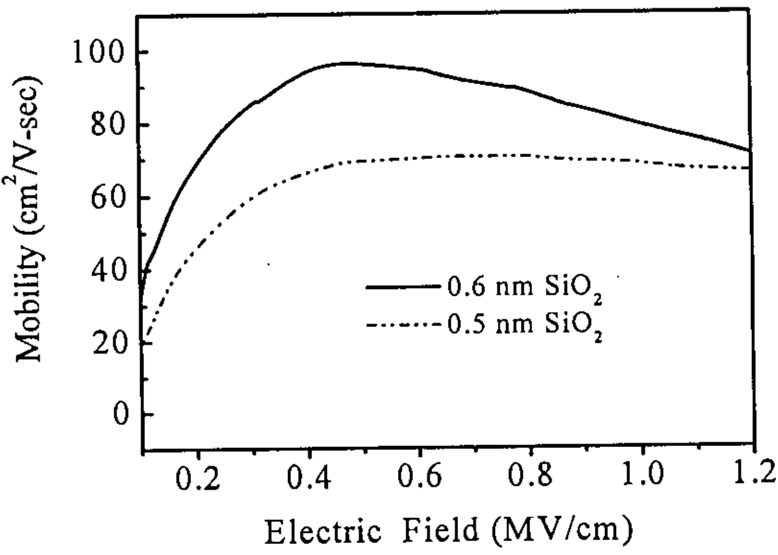


Fig. 4.17 Simulated mobility profile inside the channel with 1.67 nm EOT (considering of 0.6nm SiO_2 and 7.69 nm of HfO_2) and 1.1 nm EOT (considering of 0.5nm SiO_2 and 7.69 nm of HfO_2).

In Fig 4.17 the reduction of mobility decreased with an increase if interfacial oxide thickness is shown. So it is also evident in our model that we can improve mobility by increasing interfacial oxide layer thickness. So we can improve mobility by increasing interfacial oxide thickness. But increasing interfacial oxide thickness will increase the threshold voltage so we need to make trade up between two processes.

4.10 CONCLUSION

Here we have developed a model to simulate the charge trapping dynamics in HfO_2. Using the simulated results of our model different device characteristics has been investigated. By reducing gate oxide thickness we can achieve lower threshold voltage but detrapped electrons have considerable effect on the instability of threshold voltage and power dissipation. Again increasing the interfacial oxide thickness improves the channel mobility. But again this may result in higher threshold voltage shift. So there should be good agreement between these aspects to continue a further device scaling.

CHAPTER 5

CONCLUSION

5.1 SUMMARY

One of the important features of using High-k material is to keep the gate current lower as compare to conventional thin oxide. This is because for a same EOT the physical thickness of High-k materials is larger than SiO_2. And its large physical thickness keeps the gate current lower. But as high-k materials posses large bulk trap centers which make charges get trapped and finally these charges detrap to the gate layer making the gate current larger as expected. So there should be more discussion on High-k materials using as a gate dielectrics with further device scaling. With shrinking of physical size of the devices, EOT less than 2nm may be needed. Before using high-k materials as a potential replacement of SiO_2 several issues such as dissipated power density, mobility degradation etc. should be considered. To address these issues not only high quality films need to be deposited but also excellent electrical characteristics need to be obtained before high-k materials can be integrated into standard CMOS technology. Here we develop a model to simulate the charge trapping dynamics in HfO_2. In thiswork, these issues are investigated incorporating both forward and backward detrapping. And this charge trapping/detrapping model is used to analyze the threshold voltage instability, polaron effect, leakage current and power dissipation varying EOT, stress time, frequency and trap level. The model proposed here is compared with reported experimental results and good agreements are achieved.

5.2 SUGGESTION FOR FUTURE WORK

High-k dielectrics gate oxide can be scaled below keeping the gate leakage current density lower. But due to excessive bulk trap density of high-k dielectric, we believe, further scaling may be prohibited due increasing leakage current density as well as dissipated power density and these terms should be further studied for successful high-k integration into the Si CMOS technology. Moreover it is suggested that that thinning of HfO_2 could improve mobility. However, thin film quality at the scaling limit is often poor, making it difficult to simultaneously achieve mobility, EOT and Leakage Current target. Obtaining more than 90% universal SiO_2 mobility value is required to make use of high-K device in future technology. So there should be more discussion on High-k materials using as a gate dielectrics with further device scaling

References

[1] "The international technology roadmap semiconductors. (2006)." http://www.itrs.net/links/2006Update/2006UpdateFinal.htm"

[2] J. Robertson, "High dielectric constant oxides," Eur. Phys.J. Appl. Phys., vol. 28, no. 3, pp. 265--291, Dec. 2004.

[3] Y. Liu, A. Shanware, L. Colombo, and R. Dutton, "Modeling of charge trapping induced threshold-voltage instability in high-k gate dielectric fets," IEEE Electron Device Letters, vol. 27, no. 6, pp. 489–491, June 2006.

[4] C. Leroux, J. Mitard, G. Ghibaudo, X. Garros, G. Reimbold, B. Guillaumor, and F. Martin, "Characterization and modeling of hysteresis phenomena in high-k dielectrics,," IEDM Tech. Dig., pp. 737–740, 2004.

[5] A. Shanware, M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, J. McPherson, L. Colombo, G. A. Brown, C. H. Lee, Y. Kim, M. Gardner, and R.W.Murto, "Characterization and comparison of the charge trapping in HfSiON and HfO_2 gate dielectrics,," IEDM Tech. Dig., pp. 939–942, 2003.

[6] K. M. F. Shahil, M. N. Arafat, Q. D. M. Khosru, and M. R. Khan, "Study of charge trapping/detrapping mechanism in SiO_2/HfO_2 stack gate dielectrics considering two-way detrapping," Proceedings of International Workshop On Electron Devices And Semiconductor Technology, IEDST-2007,Beijing, China,, 2007.

[7] X. Garros, J. Mitard, C. Leroux, G. Reimbold, and F. Boulanger, "In depth analysis of vt instabilities in HfO_2 technologies by charge pumping measurements and electrical

modeling," 45th Annual international Reliability Physics Symposium Phoenix 2007, pp. 61–66, 2007.

[8] B. Nikoli, "Design in the power-limited scaling regime," IEEE Trans. on Electron Device, vol. 55, no. 1, pp. 71–83, January 2008.

[9] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," Journal of Applied Physics, vol. 89, p. 5243, 2001.

[10] D. J. Frank, "Power constrained cmos scaling limits," IBM J. RES. and Dev., vol. 46, no. 2/3, pp. 355–358, March/May 2002.

[11] Wikipedia, "http://en.wikipedia.org/wiki/MOSFET"

[12] Gerald Marcyk and Robert Chau, "New Transistors for 2005 and Beyond," presented at November 26, 2001. Retrieved on Oct 20, 2003

[13] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of Ion-Implanted MOSFETs with Very Small Physical Dimensions," IEEE J. Solid-State Circuits SC-9, 256 (1974).

[14] "The international technology roadmap semiconductors. (2003)." ITRS web page, http://public.itrs.net/Files/2003ITRS/

[15] Yongjoo Jeon, Byoung Hun Lee, Keith Zawadzki, Wen-Jie Qi, Aaron Lucas, Renee Nieh and Jack C. Lee, "Effect of Barrier Layer on the Electrical and Reliability Characteristics of High-k Gate Dielectric films", IEDM Tech. Dig., pp. 797-800, 1998.

[16] B. Cheng, M.Cao, R. Rao, A. Inani,Vande Voorde, W.M. Greene, J.M.C Stork, Yu Zhiping, P.M. Zeitzoff, J.C.S. Woo, "The impact of high-κ gate dielectrics and metal gate electrodes on sub-100 nm MOSFETs", IEEE Transactions on Electron Devices, , Vol. 46 , pp.1537 – 1544, 1999.

[17] R.D. Shannon, "Dielectric polarizabilities of ions in oxides and fluorides," J. Appl. Phys., vol. 73, no. 1, p. 348, 1993.

[18] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," J. Appl. Phys. 89, 5243 (2001).

[19] John Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices", Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, Volume 18, Issue 3, pp. 1785-1791, 2000.

[20] Qiang Lu, H. Takeuchi, Xiaofan Meng, Tsu-Jae King, Chenming Hu, K. Onishi, Hag-Ju Cho, J. Lee, "Improved performance of ultra-thin HfO2CMOSFETs using poly-SiGe gate", VLSI Technology Digest of Technical Papers 2002 Symposium , pp. 86 -87, 2002.

[21] C. H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kowng, "MOS characteristics of Ultra Thin Rapid Thermal CVD ZrO_2 and Zr silicate Gate Dielctrics", IEDM Tech. Dig., pp. 27-30, 2000.

[22] Hag-Ju Cho, Chang Seok Kang; K. Onishi, S, Gopalan, R. Nieh, Rino Choi, S. Krishnan, J. C. Lee, "Structural and electrical properties of HfO_2 with top 14 nitrogen incorporated layer", IEEE Electron Device Letters, Vol. 23, Issue 5, pp. 249-251, 2002

[23] H-J. Cho, C.S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, E. Dharmarajan, and Lee, J.C., "Novel nitrogen profile engineering for improved TaN/HfO_2/Si MOSFET

performance", Electron Devices Meeting, 2001. IEDM Technical Digest., pp. 30.2.1 -30.2.4, 2001.

[24] C.H. Choi, C.S. Kang, C.Y. Kang, R. Choi, H.J. Cho, Y.H.Kim, S.J.Rhee, M.Akbar, and J.C. Lee, "The effects of nitrogen and silicon profile on high-k MOSFET performance and bias temperature instability" , VLSI Tech. Dig. 20.4-20.5, 2004

[25] Kang, C.Y.; Rhee, S.J.; Choi, C.H.; Akvar, M.S.; Kim, H.-S.; Zhang, M.; Lee, T.; Ok, I.; Zhu, F.; Lee, J.C. "Effects of optimized nitrogen tailoring in high-k dielectrics on impurity penetration and stress induced device degradation", Reliability Physics Symposium, 2005. Proceedings. 43rd Annual. 2005 IEEE International, Page: 628 – 629 April 17-21, 2005

[26] Onishi, K.; Chang Seok Kang; Rino Choi; Hag-Ju Cho; Gopalan, S.; Nieh, R.E.; Krishnan, S.A.; Lee, J.C., IEEE Transactions on Electron Devices, Volume 50, Issue 2, Page(s):384 – 390, Feb. 2003.

[27] Denais, M.; Huard, V.; Parthasarathy, C.; Ribes, G.; Perrier, F.; Revil, N.; Bravaix, A." New methodologies of NBTI characterization eliminating recovery effects", Solid-State Device Research conference, 2004. ESSDERC 2004. Proceeding of the 34th European, Page(s):265 – 268, 21-23 Sept. 2004

[28] A. Kerber, E. Cartier, R. Degraeve, P. J. Roussel, L. Pantisano, T. Kauerauf, G. Groeseneken, H. E. Maes, U. Schwalke, "Charge trapping and dielectric reliability of SiO_2-Al_2O_3 gate stacks with TiN electrodes", Electron Devices, IEEE Transactions on Volume 50, Issue 5, Page(s):1261 – 1269 , May 2003

[29] A. Kerber, E. Cartier, L. Pantisano, M. Rosmeulen, R. Degraeve, T. Kauerauf, G. Groeseneken, H. E. Maes, U. Schwalke, "Characterization of the Vt instability in SiO_2/HfO_2 gate dielectrics", IEEE Reliability Physics Symposium Proceedings, p.41 – 45, 2003

[30] Kerber, A.; Cartier, E.; Ragnarsson, L.A.; Rosmeulen, M.; Pantisano, L.; Degraeve, R.; Kim, Y.; Groeseneken, G.;" Direct measurement of the inversion charge in MOSFETs: application to mobility extraction in alternative gate dielectrics" VLSI Technology, 2003. Digest of Technical Papers. 2003 Symposium, Page(s):159 – 160, 10-12 June 2003.

[31] Wenjuan Zhu; Jin-Ping Han; Ma, T.P. "Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-k dielectrics", Electron Devices, IEEE Transactions on, Vol.51, Iss.1, Pages: 98- 105, Jan. 2004,

[32] S.C. Sun, J.D. Plummer, IEEE T. Electron Dev. 27, 1497 (1980)

[33] S.I. Takagi, A. Toriumi, M. Iwase, H. Tango, IEEE T. Electron Dev. 41, 2357 (1994)

[34] R.W. Murto, M.I. Gardner, G.A. Brown, P.M. Zeitzoff, H.R. Huff, Solid State Technol. 46, 43 (2003)

[35] M.V. Fischetti, D.A. Neumayer, E.A. Cartier, J. Appl. Phys. 90, 4587 (2001)

[36] W. Zhu, J.P. Han, T.P. Ma, IEEE T. Electron Dev. 51, 98 (2004)

[37] V. Afanasev, A. Stesmans, Appl. Phys. Lett. 80, 1261 (2002)

[38] W.J. Zhu, J.P. Han, and T.P. Ma, "Accurate measurement of mobility in MOSFETs made with ultra-thin high-k dielectrics", IEEE Trans. ED, Vol.ED-51, No.1, pp.98-105 (2004)

[39] S. Zafar, A. Callegari, E. Gusev, and M. V. Fischetti, "Charge trapping related threshold voltage instabilities in high permittivity gate dieleetric stacks," J. Appl. Phys., vol. 93, no. 11, pp. 9298–9303, Jun. 2003.

[40] A. Kumar, M.V. Fischetti, T.H. Ning, E. Gusev, J. Appl.Phys. 94, 1728 (2003)

[41] Ribes G., Mitard J., Denais M., Bruyere S., Monsieur F., Parthasarathy C., Vincent E., and Ghibaudo G., "Review on High-k Dielectrics Reliability Issues" IEEE Trans. On Device and Materials Reliability, Vol. 5, No. 1, pp-5-19, March 2005.

[42] E.P Gusev, "The physics and chemistry of SiO_2 and the Si-SiO_2 interface", Electro-chem. Soc., pp. 477-485, 2000.

[43] Zhu, W. J., Ma, T. P., Zafar, S. and Tamagawa, T., "Charge Trapping in Ultrathin Hafnium Oxide," in IEEE Electron Device Lett., vol. 23, no. 10, pp. 597–599, Oct. 2002.

[44] Chowdhury N. A., Garg R., and Misraa D., "Charge trapping and interface characteristics of thermally evaporated HfO_2" Applied Physics Letter, Vol-85, pp-3289-3291, Oct 2004

[45] Z. A. Weinberg, "Tunneling of electrons from Si into thermally grown SiO_2," Solid-State Electron., vol. 22, p. 11, 1977.

[46] A. Haque, A. Rahman, and I. B. Chowdhury, "On the use of appropriate boundary conditions to calculate the normalized wave functions in the inversion layer of MOSFET's with ultra-thin gate oxides," Solid-State Electron., vol. 44, pp. 1833–1836, 2000.

[47] A. Haque and A. N. Khondker, "An efficient technique to calculate the normalized wave functions in arbitrary one-dimensional quantum well structures," J. Appl. Phys., vol. 84, pp. 5802–5804, 1998.

[48] M. Z. Kauser, M. S. Hasan, and A. Haque, " Effects of Wave Function Penetration into the Gate-Oxide on Self-Consistent Modeling of Scaled MOSFETs," IEEE Trans. Electron Devices, Vol. 49, No. 4, April 2002.

[49] S. Manzini and A. Modelli, "Tunneling discharge of trapped holes in silicon dioxides," in Insulating Films on Semiconductors, J. F. Verweij and D. R. Wolters, Eds. Amsterdam, The Netherlands: Elsevier, pp. 112–115, 1983.

[50] J. Robertson, "High dielectric constant oxides," Eur. Phys.J. Appl. Phys., vol. 28, no. 3, pp. 265–291, Dec. 2004.

[51] K. Matszuzawa, K. Uchida, and A. Nishiyama, "A unifiedsimulation of Schottky and Ohmic contacts," IEEE Trans. Electron Devices, vol. 47, no. 1, pp. 103–108, Jan. 2000.

[52] Darwish. M. N., Lentz. J. L., Pinto. M. R., Zeitzoff. P. M., Krutsick. T. J., Vuong. H.H., "An improved electron and hole mobility model for general purpose device simulation," in IEEE Trans. on Electron Devices, vol. 44, no. 9, September 1997.

[53] D. B. M. Klaassen, "A unified mobility model for device simulation —Part I: Model equations and concentration dependence," in Solid-State Electron., vol. 35, no. 7, pp. 953–959, 1992.

[54] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices," in IEEE Trans. Computer-Aided Design, vol. 7, pp. 1164–1171, Nov. 1988.

[55] S. A. Schwarz and S. E. Russek, "Semi-empirical equations for electron velocity in silicon—Part II: MOS inversion layer," IEEE Trans. Electron Devices, vol. ED-30, pp. 1634–1639, Dec. 1983.

[56] S. A. Mujtaba, R. W. Dutton, and D. L. Scharfetter, "Semi-empirical local NMOS mobility model for 2-D device simulation incorporating screened impurity scattering," in Proc. NUPAD V, June 1994.

[57] M. Shirahata, H. Kusano, N. Kotani, S. Kusanoki, and Y. Akasaka, "A mobility model including the screening effect in MOS inversion layer," IEEE Trans. Computer-Aided Design, vol. 11, pp. 1114–1119, Sept. 1992.

[58] A. Hartstein, T. H. Ning and, A. B. Fowler, "Electron scattering in silicon inversion layers by oxide and surface roughness," Surf. Sci., vol. 58, p. 178, 1976.

[59] Y. Matsumoto and Y. Uemura, "Scattering mechanism and low temperature mobility of MOS inversion layers," Jpn. J. Appl. Phys.,p. 367, 1974.

[60] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the university of inversion-layer mobility in Si MOSFET's—Part I: Effects of substrate impurity concentration," IEEE Trans. Electron Devices, vol. 41, pp.2357–2362, Dec. 1994.

[61] W. Zhu, J. Han, T. P. Ma, "Mobility Measurement and Degradation Mechanisms of MOSFETs Made with Ultrathin High-k Dielcctrics," in IEEE Transaction on Electron Devices, vol. 51, no. 1, January 2004.

[62] C.Y.Kang, "A study of Charge Trapping Effect on High-K Device Characteristics and Reliability; and its implication on Circuit Operation," PhD Dissertation, University of Texas at Austin,pp.90-92, December 2005