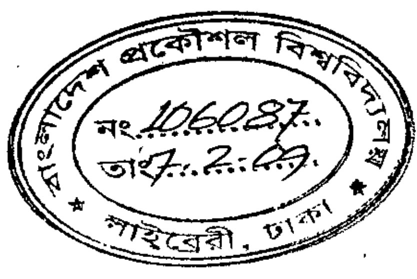
Effects of Source Drain Underlap on the Performance of Silicon Nanowire on Insulator Transistors



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MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

by

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The thesis titled " **Effects of Source Drain Underlap on the Performance of Silicon Nanowire on Insulator Transistors**" Submitted by Sishir Bhowmick, Roll No.: 100606212P, Session: October, 2006 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on December 28, 2008.

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Declaration

I hereby declare that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

(Sishir Bhowmick)

Dedication

To My Parents

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Abstract

The effects and their physics, of source-drain underlaps on the performance of silicon nanowire on insulator transistors are studied using three dimensional self-consistent Poisson-Schrodinger quantum simulation. Voltage control tunnel barrier with underlap is the device transport physics and dictates the performance of the device in the off state as well as in the on state. The off current, the on/off current ratio, and the inverse subthreshold slope improve significantly whereas the on current degrades slightly with underlap. The physics behind this behavior is the modulation of tunnel barrier with underlap. Underlap primarily affects the tunneling component of current and hence results in improvement in the subthreshold regime of the transistors and the degradation of the on state performance of the device is insignificant. About 50% contribution to the gate capacitance comes from the fringing electric fields emanating from the gate metal to the source and to the drain. The gate capacitance reduces with underlap, which can reduce the intrinsic switching delay and can increase the intrinsic cut-off frequency. However, both the on current and the transconductance reduce with underlap, and the consequence is the increase of delay and the reduction of cut-off frequency. The effects of gate length on the performance of the device have also been investigated. With the increase in gate length, the off state current reduces and the on-off ratio improves but the on state performance of the device degrades due to the increase in gate capacitance and reduction of transconductance. Therefore, appropriate choice of underlap, gate length, gate bias range and gate metal work function can optimize the device performance both in the off and on state.

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Chapter 1

Introduction

1.1 Literature Review

Silicon on insulator technology (SOI) refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics and nanoelectronics and as a result parasitic device capacitance is reduced and the device performance improved. SOI-based devices are fabricated on an electrical insulator, typically silicon dioxide or sapphire. The choice of insulator depends largely on intended application, with sapphire being used for radiation-sensitive applications and silicon dioxide preferred for improved performance and diminished short channel effects in microelectronics devices. The insulating layer and topmost silicon layer also vary widely with application. The first implementation of SOI was announced by IBM in August 1998.

The implementation of SOI technology is one of several manufacturing strategies employed to allow the continued miniaturization of microelectronic and nanoelectronic devices, colloquially referred to as extending Moore's Law. The benefits of SOI technology relative to conventional silicon (bulk CMOS) processing include

1. Lower parasitic capacitance due to isolation from the bulk silicon, which improves power consumption at matched performance. Resistance to latchup due to

complete isolation of the n- and p- well structures.

2. From amanufacturing perspective, SOI substrates are compatible with most conventional fabrication processes. In general, an SOI-based process may be implemented without special equipment or significant retooling of an existing factory.

Among challenges unique to SOI are novel metrology requirements to account for the buried oxide layer and concerns about differential stress in the topmost silicon layer. The primary barrier to SOI implementation is the drastic increase in substrate cost, which contributes an estimated 10 - 15 percent increase to total manufacturing costs.

IBM began to use SOI in high end RS64-IV Istar PowerPC processors in 2000. Other examples of microprocessors built on SOI technology include AMD's 130 nm, 90 nm and 65 nm single, dual and quad core processors since 2001.Freescale adopted SOI in their PowerPC 7455 CPU in late 2001, currently Freescale is shipping SOI products in 180nm, 130nm, 90nm and 65nm lines. The 90 nm Power Architecture based processors used in the Xbox 360, PlayStation 3 and Wii use SOI technology as well. Competitive offerings from Intel, however, such as the 65 nm Core 2 and Core 2 Duo microprocessors, are built using conventional bulk CMOS technology. Intel's new 45 nm process will continue to use conventional technology. However, Intel made a claim of single-chip silicon laser based on SOI.

1.2 Scaling of Devices and Silicon Nanowire Transistors

Scaling the transistor sizes has made significant improvement in the cost effectiveness and performance of integrated circuit over the last few decades [1]. The bulk CMOS technology is rapidly approaching the scaling limit and alternate materials or device

structures are essential for future electronics. One dimensional nanostructures such as the carbon nanotubes [2, 3, 4, 5] and silicon nanowires are the attractive materials for future nanoelectronics because their electronic properties can be controlled in a predictable manner. Controlled growth of silicon nanowires (SiNWs) down to 3 nm diameter [6], their applications as field-effect transistors (FETs) [7, 8, 9, 10], logic gates [11, 12, 13], and sensors [14, 15] have been demonstrated. Potential advantages of SiNWFETs over the planar state-of-the-art silicon devices have been examined [7, 16]. Using seminumerical ballistic model, Wang *et. al* [10] have shown that the on current of an n-channel SiNWFET is almost double the on current delivered by the equivalent p-channel FET for larger diameter nanowire, and approaches that of p-channel FET for smaller diameter nanowire. The electron velocity is higher for thicker wires and lower for thinner wires when compared to that of a planar MOSFET [10, 17].

When the transistors are scaled to nanometer regime, the device performance degrades mainly due to the short channel effects [18]. The scaling of bulk silicon MOSFETs has been facilitated by introducing the device structures with source-drain underlaps [19]. However, large underlaps are required for optimal performance of bulk MOSFETs [20], and ultra-thin body or FinFETs with undoped channels and bias dependent effective channel lengths have been proposed as the substitutes for optimal device performance [21, 22]. Source-drain underlaps have been used to improve the device performance for carbon nanotube transistors [4, 23] and silicon nanowire field-effect transistors (SiNWFETs) [24]. Shin uses multiple gates SiNWFETs and study the subthreshold behaviors with source-drain underlaps [24].

1.3 Objective of the Work

This work is primarily concerned with the study of the performance of silicon nanowire transistor with source drain underlap. The primary goal is to develop a solver that solves three dimensional Poisson-Schrodinger system quantum-mechanically. The

solver is a general one and can handle any nanowire device with a minor changes in parameter.

Several authors previously tried to study the effects of underlap on nanowire transistors mostly using 1-D or 2-D Poisson-Schrodinger solver [20] and reported primarily on the subthreshold region of the transistor operation. In this work, the effects of underlap on the on state performance of the device has been calculated using 3-D Poisson-Schrodinger solver.

The off state performances such as on/off current ratio, transconductance, inverse subthreshold slope with underlap have been calculated from I-V profile. The on state performances such as intrinsic gate delay, intrinsic cutoff frequency for different underlaps have also been calculated.

The off state performances such as on/off current ratio, transconductance, inverse subthreshold slope and on state performance such as intrinsic gate delay, intrinsic cutoff frequency for different gate lengths have also been calculated.

1.4 Organization of the thesis

The first chapter deals with the literature review and objective of the thesis. The second chapter deals with the 3-D Poisson's equation, tight binding Hamiltonian formulism, Non-equilibrium Green's function and the self-consistent solution. Non-equilibrium Green Functions algorithm has been used to get charge density profile. The Poisson's equation was solved in 3-D cartesian co-ordinates system. The second chapter also deals with the the calculation of I-V characteristics from effective mass approximation. The third chapter discusses the results of the work. Then conclusion and suggestion on the future works are made in the fourth chapter.

Chapter 2

Methodology

2.1 3-D Poisson's Equation

The simulation model uses a self-consistent solution between three dimensional (3D) Poisson equation and effective mass Schrodinger equation. The 3D Poisson equation in cartesian coordinates is

$$\frac{\partial}{\partial x}\left(\epsilon\frac{\partial V}{\partial x}\right)+\frac{\partial}{\partial y}\left(\epsilon\frac{\partial V}{\partial y}\right)+\frac{\partial}{\partial z}\left(\epsilon\frac{\partial V}{\partial z}\right)=-\frac{\rho}{\epsilon_o}, \tag{2.1}$$

where ϵ_o is the free space permittivity, ϵ is the relative dielectric constant, V is the 3D potential, and ρ is the charge density, which is non-zero in silicon nanowire only. Poisson kernel is created by discretizing Equation (2.1). We discretize Equation (2.1)using finite difference which can handle both equal and non equal grid spacing. After discretizing the equation becomes

$$\begin{aligned} a(i)V_{i+1,j,k} + b(i)Vi-1,j,k + a(j)V_{i,j+1,k} + b(j)V_{i,j-1,k} \\ +a(k)V_{i,j,k+1} + b(k)V_{i,j,k-1} + c(i,j,k)V_{i,j,k} = -\frac{\rho}{\epsilon_o} \end{aligned} \tag{2.2}$$

where,

$$a(i)=\left[\frac{\epsilon_{i+1,j,k}-\epsilon_{i-1,j,k}}{(2\Delta x_i)^2}+\frac{\epsilon_{i,j,k}}{(\Delta x_i)^2}\right]$$

$$b(i) = \left[\frac{\epsilon_{i-1,j,k} - \epsilon_{i+1,j,k}}{(2\Delta x_i)^2} + \frac{\epsilon_{i,j,k}}{(\Delta x_i)^2}\right]$$

$$a(j) = \left[\frac{\epsilon_{i,j+1,k} - \epsilon_{i,j-1,k}}{(2\Delta y_j)^2} + \frac{\epsilon_{i,j,k}}{(\Delta y_j)^2}\right]$$

$$b(j) = \left[\frac{\epsilon_{i,j-1,k} - \epsilon_{i,j+11,k}}{(2\Delta y_j)^2} + \frac{\epsilon_{i,j,k}}{(\Delta y_j)^2}\right]$$

$$a(k) = \left[\frac{\epsilon_{i,j,k+1} - \epsilon_{i,j,k-1}}{(2\Delta z_k)^2} + \frac{\epsilon_{i,j,k}}{(\Delta z_k)^2}\right]$$

$$b(k) = \left[\frac{\epsilon_{i,j,k-1} - \epsilon_{i,j,k+11}}{(2\Delta z_k)^2} + \frac{\epsilon_{i,j,k}}{(\Delta z_k)^2}\right]$$

$$c_{i,j,k} = -2\left[\frac{1}{(\Delta x_i)^2} + \frac{1}{(\Delta y_j)^2}\frac{1}{(\Delta z_k)^2}\right] \tag{2.3}$$

Here Δx, Δy, Δz are the grid spacing in x, y and z direction respectively and $i = 1, 2, 3, \ldots\ldots N_x$, $j = 1, 2, 3, \ldots\ldots N_y$, $k = 1, 2, 3, \ldots\ldots N_z$ where N_x, N_y and N_z are the number of grid points in x, y, and z direction respectively. In matrix form Equation (2.2) can be written as

$$DV = f \tag{2.4}$$

The matrix D can be regarded as a block hepta-diagonal sparse matrix. Dirichlet boundary conditions are used at the gate metal. Von Neumann boundary conditions are used in source and drain and along the exposed surface of the dielectric. There, the radial component of the electric field is set to zero. After setting the boundary conditions, Equation(2.4) is solved using Newton-Rapshon method and updated in each iteration in the self-consistent loop as

$$\mathbf{V}^{i+1} = \mathbf{V}^{i} + m\Delta\mathbf{V}, \tag{2.5}$$

where,

$$\Delta\mathbf{V} = \left[\mathbf{D} - \frac{\delta\mathbf{f}}{\delta\mathbf{V}}\right]^{-1} \{\mathbf{DV} - \mathbf{f}\} \tag{2.6}$$

and m is a mixing factor. We calculate $\frac{\delta\mathbf{f}}{\delta\mathbf{V}}$ from [25]

$$\frac{\partial\rho_L}{\partial V} = (2q)\int\frac{dE}{2\pi}\mathrm{tr}\left\{\frac{-\partial f_S}{\partial E}A^L_{L,L} + \frac{-\partial f_D}{\partial E}\left[A_{L,L} - A^L_{L,L}\right]\right\}. \tag{2.7}$$

For charge density and current calculations, we use tight binding hamiltonian formulism and apply the recursive Green's function algorithm (RGA) to solve the non-equilibrium Green function (NEGF) equations [26, 27].

2.2 Tight Binding Hamiltonian Formulism

The Schrodinger equation in 3D cartesian coordinates is

$$-\frac{\hbar^2}{2}\left[\frac{\partial}{\partial x}\left(\frac{1}{m_x}\frac{\partial\psi}{\partial x}\right) + \frac{\partial}{\partial y}\left(\frac{1}{m_y}\frac{\partial\psi}{\partial y}\right) + \frac{\partial}{\partial z}\left(\frac{1}{m_z}\frac{\partial\psi}{\partial z}\right)\right] = E\psi \tag{2.8}$$

where, ψ is the wave function, m_x, m_y, and m_z are the effective masses in device coordinates, and $\hbar$ is the reduced Planck's constant. The nanowire is grown in $\langle 100\rangle$ direction, which is device x coordinate in our study. Ballistic transport is assumed and recursive Green's function algorithm (RGFA) [26, 28] is used to solve Schrodinger equation for charge density and current calculations. The open boundary condition in transport direction (x) is included in Schrodinger equation via self-energy matrices

and hard-wall boundary condition is used in the transverse directions (y and z). The Schrodinger equation is discretized using finite difference method and it becomes

$$t_x\psi_{i+1,j,k} + t_x\psi_{i-1,j,k} + t_y\psi_{i,j+1,k}t_y\psi_{i,j-1,k} + t_z\psi_{i,j,k+1} + t_z\psi_{i,j,k-1} = E\psi_{i,j,k} \quad (2.9)$$

where,

$$\begin{aligned} t_x &= -\frac{\hbar^2}{2m_x(\Delta x)^2} \\ t_y &= -\frac{\hbar^2}{2m_y(\Delta y)^2} \\ t_z &= -\frac{\hbar^2}{2m_z(\Delta z)^2} \end{aligned} \quad (2.10)$$

Here Δx, Δy, Δz are the grid spacing in x, y and z direction respectively and $i = 1, 2$, $j = 1, 2, 3, ...N_y$, $k = 1, 2, 3, ...N_z$ where, N_y and N_z are the number of grid points in y, and z direction respectively. For RGFA, the layer (cross-section) Hamiltonian and layer-to-layer coupling matrices are calculated from discretized Schrodinger equation. The left hand side of the Schrodinger equation can be represented in matrix form as

$$\boldsymbol{D} = \begin{bmatrix} & & \vdots & & \\ & \boldsymbol{h_{00}} & & \boldsymbol{t_{01}} & \\ & & \cdot & & \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ & \boldsymbol{t_{10}} & & \boldsymbol{h_{11}} & \\ & & \vdots & & \end{bmatrix}$$

Where, h_{00} and h_{11} are the layer hamiltonian and t_{01} and t_{10} are the layer to layer coupling matrix. From the hamiltonian we generate the right connected Green's function.

2.3 Non-equilibrium Green's Function

With layer Hamiltonian H_i and layer-to-layer coupling matrix t, we create the right-connected Green function at each layer (cross-section) from

$$g_{i,i} = \left(EI - H_i - U_i - t_{i,i+1}g_{i+1,i+1}t_{i+1,i}\right)^{-1}, \tag{2.11}$$

where, U_i is the potential energy at the ith cross-section (layer) obtained from Poisson solver and I is the identity matrix. The full Green's function [26, 29] at the first layer is calculated from

$$G_{1,1} = \left(EI - D_1 - \Sigma_S - t_{1,2}g_{2,2}t_{2,1}\right)^{-1}, \tag{2.12}$$

where, $\Sigma_S = t_{1,0}g_{0,0}t_{0,1}$ is the self-energy matrix and $g_{0,0}$ is the surface Green's function. The surface Green's function is calculated from decimation method and Ref. [30] has a detail discussion. The rest $\{2, \ldots, N_x\}$ block diagonal elements of the full Green's function are calculated from

$$G_{i,i} = g_{i,i} + g_{i,i}t_{i,i-1}G_{i-1,i-1}t_{i-1,i}g_{i,i}. \tag{2.13}$$

We calculate the first column blocks of full Green's function from

$$G_{i,1} = g_{i,i}t_{i,i-1}G_{i-1,1} \tag{2.14}$$

and the left connected spectral function from

$$A^L_{i,i} = G_{i,1}\Gamma_{1,1}G^\dagger_{i,1}, \tag{2.15}$$

where, $\Gamma_{1,1} = i\left(\Sigma_S - \Sigma_S^\dagger\right)$ is the broadening function. The charge density at each cross-section is calculated from

$$\rho_{i,i} = (2e)\int \frac{dE}{2\pi}\text{diag}\left\{f_S A^L_{i,i} + f_D\left[A_{i,i} - A^L_{i,i}\right]\right\}, \tag{2.16}$$

where, e is the electronic charge, f_S and f_D are the source and drain Fermi functions, respectively, and the full spectral function is obtained from $A_{i,i} = \sqrt{-1}(G_{i,i} - G^\dagger_{i,i})$. The factor 2 at the beginning of right hand side of Equation (2.16) includes spin

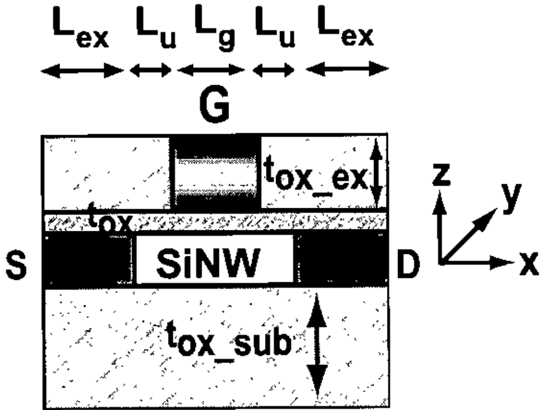


Figure 2.1: Cross section of the simulated device

degeneracy. Note that the charge density $\rho_{i,i}$ is a column vector of length $N_y \times N_z$ and is created by taking the diagonal elements of the matrix in the brace of the right hand side of Equation (2.16).

The self-consistent loop is started with the initial guess of the potential profile. Anderson mixing [31] scheme is used for convergence acceleration. Once the convergence is achieved, the coherent drain current is calculated from

$$I_D = \frac{2e}{h} \int dE \; T(E) \, (f_S - f_D) \, , \tag{2.17}$$

where, transmission $T(E)$ is calculated from [26]

$$T(E) = \mathrm{tr} \left(\Gamma_{1,1} \left[A_{1,1} - G_{1,1} \Gamma_{1,1} G_{1,1}^{\dagger} \right] \right) . \tag{2.18}$$

2.4 Self-consistent Solution

Details of the device shown in Figure 2.1 are as follows. The silicon nanowire is placed on a thick oxide layer t_{ox-sub}. The gate oxide t_{ox} is grown on the nanowire. A gate metal of length L_g is deposited on gate oxide and the exposed regions on both sides of the gate metal are covered by oxide t_{ox-ex}.

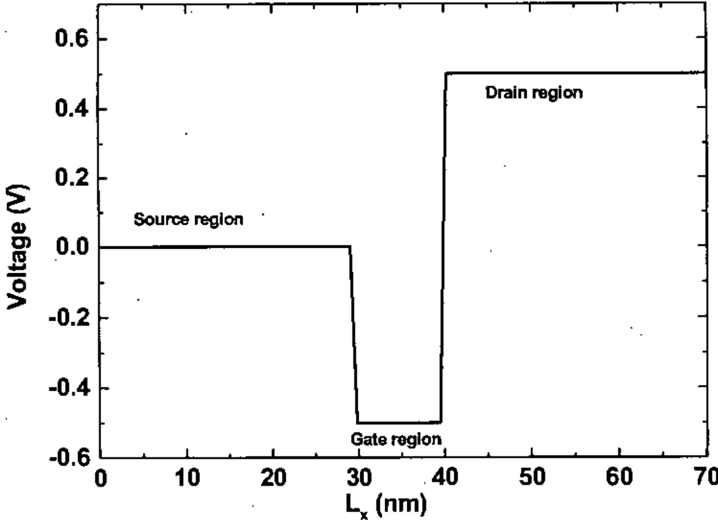


Figure 2.2: Initial guess of the potential profile

The nanowire under the gate region and the underlaps L_u between the n-type doped source and drain extension L_{ex} are undoped. The gate length L_g is 10 nm and the gate oxide thickness t_{ox} is 1 nm. The silicon nanowire (SiNW) has a square cross-section of 5×5 nm^2 and a band gap E_g value of 1.38 eV (calculated from the E-K relation). The substrate oxide, the gate oxide, and the extended oxide are assumed to be SiO_2 with a dielectric constant value of 3.9. The source Fermi level is set to zero (0) and the drain Fermi level to -V_{DS}. The gate metal is assumed to have the same work function value as the nanowire has. The L_{ex} value of 20 nm, the t_{ox-sub} value of 5 nm, and the t_{ox-ex} value of 5 nm are assumed for Poisson solver so that the fringing electric fields are treated correctly. The self-consistent solution starts by guessing an initial voltage profile given in Figure2.2 Initially potential at the source, drain region and gate region are set to 0 V, 0.5 V and -0.5 V respectively.Then charge density is calculated only for the nanowire using recursive Green's function algorithm. The charge density outside the nanowire region is considered to be zero. Then Equation (2.4) is solved from the calculated charge density profile using Newton-

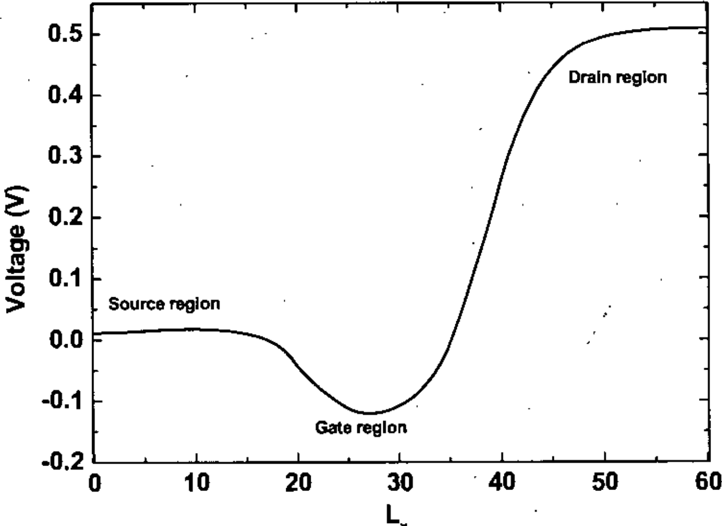


Figure 2.3: Converged potential profile along the silicon nanowire

Rapshon method and updated in each iteration in the self-consistent loop as

$$\mathbf{V}^{i+1} = \mathbf{V}^{i} + m\Delta\mathbf{V}, \tag{2.19}$$

where

$$\Delta\mathbf{V} = \left[\mathbf{D} - \frac{\delta\mathbf{f}}{\delta\mathbf{V}}\right]^{-1} \{\mathbf{DV} - \mathbf{f}\} \tag{2.20}$$

and m is a mixing factor. The loop is conducted over and over the the necessary conditions for convergence is obtained. For the quick convergence of the system we used well established Anderson mixing algorithm. The convergence criteria of the system was set to a voltage difference of $\leq$1 mV for all grid points from the previous iteration. A converged potential profile is shown in Figure 2.3

Chapter 3

Results and Discussions

3.1 I-V characteristics

We applied our simulation model on a silicon nanowire device shown in Figure 2.1

To investigate the effects of gate length, gate length L_g of the device is varied keeping the underlap at zero nm and all other parameters unchanged. A 20 nm doped source-drain extension (L_{ex}) with a uniform doping concentration value of $1.5\times10^{19}/cm^3$ is assumed in our simulation in both cases. The nanowire is model using bulk effective mass parabolic band structure. Using the tight binding (TB) dispersion relation and the bulk effective mass model, Wang *et al.* [32] argued, using a semiclassical over the top of the barrier model, that the bulk effective mass model overestimates the threshold voltage for wire width < 3 nm and the on current for wire width < 5 nm. Using $sp^3d^5s^*$ orbital basis, Zheng *et al.* [33] shows that the bulk masses are quite similar to the confinement masses for wire thickness greater than 3 nm. Poisson solver uses an extension of dielectric $t_{ox-ex} = 5$ nm in the z-direction and equal the width of the nanowire on either side of the wire (y-direction) so that the fringing electric fields emanating from the gate metal are captured.

As the dimension of the nanowire in our simulated device is very small, the confinement effects becomes important. Therefore the band gap of the nanowire is different from the bulk silicon band gap of 1.12 eV. We calculated the band gap of the silicon nanowire from the effective mass Schrodinger equation. The band structure of silicon

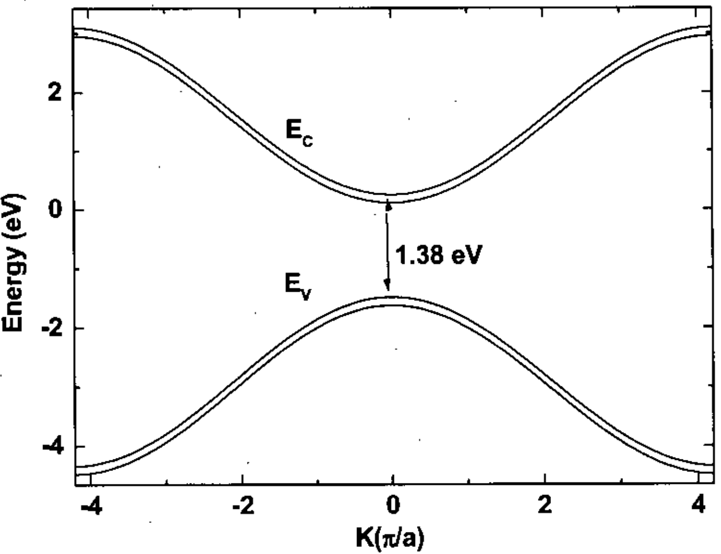


Figure 3.1: Band structure of silicon nanowire using parabolic approximation

nanowire is given in figure Figure 3.1.

In our simulation model uses effective mass Schrodinger equation so the band structure of the silicon nanowire is parabolic in shape. From the plot we calculated the band gap of the silicon nanowire to be 1.38 eV.
The simulated $\log I_D - V_{GS}$ plots for six different values of underlap are shown in Figure 3.2.From the figure we see the off current as well as the on current reduces with the increase of underlap. For a change of L_u from 0 to 13 nm, the off current reduces from $2.5 \times 10^{-5}\mu A$ to $3.0 \times 10^{-8}\mu A$ and the on current reduces from 3.8 μA to 0.15 μA. Here off current means the drain current when $V_{gs} = 0V$ and on current means the drain current when $V_{gs} = 0V$. From the data we see while the on current reduces by about one order of magnitude, the off current reduces by almost three orders of magnitude.

To understand the physics of off-state and on-state current reduction with underlap, we plot, in Figure 3.3, the band profiles superimposed on the energy distribution of current for two different values of underlap, 0 nm and 5 nm.

The source Fermi level is set to 0 eV and the drain Fermi level to -0.5 eV. Both the off-

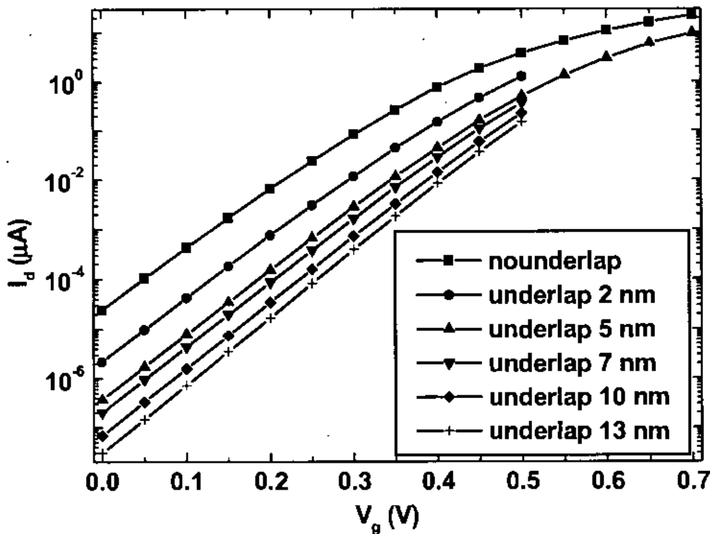
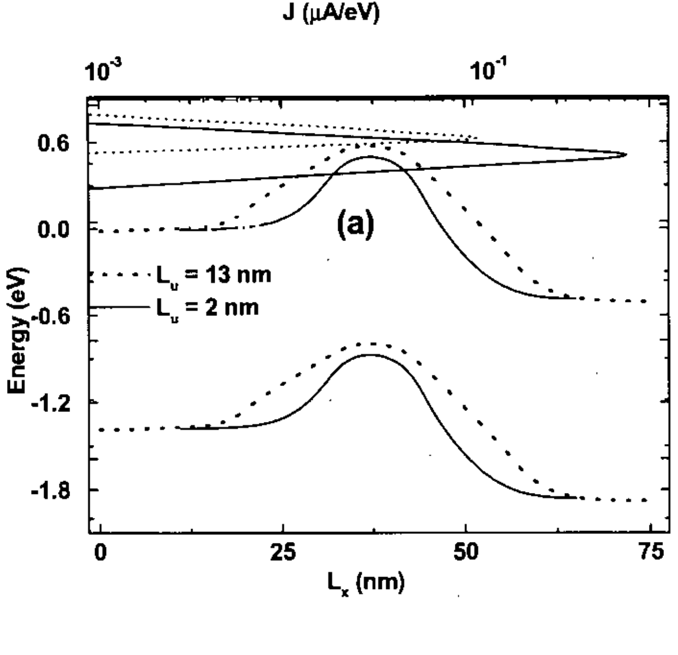


Figure 3.2: Drain current vs gate bias voltage for different underlaps

state and the on-state currents have the thermal and the tunneling components. For $L_u = 2$ nm, the tunneling component of the off-state current is $2.07 \times 10^{-6} \mu A$ and the thermal component is $1.7 \times 10^{-7} \mu A$. These values are $1.8 \times 10^{-8} \mu A$ and $1.199 \times 10^{-8} \mu A$, respectively, for $L_u = 13$ nm in the off-state. The on-state current for 2 nm underlap has $0.85 \mu A$ tunnel component and $0.42\ \mu A$ thermal component. These values for 13 nm underlap device are $0.078\ \mu A$ and $0.071\ \mu A$, respectively. The potential barrier length as well as the height becomes larger with the increase of underlap. This reduces both the tunneling and the thermal components of current. The underlap primarily affect the tunneling current and the effect of underlap is higher in the off-state.

Charge density vs gate voltage profile in the nanowire is plotted in Figure 3.4. From the figure we see that the electron charge density in the channel is initially very low as the channel is intrinsic and increases rapidly with the bias voltage and results in a drastic increment in drain current.

The off current, the on current, the on/off current ratio, and the inverse subthreshold slope (SS) are plotted in Figure 3.5 as a function of source-drain underlap.



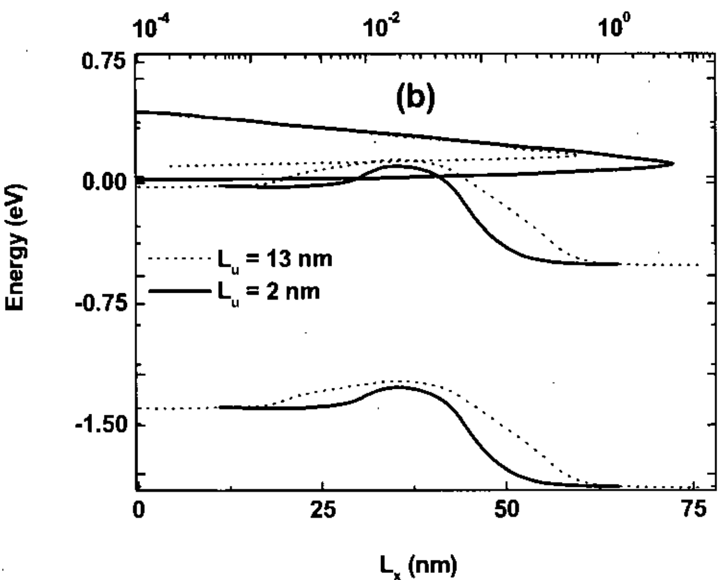


Figure 3.3: (a) Valance band and conduction band for two different lengths of underlap at off state (b) Valance band and conduction band for two different lengths of underlap at on state

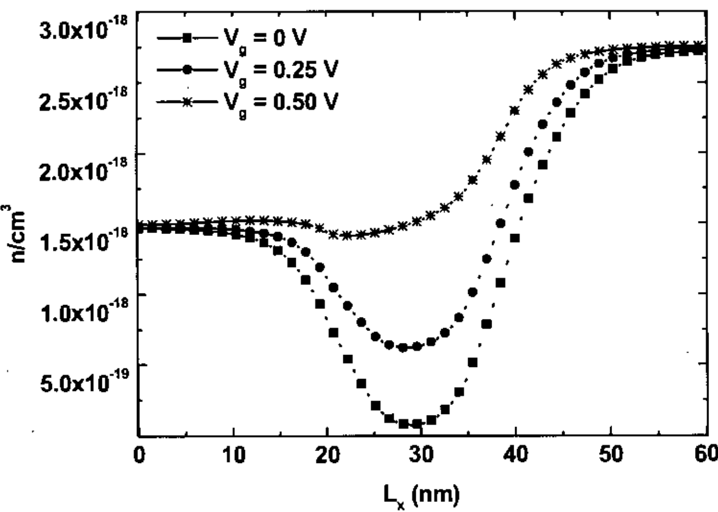


Figure 3.4: Electron charge density vs gate bias voltage

Both the on current and the inverse subthreshold slope reduce rapidly with L_u and then get almost saturated when L_u is about 6 nm. The off current and the on/off current ratio, on the other hand, do not show this behavior. This is because the effects of underlap in the off-state is more significant than its effects in the on-state. If an underlap value of 5 nm is assumed as an optimal design (as the on current and the SS do not change significantly after L_u = 5 nm), then the inverse subthreshold slopes improves from 81 to 75 mV/dec, the off current changes from $2.5 \times 10^{-5} \mu$A to $3.7 \times 10^{-7} \mu$A, the on/off current ratio improves from 1.5×10^{5} to 1.4×10^{6}, and the on current degrades from 3.8 μA to 0.51 μA. The improvement of off-state current and inverse subthreshold slope with gate underlap, and degradation of on-state current with gate underlap for gate-all-around and tri-gate silicon nanowire transistors have been reported by Shin [24]. The exponential fit to the simulated data for the off current and the on current

$$I_{off}(L_u) = 2.396 \times 10^{-5} \exp[-1.259 L_u] + 6.776 \times 10^{-7} \exp[-0.2847 L_u] \quad (3.1)$$

$$I_{on}(L_u) = 2.289 \exp[-0.8361 L_u] + 0.9542 \exp[-0.1431 L_u] \quad (3.2)$$

are shown in Figure 3.5 (a) and (b) as the dotted lines. A polynomial fit to second

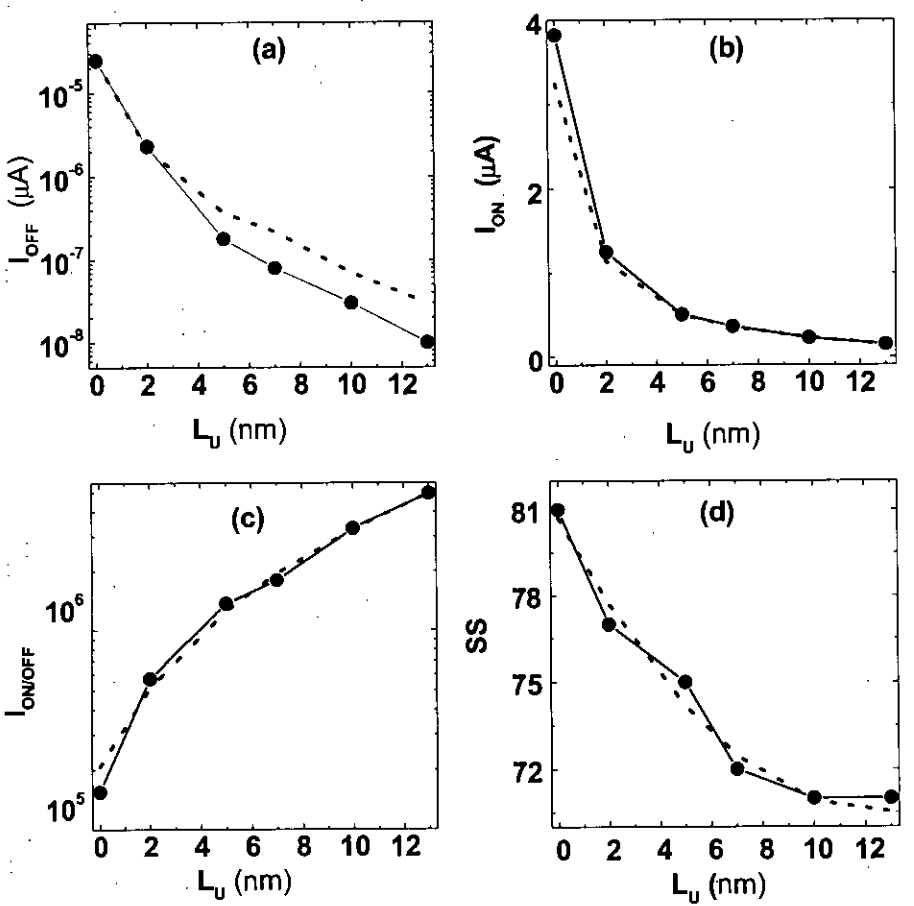


Figure 3.5: (a) Off current vs underlap (b) On current vs underlap (c) On-off current ratio vs underlap (d) Inverse subthreshold slope vs underlap. The dotted lines represents respective empirical fits.

order of the on/off current ratio and the inverse subthreshold slope results in

$$I_{on-off}(L_u) = 1.933 \times 10^4 L_u^2 + 1.136 \times 10^5 L_u + 2.08 \times 10^5 \tag{3.3}$$

$$SS(L_u) = 0.06534 L_u^2 - 1.633 L_u + 80.7 \tag{3.4}$$

The polynomials are shown in Figure 3.5 (c) and (d) as the dotted lines. Note that the on/off current ratio of 1.5×10^5 without source-drain underlap is already a decent value and the on current goes below 1.0 μA for a source-drain underlap value of 5 nm or higher. This is because of the particular device and the particular bias range (0 to 0.5 V) that have been used in this simulation study. A 10 nm gate length introduces sufficient tunnel barrier to reduce the tunneling leakage current in the off-state and to obtain a decent value of on/off current ratio. Simulations (results are not shown here) for a 5 nm gate length device with the same gate bias range (0 to 0.5 V) and drain bias fixed to 0.5 V shows that the on/off current ratio without underlap is 2.6×10^2 and it is 3.7×10^4 for 5 nm underlap. The on current with underlap goes below 1.0 μA because the significant contribution to the on current is the tunneling component (see discussion regarding Figure 3.3). This can be improved by extending the bias range or engineering the gate metal work function so that a flat band between the source Fermi level and the channel potential under the gate is obtained in the on-state. The nanowire has a band gap value of 1.38 eV. With the gate metal work function value equal to the nanowire, a flat band situation between the source Fermi level and the channel potential is obtained when the applied gate bias is about half of the band gap (0.7 eV). By extending the gate bias range from 0 to 0.7 V with drain bias fixed to 0.5 V, simulations show that the on current for 10 nm gate device changes from 22.6 μA to 11.3 μA for a change of underlap value from 0 to 5 nm.

We also simulated the effects of gate length on the performance of the silicon on insulator transistor. The drain current vs gate voltage for three different gate lengths are plotted in Fig. 3.6

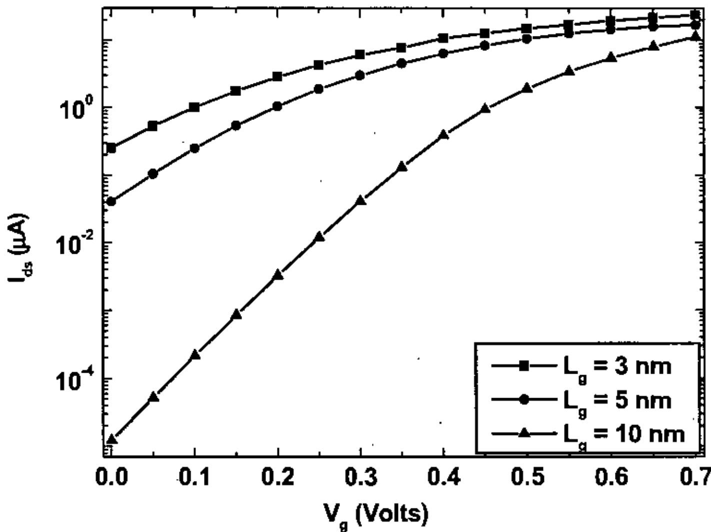


Figure 3.6: Drain current vs gate bias voltage for three different gate lengths.

From the figure we see that the on current (for $V_{gs} = 0.7V$) for different gate lengths are of the same order but the reduces drastically with the gate length.The simulated off current versus gate length and on current versus gate length are shown in Figure 3.7. The off and on currents are the drain currents corresponding to V_{GS} = 0 V, V_{DD} = 0.5 V and V_{GS} = 0.7 V, V_{DD} = 0.5 V respectively. From the figure we see that the on state currents for different gate lengths are of the same order but the off currents significantly reduce with increased gate length. For the change in gate length from 5 nm to 10 nm, on current reduces from 19.2 μA to 11.3 μA while the off current reduces from 0.047 μA to 1.23×10^{-5} μA.

The scaling behavior of inverse subthreshold slope and on/off current ratio with gate length L_g are shown in Figure 3.8.

Change in gate length from 5 nm to 10 nm improves the on/off current ratio by three orders of magnitude and the inverse subthreshold slope from 141.68 mV/dec to 82.59 mV/dec. Device performance degrades with shorter gate due to short channel effects. The physics behind this phenomenon can be understood from the conduction band profile shown in Figure 3.9.

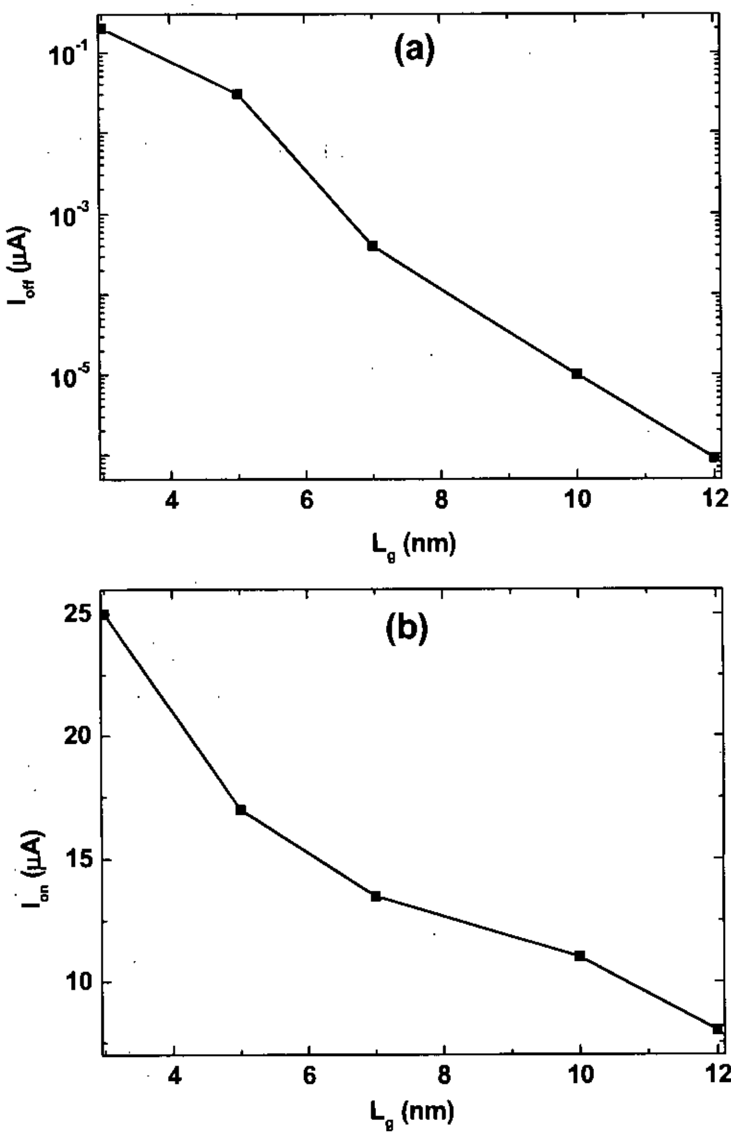


Figure 3.7: (a) Off current versus gate length (b) On current versus gate length.

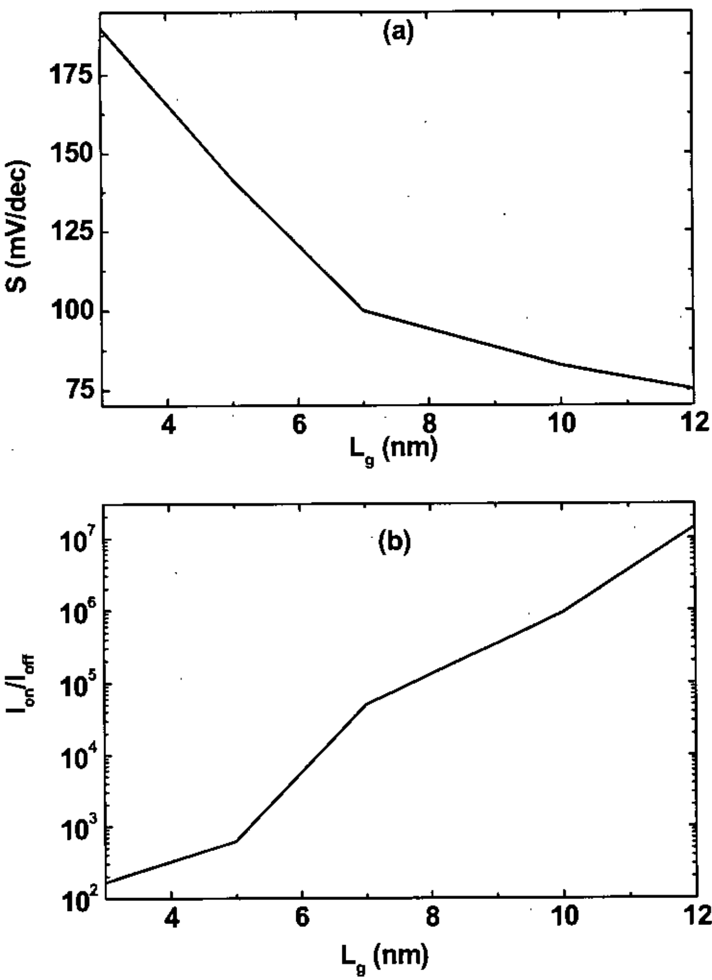


Figure 3.8: (a) Inverse subthreshold slope versus gate length (b) on/off current ratio versus gate length.

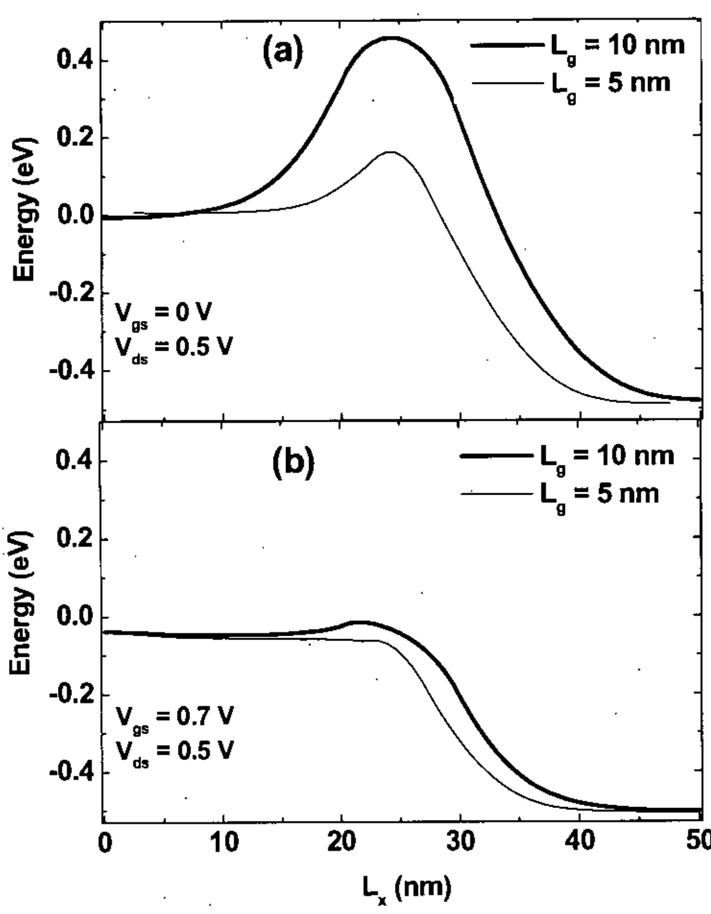


Figure 3.9: (a) Conduction band profile in the off state (b) Conduction band profile in the on state.

From the figure we see that in the off state the tunnel barrier height and width for $L_g = 10$ nm is significantly higher than that of $L_g = 5$ nm and therefore tunneling current (major component of off state current) for $L_g = 10$ nm through the barrier is greatly reduced compared to that of $L_g = 5$ nm while in the on state there is no significant the potential barrier difference for these two different gate length and hence the resulting on state currents are of the same order of magnitude.

3.2 Performance Metrics

Next we study the effects of source-drain underlap on the gate capacitance C_g, the intrinsic switching delay τ_S, and the intrinsic cut-off frequency f_T. For this, the gate capacitance is calculated from

$$C_g = \int\int dxdy \frac{\delta D_z}{\delta V_g} + \int\int dydz \frac{\delta D_x}{\delta V_g}, \tag{3.5}$$

The total gate capacitance is calculated from $C_g = C_b + C_s + C_d$. The first integral in equation Equation 3.5 takes care of the electric fluxes emanating from the bottom surface (associated with C_b) of the gate metal and the second integral takes care of the fringing fields emanating from the two sides of the gate metal (associated with $C_s and C_d$)facing to the source and drain. The intrinsic switching delay is calculated from $\tau_S = C_g V_{DD}/I_{ON}$ and the intrinsic cut-off frequency from $f_T = g_m/2\pi C_g$. The on-state current I_{ON} is the drain current corresponds to $V_{DS} = V_{GS} = 0.5$ V, V_{DD} is 0.5 V in this study, and the transconductance is calculated from $g_m = \partial I_D/\partial V_{GS}$.

The gate capacitance values and the percentage contribution of its different components versus gate bias are shown in Figure 3.10.

Here C_b corresponds to the contribution from the fluxes emanating from the bottom surface of the gate metal and evaluated by the first integral of Equation 3.5, and C_s and C_d are the fringing field contributions emanating from the left side of the gate metal to the source, and from the right side of the gate metal to the drain,

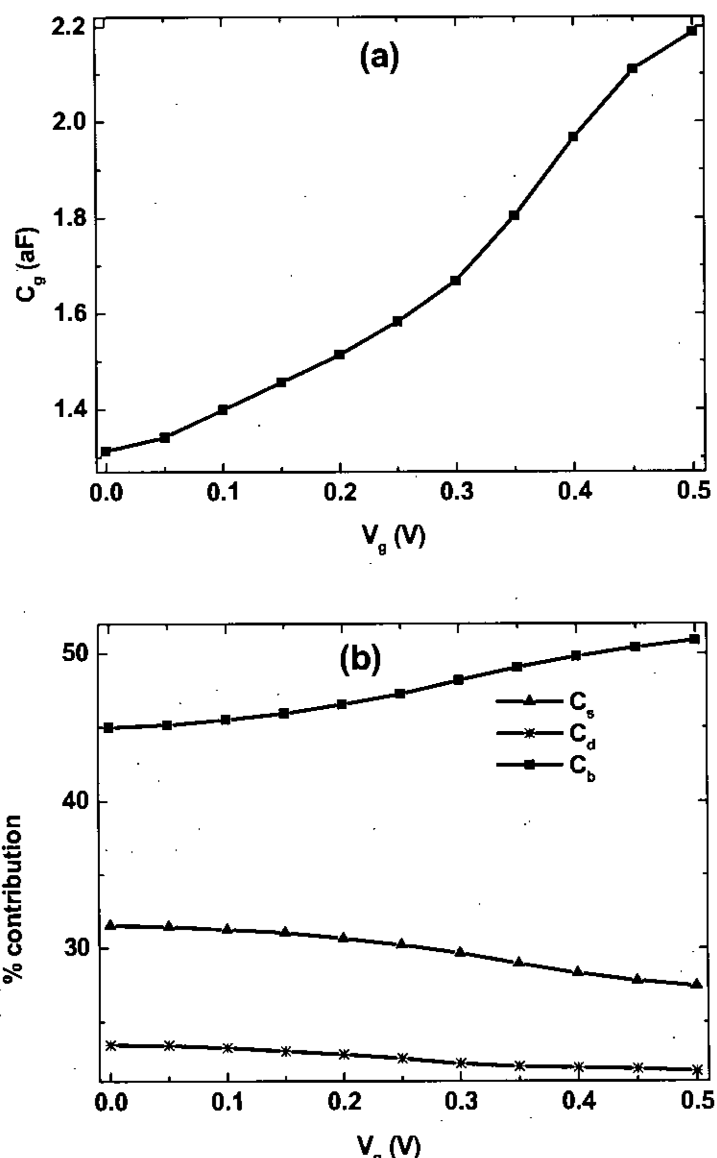


Figure 3.10: (a) On state gate capacitance C_g vs gate bias V_{gs} (b) Percentage contribution of different components of gate capacitance vs gate bias V_{gs}.

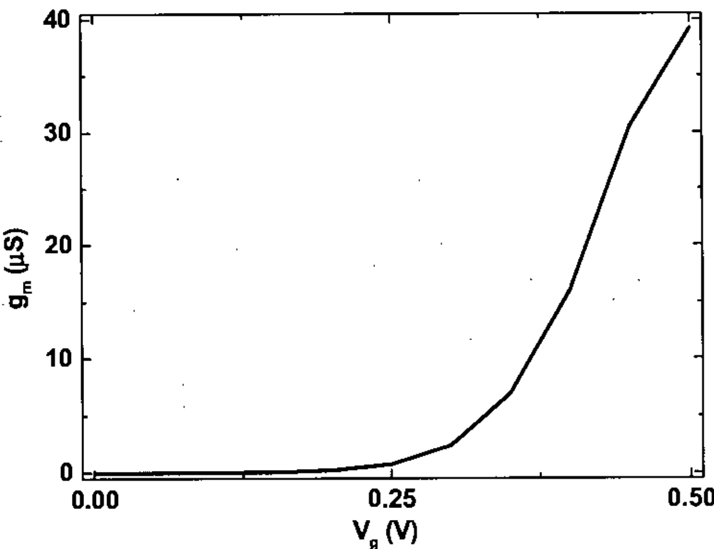
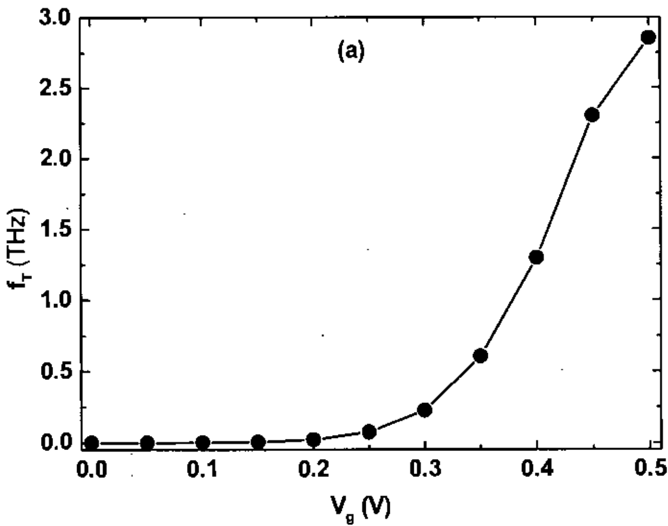


Figure 3.11: Transconductance g_m vs gate bias V_{gs}

respectively, and are evaluated from the second integral of Equation 3.5. The major contribution comes from C_b and its value in on-state is 51%. The value of C_b ranges from 45% to 51% over the entire range of gate voltage and the rest (almost 50%) comes from the fringing fields. In Figure 3.11, we plot the transconductance vs gate bias voltage profile for 0 nm underlap. From the plot we see that the transconductance was initially very low and improves with the gate bias voltage. For the change of gate bias voltage from o V to 0.5 V, transconductance changes from 0.0016 μS to 39.2 μS.

In Figure 3.12, we plot the on state switching delay and the on state intrinsic cut-off frequency with the gate bias voltage.

Although the gate capacitance increases with the gate bias voltage, the intrinsic gate delay reduces and the intrinsic cut-off frequency increases with gate bias voltage. The fact behind it is that both the transconductance and the drain current increases rapidly with gate bias and dominate over the negative impact of the increment of gate capacitance on intrinsic gate delay and intrinsic cut-off frequency.



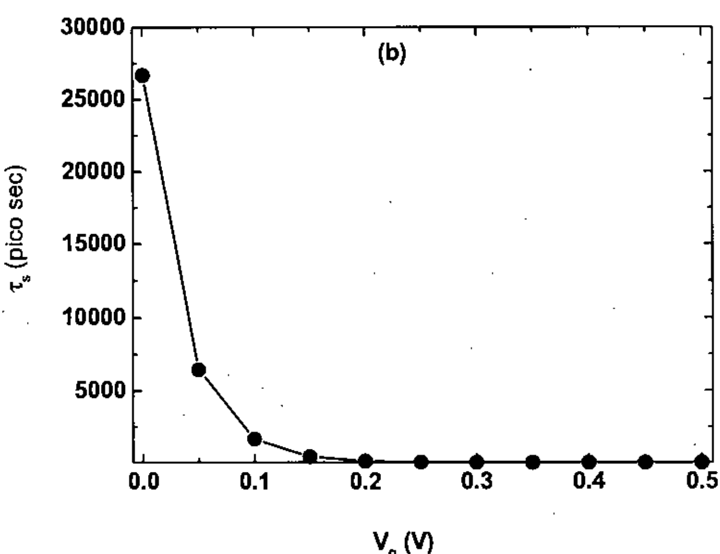


Figure 3.12: (a) On state intrinsic gate delay τ_S vs gate bias V_{gs} (b) On state intrinsic cut-off frequency τ_S vs underlap V_{gs}

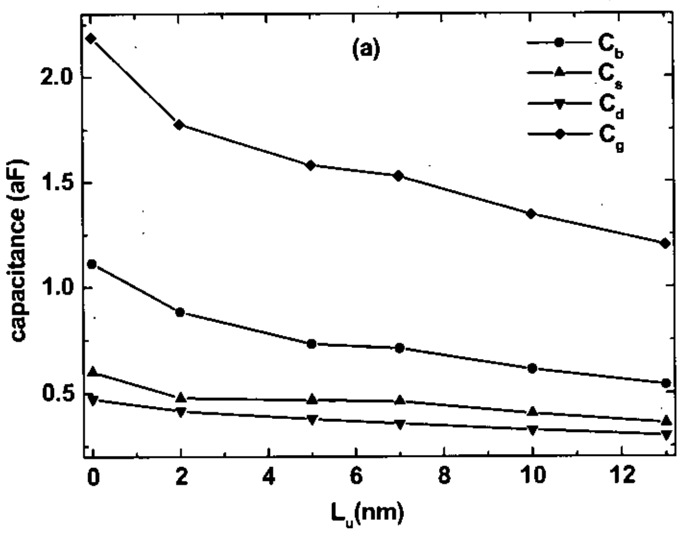
In Figure 3.13, we plot the on-state gate capacitance and its different components (C_b, C_s, and C_d) frequency as a function of underlap.

From the plot we see that the on state gate capacitance reduces with under as its all three components decreases. Looking at the percentage contribution we see that the percentage contribution of the bottom capacitance decreases and the percentage contribution of the fringing field components increases with underlap.

The transconductance vs underlap profile is plotted in figure Figure 3.14.

Looking at the plot we see that the on state transconductance drops with the increment of underlap. For the change of underlap from 0 nm to 13 nm the transconductance reduces from 39.2 μS to 2.25 μS.

Figure 3.15 shows the effects of underlap on the intrinsic gate delay and the intrinsic cut-off frequency. The gate capacitance reduces with underlap that should reduce the switching delay. However, the on current also reduces with underlap, and the combined effect is increase of the switching delay. The reduction of g_m with underlap should reduce f_T and the reduction of C_g with underlap should increase f_T. However, the reduction rate of g_m is higher and the consequence is the reduction of f_T. The gate capacitance, the transconductance, the cut-off frequency all have significant change with underlap up to 5 nm. After L_u = 5 nm, their changes are not large. However, the switching delay does not show this behavior. For a change of L_u from 0 to 5 nm, the τ_S increases from 0.286 to 1.557 pico second and the f_T reduces from 2.85 to 0.71 THz. We observe improvement in the switching delay and cut-off frequency when the bias range is extended to achieve the source-channel flat band in the on-state. Simulations for the same 10 nm gate device with the gate bias swing from 0.0 to 0.7 V and drain bias fixed to 0.5 V show that the on-state τ_S increases from 0.0563 to 0.093 pico second and the on-state f_T reduces from 8.106 to 5.0495 THz for L_u change from 0 to 5 nm.



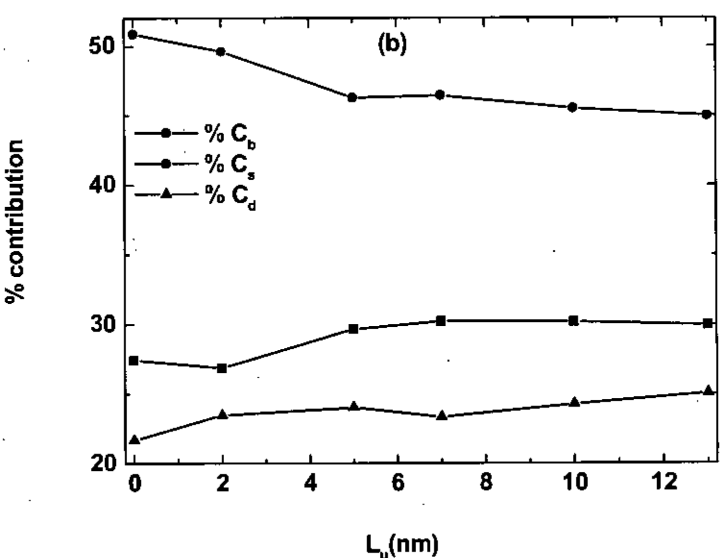


Figure 3.13: (a) On state gate capacitance C_g vs underlap L_u (b) Percentage contribution of different components of gate capacitance vs underlap L_u

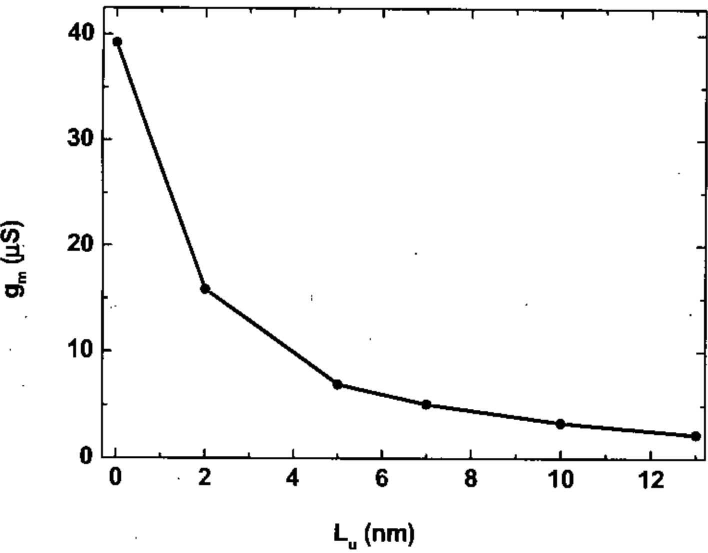
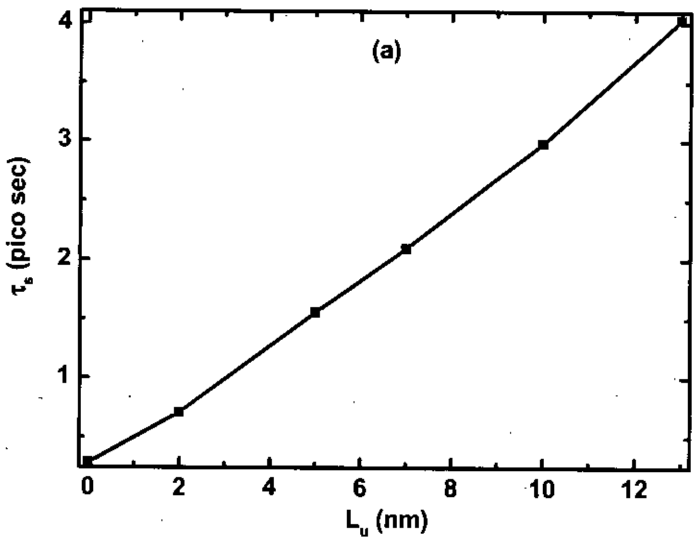


Figure 3.14: Transconductance vs underlap L_u

The simulated gate capacitance versus gate length and transconductance versus gate length are shown in Figure 3.16. From the figure we see that the gate capacitance increases and the transconductance decreases with increased gate length. As a result the intrinsic switching delay $\tau_S$increases and the unity current gain frequency f_T decreases with gate length. For the variation of gate length from 5 nm to 10 nm gate capacitance increases from 1.27 aF to 2.28 aF while the transconductance decreases from 99.3 μS to 64.2 μS. The intrinsic switching delay versus gate length and unity current gain frequency versus gate length are shown in Figure 3.17. From the figure wee see that both intrinsic switching delay and unity current gain frequency degrades with longer gate length. For the variation of gate length from 5 nm to 10 nm intrinsic switching delay rises from 0.056 pico second to 0.23 pico second and unity current gain frequency decreases from 10.53 THz to 4.4879 THz.



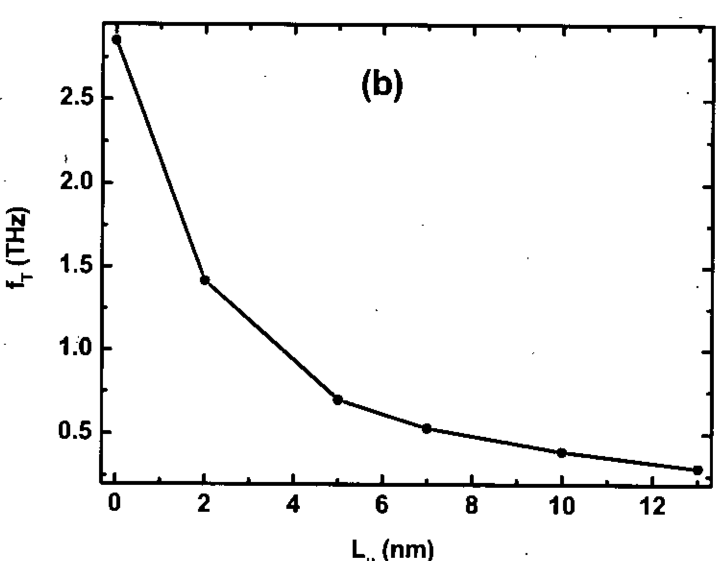


Figure 3.15: (a) On state intrinsic gate delay τ_S vs underlap length L_u (b) On state intrinsic cut-off frequency f_T vs underlap length L_u

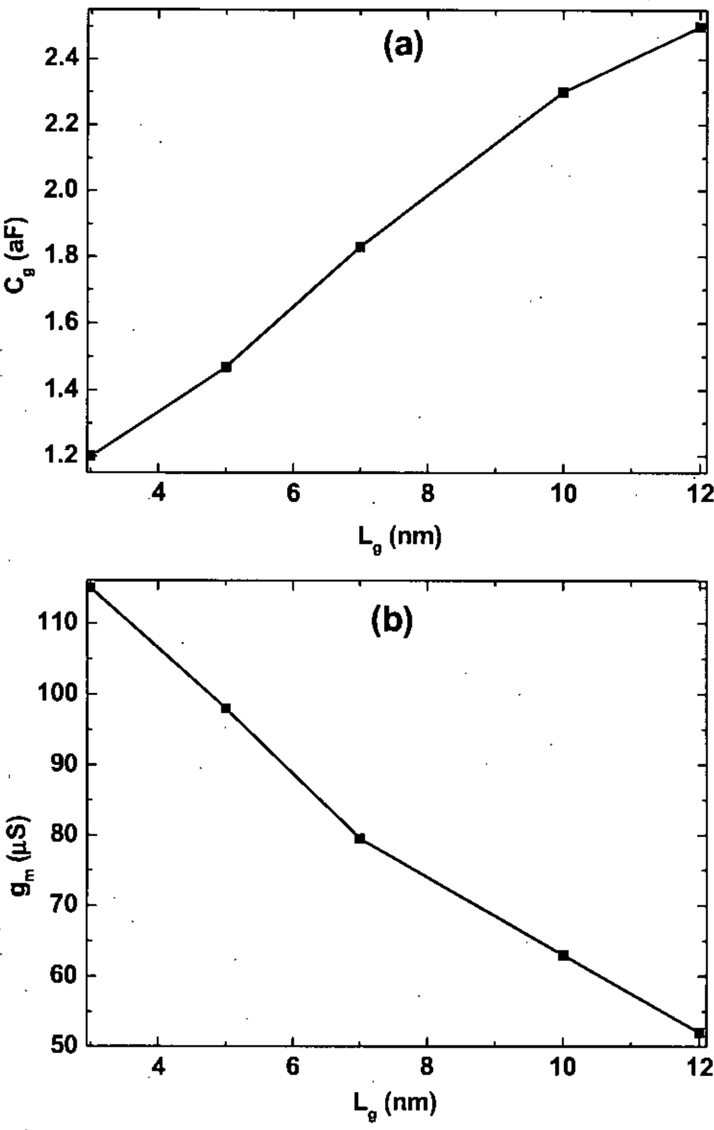


Figure 3.16: (a) Gate capacitance versus gate length (b) Transconductance versus gate length.

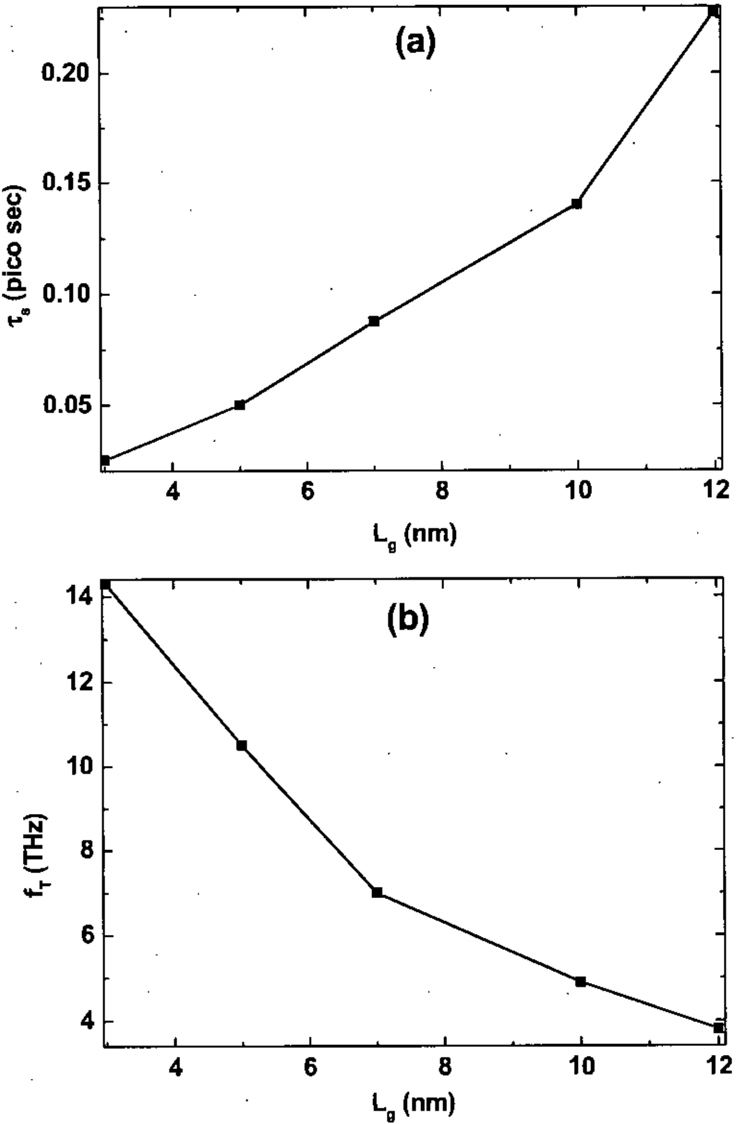


Figure 3.17: (a) Intrinsic switching delay versus gate length (b) Intrinsic cut-off frequency versus gate length.

Chapter 4

Conclusion

A three dimensional quantum simulation is performed for silicon nanowire on insulator transistors to see the effects of source-drain underlap on the device performance and to understand the physics of the effects. The underlap primarily affect the tunneling current and improves the short channel effects of the transistor at the cost of on current and the intrinsic switching performance. The effects of gate length have also been investigated and it is found that similar to underlap effects increase in gate length improves the performance of the device in the subthreshold region and degrades the device performance in the on state. Appropriate choice of bias range and gate metal work function, gate length combined with the source-drain underlap can improve the on-state current as well as the switching performance that can facilitate the optimal device design.

4.1 Summary

We developed a self-consistent 3-D Poisson-Schrodinger solver to simulate the effects of source drain underlap and its physics takin quantum-mechanical effects into account. We developed a the 3-D Poisson's equation using finite difference method (FDM) with non-uniform grid spacing which makes the solver computationally efficient and memory management becomes more tractable. The band gap of the silicon nanowire is calculated from the effective mass Schrodinger equation and found to be

1.38 eV for $5 \times 5nm^2$ cross section silicon nanowire. The final potential profile is obtained solving the self-consistent Poisson-Schrodinger solver repeatedly until the minimum criteria for convergence is achieved. once the convergence is achieved current is calculated using recursive Green's function algorithm.

We calculated various performance of the simulated device in the sub-threshold region such as off current, on-off current ratio, inverse subthreshold slope etc. and investigated the physics behind the phenomena. It is found that the both the on-off current ratio and the inverse sub-threshold slope improves with underlap. The physics behind it is modulation of channel barrier with the underlap. It is observed that with the increment of underlap the channel barrier height increases and therefore suppresses the off state current significantly. Increment of underlap length also results in reduction of on state current but this reduction is not as significant as the reduction of off state current. As a result the there is a very significant improvement in on-off current ratio with underlap.

We also investigated the performance metrics of the device such as transconductance, intrinsic gate delay and intrinsic cut-off frequency with underlap and also with gate bias. We also investigated the gate capacitance and contribution of its different components with underlap and also with gate bias. From the result it is observed that about 50 percent of the gate capacitance come from the fringing field capacitance. The gate capacitance of the device decreases with underlap so it is expected that the intrinsic gate delay will reduce and cut-off frequency will improve with underlap. But the transconductance and on current also reduces with underlap and dominates over the reduction of capacitance and as a consequence there is a increment in intrinsic gate delay and reduction in intrinsic cut-off frequency.

The gate capacitance of the device increases with the gate bias voltage and there-

fore the the intrinsic gate delay should increase and the intrinsic cut-off frequency should reduce. But the transconductance and current of the device increases drastically with gate bias and dominates over the increment of gate capacitance and therefore there is a decrement of intrinsic gate delay and increment in intrinsic cut-off frequency with underlap.

4.2 Suggestions for Further Work

Self-consistent solution is a very important tool for device simulation where quantum mechanical effects become important. We developed a model to simulate a top gate silicon nanowire on insulator transistor with highly doped source drain contact.With a very little change, this model can be used to simulate Schottky contact silicon nanowire transistor.

In recent literatures published in various scientific publications people are now paying attention to double gate, tri-gate and gate all around devices. With a very little change in our device description file our model can handle these kind of novel structures.

Our model is appropriate for simulating devices with nanowire cross section $\geq 3 \times 3\mu m^2$ because we used effective mass Schrodinger equation. For device dimension smaller than specified one the effective mass Schrodinger equation is no longer valid. In that case one must take atomistic approach for Hamiltonian formulism but the 3-D Poison's equation developed in this can still be used without any appreciable change.

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Appendix A

Value of parameters used

$q = 1.6 \times 10^{-19}$; electron charge (C)

$epsilono = 8.854 \times 10^{-21}$; permitivity of free space (F/nm)

$KB = 8.614 \times 10^{-5}$; Boltzmann constant (eV/K)

$h = 6.62 \times 10^{-34}$; Planck constant (J-sec)

$hbar = h/(2 * pi * q)$; reduced Planck constant (eV-sec)

$mo = 9.11 \times 10^{-31}$; rest mass of electron (Kg)

$TEMP = 300$; temperature (K)

$KT = KB * TEMP$; thermal energy (eV)

$Br = 0.0529$; Bohr radius (nm)

Appendix B

Flow Chart: Flow chart of the algorithm of self-consistent loop.