Improvement of Power Factor and Total Harmonic Distortion of Input Current for a Valley Fill Electronic Ballast

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Abstract

The thesis will focus on the power factor correction and harmonic reduction circuit for an electronic ballast of fluorescent lamp. At first different power factor correction techniques are investigated and compared. Among them the valley-fill (VF) passive power factor correction method is used to improve the power factor and THD. The basic VF circuit is studied in detail and it is modified with four different schemes and the effects of different circuit components are analyzed. The VF circuit is used because of its simplicity, high efficiency and less expensive. The modified VF circuit with better performance is proposed in this thesis. It is combined with a current fed resonant inverter as a power circuit, which provides isolation to the driver circuit without the use of any isolation devices. When the inverter is cascaded with the valley fill circuit, the input inductor inherits the boost inductor characteristics and allows the line current to achieve close to sinusoidal shape. As a result the total harmonic distortion reduced. Lastly the modified VF ballast with extended conduction angle is analyzed with three different configurations to have a suitable design which will enhance the performance. In this work, the best result is achieved where the power factor (PF) is 0.995, efficiency is 98.79 % and the THD is 9.83 %. The ORCAD PSPICE simulation results for each configuration are presented in the thesis to highlight the performance of the proposed circuit.

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List of Abbreviations

DC	-	Direct Current
AC	-	Alternating Current
EMI	-	Electromagnetic Interference
SSI	-	Single Stage Inverter
PF	-	Power Factor
PFC	-	Power factor Correction
THD	-	Total Harmonic Distortion
VF	-	Valley Fill
CCM	-	Continuous Conduction Mode
CRM	-	Critical Conduction Mode
DCM	-	Discontinuous Conduction Mode
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
RMS	-	Root Mean Square
CF	-	Crest Factor
HID	-	High Intensity Discharge

Chapter 1

Introduction

1.1 Introduction and Background

Modern lighting systems are based on the transformation of electrical energy into light energy. Nowadays, about 20 % of electrical energy produced in the world is consumed under a form of artificial illumination. In the artificial lighting devices field of research, the objectives are the continuous improvement of their performance, such as the light efficiency W/lm as well as the reliability, life service, cost of implementation, complexity, quality of the generated light, flexibility in the use for different applications, reduced size and weight, wide range of working temperature, power factor, total Harmonic distortion factor, electromagnetic compatibility criteria and EMI.

Once most people when think of lighting and lamps, they think of the incandescent light bulb developed by Thomas Edison and other inventors. In 1857, the French physicist Alexandre E. Becquerel who had investigated the phenomena of fluorescence and phosphorescence theorized about the building of fluorescent tubes similar to those made today. American, Peter Cooper Hewitt (1861-1921) patented the first mercury vapor lamp in 1901. The low pressure mercury arc lamp of peter Cooper Hewitt is the very first prototype of today's modern fluorescent lights. A fluorescent light is a type of electric lamp that excites mercury vapor to create luminescence.

Fluorescent lamps have become an important and popular lighting source. They provide a large percentage of today's lighting needs, even though these are considerable larger than incandescent lamps and require a large fixture. Even with these disadvantages, fluorescent lamps are preferred due to their higher light output (lumens) per electrical input power (watts) and long lifetime. This ratio (lm/W) is known as the luminous efficacy and helps to describe the efficiency of the energy conversion that takes place inside the lamp. Fluorescent lamp and all other gaseous discharge lamps exhibit negative resistance characteristics in the desired regions of operation. This produces an unstable condition if a tube is connected across a voltage source large enough to cause ionization. Therefore a current limiting device called ballast is needed. The ballast triggers the lamp and controls voltage and current corresponding to its power.

In recent years, there has been a growing trend for the consumers to use electronic ballasts. Because electronic ballast are technically much superior to their

electromagnetic counterparts. When the electronic ballasts are properly designed, they can deliver good input side performance as well as output side performance such as lighter weight and volume, flicker free operation, higher luminous efficiency, audible noise absence etc. as compared with electromagnetic ballast that is bulky, heavy and efficient with low power factor. So, numerous works have been done on the design and development of this circuit [1-3].

However electronic ballast without power factor correction uses electrolytic capacitors to filter out the input rectifier voltage. It results low power factor (PF<0.6) and a high input current total harmonic distortion (THD<130%) regardless of presenting good results of lamp current crest factor [4-5]. Power factor is an important consideration for the energy efficiency. Power factor is the ratio of the real power to the apparent power. Only the real power is capable of doing work but the apparent power determines the amount of current that flows into the load, for a given load voltage. Hence, for a low power factor the current increases and this higher current increase the energy lost in the distribution system and require larger equipment. On the other hand, high harmonic contents adversely affect other users. This creates the need for some kind of power conditioning as named “Power Factor Correction”. In electronic ballast power factor correction and input current wave shaping may be achieved by “passive” or “active” PFC methods [6].

In active PFC technique, usually some kinds of switching scheme is employed to shape the input current thereby reducing the size of filter or eliminating completely the filter at the input side. The most used active method is the boost converter which works in the discontinuous conduction mode. However this circuit increases the voltage stress to the main device and it is lossy, less efficient and not cost-effective as it operates with high peak triangular shape current with additional power devices, passive components and control circuit to work with variable load and no load [7]. Because of this the passive PFC methods are preferred. In passive PFC method, usually L-C filters are used at the input side. Since these filters are to operate at the line frequency, the size and weight of the converter rises. So among these, Valley-fill filter and its modifications are the most used. They do not require any control circuit for PFC stage and is able to achieve PF of more than 95 % and it also have high efficiency.

1.2 Literature Review

The first topologies proposed for electronic ballasts meeting this regulation were based on two-stage arrangement [8]. These solutions present some disadvantages of high cost due to large number of components and duplication of control circuitry, low efficiency

especially for the low power ratings, due to two stage configurations. Then an intensive work is being done in order to obtain low cost and high efficiency topologies to implement electronic ballast. In search of these several reduced component count topologies has been previously proposed [9-10]. One of the ways to reduce cost in high power factor electronic ballasts is the integration of two stages, a dc-to-dc converter and a resonant inverter, in a single stage by sharing more switches [11-13]. This approach requires only one energy conversion process and it is more cost effective than two stage approach. It also saves a control circuit for the PFC stage and increase the overall efficiency.

The boost preregulator, when operated in the discontinuous conduction mode, is a popular choice in SSI designs as the input inductor allows easy input current shaping and it requires only one control loop for the PFC stage [14]. However, it has the disadvantage of suffering high voltage stress across the dc-link capacitor and the switches. Hence, it is only suitable for low-input line voltage applications. The shortcomings seen in the boost SSI can be eliminated by replacing the boost converter with a buck preregulator [15]. In this way, low voltage switches can be used to reduce the overall system cost. However, the buck converter only allows the input current to circulate when the line voltage is higher than the output voltage. As a result, discontinuity in the line current lowers the power factor (PF) and increases the current total harmonic distortion (THD). In general, SSI ballasts always require a complicated control circuit to regulate both the dc-link voltage and output current [15]. The shared switch also needs to handle both the PFC inductor current and the resonant current, which increases the conduction loss of the switch.

The passive valley fill ballast circuits are more cost effective when compared to SSI topologies. However, the VF circuit generates a DC voltage that is of magnitude 50% of the peak line voltage during the line current discontinuity period at the input of the resonant inverter. As a result the crest factor increases and lifetime reduces [16-17]. By modifying the VF ballast better performance can be obtained compared to active methods.

1.3 Objective and Methodology

The objectives of this work is to overcome the problem of low power factor and input current total harmonic distortion of an electronic ballast of fluorescent lamp without PFC using valley-fill circuit. In using the basic valley-fill circuit there are discontinuity in the input current and charging spike persist which causes harmonic distortion. So this work proposes a modified VF electronic ballast circuit which will enhance the performance. At first different valley fill electronic ballast will be studied in details to

evaluate the effect of different circuit components on the power factor and THD of input current. The VF circuit will be modified and different alternate design will be proposed to improve the power factor and reduce THD. ORCAD PSPICE 9.2 will be used to perform simulation for the proposed designs. Provision will be taken to remove the charging spike in the VF circuit which is a main contributor of current harmonics. The circuit with the best power factor and THD value will be chosen for detail analysis.

1.4 Organization of this thesis

This thesis report is composed of five chapters. Chapter 1 introduces the research background on power factor correction of an electronic ballast of a fluorescent lamp, reviews recent advances of topologies and states the objective of this thesis. Chapter 2 presents the present situation of power quality, need for power factor correction, different methods of power factor correction and their comparison. Chapter 3 illustrates the principle operation of basic Valley-fill circuit, detail analysis on the effect of different circuit components in the improvement of PF and input current THD. Chapter 4 proposes a modified VF ballast circuit and its operation, comparative study on proposed modified VF ballast circuit with the three configurations, suitable design for the modified VF ballast circuit. Computer simulation verifications are presented. Chapter 5 presents the Practical Implementation of the proposed VF ballast circuit. Lastly, Chapter 6 summarizes conclusion and suggests future work.

Chapter 2

Power Factor Correction

2.1 Introduction

Power quality standards are being imposed worldwide in order to maximize the efficiency of the existing total generation capacity. Adding additional generating capacity is increasingly difficult and expensive because of environmental constraints. But with the increase of consumer electronics the power quality becomes poor. One very important aspect of improving quality of power is the control of power factor. Power factor is an important consideration for the energy efficiency of individual machines or entire plants. Low power factor means poor electrical efficiency. The lower the power factor, the higher the reactive power drawn from the supply. This is because of the use of rectification of the AC input and the use of a bulk capacitor directly after the diode bridge rectifier which also increases the harmonic contents. Reducing the input current harmonics to meet the agency standards implies improvement of power factor as well. For this reason the publications reported in this area have used 'Power factor correction methods' and 'Harmonic reduction methods' almost inter changeable. Several techniques for PFC and harmonic reduction have been reported and a few of them have achieved the acceptance over the others.

2.2.1 Power Factor (PF)

Power factor is defined as the ratio of the real power (P) to the apparent power (S) drawn by a load from an AC supply.

$$PF = \frac{P}{S} \tag{2.1}$$

Where the real power is the average, over a cycle, of the instantaneous product of current and voltage, and the apparent power is the product of the rms value of current times the rms value of the voltage. If both the current and voltage are sinusoidal and in phase then the PF is 1.0. If both are sinusoidal but are not in phase then the power factor is the cosine of the phase angle. However, in reality always a non-sinusoidal current is drawn by most of the power supplies. Assuming an ideal sinusoidal input voltage source but the line current is non-sinusoidal; the power factor can be expressed as the product of the distortion power factor and the displacement power factor, as given in equation (2.2). The distortion power factor K_d is the ratio of the fundamental root-mean-square (RMS) current (I_{1rms}) to the total RMS current (I_{rms}). The displacement power factor K_θ is the cosine of the displacement angle between the fundamental input current and the input voltage.

$$PF = K_d K_\theta \tag{2.2}$$

The distortion power factor K_d is given by the following equation (2.3)

$$K_d = I_{1rms} / I_{rms} \quad (2.3)$$

The displacement power factor K_θ is given by the following equation (2.4)

$$K_\theta = \cos\theta \quad (2.4)$$

The displacement power factor comes due to the phase dispalcemet between the current and voltage waveforms. This displacement factor K_θ can be made unity with a capacitor or inductor but making the distortion power factor K_d unity is more difficult. The distortion power factor K_d describes the harmonic content of the current with respect to the fundamental. Hence, the power factor depends on both harmonic content and displacement factor.

2.2.2 Total Harmonic Distortion (THD)

The Total Harmonic Distortion or THD of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

The total harmonic distortion factor is defined as

$$THD\ (\%) = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2}}{I_{1rms}} \quad (2.5)$$

Hence the relation between K_d and THD is

$$THD\ (\%) = 100 \times \sqrt{\frac{1}{K_d^2} - 1} \quad (2.6)$$

The distortion power factor K_d is also given by the following equation.

$$K_d = \frac{1}{\sqrt{1+\left(\frac{THD(\%)}{100}\right)^2}} \quad (2.7)$$

2.2.3 Relation between Power Factor and Total Harmonic Distortion

Though there is no direct correlation between Power factor and Total Harmonic Distortion, but the two equations (2.2) and (2.7) link them in some way.

Equation (2.2) describes Power Factor, PF = K_d K_θ

Therefore, when the fundamental component of the input current is in phase with the input voltage then K_θ = 1. Then we have

$$PF = K_d \times 1 = K_d \quad (2.8)$$

Substituting the value of equation (2.7) in equation (2.8), we have

$$PF = \frac{1}{\sqrt{1+\left(\frac{THD(\%)}{100}\right)^2}} \quad (2.9)$$

As illustrated, a perfectly sinusoidal current could also have a poor power factor if its phase was not in line with the voltage. From equation (2.9) it is apparent that a 10 % THD corresponds to a Power Factor of approximately 0.995.

Thus it is clear that specifying limits for each of the harmonics will do a better job of controlling the "pollution" of the input current, both from the standpoint of minimizing the current and reducing interference with other equipment. So, while the process of shaping this input current is commonly called "power factor correction", the measure of its effectiveness towards complying with international regulations is the amount of reduction in the harmonic content of the input current.

2.3 Power Factor Correction (PFC)

Power factor correction is a modern concept which deals with increasing the degraded power factor of a power system by use of external equipments. The objective of this described in plain words is to make the input to a power supply appear as a simple resistor. As long as the ratio between the voltage and current is constant the input will be resistive and the power factor will be 1.0. When the ration deviates from a constant the input will contain phase displacement, harmonic distortion or both and either of them will degrade the power factor.

In simple words, Power factor correction (PFC) is a technique of counteracting the undesirable effects of electrical loads that create a power factor (PF) that is less than 1.0.

2.4 Need for Power Factor Correction

The power factor gets lowered as the real power decreases in comparison to the apparent power. This becomes the case when more reactive power is drawn. This may result from

increase in the amount of inductive loads which include- Transformer, induction motor, induction generators (wind mill generators), high intensity discharge (HID) lighting etc. However in such case the displacement power factor is affected and that in turn affects the power factor.

On the other hand, with improvement in semiconductor devices field, the size and weight of control circuits are on a constant decrease. This has also positively affected their performance and functionality and thus power electronic converters have become increasingly popular in industrial, commercial and residential applications. As a result with most electronic equipment being connected to the electricity distribution network, the non-sinusoidal input current drawn by this equipment due to input line rectification which generates current harmonics and causes severe problems. These include increased magnitudes of neutral currents in three-phase systems, overheating of transformers and induction motors, additional losses and dielectric stresses in capacitors and cables and noise emissions n many products and bringing about Early failure of fuses and other safety components. This creates the need for some kind of power conditioning. Thus, the need to limit harmonic content of line currents drawn by electronic equipment connected to the electricity distribution networks, results in the need for Power factor Correction-PFC.

Power factor Correction (PFC) can be classified into two types:

- Active Power Factor Correction
- Passive Power Factor Correction

2.5 Active Power Factor Correction

An active power factor correction is a power electronic system which controls the amount of power drawn by a load and obtains a power factor as close as possible to unity. In most applications, the input current is controlled by this active PFC design in order to make the current waveform proportional to the mains voltage. A combination of some active switches and reactive elements are used in order to increase the effectiveness of the line current shaping and to obtain controllable output voltage [24].

According to the switching frequency the active power factor correction is again divided into two classes.

1. **Low frequency active PFC**

   Switching takes place at low-order harmonics of the line frequency and it is synchronized with the line voltage.

2. **High frequency active PFC**

   The switching frequency is much higher than the line frequency.

2.6 Low frequency active PFC

2.6.1 Phase controlled rectifier with dc-side inductor

The phase controlled rectifier and its control signals are shown in Fig. 2.1(a) and Fig. 2.1(b). It is similar to the rectifier circuit with a DC-side inductor except the diodes are replaced with thyristors. Near unity distortion factor K_d or displacement factor K_θ can be obtained by this method depending on the inductance L_d and the firing angle α, [18]. However, the overall power factor is always less than 0.8. In order to obtain a lagging power factor, suitable value of the inductance L_d and firing angle α are chosen to maximize k_d [19]. An additional input capacitor C_a compensates this lagging power factor even though it increases line current harmonics.

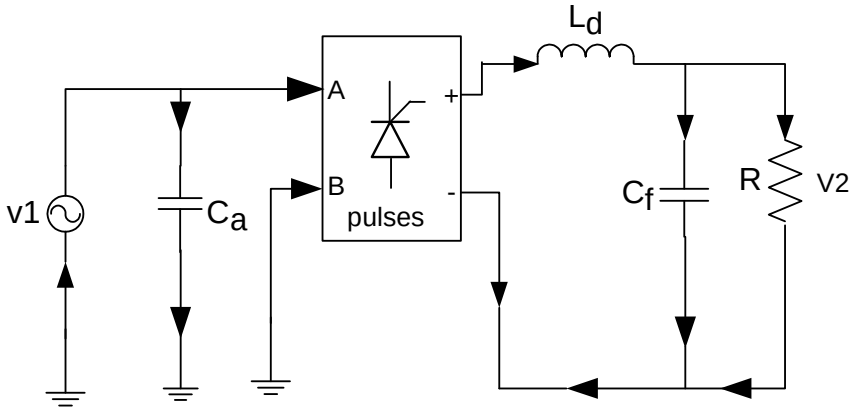

Fig 2.1 (a): Phase controlled rectifier.

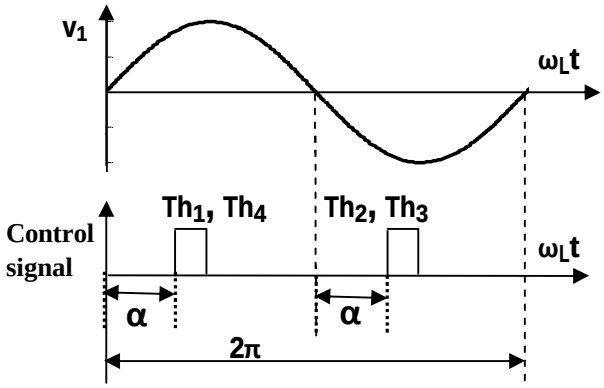

Fig 2.1 (b): Control signal.

This solution offers controllable output voltage. It is simple and reliable but it has some disadvantages. The output voltage regulation is low and it still requires a relatively large inductance L_a.

2.6.2 Low frequency switching boost converter

The low frequency switching boost converter is shown in Fig. 2.2(a). The conduction interval of the rectifier diodes extends by keeping the active switch on for the duration T_{on}, as illustrated in Fig. 2.2(b). At low switching frequency, in order to improve the shape of the line current, it is also possible to have switching per half line-cycle [18]. Nevertheless, the line current has considerable ripple content.

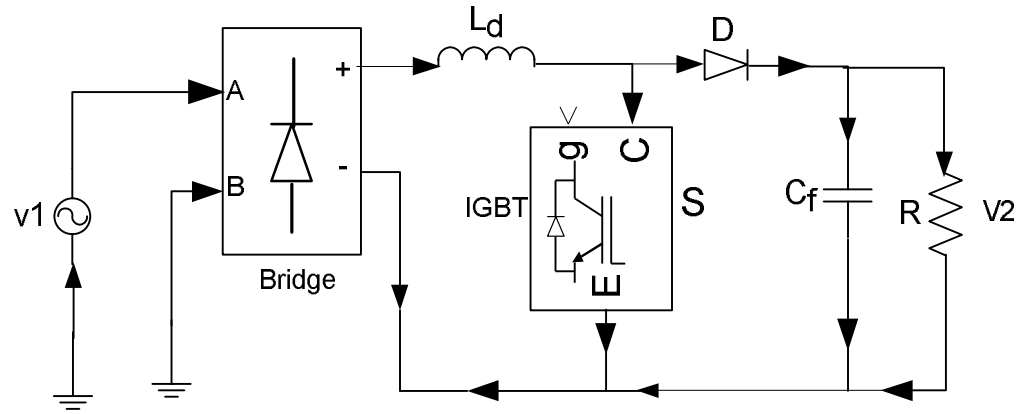

Fig. 2.2(a): Low frequency switching boost converter.

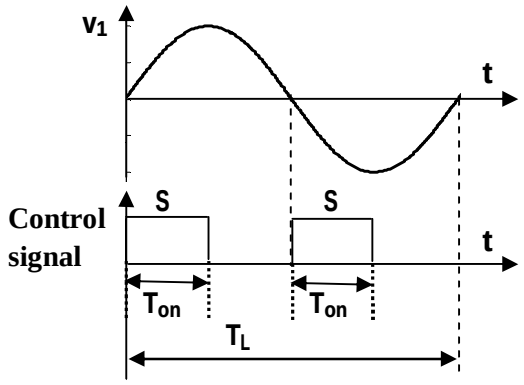

Fig. 2.2(b): One commutation per half line-cycle.

2.6.3 Low frequency switching buck converter

The low frequency switching buck converter is shown in Fig. 2.3(a). Theoretically, for a near infinity inductance L_a, the inductor current I is constant. The switch is turned on for the time duration T_{on} and the on-time interval are symmetrical with respect to the zero crossings of the line voltage as illustrated in Fig. 2.3(b). In this method the power factor

depends on the firing instance and duty cycle of the active switch . Multiple switching per line-cycle can be used to have lower harmonic contents of the line current. However, the required inductance L_a is large and impractical [20].

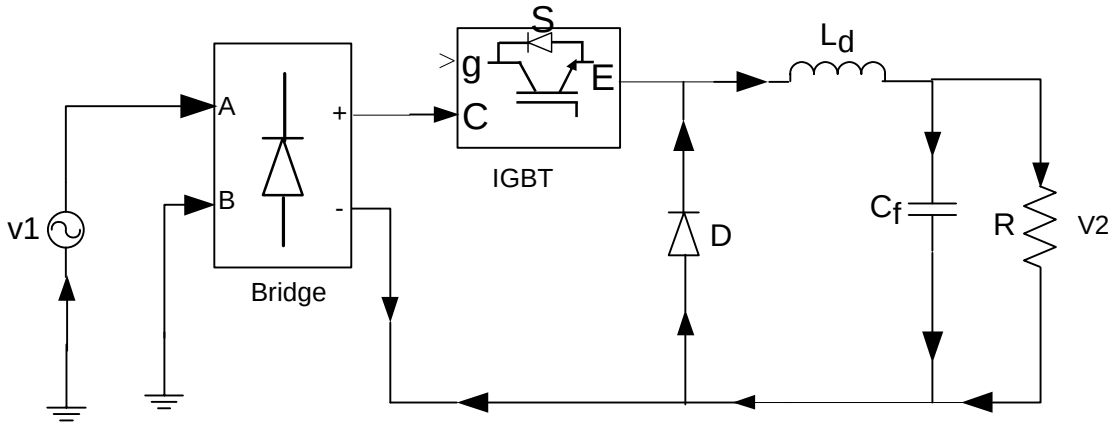

Fig. 2.3(a): Low frequency switching buck converter.

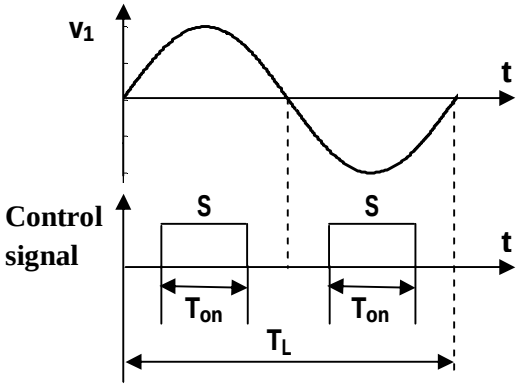

Fig. 2.3(b): One commutation per half line-cycle.

Low-frequency switching PFC offers the possibility to control the output voltage in certain limits. But the reactive elements are large and the regulation of the output voltage is slow.

2.7 High Frequency Active PFC

The high frequency active PFC circuit can be realized by placing a Buck or a Boost or a Buck-Boost converter in between the bridge rectifier and the filter capacitor of a conventional rectifier filter circuit and operating it by a suitable control method that would shape the input current. For all converter topologies, the switching frequency is

much higher than the line frequency, the output voltage ripple is twice the line-frequency and the output voltage is usually regulated.
The converters can operate in Continuous Inductor Current Mode - CICM, where the inductor current never reaches to zero during one switching cycle or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle.

2.7.1 Buck Converter based Active PFC

A Buck converter is shown in Fig. 2.4 (a). It steps down the input voltage. As a result an output voltage V_2 lower than the input voltage V_1 can be obtained. However, since the converter can operate only when the instantaneous input voltage v_1 is higher than the output voltage V_2, there is no current flow from the AC input during $0 \leq \omega_L \leq \alpha$ and during $\pi - \alpha \leq \omega_L \leq \pi$. Hence, the line current of a power factor correction based on Buck converter has crossover distortions, as illustrated in Fig. 2.4(b). Moreover, even if the inductor current is continuous, the input switching current of the converter is discontinuous as the high frequency switch S interrupts the input current during every switching cycle. Thus, the input current has significant high-frequency components that increase EMI and filtering requirements.

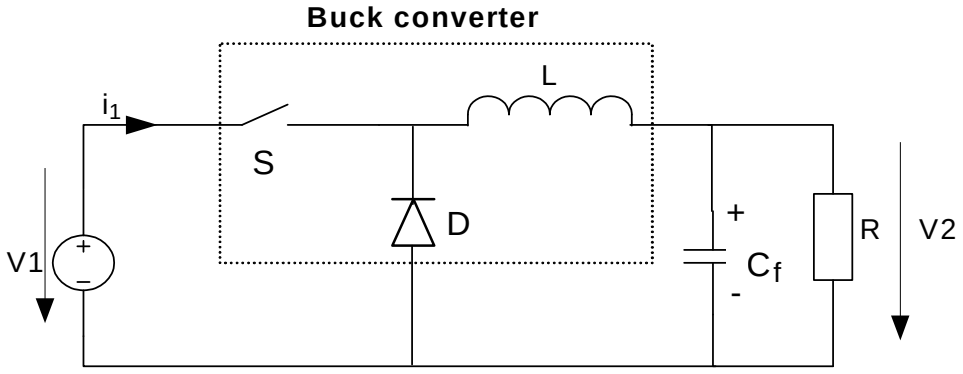

Fig. 2.4(a): Buck converter based high frequency active PFC.

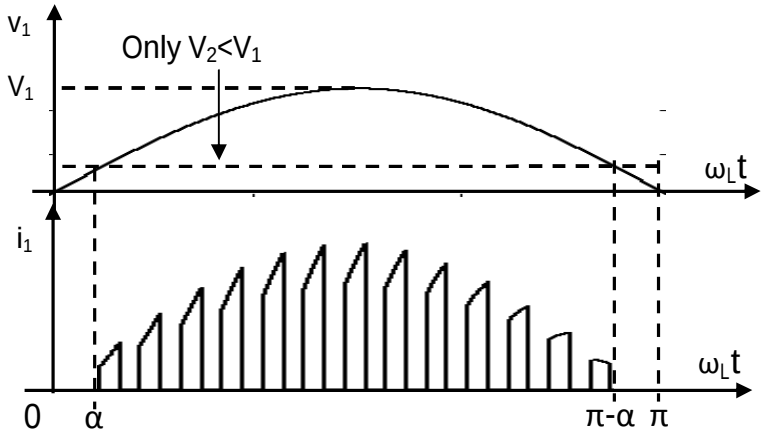

Fig. 2.4(b): Waveforms of Buck converter based high frequency active PFC.

2.7.2 Boost converter based Active PFC

One of the most common topology for power factor correction is the Boost converter. It can operate in two modes – continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The Boost converter is shown in Fig. 2.5(a). It has a step up conversion ratio for which the output voltage V_2 is always higher than the input voltage V_1. Since the converter can operate throughout the line-cycle, the input current does not have crossover distortion. The input current is continuous as illustrated in Fig. 2.5(b). Hence, an input current with reduced high-frequency content can be obtained when operating in CCM mode.

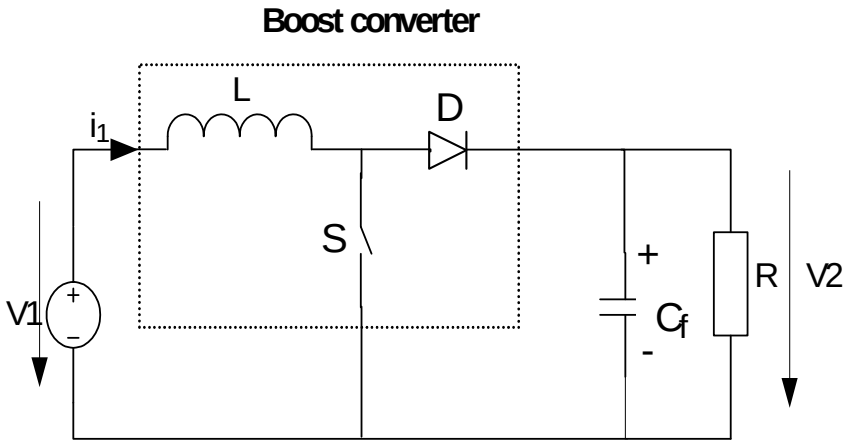

Fig. 2.5(a): Boost converter based high frequency active PFC.

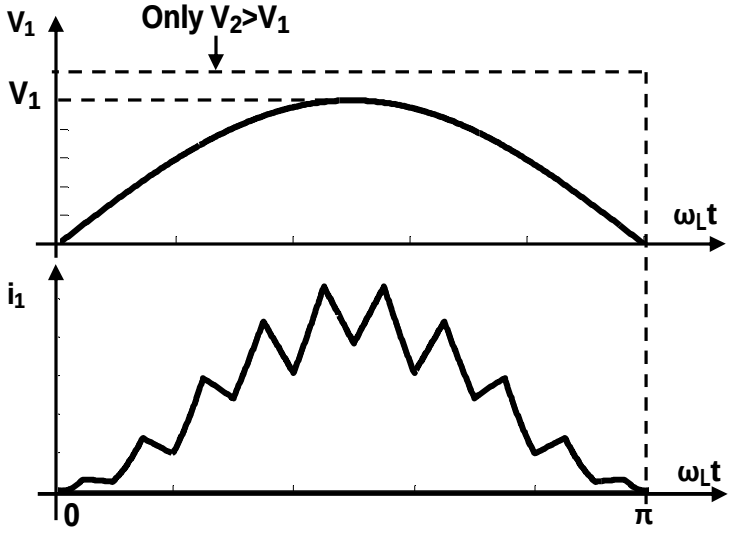

Fig. 2.5(b): Waveforms of Boost converter based Active PFC.

In the above converter the current in the inductor can be forced by the control scheme can to be either continuous or discontinuous. The DCM converter operates at fixed frequency and has switching current discontinuities in comparison to the CCM or CRM techniques. Due to this large peak currents and EMI associated with DCM converter, it is rarely or never used. Transition mode forces the inductor current to operate just at the border of CCM and DCM. The current scheme is also different and affects the component power loss and filtering requirements. The peak current in the CRM boost converter is twice the amplitude of the CCM boost converter leading to higher conduction losses [22]. The peak-to-peak ripple is twice the average current, which affects MOSFET switching losses and AC losses in the boost inductor.

2.7.3 Buck-Boost converter based Active PFC

The Buck-Boost converter is shown in Fig. 2.6(a). It can operate either as step-up or step down converter. This means that the output voltage V_2 can be higher or lower than the amplitude of the input voltage V_1. Operation is possible throughout the line-cycle and a sinusoidal line current can be obtained. However the output voltage is inverted, which translates into higher voltage stress for the switch. Moreover, similar to the Buck converter the input current is discontinuous with significant high frequency contents as illustrated in Fig. 2.6(b). Thus the input current has significant high frequency components that increase EMI and filtering requirements [21].

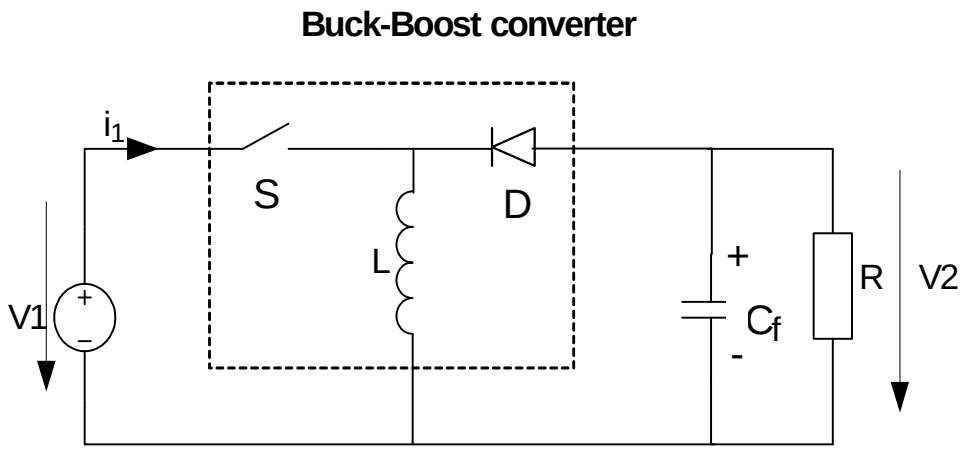

Fig. 2.6(a): Buck-Boost converter based high frequency Active PFC.

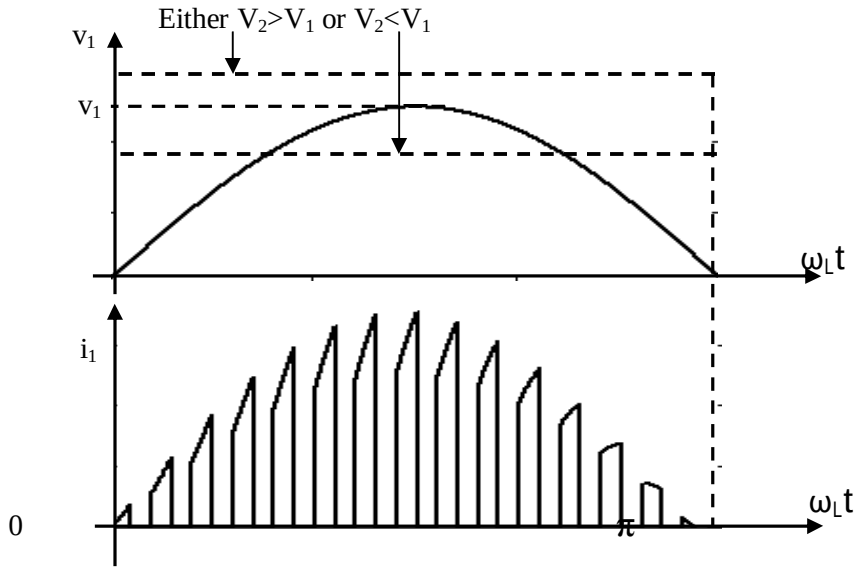

Fig. 2.6(b): Waveforms of Buck-Boost converter based high frequency Active PFC.

2.8 Passive Power Factor Correction

In passive PFC circuit passive components are used in conjunction with the diode bridge rectifier to improve the shape of the input current i.e. reduce the harmonic contents and improve the power factor. Various combinations of these passive components in different circuit locations give rise to many possible schemes. To maintain the flow of current, voltage doubler is inserted to feed the valley fill circuit. The commonly used schemes are explained in the following sections.

2.8.1 Passive PFC with Inductor in the AC side

One of the simplest methods is to add an inductor on the AC side of the diode bridge in series with the line voltage as shown in Fig. 2.7 in order to improve the power factor with the reduction in the input current harmonics. The maximum power factor that can be obtained is about 0.82.

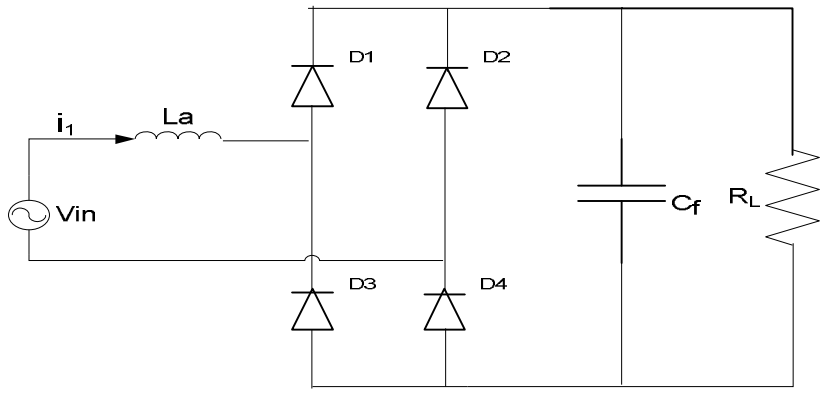

Fig. 2.7: Passive PFC in addition to AC side inductor (La = 20mH, C_f = 100uF, R_L = 50ohm).

The simulated input current, total harmonic distortion and PF are shown in Fig. 2.8(a), 2.8(b) and 2.8(c) where La = 20mH, C_f = 100uF and R_L = 50ohm.

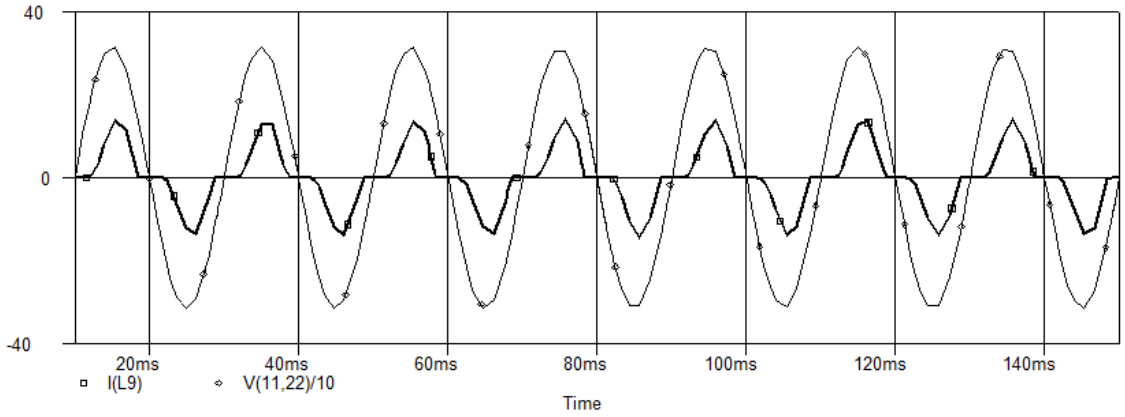

Fig. 2.8(a): Simulated input line current and input voltage.

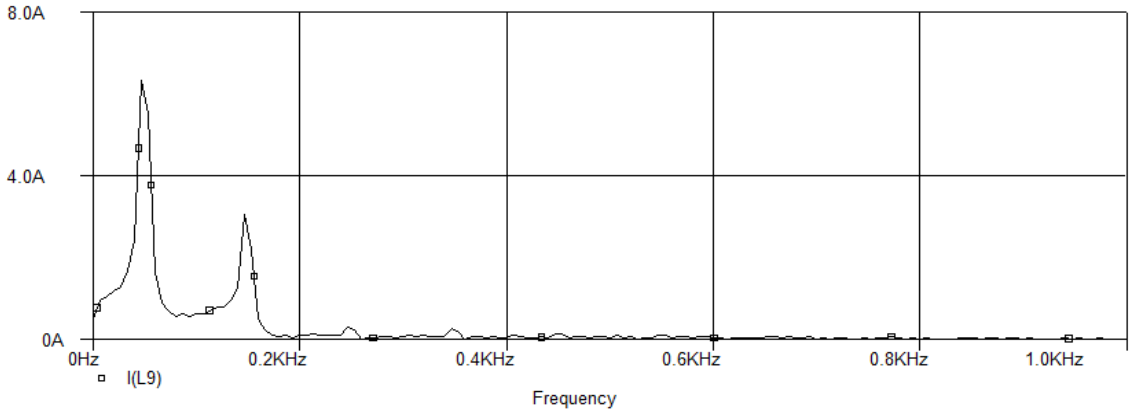

Fig. 2.8(b): Simulated line current Total Harmonic Distortion.

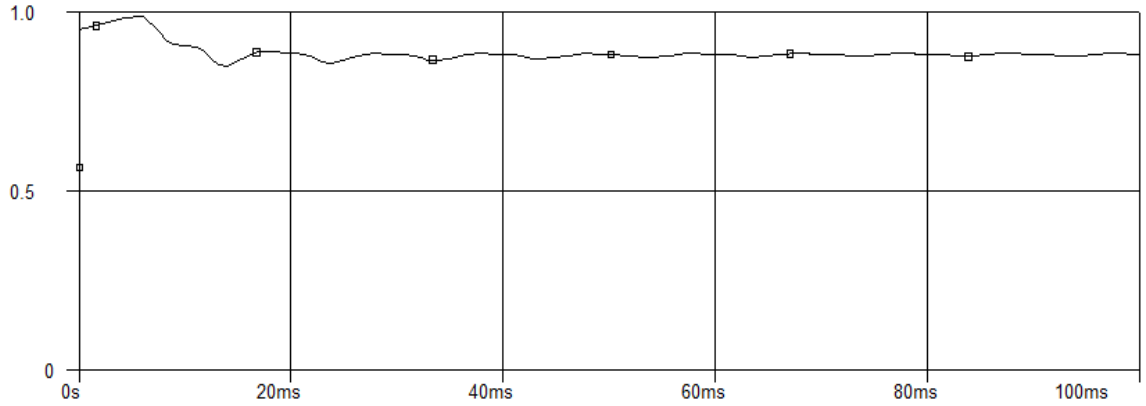

Fig. 2.8(c): PF of the passive PFC with AC side inductor.

Simulated input current, Total Harmonic Distortion are shown in Fig. 2.9(a) and Fig. 2.9(b) where La = 50 mH, C_f = 220uF and RL

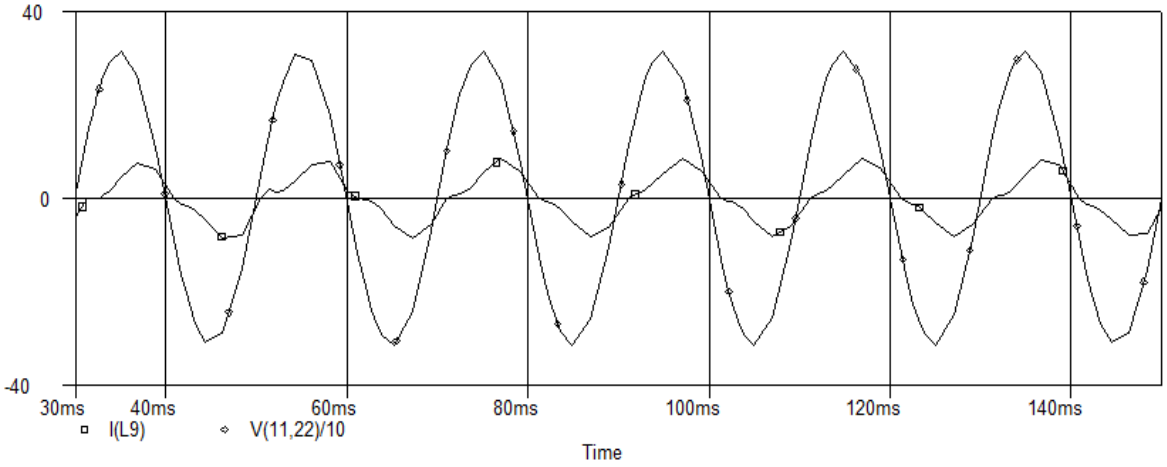

Fig. 2.9(a): Simulated input current and input voltage.

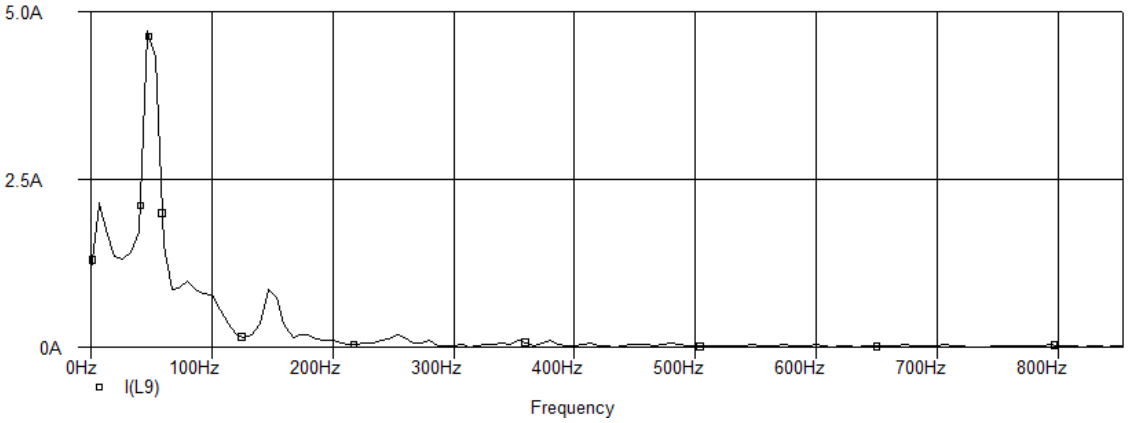

Fig. 2.9(b): Simulated line current Total Harmonic distortion.

2.8.2 Passive PFC with Inductor in the DC side

The inductor can also be placed in the DC side as shown in Fig. 2.10. If the inductor current is continuous for a given load current, the power factor can be as high as 0.9 but this requires relatively large inductance. When a lower inductance value is used the inductor current becomes discontinuous, the input current wave shape becomes similar to the wave shapes found in the previous section and the PF diorites.

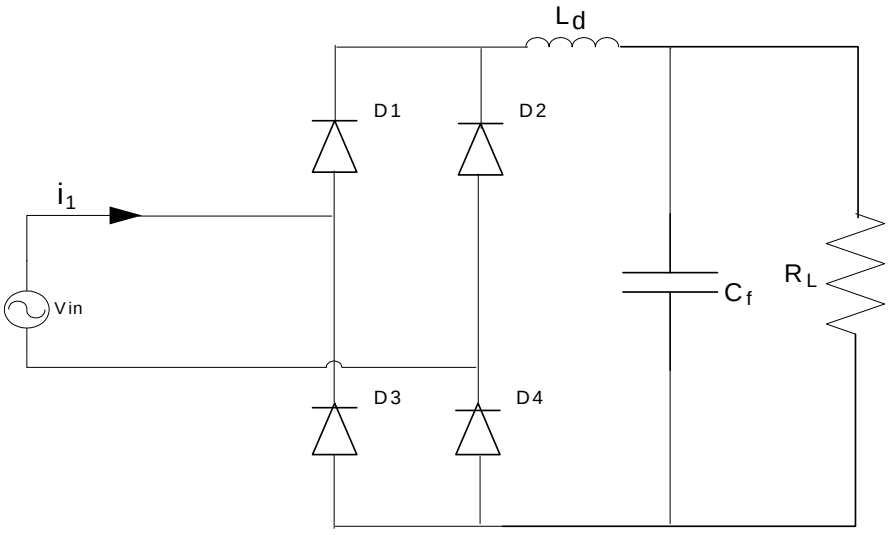

Fig. 2.10: Passive PFC with inductor in DC side.

The circuit is simulated for two configurations. Once with L_d = 250mH, C_f = 100uF and R_L = 50 ohm and then L_d = 25mH, C_f = 100uF and R_L = 50 ohm. The respective waveforms are shown in Fig. 2.11(a),(b),(c) and in Fig. 2.12(a), (b), (c).

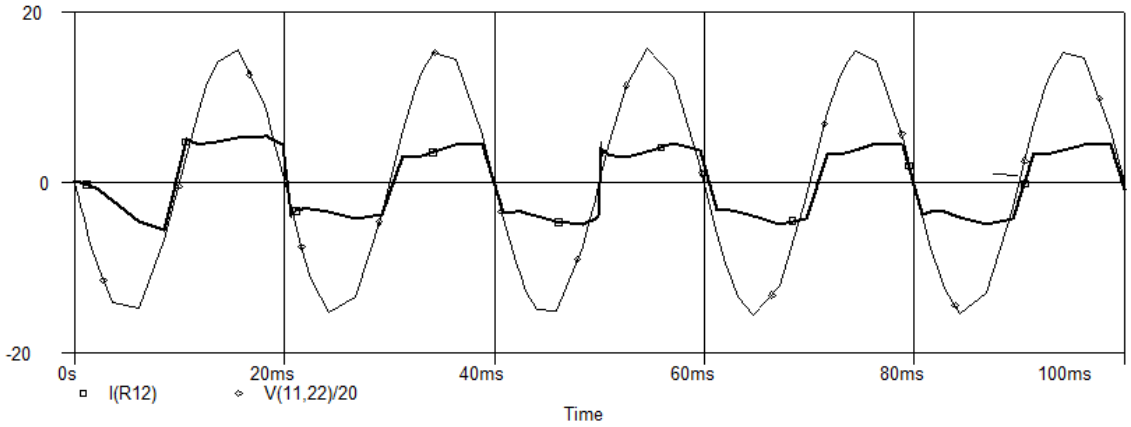

Fig. 2.11(a): Simulated input current and input voltage.

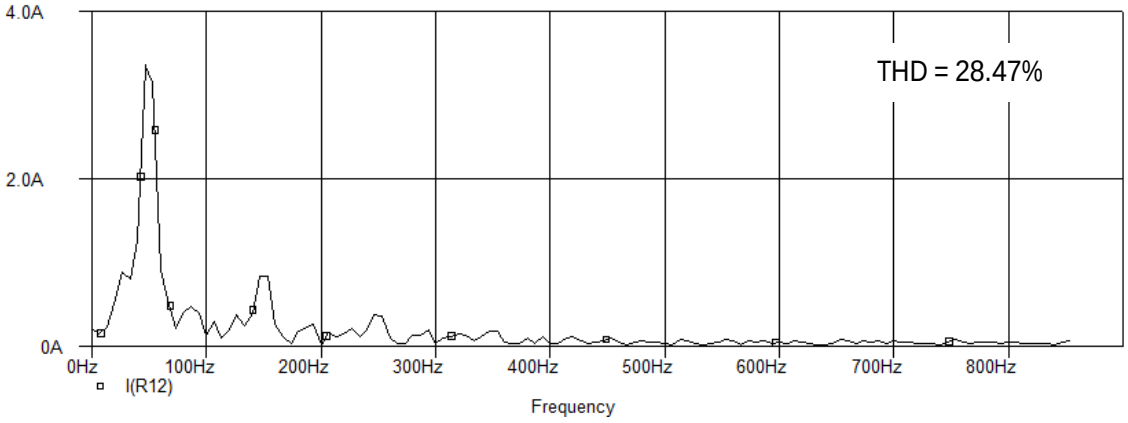

Fig. 2.11(b): Simulated line current Total Harmonic Distortion.

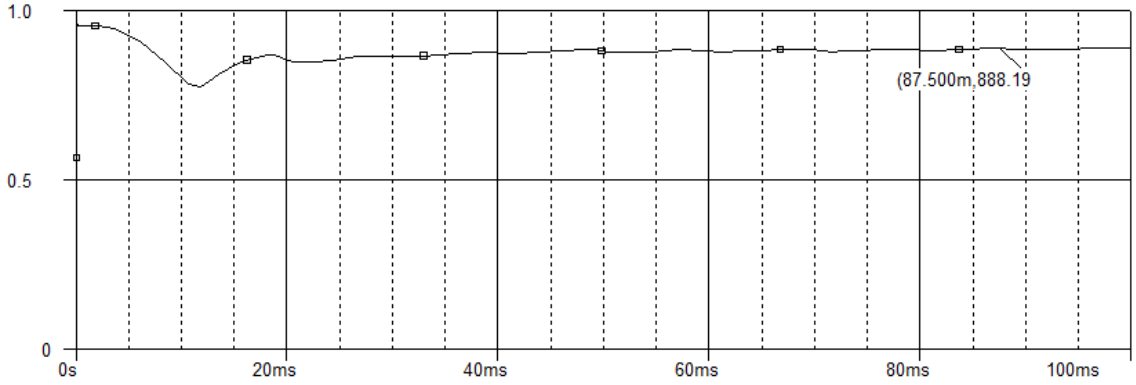

Fig. 2.11 (c): Simulated PF

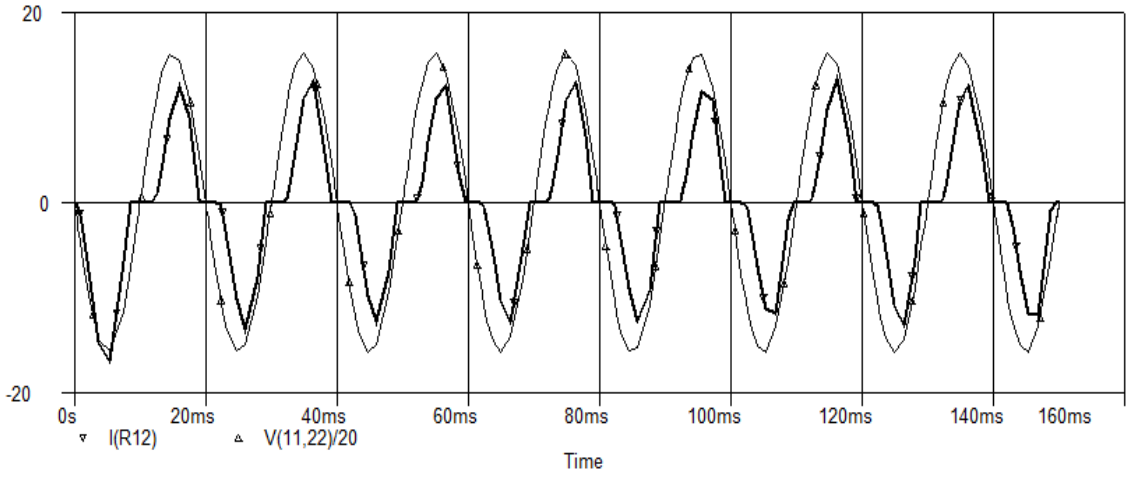

Fig. 2.12(a): Simulated input current and voltage for L_d = 25mH.

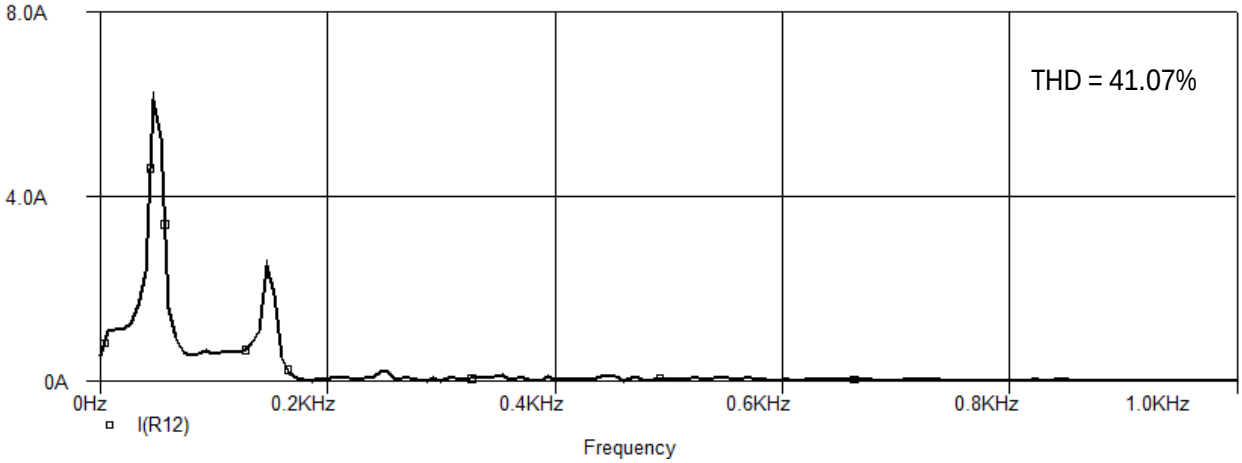

Fig. 2.12(b): Simulated line current Total Harmonic Distortion for L_d = 25mH.

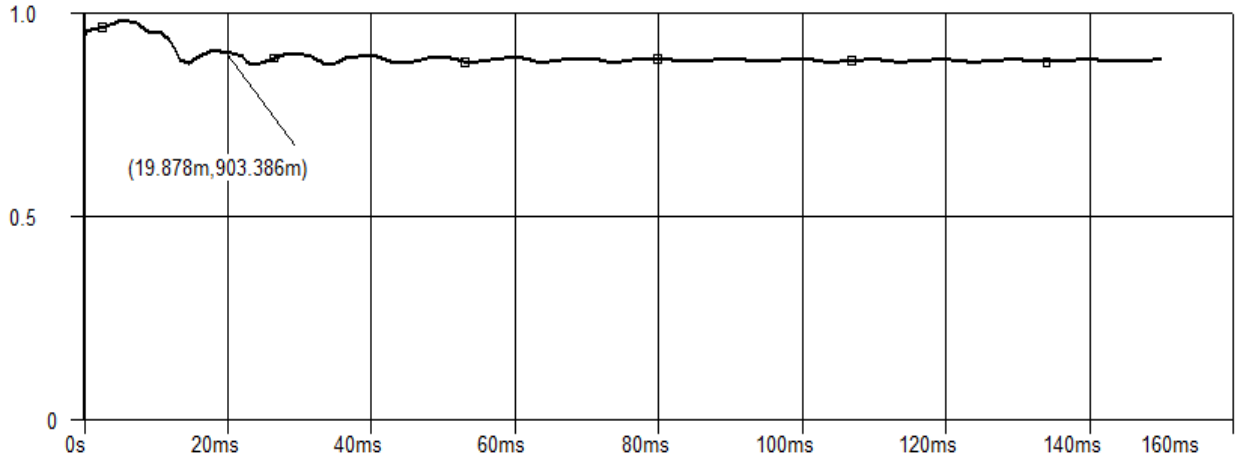

Fig. 2.12(c): Simulated PF for L_d = 25mH.

2.8.3 Passive PFC with series-resonant band-pass and series-resonant band-stop filter

There are also several solutions based on resonant networks which are used to attenuate harmonics and improve the shape of input current. For example, a band- pass filter of series resonant type, tuned at line frequency and a band-stop filter of parallel resonant type, tuned at the third harmonic are introduced in-between the AC line and the load [23]. The circuit diagrams are shown in Fig. 2.13 and Fig. 2.14.

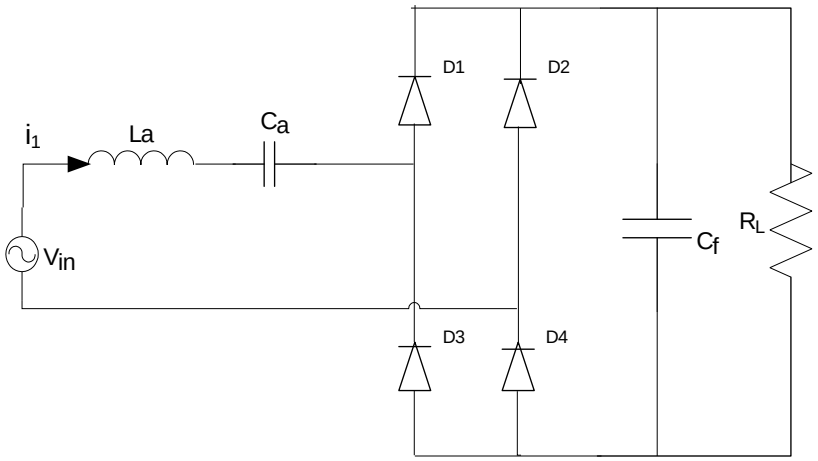

Fig. 2.13: Passive PFC with band-pass filter of series resonant type.

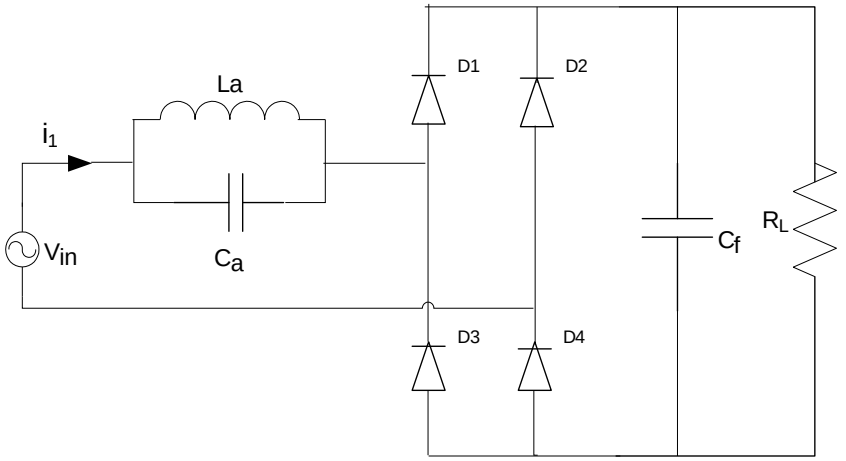

Fig. 2.14: Passive PFC with band-stop filter of parallel resonant type.

Using series resonant band-pass filter, unity power factor can be obtained but it requires large values of reactive elements. Therefore this solution is more practical for higher frequencies, such as for 400 Hz and specially 20 kHz networks.

2.8.4 Passive PFC using Valley-Fill Circuit

A Valley-fill circuit is a type of passive power factor correction circuit. This circuit includes a rectifying circuit connected to a charge storage circuit. The general idea of valley-fill PFC is to improve the shape of the input current drawn from the AC line by increasing the conduction period of the rectifier diodes and hence reduce total harmonic distortion. A conventional valley-fill circuit requires three diodes and two capacitors. The circuit diagram is shown in Fig. 2.15. The principle operation of the basic valley-fill circuit and its detail analysis is done in the next chapter.

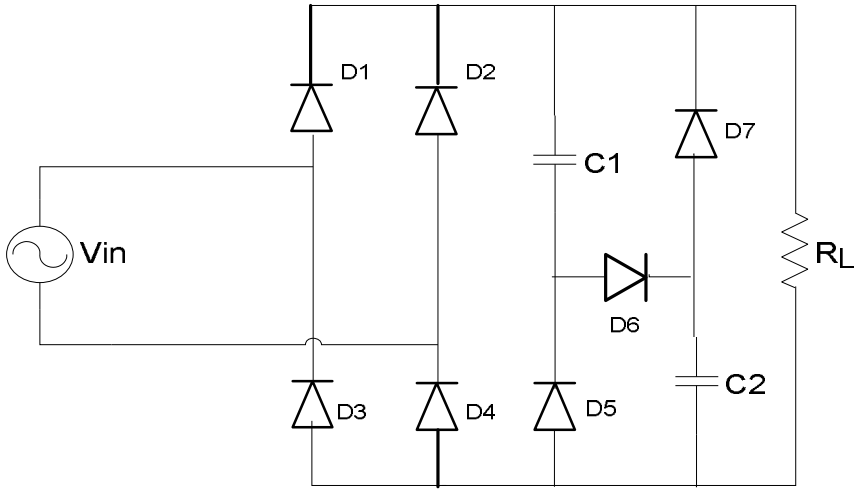

Fig. 2.15: Passive PFC with Valley-fill circuit.

2.9 Advantages of Active PFC

- Requires small and light components.
- A power factor value of over .95 can be obtained.
- Eliminates the line current total harmonic distortion.
- By this method automatic correction can be obtained for the AC line voltage.
- It is capable of operating in a full range of voltage.

2.10 Disadvantages of Active PFC

- The layout design is more complex.
- Since it needs PFC control IC, high voltage MOSFET and other circuits, it is highly expensive.
- It has lower efficiency.
- The low frequency switching active PFC requires large reactive elements and the output voltage regulation is slow.
- In high frequency switching buck converter based active PFC, the input current has significant high frequency components which increases EMI and filtering requirements.
- The high frequency switching boost converter based active PFC, when operating in the DCM mode is a popular choice but it suffers from high voltage stress across the dc-link capacitor and switches.
- It has high conduction loss.
- There is no inrush current limiting.

2.11 Advantages of passive PFC

- It has a simple structure
- It is reliable and rugged
- There is no generation of high-frequency EMI.
- There is no high frequency switching losses.
- It is insensitive to noises and surges.
- Efficiency is higher than active method.
- High power factor more than 0.95.
- Less expensive.
- It requires no control circuit.

2.12 Disadvantages of Passive PFC

- Solutions based on filters are heavy and bulky, because line-frequency reactive components are used.
- Lack voltage regulation and the shape of their input current depend on the load. Even though line current harmonics are reduced, the fundamental component may cause an excessive phase shift that reduces the power factor.
- AC range switching is required.

2.13 Comparison between Active and Passive PFC

From the above discussions, it is clear that power factor correction with passive method will give the better performance than active method according to efficiency, cost, simplicity, conduction losses, voltage stress, improved power factor and reduced THD. There are also some disadvantages of passive method having heavy and bulk reactive components. Among the passive methods one of the most efficient and cost effective method is valley-fill circuit based PFC. By modifying the Valley-fill circuit the performance can be made better and the demerits can be overcome.

Chapter 3

Analysis of Valley-Fill Electronic Ballast

3.1 Valley-Fill Electronic Ballast

Valley-fill circuits have long been recognized as a simple, low-cost option for providing power factor correction in power supplies and electronic ballasts that operate from a source of conventional AC power. The general idea of valley-fill power factor correction is to improve the shape of the current drawn from the AC line by increasing the conduction period of the rectifier diodes. This is achieved by maintaining a voltage on the bulk capacitors that is equal to a fraction of the peak value of the AC line voltage.

3.1.1Operation of Basic Valley Fill Electronic Ballast

The operation principle of valley-fill filter to power factor correction is to increase the conduction angle when the electronic ballast consumes line current, approaching its waveform to a sinusoidal one and decreasing total harmonic distortion (THD). The valley-fill circuit is capable of achieving a high power factor.But the VF circuit generates a high DC ripple voltage which causes a high crest factor in the lamp current and as a result the efficiency and the lifetime of the lamp reduces. The circuit diagram of the basic valley-fill circuit is shown in Fig 3.1 and its operation stages are shown in Fig 3.2. These operation stages show half line cycle, but the other half line cycle is identical.

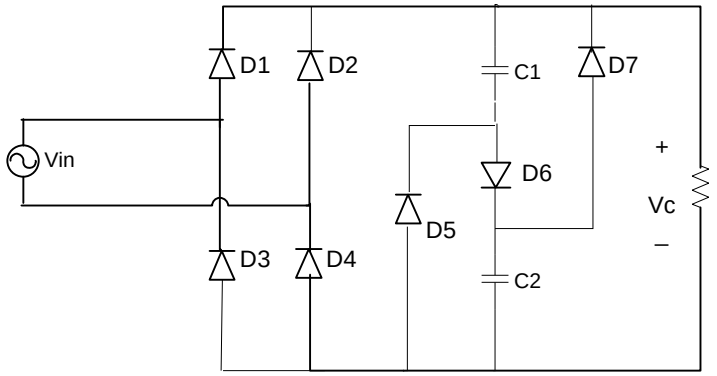

Fig 3.1: Basic Valley-fill circuit.

Stage-1

In this stage the instantaneous value of the line voltage is smaller than its peak value divided by two ($V_p/2$), D_5 and D_7 are forward biased and furtherdiodes are reverse biased. As a result the two capacitors C_1 and $C_2$are now in parallel and supply the load through D_5 and D_7 which results a determined voltage decrease. Line does not provide current to the ballast.

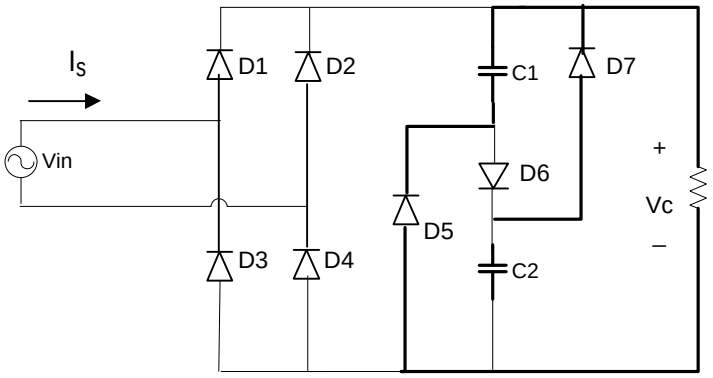

Fig 3.2(a): Operation of basic valley-fill circuit, Stage-1.

Stage-2

When the instantaneous value of the line voltage exceeds the value of stage 1, then line starts to feed the load, because D_1 and D_4 (D_2 and D_3 in the next half line-cycle) are forward biased and other diodes reverse biased. In this stage, DC bus voltage will pursue line voltage waveform.

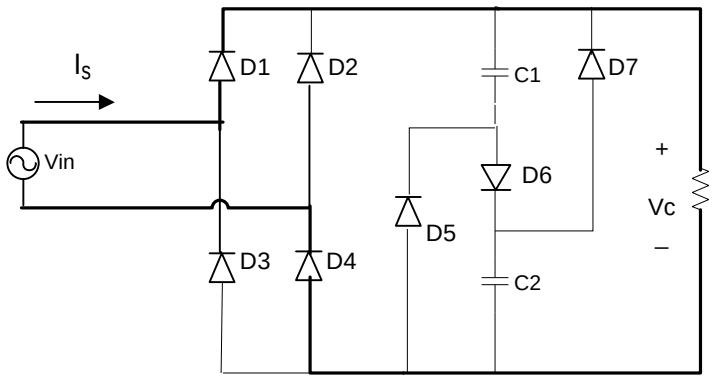

Fig 3.2(b): Operation of basic valley-fill circuit,Stage-2.

Stage-3

Diode D_6 starts conducting when the line voltage exceeds the sum of the voltages of C_1 and C_2. In this stage, besides line supplies the load, it will also charge both electrolytic capacitors in series, which will demand a peak current. DC bus voltage still pursues line voltage waveform.

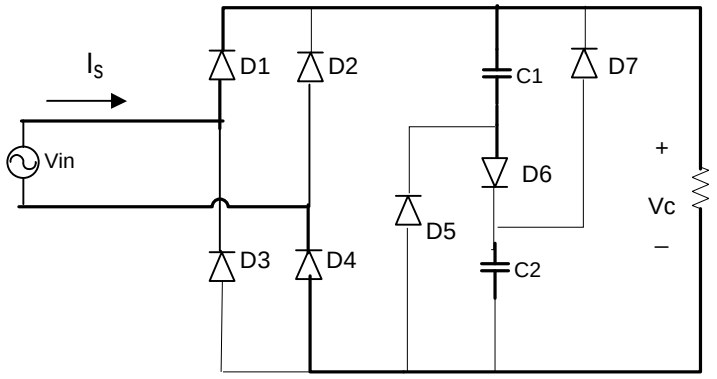

Fig 3.2(c): Operation of basic valley-fill circuit, Stage-3.

Stage-4

When the line voltage reaches its maximum value (V_p), each one of the capacitors (C_1 and C_2) will be charged with $V_p/2$. This stage operation is similar to operation of stage 2.

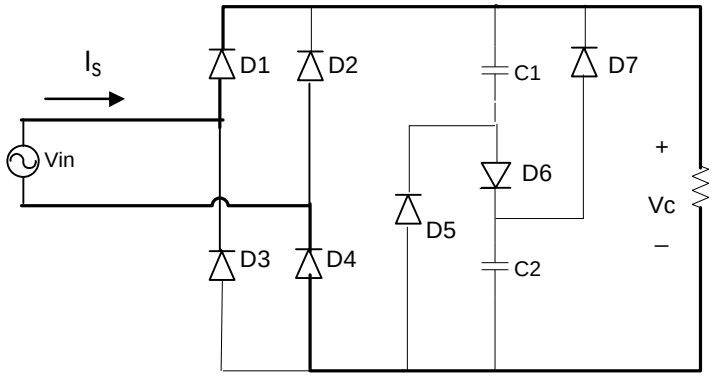

Fig 3.2(d): Operation of basic valley-fill circuit, Stage-4.

The typical waveforms of the basic valley-fill circuit are shown in Fig 3.3, Fig 3.4 and Fig 3.5.

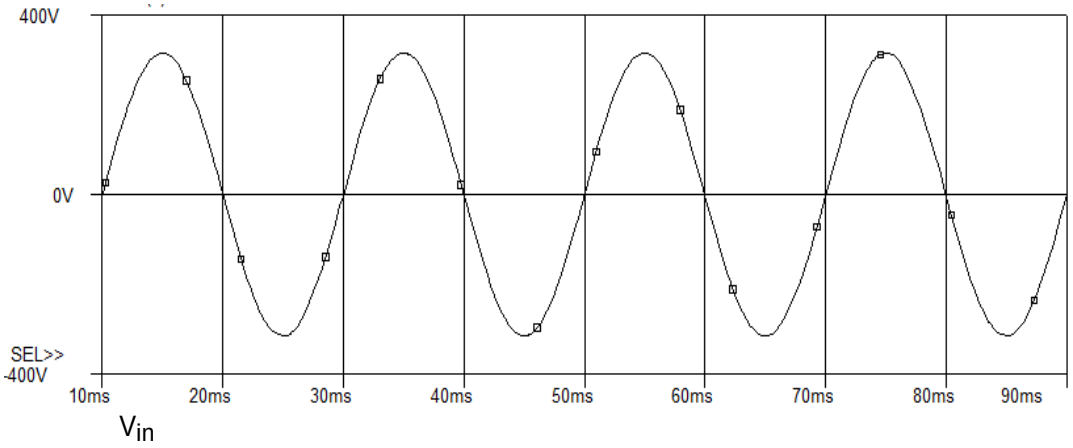

Fig 3.3: Simulated waveform of input voltage.

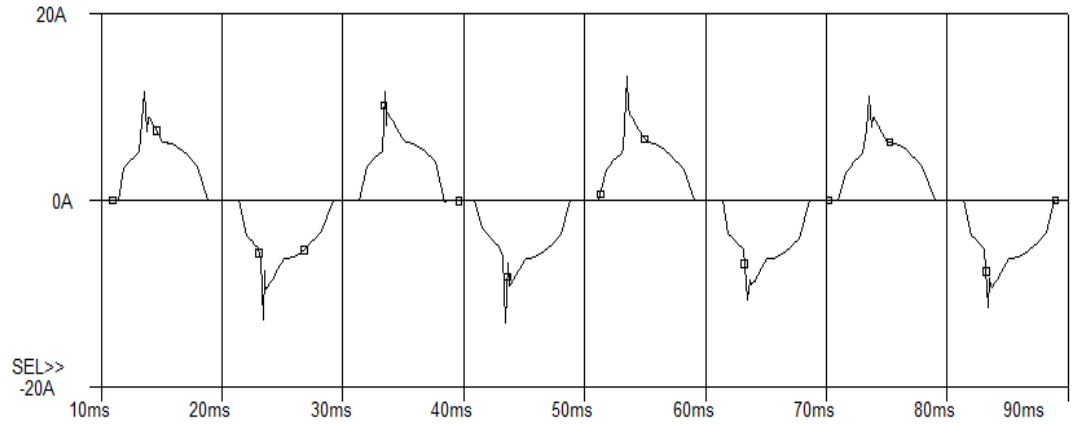

Fig 3.4: Simulated waveform of input current of the basic valley-fill circuit.

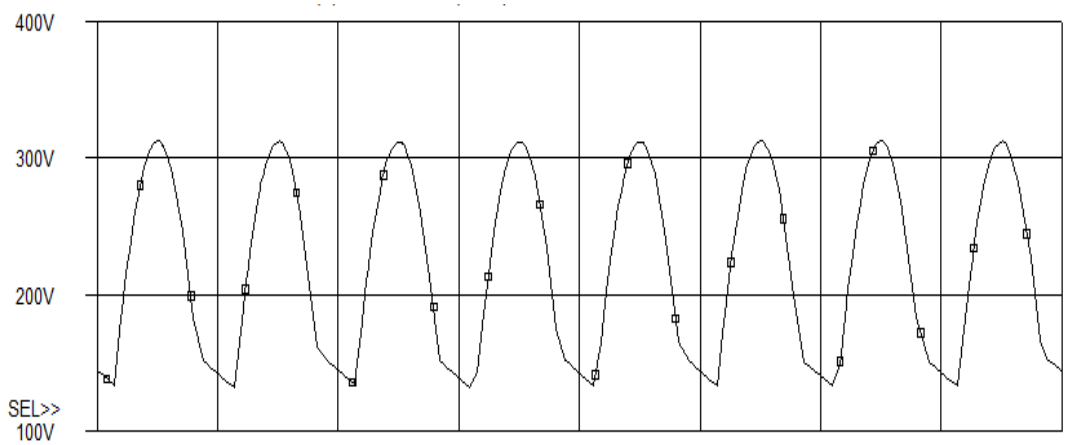

Fig 3.5: Simulated waveforms of output voltage of basic valley fill circuit.

From the above wave-shape it is observed that discontinuities occurred from $150^0$to 210^0 and from 330^0 to 360^0. This discontinuity which crosses from positive to negative and negative to positive causes most of the input current distortion during each cycle. The peak charging spike is a major contributor of current harmonics.

3.2 ImprovedVF ballast

Modified valley-fill electronic ballast has been illustrated in [25] where the conduction angle is extended and the THD is reduced than the basic VF circuit. Here the original VF circuit is extended by a circuit consisting of three diodes and one capacitor. It has achieved the same function as in the basic VF circuit but here the total capacitance is only one-third of the original capacitance during the charging action. The circuit diagram of the modified VF electronic ballast is shown below.

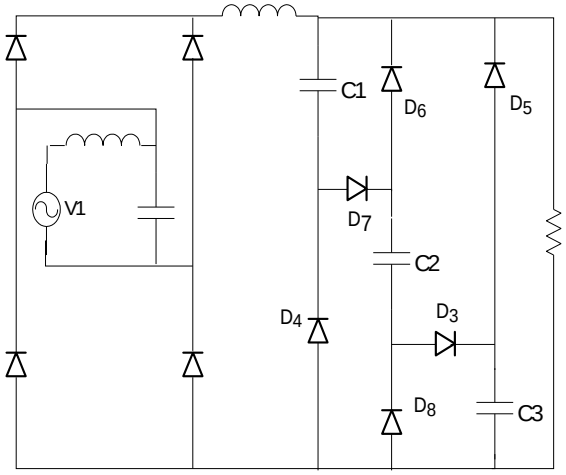

Fig 3.6: Modified version of Valley-fill electronic ballast.

Fig. 3.6 shows the circuit operating principles with the outputof the modified VF circuit replaced by a pure resistor. As theline voltage decreases and reaches the situation when Vin<Vc,the bridge rectifier stops conducting and diodes (D4, D5, D6,D8) conduct. The VF capacitors (C1, C2, C3) discharge their energy to the load. The total capacitance (C_T) during this stageis given by 3C1, where C1 = C2 = C3. When the line voltagereaches the peak voltage and is higher than the voltage acrossthe total capacitance, diodes (D3, D7) conduct, C_T in this caseis given by C1/3. As C_T = C1/3 is smaller than C1/2 in theconventional VF case, the charging action of the capacitors willonly demand a small peak of the current. This characteristic isvery helpful in reducing the THD of the resulting input current.The energy provided by the capacitors must equal the energybeing charged. This implies that the output voltage (Vc) is onethirdof the peak voltage during stage 1). The lower Vc impliesthat the line current continues to flow for an extended timeperiod. The ballast power circuit combiningthe modified VF circuit and

a current-fed resonant inverter hasshown to be able to achieve a high PF of 0.986 and THD of 16.9 %.

The simulated wave-shapes for the modified VF ballast circuit is shown in Fig 3.7:

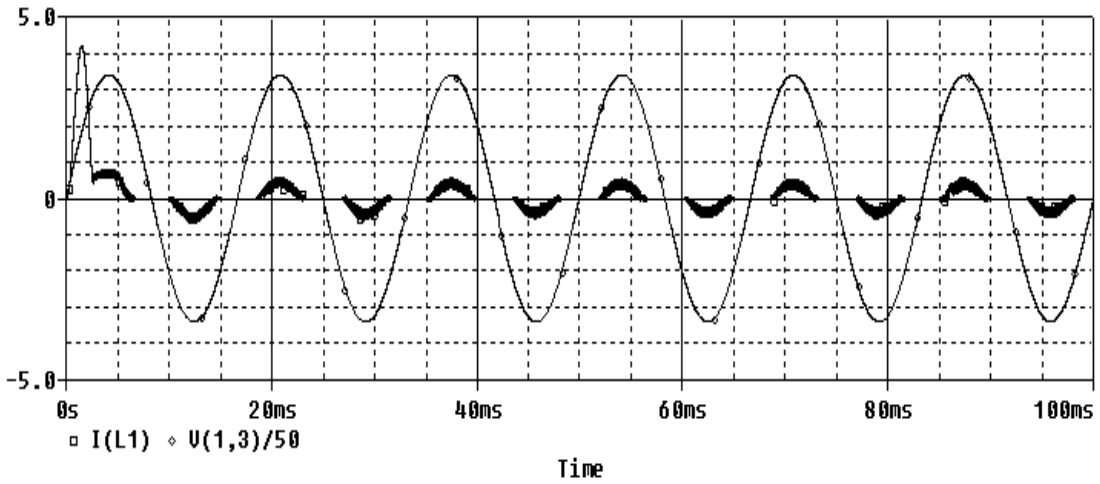

Fig 3.7: Simulated waveform of input line current and input voltage of the modified version of VF ballast circuit.

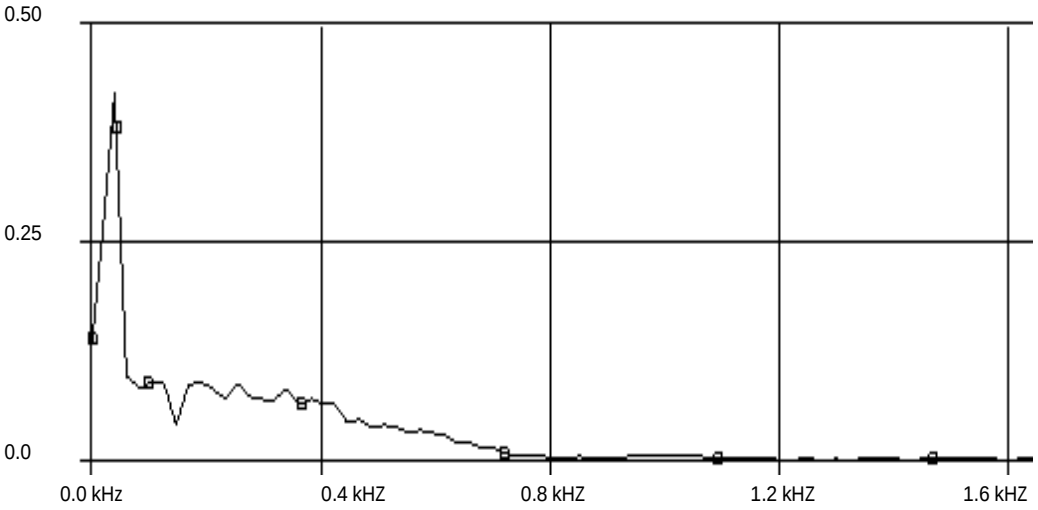

Fig 3.8: Simulated line current THD of the modified version of VF ballast circuit.

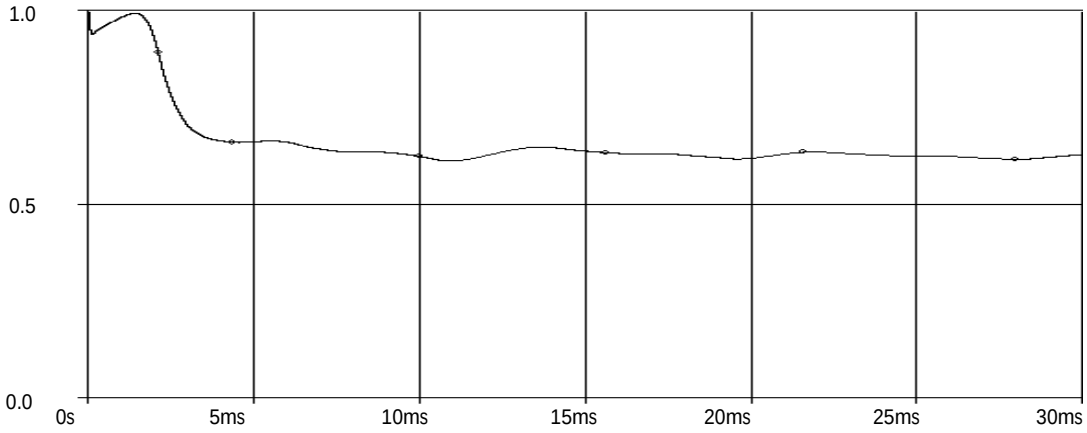

Fig 3.9: Power Factor of the modified version of VF ballast circuit.

3.3 Improvement of PF and input current THD through the analysis of the effect of different circuit components

From the above input current waveform of fig-3.1 it is found that current conduct from 30^0 to 150^0 and from 210^0 to 330^0. Much of the input current distortion is caused by these discontinuities which crosses from positive to negative, and then negative to positive, during each cycle. The peak charging spike is also a majorcontributor of current harmonics. If this cross-over distortion and the charging spike can be lessened or eliminated, then the likelihood of usingthis circuit to meet the IEC specifications would be very high. So to improve the standard circuit (i) Cross-over distortion in the input current waveform must be reduced and (ii) Charging spike at the peak of the current wave must be suppressed [25].

3.3.1 VF ballast with Voltage Doubler and a resistor

To maintain the flow of input current, a voltage doubler is inserted to feed the valley fill circuit. The circuit diagram of the valley-fill circuit with a voltage doubler is shown in Fig 3.10.As bulk of the power is conveyed in the current waveform during conduction time so a small amount of power will be required to supplement the missing currents during the discontinuities. Also the amplitude of the missing parts are small comparatively, duringthe cross-over time, whereas the amplitude of current is of much higher level during the main conduction period. So the voltage doubler is configured in such a way that it canprovide a small amount of power to the main circuit to improve the cross-over points, i.e. the capacitors used in the voltage doubler can be orders of

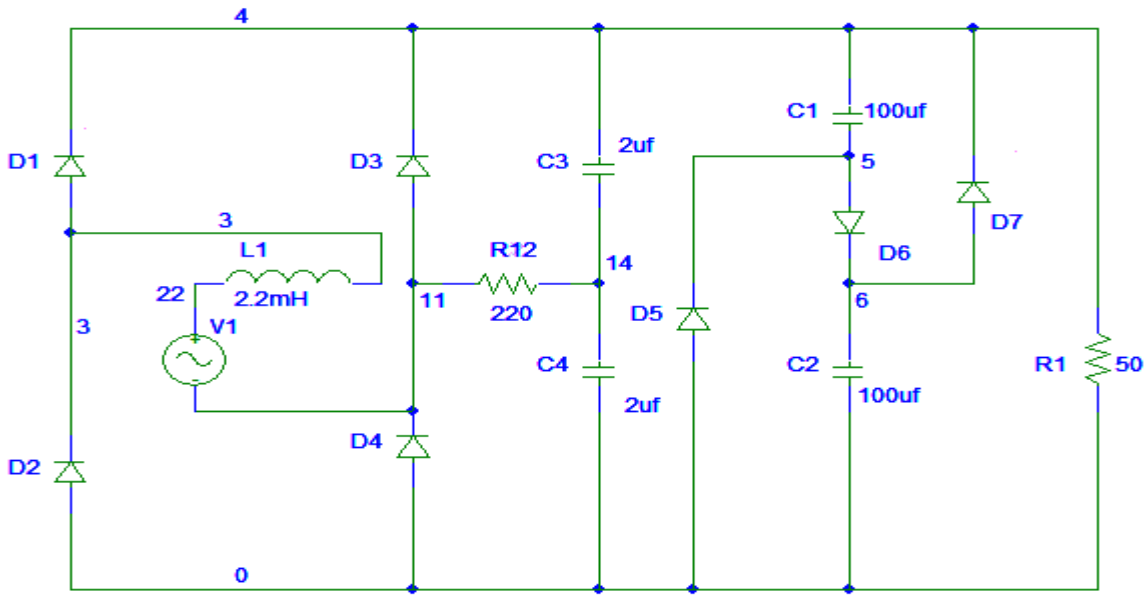

Fig 3.10: Valley-fill electronic ballast with voltage doubler and a resistor (Scheme-1).

magnitude smaller thanthe values of C1 and C2. Under normal conditions, the energy from the voltage doubleris totally absorbed by the main circuit but during the cross-over periods, it comes into play by continuing to draw current from the line. Thus the input current conduction angle is further extended. A resistor R_{12} is inserted (one terminal of the resistor is connected to the junction of D3 and D4, and the other terminal is connected to the junction of C3 and C4) to remove the charging spike at the cross-over points.

The typical simulated waveforms are shown in Fig 3.11, Fig 3.12 and Fig 3.13.

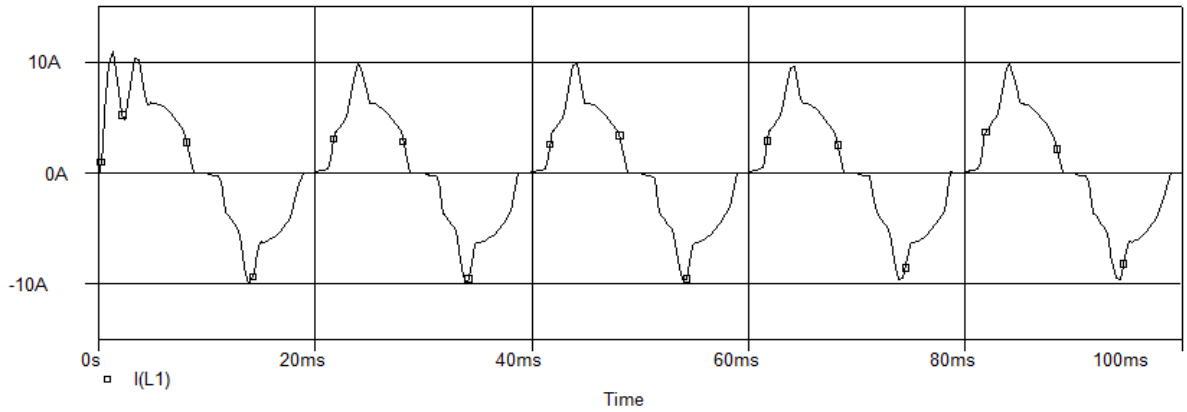

Fig 3.11: Simulated input line current (Scheme-1).

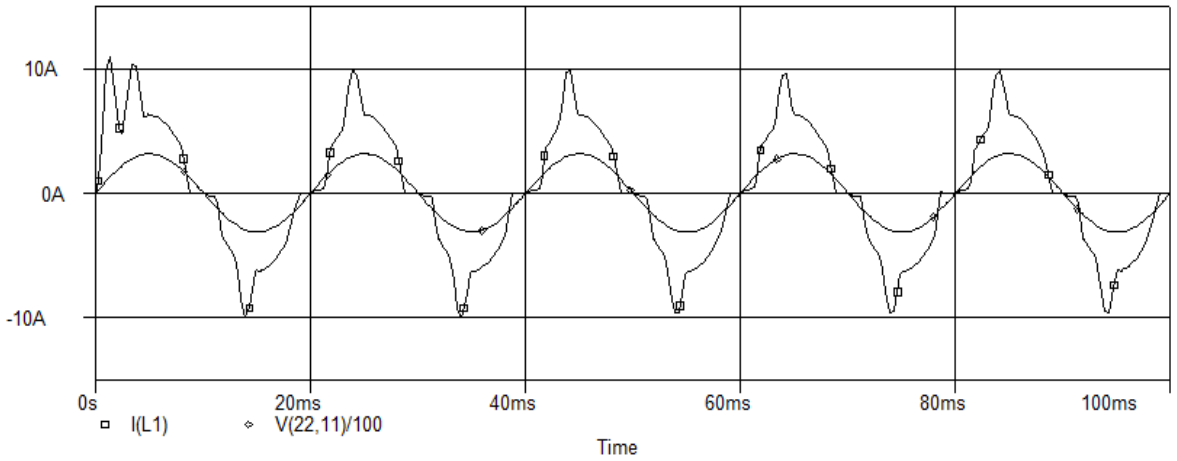

Fig 3.12: Simulated input line current and input voltage of Scheme-1.

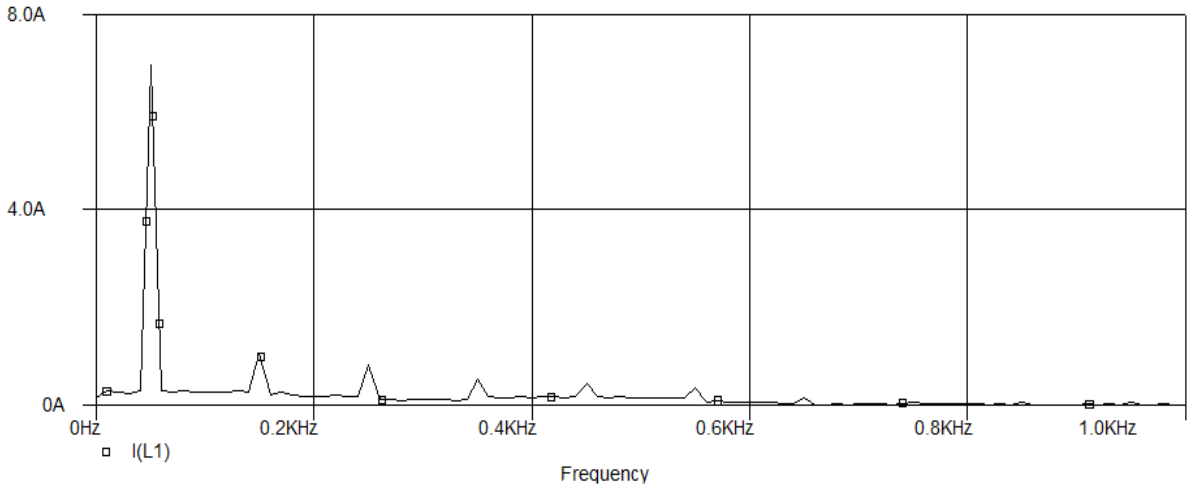

Fig 3.13: Simulated line current THD of Scheme-1.

3.3.2 Modified VF ballast Scheme-1 in addition with R_{11}

In the input line current waveform of scheme-1, still there are current discontinuities and peak charging spike. This peak current charging spike is also a major contributor of current harmonics. So to remove the peak current charging spike a resistor R_{11} is connected to the bottom electrode of C_2. By simulating the modified VF ballast Scheme-2 the waveform will be observed. The circuit diagram of the modified VF ballast scheme-2 is shown in Fig 3.14.

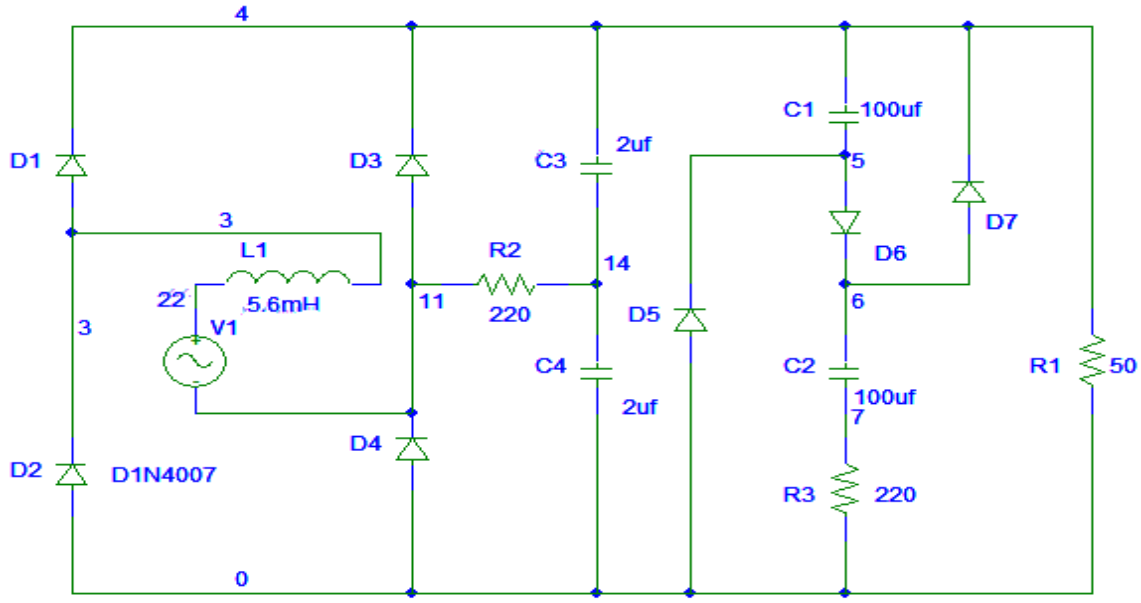

Fig 3.14: Modified VF ballast Scheme-2.

The typical waveforms of input line current, input voltageand input current THD are shown in Fig 3.15, Fig 3.16 and Fig 3.17 respectively.

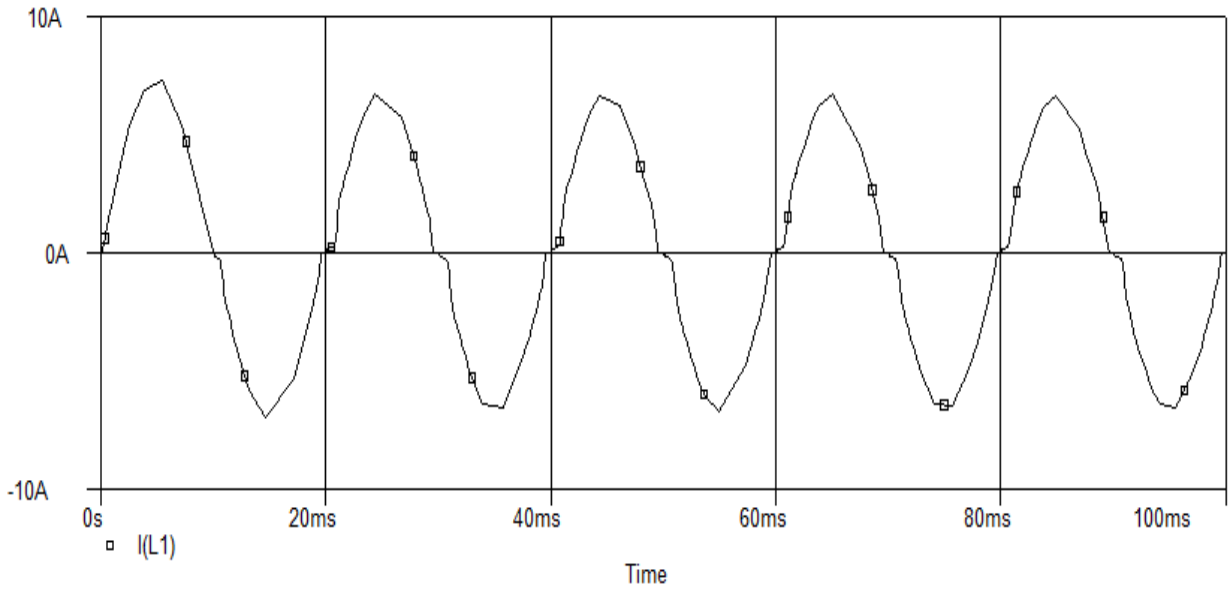

Fig 3.15: Simulated input line current of modified VF ballast Scheme-2.

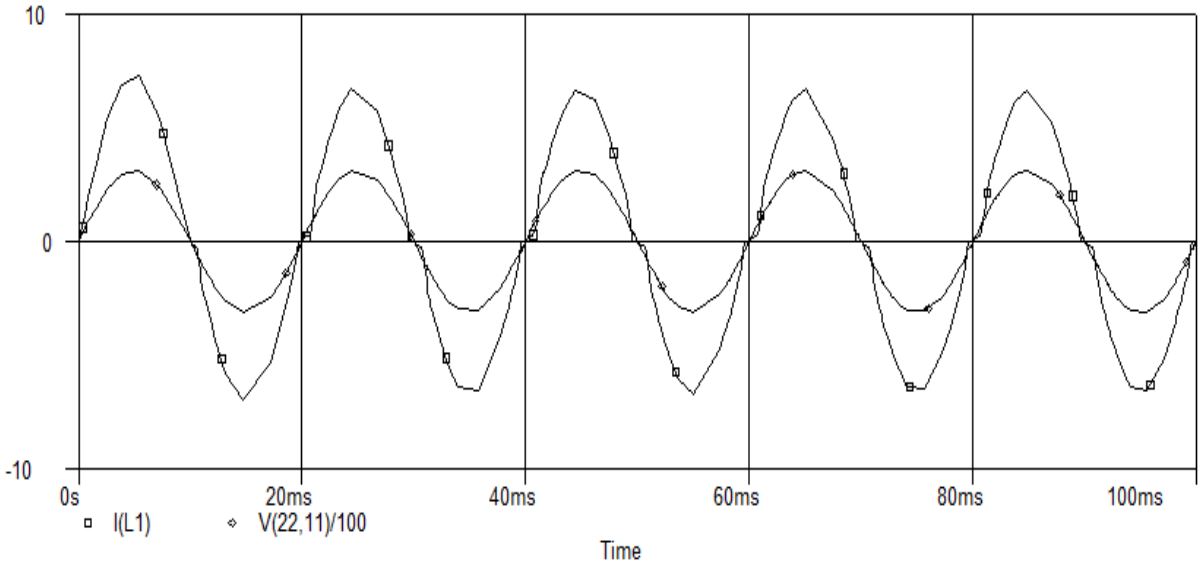

Fig 3.16: Simulated input line current and input voltage of modified VF ballast Scheme-2.

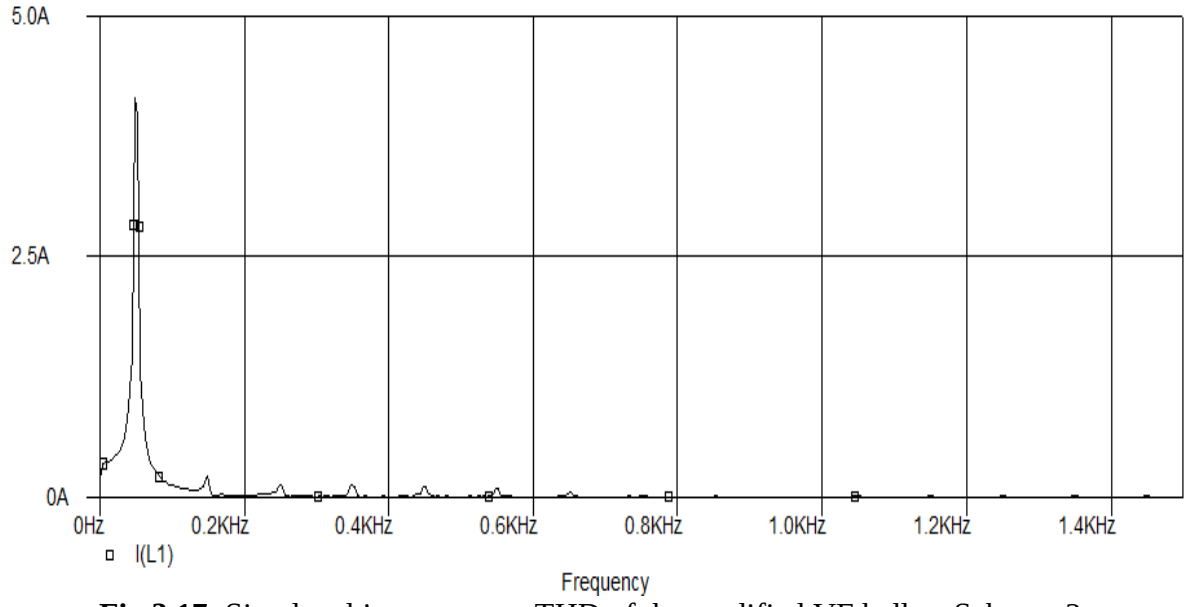

Fig 3.17: Simulated input current THD of the modified VF ballast Scheme-2.

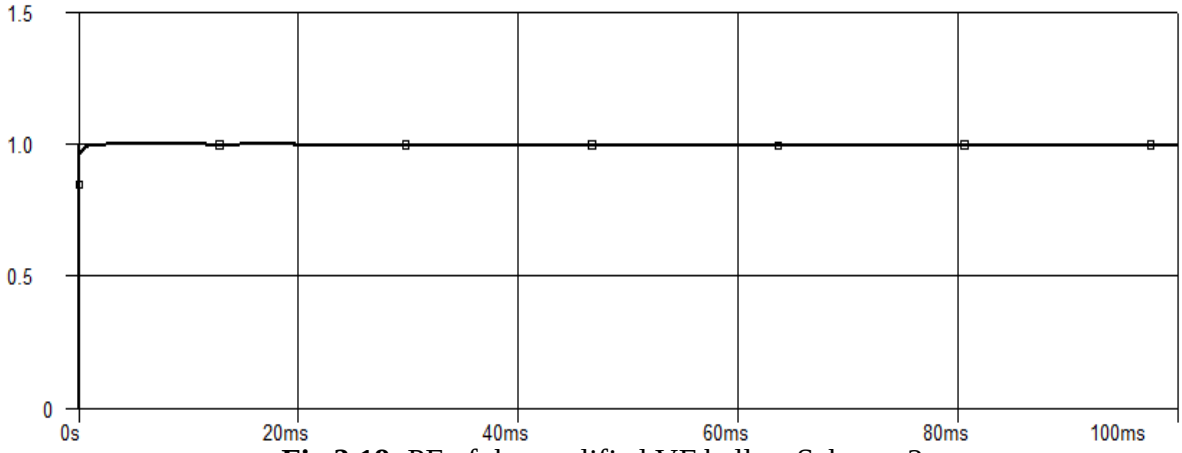

Fig 3.18: PF of the modified VF ballast Scheme-2.

3.3.3 Modified VF ballast Scheme-2 in addition with R_5 (Scheme-3)

From the waveforms of Scheme-2, it is observed that the power factor and the input current THD have been improved but still there are discontinuity in conduction. A resistor R_5 of value 20k is connected in series with the diode D_5 and analyzes the typical waveforms. The Circuit diagram of the VF circuit Scheme-3 is shown in Fig 3.19.

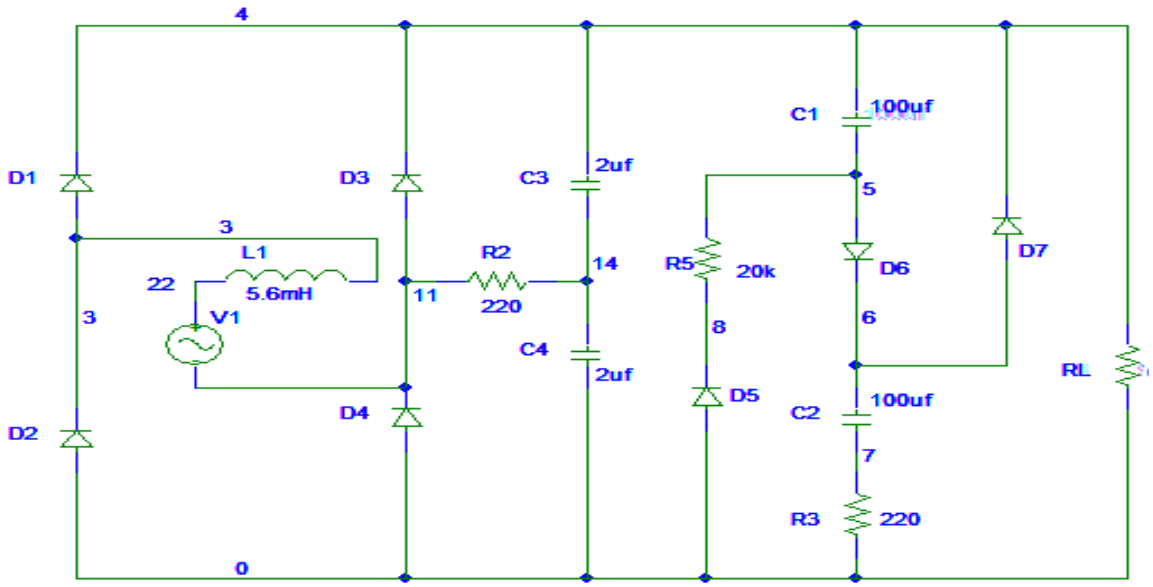

Fig 3.19: Modified VF ballast Scheme-2 in addition with R_5 (Scheme-3).

The simulated waveform of input line current, input voltage and input current THD are shown in Fig 3.20, Fig 3.21 and Fig 3.22.

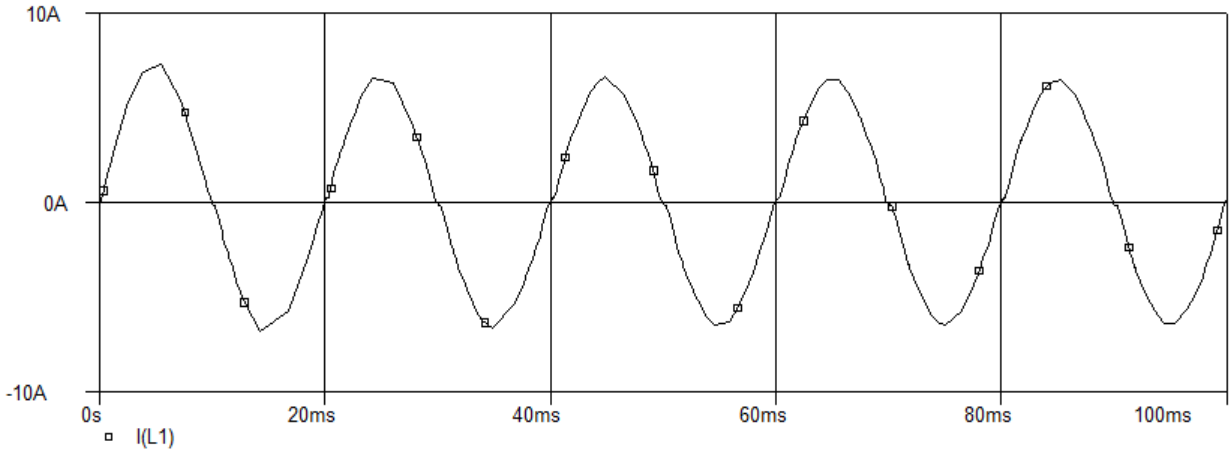

Fig 3.20: Simulated input line current of Scheme-3.

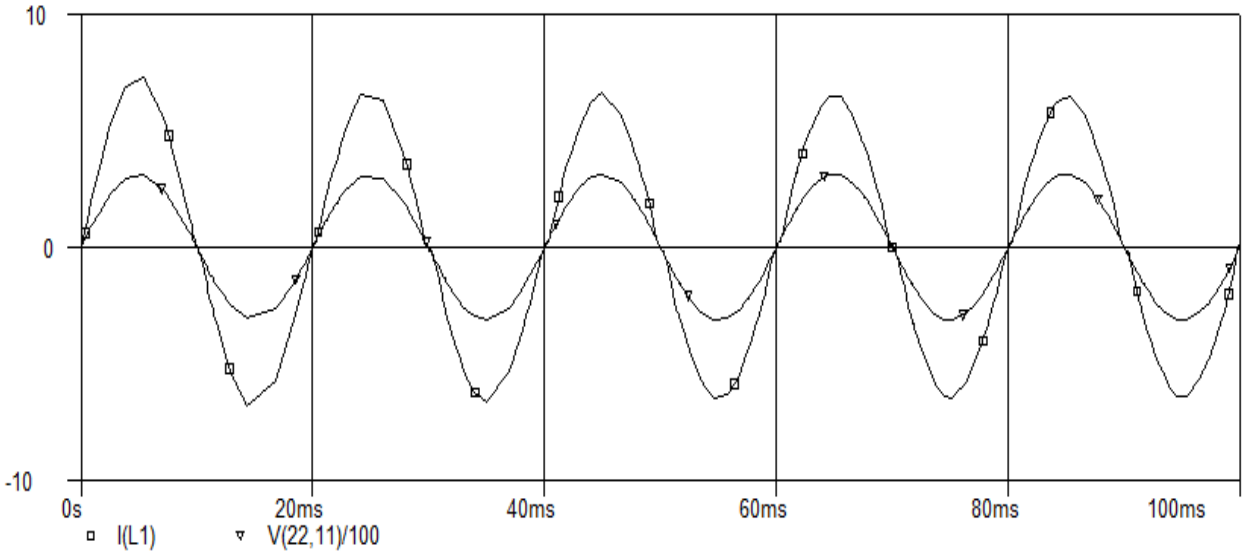

Fig 3.21: Simulated input current and input voltage of Scheme-3.

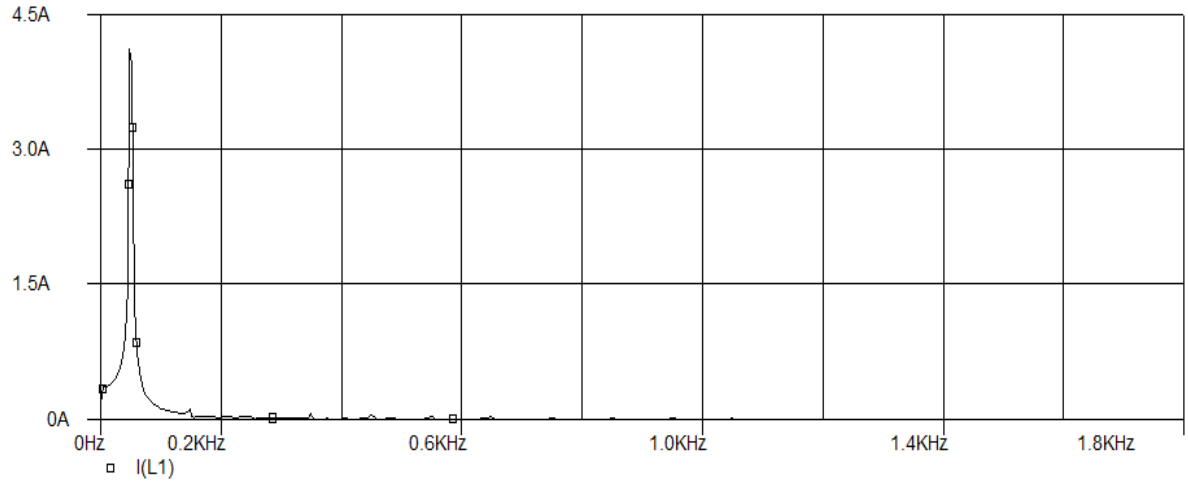

Fig 3.22: Simulated input current THD of Scheme-3.

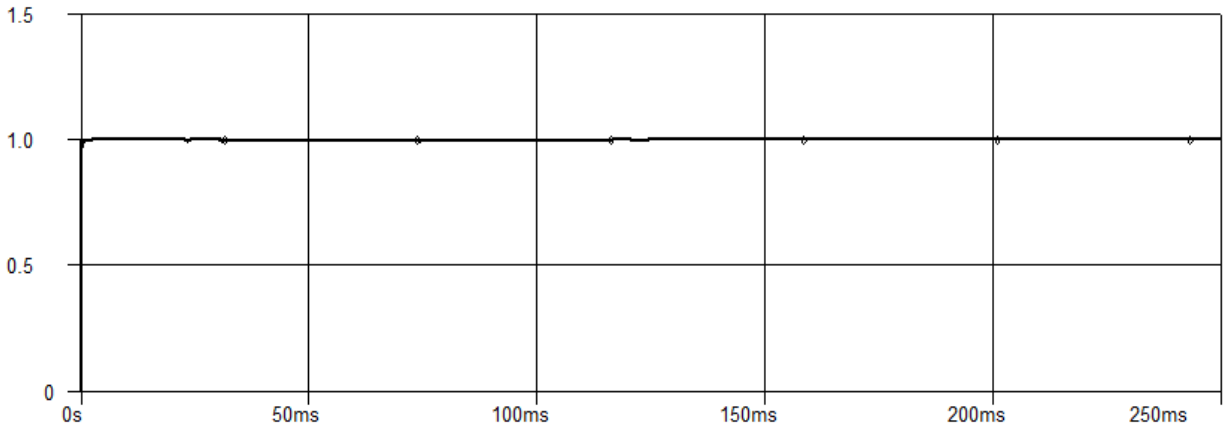

Fig 3.23: PF of Scheme-3.

From the above waveforms, it is observed that insertion of the resistor R_5 in series with D_5 extended the conduction angle than Scheme-2 but still there are some discontinuities. The power factor is one. In order to improve the input current and input current THD the modified VF ballast Scheme-2 is analyzed in other way.

3.3.4 Modified VF ballast Scheme-2 in addition with resistor R_{13} and inductor L_2(Scheme-4)

In this scheme the VF ballast is further modified by adding a resistor R_{13} (one terminal at the lower end of diode D_6 and other terminal at the upper electrode of capacitor

C_2)and an input inductor at the VF circuit. The circuit diagram of the modified VF ballast scheme-4 is shown in Fig 3.24. Here R_{13} limits the current that charges the capacitors C_1 and C_2. The input inductor L_2 at the VF circuit behaves like a boost inductor which helps to shape the line current automatically.

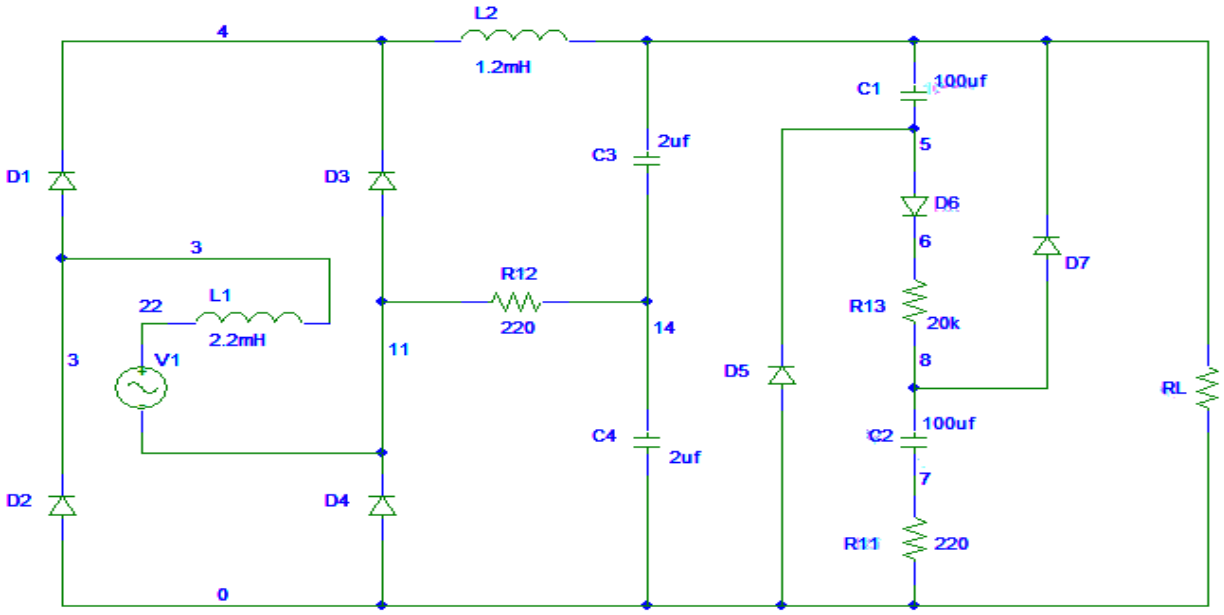

Fig 3.24: Modified VF ballast Scheme-4.

The simulated waveforms of input line current, input voltage, input current THD and power factor are shown in Fig 3.25, Fig 3.26, Fig 3.27 and Fig 3.28.

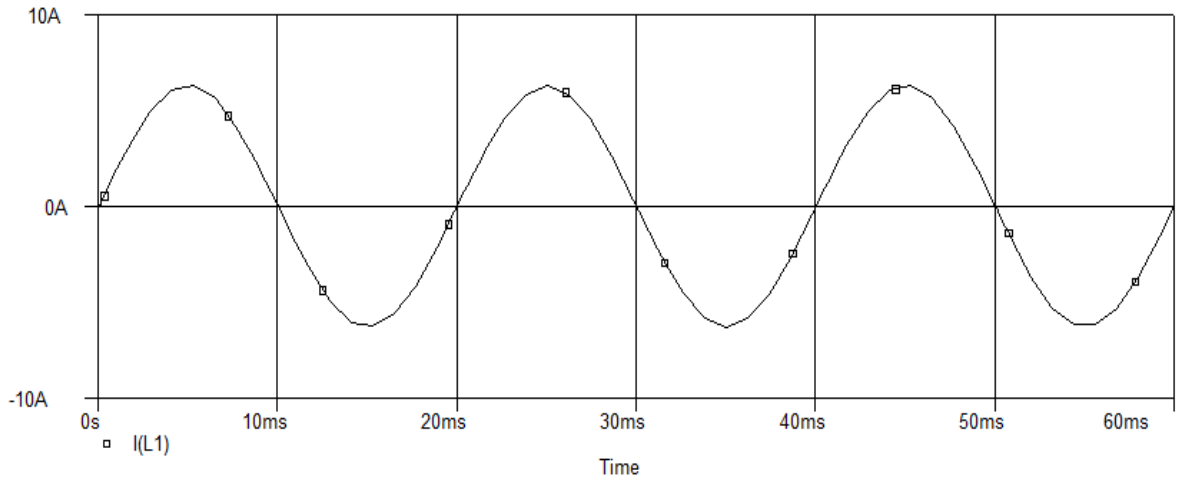

Fig 3.25: Simulated input current of modified VF ballast Scheme-4.

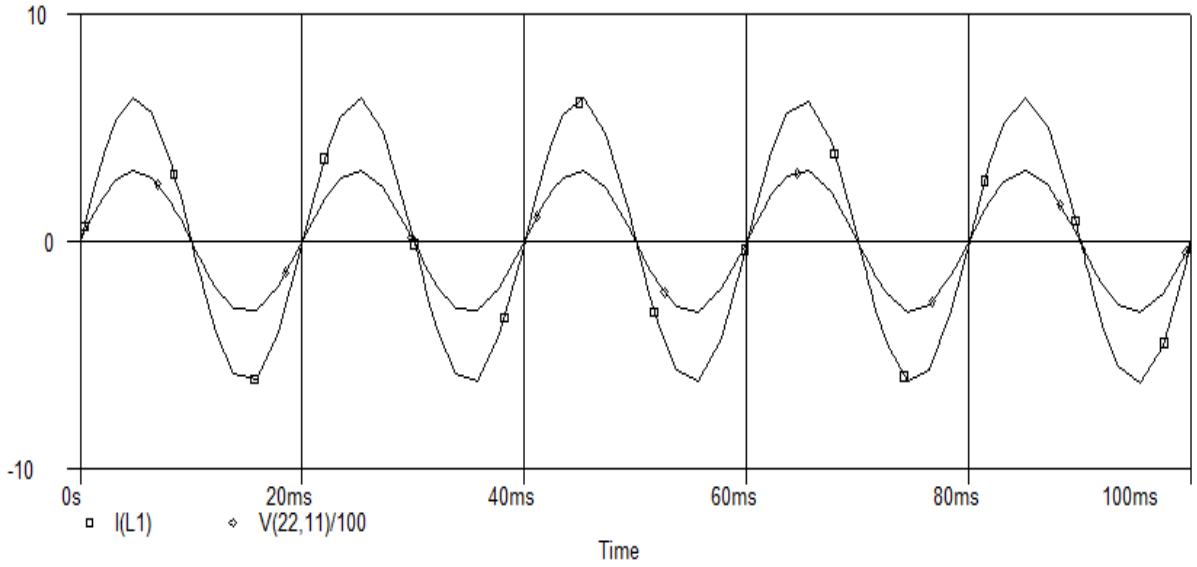

Fig 3.26: Simulated input current and input voltage of modified VF ballast Scheme-4.

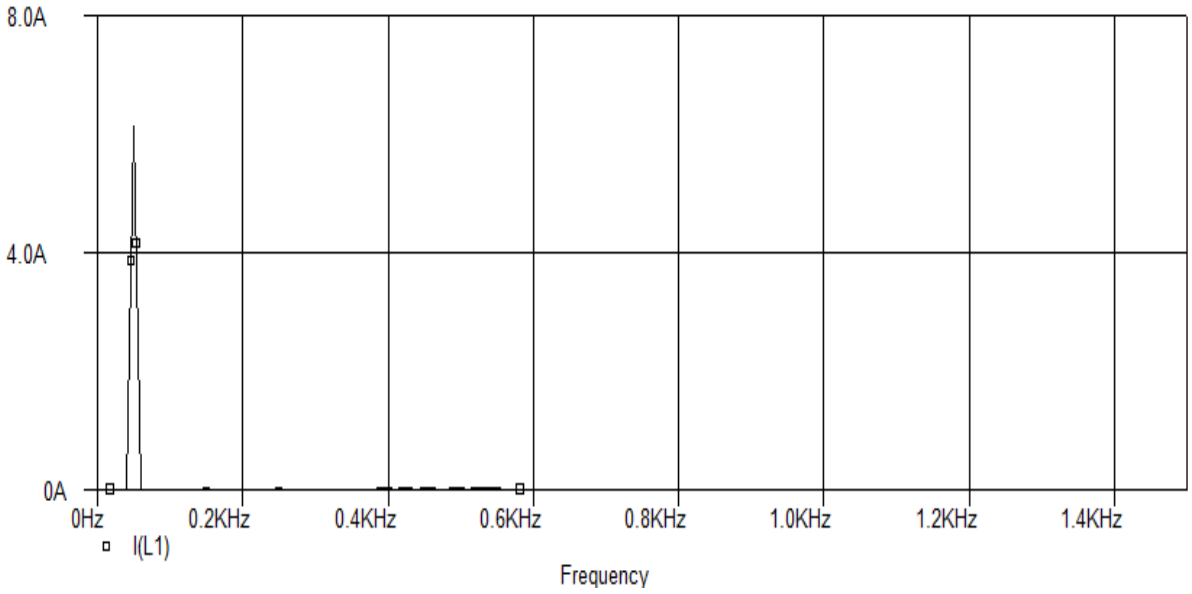

Fig 3.27: Input current THD of modified VF ballast Scheme-4.

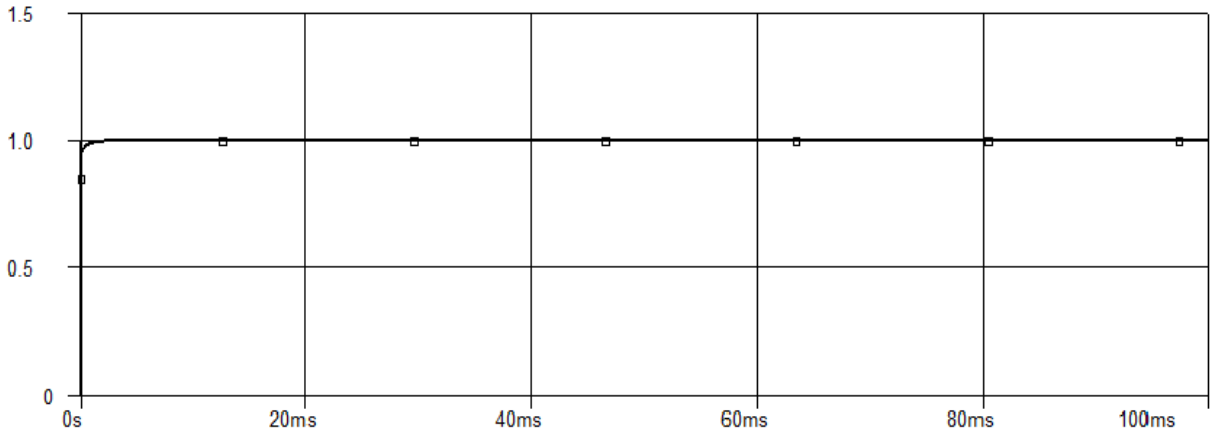

Fig 3.28: PF of modified VF ballast Scheme-4.

3.4 Performance analysis

In this work, the Valley-Fill circuit is modified from the above waveforms of different modified VF ballast schemes; it is observed that the modified VF circuit scheme-4 has the better performance. The input current waveform is sinusoidal. There is no distortion in the current waveform and the THD is minimized. The power factor is also 1.0.

Chapter 4

Performance Analysis of Proposed VF ballast Circuit

4.1Proposed Valley-Fill Electronic Ballast

The proposed modified VF ballast is combined with a current fed resonant inverter as the lamp power circuit. It has an extended conduction time which is achieved by using voltage doubler. By the modified VF ballast the output capacitor voltage of the VF circuit has been lowered and as a result the conduction time of the line current is extended. The charging spike can also be removed by this proposed modified VF ballast circuit which is a contributor of current harmonics. The input inductor at the VF circuit behaves like a boost inductor and helps to shape the line current automatically. Because of using current fed resonant inverter, there is no need to use isolation transformer or opto-coupler to provide isolation in the driver circuit [26-27].

4.1.1 Operating principle of proposed VF ballast circuit

In order to maintain continuous current drawn from the line, during the cross-over period the voltages must not be less than half of the peak input voltage. Because only half of the peak line voltage appears across each capacitor and when they are discharging, they are being in parallel. As bulk of the power is conveyed in the current waveform during conduction time so a small amount of power will be required to supplement the missing currents during the discontinuities. Also the amplitude of the missing parts is small comparatively, during the cross-over time, whereas the amplitude of current is of much higher level during the main conduction period.
The proposed modified VF circuit is composed of one voltage doubler and three resistors. The circuit diagram of the proposed VF circuit is shown in Fig 4.1. The proposed VF circuit is shown in Fig 4.2 with the output to be replaced by a pure resistor.

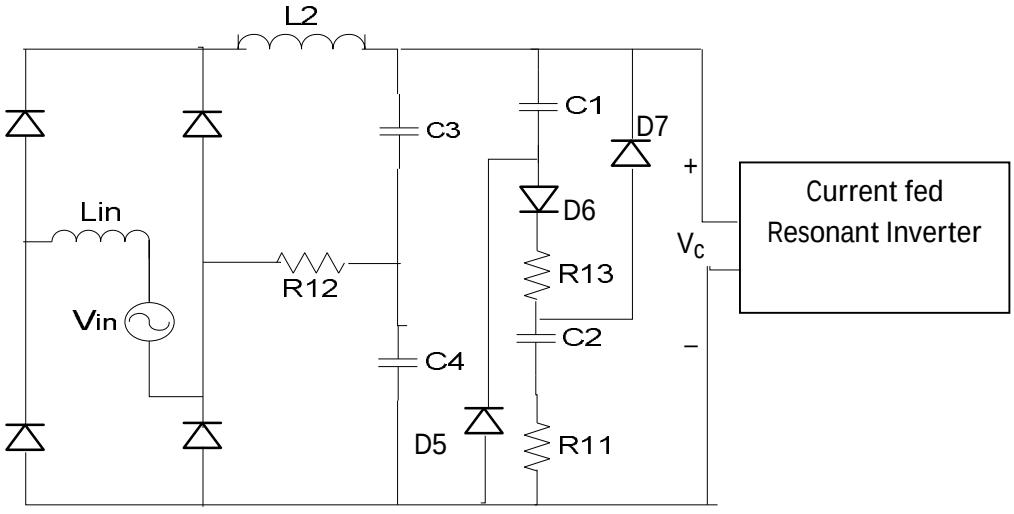

Fig 4.1: Proposed modified Valley-Fill electronic ballast.

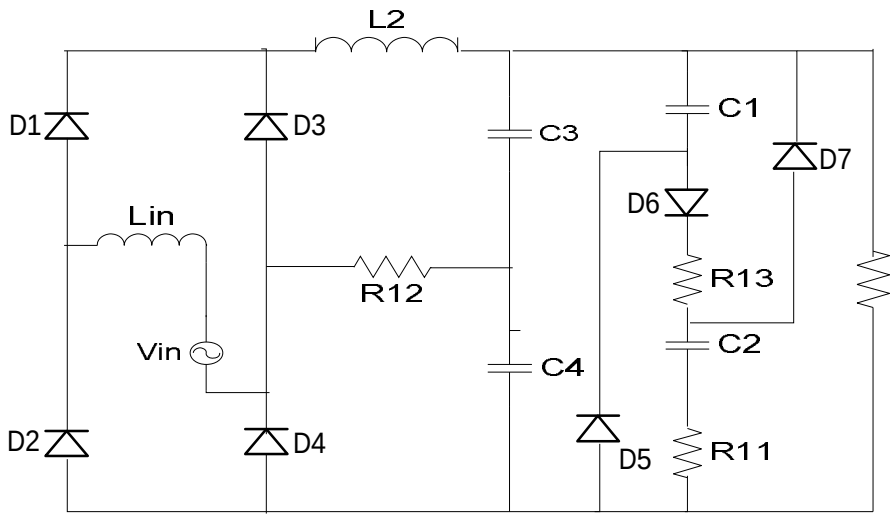

Fig 4.2: Circuit diagram of the Proposed VF electronic ballast.

When the line voltage is lower than each capacitors voltage, the capacitors (C1 and C2) of the proposed VF circuit are effectively parallel through diode D5 and D7. When the input voltage is larger than the load voltage, the bridge rectifier conducts, D5 and D7 are reverse biased and load current is provided directly from the line. The diode D6 starts conducting when the line voltage exceeds the sum of the voltages of C1 and C2. In order to maintain the flow of current, a voltage doubler is inserted and it is configured in such a way that a small amount of power can be supplied to the main circuit which is enough to improve the crossover points i.e. the magnitude of the capacitors used in the voltage doubler can be orders of magnitude smaller than the values of C1 and C2. Under normal operating condition, the main circuit absorbed the energy from the voltage doubler. But, during the crossover periods, the voltage doubler plays its role by continuing to draw current from the line and hence the input current conduction angle is further extended. However the peak charging current spike still persists which is a contributor of harmonics. In order to reduce line current total harmonic distortion, R11 (connected to the bottom electrode of C2) and R12 (one terminal of the resistor is connected to the junction of D3and D4, and the other terminal is connected to the junction of C3 and C4) are inserted. Insertion of this resistor will remove the charging spike at the cross-over points and enhance the quality of the input current. The resistor R13 limits the current that charges the capacitors C1 and C2. The network C3, C4 and R12 has the effect ofextending the conduction angle at the low values of line voltage. This feature improves the PF and reduces the THD.

4.2 Current fed resonant inverter

The schematic diagram of the current fed resonant inverter is shown in Fig. 4.3. The current fed resonant inverter consists of two input choke inductors (L1, L2). Two series diodes (D1, D2), two switches (M1, M2) and a series-parallel resonantThe schematic diagram of the current fed resonant inverter is shown in Fig. 7. The current fed resonant inverter consists of two input choke inductors (L1, L2). Two series diodes (D1, D2), two switches (M1, M2) and a series-parallel resonantcircuit.The key operating principles of the current source inverter has been illustrated in [11], by applying fundamental analysis. Equations (1) – (3) highlight the voltage gain, corner frequency and quality factor, respectively. The resonant circuit should operate below resonance so that the reverse recovery losses in the diodes can be minimized [10].

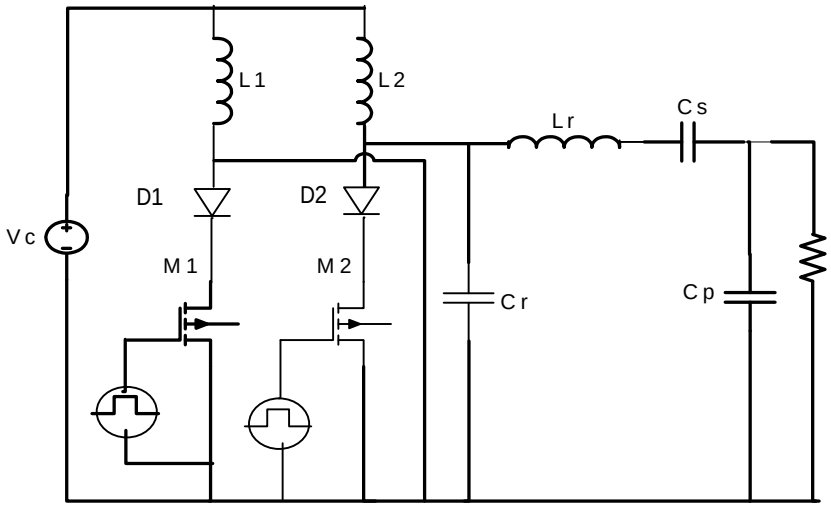

Fig 4.3: Current fed resonant inverter.

$$\left|\frac{V_0}{V_{in}}\right| = \sqrt{\left(1 - w_r^2 + \frac{1}{C_{r1}}\right)^2 + \left(\frac{w_r}{Q}\right)^2 \left(1 + C_{r2} + \frac{C_{r2}}{C_{r1}} - w_r^2 C_{r2}\right)^2} \qquad (1)$$

Where $Q = \frac{w_0 L_r}{R_{lamp}} = \frac{1}{w_0 C_r R_{lamp}} =$ quality factor (2)

With $C_{r1} = \frac{C_s}{C_r}$, $C_{r2} = \frac{C_p}{C_r}$ and

$w_r = \frac{w_s}{w_0}$ = Relative operating frequency

$$w_0 = \frac{1}{\sqrt{L_r C_r}} = \text{CORNER FREQUENCY} \qquad (3)$$

4.2 Comparative study and Simulation results

Comparative studies has been done by configuring the proposed modified VF ballast circuit with parameters of different value and analyzed in order to obtain a suitable design which will further enhance the performance of the Valley-Fill electronic ballast.For each configuration the performances of the circuits are simulated in ORCAD PSPICE 9.2. The results realized in the software are compared and analyzed.

4.2.1 Proposed Modified VF ballast circuit with Configuration-1

The circuit diagram of the proposed modified VF ballast is shown in Fig 4.4. All the circuit components value and their corresponding part numbers are listed in table-4.1.

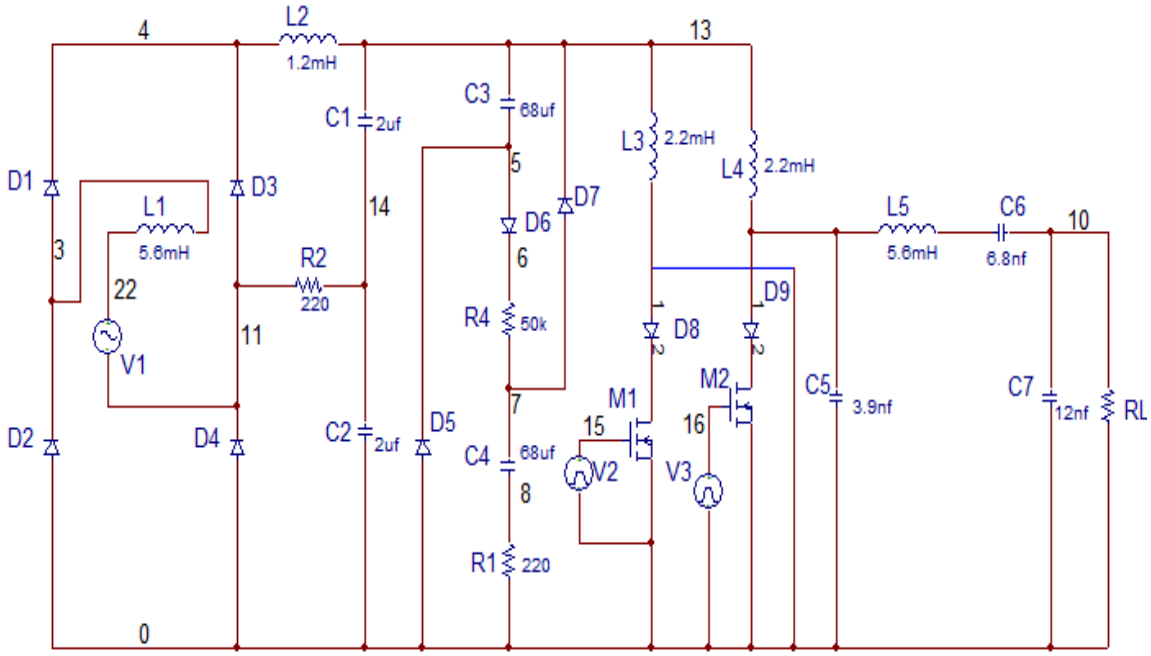

Fig 4.4: Proposed modified VF ballast circuit with configuration-1.

Table 4.1: Circuit parameters for the proposed VF ballast Circuit Configuration-1

Circuit Parameter	Value and part number
Lr	5.6 mH
Cr	3.9 nF
Cs	6.8nF
Cp	12nF
D5, D6, D7	Standard recovery D1N4007
L1, L2	2.2mH
C1, C2	68uF

C3, C4	2uF
Lin	5.6mH
M1, M2	N-channel MOSFET IRF 540
D1, D2	1N4376
R11, R12	220 ohm
R13	50k

The simulated waveforms of the proposed VF ballast with configuration-1 are shown below.

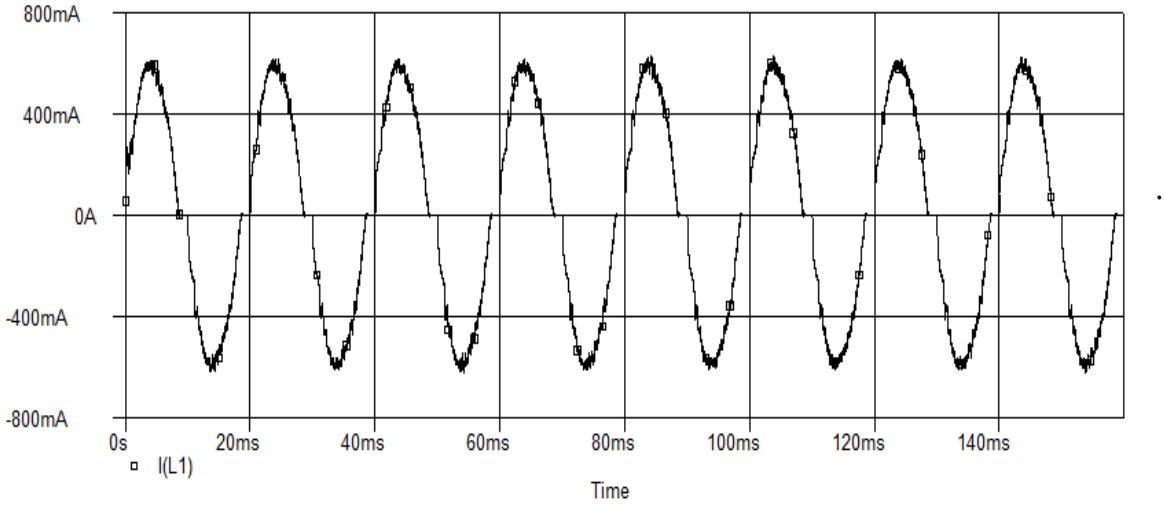

Fig 4.5: Simulated input line current of the proposed VF ballast circuit with configuration-1.

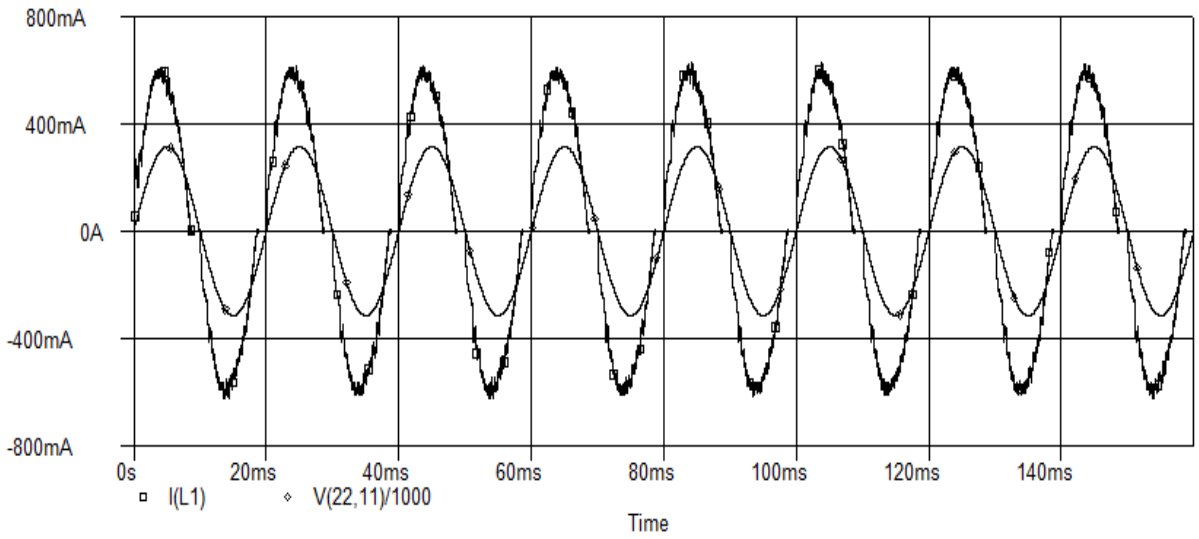

Fig 4.6: Simulated input line current and input voltage of proposed VF ballast circuit configuration-1.

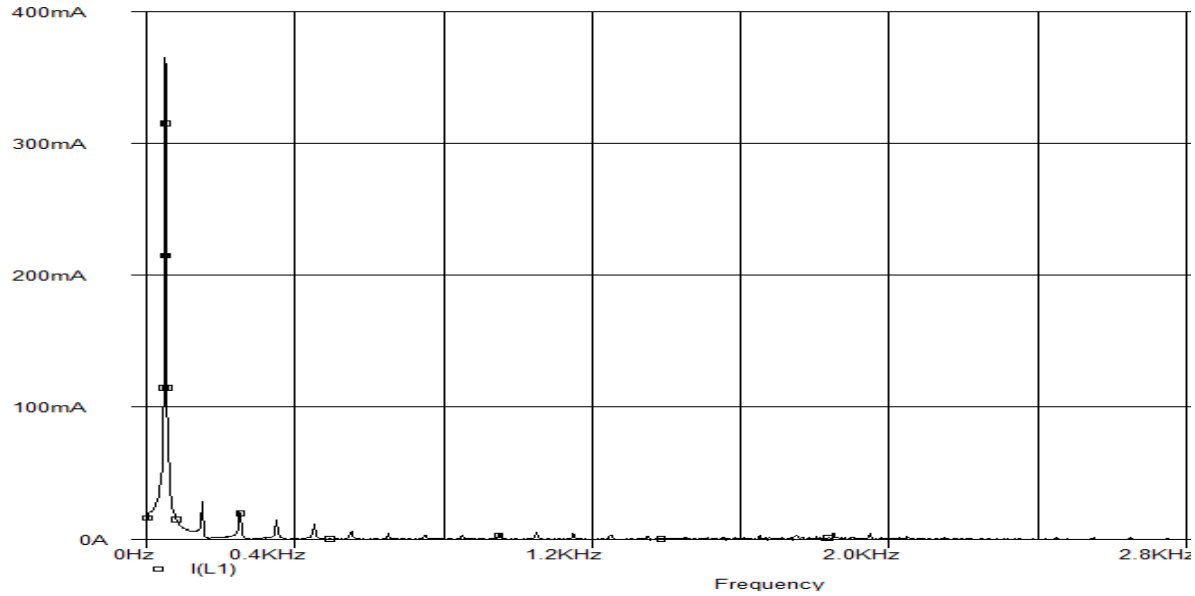

Fig 4.7: Simulated input current THD of the proposed VF ballast circuit configuration-1.

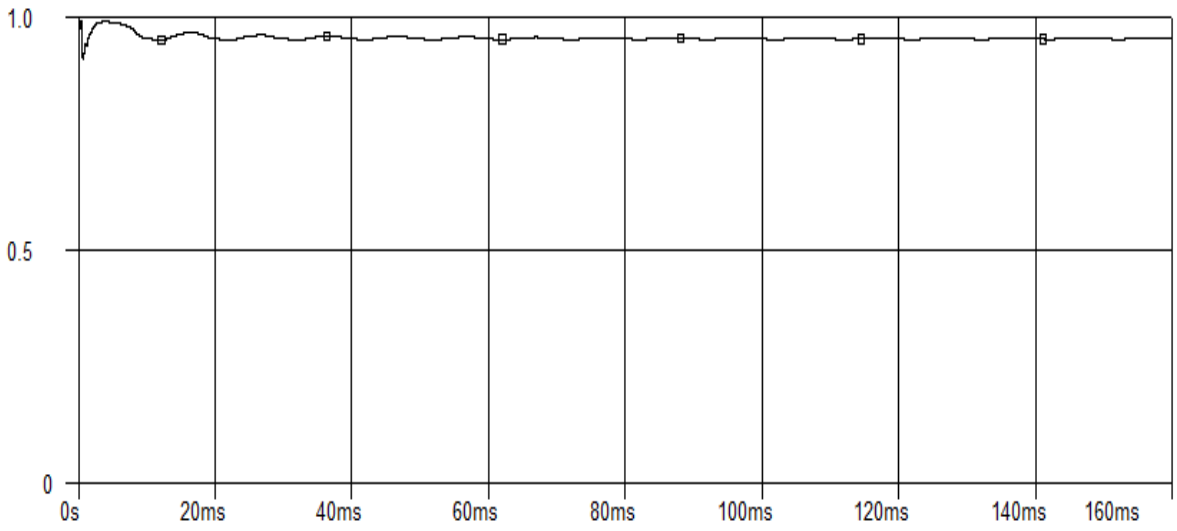

Fig 4.8: PF of the proposed VF ballast circuit configuration-1.

4.2.2 Proposed modified VF ballast circuit with configuration-2

The circuit diagram of the proposed Modified VF ballast with configuration-2 is shown in Fig 4.6. All the circuit components value and their corresponding part numbers are listed in table-4.2.

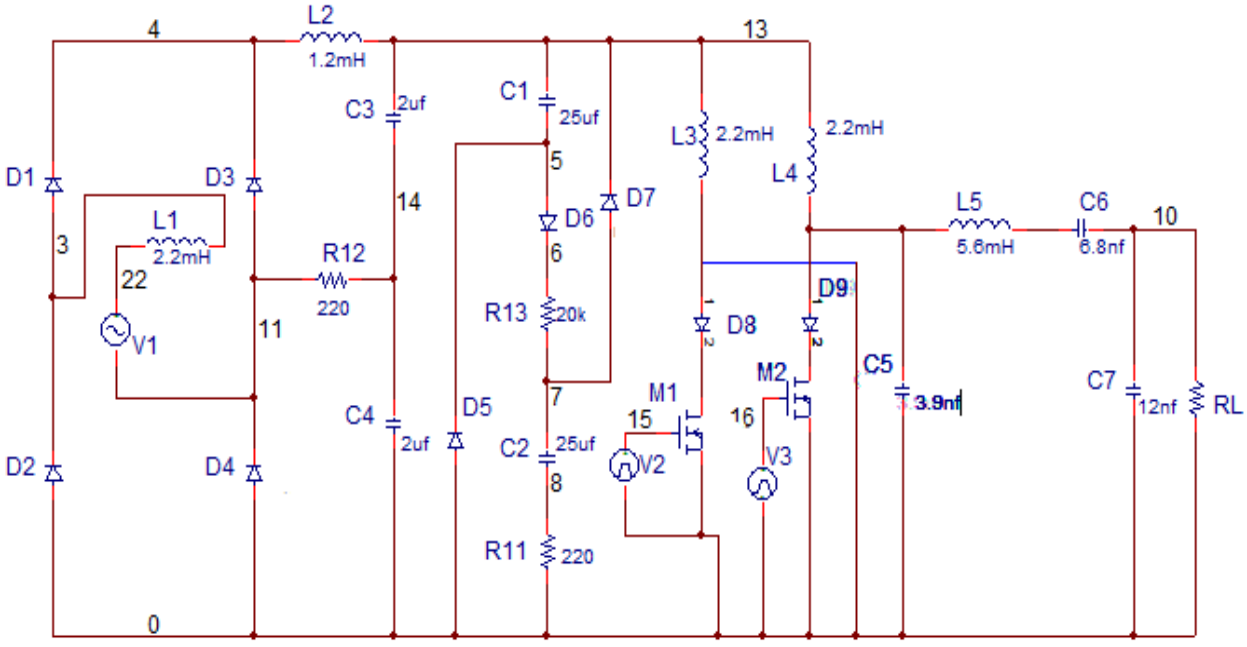

Fig 4.9: Proposed modified VF ballast circuit with configuration-2.

Table 4.2: Circuit parameters for the proposed VF ballast Circuit Configuration-2

Circuit Parameter	Value and part number
Lr	5.6 mH
Cr	3.9 nF
Cs	6.8nF
Cp	12nF
D5, D6, D7	Standard recovery D1N4007
L1, L2	2.2mH
C1, C2	25uF
C3, C4	2uF
Lin	2.2mH
M1, M2	N-channel MOSFET IRF 540
D1, D2	1N4376
R11, R12	220 ohm
R13	20k

The simulated waveforms for the proposed VF ballast circuit with configuration-2 are shown below.

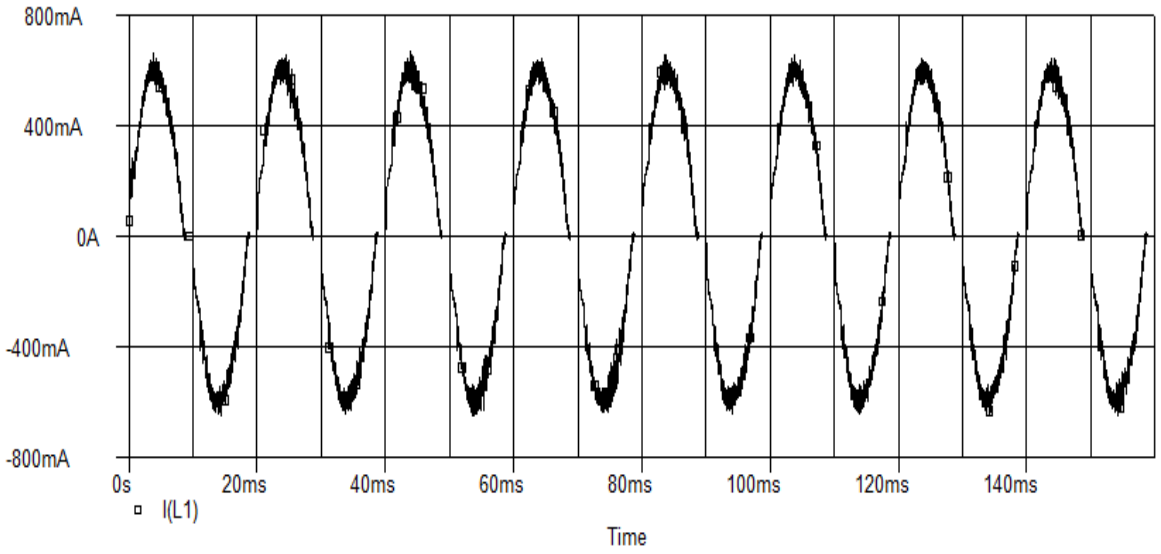

Fig 4.10: Simulated input line current of the proposed VF ballast circuit configuration-2.

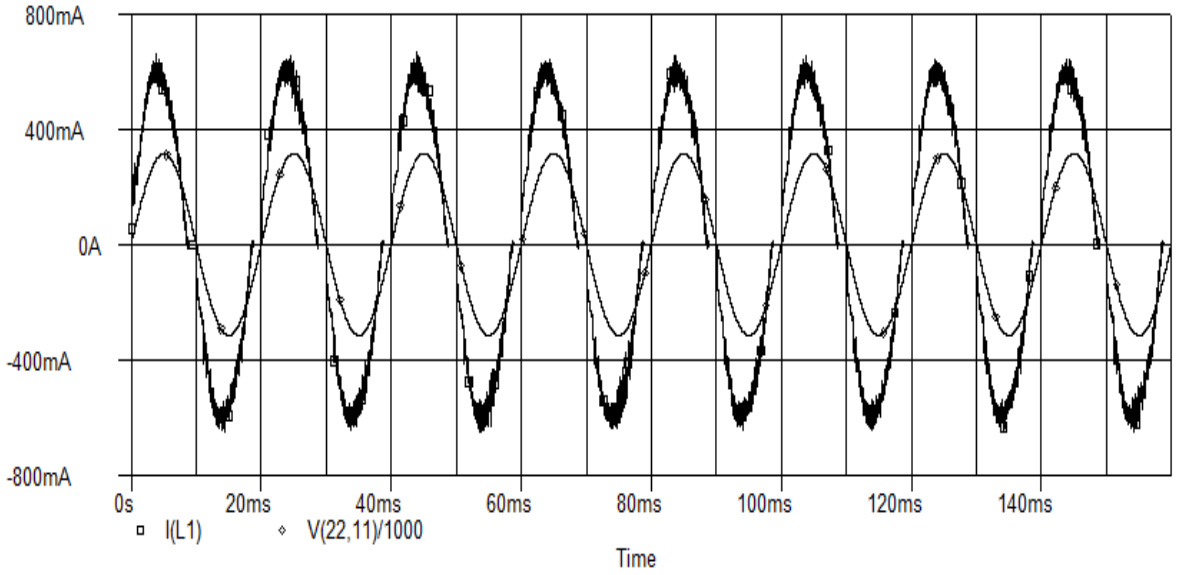

Fig 4.11: Simulated input line current and input voltage of proposed VF ballast circuit configuration-2.

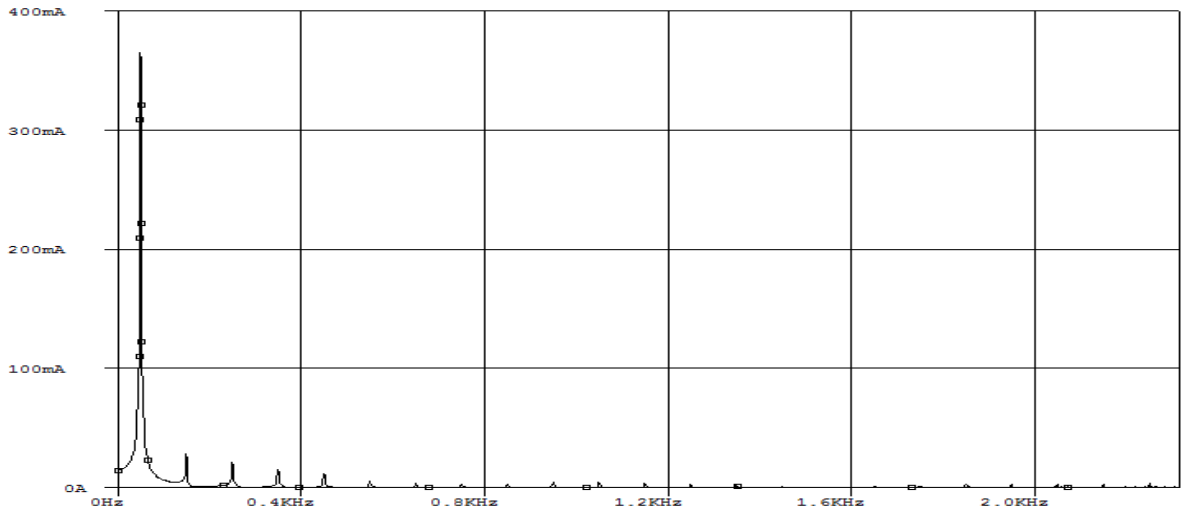

Fig 4.12: Input Current THD of the proposed VF ballast circuit configuration-2.

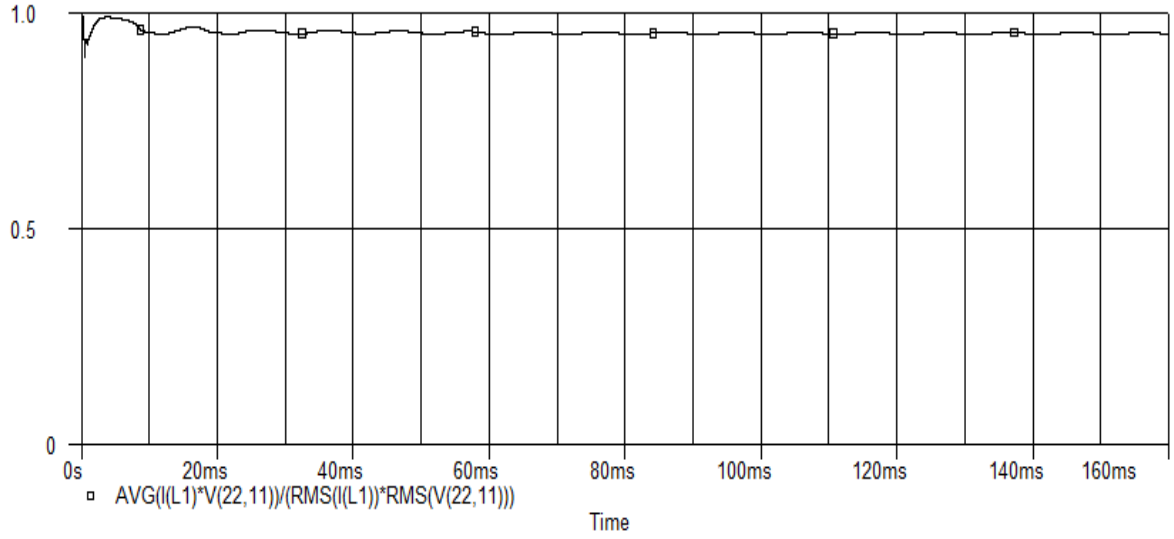

Fig 4.13: PF of the proposed VF ballast circuit configuration-2.

4.2.3 Proposed Modified VF ballast circuit with configuration-3

The circuit diagram of the proposed modified VF ballast is shown in Fig 4.11. All the circuit components value and their corresponding part numbers are listed in table-4.3.

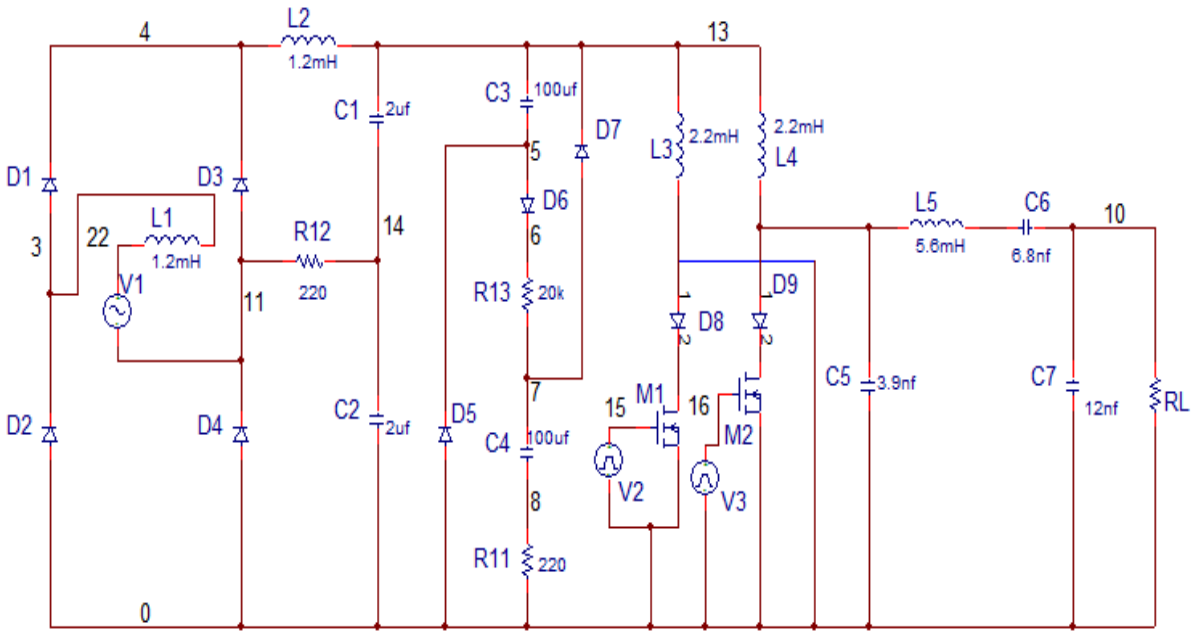

Fig 4.14: Circuit dagram of the proposed VF ballast with configuration-3.

Table 4.: Circuit parameters for the proposed VF ballast Circuit with Configuration-3

Circuit Parameter	Value and part number
Lr	5.6 mH
Cr	3.9 nF
Cs	6.8nF
Cp	12nF
D5, D6, D7	Standard recovery D1N4007
L1, L2	2.2mH
C1, C2	100uF
C3, C4	2uF

Lin	1.2mH
M1, M2	N-channel MOSFET IRF 540
D1, D2	1N4376
R11, R12	220 ohm
R13	20k

The simulated waveforms of the proposed VF ballast with configuration-3 are shown below.

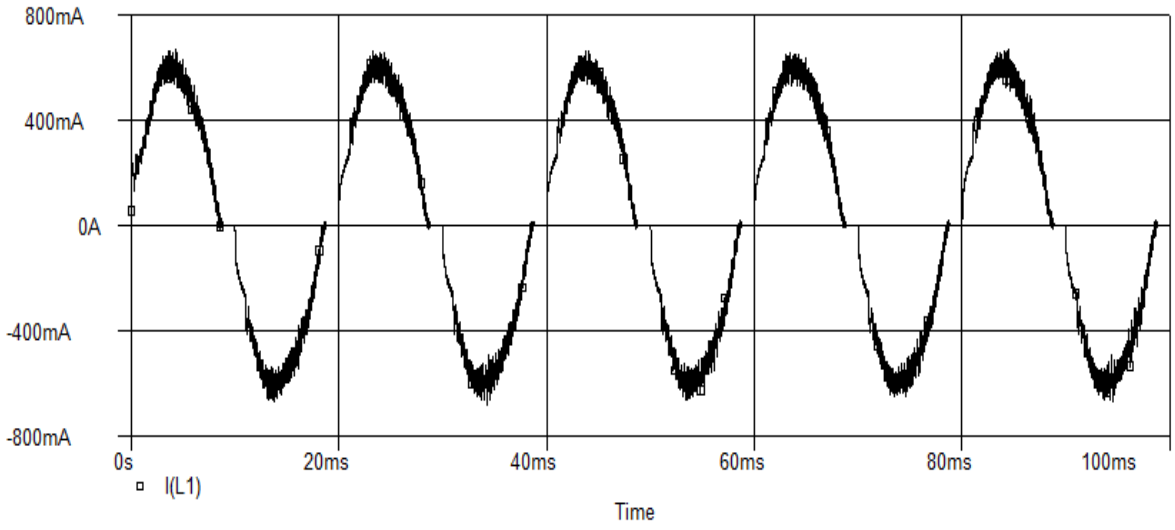

Fig 4.15: Simulated input line current of the proposed VF ballast with configuation-3.

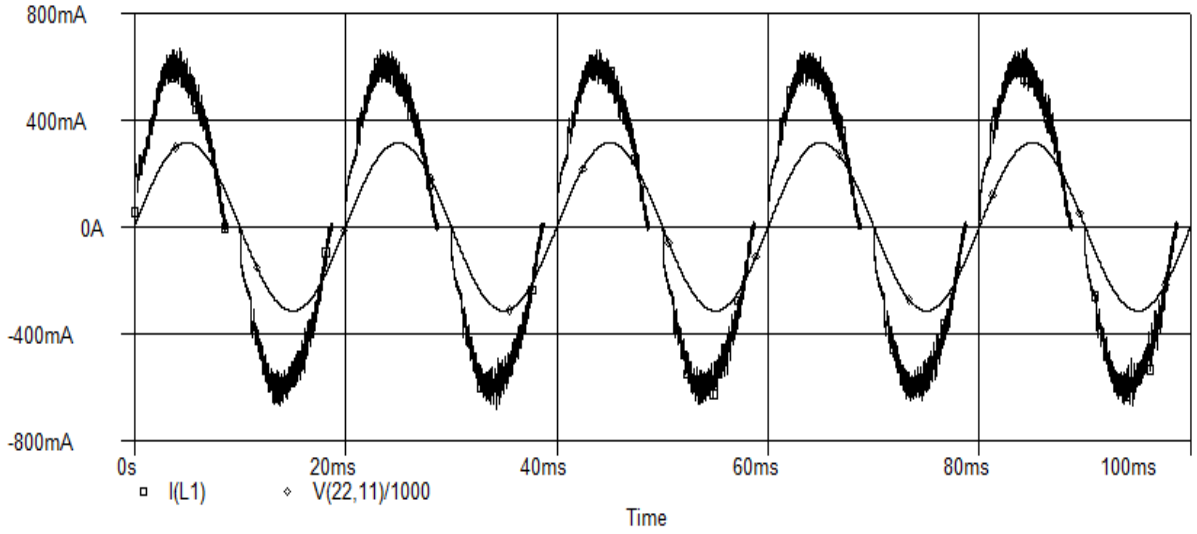

Fig 4.16: Simulated input line current and input voltage of the proposed VF ballast with configuration-3.

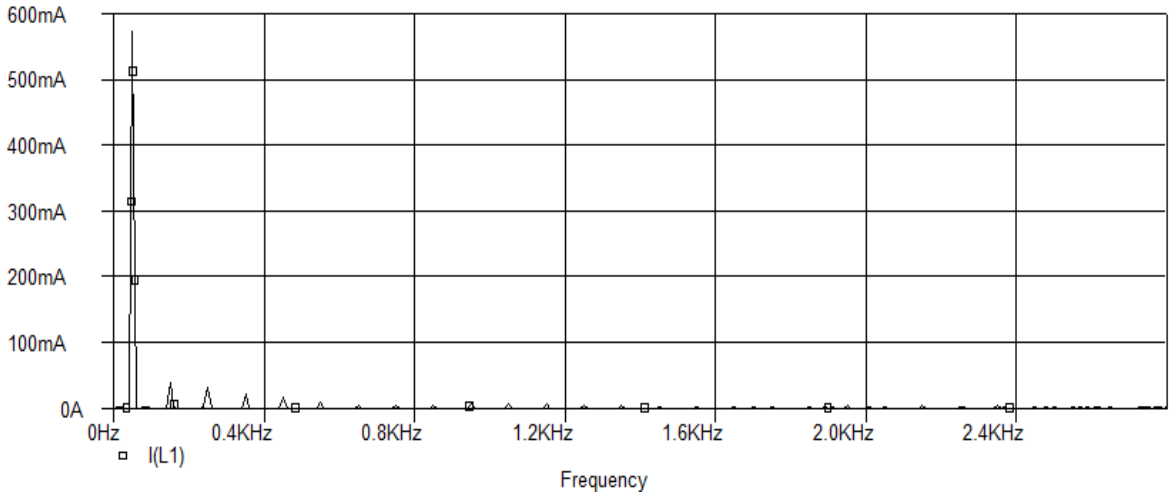

Fig 4.17: Simulated input current THD of the proposed VF ballast configuration-3.

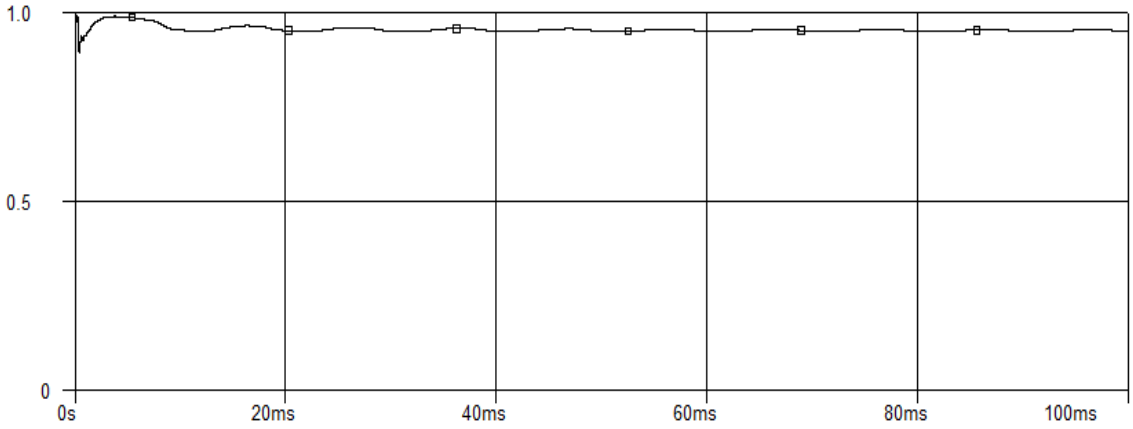

Fig 4.18: PF of the proposed VF ballast configuration-3.

4.3 THD Calculation for each configuration

It is possible to calculate the THD index of each line current waveform according to equation (4.1)

$$THD\ (\%) = \frac{\sqrt{\sum_{n}^{\infty} I_{n(rms)}^{2}}}{I_{1(rms)}} \qquad (4.1)$$

The proposed circuit is simulated for each configuration and for each one the THD is calculated from the Fourier analysis of their current waveform using the above equation and they are listed in the following table 4.4.

Table 4.4: THD calculation of the proposed VF ballast circuit for the three configurations.

Harmonic	C3,C4=2uF, R11=R12=220 ohm		
	Configuration-1 C1,2=68uF, Lin=5.6mH, R13=50k	Configuration-2 C1,2=25uF, Lin=2.2mH, R13=50k	Configuration-3 C1,2=100uF, Lin=1.2mH, R13=20k
I1	357.97mA	359.536 mA	572.052mA
I3	7.87%	7.16%	6.9%
I5	5.99%	5.94%	5.57%
I7	4.04%	4.11%	3.8%
I9	3.19%	3.03%	1.91%
THD %	11.15%	10.62%	9.83%

4.4 Power Factor Calculation for each configuration

The PF for each configuration is calculated using the equation (2.9) illustrated in chapter 2.

Table 4.5: PF calculation of the proposed VF ballast circuit for the three configurations.

Configuration	Power Factor
Configuration-1	0.993
Configuration-2	0.994
Configuration-3	0.995

From the above calculation it is observed that the proposed VF ballast circuit with configuration-3 performs better whose input current THD is 9.83 % and PF is 0.995.

4.5 Efficiency

The efficiency of the proposed VF circuit is calculated to evaluate the performance. The circuit shown in Fig 4.14 is simulated to trace the output power where P_{out} = V(10)*V(10)/ R_L and then to trace the input power where P_{in} = AVG(I(L1)*V(22,11)). After that the efficiency is calculated by doing the ratio of output power and input power. The efficiency curve of the proposed VF circuit with the three configurations for different input voltage are shown in Fig. 4.19(a) 4.19(b) and 4.19(c).

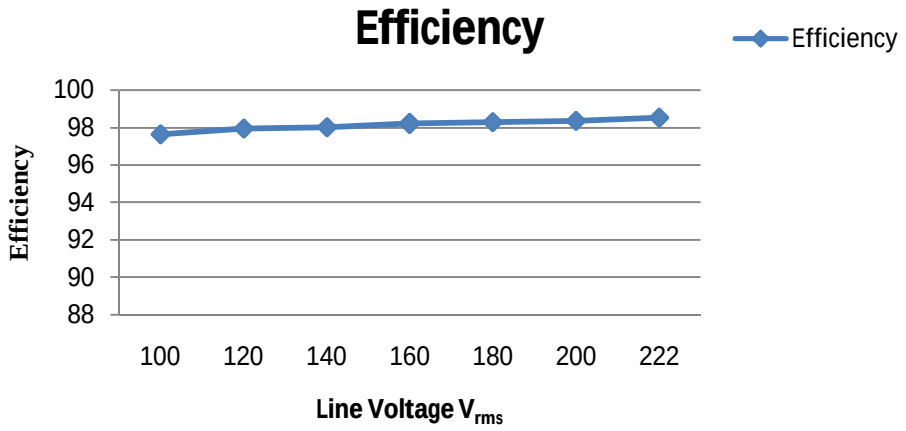

Fig 4.19(a): Efficiency VS line voltage for Configuration-1.

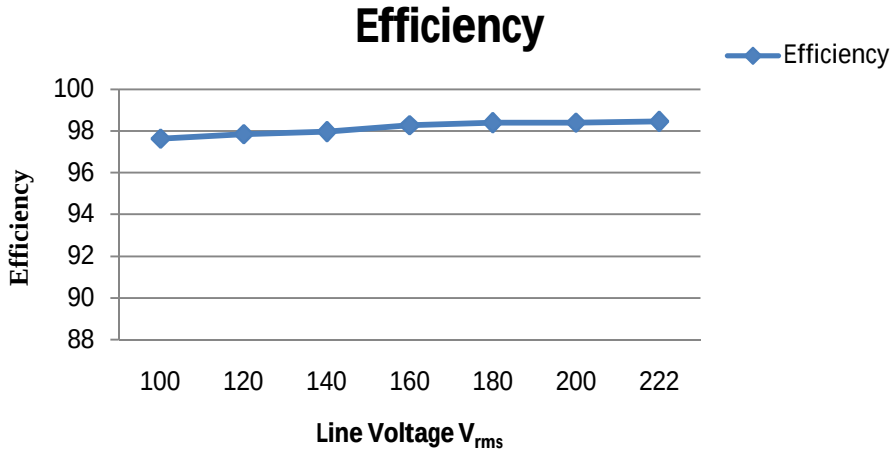

Fig 4.19(b): Efficiency VS line voltage Configuration-2.

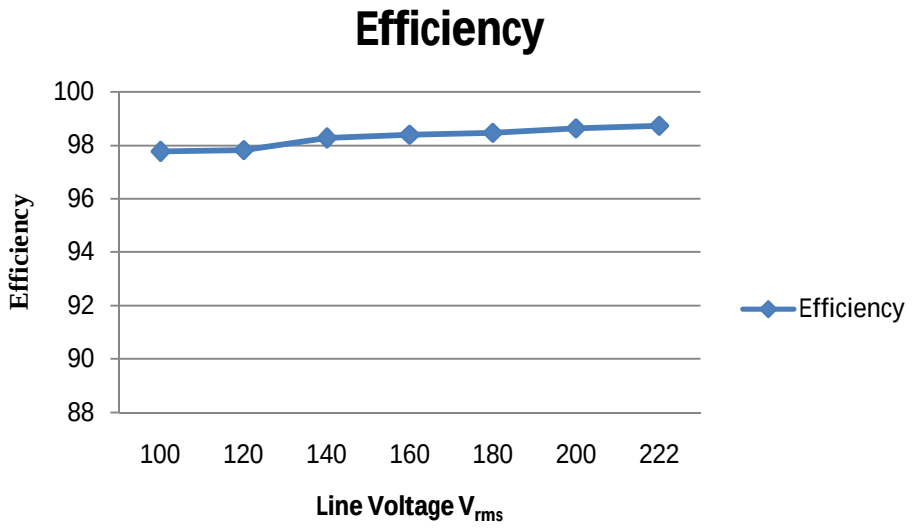

Fig 4.19(c): Efficiency VS line voltage Configuration-3.

The efficiency of the proposed VF circuit with configuration-3 is 98.79% and the efficiency of the resonant inverter is 53.56%. So the overall efficiency is 52.91%. The simulated efficiency for configuration-3 is shown in Fig. 4.20.

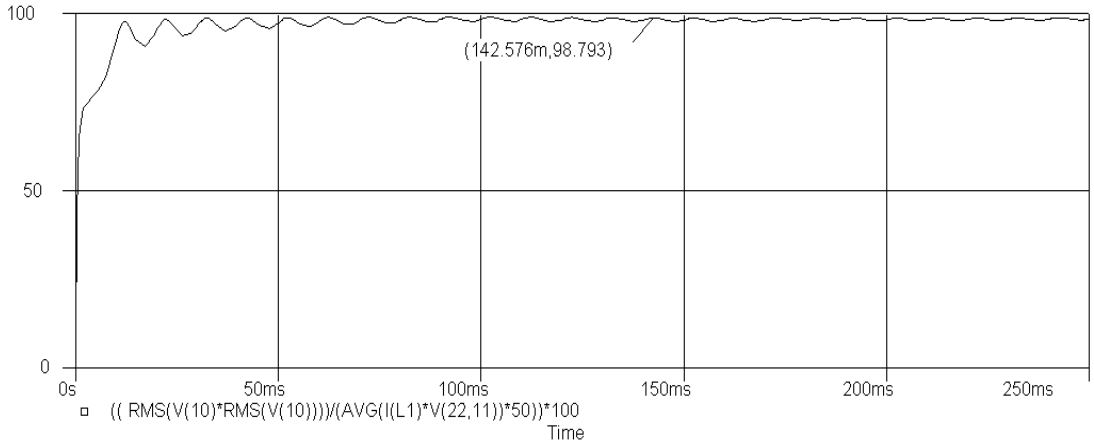

Fig 4.20: Simulated efficiency of the proposed VF circuit with Configuration-3.

Chapter 5

Practical Implementation

5.1 Practical Implementation of the Proposed VF circuit

In this work, the basic VF circuit is modified by four different schemes and their performances have been analyzed. Among them, the circuit giving the best result is chosenfor practical varification. This proposed modified VF circuit is experimentally verified through a laboratory prototype with all the components listed. Then the experimental waveform and the simulated waveform of the input current and input current FFT are compared.

The circuit diagram of the proposed VF circuit and the picture of the circuit constructed in laboratory are shown in Fig 5.1 and Fig 5.2.

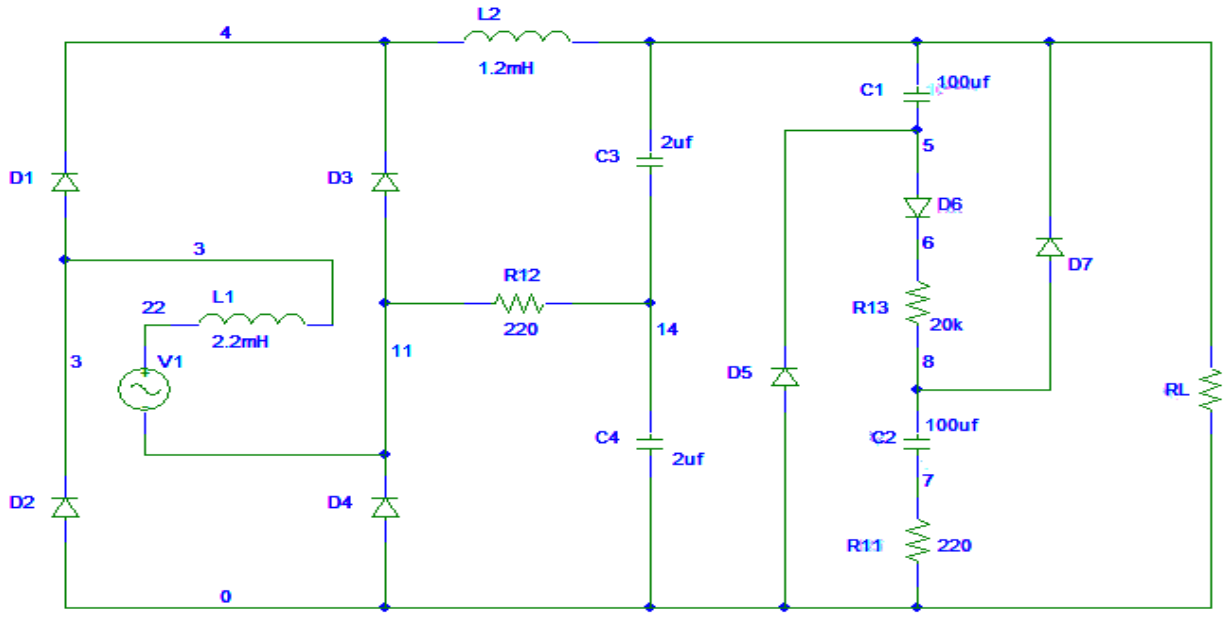

Fig 5.1: Circuit diagram of the implemented proposed VF circuit

Fig 5.2: Picture of the proposed VF circuit constructed in Laboratory

5.2 Comparison between experimental and simulated result

In the proposed circuit 50 ohm resistor has been used as a load which causes a high input current close to sinusoidal wave. But practicaaly it is difficult to find an 1.2mH inductor having such high current capability. So here firstly, a 350 ohmand secondly a 500 ohm resistor is used as load and the waveforms obtained experimentally and through simulation are captured and compared. The experimental and simulated waveforms are shown below. To obtain the current waveform in oscilloscope practically, a resistor of 2.4 ohm is connected in series with the supply and the voltage waveform acroos that resistor is taken which is actually the input current waveform.

5.2.1 Waveforms obtained considering a 350 ohm resistor as a load

The experimental and simulated input current waveform and simulated input current FFT and experimental voltage FFT are shown in Fig 5.3(a), Fig 5.3(b), Fig 5.4(a) and Fig 5.4(b) respectively.

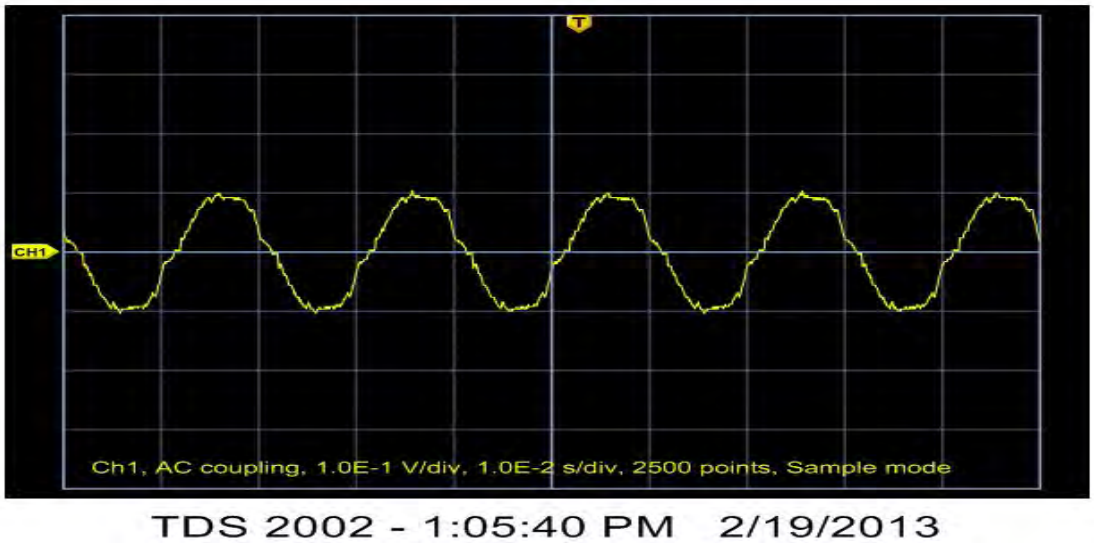

Fig 5.3(a): Experimental voltage waveform across the resistor

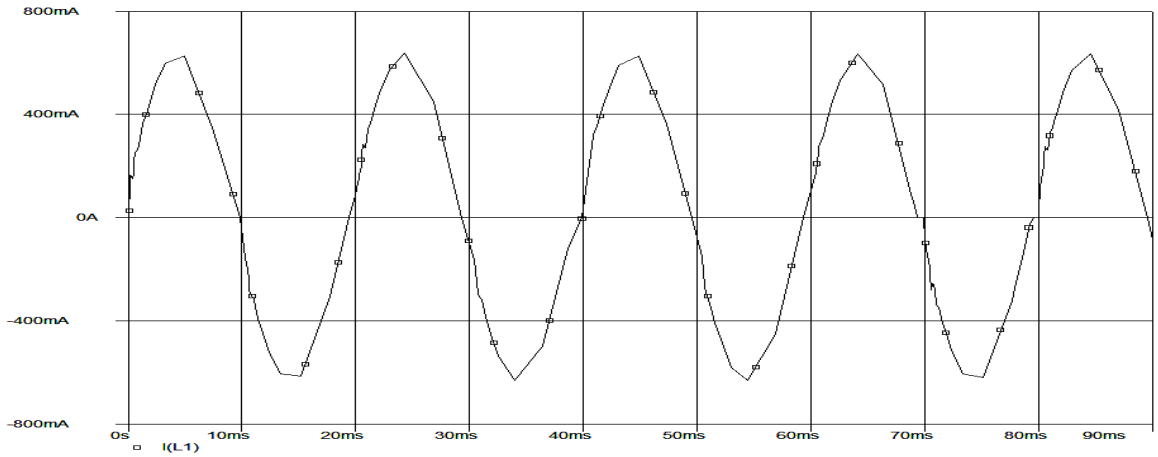

Fig 5.3(b): Simulated input current

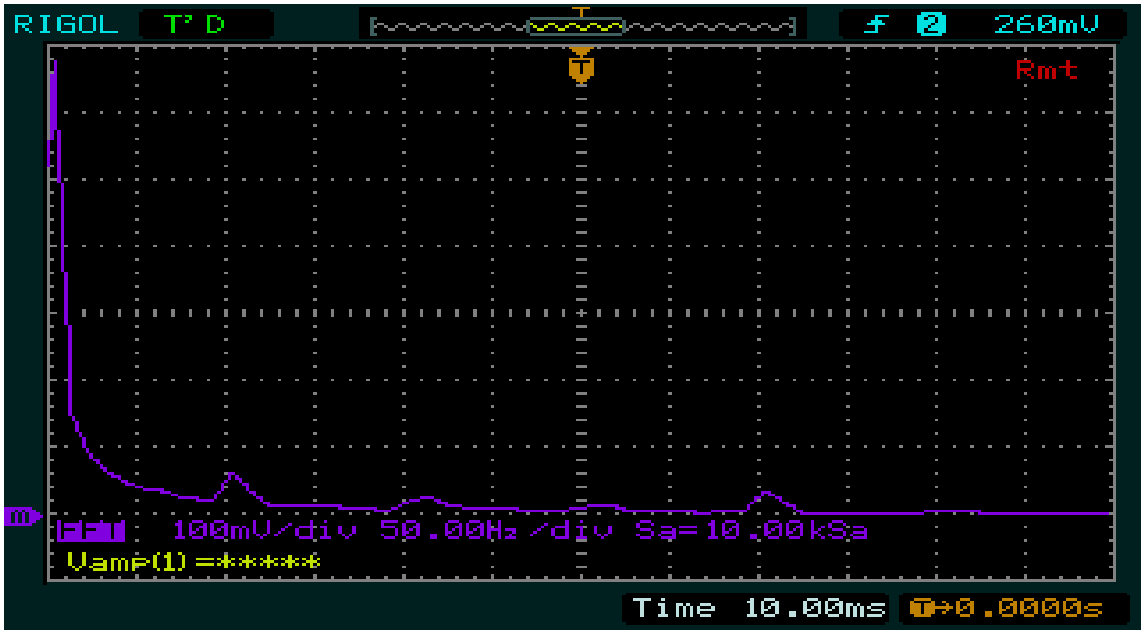

Fig 5.4(a): Experimental voltage FFT

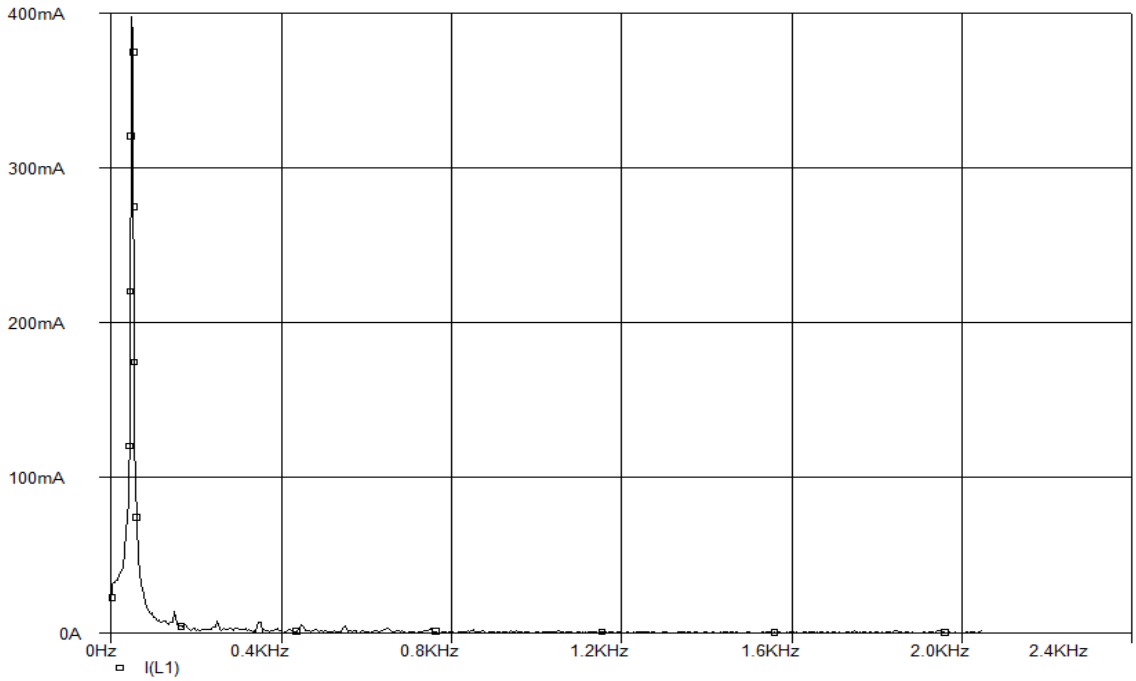

Fig 5.4(b): Simulated input current FFT

5.2.2Waveforms obtained considering a 500 ohm resistor as a load

The experimental and simulated input current waveform and simulated input current FFT and experimental voltage FFT are shown in Fig 5.5(a), Fig 5.5(b), Fig 5.6(a) and Fig 5.6(b) respectively.

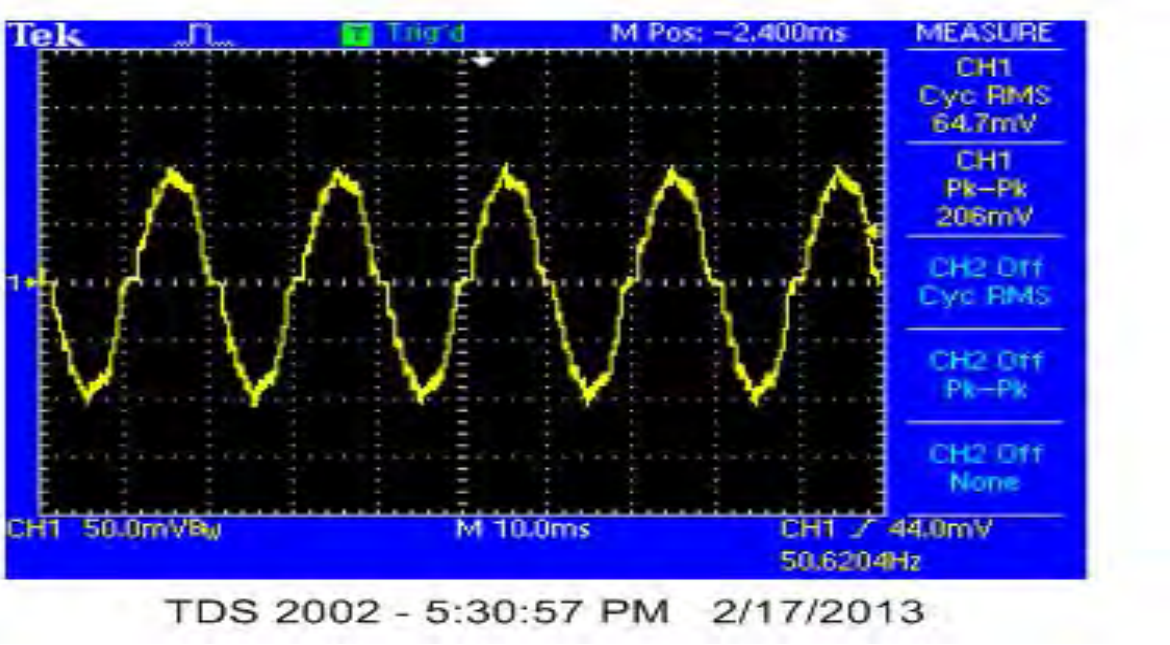

Fig 5.5(a): Experimental voltage waveform across the resistor

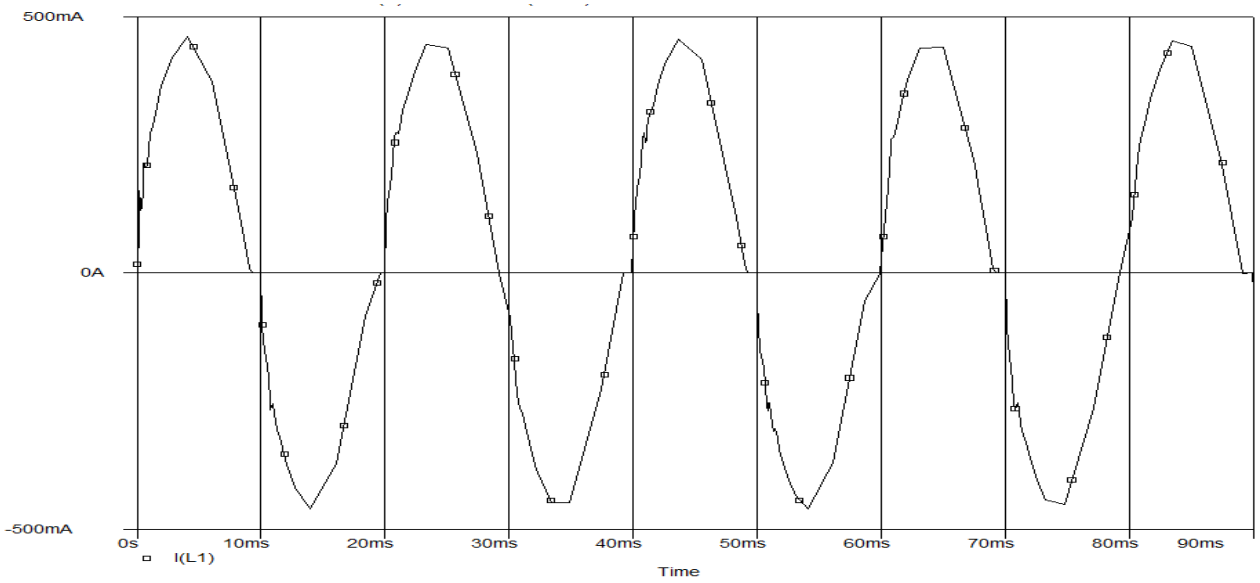

Fig 5.5(b): Simulated input current waveform

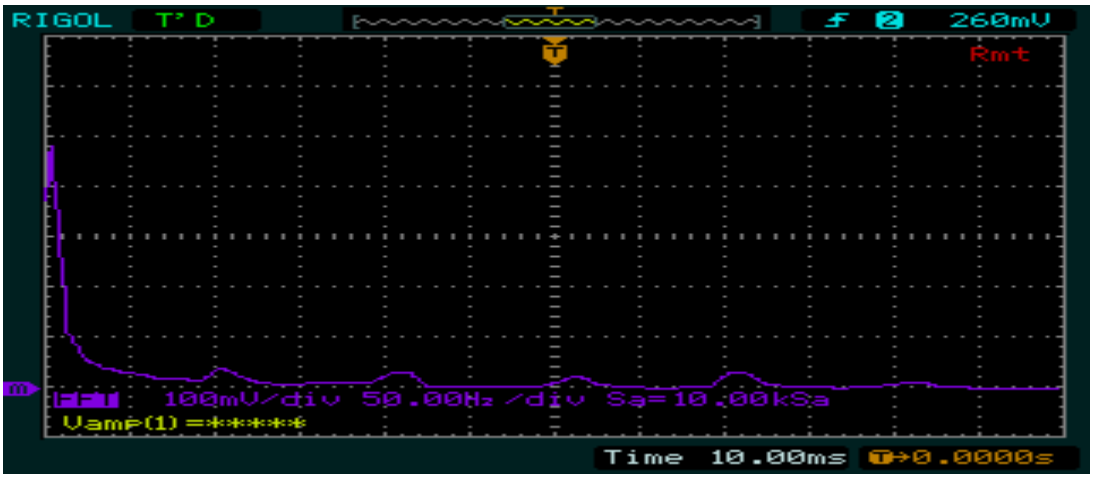

Fig 5.6(a): Experimental voltage FFT

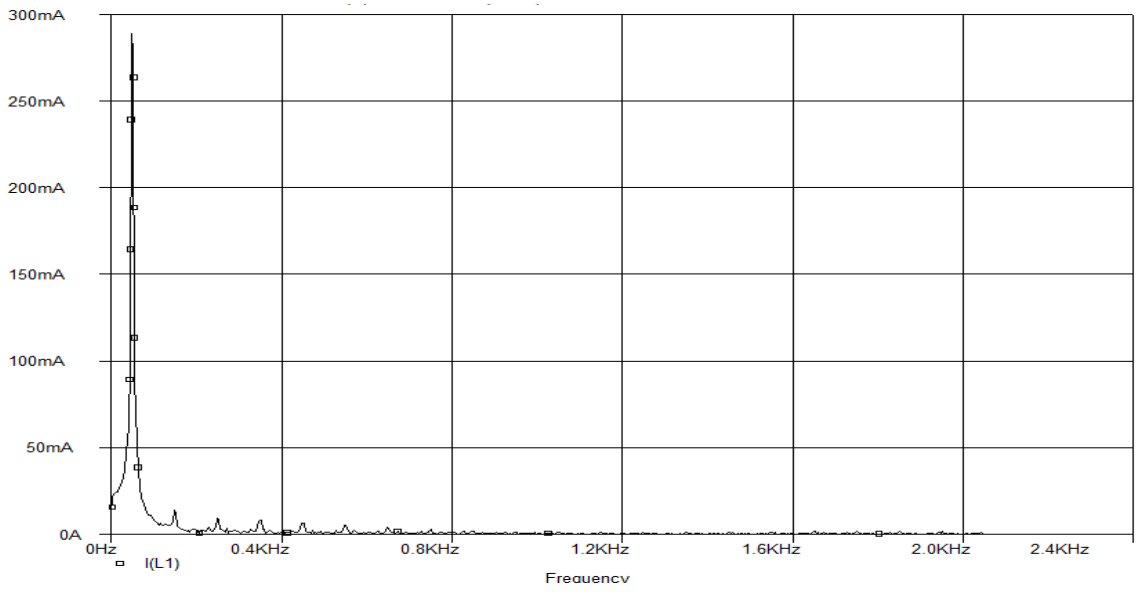

Fig 5.6(b): Simulated input current FFT

5.3 Efficiency Calculation

Experimentally the output voltage and input voltage for each load are measured and then from the ratio of output voltage and input voltage the efficiency is calculated. Using software, the circuit is simulated to trace the output power where P_{out} = V(10)*V(10)/ R_L and then to trace the input power where P_{in} = AVG(I(L1)*V(22,11)). After that the efficiency is calculated by doing the ratio of output power and input power.

Table 5.1: Experimental and Simulated Efficiency

Load	Result	Efficiency
500 ohm	Experimental	93.88
	Simulated	96.49
350 ohm	Experimental	91.67
	Simulated	94.71

5.4 Discussion

From the above waveforms it is observed that the experimental waveforms are almost similar to the simulated waveforms. From Table 5.1, it is observed that there is a small difference between the efficiency obtained experimentally and through simulation. Therefore it is varified that the proposed VF circuit gives better performance both practically and through simulation.

Chapter 6

Conclusion

6.1 Summary

Fluorescent lamps have drawn the attention of utilities and consumers due to their high energy efficiency and long life. However, due to their highly distorted current waveforms and low power factor, it is necessary to investigate their harmonic impact, particularly when there is widespread deployment in large numbers in the electrical network. So line current harmonic reduction is needed by some technique known as power factor correction. Power factor correction counter balances the unwanted effects of electric loads that create a power factor less than one.

Active and Passive power factor correction methods were discussed and compared through their performances, advantages and disadvantages. Active methods suffered from complexity, less efficient, voltage stress and conduction loss etc. On the other hand passive methods based on filters uses heavy and bulky reactive components. One example of passive method is Valley-fill circuit.

Passive Valley-fill ballast circuit and its modification were selected as power factor correction method. Because by this method the drawbacks of active methods can be overcome and it is simple and cost effective. The VF circuit was modified with four different schemes to evaluate the effect of different circuit components on power factor and harmonic distortion and to obtain the better performance each one was simulated with ORCAD PSPICE 9.2. The modified VF ballast with extended conduction angle and reduced line current THD was proposed to combine with a current fed resonant inverter as a power circuit. The proposed VF was capable of lowering the output capacitor voltage of the VF circuit; as a result the conduction time of the line current was extended. By the proposed modified VF circuit the harmonics contents were also removed and almost sinusoidal current wave shape was obtained. This modified VF circuit was designed with three configurations and analyzed. A comparative study was done among these three configurations through simulation to obtain a suitable design for the modified VF circuit which will enhance the performance of the Valley-fill electronic ballast. Brief analysis of the modified VF circuit, suitable design and simulation results were presented in this thesis.

6.2 Future work

In this work all the performance were analyzed with the resistive load only. Rather the output variations were checked for a certain range of operation. There are several opportunities for future work as,

- To study and analyze the performance for reactive load
- To analyze further to overcome the high Crest Factor (CF) problem of the conventional VF ballast circuit.

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