ELECTROSTATIC CHARACTERIZATION AND BALLISTIC LIMIT EVALUATION OF HIGH ELECTRON MOBILITY TRANSISTORS (HEMTS) USING QUANTUM MECHANICAL APPROACH

by

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DECLARATION

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

Signature of the student

(Md Zunaid Baten)

APPROVAL CERTIFICATE

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ABSTRACT

The High Electron Mobility Transistor or the HEMT is one of the most promising candidates for next generation high speed, low-power logic applications. In the highly scaled regime of operation, characterization of HEMT requires full incorporation of quantum mechanical (QM) effects. In this work the electrostatic and transport characteristics are analyzed for the generic, delta doped and spacer layered types of two single channels, such as $In_{0.53}Ga_{0.47}As$ and $In_{0.70}Ga_{0.30}As$ HEMTs, and two multi-quantum-well (MQW) channels, namely $In_{0.70}Ga_{0.30}As$ and InAs MQW HEMTs. The study shows that though delta doping increases the carrier density, on-state current and channel conductance of single channel HEMTs, it has negligible influence on the performance of MQW HEMTs. On the other hand, the addition of spacer layer decreases carrier density, drive current and channel conductance for all variants of the device. Evaluation of transport issues however shows that spacer layer can increase the mobility of HEMTs both in the long and short channel limits by reducing scattering. This work also presents a novel extraction method of the voltage at which parallel conduction initiates in highly scaled HEMTs. This entirely quantum mechanical technique defines two deterministic parameters V_{Emin} and Q_{ratio} for each device. Comparison of these parameters indicates that stronger the quantum mechanical confinement, higher the voltage for the onset of parallel conduction. For this reason in InAs MQW HEMT, which has the deepest quantum well, parallel conduction occurs at above 0.25V whereas in the $In_{0.53}Ga_{0.47}As$ HEMT it occurs at above 0.10V. Also with the onset of parallel conduction, the channel conductance in MQW HEMT can decrease by more than a factor of 1.5 whereas for single channel HEMT the conductance remains almost constant. However the MQW structure is found to reduce mobility of the HEMT in the short gate length limit. Nevertheless the mobility in all types of HEMTs is ballistic for up to 100 nm gate length, whereas in highly scaled Si devices the value is around 20 nm. The study shows that the strong confinement of MQW HEMTs, particularly of InAs MQW HEMT, causes the charge density, on-state current and channel conductance to be higher than other HEMTs at least by a factor of 1.20. Finally analyses of strain effects show that charge density, current and channel conductance are overestimated if strain is neglected in highly scaled HEMTs. Strain however can increase the mobility of the device in the short gate length limit, which is in accordance with the technology of strain enhanced channel materials like SiGe, Ge, SiN and GaAs.

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CHAPTER 1

INTRODUCTION

1.1 Preface

Advancement in the field of nanotechnology and microelectronics has allowed the semiconductor industry to be in accordance with the Moore's law for more than half a century. Scaling of CMOS technology has advanced relentlessly from a line width of over 1000 nm to the current 35 nm and as projected by International Technology Roadmap for Semiconductors (ITRS), device gate length of around 10 nm should be commercially available by the year 2016 [1]. However traditional geometric scaling of conventional silicon devices poses challenges in the form of excessive gate leakage current, increasing source–drain access resistance, carrier-mobility degradation, exponentially rising source to drain leakage and device-to-device variations [2]. These inherent limitations of conventional silicon based transistors have fuelled the exploration of both novel device structures and alternate semiconductor materials so as to bolster the continuation of Moore's law for over the next 15 years [3]. Transition from planar to non-planar multi-gate structures [4], incorporation of high-K/metal-gate stacks [5] and strained silicon technology [6] have played important roles in improving short channel performances and enhancing scalability. However the inherent low mobility of silicon necessitates consideration of alternate higher mobility materials like Ge, strained-SiGe (s-SiGe), strained-Ge (s-Ge), III-V materials like GaAs, InAs, InSb [7] and III-nitride materials like GaN, InN [8].

Over the recent years, a number of alternate substrate transistors like In rich InGaAs MOSFETs [9], InSb Quantum well FETs (QWFETs) [10], InSb and InAs Nanowire FETs [11], III-V double gate and silicon-on-insulator (SOI) MOSFETs [12] and High Electron Mobility Transistors [13]-[18] have been reported by researchers to obtain higher on-state current and reduced short channel effects. Among these next generation devices, one of the most promising candidates for high speed, low-power application is the High Electron Mobility Transistor or HEMT. The unique feature of this device is its heterostructure, in which the wide bandgap material is doped but the narrow bandgap material is kept undoped so that carriers do not have to encounter any impurity scattering when they diffuse into the undoped narrow bandgap region to form channel.

Consequently carrier mobility is significantly higher in HEMT devices compared to other transistors. This enhanced mobility promises HEMT to be one of the most prospective candidates for high-speed, low-power logic applications beyond Si-CMOS technology in the years to come [13]-[18].

The first commercially available HEMT was fabricated using GaAs as the narrow bandgap channel material and AlGaAs as the wide bandgap barrier layer [13]. Since then, major development efforts on HEMT have been on the channel materials which can further improve the electron mobility. Various III-V and III-Nitride compounds have been considered in this regard, which include GaAs, InAs, InGaAs, GaN, InN [13]-[18]. For each of these channel materials, a corresponding wide bandgap barrier layer can be used. If this wide bandgap material and the channel layer are lattice matched, then the channel layer of the HEMT remains unstrained. However HEMT structures having lattice mismatched layers are fabricated as well by using a sufficiently thin layer of one of the materials such that the crystal lattice simply stretches to fit the other material. Such HEMT structures, where the thin epitaxial layer is strained, are more commonly known as pseudomorphic HEMTs or p-HEMTs. Another type of HEMT fabricated using lattice mismatched materials is the metamorphic HEMT or m-HEMT where a thick buffer layer of graded composition is grown on the substrate. In this case the thick buffer layer allows the lattice constant to change gradually, from the substrate to whatever required for the subsequent growth of the channel layer. This ensures that all the dislocations are contained within the buffer layer and the channel layer remains unstrained [19].

Over the recent years, numerous works have been dedicated to the analysis of all these different types of HEMTs from both experimental and theoretical point of views. In fact a great deal of enthusiasm about the prospect of HEMTs comes from the excellent logic characteristics that have recently been demonstrated with gate lengths as small as 30 nm [20]. In such highly scaled regime of operation, electrostatic and transport characterization of HEMT requires full incorporation of quantum mechanical (QM) effects. However the self consistent simulation technique, which is a well established approach to investigate the QM effects in highly scaled devices [21], is yet to be applied for comparative analysis of electrostatic and transport characteristics. Particularly the capacitance-voltage (C-V) characteristic, which is an important figure of merit for

HEMTs, is yet to be reported for HEMT structures by the self-consistent simulation approach. Another area yet unexplored is the comparative analysis of the ballistic limits of HEMT for material and compositional variation. It is well established that because of higher mobility, the III–V channelled device like HEMT should reach the ballistic limit at longer channel lengths than Si devices [22]. This calls for comparative study of the on-state current limit of HEMT structures with the variation of material, composition, dimension and process parameters.

1.2 Literature Review

The evolution of the commercial HEMT started in the late 1960s from the research work on GaAs-AlGaAs superlattice by Leo Esaki and Ray Tsu at the IBM Thomas J. Watson Research Center. Carrier transport parallel to the layers of a superlattice was first considered by them in a work presented in 1969 [23]. The development of MBE and MOCVD technologies in the 1970s made heterostructures, quantum wells, and superlattices practical and more accessible. Consequently Dingle et al. were able to demonstrate enhanced mobility in the AlGaA/GaAs modulation-doped superlattice for the first time in 1978 at the Bell Laboratories [24]. This superlattice consisted of many alternate thin layers of n-type AlGaAs and undoped GaAs. It was observed that when electrons supplied by donors in the AlGaAs layers moved into the GaAs potential wells, they suffered less ionized donor scattering and could achieve higher mobility. Similar effects were observed by Stormer et. al in 1979 for a single AlGaAs/GaAs heterojunction [25]. However the works conducted till then were made on two-terminal devices, which lacked the control of a gate. This effect was first coined in by Mimura et al. in 1980 when he brought forth a new field-effect transistor with selectively doped GaAs/n-AlGaAs heterojunctions [26]. This was in fact the first demonstration of the depletion-mode HEMT. In this HEMT the entire AlGaAs layer was depleted and the electron accumulation layer remained at the interface. Later in the August of 1980, an enhancement-mode HEMT was also demonstrated by Mimura et al. [27] In this HEMT an electron accumulation layer was induced at the interface when positive gate voltage higher than the threshold voltage was applied.

The HEMT structures demonstrated by Mimura and his group were the ‘normal’ HEMT structures as the doped AlGaAs layer was grown on top of the undoped GaAs layer in these devices. In August 1980, Delagebeaudeuf et al. at Thomson-CSF, Orsay, France

reported the first 'inverted' HEMT structure, where the undoped GaAs channel layer was grown over the doped AlGaAs layer [28]. Later upon comparison of different bipolar-like and FET-like devices, the HEMT was referred to as a very promising candidate for high speed logic by Solomon [29]. Though popularly known as HEMT, the device came to be known as other names during its process of development at various laboratories. The formation of two-dimensional electron gas at the heterojunction gave it the name TEGFET (two-dimensionalelectron gas FET (France)). Because the doping is varied during the molecular beam epitaxial (MBE) growth of HEMT, it was also given the names of MODFET (modulation doped FET (University of Illinois, USA)) and SDHT (selectively doped heterojunction transistor (Bell Lab., USA)) [30].

Ever since the introduction of AlGaAs/GaAs HEMT, the major development effort has been on the channel material in order to further improve the electron mobility in the device. Channel materials having Indium (In) content gained much attraction of the research community in this regard. The ternary compound InGaAs was of particular interest because of its desirable energy bandgap range (0.36eV to 1.43eV), high electron mobilities (room temperature values of approximately $3x10^4$ $cm^2/V\text{-}s$) and high saturated electron drift velocities [31]. However an inherent advantage of the AlGaAs/GaAs system is that $Al_xGa_{1-x}As$ is latticed matched to GaAs over the entire compositional range, which allows the formation of high-quality heterojunctions free of misfit dislocations, whereas such dislocations are prevalent in the lattice-mismatched pairs of InGaAs/GaAs or InGaAs/AlGaAs. To this end came the concept of pseudomorphic HEMT. It had been reported earlier that if a lattice-mismatched layer is grown sufficiently thin, the mismatch is accommodated entirely as elastic strain [32]. In this situation the interface between the materials is essentially free from misfit dislocations and the thin layer is called pseudomorphic. This suggested that systems other than the AlGaAs/GaAs could be useful for novel HEMTs provided that only a thin layer of one of the materials is used. From this perspective, $In_{0.15}Ga_{0.85}As$/GaAs and $In_{0.15}Ga_{0.85}As$/AlGaAs pseudomorphic HEMT devices were reported in [33]. The device was fabricated using 20nm pseudomorphic epitaxial layer of $In_{0.15}Ga_{0.85}As$ and it offered better performances compared to the previously reported non-pseudomorphic HEMT in [31]. An additional advantage of the InGaAs/AIGaAs HEMT over the conventional GaAs/AlGaAs HEMT is that similar conduction band discontinuities

between the lower band-gap material and the AlGaAs can be realized with a much lower mole fraction in the $Al_xGa_{1-x}As$, thus ensuring that persistent photoconductivity effects and uncontrollable threshold voltage shifts associated with high mole fraction (x > 0.2) are eliminated or greatly reduced [33].

Indium rich materials such as $In_xGa_{1-x}As$ have been pursued instead of GaAs because of its smaller effective mass and larger ΔE_c arising from the smaller bangap. Also the higher satellite band of In rich material results less transfer-electron effect that degrades the mobility. These advantages are found to be directly related to the indium content: the higher the In percentage, the higher the performance. However a constraint of the GaAs substrate based p-HEMT is that it can accommodate a maximum of 25% In to avoid misfit dislocations [19]. Thus GaAs became unsuitable as substrate material for high indium concentration HEMT structures. Within this line of research, it was reported that InAlAs and InGaAs having around 50% In content can be lattice matched to InP, and they can thus be used as high bandgap and low bandgap material, respectively, in the HEMT structure [34].

Mishra et al. reported that $In_{0.52}Al_{0.48}As$- $In_{0.53}Ga_{0.47}As$ HEMT grown lattice matched on InP can be a superior alternative to the GaAs based HEMT. The large conduction band discontinuity coupled with the high doping efficiency of Si in AlInAs establishes a larger 2DEG density (above 3 x 10^2 cm^{-2}) in the $In_{0.52}Al_{0.48}As$- $In_{0.53}Ga_{0.47}As$ system. Also excellent electron mobility (above 10,000 cm^2 V^{-1} s^{-1}) and peak velocity give high transconductance and excellent high frequency performance [35]. Even better high frequency performance was obtained in the InP based pseudomorphic $In_{0.52-u}Al_{0.48+u}As$/ $In_{0.53+u}Ga_{0.47-u}As$ HEMT which allowed even higher In content in the channel material [36]. In fact InP based p-HEMTs having In content as high as 81% can be obtained as well if the InAlAs layer of the InAlAs /InGaAs/InP system is replaced by InP. This InP/InGaAs/InP p-HEMT has been reported as a promising alternative to the previously proposed InAlAs /InGaAs/InP system in terms of both DC and RF characteristics [37]. A comparison of GaAs and InP substrate based devices show that lower cost per chip occurs for GaAs based devices because of cheaper substrate. However the performance of these devices is often limited by the amount of indium composition (less than 25%). On the other hand, InP-based devices offer better high frequency performance as they

can incorporate indium composition higher than 53% [38]. So far the largest reported diameter of InP substrate is 150 mm [39].

To combine the advantages of low-cost and manufacturability of GaAs substrates and the high performance of InP-based devices, the metamorphic growth technology was incorporated for HEMT devices, thereby introducing the metamorphic HEMT or m-HEMT. G. Wang et al. from Cornell University successfully fabricated a 0.12µm m-HEMT using a 1.8µm thick InAlAs/InGaAs superlattice buffer layer [40]. However, due to the poor buffer layer quality, the performance of the device was limited. First successful realization of submicrometer InAlAs/InGaAs m-HEMT having 30% In content was reported by Win et al. in 1993 [41]. The reported device presented several advantages over booth conventional pseudomorphic HEMT on GaAs and over lattice matched HEMT on InP. Higuchi et al. supported this claim by reporting the first high performance InAlAs/InGaAs HEMT on GaAs exceeding that on InP [42].

Since the technology of metamorphic HEMT gained maturity, efforts have been on the improvement of DC and RF performances by introducing structural and/or compositional modification. In 1995, Chertouk reported a higher performance m-HEMT having composite channel, which consisted of 12 nm InGaAs with In content of 0.52 on top of 20 nm InGaAs with an In content of 0.32. This device, which combined the superior transport capability of $In_{0.52}Ga_{0.48}As$ and low-impact ionization property $In_{0.38}Ga_{0.68}As$, demonstrated both excellent DC characteristics and high frequency performances [43]. Only depletion mode m-HEMT devices were reported until 1999, when Eisenbeiser et al. presented the first enhancement mode (e-mode) m-HEMT. This device, which had enhancement mode $In_{0.5}Al_{0.5}As/In_{0.5}Ga_{0.5}As$ metamorphically grown on GaAs, offered good dc and RF performances with 0.6µm gate length [44]. In another work, both enchancement and depletion type $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}$ m-HEMTs were reported to show excellent DC and high frequency characteristics for a gate length of 0.3µm [45]. Still the enhancement mode HEMT is considered advantageous in the sense that it does not require a negative gate bias and, if integrated with depletion-mode (D-mode) HEMTs, can simplify many circuit designs.

Though metamorphic HEMT allows the increase of indium percentage in the channel material, the small bandgap of InAs makes high indium-content devices very susceptible to the phenomena of impact ionization, which in effect results serious kink

effect and low breakdown voltage of the In rich HEMT device [46]. So a high mobility wide bandgap channel material is much needed to continue the ongoing performance enhancement of HEMTs. The materials which gained much interest of the research community in this regard were the nitride semiconductors. The nitride semiconductors, particularly GaN is found to have the unique features of large bandgap (3.4eV), high critical breakdown electric field (greater than $3MVcm^{-1}$) and high electron mobility (typically in the 1500–2200 $cm^2V^{-1}s^{-1}$ range at room temperature) [47]. Another very unique property of nitride-based semiconductor compared to GaAs system is the existence of strong intra-crystal polarization field. As reported in [48], because of the non-central symmetry, nitrides exhibit a macroscopic spontaneous polarization field in the wurtzite lattice. In addition, a strain-induced piezoelectric polarization, which is much higher than that in the traditional III-V semiconductors, is also prevalent within the nitride heterostructures. Due to these strong polarization fields, a sheet carrier density of around 10^{13} cm^{-2} was reported at the AlGaN/GaN interface without any modulation doping [49]. Till now, the most popular model proposed by Ibbetson et al. suggests that with the electrostatic field induced by the polarization field in the AlGaN/GaN heterostructure, the band profile and the electron distribution are modified and a large number of electrons transfer from the donor-like surface states to the AlGaN/GaN hetero-interface, forming a 2 DEG [50].

Because of the unique features mentioned, the AlGaN/GaN appeared as a potential material for the fabrication of high voltage, high power and high frequency HEMT devices in the 1990s. With the successful growth of high-quality III-nitride epitaxial films by advanced metal-organic chemical vapor deposition (MOCVD) technique, the AlGaN/GaN heterostructure was demonstrated for the first time in 1991 [51]. Motivated by this success, the first functioning AlGaN/GaN HEMT was demonstrated by Khan et al. in 1993 [52]. Since then the device has showed promising characteristics for power generation at high frequency because of its high breakdown field and excellent transport properties. Modified versions of this HEMT have gained utility for power-switching applications [53], biological and chemico/physical sensors [54]-[55] and power amplification in cell-phone base stations [56].

Although AlGaN/GaN HEMTs have been studied extensively as ideal candidates for high frequency and high power applications, theoretical calculations show that

InAlN/(In)GaN HEMT performance should be superior because of expected higher two-dimensional electron gas (2DEG) density [57]. Moreover among the III-N materials, InN offers the lowest effective mass ($0.04-0.11m_0$ in comparison to $0.2m_0$ for GaN where m_0 is the free electron mass) and the highest maximum steady-state drift velocity of 5×10 m/s (in comparison to $3x10^5$ m/s for GaN) [58]. Though the growth of InN hetersostructures is still in the immature stage, it's being predicted that InN based HEMTs may provide record fast performance in the years to come [59].

Besides structural and material variation, studies have also been made on the performance evaluation of highly scaled HEMTs for beyond the Si-CMOS logic applications. It was reported in [60] that HEMTs which have extremely high electron mobility (around 10,000 cm^2/V-s at room temperature), should easily operate near the ballistic limit whereas the device performance of Si MOSFET is still 50% below the ballistic limit because of relatively low mobility of the inversion layer electrons (around 100 cm^2/V-s at room temperature). The theoretical work showed that nanoscale HEMTs can be modeled as an intrinsic ballistic transistor with extrinsic source/drain series resistances.

The first analysis on the suitability of aggressively scaled HEMT for high speed low power logic application was presented by Kim et al. [61] in 2005. The work, which made the first evaluation of 50 nm InGaAs HEMT as a potential logic technology, concluded that InAs-rich InGaAs HEMT holds considerable promise as an alternative to beyond CMOS applications. Later in 2007, 40 nm InAs HEMTs were also reported to demonstrate excellent logic performance and scalability [62]. However the following year it was reported that InGaAs HEMTs may reach a point of diminishing returns at sub 100 nm gate length if the InAlAs thickness is relatively high [63]. So the work suggested both vertical and horizontal scaling and showed that reducing the $In_{0.52}Al_{0.48}As$ insulator thickness results in much better electrostatic integrity and improved short-channel behavior down to a gate length of around 60 nm. Improved short-channel effects by scaling of the barrier thickness and the use of a thin channel was reported in the same year for 30 nm InAs pseudomorphic HEMT on an InP substrate using InAlAs as barrier layer [64].

In another work on scaled down HEMTs, simulation and experimental results of InAs/ InGaAs HEMTs having gate lengths ranging from 30-200 nm were been reported [20].

The work suggested that quantum capacitance will dominate in future scaled III-V transistors. Even more aggressive scaling (down to 15nm) of InGaAs HEMT was reported by Hwang et al., who highlighted the relevance of ballistic mobility in such short-channel devices [65]. It also reported that given the degradation of in performance of the conventionally scaled HEMTs, double gate HEMTs can offer better short channel performance. Similar modifications of conventional HEMT architecture have been reported in a very recent work by Kim et al. [66]. The work shows that by combining a thin InAlAs barrier and a thin channel containing a pure InAs sub-channel, excellent figure of merits can be obtained for InAs HEMTs scaled down to 40 nm gate length. Benchmarking of this device with state of the art Si-CMOS led to the conclusion that InAs is, indeed, a channel material with great potential for beyond Si CMOS logic applications

1.3 Objectives of the Work

Though numerous works have been conducted on the high-speed characteristics and frequency response of HEMTs over the last four decades, performance evaluation of this device for beyond Si-CMOS logic application has been considered relatively more recently. In this regard InAs and InGaAs HEMTs have gained much attention over the last few years [61]-[66]. Though numerous variants of these devices have been presented both from theoretical and experimental points of view, a comprehensive quantum mechanical (QM) analysis of the electrostatic and transport characteristics of highly scaled HEMTs with respect to structural, compositional and material variation is yet to be reported. From this perspective, this work aims to carry out the following tasks.

- Using self-consistent-analysis technique, to quantum mechanically study the electrostatic and transport characteristics of highly scaled HEMTs with respect to structural, compositional, and material variation.
- To compute C-V characteristics of the HEMTs using both the self-consistent simulation approach and the quantum capacitance model.
- To compute and compare the ballistic limits for different highly scaled HEMTs and also to evaluate their ballistic and effective mobilites.
- To investigate the strain effects on the electrostatic and transport characteristics of the HEMTs.

1.4 Outline of Methodology

In this thesis, to conduct a fully QM analysis, a coupled Shrödinger-Poisson solver has been developed for HEMTs having different channel materials and barrier layers. The coupled Shrödinger's and Poisson's equation has been solved self-consistently [21] to obtain electrostatic solutions for different gate biases. The Poisson's equation has been solved using the finite difference method to obtain the potential profile of the devices. To obtain the wave functions and eigen-states, the Shrödinger's equation is solved using Hamiltonian matrix formalism. To incorporate strain effects, the obtained energy band profiles are modified according to the two band k.p model calculation done in [67]. Incorporation of compound semiconductors in the channel or barrier layer of HEMTs necessitates appropriate determination of material parameters according composition of the semiconductor. These material parameters are evaluated using well established equations [68].

The self-consistently obtained electrostatic solutions will be used to determine the energy band diagram and carrier profile of each HEMT device. The variation of charge concentration with gate bias provides the C-V characteristics of the devices. Also the quantum capacitance model presented in [20] has been applied to evaluate and validate the C-V characteristics.

For transport characterization, the ballistic currents are measured using over-the-barrier-model [68], which was previously applied to evaluate the performance limits of Si MOSFETs. The channel conductance and ballistic and effective mobility for HEMTs having different channels and structures are also evaluated according to the definitions presented in [60].

1.5 Layout of the Thesis

Chapter 2 introduces the simulated device structures with illustrations. The device dimensions and the process parameters considered in this study are also mentioned in this chapter.

Chapter 3 at the beginning describes the self-consistent simulation technique with necessary equations. The modifications required to incorporate strain effects have also been presented here. Next the C-V characterization technique, which includes the quantum capacitance (QC) model, has been presented. Then the model for transport

characterization, which also includes the definition of ballistic and effective mobility, is discussed. Finally the models and formulations used in this study are validated using the QC model and with results reported elsewhere using simulation software Sentaurus.

Chapter 4 at first presents the electrostatic characteristics, which includes the energy band diagram, carrier profiles, eigen states, sheet carrier density and C-V profiles. Next the transport characteristics, which encompass current-voltage relations, channel conductance, ballistic and effective mobility, are described with illustrations. Finally the importance of incorporating strain effects is discussed with respect to both electrostatic and transport characteristics.

Chapter 5 draws the conclusion of this work. This chapter summarizes the findings of the study. It also puts forward suggestions regarding future scopes of works related to this thesis.

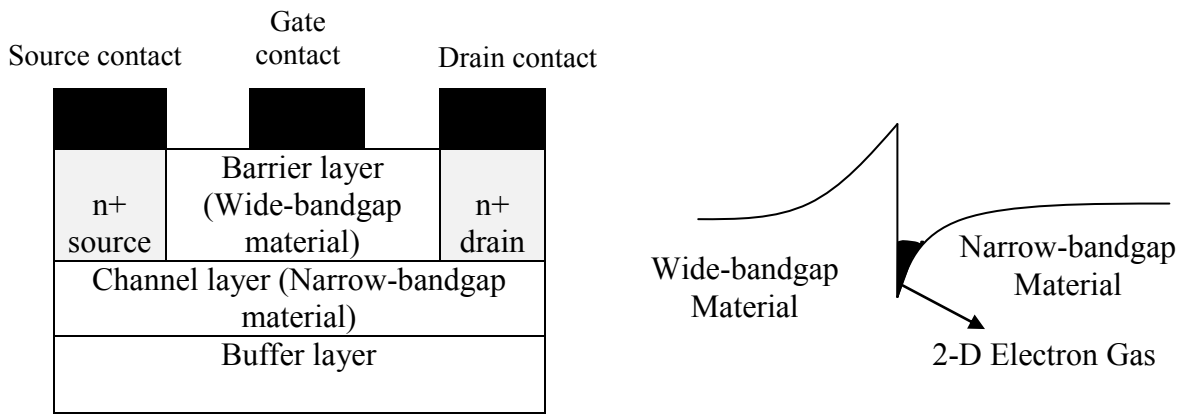
CHAPTER 2

THE HEMT STRUCTURES

In this chapter the basic HEMT structure and operations are discussed in brief with illustration. Next the simulated device structures of this study have been described with specifications. Different instances of the studied HEMTs have been presented here with device dimensions and process parameters. Finally a table has been presented at the end of the chapter to summarize the analyzed devices.

2.1 The Basic HEMT

The HEMT is actually a heterojuntion device which consists of a wide-bandgap and a narrow-bandgap material. The wide bandgap material is called the barrier layer whereas the narrow bandgap material is called the channel layer. The channel layer is epitaxially grown on a thick substrate which is normally called the buffer layer. The gate metal, which is deposited on the barrier layer, creates a Schottky barrier with the widebandgap semiconductor. The source and drain contacts on the other hand are ohmic contacts and are connected with the channel layer by highly doped regions. The basic HEMT structure is shown in Fig. 2.1(a).



(a) Basic HEMT (b) 2-D Electron Gas formation

Figure 2.1: The basic HEMT

The device HEMT is called modulation doped because here the wide bandgap barrier material is doped whereas the narrow bandgap region is kept undoped. Because a quantum well is formed at the hetero-interface of the two layers, the carriers from the barrier layer can easily diffuse into the narrow-bandgap region and thus form a channel layer. The net result of modulation doping is that channel carriers at the undoped heterointerface are spatially separated from the doped

region. Consequently these carriers do not experience any ionized impurity scattering and exhibit higher mobility. For this reason the HEMT is called a 'high electron mobility' device. The 2-D layer of electrons formed at the heterointerface is called 2-D electron gas (Fig. 2(b)).

Very often instead of uniform doping, a delta-doped charge sheet is used within the barrier layer close to the channel interface. This influences the electrostatic of the device such that the net channel carrier density and current driving capability increase. In another variant of the HEMT, a portion of the barrier layer near the heterointerface is kept undoped so that ionized impurities of the doped region cannot scatter the 2-D layer of carriers at the interface. This undoped region of barrier layer is called the spacer. The HEMT structures having delta doping and spacer layers are discussed in the next section.

2.1 Structural Variation

The three basic HEMT structures considered in this work are shown in Fig. 2.2.

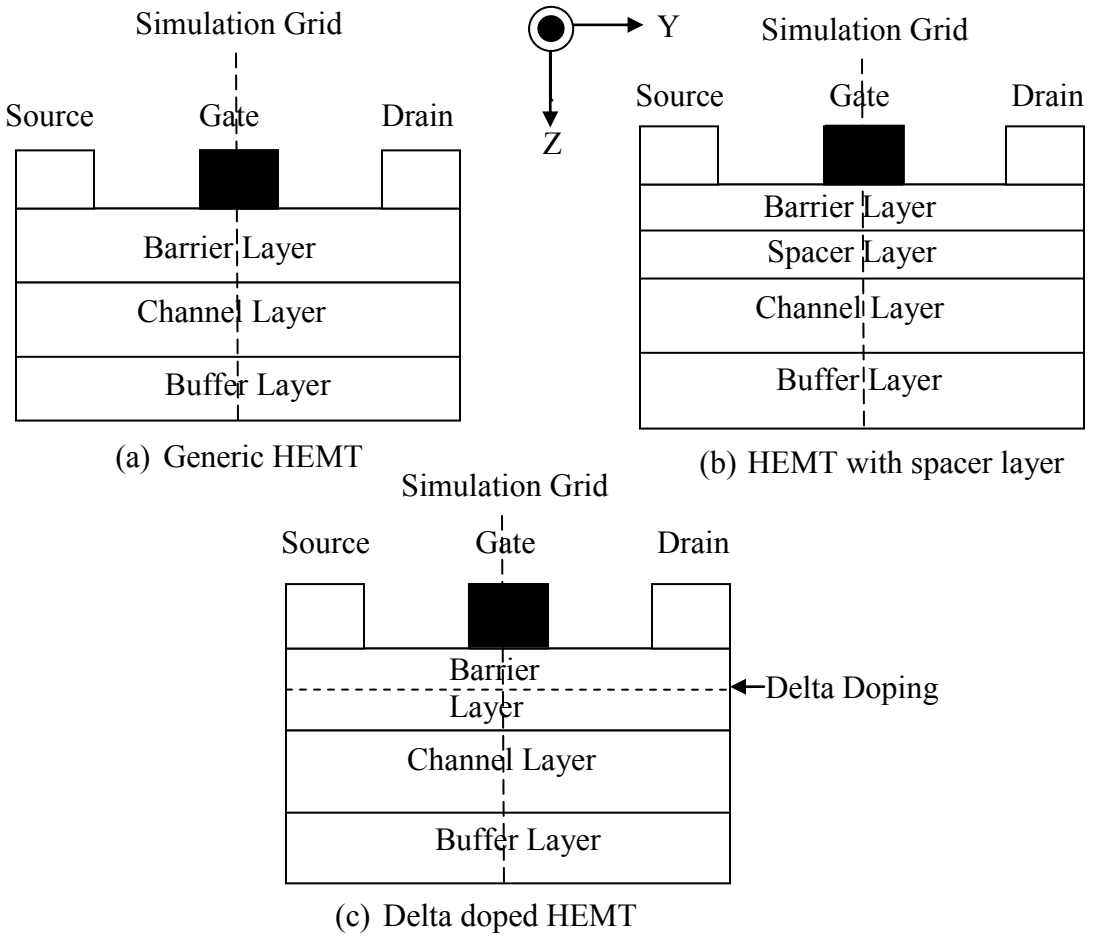


Figure 2.2: Three types of HEMT structures

The generic HEMT, which consists of a doped barrier layer, an undoped channel layer and the undoped buffer, is shown in Fig. 2.1(a). To ensure that dopants from the doped barrier layer do not diffuse into the undoped channel, an undoped spacer layer is added beneath the barrier as shown in Fig. 2.1(b). To study the effect of delta doping, a delta doped barrier layer is considered for the HEMT shown in Fig. 2.1(c). For 1-D simulation the grid line considered for all these structures is along the Z direction, which is perpendicular to the direction of transport. It should be mentioned that the figures showed here are not drawn to scale**.**

For all the structures shown in Fig. 2.1, the barrier and the buffer layers are of $In_{0.52}Al_{0.48}As$. The barrier doping concentration has been kept fixed at $5x10^{17}cm^{-3}$ throughout the study. For the delta doped structures, the delta doping considered is $5.5x10^{18}cm^{-3}$. The barrier layer thickness is 8nm and the spacer layer thickness is 3nm for the structures having spacer layers. For other structures, the barrier layer thickness is kept fixed at 11nm. The gate metal considered for all the structures is Platinum, which has a work function of 4.55eV. The buffer layer is undoped and it has been considered 100 nm throughout the study. This thick buffer layer serves to transform the lattice constant gradually, from that of $In_{0.52}Al_{0.48}As$ to whatever required for the growth of the subsequent channel layer. This ensures that all the dislocations at the channel-buffer interface are contained within the buffer layer and the channel layer remains unstrained [19]. The mentioned device dimensions and process parameters have been adopted in accordance with previously studied highly scaled HEMT structures [61]-[66].

2.2 Channel Content Variation

Besides structural variation, the impact of using different channel materials has also been studied in this work. Both single-material channels and channels formed of multiple materials, i.e. Multi Quantum Well (MQW) channels have been considered in this work. With respect to the channel material, the following four different cases have been considered.

Case1: 10nm thick $In_{0.53}Ga_{0.47}As$

Case2: 10nm thick $In_{0.70}Ga_{0.30}As$

Case3: 10nm thick MQW channel consisting of 2nm $In_{0.53}Ga_{0.47}As$, 5nm InAs and 3nm $In_{0.53}Ga_{0.47}As$

Case4: 10nm thick MQW channel consisting of 2nm $In_{0.53}Ga_{0.47}As$, 5nm $In_{0.70}Ga_{0.30}As$ and 3nm $In_{0.53}Ga_{0.47}As$

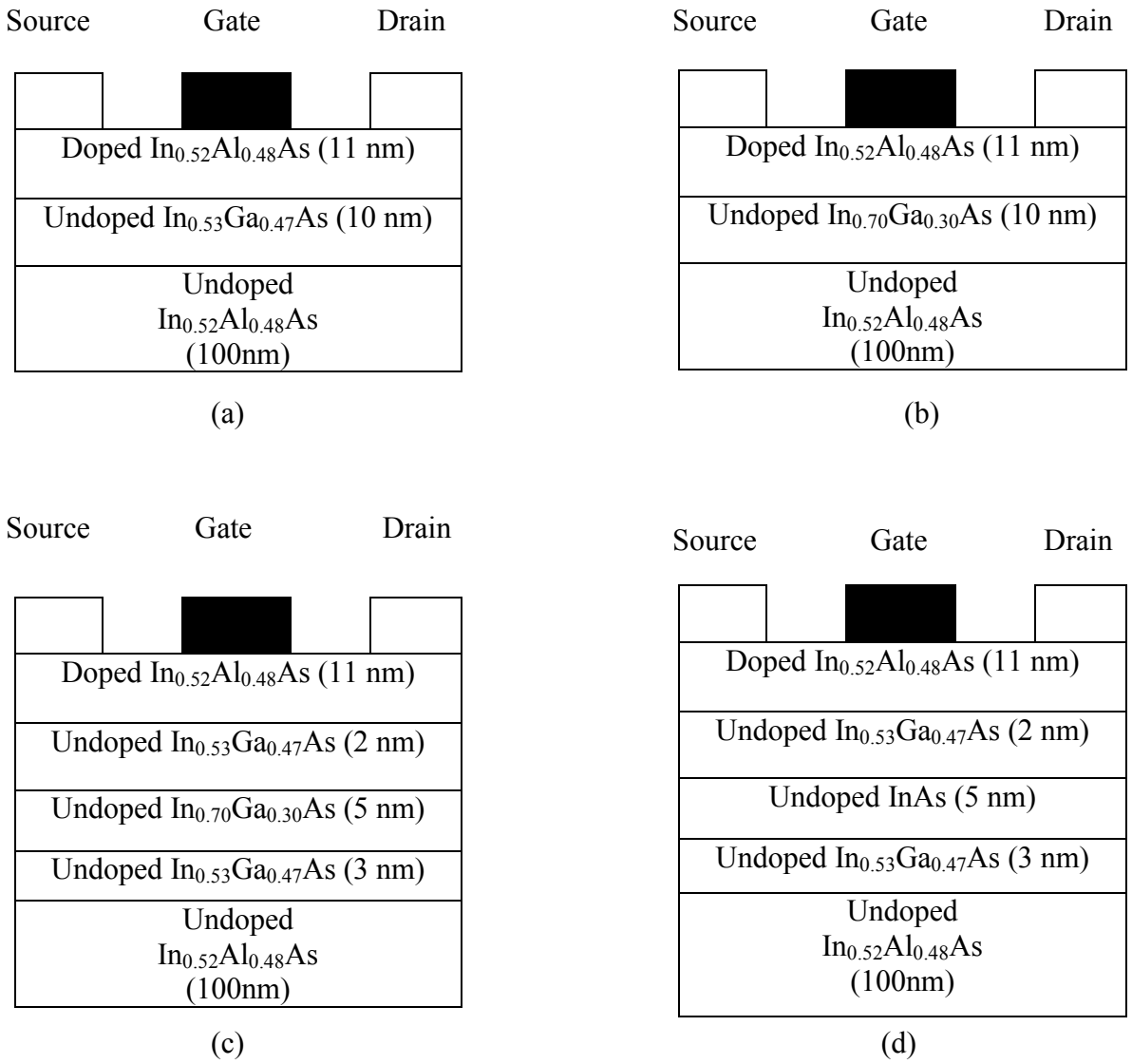


Figure 2.3: Generic (a) $In_{0.53}Al_{0.47}As$ channel, (b) $In_{0.70}Al_{0.30}As$ channel, (c) $In_{0.70}Al_{0.30}As$ MQW and (d) InAs MQW HEMTs

All the cases of the generic HEMT structure are shown in Fig. 2.2 with device dimensions. Here Fig. 2.2(a) and 2.2(b) present single-channel HEMTs whereas MQW HEMTs are shown in Fig. 2.2(c) and Fig. 2.2(d). The channel materials of the two single-channel HEMTs are $In_{0.53}Ga_{0.47}As$ (Fig. 2.2(a)) and $In_{0.70}Ga_{0.30}As$ (Fig. 2.2(b)) whereas the two MQW HEMTs contain $In_{0.70}Ga_{0.30}As$ (Fig. 2.2(c)) and InAs (Fig. 2.2(d)) in between undoped $In_{0.53}Ga_{0.47}As$. The MQW HEMT structures are in conformation with previously reported HEMT structures in [61]-[64].

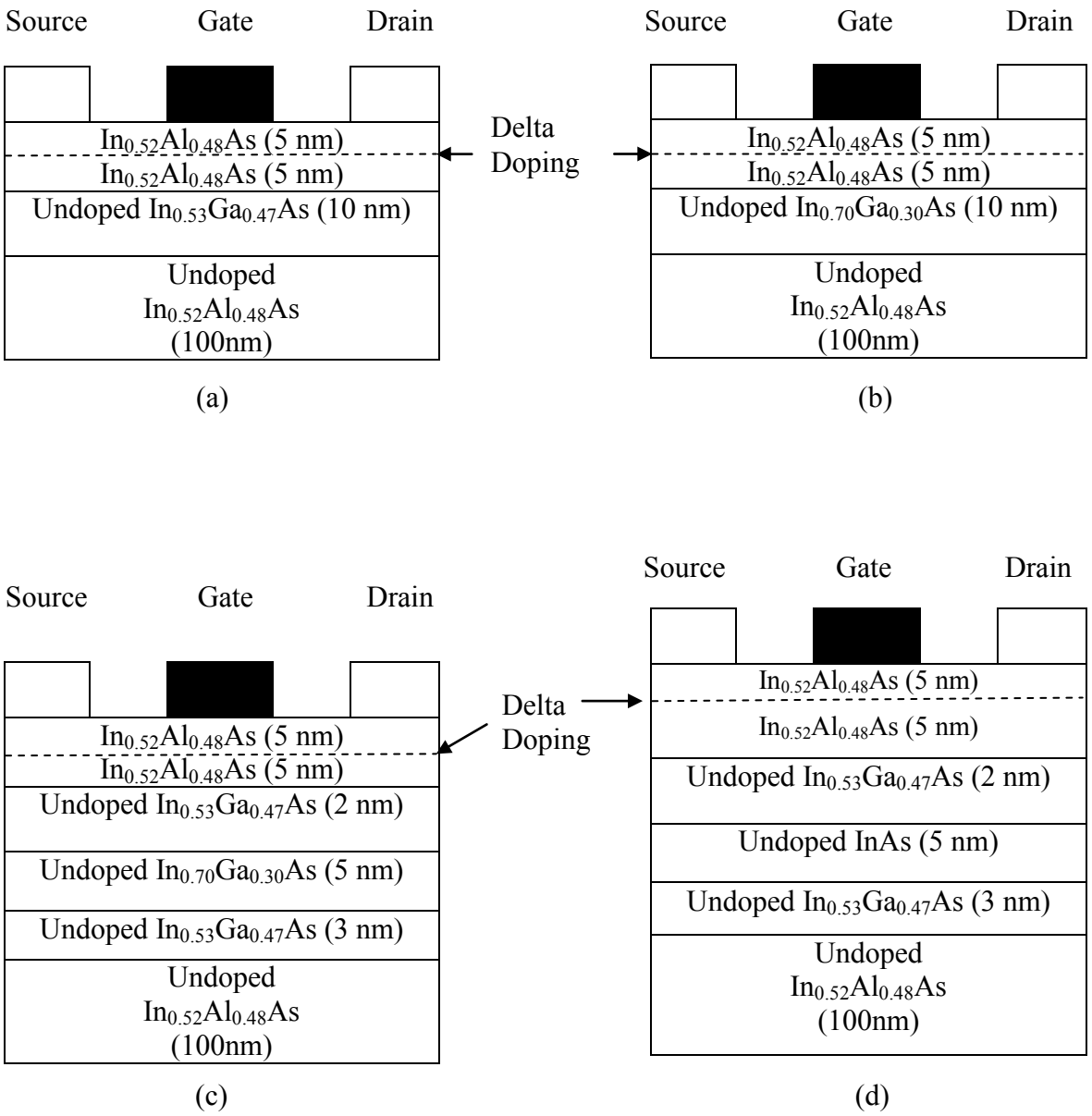


Figure 2.4: Delta doped (a) $In_{0.53}Al_{0.47}As$ channel, (b) $In_{0.70}Al_{0.30}As$ channel, (c) $In_{0.70}Al_{0.30}As$ MQW and (d) InAs MQW HEMTs

All the variants of delta doped and spacer layer HEMTs are shown in Fig. 2.3 and Fig. 2.4 respectively. Because for the generic, delta doped and spacer layered cases of the $In_{0.52}Al_{0.48}As$ HEMT the Indium mole fraction of the barrier and channel layers differ only by 1%, the two layers should be closely lattice matched. Hence the channel layer can be considered unstrained in this case. However for the rest of the structures, strain effect needs to be considered because of the significant difference of Indium mole fraction between the channel and barrier layer.

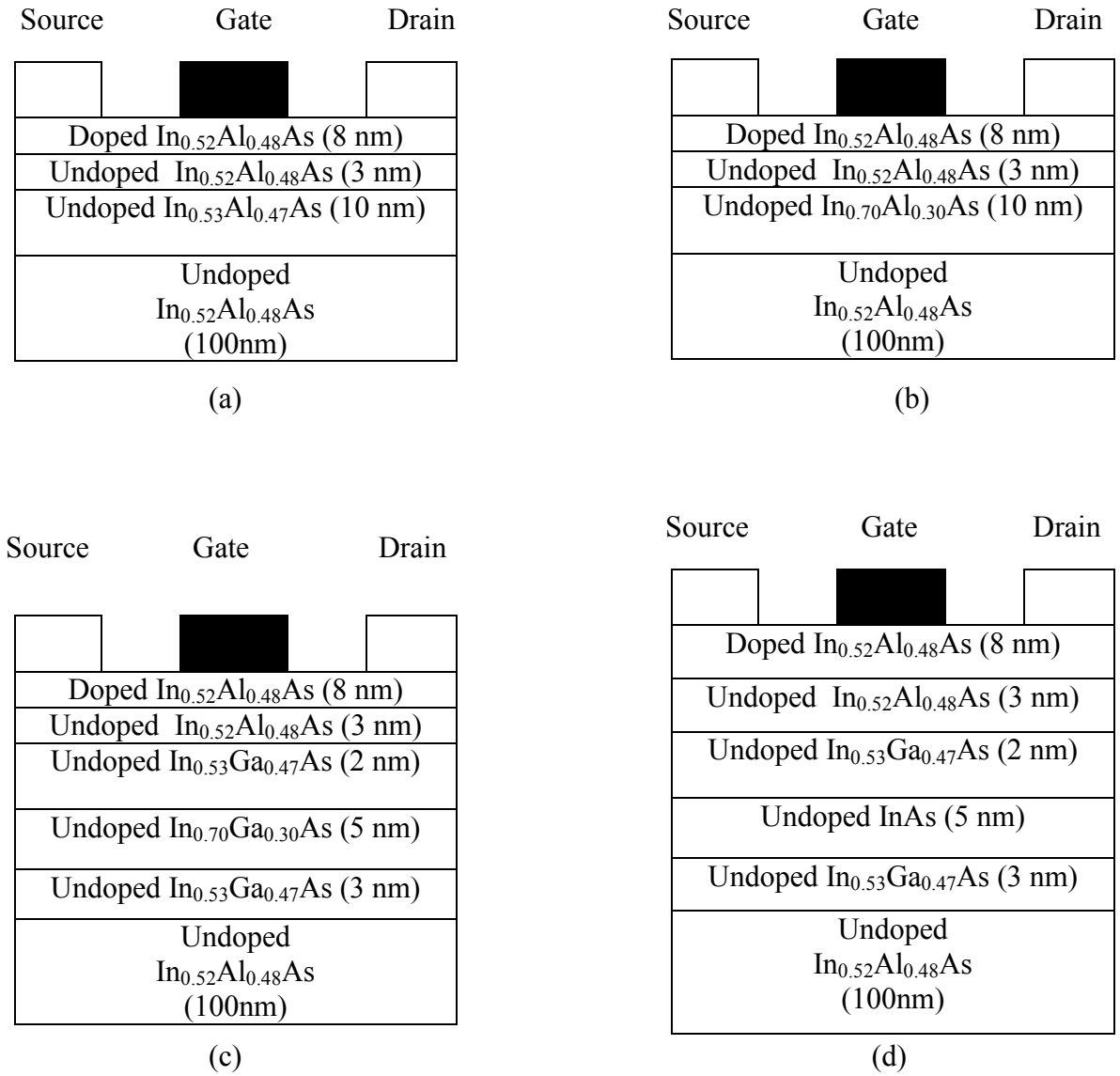


Figure 2.5: Spacer layered (a) $In_{0.53}Al_{0.47}As$ channel, (b) $In_{0.70}Al_{0.30}As$ channel, (c) $In_{0.70}Al_{0.30}As$ MQW and (d) InAs MQW HEMTs

The specifications of all the HEMTs investigated in this work are summarized in Table 2.1. All these devices have been analyzed for an applied gate bias of -0.20V to 0.40V. The transport characteristics have been studied for drain to source voltage of zero to 0.6V. These voltages are within the experimental operated range of highly scaled HEMT devices.

Table 2.1: Summary of analyzed HEMT devices

	Barrier Layer	Spacer Layer	Channel Layer	Delta Doping
Device 1	11nm $In_{0.52}Al_{0.48}As$	None	10nm $In_{0.53}Ga_{0.47}As$	None
Device 2	8nm $In_{0.52}Al_{0.48}As$	3nm $In_{0.52}Al_{0.48}As$	10nm $In_{0.53}Ga_{0.47}As$	None
Device 3	11nm $In_{0.52}Al_{0.48}As$	None	10nm $In_{0.53}Ga_{0.47}As$	$5.5x10^{18}$ cm^{-3}
Device 4	11nm $In_{0.52}Al_{0.48}As$	None	10nm $In_{0.70}Ga_{0.30}As$	None
Device 5	8nm $In_{0.52}Al_{0.48}As$	3nm $In_{0.52}Al_{0.48}As$	10nm $In_{0.70}Ga_{0.30}As$	None
Device 6	11nm $In_{0.52}Al_{0.48}As$	None	10nm $In_{0.70}Ga_{0.30}As$	$5.5x10^{18}$ cm^{-3}
Device 7	11nm $In_{0.52}Al_{0.48}As$	None	2nm $In_{0.53}Ga_{0.47}As$ 5nm InAs 3nm $In_{0.53}Ga_{0.47}As$	None
Device 8	8nm $In_{0.52}Al_{0.48}As$	3nm $In_{0.52}Al_{0.48}As$	2nm $In_{0.53}Ga_{0.47}As$ 5nm InAs 3nm $In_{0.53}Ga_{0.47}As$	None
Device 9	11nm $In_{0.52}Al_{0.48}As$	None	2nm $In_{0.53}Ga_{0.47}As$ 5nm InAs 3nm $In_{0.53}Ga_{0.47}As$	$5.5x10^{18}$ cm^{-3}
Device10	11nm $In_{0.52}Al_{0.48}As$	None	2nm $In_{0.53}Ga_{0.47}As$ 5nm $In_{0.70}Ga_{0.30}As$ 3nm $In_{0.53}Ga_{0.47}As$	None
Device11	8nm $In_{0.52}Al_{0.48}As$	3nm $In_{0.52}Al_{0.48}As$	2nm $In_{0.53}Ga_{0.47}As$ 5nm $In_{0.70}Ga_{0.30}As$ 3nm $In_{0.53}Ga_{0.47}As$	None
Device12	11nm $In_{0.52}Al_{0.48}As$	None	2nm $In_{0.53}Ga_{0.47}As$ 5nm $In_{0.70}Ga_{0.30}As$ 3nm $In_{0.53}Ga_{0.47}As$	$5.5x10^{18}$ cm^{-3}

All the devices presented here have been studied with respect to electrostatic and transport characteristics. The results have been obtained by simulating each device using the self-consistent analysis technique and capacitance-voltage and transport characterization models, which are described in the next section.

CHAPTER 3

Model and Formulation

In this section the self-consistent analysis technique used in this work is presented with necessary equations. In the subsequent section the formulation for calculating the capacitance, current and mobility has been presented. Finally validation of the numerical simulation performed in this work has been presented with illustrations.

3.1 Self Consistent Analysis

The self consistent simulation technique proposed by Stern [21] is based on the solution of the Schrödinger's and Poisson's equations in a coupled manner. The major approximation made by Stern is that here the 'effective mass approximation' is valid, so that the periodic lattice potential need not to be taken into account explicitly. Considering z direction to be the direction perpendicular to the semiconductor interface, the Schrödinger's equation within the effective mass approximation can be written in the 1-D as,

$$\left[-\frac{\hbar^2}{2m_{zi}} \frac{\partial^2}{\partial z^2} + eV(z) + \Delta E_c(z) \right] \psi_{ij}(z) = E_{ij} \psi_{ij}(z) \qquad (2.1)$$

Here m_{zi} is the quantization effective mass perpendicular to the interface, E_{ij} is the eigen energy of the j^{th} subband in the i^{th} valley in the same direction, $V(z)$ is the electrostatic potential, ΔE_c is the conduction band offset, e is the magnitude of the electronic charge and ψ_{ij} is the envelope function for the j^{th} subband in the i^{th} valley in the z direction. The boundary conditions utilized to solve the equation are as follows:

1. $\psi_{ij}(\infty) = 0$ deep inside the semiconductor, i.e. at the bottom of the device
2. $\psi_{ij} = 0$ at the metal-semiconductor interface
3. Open boundary conditions at elsewhere of the device

Considering these boundary conditions, Eq. (2.1) is solved numerically using the Hamiltonian Matrix formulation [69].

It is known that strain effects, arising from the lattice mismatch of corresponding layers, influence the energy band structure and effective mass of the device. To incorporate strain effects in this study, the bottom of the conduction band edge at the Γ point has been modified as follows according to the two-band k.p model calculation in [67].

$$E_c(\Gamma) = E_c^0 = E_v^0 + E_g + a_c(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \tag{2.2}$$

Here E_c^0 and E_v^0 are respectively the bottom of the conduction band and the top of the valence band without any strain and the factor a_c is the hydrostatic deformation potential. The factors ε_{xx}, ε_{yy} and ε_{zz} are the relative measurement of strain defined as:

$$\varepsilon_{mn} = \frac{\Delta a_m}{a_n} \tag{2.3}$$

Here a refers to the lattice constant and $m,n = x,y$ or z axis. In this work the biaxial strain of lattice mismatch is in the superlattice growth direction, which is the z axis. For this consideration, $\varepsilon_{xx} = \varepsilon_{yy} \neq \varepsilon_{zz}$ and $\varepsilon_{mn} = 0$ when $m \neq n$. According [67], these strain components are related by the elastic stiffness constant C_{11} and C_{12}.

$$\varepsilon_{zz} = -2\frac{C_{12}}{C_{11}}\varepsilon_{xx}$$

$$\text{where } \varepsilon_{xx} = \varepsilon_{yy} = \frac{a_{st} - a_0}{a_0} \tag{2.4}$$

Here a_{st} and a_0 are the lattice constants of the strained and unstrained crystals respectively.

The potential *V(z)*, which is an input to the Schrödinger's equation, is first obtained by numerically solving the Poisson's equation. This equation is formulated as following for the HEMT device,

$$\begin{aligned} \frac{\partial^2 V}{\partial z^2} &= -\frac{e}{\varepsilon_{semi}\varepsilon_0}[N_D - N_A + \rho_{inv}(z)], \text{ for the barrier layer} \\ \frac{\partial^2 V}{\partial z^2} &= -\frac{e}{\varepsilon_{semi}\varepsilon_0}[\rho_{inv}(z)], \text{ for the channel and buffer layer} \end{aligned} \tag{2.2}$$

Here ε_0 is the dielectric constant of the vacuum ε_{semi} is the dielectric constant of the corresponding semiconductor layer, N_D is the donor atom concentration, N_A is the acceptor atom concentration and ρ_{inv} is the inversion charge distribution along the *z* direction. The following two types of boundary conditions have been considered to solve the Poisson's equation.

1. Dirichlet boundary condition is imposed on the metal interfaces, where the potential is known i.e. $V(z)=V_{gb}$ where V_{gb} is the applied voltage. Also when the buffer layer is kept grounded then $V(z)=0$ at the bottom of the buffer;
2. Neuman boundary condition is imposed on the semiconductor interfaces where the electric flux is considered to be continuous i.e. $\varepsilon_1 \mathrm{E}_1 = \varepsilon_2 \mathrm{E}_2$ where ε_1 and ε_2 are the dielectric constants and E_1 and E_2 are the corresponding electric fields normal to the interfaces.

In Eq. (2.2) the inversion charge distribution ρ_{inv} is calculated by using the eigenenergies and wavefunctions obtained from the Schrödinger's equation. The equation used is:

$$\rho_{inv} = \sum_{ij} N_{ij} \, |\psi_{ij}(z)|^2 \tag{2.3}$$

Here N_{ij} is the sheet carrier density inside the semiconductor, which is obtained by

$$N_{ij} = \frac{n_{vi} m_{di} kT}{\pi \hbar^2} \ln[1 + e^{(E_F - E_{ij})/kT}] \tag{2.4}$$

Here m_{di} is the density of states effective mass of the *i*th valley, $\mathrm{E_F}$ is the Fermi level, n_{vi} is the valley degeneracy. For $\mathrm{In_xGa_{1-x}As}$, the value of n_{vi} is 1. The Poisson's equation is solved using the finite difference method, according to which

$$\frac{\partial^2 V}{\partial z^2} = \frac{V_{n+2} - 2V_{n+1} + V_n}{\Delta z^2} = -\frac{q}{\varepsilon_n \varepsilon_0}[\rho_n] \tag{2.5}$$

Here Δz is the grid spacing, *n+2, n+1* and *n* are the grid points, ρ_n is the total charge density at the n^{th} grid point, ε_n is the dielectric constant of that point. Once Eq. (2.5) is solved for a particular gate bias, the potential profile *V(z)* for that corresponding bias is obtained, which is next used as an input to Eq. (2.1). The solutions of Eq. (2.1) are again

used to calculate N_{ij} and ρ_{inv} from Eq. (2.3) and (2.4). The whole calculation is done repetitively until the margin of error between two successive potential profiles becomes less than 0.01%. Thus self consistent simulation is performed to calculate the charge concentration and potential profile of the HEMT devices, which are next used to calculate capacitance, ballistic current and mobility of the devices.

3.2 Capacitance-Voltage (C-V) Characterization

The coupled solution of the self consistent solver provides potential and charge profile of the analyzed device structures for different gate biases. The calculated total charge concentration has been used to calculate the gate capacitance (C_g) using the following basic equation:

$$C_g = \frac{dQ_{total}}{dV_g} \tag{2.6}$$

The total charge concentration (Q_{total}) for a particular gate voltage is the sum of the total inversion charge and the depletion charge for that corresponding voltage. Because Q_{total} is obtained using the self-consistent simulation technique, the calculated C_g can be said to be self-consistently obtained. In order to validate this numerically obtained result, the physical gate capacitance or the quantum capacitance model proposed in [20] has also been employed in this work. The model has been illustrated in Fig. 3.1.

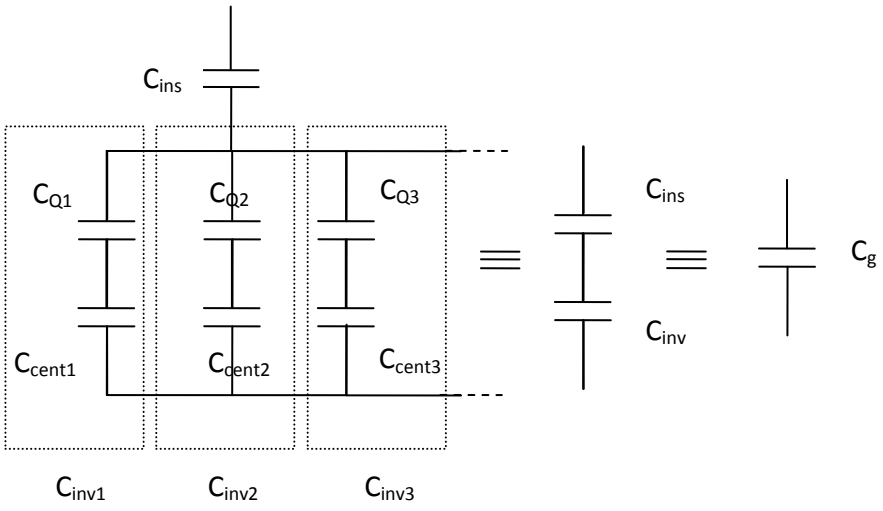


Figure 3.1: Different components of the physical gate capacitance model

According to this model:

$$C_g = \frac{C_{ins}\sum_i C_{inv_i}}{C_{ins} + \sum_i C_{inv_i}} \tag{2.7}$$

In this equation C_{ins} is the insulator capacitance, which is given by given by:

$$C_{ins} = \frac{\varepsilon_{ins}\varepsilon_o}{t_{ins}} \tag{2.8}$$

In this equation ε_{ins} and t_{ins} are respectively the dielectric constant and thickness of the insulator layer, i.e the barrier layer. C_{inv_i} in Eq. (2.7) represents the inversion capacitance of the ith subband, which is actually the series combination of the centroid capacitance (C_{cent_i}) and the quantum capacitance (C_{Q_i}) of the ith subband, i.e.

$$C_{inv_i} = \frac{C_{cent_i}C_{Q_i}}{C_{cent_i} + C_{Q_i}} \tag{2.9}$$

The C_{cent_i} and C_{Q_i} are obtained from the following equations:

$$C_{cent_i} = C_{Q_i}\frac{\partial(E_F - E_i)}{\partial(E_F - E_c)} \tag{2.10}$$

$$C_{Q_i} = \frac{\frac{m_{||}e^2}{\pi\hbar^2}}{1+\exp(\frac{E_i - E_F}{kT})} \tag{2.11}$$

Here E_i is the subband energy level, $m_{||}$ is the density of states effective mass, E_c is the conduction band edge at the barrier channel interface, k is the Boltzman constant and T is the temperature.

3.3 Transport Characterization

The calculation of ballistic current is based on the method proposed by Natori, which is also known as the over-the-barrier-model [68]. According to this model, the carrier density per unit area of the j^{th} subband can be expressed as:

$$n_j = \frac{m_{ds}^* kT}{\pi\hbar^2}\{\ln(1+\exp(\frac{E_F - E_j}{kT})) + \ln(1+\exp(\frac{E_F - E_j - eV_{DS}}{kT}))\} \tag{2.12}$$

where V_{DS} is the drain to source voltage. Because n_j is already available from the self-consistent analysis, it is possible to numerically calculate E_F from Eq. (2.12).

Considering no carrier backscattering [59], the drain to source ballistic current per unit width is given by:

$$\frac{I_{DS}}{W} = Q_i(0)\left\{v_T \frac{\Im_{1/2}(\eta_F)}{\Im_0(\eta_F)}\right\}\left\{\frac{1-\frac{\Im_{1/2}(\eta_F - U_D)}{\Im_{1/2}(\eta_F)}}{1+\frac{\Im_0(\eta_F - U_D)}{\Im_0(\eta_F)}}\right\} \tag{2.13}$$

In this equation $\Im_{1/2}(\eta)$ is the Fermi-Dirac integral of order half as defined by Blakemore [70], W is the gate width, $Q_i(0)$ is the sheet-electron density at the beginning of the channel and U_D is the drain bias dependence defined as $U_D = \frac{eV_{DS}}{kT}$. The term v_T in Eq. (2.13) represents the equilibrium unidirectional thermal velocity given by $v_T = \sqrt{\frac{2kT}{\pi m_c^*}}$ where m_c^* is the conductivity effective mass. The ballistic current I_{DS} can also be used to calculate ballistic mobility. As shown in [60], for a conventional device at low drain bias the drain current is given by:

$$\frac{I_{DS}}{W} = Q_i(0)\mu_0 \frac{V_{DS}}{L} \tag{2.14}$$

where L is the device gate length and μ_0 is the physical mobility of the channel material. For small gate length and under low drain bias $V_{DS} \ll \frac{kT}{e}$ and hence $U_D \to 0$. In that case by equating Eq. (2.13) and (2.14), the ballistic mobility (μ_B) can be defined as:

$$\mu_B = \frac{eL}{\pi m^* v_T}\frac{\Im_{-1/2}(\eta_F)}{\Im_0(\eta_F)} \tag{2.15}$$

Also noteworthy that if in Eq. (2.14) the current I_{DS} is the ballistic current and if μ_0 is replaced by μ_B, then the ballistic current can be directly calculated from Eq. (2.14). As defined in [60], in the quasi-ballistic limit according to the Mathieassien rule the effective mobility (μ_{eff}) is obtained by:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_B} + \frac{1}{\mu_0} \tag{2.15}$$

3.4 Model Validation

To experimentally validate the self-consistent analysis technique used in this study, the numerically obtained capacitance-voltage characteristic of $In_{0.53}Ga_{0.47}As$ channel generic HEMT has been compared with the results obtained using the physical gate capacitance or the quantum capacitance (QC) model described in [20]. In Fig. 3.2, the quantum and centroid capacitances of the first three subbands are plotted as a function of gate voltage. In this figure $C_{Q1,}$ C_{Q2} and C_{Q3} correspond to first, second and third subband quantum capacitance respectively whereas $C_{cent1,}$ C_{cent2} and C_{cent3} are respectively the first, second and third subband centroid capacitance.

From Fig. 3.2 it can be seen that third subband quantum and centroid capacitances are very small compared to the values of the second and first subband capacitances. Hence in the calculation of capacitance of highly scaled HEMTs according to the QC model, the contributions of the first two subbands are most dominant. The subband capacitances shown in Fig. 3.2 have been used to calculate inversion capacitance of the respective subbands according Eq. 2.9. The subband inversion capacitances have been subsequently used to calculate the overall gate capacitance according Eq. 2.7. In Fig. 3.3 the gate capacitance obtained using the self-consistent simulation technique and the corresponding values according to the QC model are shown in the same plot. Also the insulator capacitance (C_{ins}) is shown for comparison purpose. The figure shows that the results obtained using the self-consistent analysis technique are both qualitatively and quantitatively in close agreement with the QC model. This validates the self-consistent simulation technique employed in this study.

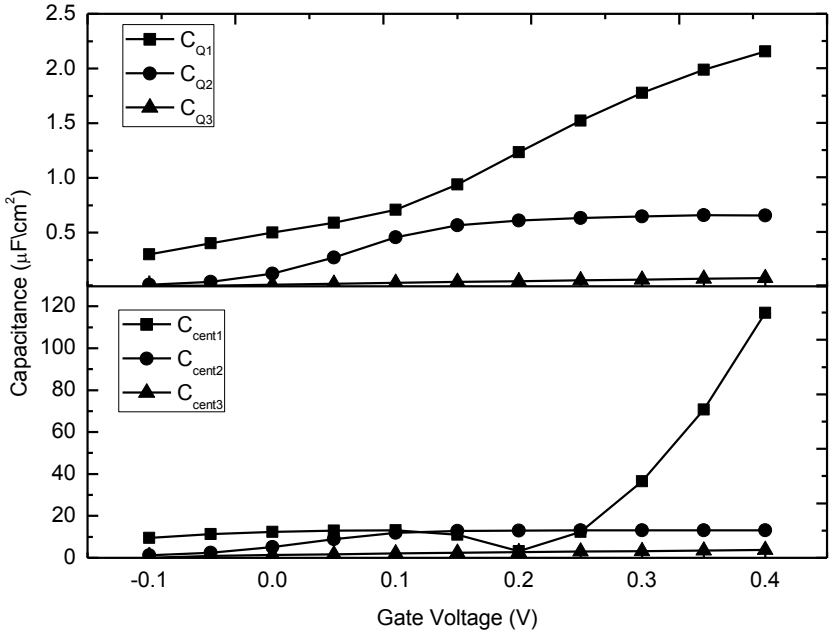


Figure 3.2: Quantum and centroid capacitances for $In_{0.53}Ga_{0.47}As$ generic HEMT

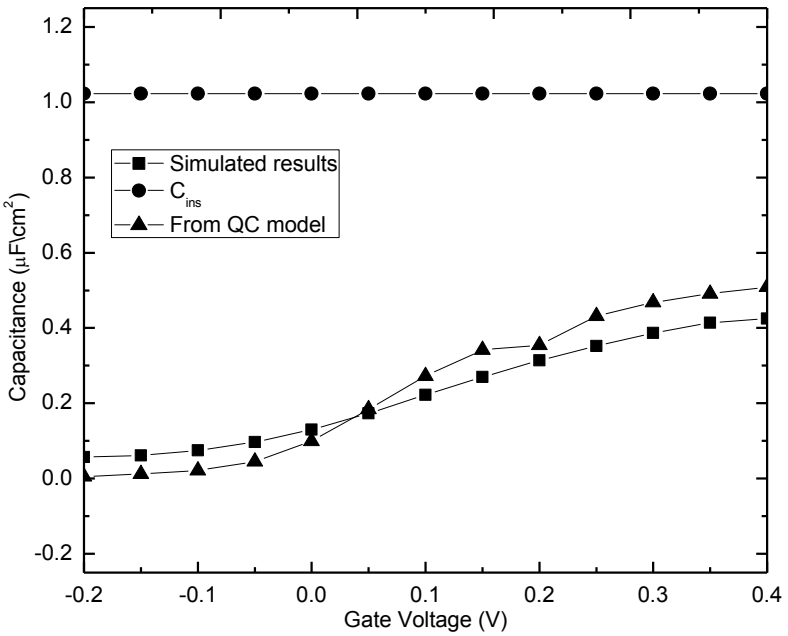


Figure 3.3: C-V characteristics according to the QC model and self-consistent simulation

To validate the transport characterization technique of this work, ballistic and effective mobility of $In_{0.53}Ga_{0.47}As$ obtained by numerical simulation have been compared with previously obtained results using Sentauras [65]. The comparative study is shown in Fig. 3.4. According to the figure, the results obtained in this study closely match the results reported in [64]. This validates the transport characterization technique as well.

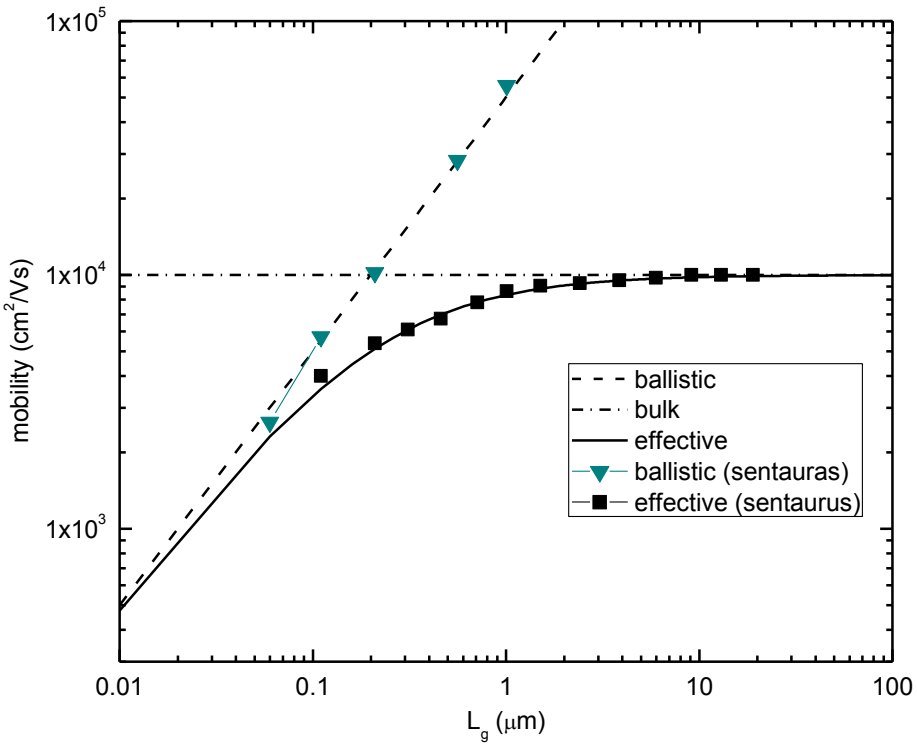


Figure 3.4: Ballistic and effective mobility obtained using numerical analysis and simulation software Sentauras

CHAPTER 4

RESULTS AND DISCUSSIONS

According to the models and formulations described in the previous chapter, electrostatic and transport characteristics of the HEMT structures mentioned in chapter 2 have been analyzed with respect to electrostatic and transport characteristics. In this chapter the results of this analysis are discussed with illustrations.

4.1 Electrostatic Performance

The electrostatic performances discussed in this section include the energy band and carrier profiles, eigen states, sheet carrier density and C-V profiles. Because the device dimensions have been kept unchanged throughout the study, for all the figures in this section the 0-11nm of the position axis corresponds to the barrier layer, the 11nm-21nm corresponds to channel layer and the rest corresponds to buffer layer.

4.1.1 Energy band and carrier profile

The bottom of the conduction band edge and the carrier profile of $In_{0.53}Ga_{0.47}As$ channel

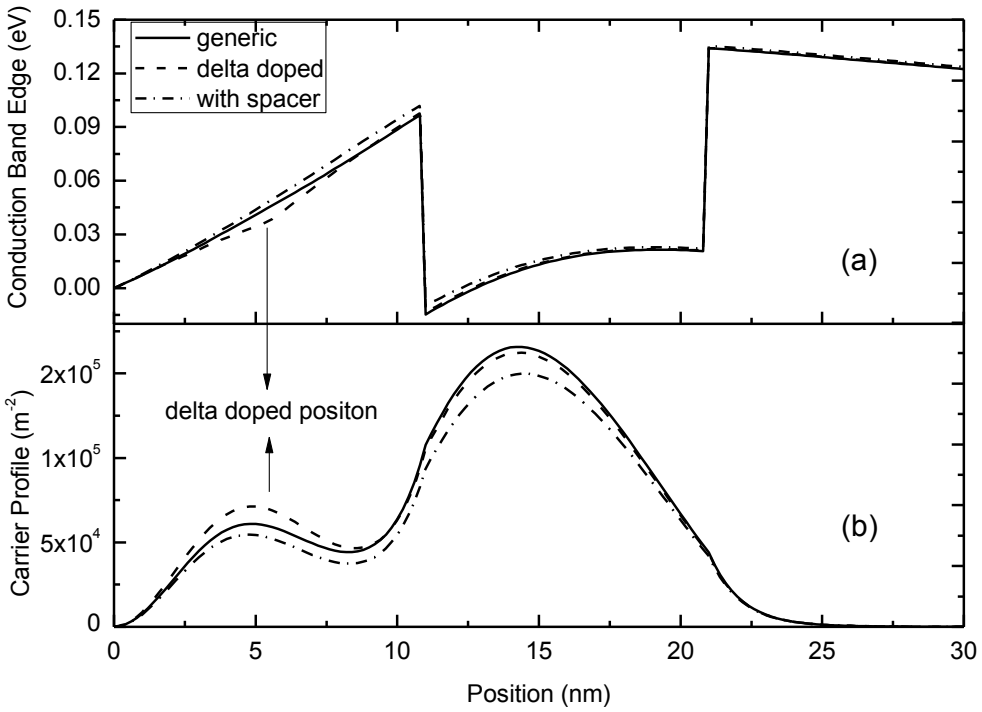


Figure 4.1: Conduction band and carrier profile of $In_{0.53}Ga_{0.47}As$ channel HEMT

HEMT is shown in Fig.4.1. All the three cases of generic, delta doped and spacer containing HEMTs are shown in this figure for zero gate bias. It has been reported earlier that delta doped HEMTs provide high channel electron density, reduced trapping effect and improved threshold voltage control and also high breakdown characteristics [72]. On the other hand to ensure that dopants from the doped barrier layer do not diffuse into the undoped channel layer, an undoped spacer layer of 3nm is placed in between the barrier and the channel layer. Fig. 4.1 illustrates the impact of delta doping and spacer layer on the conduction band and carrier profile of $In_{0.53}Ga_{0.47}As$ channel HEMT. In this figure the zero nanometer position in the horizontal axis indicates the metal-barrier layer interface. The delta doped position is at around 5nm, i.e. at the middle of the barrier layer. As can be seen from the figure, other than the notch at the band diagram of the delta doped region, there is not any significant difference between the conduction band profiles of the three cases. Because of this notch, there is less than one order higher carrier concentration at the delta doped region compared to the cases of the generic and spacer layered HEMTs. However inside the channel layer, the magnitude of the carrier profiles for the delta doped and generic HEMTs are almost the same. Similar results are obtained for $In_{0.70}Ga_{0.30}As$ channel HEMTs (Fig.4.2).

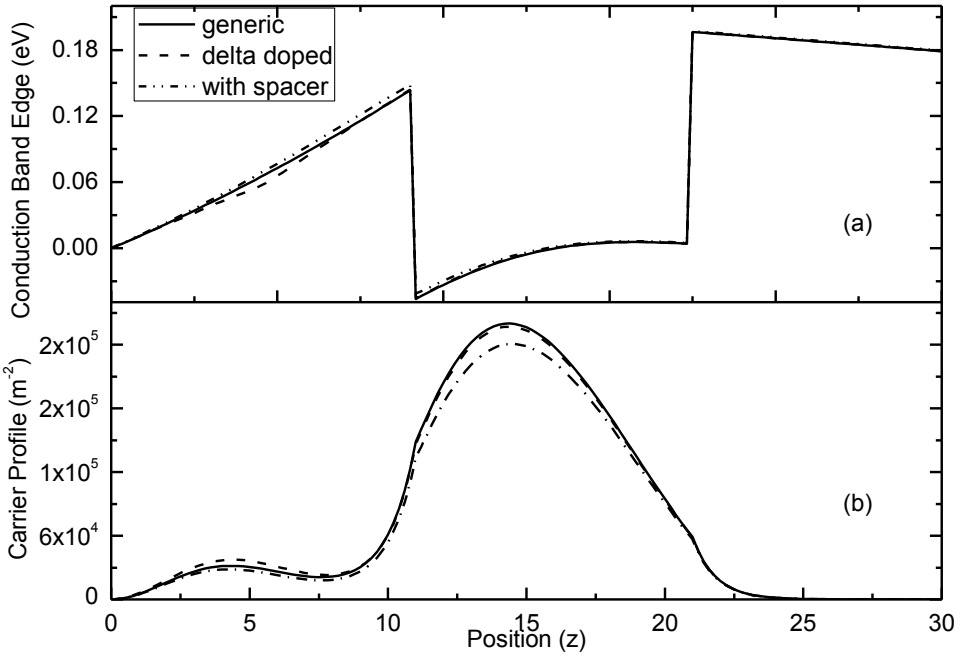


Figure 4.2: Conduction band and carrier profile of $In_{0.70}Ga_{0.30}As$ channel HEMT

According to Fig. 4.1(a) and 4.2(a), the addition of an undoped layer in the form of spacer slightly increases the energy of the conduction band profile compared to the cases of delta doped and generic structures. This increases the energy barrier seen by the carriers in the barrier layer to move into the channel region. Consequently the carrier concentration decreases slightly for the HEMT having spacer layer. However because the spacer layer prevents the diffusion of dopants into the channel layer, scattering is reduced which in effect increases ballistic mobility. This will be shown later during the discussion of transport characteristics.

The conduction band and carrier profile of MQW HEMTs are shown in Fig.4.3 and 4.4. The qualitative nature of the carrier profile in Fig. 4.3 is similar to the cases of the single channel HEMTs shown in Fig.4.1 and 4.2. Because of the presence of channel materials in different three layers, three quantum wells are formed in the channel region for the MQW HEMTs. As before a notch at the delta doped region is notable in the conduction band of the delta doped case. The carrier concentration is slightly higher in the vicinity of this region compared to the generic and spacer layered cases.

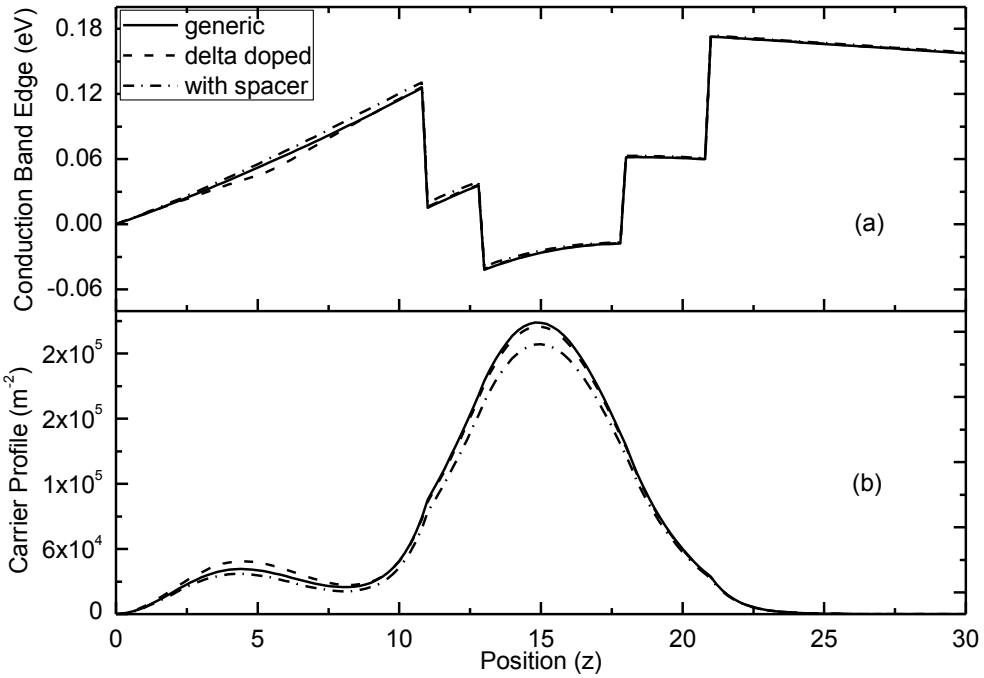


Figure 4.3: Conduction band and carrier profile of $In_{0.70}Ga_{0.30}As$ MQW HEMT

Just as in single channel HEMTs, the spacer layer slightly increases the energy of the conduction band edge in MQW HEMTs as shown in Fig. 4.3(a) and 4.4(a). So as shown in Fig. 4.3(b) and 4.4(b), the carrier concentrations slightly decreases when an undoped spacer layer is used in between the barrier and the channel layer.

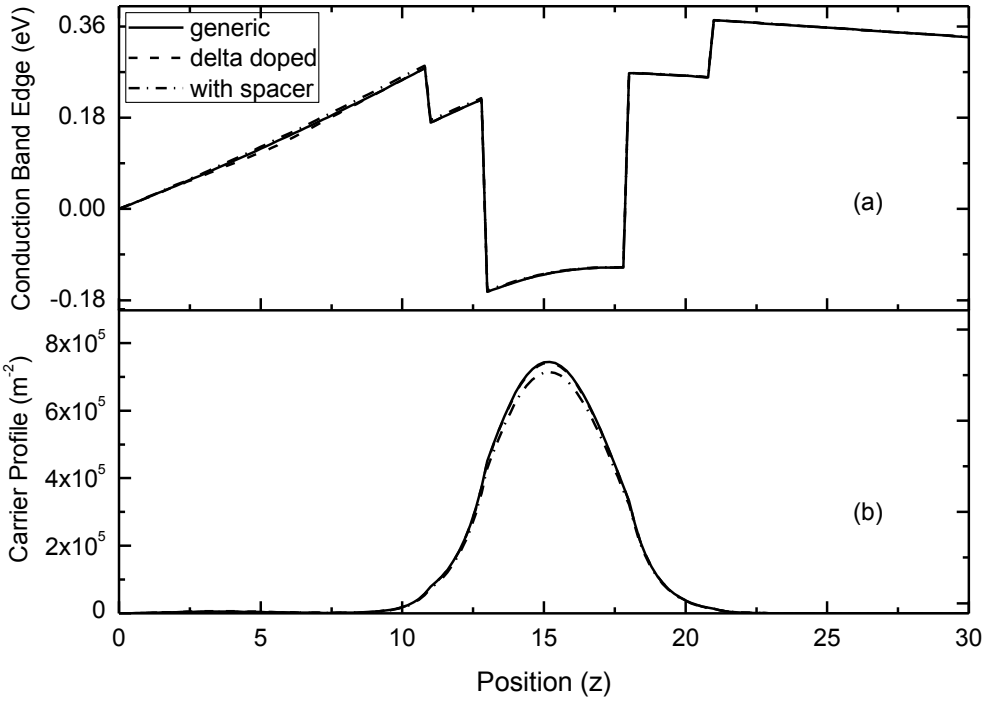


Figure 4.4: Conduction band and carrier profile of InAs MQW HEMT

From Fig. 4.4(b) it can be seen that at zero gate bias the carrier distribution is almost entirely confined into the channel region for InAs MQW HEMT. To explain this attribute the conduction band profile for all the four types of channels are shown in the same plot in Fig. 4.5. From this figure it is obvious that the quantum well formed in InAs MQW HEMT is deeper compared to the wells formed in three other types of channels. So among all the four types of channels, carrier confinement is strongest in InAs MQW HEMTs and hence almost all the carriers remain confined in the channel region at zero gate bias. The strong carrier confinement also results the high peak carrier concentration in InAs MQW HEMTs compared to the other three types (Fig. 4.5(b)). The stronger carrier confinement in InAs MQW HEMT actually arises from the lower bandgap of InAs (Table 4.1). Also the Density of State (DOS) effective mass is lowest

for InAs compared to the other channel materials as listed in Table 4.1. Because of the wider bandgap of $In_{0.53}Ga_{0.47}As$, carriers are relatively less confined in its HEMT and the peak carrier concentration is also lower.

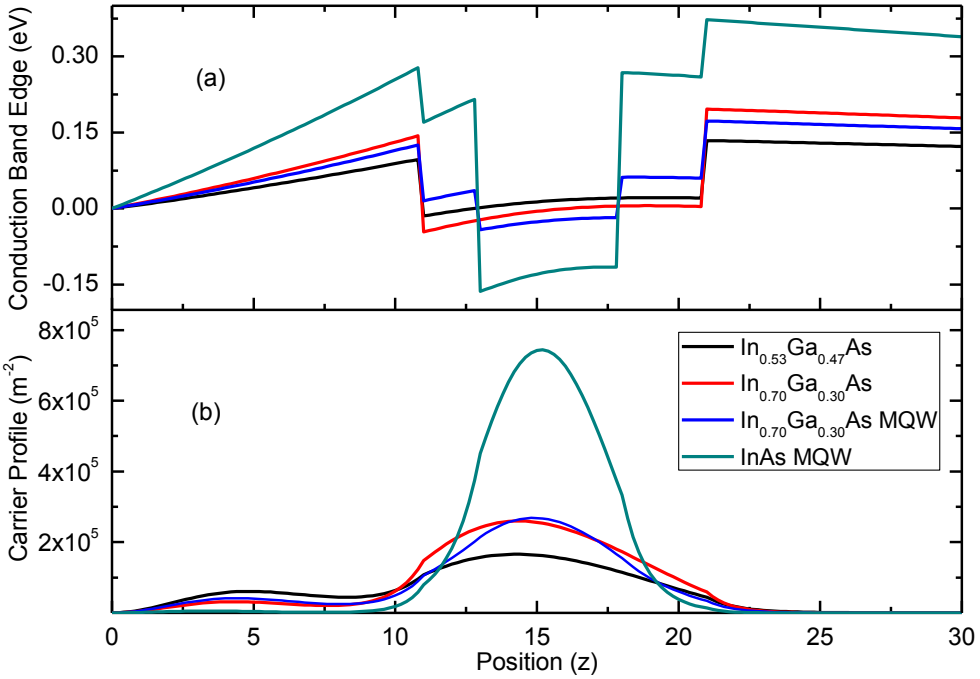


Figure 4.5: Conduction band and carrier profile of generic HEMT for different channels

Table 4.1: Specifications for four different channel HEMTs

Channel Type	Channel Bandgap (eV)	DOS Effective Mass (m_0=9.1 x 10^{-31}kg)	Energy Band Minima (eV)	Peak Carrier Conc. (x 10^5 m^{-2})
$In_{0.53}Ga_{0.47}As$	0.7359	$0.0453m_0$	-0.0147	1.6572
$In_{0.70}Ga_{0.30}As$	0.5712	$0.0383m_0$	-0.0462	2.5991
$In_{0.70}Ga_{0.30}As$ MQW	0.7359	$0.0453m_0$	-0.048	2.6839
	0.5712	$0.0383m_0$		
	0.7359	$0.0453m_0$		
InAs MQW	0.7359	$0.0453m_0$	-0.1638	7.4429
	0.3478	$0.0260m_0$		
	0.7359	$0.0453m_0$		

Also the energy band profiles indicate that multiple channel layers should both widen and deepen the quantum well and thus increase the quantum mechanical confinement. This calls for further study on increasing the channel layers in MQW HEMTs. It's noteworthy in Table 4.1 is that even though $In_{0.70}Ga_{0.30}As$ and $In_{0.70}Ga_{0.30}As$ MQW HEMTs both have channel materials having 0.5712eV bandgap, because of multi quantum well formation, the peak carrier concentration is slightly higher in the latter.

4.1.2 Allowed energy states

An important consideration in quantum mechanical analysis is the energy of the allowed states i.e. the eigen states. Energy of the first and second eigen state of $In_{0.53}Ga_{0.47}As$ and $In_{0.70}Ga_{0.30}As$ channel HEMTs are shown in Fig. 4.6 as a function of gate voltage (V_{gb}).

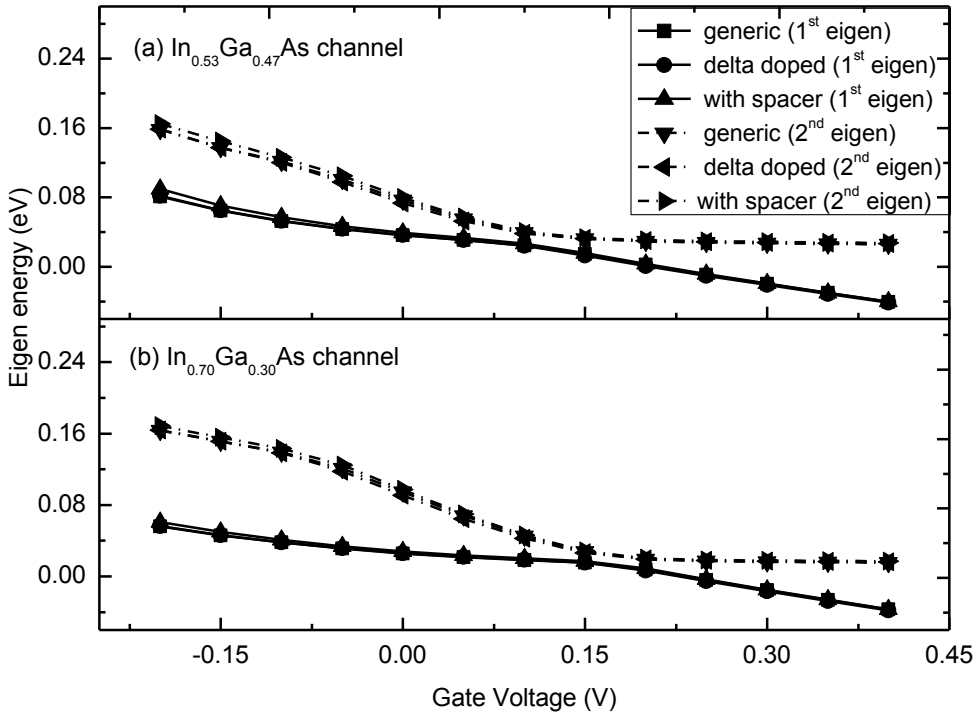


Figure 4.6: Eigen states of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ channel HEMTs

The figures show that the second eigen states are always at a higher energy compared to the first eigen states. The application of negative voltage causes the eigen state to go higher inside the quantum well. This indicates that if the applied negative voltage is

high enough, the eigen states will eventually goes beyond the quantum well. Then there will be no allowed states for the carriers to occupy in the channel region and the device turns off. Hence the characteristics shown in Fig. 4.6 refer to the depletion mode device, i.e. a device which is turned off by negative voltage. As shown in Fig. 4.7, similar results are observed for the MQW HEMTs. In both Fig. 4.6 and 4.7 it is obvious that at high gate bias delta doping or spacer layer has no impact on the position of first or second eigen state. In fact for the delta doped case the first eigen state coincides with the eigen state of the generic case for all gate biases shown in these figures. However for all channel materials the addition of spacer layer increases the eigen energy at low bias i.e the voltage required to turn off the device decreases. Hence the turn off voltage can be reduced by adding spacer layer to these highly scaled devices.

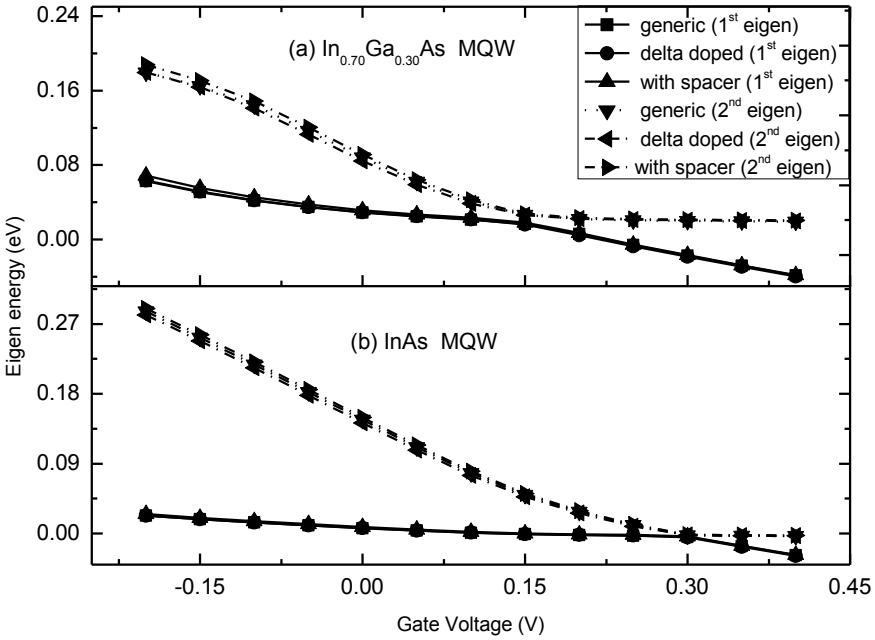


Figure 4.7: Eigen states of (a) $In_{0.70}Ga_{0.30}As$ MQW and (b) InAs MQW HEMTs

Another important consideration in quantum mechanical anlaysis is the phenomenon of energy discretization, which can be quantitatively studied by evaluating the difference of the first two eigen states. Fig. 4.8 illustrates the difference of the first two eigen states ($E_{12}=E_2-E_1$) for $In_{0.53}Ga_{0.47}As$ and $In_{0.70}Ga_{0.30}As$ channel HEMTs and the same criteria is shown for MQW HEMTs in Fig. 4.9. The increase of the value of E_{12} indicates higher quantization of energy and hence quantum mechanical effects.

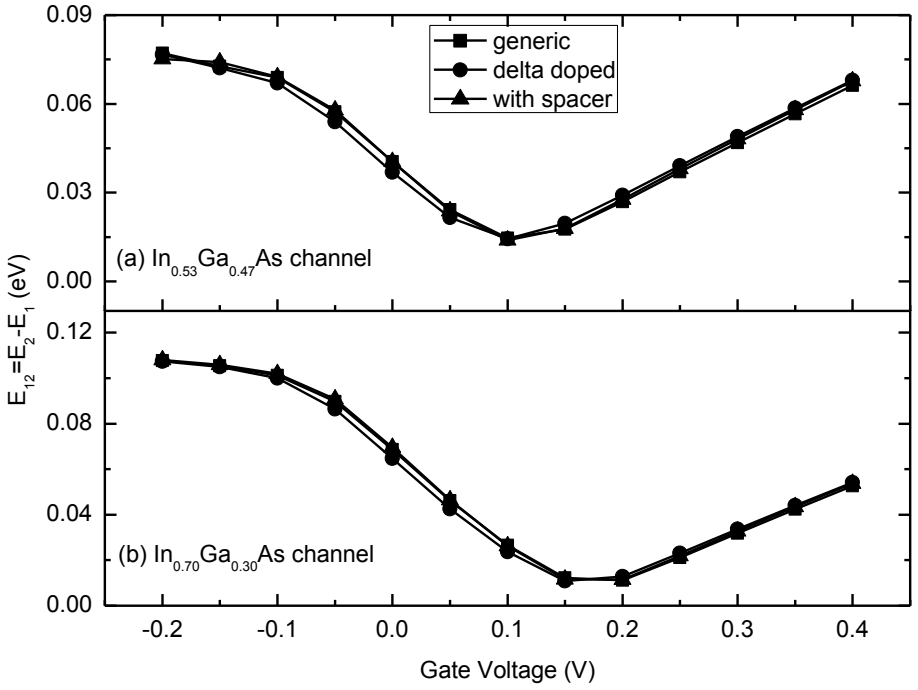


Figure 4.8: Eigen energy difference of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ channel

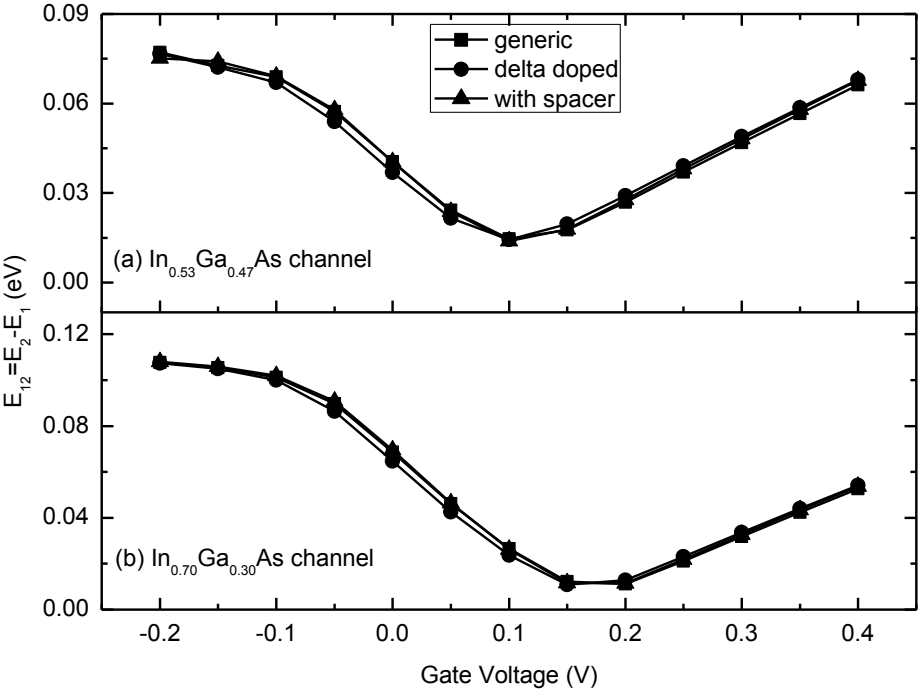


Figure 4.9: $E_{12}=E_2-E_1$ of (a) $In_{0.70}Ga_{0.30}As$ MQW and (b) InAs MQW HEMTs

Though the value of E_{12} increases with negative gate bias, this increase is of less importance because if the negative voltage is high enough the eigen states go beyond the quantum well and the device turns off. On the other hand if positive gate bias is increased, then even though the energies of the individual eigen states decrease, their difference i.e. E_{12} increases. This indicates increased quantum mechanical effects in the form of higher quantization of energy if the positive gate bias is increased in these devices. Also it can be seen from Fig. 4.7 and 4.8 that delta doping or the addition of spacer layer has negligible or no impact on the discretization of energy in the HEMTs of all four channel types.

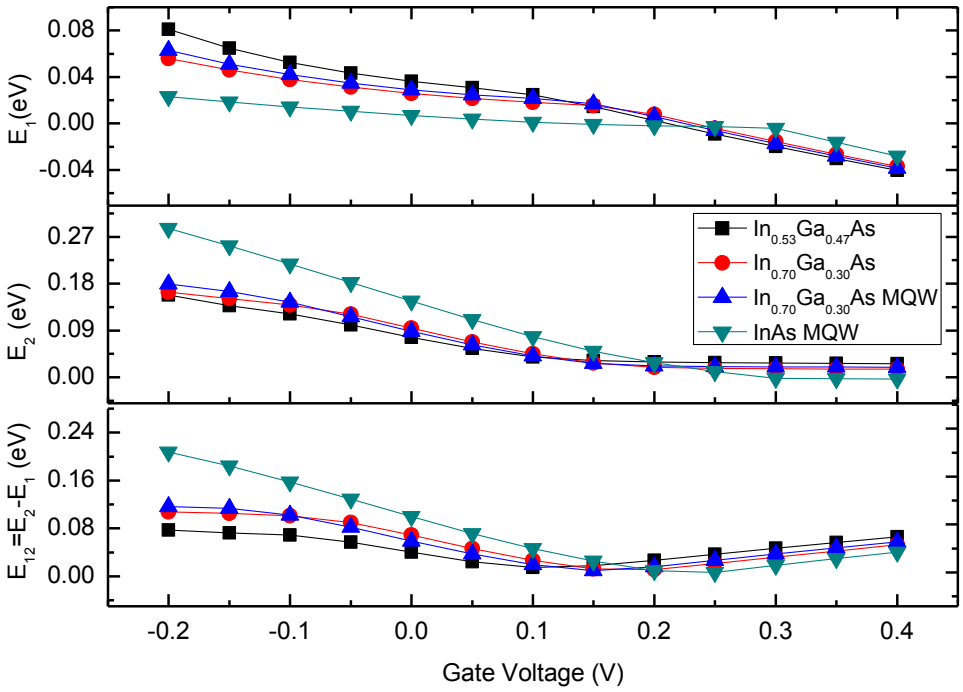


Figure 4.10: Energies for different channel materials as a function of gate voltage

For comparison among the four channel materials, the energy of the two eigen states (E_1 and E_2) and their differences (E_{12}) are shown in the same plot in Fig. 4.10. It can be seen that the values of E_1 and E_2 for $In_{0.53}Ga_{0.47}As$, $In_{0.70}Ga_{0.30}As$, $In_{0.70}Ga_{0.30}As$ MQW channel HEMTs are at vicinity for above 0.1V gate bias. Because of the deeper quantum well and lower effective mass (Table 4.1), energy discretization i.e the value of E_{12} is higher in InAs MQW HEMT for upto 0.20V. However with the increase of positive gate bias, E_{12} becomes greater for other channel materials compared to the InAs MQW case.

It is also noteworthy that the value of E_{12} increases for all HEMTs beyond respective minima, which are approximately 0.3V for InAs MQW HEMT and 0.1V for the HEMTs having other channel materials. This indicates that all these devices exhibit strong quantum confinement at high gate bias. At low and moderate gate bias, the InAs MQW HEMT shows the strongest quantum confinement.

Of particular interest is the fact that there exists a minima in the E_{12} versus V_{gb} curves (Fig. 4.8, 4.9 and 4.10) for all the HEMT devices in this discussion. From henceforth of the discussion, the voltage at which this minima occurs will be denoted by V_{Emin}. This values are shown in Table 4.2 for respective HEMTs. To explain the significance of V_{Emin}, the carrier profile of a generic HEMT is shown with respect to position in Fig. 4.11 for two different gate biases. One of the voltages (V_{gb}=0.05V) is smaller than V_{Emin} in the E_{12} vs. V_{gb} curve of Fig. 4.10 whereas the other voltage (V_{gb}=0.15V) is greater. Fig. 4.11 shows that even though for the smaller voltage the peak of carrier profile is within the channel layer, for the larger voltage

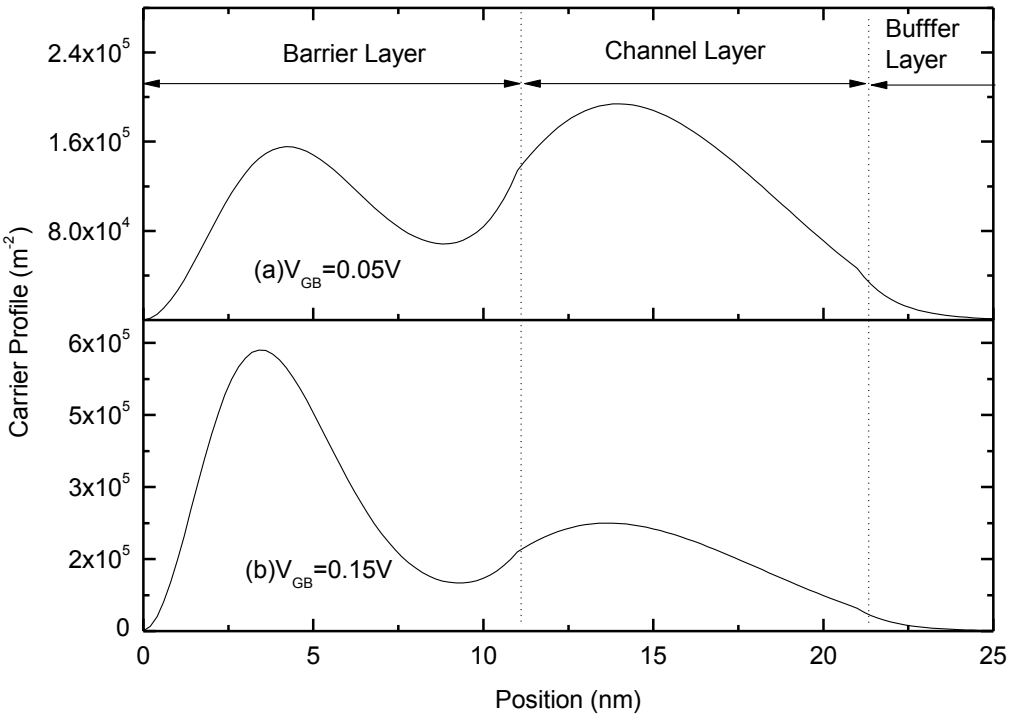


Figure 4.11: Carrier profile for (a) smaller and (b) greater than the minima voltage

the peak is actually inside the barrier layer. To further illustrate this phenomenon, the carrier profiles of a generic $In_{0.53}Ga_{0.47}As$ HEMT is shown in Fig. 4.12 for four different gate voltages. From this figure it can be seen that the carrier density increases both inside the barrier and the channel layer as the gate voltage increases. However for voltages less than V_{Emin} , the peak carrier density is more in the channel region compared to the barrier region whereas for voltages greater than V_{Emin} the opposite occurs. Also notable that with the increase of gate voltage the overall carrier density increases significantly. However because this increase is dominated by the increase of carriers in the barrier layer, the barrier should play a more dominant role in conduction compared to the channel. This phenomenon, which is also known as parallel conduction, is undesirable for HEMT devices. Hence by identifying the V_{Emin} from the E_{12} vs V_{gb} curve, it is possible to find the voltage beyond which parallel conduction occurs in highly scaled HEMTs.

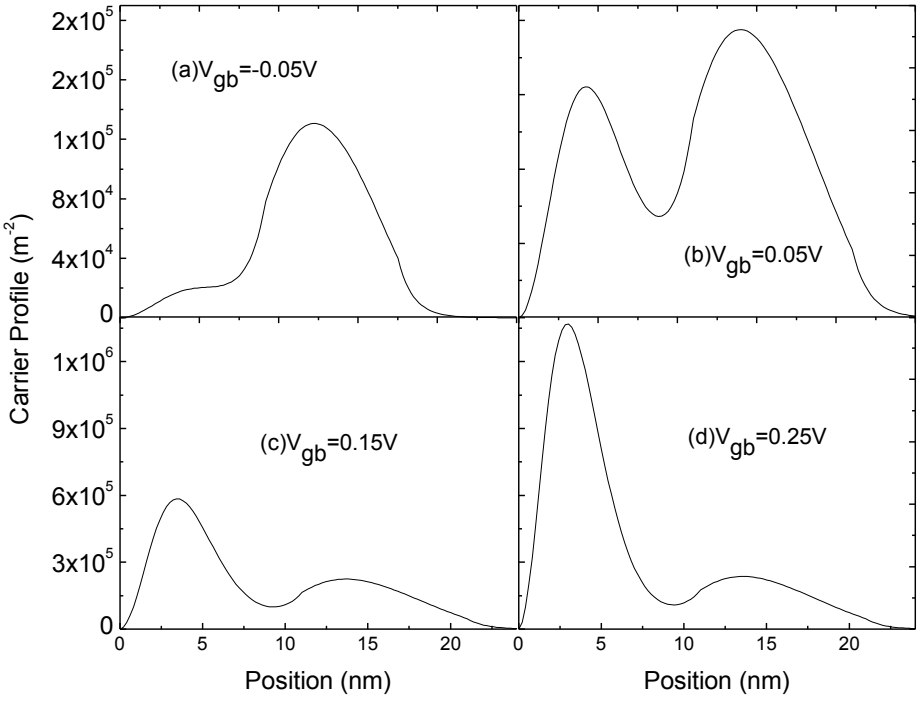


Figure 4.12: Carrier profile for four different gate voltages of a generic HEMT

In Table 4.2 the approximated V_{Emin} is shown for the different channel HEMTs. In this table $V_{smaller}$ refers to any voltage smaller than V_{Emin} and $V_{greater}$ refers to any voltage greater than V_{Emin}. Also in the table a term Q_{ratio} has been indicated which is defined as follows:

$$Q_{ratio} = \frac{\text{Peak carrier concentration inside channel layer}}{\text{Peak carrier concentration inside barrier layer}}$$

Table 4.2: Values of $V_{smaller}$, $V_{greater}$,Q_{ratio} and V_{Emin} for different channel HEMTs

Channel Type	At voltage smaller than V_{Emin}		At voltage greater than V_{Emin}		Approximated V_{Emin}
	$V_{smaller}$	Q_{ratio}	$V_{greater}$	Q_{ratio}	
$In_{0.53}Ga_{0.47}As$	0.05V	1.25	0.15V	0.39	0.10V
$In_{0.70}Ga_{0.30}As$	0.10V	1.36	0.20V	0.43	0.15V
$In_{0.70}Ga_{0.30}As$ MQW	0.10V	1.20	0.20V	0.41	0.15V
InAs MQW	0.20V	1.85	0.35V	0.49	0.25V

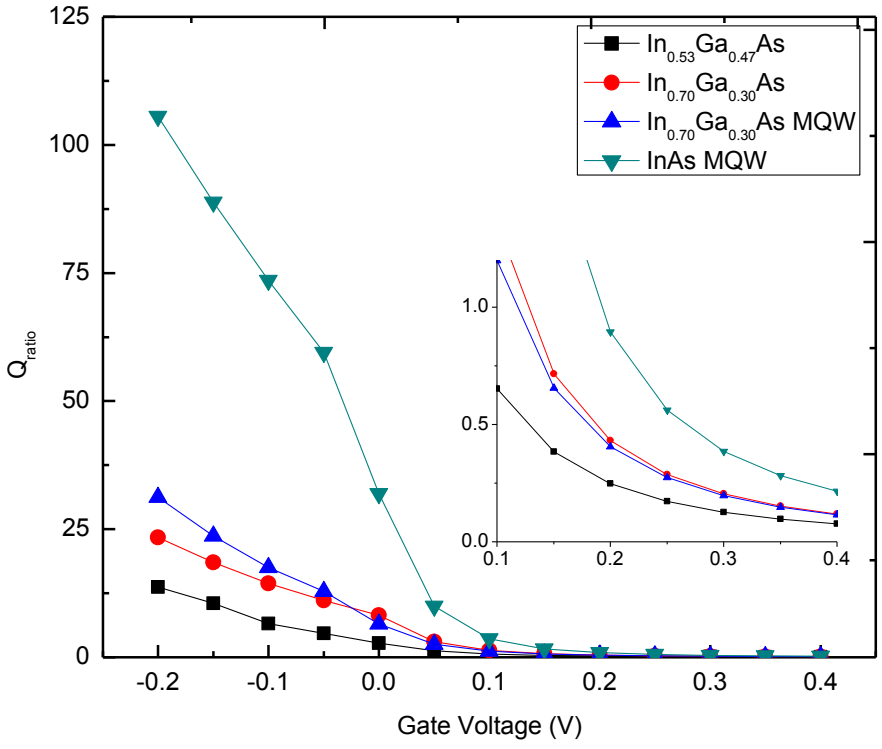


Figure 4.13: Q_{ratio} of different channel HEMTs with respect to gate voltage

As can be observed from the table, for $V_{gb}=V_{smaller}$, the value of Q_{ratio} is greater than 1 whereas for $V_{gb}=V_{greater}$ the value is smaller than 1. At $V_{gb}=V_{Emin}$, the Q_{ratio} should be unity. In Table 4.2 the value of V_{Emin} has been approximated from Fig. 4.8 and 4.9. Here noteworthy is that the value of V_{Emin} is greatest for InAs MQW HEMTs and smallest for $In_{0.53}G_{0.47}As$ channel HEMTs. For $In_{0.70}Ga_{0.30}As$ and $In_{0.70}Ga_{0.30}As$ MQW HEMTs V_{Emin} is in the mid range. Hence parallel conduction should occur for InAs MQW HEMTs at a much higher voltage compared to the other HEMTs being considered here. In Fig. 4.13 the values of Q_{ratio} are shown for all the HEMTs at different gate biases. The high value of Q_{ratio} for InAs MQW HEMT indicates that it demonstrates very strong carrier confinement in the channel compared to other devices. Also the figure illustrates that even though the V_{Emin} value is the same for $In_{0.70}Ga_{0.30}As$ and $In_{0.70}Ga_{0.30}As$ MQW HEMTs, the multi-quantum-well structure results slight increase of Q_{ratio} and hence carrier confinement in the channel of $In_{0.70}Ga_{0.30}As$ MQW HEMT.

4.1.3 Sheet carrier density

The sheet carrier density for the four different channel HEMTs studied in this work are shown in Fig. 4.14 and 4.15 as a function of gate voltage. As can be seen in these figures, for all these devices the carrier density increases exponentially with the increase of gate voltage. Also notable is that sheet carrier density almost remains unchanged if

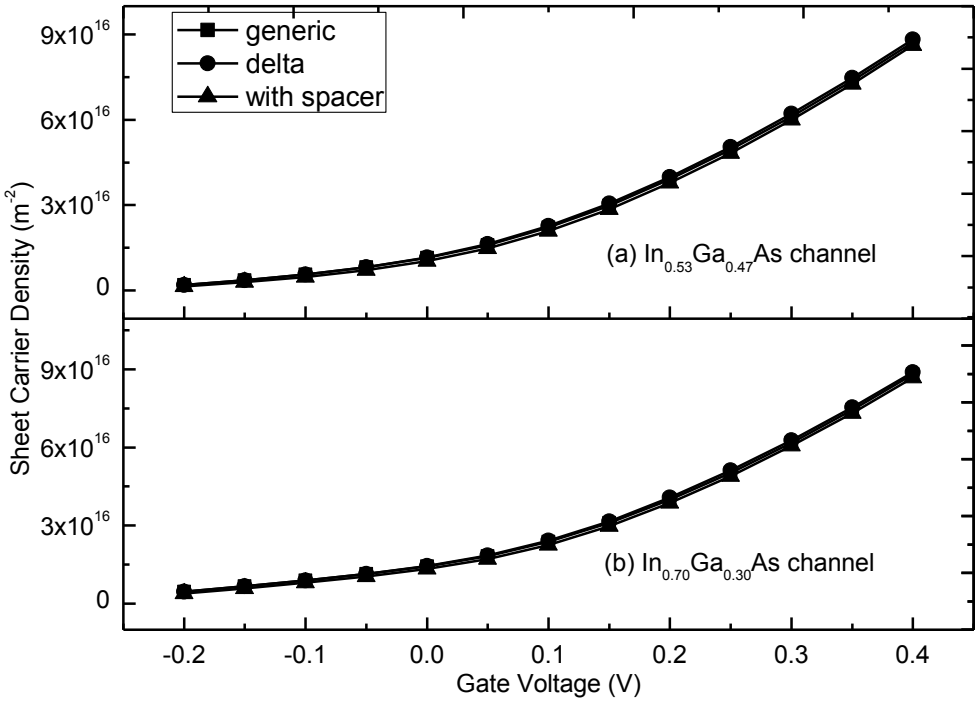


Figure 4.14: Sheet carrier density of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ channel

delta doping or space layer are added to the generic structure. This is mainly because of the negligible influence of delta doping and spacer layer on the potential and carrier profile and also on energy discretization of HEMTs, as discussed in previous subsections. To demonstrate the impact of channel material variation on carrier density, the sheet carrier density for a generic HEMT structure is plotted against gate voltage for four different channel contents in Fig. 4.16. As can be seen from this figure, the sheet carrier density in InAs MQW HEMT remains higher compared to other HEMTs for all gate biases. However for $V_{gb}>V_{Emin}$, the sheet carrier densities are at proximity for all the channels. This occurs because at gate bias greater than V_{Emin} , the carrier density in the barrier layer becomes prominent and the HEMTs goes into the undesired state of parallel conduction, as discussed in the previous sub-section.

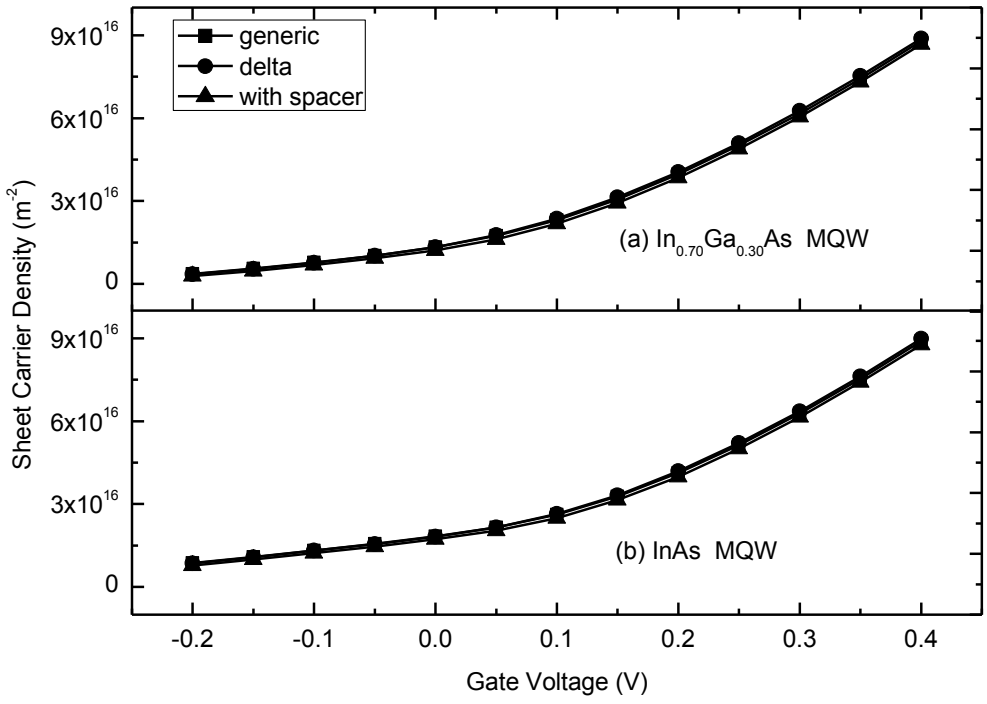


Figure 4.15: Sheet carrier density of (a) $In_{0.70}Ga_{0.30}As$ MQW and (b) InAs MQW HEMT

For $V_{gb}< V_{Emin}$, the sheet carrier density is significantly high for the InAs MQW case whereas for $In_{0.53}Ga_{0.47}As$ HEMT the sheet carrier density is the lowest. Because of the presence of $In_{0.70}Ga_{0.30}As$ in the channel of both other HEMTs, their sheet carrier densities are also almost the same. The MQW structure has only slightly increased the sheet carrier density of $In_{0.70}Ga_{0.30}As$ MQW HEMT.

The individual contribution of the first and second subbands in sheet carrier density is shown in Fig. 4.17. The carrier contribution of the first subband is always higher compared to the second subband at the same gate voltage. Though for $V_{gb}<V_{Emin}$ of InAs MQW HEMT, the carrier density of the first subband is higher compared to other device, when $V_{gb}>V_{Emin}$, then the contribution of first subband in InAs MQW channel decreases in comparison with others. However, still the net sheet carrier density remains higher (Fig. 4.16) in InAs MQW HEMT as the contribution of the second subband increases sharply (Fig. 4.17(b)) compared to other channel devices.

To compare the contribution of respective subbands, the occupancy factors of each device are plotted against V_{gb} in Fig. 4.18. At low gate bias, the sheet carrier is almost entirely contributed by the first subband. The occupancy factor of first subband for each device is found to reach minima near about the respective V_{Emin} voltage whereas the second subband reaches maxima at a higher voltage than V_{Emin}.

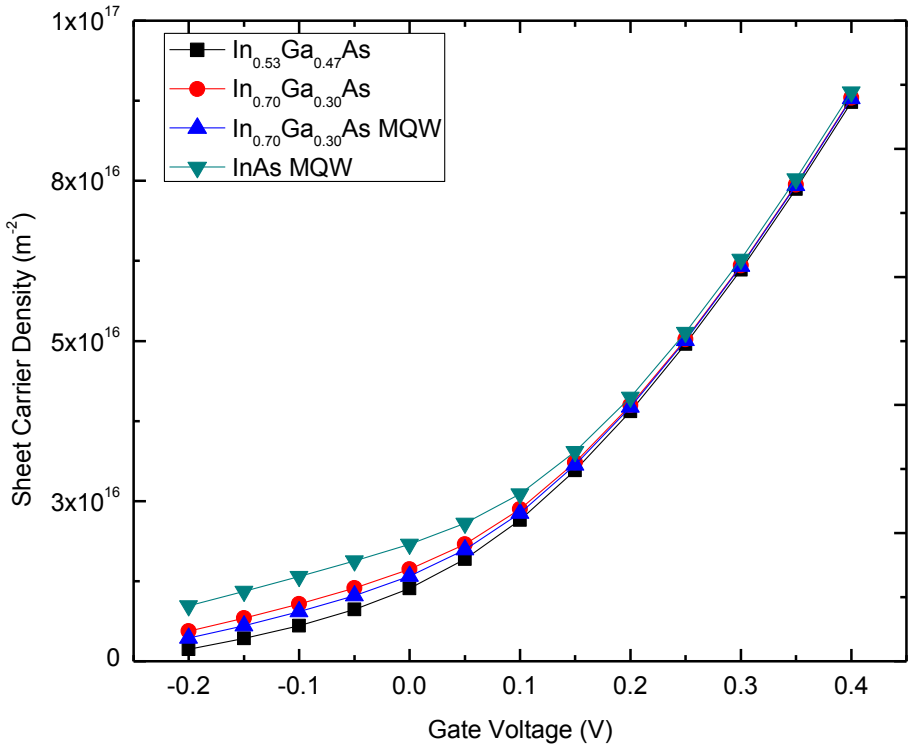


Figure 4.16: Sheet carrier density of generic HEMT for different channel contents

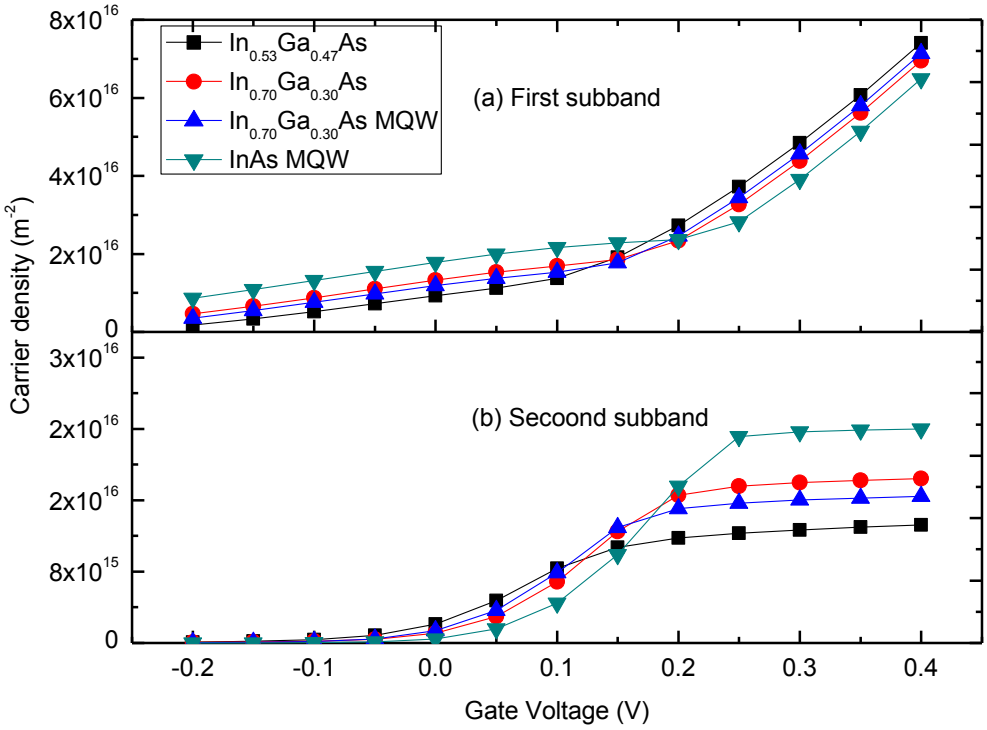


Figure 4.17: Comparison of (a) first and (b) second subband charge densities for HEMTs

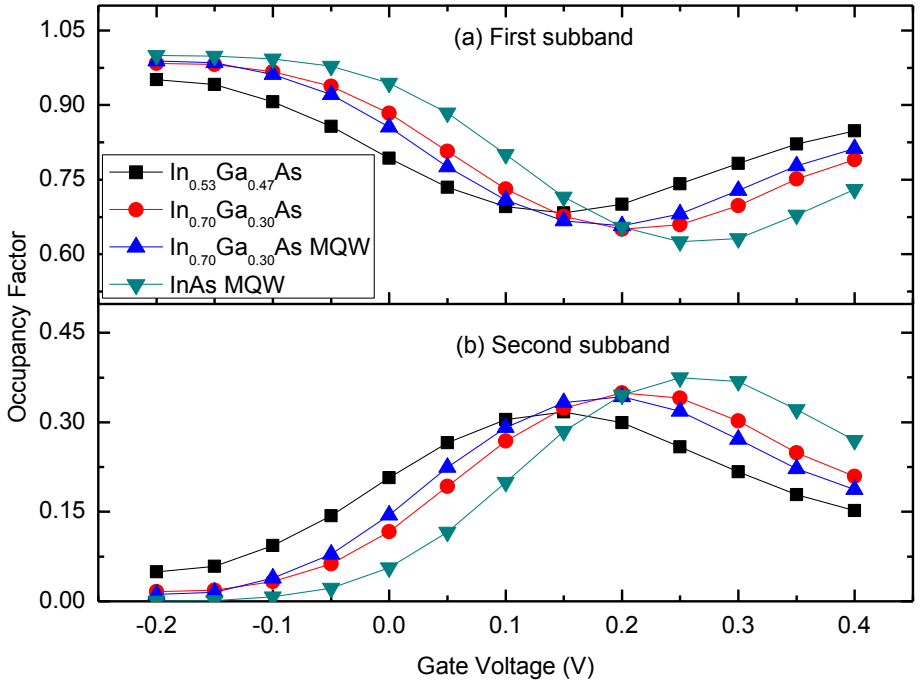


Figure 4.18: Occupancy factor of generic HEMT for different channel contents

At high gate bias the contribution of the first subband again increases whereas the carrier contribution of the second subband decreases. Hence the HEMT operation is dominated by the contribution of the first subband at low and high gate bias whereas at moderate bias both the subbands contribute significantly.

4.1.4 C-V characteristics

The gate capacitances for all the types of HEMTs in this discussion are shown as function of gate voltage in Fig. 4.19 and 4.20. As can be seen, for all the HEMTs the gate capacitance increases with gate voltage. Because delta doping or spacer layer does not significantly change the sheet carrier density, the gate capacitance is not also much influenced by the addition of delta doping or spacer layer. The voltage range here is chosen in Fig. 4.19 and Fig. 4.20 is such that the device does not go deep into the region of parallel conduction.

To compare the gate capacitance for different channel materials, the C-V curves are shown in the same plot in Fig. 4.21. According to this figure though the sheet carrier density of $In_{0.53}Ga_{0.47}As$ HEMT is low compared to others (Fig. 4.16), the device shows a higher gate capacitance i.e. a higher rate of charge buildup.

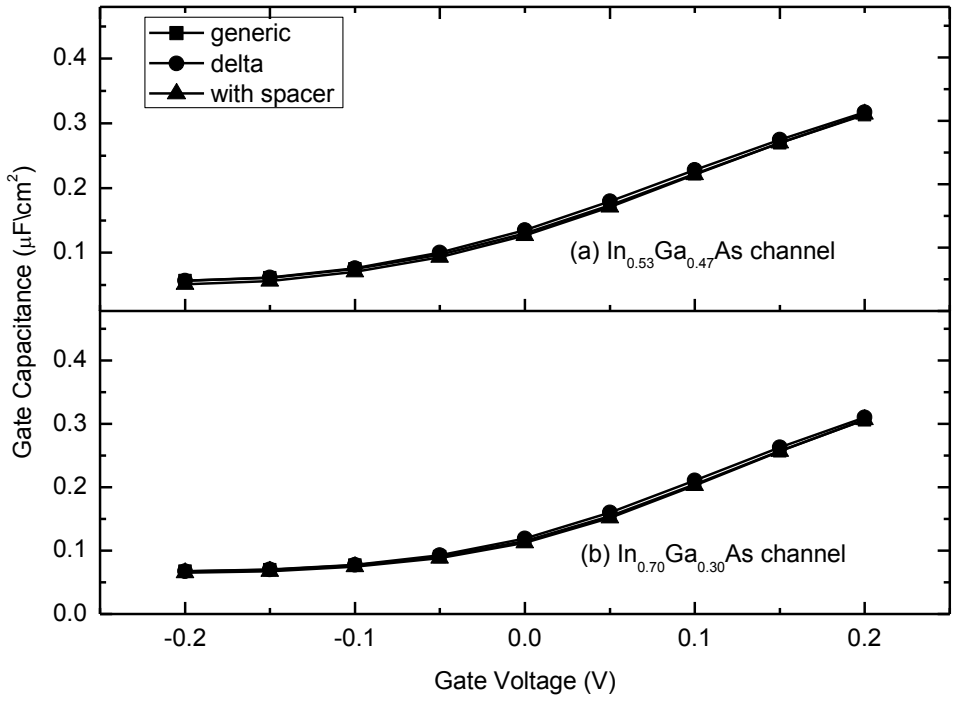


Figure 4.19: Gate capacitance of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ channel HEMTs

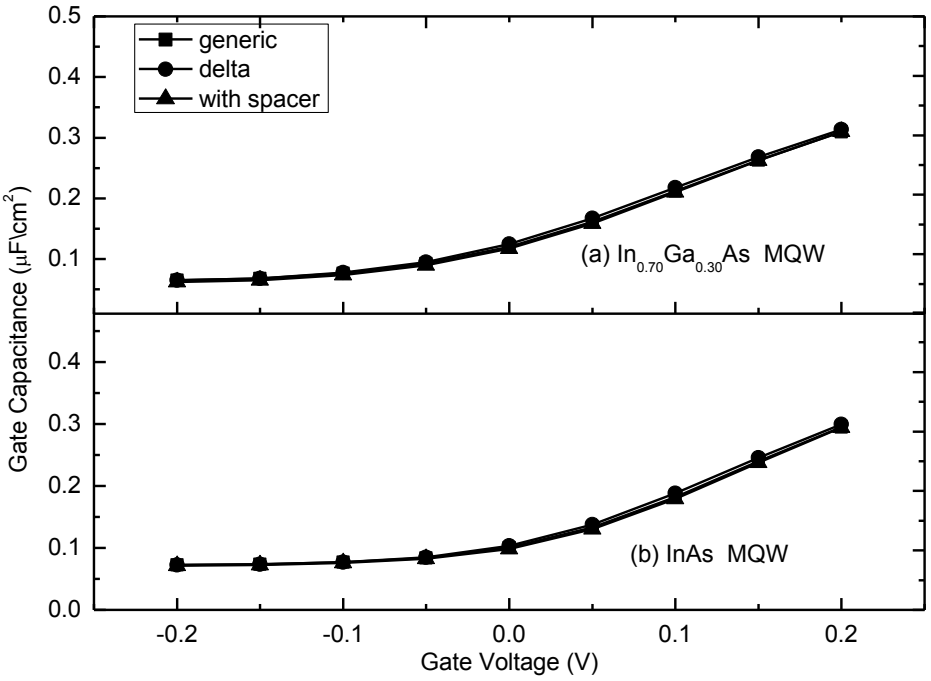


Figure 4.20: Gate capacitance of (a) $In_{0.70}Ga_{0.30}As$ MQWand (b) InAs MQW HEMTs

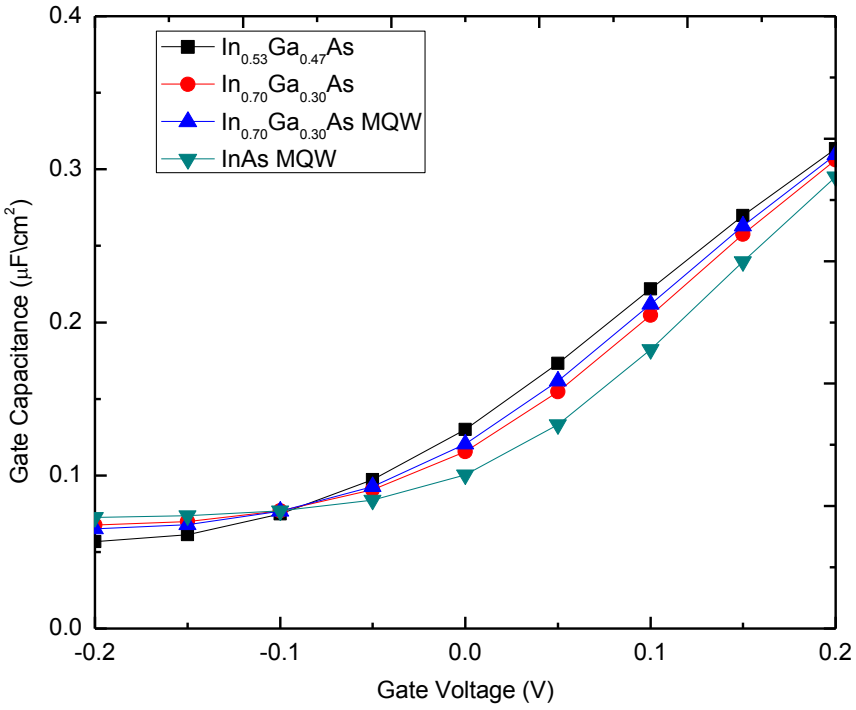


Figure 4.21: Gate capacitance of generic HEMT for different channel contents

According Fig. 4.21, InAs MQW HEMT has a high gate capacitance in comparison with others at low gate bias (within -0.2V and -0.1V). However above -0.1V its rate of charge buildup i.e. gate capacitance is significantly low when compared with other channel HEMTs. This can be related to the fact that the InAs MQW HEMT reaches V_{Emin} at a higher voltage than other HEMTs. The higher rate of charge buildup of $In_{0.53}Ga_{0.47}As$ HEMT increases carrier concentration in both the barrier and channel layer at a greater rate and thus drives the device into the regime of parallel conduction.

To further analyze the C-V characteristics, the quantum capacitance corresponding to the first and second subbands of $In_{0.53}Ga_{0.47}As$ and $In_{0.70}Ga_{0.30}As$ channel HEMTs are shown in Fig. 4.22. The quantum capacitances have been calculated according to the model described in chapter 2. Because the contribution of higher subbands has been found negligible, only the first two have been considered in this discussion.

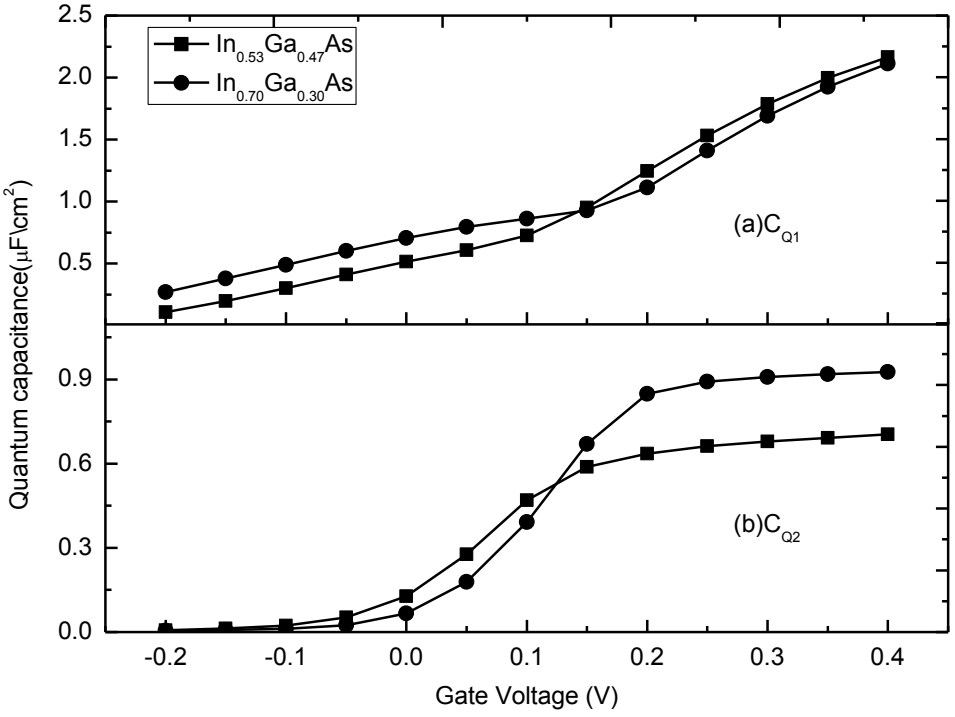


Figure 4.22: Quantum capacitance of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ HEMT

According to Fig.4.22 (a), the value of first subband quantum capacitance (C_{Q1}) is always higher than the second (C_{Q2}). It is notable that at around V_{Emin}=0.1V of $In_{0.53}Ga_{0.47}As$ HEMT, its value of C_{Q1} becomes smaller than the C_{Q1} of $In_{0.70}Ga_{0.30}As$ HEMT. On the other hand at around V_{Emin}=0.15V of $In_{0.70}Ga_{0.30}As$ HEMT, its value of C_{Q2} of becomes smaller than the C_{Q2} of $In_{0.53}Ga_{0.47}As$ HEMT.

Another component of the quantum capacitance model, the centroid capacitance, is shown in Fig.4.23 for the first and second subbands. The first subband centroid capacitance (C_{Cent1}) is large than the centroid capacitance of the second subband (C_{Cent2}) for all the gate voltages. In fact the values of both C_{Cent1} and C_{Cent2} are of higher order compared to the C_{Q1} and C_{Q2} values of Fig. 4.22. The impact of V_{Emin} is also visible in Fig. 4.23. For gate voltages greater than $V_{Emin,}$ the rate of change of C_{Q2} decreases for both the devices whereas C_{Q1} rises more sharply beyond the V_{Emin} of respective devices. Thus the capacitive component of the QC model is dominated by the nature of energy quantization in these highly scaled HEMTs.

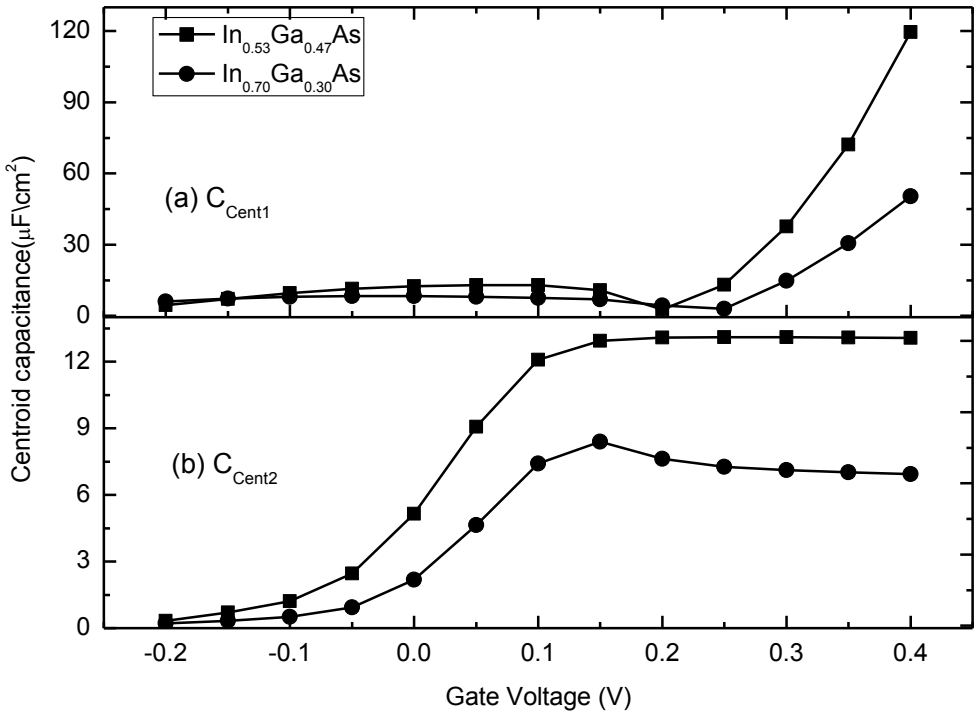


Figure 4.23: Centroid capacitance of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ HEMTs

According to the QC model, the inversion capacitance corresponding to each subband is the series combination of quantum capacitance and centroid capacitance. It is known that the series equivalence of two capacitors is always less than the smaller of the two. Because here C_{Q1}<<C_{Cent1} and C_{Q2}<<C_{Cent2}, so the first and second subband inversion capacitances should be in the order of C_{Q1} and C_{Q2}. This is the case as can be observed from the plots of first (C_{inv1}) and second (C_{inv2}) subband inversion capacitances in Fig. 4.24. In fact the C_{inv1} and C_{inv2} versus gate voltage curves qualitatively follow the nature of C_{Q1} and C_{Q2}. Hence quantum capacitances corresponding to the first and second subband eigen states are the most contributing elements of the QC model.

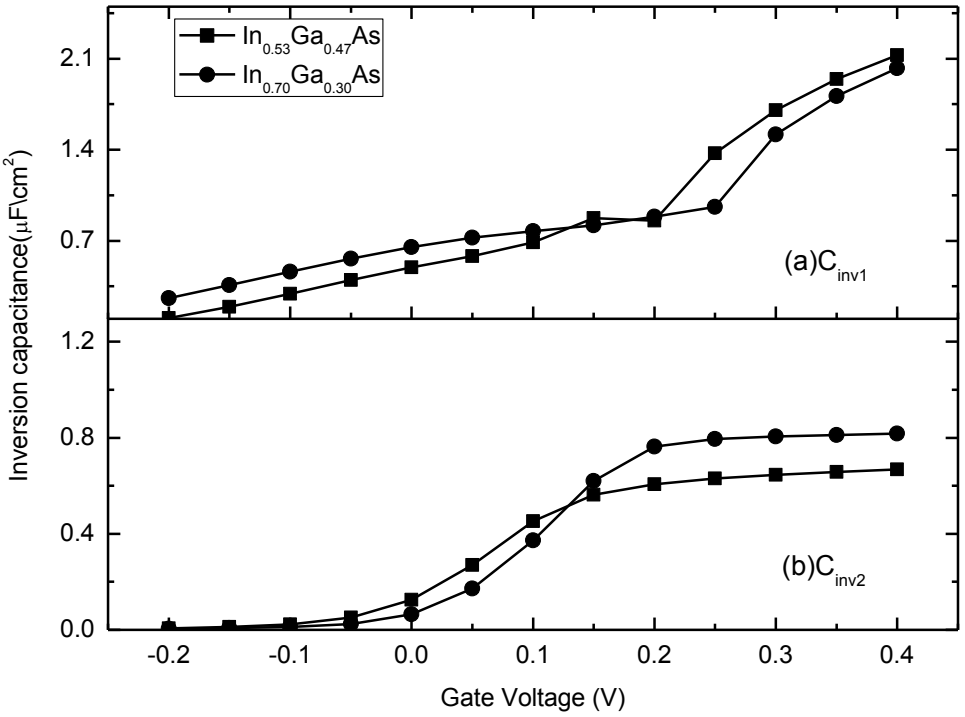


Figure 4.24: Subband inversion capacitances of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ channel HEMTs

The sum of C_{inv1} and C_{inv2} gives the macroscopic inversion capacitance, which can also be obtained by differentiating the charge density with respect to surface potential of the device. The total inversion capacitance derived from the QC model is shown for both the $In_{0.53}Ga_{0.47}As$ and $In_{0.70}Ga_{0.30}As$ channel HEMTs in Fig. 4.25. Both C_{inv1} and C_{inv2}

are found to increase with gate voltage. Also notable are the kinks near the V_{Emin} of the respective devices. Because the $In_{0.53}Ga_{0.47}As$ channel HEMT starts parallel conduction

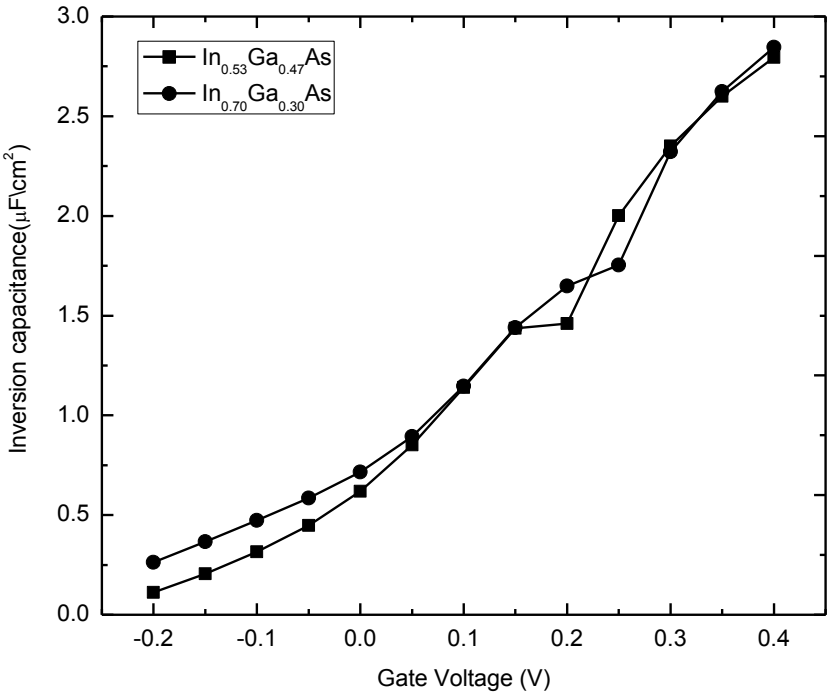


Figure 4.25: Inversion capacitance of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ HEMTs

at a lower voltage than the $In_{0.70}Ga_{0.30}As$ channel HEMT, the kink in the inversion capacitance versus gate voltage curve also appears at a lower bias. Hence from the C_{inv} versus V_{gb} relation of this highly scaled HEMTs the onset of parallel conduction can be predicted.

4.2 Transport Characteristics

The transport characteristics discussed in this section include the current voltage (I-V) relations, channel conductance, ballistic and effective mobility. The drain to source voltage considered here is 0 to 0.60V, which is within the experimental range of highly scaled devices.

4.2.1 Current-voltage relation

In Fig. 4.26 and 4.27 the drain to source current of for all the HEMTs has been shown as a function of the drain to source current for the generic, delta doped and spacer

layered cases. The gate voltage considered here -0.05V, which is smaller than the V_{Emin} of all the devices considered. This ensures that the I-V curves represent the HEMT operation of all the devices. According Fig. 4.26, for both $In_{0.53}Ga_{0.47}As$ and $In_{0.70}Ga_{0.30}As$ channel HEMTs the on-state current increases when delta doping is added to the generic case. This indicates that the slight increase of carrier density by delta doping (discussed in 4.2.2) contributes to the increase of on-state current in these devices.

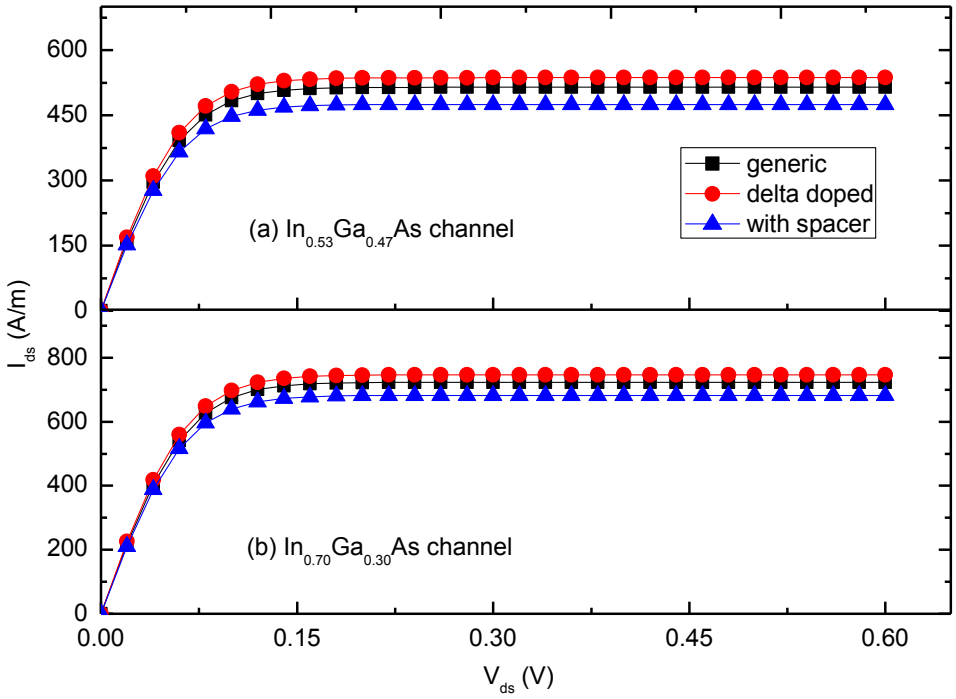


Figure 4.26: Drain-to-source current of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ HEMTs

On the contrary, the decrease of carrier density caused by the addition of spacer layer (also discussed in 4.2.2) causes the drain current to decrease compared to the generic cases. Similar is the case for the MQW HEMTs shown in Fig. 4.27, i.e. the drain current decreases in these devices as well if a spacer layer is added in between the barrier and the channel layer. However any increase of the drain current by the addition of delta-doping is unnoticeable. This happens because delta doping has comparatively less impact on the increase of carrier density in MQW structures than in single channel HEMTs.

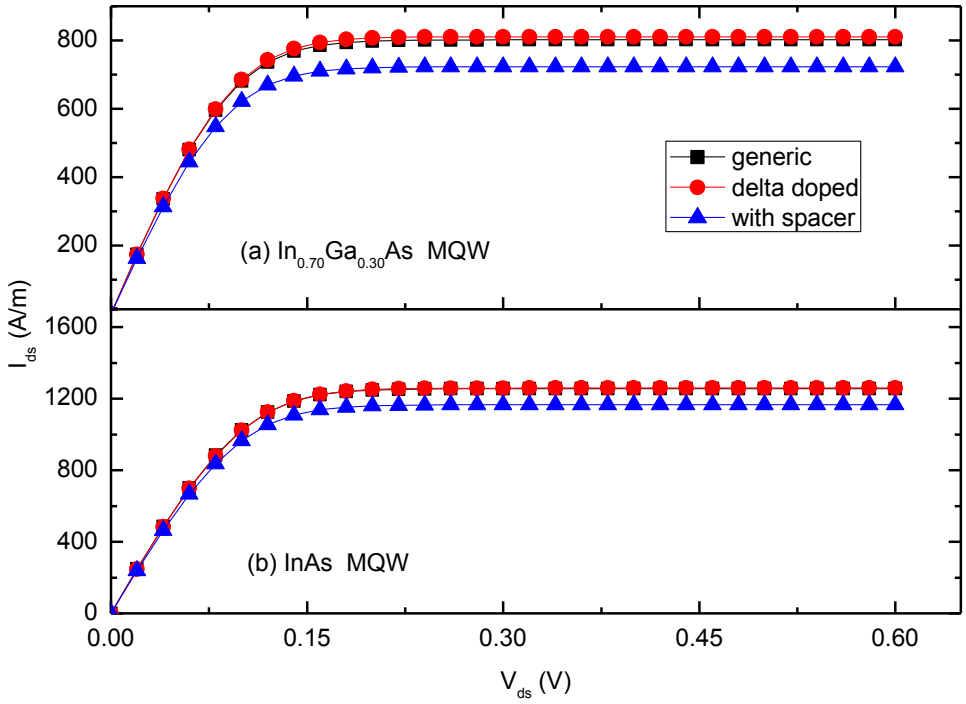


Figure 4.27: Drain current of (a) $In_{0.70}Ga_{0.30}As$ MQW and (b) InAs MQW HEMTs

In Fig. 4.28 and 4.29, the on-state currents of different channel HEMTs are shown as a function of gate voltage. The increase of on-state current by delta doping and the decrease by the addition of spacer layer for $In_{0.53}Ga_{0.47}As$ and $In_{0.70}Ga_{0.30}As$ channel HEMTs can be observed in Fig. 4.28. As can be seen from Fig. 4.28(a), for all the cases of $In_{0.53}Ga_{0.47}As$ channel HEMT, there is a kink at around 0.10V. Similarly for $In_{0.70}Ga_{0.30}As$ channel HEMTs, a kink is visible at around 0.15V (Fig. 4.28(b)). These voltages are actually equal to the V_{Emin} values of the respective devices. Hence beyond these values of gate voltage, the current actually corresponds to parallel conduction. Hence from the on-state current versus gate voltage relation of these devices it is possible to identify the onset of parallel conduction.

As in Fig. 4.29, for the delta doped case of MQW HEMTs, the on-state current versus gate voltage relation actually overlaps with the generic case. This again shows that delta doping has less impact on increasing the current in MQW HEMTs. For the spacer layered cases of however, the current decreases just as in single channel HEMTs.

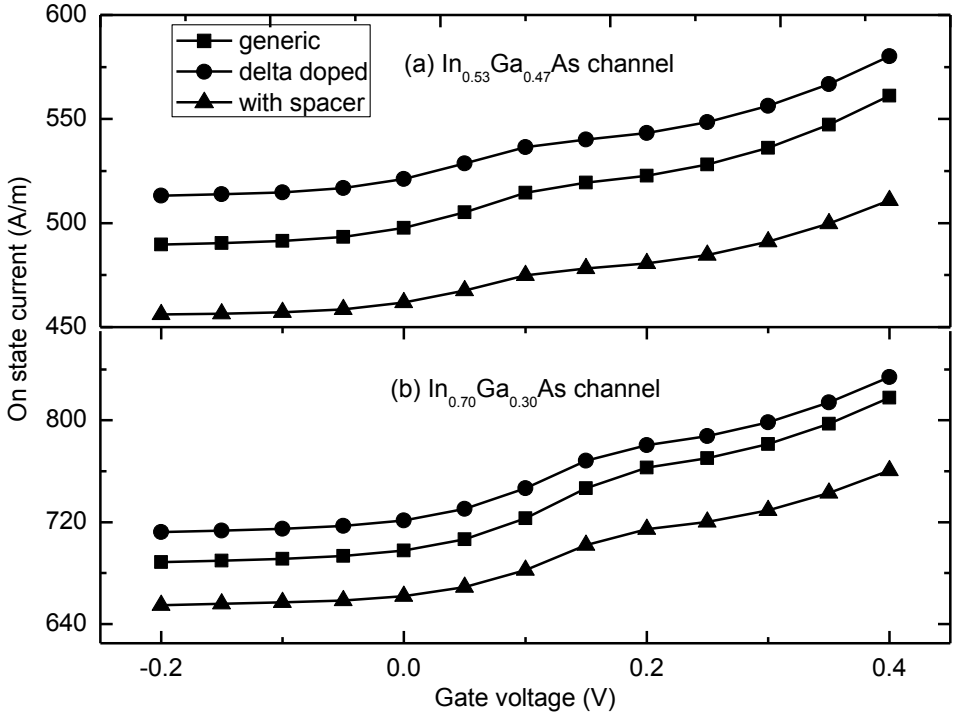


Figure 4.28: On-state current of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ channel HEMTs as a function of gate voltage

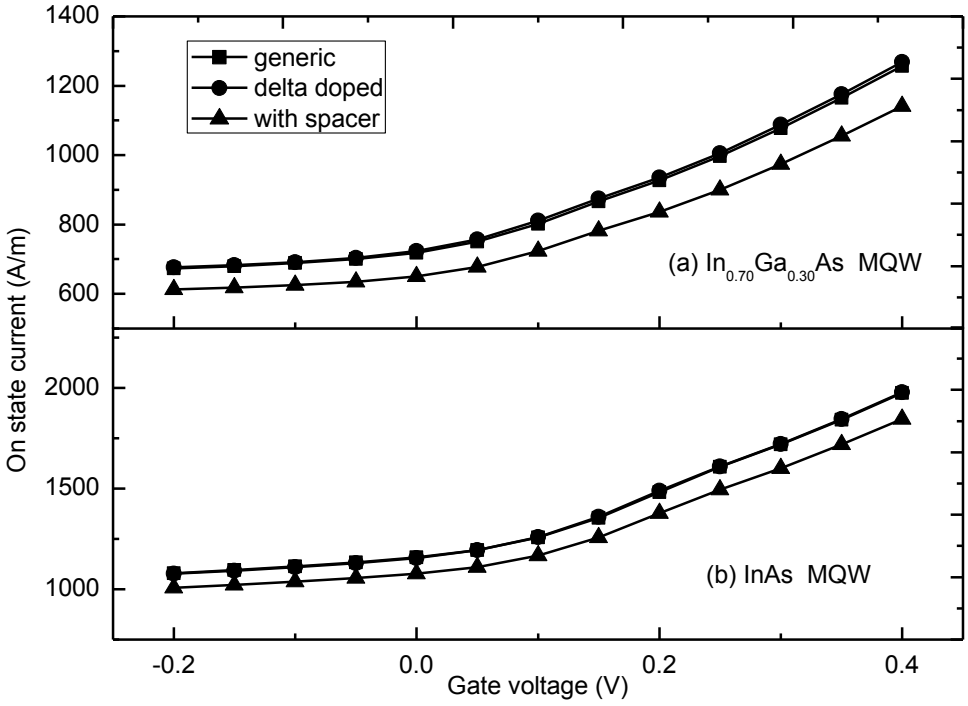


Figure 4.29: On-state current of (a) $In_{0.70}Ga_{0.30}As$ MQW and (b) InAs MQW HEMTs as a function of gate voltage

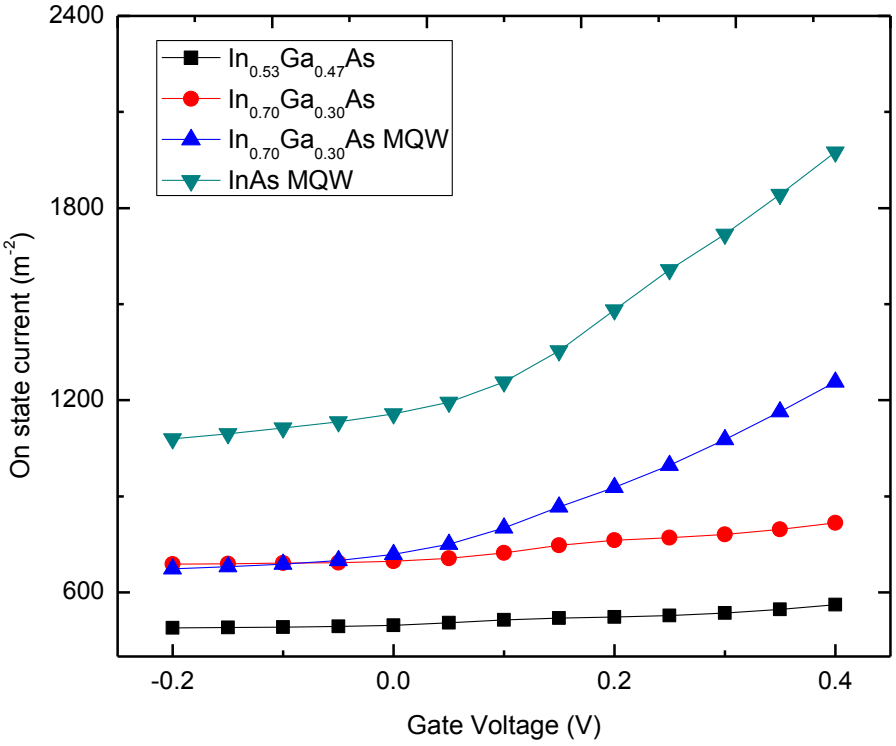


Figure 4.30: On-state current of different channel HEMTs as a function of gate voltage

In Fig. 4.30, the on-state current of different channel HEMTs are shown in the same plot for comparison purpose. For InAs MQW HEMT, the current is more than twice as high when compared with other HEMTs. For $In_{0.70}Ga_{0.30}As$ as channel material, though the currents are the same for single channel and MQW channel HEMTs up to zero gate bias, the value increases substantially in MQW HEMTs when higher gate bias. This shows that the multi-quantum-well structure can provide higher current than its single well variant.

4.2.2 Channel-conductance

The channel-conductance (g_{DS}) under low-drain bias is defined as [60]:

$$g_{DS} = \frac{\partial I_{DS}}{\partial V_{DS}} | V_{DS=0}$$

The value of g_{DS} has been shown in Fig. 4.31 and 4.32 for all cases of HEMTs being considered in this study. According Fig 4.31, for both $In_{0.53}Ga_{0.47}As$ and $In_{0.70}Ga_{0.30}As$

channel HEMTs the value of g_{DS} increases if the device is delta doped. On the contrary, g_{DS} decreases considerably when spacer layer is added to the generic structure.

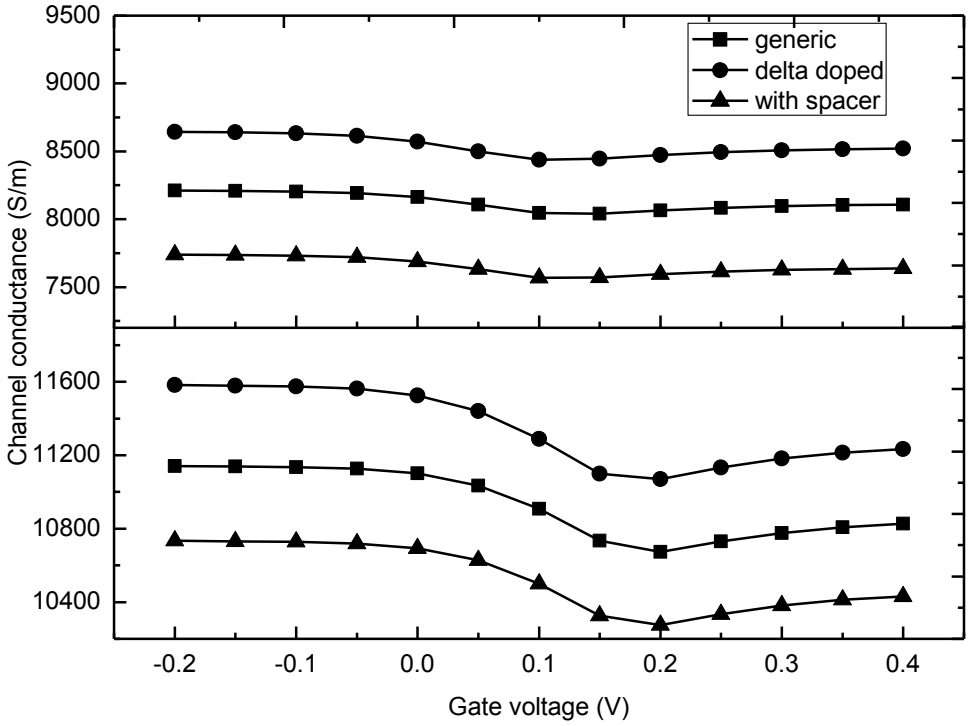


Figure 4.31: Channel conductance of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ channel HEMTs as a function of gate voltage

For the MQW structures shown in Fig. 4.32, delta doping however does not significantly influence channel-conductance. The addition of spacer layer however decreases g_{DS} for the MQW structures just as in single material channel HEMTs. These results are very much in conformation with the previously discussed I-V relations.

It can be seen that the g_{DS} versus gate voltage curves for both the single channel HEMTs mentioned in Fig.4.31 decreases up to two different minima. For the $In_{0.53}Ga_{0.47}As$ channel HEMT the voltage of these minima is around 0.1V whereas for the $In_{0.70}Ga_{0.30}As$ channel HEMT the minima voltage is around 0.15V. Because these values are respectively equal to V_{Emin} of the devices, beyond these voltage the channel conductance actually represent the conductance including the parallel conduction path.

Fig. 4.31 indicates that for both these devices the value of g_{DS} increases at gate voltages higher than $V_{Emin.}$ Hence for single material channel HEMTs the conductivity increases with the onset of parallel conduction.

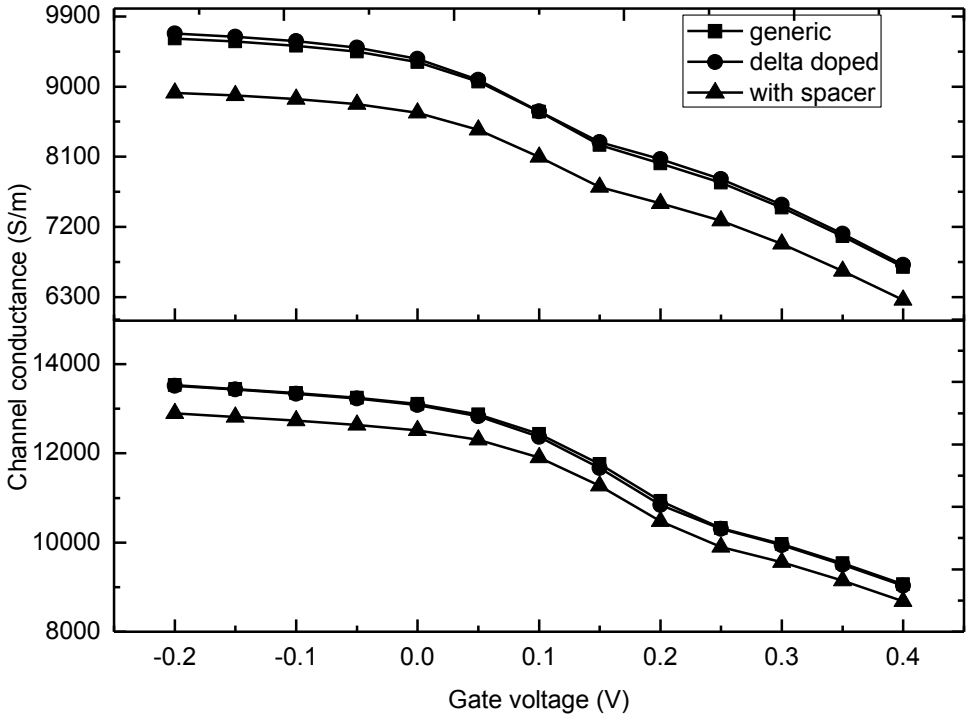


Figure 4.32: Channel conductance of (a) $In_{0.70}Ga_{0.47}As$ MQW and (b) InAs MQW HEMTs as a function of gate voltage

The channel conductance curves for the MQW HEMTs shown in Fig. 4.32 however indicate that the value of g_{DS} decreases for both the devices even for gate voltages higher than their V_{Emin} values. Though there are obvious kinks around the V_{Emin} of the respective devices, the value of g_{DS} continues to decrease, unlike the case of the single material channel HEMTs. This indicates that even after parallel conduction starts, the overall channel conduction decreases in MQW HEMTs. Hence MQW HEMTs should be less vulnerable to the phenomenon of parallel conduction.

The value of channel conductance for generic HEMTs of all channel types are shown in Fig. 4.33. The InAs MQW HEMT shows higher channel conductance compared to the three other devices for all gate biases shown in the figure. This indicates that for a fixed

gate bias, the InAs MQW HEMT responses more rapidly to the change of drain voltage when compared with other devices of this study. Fig. 4.33 also shows that the value of g_{DS} is lower for the MQW $In_{0.70}Ga_{0.30}As$ HEMT when compared with its single channel variant. Hence the MQW structure in effect reduces channel conductivity. However it is notable that for both the MQW HEMTs the channel conductance decreases rapidly

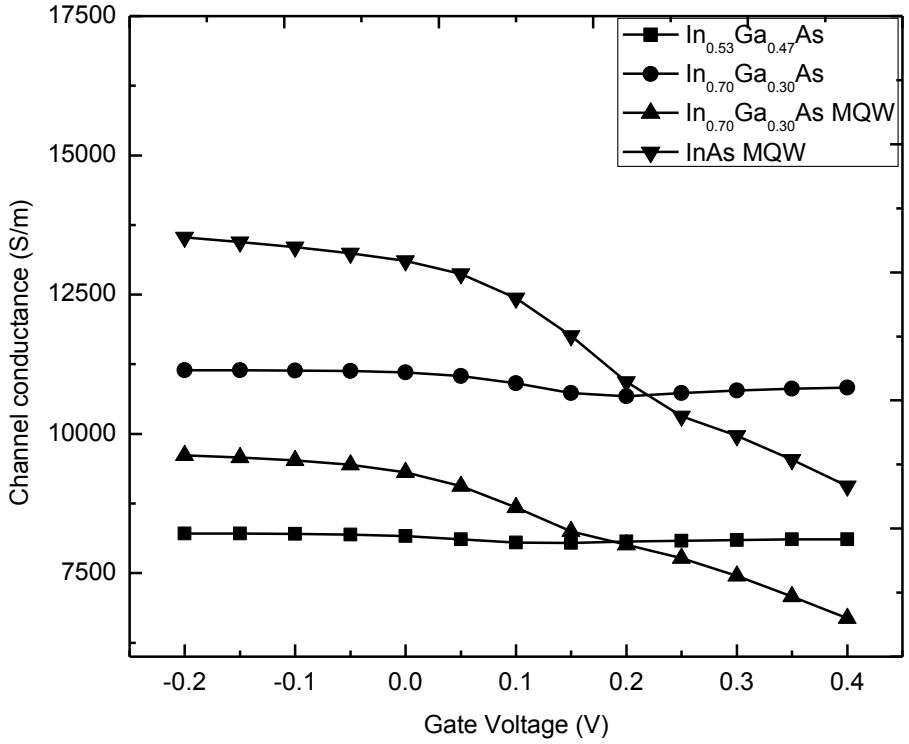


Figure 4.33: Channel conductance of different HEMTs as a function of gate voltage

beyond the respective V_{Emin} values, whereas for the single material channel devices the value of g_{DS} increases slightly beyond the V_{Emin} values. This indicates that the MQW HEMTs are more prohibitive to parallel conduction compared to the conventional single well HEMTs.

4.2.3 Mobility

The nonphysical ballistic mobility (together with the Mathiessen's rule) allows conventional FET I-V characteristics to be used under low drain bias [60]. The physical mobilities of the channel materials used in this study are shown in Table 4.3. These

values, which have been obtained from [73], indicate that higher Indium content results higher mobility. To characterize ballistic transport characteristics, the nonphysical ballistic mobilities for all the HEMTs are shown as a function of gate voltage in Fig. 4.34 and 4.35. Both the figures are drawn in logarithmic scale.

Table 4.3: Physical mobility for different channel HEMTs

HEMT types	Channel Materials	Physical Mobility (cm^2/Vs)
$In_{0.53}Ga_{0.47}As$ HEMT	$In_{0.53}Ga_{0.47}As$	$1.5x10^4$
$In_{0.70}Ga_{0.30}As$ HEMT	$In_{0.70}Ga_{0.30}As$	$2.0x10^4$
$In_{0.70}Ga_{0.30}As$ MQW HEMT	$In_{0.53}Ga_{0.47}As$	$1.5x10^4$
	$In_{0.70}Ga_{0.30}As$	$2.0x10^4$
	$In_{0.53}Ga_{0.47}As$	$1.5x10^4$
InAs MQW HEMT	$In_{0.53}Ga_{0.47}As$	$1.5x10^4$
	InAs	$3.3x10^4$
	$In_{0.53}Ga_{0.47}As$	$1.5x10^4$

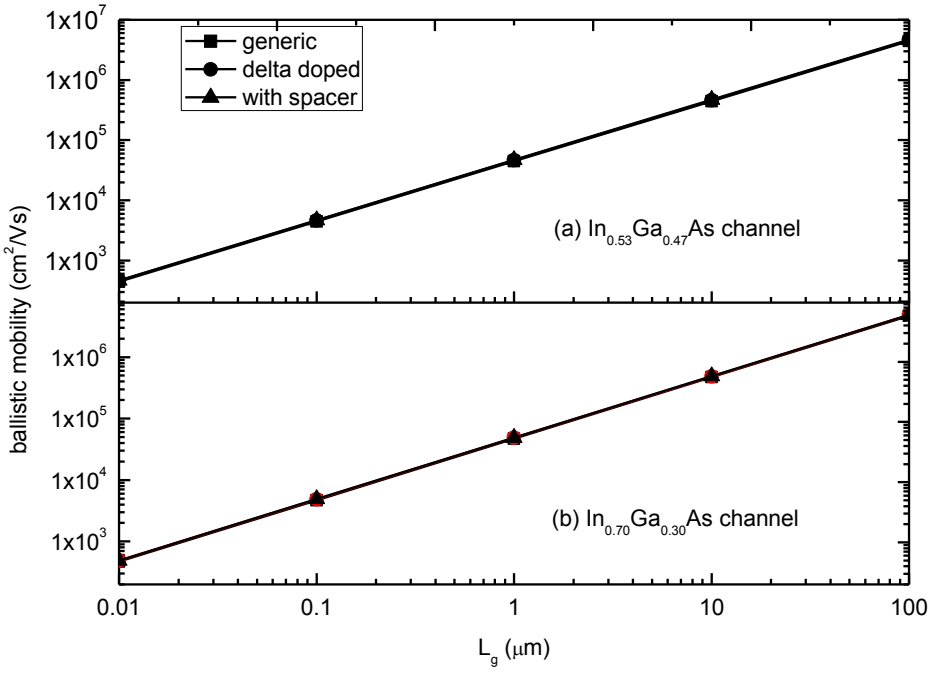


Figure 4.34: Ballistic mobility of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ channel HEMTs as a function of gate length

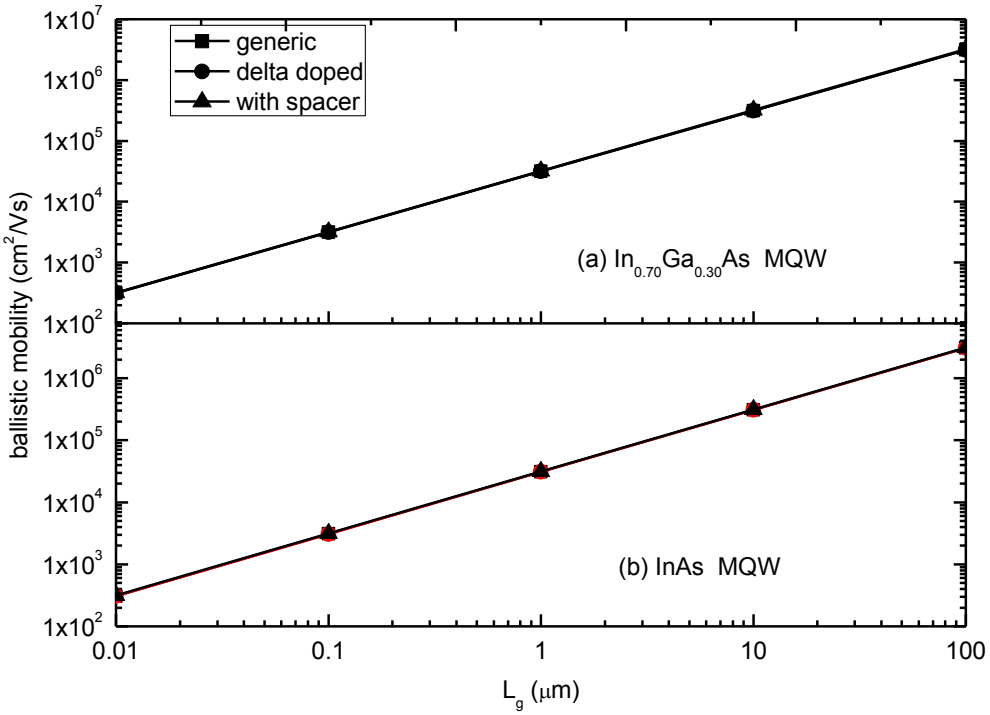


Figure 4.35: Ballistic mobility of (a) $In_{0.70}Ga_{0.30}As$ MQW and (b) InAs MQW HEMTs as a function of gate length

As can be seen in Fig.4.34 and 4.35, when the channel is long, the ballistic mobility is much larger than the physical mobility values shown in Table 4.3. However when the channel is very short compared to the electron's free mean path, the ballistic mobility is much smaller than the physical mobility. Fig. 4.34 and 4.35 also shows that delta doping and spacer layer does not apparently bring about any significant change in ballistic mobility of the device.

To further analyze the case, the ballistic mobilities at a gate length of 0.01 μm for all the devices are shown in Table 4.4. According to the table, delta doping increases the ballistic mobility of both $In_{0.53}Ga_{0.47}As$ and $In_{0.70}Ga_{0.30}As$ HEMTs whereas for MQW HETMs, the impact of delta doping on ballistic mobility is negligible. On the other hand, the addition of spacer layer increases the ballistic mobility for all the HEMTs.
This happens because the spacer layer reduces ionized impurity scattering by reducing the diffusion of dopants into the channel layer.

Table 4.4: Ballistic mobility (in units of cm^2/V-s) for a gate length of 0.01 μm

HEMT types	Generic	Delta doped	Spacer layered
$In_{0.53}Ga_{0.47}As$ HEMT	445.1842	461.97719	470.16259
$In_{0.70}Ga_{0.30}As$ HEMT	470.29842	486.72724	489.36516
$In_{0.70}Ga_{0.30}As$ MQW HEMT	314.56127	314.15796	320.48065
InAs MQW HEMT	309.36005	308.90939	313.91347

Table 4.4 also shows that the ballistic mobility is the highest for $In_{0.70}Ga_{0.30}As$ HEMTs and lowest for InAs MQW HEMTs. This case is further illustrated in Fig. 4.36 by the ballistic mobility vs. gate length relations obtained for different channel contents of a generic HEMT.

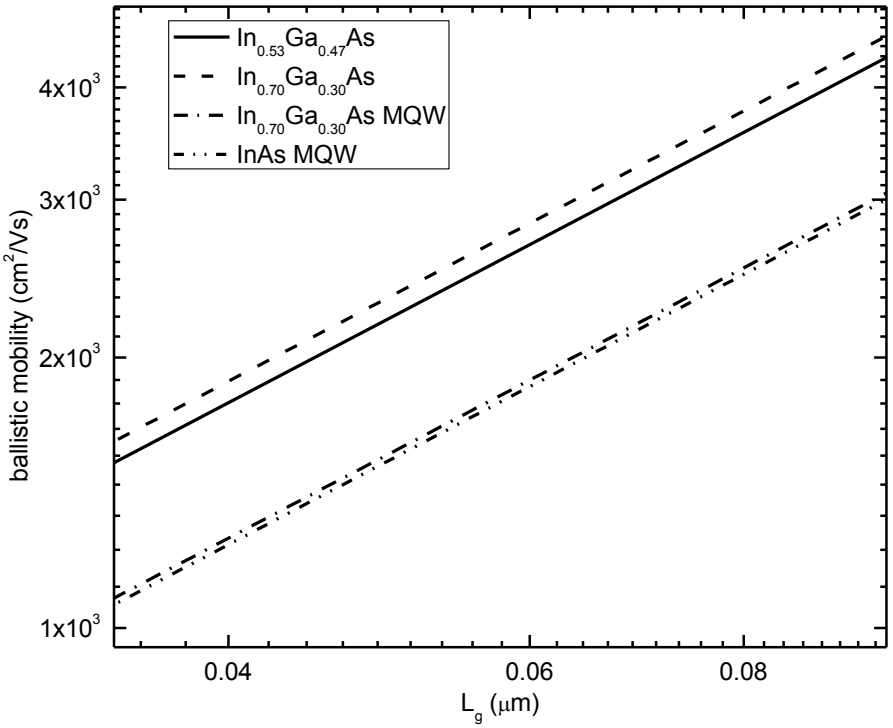


Figure 4.36: Ballistic mobility of different channel HEMTs as a function of gate length

According Fig. 4.36, ballistic mobility of $In_{0.70}Ga_{0.30}As$ channel HEMT is always higher than that of $In_{0.53}Ga_{0.47}As$ channeled ones. This though indicates that the increase of Indium content should increase ballistic mobility, it is not the case for MQW HEMT structures. As can be seen from Fig. 4.36, in spite of having $In_{0.70}Ga_{0.30}As$ in the channel

layer, the ballistic mobility of $In_{0.70}Ga_{0.30}As$ MQW HEMT is lower even than the $In_{0.53}Ga_{0.47}As$ channel case. Hence multiple quantum wells though provide increased carrier confinement, they can reduce ballistic mobility when compared to the single channel cases.

It is known that in the quasi ballistic regime the mobility used in the conventional device equations is replaced by the effective which is calculated using the Mathiessen's rule. The effective mobility for the generic, delta doped and spacer layered cases of the HEMTs are shown in Fig. 4.37 and 4.38. According to these figures, the effective mobilites for all the devices are equal to their respective ballistic mobilities in the short channel length regime of operation. Hence the experimentally measured mobilities for such highly scaled devices should be equal to the ballistic mobility, not the physical mobility. This effect is not very important in silicon devices because the mobility there is relatively low. However it is significant for devices like HEMTs where the electron mobility is considerably high.

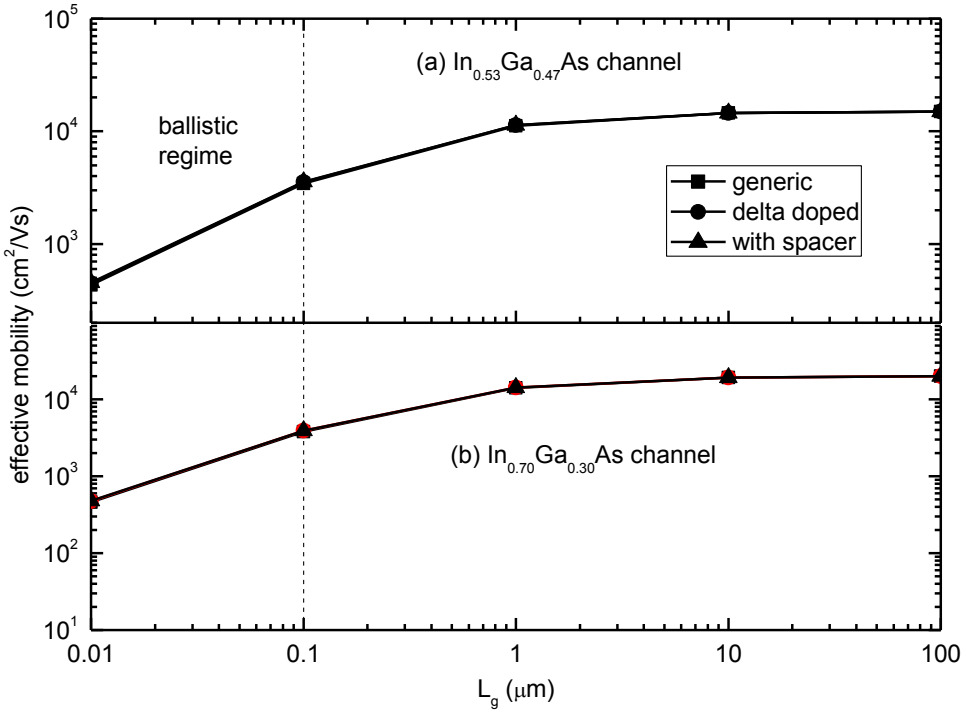


Figure 4.37: Effective mobility of (a) $In_{0.53}Ga_{0.47}As$ and (b) $In_{0.70}Ga_{0.30}As$ channel HEMTs as a function of gate length

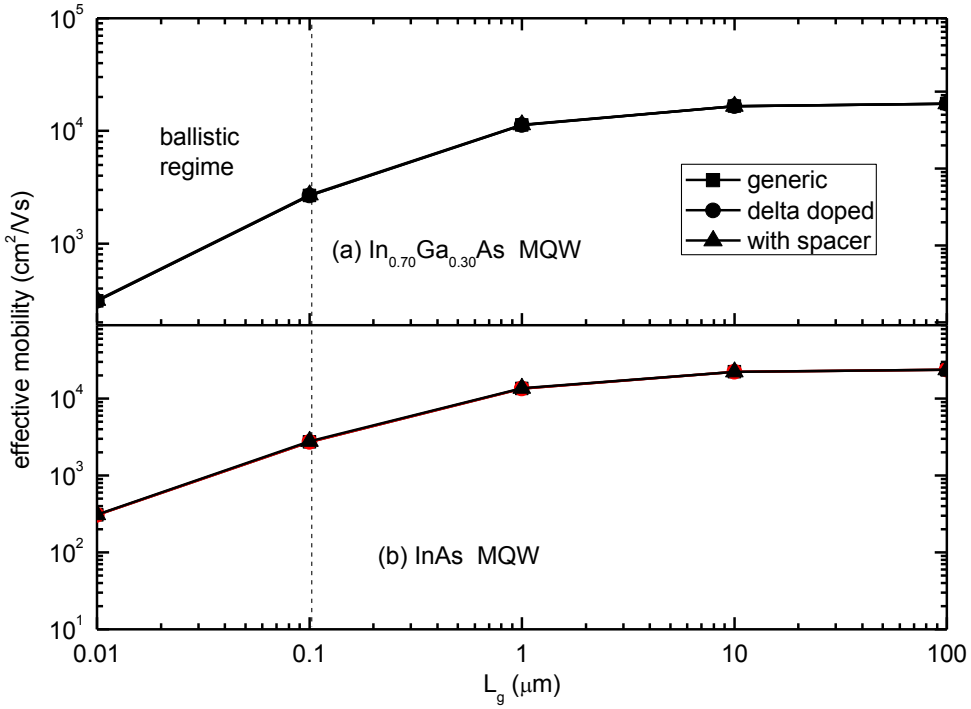


Figure 4.38: Effective mobility of (a) $In_{0.70}Ga_{0.30}As$ and (b) InAs MQW HEMTs as a function of gate length

In Fig. 4.39 the effective mobility of different channel HEMTs are shown in the same plot. The figure shows that the effective mobilities of MQW HEMTs are less than the effective mobilities of the single channel HEMTs for up to the gate length 0.1 μm. This relationship is very much similar to the ballistic mobility relation shown in Fig. 4.36. Hence for highly scaled HEMTs, the effective mobility is essentially ballistic for up to gate lengths of 0.1 μm. It has been reported earlier that highly scaled silicon devices operate in the ballistic regime at sub 0.02 μm gate length [75]. Hence HEMTs can provide ballistic transport at much higher gate lengths compared to silicon FETs. Also noteworthy from Fig. 4.39 is that the InAs MQW HEMT shows the highest effective

Table 4.5: Effective mobility (in units of cm^2/V-s) for a gate length of 10 μm

HEMT types	Generic	Delta doped	Spacer layered
$In_{0.53}Ga_{0.47}As$ HEMT	11219.6577	11323.39237	11371.9192
$In_{0.70}Ga_{0.30}As$ HEMT	14032.5087	14175.27107	14197.5599
$In_{0.70}Ga_{0.30}As$ MQW HEMT	11244.3989	11239.24125	11319.1330
InAs MQW HEMT	22272.13849	22269.79946	22295.42159

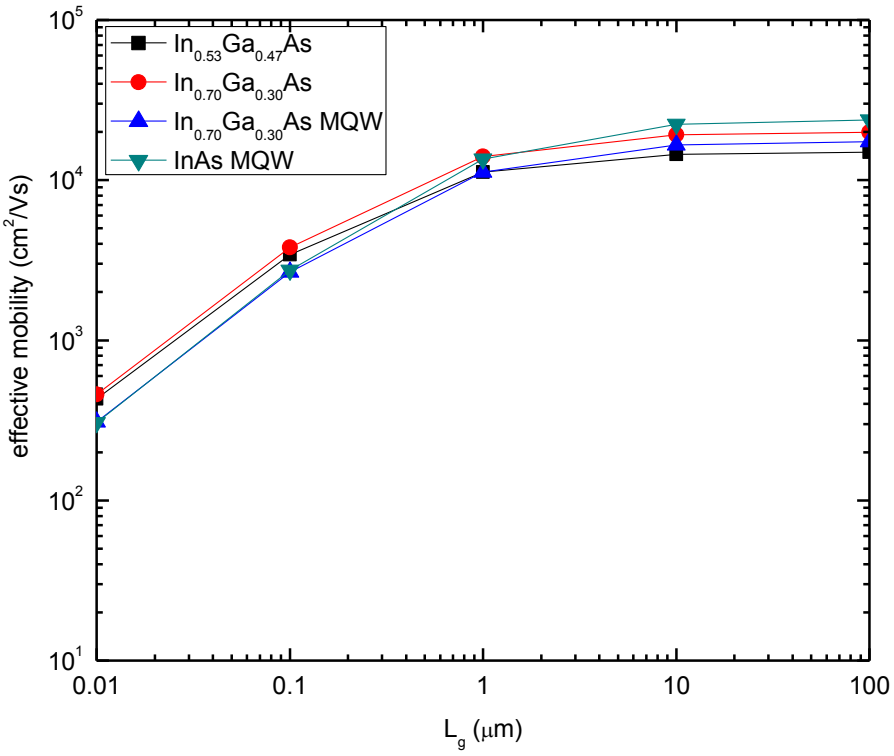


Figure 4.39: Effective mobility of different channel HEMTs as a function of gate length

mobility at high gate lengths compared to other devices. This is because at long channel the ballistic mobility is much larger compared to physical mobility and so the effective mobility reduces to the physical mobility of Table 4.3, according to which the mobility of InAs is the highest. The effective mobility can be increased further by delta doping or spacer layer in the long gate length regime, as shown with values in Table 4.5.

4.3 Strain Effects

In this section influence of strain on the electrostatic and transport characteristics of highly scaled HEMTs is discussed with illustrations. All the results discussed here correspond to the strained and unstrained cases of the InAs MQW generic HEMT.

4.3.1 Electrostatic effects

In Fig. 4.40 the energy band diagram and carrier profiles of InAs MQW generic HEMT are shown for the strained and unstrained cases. The figure shows that strain increases

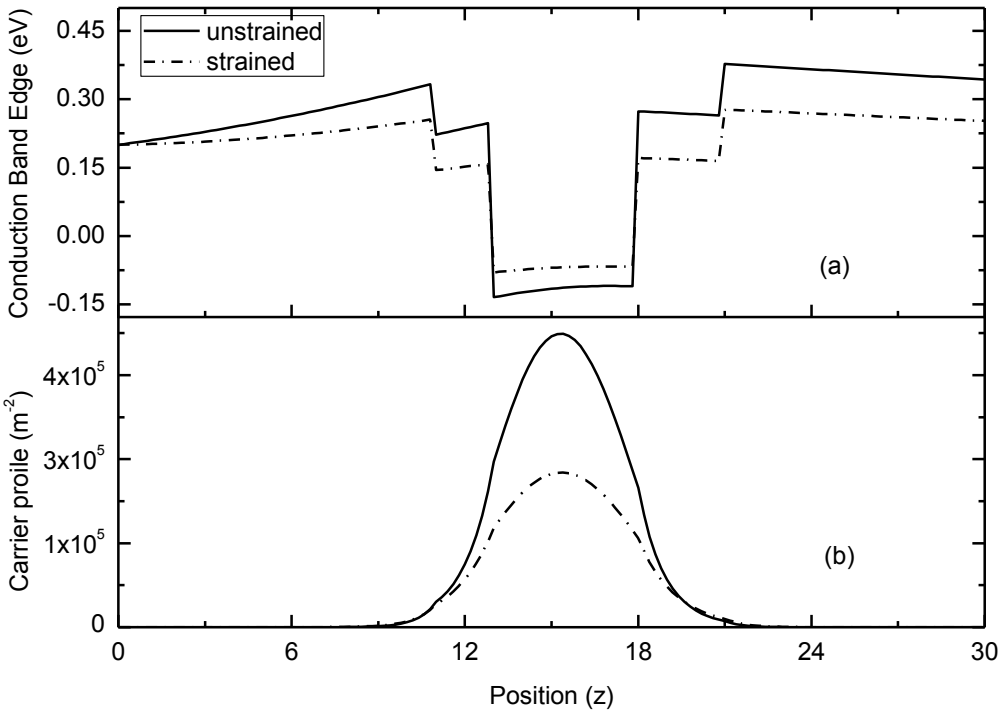


Figure 4.40: Strain effects on conduction band energy and carrier distribution profile

energy of the bottom of the conduction band, which in effect decreases the depth of the quantum well. This in effect reduces quantum mechanical confinement and thus carrier quantization inside the channel layer. This is why the peak carrier concentration is higher in the unstrained device compared to the carrier concentration of the strained device as shown in Fig. 4.40 (b).

Because of the difference of magnitude in carrier profile, the net sheet carrier density in the strained device is also lower compared to the carrier density of the unstrained device (Fig. 4.41). The difference is particularly prominent at low gate bias. At high gate bias (above 0.20V) however, the sheet carrier densities closely match each other. This happens because at voltages greater than V_{Emin}, the carrier concentration in the barrier layer of both the strained and unstrained devices becomes higher in comparison with the carrier concentration of the channel layers. This phenomenon has been discussed in details in section 4.1.2.

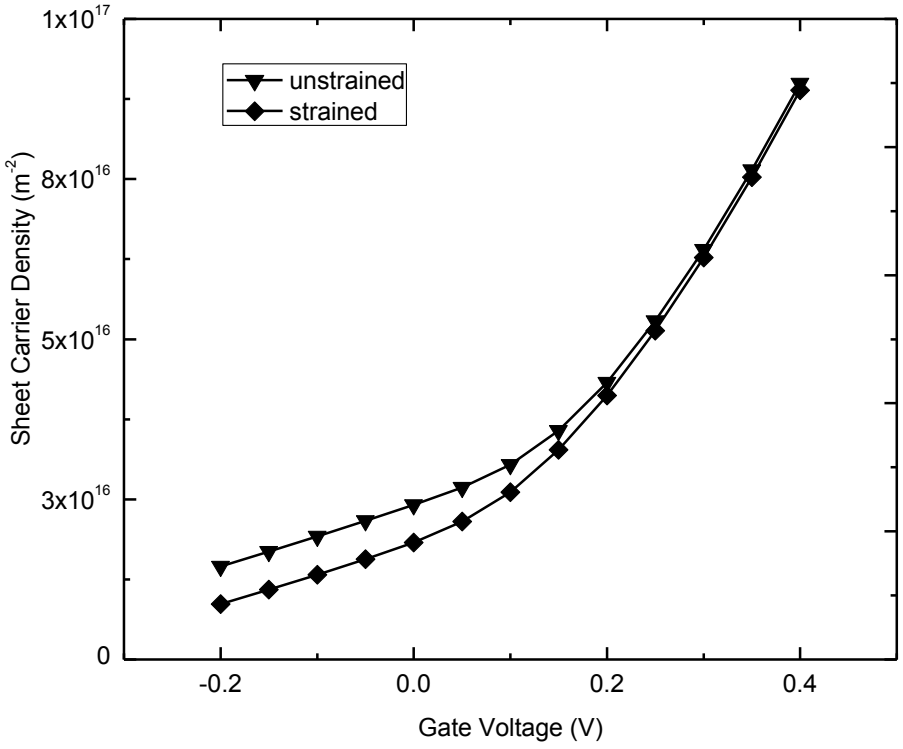


Figure 4.41: Sheet carrier density of strained and unstrained device

To compare the onset of parallel conduction for the strained and unstrained devices, the difference of the first two subband energies is shown as a function of the gate voltage in Fig. 4.42. The figure shows that the value of E_{12} reaches its minima for the strained device at a lower voltage compared to the unstrained device. This also indicates that the rate of charge buildup should be higher in the strained device compared to the unstrained one. In fact the supposition is supported by comparison of the C-V characteristic curves of the strained and unstrained cases as shown in Fig. 4.43. The figure shows that the gate capacitance is higher for the strained device. This is the reason why parallel conduction can initiate in the strained device at a lower voltage compared to the unstrained one. Therefore the capacitance is underestimated if strain effects are not incorporated in the electrostatic analysis of highly scaled HEMT devices.

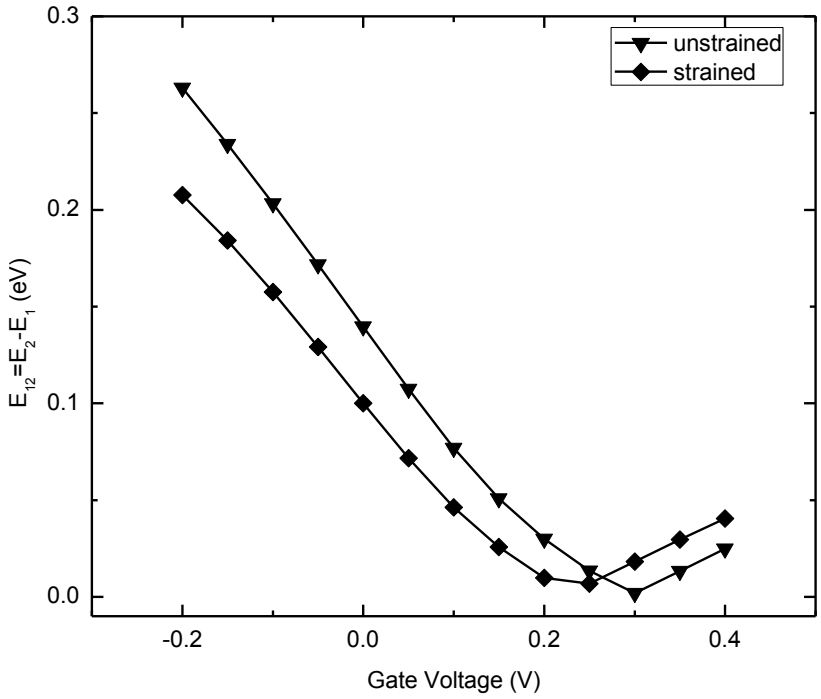


Figure 4.42: Difference of first two subband energies as a function of gate voltage

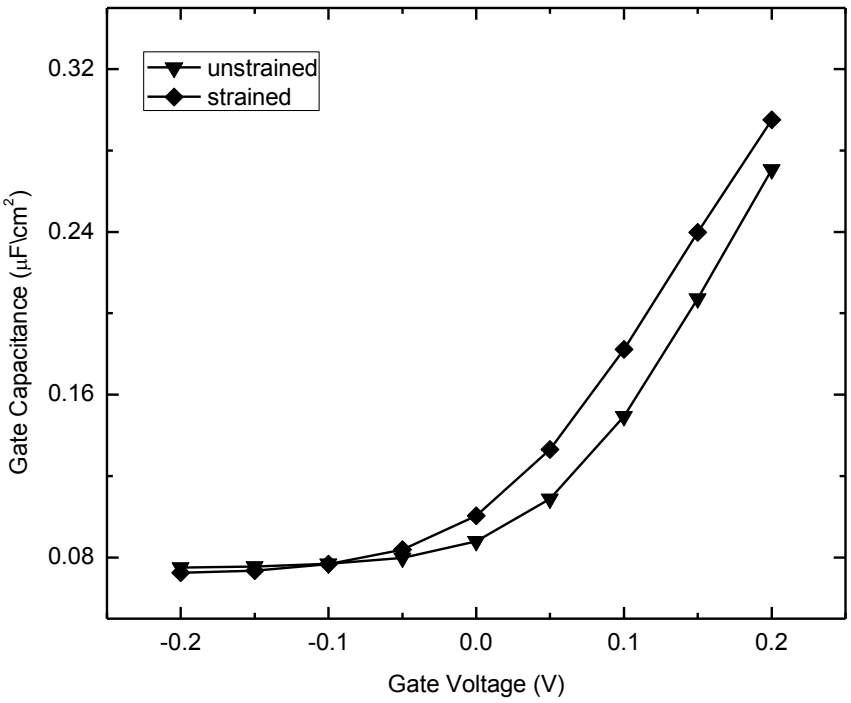


Figure 4.43: C-V characteristic curves of strained and unstrained devices

4.3.2 Transport effects

To investigate strain effects on the transport characteristics of highly scaled HEMTs, the I-V characteristic curves of InAs MQW generic HEMTs are shown for both the strained and unstrained cases at the same gate voltage (Fig. 4.44). The figure shows that the drain to source current is significantly overestimated if the device is considered unstrained. In Fig. 4.45 the on state currents of the strained and unstrained cases are shown as a function of gate voltage. The figure shows that for all gate voltages the drive current for the unstrained device is significantly higher compared to the practical strained device.

Another measure of the transport characteristic of a device is the channel conductance, which is shown in Fig. 4.45 for both the strained and unstrained devices. The figure shows that the channel conductance is overestimated as well if the device is considered unstrained.

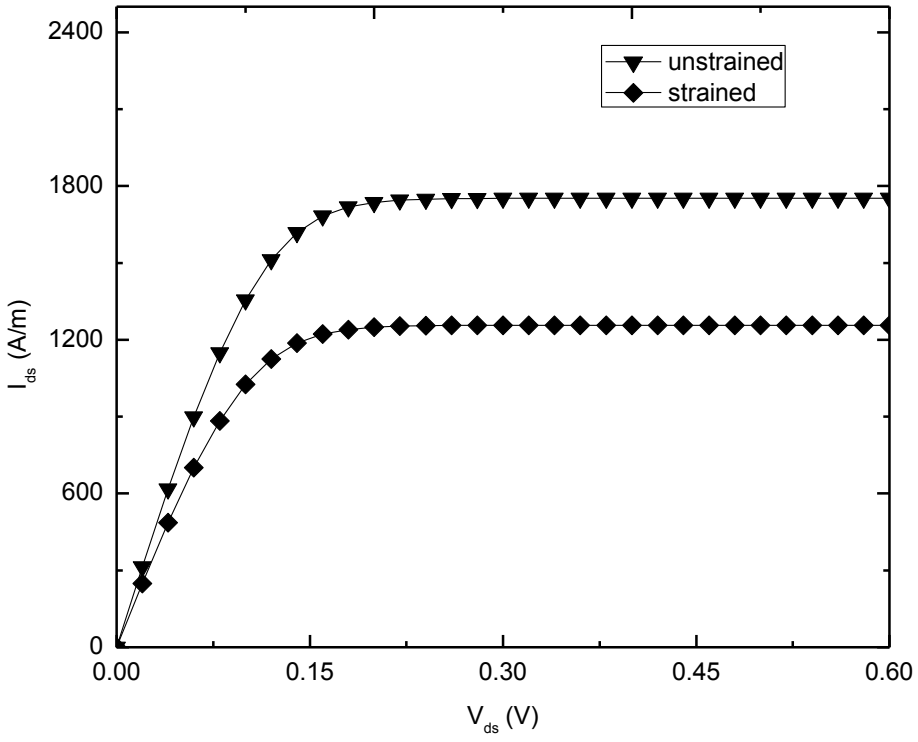


Figure 4.44: I-V characteristic curves of strained and unstrained devices

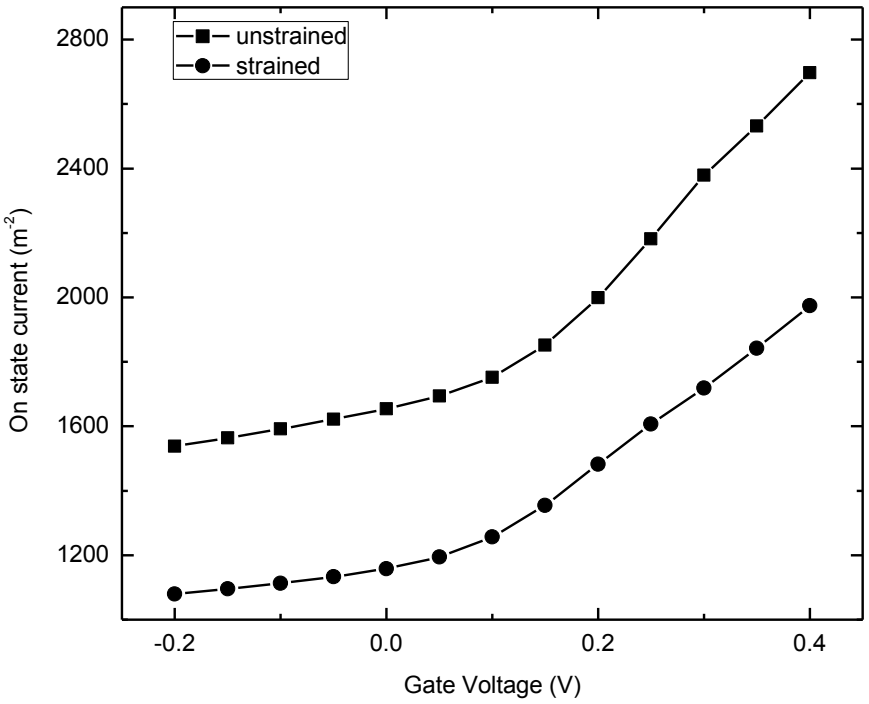


Figure 4.45: On state currents of strained and unstrained devices

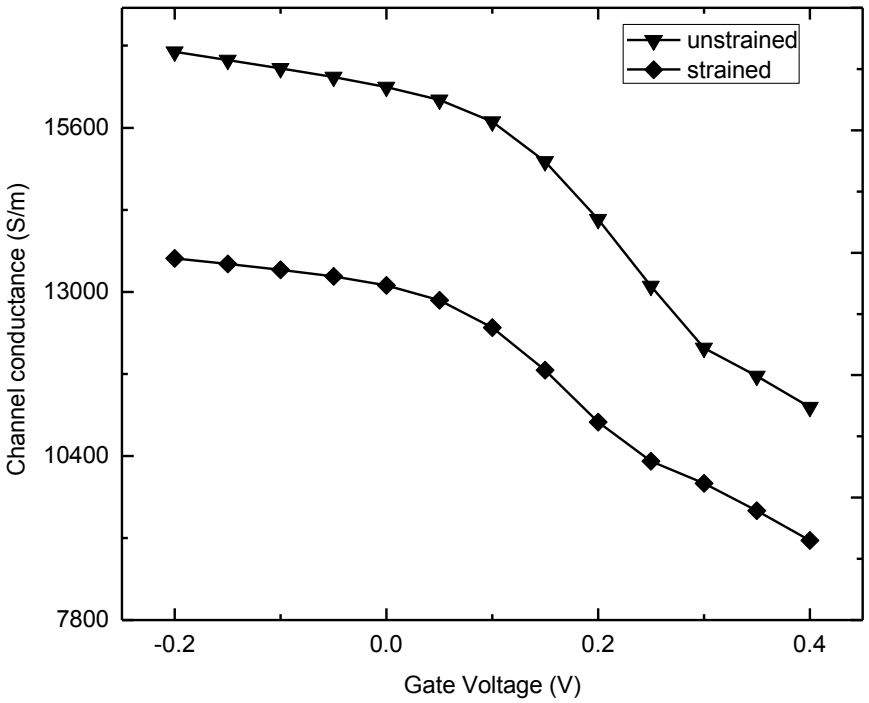


Figure 4.46: Channel conductance of strained and unstrained HEMTs

This is in accordance with the current-voltage relations shown in Fig. 4.44 and 4.45.
In Fig. 4.47, the ballistic mobility for the strained and unstrained devices are shown as a function of gate length. It has already been reported that strained silicon (Si) technology can increase the mobility in nanoscale Si-MOSFET [74]. Similar results are obtained in this study for highly scaled HEMT devices.

Table 4.6: Effective mobility for strained and unstrained device

Gate length	Unstrained device	Strained device
0.01	285.60001	305.42315
0.1	2579.71284	2740.36712
1	13112.34582	13515.07305
10	22159.97709	22272.13849
100	23802.36041	23815.24252

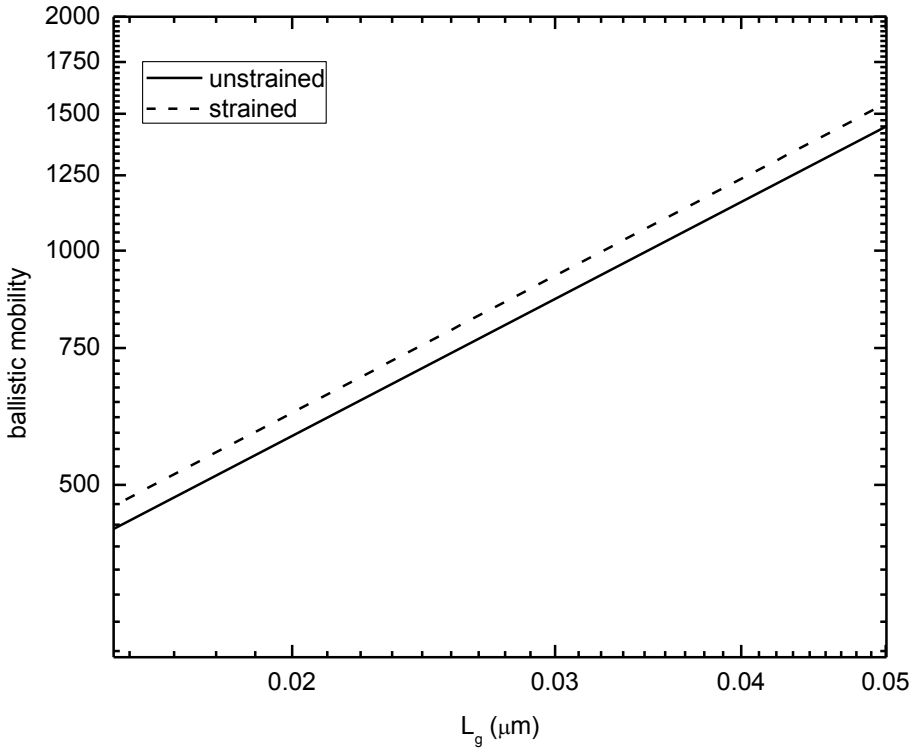


Figure 4.47: Ballistic mobility as a function of gate length

As shown in Fig. 4.47, the ballistic mobility of the strained HEMT is higher compared to that of the unstrained HEMT. Consequently the effective mobilities are also higher in strained devices within the short gate length limit (Table 4.6). However for high gate length devices, there is not much difference between the effective mobility values of the strained and unstrained devices as shown in Table 4.5.

CHAPTER 5

CONCLUSION

5.1 Summary of the Work

In this work the electrostatic and transport properties of $In_{0.53}Ga_{0.47}As$, $In_{0.70}Ga_{0.30}As$, $In_{0.70}Ga_{0.30}As$ and InAs MQW channel HEMTs are studied and compared using the quantum mechanical approach of self-consistent analysis. In this analysis technique, the coupled Schrödinger's and Poisson's are solved in a coupled manner. The solutions of these equations provide the allowed energy states, envelope functions and potential profiles. These results are subsequently used to calculate the charge concentration, capacitance-voltage and current-voltage relations according defined equations. Also ballistic and effective mobility and channel conductance values have been evaluated during this study.

For all the devices, the three different cases of generic, delta doped and spacer layered structures have been considered in the highly scaled regime. The study shows that delta doping has more influence on single channel HEMTs compared to MQW HEMTs with respect to both electrostatic and transport properties. Delta doping though increases the carrier density, on-state current and channel conductance of single channel HEMTs to some extent, it has negligible influence on the performance of MQW HEMTs. The spacer layer however influences the electrostatics and transports characteristics of both the single channel and MQW channel HEMTs. The addition of spacer layer decreases the carrier density, drive current and channel conductance for all variants of the device. However the addition of spacer layer reduces scattering, which in effect enhances both the ballistic and effective mobility of the HEMTs as found in this study.

The results presented in this work show that the self-consistently calculated capacitance is quantitatively in accordance with results obtained by the physical gate capacitance model presented elsewhere. The transport model applied here is also validated using results obtained by Sentaurus simulation in another work. The capacitive components corresponding to different eigen states show that the first two subbands are the most contributing elements with respect to device properties.

A novel extraction method regarding the onset voltage of parallel conduction in highly scaled HEMTs is also presented in this work. The entirely quantum mechanical approach described here defines two deterministic parameters V_{Emin} and Q_{ratio} corresponding to each device. Comparison of these parameters indicates that quantum mechanical confinement plays a strong role to inhibit parallel conduction in highly scaled HEMTs. The results show that the voltage for the onset of parallel conduction increases with the increase of quantum confinement. In this study the InAs MQW HEMT is found to have the deepest quantum well in the channel region. Consequently starting voltage of parallel conduction for this device is higher compared to all other devices studied here.

The evaluation of capacitance and channel conductance also shows that MQW HEMTs are more prohibitive to parallel conduction compared to conventional single well HEMTs because of the stronger confinement. In spite of this advantage, the MQW structure is found to reduce mobility of the HEMT in the ballistic limit. Nevertheless the strong confinement in MQW HEMTs, particularly in InAs MQW HEMT, causes the charge density, on-state current and channel conductance to be significantly higher compared to other HEMTs.

Finally analyses of strain effects show that charge density, current and channel conductance are significantly overestimated if strain is neglected in highly scaled HEMTs. Strain however can increase the mobility of the device in the short gate length limit. This result is very much in accordance with strained silicon technology being employed for nanoscale Si-MOSFETs to increase mobility in the highly scaled regime. Analysis of the effective and ballistic mobility values however shows that HEMTs can reach the ballistic mobility limit at much higher gate lengths compared to silicon devices.

5.2 Scopes of Future Works

There are numerous scopes of future works on the areas of this study. These are as follows.

- Instead of 1-D simulation, 2-D self-consistent analysis can be performed to carry out a more comprehensive analysis. Here 1-D simulation has been performed along a grid line perpendicular to the direction of transport. Similarly 2-D

simulation can be performed along a cross-section perpendicular to the transport direction.

- Only single gated HEMT structures have been studied in this work. Double gated HEMTs can be analyzed with respect to transport and electrostatic characteristics as well.
- The obtained results can be compared with more alternate material HEMT devices like nitride or InP HEMTs. Also more different cases of the MQW channel HEMTs can be compared for future study.
- The focus of this work has been the conduction band profile. Further study can be done with valence band profile and band to band transitions. Also the existence of energy states within the band offset can be investigated as well
- This work has mainly focused on the variation of channel layer content. Future work can be conducted with focus on the variation of barrier and buffer material.
- A more comprehensive study of both tensile and compressive strain effects on the electrostatics and transport properties of highly scaled HEMTs can be performed.
- An analytical expression regarding the voltage of onset of parallel conduction can be formulated.
- The obtained results can be compared with state of the art highly state devices.
- This study focused on the on-state characteristics of the HEMTs. Study can be conducted on the off-state current and on-off current ratios, which are important figure of merits of highly scaled devices.
- Study can be conducted on making the device less vulnerable to the phenomenon of parallel conduction. In this regard, study of the devices with respect to the variation of spacer layer thickness can be conducted. Also study can be conducted by adding a oxide layer beneath the gate material, which would be in effect the MOS HEMT structure.

LIST OF REFERENCES

[1] "The international technology roadmap for semicoductors," 2009. [Online]: http://www.itrs.net/Links/2009ITRS/Home2009.html

[2] Asenov A., "Simulation of Statistical Variability in Nano MOSFETs", in *2007 IEEE Symposium on VLSI Technology*, pp. 86–87, June 2007.

[3] Chau R., Doyle B., Datta S., Kavalieros J. and Zhang K., "Integrated nanoelectronics for the future" in *Nature Materials,* Vol. 6, Nov 2007, pp. 810-812

[4] Colinge J. P., "FinFETs and Other Multi-Gate Transistors",Springer Science+Business Media, New York, USA, 2008.

[5] Chau R. , Datta S., Doczy M., Doyle B., Kavalieros J. and Metz M., "High-κ/metal-gate stack and its MOSFET characteristics", in *IEEE Electron Device Letters,* Vol. 25, No. 6, June 2004, pp. 408-410

[6] Ghani T. *et al*., "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors", in *IEEE International Electron Device Meeting (IEDM) Technical Dig.,* pp. 1-3, Dec. 2003

[7] Saraswat K. C., Chui C. O., Kim D., Krishnamohan T. and Pethe A., "High Mobility Materials and Novel Device Structures for High Performance Nanoscale MOSFETs", in *IEEE International Electron Device Meeting (IEDM) Technical Dig.,* pp. 659-662, 2006

[8] Piprek J., "Nitride Semiconductor Devices: Principles and Simulation", 2007 WILEY, Strauss Gmbh, Germany

[9] Xuan Y., Lin H. C., Ye P. D. and Wilk G. D., "Capacitance-voltage studies on enhancement-mode InGaAs MOSFET using atomic-layer-deposited Al_2O_3 gate dielectric," in *Applied Physics Letters*, Vol. 88, no. 26, pp. 263518-263520, Jun. 2006.

[10] Datta S. *et al.,*"85nm Gate Length Enhancement and Depletion mode InSb Quantum Well Transistors for Ultra High Speed and Very Low Power Digital Logic Applications", in *IEEE International Electron Device Meeting (IEDM) Technical Dig.,* pp. 783-786, 2005

[11] Khayer M.A and Lake R.K., "The Quantum and Classical Capacitance Limits of InSb and InAs Nanowire FETs", in *IEEE Transactions on Electron Device,* Vol. 56, no. 10, pp. 2215 – 2223, Oct. 2009

[12] Cantley K., Yang L., Pal H., Low T., Ahmed S.S. and Lundstrom M.S., "Performance Analysis of III-V Materials in a Double-Gate nano-MOSFET", in *IEEE International Electron Device Meeting (IEDM) Technical Dig.,* pp. 113-116, Dec. 2007

[13] Mimura T., "The Early History of the High Electron Mobility Transistor (HEMT)", in *IEEE Transactions on Microwave Theory and Techniques*, Vol. 50, No. 3, March 2002

[14] Shur M. S., "Low Ballistic Mobility in Submicron HEMTs", in *IEEE Electron Device Letters,* Vol. 23, No. 9, September 2002

[15] Suemitsu T., Yokoyama H., Ishii T., Enoki T., Meneghesso G. and Zanoni E., "30 nm two-step recess gate InP-based InAlAs/InGaAs HEMT"s", in *IEEE Transactions on Electron Devices,* vol. 49, pp. 1694–1700, Oct.2002.

[16] Kim T. W., Kim D. H. and Alamo J. A. D., "30 nm $In_{0.7}Ga_{0.3}As$ Inverted-Type HEMTs with Reduced Gate Leakage Current for Logic Applications", in *IEEE International Electron Device Meeting (IEDM) Technical Dig.,* pp. 1-4, Dec. 2009

[17] Mishra U. K., Parikh P., and Wu Y. F., "AlGaN/GaN HEMTs-An Overview of Device Operation and Applications," in *Proceedings of the IEEE*, Vol. 90, no. 6, 1022-1031, Jun 2002.

[18] Kuzmik J. and Georgakilas A., "Proposal of High-Electron Mobility Transistors With Strained InN Channel", in *IEEE Transactions on Electron Devices,* Vol. 58, no. 3, March 2011

[19] Sze S.M. and Kwok K. Ng, "Physics of Semiconductor Devices", John Wiley & Sons, Inc., Hoboken, New Jersey, 2007

[20] Jin D., Kim D., Kim T. and Alamo J. A. D., "Quantum Capacitance in Scaled Down III-V FETs" in *IEEE International Electron Device Meeting (IEDM) Technical Dig.,* pp. 1, Dec. 2009

[21] Stern F., "Self-consistent results for n-type Si inversion layers," in *Physics Rev. B,* vol. 5, no. 12, pp. 4891–4899, 1972.

[22] Neophytou N., Rakshit T. and Lundstrom M., "Performance Analysis of 60-nm Gate Length III–V InGaAs HEMTs: Simulations versus Experiments", in *IEEE Transactions on Electron Devices*, Vol. 56, no. 7, July 2009

[23] Esaki L. and Tsu R.,"Superlattice and Negative Conductivity in Semiconductors," *IBM Research, RC 2418*, March 1969

[24] Dingle R., Stormer H. L., Gossard A. C., and Wiegmann W., "Electron Mobilities in Modulation-Doped Semiconductor Heterojunction Superlattices," *Appl. Phys. Lett.*, vol.33, no.665, 1978

[25] Stormer H. L., Dingle R., Gossard A. C., Wiegmann W., and Sturge M. D., "Two-Dimensional Electron Gas at a Semiconductor-Semiconductor Interface," *Solid State Commun*., Vol.29, no. 705, 1979

[26] Mimura T., Hiyamizu S., Fujii T., and Nanbu K., "A new field-effect transistor with selectively doped GaAs/n–Al Ga As heterojunctions," *Journal of Appl. Phys.*, vol. 19, no. 5, pp. L225–L227, 1980.

[27] Mimura T., Hiyamizu S., Hashimoto H., and Ishikawa H., "An enhancement-mode high electron mobility transistor for VLSI," in *Proc. 12th Solid-State Devices Conf., Tokyo, Japan*, p. 364 Aug. 1980,.

[28] Delagebeaudeuf D., Delescluse P., Etienne P., Laviron M., Chaplart J., and Linh N. T., "Two-dimensional electron gas MESFET structure," *Electron. Lett.*, vol. 16, no. 17, pp. 667–668, 1980.

[29] Solomon P. M., "A comparison of semiconductor devices for high speed logic," *Proc. IEEE*, vol. 70, no. 5, pp. 489-509, 1982.

[30] Roblin P. and Rohdin H., "High-speed heterostructure devices- from device concepts to circuit modeling" Cambridge University Press, New York, 2002

[31] Zipparian T. E., Dawson L. R., Osbourn G. C., and Fritz I.,"An $In_{0.2}Ga_{0.8}As$/GaAs modulation doped superlattice FET," *IEDM Tech. Dig.*, p. 696, 1983.

[32] Sugita Y. and Tamura M., "Misfit dislocations in bicrystals of epitaxially grown silicon on boron-doped silicon substrates," *Journal of Appl. Phys.*, vol. 40, no. 8, p. 3089, July 1969.

[33] Rosenberg J., Benlamri M., Kirchner P. D., Woodall I. M., and Pettit J. P., "An $In_{0.15}Ga_{0.85}As$ Pseudomorphic single quantum well HEMT," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 491-493, Oct. 1985

[34] Reid S. M., "Low-Noise Systems in the Deep Space Network" Wiley, September 2008

[35] Mishra U.K., Brwon A.S. and Rosenbaum S.E, "DC and RF performance of 0.1m gate length $A1_{.4}In_{.2}As$-$In_{.53}Ga_{.47}As$ Pseudomorphic HEMTs", *IEDM Tech. Dig.*, 1988

[36] Kuo J.M., Lalvic B. and Chang T.Y, "New Pseudomorphic MODFETs utilizing $In_{0.52-u}Al_{0.48+u}As$/ $In_{0.53+u}Ga_{0.47-u}As$ Heterostructures," *IEDM Tech. Digest*, 1986. pp. 460-460.

[37] Mesquida Kusters, Kohl, A., Brittner, S., Sommer, V., Heime, K., "Effect of indium mole fraction on charge control, DC and RF performance of single quantum-well InP/InxGa1-xAs/InP ($0.53 \leqslant x \leqslant 0.81$) HEMTs" *Proceedings of Sixth International Conference on Indium Phosphide and Related Materials*, 1994.

[38] Geok-Ing-Ng, Radhakrishnan-K,Hong-Wang, "Are we there yet?-a metamorphic HEMT and HBT perspective", *13th European Gallium Arsenide and other Compound Semiconductors Application Symposium*, Paris, France, pp.13, 2005

[39] Liang D., Bowers J.E., Oakley D.C., Napoleone A., Chapman D.C., Chen C.-L., Juodawlkis P.W., and Raday O.: „High-quality 150 mm InP-to-silicon epitaxial transfer for silicon photonic integrated circuits", *Electrochem. Solid-State Lett.*, 2009, 12, pp. H101–H104

[40] Wang G. W., Chen Y. K., Schaff W. J. and Eastman L. F., "A 0.1μm gate AlInAs/GaInAs MODFET fabricated on GaAs substrates", *IEEE Trans. on Electron Devices*, vol. 35, no. 7, pp. 818-823, Jul 1988

[41] Win P., Druelle Y., Cappy A., Cordier Y., Adam D., Favre J, "Metamorphic In0.3Ga0.7As/In0.29Al 0.71As layer on GaAs: a new structure for millimeter wave ICs", *Proceedings of IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits*,1993

[42] Higuchi K., Kudo M., Mori M., Mishima T.,"First high performance InAlAs/InGaAs HEMTs on GaAs exceeding that on InP" *IEDM Technical Digest*, 1994

[43] Chertouk M., Heiss H., Xu D., Kraus S., Klein W., Bohm G., Trankle G., Weimann G., "Metamorphic InAlAs/InGaAs HEMTs on GaAs substrates with a novel composite channels design" *IEEE Electron Device Lett.*, volume: 17, issue: 6, 1995

[44] Eisenbeiser K., Droopad R., and J.-H. Huang, "Metamorphic InAlAs/GaInAs enhancement mode HEMT"s on GaAs substrates," *IEEE Electron Device Lett.*, vol. 20, pp. 507–509, Oct. 1999

[45] Dumka D. C., Hoke W. E., Lemonias P. J., Cueva G., and I. Adesida "High performance 0.35μ gate-length monolithic enhancement/depletion-mode metamorphic $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ HEMTs on GaAs Substrates" *IEEE Electron Device Lett.*, vol. 22, no. 8, August 2001

[46] Vasallo B.G., Rodilla H., Gonz. lez T ., Moschetti G., Grahn J., Mateos J., "Monte Carlo study of impact ionization and hole transport in InAs HEMTs with isolated gate" Proceedings of *Spanish Conference on Electron Devices*, 2011

[47] Piprek J., "Nitride semiconductor devices principles and simulation", WILEY, Germany, 2007

[48] Bernardini F., Fiorentini V., and Vanderbilt D., "Spontaneous polarization and piezoelectric constants of III-V nitrides," *Phys. Rev. B*, vol. 56, no. 16, pp. 10024-10027, Oct. 1997

[49] Ambacher O., Foutz B., Smart J., Shealy J. R., Weimann N. G., Chu K., Murphy M., Sierakowski A. J., Schaff W. J., Eastman L. F., Dimitrov R., Mitchell A., and Stutzmann M., "Tow dimensional electron gases induced by spontaneous

and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 87, no. 1, pp. 334-344, Jan, 2000

[50] Ibbetson J. P., Fini P. T., Ness K. D., DenBaars S. P., Speck J. S., and Mishra U. K., "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Appl. Phys. Lett.,* vol. 77, no. 2, pp. 250-252, Jul. 2000.

[51] Khan M. A., Van Hove J. M., Kuznia J. N., and Olsen D. T., "High electron mobility GaN/AlxGa1-xN heterostructures grown by low-pressure metalorganic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 58, no. 21, pp. 2408-2410, May 1991.

[52] Khan M. A., Bhattarai A., Kuznia J. N., and Olson D. T.,"High-electron mobility transistor based on a GaN-$Al_xGa_{1-x}N$ heterojunction," *Appl. Phys. Lett*., vol. 63, no. 9, pp. 1214-1215, Aug. 1993.

[53] Saito W., Takada Y., Kuraguchi M., Tsuda K., Omura I., Ogura T.,and Ohashi H.,"High Breakdown Voltage AlGaN–GaN power-HEMT design and high current density switching behavior" *IEEE Transactions on Electron Devices*, vol. 50, no. 12, december 2003

[54] Steinhoff G., Baur B., Wrobel G., Ingebrandt S., Offenhäusser A., Dadgar A., Krost A., Stutzmann M., and Eickhoff M., "Recording of cell action potentials with AlGaN/GaN field-effect transistors" *Appl. Phys. Lett*, vol.86, 2005

[55] Stutzmann M., Steinhoff G., Eickhoff M., Ambacher O., Nebel C. E., Schalwig J., Neuberger R.and Muller G., "GaN-based heterostructures for sensor applications",*Diamond and Related Materials*, vol.11,issue 3-6,pp.886-891 2002

[56] Joshin K., Kikkawa T.,"Recent progress of high power GaN-HEMT for wireless application" *Proceedings of Microwave Conference*, Asia-Pacific, 2006.

[57] Kuzmík J., Kostopoulos A., Konstantinidis G., Carlin J.-F., Georgakilas A., and Pogany D.,"InAlN/GaN HEMTs: a first insight into technological optimization" ieee transactions on electron devices, vol. 53, no. 3, March 2006

[58] V. M. Polyakov and F. Schwierz, "Low-field electron mobility in wurtzite InN," Appl. Phys. Lett., vol. 88, no. 3, p. 032101, Jan. 2006

[59] Jan Kuzmik and Alexandros Georgakilas, Member, IEEE, "Proposal of High-Electron Mobility Transistors With Strained InN Channel" *IEEE Transactions on Electron Devices*, vol. 58, no. 3, March 2011

[60] Wang J. and Lundstrom M.,"Ballistic Transport in High Electron Mobility Transistors" *IEEE Transactions on Electron Devices*,, vol. 50, no. 7, July 2003

[61] Kim D., Alamo J. A., Lee J., and Seo K., "Performance evaluation of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs for beyond-CMOS logic applications", *IEDM Technical Digest* 2005

[62] Kim D., Alamo J. A., "Logic performance of 40 nm InAs HEMTs" *IEDM Technical Digest* 2007

[63] Kim D. and Alamo J. A., "Lateral and vertical scaling of $In_{0.7}Ga_{0.3}As$ HEMTs for post-Si-CMOS logic applications" ieee transactions on electron devices, vol. 55, no. 10, october 2008

[64] Kim D. and Alamo J. A., "30-nm InAs pseudomorphic HEMTs on an InP substrate with a current-gain cutoff frequency of 628 GHz", *IEEE Transactions on Electron Devices*, vol. 29, no. 8, august 2008

[65] Hwang E., Mookerjea S., Hudait M. K. and Datta S., "Scalability study of $In_{0.7}Ga_{0.3}As$ HEMTs for 22nm node and beyond logic applications" *Proceedings 68th Device Research Conference,* pg. 61-62 June 2010

[66] Kim D. and Alamo J. A.,"Scalability of sub-100 nm InAs HEMTs on InP substrate for future logic applications", *IEEE Transactions on Electron Devices*,, vol. 57, no. 7, July 2010

[67] Piprek J., "Semiconductor Optoelectronic Devices: Introduction to Physics and Simulation," Academic Press: San Diego, California, 2003.

[68] Natori K., "Ballistic metal-oxide-semiconductor field effect transistor," in *Journal of Applied Physics*, vol. 76, pp. 4879–4890, 1994

[69] Datta S., "Quantum Transport: Atom to Transistor", Cambridge University Press, New York, 2005

[70] Blakemore J. S., "Approximate for the Fermi-Dirac integrals, especially the function $\Im_{1/2}(\eta)$ used to describe electron density in a semiconductor," *Solid-State Electron.*, vol. 25, pp. 1067–1076, 1982

[71] Kim K. W., Tian H., and Littlejohn M. A., "Analysis of delta-doped and uniformly doped AlGaAs/GaAs HEMT"s by ensemble Monte Carlo simulations" *IEEE Transactions on Electron Devices*,vol.38, no 8., August 1991

[72] Sadao A. "Properties of Semiconductor Alloys: Group-IV, III–V and II–VI Semiconductors", John Wiley & Sons Ltd, Great Britain, 2009

[73] Chu M., Sun Y., Aghoram U., and Thompson S. E., "A solution for higher carrier mobility in nanoscale MOSFETs", *Annual Review of Materials Research*, vol. 39, pp. 203-229, August 2009

[74] Martin J., Bournel A., and Dollfus P., "On the ballistic transport in nanometer-scaled DG MOSFETs", *IEEE Transactions on Electron Devices* vol. 51, no. 7, pp. 1148–1155, July 2004