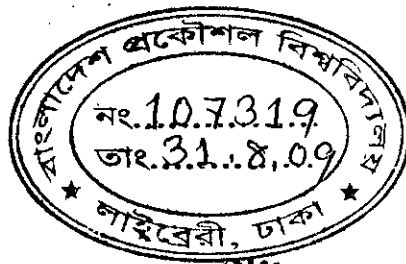


**CAPACITANCE-VOLTAGE CHARACTERISTICS OF
PARTIALLY DEPLETED FOUR GATE TRANSISTOR
UNDER DIFFERENT GATE BIAS CONDITIONS**

A thesis submitted to the
Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology
in partial fulfillment of the requirements
for the degree of
MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

by
Somaia Sarwat Sylvia



BUET

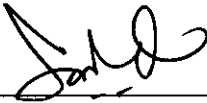
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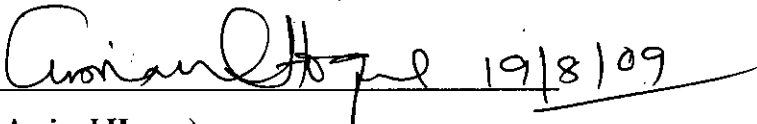
AUGUST, 2009





The thesis titled "CAPACITANCE-VOLTAGE CHARACTERISTICS OF PARTIALLY DEPLETED FOUR GATE TRANSISTOR UNDER DIFFERENT GATE BIAS CONDITIONS" submitted by Somaia Sarwat Sylvia, Student No: 100706206P, Session: October 2007 has been accepted as satisfactory in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on August 19, 2009.

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S. S. Sylvia 19.08.2009

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To My Parents

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Acknowledgements

First of all, I must express my heartfelt gratitude and best regards to Almighty Allah for making me successful in completing all the tasks in time.

I would like to take the opportunity to express my sincere indebtedness to my thesis supervisor Dr. Quazi Deen Mohd Khosru, Professor, Department of Electrical and Electronic Engineering, for his valuable suggestions during the entire thesis work. His guidance have encouraged me to carry out the thesis work in a fruit full manner.

I also express thanks to Professor and Head, Dr. Aminul Hoque for his support throughout.

Thanks to Dr. Kazi Mujibur Rahman, Professor, Department of Electrical and Electronic Engineering, and Dr. Mohammed Imamul Hassan Bhuiyan, Assistant Professor, Department of Electrical and Electronic Engineering for their cooperation in obtaining BUET lab facilities.

Thanks to my family and all my well wishers, colleagues and friends who helped in various ways to complete the work.

BUET, Dhaka
August, 2009

Somaia Sarwat Sylvia

Abstract

The Capacitance-Voltage (C-V) characteristics has been analyzed for the partially depleted Four Gate Transistor (G^4 -FET). Effects of different gate bias on the C-V characteristics have also been studied. A solver, based on Finite Element Method and semi-classical formalism, is tested for validity with standard numerical solver, Schred, which has been applied for the solution of Poisson's equation. Since the G^4 -FET is a multiple gate structure, only the front gate is chosen for C-V characterization. Analyzing the C-V characteristic curves for the front gate, it is found that the lateral junction gates and back gate, surrounding the channel, have significant effect on the capacitance. Junction gate reverse bias causes a shift in the C-V curves and makes the transition from depletion to inversion steeper. On the other hand, back gate accumulation or inversion does not have noticeable impact on the C-V in accumulation or inversion region, whereas inversion at the back gate lowers the capacitance in depletion region significantly. Therefore, the simulation-based study carried out in this work will be useful in predicting the impacts of various gate biases on the C-V characteristics at the front gate of the G^4 -FET.

List of Symbols

BOX	Buried oxide
C	Capacitance
C_{ox}	Oxide capacitance
C_{ox1}	Front oxide capacitance for G^4 -FET
C_{SD}	Capacitance of depletion region
C_{PG}	Capacitance of poly/top gate in G^4 -FET
D	Drain
FOX	Field oxide
K_{si}	Dielectric constant of silicon
L_G	Transistor gate length
n	Concentration of electron
n_0	Concentration of electron in equilibrium
n_i	Intrinsic carrier density
N_D	Donor concentration
N_A	Acceptor concentration
N_D^+	Ionized donor concentration
N_A^-	Ionized acceptor concentration
p	Concentration of hole
p_0	Concentration of hole in equilibrium
q	magnitude of electronic charge
Q_{total}	Total charge inside silicon film in G^4 -FET
S	Source
t_{si}	Silicon film thickness
t_{ox}	Thickness of oxide
V	Electrostatic potential
V_{dd}	Drain bias
V_{ss}	Source bias
V_{PG}	Poly/ top gate applied voltage

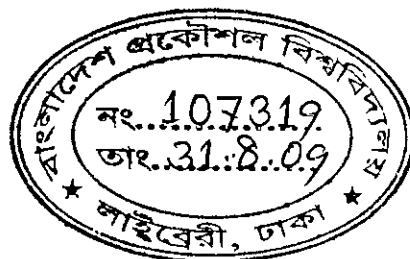
V_{JG}	Junction gate applied voltage
$V_{SUBSTRATE}$	Back gate applied voltage
w_{Si}	Silicon film width
x_{dmax}	Maximum depletion depth
x_d	Space charge width
ρ	Charge density
ϵ	Permittivity of any medium
ϵ_0	Free space permittivity
ϵ_{ox}	Permittivity of oxide
ϵ_s	Permittivity of semiconductor
α	Weighting factor in Gauss-Seidel iteration method

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Chapter 1

Introduction

1.1 Introduction

Since the invention of the integrated circuit in 1958, the number of transistors that can be placed inexpensively on an integrated circuit has increased exponentially, doubling approximately every two years. This has come to be popularly known as Moore's Law [1]. Increase in the device density is made possible by shrinking the dimensions of each transistor. Shrinking transistor dimensions has resulted in increased transistor count and operating frequencies, thus enabling tremendous technological progress such as: microprocessors with greater than 100 million transistors and memory chips with greater than one Giga Byte densities. The key dimension that is reduced from one transistor generation to the next is the gate length (L_G).

In 1965 the smallest MOSFET had an $L_G = 25 \mu\text{m}$. In 1990, industry-standard versions of MOS device structures boast submicron dimensions. However, down-scaling device dimensions lead to some small-dimension effects in MOSFETs which are mostly associated with the reduction in channel length. Reducing channel length below some minimum value may lead to velocity saturation, parasitic BJT action and even modification in the threshold voltage for the MOSFET [2]. Moreover, the conduction channel must be controlled by the gate, not by the drain. As L_G is reduced, drain-to-channel capacitance increases. Therefore, gate-to-channel capacitance must also be raised, i.e., oxide must be thinner.

The main challenges in device-scaling are:

- SiO_2 is too leaky below 1.2nm.
- Even a very thin oxide cannot control a current path far from the gate.

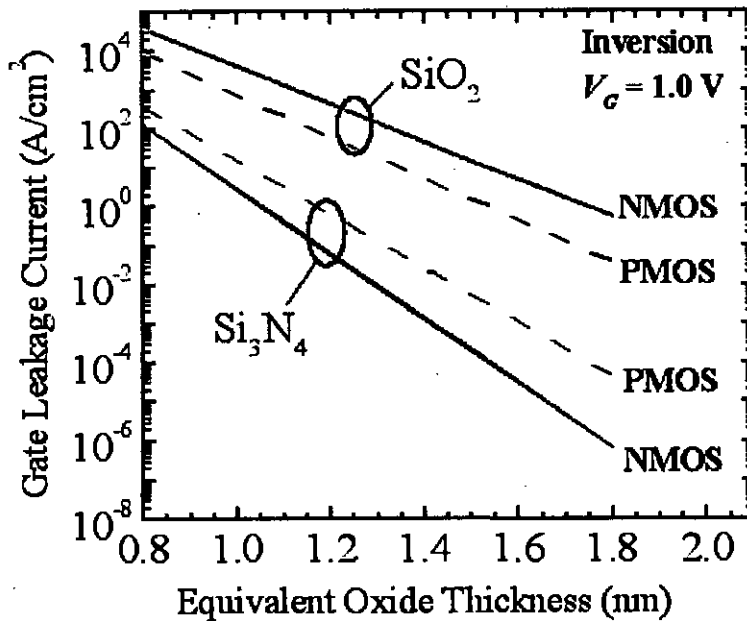


Figure 1.1: Gate Leakage Current vs. Oxide Thickness [courtesy: Chenming Hu, DAC, 2000]

Hence, gate leakage current increases as device dimension shrinks [Figure 1.1].

Therefore, device scaling which increases the number of transistors cannot continue forever.

1.2 Introduction to SOI Technology

There are two primary device structures that have been widely studied and used in CMOS (complementary MOS) technology. The first is the bulk structure, where a transistor is directly fabricated on the semiconductor substrate and the second, is called SOI (silicon-on-insulator), where a transistor is built on a thin silicon layer which is separated from the substrate by a layer of insulator.

SOI Technology has got several benefits over the bulk structure [3], such as:

- Simple IC processing (isolation)
- Higher density
- No latch-up
- No body effect

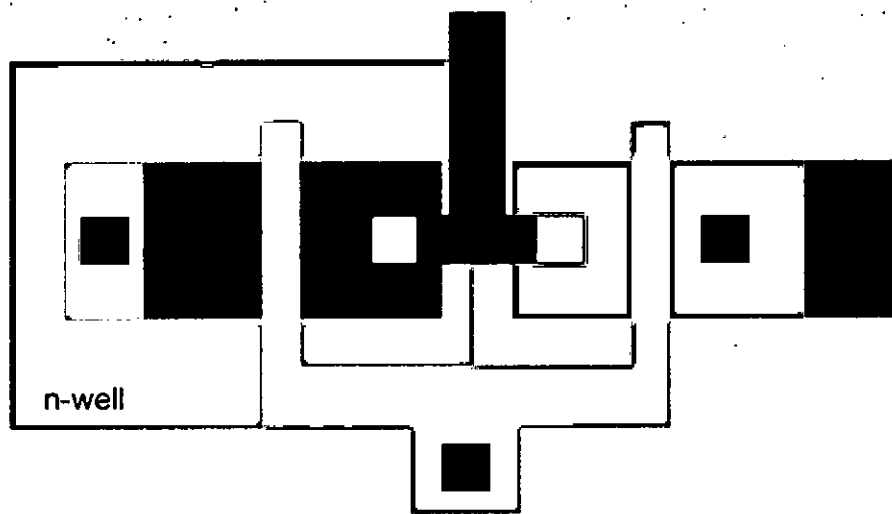


Figure 1.2: Layout for bulk CMOS [3]

- Reduced S/D junction capacitance (speed/power)
- Better Sub-Threshold slope.

So far as device scaling is concerned, Figures 1.2 and 1.3 will illustrate the benefit of SOI CMOS structures over the bulk structures.

Simpler isolation in SOI technology leads to simpler process and smaller layout. SOI has reduced junction capacitance and increased drive capability for same technology generation. Therefore, most of the proposed new structures are SOI devices.

SOI devices can be fully depleted (FD) or partially depleted (PD), where the amount of depletion refers to the channel region of a transistor. Partially depleted SOI transistors resemble their bulk counterparts, where doping concentrations in the channel determine the depletion depth, leaving a neutral silicon “floating body” isolated from the grounded substrate residing below the buried oxide (Figure 1.4).

In contrast, a thin-film SOI transistor in which the depletion region extends down to the buried oxide, leaving no neutral region, is considered fully depleted (FD) (Figure 1.5). Fully depleted transistors require an ultrathin silicon film to control short-channel effects, where the threshold voltage (V_t) depends heavily on the gate length, and in general provide only low- V_t transistors.

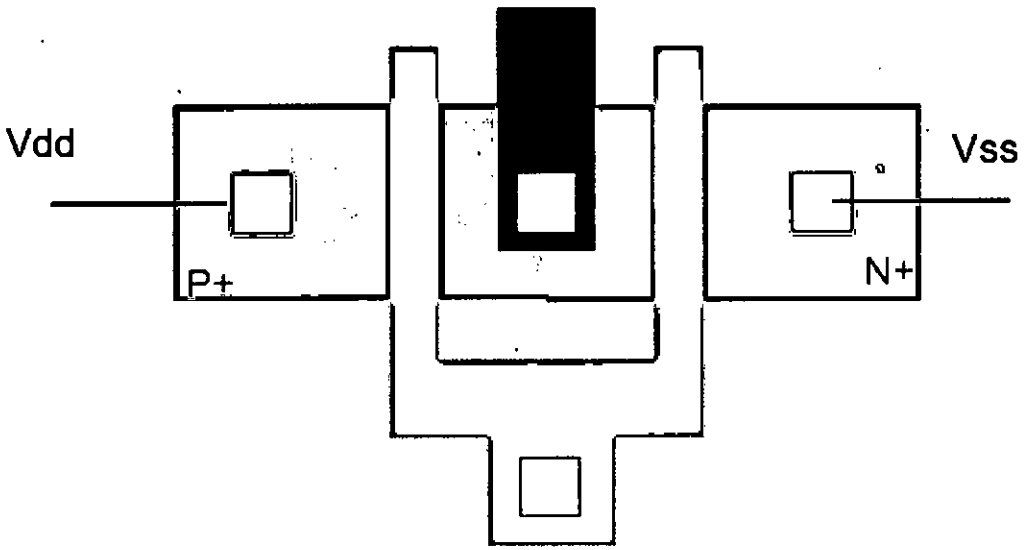


Figure 1.3: Layout for SOI [3]

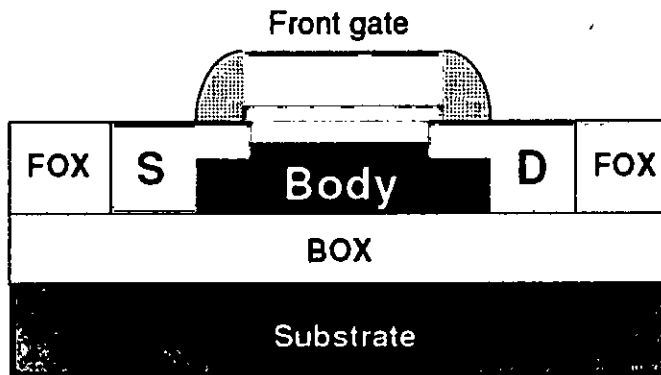


Figure 1.4: Partially depleted (PD) body [3]

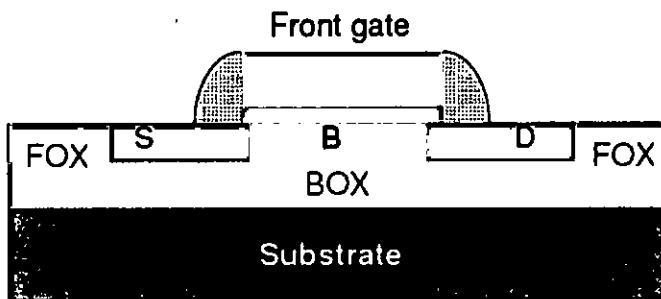


Figure 1.5: Fully depleted (FD) body [3]

1.3 Multiple Gate Transistors

At the current pace of scaling, the industry predicts that planar transistors will reach feasible limits of miniaturization by 2010, concurrent with the widespread adoption of 32 nm technologies. At such sizes, planar transistors, as already mentioned, are expected to suffer from undesirable short channel effects, especially “off-state” leakage current, which increases the idle power required by the device. As solutions to improve the performance and scalability in future transistors, multiple gate transistors are being explored.

In a multigate device, the channel is surrounded by several gates on multiple surfaces, allowing more effective suppression of “off-state” leakage current. Multiple gates also allow enhanced current in the “on” state, also known as drive current. These advantages translate to lower power consumption and enhanced device performance. Nonplanar devices are also more compact than conventional planar transistors, enabling higher transistor density.

In an ever increasing need for higher current drive and better short-channel characteristics, silicon-on-insulator MOS transistors are evolving from classical, planar, single-gate devices into three-dimensional devices with multiple gates (double-, triple- or quadruple-gate devices) [4]. These devices offer a higher current drive per unit silicon area than conventional MOSFETs. In addition, they offer optimal short-channel effects (reduced Drain Induced Barrier Lowering: DIBL and subthreshold slope degradation).

The first publication describing a double-gate SOI MOSFET dates back to 1984. This initial paper predicted the good short-channel characteristics of such a device. The triple-gate MOSFET is a thin-film, narrow silicon island with a gate on three of its sides. Improved versions feature a field-induced, pseudo-fourth gate such as the π -gate device [5] and the Ω -gate device [6](Figure 1.6)

It is possible to predict how small the silicon film thickness should be in multiple-gate devices to avoid short-channel effects (or, at least, to maintain a decent subthreshold swing)[4]. Figure 1.7 shows the maximum allowed silicon film thickness (and device width in a triple-gate device with $w_{si} = t_{si}$) to avoid short-channel effects. It reveals that for a particular gate length, the thickness of the silicon film in a single-gate, fully depleted device needs to be 3-5 times smaller than the gate length[4]. If a double-gate structure is used, the silicon film thickness is more relaxed and needs to be only half the gate length[4]. Further relaxation is obtained using a surrounding gate structure, where the silicon film

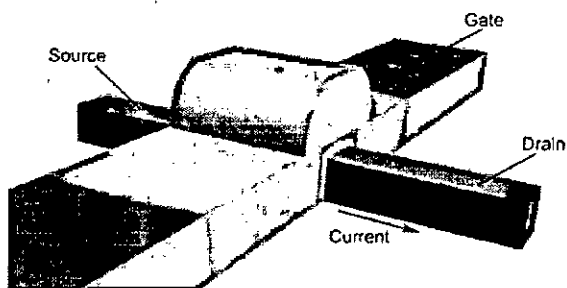


Figure 1.6: Triple-gate SOI MOSFET [6]

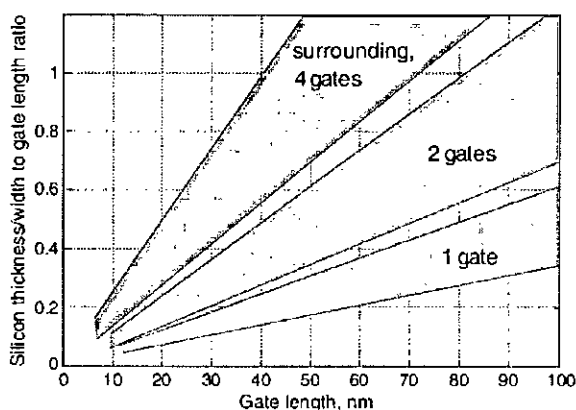


Figure 1.7: Maximum allowed silicon film thickness and device width vs. gate length to avoid short-channel effects in single-, double- and quadruple-gate SOI MOSFETs [4]

thickness/width can be as large as the gate length.

Increasing the number of gates further improves the subthreshold swing because the control of the channel region by the gate(s) becomes more effective [4]. Figure 1.8 compares the subthreshold swing of transistors with 2-4 gates.

From the above considerations it is clear that the double-, triple- and quadruple-gate devices demonstrate improved current drive and short-channel characteristics compared to single-gate planer SOI transistors. However, in these devices, the term “multiple” generally represents the number of channels switched by one gate and not the number of gates.

As the progression in multiple-gate structures continues, a novel four-gate transistor (G^4 -FET) have been proposed in [7]. The initial characteristics showed the possibility to independently bias its four gates [7]. This device can be manufactured using conventional SOI processes, without necessitating additional fabrication steps, being adaptable to more aggressive technology nodes. The G^4 -FET's fully operational characteristics, therefore,

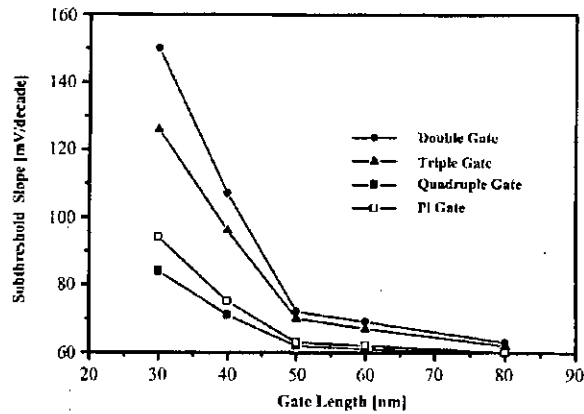


Figure 1.8: Sub-threshold slope in double-, triple-, quadruple- and π -gate MOSFETs as a function of gate length [4]

has drawn the fascination of researchers in recent years.

1.4 Literature Review

Blalock *et al.* in 2002, first proposed the idea of the G^4 -FET, which was then known as the MOS-JFET [7]. The MOS-JFET, a combination of two different transistors: 1- JFET and 2- MOSFET was experimented and was proved to be fully functional that has the capability to control the conduction characteristics with each of the four gates[7]. In the same year, Cristoloveanu *et al.* also provided the two dimensional simulation results of the cross-section of the G^4 -FET along with measured electrical characteristics.[8].

Performance of the G^4 -FET from low voltage to high voltage regime was studied by Dufrene *et al.*[9] in 2003 and it was shown that breakdown voltage of G^4 -FET is beyond 15V. As a general trend, the breakdown voltage will increase by depleting the various gates (front, back, or junctions).

A saturation current model for G^4 -FET has been proposed by Dufrene *et al.* in 2003 [10] Since the G^4 -FET is an accumulation-mode device, the conventional first-order JFET model was used as the basis for the G^4 -FET saturation current model. The model was developed using measured data from n-channel devices fabricated in $0.35\mu\text{m}$ Partially Depleted SOI (PDSOI).

Multiple bias dependence of threshold voltage, subthreshold swing, and mobility as viewed from the top gate or lateral gates have been measured and studied by Akarvardar *et al.* in 2003 [11]. The results allow understanding the particular influence of each particular

gate and offer guidelines for optimization of device architecture and biasing. Subthreshold swing was further investigated by Dufrene *et al.* in 2004 [12]. A new model was developed to explain the subthreshold swing variation induced by the biasing of the remaining three gates. The model is based on the concept that effective doping seen by the control gate is a function of channel width and bias of the other gates.

The current-voltage, transconductance and threshold voltage characteristics of the G^4 -FET have been systematically presented and analyzed by Dufrene *et al.* in 2004 [13]. A physics-based analysis was made in order to clarify the mechanisms of operation by accounting for the different conduction channels and their interaction. It has been shown that the subthreshold swing, transconductance and the threshold voltages are functions of biases applied to the gates. With adjusted gate bias, the G^4 -FET can offer a clear improvement in subthreshold swing values (as low as $\sim 65\text{mV/decade}$ for junction gates and $\sim 73\text{mV/decade}$ for top gate). A high value of mobility, $\sim 550\text{cm}^2/\text{Vs}$, can be achieved for volume conduction when carriers do not experience surface scattering.

An analytical threshold voltage model has been proposed by Akarvardar *et al.* in 2004 [14] where 2-D analytical relation for fully depleted body potential has been derived. Later in 2006 Akarvardar *et al.* published another paper where the 2-D potential distribution in G^4 -FETs is modeled based on a parabolical potential variation between the junction-gates [15]. The potential model is used to derive analytical expressions for the front threshold voltage of the G^4 -FET for all possible steady-state charge conditions at the back interface.

A specific operation mode providing volume conduction, called depletion-all-around (DAA)[16, 17], has been elaborately presented based on experimental results, 3-D device simulations and analytical modeling by Akarvardar *et al.* in 2007 [18]. It was shown that when both interfaces are driven from depletion to inversion, the DAA operation provides a subthreshold swing of 60 mV/dec , high mobility, high transconductance, very high transconductance-to-current ratio and Early voltage, minimum noise operation and intrinsic radiation hardness.

In 2006, low frequency noise characteristics of the G^4 -FET were reported by Akarvardar *et al.* in [19]. The noise power spectral density as a function of biasing conditions is presented and compared for surface and volume conduction modes. It was shown that, for a fixed drain current, the noise related to the volume of the transistor could be more than 1 decade lower than that generated at the surface.

The fully-depleted version of the SOI four-gate transistor is introduced and systematically characterized by Akarvardar *et al.* in 2007 [20]. It was shown that the thinning-down of the silicon film promotes vertical coupling between the front and the back gates while mitigating the horizontal coupling between the lateral gates. As a consequence the direct influence of the lateral junction-gates on the body potential distribution is reduced. However, by biasing the back interface in inversion the junction-gates can indirectly modulate the body potential. This provides a very efficient control of the front-channel conduction parameters such as threshold voltage, subthreshold swing and transconductance by the junction-gates regardless the device width.

In 2008, Tejada *et al.* proposed a noise model for the G^4 -FET that takes into account both volume and surface effects [21]. The proposed model reproduced the experiments and confirmed the different origins of the noise which had been tested in different operating modes of the transistor and gave an explanation of the experimental measurements carried out by other authors. The model's future usefulness lies in the possibility of calculating the local noise contribution in any part of the device in order to locate those regions that contribute higher noise, and thus, estimate the applied voltages that will minimize the total noise in these devices.

1.5 Objective of the Thesis Work

Capacitance-Voltage (C-V) measurement is a fundamental technique for MOS devices. Accurate determination of device capacitance is crucial to the measurement of equivalent oxide thickness, inversion layer charge, interface trap density, channel carrier mobility, channel length and other electrical characteristics of MOS field effect transistors [22, 23]. Knowledge of MOS capacitors and C-V characteristics is essential in order to understand the principles of operation and I-V characteristics of MOS transistors.

So far, experimental and simulation works performed on the G^4 -FET were focussed on testing the functionality of this novel device [7, 10, 11, 16, 17]. Because simulation is necessary in order to gain insight into the operation of a real-life system, we attempted to predict the C-V characteristics of the G^4 -FET which is yet to be simulated and experimentally tested.

Objectives of this work are briefly mentioned below:

- To prepare a simulator that will predict the C-V characteristics of the G^4 -FET taking

device parameters and biasing conditions as inputs.

- To compare the effects of gate biases on the C-V characteristics under different gate bias conditions.

Although actually measured C-V curves are not expected to coincide fully with the idealized models, the results are supposed to qualitatively represent the actual device under test.

1.6 Organization of the Thesis

Chapter 2 contains a discussion on the structure and some remarkable features of the G^4 -FET. Detailed procedure for the semi-classical formalism of the simulator along with verification is also included in this chapter. Chapter 3 deals with results of the thesis work. In chapter 4, conclusion of the work is presented followed by some suggestions for future work.

Chapter 2

The Four Gate Transistor

2.1 Introduction

The Four Gate Transistor or the G^4 -FET, also known as the MOS-JFET is a new device that takes advantage of the unique flexibility and isolation capability of SOI technology to combine both MOS (Metal-Oxide-Semiconductor) field-effect and junction field-effect for conduction control within a single transistor body [7]. Through the combination of MOS gates and junction-based gates, the SOI-based G^4 -FET allows manipulation of multiple gates, from one to four, according to the application envisioned. Utilizing these gates separately, or in a combinatorial fashion, provides new circuit opportunities for analog, RF, mixed-signal, and digital applications.

It is also to note that CMOS technology scaling should enhance the performance of the G^4 -FET as MOS gate length shrinks (therefore reducing the lateral separation between the junction gates). This implies that it should be easier to pinch-off the conduction channel as technology is scaled, particularly if body doping of the transistor is optimized. Subsequently the G^4 -FET is highly amenable to modern trends in the microelectronics industry.

In this chapter, a brief introduction to the G^4 -FET will be presented first. C-V modeling for this device will then be described systematically.

2.2 The Four Gate Transistor Structure

The n-channel G^4 -FET (shown in Fig. 2.1 and 2.2) is constructed from a regular p-channel SOI MOSFET (MOS Field-Effect Transistor) (and vice versa) that has two independent body contacts located on either side of the MOSFET. The body contacts are used as source

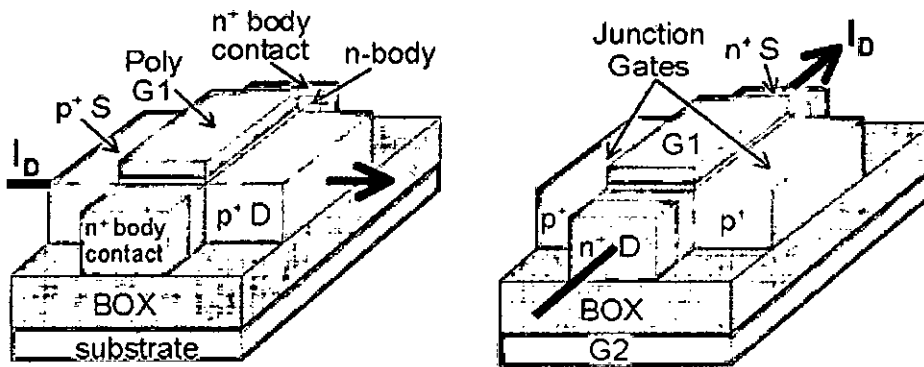


Figure 2.1: Configuration of the n-channel G^4 -FET

and drain for the transversal n-channel JFET (Junction Field-Effect Transistor).

Drain-current, which comprises of majority carriers, flows in the direction perpendicular to that of the p-MOSFET current. Therefore, channel length and width in the G^4 -FET lie along the channel width and length of the conventional SOI MOS. The standard source and drain of the MOSFET are promoted as gates for the JFET and used to control the size of the conductive path. The lateral junction-gates are reverse biased with respect to the channel and provide JFET-like control on the draincurrent. The G^4 -FET can basically be seen as an “accumulation-mode MOSFET featuring two junctiongates” or reciprocally, as a “JFET provided with two MOS gates”. The front gate G1 induces accumulation when the G^4 -FET operates in accumulation mode and induces depletion or inversion when the G^4 -FET operates in buried-channel (volume conduction) mode. The substrate emulates a back gate G2, and its action is similar to that of G1.

It is apparent from the G^4 -FET structure that no specialized processing is required to manufacture the device. The maximum extension of the conductive path corresponds to the gate length of the original MOSFET, whereas the JFET channel length is defined by adjusting the width of the MOSFET. When only the two side gates are operated, the device is somewhat similar to a double-gate MOS transistor. The unique feature of the four gate transistor stems from combining both MOS and junction field-effects to achieve current modulation through four-gate manipulation.

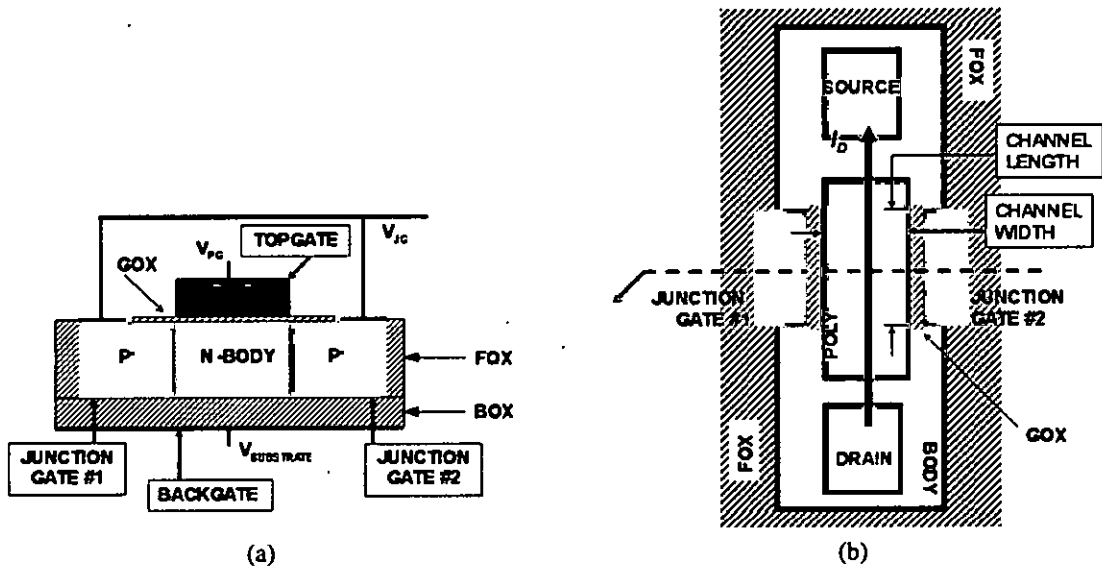


Figure 2.2: G^4 -FET structure (a) cross-section (b) top view

2.3 Features

The G^4 -FET takes advantage of the flexibility and isolation capability of SOI technology which is not feasible in bulk CMOS. It combines both MOS field-effect and junction field-effect to modulate conduction. Furthermore, the device is highly amenable to technology scaling, as narrower channels will enhance pinch-off, particularly for lower channel doping. This unique device can be used to modulate both high and low current levels.

One important fact about the device is that, even in the partially depleted (PD) G^4 -FET, where the classical maximum depletion depth is less than the silicon film thickness ($x_{dmax} < t_{si}$), the body can be fully depleted by reverse-bias on the junction gates [13]. However, in a fully-depleted (FD) G^4 -FET, full body depletion is enabled just by the doping-thickness combination [20].

2.3.1 Modes of Operation

The drain current in the partially depleted G^4 -FET is governed by two mechanisms, depending on which, distinction is made between two operation modes [8]:

- MOSFET mode: near-surface variation of the carrier density in the channel, operation being based on the front surface accumulation current controlled by V_{PG} . In this case, $V_{SUBSTRATE}$ and junction gate voltage V_{JG} are parameters.

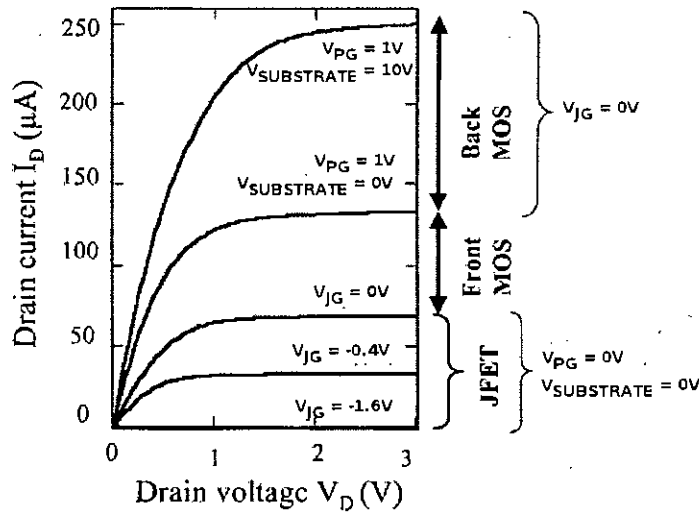


Figure 2.3: Typical output characteristics of the G⁴-FET for various gate bias conditions [13]

- JFET mode: Operation based on the variation of the cross-section of the channel (volume 'neutral' current) controlled by V_{JG} while V_{PG} and $V_{SUBSTRATE}$ are parameters inducing depletion or inversion at the interfaces.

Typical output characteristics for an n-channel G⁴-FET shown in Fig. 2.3 will reveal the operation modes [13]. The bottom three curves correspond to the modulation of the volume current by the JFET effect because the top and back interfaces are weakly depleted and kept fixed at zero bias (channel cross-section is shown in Fig. 2.4(a)). The front gate is driven from depletion to accumulation from the third to fourth curve and this is the front MOS mode of operation. The total drain current is the sum of volume current and top interface accumulation current (Fig. 2.4(b)). An additional current flows from the forth to fifth curve, when the back gate is driven to accumulation, keeping other gate voltages constant (Fig. 2.4(d)). This is the back MOS mode of operation.

2.3.2 Formation of Quantum Wire

When all the four gates are depleted, the conduction aperture formed in the center portion of the transistors body is, in effect, a variable size wire. Furthermore, by varying each gates level of depletion, the wires size and position can be varied within the film. By controlling conduction away from both the top and bottom oxide interfaces, allows the G⁴-FET to

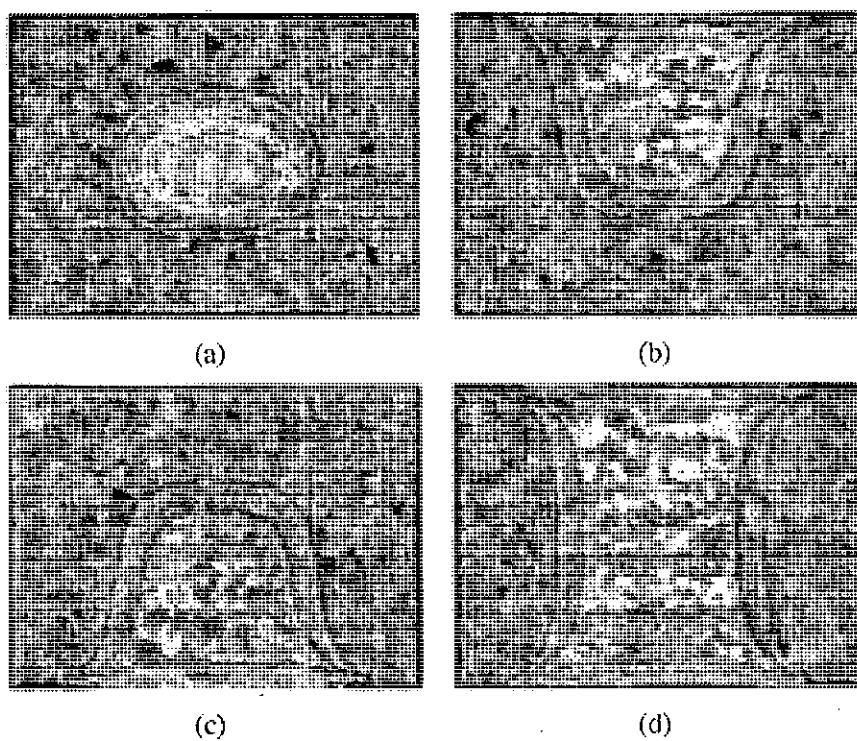


Figure 2.4: Three dimensional simulation of current density in the channel cross-section: (a) volume channel (b) volume and front channels (c) volume and back channels (d) volume, front and back channels [13]

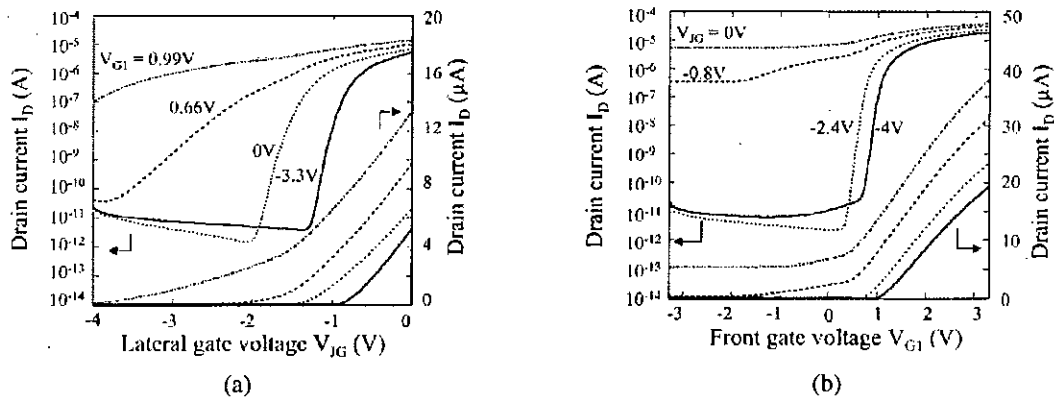


Figure 2.5: (a) Lateral-gate transfer characteristics (b) Front-gate transfer characteristics [13]

achieve very low flicker noise. Interestingly, since the conduction aperture can be focused to very fine dimensions, a quantum wire may be realizable using this structure [7].

2.3.3 Improved Subthreshold Swing

As stated previously in chapter 1, subthreshold swing improves in multiple gate structures. The G^4 -FET can tune the subthreshold swing of a selected gate with varying bias on a separate gate, making modulation and optimization easier [12]. As reported by Dufrene *et al.* [13] considerable improvement in subthreshold swing is achieved when the front interface is in depletion or inversion (volume current) (Fig. 2.5a). Excellent swing values as low as 65 mV/dec, which is unachievable in regular PD SOI MOSFETs, are obtained with respect to lateral gates when front interface is in inversion. Inherent to this structure used to measure subthreshold characteristics, for the p-channel MOSFET, the minimum swing value for the front-gate characteristics achievable is 78 mV/dec whereas it is 75 mV/dec when the junction gates are strongly reverse-biased ($V_{JG} = -2.4V$ and $V_{JG} = -4V$) (Fig. 2.5b).

Considering the above facts, it is apparently clear that, four-gate modulation opportunities provided by this new device open the door for many new circuit opportunities in analog, RF, mixed-voltage, and digital applications and ensure improved current drive and subthreshold characteristics. Much work is needed, however, to fully explore the capabilities of this new device.

2.4 The MOS Capacitor

The MOS capacitor structure is the heart of the MOSFET. A great deal of information about oxide-semiconductor interface and any MOS device can be obtained from the capacitance-voltage or C-V characteristics of the device. The capacitance of a device is defined as:

$$C = \frac{dQ}{dV} \quad (2.1)$$

where dQ is the magnitude of the differential change in charge on one plate as a function of the differential change in voltage dV across the capacitor.

There are three operating conditions of interest in the MOS capacitor: accumulation, depletion and inversion [24]. During accumulation, a small differential change in voltage across the MOS structure will cause a differential change in charge on the metal gate and also in accumulation charge, which occur at the edges of the oxide, as in a parallel-plate capacitor. In the inversion mode, also, a small incremental change in voltage will cause a differential change in the inversion layer charge density at oxide-semiconductor interface. Thus the capacitance per unit area for accumulation and inversion mode is just the oxide capacitance, or

$$C(acc) = C(inv) = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad [Fm^{-2}] \quad (2.2)$$

ϵ_{ox} and t_{ox} are the permittivity and thickness of oxide respectively.

In depletion mode, the oxide capacitance and the capacitance of the depletion region are in series. A small differential change in voltage across the capacitor will cause a differential change in space charge width. The total capacitance of the series combination is:

$$\frac{1}{C(depl)} = \frac{1}{C_{ox}} + \frac{1}{C_{SD}} \quad [Fm^{-2}] \quad (2.3)$$

where, $C_{SD} = \frac{\epsilon_s}{x_d}$, ϵ_s and x_d being the permittivity of the semiconductor and space charge width respectively.

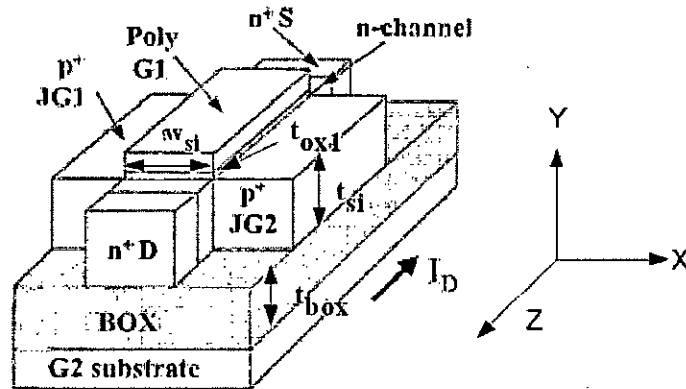


Figure 2.6: The analyzed G⁴-FET structure

2.5 Capacitance-Voltage Modeling for the G⁴-FET

A semi-classical model to predict the effect of different gate biases on the C-V characteristics for a partially depleted G⁴-FET has been developed. Detailed description of the procedure is given in subsequent sections.

2.5.1 Device Description

The n-channel G⁴-FET shown in Fig. 2.6 has been analyzed in this work. 2D schematic diagram of the device is shown in Fig. 2.7

Parameters are selected for the device according to Cristoloveanu et al [8]. The simulated G⁴-FET had a 5 nm thick gate-oxide, a 100 nm thick active silicon layer and a 100 nm thick buried oxide. The channel width (between the two lateral gates) was 0.3 μm . Because the G⁴-FET is an accumulation mode device, the transistor body received a $2 \times 10^{17} \text{ cm}^{-3}$ N-type doping. The lateral gates had a $2 \times 10^{20} \text{ cm}^{-3}$ P-type doping. A thick silicon layer ensures that the device will operate in partial depletion mode.

2.5.2 Poisson's Equation

General Poisson's Equation in three dimensional cartesian co-ordinate system is written as:

$$\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}\right)V(x,y,z) = -\frac{\rho(x,y,z)}{\epsilon} \quad (2.4)$$

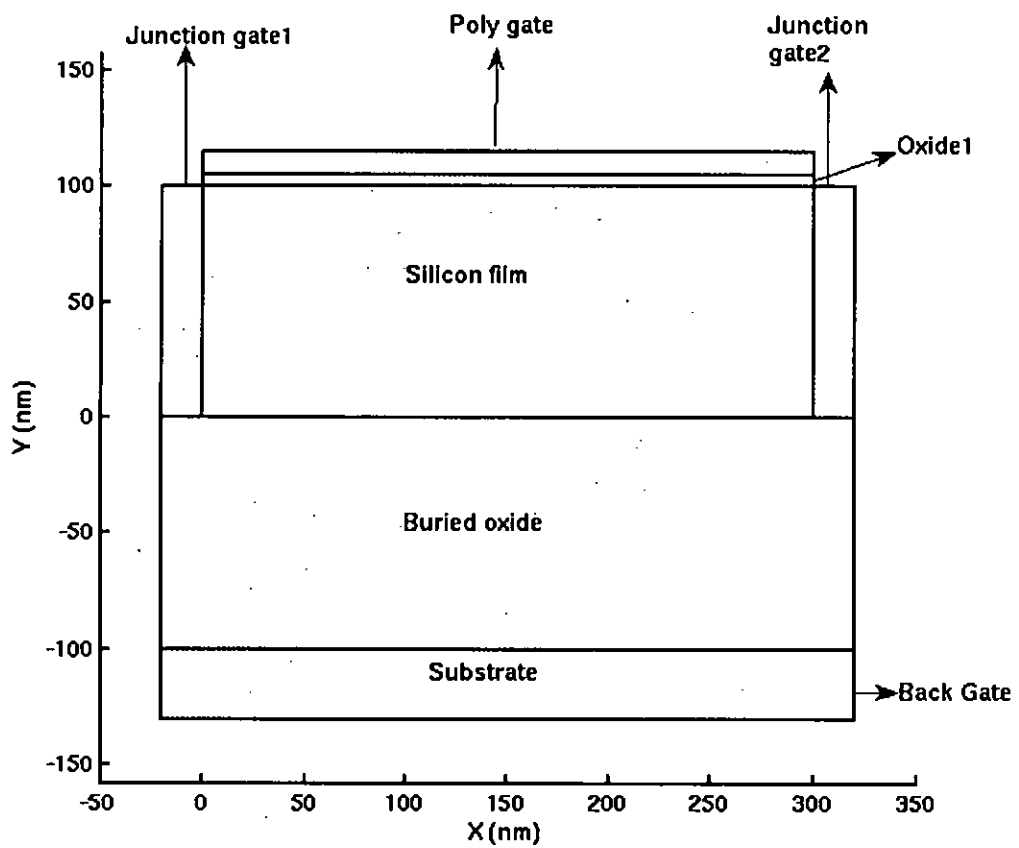


Figure 2.7: 2D geometry of the analyzed structure

where, V is the potential, ρ is the charge density and ϵ is the permittivity. Both V and ρ are functions of space co-ordinates.

In order to find the C-V characteristics, we solved two dimensional Poisson's equation.

In two dimension, Eq. (2.4) reduces to the following form and is used to find the potential profile inside the Four Gate Transistor:

$$\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}\right)V(x,y) = -\frac{\rho(x,y)}{\epsilon} \quad (2.5)$$

Assuming zero flat band voltage and negligible potential drop in the lateral junction gates, 2D Poisson's equation was solved for the active silicon and oxide regions. This assumption reduces simulation time considerably without introducing significant error in results. Eq. (2.5) is repeated below once again for the two regions:

$$\begin{aligned} \left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}\right)V(x,y) &= -\frac{\rho(x,y)}{\epsilon_0 K_{si}}, & 0 < x < w_{si} \text{ and } 0 < y < t_{si} \\ &= 0, & 0 < x < w_{si}, t_{si} < y < t_{si} + t_{ox} \text{ and } -t_{box} < y < 0 \end{aligned} \quad (2.6)$$

where, K_{si} is the dielectric constant of silicon and ϵ_0 is the free space permittivity. Charge density is calculated from:

$$\rho(x,y) = q[p(x,y) - n(x,y) + N_D^+ - N_A^-] \quad (2.7)$$

$p(x,y)$, $n(x,y)$, N_D^+ and N_A^- respectively being the hole, electron, ionized donor and ionized acceptor concentration. If complete ionization is assumed, N_D^+ will be equal to donor concentration, N_D and N_A^- will be equal to acceptor concentration, N_A .

2.5.3 Semi-Classical Solution using Comsol Multiphysics

Comsol is a powerful, interactive environment for modeling and solving scientific and engineering problems based on partial differential equations. It is extremely powerful because of its integration with MATLAB. Comsol along with MATLAB was used for rigorous simulations throughout this work.

Poisson's equation in coefficient form is given in Comsol as:

$$-\nabla \cdot (c \nabla u) = f \quad (2.8)$$

where,

c = permittivity of the subdomain, $K\epsilon_0$

u = electrostatic potential, $V(x, y)$

f = charge density termed as source term, $q[p(x, y) - n(x, y) + N_D - N_A]$

concentration of hole and electron are calculated using semi-classical formulae:

$$p(x, y) = p_0 \exp\left(\frac{-V(x, y)}{V_t}\right) \quad (2.9)$$

$$n(x, y) = n_0 \exp\left(\frac{V(x, y)}{V_t}\right) \quad (2.10)$$

where, n_0 and p_0 are equilibrium electron and hole concentrations, respectively. Assuming complete ionization, $n_0 = N_D$ and $p_0 = \frac{n_i^2}{n_0}$, n_i being the intrinsic carrier density.

Solving Poisson's Equation

As stated earlier, for valid reasons, we solved Poisson's equation iteratively inside the oxide and semiconductor regions only. Therefore, the device geometry shown in Fig. 2.8 with the silicon and oxide regions was defined first.

Appropriate boundary conditions were set through Comsol linear PDE solver. Dirichlet boundary conditions were used at boundaries 7, 2, 3 and 9 that equal top gate, back gate, junction gate1 and junction gate 2 applied bias respectively. For simplicity, we assumed the two junction gates tied, i.e. $V_{JG1} = V_{JG2} = V_{JG}$. Neumann boundary condition for continuous electric field was set at all other boundaries and interfaces.

The source term in Poisson's equation was calculated using Eq. (2.7), (2.9) and (2.10) for a trial potential profile with zero voltage at every point inside the semiconductor. Eq. (2.8) was then solved to find a new potential profile which was used to find the source term for next iteration. A fine mesh-grid was created to compare the newly calculated potential with the previous solution after each iteration. This procedure was repeated in an iterative fashion until a convergence criteria [for successive iteration, change in electrostatic potential at

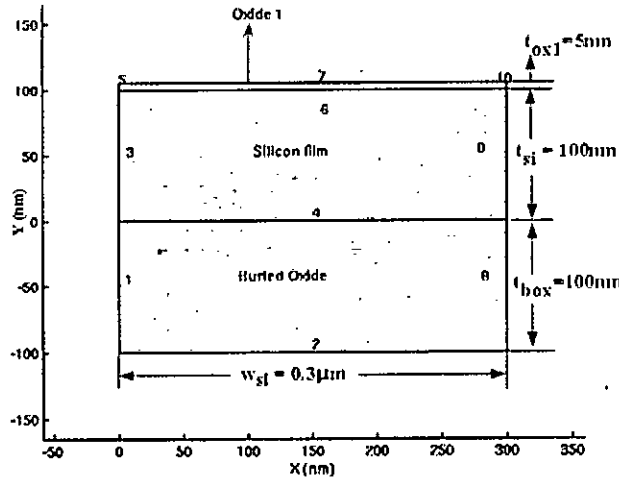


Figure 2.8: 2D geometry of the simulated structure

every grid point should be less than 10^{-5}] was satisfied. Hence we get the actual potential profile. A sample potential profile for depletion all around operation ¹ is shown in Fig. 2.9 and 2.10 which results in the majority carrier concentration profile as displayed in Fig. 2.11

Gauss-Seidel iteration method has been used for numerical convergence throughout the work. The electrostatic potential was updated according to Eq. (2.11) after each iteration was completed to renew the source term for the next iteration.

$$V = V_{new} \times (1 - \alpha) + V_{old} \times \alpha \quad (2.11)$$

Here, α is the weighting vector which should be greater than 0.9. The higher the weighting factor, the higher the assurance of convergence, but the simulation time and no of required iterations increase as well. Therefore, a compromise is to be made while selecting the weighting factor.

Charge Calculation and C-V

Poisson's equation was solved sweeping top gate bias for a range of -4V to +3V. Back gate and junction gate voltages are kept as parameters. Charge density per unit length was then calculated using Eq. (2.12):

$$Q_{total} = q \int_{y=0}^{t_{si}} \int_{x=0}^{w_{si}} [p(x,y) - n(x,y) + N_D - N_A] dx dy \quad (2.12)$$

¹ $V_{PG} = -5V$, $V_{SUBSTRATE} = -10V$, and $V_{JG} = -1V$

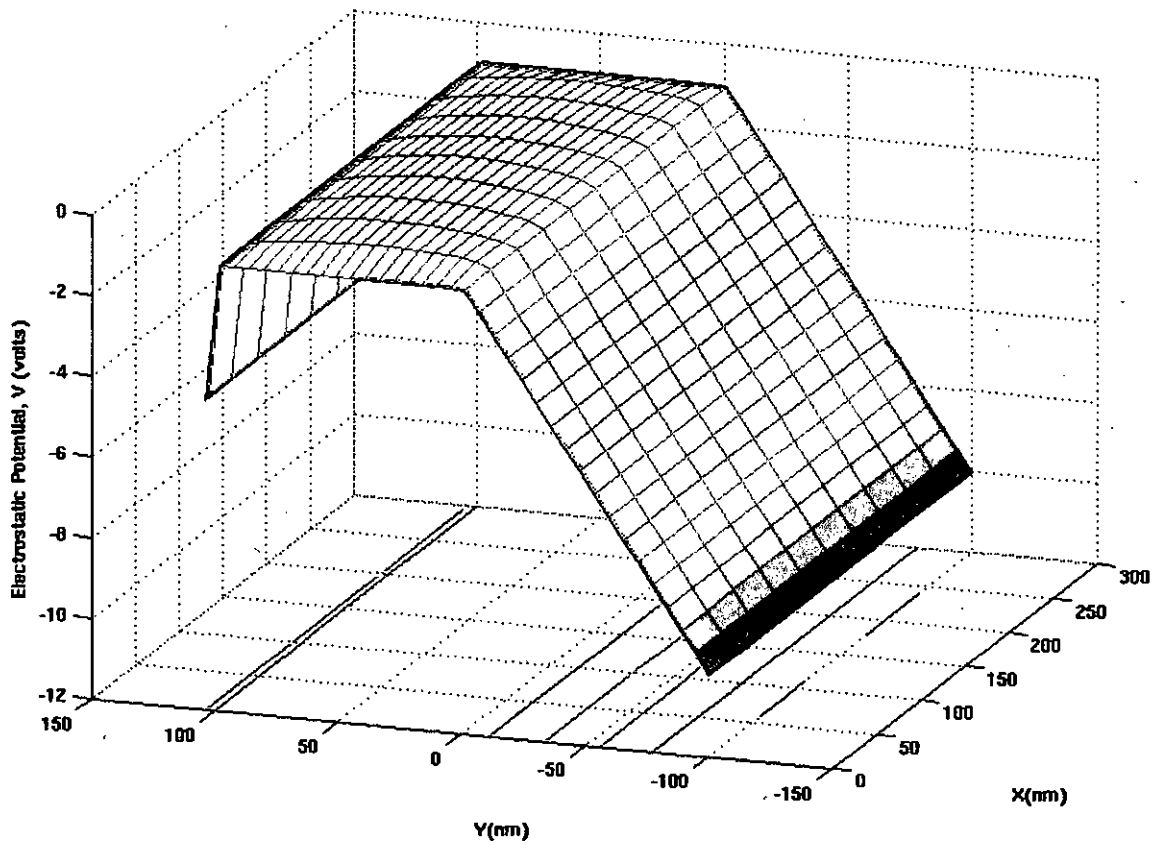


Figure 2.9: Electrostatic potential profile in oxide and active silicon areas inside G^4 -FET

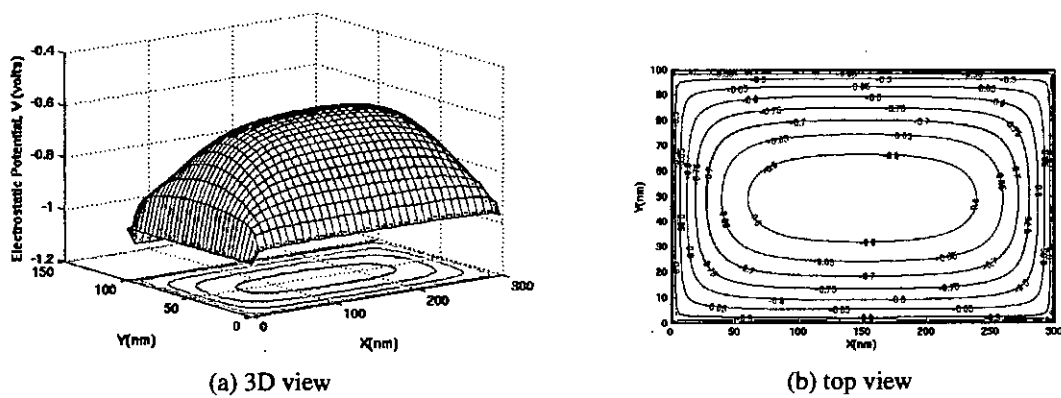


Figure 2.10: Electrostatic potential profile in active silicon areas inside G^4 -FET

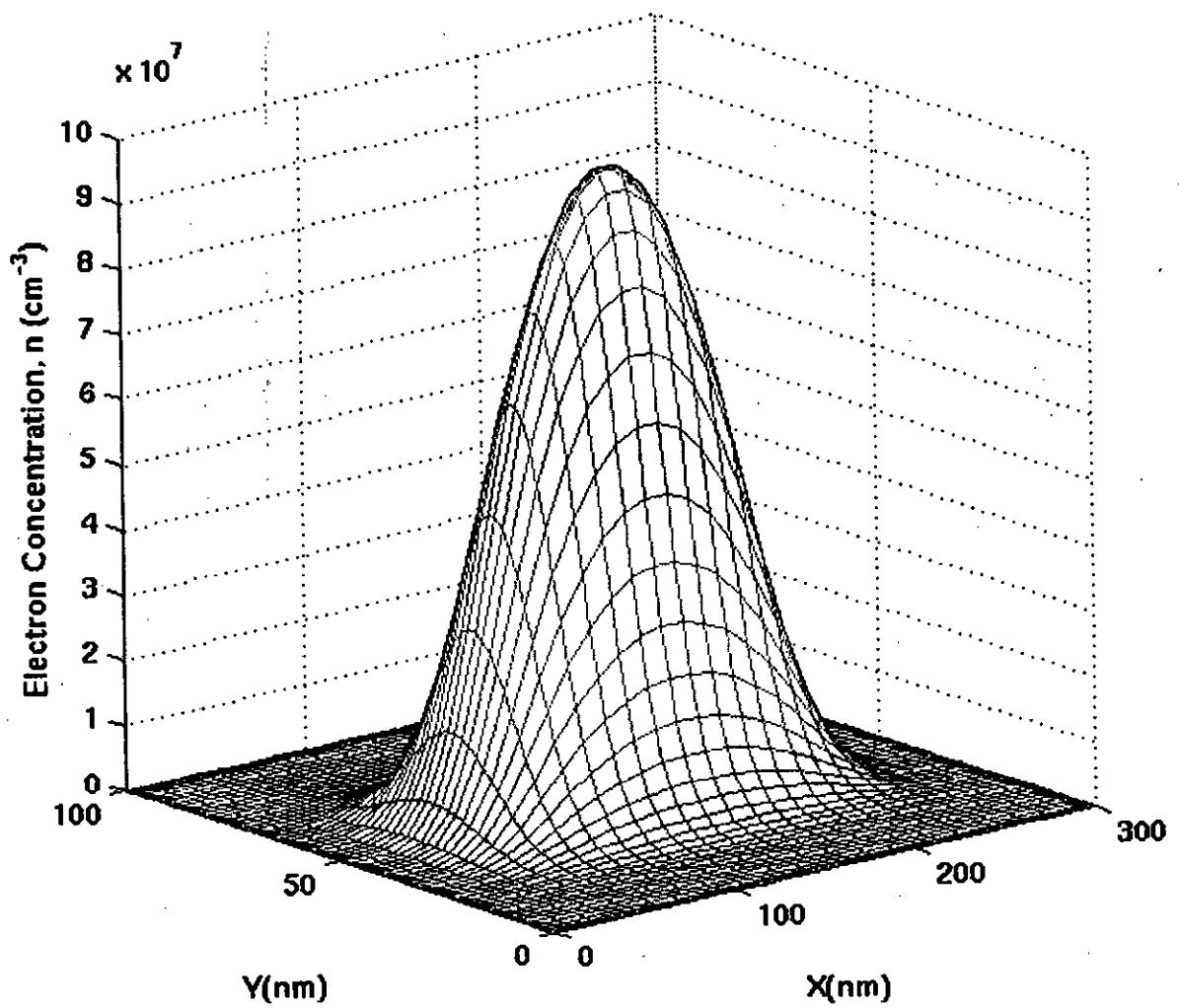


Figure 2.11: Concentration profile of the G⁴-FET with main conduction in the middle channel

where,

Q_{total} = total charge at any particular top gate voltage per unit length [Cm^{-1}]

Charge calculation finally leads to exploring C-V. Our simulated device had 4 gates surrounding the silicon film, thereby demanding charge calculation per unit length of the device. And hence, we get capacitance in per unit length. Capacitance was found by calculating the differential change in charge (Q_{total}) for a differential change in voltage. Eq. (2.1) will be repeated here for front gate capacitance, C_{PG} as the gate voltage, V_{PG} is varied:

$$C_{PG} = \frac{dQ_{total}}{dV_{PG}} \quad [Fm^{-1}] \quad (2.13)$$

For accumulation and inversion modes of operation, Eq. (2.2) will be revised here for capacitance in per unit length:

$$C(acc) = C(inv) = C_{ox} = \frac{\epsilon_{ox} w_{si}}{t_{ox}} \quad [Fm^{-1}] \quad (2.14)$$

Validity of the above model will be checked and discussed in the following section.

2.6 Validity of the model

In order to test the validity of the proposed model, a double gate SOI structure was simulated with device dimensions and doping adopted for the G^4 -FET throughout this work. Device physics and boundary conditions were described for Fig. 2.8 with Dirichlet boundary condition at boundary no. 2 and 7 only, keeping junction gates open. 2D and 3D sample potential profiles for front gate accumulation² are shown in Fig. 2.12.

A positive 0.5 V bias at front gate induce accumulation at the gate. The majority carrier (electron), minority carrier (hole) and total charge profile inside the silicon film are shown in Fig. 2.13, 2.14 and 2.15.

Because Neumann boundary condition was used at lateral junction gates, the electrostatic potential and carrier concentration profiles are symmetric in between the junction gates. Positive bias at the front gate induces a very thin accumulation channel. Most of

² $V_{PG} = 0.5V$ and $V_{SUBSTRATE} = 0V$

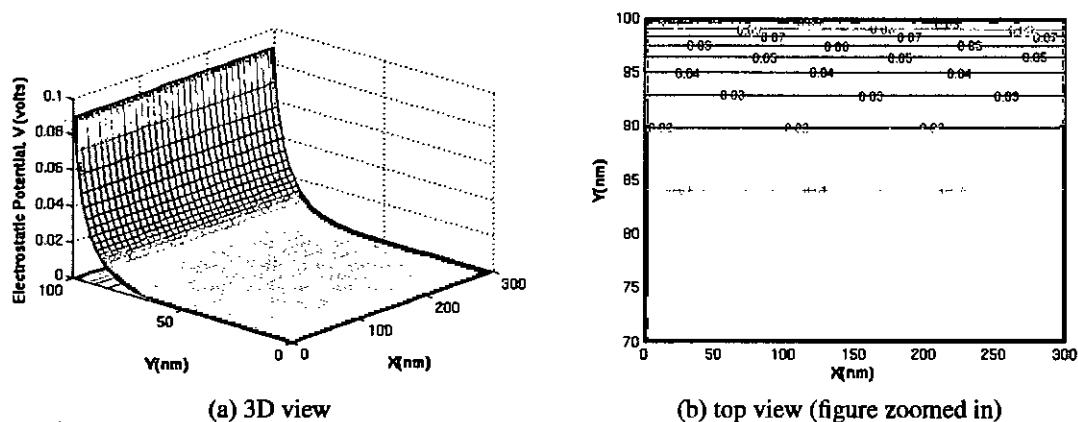


Figure 2.12: Electrostatic potential profile in active silicon area inside G^4 -FET

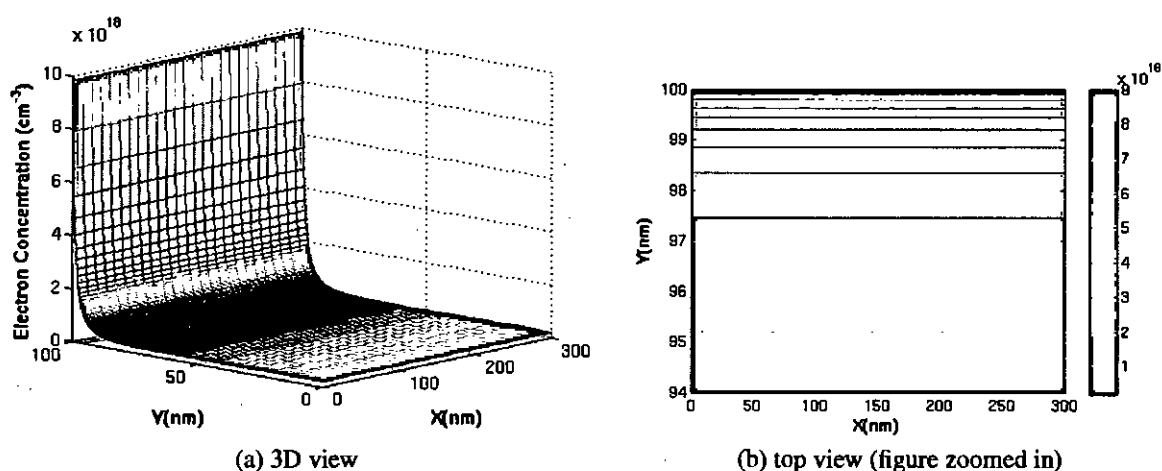


Figure 2.13: Majority carrier, n , concentration profile in active silicon area inside G^4 -FET

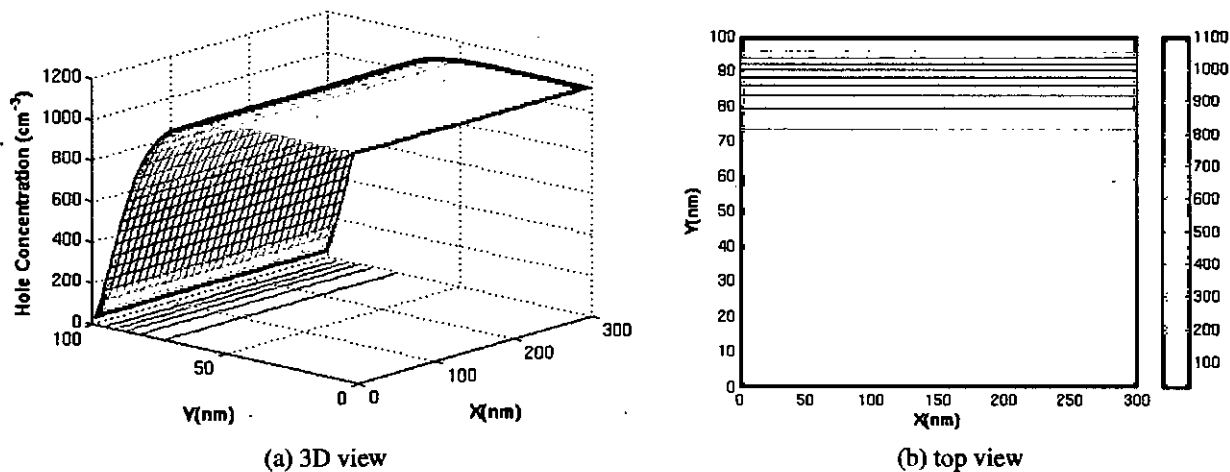


Figure 2.14: Minority carrier, p , concentration profile in active silicon area inside G^4 -FET

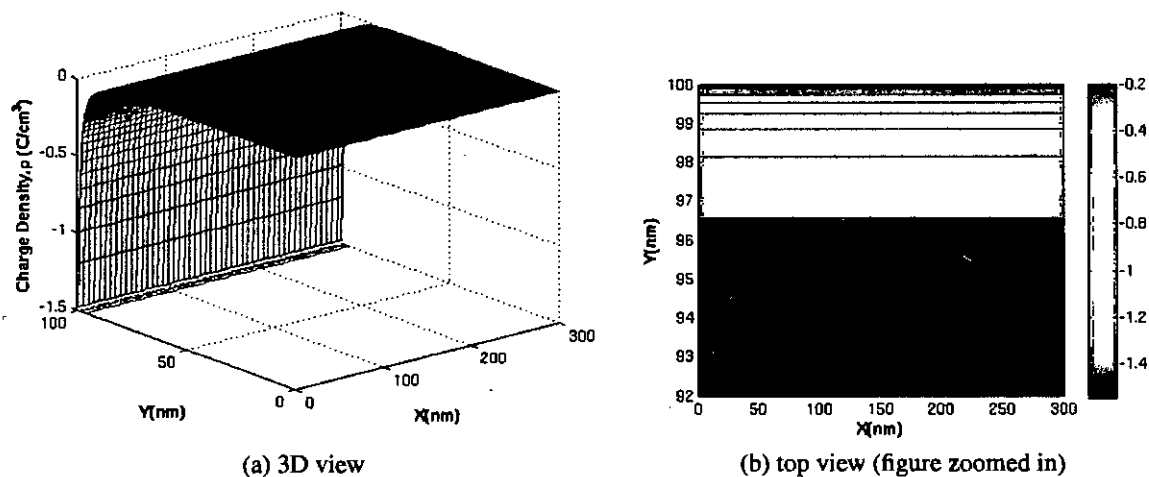


Figure 2.15: Total charge, ρ , concentration profile in active silicon area inside G^4 -FET

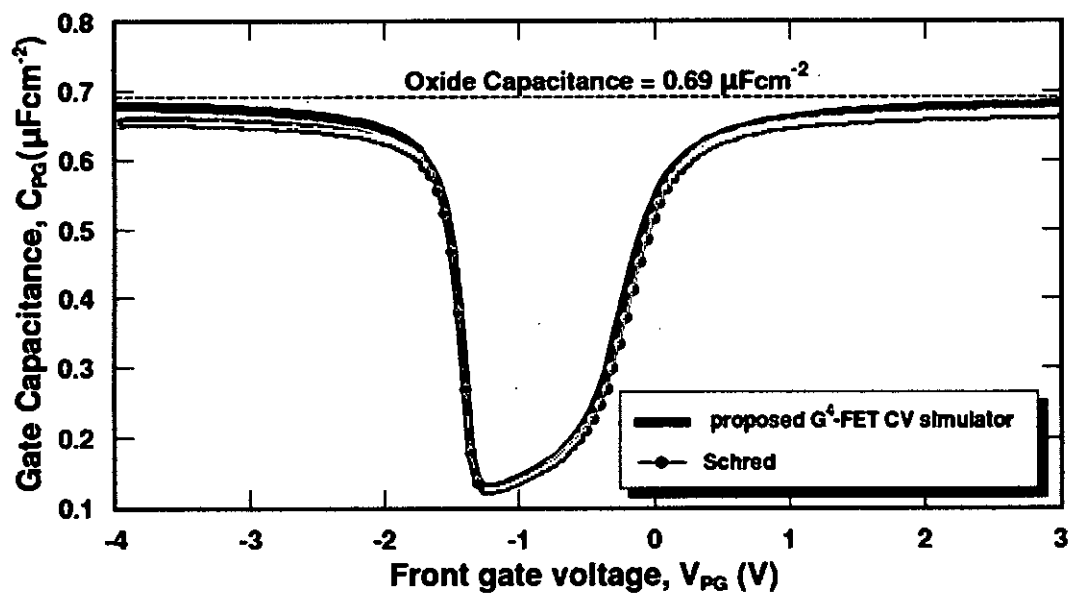


Figure 2.16: Comparison between Schred calculated and G^4 -FET simulator calculated C-V

the changes in the electrostatic potential, therefore, occurs along a very thin region at the oxide-silicon interface. Capacitance per unit area was calculated as described in previous chapter and was compared with results from Schred [25], a well known established 1D numerical solver. Semi-classical charge model was selected for simulation and the plotted C-V was found to closely coincide with the C-V as found from our simulator [Figure 2.16].

Chapter 3

Results and Discussion

3.1 Introduction

Impacts of different gate bias on the C-V characteristics will be studied in this chapter with the help of simulation results. These will illustrate the effects of different gate biases on the C-V characteristics of the PD G⁴-FET.

Oxide capacitance for the device described in subsection 2.5.1 is calculated using equation 2.14 to be 20.7 pFcm⁻¹. Therefore, a capacitance nearly equal to 20.7 pFcm⁻¹ is expected in the inversion and accumulation regions.

3.2 Effect of Junction Gate bias

First thing to note about PD G⁴-FET C-V characteristics is that there is a minimum non-zero value capacitance in depletion region of operation. This is because, the body is partially depleted, so even when there is no accumulation or inversion, depletion area changes with change in applied gate bias.

3.2.1 Observations

The C-V resembles a double gate SOI MOSFET when junction gates are floating. As we apply 0V bias at lateral junction gates, the capacitance is slightly reduced in depletion mode. From Fig. 3.1 it is observed that at depletion, the capacitance is slightly reduced than the floating gate case. Although the characteristic nature exactly follows the floating gate during accumulation, inversion is somewhat delayed with 0V applied bias. Contrary to this, when -1V bias is applied to junction gates, accumulation is delayed, but inversion starts earlier i.e. at reduced voltage and it matches with the floating gate at inversion.

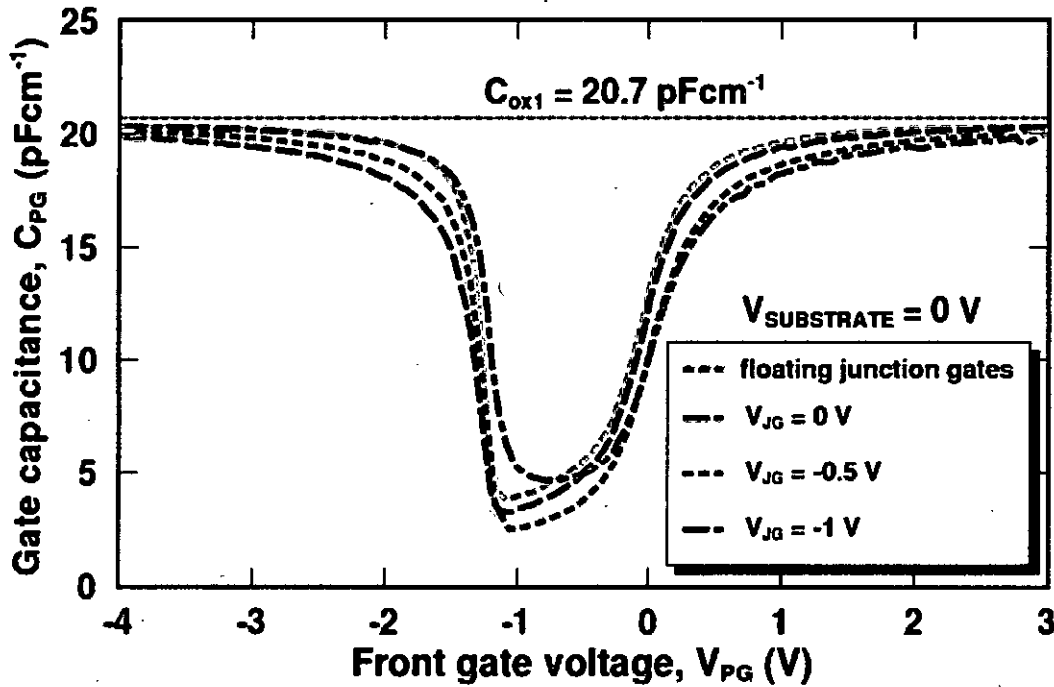


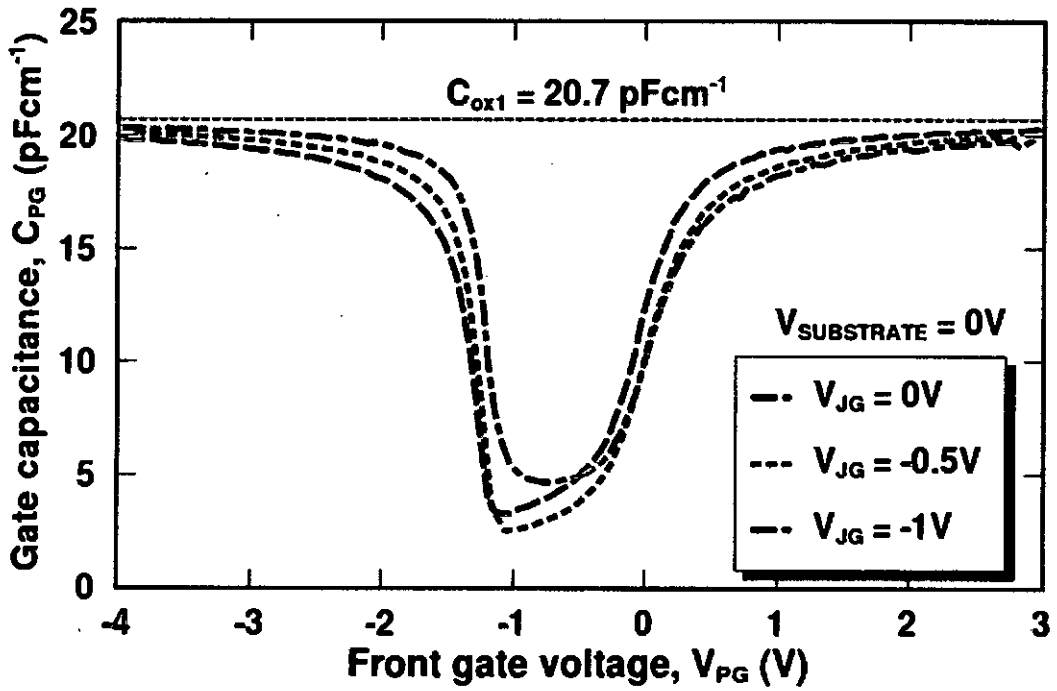
Figure 3.1: Effect of junction gate bias over floating gates

C-V characteristics are compared for different junction gate bias at various back gate voltage in Figure 3.2 (a), (c) and (b).

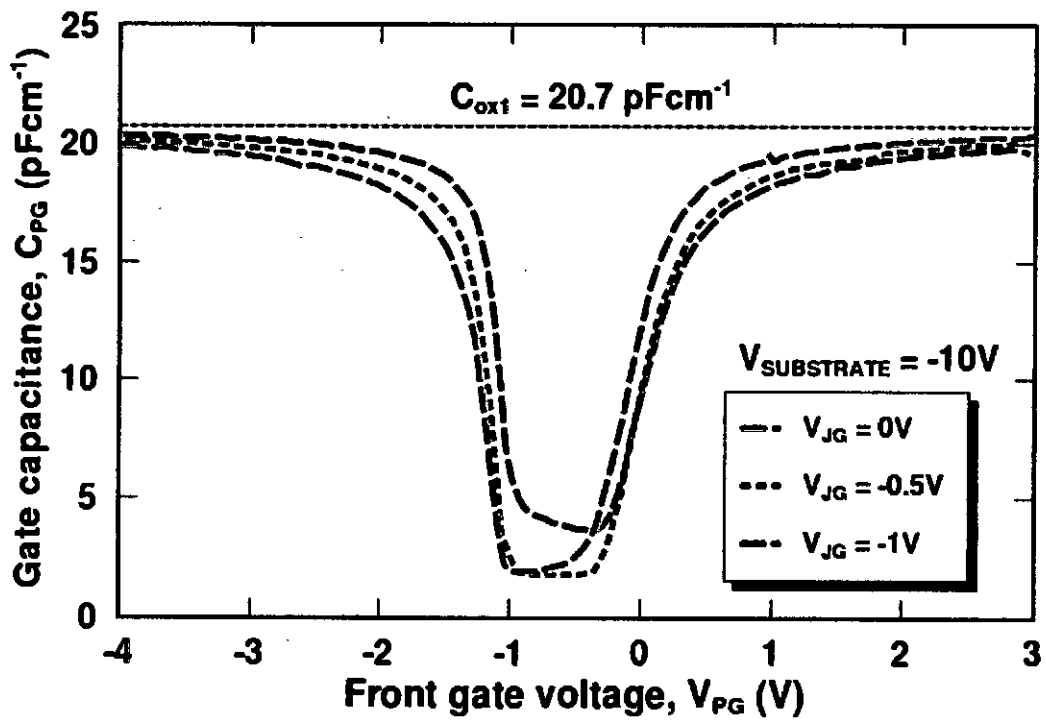
From the three figures, it is clearly evident that, junction gate bias has a significant effect on C-V characteristics and the effect is identical for back gate at 0V, inversion ($V_{SUBSTRATE} = -10\text{V}$) or accumulation ($V_{SUBSTRATE} = 10\text{V}$). As we apply a moderate reverse bias of -0.5 V at junction gates, capacitance in depletion mode is reduced while at -1V strong reverse bias, the capacitance increases. With reverse bias applied at junction gates, front gate inversion occurs at a lower voltage and the rise from depletion to inversion is sharper than that at 0V bias. Opposite is the case for front gate accumulation. The rise to accumulation is delayed at reverse bias and a large voltage is needed to obtain the constant capacitance value at accumulation.

3.2.2 Discussions

Effects of junction gate bias on C-V characteristics will be discussed for back gate at 0V bias (Figure 3.2 (a)). The reduction in capacitance with moderate reverse bias of -0.5V at junction gates and the increase in same with strong reverse bias of -1V at junction gates, in

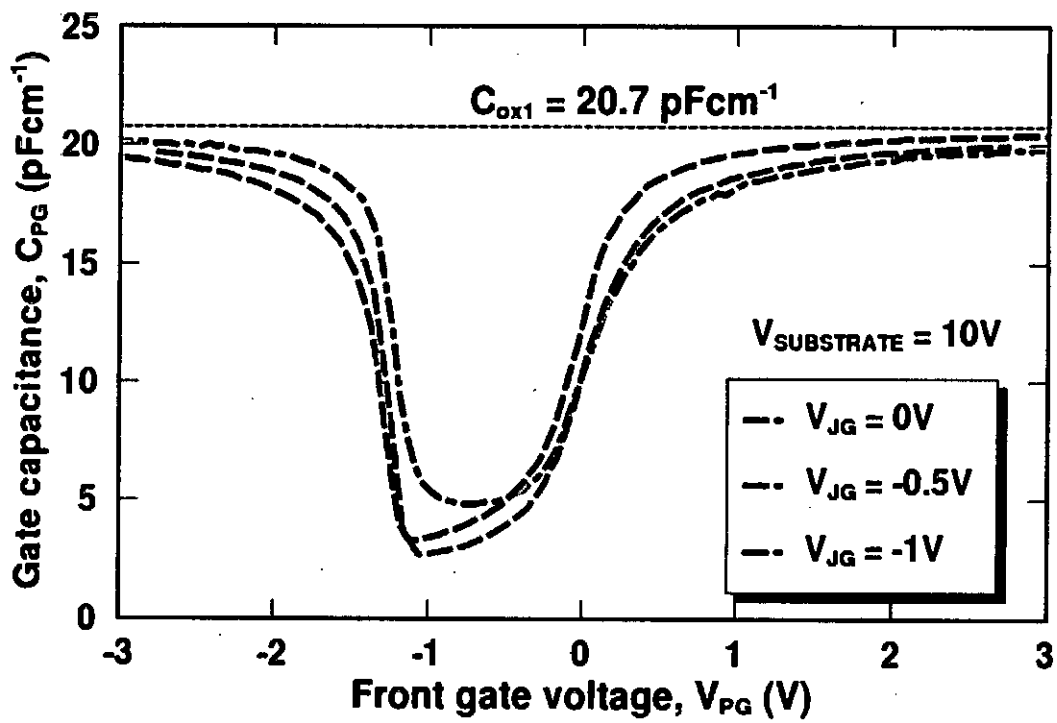


(a) Effect of junction gate bias with back gate at 0V



(b) Effect of junction gate bias with back gate at -10V

Figure 3.2: Effect of junction gate bias with various back gate voltages



(c) Effect of junction gate bias with back gate at +10V

Figure 3.2: Effect of junction gate bias with various back gate voltages (cont'd)

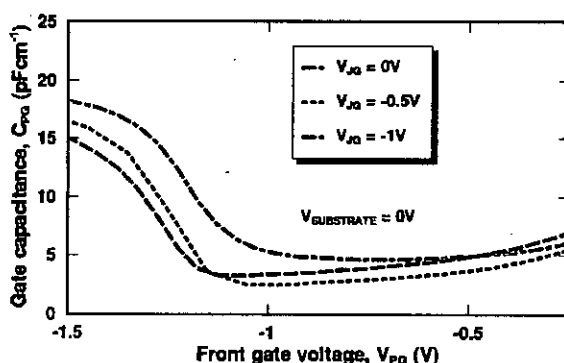


Figure 3.3: Capacitance in depletion region with varying junction gate bias

depletion region of operation (Figure 3.3), can be explained using Figure 3.4 (a), (b) and (c)

If the change in charge density occurs far away from the gate at which the voltage is swept, we expect a reduction in capacitance. Comparing Figure 3.4 (a), and (b) we see that, most of the change in charge density, as $-0.5V$ junction gate bias is applied, occurs far from the gate than that with $0V$ bias, thereby reducing the capacitance. In fact, at $V_{JG} = -0.5V$, depletion area increases (Figure 3.5), indicating a reduced amount of change in charge for the same amount of change in voltage, which leads to the reduction in capacitance. But, as V_{JG} is further increased to $-1V$, capacitance is found to increase in the depletion region. This is because, at $-1V$ bias, we can observe a sharp change in charge density (Figure 3.4 (c)) near the junction gates at the front gate. An increase in differential change in charge density, which occurs at the front interface, essentially increases the capacitance.

An increase in reverse bias at the junction gates will enhance inversion (Figure 3.6). Comparing Figure 3.7 (a), (b) and (b), we will see that as we go on increasing junction gate voltage, inversion charge at front gate will increase. This phenomenon is further illustrated in Figure 3.8 which shows that at $V_{JG} = -1V$, there is a huge increment in inversion charge at the front interface, which indicates that at this voltage, the front interface edges are deeper in inversion and hence, the capacitance is the largest at this voltage.

Increase in junction gate reverse bias will delay the achievement of accumulation (Figure 3.9). Figure 3.10 (a), (b) and (c) will show that, reverse bias at the junction gates retard the accumulation of majority carrier, electron at front interface near junction gate edges which is more clearly illustrated in Figure 3.11. A reduction in the accumulation of majority carriers will certainly reduce the capacitance.

Similar discussions apply to Figure 3.2 (b) and (c) in explaining the effects of junction

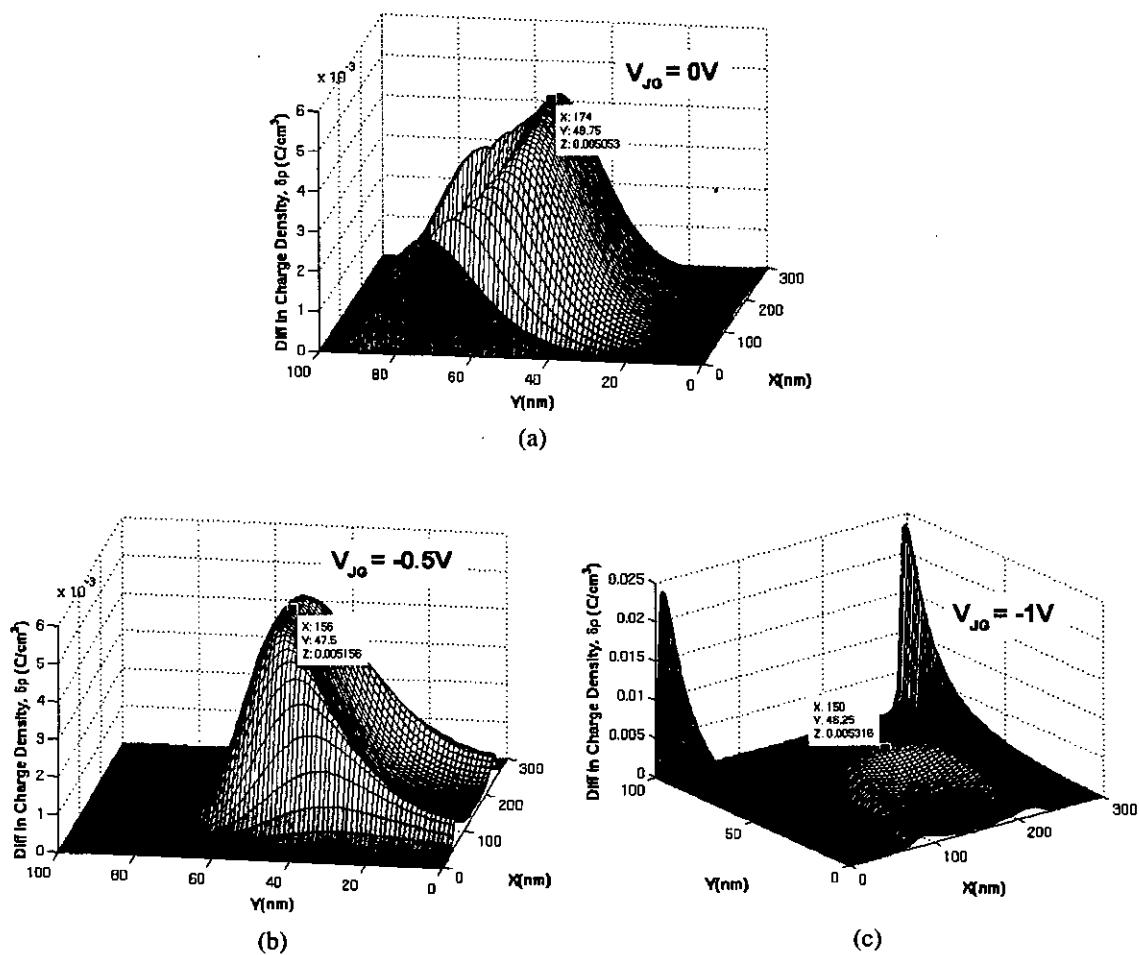


Figure 3.4: Spatial variation of differential change in charge density for a 0.1V change in V_{PG} in depletion region

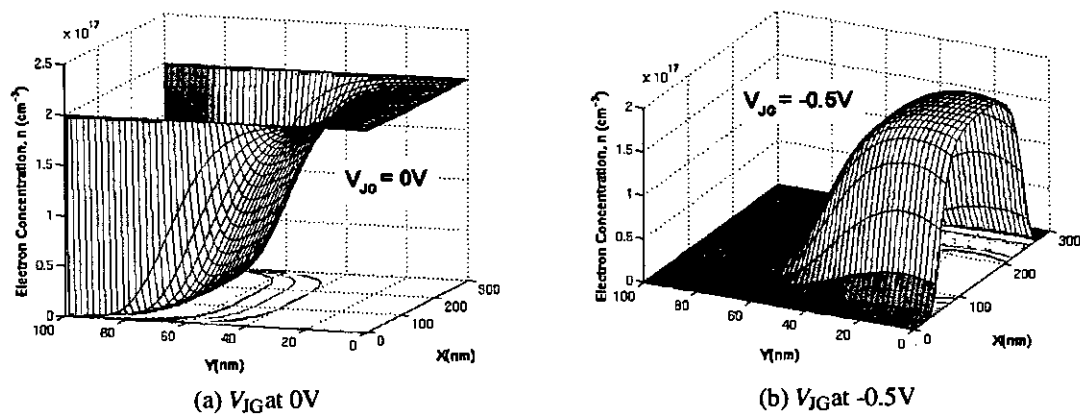


Figure 3.5: Majority carrier concentration with $V_{SUBSTRATE} = 0V$ and $V_{PG} = -0.7V$

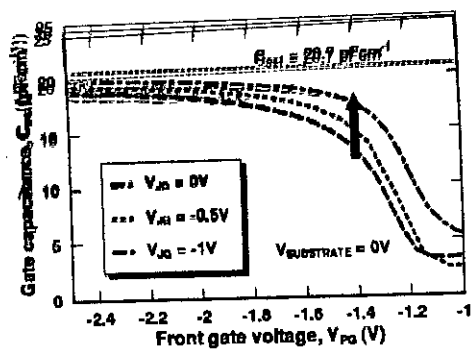


Figure 3.6: Capacitance in inversion region with varying junction gate bias

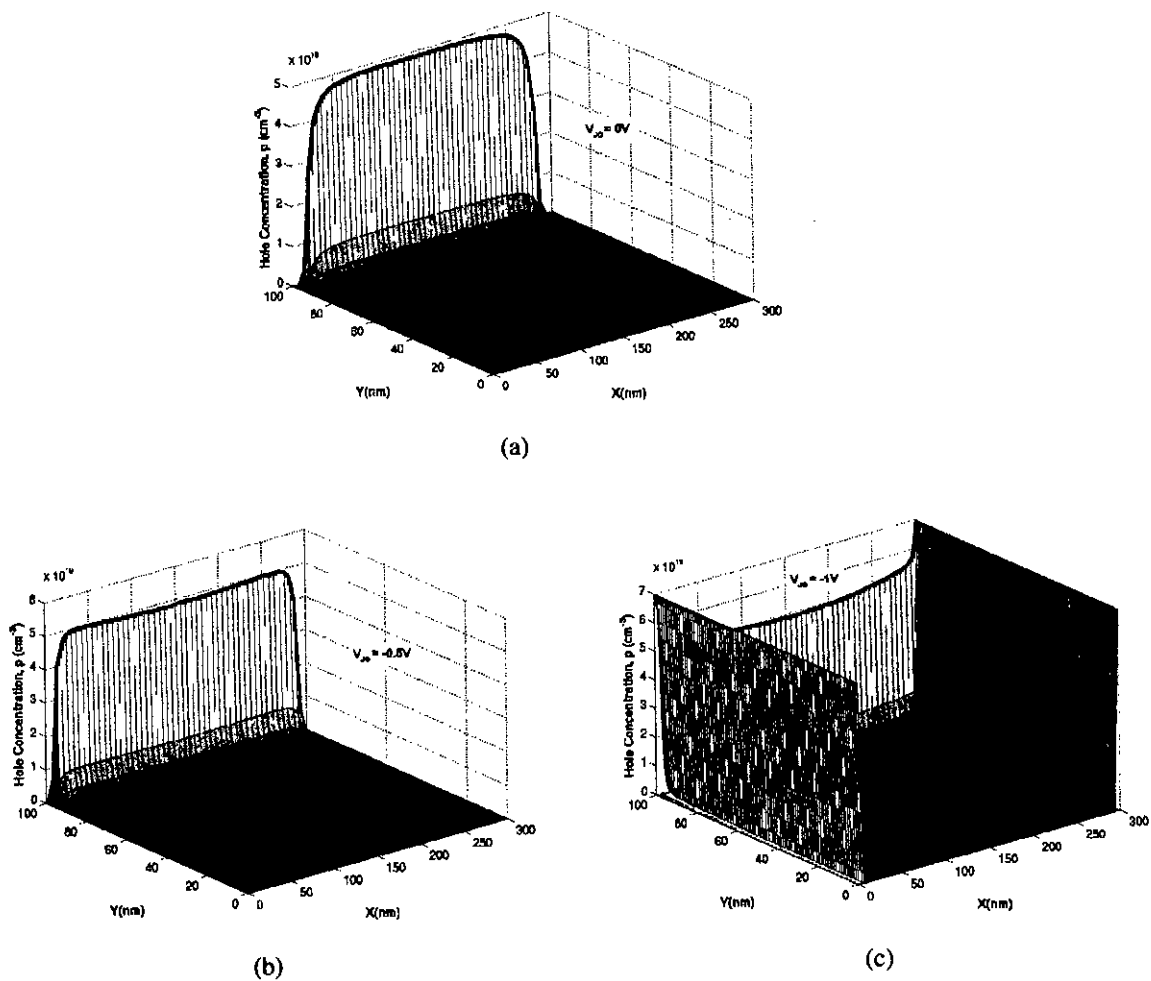


Figure 3.7: Minority carrier, hole concentration at different junction gate bias for $V_{\text{SUBSTRATE}} = 0\text{V}$ (plots generated at $V_{\text{PG}} = -2\text{V}$)

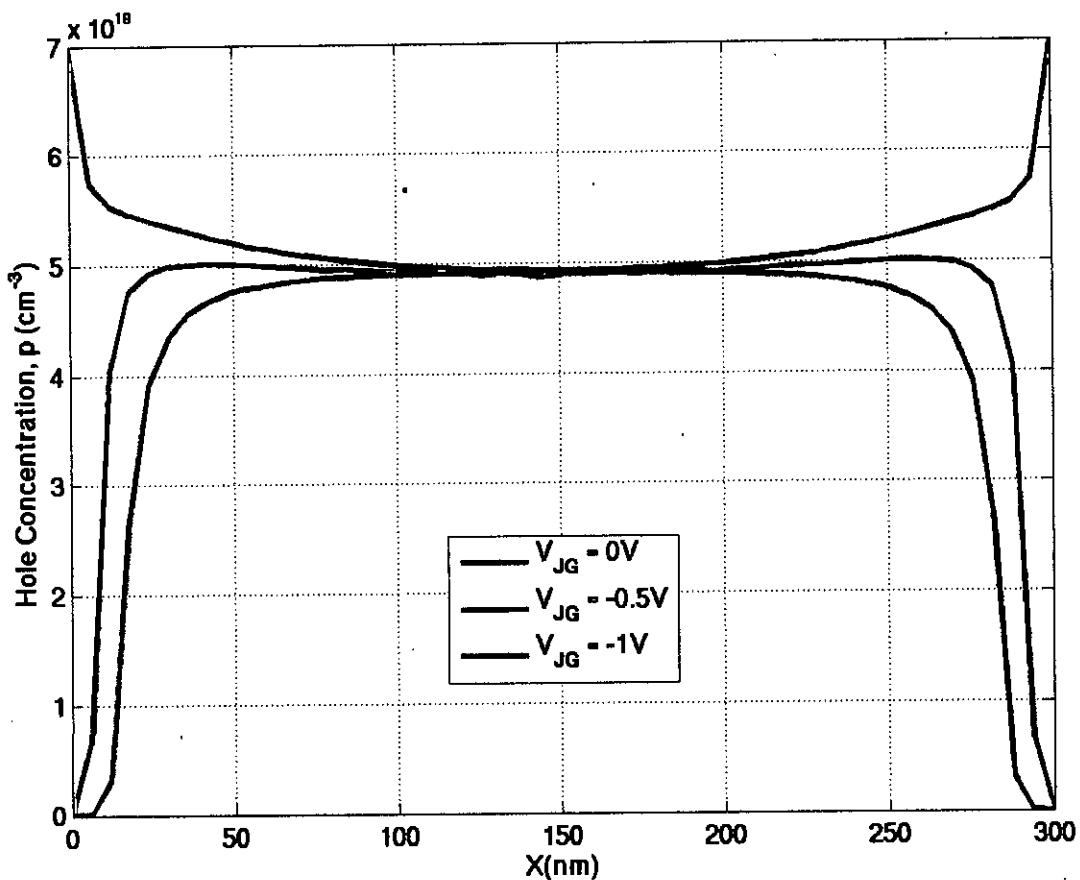


Figure 3.8: Hole concentration at front interface (plot generated at $V_{PG} = -2V$)

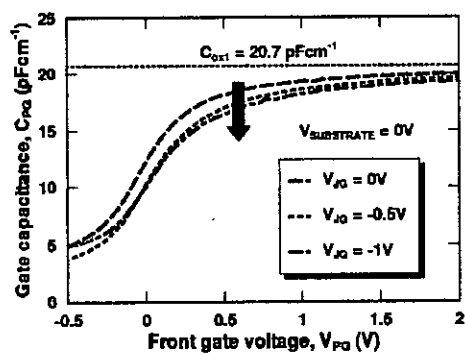
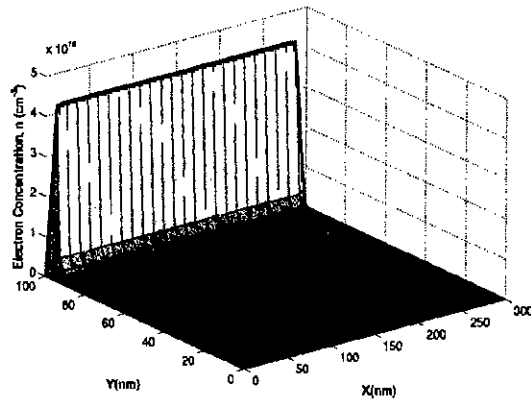
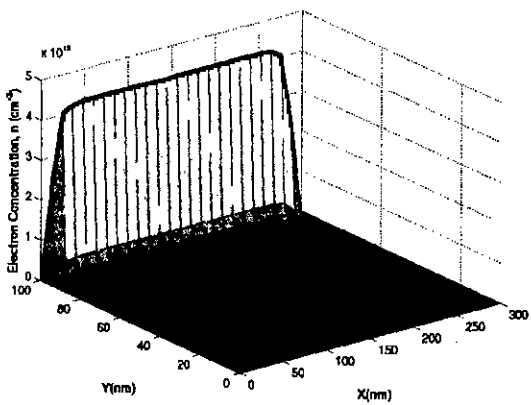


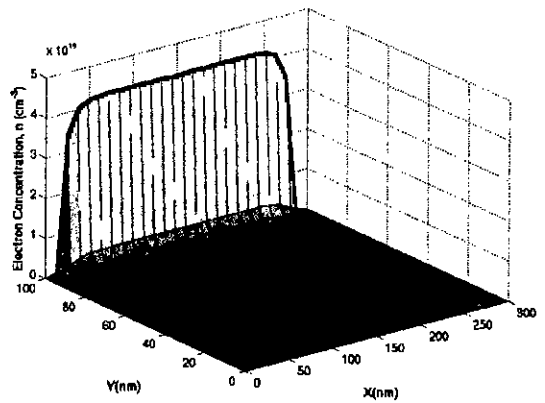
Figure 3.9: Capacitance in accumulation region with varying junction gate bias



(a)



(b)



(c)

Figure 3.10: Majority carrier, electron concentration at different junction gate bias for $V_{\text{SUBSTRATE}} = 0\text{V}$ (plots generated at $V_{\text{PG}} = 1\text{V}$)

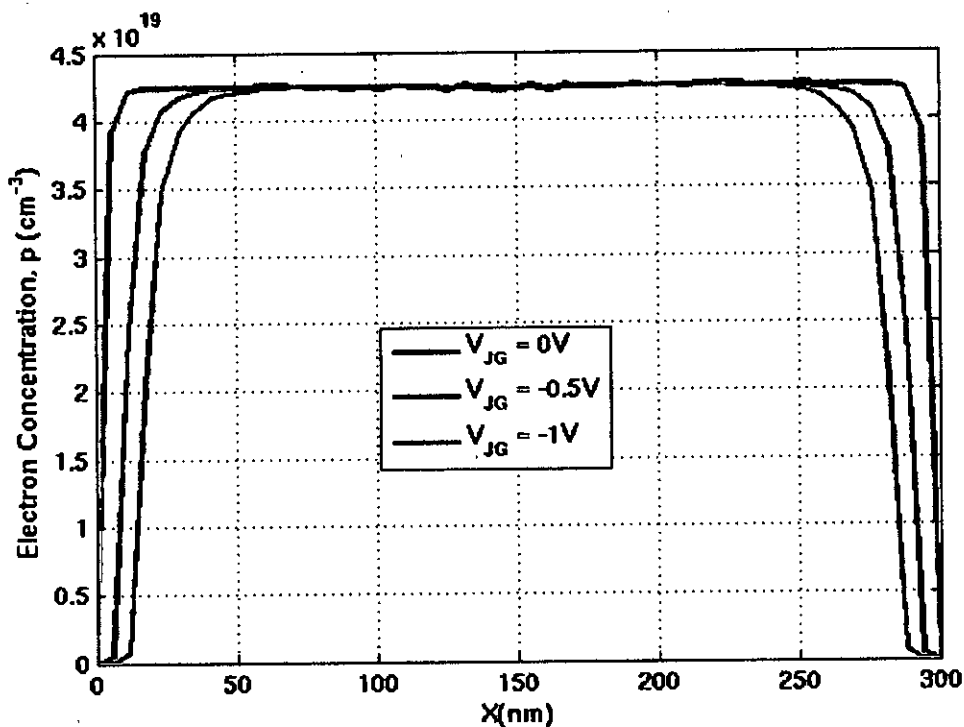


Figure 3.11: Electron concentration at front interface (plot generated at $V_{PG} = 1V$)

gates.

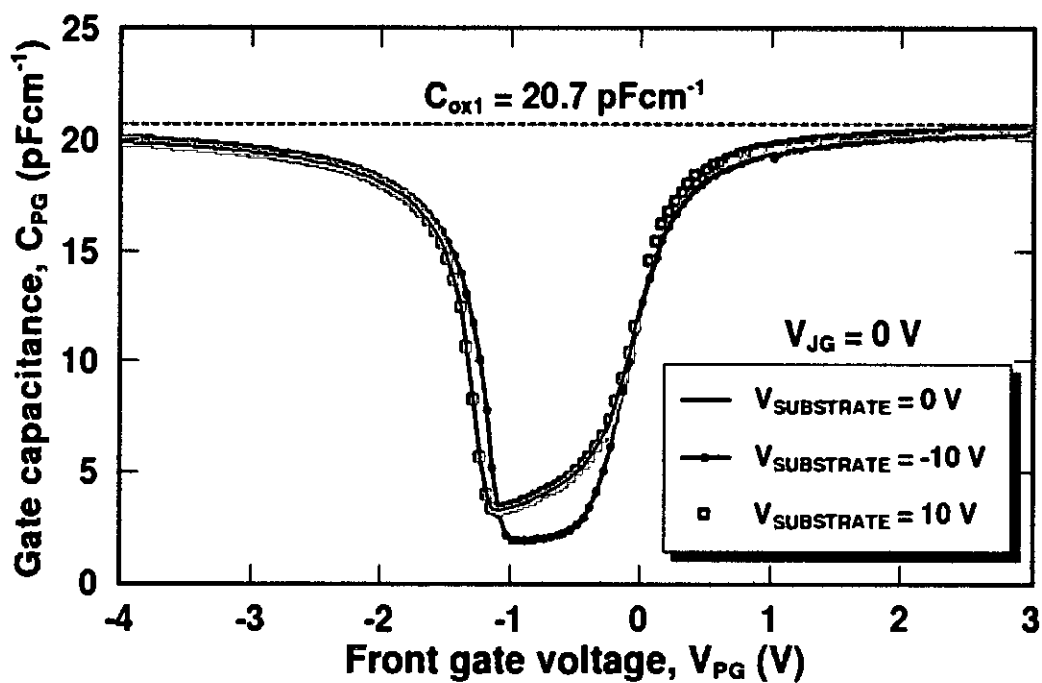
3.3 Effect of Back Gate bias

C-V plots at different junction gate bias using back gate bias as parameters are shown in Figure 3.12 (a), (b) and (c).

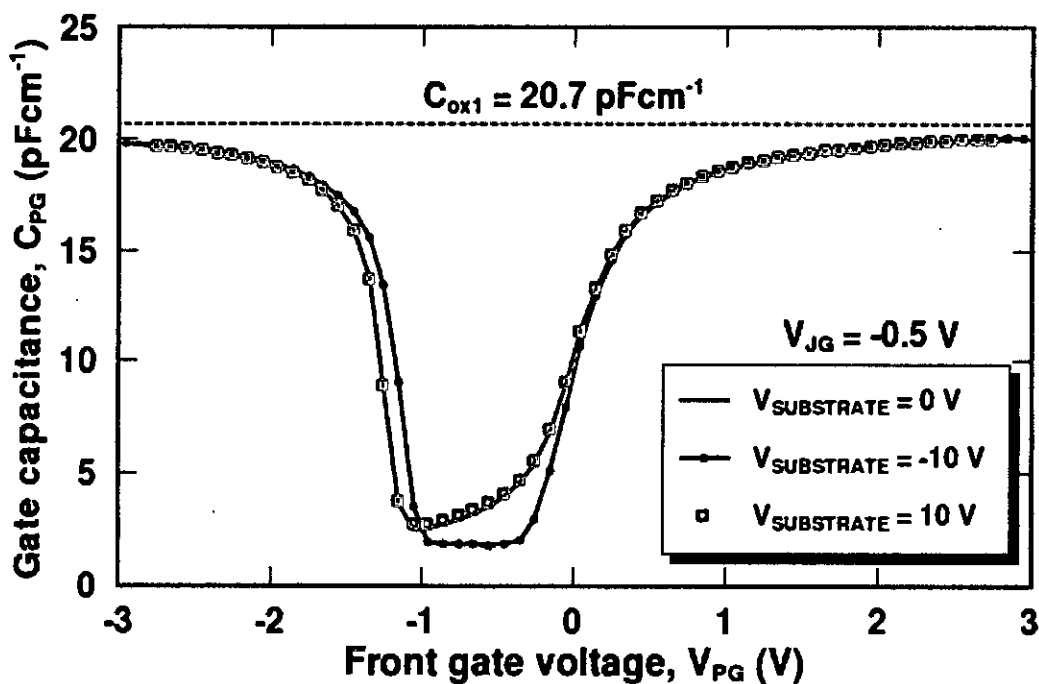
3.3.1 Observations

From the plots, it is clearly observed that, back gate accumulation ($V_{SUBSTRATE}=10V$) does not have any effect on the capacitance in any one of the 3 regions of operation. In all of the three cases, where junction gates are at 0V, -0.5 V or -1V, the C-V curves with back gate at 0 bias and accumulation exactly coincide. This is because, although there is an accumulation channel at the back interface, front gate, whether at depletion, inversion or accumulation, the differential change in charge for a differential change in voltage occurs away from the back interface.

The C-V characteristics is significantly affected when the back interface is at inversion ($V_{SUBSTRATE}=-10V$), irrespective of junction gate voltage. Although during front inversion

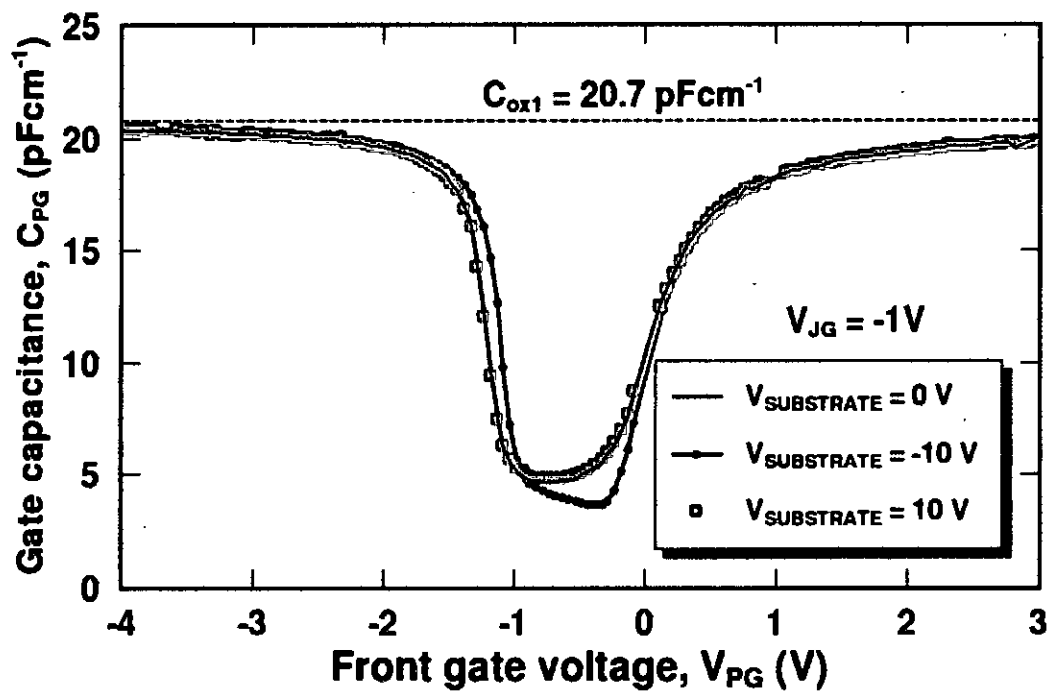


(a) Effect of back gate bias with junction gate at 0V



(b) Effect of back gate bias with junction gate at -0.5V

Figure 3.12: Effect of back gate bias with various junction gate voltages



(c) Effect of junction gate bias with back gate at +10V

Figure 3.12: Effect of back gate bias with various junction gate voltages (contd)

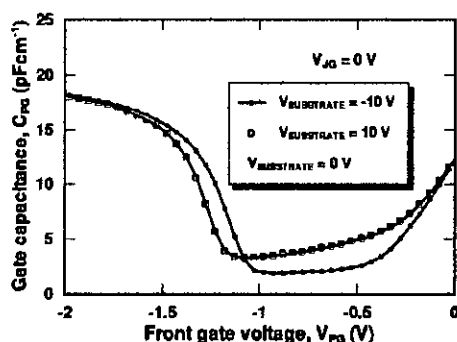


Figure 3.13: Capacitance in depletion region with varying back gate bias

and accumulation, the characteristics are similar, during depletion, for a voltage range of nearly 0.8 V, the capacitance is smaller than that with $V_{\text{SUBSTRATE}}$ at 0V or 10V. While at depletion, change in front gate voltage causes change in the back interface inversion layer charge which is far from the front gate. Because of this distance, we will experience a reduction in capacitance.

3.3.2 Discussions

Effects of back gate bias on the C-V characteristics will be discussed for junction gate at 0V Figure 3.12 (a). In the depletion region (Figure 3.13), capacitance is not affected by back gate accumulation. Figure 3.14 (a) and (b) show that, spatial variation in differential change in charge density is same whether back gate is at 0V(flat band) or 10V(accumulation). But as the back gate is strongly reverse biased with -10V, an inversion channel occurs at the back interface (Figure 3.15). Change in front gate voltage in depletion mode of operation causes change in charge in this channel (Figure 3.14 (c)), which is situated far from the gate. As the change occurs far from the gate, a reduction in capacitance follows. The reduced value may be approximated by assuming two capacitances connected in series, one is the front oxide capacitance and the other is the depletion area inside the silicon film.

From Figure 3.12 (a) it is clearly evident that inversion and accumulation capacitance is not affected much by change in back gate bias. This may be clarified from Figure 3.16 (a), (b) and (c) which show that, minority carrier, hole concentration in inversion mode is same for the three different bias conditions at back gate. The same is true for majority carrier, electron concentration in accumulation mode (Figure 3.17 (a), (b), (c)). Thus, we expect the same capacitance in inversion and accumulation region irrespective

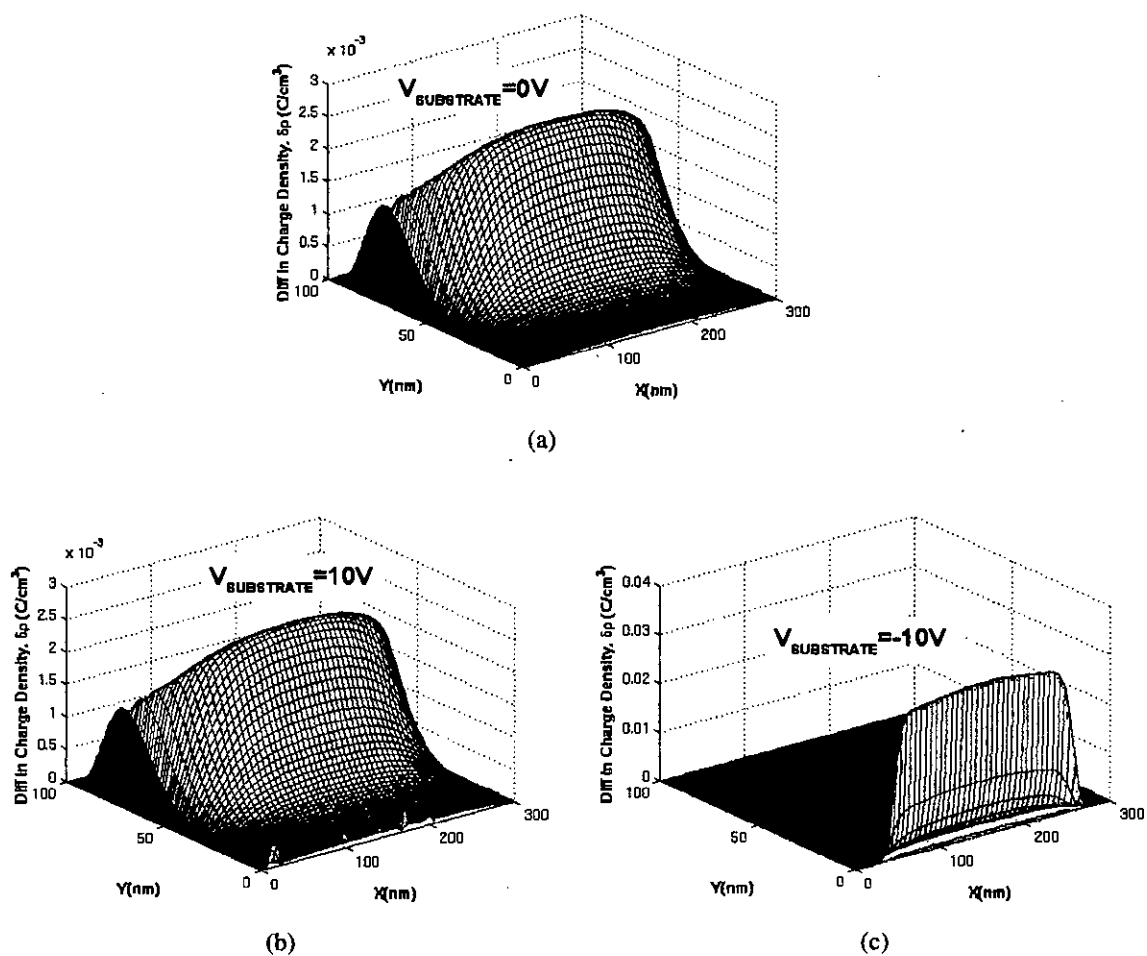


Figure 3.14: Spatial variation of differential change in charge density for a 0.05V change in V_{PG} in depletion region

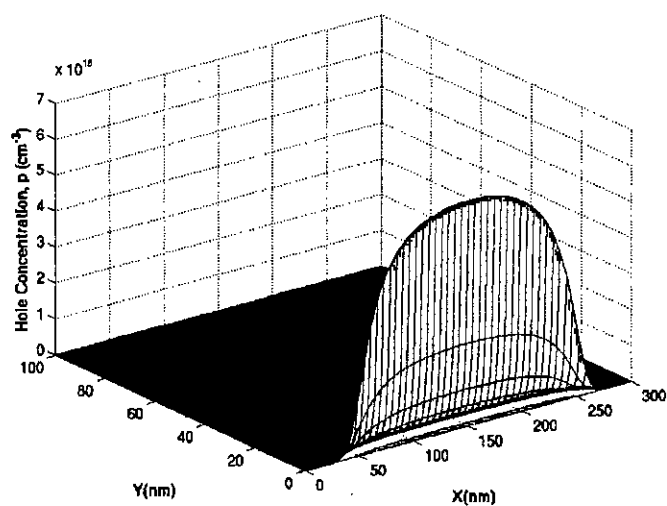
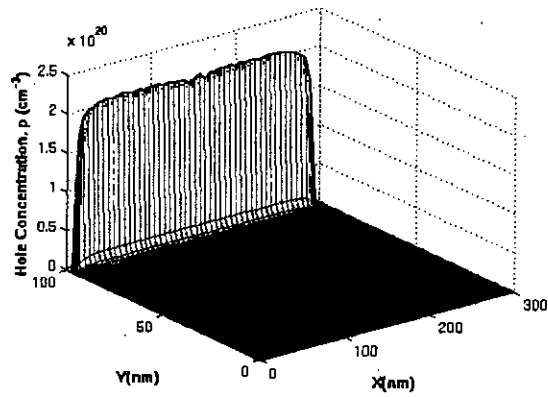
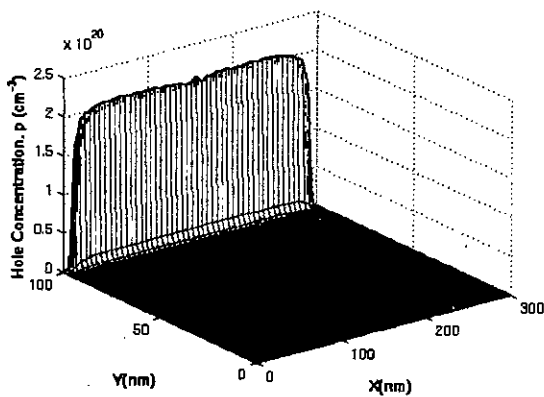


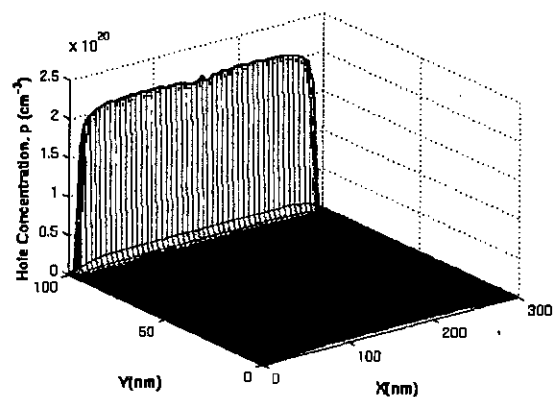
Figure 3.15: Occurrence of inversion channel with $V_{SUBSTRATE} = -10V$



(a)



(b)



(c)

Figure 3.16: Minority carrier, hole concentration at different back gate bias for $V_{JG} = 0\text{V}$ (plots generated at $V_{PG} = -3\text{V}$)

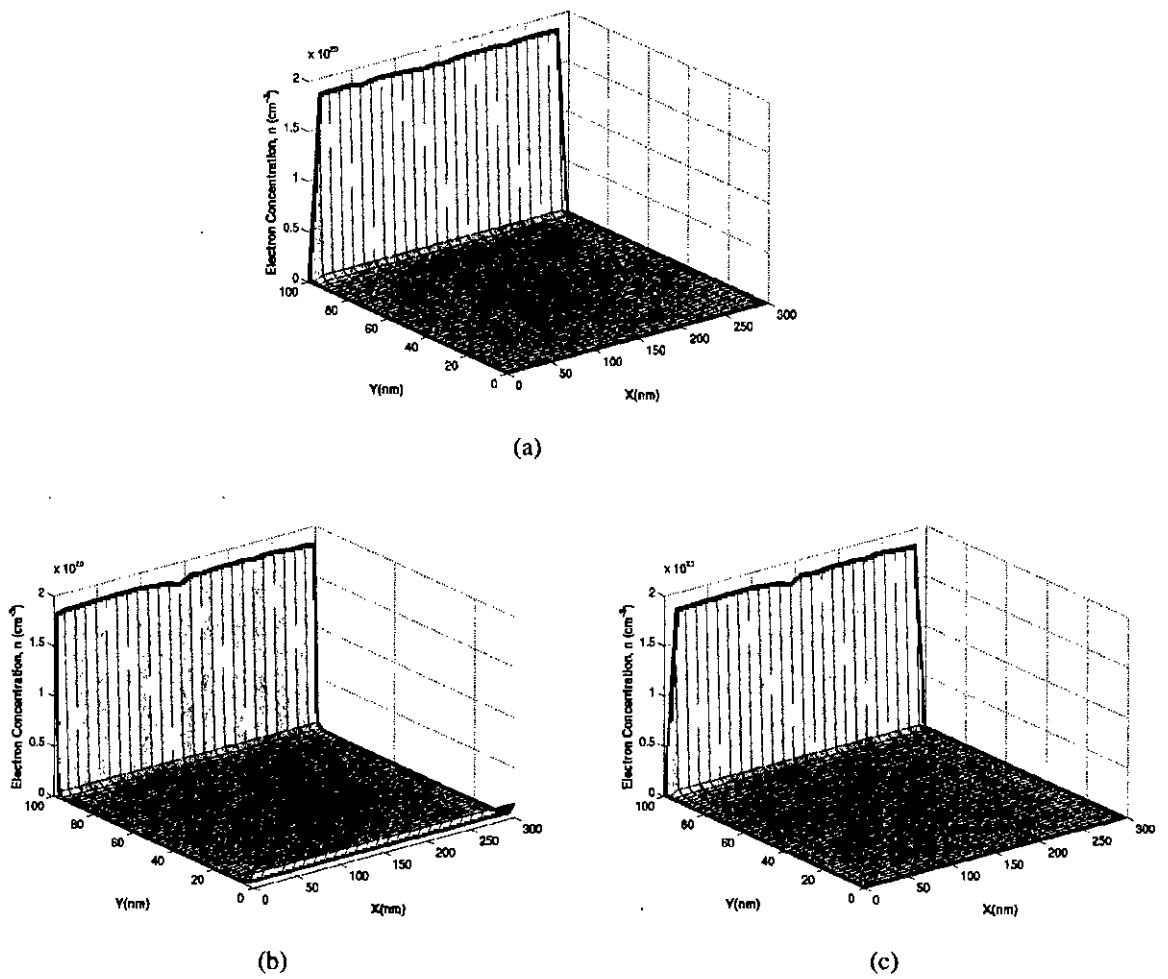


Figure 3.17: Majority carrier, electron concentration at different back gate bias for $V_{JG} = 0V$ (plots generated at $V_{PG} = 2V$)

of back gate bias. In brief, we can conclude that, variation in back gate bias will affect capacitance in depletion mode only.

Chapter 4

Conclusion

4.1 Summary

A simulator for C-V characterization in the G^4 -FET, based on semi-classical formalism is used to predict the effects of different gate bias on the front gate capacitance for the partially depleted device.

The effect of junction gate bias over floating gates was studied first. C-V characteristics for three different values of gate bias was simulated and it was found that, as some fixed bias is applied at the lateral gates, the capacitance is affected for our narrow channel device.

Effects of junction gate bias at three back gate bias was studied to conclude that junction gate reverse bias will not only shift the C-V curves irrespective of back gate voltage, but also will affect the characteristics in all of the three regions of operation. Furthermore, it will have significant impact in transition from depletion to inversion or accumulation. A reverse bias at the junction gate will retard the achievement of front interface accumulation while assisting inversion.

As back gate voltage was used as parameters to predict its effect on the C-V, it was discovered that the characteristics are not affected much in accumulation and inversion region. Even back gate accumulation does not change the C-V considerably in the depletion mode. But, as we invert the back interface with a strong reverse bias, capacitance in depletion region is severely affected with a degraded value from the back accumulation case.

4.2 Scope for future work

The G^4 -FET, quite a novel device, has so far been experimented and simulated for testing its functionality only. C-V characteristics for the partial depletion case, has been studied in this work.

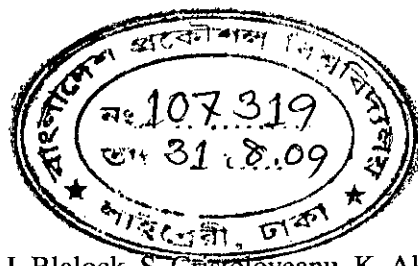
The simulator, a semi-classical one, may be further improved by incorporating the quantum mechanical i.e. wave function penetration effects and may be used to extract several device parameters like equivalent oxide thickness, threshold voltage and also for understanding electrical characteristics of the device.

A wide-channel device and a narrow-channel device will certainly produce different electrical characteristics. In the same manner, film thickness will also affect the device characteristics. Impacts of these dimensions, i.e. film thickness and width may be studied using the simulator.

Furthermore, we did not consider the effects from drain and source while simulating the C-V. Effects of drain and source voltage is another important issue to consider.

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