Study of Gate Leakage Current in Double Gate MOS Structures Incorporating Quantum Mechanical Effects

A thesis submitted to

Department of Electrical and Electronic Engineering

Bangladesh University of Engineering and Technology

in

partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

By

Sabbir Ahmed

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY

December, 2007

The thesis entitled **"Study of Gate Leakage Current in Double Gate MOS Structures Incorporating Quantum Mechanical Effects"** submitted by Sabbir Ahmed, Roll No.: 100506210P, Session: October, 2005 has been accepted as satisfactory in partial fulfillment of the requirements for the degree of 'MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING' on December 9, 2007.

BOARD OF EXAMINERS

1. _____ **Chairman**
(Dr. Quazi Deen Mohd Khosru) **(Supervisor)**
Professor
Department of Electrical and Electronic Engineering, BUET
Dhaka-1000, Bangladesh

2. _____ 9.12.07 **Member**
(Dr. Satya Prasad Majumder) **(Ex-officio)**
Professor and Head
Department of Electrical and Electronic Engineering, BUET
Dhaka-1000, Bangladesh

3. _____ **Member**
(Dr. M. M. Shahidul Hassan)
Professor
Department of Electrical and Electronic Engineering, BUET
Dhaka-1000, Bangladesh

4. _____ **Member**
(Dr. M. Ruhul Amin) **(External)**
Professor and Chairperson
Department of Applied Physics and Communication Engineering
East West University, 43 Mohakhali, Dhaka, Bangladesh

Declaration

I hereby declare that this thesis has been done by me and it or any part of it has not been submitted elsewhere for the award of any degree or diploma.

(Sabbir Ahmed)

To My Family

Acknowledgements

I would like to express my sincere gratitude to my supervisor Dr. Quazi Deen Mohd Khosru, Professor, Department of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technoogy (BUET) for his generous help, encouragement and continuous support.

I heartily thank Professor S. P. Majumder, Head of EEE department, for the simulation facilities in Robert Noyce Simulation Lab (RNSL) and EEE Department Computer Lab.

This thesis is benefited from discussions with several of my colleagues in EEE, BUET and I am in their debt. I especially appreciate Md. Kawsar Alam and Ahsan-Ul-Alam for their stimulating discussions and enthusiasm about my thesis. I also thank Professor M. M. Shahidul Hassan for simulation facilities in Robert Noyce Simulation Lab (RNSL).

Finally, I am ever grateful to my family members for their continuous support and encouragement and all others who have directly or indirectly helped me in my research.

Contents

List of Tables

List of Figures

Abstract

This thesis discuses the calculation of gate leakage current of an ultra thin body double gate (DG) MOS structure for a variety of physical parameters incorporating quantum mechanical effects. Self-consistent modeling of double gate MOS inversion layer has been performed, taking into account the effects of wave function penetration on the solutions of both Schrödinger and Poisson equations. A solver, based on Finite Element Method using FEMLAB, has been developed for the solution of both Schrödinger and Poisson equations that is much faster and efficient than conventional Schrödinger-Poisson solver. The developed numerical solver has been applied to fully depleted DG MOSFET (with different silicon and oxide thickness on both <100> and <111> silicon) for analyzing electrostatics of the device such as, inversion region charge, transmission probability, carrier lifetime and gate leakage current. The solver has the capability of analyzing both symmetric and asymmetric DGMOS structures. It has been shown in this report that the gate leakage current is greatly dependent on the thickness of the silicon and the oxide layer. Also it has been revealed that there is some variation in the gate leakage current for different crystallographic orientation of silicon surface though this variation is less significant in comparison to the effects of other parameters and the reason behind all these are discussed in detail. Finally, the simulated results have been compared with reported experimental data.

Chapter -1
INTRODUCTION

1.1 Overview of Scaling

For decades, progress in device scaling has followed an exponential curve, with the device density on a microprocessor doubling every three years. This has come to be known as Moore's law [1]. Increase in the device density is made possible by shrinking the dimensions of each transistor. Shrinking transistor dimensions has resulted in increased transistor count and operating frequencies, thus enabling tremendous technological progress such as: microprocessors with greater than 100 million transistors and memory chips with greater than 1 Giga Byte densities. The key dimension that is reduced from one transistor generation to the next is the gate length (L_G). Continued success in device scaling is necessary for maintaining the evolutionary technological advancements that have been the foundation for integrated circuit development and design this far.

A group of leading companies publish their projections for the next decade in an International Technology Roadmap for Semiconductors (ITRS-06) [2]. This roadmap projects a device gate-length of ~9 nm for the year 2016 [2]. Scaling devices to these dimensions is much more difficult and different compared to existing scaling methodologies. This is because, metal-oxide-semicondcutor (MOS) technology is approaching its limits at these dimensions. The most important issue to be addressed is how further can aggressive device scaling be continued? Although very difficult to answer, it is clear that new and revolutionary technologies will be needed to replace conventional MOS transistors as the driver behind electronic products in the future. Development of nanoscale transistors at the limit poses numerous practical and theoretical challenges that need to be surmounted if device scaling is to continue. Device simulation requires new modeling techniques that helps improve the understanding of device physics and design, for devices at the scaling limit.

1.2 Device Scaling

There are two primary device structures that have been widely studied and used in CMOS (complementary MOS) technology. The first is the bulk structure, where a transistor is directly fabricated on the semiconductor substrate and the second, is called SOI (silicon-on-insulator), where a transistor is built on a thin silicon layer which is separated from the substrate by a layer of insulator. The bulk structure is relatively simple from fabrication point of view and is still the standard structure in almost all CMOS based products.

Device scaling requires a balance between device functionality and device reliability. Both of these have to be maintained as one scales channel lengths to smaller sizes. To accomplish this, short channel effects (SCEs) have to be suppressed as much as possible. SCEs include threshold voltage (V_{TH}) variations versus channel length and drain induced barrier lowering (DIBL). Threshold voltage rolloff due to SCEs, results in a degraded subthreshold swing (S), which in turn renders it difficult to turn off a device, while DIBL results in a drain voltage dependent V_{TH}, which complicates CMOS design at a circuit level. As critical transistor dimensions are scaled, reliability concerns become more pronounced. Unwanted leakage currents due to gate tunneling and junction tunneling rapidly increase, resulting in high off-state power dissipation.

In these respect, partially and fully depleted single-gate SOI MOSFET structures have been investigated as candidates for device scaling below ~25nm because they offer improved electrical isolation between the substrate and the active device region. However, since these MOSFETs (single-gate) have a thick buried oxide which cannot terminate the electric field lines from the drain end, they exhibit severe SCE [3] [4].

Although the semiconductor industry is still working hard to push the scaling further using conventional single gate MOS, new structures inevitably come into the horizon as the semiconductor industry and technology itself needs to gain new force to go further ahead. Double gate MOSFETs are one of these novel devices. DGMOSFETs are becoming intense subject of VLSI design as CMOS scaling is approaching its

limit due to processing as well as fundamental considerations. Compared to SOI MOSFET, DGMOSFET has mainly two advantages. Because of the extremely good control of silicon body potential when both the top and the bottom gate voltages are applied, significant improvement of short-channel threshold roll-off has been predicted for DG devices [5]. It is estimated that the silicon body thickness of DG MOSFET can be two times thicker than that of SOI MOSFET for the same channel length, which will partially reduce the quantum-confinement effect [6]. Secondly, it was found that the carriers are not just confined at the top and bottom silicon interface of a DGMOSFET with sufficiently thin silicon body. Because of the coupling between the two gates, the carrier is induced not just at the interface. This in particular provides with enhanced transconductance performances, since inverted carriers within the volume of the silicon undergoes less scattering than those at the silicon surface [7].

1.3 Modeling of Double- Gate (DG) MOSFET

Double gate MOSFETs are becoming intense subject of VLSI design as CMOS scaling is approaching its limit due to processing as well as fundamental considerations. Among the advantages of double-gate MOSFETs are: significant reduction of Short Channel Effects (SCE) as observed in single-gate SOI geometry, near-ideal subthreshold swing of 60 mv/decade, high transconductance, good electrostatic integrity which minimizes drain-induced barrier lowering and threshold variation with channel length [8], [9], [10], [11].

As the gate length goes below deep submicron dimensions, the device design, as guided by scaling rules, can result in large nominal electric fields at the Si/SiO_2 interface, even near the threshold of inversion. This leads to a significant bending of the energy band at the Si/SiO_2 interface. It has long been known that with sufficient band bending, the potential well can become sufficiently narrow to quantize the motion of inversion layer carriers in the direction perpendicular to the interface [12]. This gives rise a splitting of the energy levels into subbands (2-dimnsional density-of-states), such that, the lowest of the allowed energy levels for electrons in the well does not coincide with the bottom of the conduction band. Due to quantization, the electron

density does not reach its maximum at the oxide-semiconductor interface as in the semi-classical profile [13] [14], instead some distance inside the semiconductor. Fig 1.1 shows a typical conduction band profile for a double gate n-MOSFET device and Fig 1.2 shows the electron density in silicon near Si/SiO_2 interface as obtained from Quantum Mechanical (QM) calculations.

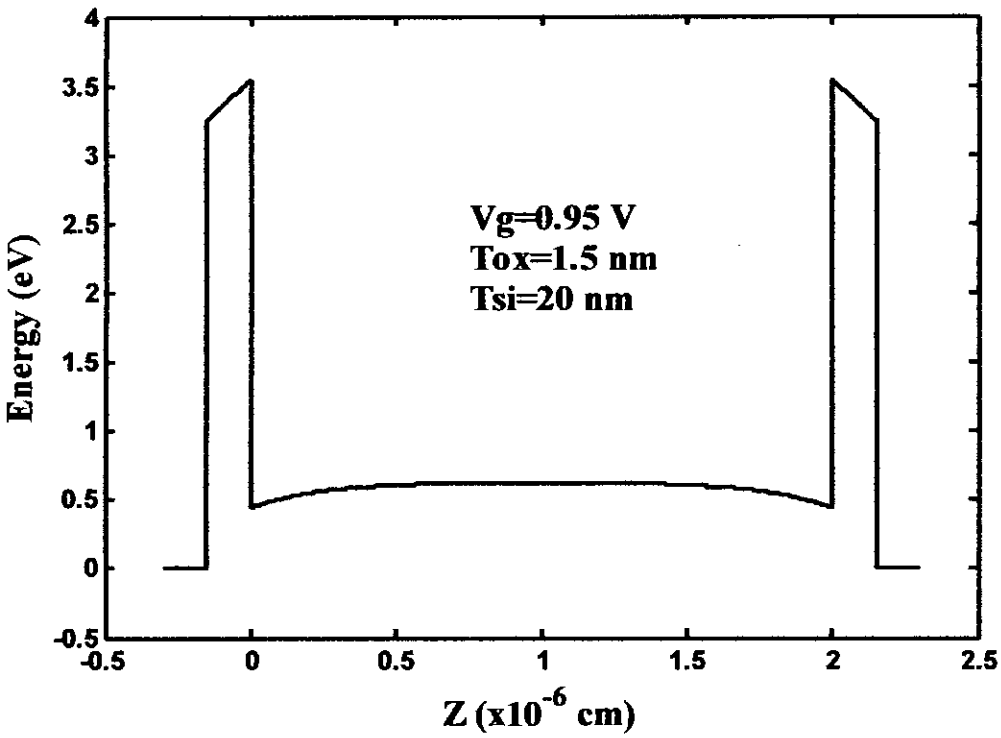

Fig 1.1. A typical conduction band profile of a double gate n-MOSFET

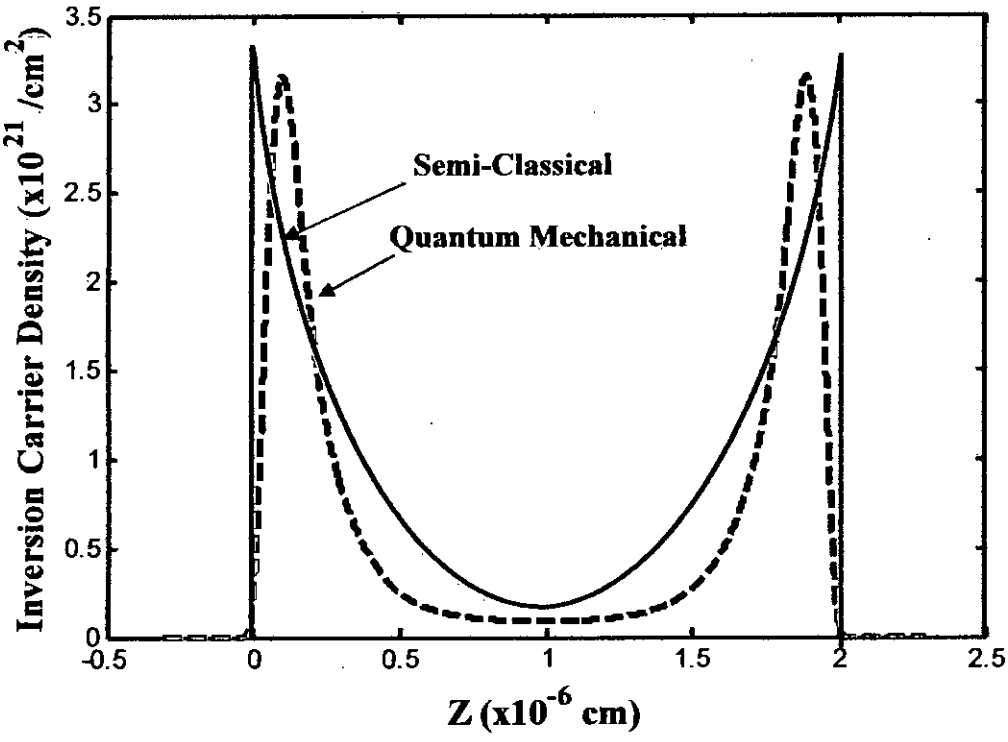

Fig 1.2. Semi-classical and Quantum Mechanical inversion carrier density profile in silicon near Si/SiO_2 interface

Due to this extension of the electron density inside semiconductor, (i) the electric potential value at the interface is greater and (ii) the capacitance and the transconductance are reduced from those predicted by the semi-classical model. Thus, it is important that the above mentioned inversion layer QM effects are incorporated in deep submicron device models. The use of traditional or semi-classical technique in device analysis and design, in which these effects are neglected, is inadequate at deep submicron dimensions and will lead to erroneous and misleading prediction of device structure and electrical behavior. These include physical oxide thickness, threshold voltage, drive current, gate capacitance and electrostatic potential. For this reason, the two-dimensional nature of electrons needs to be considered in the inversion layer.

As devices are scaled down, the thickness of the oxide layer has continued to be decreased. With the decreasing thickness of the oxide layer, the tunneling current

increases in a nearly exponential manner. Also, since charges can move from source to drain by tunneling through the channel, the off-current value and the subthreshold swing may be dramatically degraded [15]. As a consequence of ultra-thin gate oxide requirements, electrons can tunnel to the gate, creating the gate-leakage current that is considered as one of the most severe challenge to take up for scaled complementary metal oxide-semiconductor (CMOS) generations, especially regarding the power consumption [15]. Thus, predicting the tunneling current at high as well as at low bias levels is important for the development of advanced MOS devices. So, the effect of the gate leakage current is studied extensively for a variety of MOS structures.

1.3 Literature Review

The first publication describing a double-gate SOI MOSFET dates back to 1984. The device received the acronym XMOS because of the resemblance of the structure with the Greek letter Ξ [16]. This initial paper predicted good short-channel characteristics of such a device. The first fabricated double-gate SOI MOSFET was the "fully Depleted Lean-channel Transistor (DELTA, 1989)", where the silicon film stands vertical on its side (Fig 1.3) [17]. Later vertical-channel, double-gate SOI MOSFETs (FinFET) [18] was implemented. Volume inversion was discovered in 1987 [19], and the superior transconductance brought about by this phenomenon were first experimentally observed in 1990 in the first practical implementation of a planar double-gate MOSFET called the "gate-all-around" (GAA) device [19] (Fig 1.4).

The structure that theoretically offers the best possible control of the channel region by the gate is the surrounding-gate MOSFET. Such a device is usually fabricated using a pillar-like silicon island with a vertical-channel which include the cylindrical thin-pillar transistor (CYNTHIA) (Fig 1.5) [20] and the pillar surrounding-gate MOSFET [21].

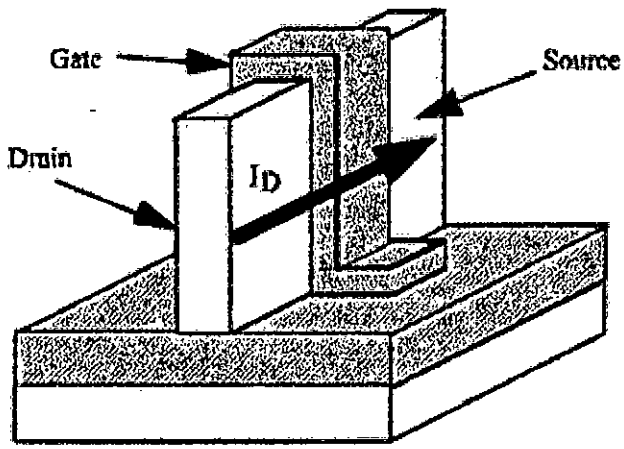

Fig 1.3. Delta/FinFET structure

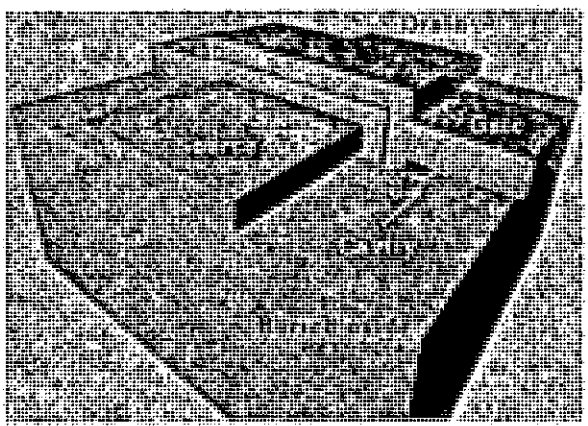

Fig 1.4. Gate-all-around (GAA) MOSFET

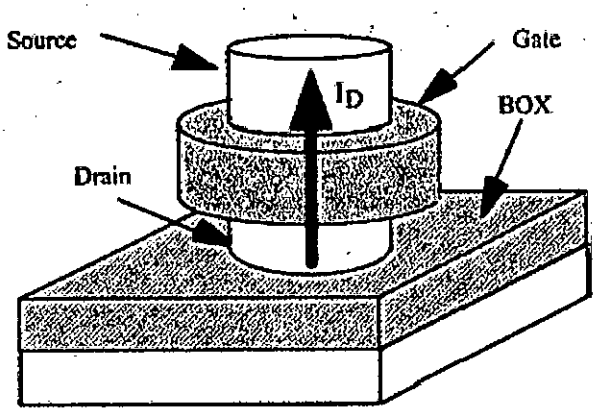

Fig 1.5. CYNTHIA / surrounding-gate MOSFET structure

The effects of volume inversion in thin-film short-channel SOI MOSFETs and the efficacy of dual-gate operation in enhancing their device performance have been analyzed by R. F. Pierret *et al.* [22] using two-dimensional device simulations and one dimensional analytical computations. Their analyses have been restricted to the strong inversion regime, which is the practically useful region of operation of SOI MOSFETs. In this region, they suggested that when compared at constant $V_g - V_t$ values, the dual channel volume inverted devices do not offer significant current-enhancement advantages, other than that expected from the second channel, over the conventional single-channel devices for silicon thickness in the 0.1 μm range.

K. Suzuki *et al.* [23] established a scaling theory for double-gate SOI MOSFETs, which gives guidance for the device design. They calculated dependence of subthreshold slope S on device parameters. According to their theory, a device can be designed with a gate length of less than 0.1 μm while maintaining the ideal subthreshold factor, which is verified numerically with a two-dimensional device simulator. In a latest publication [24], they developed models for short channel n^+-p^+ double-gate SOI MOSFETs by solving a two-dimensional (2-D) Poisson's equation in the channel region, and showed how to design a device with a decreased gate length, suppressing short channel threshold voltage shift ΔV_{th} and subthreshold swing (S-swing) degradation.

G. Baccarani *et al.* [25] presented a compact model for the Double-Gate MOSFET (DG-MOSFET), which accounts for quantum mechanical effects, including motion quantization normal to the Si-SiO_2 interface, band splitting into subbands and non-static effects in the transport model. The model holds both in subthreshold and strong inversion, and ensures a smooth transition between the two regions.

J. M. Hergenrother *et al.* [26] showed that short-channel effects in fully-depleted double gate (DG) and cylindrical, surrounding-gate (Cyl) MOSFETs are governed by the electrostatic potential as confined by the gates, and thus by the device dimensions. For equivalent silicon and gate oxide thicknesses, evanescent-mode analysis indicates that Cyl-MOSFETs can be scaled to 35% shorter channel lengths than DG-MOSFETs.

S.-L. Jang *et* at. [27] have developed an analytical drain current model for symmetric double-gate SOI MOSFETs using a quasi-two-dimensional Poisson's equation. The model applicable for digital/analog circuit simulation contains the description of the subthreshold, near threshold and above-threshold regions of operation by one single expression. They considered effects of the source/drain resistance; on important short channel effects such as- velocity saturation, drain induced barrier lowering, channel length modulation, self-heating effect due to the low thermal conductivity of the buried oxide, impact-ionization of MOS devices, parasitic bipolar junction transistor associated with drain breakdown, etc.

B. Majkusiak *et* at. [28] have analyzed the influence of the semiconductor film thickness in the double-gate silicon-on-insulator (SOI) MOSFET on the electron concentration distribution, electron charge density, threshold voltage, electron effective mobility, and drain current. The consideration of the semiconductor region is based on two descriptions: the "classical" model based on a solution to the Poisson's equation and the "quantum" model based on a self-consistent solution to the Schrödinger's and Poisson's equation system. The electron effective mobility and the drain current are calculated with the use of the local mobility model.

Y. Taur [29] has derived a one-dimensional (I-D) analytical solution for an undoped (or lightly-doped) double-gate MOSFET by incorporating only the mobile charge term in Poisson's equation. The solution gives closed forms of band bending and volume inversion as a function of silicon thickness and gate voltage. A threshold criterion has been derived which serves to quantify the gate work function requirements for a double gate CMOS. Then in [30] the solution is applied to both symmetric and asymmetric DG MOSFETs to obtain closed forms of band bending and inversion charge as a function of gate voltage and silicon thickness. It is shown that for the symmetric DG device, "volume inversion" only occurs under subthreshold conditions, with a slightly negative impact on performance. Comparisons under the same off-state conditions show that the on-state inversion charge density of an asymmetric DG with one channel is only slightly less than that of a symmetric DG with two channels, if the silicon film is thin. From the analytic solutions, expressions for the various components of the equivalent capacitance circuit have been derived for symmetric and asymmetric DG devices.

J. O. Fossum *et al.* [31] have developed a compact physics-based quantum-effects model for symmetrical double-gate (DG) MOSFETs of arbitrary Si-film thickness. The model, based on the quantum-mechanical variational approach, not only accounts for the thin Si-film thickness dependence but also takes into account the gate-gate charge coupling and the electric field dependence; it can be used for FD/SOI MOSFETs as well. The analytical solutions, verified via results obtained from self-consistent numerical solutions of the Poisson and Schrödinger equations, provide good physical insight regarding quantization and volume inversion due to carrier confinement, which is governed by the Si-film thickness and/or the transverse electric field. A design criterion for achieving beneficial volume-inversion operation in DG devices has quantitatively defined for the first time. Further, the utility of the model for aiding optimal DG device design, including exploitation of the volume-inversion benefit to carrier mobility, is exemplified.

J. D. Meindl *et al.* [32] have developed an analytical subthreshold swing (S) model for symmetric DG MOSFETs using evanescent-mode analysis. Through a concept of effective conducting path, it explains a doping concentration (NA) dependence of S, providing a unified understanding of previous models and leading to a new model for undoped DG MOSFETs. Expressions of a scale length have been derived, which expedite projections of scalability of DG MOSFETs and its requirement.

T. Ernst *et al.* [33] have analyzed the operation of 1-3 nm thick SOI MOSFETs, in double-gate (DG) mode and single-gate (SG) mode (for either front or back channel). They found some typical effects in these ultra-thin MOSFETs such as- threshold voltage variation, large influence of substrate depletion underneath the buried oxide, absence of drain current transients, and degradation in electron mobility. By comparing SG and DG configurations they have shown the superiority of DG-MOSFETs: ideal subthreshold swing and remarkably improved transconductance (consistently higher than twice the value in SG-MOSFETs). The experimental data and the difference between SG and DG modes have been explained by combining classical models with quantum calculations. They found that the key effect in ultimately thin DG-MOSFETs is volume inversion, which primarily leads to an improvement in mobility, whereas the total inversion charge is only marginally modified.

M. Wong *et al.* [34] have derived an analytical expression relating the potential and the electric field at the oxide-semiconductor interface of a symmetrical double-gate oxide intrinsic semiconductor-oxide system. The expression is applicable to all regimes of operation. The "turn-on" behavior of the system has been studied and an extrapolated threshold voltage has been defined. Opposite to the behavior of a conventional bulk metal-oxide-semiconductor capacitor realized on a doped substrate, this threshold voltage was shown to decrease with increasing oxide thickness.

M. Alessandrini *et at.* [35] have developed an analytical model for the electron mobility limited by surface optical phonons and applied to the simulation of ultra-thin SOI MOSFETs. The developed model reproduces the main features of experimental data recently reported in the literature and has been implemented in a conventional device simulator. An application to the analysis of technological options such as doping concentration and silicon thickness in SOI MOSFETs, have been reported.

M. J. Kumar *et at.* [36] have discussed how the short channel behavior in sub 100 nm channel range can be improved by inducing a step surface potential profile at the back gate of an asymmetrical double gate (DG) silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect-transistor (MOSFET) in which the front gate consists of two materials with different work functions.

1.4 Objective of the Work

This work is concerned with the study of Gate Leakage Current of Double Gate n-MOS structure, taking into account the effect of wave function penetration on the solutions of both Schrödinger's and Poisson's equations. Thus, penetration effects are included in the self-consistent loop. To make the procedure numerically efficient, Schrödinger's equation is solved using open boundary conditions allowing for wave function penetration [37]. Finite element method using FEMLAB is used to compute the solutions of both the equations. Finite element method is a technique to solve linear and nonlinear partial differential equations (PDEs) using discretisation of the whole problem. This system is very efficient and requires a very low amount of computational time.

Thus, the objective of this work is to develop a one dimensional (1D) self-consistent Schrödinger-Poisson solver using appropriate boundary condition to incorporate wave function penetration effects with established accuracy and efficiency. The developed numerical solver will be applied for the calculation of Gate Leakage Current of fully depleted DG MOSFET structures with different body and oxide thickness for both <100> and <111> orientations of silicon. Very little work has so far been done to analyze the effect of Gate Leakage current on the physical parameters of Double gate MOS. So, the results will be presented and compared with data that are available.

1.5 Organization of the Thesis

Chapter 2 is devoted to the theoretical study of and Double Gate MOS. Why a DG MOSFET is better in comparison to a Single gate MOSFET is also presented in this chapter.

Chapter 3 is centered on the thorough discussion on the Finite Element Method and FEMLAB. This chapter also gives a description of the Schrödinger-Poisson self-consistent solver that incorporates the effect of wavefunction penetration. Using the results, the potential profile, eigen energies, normalized wavefunction, carrier concentration at different eigen energies and the inversion region charge density can be examined. In the concluding part of this chapter, an efficient and fast technique for the determination of Gate Leakage current is presented.

Chapter 4 covers the results and discussions. In this chapter, results obtained for Double Gate MOS structures with different body and oxide thickness and orientation of silicon surface are reported and analyzed.

Chapter 5 summarizes the conclusions of this research and lists a few potential directions for future work.

Chapter -2

DOUBLE GATE MOSFET

2.1 Basic Concepts of DGMOS

Double-gate metal–oxide–semiconductor field-effect-transistors (DGMOSFETs) are currently considered a serious alternative to standard-bulk MOSFETs to increase the integration capacity of silicon technology in the near future. A dual-gate-silicon-on-insulator DGSOI Structure consists, basically, of a silicon slab sandwiched between two oxide layers (Fig. 2.1). A metal or a polysilicon film contacts each oxide. These films act as front and back gate, which can generate an inversion region near the Si–SiO2 interfaces, if an appropriate bias is applied. Thus we would have two MOSFETs sharing the substrate, source, and drain.

The salient features of the DG MOSFET [38] (Fig. 2.1) are control of short-channel effects by device geometry, as compared to bulk FET, where the short-channel effects are controlled by doping (channel doping and/or halo doping); and a thin silicon channel leading to tight coupling of the gate potential with the channel potential.

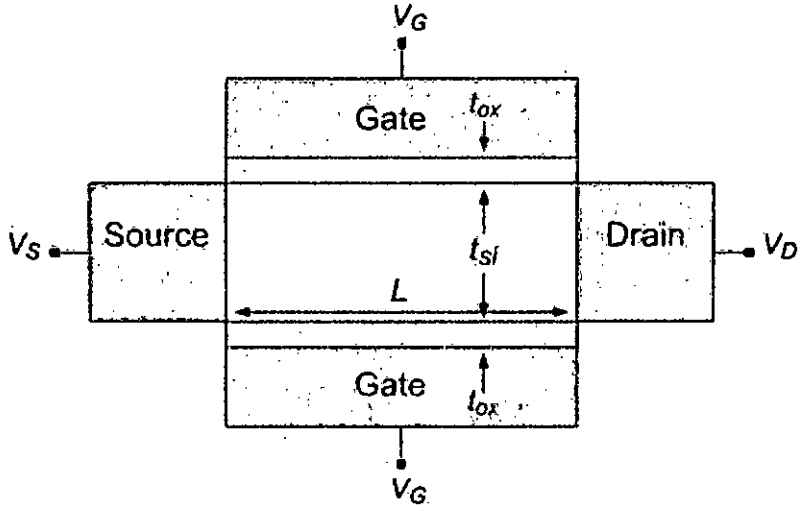

Fig 2.1. Double gate MOSFET

These features provide potential DG FET advantages that include 1) reduced 2D short channel effects leading to a shorter allowable channel length compared to bulk FET; 2) a sharper subthreshold slope (60 mV/dec compared to > 80 mV/dec for bulk FET) which allows for a larger gate overdrive for the same power supply and the same off-current; and 3) better carrier transport as the channel doping is reduced (in principle, the channel can be undoped). Reduction of channel doping also relieves a key scaling limitation due to the drain-to-body band-to-band tunneling leakage current. A further potential advantage is more current drive (or gate capacitance) per device area; however, this density improvement depends critically on the specific fabrication methods employed and is not intrinsic to the device structure.

The most common mode of operation of the DG FET is to switch the two gates simultaneously. Another use of the two gates is to switch only one gate and apply a bias to the second gate to dynamically alter the threshold voltage of the FET [39]. In this mode of operation, called "ground plane" (GP) or back gate (BG), the subthreshold slope is determined by the ratio of the switching gate capacitance and the series combination of the channel capacitance and the non-switching gate capacitance, and is generally worse than the DG FET. A thin gate dielectric at the non-switching gate reduces the voltage required to adjust the threshold voltage and preserves the drain-field-shielding advantage of the double-gate device structure. However, a thinner gate dielectric also means extra capacitance that does not contribute to channel charge for switching. Since the back-gate FET is very similar to a single-gated SOI FET with an adjustable threshold voltage [39].

DG-MOSFETs are claimed to be more immune to short channel effects (SCE) than bulk silicon MOSFETs and even more than single gate fully depleted SOI MOSFETs. This is due to the fact that the two gate electrodes jointly control the carriers, thus screening the drain field from the channel. This latter feature would permit a much greater scaling down of these devices than ever imagined in conventional MOSFETs.

2.2 Advantages of DG MOSFET over SG MOSFET

2.2.1 Limitation of Scaled SG MOSFET

- **Effect of Reducing Channel Length : Drain Induced Barrier Lowering (DIBL)**

In devices with long channel lengths, the gate is completely responsible for depleting the semiconductor. In very short channel devices, part of the depletion is accomplished by the drain and source bias. Since less gate voltage is required to deplete the semiconductor, the barrier for electron injection from source to drain decreases. This is known as drain induced barrier lowering (DIBL).

DIBL results in an increase in drain current at a given gate voltage, V_G. Therefore V_t decreases as channel length decreases. Similarly, as drain voltage V_D increases more semiconductor region is depleted by the drain bias, and hence I_d increases and V_t decreases.

- **Carrier Mobility : Velocity Saturation**

The mobility of the carrier reduces at higher electric fields normally encountered in small channel length devices due to velocity saturation effects. As the channel length, L is reduced while the supply voltage is not, the tangential electric field will increase, and the carrier velocity may saturate at $E_C \approx 10^4$ V/cm for electrons. Hence for n-MOSFET with $L < 1$ μm, velocity saturation causes the channel current to reach saturation before $V_D=V_G-V_t$. $E_C \approx 5 \times 10^4$ V/cm for holes, hence velocity saturation for p-MOSFET will not become important until $L < 0.25$ μm.

- **Sub-threshold Conduction**

When the surface is in weak inversion ($V_G < Vt$), a conduction channel starts to form a low level of current flow between source and drain. As a result, drain leakage current and static power loss increases. Hence circuit stability decreases.

- **Hot Carrier Effect**

Hot carrier effects are among the main concerns when shrinking FET dimensions into the deep sub-micron regime. Reducing the channel length while retaining high power supply levels, known as constant voltage scaling, results in increased electric field strengths in the channel, causing acceleration and heating of the charge carriers. The free carriers passing through the high-field can gain sufficient energy to cause several hot-carrier effects. This can cause many serious problems for the device operation. Some of the manifestations of hot electrons on device operation are breakdown and substrate current caused by impact ionization, creation of interface states, gate current resulting from hot-electron emission across the interface barrier, oxide charges owing to tunneling of charge carriers into oxide states and photocurrents caused by electron-hole recombination with emission of photons. The substrate current resulting from electron-hole pair generation may overload substrate-bias generators, introduce snapback breakdown, cause CMOS latch-up and generate a significant increase in the sub-threshold drain current.

2.2.2 Short Channel Effects

Collectively, threshold voltage roll-off and subthreshold roll-up are commonly known as short-channel effects (SCEs). In consequence of SCEs, the ratio of the drive (ON) current to the leakage (OFF) current is substantially reduced, which imposes severe tradeoffs between circuit speed and standby power. In addition, SCEs amplify the impact of process variations on CMOS circuits.

In conventional bulk MOSFETs, SCEs are caused by the lateral electric fields from the source to channel and drain to channel. As L decreases, the lateral fields terminate on further into the channel, which essentially steals the charge that would normally be terminated by the gate voltage in a long-channel device. This stealing of charge by the lateral fields effectively lowers the source-to-channel barrier, which controls the conduction of electrons from source to drain. To limit this charge stealing and thus mitigate SCEs, heavy channel doping is exploited in bulk MOSFETs. As the gate length is scaled to 50 nm and below, the required channel doping concentration is expected to be on the order of 10^{18} cm^{-3} and above. These extremely high doping levels, however lead to,

a) Severe degradation of the carrier mobility as the impurity scattering becomes dominant [40].
b) Severe threshold voltage variations due to random microscopic fluctuations of the dopant atoms [41].

The DG MOSFET does not require channel doping for SCE control. Instead, this novel device uses a second gate and a fully depleted silicon film as the channel to enhance the electrostatic control of the gates over the channel, which effectively suppresses the impact of the source/drain. The thin silicon film is undoped or lightly doped (typical doping concentration $N_A < 10^{18}$ cm^{-3}) to ensure the full depletion condition. For most effective SCE control, the two gate-oxide layers are equally thin. Use of an identical material for both gates results in a symmetric DG MOSFET.

2.2.3 Concept of Volume Inversion

The outstanding feature of these structures lies in the concept of volume inversion, introduced by Balestra *et al* [42]; if the Si film is thicker than the sum of the depletion regions induced by the two gates, no interaction is produced between the two inversion layers, and the operation of this device is similar to the operation of two conventional MOSFETs connected in parallel. However, if the Si thickness is reduced, the whole silicon film is depleted and an important interaction appears

between the two potential wells. In such conditions the inversion layer is formed not only at the top and bottom of the silicon slab i.e., near the two silicon–oxide interfaces, but throughout the entire silicon film thickness. It is then said that the device operates in "**volume inversion**," i.e., carriers are no longer confined at one interface, but distributed throughout the entire silicon volume.

It has been reported [22, 29] that volume inversion presents some significant advantages, such as

i. Enhancement of the number of minority carriers.
ii. Increase in carrier mobility and velocity due to reduced influence of scattering associated with oxide and interface charges and surface roughness.
iii. As a consequence of the latter, an increase in drain current and transconductance.
iv. Decrease of low frequency noise.
v. A great reduction in hot-carrier effects.

Chapter -3

SELF CONSISTENT SOLUTION

This chapter is devoted to the 1D simulation of double gate MOS structure. At first we study the self consistent system. We also study how FEMLAB, which is a powerful tool, is used to solve Schrödinger's and Poisson's equations. Finally, the equations that are used for the calculation of direct tunneling gate leakage current are presented.

3.1 Self - Consistent Analysis

This self - consistent solution of coupled Schrödinger's and Poisson's equations is the most significant part of the study of a double gate MOS. These two equations and how they are solved using FEMLAB is presented in this section.

3.1.1 Schrödinger Equation

The Schrödinger equation is solved within the effective mass approximation. Within this approximation, Schrödinger's equation for a wave function ψ_{0ij} can be written as,

$$-[\frac{1}{2}\hbar^2\nabla m^{*-1}\nabla + qV(z)]\psi_{0ij} = \mathrm{E}'_{ij}\psi_{0ij}\ , \tag{3.1}$$

where, m^{*-1} represents the effective mass tensor, $V(z)$ the electrostatic potential, q the magnitude of the electron charge and E'_{ij} is the energy. z is reckoned positive into the semiconductor. Following [12], the electronic wavefunction ψ_{0ij} for the j th subband in the i th valley can be expressed in terms of Bloch waves traveling parallel to the interface, constrained by an envelope function normal to it, thus:

$$\psi_{0ij}(x,y,z) = \psi_{ij}(z)\mathrm{e}^{\mathrm{i}\theta_z}\mathrm{e}^{ik_x x + ik_y y}\ , \tag{3.2}$$

here, k_x and k_y represent the transverse components of the wave vector k of the electron measured relative to the band edge. θ depends on k_x and k_y. Envelope function $\psi_{ij}(z)$ is the solution of,

$$[-\frac{\hbar^2}{2m_{zi}}\frac{d^2}{dz^2}+qV(z)]\ \psi_{ij}(z)=\mathrm{E}_{ij}\psi_{ij}(z)\ , \tag{3.3}$$

where, m_{zi} is the effective mass perpendicular to the interface and E_{ij} is the eigenenergies of the jth subband in the ith valley in the same direction. Each eigenvalue E_{ij} found from the solution of Eq. (3.3) is the bottom of a continuum of levels called a subband, with energy levels given by the relationship,

$$\mathrm{E}'_{ij}=\mathrm{E}_{ij}+\frac{\hbar^2k_x^2}{2m_x}+\frac{\hbar^2k_y^2}{2m_y}\ , \tag{3.4}$$

here, m_x and m_y are the principle effective masses for motion parallel to the surface. There can be as many as three values of m_z depending on the surface orientation because the conduction band of silicon has six ellipsoidal valleys along the [100] direction of the Brillouin zone. In the effective mass approximation, the valleys are degenerate in pairs. Thus, solution of Eq. (3.3) gives the eigenenergy E_{ij} and the envelope function $\psi_{ij}(z)$.

Within the effective mass approximation, the 3D Schrödinger's equation in a MOS inversion layer may be decoupled into a 1D equation that describes the envelope function in the direction normal to the interface. In order to include the effect of wave function penetration, an open boundary condition is required to be applied at the silicon – oxide interface of the two gates that should take into account the quasi – bound nature of the inversion layer states [43].

3.1.2 Poisson's Equation

The Poisson's equation that is used to find the potential profile V(z) can be written as,

$$\frac{d^2V(z)}{dz^2} = -\frac{\left[\rho_{depl}(z) - q\sum_{ij} N_{ij}\left|\psi_{ij}(z)\right|^2\right]}{\varepsilon_{si}\varepsilon_0}, \tag{3.5}$$

where, ε_{si} is the dielectric constant of the semiconductor, N_{ij} is the carrier concentration in the j th subband in the i th valley.

$\rho_{depl}(z)$ is the charge density in the depletion layer, which can be defined as,

$$\begin{aligned} \rho_{depl}(z) &= -q(N_A - N_D), && 0 < z < T_{si} \\ &= 0, && z \le 0 \text{ and } z \ge T_{si} \end{aligned} \tag{3.6}$$

here, T_{si} is the silicon body thickness, hole concentration and N_D, N_A are the ionized donor, acceptor concentration respectively. Since, the body thickness is less than 50 nm, the MOS structure can be considered to be fully depleted.

Since a fraction of inversion charge resides within the gate oxide due to wave function penetration, Poisson's equation should be solved for both the oxide and semiconductor regions. Considering wave function penetration, Poisson's equation can be represented as,

$$\begin{aligned} \frac{d^2V(z)}{dz^2} &= -\frac{\rho_{inv}(z)}{\varepsilon_0\varepsilon_{ox}}, && -T_{ox} < z < 0 \text{ and } T_{si} < z < (T_{si} + T_{ox}) \\ &= -\frac{[\rho_{depl}(z) + \rho_{inv}(z)]}{\varepsilon_0\varepsilon_{si}}, && 0 < z < T_{si} \end{aligned} \tag{3.7}$$

where,

$$\rho_{inv}(z) = -q\sum_{ij} N_{ij}\left|\psi_{ij}(z)\right|^2, \tag{3.8}$$

and $\rho_{depl}(z)$ is defined by Eq. (3.7). When $|\psi_{ij}(z)|^2$ is used to define $\rho_{inv}(z)$ in Eq. (3.9), effects of shift of inversion charges on the solution of Poisson's equation are also included.

The boundary conditions required to solve Eq. (3.7) are that, value of dV/dz at the gate metal – oxide interface ($z = -T_{ox}$ and $z = T_{si} + T_{ox}$) should be $-F_{ox}$, where

$$F_{ox} = \frac{q(N_{inv} + N_{depl})}{\varepsilon_0 \varepsilon_{ox}}, \tag{3.9}$$

here,

$$N_{inv} = \sum_{ij} N_{ij} \quad \text{and}$$

$$N_{depl} = z_d (N_A - N_D), \tag{3.10}$$

where, N_{inv} and N_{depl} are the total inversion carrier concentration and depletion carrier concentration respectively.

Equation (3.10) assumes that the wave function tail in the gate oxide region has decayed to an insignificant value at $z = -T_{ox}$ and $z = T_{si} + T_{ox}$. Another relationship necessary to relate oxide field F_{ox} to silicon field F_{si} is that at $z = 0$ and at $z = T_{si}$, $\varepsilon_{ox} F_{ox} = \varepsilon_{si} F_{si}$.

3.2 Self Consistent Solution using FEMLAB

With the advancement of semiconductor technology, device dimensions are entering into the nanoscale regime; quantum mechanical effects are playing a growing role in device operations and performance. So, semi-classical models are no longer valid and quantum mechanical modeling is inevitable. Although the quantum corrections improve the classical data, these approaches are unable to model or predict all

quantum mechanical effects. As described in the previous section, in a fully quantum mechanical model the coupled Schrödinger's and Poisson's equations are solved self consistently. The Schrödinger's equation is solved under the effective mass approximation. The boundary condition for solving the Schrödinger's and Poisson's equations is also a critical issue. To calculate quantum mechanical charge distribution in MOS devices incorporating wave function penetration effects within the oxide layer of MOS devices, an open boundary condition is a must for the solution of Schrödinger's equation [43]. In the absence of suitable boundary conditions, zero penetration of wave function into gate oxide is assumed in the simulation of even deep submicron MOSFETs. While an open boundary condition can be neglected in devices with thick oxide layers, its negligence in deep submicron MOSFETs cannot be justified.

In this section, the solution procedure is portrayed for a dual gate n-MOS structure shown in Fig. 2.1 in the inversion region. FEMLAB with MATLAB has been used as the Partial Differential Equation (PDE) solver (suitable for linear or nearly linear problems), for the self consistent solution.

The classical PDEs coefficient form in in multiphysics mode is used for the solution of Poisson's and Schrödinger's equation.

Poisson equation in coefficient form is given in FEMLAB as:

$$-\nabla.(c\nabla u) = f, \tag{3.11}$$

where,

c = permittivity of the sub domain, $\varepsilon_0\varepsilon$

u = Electrostatic potential, $v(z)$

f = Charge density termed as source term in FEMLAB, $q[p(z) - n(z) + N_D - N_A]$

z = the direction along the depth of the MOS structure

Using relevant parameters of MOS structures, Eq. (3.11) can be written as,

$$-\varepsilon_0\varepsilon\frac{d^2v(z)}{dz^2} = q[p(z) - n(z) + N_D - N_A], \tag{3.12}$$

where, $n(z)$, $p(z)$ are the electron and hole concentration. ε is the relative dielectric constant of the material and ε_0 is the permittivity of free space.

The electron concentration $n(z)$ is obtained for n-MOS structure according to the following expression:

$$n(z) = \sum_{ij} N_{ij} \left|\psi_{ij}(z)\right|^2 , \tag{3.13}$$

where,

$$N_{ij} = \frac{n_{vi} m_{di} kT}{\pi\hbar^2} \ln\left[1 + \exp\left(\frac{E_F - E_{ij}}{kT}\right)\right], \tag{3.14}$$

$$E_F = E_{Fbulk} + V_G . \tag{3.15}$$

In this case, N_{ij} is the carrier concentration in the j th subband of the i th valley, n_{vi} is the i th valley degeneracy and m_{di} is the density – of – states effective mass of the i th valley, given by $m_{di} = \sqrt{m_{xi} m_{yi}}$. E_F *is* the Fermi energy. E_{ij} and ψ_{ij} are the eigenvalue and the eigenfunction of an electron in the j th energy level of the i th valley, which are obtained as a solution of the one dimensional Schrödinger equation.

Schrödinger equation in coefficient form is defined in FEMLAB as:

$$-\nabla.(c\nabla u) + au = \lambda u , \tag{3.16}$$

where,

$c = \hbar^2 / 2m^*$, m^* = effective mass for the subdomain

a = Electrostatic potential, $v(z)$

λ = eigen energies, E_{ij}

u =eigenfunction, ψ_{ij} .

Using relevant parameters of effective mass Schrödinger's equation for one dimensional MOS structure quantum well Eq. (3.16) can be written as,

$$[-\frac{\hbar^2}{2m^*}\frac{d^2}{dz^2}+v(z)]\psi_{ij}(z)=E_{ij}\psi_{ij}(z). \qquad (3.17)$$

At first, the device geometry (the fully depleted double gate structure) is defined as shown in Fig. 3.1 in FEMLAB. The trial potential as presented in Fig. 3.2 is obtained by solving Eq. (3.11) using the full depletion approximation assuming zero mobile charge density i.e. $n(z)=0$ in Eq. (3.12) with appropriate boundary condition at each interface through FEMLAB linear PDE solver.

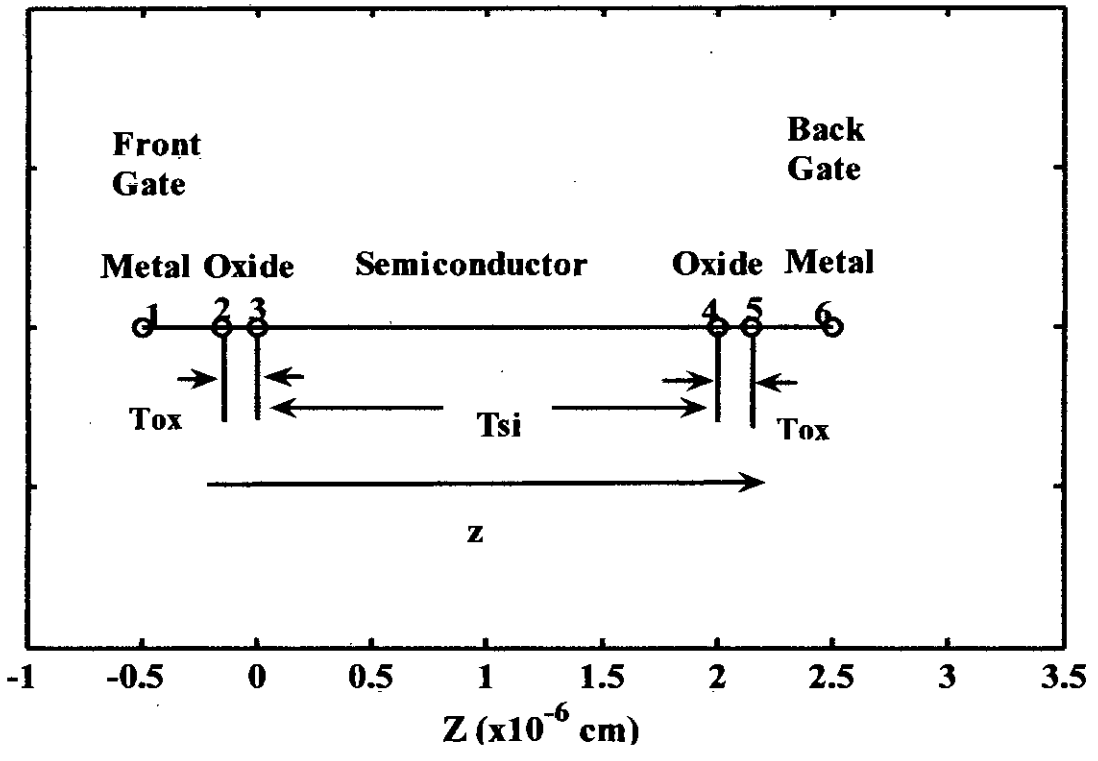

Fig 3.1. 1D geometry of Double Gate MOS structure

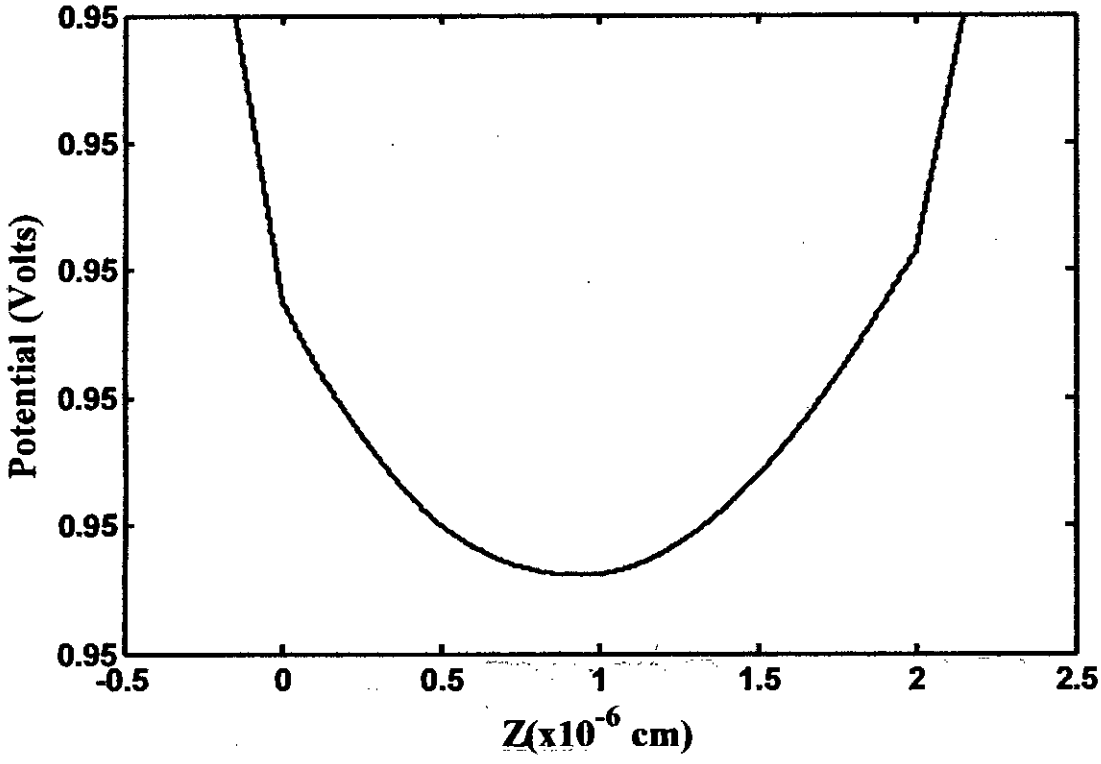

Fig 3.2. Trial Potential from full depletion approximation

For the solution of Poisson's equation, Dirichlet boundary condition (i.e. fixed value of voltage) is used at boundary points 1, 2, 5, 6 and Neumann boundary condition (i.e. continuous electric flux density,) is used at interfaces 3 and 4.

For the solution of Poisson's equation, a discontinuous electric field boundary condition is required. For achieving this condition, Neumann boundary condition (needed for open boundary condition to consider penetration effect) is applied at all the points.

The charge density profile $n(z)$ is determined from Eq. (3.13) by solving Eq. (3.16) using FEMLAB eigen value solver with Neumann boundary condition, which is shown in Fig 3.3.

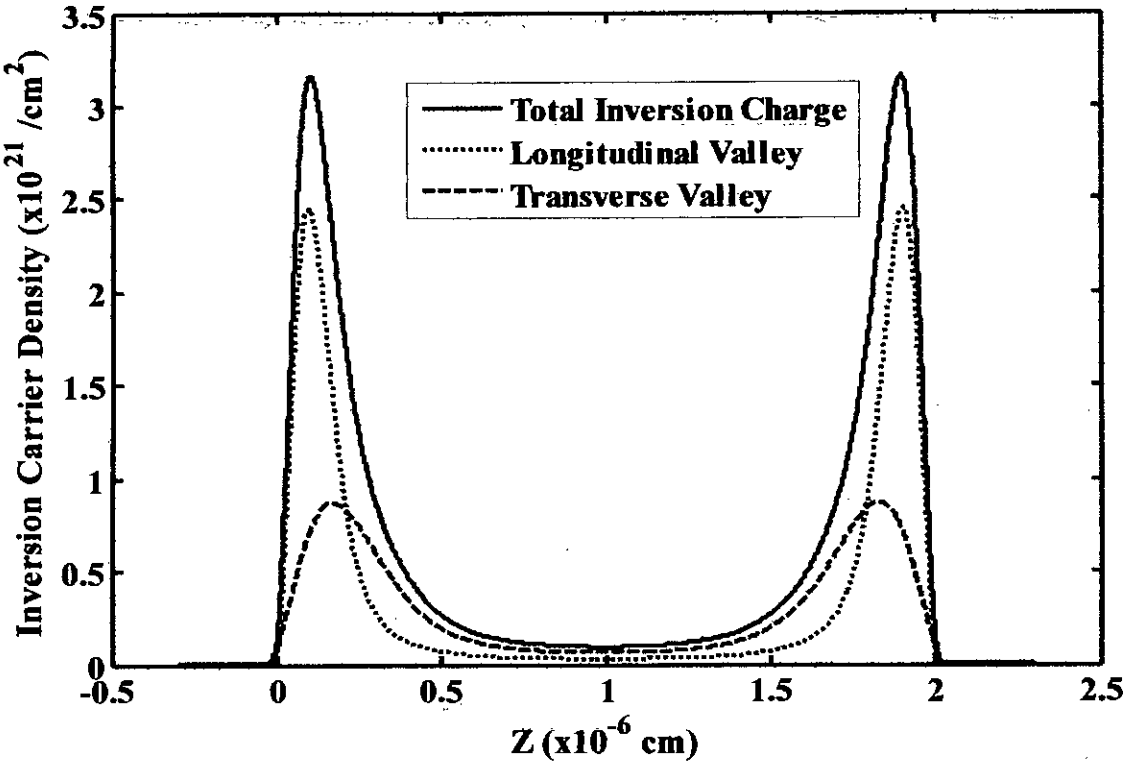

Fig 3.3. Inversion carrier density as a function of depth, z

This charge density profile is added to the source term of Poisson's equation and then Eq. (3.11) and Eq. (3.16) are solved iteratively until the given convergence criteria [for successive iteration, change in electrostatic potential at any node point is less than 10^{-7} volts] are fulfilled. Hence we get the actual band profile presented in Fig 3.4 and electrostatic potential incorporating wave function penetration as demonstrated in Fig 3.5. If the solution is to run without penetration effect, we just increase the barrier height in the oxide region to a very large value (e.g. 100 eV) that can be considered as an infinite potential barrier.

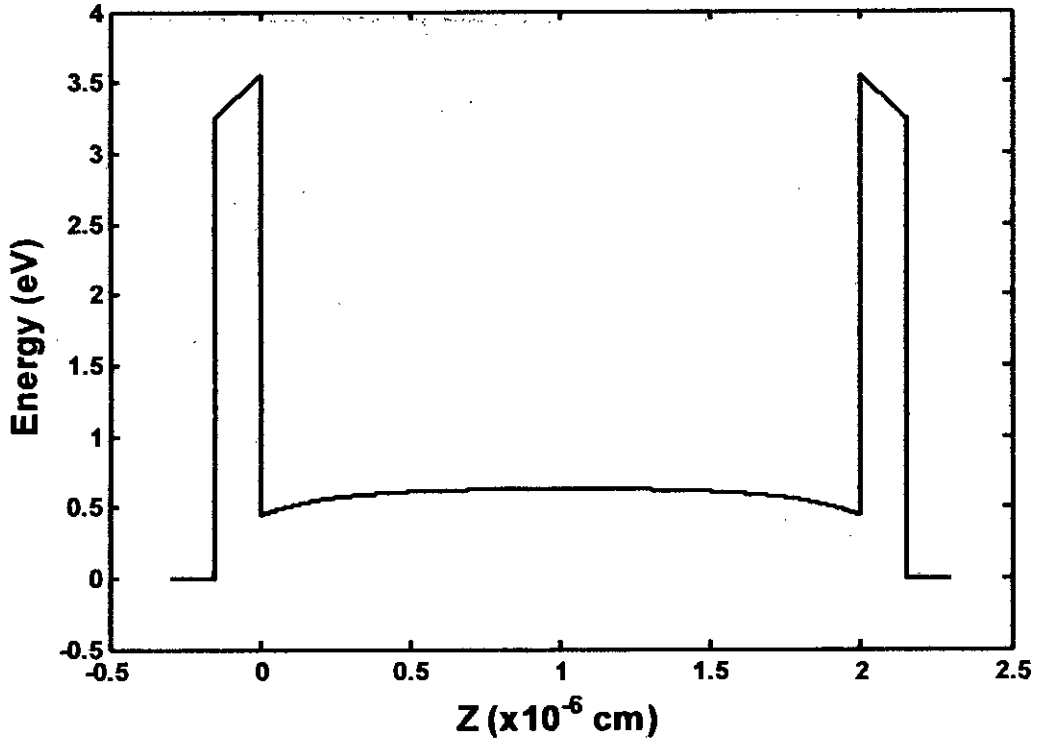

Fig 3.4. Actual Energy band diagram for the simulated structure

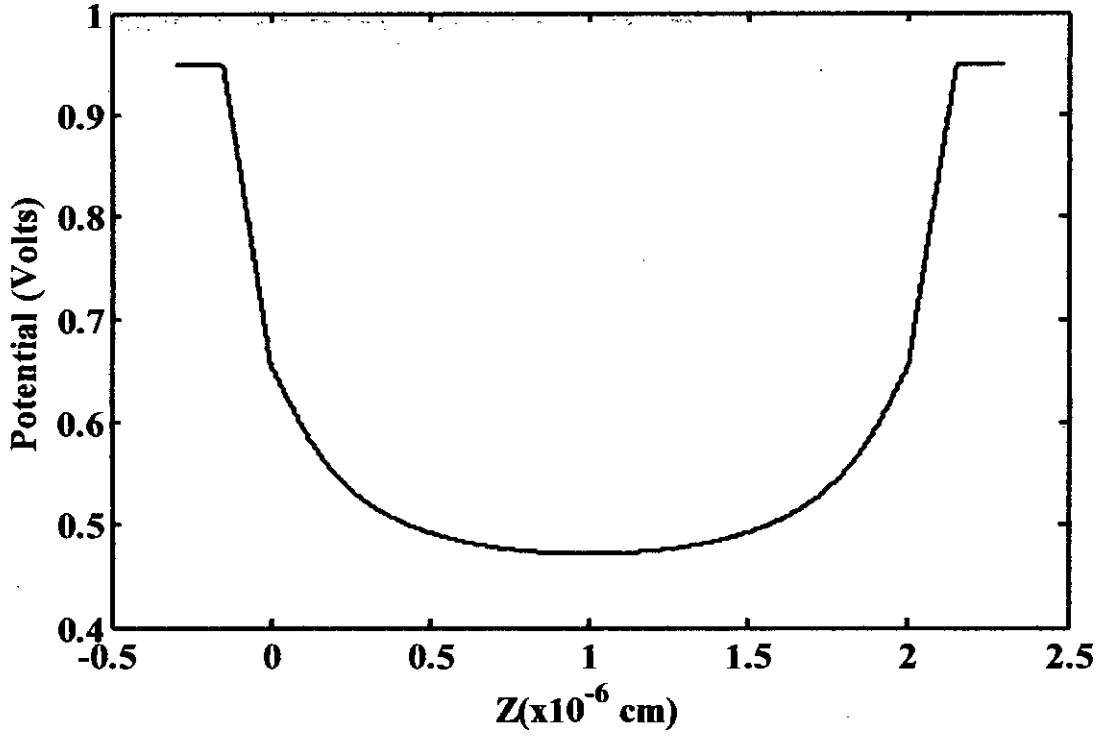

Fig 3.5. Actual Potential profile for the simulated structure

Gauss-Seidel iteration method has been used for the numerical convergence. The weighting factor should be greater than 0.9. With the increase of weighting factor the assurance of convergence increases but the simulation becomes slower and more iteration is needed. Throughout this thesis, 0.95 is used as the Gauss-Seidel update coefficient, e.g. if 'delta' is the weighting factor then the updated profile is calculated as:

$$Vprof = Vold \times delta + Vnew \times (1\text{-}delta)$$

Where, Vprof is the new interpolated profile

Vold is the previous profile

Vnew is the new calculated profile

All the simulation results presented in this chapter has been generated for,

$N_A = 5 \times 10^{17}$ /cm^3, Tox=1.5 nm, Tsi = 20 nm and $V_G - V_{FB} = 0.95$ volts.

Detail flowchart of the solution procedure is given in appendix A.

3.3 Gate Leakage Current

Direct tunneling current increases exponentially with decreasing oxide thickness and gate bias, which introduces a potential limitation for aggressive scaling of the gate oxide in advanced CMOS technology. Even though there are many reports concerning the effects of the gate leakage current on MOS transistor operation, few studies have been made regarding the impact of the gate current on circuit operation, due to lack of a circuit simulation model for gate tunneling current. The gate current effects on I-V characteristics become minimized [44] as the channel length becomes shorter due to the electric field effects near the drain. Since gate current becomes an integral part of intrinsic device operation, circuit simulation which includes accurate modeling of tunneling characteristics is required. Hence, a compact gate tunneling current model for circuit simulation is needed to analyze circuit immunity against the gate leakage current including dependencies on architecture and operating conditions. Some very

good works have been done so far on the calculation of gate leakage current MOS structures such as the done by Chang *et. al.* [49].

In order to find the gate leakage current, accurate determination of "Tunneling Lifetime" is very important. The "Tunneling Lifetime" from the j th energy subband in the i th valley may be defined as τ_{ij}/T_{ij} [44]. Here, T_{ij} is the transmission probability of electrons in the j th energy subband of the i th valley which is solved using the transmission line analogy, matching of the impedances seen by a carrier in the potential well [45] and τ_{ij} is defined as [44],

$$\tau_{ij} = \frac{j\pi\hbar}{E_{ij}}, \tag{3.18}$$

where, E_{ij} is the eigen energy of the electrons in the j th subband of the i th valley. E_{ij} is obtained from the solution of Schrödinger and Poisson's Equation.

Combining the results from the quantum mechanical calculation for the Si substrate and determining the carrier concentration in the j th subband and in the i th valley, N_{ij} from the solution of Schrödinger and Poisson's Equation, and using (3.), one can readily obtain the total Direct Tunneling Gate Leakage Current [44],

$$J = \sum_{ij} J_{ij} = q\sum_{ij} N_{ij} T_{ij}/\tau_{ij}, \tag{3.19}$$

as a function of applied gate voltage (V_G) or as a function of inversion region charge density (N_{inv}).

Fig 3.6 shows the cross-sectional view of the MOS structure that was used in this analysis.

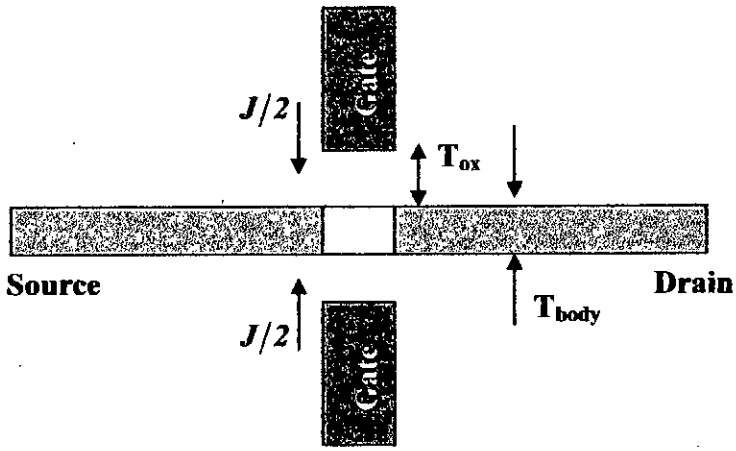

Fig 3.6. Schematic DGMOS structure used in this work

Gate Leakage current is studied for MOS structures with different body and oxide thickness and orientation of silicon surface and the results are presented in the following chapter.

Chapter -4

RESULTS AND DISCUSSION

The results of the self-consistent calculation of gate leakage current for double gate MOS devices considering the effects of wave function penetration are presented in this chapter. The self-consistent calculations for double gate n-MOS structures have been carried out for two different orientations of silicon, (100) and (111).

4.1 Effective Mass Approximation

In MOS devices, for chosen interface that lies in the (100) crystal planes, the effective mass tensor becomes diagonal in the co-ordinate system which has its z-axis perpendicular to the surface pointing into the semiconductor. It is known that silicon has six ellipsoidal constant surfaces in the conduction band. The (111) surfaces have only one ladder of subbands with degeneracy 6 in the direction normal to the interface, since all the valleys have the same orientation with respect to the surface. For the (100) oriented surfaces, m_z for electrons can take the value of the longitudinal effective mass, m_l, for the two bulk constant energy ellipsoid perpendicular to the surface giving rise to a two-fold degenerate subband ladder and the value of the transverse effective mass, m_t, for the other four ellipsoids, giving rise to a four-fold degenerate ladder. The valleys which present the higher effective mass perpendicular to the surface have the lowest kinetic energy levels. Effective mass approximation has been found to be accurate in describing the quantization effects of electrons in a MOS inversion layer [46]. The values of different parameters used in the calculation are taken from Ref. [12] and are summarized in Table 4.1.

Surface	(111)	(100)	
Valleys	All	m_l	m_t
Degeneracy, n_v	6	2	4
Normal Mass, m_z/m_0	0.258	0.916	0.190
Density of state Mass, m_d/m_0	0.358	0.190	0.417

Table 4.1. Effective masses of electrons in different valleys

4.2 n-MOS Devices on (100) silicon

Self-consistent calculations for n-MOS devices on (100) silicon are presented in this section. All the results are calculated at room temperature. The potential barrier height at the silicon-oxide interface is considered to be 3.1 eV. Electron effective mass in oxide is assumed to be $0.5m_0$ with a parabolic dispersion relationship. Effective masses inside the silicon is taken from Table-4.1 for (100) and (111) surfaces. Metal is considered as the gate electrode with a work function equal to 3.25 eV.

In this work, same amount of voltage is applied to a symmetric DG MOSFET at the two gates having the same work function. At zero gate voltage, the position of the silicon bands is largely determined by the gate work function, because as long as the thin silicon is lightly doped and the depletion charge is negligible, the bands remain essentially flat throughout the thickness of the film. Since there is no contact at the silicon body, the energy levels are referenced to the electron quasi-Fermi level or the conduction band of the n+ source-drain.

As the gate voltage increases toward the threshold voltage, mobile charge or electron density becomes appreciable when the conduction band of the silicon body approaches the conduction band of the source-drain. Fig. 4.1 shows the energy band profile as a function of depth inside the silicon for different values of gate voltage of a fully depleted symmetrical double gate MOS with doping density, $N_A = 5\times10^{17}$ cm^{-3}, silicon thickness, T_{si} of 5 nm and oxide thickness, T_{ox} of 1 nm. The figure shows that

as the gate voltage is increased, the Fermi energy, E_F of the silicon will continue to rise with respect to the Fermi energy of the metal which causes increasing positive slope inside both the silicon and the oxide region [47]. More and more minority carrier electrons will be concentrated in the vicinity of the oxide-semiconductor interface and the silicon will move from the region of weak inversion towards the region of strong inversion.

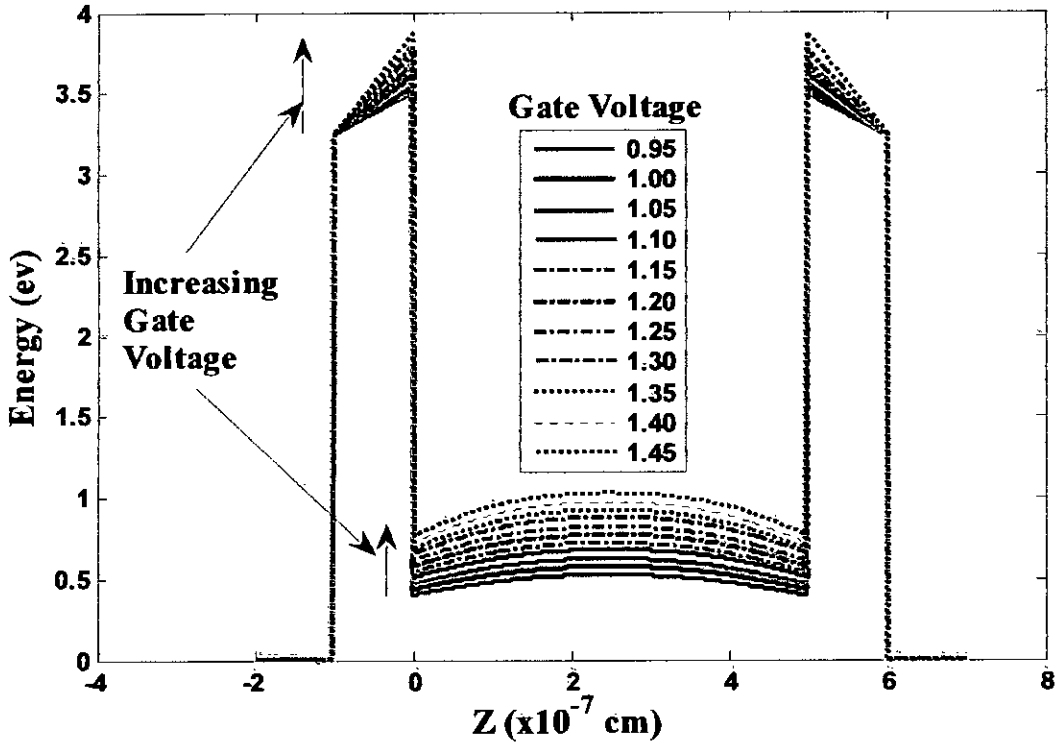

Fig 4.1. Energy Band profile of an n channel DGMOS structure on (100) surface

Fig.4.2 and Fig 4.3 shows the inversion charge density, $\rho_{inv}(z)$ as function of depth, z calculated using the self-consistent solver for the same structure as used in Fig 4.1. As expected, the charge density profile is seen to extend inside the oxide region instead of being zero at the silicon-oxide interface because of the penetration effect.

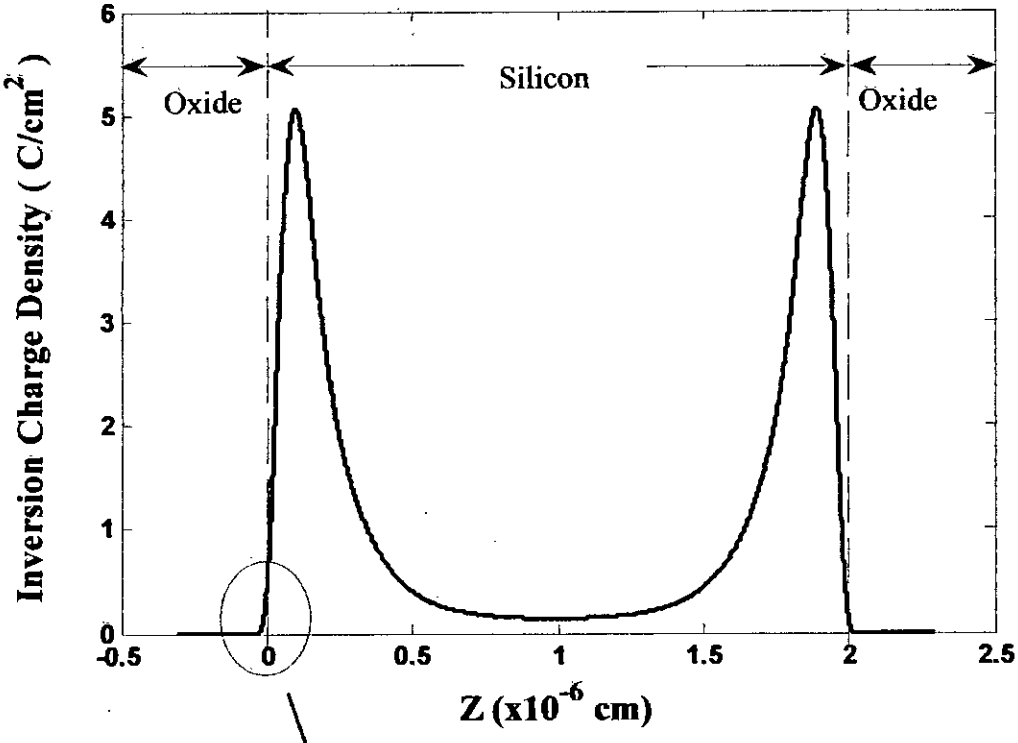

Fig 4.2. Inversion charge density as a function of depth, z

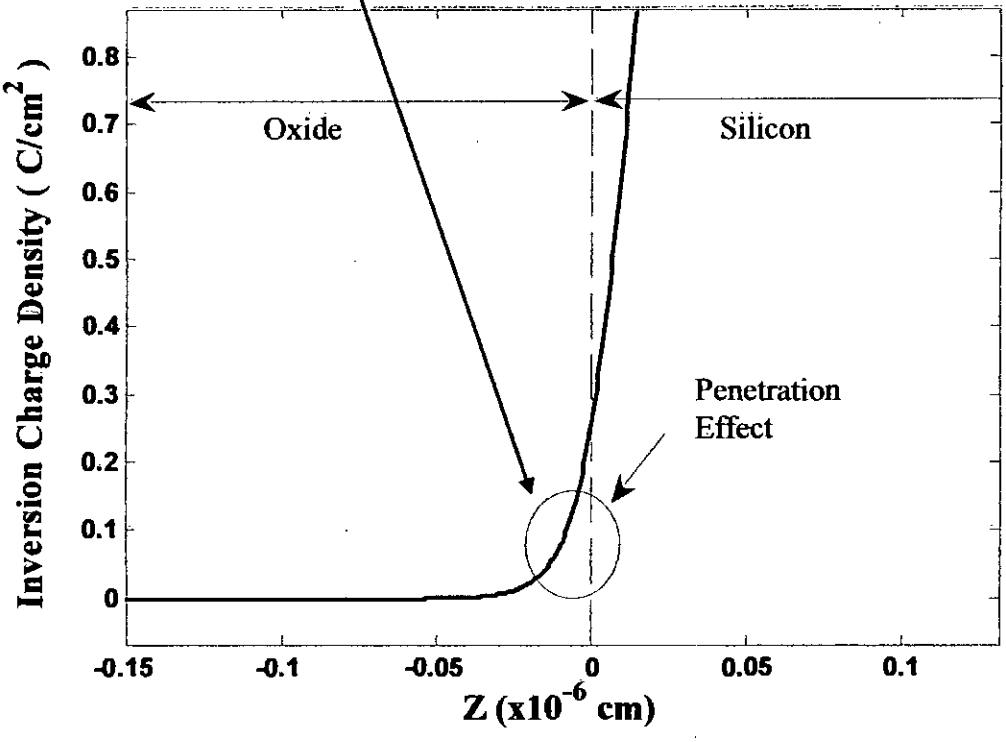

Fig 4.3. Inversion charge density as a function of depth, z

(zoomed view of the left gate)

4.3 Gate Leakage Current of n-MOS on (100) silicon

It has been reported that the gate leakage current in SOI devices is affected by the electric field distribution in the body [48]. When a large positive voltage is applied to the substrate, gate current decreases – which essentially drives the backside of the SOI into inversion and reduces the vertical electric field in the channel. Using potential profiles from the Schrödinger- Poisson solver and the transmission line analogy [44], gate leakage current for a DGMOS have been calculated in our study. Because this method considers the entire domain of the device structure, wave function penetration into the gate dielectric is allowed. The Schrödinger- Poisson solver also incorporates this penetration effect by considering a finite barrier at the silicon/oxide interface.

In double-gate MOSFETs, gate leakage is affected by the reduced vertical electric field. In particular, the electric field near the bottom of the inversion layer is dramatically reduced, as can be seen in Fig 4.1. This reduces the depth of the potential well, which lowers the bound state energy and broadens the inversion charge distribution, thus resulting in a lower tunneling probability and an increased lifetime of each quasibound state. This effectively reduces both the tunneling probability and the impingement frequency at which electrons are directed toward the silicon–dielectric interface. Depending on device dimensions, gate current in an ultrathin body MOSFET can be reduced by up to a factor of 3 when compared with that of a bulk device at a constant inversion charge density (Fig. 6 of Ref. [49]). The improvement is enhanced in the double-gate device because the inherent symmetry of the two gate electrodes further decreases the effective vertical electric field.

The effectiveness of our method has already been demonstrated by Ahmed *et al.* [50] and is in good agreement with the work of Chang *et al.* [49]. Fig 4.4 shows the gate leakage current in the inversion region of an n-MOS device with oxide thickness, T_{ox} of 1 nm and different silicon thickness, T_{si} in the range 5 ~ 25 nm with (100) crystallographic orientation as a function of inversion carrier density, N_{inv}. It reveals the impact of body thickness on the direct tunneling gate leakage current. It can be seen that, for the same oxide thickness, as the body thickness is decreased, gate leakage current increases significantly.

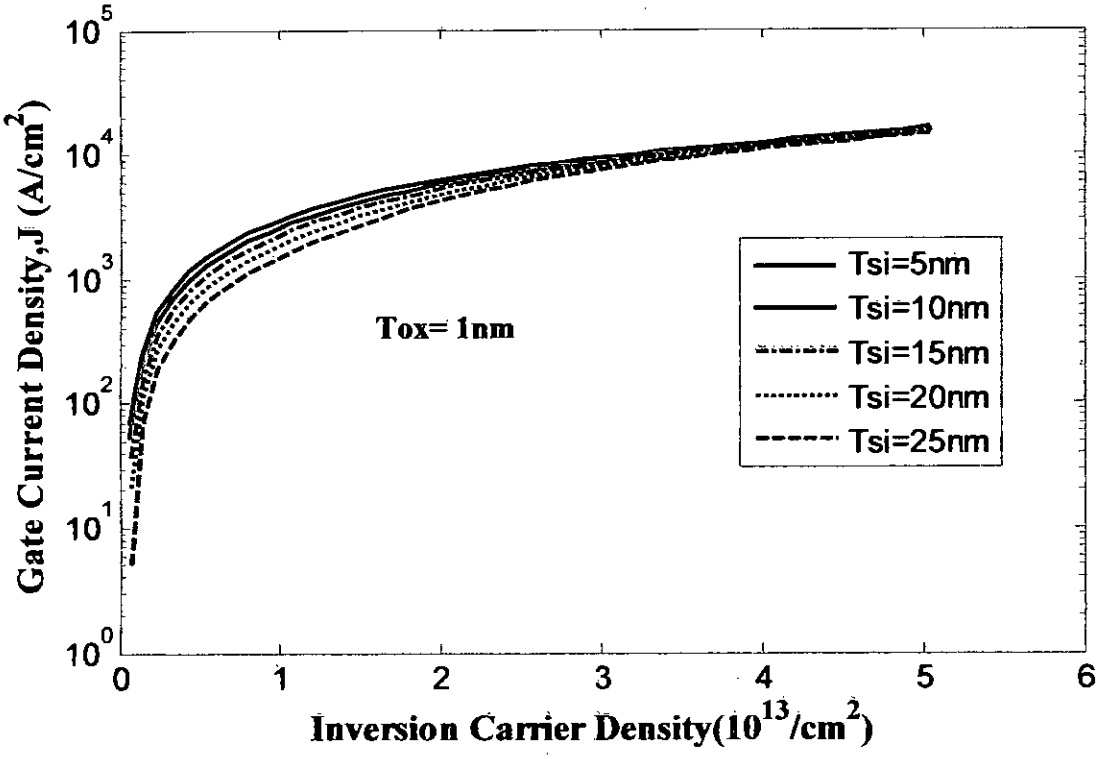

Fig 4.4. Gate Leakage current for T_{ox}=1nm as a function of inversion carrier density, N_{inv} with silicon body thickness, T_{si} as a parameter

The gate leakage currents presented in Fig 4.4 have been reproduced in Fig 4.5 as a function of gate voltage, $V_g = V_{app} - V_{FB}$ for (100) silicon.

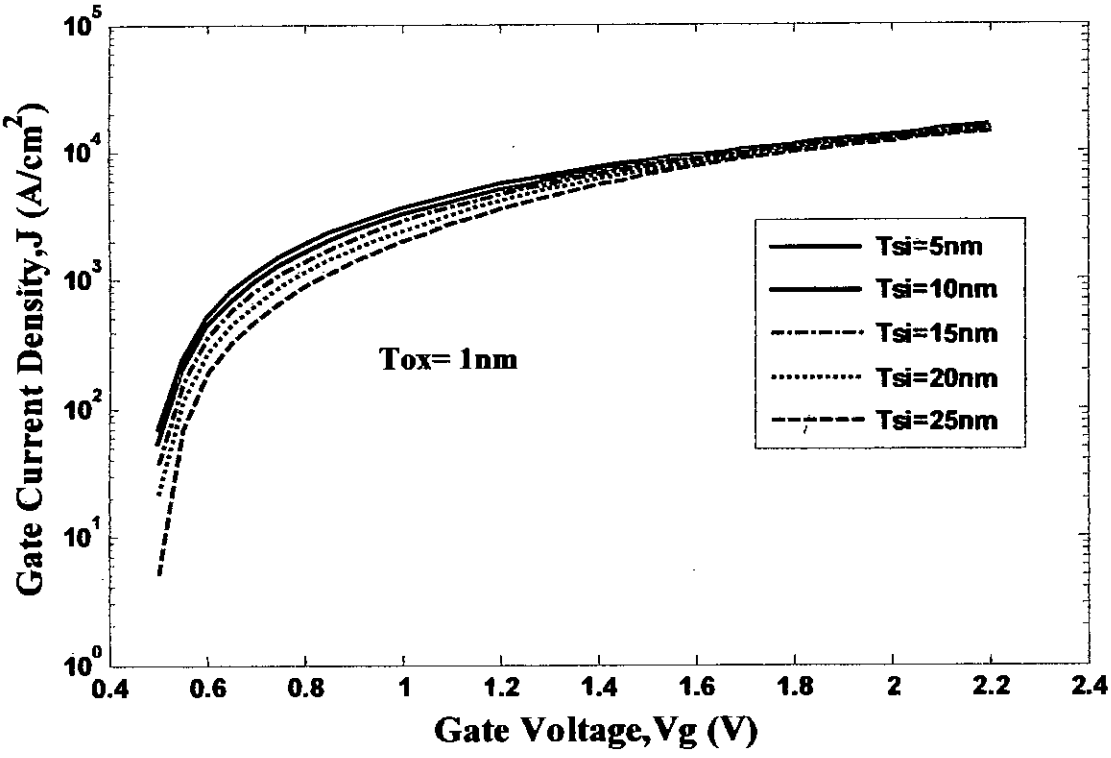

Fig 4.5. Gate leakage current for T_{ox}=1nm as a function of gate voltage, V_g with silicon body thickness, T_{si} as a parameter

In Fig 4.6 simulated results have been compared with the experimental data obtained from Chang *et al.* [49] for an oxide thickness, T_{ox} of 1 nm and silicon thickness, T_{si} of 5 nm to verify the effectiveness of our numerical calculation. It reveals that the simulated results are in good agreement with the reported experimental data.

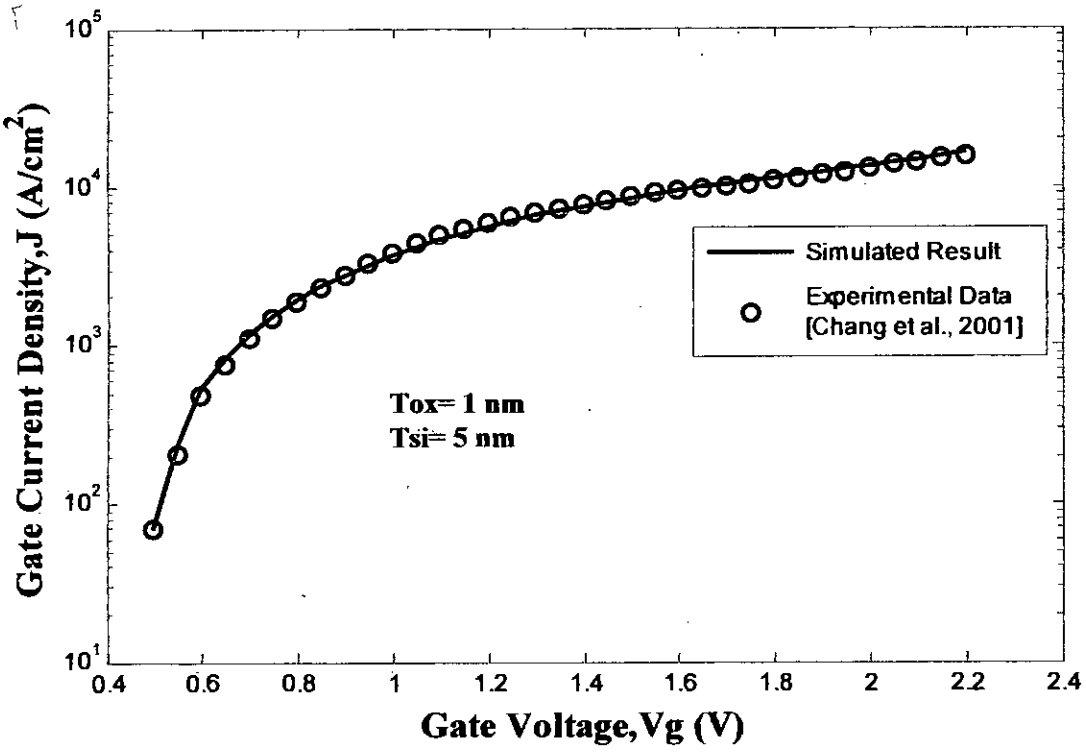

Fig 4.6. Simulated and Experimental Gate leakage current for T_{ox}=1nm, T_{si}=5nm as a function of gate voltage, V_g

The thickness of the oxide layer greatly affects the gate leakage current. As the oxide thickness, T_{ox} is reduced, the effective tunneling distance reduces. As a result the probability for an electron to tunnel through the oxide increases. Again it was observed that, with the decreasing thickness of the oxide, the carrier concentration, N_{ij} at each energy subband of each valley increases greatly. At the same time, corresponding eigen energies also increases which results in a decrease of tunneling lifetime. As a consequence, the gate leakage current increases to a large extent.

Fig. 4.7 and Fig. 4.8 shows the gate leakage current for oxide thickness, T_{ox}=1.5 nm for the same silicon thicknesses and the same applied gate voltages used in Fig. 4.4 as a function of inversion charge density, N_{inv} and gate voltage, V_g respectively.

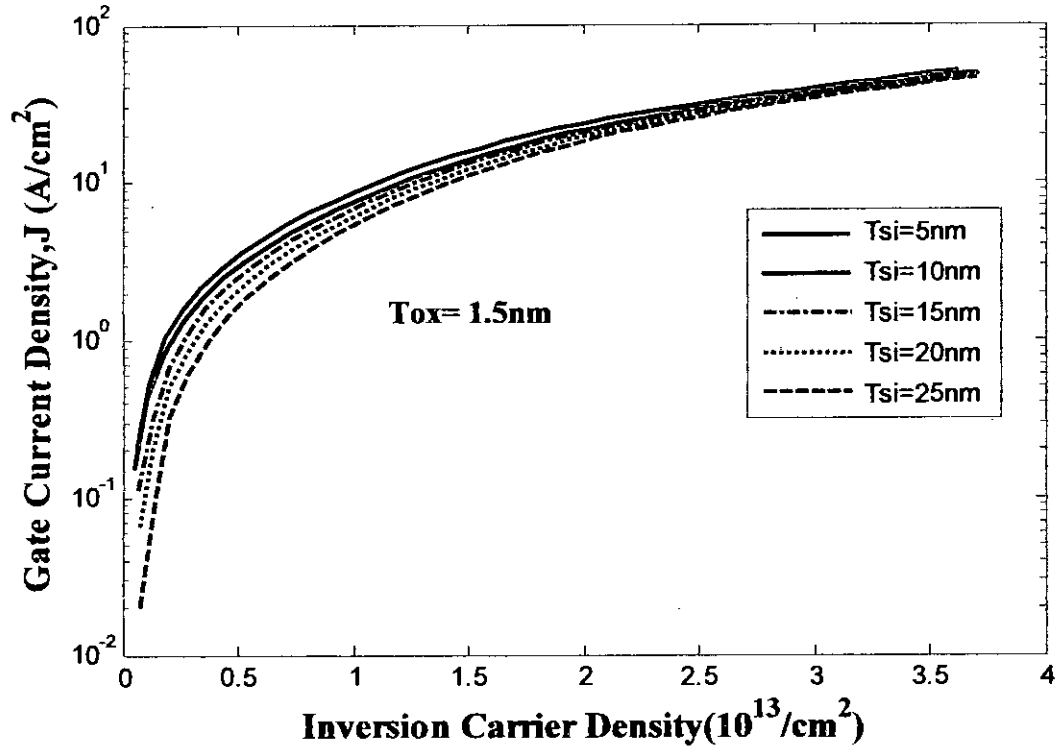

Fig 4.7. Gate Leakage current for T_{ox}=1.5nm as a function of inversion carrier density, N_{inv} with silicon body thickness, T_{si} as a parameter

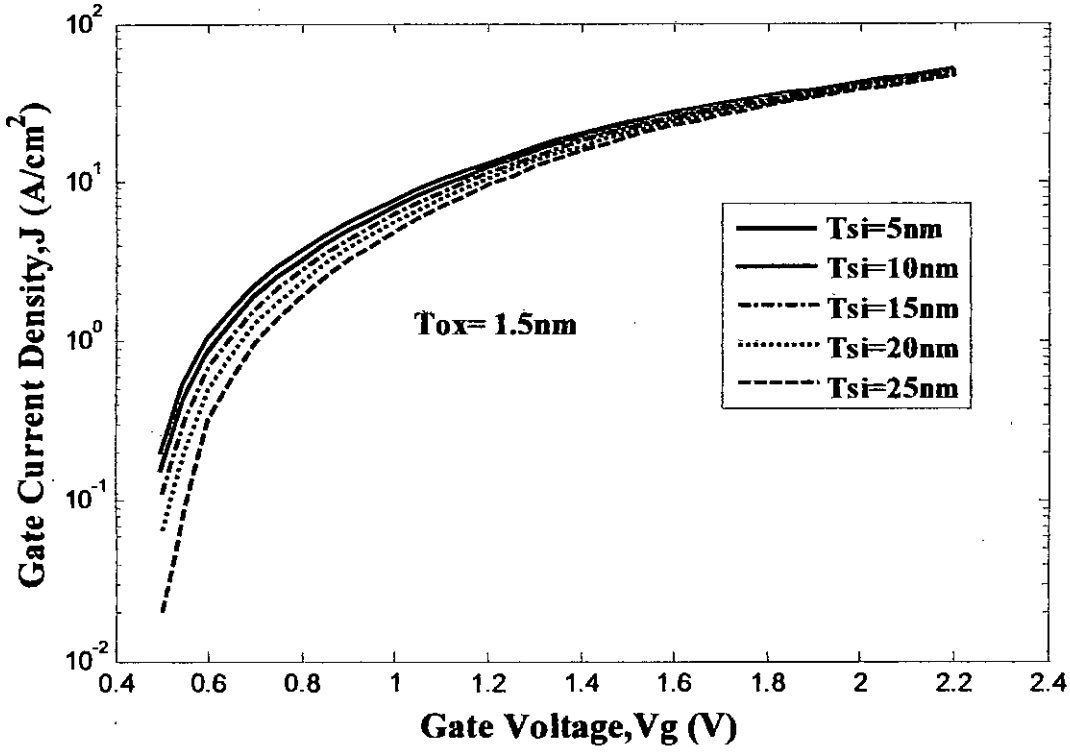

Fig 4.8. Gate leakage current for T_{ox}=1.5nm as a function of gate voltage, V_g with silicon body thickness, T_{si} as a parameter

Similarly, Fig. 4.9 and Fig. 4.10 shows the gate leakage current for oxide thickness, T_{ox}=2 nm for the same silicon thicknesses and the same applied gate voltages used in Fig. 4.4 as a function of inversion charge density, N_{inv} and gate voltage, V_g respectively.

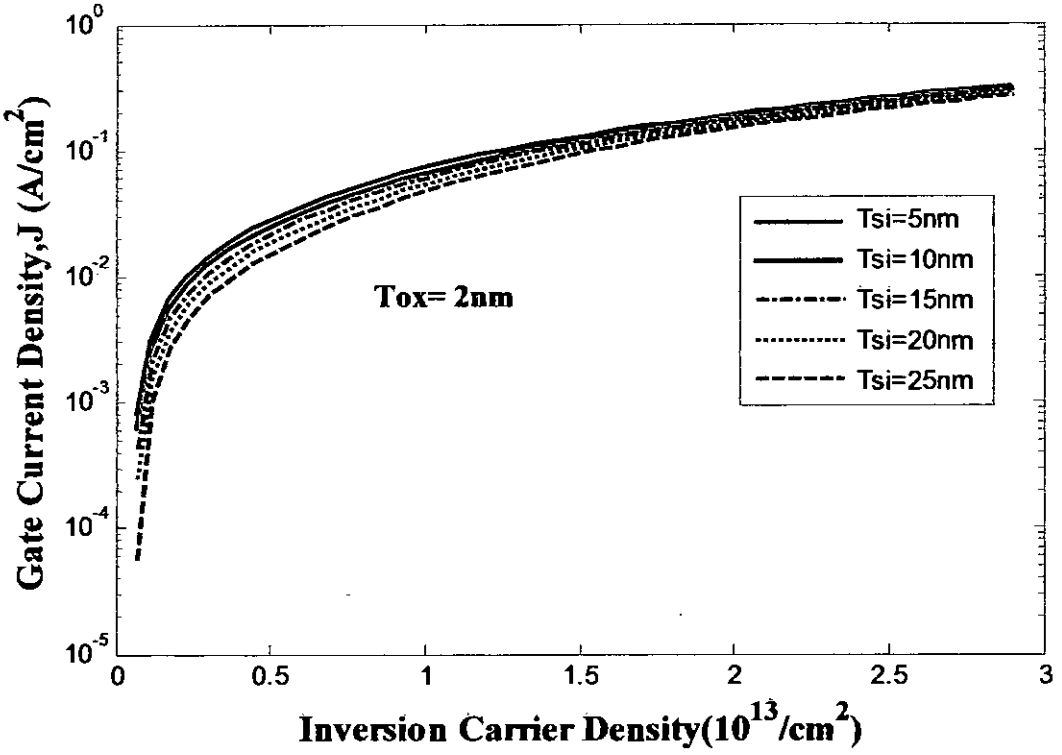

Fig 4.9. Gate Leakage current for T_{ox}=2nm as a function of inversion carrier density, N_{inv} with silicon body thickness, T_{si} as a parameter

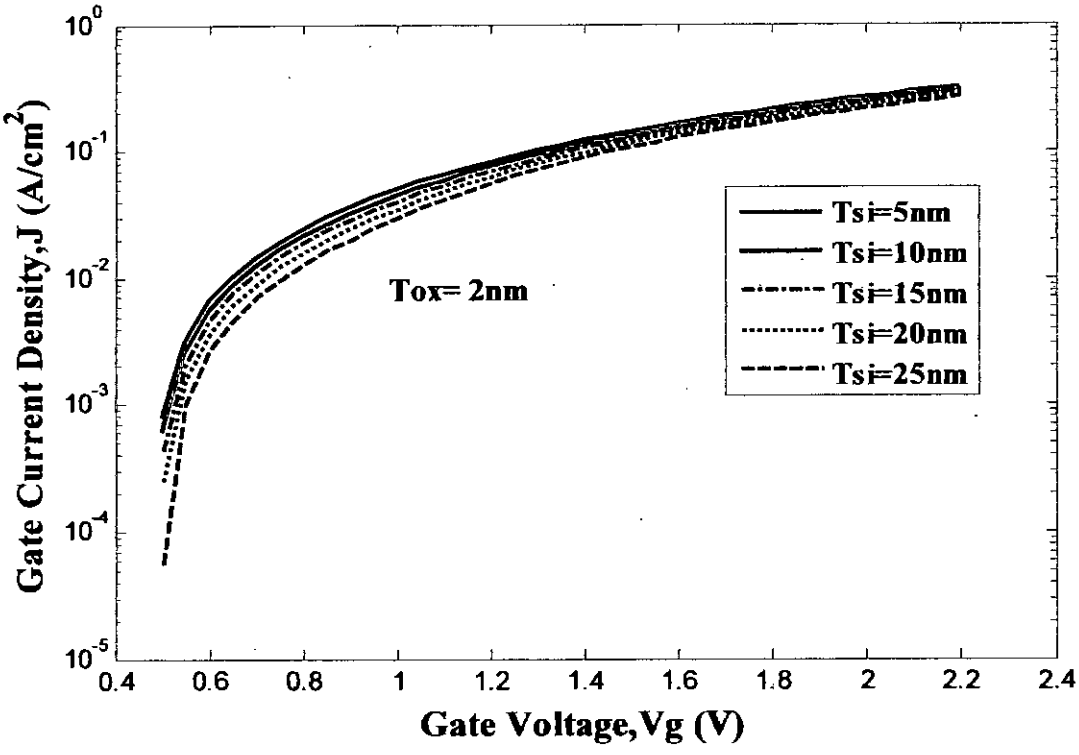

Fig 4.10. Gate leakage current for T_{ox}=2nm as a function of gate voltage, V_g with silicon body thickness, T_{si} as a parameter

Finally, Fig 4.11 provides a comparative study of the gate leakage current of a DGMOS structure on <100> silicon with a silicon thickness of 5 nm with different oxide thickness as a function of gate voltage, V_g.

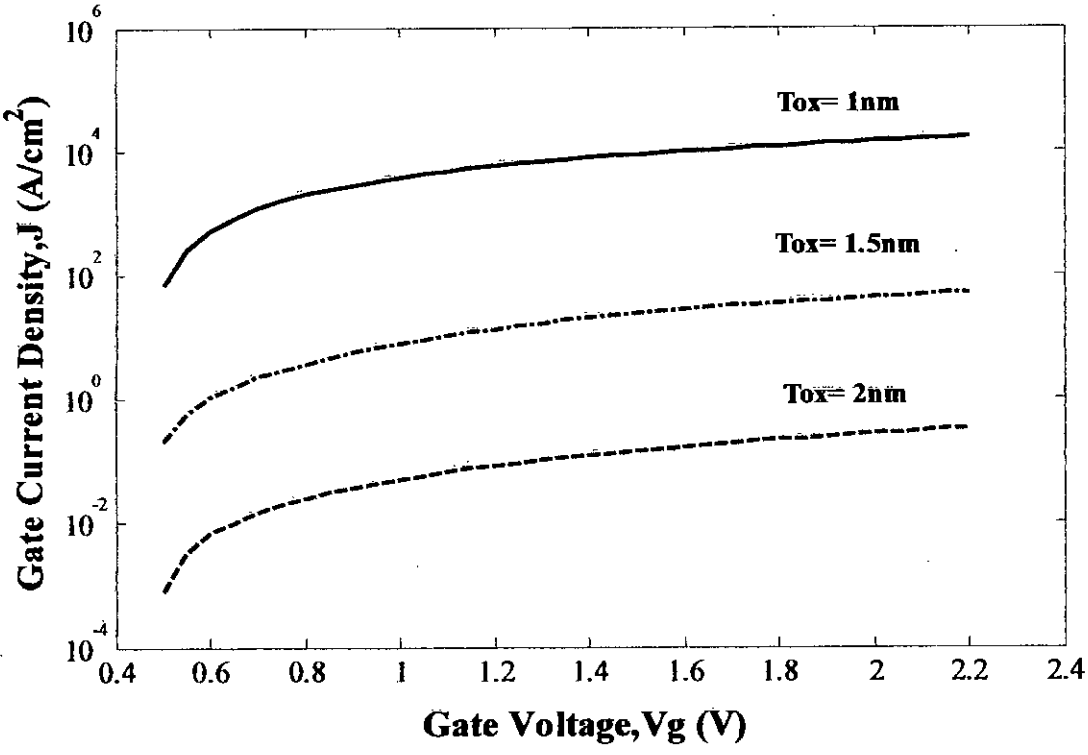

Fig 4.11. Gate leakage current for T_{si} = 5 nm as a function of gate voltage, V_g with oxide thickness, T_{ox} as a parameter

4.4 Silicon crystal orientation dependence of gate leakage current

An important issue that may affect the gate leakage current is the crystallographic orientation of the silicon surface. In this section, we compare the gate leakage current of an n-type DGMOS for (100) and (111) orientation of silicon surface.

From Ref. [12], it can be concluded that, penetration effects are more severe for the (111) orientation than for the (100) orientation. (111) silicon has only one bulk subband in the conduction band with six valleys of degeneracy, having an effective mass ($m_z = 0.258$) which is much lower than that for an electron in the longitudinal valley ($m_l = 0.916$) in (100) silicon. Due to the lower effective mass of electrons in (111) silicon, the average distance of carrier from the interface is high and the effect of penetration is more.

So, a change in the crystallographic orientation of the channel alters the carrier effective mass in the silicon for both tunneling and density of states calculation [12]. This affects the inversion charge distribution and also the charge centroid. Because of all these effects, the gate leakage current for (111) silicon will be greater than that of (100) silicon for the same silicon and oxide thickness at the same inversion charge density, N_{inv} or same gate voltage, V_g. But, it is revealed from our numerical calculations that when the oxide thickness reduces into the direct-tunneling (deep sub micron, T_{ox}<2 nm) regime, variation of gate leakage current for (100) and (111) silicon is less significant for low (V_g< 0.7 V) and high biases (V_g> 1.6 V) but provides some significant variations for medium range of biasing voltages (V_g=0.7 ~1.6 V) which has been established in [51].

The gate leakage current for both (100) and (111) orientations for silicon thickness, T_{si} = 5 nm, 10 nm and 15 nm with oxide thickness, T_{ox} as a parameter at the same gate voltages used in Fig. 4.4 has been reported in Figs 4.12 ~ 4.17.

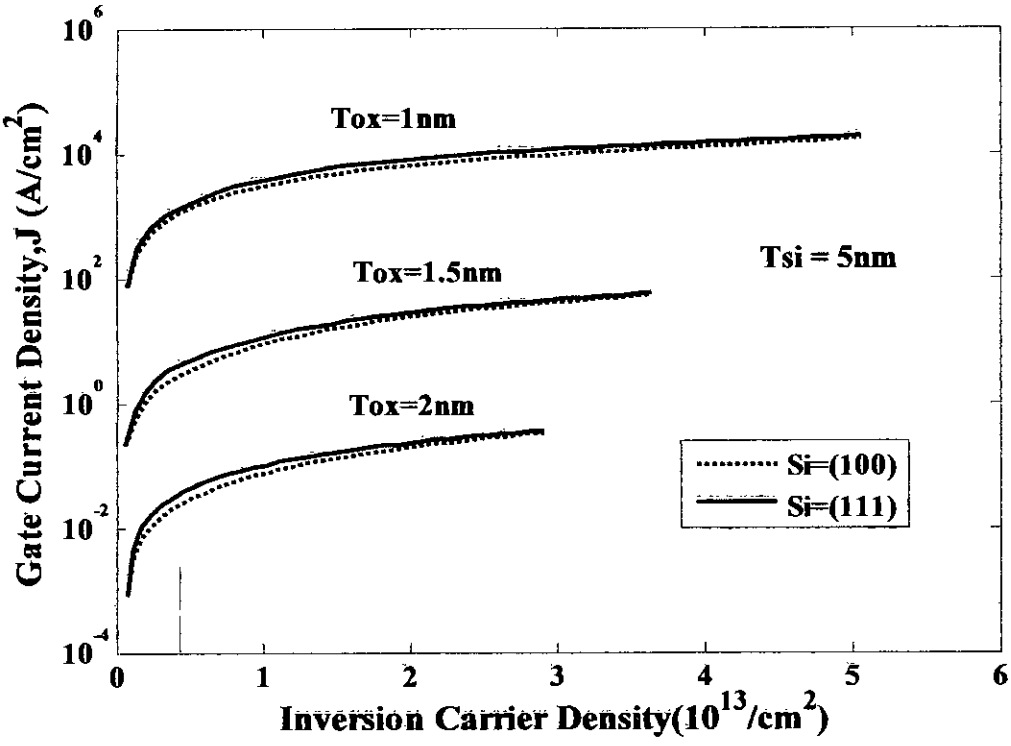

Fig 4.12. Gate leakage current for T_{si} = 5 nm as a function of inversion carrier density, N_{inv} with oxide thickness, T_{ox} as a parameter for (100) and (111)

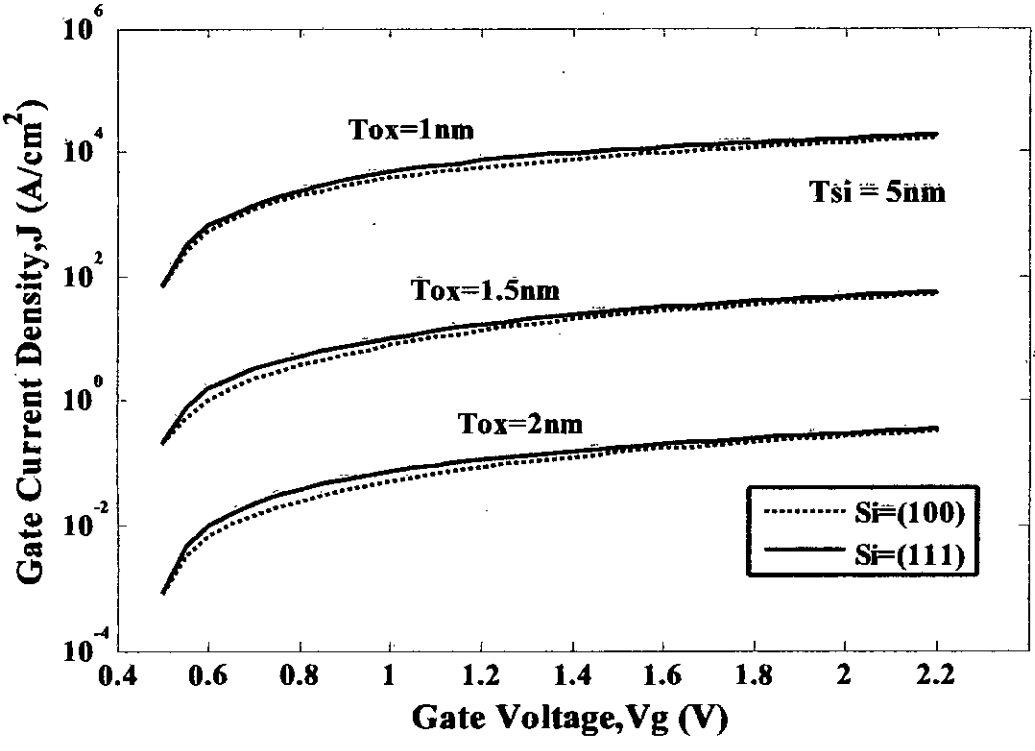

Fig 4.13. Gate leakage current for T_{si} = 5 nm as a function of gate voltage, V_g with oxide thickness, T_{ox} as a parameter for (100) and (111)

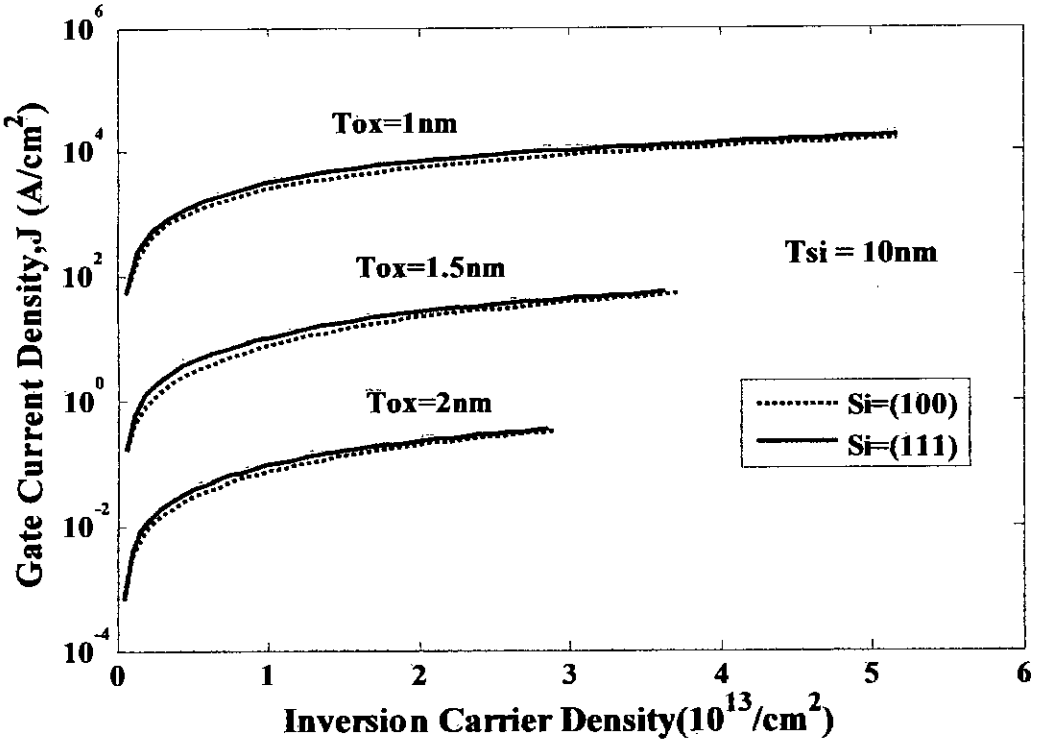

Fig 4.14. Gate leakage current for T_{si} = 10 nm as a function of inversion carrier density, N_{inv} with oxide thickness, T_{ox} as a parameter for (100) and (111)

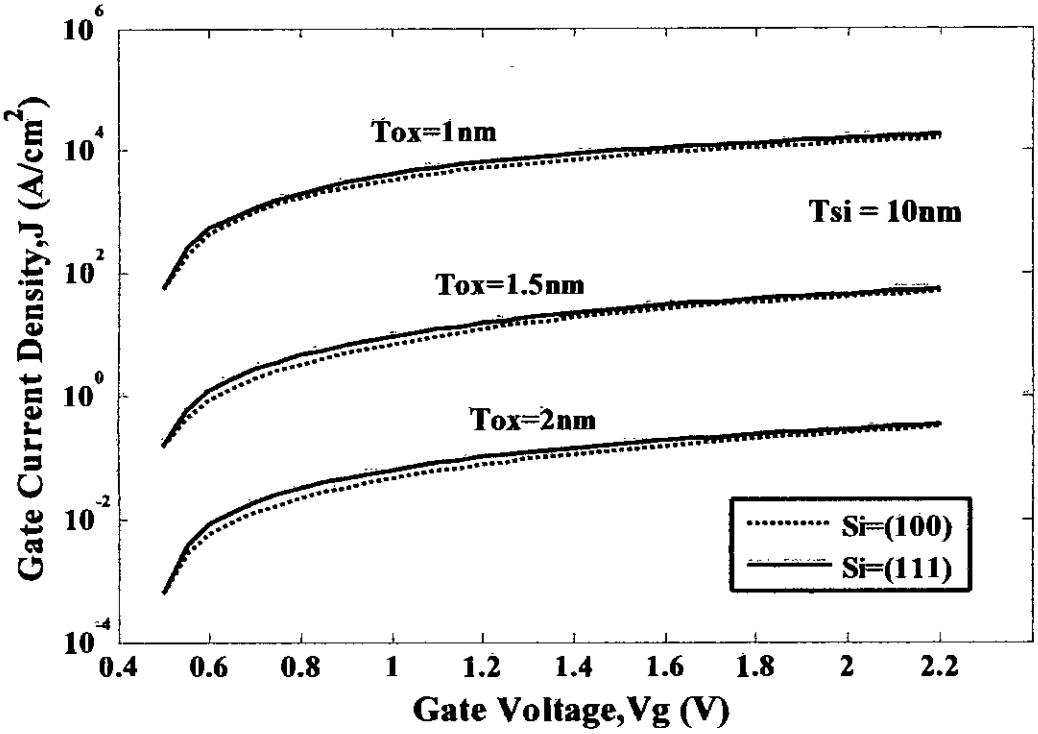

Fig 4.15. Gate leakage current for T_{si} = 10 nm as a function of gate voltage, V_g with oxide thickness, T_{ox} as a parameter for (100) and (111)

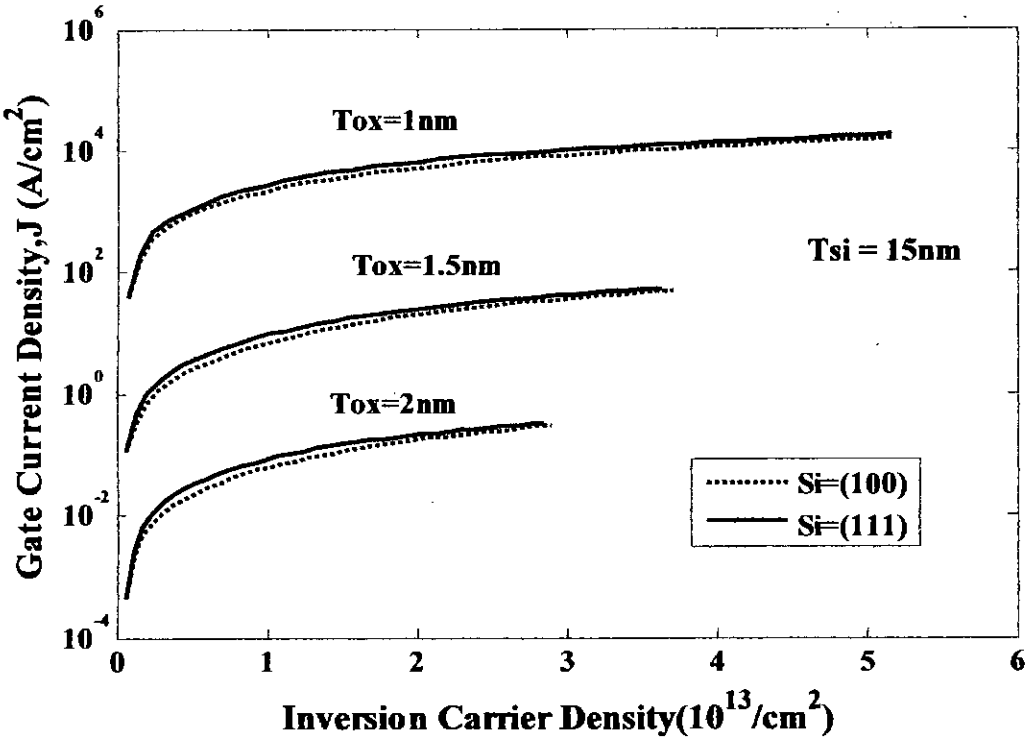

Fig 4.16. Gate leakage current for T_{si} = 15 nm as a function of inversion carrier density, N_{inv} with oxide thickness, T_{ox} as a parameter for (100) and (111)

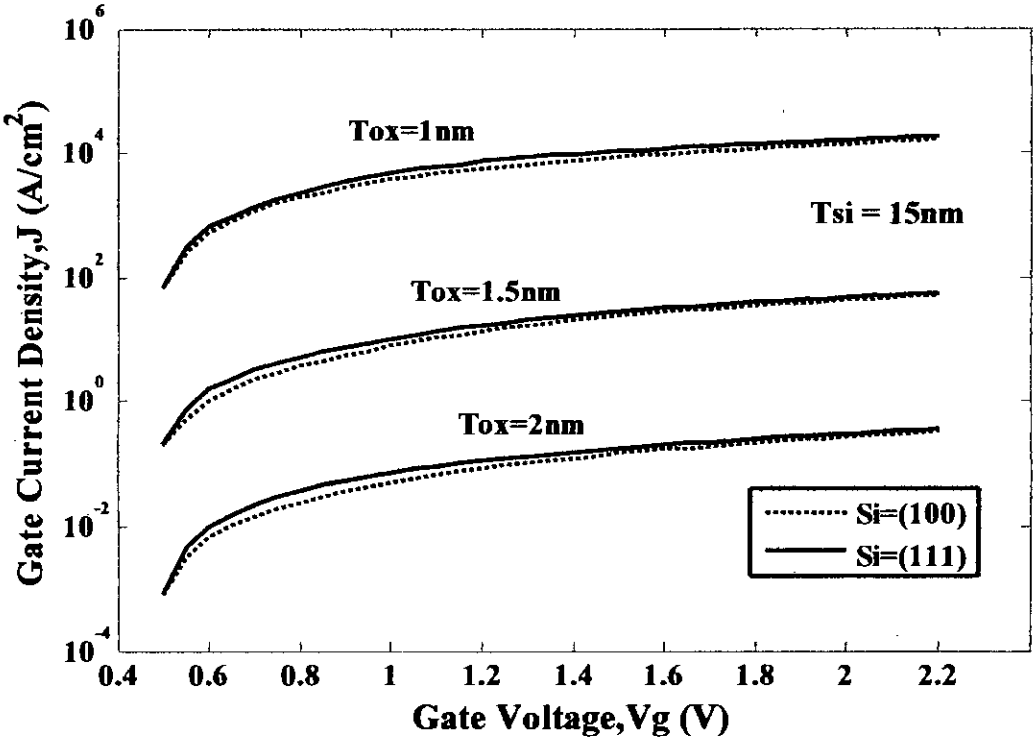

Fig 4.17. Gate leakage current for T_{si} = 10 nm as a function of gate voltage, V_g with oxide thickness, T_{ox} as a parameter for (100) and (111)

4.5 Body and oxide dependence of gate leakage current

Scaling down of body thickness of a double gate MOS increases the gate current. This is due to inversion carrier congestion near Si/SiO_2 interface for a reduced width of potential well, increasing eigen-energy and decreasing carrier lifetime. The gate current dependence on the body thickness emphasizes the importance of considering not only the simple concept of the average vertical electric field, but also the exact bound state energy, which is determined both by this field and by the width of the potential well (the body thickness). However, quantum confinement can be affected, which changes the bound-state energies and, as shown in Fig 4.18 for a gate voltage, V_G=1.1 V both (100) and (111) silicon, can significantly affect gate leakage current. This effect is enhanced in the double-gate structure due to merging of the two inversion layers.

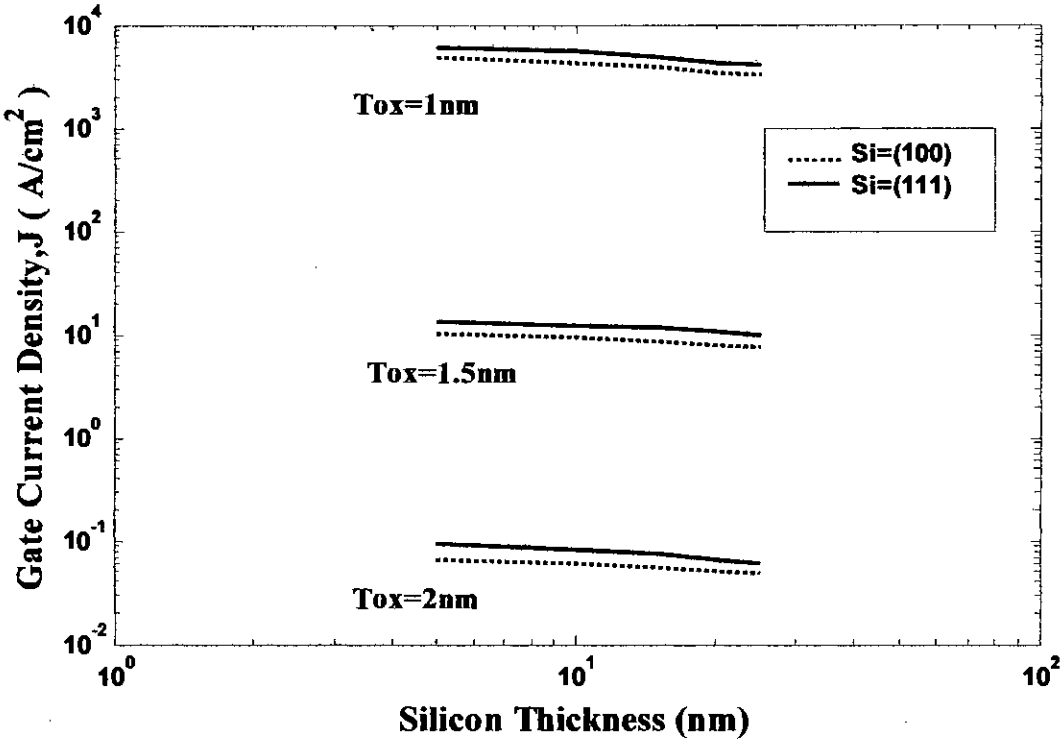

Fig 4.18. Dependence of gate leakage current on silicon body thickness for (100) and (111) orientations of silicon

Also, the parameters, used for the calculation of gate leakage current, are not affected in the same way for (100) and (111) orientations as the thickness of the silicon and oxide layer is changed. So, at the same silicon thickness, the deviation of gate leakage current between the (100) and (111) crystal orientations are not constant at different oxide thicknesses. This is clearly observed in Fig 4.18.

Similarly, as the oxide thickness is down scaled keeping the silicon thickness constant, the gate leakage current will increase. This is shown in Fig 4.19 for (100) silicon and in Fig 4.20 for (111) silicon for a gate voltage, $V_g = 1.1\,\mathrm{V}$.

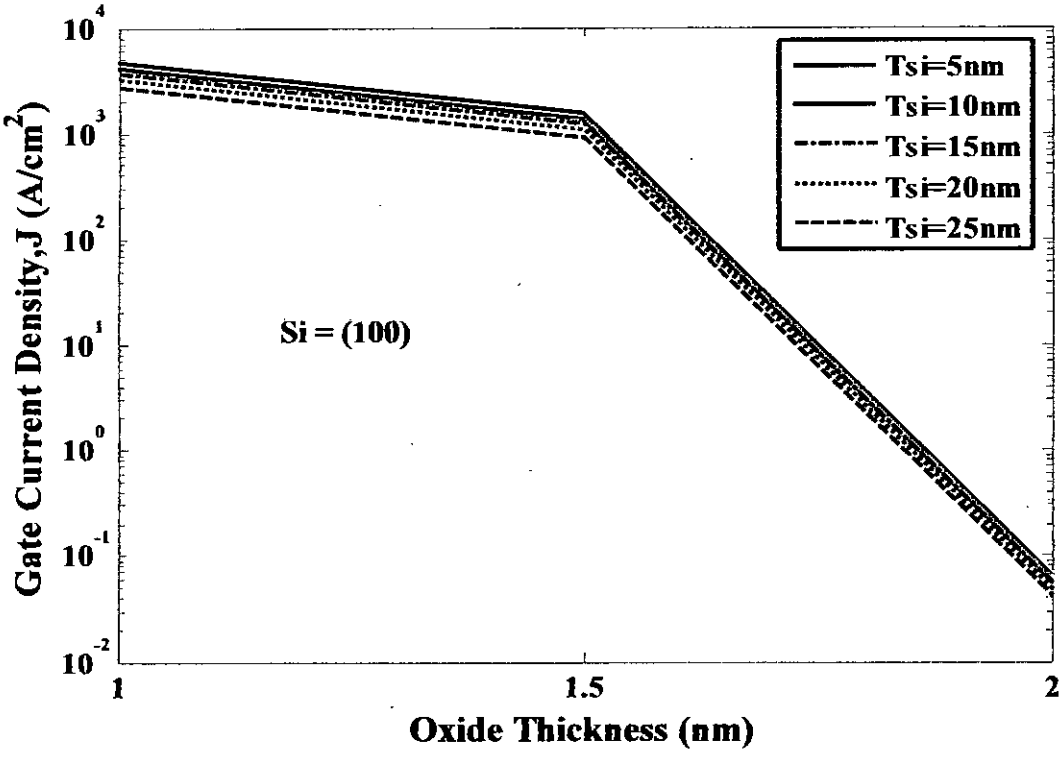

Fig 4.19. Dependence of gate leakage current on oxide thickness for different silicon thickness for (100) silicon

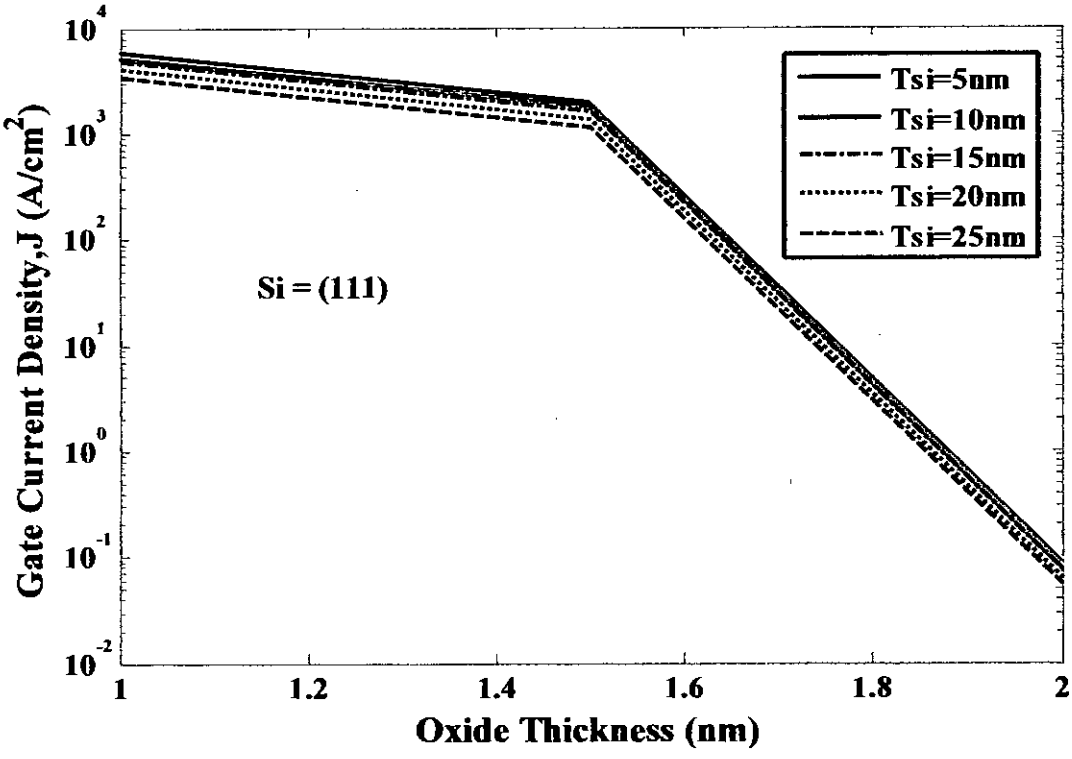

Fig 4.20. Dependence of gate leakage current on oxide thickness for different silicon thickness for (111) silicon

Chapter -5
CONCLUSION

An improved and numerically efficient self-consistent process has been developed for the 1D simulation of n-type DGMOS incorporating the effect of wave function penetration. This process is used to calculate the gate leakage current of an n-type DGMOS for different values of oxide and silicon body thickness and orientation of silicon. Finally, the results have been compared with reported experimental data.

5.1 Summary

Effects of the physical parameters on the gate leakage of an n-type DGMOS have been studied for (100) and (111) orientations of silicon considering the effects of wave function penetration. Penetration effects are included within the self-consistent loop while solving both Schrödinger's and Poisson's equations. An accurate and fast formalism has been used for the solution of Schrödinger's equation using FEMLAB. Poisson's equation is solved for the combined oxide and semiconductor regions by applying an appropriate boundary condition at the gate metal-oxide interface. Rest of the work has been done in MATLAB interfacing with FEMLAB.

Numerical results for n-MOS for both (100) and (111) devices show that, as the gate voltage at the two metal gates increases toward the threshold voltage, mobile charge or electron density becomes appreciable when the conduction band of the silicon body approaches the conduction band of the source-drain. At this, the Fermi energy, E_F of the silicon will continue to rise with respect to the Fermi energy of the metal which causes increasing positive slope inside both the silicon and the oxide region. More and more minority carrier electrons will be concentrated in the vicinity of the oxide-semiconductor interface and the silicon will move from the region of weak inversion towards the region of strong inversion. . As expected, the charge density profile is seen to extend inside the oxide region instead of being zero at the silicon-oxide interface because of the penetration effect.

The numerical results show the impact of body thickness on the gate leakage current. It reveals that, for the same oxide thickness, as the body thickness is decreased, gate leakage current increases significantly. Also, as the thickness of the oxide region is varied, there will be significant variation of the gate leakage current. As the thickness of the oxide is reduced, the effective tunneling distance reduces. So, more and more electrons can tunnel through the oxide region thus increasing the gate leakage current.

Comparing the results obtained in our work for (111) and (100) electrons, it can be concluded that, penetration effects are more severe for the (111) orientation. Because of all these effects, the gate leakage current for (111) silicon will be greater than that of (100) silicon. But, it is revealed from our numerical calculations and also been reported in literature that when the oxide thickness reduces into the direct-tunneling (deep sub micron, T_{ox}<2 nm) regime, variation of gate leakage current for (100) and (111) silicon is less significant for low and high biases but provides some significant variations for medium range of biasing voltages. Finally, the developed method of simulation has been established by comparing the obtained results with reported experimental data.

5.2 Suggestions for Future Work

Self-consistent solution is an important tool for simulation of many devices where the QM effects become significant. Our self-consistent model may be used for simulating many systems, such as single gate, double gate MOS structure, high electron mobility transistors, resonant tunneling diodes and quantum well lasers, where self-consistent calculation with open boundary condition is necessary. A few suggestions for future work are given below.

The developed method can be also applied for the calculation of gate leakage current of a p-MOS by taking some modifications into account. Hence, this method can ultimately be used for the case of CMOS devices which is very crucial for VLSI technology.

In this thesis, 1-D analysis of DGMOS structure has been performed. But, when voltage is applied between the drain and the source, 2-D nature of QM effects arise in the channel. Also a 2-D analysis is greatly required for the determination of carrier mobility and I-V characteristics to establish the effectiveness of the device. So, 2-D simulation should be performed.

As the gate length of CMOS devices are continued to be scaled below the sub-100 nm regime, scaling rules dictate that the gate oxide thickness be scaled down to well below 1 nm. It is found from the results that, with decreasing dielectric thickness, gate leakage current increases rapidly. In order to decrease this leakage current, high-k materials are in consideration as a replacement for SiO_2. Also, for high-k dielectrics it is very important to consider the effect of trap charges. The modeling of such devices can be done easily with the proposed self-consistent model.

In the calculations, effective mass approximation has been used for the electrons. To use this model for holes, due to anisotropy and mixing of valence bands, the use of effective mass approximation for holes has been a point of debate. The developed model can be used for p-MOS devices by incorporating the non-parabolic valence band structure.

BIBLIOGRAPHY

[1] G. Moore, "Progress in digital integrated electronics," in *IEDM Tech. Digest*, pp.11-13, 1975.

[2] *The International Tech. Roadmap for Semiconductors.* San Jose, CA, Semiconductor industry Assoc., 2006.

[3] S. Wind, D. Frank, and H. Wong, "Scaling silicon mos device to their limits," *Microelectronics Engg.*, vol. 32, pp. 271-282, 1996.

[4] L. Su, J. Jacobs, J. Chung, and D. Antoniadis, "Deep-submicrometer channel design in silicon-on-insulator (SOI) MOSFETs," in *IEDM Tech. Digest*, pp. 183-186, 1994.

[5] H. Wong, D. Frank, and P. Solomon, "Device design considerations for double gate, ground-plane, and single-gated ultra-thin soi mosfets at the 25 nm channel length generation," in *IEDM Tech. Digest*, pp. 407-410, 1998.

[6] L. Chang, S. Tang, T. King, J. Bokor, and C. Hu, "Gate length scaling and threshold voltage control of double-gate mosfets," in *IEDM Tech. Digest*, pp. 719-722, 2000.

[7] Z. Ren, S. Bourland, S. Lee, J. Denton, M. Lundstrom, and R. Bashir, "Ultra-thin body soi by controlled oxidation of thin si membranes," in *IEEE Silicon Nanoelectronics Workshop*, pp. 11-12, 2000.

[8] F. G. Pikus and K. K. Likharev, "Nanoscale field-effect transistors: An ultimate size analysis," *Appl. Phys. Lett.*, Vol. 71, (25), 1997.

[9] Z. Ren, R. Venugopal, S. Datta, M. Lundstrom, D. Jovanovic and J. G. Fossum, "The Ballistic Nanotransistor: A Simulation Study," *Tech. Dig., Int. Electron Dev. Mtg.*, pp. 715-718, Dec. 2000.

[10] K. Suzuki and T. Sugii, "Analytical Models for n+-p+ Double-Gate SOIMOSFET's," *IEEE Trans. Electron Devices*, Vol. 42, pp. 1940-1948, 1995.

[11] G. Baccarani, S. Reggiani, "A Compact Double-Gate MOSFET Model Comprising Quantum-Mechanical and Nonstatic Effects," *IEEE Trans. Electron Devices,* Vol. 46, pp. 1656-1666, 1999.

[12] F. Stern, "Self-consistent results for n-type Si inversion layers," *Phys. Rev. B,* vol. 5, pp. 4891-4899, 1972.

[13] S. M. Sze, *Physics of Semiconductor Devices,* Wiley Eastern Limited, pp. 362-366, 1987.

[14] Y. Tsividis, *Operation and Modeling of MOS Transistor,* McGraw-Hill, Ch-2, 1999.

[15] J. Wang and M. Lundstrom, Tech. Dig. - Int. Electron Devices Meet. 2002, 707 (2002).

[16] T. Sekigawa and Y. Hayashi, "Calculated Threshold-Voltage Characteristics of an XMOS Transistor Having an Additional Bottom Gate," *Solid-State Electron.* 27, 827 1984.

[17] D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda, "A Fully Depleted LeanChannel Transistor (DELTA)," *IEDMTech. Digest,* pp. 833-836, 1989.

[18] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," *IEDMTech. Digest,* pp. 67-70, 1999.

[19] J.P. Colinge, M.H. Gao, A. Romano, H. Maes, and C. Claeys, "Silicon-on-insulator gate-all-around device", *IEDMTech. Digest,* p. 595, 1990.

[20] S. Miyano, M. Hirose, and F. Masuoka, "Numerical analysis of a cylindrical thinpillar transistor (CYNTHIA)," *IEEE Trans. Electron Devices,* vol. ED-39, pp. 1876 1881,1992

[21] A. Nitayama, H. Takato, N. Okabe, K. Sunouchi, K. Hieda, H. Horiguchi, and F. Masuoka, "Multi-Pilliar surrounding gate transistor (M-SGT) for compact high-speed circuits," *IEEE Trans. Electron Devices,* vol. 38, pp. 579-583, Mar. 1993.

[22] S. Venkatesan, G. V. Neudeck, and R. F. Pierret, "Double-gate operation and volume inversion in n-channel SOl MOSFET's," *IEEE Electron Device Left.,* vol. 13, pp 44-46, Jan. 1992.

[23] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOl MOSFET's," *IEEE Trans. Electron Devices,* vol. 40, pp. 2326-2329, Dec. 1993.

[24] K. Suzuki, Y. Tosaka, and T. Sugii, "Analytical threshold voltage model for short channel n+ -p+ double-gate SOI MOSFET's," *IEEE Trans. Electron Devices,* vol. 43, pp. , 732-738, May 1996.

[25] G. Baccarani and S. Reggiani, "A compact double-gate MOSFET model comprising. quantum-mechanical and nonstatic effects," *IEEE Trans. Electron Devices,* vol. 46, pp. 1656-1666, Aug. 1999.

[26] S.-H. Oh, D. Monroe, and J. M. Hergenrother, "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical surrounding-gate MOSFETs," *IEEE Electron Device Left.,* vol. 21, pp. 397-399, Sept. 2000.

[27] S.-L. Jang, M.-C. Hu and S.-S Uu, "An analytical symmetric double-gate silicon-oninsulator metal-oxide-semiconductor field-effect-transistor model," *Jpn. J Appl. Phys.* Vol. 36, pp. 6250-6253, 1997.

[28] B. Majkusiak, T. Janik and J. Walczak, "Semiconductor thickness effects in the double-gate SOI MOSFET," *IEEE Trans. Electron Devices,* vol. 45, pp. 1127-1134, May 1998.

[29] Y. Taur, "An analytical solution to a double-gate MOSFET with undoped body," *IEEE Electron Device Let/.,* vol. 21, no. 5, May. 2000.

[30] Y. Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs," *IEEE Trans. Electron Devices,* vol. 48, pp. 2861-2869, Dec. 2001.

[31] L. Ge and J. G. Fossum, "Analytical modeling of quantization and volume inversion in thin Si-film DG MOSFETs," *IEEE Trans. Electron Devices,* vol. 49, pp. 287-294, Feb. 2002.

[32] Q. Chen, B. Agrawal, and J. D. Meindl, "A comprehensive analytical subthreshold swing (S) model for double-gate MOSFETs," *IEEE Trans. Electron Devices,* vol. 49, pp. 1086-1090, June 2002.

[33] T. Ernst, S. Cristoloveanu , G. Ghibaudo, T. Ouisse, S. Horiguchi, Y. Ono, Y. Takahashi, and K. Murase, "Ultimately thin double-gate SOI MOSFETs, " *IEEE Trans. Electron devices,* Vol. 50, No.3, pp. 830 - 838, March 2003.

[34] M. Wong and X. Shi, "On the threshold voltage of symmetrical DG MOS capacitor with intrinsic silicon body," *IEEE Trans. Electron devices,* Vol. 51, No.1 0, pp. 16001604, October 2004.

[35] M. Alessandrini, D. Esseni, and C. Fiegna, "Development of an analytical mobility model for the simulation of ultra-thin single- and double-gate SOI MOSFETs," *SolidState Electron,* vol. 48, p. 589,2004.

[36] H. C. Pao and C. T. Sah, "Effects of diffusion current on characteristics of metaloxide (insulator)-semiconductor transistors," *Solid-State Electron.,* vol. 9, p. 927, 1966.

[37] A. Haque, A. N. Khondker, ''An efficient technique to calculate the normalized wavefunction in arbitrary 1-dimensional quantum well structure", *J. Appl. Phys.*, vol. 84, pp. 5802-5804, 1998.

[38] M. Bohr, Ed. "Novel Device Options for Sub-100 nm CMOS," H.-S. P. Wong, in *IEDM Short Course: Sub-100 nm CMOS"*, presented at the IEEE International Electron Devices Meeting, 1999.

[39] H.-S. Wong, D. Frank, and P. Solomon, "Device Design Considerations for Double-Gate, Ground-Plane, and Single-Gated Ultra-Thin SOI MOSFETs at the 25 nm Channel Length Generation,", *IEDM Tech. Digest*, p. 407 (1998).

[40] T. Ghani *et al.*, "Scaling Challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors", *Symp. VLSI Technology Dig. Tech. Papers*, Honolulu, HI, June 2000, pp. 174-175.

[41] X. Tang, V.K. De and J.D. Meindl, "Intrinsic MOSFET parameter fluctuations due to random dopant placement", *IEEE Trans. VLSI Syst.*, vol. 5, pp. 369-376, Dec. 1997.

[42] F. Balestra, S. Cristoloveanu, M. Benachir and T. Elewa, "Double gate Silicon-on-Insulator Transistor with Volume inversion: A New Device with Greatly Enhanced Performance", *IEEE Electron. Dev. Lett.* 8 (1987), p.410.

[43] A. Haque and M. Z. Kauser, "A comparison of wave-function penetration effects on gate capacitance in deep submicron n- and p-MOSFETs," *IEEE Trans. Electron Devices,* vol. 49,no.9,pp.1580-1587,Sep.2002.

[44] N. Yang, W. K. Henson, J. R. Hauser, and J. J. Wortman, "Modeling Study of Ultrathin Gate Oxides Using Direct Tunneling Current and Capacitance – Voltage Measurements in MOS Devices", *IEEE Transactions On Electron Devices*, vol. 46, no. 7, July 1999.

[45] A. N. Khondker, M. Rezwan Khan and A.F.M. Anwar, "Transmission line analogy of resonance tunneling phenomena: The generalized Impedance concept," *J. Appl. Phys.*, 63(10), 15 May, 1988.

[46] S. Jallepalli, J. Bude *et ai,* "Electron and hole quantization and their impact on deep submicron silicon p- and n-MOSFET characteristics," *IEEE Trans. Electron Devices,* vol. 44,pp.297-302,1997.

[47] R. F. Pierret and G. W. Neudeck, *"Field Effect Devices", Second Edition,* Addison-Willey Publishing Company, Ch-2, 1990.

[48] L. T. Su, H. Fang, J. E. Chung, and D. A. Antoniadis, "Hot-carrier effects in fully-depleted SOI nMOSFETs," in *IEDM Tech. Dig.*, Dec. 1992, pp. 349–352.

[49] L. Chang, K. J. Yang, Y.-C. Yeo, Y.-K. Choi, T.-J. King, and C. Hu, "Reduction of direct-tunneling gate leakage current in double-gate and ultra-thin body MOSFETs," in *IEDM Tech. Dig.*, Dec. 2001, pp. 99–102.

[50] S. Ahmed, M. K. Alam, A. Alam, M. G. Rabbani and. Q. D. M. Khosru ," Quantum Mechanical Study of Gate Leakage Current in Double Gate MOS Structures", accepted for publication at the *International Semiconductor Device Research Symposium (ISDRS 2007),* College Park, MD, USA, to be held on Dec. 12-14, 2007.

[51] H. S. Momose, T. Ohguro, S. Nakamura, Y. Toyoshima, H. Ishiuchi, and H. Iwai, "Study of wafer orientation dependence on performance and reliability of CMOS with direct-tunneling gate oxide," in *Symp. VLSI Tech.*, June 2001, pp. 77–78.

APPENDIX A

The modified self-consistent model, which has been used in this study, has been described in detail in section 3.2. A flow diagram of the solver is given in this section for better understanding.

A.1 Flowcharts

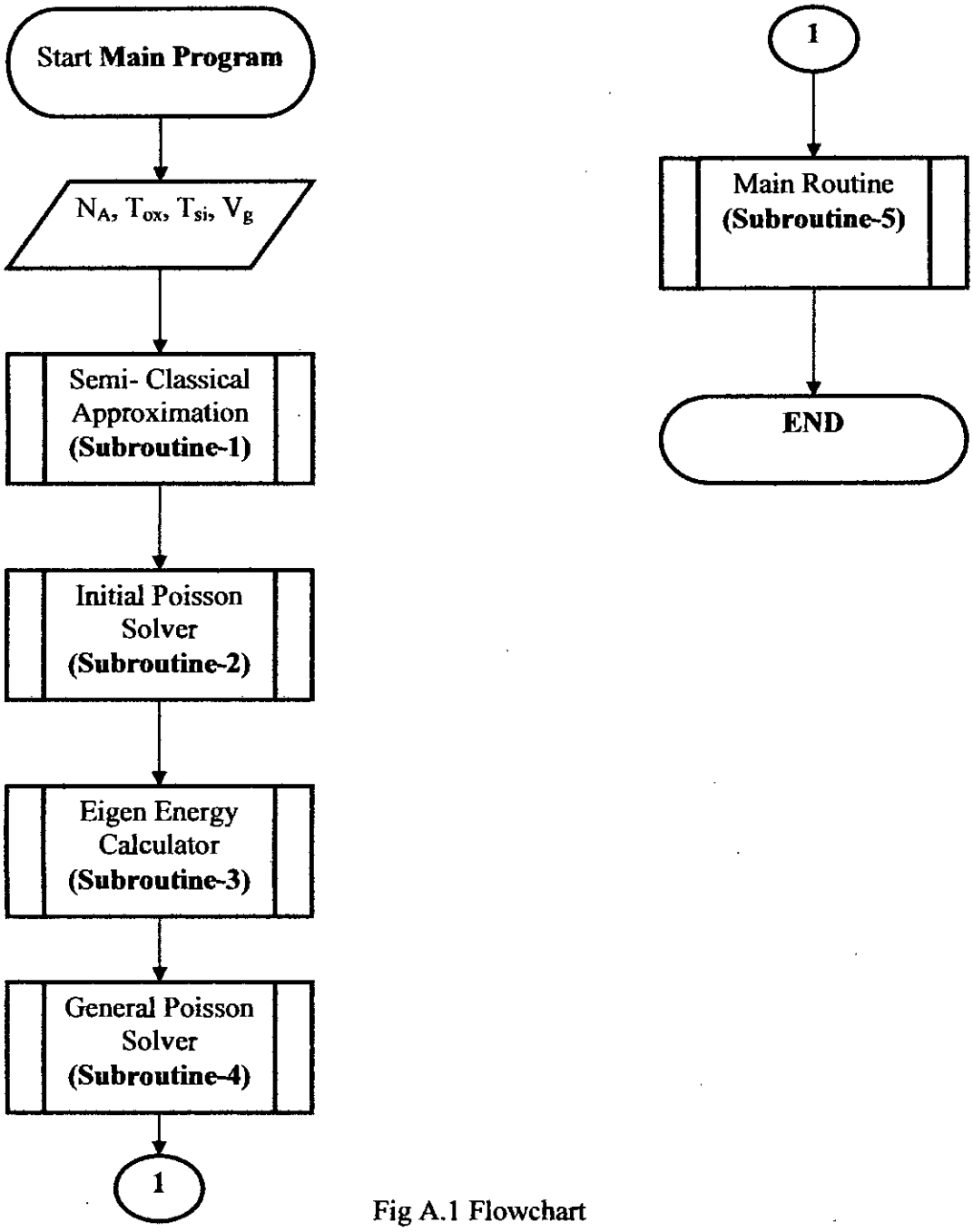

Fig A.1 Flowchart

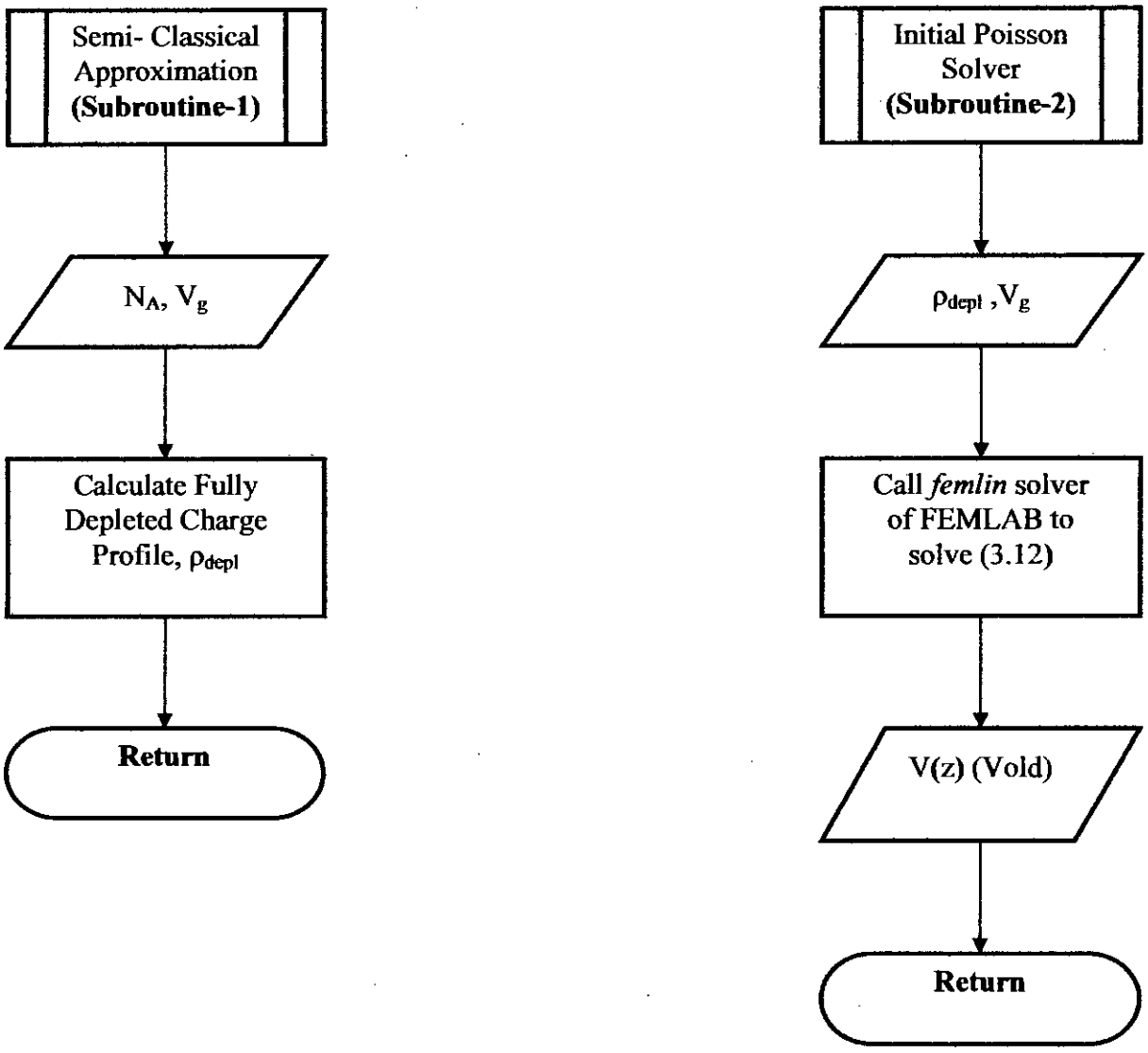

Fig A.2 Flowchart (contd.)

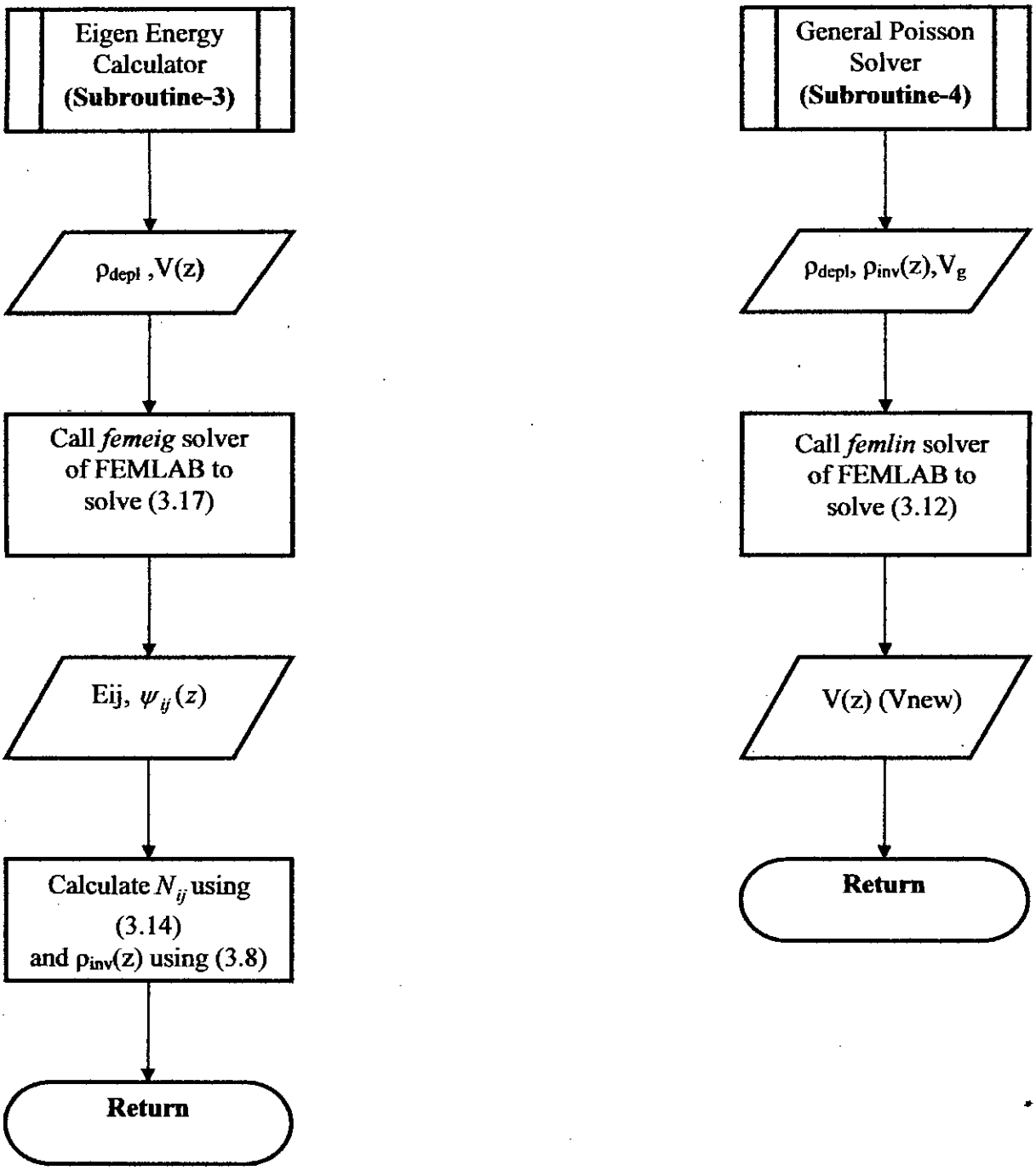

Fig A.3 Flowchart (contd.)

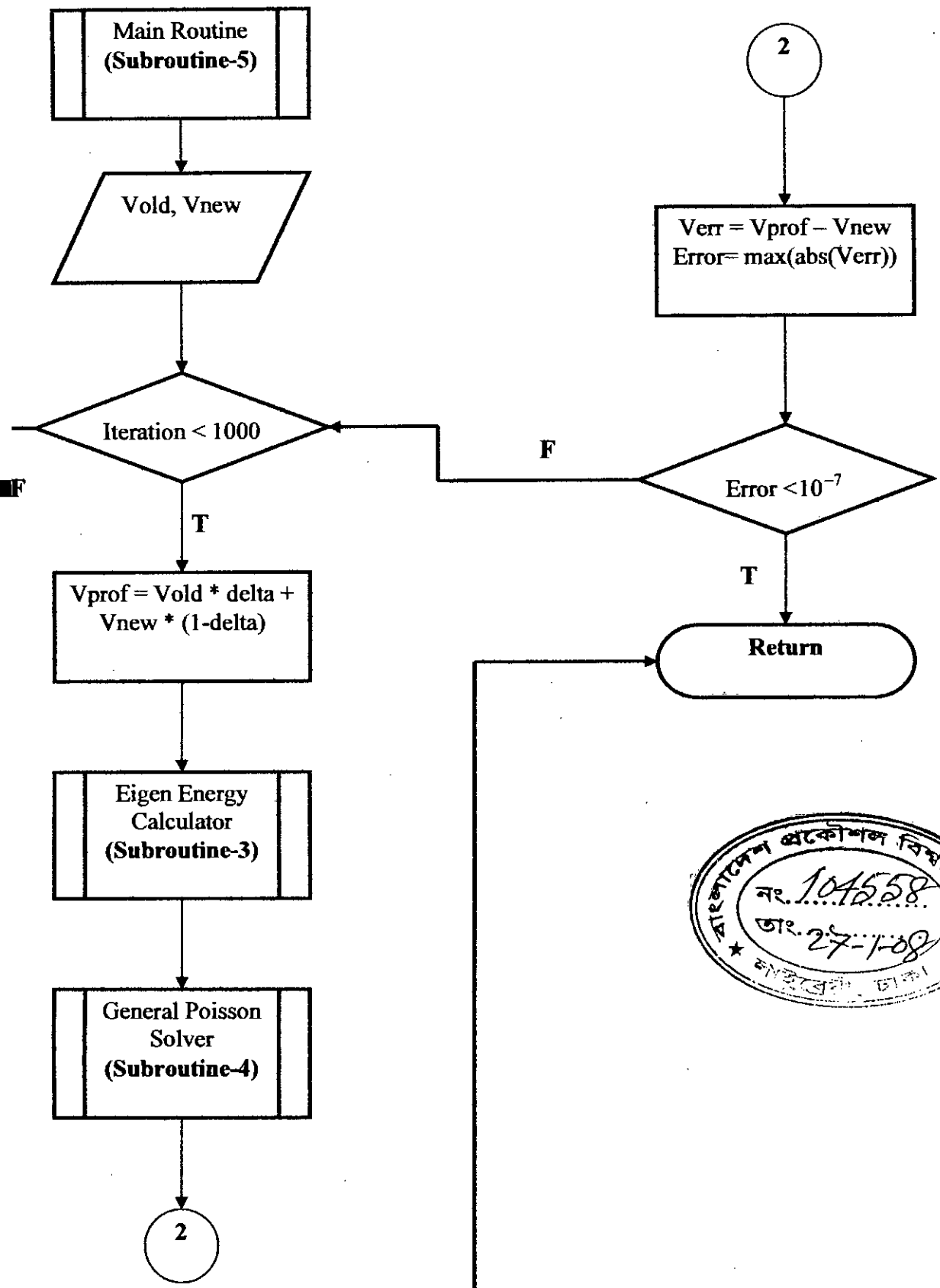

Fig A.4 Flowchart (contd.)