

19/11/12

L-3/T-2/CSE

Date : 19/11/2012

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations 2010-2011

Sub : CSE 315 (Microprocessors and Microcontrollers)

Full Marks: 210

Time : 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks.

**SECTION - A**

There are **FOUR** questions in this Section. Answer any **THREE**.

1. (a) Suppose you are to design an automated fire control system for a highly sophisticated room. To detect the fire, a pair of sensors (a smoke (S) and a temperature (T) sensor) is used. The sensors work in this way: the S sensor provides 0 volt if there is no smoke in the room. When it detects smoke, it jumps to 5 volt. The T sensor provides analog voltage in the range of 0 to 5 volt in proportional to the temperature between 0 C to 100 C. To be sure that the smoke is indeed caused by the fire you have to check the temperature of the room. So, the system continuously listens to the S sensor and collects the temperature from T sensor only after detection of smoke in the room. If the temperature of the room is found greater than 60 C after detection of smoke, the system will initiate an alarm to buzz. There will be a switch to stop the alarm. If the alarm is not switched off within one minute of the initiation of buzz, the system will send a start signal to the automated fire fighting system which is connected to the fire control system. (8+8=16)

Now,

- (i) Draw the block diagram with appropriate connections of the system along with pin names. You cannot use polling approach to collect data from any of the sensors.
  - (ii) Show the working procedure of your designed system using a flow chart.
- (b) Explain with figure the Program memory map and Data memory map of ATmega micro-controller. (7)
- (c) Explain Harvard architecture and von-Neumann architecture. What architecture is followed by the ATmega micro-controller? (7)
- (d) Write five applications where micro-controllers are used. (5)
2. (a) Explain how an ATmega CPU can read or write the 16-bit Timer/Counter (TCNT1) register in a single clock cycle using its 8-bit data bus. Write the necessary assembly code fragment for the following two atomic operations: (5+4+4=13)
- (i) Write the value 0x3F55 to TCNT1
  - (ii) Read the value of TCNT1 to the registers r15 & r16, where r16 contains the high byte.
- (b) Draw the block diagram of the input capture unit of the Timer1 of an ATmega micro-controller and explain its operation assuming input is coming from an external source. (12)
- (c) Explain the working principle of the three major applications of Timer1 of an ATmega micro-controller. Specify the interrupts that are needed to use for each of those applications. (10)

**CSE 315**

3. (a) Suppose you want to produce a custom waveform having duty cycle = 0.5 and period = 1000  $\mu$ s. Show with figure how you can generate the custom waveform using each of the CTC, Fast PWM, and Phase Correct PWM operational modes of Timer1 of an ATmega micro-controller. Specify the necessary values of the related registers for each mode. Assume that the micro-controller is operating at 1MHz clock rate. (4+4+4=12)
- (b) Draw the block diagram of the memory and central processing unit of an ATmega Micro-controller. How does it ensure instructions to be executed in every clock cycle? (16)
- (c) What precautions must be taken when using Data Register empty Interrupt (UDRI) and Receive Complete Interrupt (RXCI) in interrupt-driven data transmission for serial communication using an ATmega micro-controller? (7)
- (d) Why ADCL must be read before ADCH when ADC of an ATmega 16 generates 10-bit result. (6)
4. (a) Suppose you are designing a micro-controller based automated system that takes input from an analog device and sends it to a computer via USART after the necessary conversion is done. The analog device generates analog voltage precisely in every 200  $\mu$ s and the analog voltage persists for a very brief period of time. Assume that the micro-controller is operating at 1MHz clock rate. You cannot use polling approach in any step of your automated system. Now answer the following: (3+3+3+3+6=18)
- (i) Which mode of the ADC is appropriate in this case and why?
  - (ii) How can you ensure that ADC samples analog voltage precisely in every 200  $\mu$ s?
  - (iii) What will be triggering event to start the A-to-D conversions?
  - (iv) How many ISRs you need to write and what are the purposes of those ISRs?
  - (v) Write the necessary steps to configure the micro-controller for the automated system. You need to mention the name of the necessary registers and action on the register.
- (b) Describe with figure the Start Bit Sampling process used by the clock recovery logic of an ATmega micro-controller to synchronize its internal clock to the incoming serial frames for both normal mode and double speed mode. (11)
- (c) What are the values of the necessary registers to configure the baud rate of 9600 bps in Asynchronous Double Speed Mode for serial communication using an ATmega 16? Assume system clock is configured as 2MHz. (6)

**CSE 315**

**SECTION – B**

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) Discuss with appropriate figure how memory addressing is done. Assume that the current segment selector is pointing to GDT. (20)

(b) Suppose DS has the value 000B (in Hex). The following table describes the GDT: (15)

Entry	Descriptor Value (in Hex)
0	—
1	0031E110FFFF0000
2	0031E101FFFF0000
3	0031E100FFFF0000

The base address stored in GDTR is 0000FFFF.

Now answer the following questions:

- (i) What should be the value of the limit field of GDTR?
- (ii) Suppose you are using DS as the segment selector (with the value given above) to access a memory location for reading and writing data. Will the instruction execute successfully? Justify your answer.
- (iii) Suppose you want to read some data from the GDT. Using the above configuration, would it be possible? Explain.

6. (a) Describe with appropriate figure how calling is done through a call gate. (20)

(b) Describe the rule that determines who can use a call gate. (5)

(c) What problems may arise with regards to the stack when a call gate is used and how this problem is tackled? (10)

7. (a) Describe the linear-to-physical address translation procedure with appropriate figure. (18)

(b) How can you effectively "turn off" segmentation? (5)

(c) Describe how you can produce contiguous linear addresses through page translation. (12)

8. (a) Describe the task switch operation with appropriate figure. (25)

(b) Consider the effect of a task switch on the TSS. Present in a tabular format the status of NT bit and Busy bit in the Old TSS and New TSS respectively for JMP, Call Interrupt/Exception and IRET instructions. (10)

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**SECTION - A**

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) Describe functionality of different layers in OSI reference model. Discuss how the TCP-IP reference model is workable with less number of layers compared to OSI reference model. (20)
- (b) What do you mean by public key cryptography? Describe with example. What are the advantages of public key cryptography over symmetric key cryptography? (13 2/3)
- (c) How can you distribute public and private keys through certification? (13)
  
2. (a) How is flooding as a means of routing packets? Explain the advantages and disadvantages. (15)
- (b) Consider the subnet shown in Fig. 2(b). Distance vector routing (10)

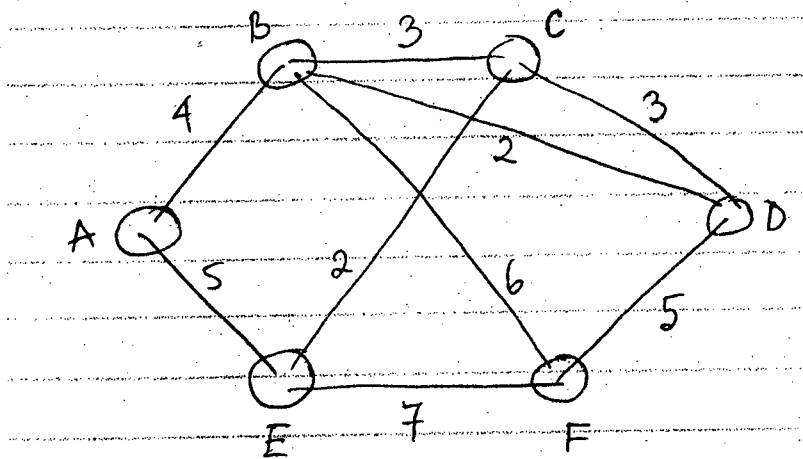


Fig 2(b)

is used and the following vectors have just come to router D.

B (6, 0, 11, 10, 5, 7)

C (5, 2, 0, 8, 3, 9)

F (8, 5, 4, 9, 7, 0)

The number shown on the links are the measured delays between two routers. Give the outgoing line to be used as well as the expected delay from router D.

- (c) Show that the hierarchical routing saves the memory for routing tables and searching time in routing packets. (9 2/3)
- (d) Describe how pruning is done in multicast routing if distance vector routing is used as routing algorithm. (12)

**CSE 321**

3. (a) Introduce leaky bucket and token bucket algorithm. How can you relate these algorithms with traffic shaping in IP networks? (15)
- (b) A computer on a 6 Mbps network is regulated by a token bucket. The token bucket is filled at a rate of 1 Mbps. It is initially filled to capacity with 8 megabits. How long can the computer transmit at the full 6 Mbps? (10)
- (c) What are the main reasons of fragmentation? How can handle fragmentation in IPV4? (11 $\frac{2}{3}$ )
- (d) Consider a IP packet with length 1 GB. Show the value of fields related to the packet length for this transmission. (10)
4. (a) Write short note on "Virtual Private Network". (13)
- (b) Consider a machine with domain name mango.buet.ac.bd is accessing a web server www.uvic.ca. Show the DNS resolution steps used in recursive and iterative techniques. (13)
- (c) Describe SMTP and POP3 protocol for email system with necessary examples. (13)
- (d) Describe quote-printable encoding in email system. (7 $\frac{2}{3}$ )

**SECTION - B**

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) For any code with 'm' message bits and 'r' check bits that allows all single bit errors to be corrected, it is required that  $(m+r+1) \leq 2^r$ . Show how this lower limit on the number of check bits 'r' is determined? Explain how hamming codes can be used to correct burst error of length 'k'? (10+8)
- (b) A bit stream 10101010101010 is transmitted using standard CRC method where the generator polynomial is  $(x^3 + x + 1)$ . Show the actual bit string transmitted. (12)
- (c) In the sliding window protocol using selective repeat, the maximum window size is  $(2^{n-1})$  where 'n' is the number of bits used for sequence numbers. Justify this restriction on the maximum window size with a suitable scenario. Explain how the Negative Acknowledgement (NAK) frame is used in the selective repeat protocol. (12+4 $\frac{2}{3}$ )
6. (a) Explain why Ethernet which runs CSMA/CD at the MAC layer enforces a minimum frame length and describe how this minimum length has been determined for 10 Mbps Ethernet. (8+5)
- (b) Why layer 2 Ethernet switches may need to run 'Spanning Tree Protocols'? Explain with an example scenario. Describe a scenario where it is preferred to use Virtual LAN (VLAN). (8+8)

Contd ..... P/3

**CSE 321**

**Contd ... Q. No. 6**

- (c) Using a suitable scenario explain how 802.11 (Wi-Fi) MAC protocol attempts to avoid collisions in the presence of hidden terminals using RTS/CTS mechanism. (9)
- (d) Consider 802.11 data frame format in the Figure for Q. 6(d). Note that in the frame, there are four address fields. Now describe a scenario where all four address fields are used. (8 $\frac{2}{3}$ )

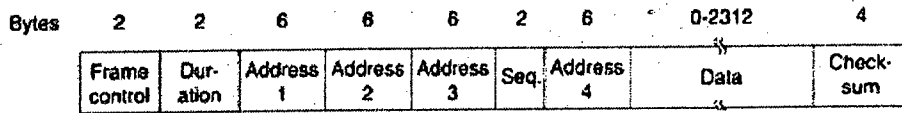


Figure for Question 6(d)

7. (a) Why is the starting sequence number of a TCP connection not always zero (0)? Explain with a suitable scenario. (12)
- (b) Why is it not desirable to send small size segments? Describe Nagle's algorithm for limiting small size segments from sender. Give example of an application for which Nagle's algorithm should be disabled. (4+4+4)
- (c) Describe TCP's acknowledgement policy. (10)
- (d) What is "symmetric connection release"? How does TCP implement "symmetric connection release"? Why does TCP wait in 'TIME WAIT' state before closing a connection during active close? (4+5+3 $\frac{2}{3}$ )
8. (a) Why is the timeout value of retransmission timer set dynamically in TCP? Describe Jacobson algorithm for calculating the timeout value (of retransmission timer) in TCP? What is the problem of updating RTT on retransmitted segments? (6+6+4)
- (b) Answer the following question in the context of TCP congestion control algorithm.
- (i) How 'congestion window' is updated during 'Slow Start' state and 'Congestion Avoidance' state? What is the intuition behind these two different update strategies? Explain. (3+5)
- (ii) What is the function of the variable 'Threshold'? (2)
- (iii) What are the two events that TCP uses to detect congestion? How do TCP's responses to these two events differ? What is the intuition behind such differences? (2+2+5)
- (c) It may be required to extend the size of the 'Sequence Number' field in TCP header with increasing network bandwidth. Explain. (5 $\frac{2}{3}$ )
- (d) Why do some applications prefer UDP over TCP as underlying transport protocol? Explain with an example application. (6)

L-3/T-2/CSE

Date : 17/12/2012

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations 2010-2011

Sub : **CSE 313** (Operating System)

Full Marks: 210

Time : 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks.

**SECTION – A**There are **FOUR** questions in this Section. Answer any **THREE**.

1. (a) Given that the maximum file size of combination of direct, single indirection, double indirection and triple indirection in an inode-based filesystem is approximately the same as a filesystem solely using triple indirection. Then why do not simply use only triple indirection to locate all file blocks? (10)
- (b) What is the maximum file size supported by a file system with 16 direct blocks, single, double, and triple indirection? Here the block size is 512 bytes and disk block numbers can be stored in 4 bytes. Locate the middle data block. (7+8=15)
- (c) How many pointers are there in a Buffer Header? Shortly describe the necessity of the pointers? (10)
2. (a) What is reference count and link count of an inode? [see iput algorithm in Fig. 2] (10)
- (b) Discuss a system implementation that keeps track of free disk blocks with a bit map instead of a linked list of blocks. What are the advantages and disadvantages of this scheme? (15)
- (c) Suppose you have a 700 MB CD-ROM. Do you think it is possible to store a 700 MB file in this CD-ROM? Explain your answer. (10)
3. (a) To maintain atomicity of buffer cache, we raise or lower processor execution level. Is it possible to avoid raising/lowering execution level using lock? If yes, describe how would you apply it for scenario 5 in getblk algorithm. [see getblk algorithm in Fig. 1.] (10)
- (b) Which part of getblk algorithm is responsible to maintain Least Recently Used structure in Buffer Cache? [see getblk algorithm in Fig. 1] (7)
- (c) Why is there the while loop in getblk algorithm? [see getblk algorithm in Fig. 1] (8)
- (d) Why size of a disk block is a critical issue? What are the problems if it is too large or too small? (10)
4. (a) Compare "Linked list allocation file system" and "Linked list allocation using a table in memory file system". (12)
- (b) How free disk blocks are managed in the free disk block list of a super block? (13)
- (c) Suppose all the processes are in "asleep" state. How it is possible that a process will wakeup and come to "ready to run" state? (10)

Contd ..... P/2

**CSE 313**

**SECTION - B**

There are **FOUR** questions in this Section. Answer any **THREE**.

5. The "Search-Insert-Delete" problem can be stated as follows:

Three kinds of threads share access to a file: *Searchers*, *Inserters* and *Deleters*. *Searchers* merely examine the list; hence they (Searchers) can execute concurrently with each other. *Inserters* add new items to the end of the list; insertions must be mutually exclusive to preclude two inserters from inserting new items at about the same time. However, one insert can proceed in parallel with any number of searches. Finally, *deleters* remove items from anywhere in the list. At most one *Deleter* process can access the list at a time, and deletion must also be mutually exclusive with searches and insertions.

(a) Write pseudocodes for Searchers, Inserters and Deleters that enforce this kind of three-way categorical mutual exclusion mentioned above using Semaphore and/or Mutex. (27)

(b) What do you mean by starvation? Does your solution of the "Search-Insert-Delete" problem result in any starvation? Briefly explain. (3+5=8)

6. (a) Write down two advantages of Micro-kernel architecture. (4)

(b) Write short notes on (5×3=15)

- (i) Remote Procedure Call (RPC)
- (ii) Upcall in Scheduler Activation
- (iii) System call implementation of Finite State Machine thread model.

(c) Given the following state for the Banker's Algorithm. There are 6 processes P0 through P5 and 4 resource types: A (15 instances); B (6 instances), C( 9 instances); D (10 instances). For the following current allocation and maximum need, should a new request (3, 2, 3, 3) from P5 be granted? (10)

Current Allocation					Maximum Need				
Process	A	B	C	D	Process	A	B	C	D
P0	2	0	2	1	P0	9	5	5	5
P1	0	1	1	1	P1	2	2	3	3
P2	4	1	0	2	P2	7	5	4	4
P3	1	0	0	1	P3	3	3	3	2
P4	1	1	0	0	P4	5	2	2	1
P5	1	0	1	1	P5	4	4	4	4

(d) What is memory segmentation? What are the benefits of using multiple segments? (3+3=6)



**CSE 313**

- 7. (a) Explain the architecture of a typical virtual machine. Write down some disadvantages of this approach. (7)
- (b) What are the disadvantages of implementing threads in kernel space solely? (6)
- (c) Verify whether the following code snippet solves the critical section problem for a two process environment. Two processes, say Process 1 and Process 2, running infinitely call **enter\_critical\_section** and **leave\_critical\_section** procedures with their corresponding ids before entering and after leaving the critical section respectively. (15)

```
Boolean blocked [2];
Int turn;

void enter_critical_section(int process_id)
{
    blocked[process_id] = true;
    while(turn != id) {
        while(blocked[1 - process_id]) {
            //do nothing
        }
        turn=id;
    }
}

void leave_critical_section(int process_id)
{
    blocked[id] = false;
}
```

- (d) Write down the address translation procedure for inverted page table scheme with its advantages. (7)
8. (a) Write down the conditions for occurrence of deadlocks. (8)
- (b) Consider the following workload: (5×3=15)

Process	Priority (Lowest number has the highest priority)	Burst Time (sec)	Arrival Time (sec)
P1	4	40	50
P2	3	70	10
P3	1	50	0
P4	5	100	0
P5	2	50	70

Draw the Time scale diagram and calculate the average waiting time for the following scheduling algorithms:

- (i) Non-preemptive Shortest Job First
  - (ii) Shortest Remaining Time First
  - (iii) Round Robin with quantum 30 sec.
- (c) Consider the following string of page references 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1. List the total number of page faults for the following page replacement strategies with frame size = 3 (12)
- (i) Optimal page replacement algorithm
  - (ii) First-in-first-out page replacement algorithm

```

algorithm getblk
input:  file system number
       block number
output: locked buffer that can now be used for block
(
    while (buffer not found)
    (
        if (block in hash queue)
        (
            if (buffer busy)      /* scenario 5 */
            (
                sleep (event buffer becomes free);
                continue;        /* back to while loop */
            )
            mark buffer busy;      /* scenario 1 */
            remove buffer from free list;
            return buffer;
        )
        else /* block not on hash queue */
        (
            if (there are no buffers on free list) /* scenario 4 */
            (
                sleep (event any buffer becomes free);
                continue; /* back to while loop */
            )
            remove buffer from free list;
            if (buffer marked for delayed write) { /* scenario 3 */
                asynchronous write buffer to disk;
                continue; /* back to while loop */
            }
            /* scenario 2 -- found a free buffer */
            remove buffer from old hash queue;
            put buffer onto new hash queue;
            return buffer;
        )
    )
)

```

Fig 1. getblk algorithm

```

algorithm iput /* release (put) access to in-core inode */
input:  pointer to in-core inode
output: none
(
    lock inode if not already locked;
    decrement inode reference count;
    if (reference count == 0)
    (
        if (inode link count == 0)
        (
            free disk blocks for file (algorithm free, section 4.7);
            set file type to 0;
            free inode (algorithm ifree, section 4.6);
        )
        if (file accessed or inode changed or file changed)
            update disk inode;
        put inode on free list;
    )
    release inode lock;
)

```

Fig 2. iput algorithm

L-3/T-2/CSE

Date : 24/12/2012

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations 2010-2011

Sub : **CSE 301** (Mathematical Analysis for Computer Science)

Full Marks : 210

Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

**SECTION - A**There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) Argue in favour of the recurrence relations Josephus number  $J(n)$  satisfies. Compute  $J(25321)$ . (10+5=15)
- (b) Write down an algorithm for solving <sup>Multi</sup> Multi Peg Tower of Hanoi (MPTOH) problem based upon presumed optimal solution strategy. Show the solution of the problem for  $(n, p) = (361, 8)$  in a binary tree. (10+10=20)
2. (a) There is a roulette wheel with 10,000 slots, numbered 1 to 10000. Assume that if the number that comes up on a spin is divisible by the floor of its 4th root then it is a winner and the house pays \$ 7 and otherwise it is a loser and the player must pay \$ 1. Can we expect to make money if we play this game? (15)
- (b) Discuss how analysis of average performance of quicksort can be done using summation factor. (20)
3. (a) Deduce how many 0s are there in decimal representation of  $600!$ ? (15)
- (b) Construct combinatorial arguments in favour of the equations (10+10=20)
- $$\sum_{0 \leq k \leq m} \binom{k}{n} = \binom{m+1}{n+1} \quad \text{and} \quad \sum_{k \leq m} \binom{n+k}{k} = \binom{n+m+1}{n+1}$$
4. (a) Prove the inversion formula. Use this formula to compute number of derangements on  $n$  distinct objects. (5+10=15)
- (b) Argue in favour of the recurrence Stirling's numbers of the first and second kinds satisfy. Deduce how large an overhang can be made placing  $n$  cards, each of length 2, on a table. (10+10=20)

**SECTION - B**There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) A football team, Cactus, wins a match with probability 0.75 irrespective of its opponents. What is the probability that the team wins 4 matches out of 5 matches? (5+5+5=15)
- In a knockout tournament, Cactus faces a series of opponents until it loses to someone. How many matches does Cactus expect to play before it gets eliminated from the tournament? If Cactus is already in Quarter final, what is the probability that it's going to play the Final and becomes Champion?

Contd ..... P/2

**CSE 301**

**Contd ... Q. No. 5**

(b) A laboratory blood test is 96% effective in detecting a certain disease when it is "in fact" present. However, the test also yields a "false" positive result for 5% of the healthy persons tested (that is, a healthy person, with 0.05 probability, would be detected to have the disease!). If 30% of the population actually has the disease, what is the probability that a person has the disease given that his test result is positive?

**(15)**

(c) Bangladesh Cricket team lost tosses for the last 5 games. As we know, tosses are done by a fair coin at each game; we can argue that in the next game there is a high chance that BD team is going to win the toss. Frankly speaking, if you lose consecutively, your chance of winning on the next attempt increases. What is the fallacy of this argument?

**(5)**

6. (a) A miner is trapped in a mine containing three doors. The first door leads to a tunnel that takes him to safety after two hours of travel. The second door leads to a tunnel that returns him to the mine after three hours of travel. The third door also does the same like the second door, but takes five hours in the tunnel. Assuming that the miner is all time equally likely to choose any of one of the doors, what is the expected length of time until the miner reaches safety?

What happens when the miner can remember which door he took earlier and does not take the same door again in the next attempt? What is the expected exit time then? **(10+10=20)**

(b) Let us consider a "simplified" version of a medium access scheme by a set of wireless hosts (the full version is widely known as IEEE 802.11 protocol). In principle, in a wireless medium only one host can transmit at a time. Each host senses the medium before it attempts to transmit a packet. If the channel is sensed free (none is transmitting), the packet is sent to the air immediately. Otherwise (i.e., if the channel is busy), the host waits for a while. In that, the host sets a counter to  $k$  (some constant) and then decrements the counter by 1 in each slot time (say, 100 ms) until the counter becomes zero. When the counter becomes zero, the host tries to access the channel again and the process continues.

**(15)**

Let  $p$  be the probability that the channel is sensed busy at any time. Now, construct a Markov chain to analyze this system. Define Markov states and associated transition probabilities. You can consider defining Markov states based on the number of slots the host needs to wait before attempting the medium access.

**CSE 301**

7. (a) Given the following transition probabilities for a Markov chain with three states; A, B and C –

(10)

	A	B	C
A	0.5	0.5	0
B	0.2	0.8	0
C	0	0.6	0.4

Answer the following:

- (i) Is there any transient state in this chain? If any, which one?
- (ii) Is this Markov chain Ergodic? Why?
- (iii) Try to compute long-run state probabilities for this chain. Can you argue the results?

(b) A software component for an embedded device is written with four code blocks—A, B, C and D (the flow is shown in Figure for Question 7(b)). Based on inputs and other conditions, the execution takes branching, and the associated branching probabilities are shown on the corresponding edges. Due to some implementation issues, the program produces "faulty" outputs when it executes code in block C. In other blocks, outputs are "good".

(10+15=25)

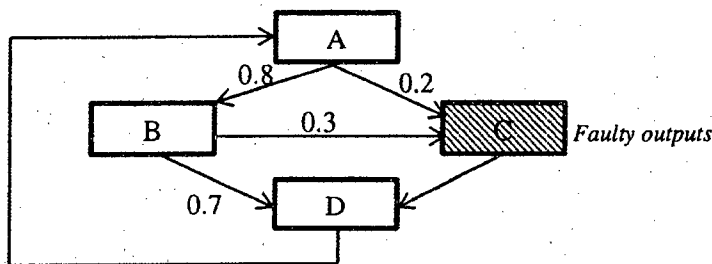


Figure for Question 7 (b)

Assuming that each code block executes 1 unit of time and the program executes in a continuous loop forever, construct the Markov chain associated with this software process along with the corresponding transition probability matrix. Hence, compute the following–

- (i) The rate at which faulty outputs are produced.
- (ii) The expected length of time the system produces consecutive good results.

**CSE 301**

8. (a) What is meant to be the Markovian property of a continuous-time Markov chain? (8)

(b) For a pure birth process (also known as Yule process) with an individual birth rate  $\lambda$ , argue that for a population with  $n$  individuals, the effective birth rate becomes  $n\lambda$ . (12)

(c) What do symbols in M/M/s queuing system stand for? For an M/M/1 queuing system (of infinite queue capacity) with arrival rate  $\lambda$  and service rate  $\mu$ , compute the limiting probabilities  $P_n$ , for  $n = 0, 1, 2, \dots$ , where: (15)

$P_n$  = steady-state probability that the system has exactly  $n$  customers

Hence, compute –

(i)  $L$ , the average number of customers in the system

(ii)  $L_Q$ , the average number of clusters waiting in the queue

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**SECTION – A**

There are **NINE** questions in this section. Answer any **SEVEN**.

1. You have designed a deterministic finite automaton (DFA) for a certain language from another nondeterministic finite automaton (NFA) using subset construction method. Do you think that the new DFA will accept/reject the same languages as the original NFA? Explain with necessary justification. (10)

2. Design a deterministic finite automaton which accepts the language consisting of strings from  $\{a, b\}^*$  and  $n \bmod 3 = 1$ , where  $n$  is the number of  $a$ 's in the string. (10)  
Depict the automaton using transition diagram as well as mathematical representation.

3. Convert the NFA shown below into an equivalent DFA using lazy evaluation. (10)

	0	1
$\rightarrow p$	$\{p, q\}$	$\{p\}$
$q$	$\{r, s\}$	$\{t\}$
$r$	$\{p, r\}$	$\{t\}$
$s^*$	$\emptyset$	$\emptyset$
$t^*$	$\emptyset$	$\emptyset$

4. Design a deterministic finite automaton which accepts the language consisting of strings from  $\{0, 1\}^*$  and the language does *not* contain the substring 110. (7+3=10)  
Now, show the regular expression for this language.

5. State and prove the pumping lemma. (10)

6. Using pumping lemma show whether the language  $L = \{0^m 1^n 0^n \mid m, n \geq 0\}$  is a regular language or not. (10)

**CSE 211**

7. Consider the grammar  $G = (V, \Sigma, P, S)$ , where  
 $V = \{a, b, S, A\}, \Sigma = (a, b),$  (10)  
 $P = \{S \rightarrow AA, A \rightarrow AAA, A \rightarrow a, A \rightarrow bA, A \rightarrow Ab\}.$   
 For any  $m, n, p > 0$ , describe with necessary explanation a derivation in  $G$  of the string  $b^m ab^n ab^p$ .
8. Consider the alphabet  $\Sigma = \{a, b, (, ), \cup, *, \emptyset\}$ . Use the rules (basic and inductive) for building regular expressions to construct a context-free grammar that generates all strings in  $\Sigma^*$  that are regular expressions over  $\{a, b\}$ . (10)
9. Give a context-free grammar for each of the following languages. (10)
- (a)  $L_1 = \{0^n 1^m 0^n \mid n, m \geq 0\},$   
 (b)  $L_2 = \{a^n b^m c^k \mid n, m, k \geq 0 \text{ and } n = m + k\},$   
 (c)  $L_3 = \{a^n b^m c^k \mid n, m, k \geq 0 \text{ and } n = 2m + 3k\},$   
 (d)  $L_4 = \{a^n b^m \mid 0 \geq n \geq m \geq 2n\}.$

**SECTION - B**

There are **FOUR** questions in this Section. Answer any **THREE**.

10. (a) Show that the set of all infinite binary sequence is uncountable. (4)  
 (b) Using the findings of Question 10(a), prove that some languages are not Turing-recognizable. (8 1/3)  
 (c) Prove that a language is decidable if and only if both the language and its complement are Turing-recognizable. (7)  
 (d) Give a formal description of the halting problem. Give an example of a language that is not Turing-recognizable. (4)
11. (a) Describe equivalent single tape Turing machines that can be used to completely simulate the following variants of Turing machines. (3×5=15)
- (i) Multi-tape Turing machine,  
 (ii) Non-deterministic Turing machine with a single-tape,  
 (iii) Turing machine with two-dimensional tape stretched to infinity in all directions.
- (b) Describe a Turing machine that decides the following language: (8 1/3)

$$L = \{a^{2^n} b \mid n \geq 0\}$$

Show the state diagram of the machine. Show the sequence of configurations of the machine for the input string  $aaaab$ .



**CSE 211**

12. (a) What is the difference between Turing-decidable and Turing-recognizable languages? What are the three conditions that must be met by a Turing Machine  $M$  if it is to recognize a string  $w$  of a language  $L$ ? (4)

(b) What does the following Turing machine do? (3)

$$\triangleright R \xrightarrow{a \neq \sqcup} R \xrightarrow{b \neq \sqcup} R_{\sqcup} a R_{\sqcup} b$$

Do the Turing machines  $LR$  and  $RL$  always automate the same way? Explain.

(c) Prove that if a PDA recognizes some language  $L$ , then  $L$  is context free. (11)

(d) Give an informal description and state diagram for the PDA that recognizes the following CFG: (5 1/3)

$$\begin{aligned} S &\rightarrow TX \\ T &\rightarrow 0T0 \mid 1T1 \mid \#X \\ X &\rightarrow 0X \mid 1X \mid \epsilon \end{aligned}$$

where the starting symbol is  $S$ .

13. (a) Formally describe a PDA that recognizes the following language: (8)

$$L = \{w \in \{0, 1\}^* \mid w = w^R\}$$

(b) Convert the PDA derived in Question 13(a), into an equivalent CFG following standard rules of conversion. (7 1/3)

(c) Automate the following PDA for the input  $1001$  and  $0101$  separately. What does the PDA do? (8)

