Single Phase Switch Mode Cycloconverters

by

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It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma and that all sources are acknowledged.

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Dedication

To my parents.

Acknowledgement

First of all, I would like to thank Allah for giving me the ability to complete this thesis work.

I would like to express my sincere gratitude to my supervisor, Dr. Mohammad Ali Choudhury. This thesis would not have been completed without his support and guidance. His constant encouragement gave me the confidence to carry out my work.

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ABSTRACT

This thesis proposes new single phase cycloconverters based on switch mode topologies. Boost, Buck-Boost and Ćuk switch mode schemes are employed to control the output voltages. The proposed cycloconverters provide control in terms of both frequency and amplitude of the output voltage. The design of the proposed circuits is divided into two steps. First, the input AC signal is made unidirectional by employing full bridge rectifier. Based on the requirement of frequency and amplitude of the voltage at the load, this unidirectional voltage either applied on the same side or on opposite side of the load. The proposed topologies consist of two SMPS based converters namely the P and the N converters that are connected across the load. Input AC chopping at high frequency provides switched AC current that requires small filter to make the current waveform nearly sinusoid and in phase with input voltage. As a result, the input current THD reduces and the power factor improves. High frequency switch mode conversion for both positive and negative cycles of the input signal achieves this goal. Switch mode schemes in the P and N converters provide high frequency switching of the input current and thereby ensuring low input current THD and high input power factor which are the two desirable power quality criteria for power electronic converters.

Compared to conventional 8 SCR cycloconverters the proposed topologies are able to provide output voltages both higher and lower than the supply. Depending on the load demand it is possible to offer output frequencies higher or lower than the input signal. Moreover, the proposed topologies have reduced number of switches. The numbers of solid state switches for each converter are two and in total each of the proposed topologies consist four switches. This reduction of switches has incorporated some advantages in the switch mode cycloconverters. First, the reduction of switch count has reduced the switching losses. Consequently the efficiency of proposed converters is increased. Second, less number of isolation schemes will be required in the proposed circuits. Third, the number of signal drives is reduced and finally, the proposed topology has higher reliability as the number of switches is reduced.

The control scheme employed here is the open-loop sliding control. This scheme directly controls the gate pulses of the solid state switches without any current sensing and feedback. Compared to the reported cycloconverter control schemes that involve complex algorithms requiring current sensing and feedback, the proposed control schemes provides simplicity and improved reliability of operation. Results are obtained for standard metrics like, input current total harmonic distortion, input power factor and energy conversion efficiency. The obtained results showed that the proposed schemes are able to provide AC-AC conversion at high efficiencies maintaining low input current THD and high input power factors along the range of the duty cycle of the control signal.

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LIST OF ABBRAVIATIONS

APF	**:**	Active Power Filter
DM	**:**	Delta Modulation
DVM	**:**	Dynamic Voltage Restorer
FC	**:**	Frequency Changers
FCC	**:**	Forced Commutated Cycloconverter
GF	**:**	Group Frequency
HFAC	**:**	High Frequency Alternating Current
ICC	**:**	Integral Cycle Controller
IGBT	**:**	Insulated Gate Bipolar Transistor
IGR	**:**	Intergroup Reactor
PF	**:**	Power Factor
PWM	**:**	Pulse Width Modulation
SCR	**:**	Silicon Controlled Rectifier
SFC	**:**	Static Frequency Changer
SMPS	**:**	Switch Mode Power Supply
SVM	**:**	Space Vector Modulation
THD	**:**	Total Harmonic Distortion
TRIAC	**:**	Triode Alternating Current
UPFC	**:**	Unified Power Quality Conditioner
VSCF	**:**	Variable Speed Constant Frequency

LIST OF SYMBOLS

V_s, V_{in}	:	Input Voltage
f_s, f_i	:	Input Frequency
α	:	Firing Angle
f_o	:	Output Frequency
V_d	:	DC Output of Each Rectifier
V_{out}, V_L, V_{Load}	:	Output voltage
I_{cc}	:	Circulating Current
v_r	:	Reference voltage
e	:	Error Signal
E_{GF}	:	Efficiency Factor
D	:	Duty Cycle of the Control Signal
I_s, I_{in}	:	Input Current
T	:	Thyristor Switches
S	:	IGBT Switches
η	:	Overall Efficiency
ϕ	:	Phase of Supply Voltage
I_d	:	Unidirectional Converter Current
i_r	:	Reference current
H	:	Hysteresis Band of Error Signal
E	:	Quantized Error Signal
N_{GF}	:	Number of Group Frequencies
N_f	:	Total Number of Frequency Components
$\emptyset$	:	Power Factor Angle
PF_{in}	:	Input Power Factor

CHAPTER 1
INTRODUCTION

1.1 Cycloconverters

A cycloconverter is a static frequency changer (SFC) designed to convert constant voltage, constant frequency AC to variable voltage variable frequency AC without any DC link. A cycloconverter is a naturally commutated SFC capable of bidirectional power flow. Because of the omission of DC link, its efficiency is higher than other frequency changers (FCs). The idea of these converters were proposed by Hazeltine in 1926 [1], and the first cycloconverter was built in 1930s using mercury arc valves for converting standard 50Hz AC to 15, 16.5 and 25Hz AC and were used for traction drives [2]. The majority of cycloconverters are naturally commutated and the maximum output frequency is limited to a value that is only a fraction of the source frequency.

Practical and commercial cycloconverters were not available till thyristors were developed in 1960s [3]. Its size is limited by the availability of the rating of thyristors. Cycloconverters can be classified according to its input and output phases as, single phase to single phase, three phase to single phase, and three phase to three phase cycloconverters. Moreover, there are two main structures available for cycloconverters namely, circulating free and circulating current cycloconverter. Major applications of cycloconverters are low-speed ac motor drives usually above 1 MW with frequencies from 0 to 20 Hz. With the advent of thyristors of high power rating and development of microcomputer/ microcontroller control strategies, cycloconverters are being used in heavy industries like rolling mills [4-6], electric traction [7], cement tube mill drive industries above 5 MW [8-10], wind tunnel fan drives [11], and ship propellers [12, 13], etc. [14].

The traditional cycloconverter requires a large number of thyristors, at least 36 and usually more for good motor performance, together with a complex control circuit, and it has some performance limitations, for satisfactory operation of the converter the realistic upper limit of the output frequency is about one third of the input frequency [15]. Cycloconverters deliver averaged sinusoidal output waveform which results low pulsating torque in rotary loads. Their input current is distorted and its Fourier series involves harmonics which include, a) higher order harmonics [7], b) sub-harmonics [16], and c) nonstandard

harmonics [2], [17]. Cycloconverter output voltages also involve harmonics and sub-harmonics. As a result, the control strategy must be chosen in a way to limit these harmonics and minimize their effect on output voltage. Generally, harmonic behavior of cycloconverters is dependent on their pulse number, structure and switching strategy. The higher the pulses number the better the cycloconverter performance [18]. Circulating current cycloconverters have better harmonic performance compared to the circulating current free cycloconverters [19].

The conventional methods of filter [20] cannot be used to reduce harmonics in cycloconverters. Different control strategies widely influence cycloconverter harmonic behavior. The change of a control strategy may result in the change of the input currents, and further, the electric power quality in the supply feeder. Several control strategies have been developed so far including cosine-wave control [2], ripple voltage integral feedback control [3], current feedback method [18], integral and double integral control [21] etc. Various modulation techniques are also employed [22] to improve the quality of load voltage.

In this thesis, switch mode power supply (SMPS) converters are employed to control the output voltages. In each cycle of the input AC signal the voltage is made unidirectional by employing full bridge rectifier. Then, depending on the required frequency at the load, this unidirectional voltage either appears on the same side or on the opposite side of the load. To provide output voltages at opposite polarities two SMPS topology based converters (one p and one n converter) are connected across the load [23]. The proposed topology differs from the available circuits in two ways. Firstly, for single phase AC-AC conversion, SMPS topology based converters is employed instead of conventional eight SCR cycloconverter scheme, thereby, output voltage both higher and lower than the supply voltage is achievable by controlling the duty cycle of the SMPS converter. Secondly, in case of single phase AC supply, the p and n type converters have reduced number of switches. The reduction of switches has four advantages compared to conventional cycloconverter topologies. Firstly, it reduces the switching losses and thereby increases the efficiency. Secondly, the proposed circuits have to deal with less number of isolation schemes. Thirdly, the number of drives is reduced and finally, the proposed topology has higher reliability as the number of switches is reduced. The performance of the proposed topology is evaluated in terms of THD, input power factor, output voltage, output frequency and efficiency along the range of the duty cycle of the control signal.

1.2 Review of Literature

A cycloconverter consists of one or more pairs of back to back connected controlled rectifiers. The delay angles of those rectifiers are modulated so as to provide an AC output voltage at the desired frequency and amplitude to the load. The simplest three-phase cycloconverter, 3-pulse half-wave cycloconverter, consists of 18 thyristors. Higher pulse order systems are large and complicated and tend to be used for large loads such as applications of 1 MW or more.

A conventional cycloconverter is a naturally commutated converter with inherent capability of bidirectional power flow and there is no real limitations on its size which is otherwise restricted in the case of a thyristor inverter due to the size of commutating elements. Here the switching losses are considerably low, the regenerative operation at full power over complete speed range is inherent and it delivers a nearly sinusoidal waveform resulting in minimum torque pulsations and harmonic heating effects. It is capable of operation even with blowing out of individual thyristor fuse (unlike inverter) and the requirements regarding turn-off time, current rise time and dv/dt sensitivity of thyristors are low.

Based on the structure of the rectifiers used in cycloconverters, these converters are classified into half-wave cycloconverters and bridge cycloconverters. The three-phase 3-pulse half-wave cycloconverter is composed of three back to back connected half-wave rectifiers. Each rectifier contains a positive and a negative converter. It is common to use a 6-pulse half-wave cycloconverter to make the output voltage smoother. Six-phase transformers are required to provide voltages for a 6-pulse half-wave cycloconverter. Three-phase half-wave cycloconverters are often used as large motor drives such as rolling mills.

Another scheme is the bridge cycloconverter that consists of two back to back connected bridge rectifiers, called as a P converter and an N converter respectively. Single-phase bridge cycloconverters are extensively used in electric traction applications (e.g., output frequency is 25 Hz in the USA and 16.67 Hz in Europe). It is usual to use 12-pulse bridge cycloconverters to make the output voltage smoother. The 12-pulse bridge cycloconverter is composed of two series 6-pulse bridge cycloconverters. Their input voltages are provided from a ‘wye-delta’ transformer and a ‘wye-wye’ transformer, respectively [3]. The single-phase to three-phase cycloconverter induction motor drives can be used for a single-phase traction system. Control circuits for these devices are available in the literature [24].

Depending on the direction and continuity of current two major cycloconverter structures, non-circulating current or blocked mode and circulating current cycloconverters are considered.

Cycloconverters using high-frequency, self-controlled ac switches (e.g. IGBTs) are known as Matrix converters. For a 3 phase converter a matrix of nine switches is utilized where any input phase can be connected to any output phase. The switches are controlled by Pulse Width Modulation (PWM) to fabricate an output fundamental voltage whose amplitude and frequency can be varied to control an AC motor. Matrix converters offer the advantage over thyristor cycloconverters of being able to produce unity power factor (PF) line current. However, compared to PWM voltage-fed converters, the parts count is significantly higher.

The main limitations of the naturally commutated cycloconverters are limited frequency range (less than half of the input frequency) for sub-harmonic free and efficient operation and poor input displacement and power factor, particularly at low output voltages. However, with improved control techniques these problems are being overcome.

Significant developments have taken place in control, modeling, analysis, and application aspects of cycloconverter drives. The control strategies have been developed so far includes cosine-wave control [2], ripple voltage integral feedback control [3], current feedback method [18], integral and double integral control [21] etc. Various modulation techniques are also employed [22] to improve the quality of load voltage.

Cosine-wave modulation was first introduced by Pelly [2]. He mathematically proved that this modulation is the most suitable modulation in case of output voltage power quality and total harmonic distortion (THD) when applied to an idealized cycloconverter. This method produces an output voltage with fundamental amplitude proportional to the reference waveform amplitude. Although the method is severely used universally in motor drives, it has some serious limits when used in practice. The main limits are due to the production of sub-harmonics in output voltage. Sub-harmonics are non-standard harmonic (inter-harmonic) contents of a signal which have frequencies lower than the fundamental frequency.

Ripple voltage integral feedback was mainly developed to overcome classical cosine-wave sub-harmonics problem. This feedback attenuates sub-harmonics in cycloconverter output voltage. Current feedback is more popular than voltage feedback because of the simplicity of applying vector control. In the current feedback method the current signal is proportional

to the integral of the output voltage minus the back emf which is approximately equal to the wanted reference voltage. The current feedback and ripple voltage integral feedback operate the same way [25].

Many modulation technique based control strategies utilize carrier based PWM. For the cycloconverter, when the polarity of the output voltage is positive, the gate signals for the cycloconverter switches are the same as those for a conventional three phase full bridge inverter. On the other hand, when the polarity is negative, the gate signals for the cycloconverter switches can be obtained by reversing the PWM signals for the three phase inverter. To achieve this, it is essential to know the polarity of the secondary voltages which is difficult to sense as the AC voltage is high frequency with a high amplitudes due to the high switching noise.

To overcome the problem of PWM, digital control strategy based on space vector modulation (SVM) is proposed. In the control strategy, the three phase output line-to-line voltages are sampled and the Clark and Park transformations are applied to get the desired output. SVM has the advantages of low harmonics and a higher modulation index in addition to the feature of complete implementation with a digital signal processor [26, 27].

Delta modulation (DM) is simple and has characteristics advantageous to the operation of cycloconverters. These cycloconverters use high-frequency; self-controlled ac switches (e.g. IGBTs). To optimize the harmonics and improve the output, gate pulses to different IGBTs are modulated using Delta modulation technique. A delta modulator is a closed loop network consisting of a forward comparator and a feedback filter. Delta modulation [28] has become an established alternative to sine PWM for offering a sinusoidal output with low harmonic contents.

Cycloconverter today is a practical proposition in large power applications with synchronous or induction motors like gearless mill drive in cement industry [29-31], centrifugal pump and compressors [32], electric traction [33, 34], rolling mill [4, 35, 36], variable-speed constant frequency (VSCF) systems [37], static Scherbius drives [38, 39], mine winders [40], ship propellers [41] etc.

1.3 Objective

SMPS topology has the advantage to provide controllable output voltages. Moreover, employing high frequency switching enables the converter to chop the input current and thereby shifting the lower order harmonic components far apart from the fundamental. In the proposed topologies, the input AC is made unidirectional by employing full bridge rectifier at first. Afterwards, considering load frequency requirement this unidirectional voltage either appears on the same side or on opposite sides of the load. The output voltage amplitudes are controllable by the duty ratio of the high frequency switching pulse. Two SMPS topology based converters (one p and one n converter) are connected across the load to provide output voltages at opposite polarities [23]. The proposed topologies provide from the conventional eight SCR circuits in two ways. Firstly, output voltage both higher and lower than the supply voltage is achievable by controlling the duty cycle of the SMPS converters for single phase AC-AC conversion compared to conventional eight SCR cycloconverter scheme. Secondly, it has been possible to reduce the number of switches of the converters to four compared to eight SCR cycloconverters. The reduction of switches has four major advantages compared to conventional cycloconverter topologies. First, the efficiency has been improved as the switching loss is reduced. Second, the provision of isolation among switching pulses is simpler in the proposed scheme. Third, the number of required driving circuit is reduced and finally, the proposed topology has higher reliability due to less number of switches.

The objectives of this thesis are to investigate new single phase cycloconverter topologies that will provide controllable AC voltages both higher and lower than the input AC voltage at controllable frequencies. The target is to develop new cycloconverter topologies that will provide adjustable voltage and adjustable frequency AC with low input current total harmonic distortion (THD), high input power factor and maintain high efficiency. Design of switch mode cycloconverters with reduced switch topology (less than eight switches as required in 1-phase AC-AC SCR cycloconverter) will be proposed. The performance of the proposed topologies will be investigated and compared with conventional single phase 8-SCR cycloconverter. The outcome of this thesis will be new cycloconverter topologies to provide adjustable AC with low distortion and high input power factor at good efficiencies.

1.4 Outline of the Thesis

This thesis is organized as follows:

Chapter 1. Introduces the research work. It comprises an introduction on cycloconverters along with its application and circuit types. Afterwards it provides a review on some of the state-of-the-art control techniques for cycloconverters and their corresponding problems. Then it presents the motivation towards this thesis and a brief overview of the positive features of the proposed switch mode cycloconverters. The layout of this thesis is also presented in this chapter.

Chapter 2. Illustrates the types of cycloconverters based on their constructions. It explains the classification of cycloconverters based on criteria like, characteristics of energy conversion and method of current flow. Some newer types of cycloconverters presented in the literature are also briefly discussed.

Chapter 3. Discusses the control topologies reported in the literature. It analyzes the principle of different control schemes and their impact on the performance of the conventional cycloconverters. This chapter also presents the relative advantages and disadvantages of reported control schemes.

Chapter 4. Provides basic ideas of power quality parameters used to justify the performance of the proposed switch mode cycloconverters. It explains the impact of these parameters in maintaining desirable operation and presents the equations to determine these parameters.

Chapter 5. Presents the proposed Buck-Boost topology based cycloconverter. It describes the circuit, analyzes its operation and presents its performance under different load conditions.

Chapter 6. Demonstrates the proposed cycloconverter based on Ćuk topology. First the description of the proposed circuit is presented along with the analysis of its operation. Then it provides details on the performance of the proposed cycloconverter under different load conditions.

Chapter 7. Presents the proposed switch mode cycloconverter based on Boost topology. It describes the circuit configuration, analyzes its operation and presents its performance under different load conditions.

Chapter 8. Compares the performance of the proposed switch mode cycloconverters with conventional 8 SCR cycloconverter. First it analyzes the behavior of the conventional cycloconverter under different conditions of control and load. Then it presents the comparison of its performance with the proposed cycloconverters and shows the advantages of the proposed schemes compared to the conventional one.

Chapter 9. Concludes the thesis with a summary on the research. It also discusses the scopes for future development of the proposed switch mode cycloconverters.

CHAPTER 2
CYCLOCONVERTER TYPES

Literature has different types of cycloconverters based on their circuit constructions. These classifications can be performed based on characteristics like, criteria of signal conversion, method of current flow etc. There are some newer types of cycloconverter circuits like, matrix converter or single phase to three phase cycloconverters.

Different constructions of cycloconverter circuits have classified them in various types. Separate criterions can be set to discrete cycloconverters. Firstly, there is criterion of input to output signal conversion. The energy conversion types may be single-phase to single-phase, three-phase to single-phase, or three-phase to three-phase. Next, depending on the path or method of current flow cycloconverters can be classified in blocked mode and circulating current mode cycloconverters. Finally, some new cycloconverter circuits proposed in literature will be discussed.

2.1 Classification Based on Criterion of Energy Conversion

Cycloconverters are AC-AC variable frequency converters. Based on input and load connection architectures they can be classified in the following schemes.

2.1.1 Single-phase to Single-phase (1ϕ-1ϕ) Cycloconverter

The circuit of a 1ϕ-1ϕ cycloconverter is shown in Fig. 2.1. This converter consists of back-to-back connection of two full-wave rectifier circuits. Fig 2.2 shows the operating waveforms for this converter with a resistive load. The input voltage, V_s is an AC voltage at a frequency, f_i as shown in Fig. 2.2. Assume that all the thyristors are fired at α=0° firing angle, i.e. thyristors act like diodes.

Consider the operation of the cycloconverter to get one-fourth of the input frequency at the output. For the first two cycles of V_s, the positive converter operates supplying current to the load. It rectifies the input voltage; therefore, the load sees four positive half cycles as seen in Fig. 2.2(b). In the next two cycles, the negative converter operates supplying current to the load in the reverse direction. The current waveforms for the resistive load will have the same waveform as the voltage but only scaled by the resistance. When one of the converters operates the other one is disabled, so that there is no current circulating between the two rectifiers.

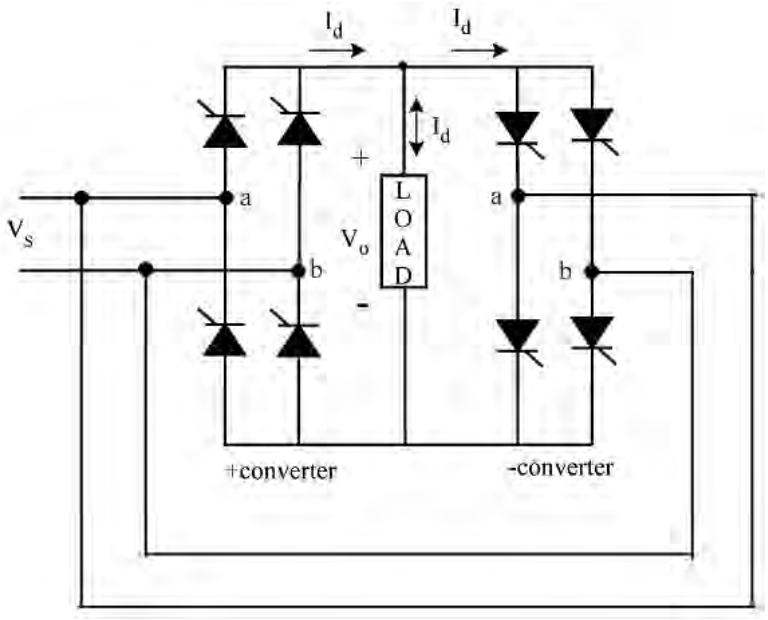

Fig. 2.1 Single-phase to single-phase cycloconverter

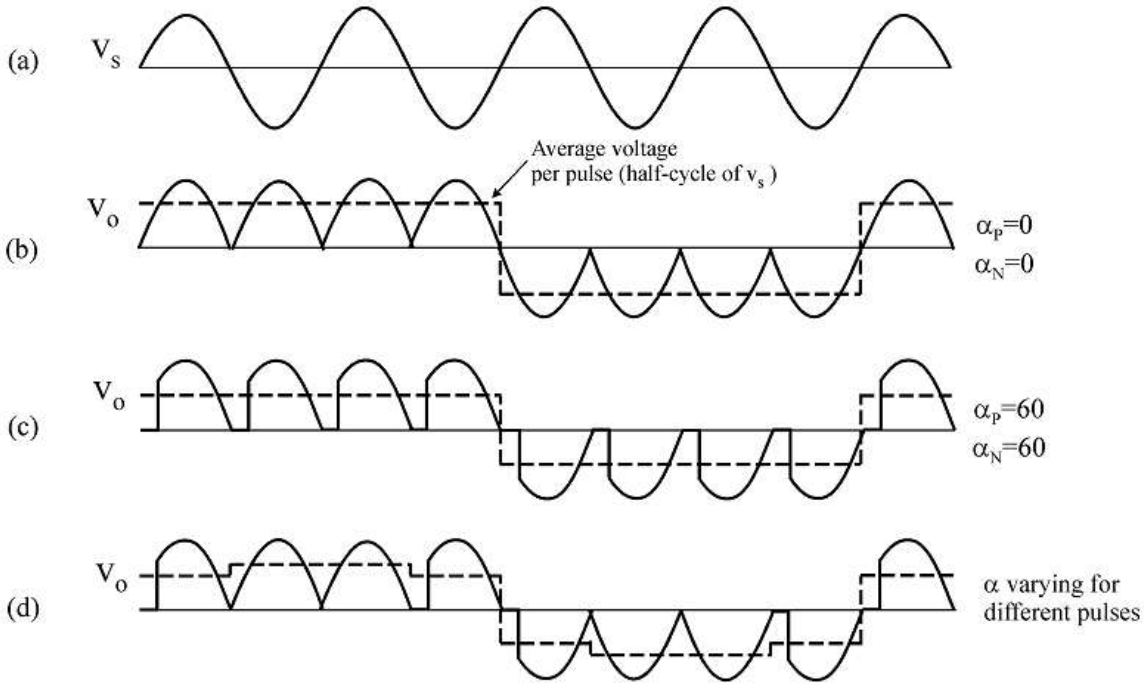

Fig. 2.2 Single-phase to single-phase cycloconverter waveforms. a) Input voltage, b) Output voltage for zero firing angle, c) Output voltage with firing angle $\pi/3$ rad, and d) Output voltage with varying firing angle

The frequency of the output voltage, V_o in Fig. 2.2(b) is four times less than that of V_s, i.e. $f_o/f_i=1/4$. Thus, this is a step-down in frequency cycloconverter. On the other hand, cycloconverters those have $f_o/f_i > 1$ frequency relation are called step-up frequency cycloconverters. Note that step-down cycloconverters are more widely used than the step-up ones.

The frequency of V_o can be changed by varying the number of cycles the positive and the negative converters work. It can only change as integer multiples of f_i in 1ϕ-1ϕ cycloconverters. With the above operation, the 1ϕ-1ϕ cycloconverter can only supply a certain voltage at a certain firing angle α. The DC output of each rectifier is:

$$V_d = \frac{2\sqrt{2}}{\pi} V \cos \alpha, \qquad 2.1$$

Where, *V* is the input root mean square (RMS) voltage. The DC value per half cycle is shown as dotted in Fig. 2.2(d). The peak of the fundamental output voltage is:

$$V_{o_{peak}} = \frac{4}{\pi}\frac{2\sqrt{2}}{\pi} \cos \alpha, \qquad 2.2$$

Equation 2.2 implies that the fundamental output voltage depends on α. By varying α, the fundamental output voltage can be controlled. Constant α operation gives a crude output waveform with rich harmonic content. The dotted lines in Fig. 2.2(b) and (c) show a square wave. If the square wave can be modified to look more like a sine wave, the harmonics would be reduced. For this reason α is modulated as shown in Fig. 2.2(d) where, the six-stepped dotted line is more like a sine-wave with fewer harmonics. The more pulses there are with different α's, the less are the harmonics.

2.1.2 Three-Phase to Single-Phase (3ϕ-1ϕ) Cycloconverter

There are two types of three-phase to single-phase (3ϕ-1ϕ) cycloconverters: 3ϕ-1ϕ half-wave cycloconverter as shown in Fig. 2.3 and 3ϕ-1ϕ full-wave bridge cycloconverter as in Fig. 2.4. Like the 1ϕ-1ϕ case, the 3ϕ-1ϕ cycloconverter applies rectified voltage to the load. Both positive and negative converters can generate voltages at either polarity, but the positive converter can only supply positive current and the negative converter can only supply negative current. Thus, the cycloconverter can operate in four quadrants: (+v, +i)

and (-v, -i) rectification modes and (+v, -i), and (-v, +i) inversion modes. Sinusoidal output voltage is possible to obtain by sinusoidally modulating the firing angle α.

The polarity of the current determines if the positive or negative converter should be supplying power to the load. When the polarity of the current changes, the converter previously supplying the current is disabled and the other one is enabled. The load always requires the fundamental voltage to be continuous. Therefore, during the current polarity reversal, the average voltage supplied by both of the converters should be equal. Otherwise, switching from one converter to the other one would cause an undesirable voltage jump. To prevent this problem, the converters are forced to produce the same average voltage at all times. Thus, the following condition for the firing angles should be met.

$$\alpha_P + \alpha_N = \pi \qquad 2.3$$

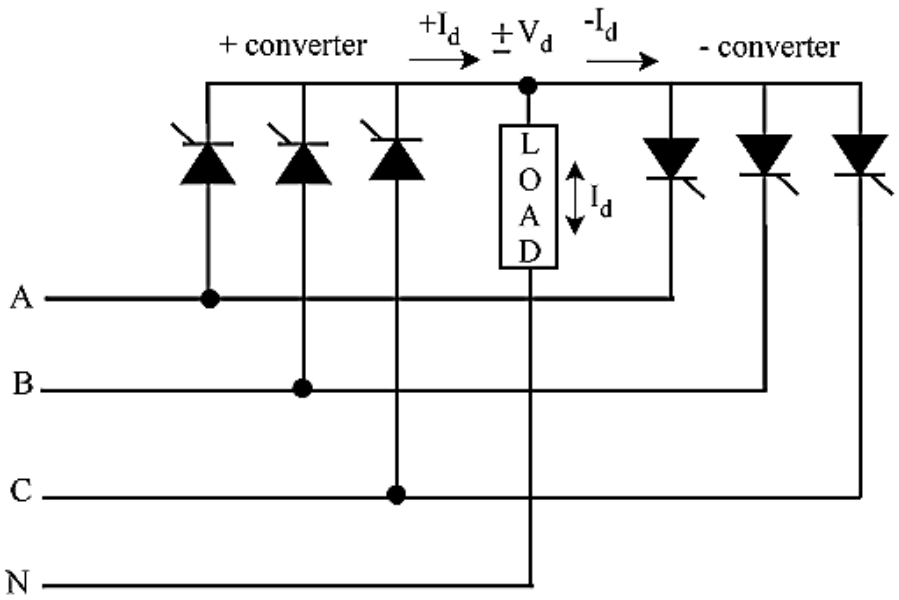

Fig. 2.3 3ϕ-1ϕ half-wave cycloconverter

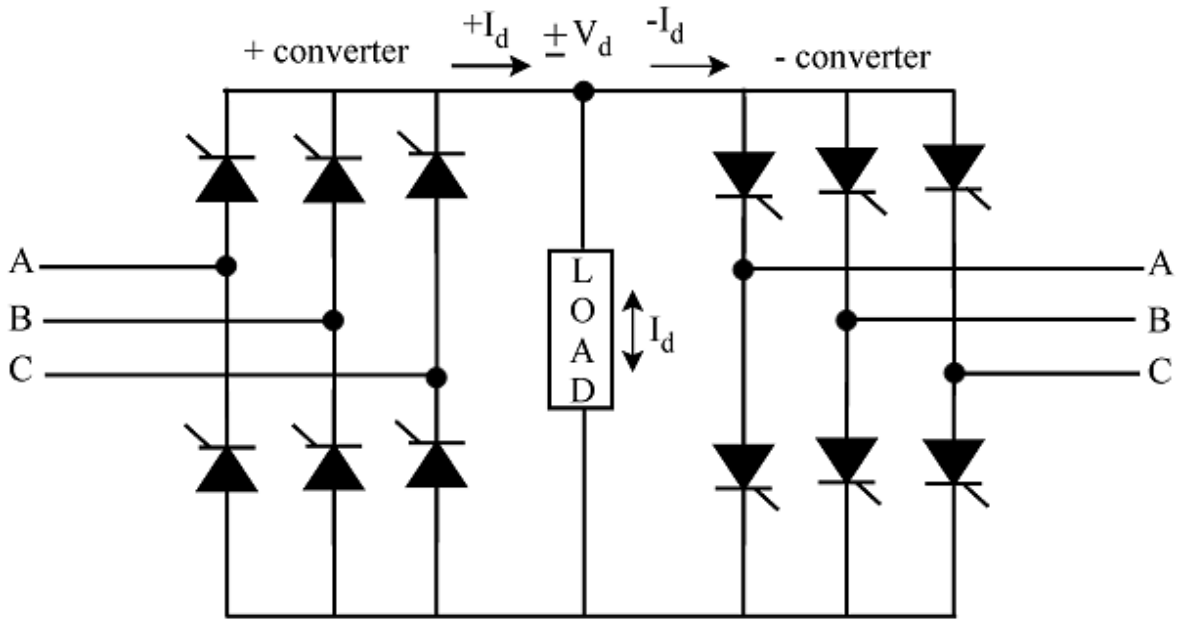

Fig. 2.4 3ϕ-1ϕ full-wave bridge cycloconverter

The fundamental output voltage can be given as:

$$V_{o1} = \sqrt{2}V_o \sin(2\pi f_o t) \qquad 2.4$$

Where V_o is the RMS value of the fundamental voltage and f_o is the fundamental output frequency. The operation of the 3ϕ-1ϕ full-wave bridge cycloconverter is similar to the above 3ϕ-1ϕ half-wave cycloconverter with the pulse number being doubled.

2.1.3 Three-Phase to Three-Phase (3ϕ-3ϕ) Cycloconverter

If the outputs of three 3ϕ-1ϕ converters of the same kind are connected in wye or delta and if the output voltages are 2π/3 radians or 120^o phase shifted from each other, the resulting converter is a three-phase to three-phase (3ϕ-3ϕ) cycloconverter. The resulting half-wave cycloconverter is shown in Fig. 2.5 and full-wave cycloconverter is shown in Fig. 2.6 with wye connected loads. If the three converters connected are half-wave converters, then the new converter is called a 3ϕ-3ϕ half-wave cycloconverter. If instead, bridge converters are used, then the result is a 3ϕ-3ϕ bridge cycloconverter.

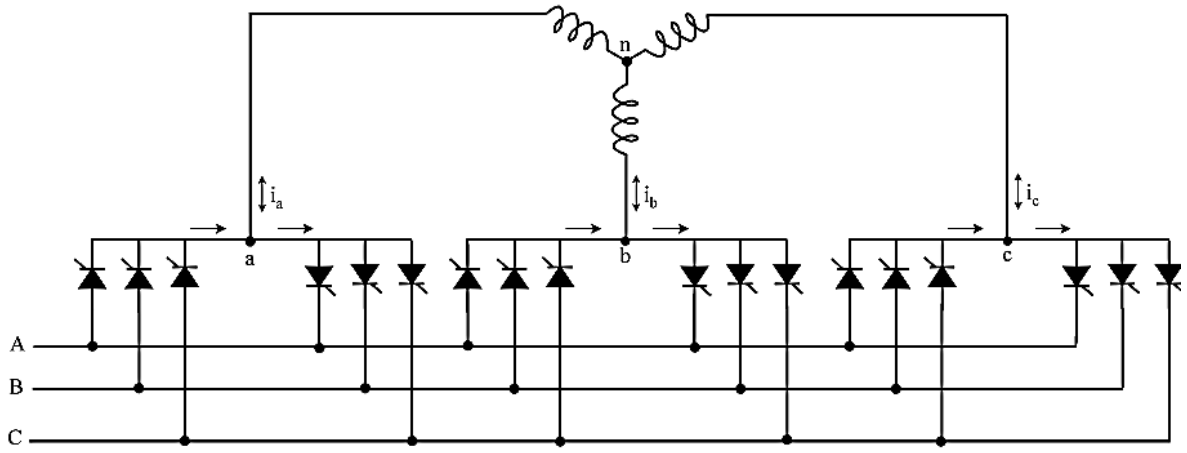

Fig. 2.5 3ϕ-3ϕ half-wave cycloconverter

3ϕ-3ϕ half-wave cycloconverter is also called a 3-pulse cycloconverter or an 18-thyristor cycloconverter. On the other hand, the 3ϕ-3ϕ bridge cycloconverter is also called a 6-pulse cycloconverter or a 36-thyristor cycloconverter. The operation of each phase is similar to 3ϕ-1ϕ cycloconverters except their load connections.

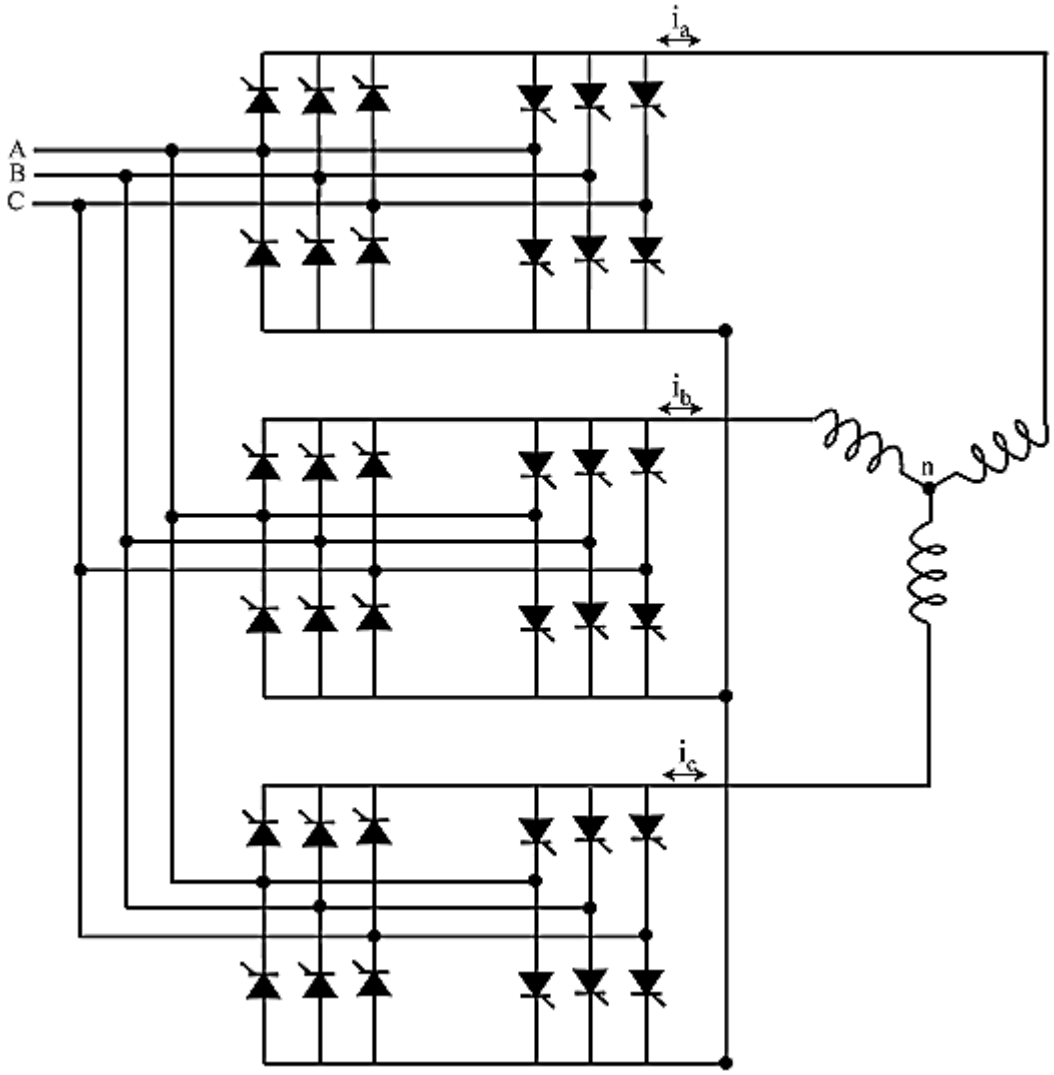

Fig. 2.6 3ϕ-3ϕ full-wave bridge cycloconverter

2.2 Classification Based on Method of Current Flow

Depending on the direction and continuity of current two major cycloconverter structures, non-circulating current or blocked mode and circulating current cycloconverters are considered.

During the positive load current, the positive converter supplies the required voltage and the negative converter is disabled. On the other hand, when the load current is negative, then the negative converter supplies the required voltage and the positive converter is blocked. This operation is called the blocked mode operation, and the cycloconverters using this approach are called blocking mode cycloconverters. However, if in any case, both of the converters are enabled, then the supply is short-circuited.

To avoid this short circuit, an intergroup reactor (IGR) can be connected between the converters as shown in Fig. 2.7. Instead of blocking the converters during current reversal, if they are both enabled, then a circulating current is produced. This current is called the circulating current. It is unidirectional because the thyristors allow the current to flow in only one direction. Some cycloconverters allow this circulating current at all times. These are called circulating current cycloconverters.

2.2.1 Blocking Mode Cycloconverters

The circuit for blocking mode operation of 3ϕ-3ϕ half-wave cycloconverter is shown in Fig. 2.5. The operation of these cycloconverters has been explained in section 2.1.1. They do not let circulating current flow, and therefore they do not need a bulky IGR. When the current goes to zero both positive and negative converters are blocked. The converters stay off for a short delay time to assure that the load current ceases. Then, depending on the polarity, one of the converters is enabled. With each zero crossing of the current, the converter, which was disabled before the zero crossing, is enabled. A toggle flip-flop, which toggles when the current goes to zero, can be used for this purpose.

The blocking mode operation has some advantages and disadvantages over the circulating mode operation. During the delay time, the current stays at zero distorting the voltage and current waveforms. This distortion means complex harmonics patterns compared to the circulating mode cycloconverters. In addition to this, the current reversal problem brings more control complexity. However, no bulky IGRs are used, so the size and cost is less than that of the circulating current case. Another advantage is that only one converter is in conduction at all times rather than two. This means less losses and higher efficiency.

2.2.2 Circulating Current Cycloconverters

The circuit diagram of Circulating current mode (3ϕ-3ϕ half-wave) cycloconverter and IGR is shown in Fig. 2.7. In this case, both of the converters operate at all times producing the same fundamental output voltage. The firing angles of the converters satisfy the firing angle condition of Eq. (3.3), thus when one converter is in rectification mode the other one is in inversion mode and vice versa. If both of the converters are producing pure sine waves, then there would not be any circulating current because the instantaneous potential difference between the outputs of the converters would be zero. In reality, an IGR is connected between the outputs of two phase controlled converters (in either rectification or inversion mode). The voltage across the IGR is the difference of the instantaneous output voltages produced by the two converters. It becomes zero when both of the converters

produce the same instantaneous voltage. The center tap voltage of IGR is the voltage applied to the load and it is the mean of the voltages applied to the ends of IGR, thus the load voltage ripple is reduced.

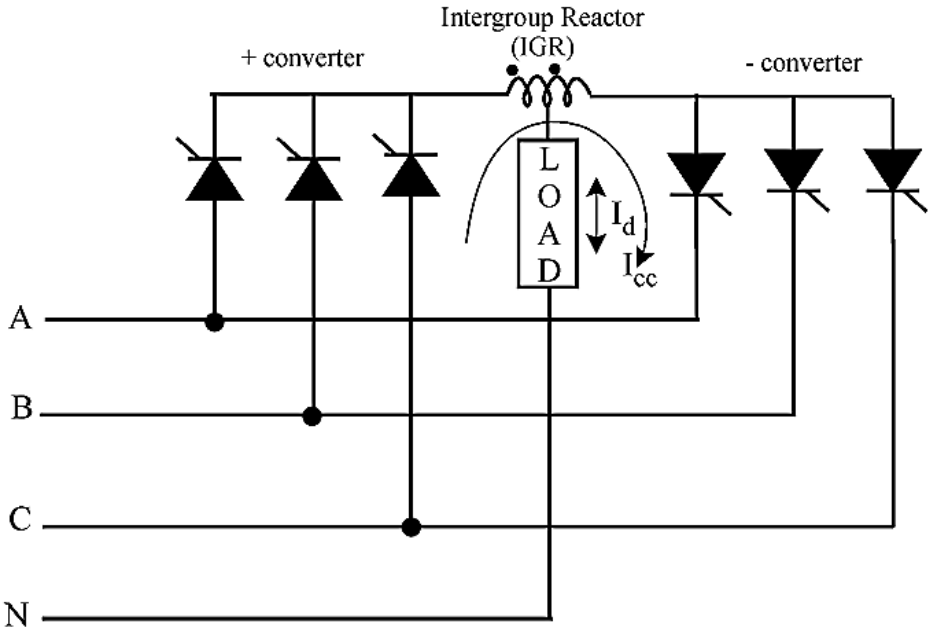

Fig. 2.7 Circulating current mode (3ϕ-3ϕ half-wave) cycloconverter and IGR

The circulating current cycloconverter applies a smoother load voltage with fewer harmonics compared to the blocking mode case. Moreover, the control is simple because there is no current reversal problem. However, the bulky IGR is a big disadvantage for this converter. In addition to this, the number of devices conducting at any time is twice that of the blocking mode converter.

The blocking and circulating current cycloconverters can be combined to give a hybrid system, which has the advantages of both. The resulting cycloconverter looks like a circulating mode cycloconverter circuit, but depending on the polarity of the output current only one converter is enabled and the other one is disabled as with the blocking mode cycloconverters. When the load current decreases below a threshold, both of the converters are enabled. Thus, the current has a smooth reversal. When the current increases above a threshold in the other direction, the outgoing converter is disabled. This hybrid cycloconverter operates in the blocking mode most of the time so a smaller IGR can be used. The efficiency is slightly higher than that of the circulating current cycloconverter but much less than the blocking mode cycloconverter. Moreover, the distortion caused by the blocking mode operation disappears due to the circulating current operation around zero current. Moreover, the control of the converter is still less complex than that of the blocking mode cycloconverter.

2.3 Newer Types of Cycloconverters

2.3.1 Matrix Converter

The matrix converter is a fairly new converter topology, which was first proposed in the beginning of the 1980s. A matrix converter consists of a matrix of 9 switches connecting the three input phases to the three output phases directly as shown in Fig. 2.8. Any input phase can be connected to any output phase at any time depending on the control. However, no two switches from the same phase should be on at the same time, otherwise this will cause a short circuit of the input phases. These converters are usually controlled by PWM to produce three-phase variable voltages at variable frequency.

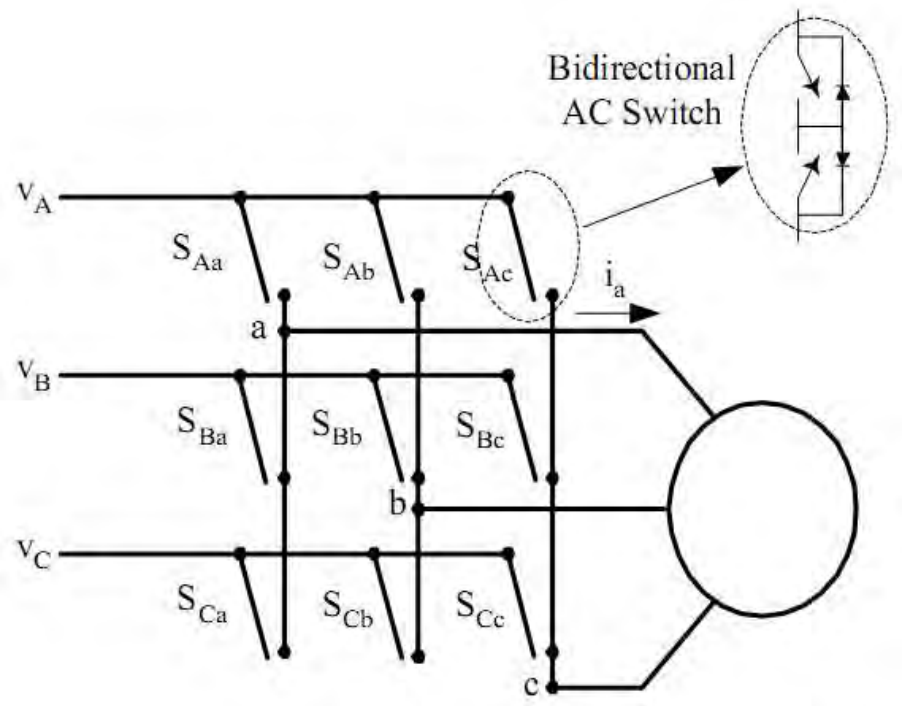

Fig. 2.8 Matrix Converter

This direct frequency changer is not commonly used because of the high device count, i.e. 18 switches compared to 12 of a DC link rectifier-inverter system. However, the devices used are smaller because of their shorter ON time compared to the conventional cycloconverters.

2.3.2 Single-Phase to Three-Phase (1ϕ - 3ϕ) Cycloconverters

Recently, with the decrease in the size and the price of power electronics switches, single-phase to three-phase (1ϕ - 3ϕ) cycloconverters started drawing more research interest. Usually, an H-bridge inverter produces a high frequency single-phase voltage waveform, which is fed to the cycloconverter either through a high frequency transformer or else. If a transformer is used, it isolates the inverter from the cycloconverter. In addition to this, additional taps from the transformer can be used to power other converters producing a high frequency ac link. The single-phase high frequency ac (HFAC) voltage can be either sinusoidal or trapezoidal. There might be zero voltage intervals for control purposes or zero voltage commutation. Fig. 2.9 shows the circuit diagram of a typical HFAC link converter. These converters are not commercially available yet. They are in the research stage. Different types of single-phase to three-phase (1ϕ - 3ϕ) cycloconverters are available in literature. Two special types of cycloconverters will be addressed here.

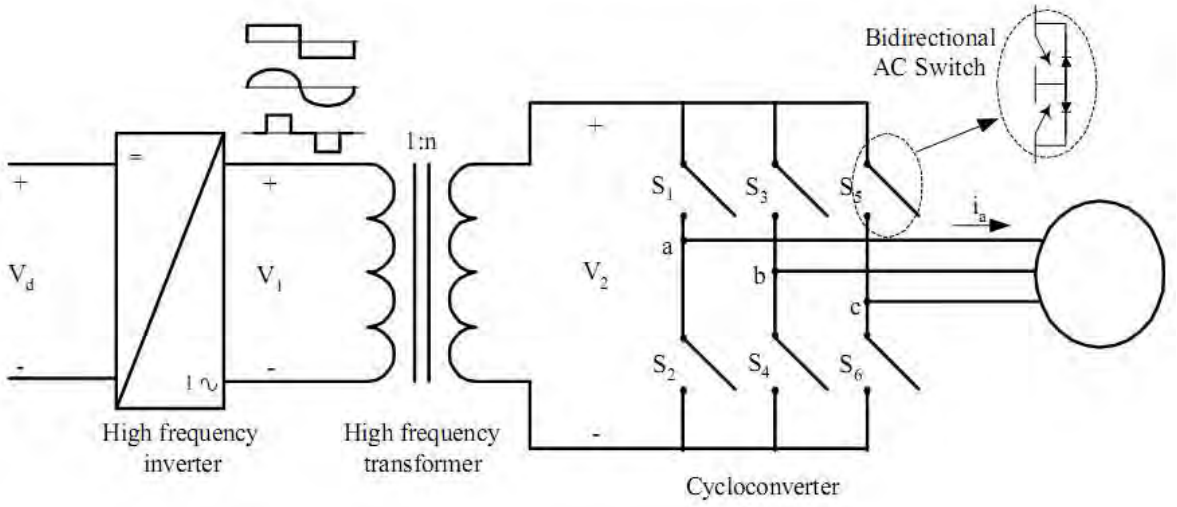

Fig. 2.9 High frequency AC link converter

A) Integral Pulse Modulated (1ϕ - 3ϕ) Cycloconverters [42]:

The input to these cycloconverters is single-phase high frequency sinusoidal or square waveforms with or without zero voltage gaps. Every half-cycle of the input signal, the control for each phase decides if it needs a positive pulse or a negative pulse using integral pulse modulation. For integral pulse modulation, the command signal and the output phase voltage are integrated and the latter result is subtracted from the former. For a positive difference, a negative pulse is required, and vice versa for the negative difference. For the

positive input half-cycle, if a positive pulse is required, the upper switch is turned on; otherwise, the lower switch is turned on.

The three-phase output voltage consists of positive and negative half-cycle pulses of the input voltage. This converter can only work at output frequencies which are multiples of the input frequency.

B) Phase-Controlled (1ϕ - 3ϕ) Cycloconverter [43]:

This cycloconverter converts the single-phase high frequency sinusoidal or square wave voltage into three-phase voltages using the phase control principles. The voltage command is compared to a saw-tooth waveform to find the firing instant of the switches. Depending on the polarity of the current and the input voltage, the next switch to be turned on is determined. Compared to the previous one, this converter has more complex control but it can work at any frequency.

Cycloconverters are widely used in industry for AC-AC conversion. With recent device advances, newer forms of cycloconverters are being developed. These newer forms are drawing more research interest now a day. In this section, the most commonly known cycloconverter schemes are briefly described, and their operation principles are discussed.

CHAPTER 3
CYCLOCONVERTER CONTROL SCHEMES

A cycloconverter control strategy refers to a set of firing signals that triggers cycloconverter thyristors to produce a specific output voltage. Different control strategies lead to different characteristics in input current and output voltage of cycloconverter. The control schemes deal with the regulation of cycloconverter outputs, input current shaping, dynamic performance, and efficiency etc. Various control schemes are presented in literature so far, some selective ones will be presented in this chapter. Among various phase control methods developed in the past, cosine wave crossing control has found widespread use. To overcome the limitations of cosine wave control, some correction methods like, regular sampling, ripple voltage integral feedback control and current feedback methods are employed. Integral phase control methods have also gained attentions because of their relative advantages over cosine wave control. Some control methods like, Space Vector Modulation (SVM), Delta Modulation (DM) and Group Frequency (GF) methods used for cycloconverter control are briefly described in this chapter.

3.1 Cosine Wave Control:

In the cosine wave crossing control method, the output reference wave is compared with cosine waves and when the two waveforms cross, the thyristors are triggered. The procedure is shown in Fig. 3.2 for a three phase three pulse cycloconverter as in Fig. 3.1. An example of an idealized output waveform for a 45° load phase angle with cosine wave control where the output load current is sinusoidal is shown in Fig. 3.3.

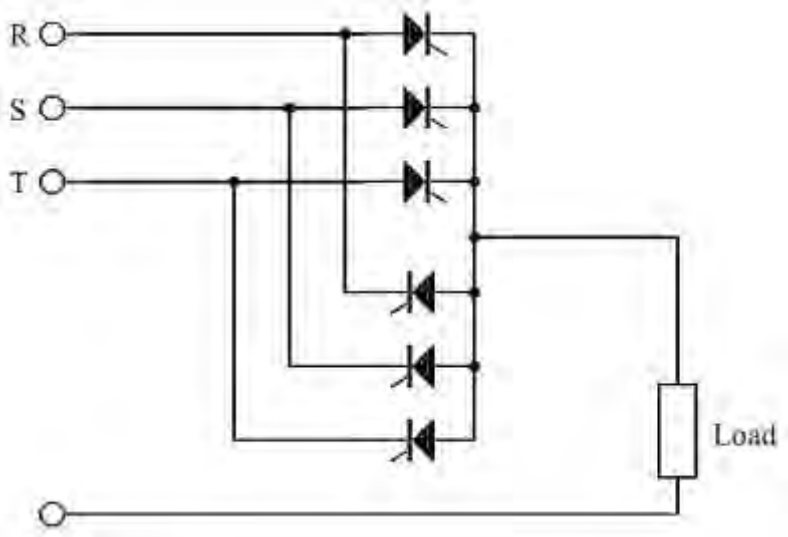

Fig. 3.1 Three phase, 3-pulse cycloconverter for cosine wave control

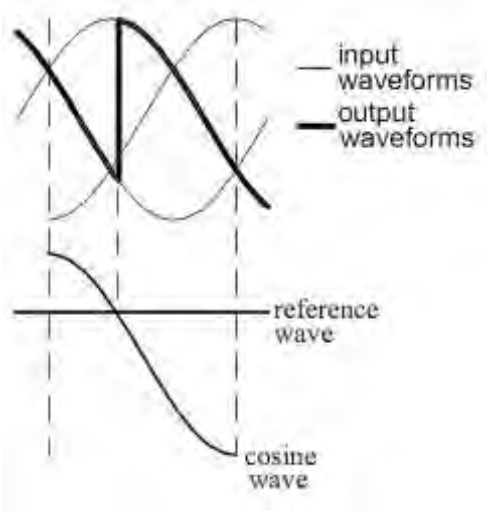

Fig. 3.2 Cosine wave crossing phase control method for 3 pulse cycloconverter

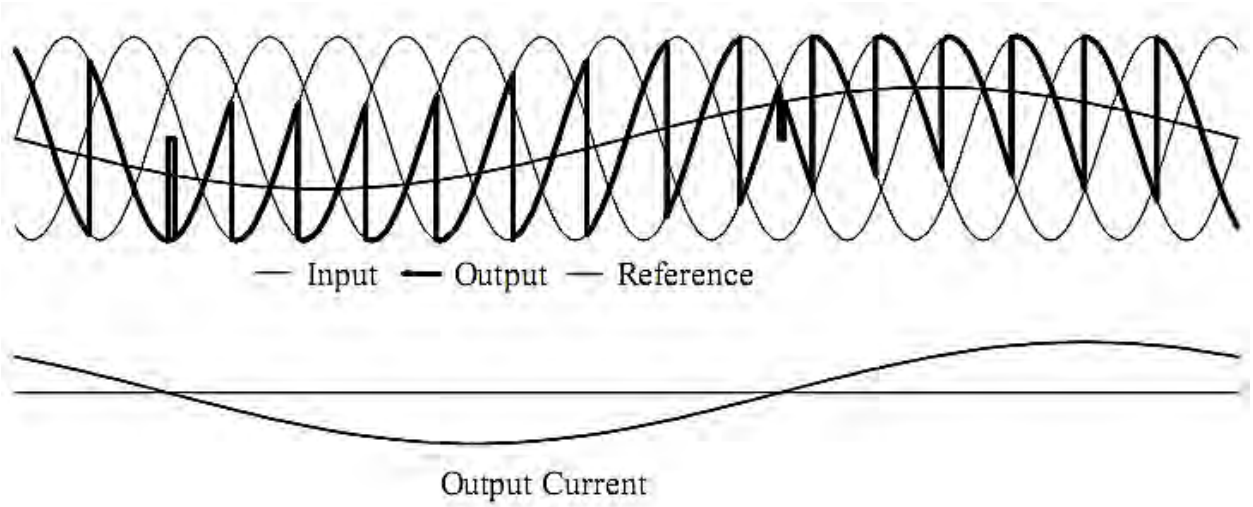

Fig. 3.3 Idealized waveforms with cosine wave control for a 3-pulse cycloconverter with 45° lagging load current

The cosine wave crossing control method was originally developed for DC output thyristor converters. For this application, the method produces an average output voltage which is directly proportional to the reference voltage for the idealized case of continuous output current. Cosine wave control is an open-loop control method which produces firing pulses based on wanted output voltage and modulation waves. Bock diagram [2] of this control method is depicted in Fig. 3.4. Pelly [17] showed that when applied to the idealized (continuous output current) cycloconverters, this method produces an output voltage whose fundamental component amplitude is proportional to the reference waveform amplitude and whose frequency spectrum contains no multiples of the fundamental components.

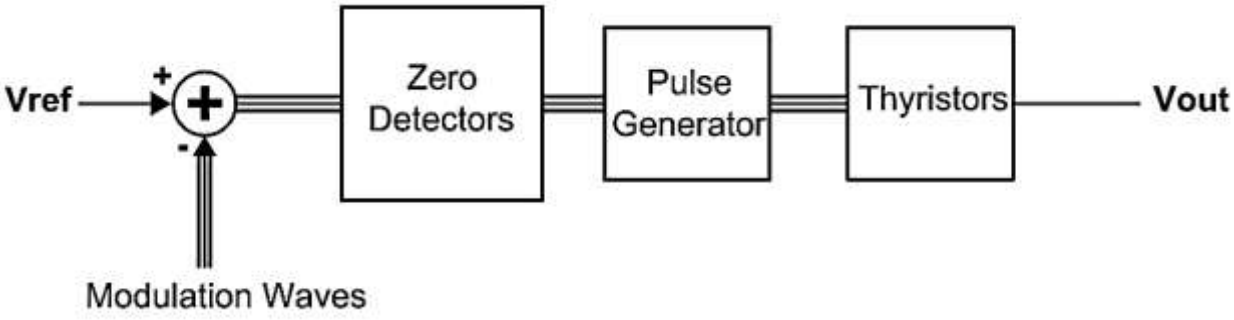

Fig. 3.4 Block diagram of cosine-wave modulation

Even though the cosine wave crossing control method is almost universally used for cycloconverter motor drives, the method has limitations. The main limitation is that the method generates intermodulation products on the output, the frequency of which may be less than the wanted output frequency. When this occurs, the intermodulation product is called a sub-harmonic.

For example, a 3-pulse cycloconverter which has an input frequency, f_i, of 50 Hz and a fundamental output frequency, f_o of 24 Hz can generate intermodulation products of frequencies ($3nf_i + mf_o$), where, n and m are integers. The intermodulation product, ($3f_i - 6f_o$), has a frequency of 6 Hz which is less than f_o and is thus a sub-harmonic. For cosine wave crossing control, assuming maximum output modulation and a load phase angle of 30° lagging, its amplitude is 9.5% of the fundamental [17, 21]. For an induction motor operating at a synchronous speed of 24 Hz, its impedance at 6 Hz would be very low and the currents and resulting torque pulsations produced from this sub-harmonic would be high.

Another major problem with cosine wave crossing control is the distortion produced from discontinuous output current. When the motor is operating under light load, the high ripple current may bring the output current in phase, turning off the conducting thyristor before the next thyristor turns on. The output voltage will then revert to the motor open circuit voltage rather than the input phase voltage, causing voltage distortion on the output. Cosine wave crossing control is not viable in this situation.

3.2 Correction Methods for Cosine Wave Crossing Control

There have been various techniques devised over the years to correct the deficiencies of the cosine wave crossing control method. Most commercial drives use one of these techniques. The important ones are described below.

3.2.1 Regular Sampling

The regular sampling method was developed by Bird and Ford [44] for circulating current cycloconverters. The method is to modify the reference waveform by doing a sample and hold at the start of each cosine wave. This was found to reduce the amplitudes of sub-harmonics on the output. Improved results could be obtained by pre-distorting the reference wave. This work also showed that this technique provides minimal improvement for circulating current free cycloconverters.

3.2.2 Ripple Voltage Integral Feedback

Ripple voltage integral feedback is a technique introduced by Gyugyi and Pelly [2]. It involves feeding back the integral of the difference between the output voltage and the reference voltage. A block diagram of this scheme is shown in Fig. 3.5. With this system, any low frequency sub-harmonics are attenuated by the feedback, the gain of which is inversely proportional to frequency. The feedback would also assist in reducing voltage distortion due to discontinuous current.

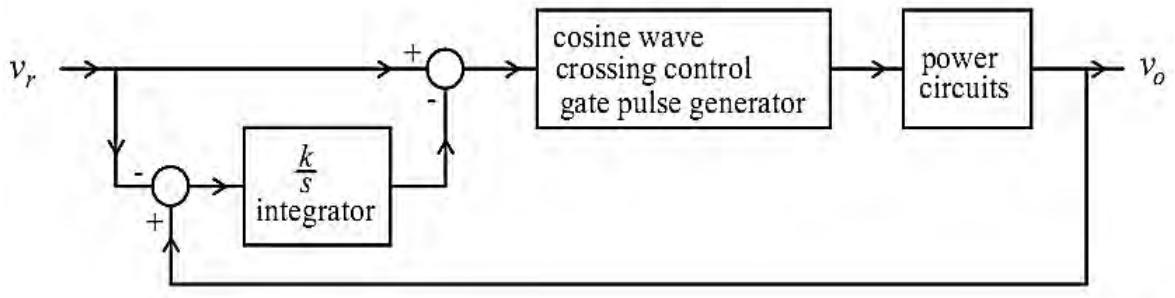

Fig. 3.5 Simplified block diagram of ripple voltage integral feedback control scheme

The limitation of this technique is that the maximum stable loop gain is rather low and is reduced as the maximum output frequency is increased. Table 3.1 shows the approximate maximum stable unity gain frequency of the feedback loop for a 50 Hz input frequency, 3-pulse cycloconverter for various output frequencies. This table is constructed from data presented by Gyugyi and Pelly [2].

TABLE 3. 1 Approximate maximum stable unit gain frequency of the feedback loop for a 50 Hz input frequency, 3-pulse cycloconverter

Output Frequency (Hz)	Unity Gain Frequency (Hz)
5.56	9.5
8.33	7
16.67	5.5
25	4.5
33.33	3.5

It is evident from Table 3.1 that, for a 3-pulse cycloconverter operating up to 25 Hz, the feedback gain is quite low and of limited benefit. Assuming that the loop gain drops off by 20 dB per decade, then at 6 Hz, the maximum gain is only 0.75, producing only a marginal reduction in a sub-harmonic at this frequency. A way of increasing the maximum stable unity gain frequency is to increase the pulse number. For a 6-pulse cycloconverter, the maximum unity gain frequency can be multiplied by 4, and for 12-pulse, by 16. Gyugyi and Pelly [2] demonstrated good results using this system for a 6-pulse cycloconverter operating up to 2/3 of the input frequency and driving a 30 HP induction motor.

3.2.3 Current Feedback Method

The most common commercial method of improving the output waveform is to consider the feedback of the output current. This method evolved from its use in thyristor controlled DC motor drives. A block diagram of current feedback control is shown in Fig. 3.6.

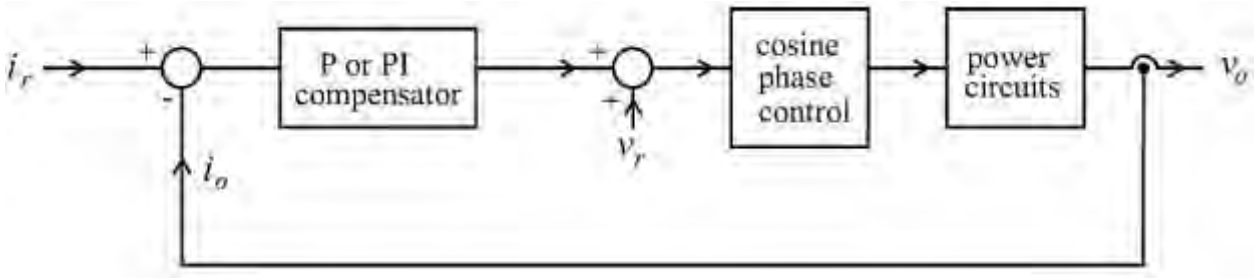

Fig. 3.6 Simplified block diagram of current feedback control scheme

In terms of feedback stability and gain, the current feedback system is virtually identical to ripple voltage integral feedback. The approximate equivalent circuit of the motor is a back e.m.f. in series with a leakage inductance, so the current signal is proportional to the integral of the output voltage minus the back e.m.f. which is approximately equal to the wanted reference voltage. This means that the maximum feedback gain without instability is similar to that which can be obtained from ripple voltage integral feedback. This limits the usefulness of current feedback to 6-pulse and higher cycloconverters. Even with 6-pulse cycloconverters, an estimate of the wanted output voltage must be added to the error voltage as shown in Fig. 3.6 to reduce the error in the output current.

Although there is little difference in performance between ripple voltage integral feedback and current feedback, current feedback is usually chosen in practice because it allows easier implementation of vector control.

3.3 Integral Control

Integral control is a seldom used method of phase control for the cycloconverter which was invented by Gyugyi, Rosa and Pelly [45]. The basic method is to trigger the next thyristor when the integral of the difference between the reference and the output voltage waveforms reaches zero. A block diagram of an integral control system is shown in Fig. 3.7. The difference between the reference voltage and the output voltage is fed to an integrator, the output of which is connected to a zero detector. The zero detector is used to advance a ring counter which turns on each thyristor in sequence in the conducting bank. The same circuit, or computer algorithm if implemented in software, can be used for both the positive and negative bank by reconnecting the outputs of the ring counter to the appropriate thyristors. The relevant waveforms for positive and negative load current for a 2-pulse cycloconverter are shown in Fig. 3.8.

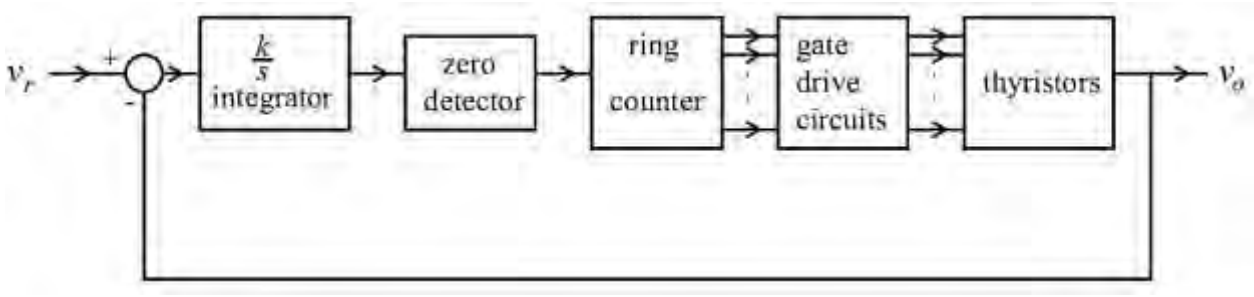

Fig. 3.7 Block diagram of integral control

A problem with the basic integral control method is that it can exhibit instability, an example of which is shown in Fig. 3.9. Several methods have been developed to suppress the instability without upsetting the integral control action [45-47].

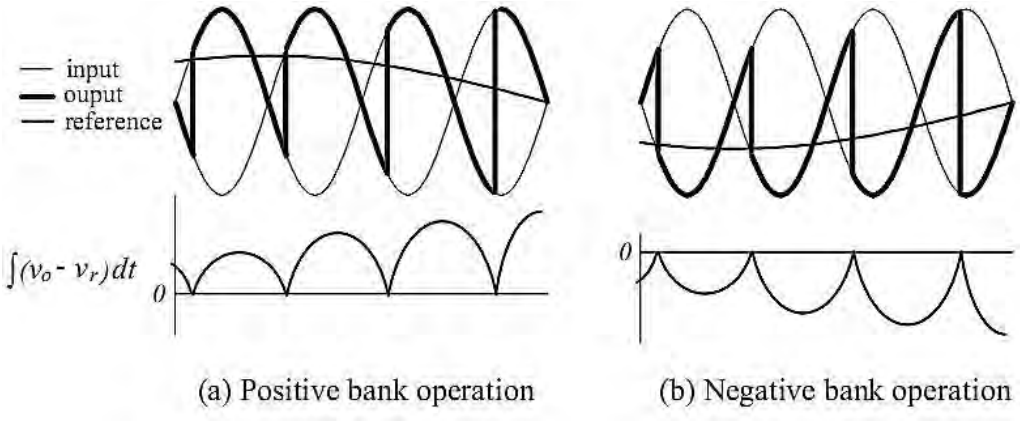

Fig. 3. 8 Waveforms obtained from a 2-pulse cycloconverter with integral control

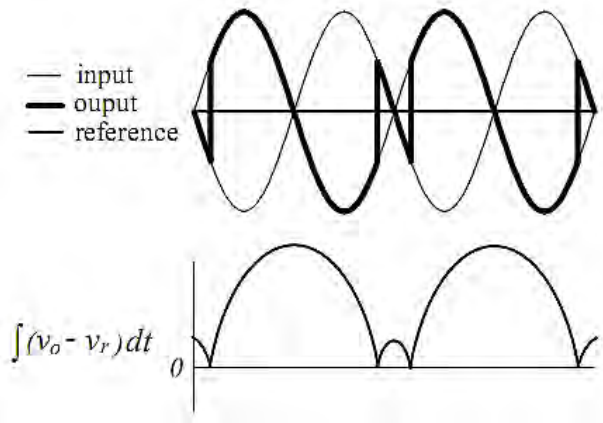

Fig. 3.9 An example of instability for a 2-pulse cycloconverter with integral control

3.4 Pre-integral Control

Pre-integral control is an interesting variation of integral control. It was developed for the 3-pulse cycloconverter [48] but can be applied to cycloconverters of any pulse number. Its operation is shown in Fig. 3.10. For each output phase, the output waveform is divided into periods called trigger periods, each of which contains only one thyristor switching instance. Each trigger period starts when the reference waveform crosses the input waveform which is currently connected to the output and ends when the reference waveform crosses the input waveform connected to the next thyristor to be turned on.

These start and end times are chosen because these are the limits within which the thyristor will always turn on. The thyristor is triggered on when it is estimated by computer calculation that the integral of the difference between the output and reference waveforms will be zero at the end of the current trigger period.

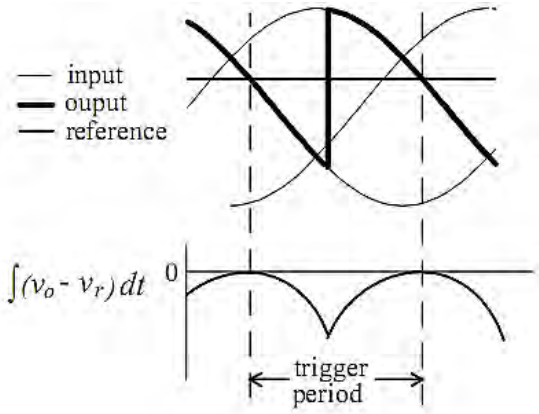

Fig. 3.10 Illustration of the pre-integral control method for positive load current

The advantage of pre-integral control over integral control is that it is inherently stable. The disadvantage is that a microprocessor is required to calculate the difference integral in advance. If the output current is discontinuous, as shown in Fig. 3.11, then the microprocessor must continually recalculate the turn-on time of the next thyristor up to when the thyristor is turned on because with no thyristor conducting, the output voltage cannot be determined in advance.

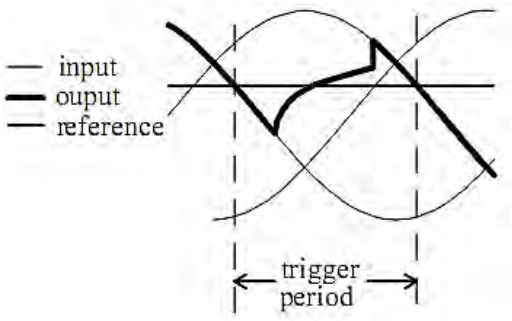

Fig. 3.11 Pre-integral control with discontinuous current

3.5 Double Integral control [21]:

In the integral control methods, it is important to keep the integral of the applied voltage as close as sinusoidal to keep the motor flux sinusoidal with minimum flux ripple. Cosine wave crossing control fails to meet this requirement because the voltage sub-harmonics generated in the output produce large deviations in the integral of its output voltage. Integral and pre-integral controls fail because they produce distorted voltage integral waveforms, although they do prevent sub-harmonic generation. The double integral control is developed directly from this basic requirement to keep the integral of the output voltage sinusoidal with minimum ripple thus ensuring that this condition is met.

The requirement here is to determine when to turn on each thyristor so that the integral of the output voltage is kept as close as possible to a reference voltage integral waveform which is normally sinusoidal. This pseudo flux is designated here as the integral of a reference voltage. The output is first divided into time periods called trigger periods which are the same as those used for pre-integral control. The advantage of having a trigger period which is synchronized to the mains is that it greatly reduces the calculations required to determine the TRIAC trigger instant.

The choice the trigger instant can be done over the time of one trigger period by choosing the trigger instant so that the average over a trigger period of the difference between the reference voltage integral and the integral of the output voltage is zero. This method has the ability to overcome the sub-harmonic generation problem with cosine wave control and distortion problems with integral control and pre-integral control.

3.6 Space Vector Modulation (SVM):

SVM is a pulse width modulation technique that is based on the space vector representation of the output voltages and input currents in the complex plane. SVM has the advantages of low harmonics and a higher modulation index in addition to the feature of complete implementation with a digital signal processor [26], [27]. For a three phase controllable rectifier incorporating cycloconverters SVM can yield high quality input currents with an almost unity power factor.

SVM based control technique for forced commutated cycloconverters (FCCs) is presented in [49] and [50]. In [49], with the allowable switching combinations, six output voltage space vectors with varying amplitudes can be obtained, in addition to the zero vector. The variation is compensated by adapting the standard modulation technique. The technique permits space vector synthesis of a three-phase, nonsymmetrical, non-sinusoidal output voltage, even under non-steady-state conditions, which is essential for the control of AC servo drives.

The resultant output line voltages and input phase currents under SVM technique do not contain low frequency harmonics. The input current displacement factor and the converter voltage gain can be freely varied, regardless of the load power factor. The only restriction in SVM is the equality of input and output active powers. The modulation technique holds for any input and output frequencies, so that it can be also applied for 3Φ AC to DC and DC to 3Φ AC conversion, thus making FCC a universal power conversion module.

3.7 Delta Modulation (DM) Techniques:

Delta modulation [28] has become an established alternative to sine PWM for offering a sinusoidal output with low harmonic contents. In order to optimize the harmonics and to improve the output of cycloconverter, gate pulses to different IGBTs are modulated using Delta modulation technique. A delta modulator is a closed loop network consisting of a forward comparator and a feedback filter as shown in Fig. 3.12.

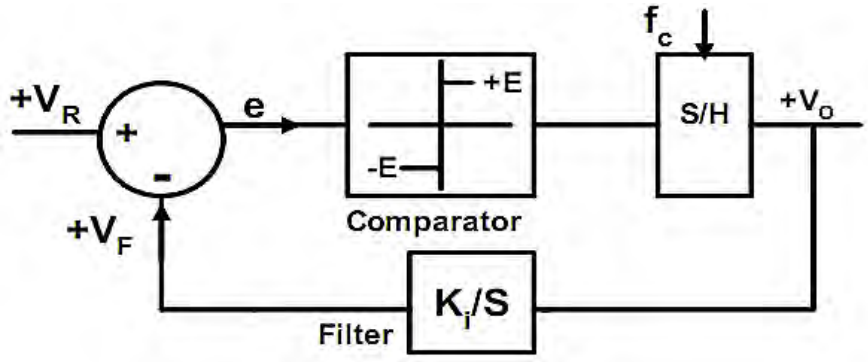

Fig. 3.12 Block diagram of delta modulator

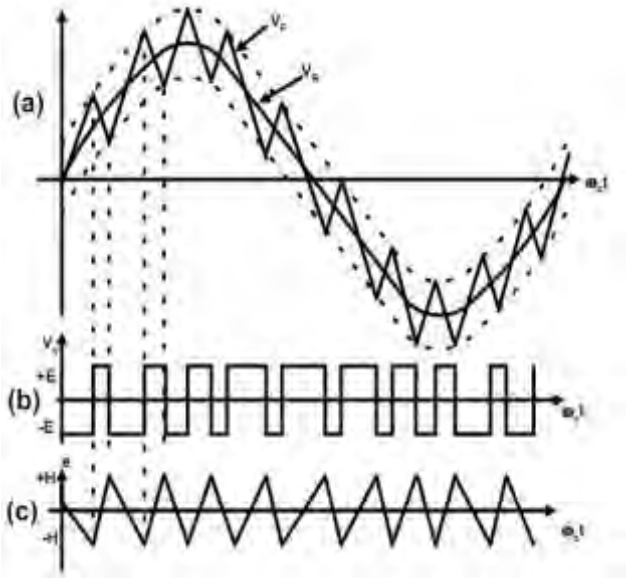

Fig. 3. 13 Delta Modulation Technique; (a) Reference signal and carrier signal, (b) Delta modulated switching functions, (c) Error signal with hysteresis band ±H

DM utilizes a sine reference wave V_R and a delta shaped carrier wave V_F. The carrier wave V_F is allowed to oscillate within a defined window extending equally above and below the reference wave V_R. The reference signal V_R is compared with carrier signal V_F obtained by integrating the comparator output signal to produce an error signal, e. The error signal, e, is quantized into one of two possible levels ± E depending on its polarity, whereas the slope of reference signal determines the time duration between two successive levels.

The comparator output is regularly sampled by the signal, f_c to produce the output binary pulses. Fig. 3.13 shows the waveforms at various nodes in the modulator block diagram. The closed loop arrangement of the modulator ensures that the integrated output faithfully tracks the reference signal within the upper and lower boundary levels ±H.

However, as V_R increases in frequency, the component of output voltage, V_o at that frequency also increases in amplitude. Thus the amplitude transfer characteristic of linear delta modulator demonstrates strong frequency dependence, [22] often undesirable in power electronic applications, where the demodulator, most frequently, is a simple low pass filter.

3.8 Group Frequency (GF) Method:

GF is a technique whereby many frequency components in the cycloconverter voltage and current spectra are collapsed into several group frequencies, and the power quality impact of the group frequencies is the same as that of the full spectrum of the cycloconverter signals. The concept of group frequency (GF) is proposed by Liu and Chang [51], [52] to simplify the harmonic analysis of integral cycle controllers (ICCs). A group frequency is defined as a single frequency component of a current or voltage signal placed in a given frequency band so that the single component has a same power quality index (e.g., K-factor) as that of all frequency components in the band.

K-factor is a power quality index used to evaluate the impact of loads on transformers [53]. The K-factor of a load current refers to transformer losses. K-factor is based on the assumption of that the eddy current losses due to each harmonic component of a non-sinusoidal current are proportional to the square of the harmonic order [53]. The K-factor is given by,

$$K = \frac{\left\{\sum_{h=1}^{N}(\frac{f_h}{f_i}I_h)^2\right\}}{\{\sum_{h=1}^{N}(I_h)^2\}} \qquad 3.1$$

Where, N is the number of harmonic plus nonstandard frequency components, and h is their index number. In the definition for K-factor, the subscript i in f_i refers to the

fundamental supply frequency (50 Hz). The traditional *K*-factor definition includes only (integer) harmonics. For the purpose of cycloconverter analysis, the traditional definition was extended to account for nonstandard frequency components.

Utilization of GFs allows for power quality analysis through the study of fewer GFs than the actual extent of frequency components. In order to utilize the GFs efficiently, the efficiency factor of a group frequency is defined. The efficiency factor of a group frequency can be expressed as,

$$E_{GF} = \frac{N_f}{N_{GF}} \tag{3.2}$$

Where, E_{GF} is the efficiency factor, N_f is the number of frequency components of a voltage or current waveform, and N_{GF} is the number of their group frequencies. To keep group frequencies efficient, a high threshold of E_{GF} is necessary. If E_{GF} is lower than the threshold, group frequencies are not recommended.

Application of GFs in the control of cycloconverters is reported in [3] and it has been shown that the efficiency factor is equal to 15, meaning that calculation is improved by a factor of 15 in analysis of frequencies present for a 4 Hz from 60–Hz supply, 0.8 lagging load and there is no zero sequence in a cycloconverter input current.

CHAPTER 4
POWER QUALITY ANALYSIS OF CYCLOCONVERTERS

Power Quality means to maintain purely sinusoidal current wave form in phase with a purely sinusoidal voltage wave form. It is a set of electrical boundaries that allows a piece of equipment to function in its intended manner without significant loss of performance or life expectancy [55]. The three phase AC power generated at the generating station is purely sinusoidal in nature. Wide spread application of static power electronics converters, zero and negative sequence components originated by the use of single phase and unbalanced loads, reactive power, voltage sag, voltage swell, flicker, voltage interruption etc. results voltage and current harmonics. Power quality improvement using traditional compensation methods include many disadvantages like electromagnetic interference, possible resonance, fixed compensation, bulkiness etc. So power system and power electronic engineers need to develop adjustable and dynamic solutions using custom power devices. These power conditioning techniques use static power electronic converters to improve the power quality of distribution system customers. The devices include Active Power Filter (APF), dynamic voltage restorer (DVR) and Unified Power Quality Conditioner (UPQC). Although these devices provides better power quality improvement compared to conventional compensation schemes, their structures embed constructional complexity and operation requires development of sophisticated computational algorithms.

The power quality analysis of the proposed switch mode cycloconverter topologies will be performed based on two standard matrices namely; Total Harmonic Distortion (THD) and power factor of the cycloconverter input current (PF_{in}). Moreover, the proposed cycloconverters perform AC-AC conversion at high efficiencies along a certain range of duty cycles and this property will also be considered as the performance parameters of these topologies.

4.1 Harmonic Distortion

Distortion is a power quality terminology indicating the deviation of a periodic sinusoidal wave from its ideal waveform characteristics. Fig. 4.1 contains an ideal sinusoidal wave along with a distorted wave. The distortion introduced in a wave can create waveform deformity as well as phase shift. Harmonics can be defined as the sinusoidal component of a periodic wave having a frequency that is an integral multiple of the fundamental frequency. If the fundamental frequency is 50 Hz, then the second harmonic is a sinusoidal wave of 100 Hz, the sixth harmonic is a sinusoidal wave of 300 Hz, and so on. Harmonic distortion is the quantitative representation of the distortion from a pure sinusoidal

waveform. Harmonic distortion is measured in terms of distortion factor. It is the ratio of the RMS of the harmonic content of a periodic wave to the RMS of the fundamental content of the wave, expressed as a percent. This is also known as the total harmonic distortion (THD).

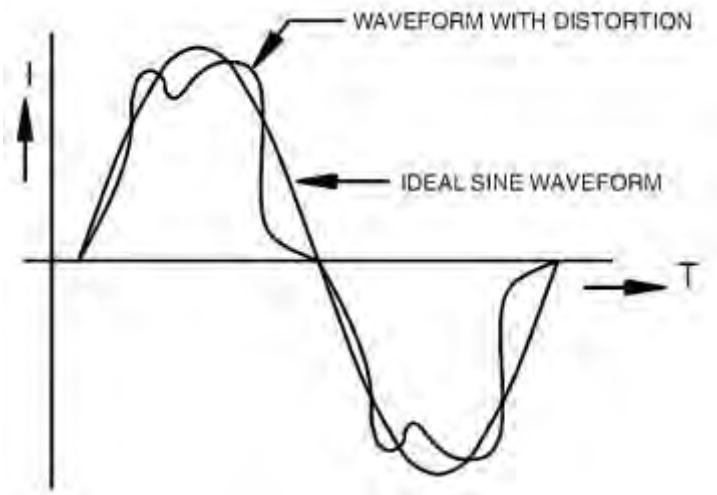

Fig. 4. 1 Waveform with distortion

A sinusoidal voltage or current function that is dependent on time *t* may be represented by the following expressions:

$$\text{Voltage function, } v(t) = V \sin(\omega t) \quad 4.1$$

$$\text{Current function, } i(t) = I \sin(\omega t \pm \text{Ø}) \quad 4.2$$

where $\omega = 2 \times \pi \times f$ is known as the angular velocity of the periodic waveform and Ø is the difference in phase angle between the voltage and the current waveforms referred to as a common axis. The sign of phase angle Ø is positive if the current leads the voltage and negative if the current lags the voltage. Fig. 4.2 contains voltage and current waveforms expressed by Eqs. (4.1) and (4.2) and which by definition are pure sinusoids.

For the periodic non-sinusoidal waveform shown in Figure 4.3, the simplified Fourier expression states:

$$v(t) = V_0 + V_1 \sin(\omega t) + V_2 \sin(2\omega t) + \ldots + V_n \sin(n\omega t) + V_{n+1} \sin((n+1)\omega t) + \ldots \quad 4.3$$

The Fourier expression is an infinite series. In this equation, V_0 represents the constant or the DC component of the waveform. V_1, V_2, V_3, …, V_n are the peak values of the successive terms of the expression. The terms are known as the harmonics of the periodic waveform. The Fourier series allows expression of nonsinusoidal periodic waveforms in terms of sinusoidal harmonic frequency components. Figure 4.4 illustrates how individual harmonics that are sinusoidal can be added to form a non-sinusoidal wave-form.

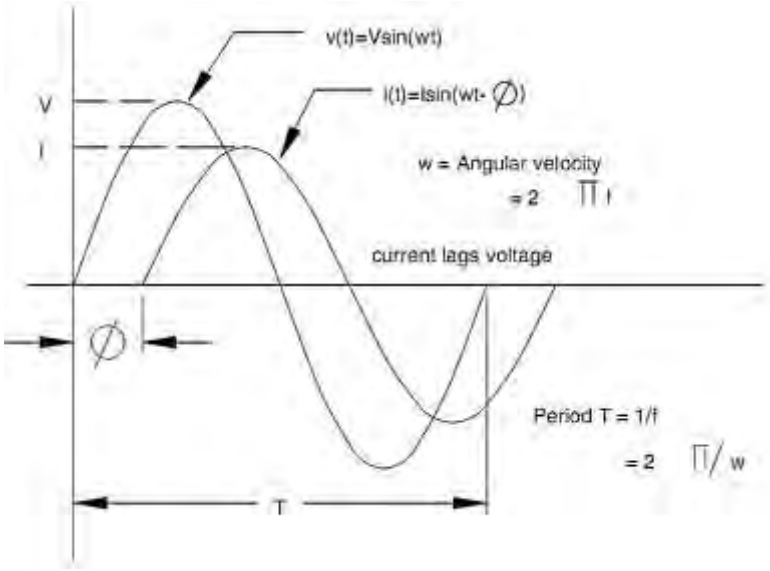

Fig. 4. 2 Sinusoidal voltage and current functions of time (t). Lagging functions are indicated by negative phase angle and leading functions by positive phase angle.

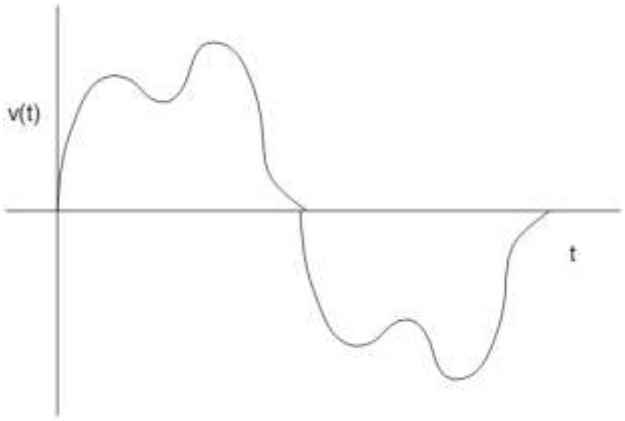

Fig. 4. 3 Non-sinusoidal voltage waveform Fourier series.

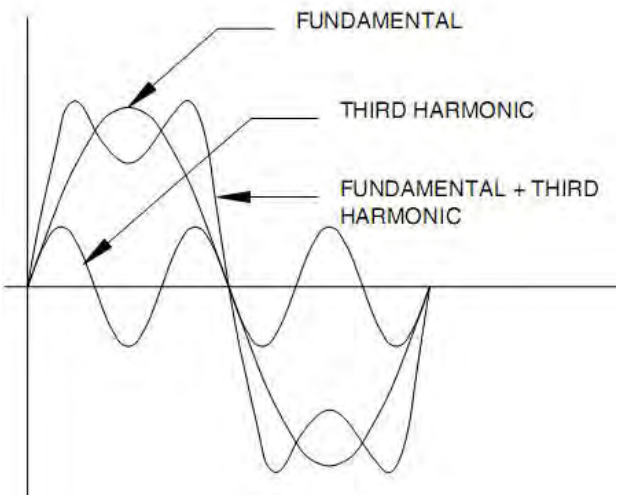

Fig. 4. 4 Creation of nonlinear waveform by adding the fundamental and third harmonic frequency waveforms.

The Fourier expression in Eq. (4.3) has been simplified to clarify the concept behind harmonic frequency components in a nonlinear periodic function. For the purist, the following more precise expression is offered. For a periodic voltage wave with fundamental frequency of $\omega = 2\pi f$,

$$v(t) = V_0 + \sum (a_k \cos k\omega t + b_k \sin k\omega t) \text{ (for } k = 1 \text{ to } \infty) \quad 4.4$$

where a_k and b_k are the coefficients of the individual harmonic terms or components. The coefficients of the harmonic terms of a function f(t) contained in Eq. (4.4) are determined by:

$$a_k = \frac{1}{\pi}\int_{-\pi}^{+\pi} f(t) \cos kt.\, dt, (k = 1,2,3 \ldots n) \quad 4.5$$

$$b_k = \frac{1}{\pi}\int_{-\pi}^{+\pi} f(t) \sin kt.\, dt, (k = 1,2,3 \ldots n) \quad 4.6$$

The coefficients represent the peak values of the individual harmonic frequency terms of the nonlinear periodic function represented by *f(t)*.

4.2 Individual and Total Harmonic Distortion

Individual harmonic distortion (IHD) is the ratio between the root mean square (RMS) value of the individual harmonic and the RMS value of the fundamental

$$IHD_n = I_n/I_1 \quad 4.7$$

For example, assume that the RMS value of the third harmonic current in a nonlinear load is 20 A, the RMS value of the fifth harmonic current is 15 A, and the RMS value of the fundamental is 60 A. Then, the individual third harmonic distortion is:

$$IHD_3 = 20/60 = 0.333, \text{ or } 33.3\%$$

and the individual fifth harmonic distortion is:

$$IHD_5 = 15/60 = 0.25, \text{ or } 25.0\%$$

Under this definition, the value of IHD1 is always 100%. This method of quantifying the harmonics is known as harmonic distortion based on the fundamental. This is the convention used by the Institute of Electrical and Electronic Engineers (IEEE) in the U.S. The European International Electrotechnical Commission (IEC) quantifies harmonics based on the total RMS value of the waveform. Using the same example shown above, the RMS value of the waveform is:

$$I_{rms} = \sqrt{(60^2 + 20^2 + 15^2)} = 65A$$

Based on the IEC convention,

$$IHD_1 = 60/65 = 0.923, \text{ or } 92.3\%$$

$$IHD_3 = 20/65 = 0.308, \text{ or } 30.8\%$$

$$IHD_5 = 15/65 = 0.231, \text{ or } 23.1\%$$

The examples illustrate that even though the magnitudes of the harmonic currents are the same, the distortion percentages are different because of a change in the definition. It should be pointed out that it really does not matter what convention is used as long as the same one is maintained throughout the harmonic analysis.

Total harmonic distortion (THD) is a term used to describe the net deviation of a nonlinear waveform from ideal sine waveform characteristics. Total harmonic distortion is the ratio between the RMS value of the harmonics and the RMS value of the fundamental. For example, if a nonlinear current has a fundamental component of I_1 and harmonic components of I_2, I_3, I_4, I_5, I_6, I_7, …, then the RMS value of the harmonics is:

$$I_H = \sqrt{\left({I_2}^2 + {I_3}^2 + {I_4}^2 + {I_5}^2 + {I_6}^2 + \cdots\right)} \quad 4.8$$

$$\text{THD} = (I_H / I_1) \times 100\% \quad 4.9$$

For example, in order to find the total harmonic distortion of a voltage waveform with the following harmonic frequency make up: Fundamental = V1 = 114 V, 3rd harmonic = V3 = 4 V, 5th harmonic = V5 = 2 V, 7th harmonic = V7 = 1.5 V, 9th harmonic = V9 = 1,

RMS value of the harmonics,

$$V_H = \sqrt{(4^2 + 2^2 + 1.5^2 + 1)} = 4.82V$$

$$\text{THD} = (4.82/114) \times 100 \cong 4.23\%$$

and the individual harmonic distortions are,

$$\text{IHD}_3 = 4/114 = 3.51\%$$

$$\text{IHD}_5 = 2/114 = 1.75\%$$

$$\text{IHD}_7 = 1.5/114 = 1.32\%$$

$$\text{IHD}_9 = 1/114 = 0.88\%$$

By definition, IHD1 = 100%, so

$$THD = \sqrt{\left({IHD_3}^2 + {IHD_5}^2 + {IHD_7}^2 + {IHD_9}^2\right)} \cong 4.23\%$$

The results are not altered by using either the magnitude of the RMS quantities or the individual harmonic distortion values. The THD equation that will be utilized here to examine the performance of the proposed cycloconverters is as below.

$$THD\ (\%) = \sqrt{\frac{{I_s}^2 - {I_{s1}}^2}{{I_{s1}}^2}} \times 100\%$$

Here, I_s is the total input RMS current and I_{s1} is the fundamental component of the input current. The individual harmonic distortion indicates the contribution of each harmonic frequency to the distorted waveform, and the total harmonic distortion describes the net deviation due to all the harmonics. These are both important parameters. In order to solve harmonic problems, we require information on the composition of the individual distortions so that any treatment may be tailored to suit the problem. The total harmonic distortion, while conveying no information on the harmonic makeup, is used to describe the degree of pollution of the power system as far as harmonics are concerned. Defining

the individual and total harmonic distortions will be helpful as we look at some typical nonlinear waveforms and their harmonic frequency characteristics.

4.3 Power Factor

Power factor is included in the discussion of power quality for several reasons. Power factor is a power quality issue in that low power factor can cause equipment to fail. In many instances, the cost of low power factor can be high; utilities penalize facilities that have low power factor because they find it difficult to meet the resulting demands for electrical energy. The study of power quality is about optimizing the performance of the power system at the lowest possible operating cost. Power factor is definitely an issue that qualifies on both counts.

Several different definitions and expressions can be applied to the term power factor, most of which are probably correct. Apparent power (S) in an electrical system can be defined as being equal to voltage times current:

$$S = V \times I(1Ø) \tag{4.10}$$

$$S = \sqrt{3}V \times I(3Ø) \tag{4.11}$$

Where, V = phase-to-phase voltage (V) and I = line current (VA). Power factor (PF) may be viewed as the percentage of the total apparent power that is converted to real or useful power. Thus, active power (P) can be defined by:

$$P = V \times I \times PF \text{ for } 1Ø \tag{4.12}$$

$$P = \sqrt{3}V \times I \times PF \text{ for } 3Ø \tag{4.12}$$

In an electrical system, if the power factor is 0.80, 80% of the apparent power is converted into useful work. Apparent power is what the transformer that serves a home or business has to carry in order for that home or business to function. Active power is the portion of the apparent power that performs useful work and supplies losses in the electrical equipment that are associated with doing the work. Higher power factor leads to more optimum use of electrical current in a facility.

Any electrical circuit or device when subjected to an electrical potential develops a magnetic field that represents the inductance of the circuit or the device. As current flows in the circuit, the inductance produces a voltage that tends to oppose the current. This effect, known as Lenz's law, produces a voltage drop in the circuit that represents a loss in the circuit. At any rate, inductance in AC circuits is present whether it is needed or not. In

an electrical circuit, the apparent and reactive powers are represented by the power triangle shown in Fig. 4.5. The following relationships apply:

$$S = \sqrt{P^2 + Q^2} \quad 4.13$$

$$P = S \cos\text{Ø} \quad 4.14$$

$$Q = S \sin\text{Ø} \quad 4.15$$

$$Q/P = \tan\text{Ø} \quad 4.16$$

Where, S = apparent power, P = active power, Q = reactive power, and Ø is the power factor angle. In Fig. 4.6, V is the voltage applied to a circuit and I is the current in the circuit. In an inductive circuit, the current lags the voltage by angle Ø, as shown in the figure, and Ø is called the power factor angle.

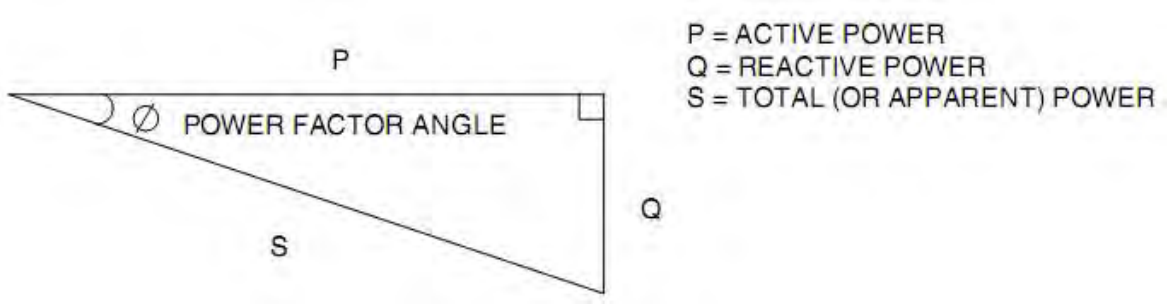

Fig. 4.5 Power triangle and relationship among active, reactive, and apparent power.

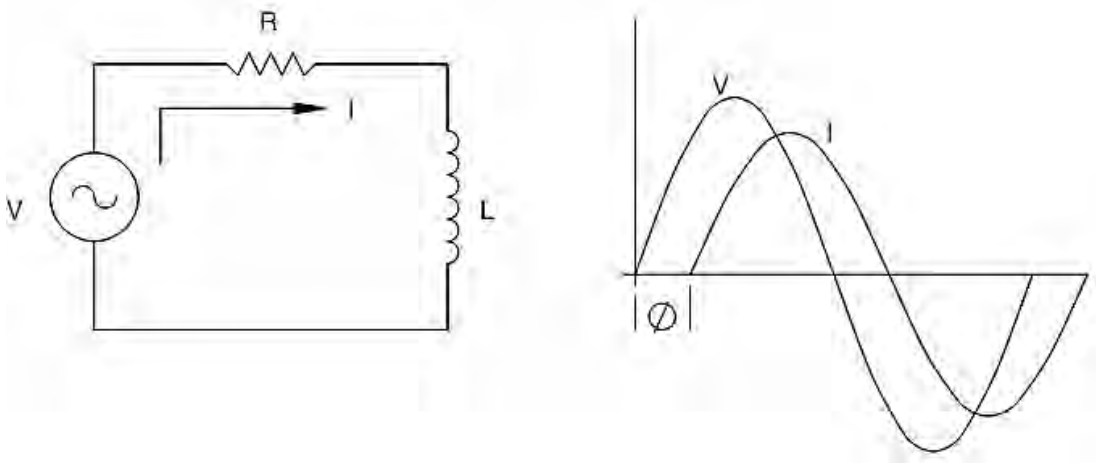

Fig. 4. 6 Voltage, current, and power factor angle in a resistive/inductive circuit.

If XL is the inductive reactance given by:

$$X_L = 2\pi fL \quad 4.17$$

then total impedance (Z) is given by:

$$Z = R + jX_L \quad 4.18$$

The power factor angle is calculated from the expression:

$$\tan\emptyset = (X_L/R) \text{ or } \emptyset = \tan^{-1}(X_L/R) \quad 4.19$$

4.4 Displacement and True Power Factor

The terms displacement and true power factor, are widely mentioned in power factor studies. Displacement power factor is the cosine of the angle between the fundamental voltage and current waveforms. The fundamental waveforms are by definition pure sinusoids. But, if the waveform distortion is due to harmonics (which is very often the case), the power factor angles are different than what would be for the fundamental waves alone. The presence of harmonics introduces additional phase shift between the voltage and the current. True power factor is calculated as the ratio between the total active powers used in a circuit (including harmonics) and the total apparent power (including harmonics) supplied from the source:

True power factor = total active power/total apparent power.

The input power factor equation that will be utilized here to examine the performance of the proposed cycloconverters is as below.

$$pf_{input} = \frac{Average(P_{input})}{RMS(V_{input}) \times RMS(I_{input})}$$

Good power factor is not necessarily critical for most equipment to function in a normal manner. Having low power factor does not cause a piece of machinery to shut down, but high power factor is important for the overall health of the power system. Operating in a high power factor environment ensures that the power system is functioning efficiently. It also makes economic sense. Electrical power generation, transmission, and distribution equipment have maximum rated currents that the machines can safely handle. If these levels are exceeded, the equipment operates inefficiently and suffers a loss of life expectancy. That is why how power factor is considered as an important power quality parameter.

CHAPTER 5
SINGLE PHASE BUCK-BOOST CYCLOCONVERTER

A static Buck-Boost converter is a switch mode DC-DC converter that can provide output greater or less than the supply voltage by controlling the duty cycle of the control pulse. In the proposed single phase cycloconverter based on Buck-Boost topology, the P and N converters are configured as the corresponding switch mode scheme. This chapter will analyze the configuration, operation and performance of the proposed single phase Buck-Boost cycloconverter.

5.1 Circuit Configuration

The circuit diagram of the proposed Buck-Boost cycloconverter topology is presented in Fig. 5.1. The resistive load RL is differentially connected between the P-converter and N-converter. The output capacitor, C_{out} stabilizes the output voltage across the load. Switch S11 and S12 are used to chop the P-converter input. Switch S21 and S22 are used to chop the N-converter input.

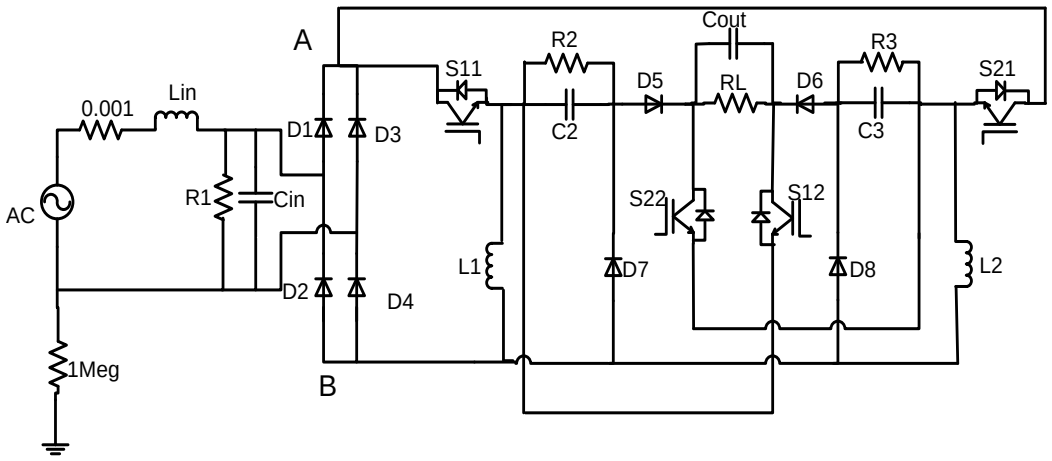

Fig. 5.1 Proposed single phase cycloconverter based on Buck-Boost topology

C2 and C3 are the functioning capacitors for P and N-converter respectively. L1 and L2 are the functioning inductors for P and N-converter respectively. The diodes D1, D2, D3, D4 forms a full-bridge rectifier which allows the AC input from AC source to always maintain a certain direction in the converter circuit. Thus point A is always at positive and point B is always negative voltage, which ensures DC input for basic cycloconverter circuit topology. Diodes D5 and D6 are used to restrict current flow in backward direction from the load for P and N-converter respectively. Diodes D7 and D8 provide the discharging path for the capacitors C2 and C3 respectively when the corresponding switches are in OFF position.

5.2 Operation

The proposed topology comprises of two basic topologies, Cycloconverter and Buck-Boost converter. For basic cycloconverter, operation can be defined in two steps: P-conversion and N-conversion. The switching scheme for the cycloconverter is indicated at Fig 5.2. For basic Buck-Boost converter, operation can be defined by charging and discharging of a capacitor, maintaining the current through the inductor always flowing in a single direction. S11 and S12 are switched ON/OFF while S21 and S22 are kept OFF for P converter operation. Alternatively S21 and S22 are turned ON/OFF while S11 and S12 are kept OFF for N converter operation.

Combining these two topologies, proposed Buck-Boost based cycloconverter operates in four different states:

1. Switch ON in P-converter
2. Switch OFF in P-converter
3. Switch ON in N-converter
4. Switch OFF in N-converter

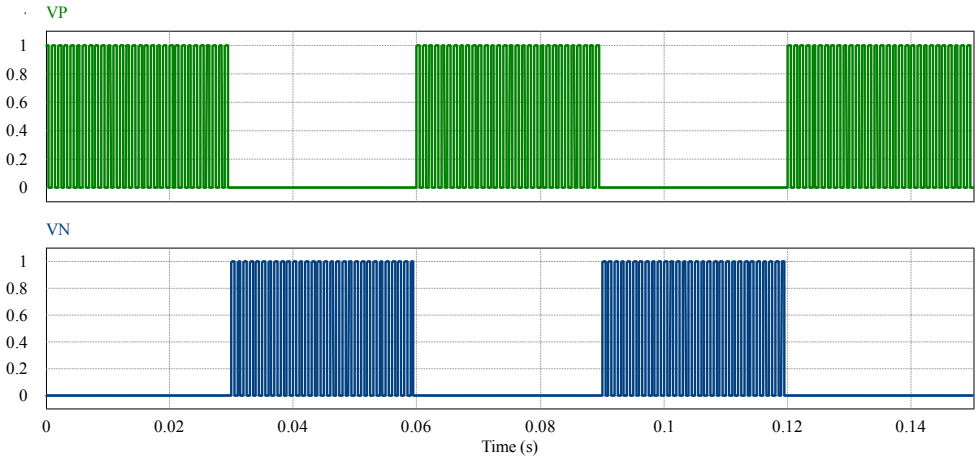

Fig. 5.2 Switching characteristics of the P and N converter for Buck-Boost Topology

It is clear from the figure, that only one switching scheme is active at a time. When P-converter is in operation, the N-converter switches are completely in OFF position, and vice versa.

5.2.1 The P-converter

At the P–conversion cycle, the output is always positive irrespective of the polarity at the input. The P-converter can be realized from the Fig. 5.3. The switching of the P-converter is given in Fig 5.4

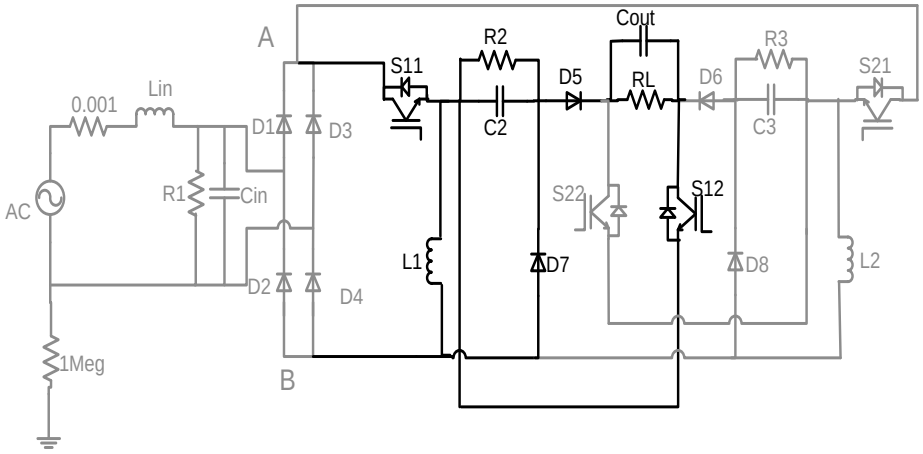

Fig. 5.3 Buck-Boost topology based P-converter

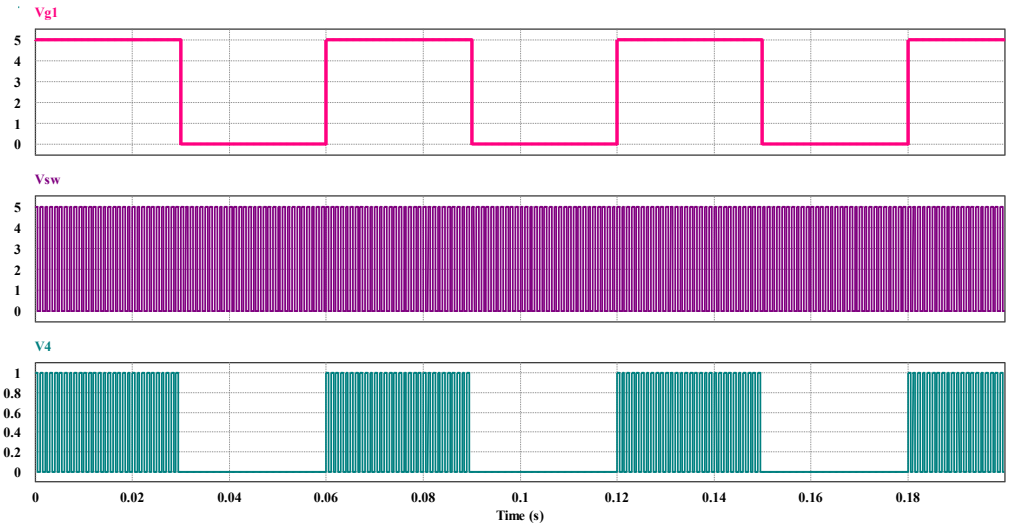

Fig. 5.4 Switching scheme of the P-converter

The high frequency signal is to activate the switching topology. The low frequency signal is to initiate the P-converter only. By multiplying these 2 signals, P-converter is active at high switching frequency.

5.2.1.A Switch on in P-converter

When the switch S11 and S12 is ON in the P-conversion cycle, the inductor is charged. The current flow diagram is given in Fig. 5.5. For the switch in ON position at P-converter, S11 and S12 work as a short circuit connection ideally. Current flows from A to B through the inductor L1 (downward). The capacitor C2 is charged having positive terminal at C and negative terminal at D. Diode D5 ensures unidirectional

flow from D to E. The current through the load flows from E to F. Via the switch S12, the current returns to C, completing the loop.

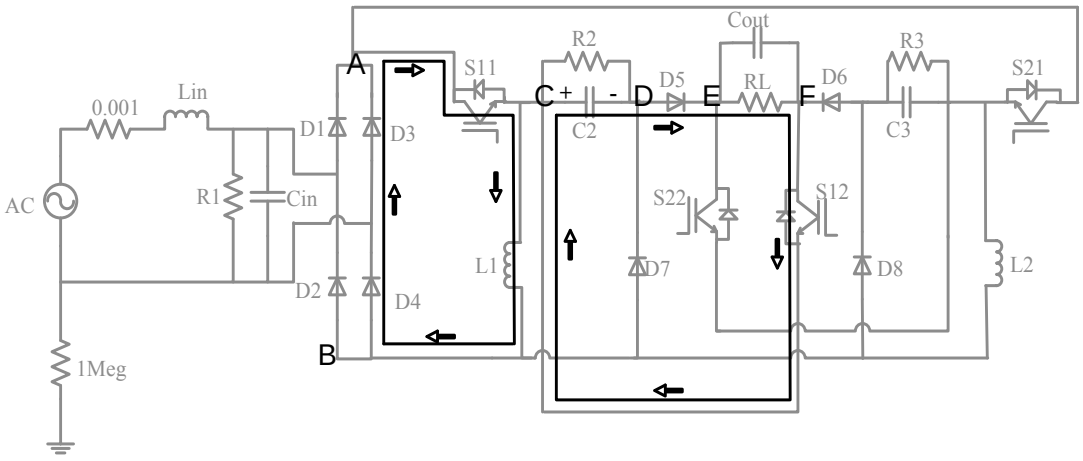

Fig. 5.5 Current flow direction during switch is ON in P-converter

At the same time, the output capacitor, Cout is charged having positive at E and negative at F. If we connect a voltmeter with positive terminal at E and negative terminal at F, it will show a positive voltage irrespective of the input AC voltage direction. Thus this converter is denoted as the P-converter. As D6 is in reverse bias condition, the current through the output cannot effect the N-converter components. The switches S11 and s12 are ON when the input signal at their gate is HIGH, and turned OFF when the gate signal is LOW. This is shown in Fig. 5.6

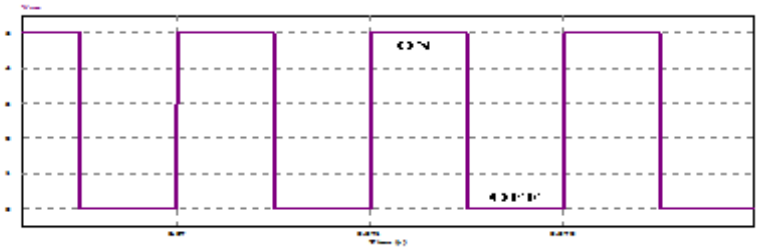

Fig. 5.6 On-Off cycle of the switches

5.2.1.B Switch off in P-converter

When the switches S11 and S12 in turned OFF in the P-convverter, the current flow path is indicated in Fig. 5.7. For the switch in OFF position at P-converter, S11 and S12 work as an open circuit connection ideally. The direction of current through the

inductor L1 cannot be changed instantaneously. Thus it flows in the same direction from C to B. Diode D7 then conducts from B to D. The capacitor C2 is charged having positive terminal at D and negative terminal at C (opposite from previous P cycle).

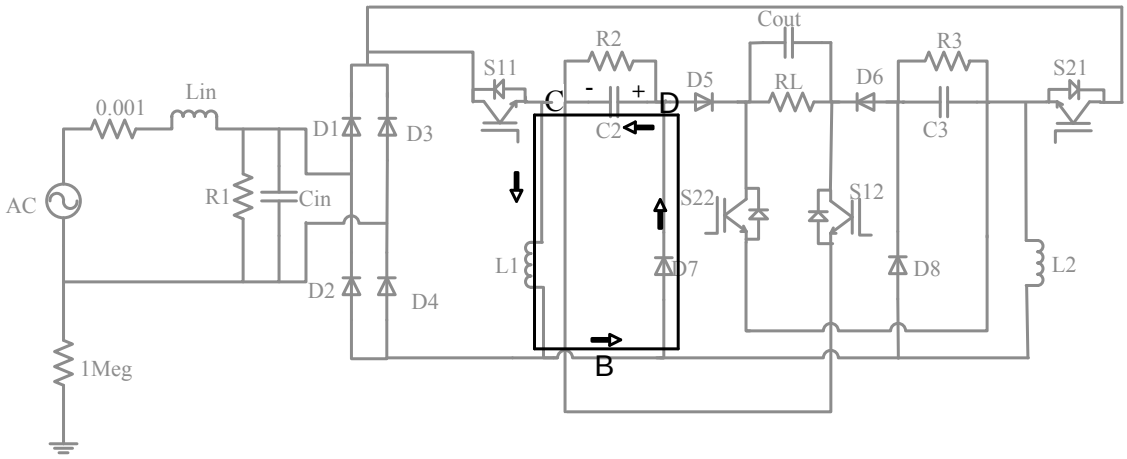

Fig. 5.7 Current flow direction when switch is OFF in P-converter

In this manner by charging the capacitor C2, the Buck-Boost converter basic topology is satisfied. The diodes D5 and D6 prevent current to flow towards C2 and C3 respectively.

5.2.1.C Overall P-conversion

When switch is ON in P-conversion cycle, both capacitors C2 and C_{out} are charged. When the switch is OFF in P-conversion cycle, both capacitors are discharged leaving the circuit in rest position.

When the switching frequency is large compared to RC time constant of the C_{out}-RL loop, C_{out} does not get sufficient time to get completely discharged and return to previous voltage level. Again at the charging cycle, capacitor voltage increases to a higher value keeping pace with the input voltage. As the input voltage decreases sinusoidally, the capacitor voltage decreases more at discharging cycle than it increases at charging cycle. Thus the overall behavior of the output capacitor resembles a sinusoidal waveform.

The higher is the switching frequency, the better is this response and the output is more likely to be a sinusoid because the capacitor C_{out} gets very little time to be discharged.

At the P-conversion cycle, the output waveform at single input half wave is similar as shown is Fig 5.8

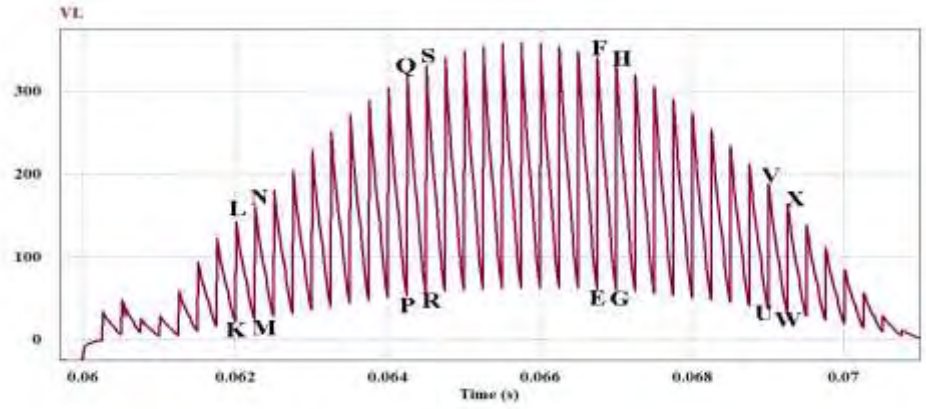

Fig. 5.8 Charging and discharging of the output capacitor at P conversion

At the rising of input at ON cycle, Output voltage rises from P to Q. At the discharging cycle, output voltage drops from Q to R. As seen from the output waveform R > P, indicating that the capacitor cannot come back to previous level. Again at charging cycle, the capacitor voltage rises to S, while S > Q.

Similar arguments can be given for the voltages at K, L, M and N points. It can be observed that voltage rise is much faster at the beginning of the sinusoid than at near to the peak. It can also be expressed as (N-L) > (S-Q).

At the falling of input at ON cycle, Output voltage rises from E to F. At the discharging cycle, Output voltage drops from F to G. As seen from the output waveform E > G, indicating that the capacitor is discharged below the previous level. Again at charging cycle, the capacitor voltage rises to H, while H < F.

Similar arguments can be given for the voltages at U, V, W and X points. It can be observed that voltage fall is much faster at the ending of the sinusoid than at near the peak. It can also be expressed as (V-X) > (F-H). The P-converter output at a complete half cycle of the output waveform is similar to the output shown if Fig. 5.9

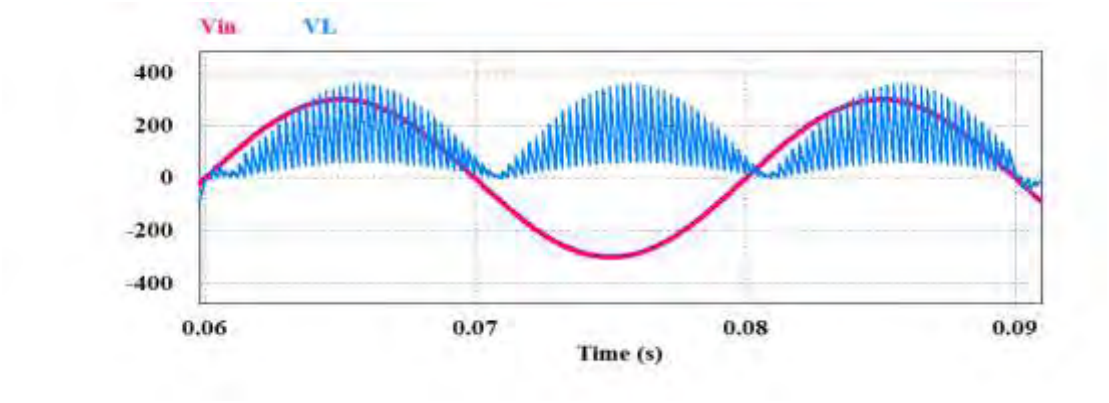

Fig. 5.9 Input and Output voltages at P-conversion

5.2.2 The N-converter

At the N –conversion cycle, the output is always negative irrespective of the polarity at the input. The N-converter can be realized from the Fig. 5.10. The switching scheme of the N-converter is similar to that of the P-converter. P-converter is completely inactive when the N-conversion is operating. This is ensured by turning OFF the gate pulses to P converter switches and turning ON/OFF the N converter switches.

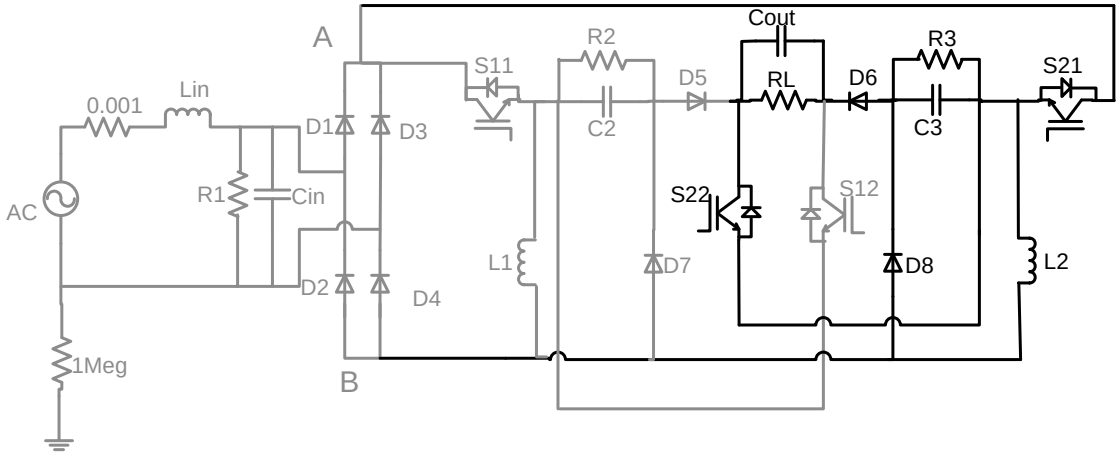

Fig. 5.10 Buck-Boost topology based N-converter

5.2.2.A Switch on in N-converter

When switches S21 and S22 are ON in the N-converter, the current flow is indicated in Fig. 5.11. For the switch in ON position at N-converter, S21 and S22 work as a short circuit connection ideally. Current flows from A to B through the inductor L2 (downward). The capacitor C3 is charged having positive terminal at C and negative terminal at D. Diode D6 ensures unidirectional flow from D to E. The current through the load flows from E to F via the switch S22, the current returns to C, completing the loop.

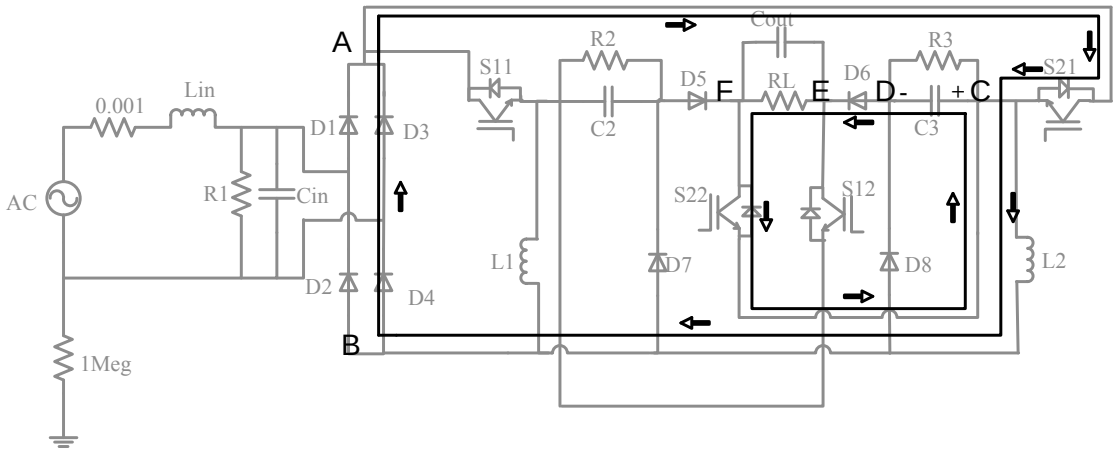

Fig. 5.11 Current flow direction when switch is ON in N-converter

At the same time, the output capacitor, Cout is charged having positive at E and negative at F. If we connect a voltmeter with positive terminal at F and negative terminal at E(as previous), it will show a negative voltage irrespective of the input AC voltage direction. Thus this converter is denoted as the N-converter.

5.2.2.B Switch off in N-converter

When the switches S21 and S22 are OFF, the current flow path is given in Fig.5.12. For the switch in OFF position at P-converter, S21 and S22 work as an open circuit connection ideally. The direction of current through the inductor L2 cannot be changed instantaneously. Thus it flows in the same direction from C to B. Diode D8 then conducts from B to D. The capacitor C3 is discharged having positive terminal at D and negative terminal at C (opposite from previous N cycle). In this manner by charging and discharging the capacitor C3, the Buck-Boost converter basic topology is achieved.

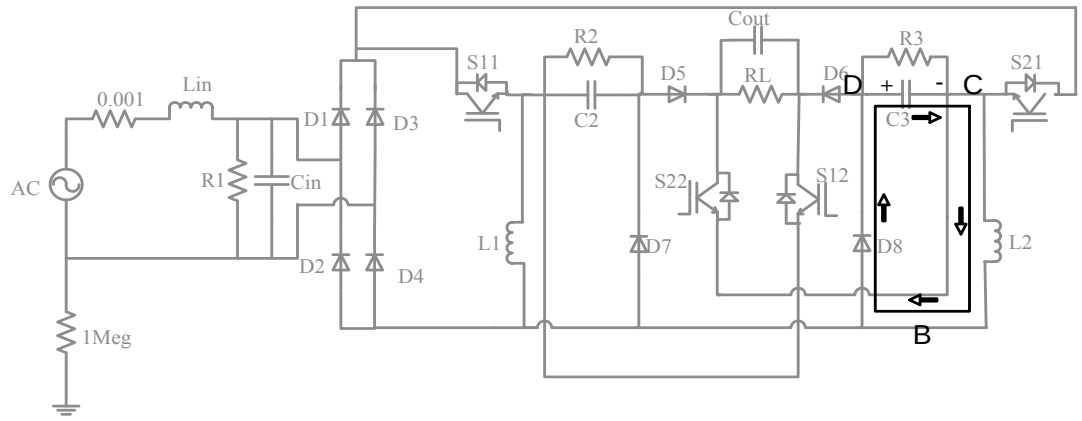

Fig. 5.12 Current flow direction when switch is OFF in N-converter

5.2.2.C Overall N-conversion

At the N-conversion cycle, the output waveform at single input half wave is similar as shown is Fig 5.13. When switch is ON in N-conversion cycle, both capacitors C3 and Cout are charged. When the switch is OFF in N-conversion cycle, both capacitors are discharged leaving the circuit in rest position.

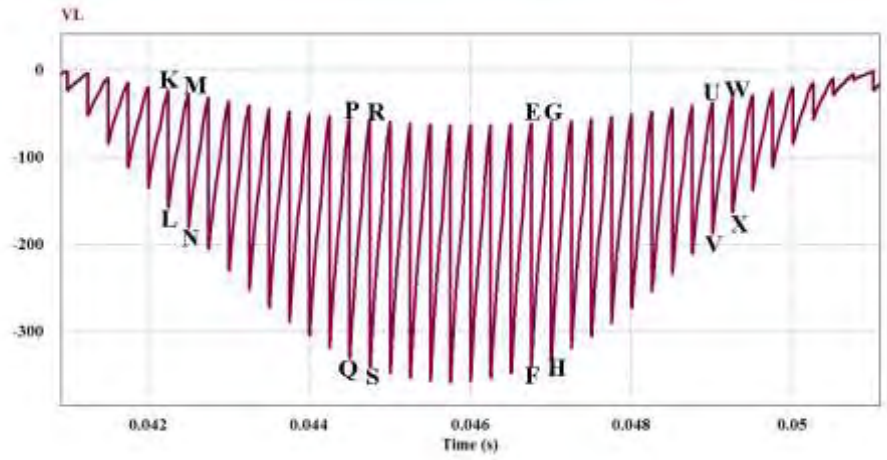

Fig. 5.13 Charging and discharging cycle of the output capacitor at N-conversion

At the rising of input at ON cycle, Output voltage rises from P to Q. At the discharging cycle, output voltage drops from Q to R. As seen from the output waveform |R| > |P|, indicating that the capacitor cannot come back to previous level. Again at charging cycle, the capacitor voltage rises to S, while |S| > |Q|.

Similar arguments can be given for the voltages at K, L, M and N points. It can be observed that voltage rise is much faster at the beginning of the sinusoid than at near to the peak. It can also be expressed as |(N-L)| > |(S-Q)|.

At the falling of input at ON cycle, Output voltage rises from E to F. At the discharging cycle, Output voltage drops from F to G. As seen from the output waveform |E| > |G|, indicating that the capacitor is discharged below the previous level. Again at charging cycle, the capacitor voltage rises to H, while |H| < |F|.

Similar arguments can be given for the voltages at U, V, W and X points. It can be observed that voltage fall is much faster at the ending of the sinusoid than at near the peak. It can also be expressed as |(V-X)| > |(F-H)|. The over-all N-conversion at a complete half cycle of the output is given by Fig. 5.14

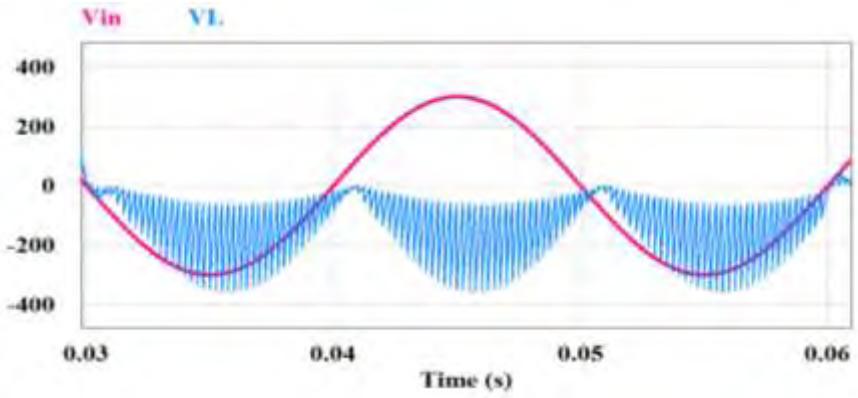

Fig. 5.14 Input and Output voltages at N-conversion

5.3 Simulation results:

The simulation of the proposed circuit is performed using PSIM Professional Version 9.0.3.400. It is a specialized simulator for power electronics circuit.

5.3.1 Performance under variable control conditions

Table 5.1 presents the results of the proposed Buck-Boost cycloconverter at different duty cycles for different frequencies.

Table 5.1 Simulation output for different duty cycle at different switching frequencies

f	D	Vo.max	Vo.rms	Iin.max	THD	Pf(in)	Pin	Pout	Ploss	η
10	0.2	53	26	0.95	1.21	0.238	18	7	5	60.9
	0.3	105	49	0.96	2.79	0.546	48	24	6	80
	0.4	255	84	1.17	2.81	0.83	128	71	9	88.7
8	0.2	52	25	0.95	2.17	0.245	18	6	5	57.1
	0.3	78	38	0.96	4.04	0.422	34	14	5	73.7
	0.4	168	77	1.11	2.98	0.83	114	59	9	86.7
6	0.3	102	41	0.96	17.15	0.488	41	16	14	56.2
	0.4	139	67	1.02	3.99	0.78	95	45	28	61.6
	0.5	219	109	1.79	4.43	0.95	229	119	38	75.8
4	0.4	301	91	1.09	1.54	0.89	206	83	27	75.5
	0.5	384	118	1.30	2.89	0.93	332	139	32	81.3
	0.6	470	146	2.98	3.83	0.95	489	213	36	85.5
3	0.5	268	97	1.50	3.12	0.957	205	94	16	85.5
	0.6	349	127	2.36	3.18	0.985	334	162	18	90
	0.7	580	218	6.51	4.52	0.990	938	474	32	93.7
2	0.6	468	147	3.44	6.46	0.997	474	215	32	86.3
	0.7	544	173	4.60	6.05	0.998	638	300	60	90.4
	0.8	974	311	15.01	12.23	9.919	1995	968	80	94.2

The result from this simulation shows that for a particular frequency the performance of the proposed converter varies with different duty cycles. For instance, at switching frequency of 6kHz, the THD with 30% duty cycle is 17.15% whereas it reduces to 3.99 % with a duty cycle of 40%. Moreover, the input power factor and efficiency for D equal to 0.4 is 0.75 and 61.6% respectively whereas, for a duty cycle of 50% the power factor and efficiency are 0.95 and 75.5% respectively. Similar observation can be made for other switching frequencies as well. Considering this analysis as the basis, open loop sliding control has been developed in this thesis.

5.3.2 Open Loop Sliding Control

Open loop sliding control is the gate pulse generation scheme employed in this thesis. For a given load, the performance of the proposed cycloconverter is examined for a varied range of duty cycles and frequencies. Then an optimum operating point, designated by a specific duty cycle is selected for a specific frequency. Since, in this gate pulse generation scheme, the switching frequency slides through the range of duty cycle of the control pulse this method is specified as the open loop sliding control. The optimum set of duty cycle and frequency values selected for 100 ohm resistive load is presented in Table 5.2. This table also presents the simulation results for the corresponding control parameters. For the proposed buck-boost converter the sliding frequency values are presented in Fig. 5.15. This figure shows the open loop sliding control graph for the proposed buck-boost cycloconverter.

Table 5. 2 Output behavior for sweeping characteristics of the converter

D	f	Vo.max	Vo.rms	Iin.max	THD	Pf(in)	Pin	Pout	Ploss	η
0.2	10	53	26	0.95	**1.21**	**0.238**	18	7	5	**61**
0.3	8	78	38	1.12	**4.04**	**0.422**	34	14	5	**74**
0.4	6	139	67	1.21	**3.99**	**0.78**	95	45	28	**62**
0.5	4	384	118	1.49	**2.89**	**0.93**	332	139	32	**81**
0.6	3	349	127	2.36	**3.18**	**0.985**	334	162	18	**90**
0.7	2	544	173	4.59	**6.05**	**0.998**	638	300	60	**90**
0.8	1.5	1043	279	12.82	**9.22**	**0.961**	1654	777	63	**93**
0.9	1	1693	318	25.25	**19.21**	**0.667**	2217	1014	70	**94**

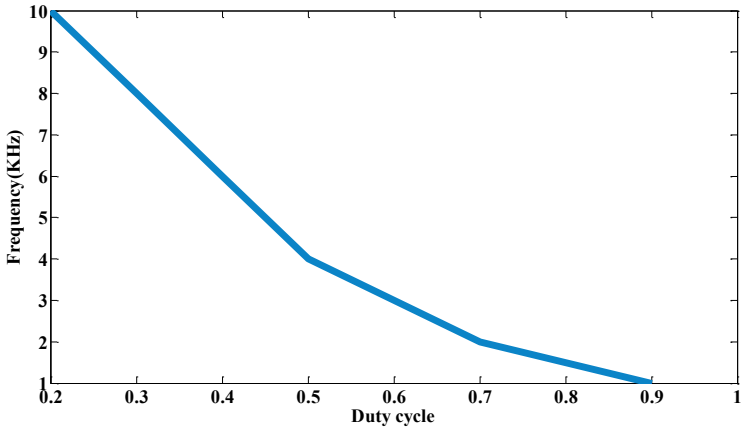

Fig. 5.15 Sweeping characteristics for Buck-Boost cycloconverter

5.3.3 Typical Waveforms

Fig. 5.16 shows typical input current, input and output voltages for the proposed buck-boost cycloconverter with 50% duty cycle. The switching frequency is set to 4 kHz as determined form the open loop sliding control of this cycloconverter. For D=0.5 the output voltage is almost equal to the input voltage, as should be the case in ideal Buck-Boost converter. Fig. 5.17 shows the waveforms for D=0.3 and in this case, the output voltage is much smaller than the input voltage ($V_{out} < V_{in}$ for D < 0.5)

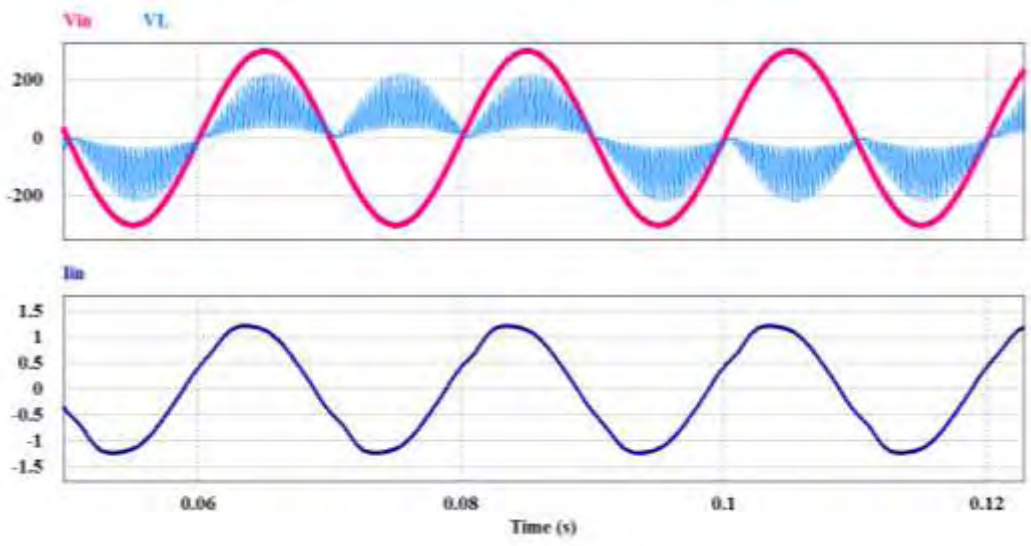

Fig. 5.16 Input & output voltages and input current at D=0.5 and f=4 KHz

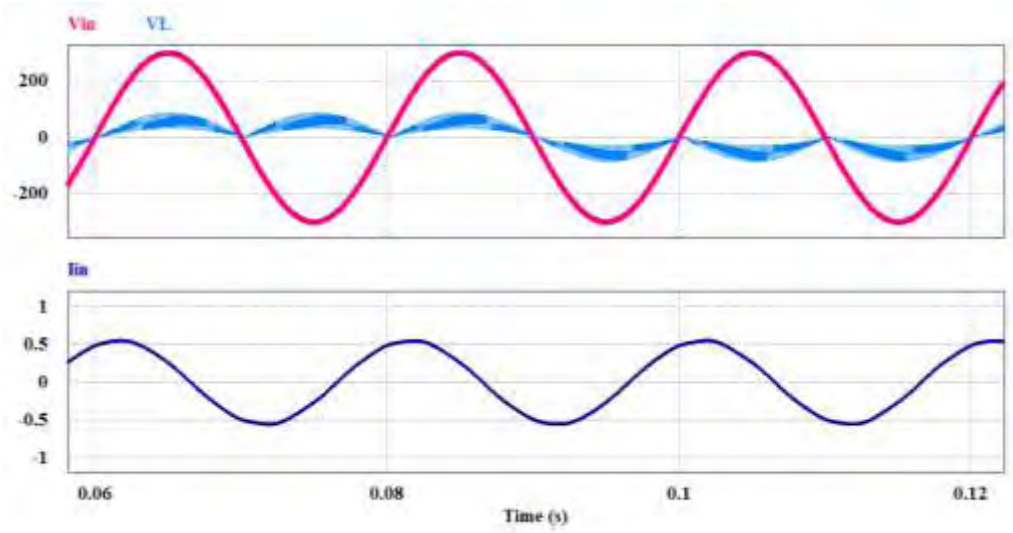

Fig. 5.17 Input & output voltages and input current at D=0.3 and f=8 KHz

Fig. 5.18 shows typical input current, input and output voltages for the proposed buck-boost cycloconverter with 70% duty cycle. The switching frequency is set to 2 kHz according to the open loop sliding control of this cycloconverter. For D=0.7, the output voltage is much larger than the input voltage ($V_{out} > V_{in}$ for $D > 0.5$)

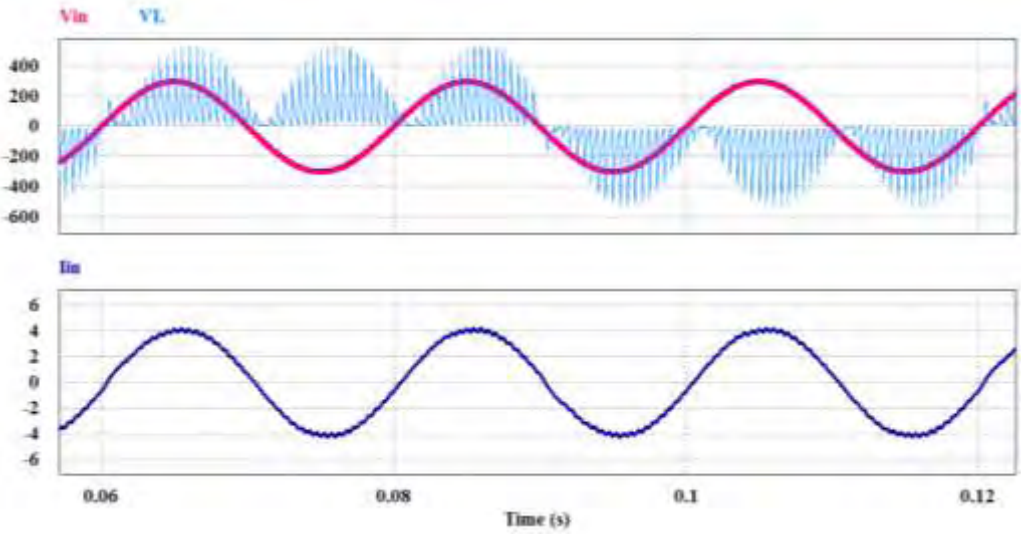

Fig. 5.18 Input & output voltages and input current at D=0.7 and f=2 KHz

Spectrum of the input current of Fig. 5.16 is shown in Fig. 5.19 which shows a small magnitude of current near 4 kHz (the switching frequency). It is evident that these circuits can reduce the input current harmonic distortion.

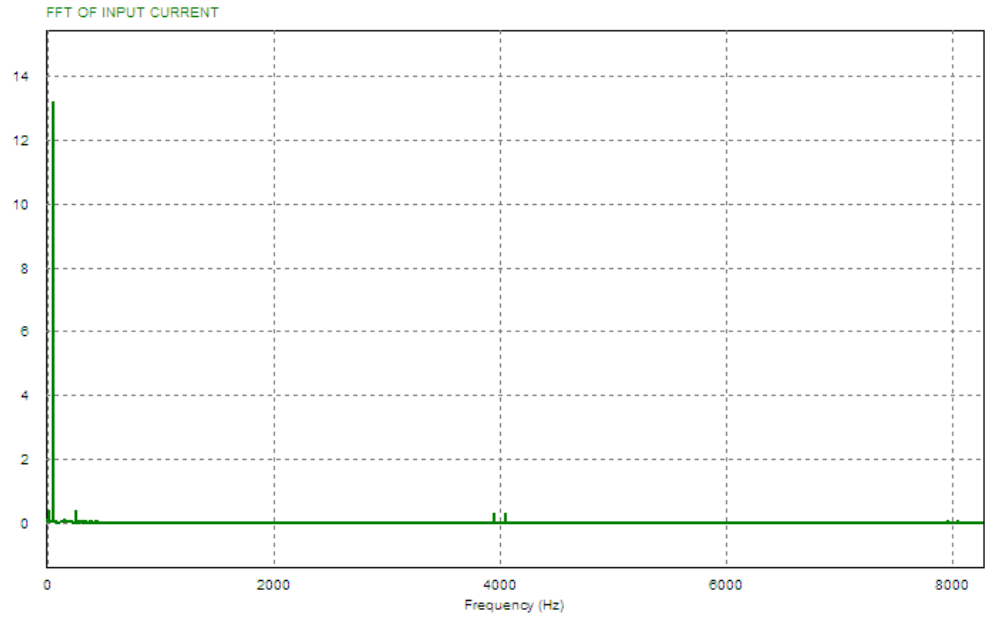

Fig. 5.19 Spectrum of the input current for D= 0.5 and f = 4 kHz

5.3.4 Performance Under Variable Load Conditions

Table 5.3 shows the performance of the proposed Buck-Boost cycloconverter with variable resistive loads. It is observed from the results presented in table 5.3 and Figs. 5.20, 5.21 and 5.22 that variation of load has a little effect on the input current THD of the proposed converter. However, with the increment of load resistance the input power factor and efficiency slightly degrades at lower duty cycles of the proposed Buck-Boost cycloconverter.

Table 5.3 Change in output behavior with load

D	f	R=50			R=100			R=200		
		THD	Pf(in)	η	THD	Pf(in)	η	THD	Pf(in)	η
0.2	10	0.85	0.328	60	1.21	0.238	61	2.38	0.202	54
0.3	8	1.82	0.632	80	4.04	0.422	74	3.39	0.398	71
0.4	6	3.19	0.876	86	3.99	0.78	85	4.59	0.679	81
0.5	4	1.62	0.964	89	2.89	0.93	88	2.72	0.914	86
0.6	3	3.41	0.997	91	3.18	0.985	90	3.27	0.982	88
0.7	2	5.56	0.997	91	6.05	0.998	90	5.77	0.998	89
0.8	1.5	9.51	0.956	93	9.22	0.961	93	9.08	0.975	91
0.9	1	19.35	0.665	94	19.21	0.667	94	18.14	0.683	92

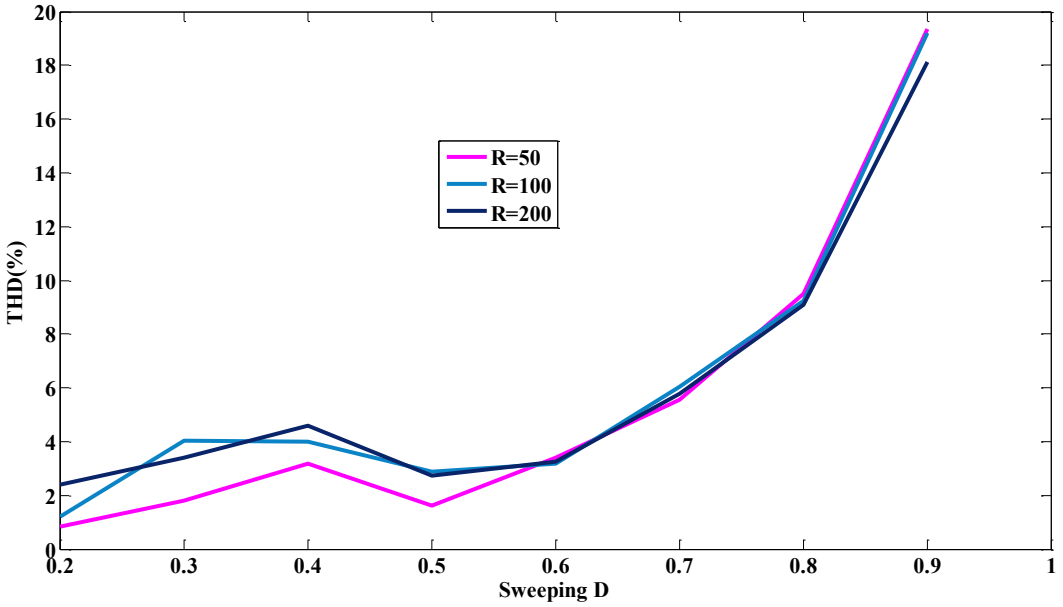

Fig. 5.20 Variation in THD with different load at different position

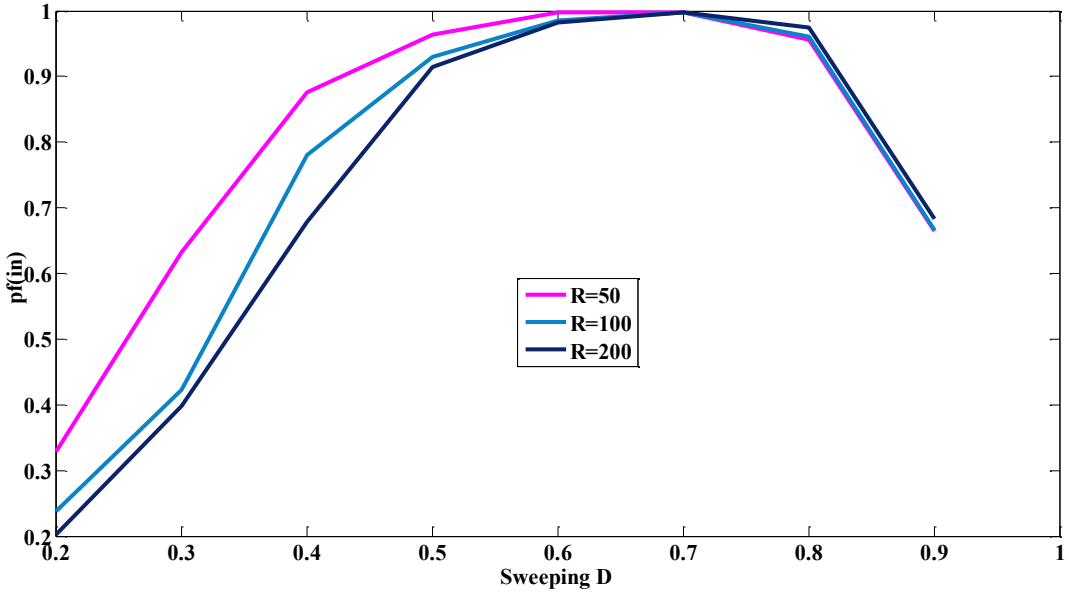

Fig. 5.21 Variation in input power factor with different load at different position

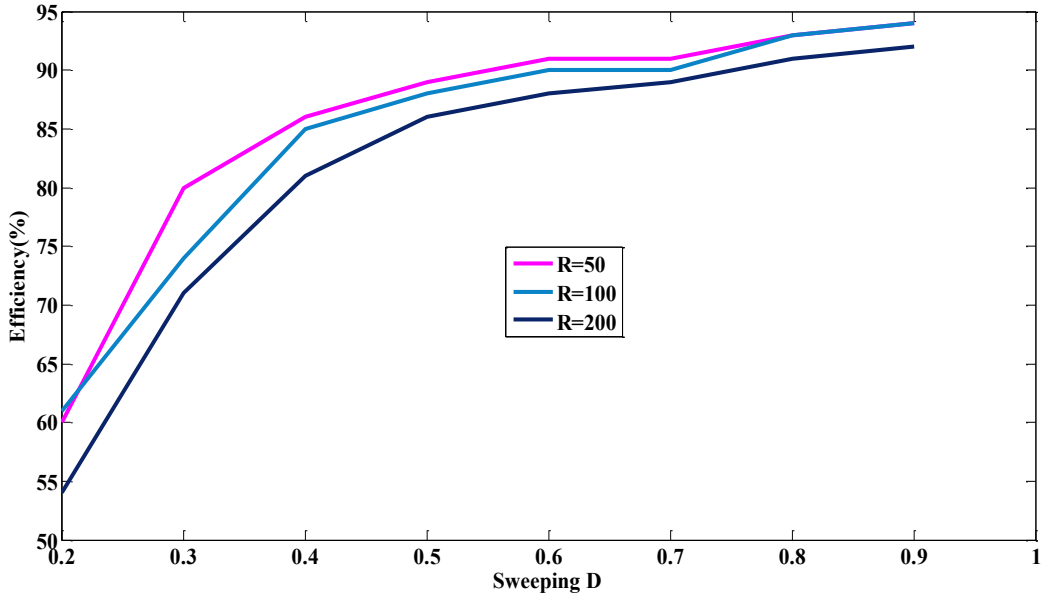

Fig. 5.22 Variation in efficiency with different load at different position

5.3.5 Performance at Step-up Frequency Operation

Output frequency and output voltage both can be increased in the proposed Buck-Boost cycloconverter only by changing the gate pulses to IGBTs. Performance at higher output frequencies also changes with duty cycle and switching frequencies. Table 5.4 shows performance of the circuit for step-up frequency operation of the proposed cycloconverter. Fig. 5.23 and 5.24 show the typical input current, input and output voltages for the proposed buck-boost cycloconverter with 30% and 70% duty cycles respectively at output frequency of 150 Hz. The switching frequency is set to 8 kHz for D=0.3 and 2 kHz for D=0.7 according to the open loop sliding control of this cycloconverter.

Table 5.4 Output behavior for output frequency double than input

D	f	Vo.max	Vo.rms	Iin.max	THD	Pf(in)	Pin	Pout	Ploss	η
0.2	10	58	28	0.95	6.99	0.269	21	8	6	57
0.3	8	106	46	0.98	15.32	0.524	46	21	8	72
0.4	6	148	67	1.03	17.46	0.781	97	46	12	79
0.5	4	216	88	1.34	11.99	0.909	169	78	17	82
0.6	3	339	125	2.32	10.52	0.984	332	156	23	87
0.7	2	496	169	4.51	9.88	0.993	618	286	35	89
0.8	1.5	712	224	8.85	14.38	0.851	1103	501	57	90
0.9	1	1602	247	18.21	10.91	0.597	1370	610	60	91

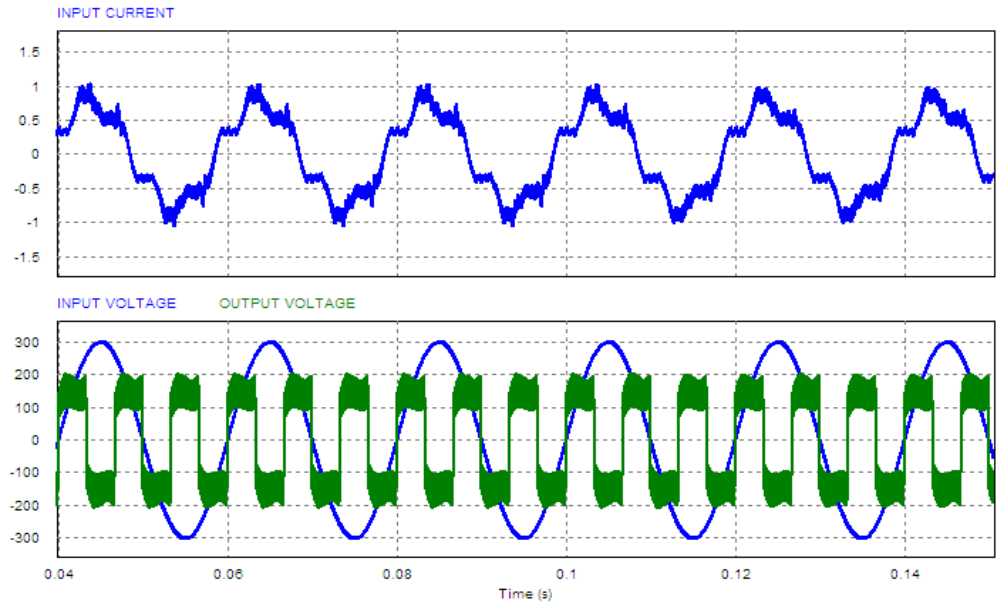

Fig. 5.23 Input current and Output & Input voltages at D=0.3 and f=8 KHz

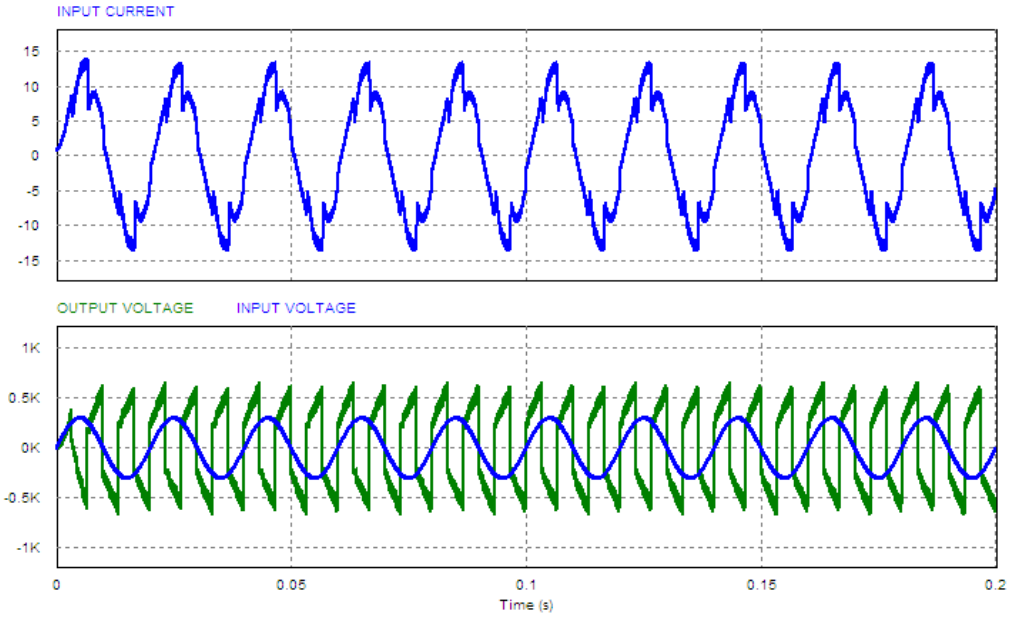

Fig. 5.24 Input current and Output & Input voltages at D=0.7 and f=2 KHz

5.3.6 Performance with R-L Load

The performance of the proposed Buck-Boost topology with R-L load is presented in Table 5.5. The resistance and inductance values for the R-L load are set to 25 ohm and 100 mH respectively. Here the control parameters (duty cycle and switching frequency) are maintained same as for the resistive loads. Typical input current, input and output voltage waveforms for R-L load is presented in Fig. 5.25 and 5.26 for 40% and 80% duty cycles respectively. Results show that the behaviors of the proposed cycloconverter under R and R-L loads are almost equivalent.

Table 5. 5 Performance of the proposed Buck-Boost cycloconverter with R-L load

D	f	Vo.max	Vo.rms	Iin.max	THD	Pf(in)	η
0.2	10	235.6	163.1	1.12	18.1	0.93	73.8
0.3	8	263.7	182.3	2.12	17.4	0.95	76
0.4	6	298.2	209.1	2.67	16.1	0.96	78.3
0.5	4	352	249.3	3.69	13.9	0.96	80.6
0.6	3	436.5	314.3	5.57	11.5	0.97	82.5
0.7	2	570.5	418.6	9.55	8.66	0.96	83.1
0.8	1.5	731.7	575.4	19.5	5.63	0.88	80.4
0.9	1	778.4	554.7	47.2	6.26	0.47	66.5

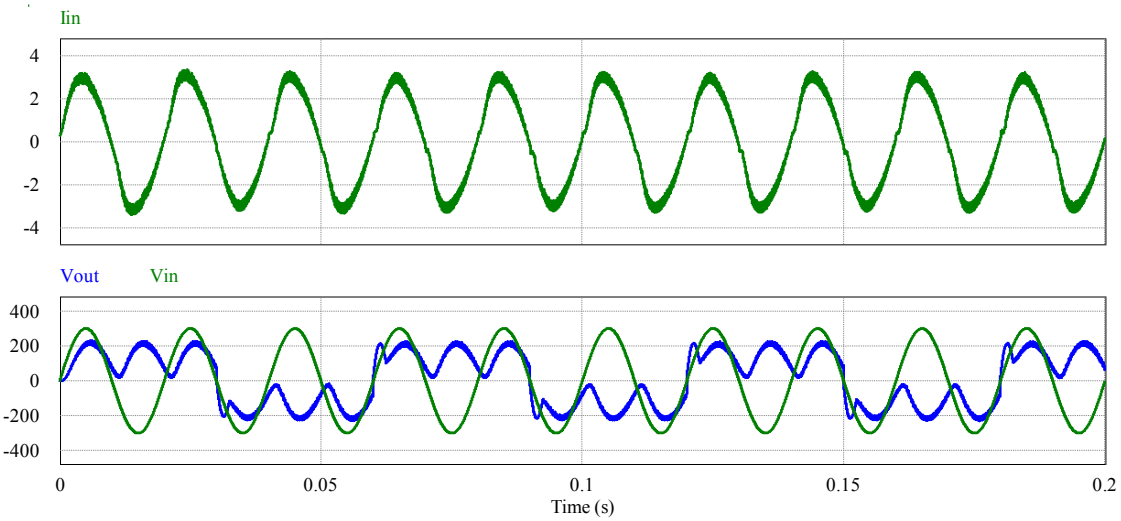

Fig. 5. 25 Input current, input and output voltage waveforms for R-L load with D = 0.4 and f=6 kHz

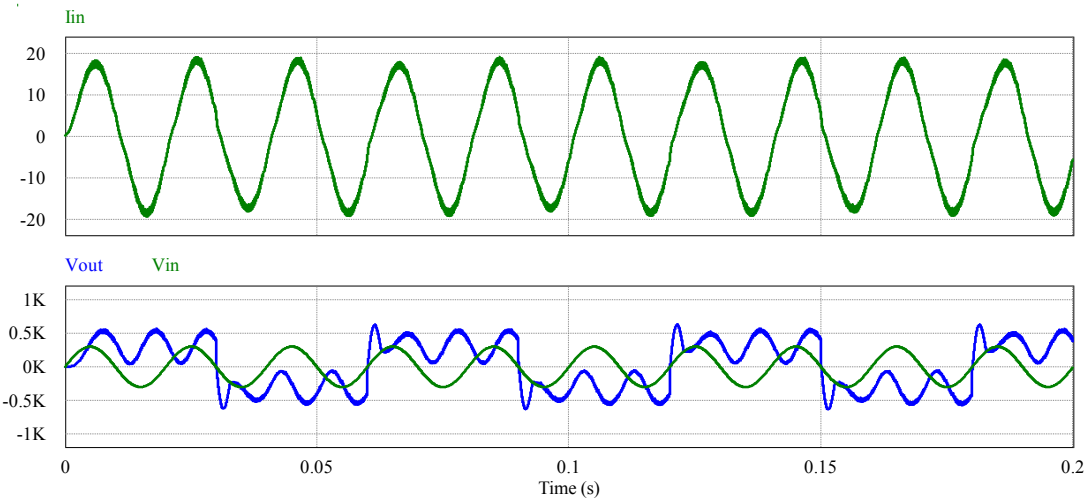

Fig. 5. 26 Input current, input and output voltage waveforms for R-L load with D = 0.8 and f=1.5 kHz

5.4 Discussion

The results presented in section 5.3 prove that the proposed Buck-Boost cycloconverter can provide AC-AC conversion at high efficiencies maintaining high power quality. Moreover, the proposed cycloconverter can increase or decrease output frequency effectively with high power quality. The proposed cycloconverter offers better flexibility than traditional cycloconverter with reduced switch and improved efficiency. Different control strategies can be employed to increase the efficiency of the converter further.

CHAPTER 6
ĆUK TOPOLOGY BASED CYCLOCONVERTER

The proposed circuit of this chapter is a combination of Ćuk converter and cycloconverter topology. Cycloconverters are AC to AC converters that change the RMS value as well as frequency of an AC signal. Likewise, a Ćuk converter is a DC to DC converter that changes the level of DC voltage to an upper or lower value. In our proposed circuitry, we have made use of the operations of both topologies along with rectification process to ensure variable frequency single phase AC output with high power quality from a single phase AC input.

6.1 Circuit Configuration

Fig. 6.1 shows the proposed scheme of Ćuk topology based cycloconverter. It changes the frequency as well as RMS value of a single phase AC input signal while the output is a single phase AC having different frequency and voltage. The control pulses of the proposed topology can be designed such that the topology is able to provide AC output both higher and lower than the supply voltage at frequencies higher or lower than the input frequency. Because of high frequency switching a small input filter is able to reduce the sub-harmonic components and improve the input current shape, reducing the THD of input current. A full-bridge rectifier converts the single phase AC to a DC voltage. The switch mode topology utilizes two converters analogical to the P and N converters of a typical cycloconverter. Each of these converters is separately based on Ćuk topology, which results in the positive and negative half cycle of the final AC output. The load is differentially connected between these two converters.

Fig. 6.1 presents the proposed Ćuk topology based cycloconverter. In this circuit L_{in} and C_{in} are the elements of the input filter. Four diodes D1-D4 comprise the single phase full bridge rectifier unit. S1, S2, S3, and S4 are the IGBT switches for the controlling purpose. S1, S4 works for P converter, and S2, S3 for N converter unit. S1 and S4 are switched on or off simultaneously. S2, S3 are also driven by the same control pulse. S1, S4 and S2, S3 are switched alternatively to construct the positive and negative half cycle of the output.

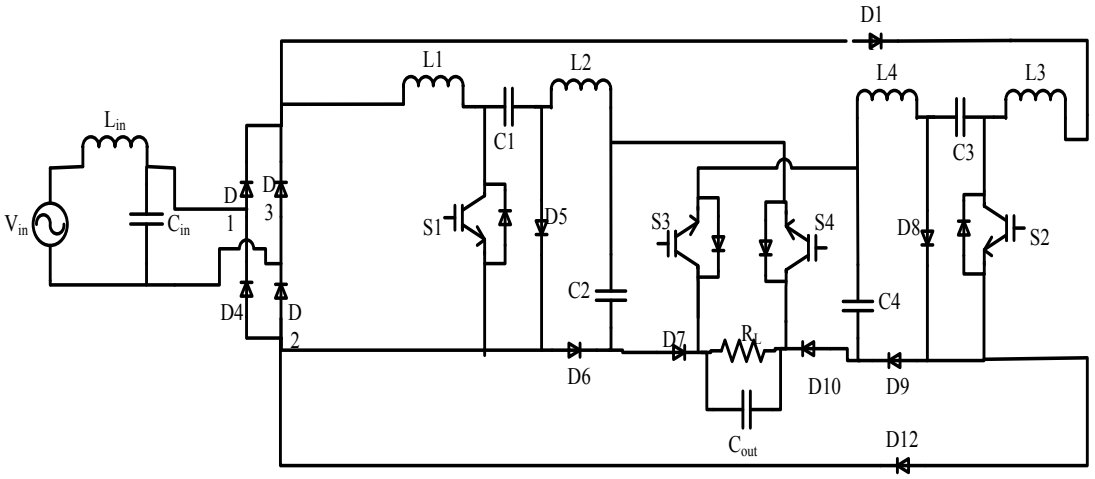

Fig. 6. 1 Circuit diagram of a cycloconverter based on Ćuk topology.

6.2 Operation

The proposed topology comprises of two basic topologies, Cycloconverter and Ćuk converter. For basic cycloconverter, operation can be defined in two steps: P-conversion and N-conversion. The switching scheme for the cycloconverter is indicated in Fig 6.2. For basic Ćuk converter, operation can be defined by charging and discharging of a capacitor, maintaining the current through the inductor always flowing in a single direction. Combining these two topologies, proposed Ćuk topology based cycloconverter operates in four different states:

1. P converter-switched ON state
2. P converter-switched OFF state
3. N converter-switched ON state
4. N converter-switched OFF state

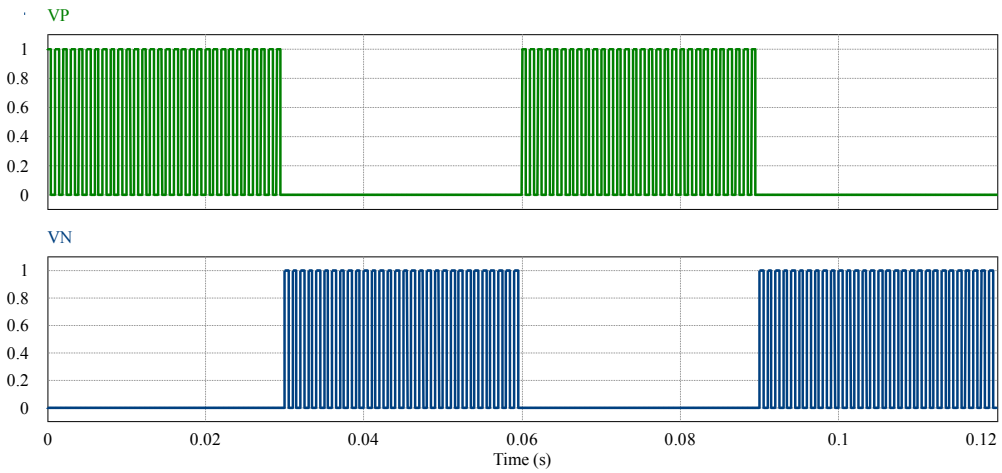

Fig. 6. 2 Switching characteristics of the P and N converter for Ćuk Topology

6.2.1 P converter

In the P–conversion cycle, the output is always positive irrespective of the polarity at the input. The P-converter can be realized from the Fig. 6.3 and the switching signal of the P-converter is given in Fig 6.4. The high frequency signal is to activate the switching topology. The low frequency signal is to initiate the P-converter only. By multiplying these 2 signals, P-converter is active at high switching frequency.

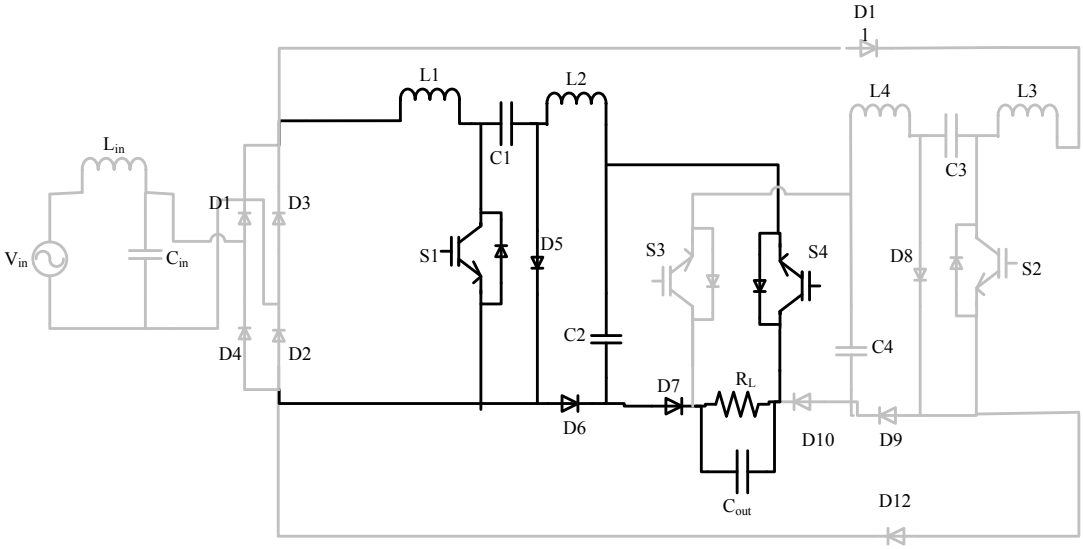

Fig. 6. 3 The Ćuk topology based P converter

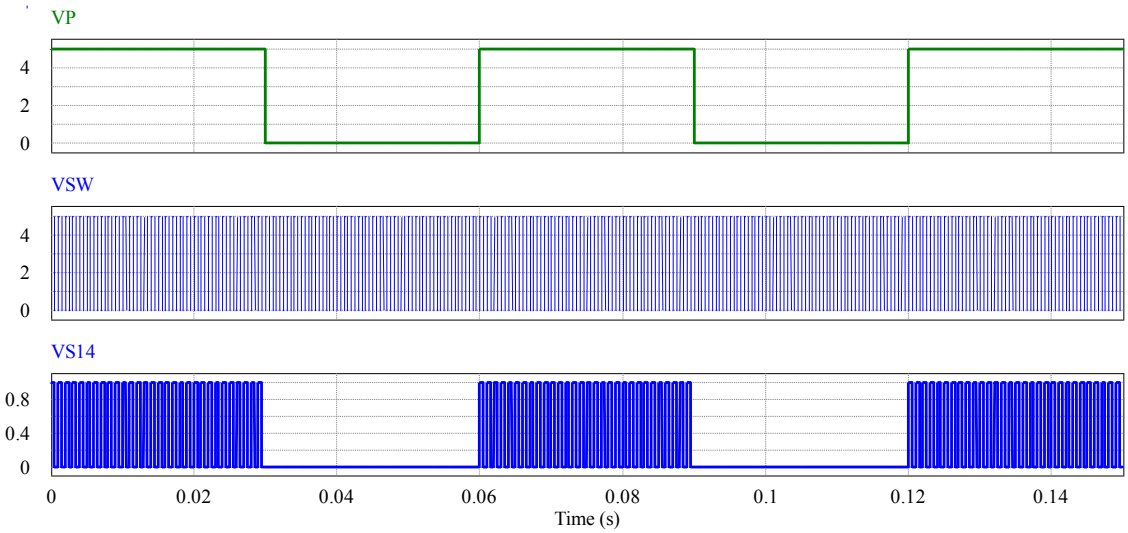

Fig. 6. 4 Switching scheme of the P-converter

6.2.1.A P converter-switched ON state

Fig. 6.5 shows the direction of current once P converter is switched on. Here S1 and S4 are turned on simultaneously. Current flows through L1 and L2 and then they combine together flowing through S1 which acts ideally as a short circuit. C1 is charged with the positive polarity at right as shown in Fig. 6.5. Another loop is created combining L2, C1 and C2 and positive polarity appears at the bottom of C2. Current is also flowing through the output via the loop created by S4. If a voltmeter is connected across the load with its positive terminal at left then it will show positive voltage across the load. D7 ensures unidirectional flow through the load as well as provides unidirectional charging to the associated capacitors. This converter is denoted as the P-converter. As D10 is at reverse bias condition, the current through the output cannot effect the N-converter components. The switches S1 and S4 are ON when the input signal at their gate is HIGH, and turned OFF when the gate signal is LOW. This is shown in Fig. 6.6.

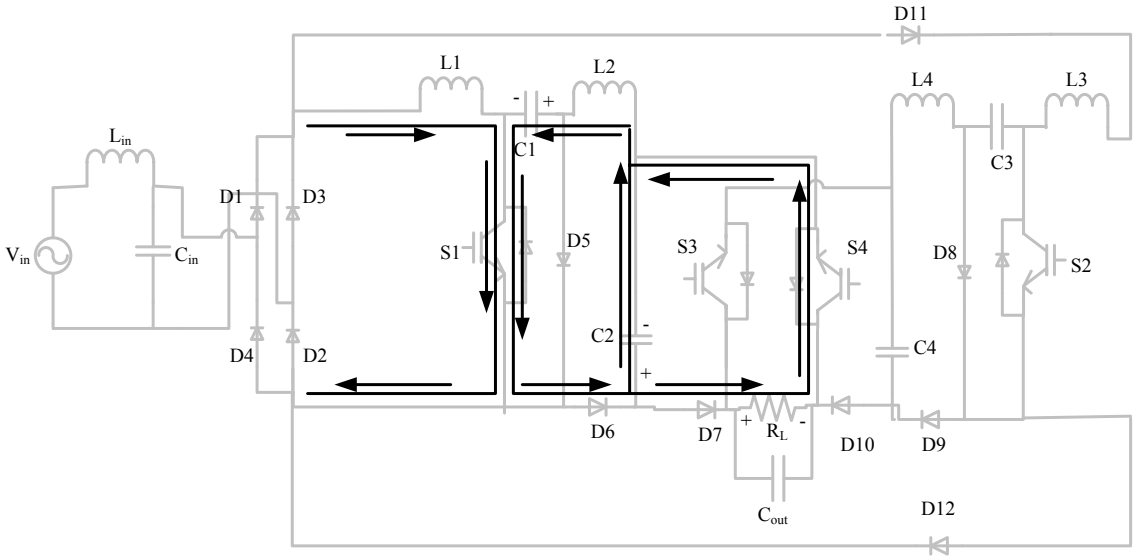

Fig. 6. 5 Current flow path in Ćuk P converter switched ON mode

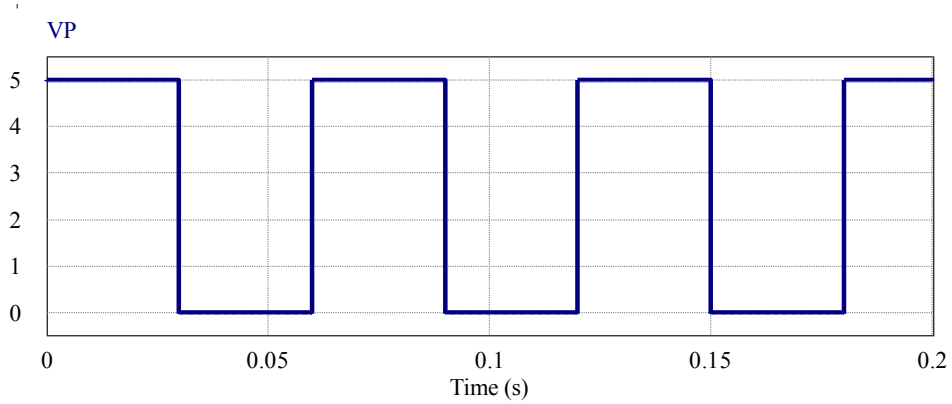

Fig. 6.6 On-Off cycle of the switches of P-converter

6.2.1.B P converter-switched OFF state

During the switched OFF state, S1, S4 are turned off at the same time. The changed current directions are shown in Fig. 6.7. We know that current through the inductors cannot change instantaneously. For this, L1 and L2 will continue to flow in the previous directions. The polarity of C1 changes as it discharges. All these conditions forces D5 on. An internal loop forms with L2, D5, and C2 in which current flows in counterclockwise direction as shown in Fig. 6.7 and C2 gets charged maintaining the same polarity. The output capacitor discharges by supplying current to R_L thereby stabilizing the output voltage. The time constant of C_{out} is chosen sufficiently large enough so that it holds the output voltage steady without being discharged quickly.

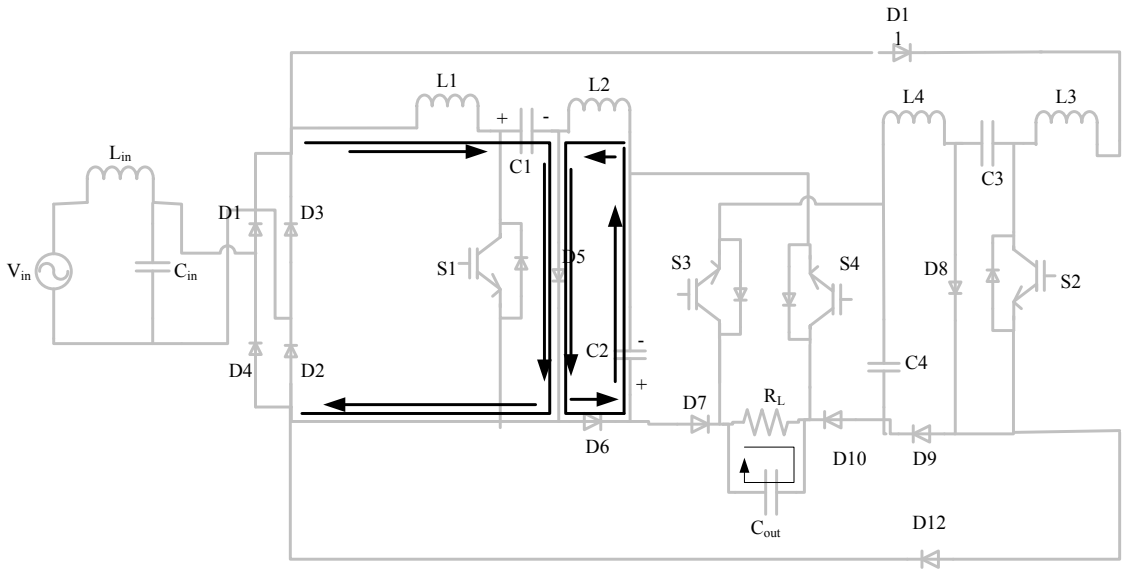

Fig. 6.7 Current flow path in Ćuk P converter switched OFF mode

6.2.2 N converter

At the N –conversion cycle, the output is always negative irrespective of the polarity at the input. The N-converter can be realized from the Fig. 6.8. The switching scheme of the N-converter is similar to that of the P-converter. P-converter is completely deactivated from the circuit when the N-conversion is in operation.

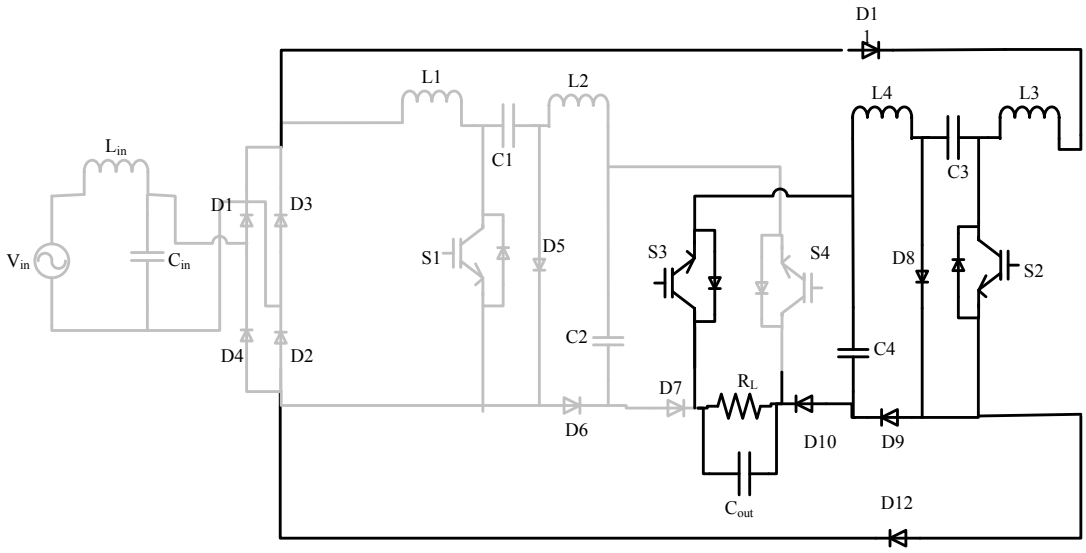

Fig. 6.8 The proposed Ćuk topology based N converter

6.2.2.A N converter-switched ON state

The current flow directions of the N-converter during switches S2 and S3 are On is shown in Fig. 6.9. The dc output of the rectifier forces current to flow through L3 along the shown direction. Current also flows through an internal loop comprising L4, C3, and C4. Current through L3 and L4 are combined together and flow via S1, which acts as a short circuit. C3 is charged with the positive polarity at left and C4 is charged with positive polarity appearing at the bottom as shown in Fig. 6.9. Current is also flowing through the output via the loop created by S3. If a voltmeter is connected across the load with its positive terminal at left then it will show negative voltage across the load. D9 ensures unidirectional flow through the load as well as provides unidirectional charging to the associated capacitors. As D7 is at reverse bias condition, the current through the output cannot effect the P-converter components.

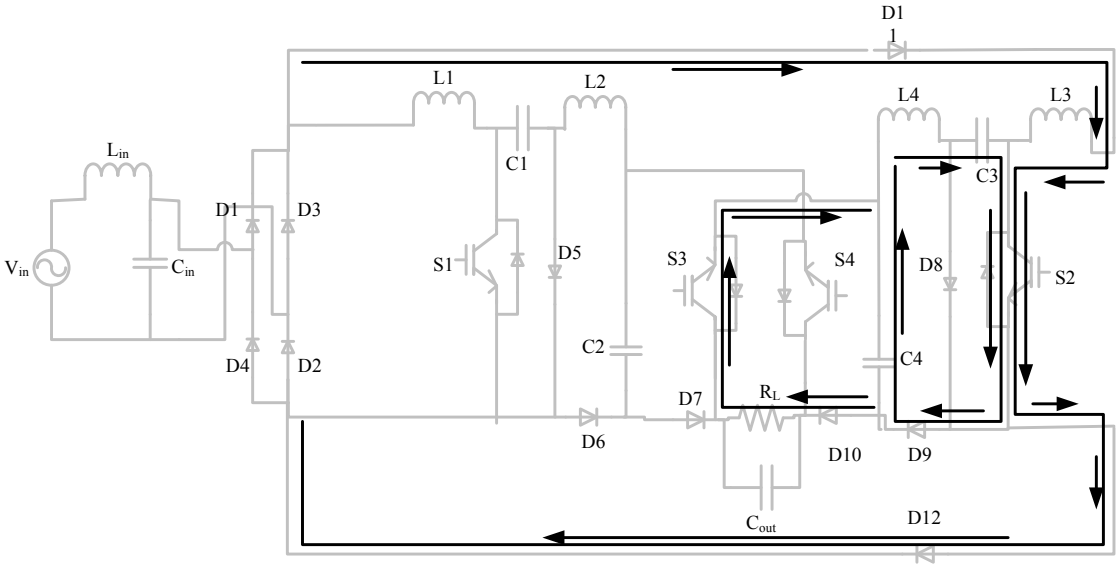

Fig. 6.9 Current flow path in N converter switched on mode

6.2.2.B N converter-switched OFF state

When the switches S1 and S4 are turned off the switch OFF state of the N converter occurs. The changed current directions are shown in Fig. 6.10. The current through the inductors cannot change instantaneously. For this, L3 and L4 will continue to carry current in the previous directions. The polarity of C3 changes as it discharges. All these conditions forces D8 on. An internal loop forms with L4, D8, and C4 in which current flows in counterclockwise direction as shown in Fig. 6.10 and C4 gets charged maintaining the same polarity. The output capacitor discharges by supplying current to R_L, thereby, stabilizing the output voltage. The time constant of C_{out} is chosen sufficiently large enough so that it holds the output voltage steadily without being discharged quickly.

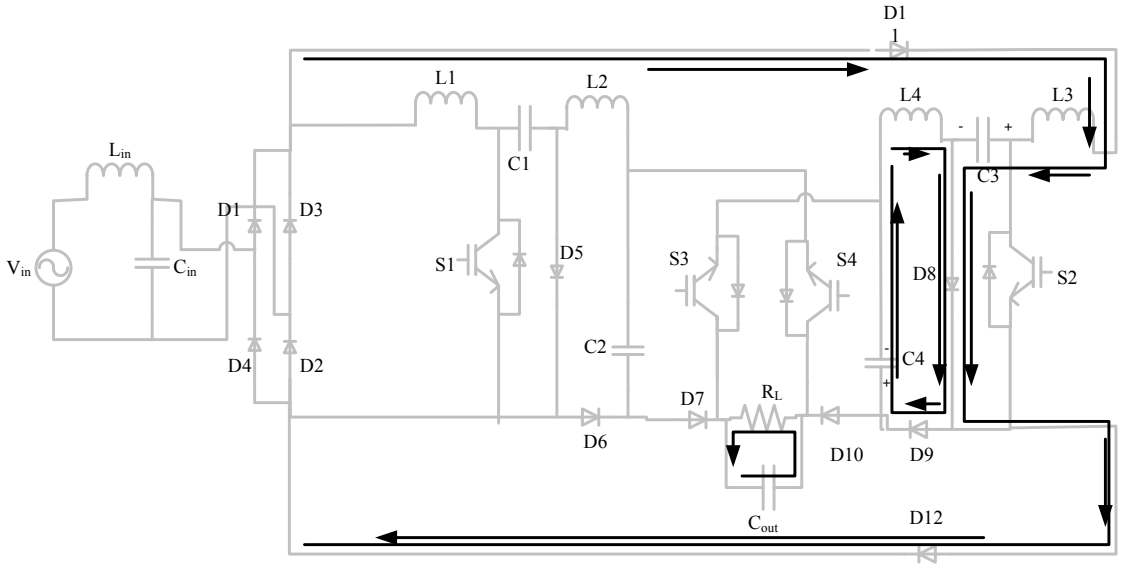

Fig. 6.10 Current flow path in N converter switched off mode

6.3 Simulation Results

The way the proposed circuitry differs from conventional cycloconverter is the simpler control circuit with reduced number of switches. Generally for a single phase cycloconverter eight SCR switches are needed, the proposed cycloconverter requires only 4 solid state switches. It reduces the size, complexity and cost of the cycloconverter. The performance of the proposed circuitry was examined using PSIM software. The performance of this cycloconverter is analyzed under different load conditions. It has shown satisfactory input power factor, input current THD and operates at high efficiencies.

6.3.1 Performance at Variable Control Conditions

Table 6.1 presents the results of the proposed Ćuk cycloconverter at different duty cycles for different frequencies. The result from simulation shows that for a particular duty cycle the performance of the proposed converter varies with different frequencies. From the set of values presented in Table 6.1 an optimum operating point, designated by a specific duty cycle is selected for a specific frequency.

Table 6.1 PSIM simulation results for different switching frequencies and duty cycles

D	f (kHz)	Input pf	THD (%)	η (%)
0.3	10	.99	6.2	75.6
	12	.99	7.78	72.7
	14	.98	6.57	67.89
	16	.98	4.76	65.4
0.4	8	.98	5.73	78
	10	.97	5.98	76.55
	12	.975	5.77	73.6
	14	.975	5.96	68.46
0.5	7.5	.95	6.5	75.1
	7	.95	6.3	76.2
	6.5	.958	5.98	75.8
	6	.962	5.7	82.3
0.6	6	.933	5.32	75.8
	4	.935	5.1	85.72
	3.5	.94	5.1	75.25
	3	.943	5.19	75.3
0.7	3.5	.88	4.3	80.8
	4	.88	4.42	74.6
	6	.883	4.438	74.345
	8	.89	4.6	73.02
0.8	3	.8	4.06	82.87
	5	.78	4.01	73
	6	.776	3.84	71.7
	8	.773	3.757	71.66
0.9	1.5	.47	2.5	67.6
	2	.53	2.9	78
	4	.525	7.38	63.8
	6	.516	4.58	63.5

6.3.2 Open Loop Sliding Control

The values of duty cycles and frequencies that obtain optimum operating conditions for the proposed Ćuk cycloconverter are used as the open loop sliding control parameters. The results of open loop sliding control for the proposed Ćuk cycloconverter are presented in Table 6.2 for 100 ohm resistive load.

Table 6.2 Results from the open loop sliding control of the converter

Duty cycle	Switching frequency (kHz)	Input current (RMS)	Input current THD (%)	Input power factor	Output voltage (RMS)	Efficiency (%)
0.3	10	5.99	6.2	0.99	126.9	75.6
0.4	8	8.67	5.73	0.98	220.22	78
0.5	6	11.7	5.7	0.962	402.47	82.3
0.6	4	15.76	5.1	0.935	591.42	85.72
0.7	3.5	21.45	4.3	0.88	787.51	80.8
0.8	3	27.34	4.06	0.8	850.5	82.87
0.9	2	38	2.9	0.53	889.35	78

For the proposed Ćuk topology based cycloconverter the sliding frequency values are presented in Fig. 6.11. This figure shows the open loop sliding control graph for the proposed buck-boost cycloconverter.

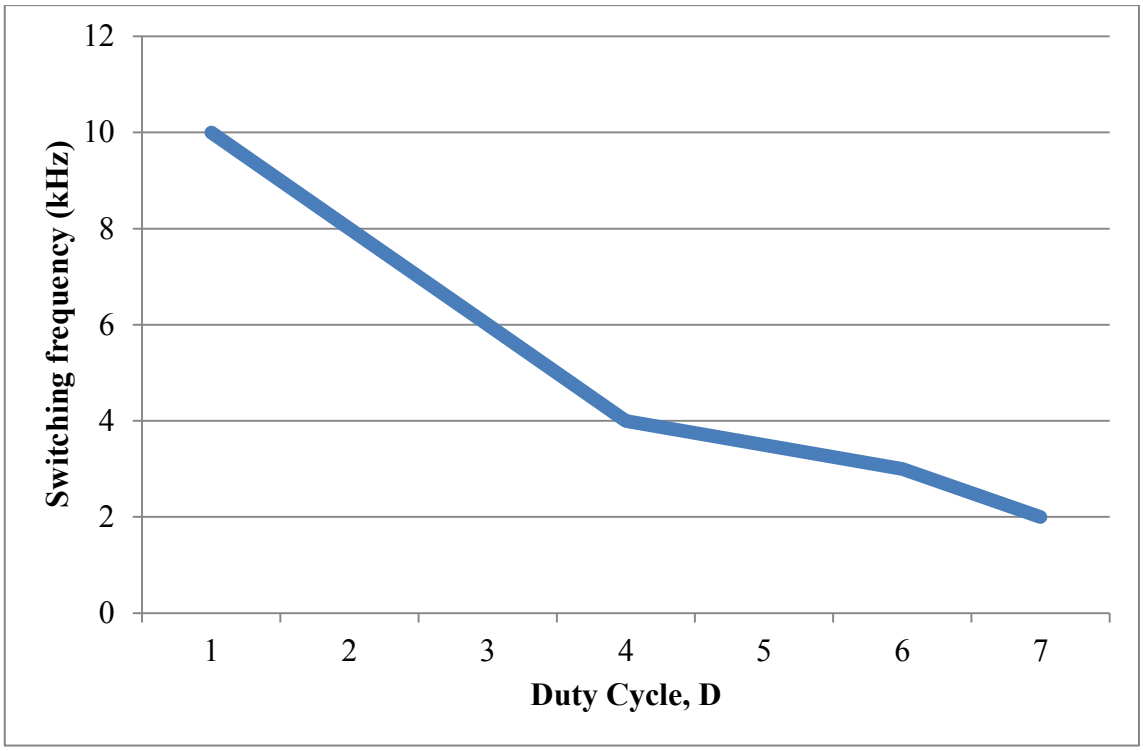

Fig. 6.11 Sliding characteristics of the Ćuk cycloconverter

6.3.3 Typical Waveforms

Fig. 6.12 shows typical input current, input and output voltages for the proposed Ćuk cycloconverter with 50% duty cycle. The switching frequency is set to 6 kHz as determined form the open loop sliding control of this cycloconverter. For D=0.5 the output voltage is almost equal to the input voltage, as should be the case in ideal Ćuk converter. Fig. 6.13 shows the waveforms for D=0.3 and switching frequency of 10 kHz. In this case, the output voltage is smaller than the input voltage ($V_{out} < V_{in}$ for $D < 0.5$)

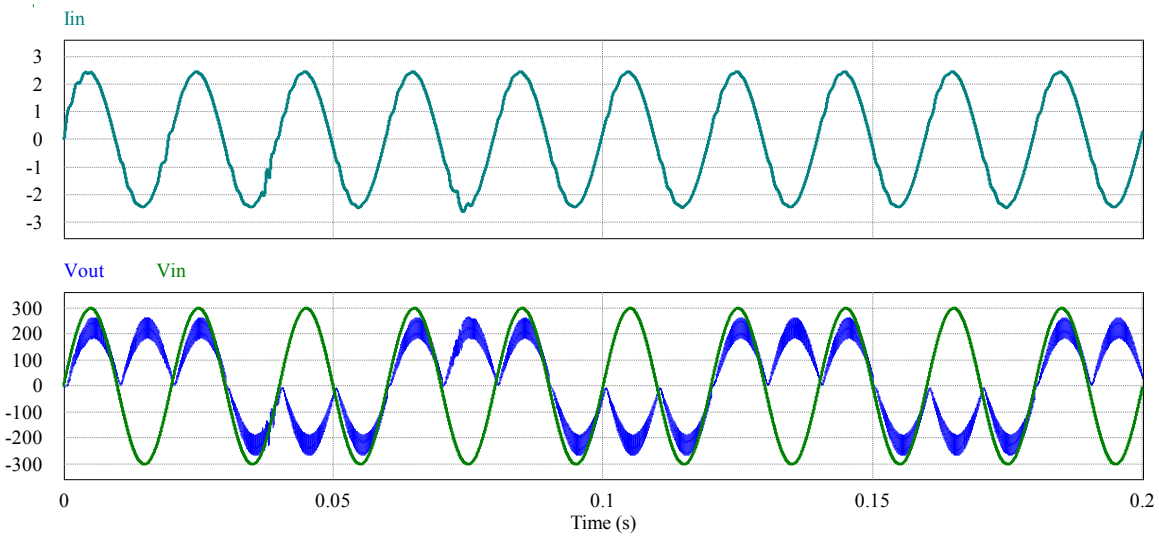

Fig. 6. 12 Input current, input voltage and output voltage at D=0.5, f=6000 Hz

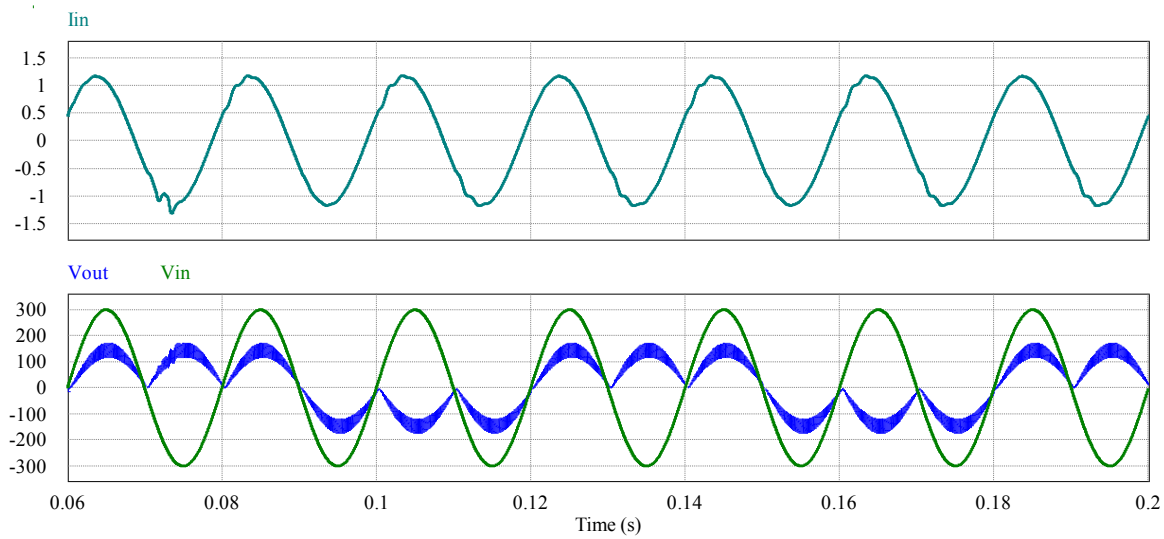

Fig. 6.13 Input current, input voltage and output voltage with D=0.3, f=10 kHz

Fig 6.14 shows typical input current, input and output voltages for the proposed Ćuk cycloconverter with 70% duty cycle. The switching frequency is set to 3.5 kHz according to the open loop sliding control of this cycloconverter. For D=0.7, the output voltage is much larger than the input voltage ($V_{out} > V_{in}$ for $D > 0.5$)

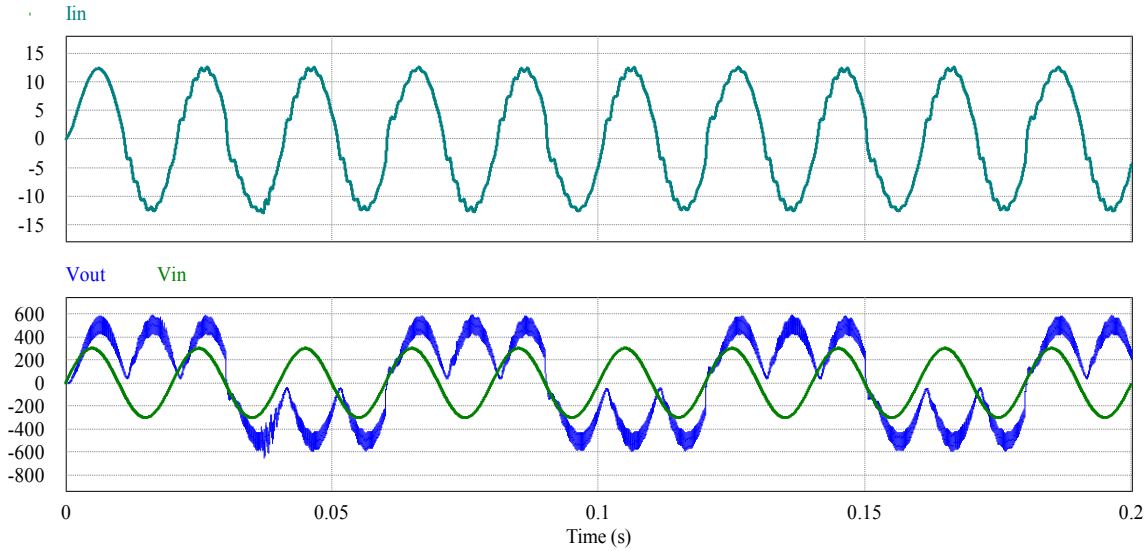

Fig. 6.14 Input current, input voltage and output voltage with D=0.8 , f=3.5 kHz

Spectrum of the input current of Fig. 6.13 is shown in Fig. 6.15 which shows a small magnitude of current near 10 kHz (the switching frequency). It is evident that these circuits can reduce the input current harmonic distortion.

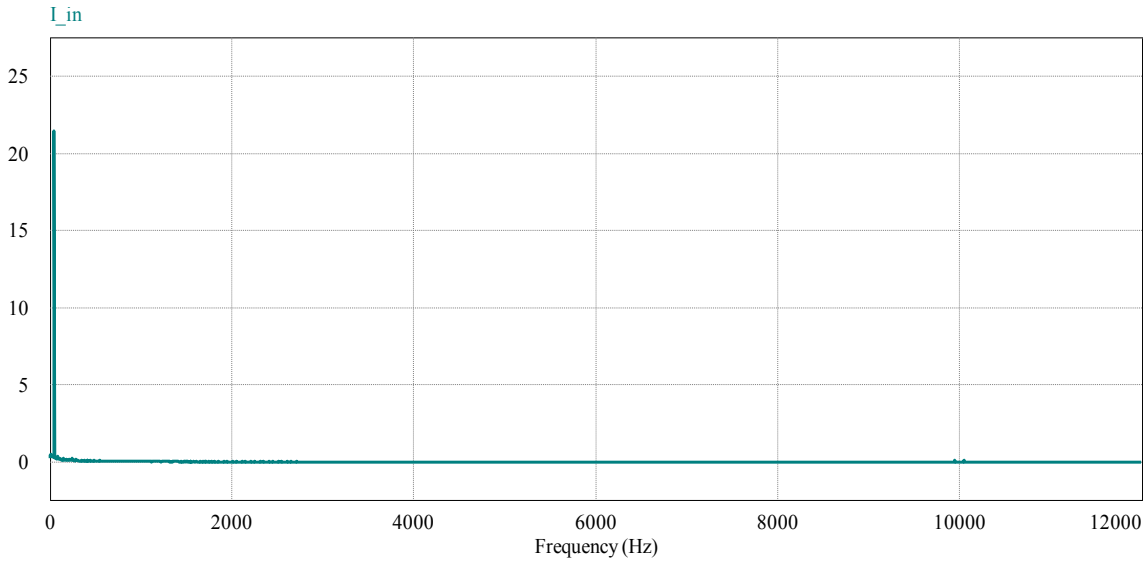

Fig. 6.15 Spectrum of the input current for D= 0.3 and f = 10 kHz

6.3.4 Performance at Variable Load Conditions

Table 6.3 shows the performance of the proposed Ćuk cycloconverter with variable resistive loads. It is observed from the results presented in Table 6.3 and Figs. 6.16, 6.17 and 6.18 that variation of load has little effects on the input current THD of the proposed converter. However, with the increment of load resistance the input power factor and efficiency slightly degrades at lower duty cycles of the proposed Ćuk cycloconverter.

Table 6.3 Proposed Ćuk cycloconverter performance at varying loads

D	f	R=50			R=100			R=200		
		Input pf	THD (%)	η (%)	Input pf	THD	η (%)	Input pf	THD (%)	ŋ (%)
0.3	10	0.99	5.5	76.7	0.99	6.2	75.6	0.989	8.92	68.17
0.4	8	0.977	5.511	78.6	0.98	5.73	76	0.98	6.87	65.45
0.5	6	0.96	5.327	78.18	0.962	5.7	75.3	0.962	6.077	68.4
0.6	4	0.93	5.08	77.8	0.935	5.1	75.72	0.939	5.86	68.50
0.7	3.5	0.88	4.5	76.66	0.88	4.3	74.9	0.884	5.07	67.4
0.8	3	0.79	4.15	73.8	0.8	4.06	73	0.8	4.11	66.41
0.9	2	0.52	6.08	65.35	0.53	2.9	65	0.533	2.66	61.36

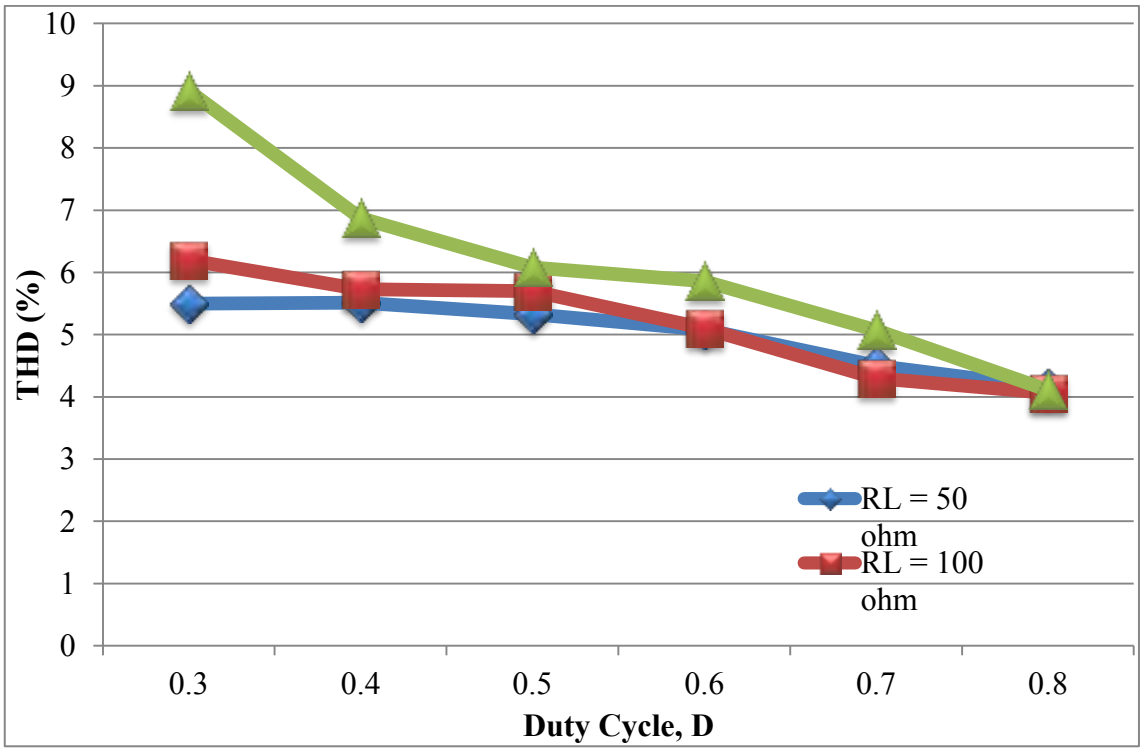

Fig. 6.16 Variation of input current THD(%) of different loads at different sliding points

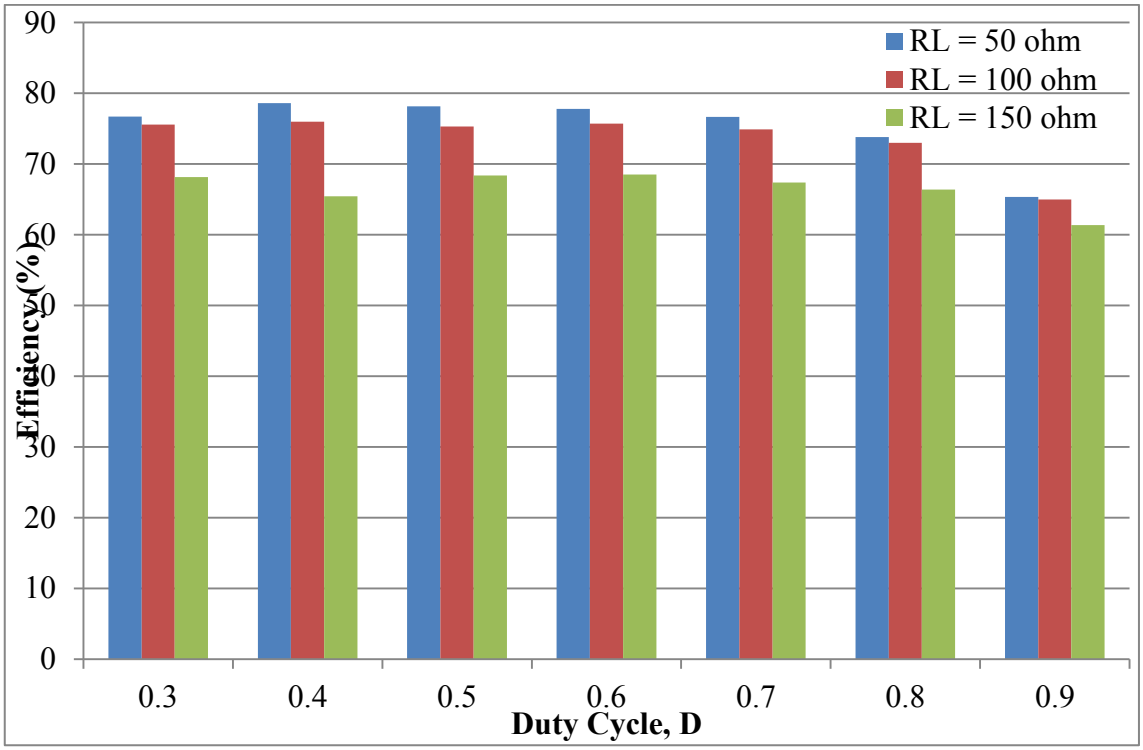

Fig. 6.17 Variation of efficiency of different loads at different sliding points

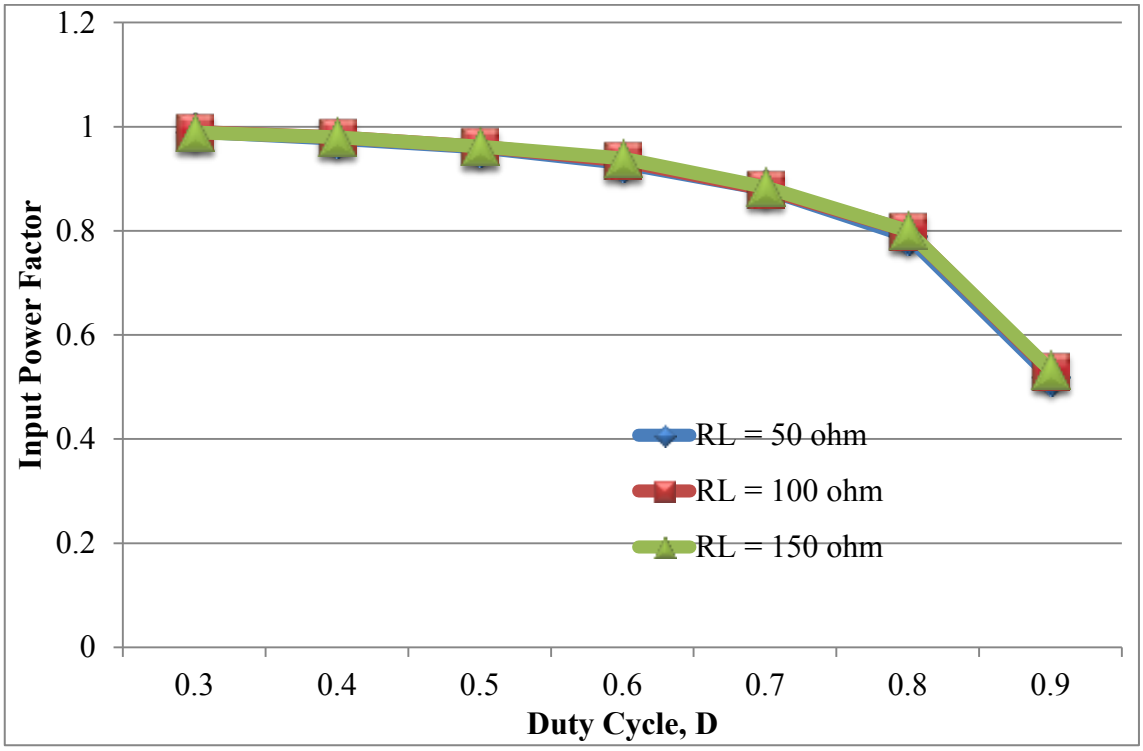

Fig. 6.18 Variation of input power factor of different loads at different sliding points

6.3.5 Performance of Step-up Frequency Operation

Output frequency and output voltage both can be increased in the proposed Ćuk cycloconverter by changing the gate pulses to IGBTs. Performance at higher output frequencies also changes with duty cycle and switching frequencies. Table 6.4 shows performance of the circuit for step-up frequency operation of the proposed cycloconverter. Fig. 6.19 and 6.20 show the typical input current, input and output voltages for the proposed Ćuk cycloconverter with 60% and 30% duty cycles respectively at output frequency of 150 Hz. The switching frequency is set to 4 kHz for D=0.6 and 10 kHz for D=0.3 according to the open loop sliding control of this cycloconverter.

Table 6.4 Simulation results for output frequency 150 Hz

Duty cycle	Switching frequency (Hz)	Input current (RMS)	Input current THD(%)	Input power factor	Output voltage (RMS)
0.3	10	6.48	6.7	0.99	156.9
0.4	8	9.13	6.06	0.98	250.22
0.5	6	12.1	5.46	0.96	432.47
0.6	4	15.9	5.02	0.93	621.42
0.7	3.5	21.35	4.5	0.88	754.51
0.8	3	27.26	4.15	0.79	851.5
0.9	2	37.9	2.9	0.53	932.35

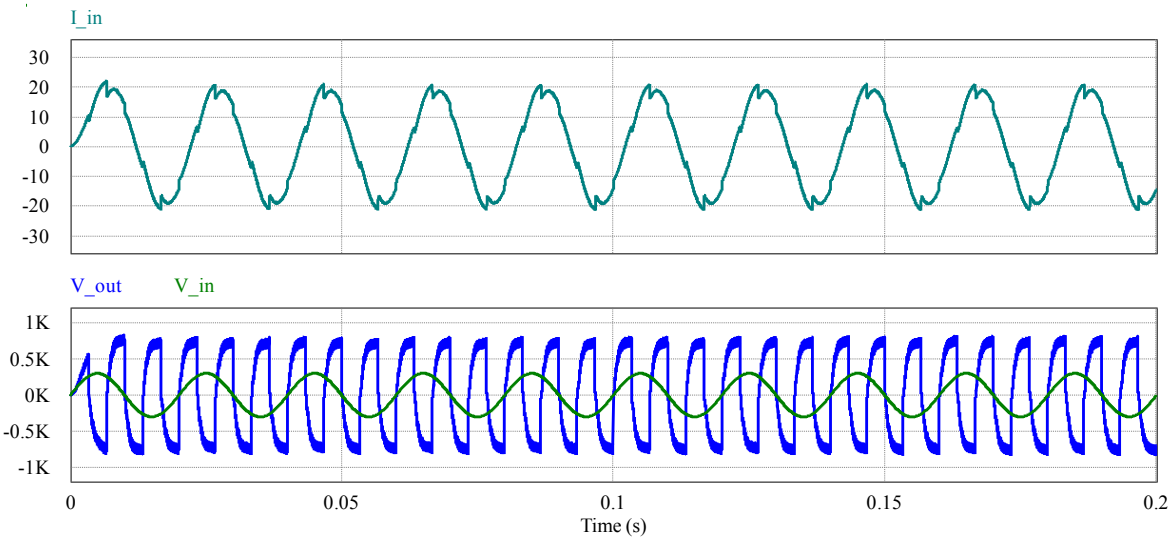

Fig. 6.19 Input current, input voltage and output voltage with D=0.6 , f=4 kHz

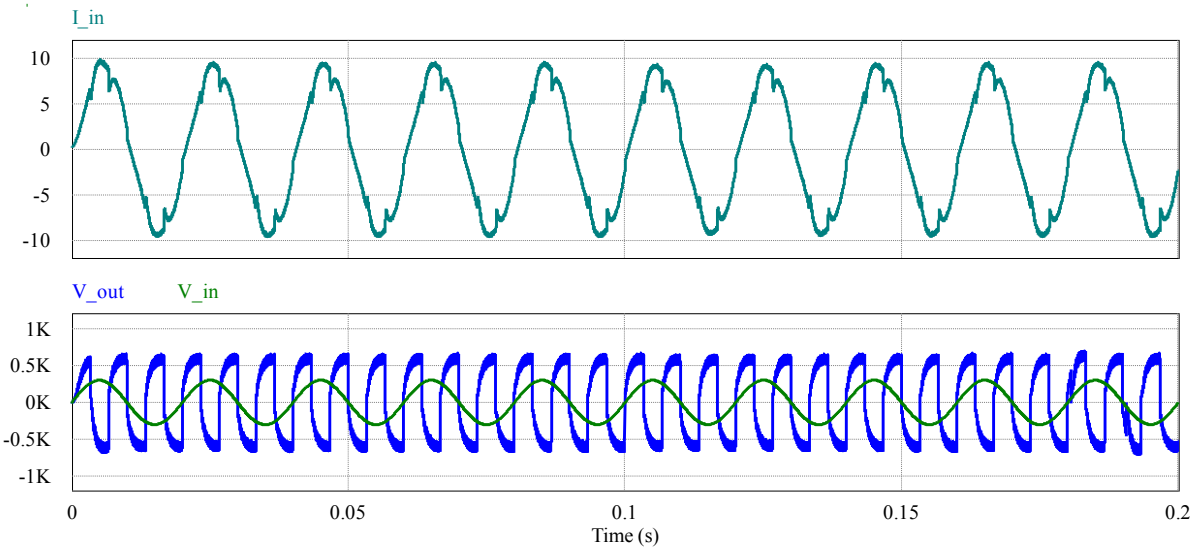

Fig. 6.20 Input current, input voltage and output voltage with D=0.3 , f= 10 kHz

6.3.6 Performance with R-L Load

The performance of the proposed Ćuk topology with R-L load is presented in table 6.5. The resistance and inductance values for the R-L load are set to 25 ohm and 100 mH respectively. Here the control parameters (duty cycle and switching frequency) are maintained same as for the resistive loads. Typical input current, input and output voltage waveforms for R-L load is presented in Fig. 6.21 and 6.22 for 40% and 80% duty cycles respectively. Results show that the behaviors of the proposed cycloconverter under R and R-L loads are almost similar.

Table 6.5 Performance of the proposed Ćuk cycloconverter with R-L load

D	f	Vo.max	Vo.rms	Iin.max	THD	Pf(in)	η
0.2	10	235.6	163.1	1.12	18.1	0.93	73.8
0.3	8	263.7	182.3	2.12	17.4	0.95	76
0.4	6	298.2	209.1	2.67	16.1	0.96	78.3
0.5	4	352	249.3	3.69	13.9	0.96	80.6
0.6	3	436.5	314.3	5.57	11.5	0.97	82.5
0.7	2	570.5	418.6	9.55	8.66	0.96	83.1
0.8	1.5	731.7	575.4	19.5	5.63	0.88	80.4
0.9	1	778.4	554.7	47.2	6.26	0.47	66.5

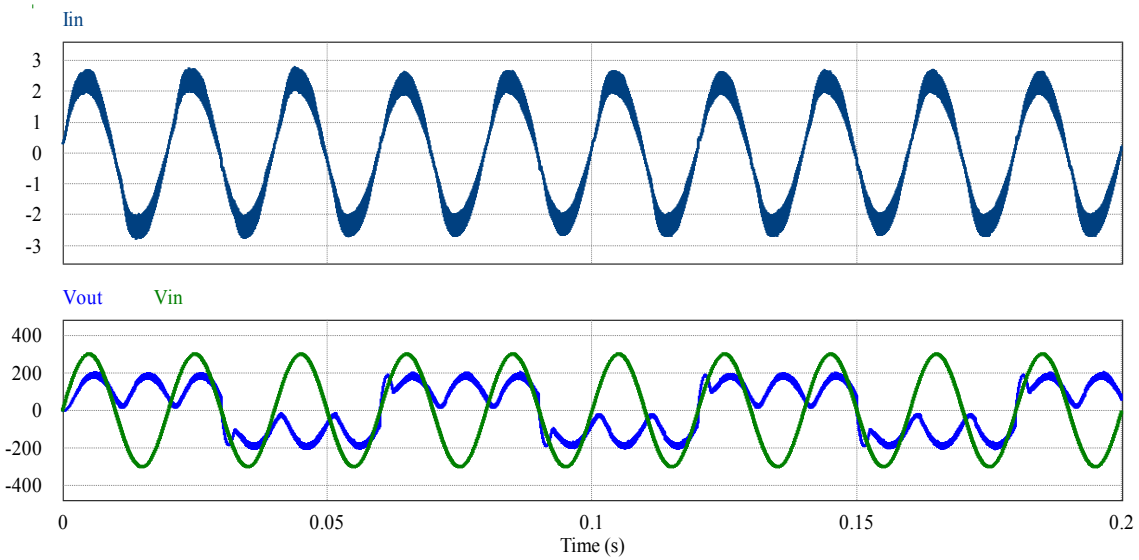

Fig. 6.21 Input current, input and output voltage waveforms for R-L load with D = 0.4 and f=6 kHz

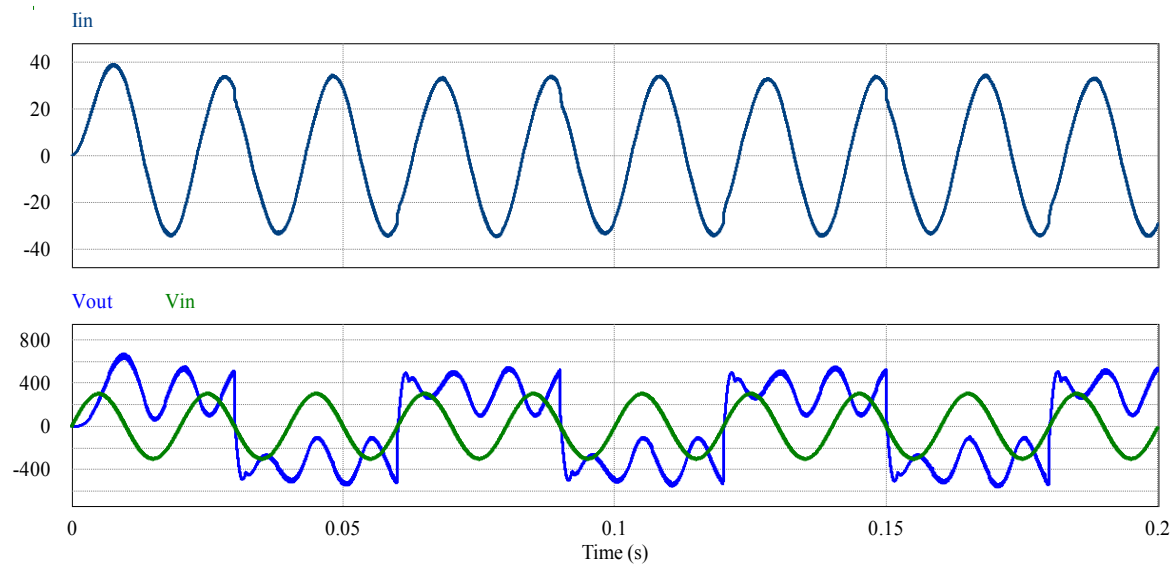

Fig. 6.22 Input current, input and output voltage waveforms for R-L load with D = 0.8 and f=1.5 kHz

6.4 Discussion

The results presented in section 6.3 prove that the proposed Ćuk cycloconverter can provide AC-AC conversion at moderately high efficiencies maintaining high power quality. Moreover, the proposed cycloconverter can increase or decrease output frequency effectively with high power quality. The proposed cycloconverter offers better flexibility than traditional cycloconverter with reduced switch and improved efficiency. Different control strategies can be employed to increase the efficiency of the converter further.

CHAPTER 7
SINGLE PHASE BOOST CYCLOCONVERTER

Boost converter refers to the switch mode topology that provides controllable output voltage greater than the supply by varying the duty cycle of the control pulse. In the proposed single phase cycloconverter based on Boost topology the P and N converters are configured as the corresponding switch mode scheme. This chapter presents analysis of the configuration, operation and performance of the proposed single phase Boost cycloconverter.

7.1 Circuit Configuration

The circuit diagram of the proposed Boost cycloconverter topology is presented in Fig. 7.1. The resistive load R_{Load} is differentially connected between the P-converter and N-converter. The output capacitor, C_{Load} stabilizes the output voltage across the load. Switch S11 and S12 are used to chop the P-converter input. Switch S21 and S22 are used to chop the N-converter input.

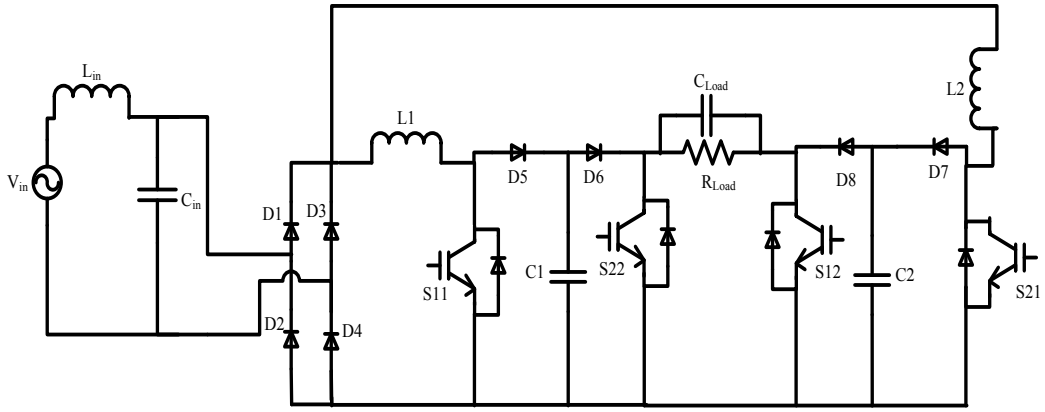

Fig. 7.1 Proposed single phase cycloconverter based on Boost topology

C1, L1 and C2, L2 are the functioning capacitors and inductors for P and N-converter respectively. The diodes D1, D2, D3, and D4 form a full-bridge rectifier which allows the AC input from the supply to maintain a unidirectional input at the converter circuit. Diodes D6 and D8 are used to restrict current flow in backward direction from the load for P and N-converter respectively. Diodes D5 and D7 provide the discharging path for the capacitors C1 and C2 respectively when the corresponding switches are in OFF position.

7.2 Operation

The proposed circuit comprises of two basic topologies, Cycloconverter and Boost converter. For basic cycloconverter, operation can be defined in two steps: P-conversion and N-conversion. The switching scheme for the cycloconverter is shown in Fig 7.2. For basic Boost converter, operation can be defined by charging and discharging of a capacitor, maintaining the current through the inductor always flowing in a single direction. Combining the switching conditions for the P and N-converters, the proposed Boost topology based cycloconverter operates in four different states:

1. Switch ON in P-converter
2. Switch OFF in P-converter
3. Switch ON in N-converter
4. Switch OFF in N-converter

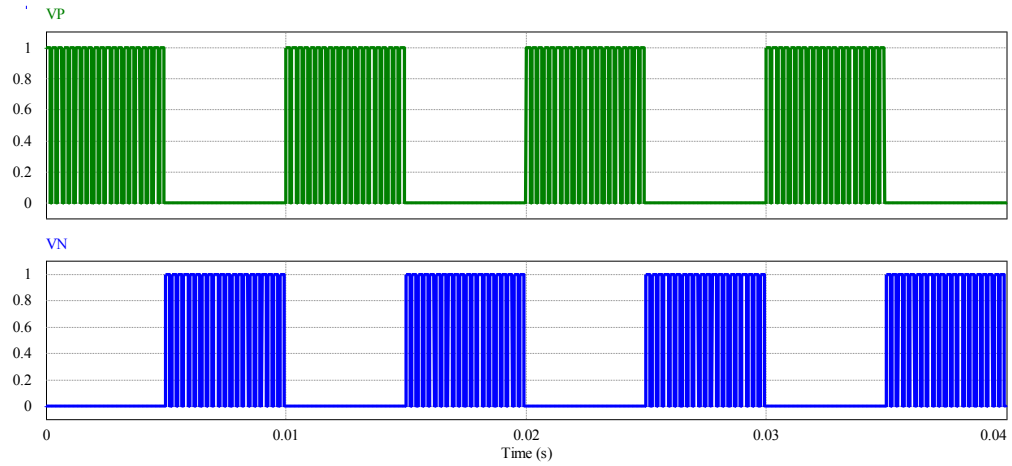

Fig. 7.2 Switching characteristics of the P and N converter for Boost Topology

It is clear from the figure, that only one converter's switching scheme is active at a time. When P-converter is in operation, the N-converter switches are completely in OFF position, and vice versa.

7.2.1. The P-converter

At the P–conversion cycle, the output is always positive irrespective of the polarity at the input. The P-converter can be realized from the Fig. 7.3. The switching of the P-converter is shown in Fig 7.4. The high frequency signal is to activate the switching

topology. The low frequency signal is to initiate the P-converter only. By multiplying these 2 signals, P-converter is active at high switching frequency. In Fig. 7.4 V_{sw}, V_P, and V_{S11} indicate the switching pulse, the ON time pulse for the P-converter and the control pulse for the solid state switch, S11 at the Boost cycloconverter in the circuit of Fig. 7.1.

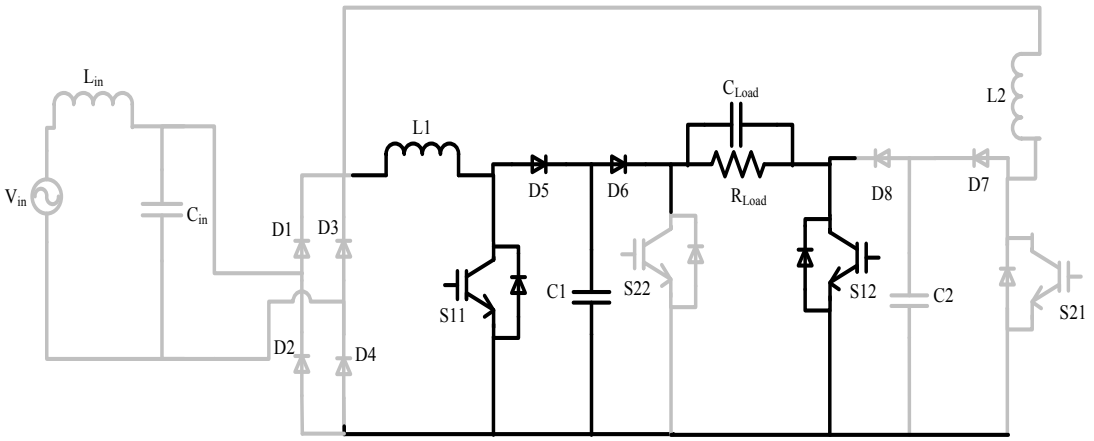

Fig. 7.3 Boost topology based P-converter

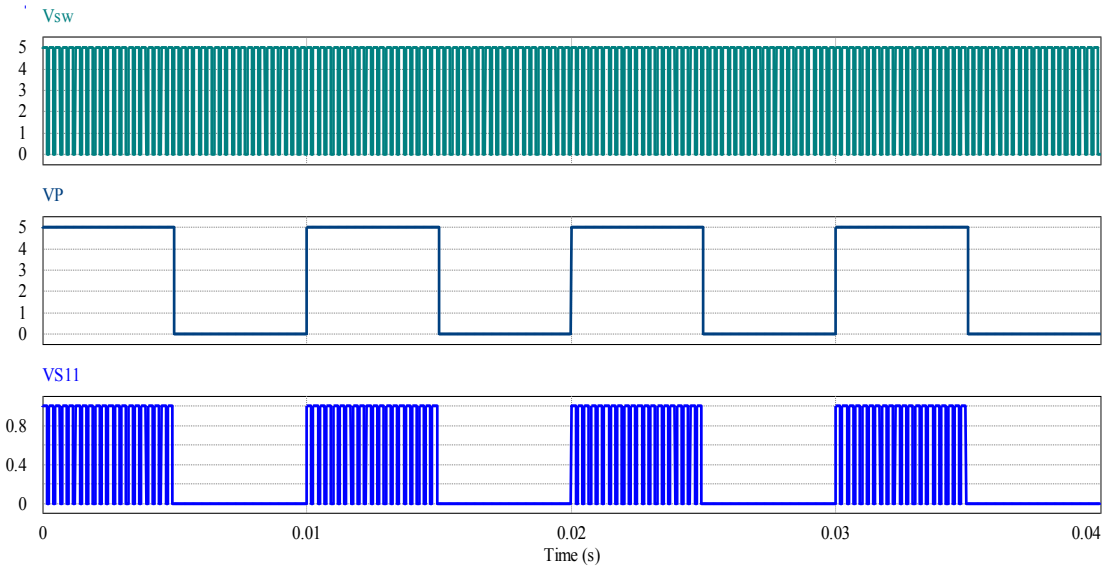

Fig. 7.4 Switching scheme of the P-converter

7.2.1.A Switch S11 on in P-converter

The high frequency switching signals for S11 and S12 are complementary for the proposed boost topology. When the switch S11 is ON in the P-conversion cycle, the inductor is charged. The current flow diagram is presented in Fig. 7.5. The current flow through the inductor L1 of Fig. 7.5 from left to right. For the switch in ON position at P-converter, S11 connects the inductor L1 to the source side as shown in

Fig. 7.5 and thereby completing the loop. Switch S11 is ON when the input signal at their gate is HIGH and S12 is ON when the gate signal is LOW. This is shown in Fig. 7.6

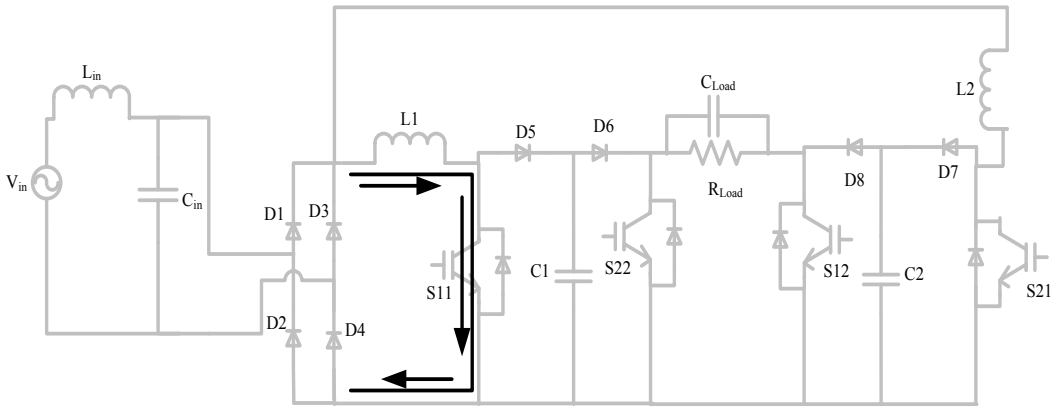

Fig. 7.5 Current flow direction during switch is ON in P-converter

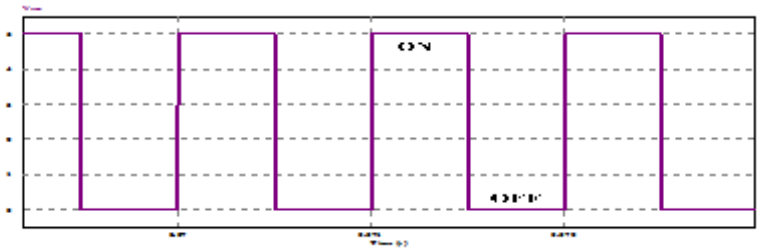

Fig. 7.6 On-Off cycle of the switches

7.2.1.B Switch S11 off in P-converter

When the switch S11 is turned OFF, the complementary pulse turns switch S12 ON in the P-converter, the current flow path is indicated in Fig. 7.7. Switch S12 provides a closed loop across the converter supply terminal consisting the inductor L1, diodes D5 and D6, the Load capacitance C_{Load} and resistance R_{Load}. Moreover, current flows through capacitor C1 and charging it with positive polarity at its top. The direction of current through the inductor L1 is not changed and thereby maintaining the condition of switch mode topologies.

At the same time, the output capacitor, C_{Load} is charged having positive polarity at its left terminal. If a voltmeter is connected with positive terminal at left across R_{Load}, it will show a positive voltage irrespective of the input AC voltage direction. Thus this converter is denoted as the P-converter. As D8 is in reverse bias condition, the current through the output cannot effect the N-converter components.

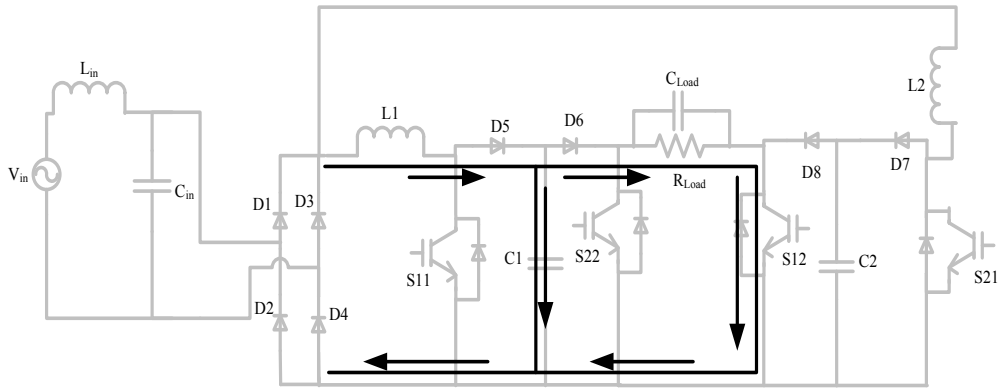

Fig. 5.7 Current flow direction when switch is OFF in P-converter

In this manner the basic Boost converter scheme is satisfied in the proposed cycloconverter. The output capacitor, C_{Load} is discharged via the load resistance, R_{Load}. The diodes D6 and D8 prevent current to flow towards C1 and C2 respectively.

7.2.1.C Overall P-conversion

When stitch S12 is ON in P-conversion cycle, both the capacitors C1 and C_{Load} are charged. When the switch S11 is ON in P-conversion cycle, both the capacitors are discharged leaving the circuit in rest position.

When the switching frequency is large compared to RC time constant of the C_{Load}-R_{Load} loop, C_{Load} does not get sufficient time to get completely discharged and return to previous voltage level. Again at the charging cycle, capacitor voltage increases to a higher value keeping pace with the input voltage. As the input voltage decreases sinusoidally, the capacitor voltage decreases more at discharging cycle than it increases at charging cycle. Thus the overall behavior of the output capacitor resembles a sinusoidal waveform.

The higher is the switching frequency, the better is this response and the output is more likely to be a sinusoid because the capacitor C_{Load} gets very little time to be discharged. At the P-conversion cycle, the output waveform at single input half wave is similar as shown is Fig 7.8

At the rising of input at charging cycle, Output voltage rises from P to Q. At the discharging cycle, output voltage drops from Q to R. As seen from the output waveform R > P, indicating that the capacitor cannot come back to previous level. Again at charging cycle, the capacitor voltage rises to S, while S > Q.

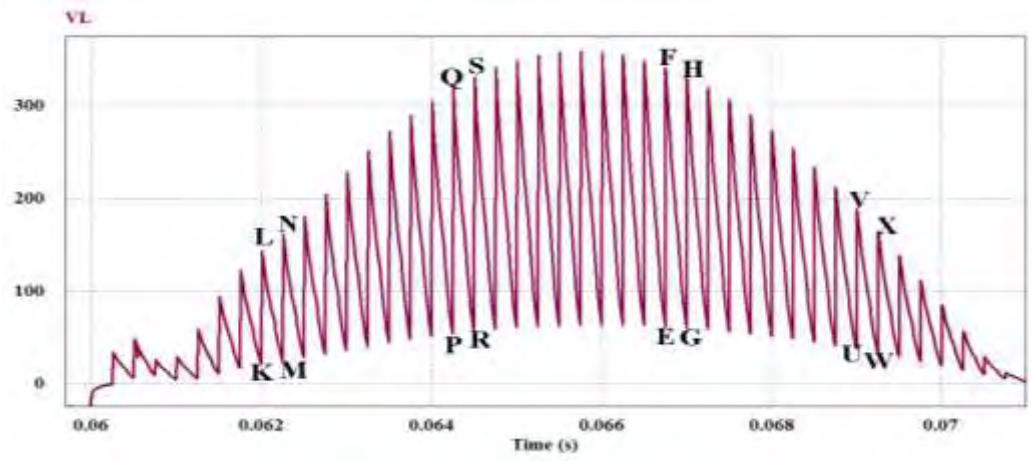

Fig. 5.8 Charging and discharging of the output capacitor at P conversion

Similar arguments can be given for the voltages at K, L, M and N points. It can be observed that voltage rise is much faster at the beginning of the sinusoid than at near to the peak. It can also be expressed as (N-L) > (S-Q).

At the falling side of input signal at ON cycle, Output voltage rises from E to F. At the discharging cycle, Output voltage drops from F to G. As seen from the output waveform E > G, indicating that the capacitor is discharged below the previous level. Again at charging cycle, the capacitor voltage rises to H, while H < F.

Similar arguments can be given for the voltages at U, V, and W, X points. It can be observed that voltage fall is much faster at the ending of the sinusoid than at near the peak. It can also be expressed as (V-X) > (F-H). The P-converter output at a complete half cycle of the output waveform is similar to the output shown if Fig. 7.9

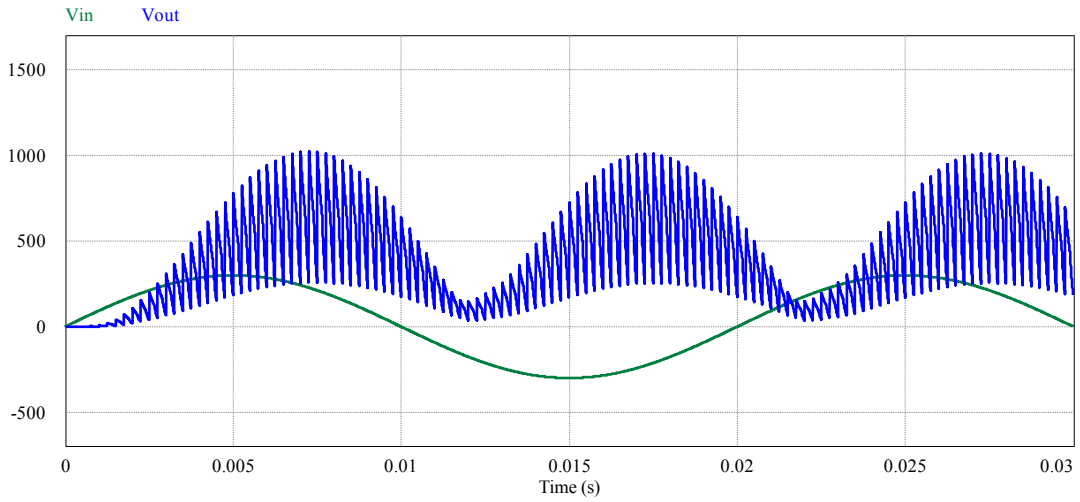

Fig. 7.9 Input and Output voltages at P-conversion

7.2.2. The N-converter

At the N–conversion cycle, the output is always negative irrespective of the polarity at the input. The N-converter can be realized from the Fig. 7.10. The switching scheme of the N-converter is similar to that of the P-converter. P-converter is completely deactivated from the circuit when the N-conversion is in operation.

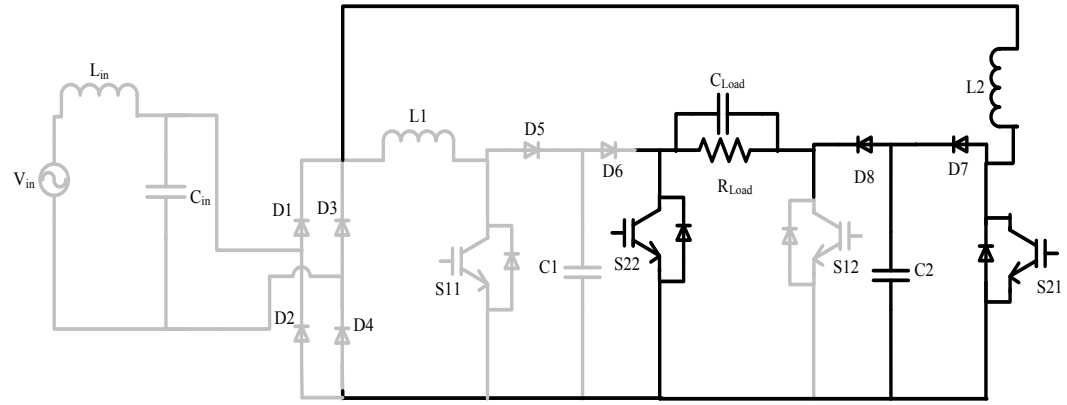

Fig. 7.10 Boost topology based N-converter

7.2.2.A Switch S21 on in N-converter

When the switch S21 is ON in the N-converter S22 remains OFF as they are driven by complementary pulses, the current flow is indicated in Fig. 7.11. When the switch S21 is ON in the P-conversion cycle, the inductor is charged. The current flow diagram is presented in Fig. 7.11. The current flows through the inductor L1 of Fig. 7.11 from top to bottom. For the switch in ON position at P-converter, S21 connects the inductor L1 to the source side as shown in Fig. 7.11 and thereby completing the loop.

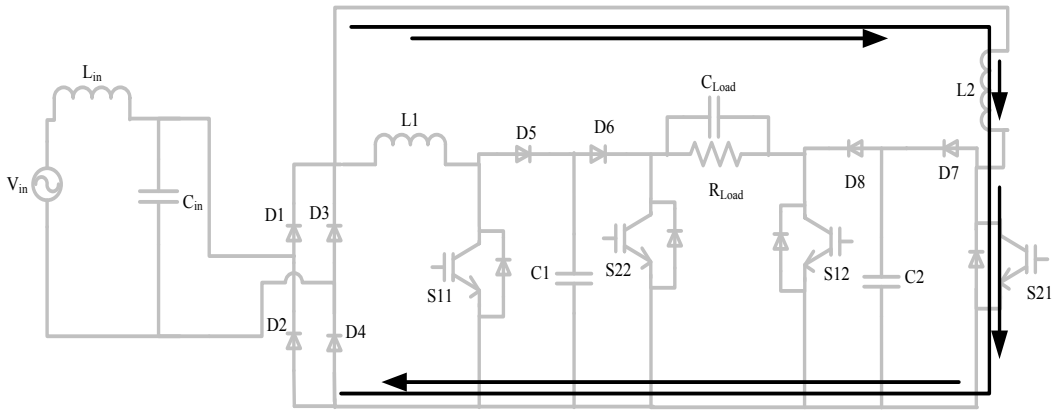

Fig. 7. 11 Current flow direction when switch is ON in N-converter

7.2.2.B Switch S21 off in N-converter

When the switch S21 is turned OFF, the complementary pulse turns switch S22 ON in the N-converter; the current flow path is indicated in Fig. 7.12. Switch S22 provides a closed loop across the converter supply terminal consisting of the inductor L2, diodes D7 and D8, the Load capacitance C_{Load} and resistance R_{Load}. Moreover, current flows through capacitor C2 charging it with positive polarity at its top. The direction of current through the inductor L2 is not changed and thereby maintain the condition of switch mode topology.

At the same time, the output capacitor, C_{Load} is charged having positive polarity at its right terminal. If a voltmeter is connected with positive terminal at left across R_{Load}, it will show a negative voltage irrespective of the input AC voltage direction. Thus this converter is denoted as the N-converter. As D6 is in reverse bias condition, the current through the output cannot flow through the P-converter components.

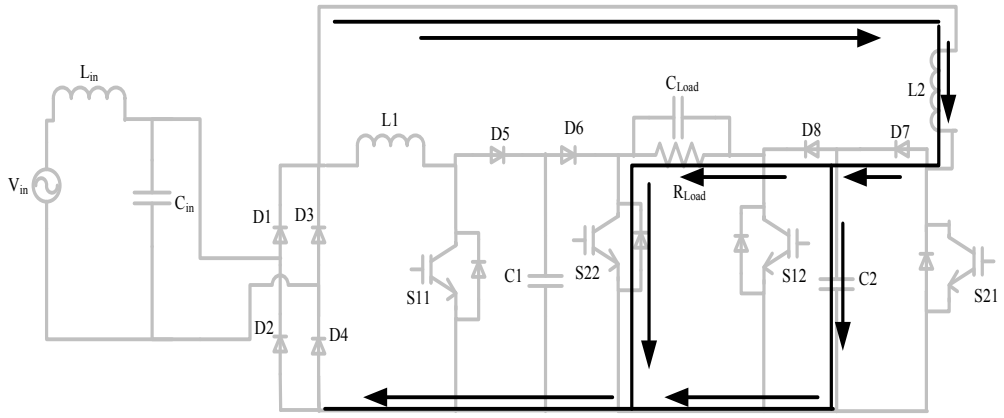

Fig. 7.12 Current flow direction when switch is OFF in N-converter

7.2.2.C Overall N-conversion

At the N-conversion cycle, the output waveform at single input half wave is similar as shown is Fig 7.13. When switch S22 is ON in N-conversion cycle, both the capacitors C3 and C_{Laod} are charged. When the switch S21 is ON in N-conversion cycle, both the capacitors are discharged leaving the circuit in rest position.

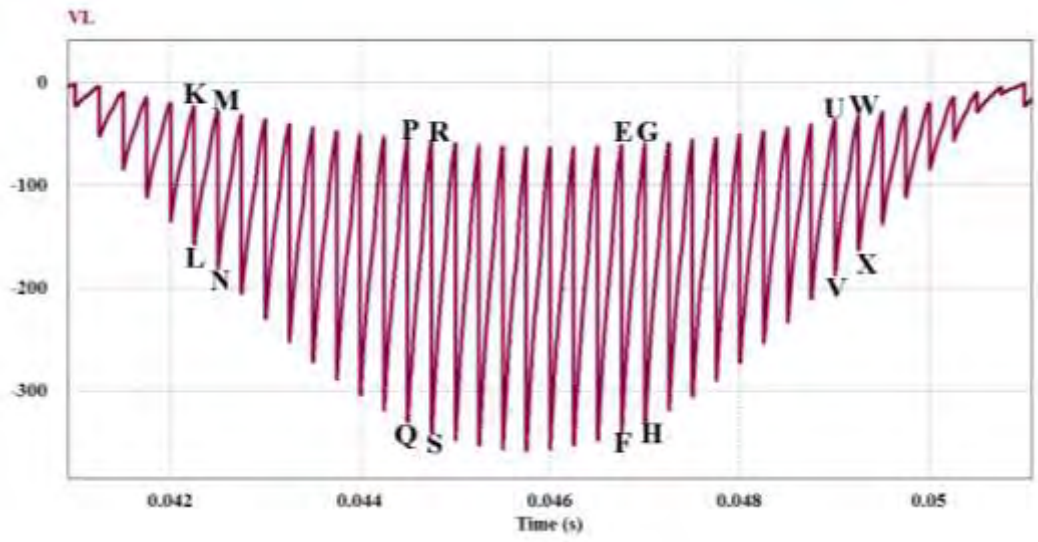

Fig. 7.13 Charging and discharging cycle of the output capacitor at N-conversion

At the rising of input at ON cycle, Output voltage rises from P to Q. At the discharging cycle, output voltage drops from Q to R. As seen from the output waveform |R| > |P|, indicating that the capacitor cannot come back to previous level. Again at charging cycle, the capacitor voltage rises to S, while |S| > |Q|.

Similar arguments can be given for the voltages at K, L, M and N points. It can be observed that voltage rise is much faster at the beginning of the sinusoid than at near to the peak. It can also be expressed as |(N-L)| > |(S-Q)|.

At the falling of input at ON cycle, Output voltage rises from E to F. At the discharging cycle, Output voltage drops from F to G. As seen from the output waveform |E| > |G|, indicating that the capacitor is discharged below the previous level. Again at charging cycle, the capacitor voltage rises to H, while |H| < |F|.

Similar arguments can be given for the voltages at U, V, and W, X points. It can be observed that voltage fall is much faster at the ending of the sinusoid than at near the peak. It can also be expressed as |(V-X)| > |(F-H)|. The over-all N-conversion at a complete half cycle of the output is given by Fig. 7.14

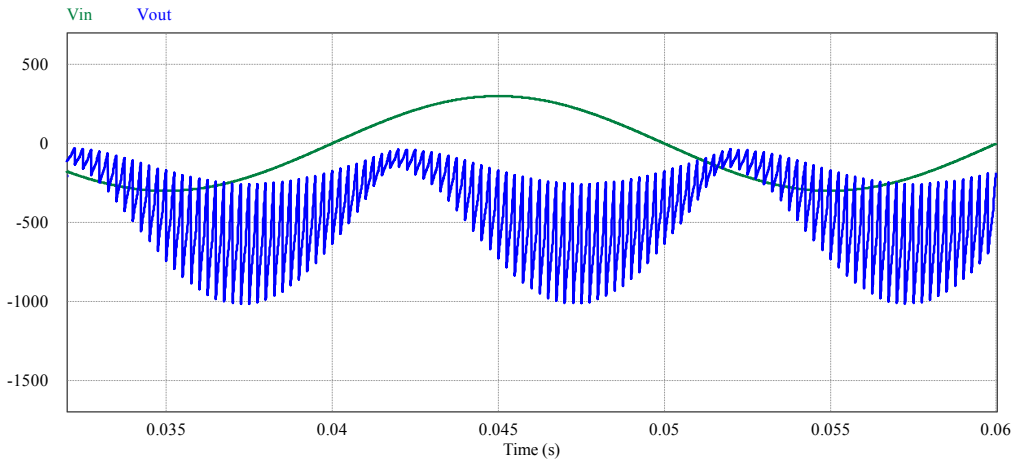

Fig. 7.14 Input and Output voltages at N-conversion

7.3 Simulation results:

The simulation of the proposed circuit is performed using PSIM Professional Version 9.0.3.400. Table 7.1 presents the results of the proposed Boost cycloconverter at different duty cycles for different frequencies.

7.3.1 Performance at Different Control Conditions

The results from simulations show that for a particular frequency the performance of the proposed converter varies with different duty cycles. For instance, at switching frequency of 3 kHz, the THD with 60% duty cycle is 10.87%, whereas, it reduces to 7.41 % with a duty cycle of 70%. Moreover, the input power factor and efficiency for D equal to 0.8 is 0.823 and 80.8% respectively, whereas, for a duty cycle of 70% the power factor and efficiency are 0.964 and 83% respectively. Similar observation can be made for other switching frequencies as well. Considering this analysis as the basis, open loop sliding control has been developed for the Boost cycloconverter topology.

7.3.2 Open Loop Sliding Control

For a given load, the performance of the proposed Boost cycloconverter is examined for a varied range of duty cycles and frequencies. Then an optimum operating point, designated by a specific duty cycle is selected for a specific frequency. The optimum set of duty cycle and frequency values selected for 100 ohm resistive load is presented in Table 7.2. This table also presents the simulation results for the corresponding control parameters. For the proposed boost converter the sliding frequency values are presented in Fig. 7.15. This figure shows the open loop sliding control graph for the proposed boost cycloconverter.

Table 7.1 Simulation output for different duty cycle at different switching frequencies

Frequency, f (kHz)	D	I_{in} (max)	THD	Input PF	Efficiency	V_0 (max)	V_0 (rms)
	0.6	3.05	10.8%	0.99	81.8%	447	346
	0.7	5.61	7.41%	0.964	82.84%	574.4	478.6
3	0.8	9.41	5.33%	0.823	80.80%	713	585
	0.5	2.96	8.2%	0.995	81%	399	313
	0.6	4.7	6.8%	0.985	83%	495	395
4	0.7	8.0	5.2%	0.940	83.6%	615	507
	0.5	3.49	6.2%	0.990	82.67%	430	346.6
	0.6	5.52	5.3%	0.975	84.07%	524.8	431.1
5	0.7	7.99	4.3%	0.912	84.02%	641.3	540.3
	0.5	3.7	5.87%	0.989	83.70%	455.5	373
	0.6	6.22	5.11%	0.971	84.50%	547.5	459
6	0.7	8.67	4.23%	0.887	83.99%	658	562
	0.5	4.16	5.70%	0.985	84.90%	478	397
	0.6	6.3	5.30%	0.955	85.00%	572	483
7	0.7	9.11	4.39%	0.861	84.00%	674	578
	0.5	4.59	6.08%	0.98	85.25%	495.6	414.3
	0.6	6.82	5.26%	0.94	85.20%	587.6	500.9
8	0.7	9.43	4.50%	0.84	83.70%	685	587
	0.4	2.13	18%	0.978	87.02%	427.2	291.8
	0.5	4.9	7.32%	0.977	85.76%	513.7	424.9
9	0.6	7.25	5.56%	0.934	85.63%	603.8	517.5
	0.4	2.16	9.37%	0.977	87.60%	431.5	292
	0.5	5.08	8.31%	0.976	85.70%	528.5	426.5
10	0.6	7.6	5.73%	0.924	85.60%	617	530.2

Table 7.2 Output behavior for sweeping characteristics of the converter

D	**f**	I_{in} (max)	THD	Input PF	Efficiency	V_0 (max)	V_0 (rms)
0.4	10	2.16	9.37%	0.977	87.60%	510.5	392
0.5	9	4.9	7.32%	0.977	85.76%	523.7	424.9
0.6	6	6.22	5.11%	0.971	84.50%	547.5	459
0.7	4	8.0	5.2%	0.940	83.6%	615	507
0.8	3	9.41	5.33%	0.823	80.80%	713	585

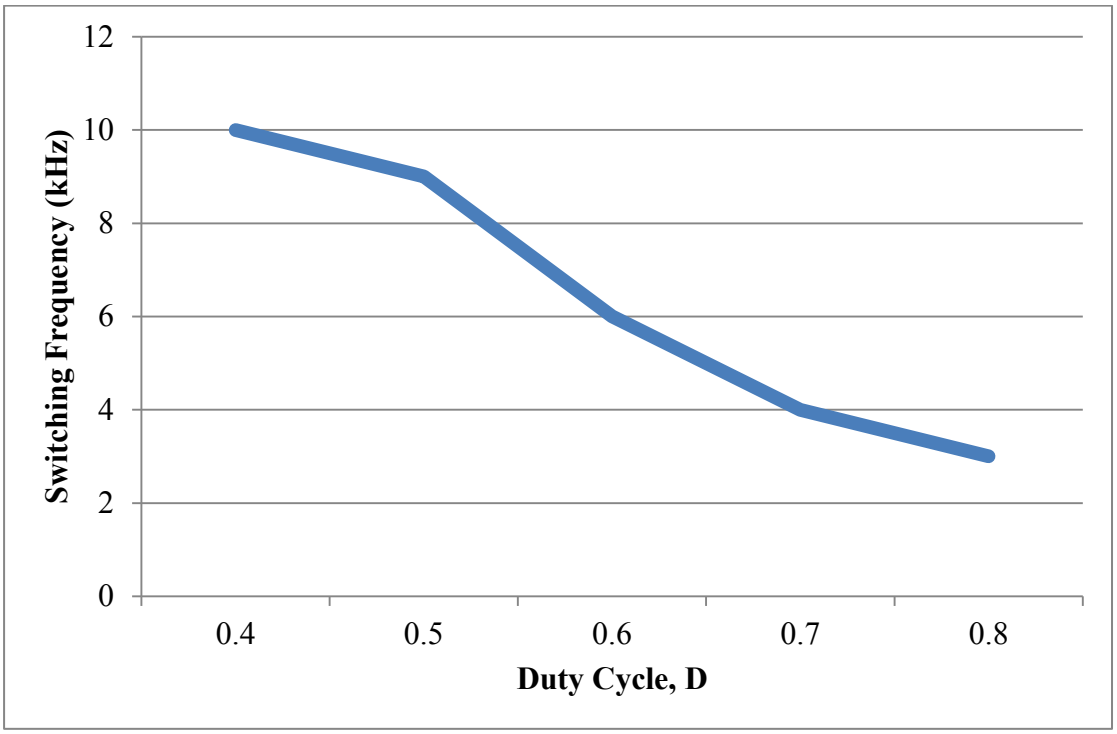

Fig. 7.15 Sweeping characteristics for Boost cycloconverter

7.3.3 Typical Waveforms

Fig. 7.16 shows typical input current, input and output voltages for the proposed boost cycloconverter with 40% duty cycle. The switching frequency is set to 10 kHz as determined form the open loop sliding control of this cycloconverter. For D=0.4 the maximum output voltage is 510 volt with an RMS value of 392 volt. Fig. 7.17 shows the waveforms for D=0.6 and in this case the switching frequency was considered to be 6 kHz.

Fig. 7.18 shows typical input current, input and output voltages for the proposed boost cycloconverter with 80% duty cycle. The switching frequency is set to 3 kHz according to the open loop sliding control of this cycloconverter. For D=0.8, the maximum output voltage is 713 volt with an RMS value of 585 volt. Spectrum of the input current of Fig. 7.16 is shown in Fig. 7.19 which shows a small magnitude of current near 3 kHz (the switching frequency). It is evident that these circuits can reduce the harmonic distortion.

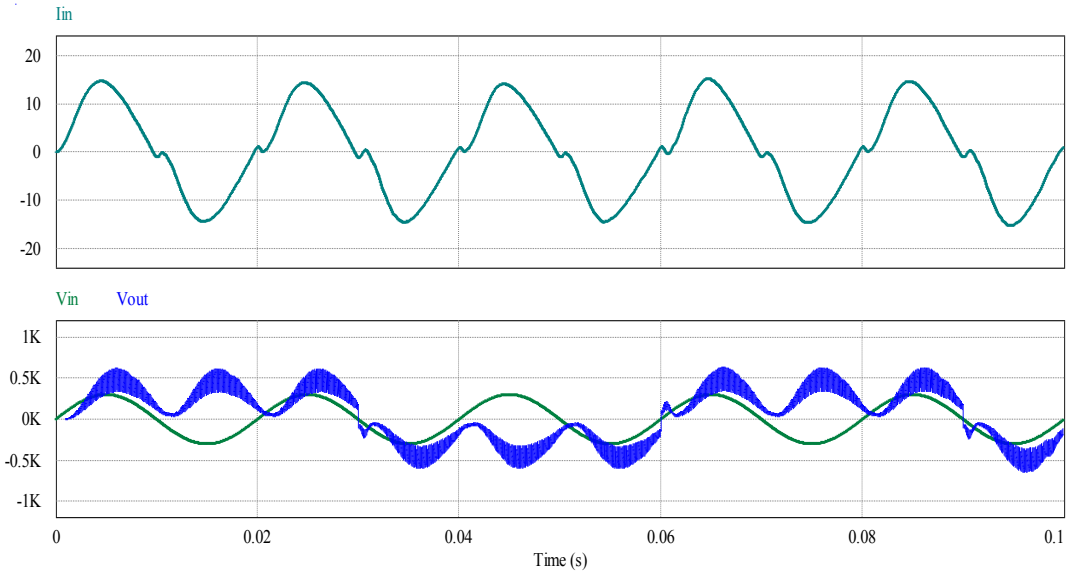

Fig. 7.16 Input current and Input & Output voltages at D=0.4 and f=10 KHz

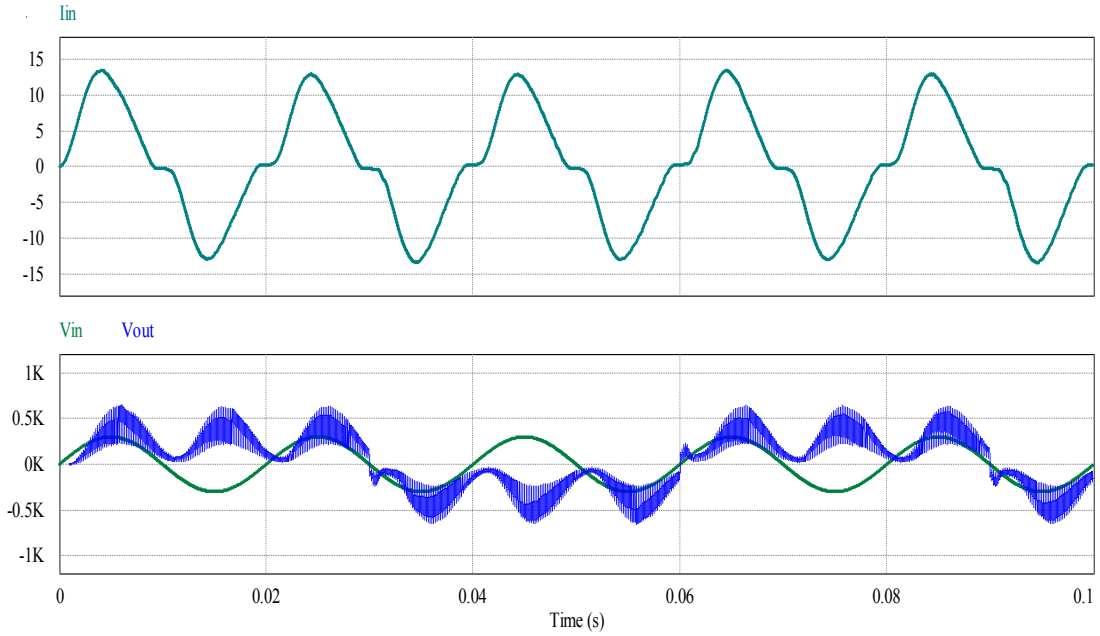

Fig. 7.17 Input current and Input & Output voltages at D=0.6 and f=6 KHz

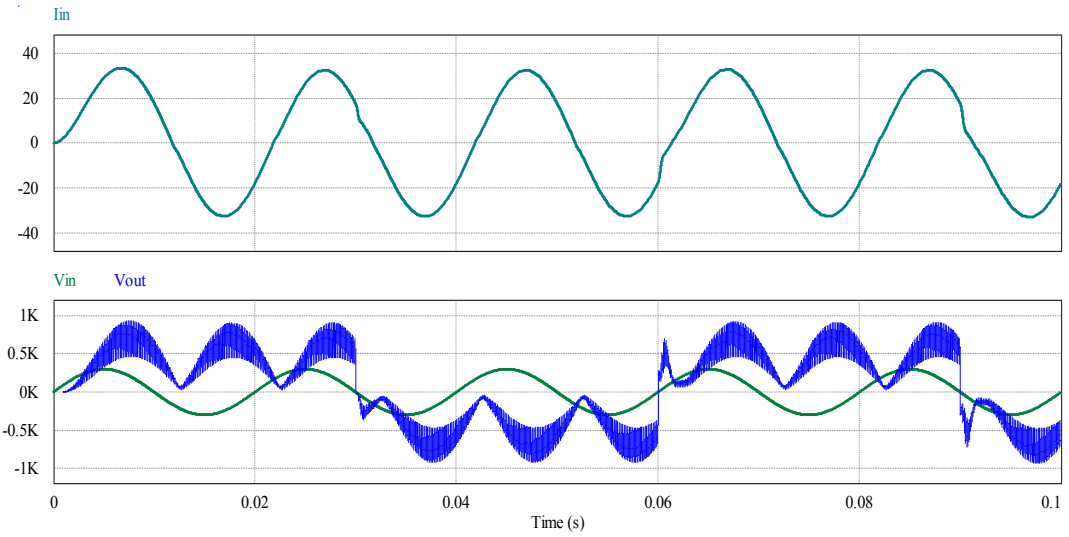

Fig. 7.18 Input current and Input & Output voltages at D=0.8 and f=3 KHz

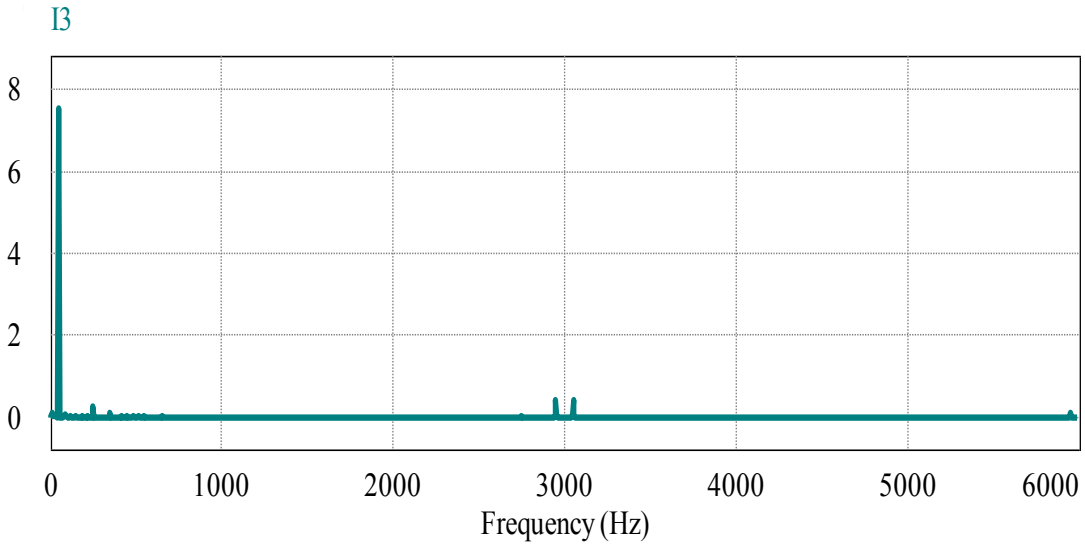

Fig. 7.19 Spectrum of the input current for D= 0.8 and f = 3 kHz

7.3.4 Performance at Variable Load Conditions

Table 7.3 shows the performance of the proposed Boost cycloconverter with variable resistive loads. It is observed from the results presented in table 7.3 and Figs. 7.20, 7.21 and 7.22 that variation of load has a little effect on the input current THD or input power factor of the proposed converter. However, with the increment of load resistance the overall efficiency slightly degrades at the proposed Boost cycloconverter.

Table 7.3 Change in output behavior with load

D	f	R=50			R=100			R=200		
		THD	Pf(in)	η	THD	Pf(in)	η	THD	Pf(in)	η
0.4	10	9.19	0.88	86	9.37	0.98	88	9.59	0.68	81
0.5	9	6.82	0.96	89	7.32	0.98	86	7.71	0.92	86
0.6	6	5.31	0.98	91	5.11	0.97	85	5.37	0.98	88
0.7	4	5.06	0.99	91	5.2	0.94	84	5.54	0.99	89
0.8	3	4.51	0.98	93	5.33	0.82	81	6.11	0.98	91

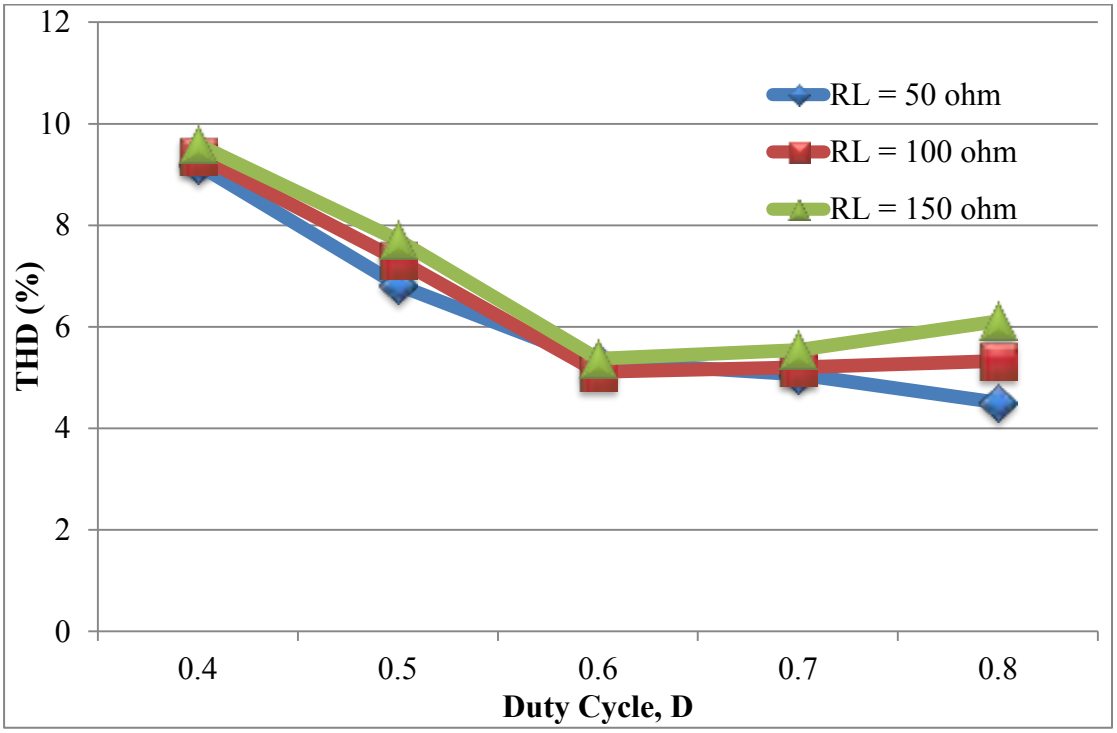

Fig. 7.20 Variation in THD with different load at different position

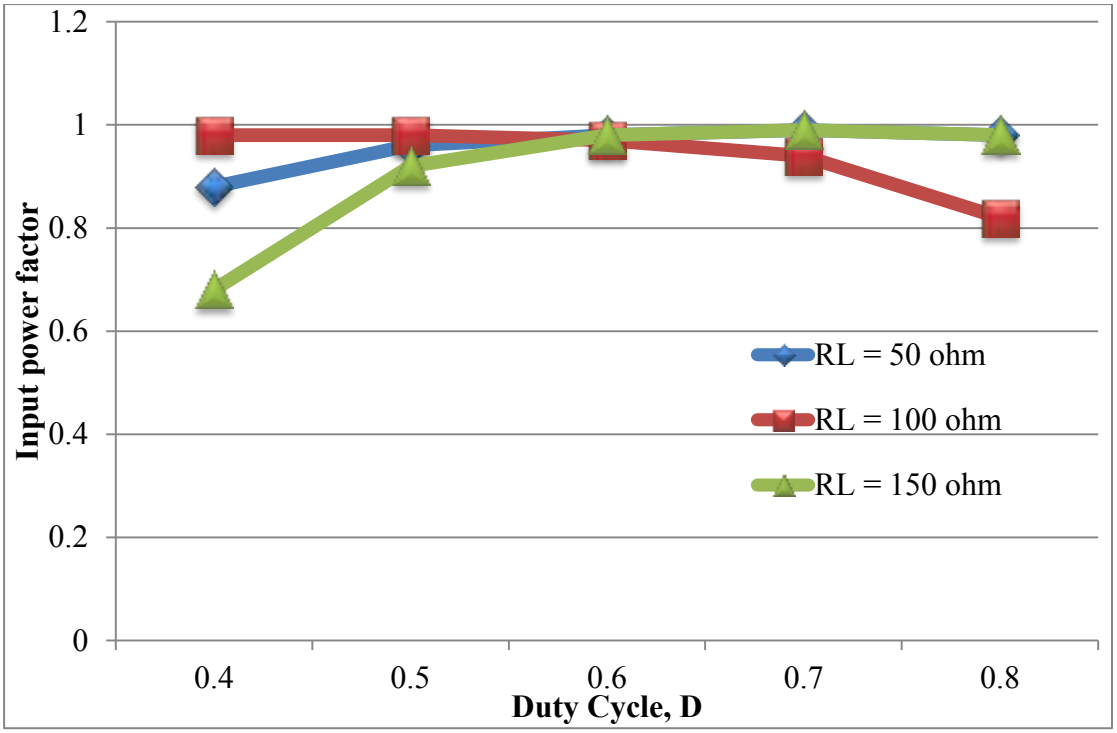

Fig. 7.21 Variation in input power factor with different load at different position

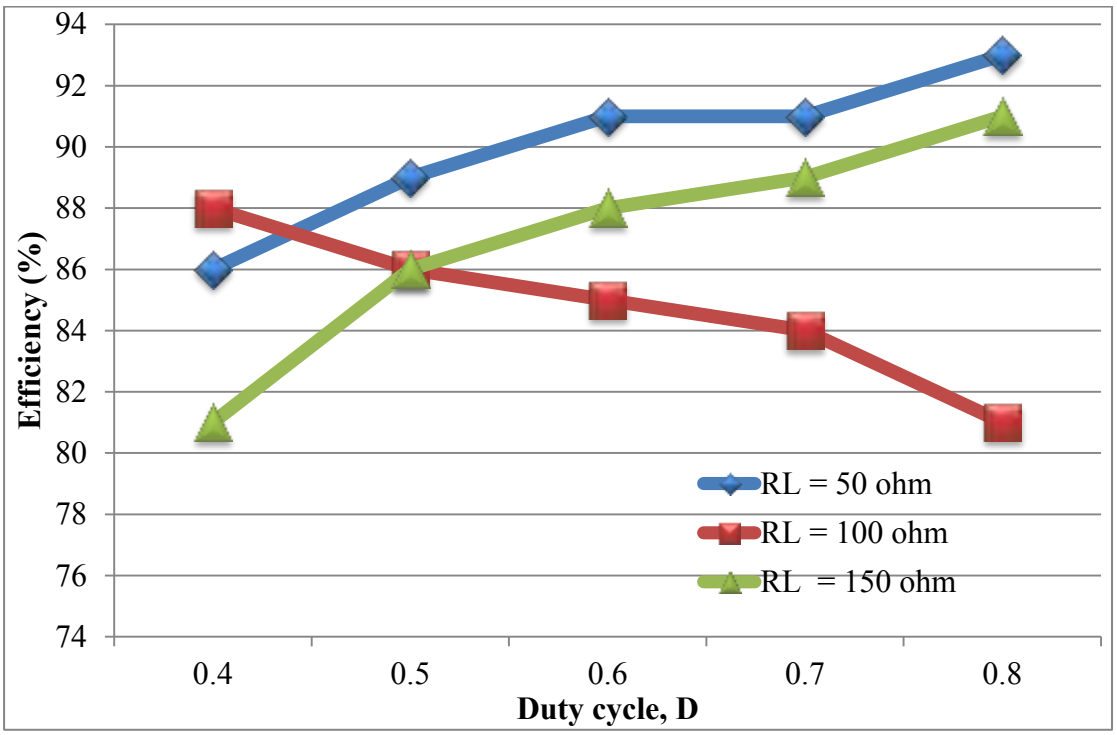

Fig. 7.22 Variation in efficiency with different load at different position

7.3.5 Performance of Step-up Frequency Operation

Output frequency and output voltage both can be increased in the proposed Boost cycloconverter by changing the gate pulses to IGBTs. Performance at higher output frequencies also changes with duty cycle and switching frequencies. Table 7.4 shows performance of the circuit for step-up frequency operation of the proposed cycloconverter. Fig. 7.23 and 7.24 show the typical input current, input and output voltages for the proposed boost cycloconverter with 50% and 80% duty cycles respectively at output frequency of 150 Hz. The switching frequency is set to 9 kHz for D=0.5 and 3 kHz for D=0.8 according to the open loop sliding control of this cycloconverter.

Table 7.4 Output behavior for output frequency double than input

D	f	I_{in} (max)	THD	Input PF	Efficiency	V_0 (max)	V_0 (rms)
0.4	10	2.16	17	.96	78	316.5	223.59
0.5	9	4.9	16.8	.98	83	323.7	242.9
0.6	6	6.22	12.8	.99	80	347.5	259.67
0.7	4	8.0	8.5	.98	82	356.97	269.25
0.8	3	9.41	5.6	.92	83	371.5	311.59

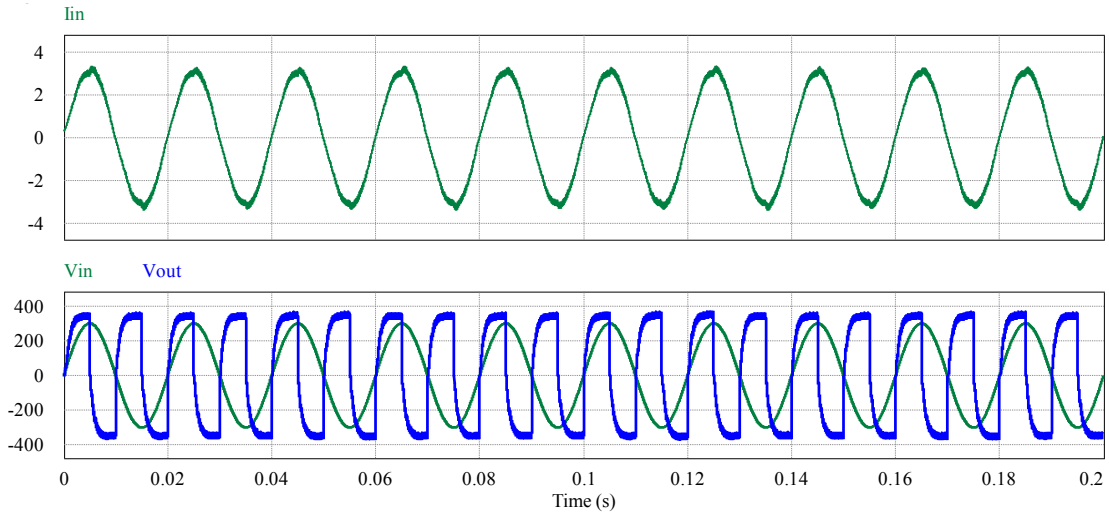

Fig. 7.23 Input current and Output & Input voltages at D=0.5 and f=9 KHz

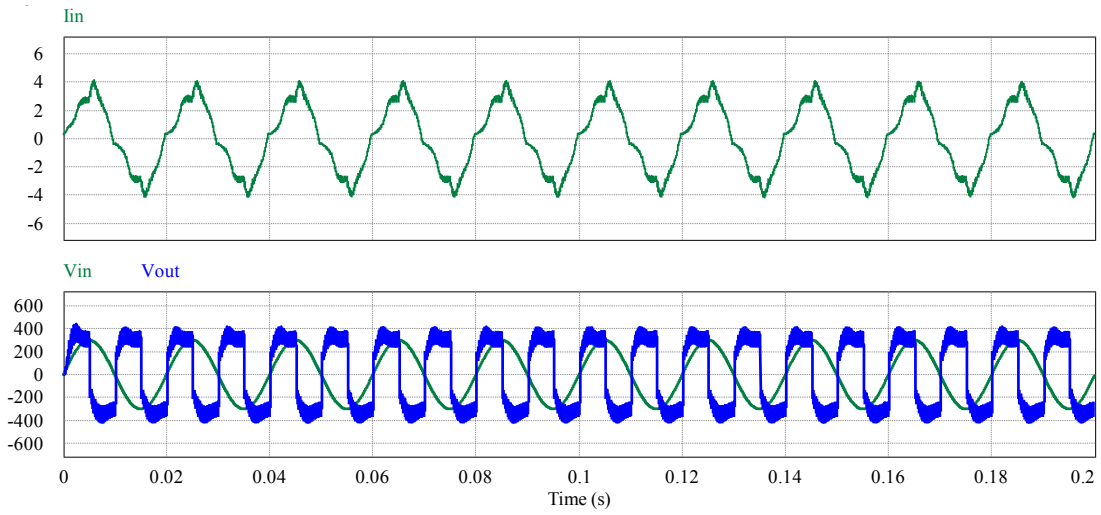

Fig. 7.24 Input current and Output & Input voltages at D=0.8 and f=3 KHz

7.3.6 Performance with R-L Load

The performance of the proposed Boost cycloconverter with R-L load is presented in table 7.5. The resistance and inductance values for the R-L load are set to 25 ohm and 100 mH respectively. Here the control parameters (duty cycle and switching frequency) are maintained same as for the resistive loads. Typical input current, input and output voltage waveforms for R-L load is presented in Fig. 7.25 and 7.26 for 40% and 80% duty cycles respectively. Results show that the behaviors of the proposed cycloconverter under R and R-L loads are almost similar.

Table 7.5 Performance of the proposed Boost cycloconverter with R-L load

D	f	Iin (max)	THD	Input PF	Efficiency	V0 (max)	V0 (rms)
0.4	10	2.93	12.4	0.98	78.3	323	285
0.5	9	3.73	10.23	0.99	79.6	370	330.4
0.6	6	5.76	9.7	0.99	81.4	341.4	414
0.7	4	9.9	9	0.958	84.2	447	546
0.8	3	15.41	7.15	0.823	86.4	590	718

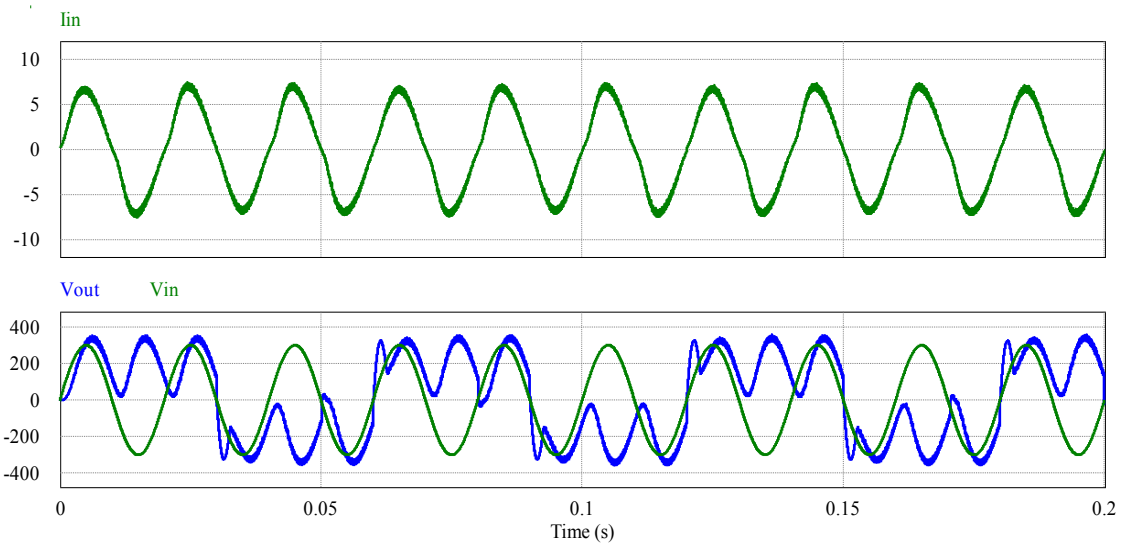

Fig. 7.25 Input current, input and output voltage waveforms for R-L load with D = 0.4 and f=10 kHz

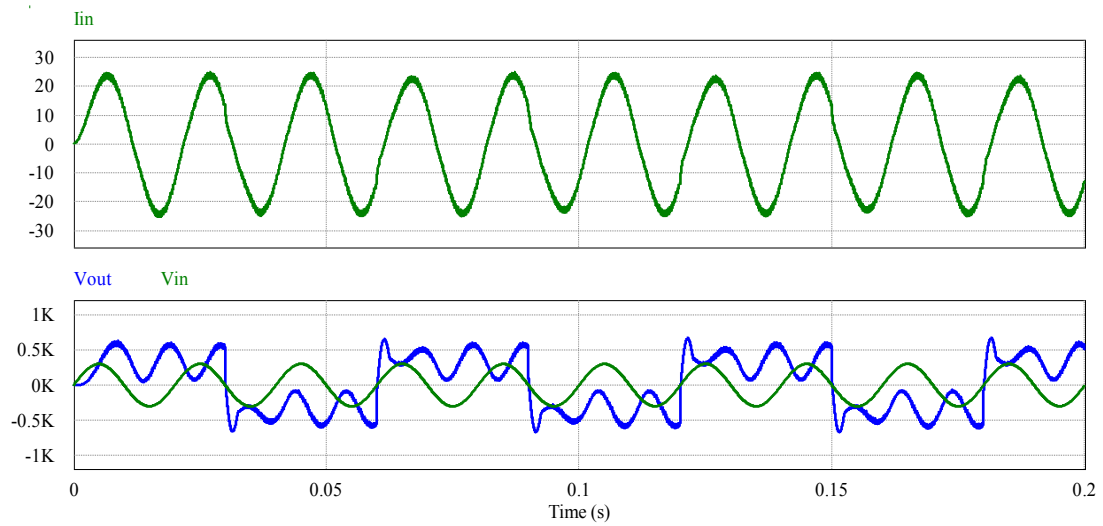

Fig. 7.26 Input current, input and output voltage waveforms for R-L load with D = 0.8 and f=3 kHz

7.4 Discussion

The results presented in section 7.3 prove that the proposed Boost cycloconverter can provide AC-AC conversion at high efficiencies maintaining high power quality. Moreover, the proposed cycloconverter can increase or decrease output frequency effectively with high power quality. The proposed cycloconverter offers better flexibility than traditional cycloconverter with reduced switch and improved efficiency. Different control strategies can be employed to increase the efficiency of the converter further.

CHAPTER 8
COMPARISON OF RESULTS

The performance evaluation of the proposed switch mode topologies is executed in comparison to conventional single phase 8 SCR cycloconverters.

8.1 Single Phase 8 SCR Cycloconverter

The principle of operation of a single phase to single phase (1ϕ-1ϕ) cycloconverters can be explained with the help of Fig. 8.1. It consists of two single phase controlled converters known as P-converter and N-converter. These two converters operate as bridge rectifiers. However, their delay angles are such that the output voltage of one converter is equal to and opposite to that of the other converter. If P-converters operating alone, the average output voltage is positive. If N-converter is operating, the output voltage is negative.

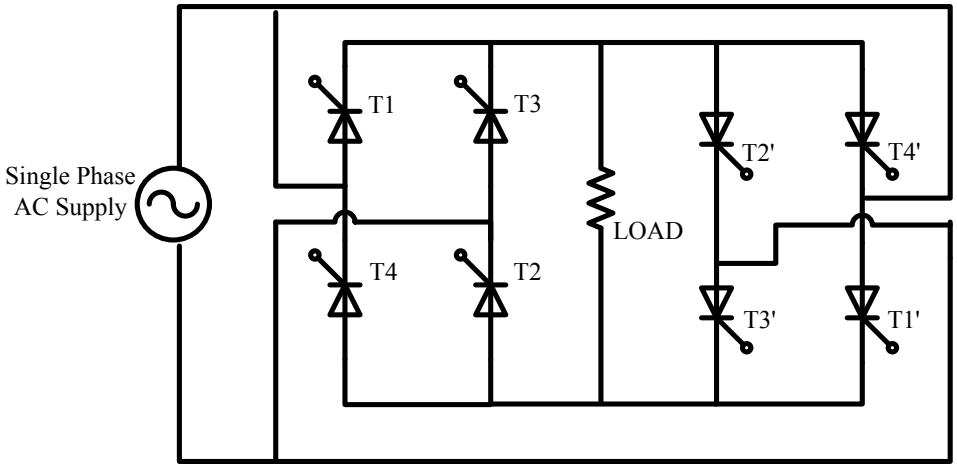

Fig. 8.1 Single Phase 8 SCR Cycloconverters

8.1.1 Gating Sequence:

Each of the P and N converters consists of 4 controlled thyristors. Therefore, they are called 8 SCR cycloconverters. The gating sequence [56] of single phase eight thyristors cycloconverters is as follows:

During the first half period of the output frequency $T_0/2$, operate converter P as a normal controlled rectifier with a delay angle of $\alpha_p = \alpha$, that is by gating T_1 and T_2 at α and gating T_3 and T_4 at $\pi + \alpha$.

During the second half period of the output frequency $T_0/2$, operate converter N as a normal controlled rectifier with a delay angle of $\alpha_N = \pi - \alpha$, that is by gating T'_1 and T'_2 at $\pi - \alpha$ and gating T'_3 and T'_4 at $2\pi - \alpha$. Since our analysis of the proposed cycloconverters are based on duty ratio, that is the percentage of time a control pulse remain active of the total pulse period, we will interpret the firing angle of the conventional cycloconverters in terms of duty ratios, D. In order to accomplish that, we consider firing angle of $\alpha = \pi$ as 0% and $\alpha = 0$ as 100% duty ratio. In that terms a firing angle of $\alpha = \pi/4$ will be equal to 75% duty ratio. The control pulse sequence for this conventional cycloconverter is presented in Fig. 8.2 for $\alpha = \pi/2$ or 50% duty ratio.

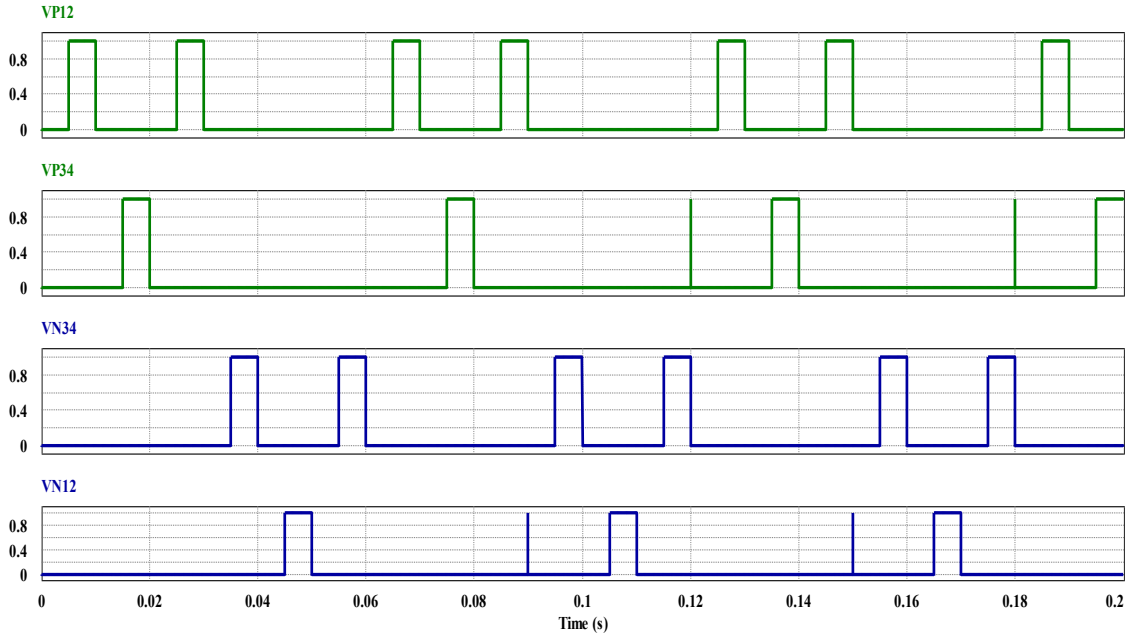

Fig. 8. 2 Gating sequence for a conventional single phase 8 SCR cycloconverter

8.1.2 Characteristics Waveforms

Fig. 8.3 shows the waveforms for the output voltage and gating signals of positive and negative converters, with the positive converter on for time $T_0/2$ and the negative converter operating for time $T_0/2$. The results are shown for output frequency, f_0 being one third of the input frequency, f_i. Here, the input AC is a 50 Hz signal. So, the output frequency of Fig. 8.3 is 16.67 Hz. As a result T_0 will be equal to 60ms. The waveforms in Fig. 8.3 is shown for $\alpha = 54^0$.

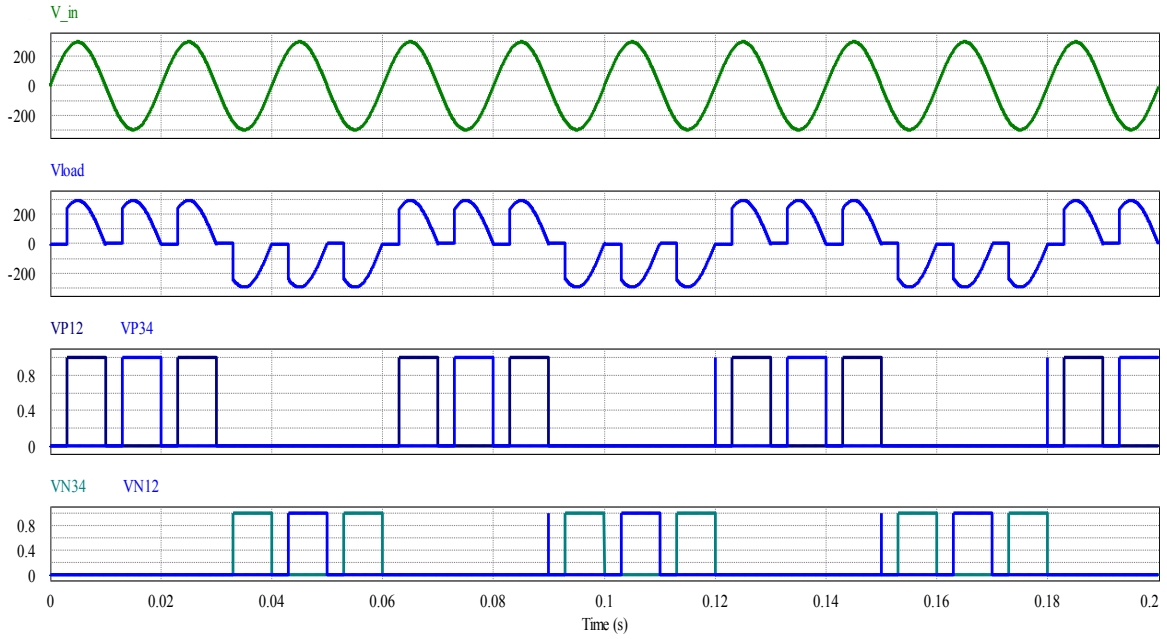

Fig. 8. 3 Waveforms of conventional cycloconverters with resistive load

If α_P is the delay angle of the positive converter, the delay angle of the negative converter is $\alpha_N = \pi - \alpha_P$. The average output voltage of the positive converter is equal and opposite to that of the negative converter, that is $V_{dc2} = -V_{dc1}$. Similar to dual converters the instantaneous value of two output voltages may not be equal. It is possible for large harmonic currents to circulate within the converters [57]. Typical input current, input voltage and output voltage are shown if Fig. 8.4 and 8.5 for a conventional single phase cycloconverter with $f_0=f_i/3$ and $\alpha = 36^0$ and $\alpha = 54^0$ respectively.

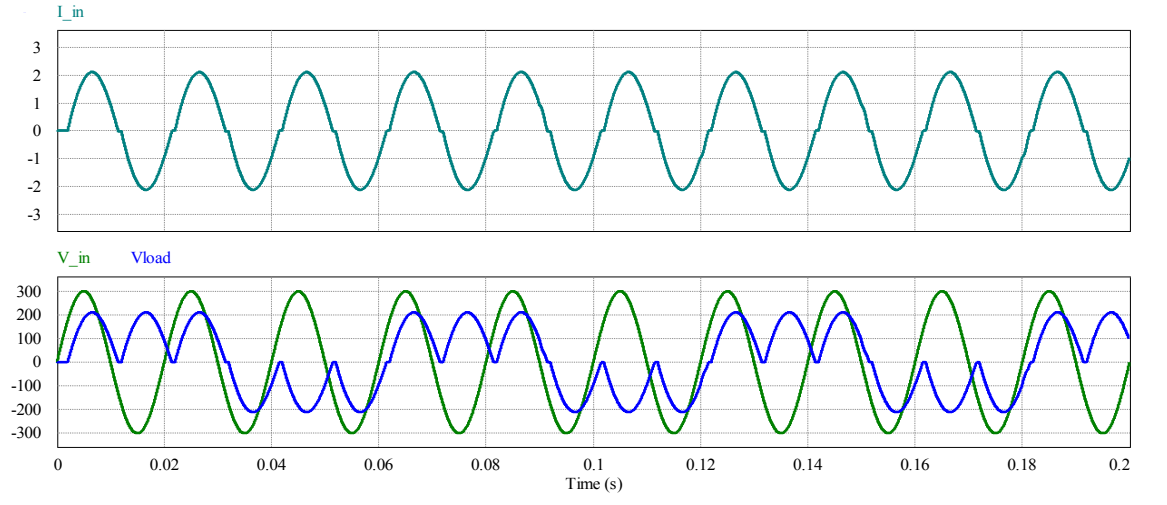

Fig. 8. 4 Typical input current, input and output voltage of cycloconverters for $\alpha = 36^0$

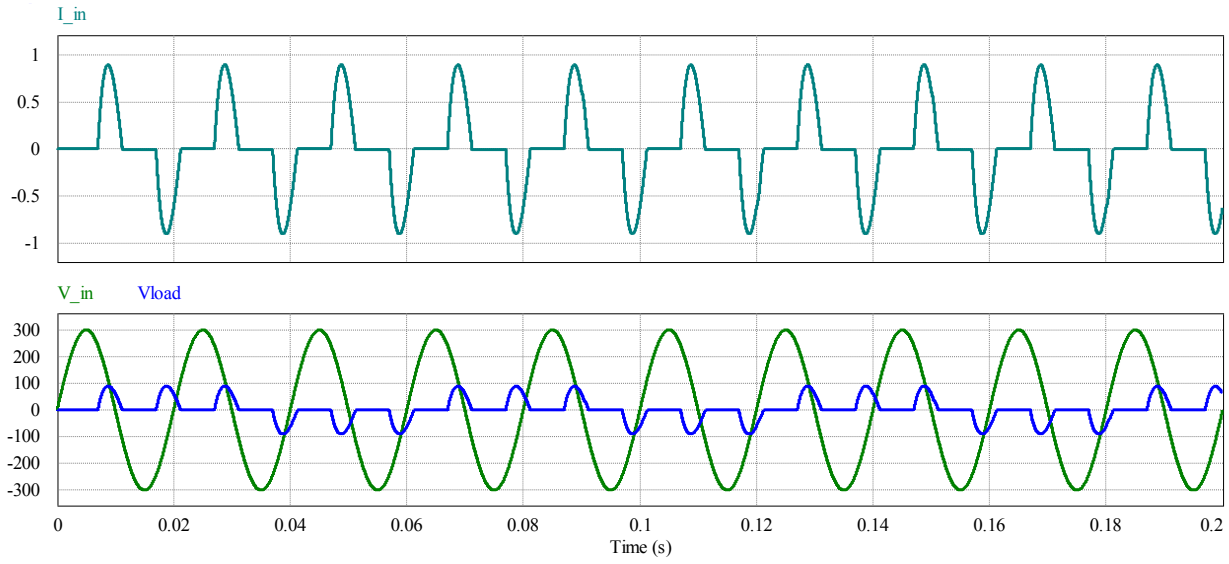

Fig. 8. 5 Typical input current, input and output voltage of cycloconverters for $\alpha = 54^0$

8.1.3 Simulation results

Performance of the conventional 8 SCR cycloconverter is analyzed by simulating an eight 8 SCR cycloconverter in PSIM software. Results are obtained for a resistive load of 100 ohm. In order to suppress the harmonic component of the circulating current IGRs of 200 mH are added across the load. The results of simulation for different duty ratios of the control signal are presented in table 8.1.

Table 8.1 Performance of the conventional 8 SCR cycloconverters

Firing Angle α (^{0})	Duty Cycle D	V_o (max)	V_o (rms)	I_o (max)	THD (%)	Input Power Factor	I_{in} (max)	η (%)
144	0.2	170	46.77	14.17	100.5	0.112	14	73
126	0.3	239.25	81	20	70.7	0.235	19.93	76
108	0.4	282.84	117.42	23.57	50.95	0.379	23.57	78
90	0.5	300	150	25	35.72	0.525	25	78
72	0.6	300	176.67	25	22.97	0.837	25	79
54	0.7	300	195.72	25	11.79	0.763	25	79
36	0.8	300	206.9	25	2.92	0.657	25	79

8.2 Performance Comparison

Proposed cycloconverter topologies are advantageous than conventional ones for three reasons. Firstly, the input current THD will be much lower in the proposed topologies due to high frequency switching of the switch mode topologies. Another advantage of this input current switching is the requirement of much smaller input filters. The input current THD of the conventional converters will be possible to reduce if large intergroup reactors (IGRs) as shown in Fig. 8.6 are added. This addition of reactor will degrade the input power factor as well as efficiency of the conventional cycloconverters. In this section, the performance of the proposed topologies will be compared in terms of standard parameters for power electronic converters namely, input current THD, input power factor and efficiency.

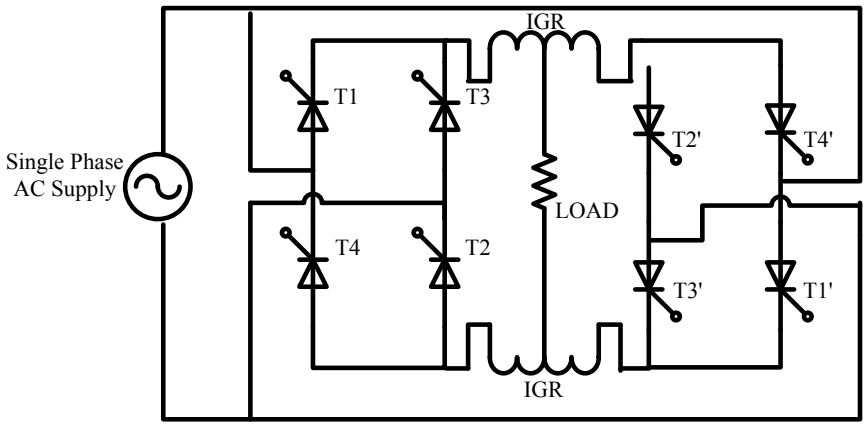

Fig. 8. 6 Conventional 8 SCR cycloconverters with intergroup reactors (IGRs)

8.2.1 Based on input current THD

The input current of the conventional cycloconverters is similar to that of controlled rectifiers as shown in Fig. 8.4 and 8.5. This current is rich in harmonics as it only conducts during the fraction of amount of input frequency half cycles determined by the firing angle of the control signal. The Fourier series representation of the input currents at cycloconverter inputs are shown in Fig. 8.7. From this representation it is visible that the conventional cycloconverter input current contains many undesirable harmonic components. In order to improve the THD performance of the conventional cycloconverter large intergroup reactors need to be connected across the load terminal as shown in Fig. 8.6. Although this addition of IGR will improve the THD performance of the 8 SCR cycloconverter, they require a very large value of inductance as shown in Table 8.2. The results are shown for $\alpha = 144^0$ and 36^0 (duty ratios of 0.2 and 0.8). This large inductances

result in two problems, firstly, adding this large inductor will make the converters bulky and will increase its weight. Secondly, this addition of IGR will degrade the system power factor and efficiency as will be illustrated in the following sections.

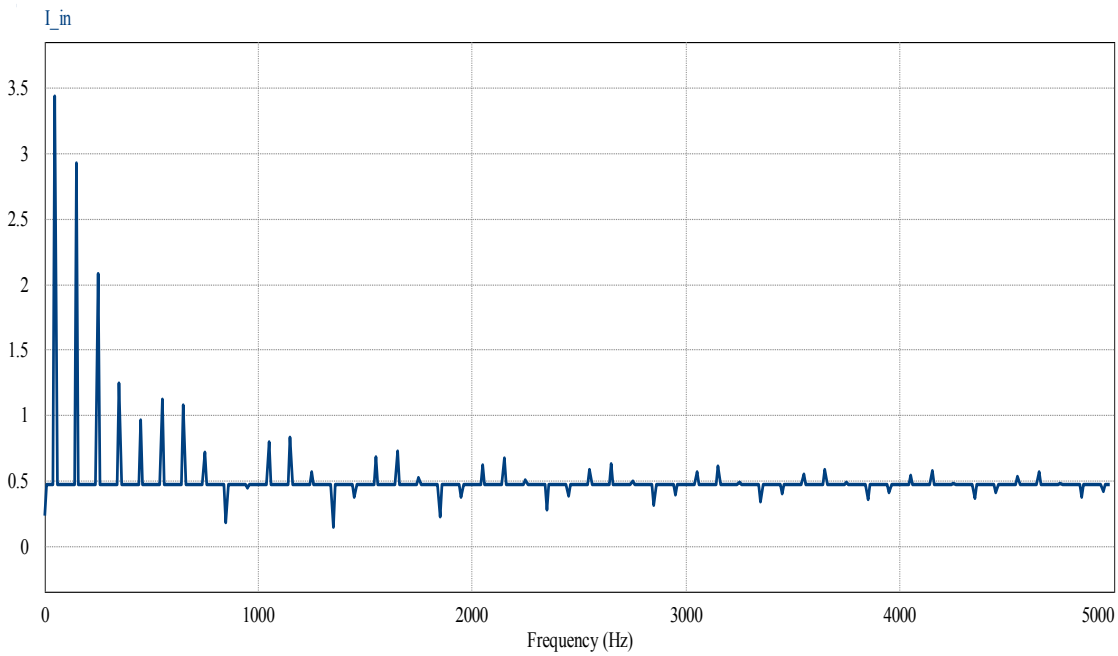

Fig. 8. 7 Fourier representation of 8 SCR cycloconverter input current

Table: 8.2 Variation of input current THD with the value of IGRs for single phase 8 SCR cycloconverters

$\alpha = 144^0$ D = 0.2		$\alpha = 36^0$ D = 0.8	
IGR Value	Input Current THD	IGR Value	Input Current THD
20m	140	20m	17.5
40m	129	40m	15.56
80m	115.5	80m	11.63
100m	111.3	100m	9.76

In the proposed topologies, the high frequency switching shifts the harmonic components of the input current towards the switching frequency as shown in the previous chapters. As a result a small input filter is necessary to reduce the input current THD. Fig. 8.8 provides

the performance comparison of the proposed cycloconverter topologies with the conventional 8 SCR cycloconverter with IGR value equal to 200 mH along the range of duty cycle of the control signal.

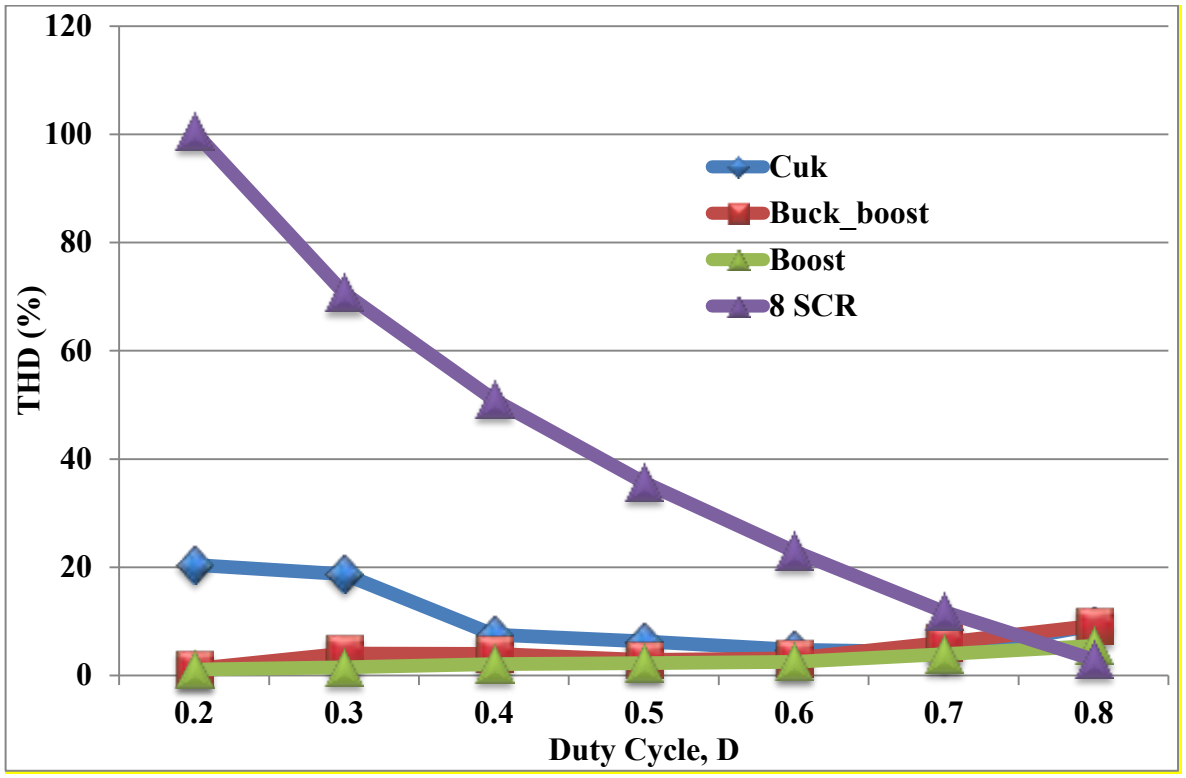

Fig. 8. 8 Performance comparison in terms of input current THD

The results depicted in Fig. 8.8 show that, under a certain value of duty ratio D, for the same input filter, the input current THD for the conventional 8 SCR cycloconverter is higher than the proposed topologies. The important thing to note down here is that, although the conventional cycloconverter show lower THD than the proposed ones at D = 0.9, it has already burdened with a large inductor of 400 mH (200 mH at each side of the load) and will show degraded performance in terms of power factor and efficiency which is illustrated in the following sections.

8.2.2 Based on input power factor

The inductors an AC electrical network will create phase lag between the supply voltage and current of the network. In order to reduce the harmonics from the input current of the conventional 8 SCR cycloconverters we have put large value intergroup reactors on each side of the load. This will shift the input current further from the input voltages as the impedance become much higher. As a result, the power factor of the conventional 8 SCR cycloconverter will be reduced.

In case of the proposed cycloconverter topologies high switching frequency of the power switch ensures the requirement of a small input filter to reduce the THD. Consequently, the resulting phase shift will be very small compared to the conventional ones under same THD performance. The input power factor results for three certain ranges of THD values for D = 0.7 are provided in table 8.3.

Table 8.3 Comparison of proposed and conventional cycloconverters' input power factors in terms of certain range of input current THD (%)

THD range (%)	Input power factors			
	Proposed			conventional
	Ćuk	Buck-Boost	Boost	8 SCR
THD<5	0.953	0.96	0.98	0.837
5<THD<12	0.955	0.98	0.99	0.863
12<THD<23	0.98	0.998	0.99	0.89

From the results displayed in table 8.3 it can be inferred that for a certain value of duty cycle and range of input current THD, the proposed cycloconverter topologies are able to achieve much higher value of input power factors. Fig. 8.9 provides the performance comparison based on input power factor of the proposed cycloconverter topologies with the conventional 8 SCR cycloconverter with each IGR value equal to 200 mH along the range of duty cycle of the control signal. It is implied from the results shown in Fig. 8.9 that, for a certain value of duty cycle the proposed switch mode cycloconverters outperform the conventional 8 SCR cycloconverter as they show higher power factors.

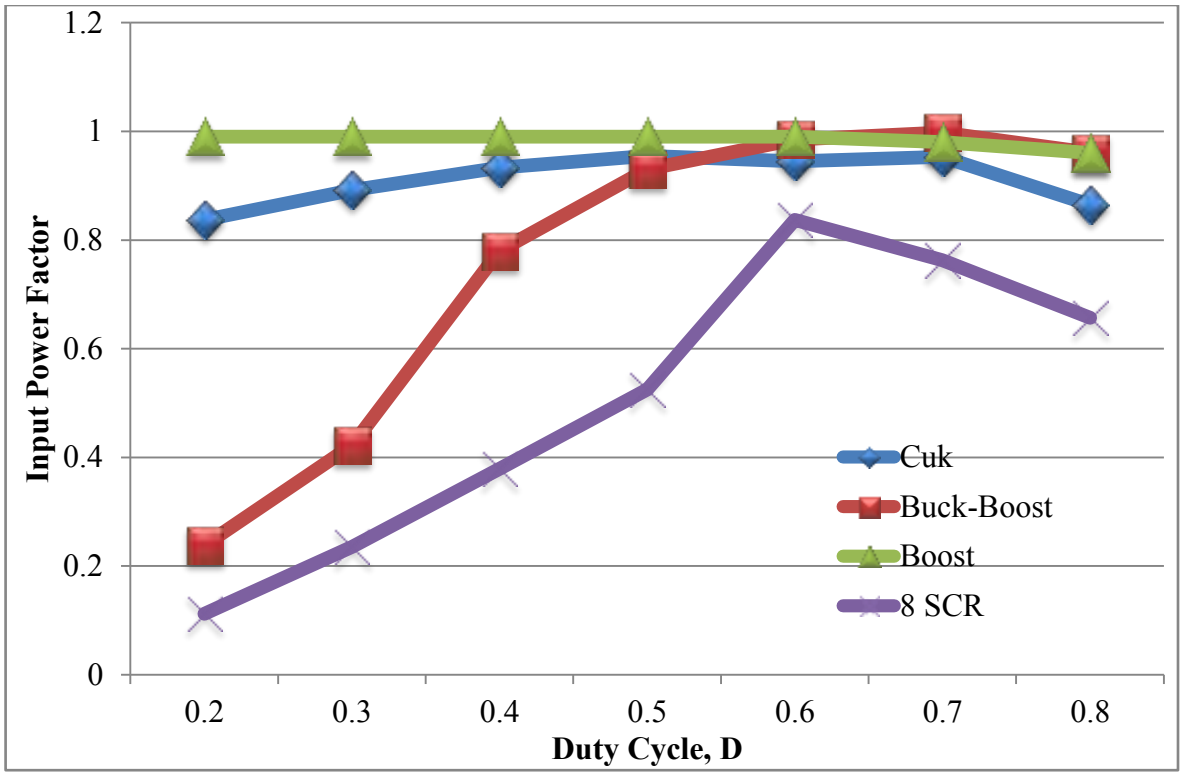

Fig. 8. 9 Performance comparison in terms of input power factor

8.2.3 Based on power conversion efficiency

The number of solid state switches in conventional cycloconverter is eight. These SCRs remain in On state unless their anode to cathode voltage become negative or the current flowing become less than their holding current [57]. As a result these SCRs will cause a significant amount of power losses during their conduction period. Moreover, there will be losses associated with the IGRs as the high value inductances used for this purpose will have some series resistance. There will be unwanted voltage drops while circulating currents flows through the IGRs. Considering these circumstances the efficiency of the conventional 8 SCR cycloconverters will degrade.

The number of solid state switches in the proposed topologies is reduced to four. Reduction in the number of switches will reduce switching losses in the converters. Moreover, there are no large-value reactors in the proposed topologies so there will be no large voltage drop or losses across their series resistances. The comparison based on efficiencies is presented as a bar plot in Fig. 8.10. From this figure it is evident that along a certain range of duty cycles, the proposed switch mode cycloconverters provides AC-AC conversion at higher efficiencies than the conventional ones.

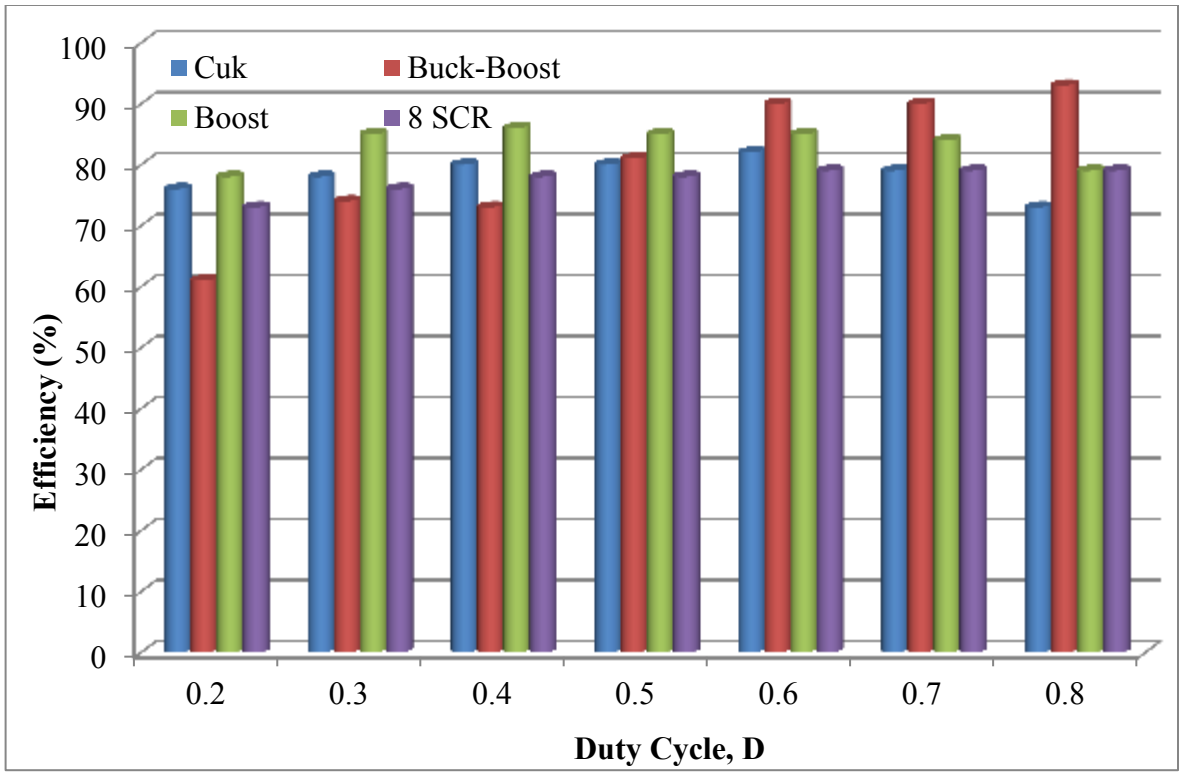

Fig. 8. 10 Performance comparison based on converter efficiency

8.3 Discussion

The objective of this chapter was to compare the performance of the proposed switch mode topologies with the conventional 8 SCR cycloconverters. The results presented in this chapter showed that the proposed cycloconverters are able to provide AC-AC conversion at higher efficiencies maintaining better power quality than the conventional 8 SCR cycloconverters. Another advantage worth mentioning here is that, the proposed topologies are able to provide output voltages with controllable amplitude and frequencies both smaller and greater than the input ones. In summary, the proposed switch mode cycloconverter topologies render wider range of AC-AC conversion ensuring higher power quality.

CHAPTER 9
CONCLUSION

9.1. Summary

The work presented in this thesis is focused on the design of single phase switch mode cycloconverters. The designed cycloconverters consist of two SMPS based converters namely the P and the N converters. The proposed converters provide control in terms of both frequency and amplitude of the output voltage. Compared to conventional 8 SCR cycloconverters these switch mode cycloconverters consist of reduced number of switches. The incorporation of switch mode topologies provides some advantageous features in the proposed topologies. Firstly, compared to conventional single phase cycloconverters, where, output voltage higher than the input is not possible, the proposed topologies provide output voltage both higher and lower than the supply voltage with the control of the duty ratio of the SMPS converters. Secondly, conventional cycloconverters were not able to supply output frequency higher than the input, whereas in the proposed cycloconverters output frequency higher than the input AC supply is obtainable. Finally, the proposed P and N converters have reduced number of solid state switches to half compared to conventional 8 SCR cycloconverters. With the reduction of switches the switching losses has been reduced and the converter efficiency has increased. Moreover, the proposed circuits have to deal with less number of isolation schemes and the number of drives is reduced. As a result, the proposed topology has higher reliability. The control of the proposed topology is accomplished with open loop sliding control which is simpler than the complex closed loop current sensing control techniques. The analysis of the proposed switch mode topologies are executed by simulating the cycloconverters at different duty cycle and different switching frequencies for a specific load. Then the simulation results are studied to determine the optimum operating point defined by a specific duty ratio and switching frequency for a particular load under consideration. These operating points are considered to be the control specification of the cycloconverters in open loop sliding control. The performance of the proposed topologies are evaluated in terms of standard metrics like, THD, input power factor, output voltage, output frequency and efficiency along the range of the duty cycle of the control signal. Results showed that, compared to conventional cycloconverters, the proposed topologies are able to perform AC-AC conversion ensuring better power quality at higher efficiencies and are applicable for wider range of load voltage and frequency demands.

9.2. Scope for future work

The proposed cycloconverter topologies provide satisfactory results for the resistive and motor load under consideration. In practice the electromechanical load connected to the cycloconverter output may show variation in their operating condition with time, which is known as the dynamic behavior. To cope up with this practical phenomenon, the behavior of the proposed cycloconverters may be analyzed under dynamic load. Future extension of this work may include development of the mathematical model of the proposed topologies by developing the transfer functions of the P and N converters. The driving circuit may incorporate control algorithms like particle swarm optimization (PSO) or fuzzy logic to generate the control pulses under a specific load to optimize the performance of the proposed cycloconverters.

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