Analysis of Double-Gate (DG) MOSFETs through a Non Charge-Sheet Model.

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by

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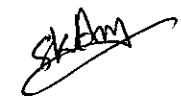

(Shaikh Asif Mahmood)

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Dedication

To My Parents

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Abstract

An analytical model has been developed to represent undoped symmetric Double Gate Field Effect Transistors (DGFET). Simple one dimensional Poisson's equation has been solved in the gate-to-gate direction. The solution gives direct expressions of potential profiles along the silicon thickness. The critical role of the silicon thickness on threshold voltage, subthreshold slope and volume inversion effects has been studied. Conditions of weak and strong volume inversion have been analyzed. The current-voltage relation has been derived by taking the gradual channel approximation. The potential profile along the oxide-silicon interface, as well as that inside the silicon has been calculated. These potential profiles would give valuable information regarding field-constraints in designing sub 100nm devices. Using the electric field profile channel length modulation (CLM) effect has been calculated. Effects of the channel length on device performance have been analyzed through a quasi 2D analysis. The potential profile calculated through the gradual channel approximation has been used to solve the Poisson's equation along the channel length direction. The solution is then superimposed on a remnant 2D solution to achieve the two dimensional potential profile. The resulting expression of the threshold voltage incorporates the short channel effects. It has been shown that the effect of threshold voltage roll-off, observed in conventional MOSFETs for dimensions below 100nm, can be compensated in the DGFET structure through careful adjustment of the silicon thickness. Improvements in performance of the DGFET structure in terms of current drivability, Short Channel Effects, Subthreshold Slope, etc. compared to conventional bulk MOSFET has been analyzed. Results obtained through our model are in agreement with published simulation results.

Chapter 1

Introduction

1.1 Transistor Scaling

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been the most important device for today's advance Integrated Circuit (IC) industry. The size of the Metal-Oxide-Semiconductor (MOS) transistor has been continually reduced by a factor of two every two years, which has resulted in chips which are significantly faster, contain more transistors, and consume less power per transistor in every generation. With ever demanding market for higher speed and lower power dissipation and higher packing density, the MOS transistor size have shrunk from a few micrometers to less than a quarter micrometer. Transistor scaling has been made possible by the improved lithographic capability to print shorter gate lengths and the ability to grow nearly perfect insulators with ever decreasing thickness.

Even if lithography and etching techniques can provide the necessary dimensions, bulk CMOS will run into a number of short channel effects associated with transistor scaling. The short channel effect (SCE) is characterized by threshold voltage (V_t) rolloff, drain induced barrier lowering (*DIBL*), and subthreshold swing S. As the gate length (L_G) of a MOSFET is scaled with all other device parameters held constant, S increases and V_t decreases, which degrades MOSFET performance. The ratio of on current to off current (I_{ON}/I_{OFF}) is reduced, giving designers a tradeoff between circuit speed and static power dissipation.

1.2 Alternative Design Approach

Currently, a number of front-end process solutions can be employed for scaling bulk CMOS to avoid unwanted SCE. These include high-k dielectrics, incorporation of metal gates, and elevation of the source and drain regions. High-k dielectrics can be used to decrease the effective oxide thickness without increasing I_{OFF} by reducing oxide tunneling current. Metal gates solve the gate poly-Si depletion problem, which causes an increase in the oxide capacitance and lowers I_{ON}. Elevated source/drain regions allow for lower series resistance and thus, greater ON current. Also, tailoring the doping profile with retrograde channel profiles, halo ion implants, and ultra-shallow junction depths is often performed in order to tame the SCE. However, these improvements are not expected to push CMOS scaling down below the $65nm$ [1, 2].

As the limit of bulk Si CMOS scaling approaches, new devices with slight variations to classical bulk CMOS have brought much attention to university labs and industry alike. Some of these devices include partially- and fully-depleted silicon-on-insulator (SOI), the gate-all-around or surrounding-gate MOSFET, SiGe MOSFETs, low-temperature CMOS, and double-gate (DG) MOSFETs. With the possibility for scaling down to $10nm$ gate lengths [3, 4], DG MOSFET devices show much promise. The benefits include higher drive current, improved subthreshold swing, greater SCE control, and circuit design flexibility.

1.3 Modeling of DG MOSFET

As CMOS scaling is approaching its limits due to processing as well as fundamental considerations, double-gate (DG) MOSFET is becoming an intense subject of VLSI research. In theory, DG MOSFETs can be scaled to the shortest channel length possible for a given oxide thickness [5]. Among the advantages advocated for double-gate MOSFETs are: ideal 60mv/decade subthreshold slope, volume inversion [6], setting of threshold voltage by the gate work function thus avoiding dopants and associated number

fluctuation effects, etc. DG MOSFETs can be fabricated in three basic configurations: Planar, Fin, and Vertical [7]. Several approaches for the device architecture have been explored: gate-all-around (GAA) [8], folded-gate [9], Fin-gate [10], Self-alignment [11-12] etc.

Analytic current-voltage (I-V) models are indispensable in compact modeling and comprehension of the fundamentals of MOSFET characteristics. In a bulk MOSFET, the starting point is the Pao-Sah integral based on Poisson and current continuity equations with gradual channel approximation. The Pao-Sah integral uses the channel quasi-Fermi potential and contains both the drift and diffusion current components hence is valid under all regions of MOSFET operation (subthreshold, linear, saturation). However, mathematical form renders no general analytic solution. This would necessitate the charge sheet approximation, which would lead to further simplification into separate current expressions for different bias regions. The final piecewise current solutions, would cause severe numerical problems like convergence in compact modeling application. Charge-sheet models are not in agreement with numerical simulation results without fitting terms or parameters and require lengthy and time consuming computations. Non charge-sheet approximation is a key to the proper depiction of "volume inversion" in subthreshold. Non charge-sheet approaches of DG MOSFETs have been reported by a number of groups [13-16]. But they didn't obtain the source to drain potential profile along the channel, which would require obtaining electric field profile, carrier profile and channel length modulation (CLM) effect. Expression of threshold voltage obtained by Meindl *et al.* [38] didn't consider the effect of drain to source voltage, which would be important to show drain induced barrier lowering (DIBL) effect.

1.4 Thesis Objective

The focus of the work will be to analyze a double-gate (DG) MOSFET through analytical modeling. Gate to gate potential profile and *I-V* characteristics of a double-gate (DG) MOSFET with undoped/lightly doped body using non-charge sheet model will be derived

from analytic solutions of 1-D Poisson's equation. Source to drain potential profile will be obtained using the gate to gate potential profile and the current equation. Carrier density profile and electric field profile from the source to drain will be obtained from the potential profile. Electric field profile will be used to obtain channel length modulation (CLM) effect. Short-channel threshold voltage model will be derived based on an analytical solution of the 2-D Poisson's equation, which includes the effect of drain to source voltage, V_{ds}. Besides the effect of drain to source voltage on threshold will be shown by 1-D analysis of Poisson's equation. Furthermore, comparison of performance between various double-gate MOSFET structures will be presented.

1.5 Thesis Outline

Chapter 1 discusses about the background and intention of this thesis and providing a general idea of what the thesis presents.

In chapter 2, theory of Single Gate and Double Gate MOSFETs has been studied and literature review of DG MOSFETs has been presented.

In chapter 3 analytical models for the study of Double Gate MOSFET have been developed. A continuous *I–V* model is derived from analytic solutions of 1-D Poisson's and current continuity equations for long channel DG MOSFETs. A potential profile has been obtained from the *I-V* model. From the electric field profile channel length modulation (CLM) effect has been presented. A compact, physical, short-channel threshold voltage model has been derived based on an analytical solution of the 2-D Poisson equation, which includes the effect of drain to source voltage, V_{ds}.

Chapter 4 covers the analysis of graphical results obtained from our developed model. Analysis of the three types of DG MOSFET structures is also presented.

Chapter 5 summaries on the findings of this thesis and suggests on possible future works.

Chapter 2

Analysis of SG and DG MOSFET

2.1 Single-gate (conventional) MOSFET

A single-gate (SG) MOSFET (Figure 2.1) consists of a drain contact and a source contact with a channel in between. The channel is doped in a way so that it will not conduct when a potential is applied between the drain and source. It cannot conduct because it has no charge carriers of the type produced by the source electrode. If a positive potential (voltage) is applied between the gate electrode and the source then the free holes (which are positively charged) will be repelled from the region of the substrate under the gate (the channel region). These holes are pushed downward into the substrate, leaving behind a carrier-depletion region. The depletion region is populated by the bound negative charge associated with the acceptor atoms. When a sufficient number of electrons accumulate under the gate, an *n* region is in effect created, connecting the source and drain regions. Now if a voltage is applied between drain and source, current flows through this induced *n* region. The induced *n* region thus forms a channel for current flow and correspondingly the MOSFET is called an n-channel MOSFET.

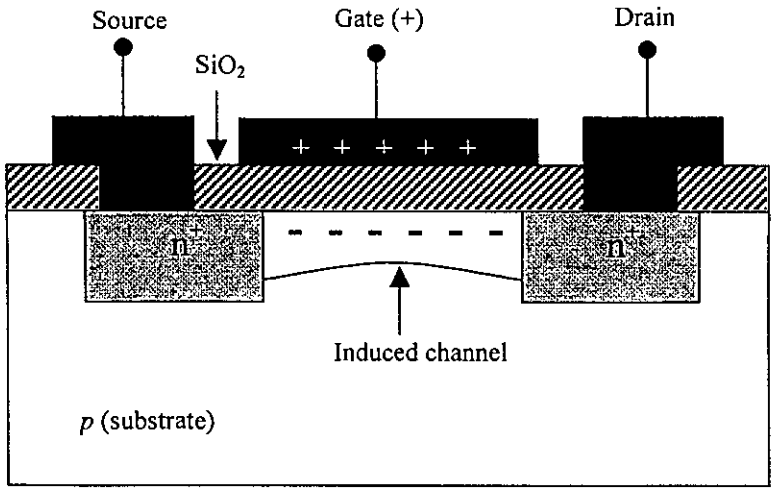

Figure 2.1 Basic structure of a single-gate (SG) MOSFET

The description above indicates that for the MOSFET to conduct, a channel has to be induced. Then increasing gate to source voltage enhances the channel, hence the name enhancement-type MOSFET. Note that the n-channel device needs a positive voltage on its gate relative to the source to make it conduct. On the other hand the p-channel device needs a negative voltage on its gate to make it conduct. Its charge carriers are positive and hence the drain needs to be negative relative to the source in order to attract the carriers and produce a current flow.

2.2 Short-Channel Effects and DG SOI MOSFETs

Two key characteristics of a MOSFET are the threshold voltage (V_{th}) and the subthreshold swing (S). The threshold voltage is the value of the gate voltage that turns on the transistor by inducing a highly conductive channel from the source to the drain. The subthreshold swing is the gate voltage change that is required for an order-of-magnitude change of the drain current in the subthreshold region. As the channel length (L) of a typical MOSFET is reduced with all other parameters held constant, the threshold voltage decreases and the subthreshold swing increases, as illustrated in Figure 2.2.

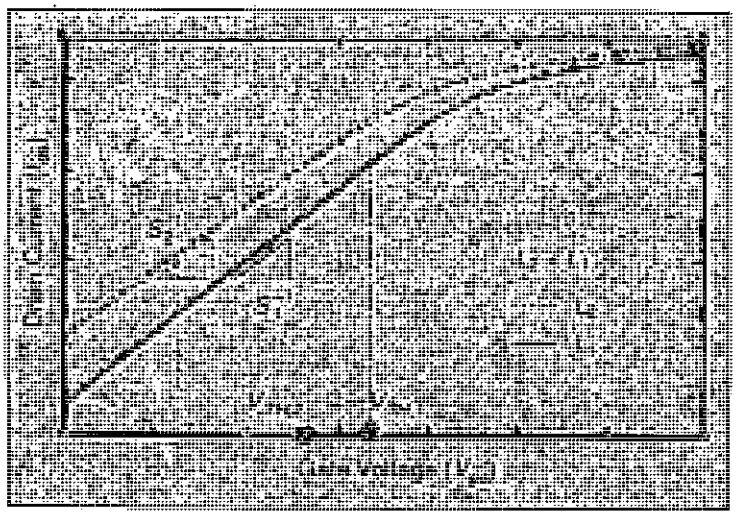

Figure 2.2 Impact of short-channel effects on drain current. As the channel length (L) is reduced, subthreshold swing increases ($S_2 > S_1$) and threshold voltage decreases ($V_{TH,2} < V_{TH,1}$). [3]

Collectively, threshold voltage rolloff and subthreshold swing rollup are commonly known as short-channel effects (SCEs). In consequence of SCEs, the ratio of the drive (ON) current to the leakage (OFF) current is substantially reduced, which imposes severe tradeoffs between circuit speed and standby power. In addition, SCEs amplify the impact of process variations on CMOS circuits.

In conventional bulk MOSFETs, SCEs are caused by the lateral electric fields from the source to channel and drain to channel. As L decreases, the lateral fields terminate on more charge further into the channel, which essentially steals the charge that would normally be terminated by the gate voltage in a long-channel device. This stealing of charge by the lateral fields effectively lowers the source-to-channel barrier, which controls the conduction of electrons from source to drain. To limit this charge stealing, and thus mitigate SCEs, heavy channel doping is exploited in bulk MOSFETs. As the gate length is scaled to 50 nm and below, the required channel doping concentration is expected to be a few times 10^{18} cm^{-3} and above [17]. These extremely high doping levels, however, lead to i) severe degradation of the carrier mobility as the impurity scattering becomes dominant [17] and ii) severe threshold voltage variations due to random microscopic fluctuations of dopant atoms [18].

The DG MOSFET, as illustrated in Figure 2.4, does not require channel doping for SCE control. Instead, this novel device uses a second gate and a fully depleted silicon film as the channel to enhance the electrostatic control of the gates over the channel, which effectively suppresses the impact of the source/drain. The thin silicon film is undoped or lightly doped (typical doping concentration $N_A<10^{16}$ cm^{-3} [19]) to guarantee the full depletion condition. For the most effective SCE control, the two gate-oxide layers are equally thin. Use of an identical material for both gates results in a symmetric DG MOSFET.

2.3 Double-gate metal-oxide-semiconductor

A dual-gate-silicon-on-insulator DGSOI structure consists, basically, of a silicon slab sandwiched between two oxide layers (Figure 2.3 (a)). A metal or a polysilicon film contacts each oxide. Each one of these films acts as a gate electrode, which can generate an inversion region near the Si–SiO_2 interfaces with an appropriate bias. Thus we would have two conventional MOSFETs sharing the substrate, source, and drain. The circuit symbol [41] is shown in Figure 2.3 (b).

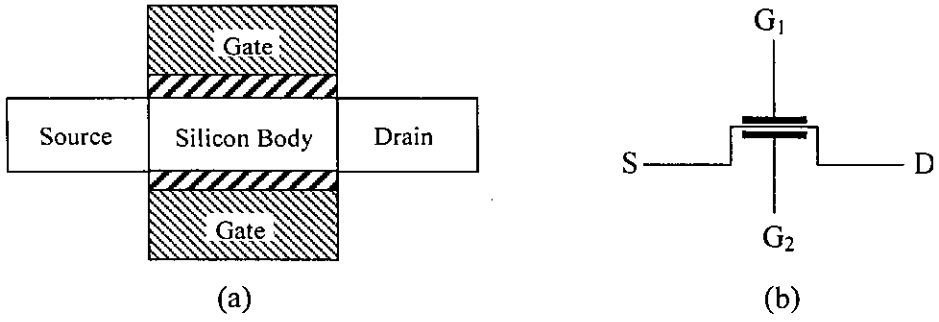

Figure 2.3 (a) SOI MOSFET with top and bottom gate **(b)** Circuit Symbol

2.4 Concept of volume inversion

The outstanding feature of these structures lies in the concept of volume inversion, introduced by Balestra *et al* [6]. If the Si film is thicker than the sum of the depletion regions induced by the two gates, no interaction is produced between the two inversion layers, and the operation of this device is similar to the operation of two conventional MOSFETs connected in parallel. However, if the Si thickness is reduced, the whole silicon film is depleted and an important interaction appears between the two potential wells. In such conditions the inversion layer is formed not only at the top and bottom of the silicon slab i.e., near the two silicon–oxide interfaces, but throughout the entire silicon film thickness. The device under this condition operates in 'volume inversion', i.e., carriers are no longer confined at interfaces, but distributed throughout the entire

silicon volume. Several authors have claimed that volume inversion presents a significant number of advantages, such as

i. enhancement of the number of minority carriers
ii. increase in carrier mobility and velocity due to reduced influence of scattering associated with oxide and interface charges and surface roughness
iii. as a consequence of the latter, an increase in drain current and transconductance
iv. decrease of low frequency noise
v. a great reduction in hot-carrier effects

2.5 Literature review

The first publication describing a double-gate SOI MOSFET dates back to 1984. The device received the acronym XMOS because of the resemblance of the structure with the Greek letter Ξ [20]. This initial paper predicted the good short-channel characteristics of such a device. The first fabricated double-gate SOI MOSFET was the "fully DEpleted Lean-channel TrAnsistor (DELTA, 1989)", where the silicon film stands vertical on its side (Figure 2.4) [21]. Later vertical-channel, double-gate SOI MOSFETs (FinFET) [10] was implemented. Volume inversion was discovered in 1987 [6], and the superior transconductance brought about by this phenomenon were first experimentally observed in 1990 in the first practical implementation of a planar double-gate MOSFET called the "gate-all-around" (GAA) device [22] (Figure 2.5).

The structure that theoretically offers the best possible control of the channel region by the gate is the surrounding-gate MOSFET. Such a device is usually fabricated using a pillar-like silicon island with a vertical-channel which include the cylindrical thin-pillar transistor (CYNTHIA) (Figure 2.6) [23] and the pillar surrounding-gate MOSFET [24].

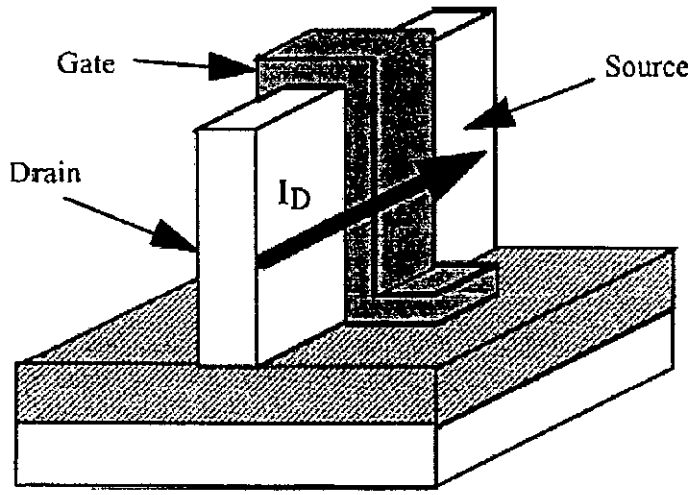

Figure 2.4 DELTA/FinFET structure.

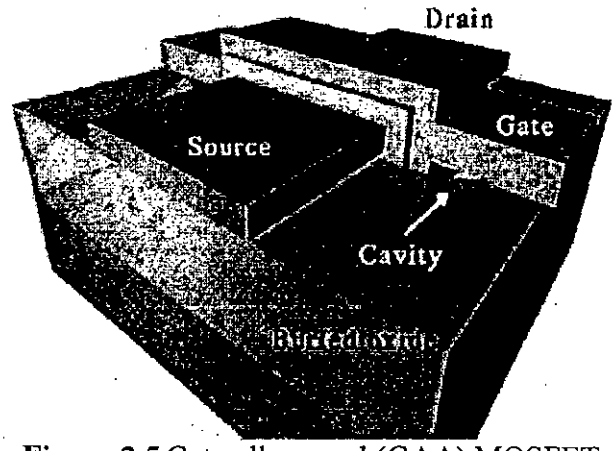

Figure 2.5 Gate-all-around (GAA) MOSFET.

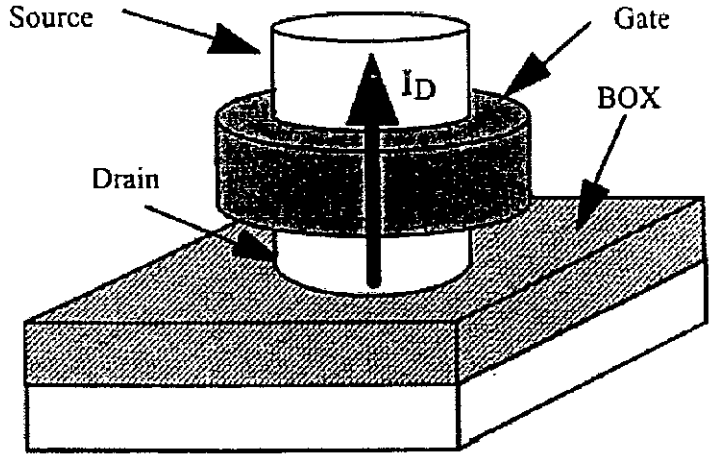

Figure 2.6 CYNTHIA/surrounding-gate MOSFET structure.

The effects of volume inversion in thin-film short-channel SOI MOSFETs and the efficacy of dual-gate operation in enhancing their device performance have been analyzed by R. F. Pierret *et al.* [25] using two-dimensional device simulations and one-dimensional analytical computations. Their analyses have been restricted to the strong inversion regime, which is the practically useful region of operation of SOI MOSFETs. In this region, they suggested that when compared at constant V_g - V_t values, the dual-channel volume inverted devices do not offer significant current-enhancement advantages, other than that expected from the second channel, over the conventional single-channel devices for silicon thickness in the 0.1-μm range.

K. Suzuki *et al.* [26] established a scaling theory for double-gate SOI MOSFETs, which gives guidance for the device design. They calculated dependence of subthreshold slope S on device parameters. According to their theory, a device can be designed with a gate length of less than 0.1μm while maintaining the ideal subthreshold factor, which is verified numerically with a two-dimensional device simulator. In a latest publication [27], they developed models for short channel n^+-p^+ double-gate SOI MOSFETs by solving a two-dimensional (2-D) Poisson's equation in the channel region, and showed how to design a device with a decreased gate length, suppressing short channel threshold voltage shift ΔV_{th} and subthreshold swing (S-swing) degradation.

Giorgio Baccarani *et al.* [28] presented a compact model for the Double-Gate MOSFET (DG-MOSFET), which accounts for quantum mechanical effects, including motion quantization normal to the Si-SiO_2 interface, band splitting into subbands and non-static effects in the transport model. The model holds both in subthreshold and strong inversion, and ensures a smooth transition between the two regions.

J. M. Hergenrother *et al.* [29] showed that short-channel effects in fully-depleted double-gate (DG) and cylindrical, surrounding-gate (Cyl) MOSFETs are governed by the electrostatic potential as confined by the gates, and thus by the device dimensions. For equivalent silicon and gate oxide thicknesses, evanescent-mode analysis indicates that Cyl-MOSFETs can be scaled to 35% shorter channel lengths than DG-MOSFETs.

S.-L. Jang *et al.* [30] have developed an analytical drain current model for symmetric double-gate SOI MOSFETs using a quasi-two-dimensional Poisson's equation. The model applicable for digital/analog circuit simulation contains the description of the subthreshold, near threshold and above-threshold regions of operation by one single expression. They considered effects of the source/drain resistance; on important short channel effects such as- velocity saturation, drain induced barrier lowering, channel length modulation, self-heating effect due to the low thermal conductivity of the buried oxide, impact-ionization of MOS devices, parasitic bipolar junction transistor associated with drain breakdown, etc.

B. Majkusiak *et al.* [31] have analyzed the influence of the semiconductor film thickness in the double-gate silicon-on-insulator (SOI) MOSFET on the electron concentration distribution, electron charge density, threshold voltage, electron effective mobility, and drain current. The consideration of the semiconductor region is based on two descriptions: the "classical" model based on a solution to the Poisson's equation and the "quantum" model based on a self-consistent solution to the Schrodinger's and Poisson's equation system. The electron effective mobility and the drain current are calculated with the use of the local mobility model.

Y. Taur [14] has derived a one-dimensional (1-D) analytical solution for an undoped (or lightly-doped) double-gate MOSFET by incorporating only the mobile charge term in Poisson's equation. The solution gives closed forms of band bending and volume inversion as a function of silicon thickness and gate voltage. A threshold criterion has been derived which serves to quantify the gate work function requirements for a double-gate CMOS. Then in [19] the solution is applied to both symmetric and asymmetric DG MOSFETs to obtain closed forms of band bending and inversion charge as a function of gate voltage and silicon thickness. It is shown that for the symmetric DG device, "volume inversion" only occurs under subthreshold conditions, with a slightly negative impact on performance. Comparisons under the same off-state conditions show that the on-state

inversion charge density of an asymmetric DG with one channel is only slightly less than that of a symmetric DG with two channels, if the silicon film is thin. From the analytic solutions, expressions for the various components of the equivalent capacitance circuit have been derived for symmetric and asymmetric DG devices.

J. G. Fossum *et al.* [32] have developed a compact physics-based quantum-effects model for symmetrical double-gate (DG) MOSFETs of arbitrary Si-film thickness. The model, based on the quantum-mechanical variational approach, not only accounts for the thin Si-film thickness dependence but also takes into account the gate–gate charge coupling and the electric field dependence; it can be used for FD/SOI MOSFETs as well. The analytical solutions, verified via results obtained from self-consistent numerical solutions of the Poisson and Schrödinger equations, provide good physical insight regarding the quantization and volume inversion due to carrier confinement, which is governed by the Si-film thickness and/or the transverse electric field. A design criterion for achieving beneficial volume-inversion operation in DG devices has quantitatively defined for the first time. Further, the utility of the model for aiding optimal DG device design, including exploitation of the volume-inversion benefit to carrier mobility, is exemplified.

J. D. Meindl *et al.* [33] have developed an analytical subthreshold swing (S) model for symmetric DG MOSFETs using evanescent-mode analysis. Through a concept of effective conducting path, it explains a doping concentration (N_A) dependence of S, providing a unified understanding of previous models and leading to a new model for undoped DG MOSFETs. Expressions of a scale length have been derived, which expedite projections of scalability of DG MOSFETs and its requirement.

T. Ernst *et al.* [34] have analyzed the operation of 1–3 nm thick SOI MOSFETs, in double-gate (DG) mode and single-gate (SG) mode (for either front or back channel). They found some typical effects in these ultra-thin MOSFETs such as- threshold voltage variation, large influence of substrate depletion underneath the buried oxide, absence of drain current transients, and degradation in electron mobility. By comparing SG and DG configurations they have shown the superiority of DG-MOSFETs: ideal subthreshold

swing and remarkably improved transconductance (consistently higher than twice the value in SG-MOSFETs). The experimental data and the difference between SG and DG modes have been explained by combining classical models with quantum calculations. They found that the key effect in ultimately thin DG-MOSFETs is volume inversion, which primarily leads to an improvement in mobility, whereas the total inversion charge is only marginally modified.

M. Wong *et al.* [35] have derived an analytical expression relating the potential and the electric field at the oxide–semiconductor interface of a symmetrical double-gate oxide-intrinsic semiconductor–oxide system. The expression is applicable to all regimes of operation. The "turn-on" behavior of the system has been studied and an extrapolated threshold voltage has been defined. Opposite to the behavior of a conventional bulk metal–oxide–semiconductor capacitor realized on a doped substrate, this threshold voltage was shown to decrease with increasing oxide thickness.

M. Alessandrini *et al.* [16] have developed an analytical model for the electron mobility limited by surface optical phonons and applied to the simulation of ultra-thin SOI MOSFETs. The developed model reproduces the main features of experimental data recently reported in the literature and has been implemented in a conventional device simulator. An application to the analysis of technological options such as doping concentration and silicon thickness in SOI MOSFETs, have been reported.

M. J. Kumar *et al.* [36] have discussed how the short channel behavior in sub 100 nm channel range can be improved by inducing a step surface potential profile at the back gate of an asymmetrical double gate (DG) silicon-on-insulator (SOI) metal–oxide–semiconductor field-effect-transistor (MOSFET) in which the front gate consists of two materials with different work functions.

Chapter 3

Modeling of DG FET

3.1 Derivation of *I-V* model

Let us consider an undoped (or lightly doped), symmetric DG MOSFET shown schematically in Figure 3.1(a). Following Pao-Sah's gradual channel approach [36], Poisson's equation along a vertical cut perpendicular to the Si film [Figure 3.1(b)] takes the following form with only the mobile charge (electrons) term:

$$\frac{d^2\psi}{dy^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{q(\psi - V)}{kT}} \qquad (1)$$

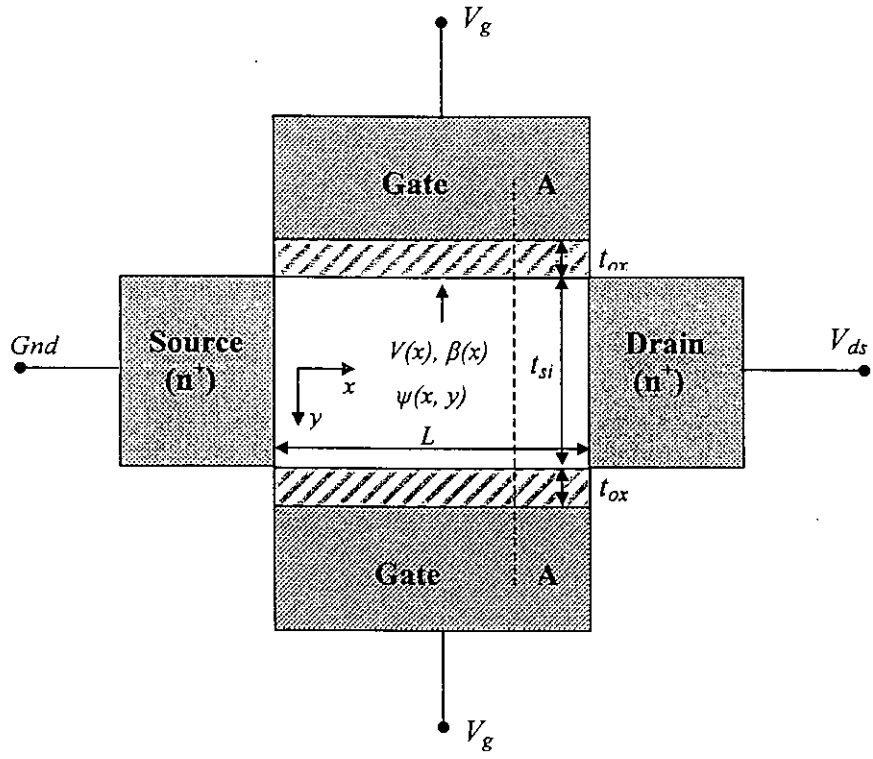

Figure 3.1(a) Schematic diagram of a DG MOSFET

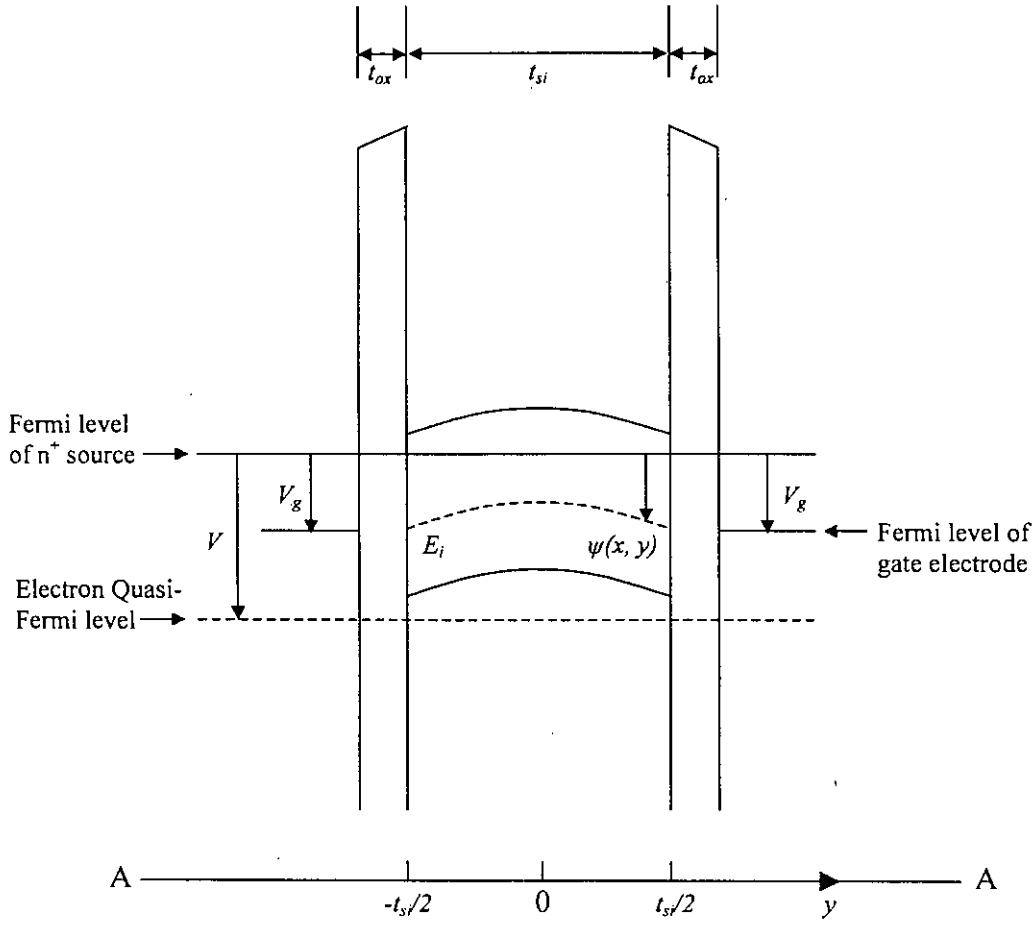

Figure 3.1(b) Band diagram along a vertical cut (AA) in (a).

where q is the electronic charge, ε_{si} is the permittivity of silicon, n_i is the intrinsic carrier density, $\psi(y)$ is the electrostatic potential [reference shown in Figure 3.1(b)] and V is the electron quasi-Fermi potential. Here we consider an nMOSFET with $\frac{q\psi}{kT} >> 1$ so that the hole density is negligible.

Since the current flows predominantly from the source to the drain along the x-direction, the gradient of the electron quasi-Fermi potential is also in the x-direction. This justifies the gradual channel approximation that V is constant in the y-direction. Equation (1) can then be integrated twice to yield the solution [14] (see Appendix I)

$$\psi(y) = V - \frac{2kT}{q}\ln\left[\frac{t_{si}}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}\cos\left(\frac{2\beta y}{t_{si}}\right)\right] \qquad (2)$$

where β is a constant (of y) to be determined from the boundary condition

$$\varepsilon_{ox}\frac{V_g - \Delta\phi - \psi(y = \pm\frac{t_{si}}{2})}{t_{ox}} = \varepsilon_{si}\left.\frac{d\psi}{dy}\right|_{y=\pm\frac{t_{si}}{2}} \qquad (3)$$

Here ε_{ox} is the permittivity of oxide, V_g is the voltage applied to both gates, t_{si} and t_{ox} are the silicon and oxide thicknesses respectively; and $\Delta\phi$ is the work function of both the top and bottom gate electrodes with respect to the intrinsic silicon. In other words, $\Delta\phi=0$ for midgap work function gate, $-E_g/2q$ for n^+ poly, and $+E_g/2q$ for p^+ poly, etc. Substituting (2) into (3) leads to

$$\frac{q(V_g - \Delta\phi - V)}{2kT} - \ln\left[\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}\right] = \ln\beta - \ln[\cos\beta] + \frac{2\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta\tan\beta \qquad (4)$$

For a given V_g, β can be solved from (4) as a function of V. Along the channel direction (x), V varies from the source to the drain. So does β. The functional dependence of $V(x)$ and $\beta(x)$ is determined by the current continuity condition which requires the current, $I_{ds}=\mu W Q_i dV/dx$=constant independent of V or x. Here μ is the effective mobility, W is the device width, and Q_i is the total mobile charge per unit gate area. Integrating $I_{ds}\,dx$ from the source to the drain and expressing dV/dx as $(dV/d\beta)(d\beta/dx)$, Pao-Sah's integral [36] can be written as

$$I_{ds} = \mu\frac{W}{L}\int_0^{V_{ds}} Q_i(V)dV = \mu\frac{W}{L}\int_0^{V_{ds}} Q_i(\beta)\frac{dV}{d\beta}d\beta \qquad (5)$$

where β_s, β_d are solutions to (4) corresponding to $V=0$ and $V=V_{ds}$ respectively. From Gauss's law, $Q_i=2\varepsilon_{si}(d\psi/dy)_{y=tsi/2}$, which equals $2\varepsilon_{si}(2kT/q)(2\beta/t_{si})tan\beta$ using (2). $dV/d\beta$ can also be expressed as a function of β by differentiating (4). Substitute these factors in (5) and carry out the integration analytically, [15] we have:

$$I_{ds} = \mu \frac{W}{L} \frac{4\varepsilon_{si}}{t_{si}} \left(\frac{2kT}{q} \right)^2 \times$$

$$\left[\beta_s \tan \beta_s - \frac{\beta_s^2}{2} + \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox} t_{si}} \beta_s^2 \tan^2 \beta_s - \beta_d \tan \beta_d + \frac{\beta_d^2}{2} - \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox} t_{si}} \beta_d^2 \tan^2 \beta_d \right] \tag{6}$$

3.2 Determination of Potential profile

The channel current originating from the drain end and terminating in the source end is given by equation (6). The current at any point in the channel can be written as

$$I_x = \mu \frac{W}{x} \frac{4\varepsilon_{si}}{t_{si}} \left(\frac{2kT}{q} \right)^2 \times$$

$$\left[\beta_s \tan \beta_s - \frac{\beta_s^2}{2} + \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox} t_{si}} \beta_s^2 \tan^2 \beta_s - \beta_x \tan \beta_x + \frac{\beta_x^2}{2} - \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox} t_{si}} \beta_x^2 \tan^2 \beta_x \right] \tag{7}$$

where β_x is the constant (of y) corresponding to the voltage V_x in the channel.

As current at any point in the channel is constant, equations (6) and (7) can be equated as

$$x = L\frac{\left[\beta_s \tan\beta_s - \frac{\beta_s^2}{2} + \frac{\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta_s^2\tan^2\beta_s - \beta_x\tan\beta_x + \frac{\beta_x^2}{2} - \frac{\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta_x^2\tan^2\beta_x\right]}{\left[\beta_s \tan\beta_s - \frac{\beta_s^2}{2} + \frac{\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta_s^2\tan^2\beta_s - \beta_d\tan\beta_d + \frac{\beta_d^2}{2} - \frac{\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta_d^2\tan^2\beta_d\right]} \quad (8)$$

For a given V_g, V varies along the channel from the source to the drain and corresponding β_x varies from β_s to β_d. Corresponding potential variation from source to drain can be obtained from the equation (2). From the potential variation electric field variation along the x-direction can be obtained. The carrier profile can be obtained by

$$n = n_i e^{q(\psi - V)/kT} \quad (9)$$

3.3 Determination of pinchoff region

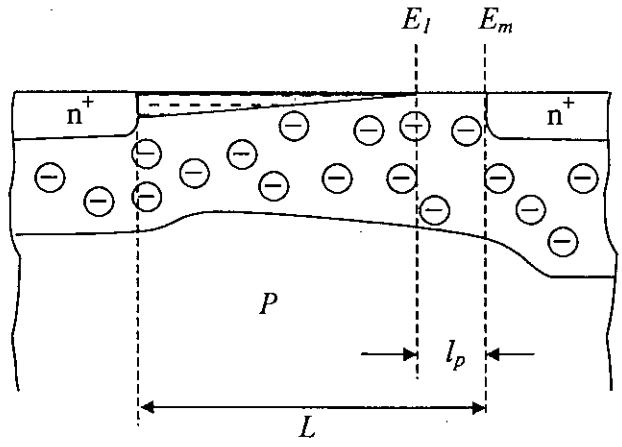

Figure 3.3 Channel above pinchoff for a single-gate MSOFET

According to one of the most accepted pseudo-two-dimensional analysis [37], the pinchoff region length can be written as

$$l_p = l_a \ln \frac{\sqrt{E_m^{\,2} - E_1^{\,2}} + E_m}{E_1} \qquad (10)$$

where E_m is the maximum magnitude of the x-directed electric field in the pinchoff region (figure 3.3), E_1 is the magnitude of the field in the beginning of the pinchoff region and l_a is a characteristic length given by

$$l_a = \sqrt{\frac{\varepsilon_{si} t_{ox} x_1}{3\varepsilon_{ox}}} \qquad (11)$$

where x_1 is the distance from the surface where the y-directed electric field is assumed to be zero. For a symmetric DG MOSFET the y-directed electric field is zero at the middle of the silicon film. So taking $x_1 = t_{si}/2$ for a symmetric DG MOSFET,

$$l_a = \sqrt{\frac{\varepsilon_{si} t_{ox} t_{si}}{6\varepsilon_{ox}}} \qquad (12)$$

Once the length of pinchoff region is obtained channel length modulation (CLM) effect can be determined.

3.4 Derivation of threshold voltage model

The solution of 2-D Poisson equation for a symmetric DG MOSFET can be found in the following form [38]

$$\psi(x,y) = \psi_0(x) + \psi_1(x,y) \qquad (13)$$

where $\psi_0(x)$ is the solution to the 1-D Poisson equation

$$\frac{d^2\psi_0}{dx^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{q}{kT}(\psi_0 - V)} \qquad (14)$$

with boundary conditions

$$\psi_0(0) = V_{bi} \qquad (15)$$

$$\psi_0(L) = V_{bi} + V_{ds} \qquad (16)$$

and $\psi_1(x, y)$ is the solution to the remnant 2-D equation

$$\frac{\partial^2\psi_1}{\partial x^2} + \frac{\partial^2\psi_1}{\partial y^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{q}{kT}(\psi_0 - V)}\left[e^{\frac{q}{kT}\psi_1(x,y)} - 1\right] \qquad (17)$$

with boundary conditions

$$\psi_1(0, y) = 0 \qquad (18)$$

$$\psi_1(L, y) = 0 \qquad (19)$$

$$\varepsilon_{ox}\frac{V_{GS} - \Phi_{MS} - \psi_1\left(x, \pm\frac{t_{si}}{2}\right) - \psi_0(x)}{t_{ox}} = \varepsilon_{si}\left.\frac{\partial\psi_1(x,y)}{\partial y}\right|_{y=\pm\frac{t_{si}}{2}} \qquad (20)$$

Here V_{bi} is the built-in voltage given as $V_{bi} = (kT/q)\ln(N_{D/S}/n_i)$, where $N_{D/S}$ is the source/drain doping density. Assuming $V = V_{ds}x/L$ the 1-D equation (14) can be solved as (see Appendix II)

$$\psi_0(x) = V_{ds}\frac{x}{L} + \psi_{0m} + \frac{kT}{q}\ln\left\{\sec^2\left[B\left(\frac{x}{L} - \frac{1}{2}\right)\right]\right\} \qquad (21)$$

where

$$\psi_{0m} = V_{bi} - \frac{2kT}{q}\ln\frac{2 + e^{\frac{qV_{bi}}{2kT}}\frac{L}{\lambda_D}}{\pi} \qquad (22)$$

$$B = \frac{\pi}{1 + 2e^{\frac{-qV_{bi}}{2kT}}\frac{\lambda_D}{L}} \qquad (23)$$

where λ_D is given as $\lambda_D = \sqrt{2\varepsilon_{si}kT/q^2 n_i}$ and can be called intrinsic Debye length. The complete solution of 2-D Poisson equation is given as: (Appendix II)

$$\psi(x,y) = V_{ds}\frac{x}{L} + \psi_{0m} + \frac{kT}{q}\ln\left\{\sec^2\left[B\left(\frac{x}{L}-\frac{1}{2}\right)\right]\right\} + \frac{V_{GS} - \Phi_{MS} - \psi_0(x)}{\eta}\frac{\cos\left[2\theta\left(\frac{y}{t_{si}}\right)\right]}{\cosh\theta} \quad (24)$$

where $\theta = (Bt_{si}/L)$, $\eta = 1+(2\theta/\gamma)\tanh\theta$, and $\gamma = (\varepsilon_{ox}t_{si}/\varepsilon_{si}t_{ox})$. The minimum potential in the channel will be at $\frac{d\psi}{dx} = 0$ and is found that

$$x = L\left[\frac{1}{2} + \frac{1}{B}\tan^{-1}\left(-\frac{q}{2kT}\frac{V_{ds}}{B}\right)\right] \quad (25)$$

The minimum sheet density of inversion carriers Q_{inv} is obtained by integrating their spatial density calculated from (24) and (25) throughout the entire channel thickness and at threshold it becomes [38]

$$Q_{TH} = 2n_i e^{\frac{q}{kT}\left(V_{ds}\frac{x}{L}+\varphi_{0m}\right)}\sec^2\left[B\left(\frac{x}{L}-\frac{1}{2}\right)\right]\int_{y=0}^{y=\frac{t_{si}}{2}} \times \exp\left\{\frac{q}{kT}\frac{V_{th} - \Phi_{MS} - V_{ds}\frac{x}{L} - \psi_{0m} - \frac{kT}{q}\ln\left\{\sec^2\left[B\left(\frac{x}{L}-\frac{1}{2}\right)\right]\right\}\cosh\left[2\theta\left(\frac{y}{t_{si}}\right)\right]}{\eta}\right\}dy \quad (26)$$

The relatively insignificant change of the carrier density in the gate direction under threshold condition allows the integral of (26) to be approximated [38] by using the value of the integrand at $y=t_{si}/4$, leading to an explicit expression for V_{th}

$$V_{th} = \Phi_{MS} + \eta \frac{kT}{q} \frac{\cosh\theta}{\cosh\left(\frac{\theta}{2}\right)} \ln\left[\frac{Q_{TH}}{n_i t_{si}}\right]$$
$$- \left[\eta \frac{\cosh\theta}{\cosh\left(\frac{\theta}{2}\right)} - 1\right]\left[V_{ds}\frac{x}{L} + \psi_{0m} + \frac{kT}{q}\ln\left\{\sec^2\left[B\left(\frac{x}{L} - \frac{1}{2}\right)\right]\right\}\right] \quad (27)$$

Where x is given by equation (25) and Q_{TH} is the sheet density of inversion carriers at threshold and is equal to $3.24*10^{10}\ cm^{-2}$ [38]. The long channel V_{th} model is

$$V_{th,long} = \Phi_{MS} + \frac{kT}{q}\ln\left[\frac{Q_{TH}}{n_i t_{si}}\right] \quad (28)$$

as θ approaches zero and η approaches unity for large L-values. Threshold voltage rolloff ΔV_{th}, which is the difference between short- and long-channel V_{th} obtained from (27) and (28) as

$$\Delta V_{th} = \left[\frac{kT}{q}\ln\frac{Q_{TH}}{n_i t_{si}} - V_{ds}\frac{x}{L} - \psi_{0m} - \frac{kT}{q}\ln\left\{\sec^2\left[B\left(\frac{x}{L} - \frac{1}{2}\right)\right]\right\}\right]\left[\eta\frac{\cosh\theta}{\cosh\left(\frac{\theta}{2}\right)} - 1\right] \quad (29)$$

The sheet density of inversion carriers at threshold, Q_{th} can be obtained by integrating the 1-D potential profile (2) throughout the entire channel thickness [38] and it becomes

$$Q_{th} = 2n_i \int_{y=0}^{y=t_{si}/2} e^{\frac{q\psi(y)}{kT}} = e^{\frac{qV}{kT}} \frac{8\beta}{t_{si}} \frac{\varepsilon_{si} kT}{q^2} \tan\beta \quad (30)$$

where β is the constant (of y) and V is the drain voltage. Using $Q_{th} = 3.24*10^{10}\ cm^{-2}$ [38] β can be determined from equation (30) for a certain drain voltage. Then from equation (4) threshold voltage can be obtained for different silicon thickness, t_{si}.

Chapter 4

Results and discussion

4.1 Gate to gate potential variation

Figure 4.1 shows the potential profile obtained from equation (2) (see section 3.1) along the gate to gate direction (y-direction in the figure 3.1(a)) at the source end (x=0, figure 3.1(a)) for three different silicon thicknesses. Here $y=0$ is the center of the channel (figure 3.1(a)). The gate voltage is chosen such that the channel enters into strong inversion condition. It is found that variation of surface potential (ψ_s) from the center potential (ψ_0) increases as silicon film thickness increases. In central region electric field is zero in all cases. For thicker silicon film ψ is almost zero at the center and the operation of the device is similar to the operation of two conventional MOSFETs connected in parallel and volume inversion does not occur. For thinner silicon film stronger influence from gate at the middle region is observed.

Figure 4.2 shows the same profile at the drain end for $V_{ds} = 1.5V$. Here almost flat potential profile at the drain end is observed for $t_{si}=5nm$. Variation in the potential increases for $V_{ds} = 1V$ as shown in figure 4.3. This is due to the fact that influence of the gate voltage is stronger near the drain end as compared to that in figure 4.2.

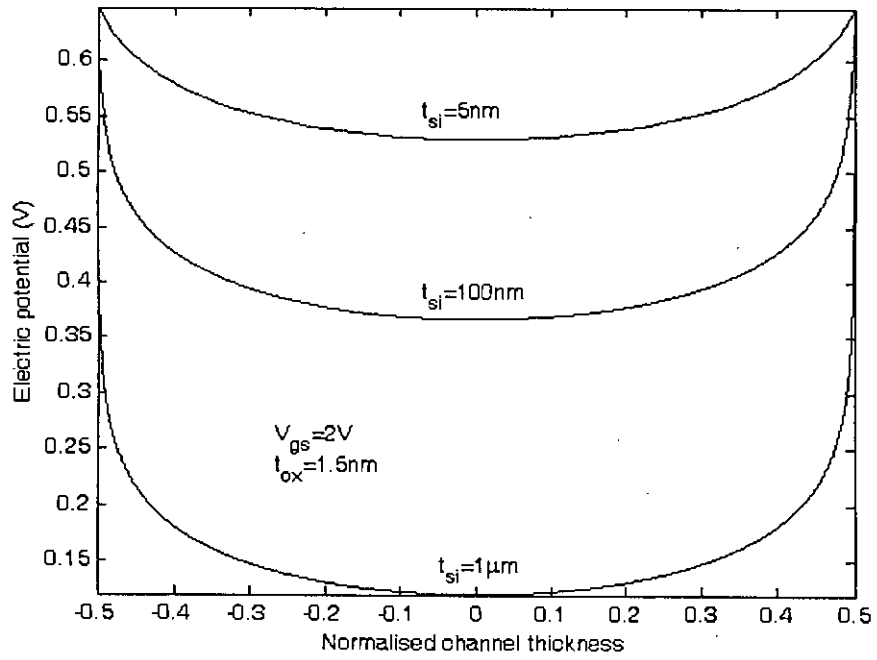

Figure 4.1 Potential ψ as a function of normalized channel thickness (y/t_{si}) at the source end ($x=0$) for three different values of t_{si}.

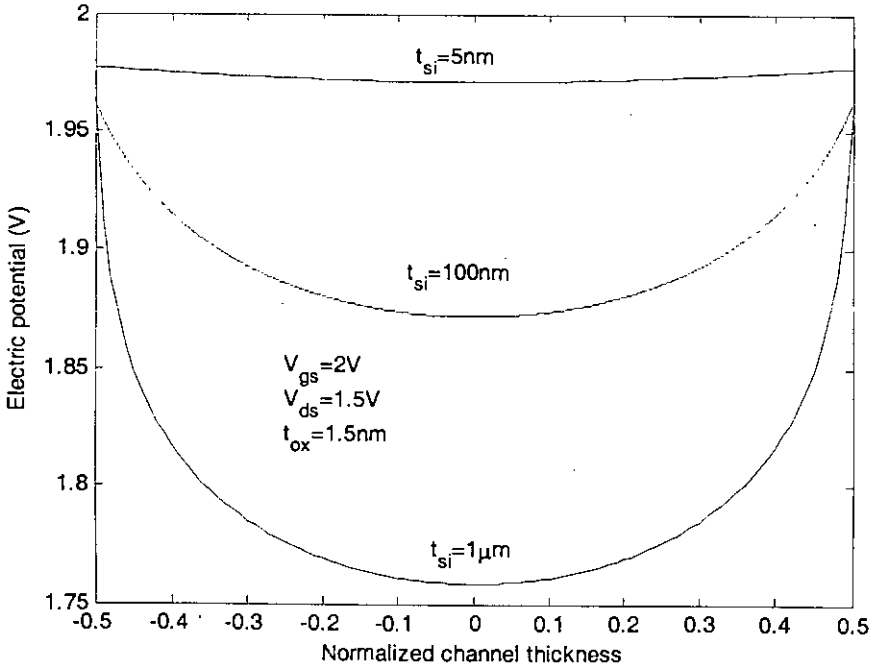

Figure 4.2 Potential ψ as a function of normalized channel thickness (y/t_{si}) at the drain end ($x=L$) when $V_{ds}=1.5V$.

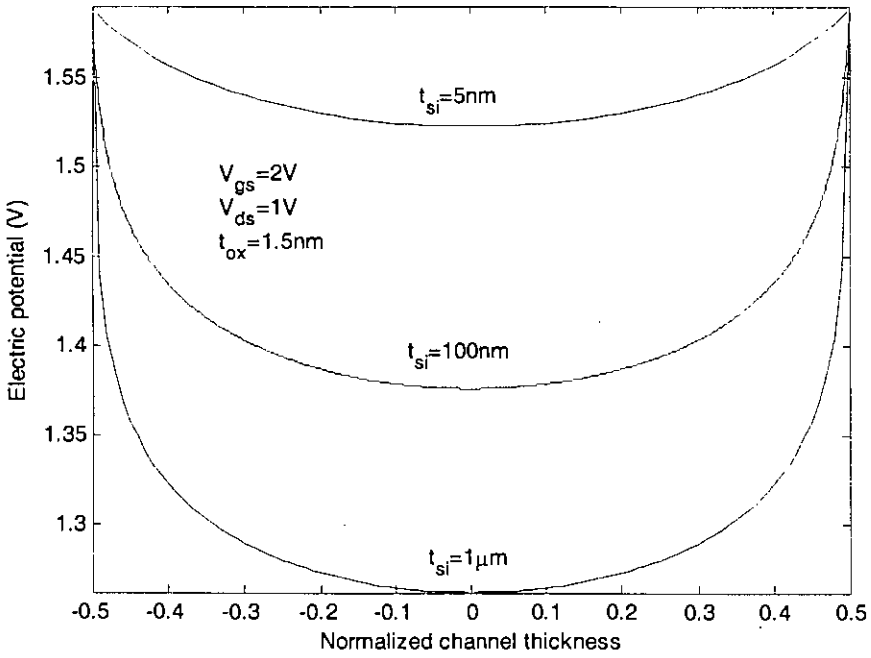

Figure 4.3 Potential ψ as a function of normalized channel thickness (y/t_{si}) at the drain end ($x=L$) when $V_{ds}=1V$.

4.2 Effect of silicon thickness on volume inversion

Figure 4.4 shows the surface potential variation (ψ_s) as a function of gate voltage. The potential variation at the center of the silicon film (ψ_0) is also shown by dotted lines. Here ψ_s does not vary with silicon thickness. It is also found that ψ_s and ψ_0 decouple at higher values of V_{gs}. For smaller silicon thickness, ψ_0 follows ψ_s for a longer range of gate voltage, signifying larger volume inversion.

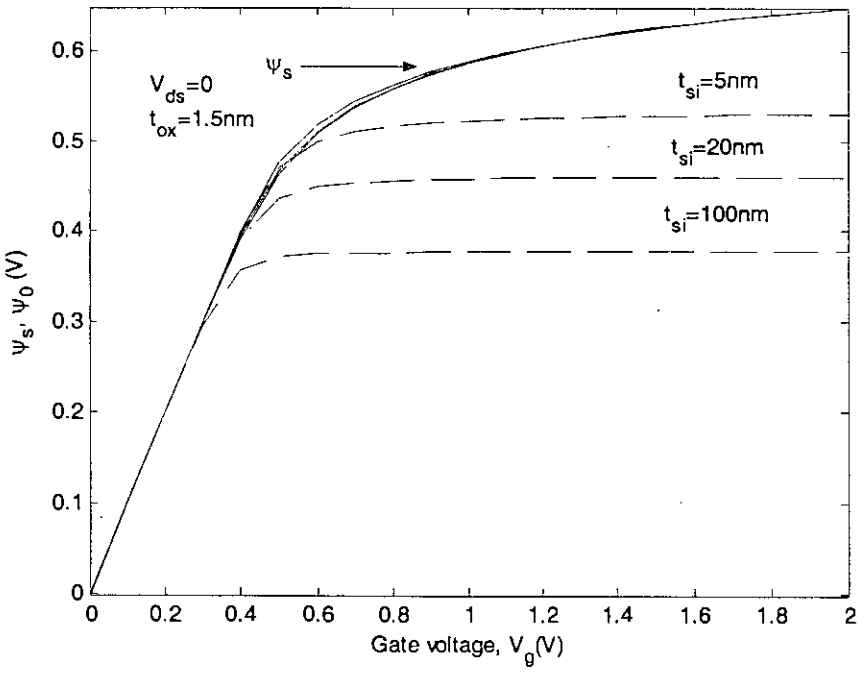

Figure 4.4 Potential variation at the surface ψ_s (continuous lines) and at the center of the silicon film ψ_0 (broken lines) as a function of gate voltage for three different values of t_{si}.

4.3 I-V characteristics with variation of silicon thickness

Figure 4.5 shows I_{ds}-V_{ds} curve for two different film thicknesses and it is found that current does not vary widely. Figure 4.6 shows I_{ds}-V_g characteristics for two different values of t_{si}. From the figure it is found that subthreshold current increases for increased silicon thickness but the subthreshold slope remains almost the same. So silicon thickness has little effect on post threshold current.

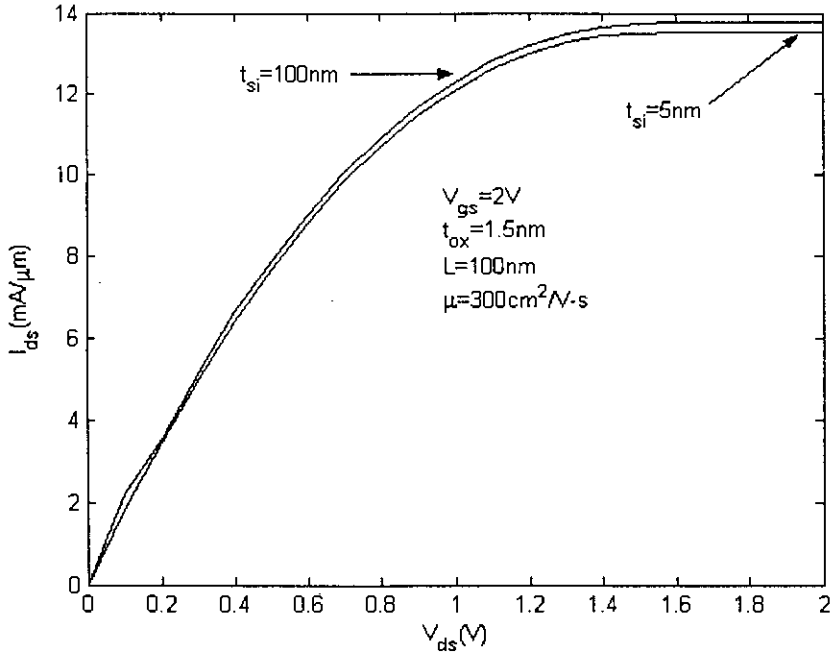

Figure 4.5 I_{ds}-V_{ds} curves for two different film thicknesses.

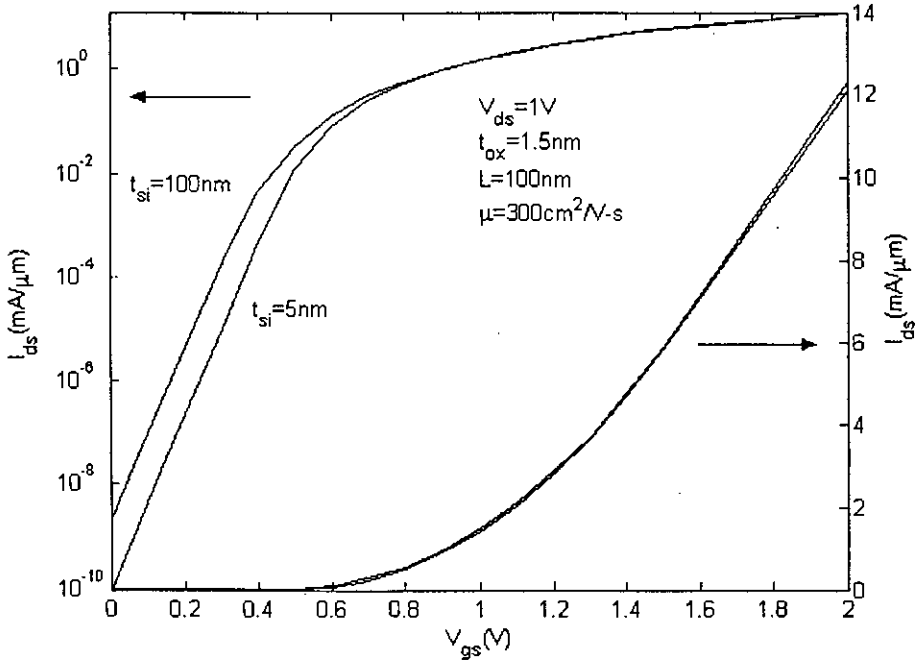

Figure 4.6 I_{ds}-V_g characteristics for two different values of t_{si} in both logarithmic (left) and linear (right) scales.

4.4 Effect of silicon thickness on the sheet density of mobile charge

Figure 4.7 shows the sheet density of mobile charge, $Q_i = 2\varepsilon_{si}(d\psi/dy)_{y=t_{si}/2}$ as a function of gate voltage for two silicon film thicknesses, assuming zero drain-to-source voltage. The charge subthreshold slope S measured as the inverse of the semi-logarithmic charge-gate voltage slope has a value very close to the ideal value of 60 mV per decade of charge change. This sub-threshold slope is not affected by gate oxide thickness (shown later), as it is in the case of conventional doped-body devices. It is found that the charge density increases exponentially above threshold (when V_{gs}>0.4V) and the threshold voltage decreases with the silicon thickness but subthreshold slope remains unchanged. We notice that the silicon thickness affects the carrier charge below threshold but has little effect above threshold. This is consistent with the fact that below threshold there is volume inversion and the charge is essentially proportional to silicon film thickness for a given gate voltage bias. Figure 4.7 also indicates that the on-off ratio increases as the silicon film thickness decreases.

Figure 4.8 shows the sheet density of mobile charge at the drain end as a function of drain to source voltage (V_{ds}) for two silicon film thicknesses. Here gate voltage is equal to 1V. The charge density decreases with V_{ds} at the drain end. The pinchoff occurs when V_{ds}>0.6V. It is found that below the saturation region (when V_{ds}<0.6V) silicon thickness has no effect in charge density. In the saturation region the sheet density of mobile charge increases with silicon thickness but the rate of decrease with V_{ds} (slope) remains same.

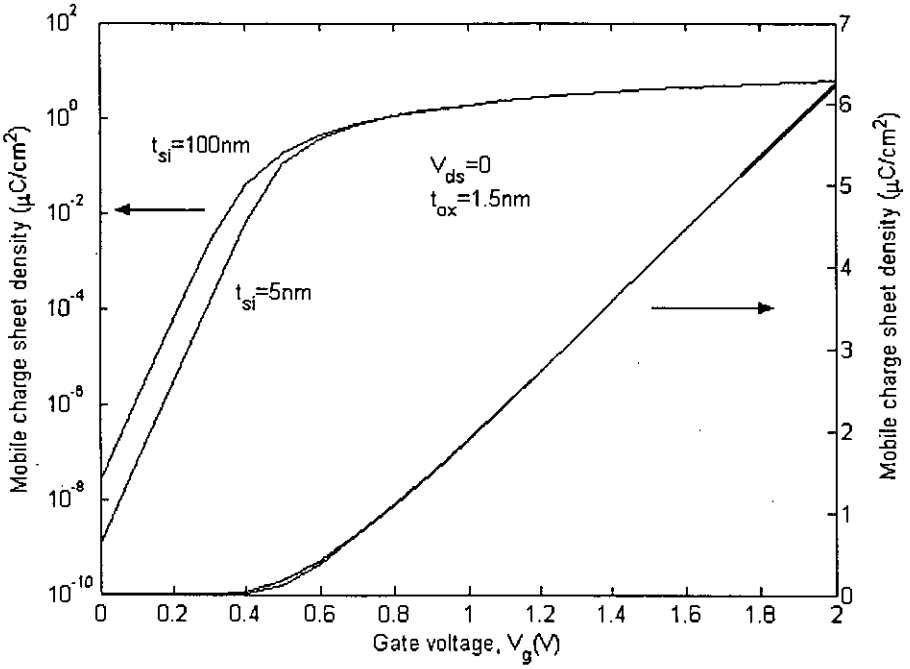

Figure 4.7 Sheet density of mobile charge as a function of gate voltage for two silicon film thicknesses in both logarithmic (left) and linear (right) scales.

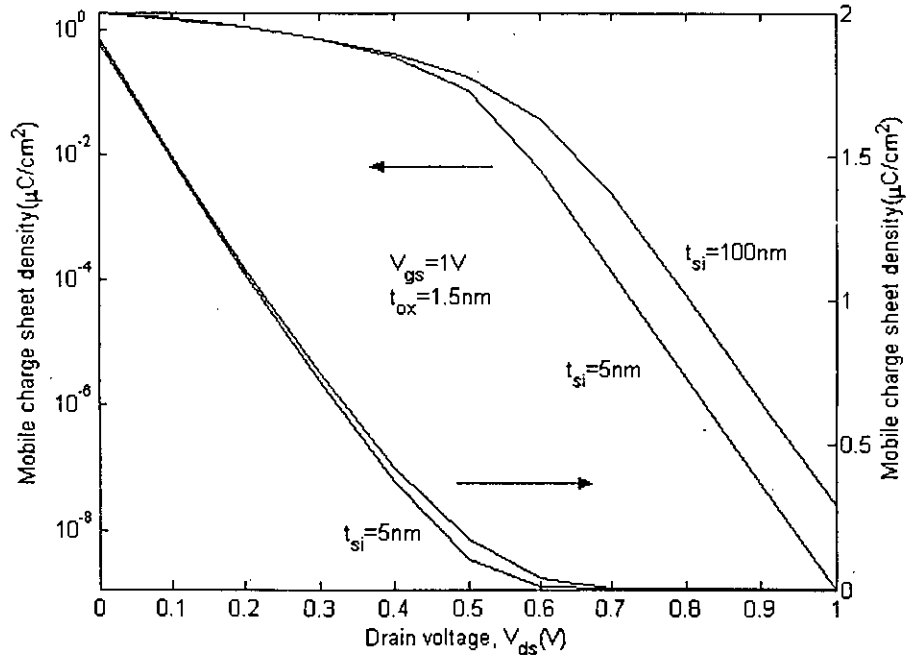

Figure 4.8 Sheet density of mobile charge as a function of drain voltage for two silicon film thicknesses in both logarithmic (left) and linear (right) scales.

4.5 Electron density profile

Figure 4.9 shows the electron density variation obtained from equation (9) along the gate to gate direction (y) at different positions along the channel (x). The drain end (at $x=L$) electron density is much lower than the electron density at other positions in the channel. Figure 4.10 shows the electron density at the surface as a function of position along the channel (x) at different drain voltages. For smaller drain voltages little variation of surface electron density from source to drain is observed. When the drain voltage is higher than the pinchoff voltage ($V_{ds}>V_{gs}-V_t$) drain end electron density falls much below than that in the source end.

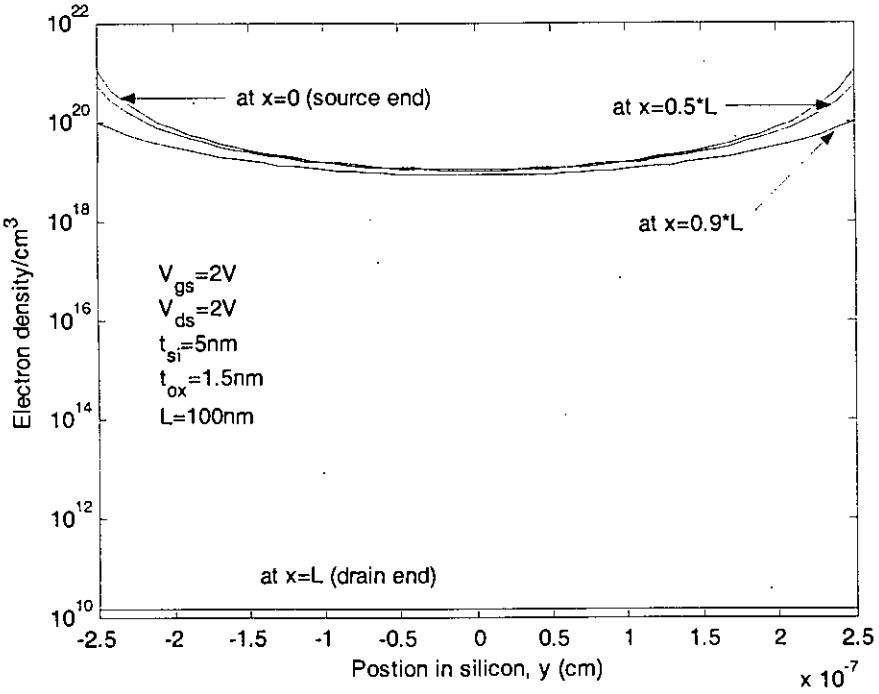

Figure 4.9 Electron density as a function of position in the silicon film at different positions along the channel.

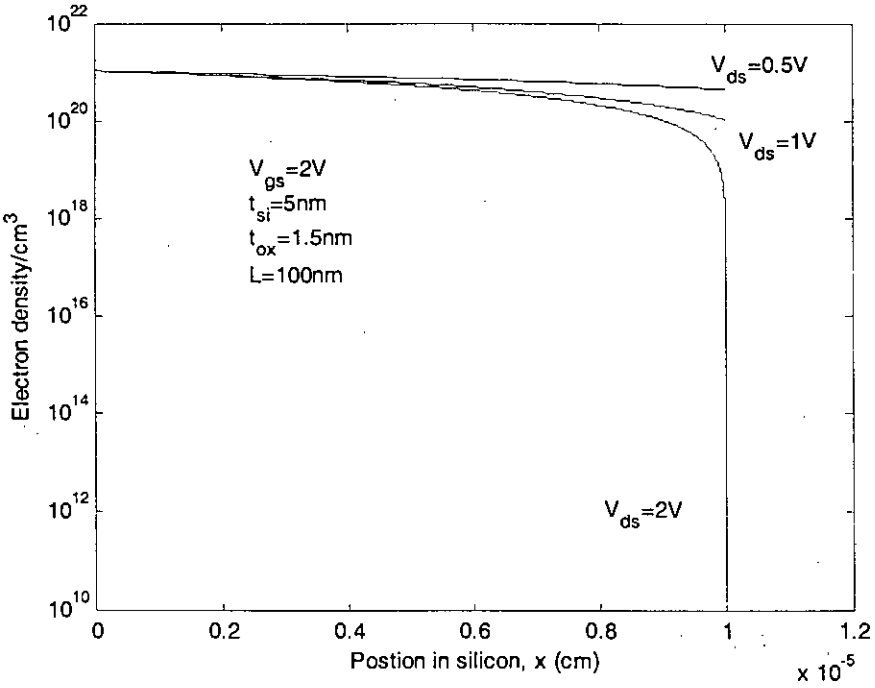

Figure 4.10 Electron density as a function of position along the channel at different drain voltage.

4.6 Effect of drain voltage on volume inversion

Figure 4.11 shows surface potential ψ_s and potential at the center of the channel, ψ_0 versus gate voltage for different drain voltage. It is found that at the drain end the channel remains at volume inversion at higher gate voltage if drain voltage is high. It is observed from the figure that, ψ_s and ψ_0 are decoupled when $V_{gs}>(V_{ds}+V_t)$. Figure 4.12 shows the sheet density of mobile charge, Q_i as a function of gate voltage for three values of drain voltages. It is found that mobile charge sheet density decreases with drain voltage. Comparing figure 4.11 and 4.12 we notice that at the drain end threshold voltage

increases with V_{ds} and when $V_{gs}>(V_{ds}+V_t)$ with $V_t=0.4V$, drain end charge density increases exponentially.

Figure 4.13 shows the electric potential ψ, along the gate to gate direction for two values of drain voltage. It is found that if V_{ds} is increased from 0 to 0.5 volts potential profile at the drain end becomes flat at the same gate voltage and the drain end goes to volume inversion condition. That is to achieve strong inversion at the drain end higher gate voltage will be required. From figure 4.11 and 4.12 it is found that the required gate voltage should be greater than 0.9V.

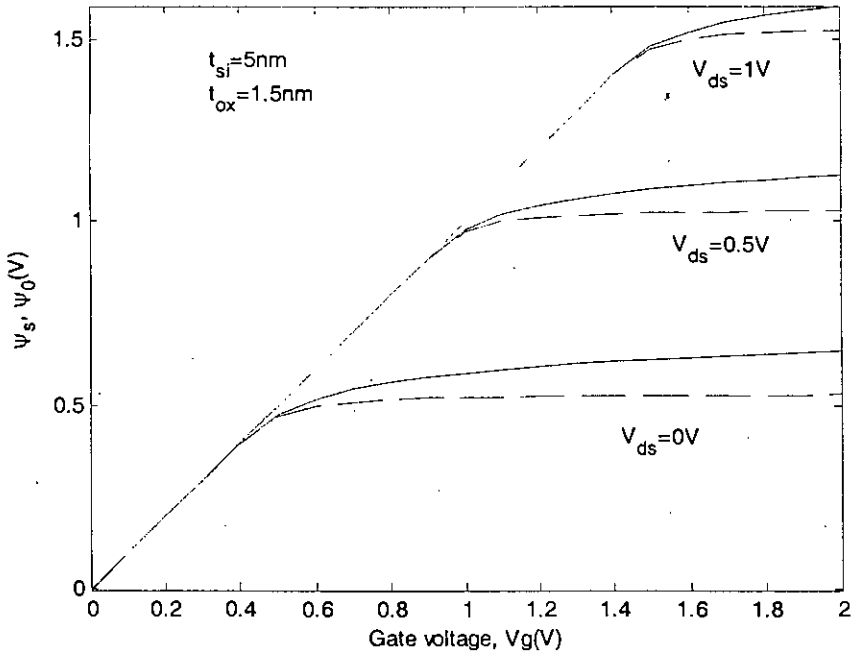

Figure 4.11 Surface potential ψ_s (continuous lines) and potential at the center of the channel ψ_0 (broken lines) versus the gate voltage.

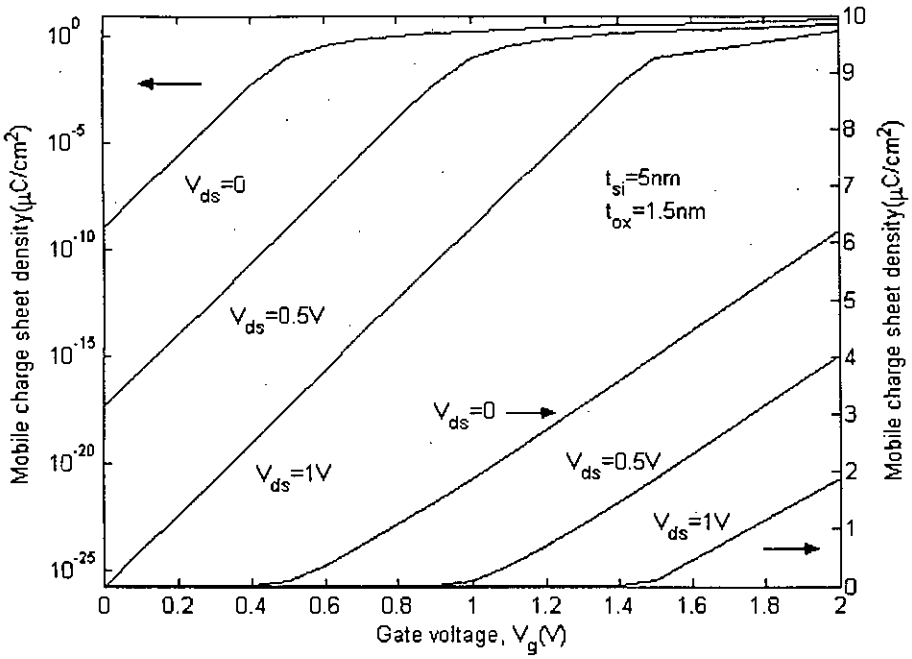

Figure 4.12 Sheet density of mobile charge as a function of gate voltage for three values of drain voltages in both logarithmic (left) and linear (right) scales.

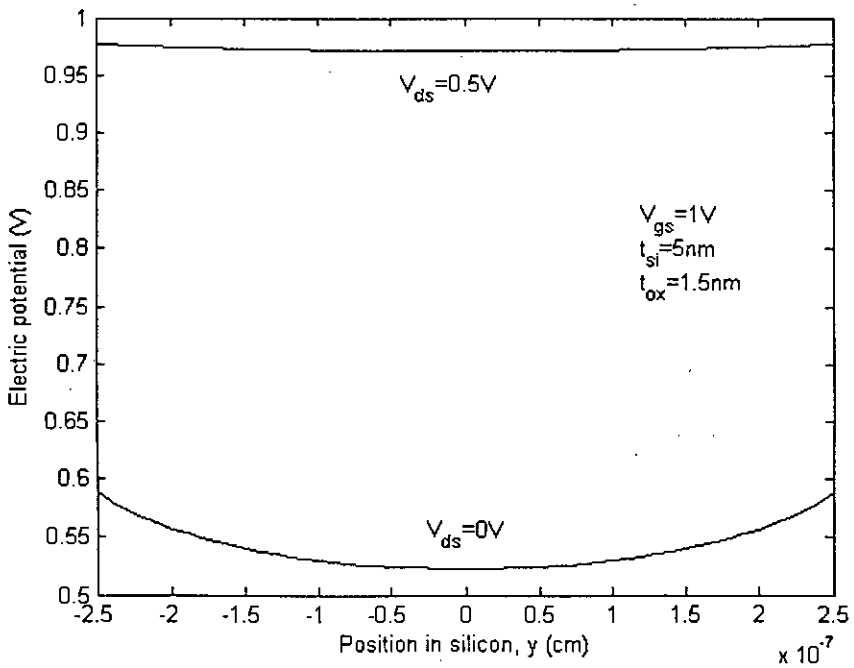

Figure 4.13 Potential ψ as a function of position in the silicon film for two values of drain voltages.

4.7 Potential variation along the channel

Figure 4.14 shows the variation of surface potential ψ_s along the channel (from source to drain) at different drain voltages. At lower V_{ds} the variation is almost linear. When V_{ds} is greater than $1.5V$ the surface potential profile does not change. This is illustrated in the following discussion. Figure 4.15 shows the surface potential ψ_s at the drain end as a function of drain voltage for a given V_g. For a given gate voltage surface potential flattens out after a certain drain voltage as shown in the figure. At this drain voltage the channel goes to weak inversion (volume inversion). Further increase in drain voltage causes depletion of charge similar to single gate MOSFET [39]. Form figure 4.11 we notice that for a certain gate voltage drain end surface potential will not increase with drain voltage as the channel remains in volume inversion condition. The figure 4.14 shows the potential profile corresponding to the linear region of I-V characteristics. In the saturation region the potential profile will not change with V_{ds}.

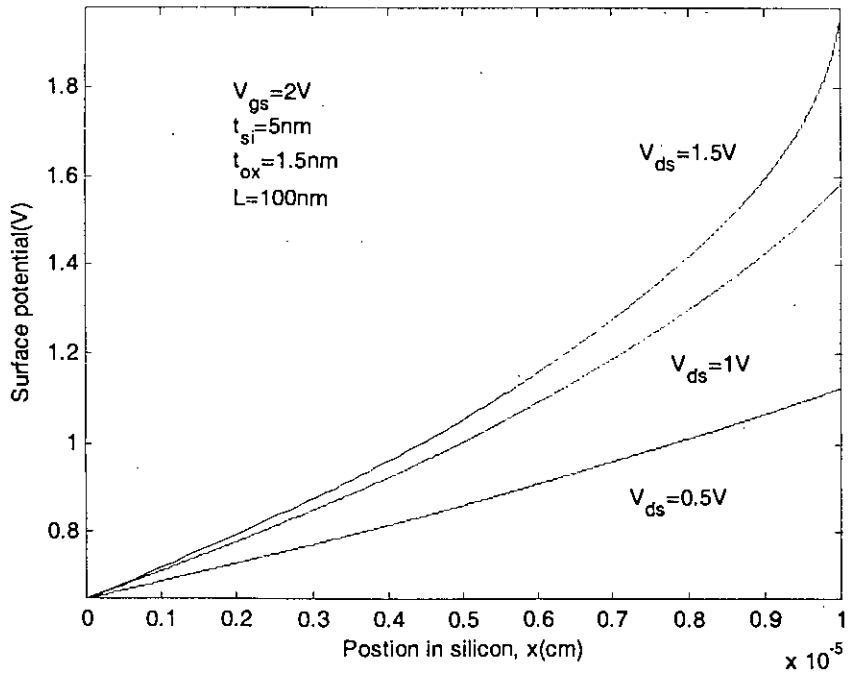

Figure 4.14 Variation of surface potential ψ_s along the channel (source to drain)

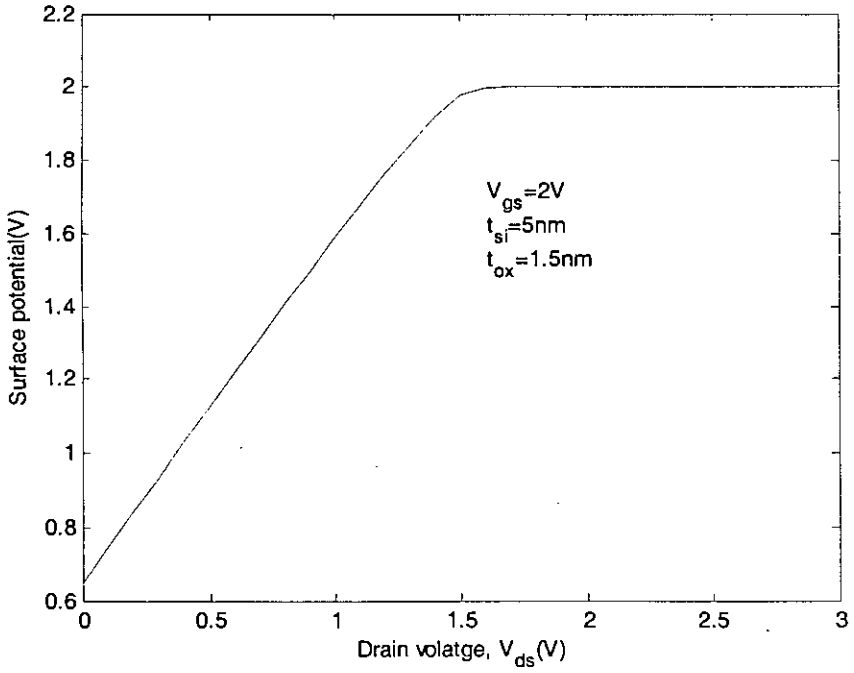

Figure 4.15 Surface potential ψ_s at the drain end as a function of drain voltage for a given V_g.

Figure 4.16 shows the variation of potential profile along the channel at different positions (y) inside the silicon film when $V_{ds} = 1.5V$. Figure 4.17 shows the same potential profile when $V_{ds} = 1V$. It is found that if we move further from the surface potential will decrease. Besides if drain voltage is reduced more reduction of potential from the surface. At high drain voltage potential inside the surface becomes equal to the surface potential at the drain end. That is at the drain end gate-to-gate potential variation will be flat which corresponds to volume inversion condition.

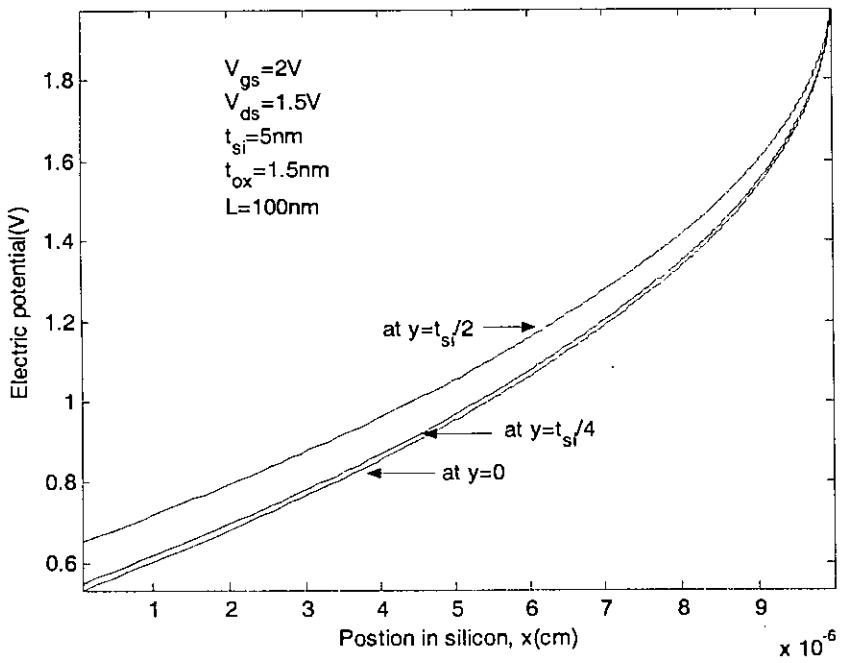

Figure 4.16 Electric potential profile from source to drain at different depths of the silicon channel for $V_{ds} = 1.5V$.

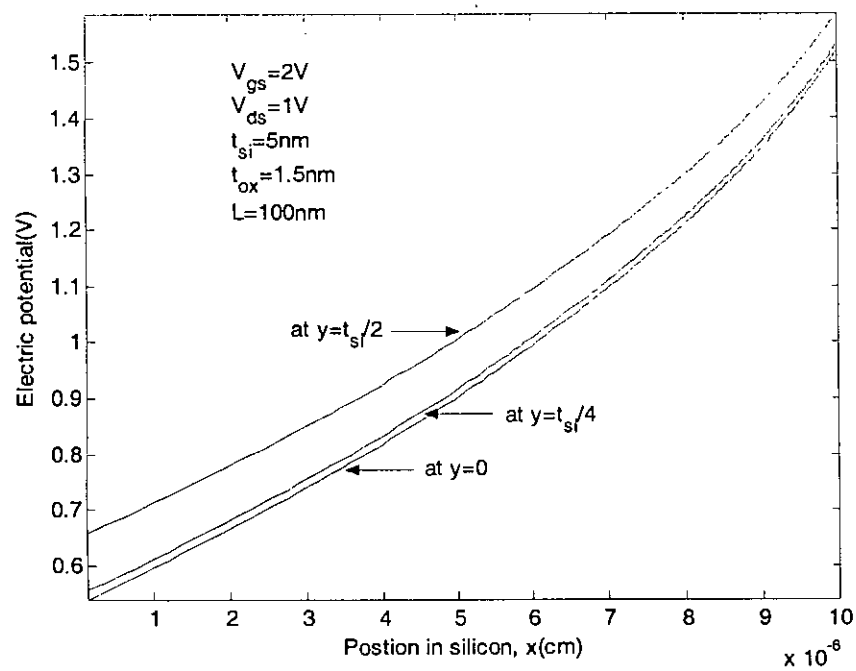

Figure 4.17 Electric potential profile from source to drain at different depths of the silicon channel for $V_{ds} = 1V$.

4.8 Electric field variation

Figure 4.18 shows the variation of electric field at the surface, E_s along the channel (from source to drain) at different drain voltages. Figure 4.19 shows the variation of electric field along the channel at different position (y) inside the silicon film when $V_{ds} = 1.5V$. Figure 4.20 shows the same variation when $V_{ds} = 1V$. At high drain voltage electric field variation inside the surface follows the surface electric field because of the nature of the potential profile. That is when drain voltage increases gate-to-gate electric field variation at the drain end becomes negligible which corresponds to volume inversion condition. Almost constant electric field along the channel is observed for values of V_{ds} below saturation. It is found that longitudinal field (x-directed field) inside the silicon is higher than the surface. Figure 4.21 shows the gate to gate field (transverse field) at the source and drain end. At the centre of the film transverse field (y-directed field) is zero. As drain end potential profile has little variation drain end transverse field is almost negligible compared to source end field.

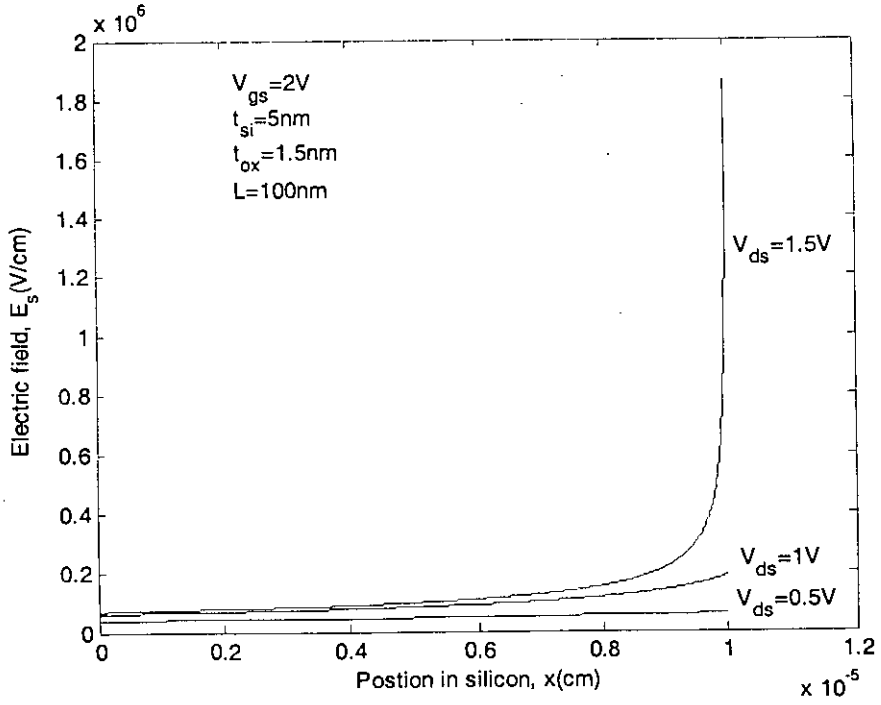

Figure 4.18 Variation of electric field at the surface, E_s along the channel (source to drain)

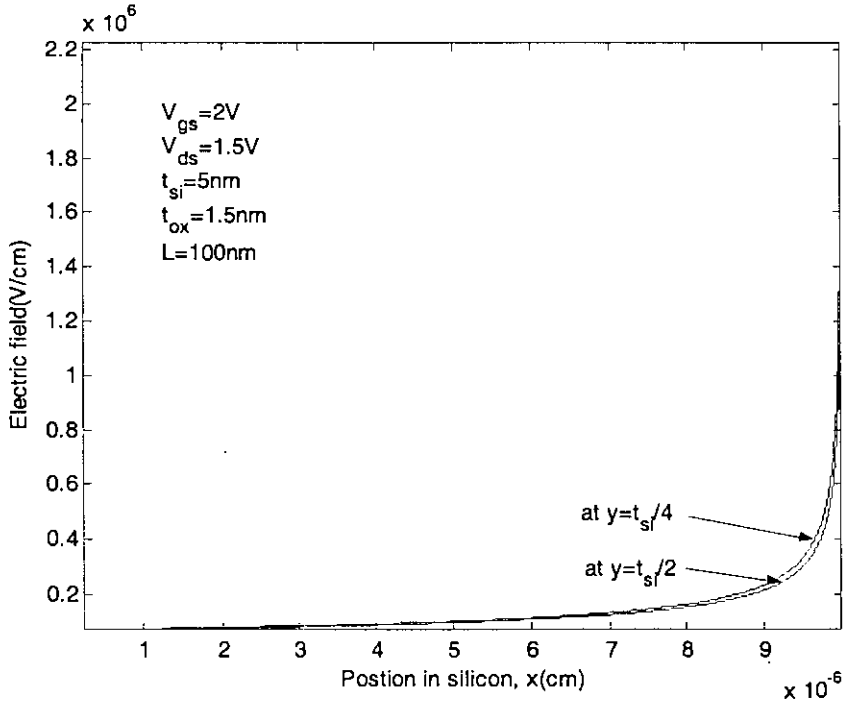

Figure 4.19 Electric field profile from source to drain at different depths of the silicon channel for $V_{ds} = 1.5V$.

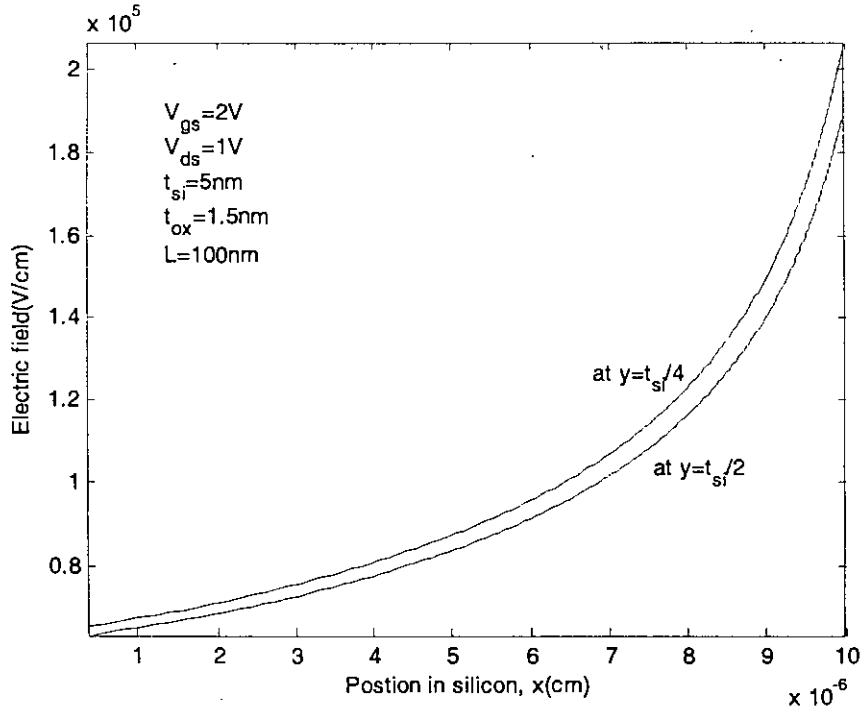

Figure 4.20 Electric field profile from source to drain at different depths of the silicon channel for $V_{ds} = 1V$.

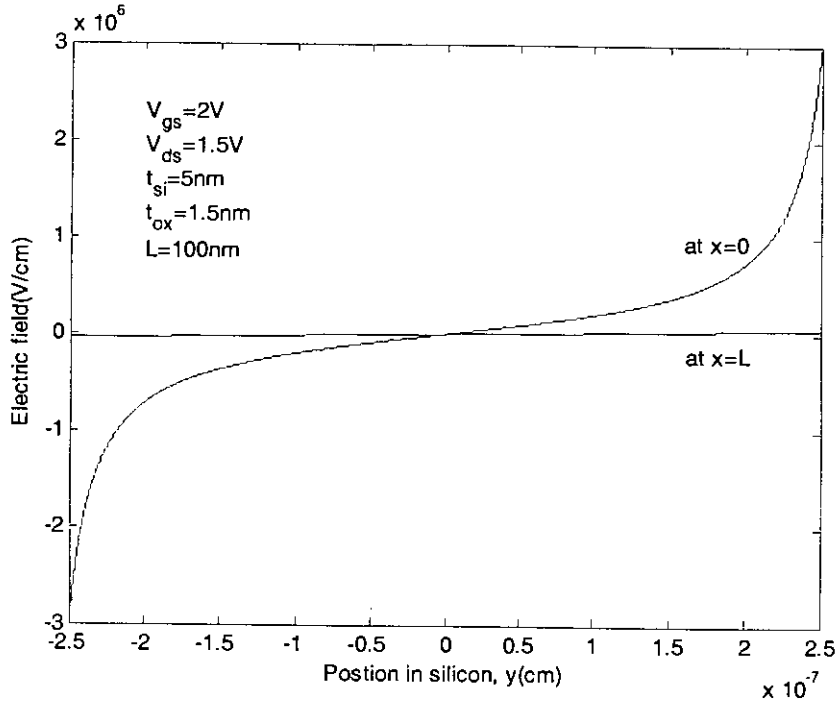

Figure 4.21 Gate to gate electric field profile at the source ($x=0$) and at the drain ($x=L$).

Figure 4.22 shows the channel length modulation (CLM) effect for $L=1\mu m$. From the electric field profile maximum electric field is obtained at different drain voltage. By choosing one of this electric field as critical electric field the pinchoff region length l_p is obtained from equation (10) (section 3.3) and the drain current I_{ds} is obtained from equation (6) with $L_{eff}=L-l_p$ at corresponding drain voltages. By choosing a lower electric field as critical field the same process is repeated until the drain current becomes almost equal to ideal current. At this critical field the effective channel length L_{eff} is almost equal to actual length L. Figure 4.23 shows the CLM effect for $L=100nm$. It is found that drain current increases due to reduced channel length and for a certain gate voltage this effect is higher for shorter channel. We also notice that for shorter channel CLM effect is observed at lower drain voltages.

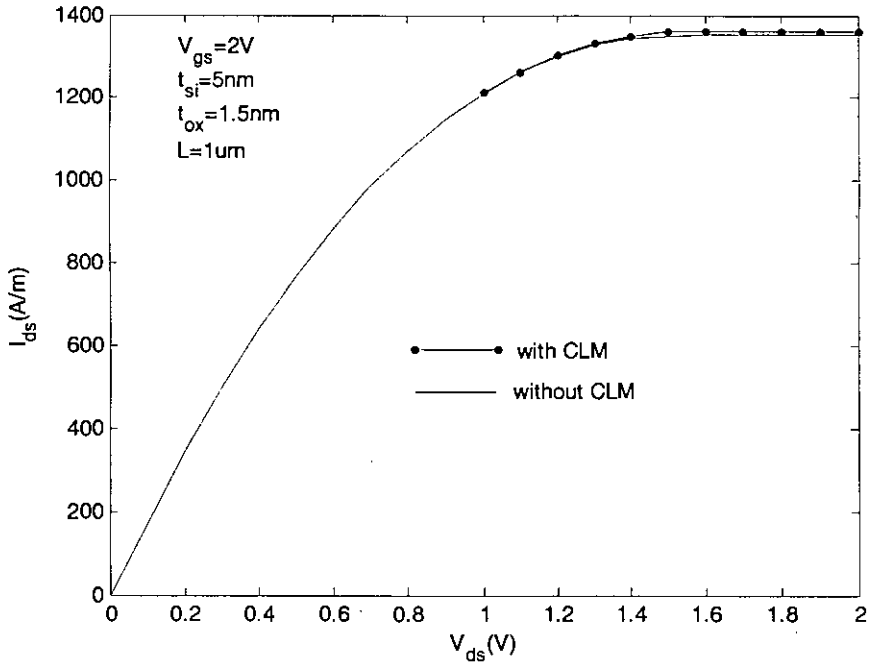

Figure 4.22 I_{ds}-V_{ds} curves with channel length modulation effect when $L = 1\mu m$.

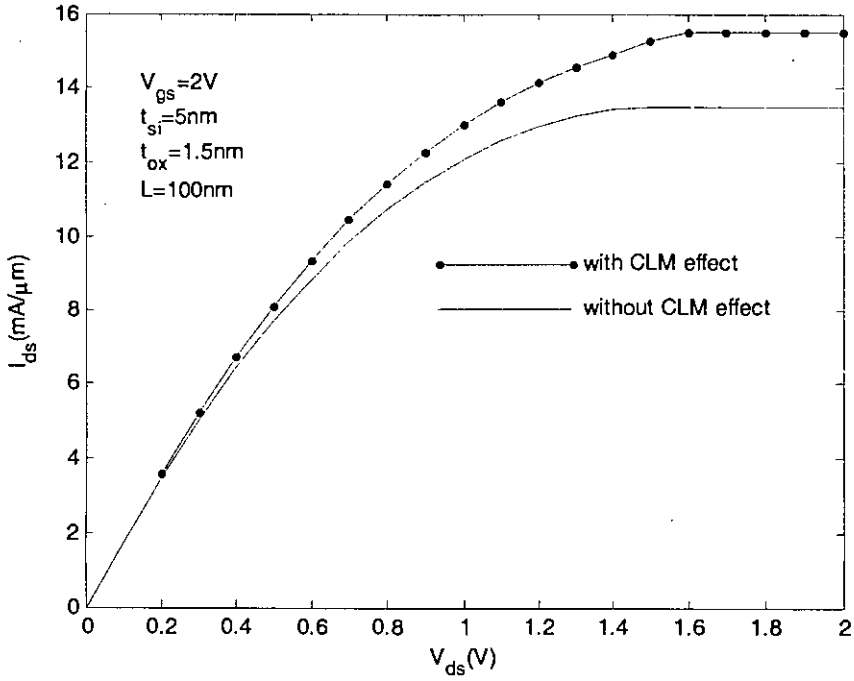

Figure 4.23 I_{ds}-V_{ds} curves with channel length modulation effect when $L = 100nm$.

4.9 Effect of oxide thickness

Figure 4.24 shows the sheet density of mobile charge as a function of gate voltage for two oxide thicknesses, assuming zero drain-to-source voltage. It is found that below threshold (V_g<0.4V) oxide thickness has little effect on sheet density of mobile charge and above threshold charge density decreases for thicker oxide. Figure 4.25 shows the sheet density of mobile charge as a function of drain voltage for two oxide thicknesses. We observe that in post pinchoff region (V_{ds}>0.6V) oxide thickness has no effect on sheet density of mobile chatge. Figure 4.26 shows the surface potential at the source end versus gate voltage for different gate oxide thicknesses. Higher the oxide thickness higher the voltage drops on the oxide and lower the surface potential.

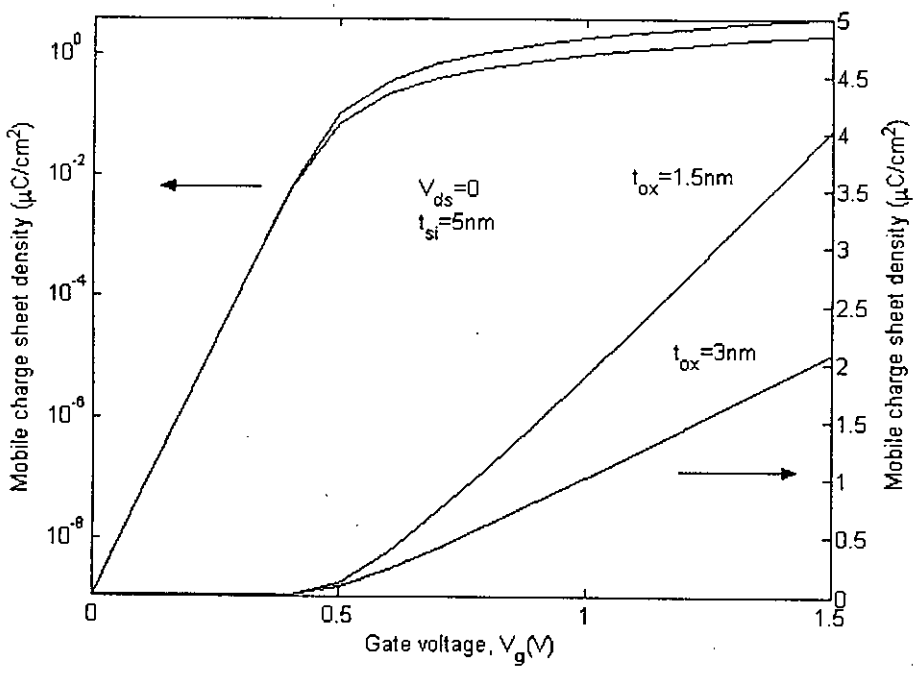

Figure 4.24 Sheet density of mobile charge at the source end as a function of gate voltage for two oxide thicknesses in both logarithmic (left) and linear (right) scales.

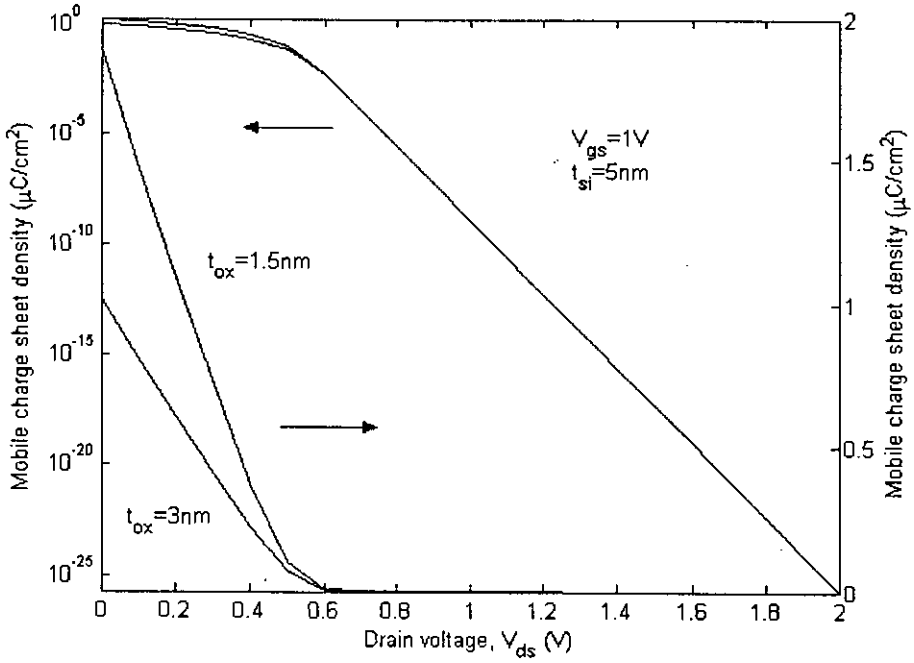

Figure 4.25 Sheet density of mobile charge as a function of drain voltage for two oxide thicknesses in both logarithmic (left) and linear (right) scales.

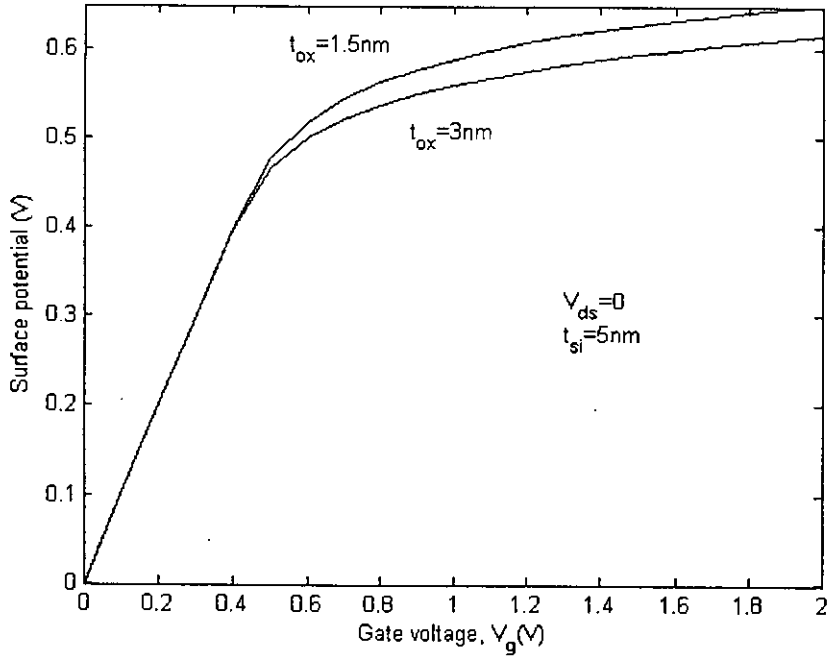

Figure 4.26 Surface potential, ψ_s as a function of gate voltage for two oxide thicknesses, assuming zero drain-to-source voltage.

4.10 Short channel effect

Obtained from equation (29) (section 3.4) figure 4.27 shows the threshold voltage rolloff (ΔV_{th}) as a function of channel length, assuming zero drain-to-source voltage. The threshold voltage rolloff at $V_{ds}=2V$ is shown in figure 4.28. Comparing figure 4.27 and 4.28, it is found that for a given channel length threshold voltage reduces due to drain induced barrier lowering.

Figure 4.29 shows the dependence of the threshold voltage of a long channel device on silicon film thickness as derived from equation (30). From equation (30) we notice that the threshold voltage is not a function of channel length. It is found that due to drain induced barrier lowering threshold voltage reduces for thicker channel.

Figure 4.30 shows dependence of the threshold voltage of a long channel device on silicon film thickness as derived from equation (29). Equation (29) is also a function of channel length. Comparing with figure 4.29 it is found that for silicon thickness greater than $20nm$ the threshold voltage for a channel length $L=1\mu m$ increases when $V_{ds}=2V$. But if t_{si} is less than $20nm$ the drain voltage has no effect on V_{th}.

Figure 4.31 shows silicon thickness versus channel length for different threshold rolloff with $V_{ds}=0$. It is found that for a certain threshold rolloff reduction of silicon thickness allows more reduction of channel length. We also notice that channel length can be reduced further if higher threshold rolloff is allowed.

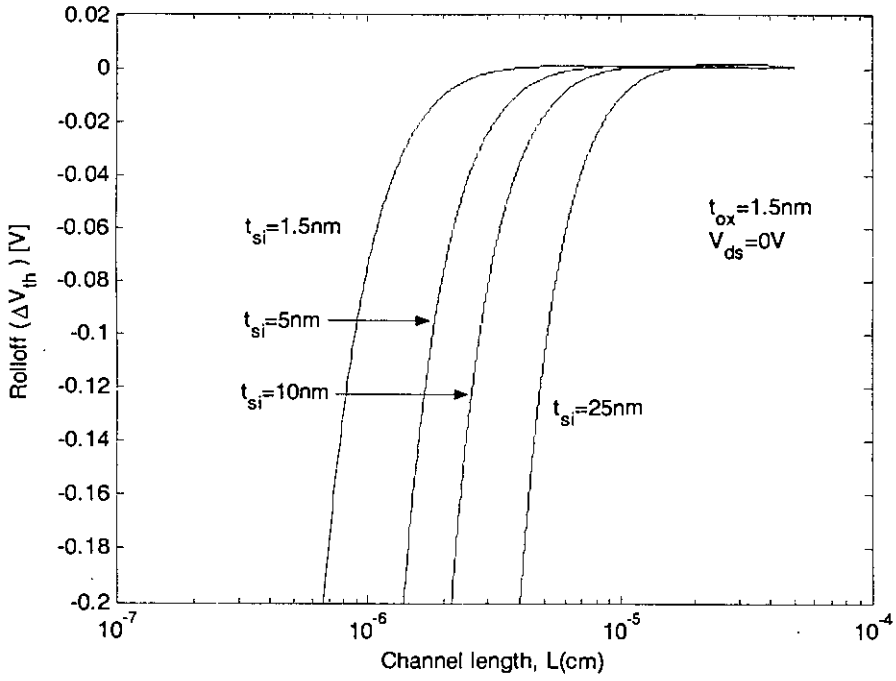

Figure 4.27 Threshold voltage rolloff as a function of channel length for different silicon thicknesses when $V_{ds}=0$.

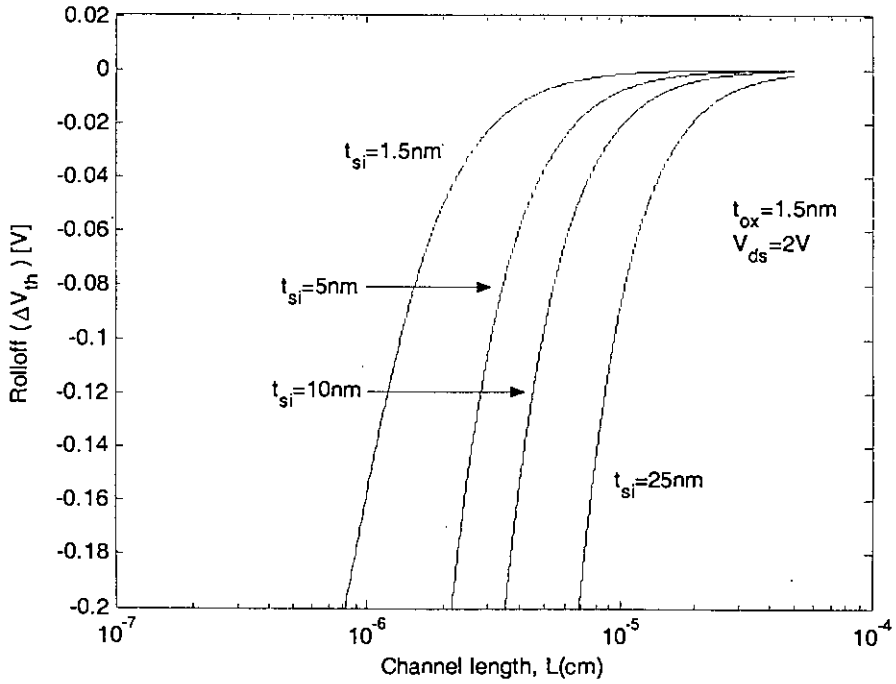

Figure 4.28 Threshold voltage rolloff as a function of channel length for different silicon thicknesses when $V_{ds}=2V$.

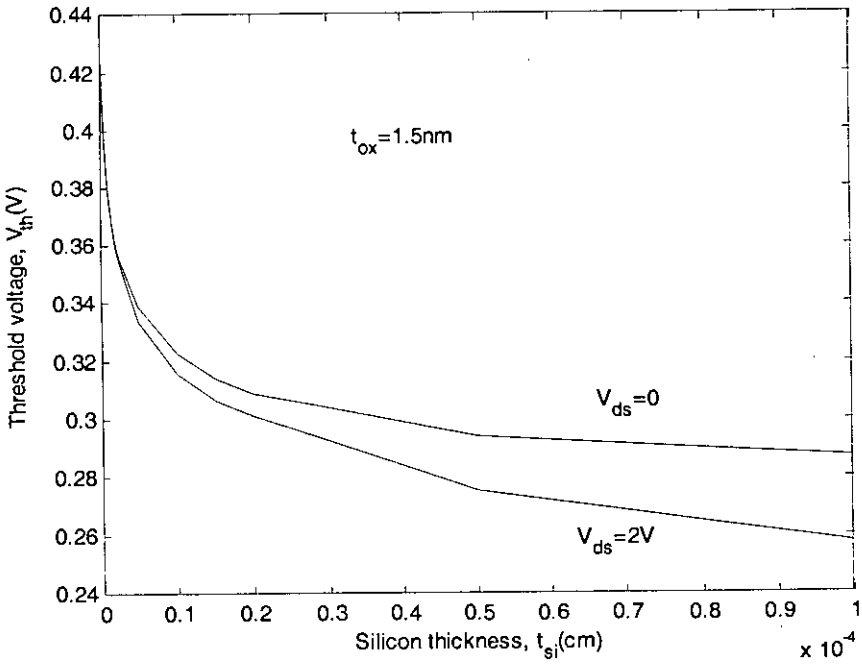

Figure 4.29 Threshold voltage of a long channel DGFET versus silicon film thickness.

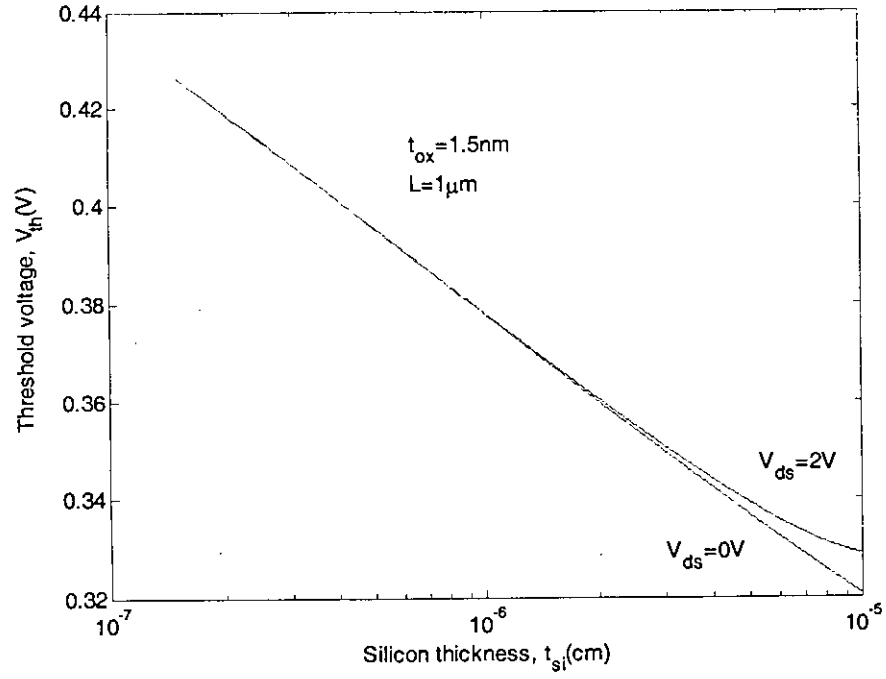

Figure 4.30: Threshold voltage of long channel DGFET versus silicon film thickness.

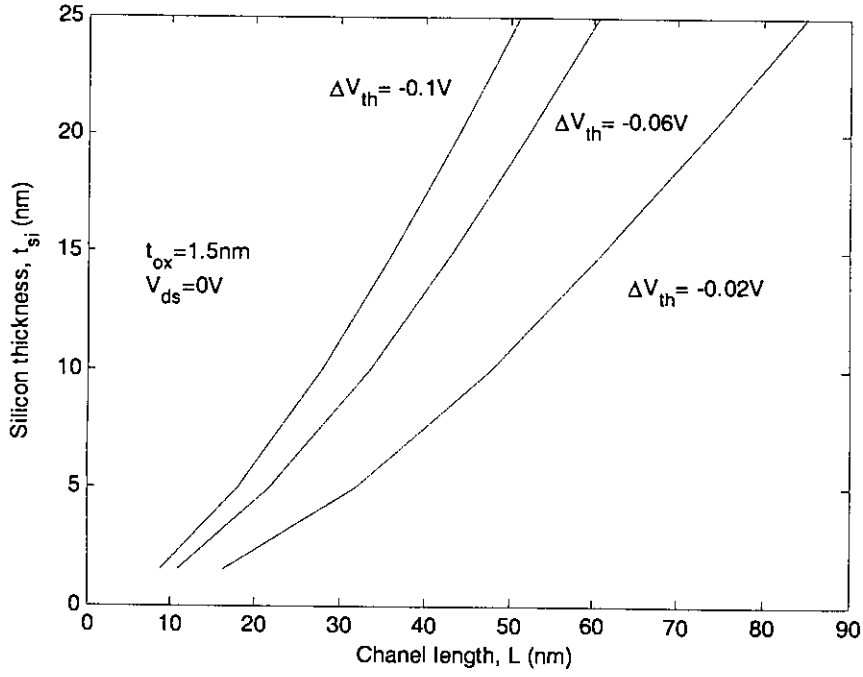

Figure 4.31 Silicon thickness versus channel length for different threshold rolloff.

4.11 Comparison of three types of DG MOSFET structure

The three types of double-gate (DG) MOSFET structure is shown in figure 4.32. For Planar DG MOSFET silicon thickness t_{si} can be achieved down to *5nm*. But for FinFET and Vertical DG MOSFET minimum value silicon thickness can be achieved is about *20nm*. Because for FinFET structure the gate oxide is on the etched sidewall of the fin and its uniformity is more difficult to control [40]. Similar case is for the Vertical structure imposes a limitation of silicon thickness. The I_d-V_{gs} curve for three types of DG MOSFET structure is shown in figure 4.33 with the channel length $L=100nm$ and the oxide thickness t_{ox} = *1.5nm* for each structure. It is found that threshold voltage for the FinFET and Vertical structures is higher than that for the Planar structure. Figure 4.34 shows the threshold voltage rolloff (ΔV_{th}) as a function of channel length for three types of DG structure. We notice that Planar structure shows less threshold rolloff than the Vertical and FinFET structure for the same channel length.

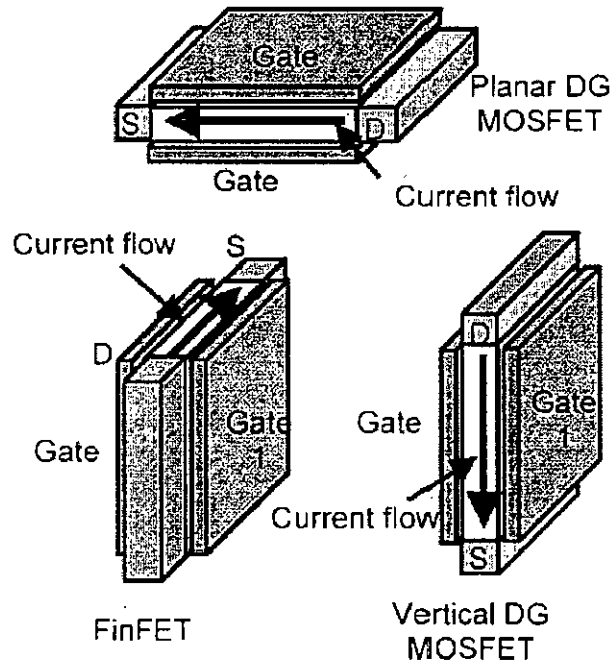

Figure 4.32 Planar, Vertical and FinFET Architectures.

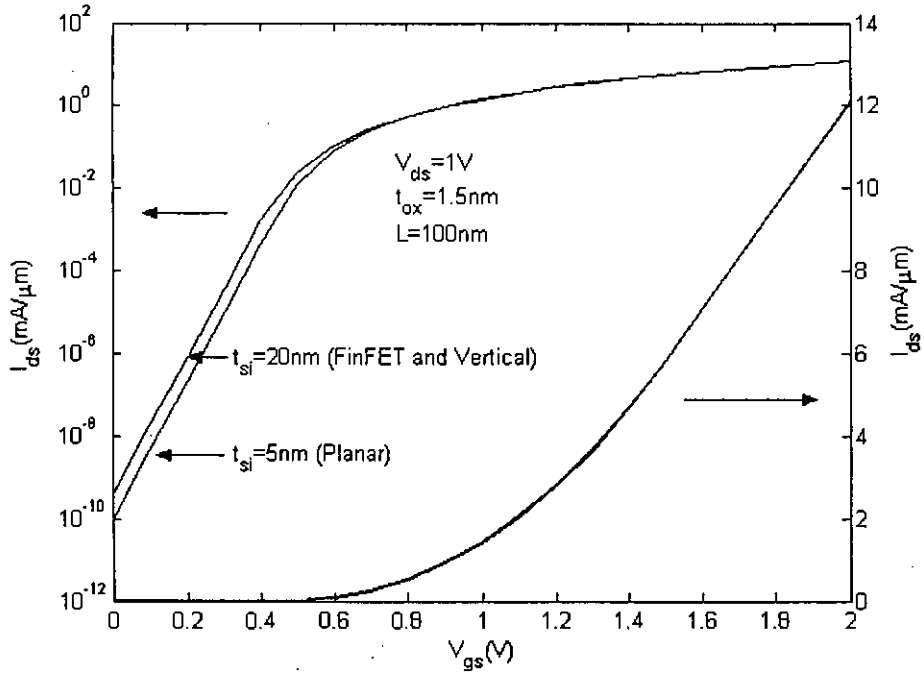

Figure 4.33 I_{ds}-V_g characteristics for Planar, Vertical and FinFET Architectures in both logarithmic (left) and linear (right) scales.

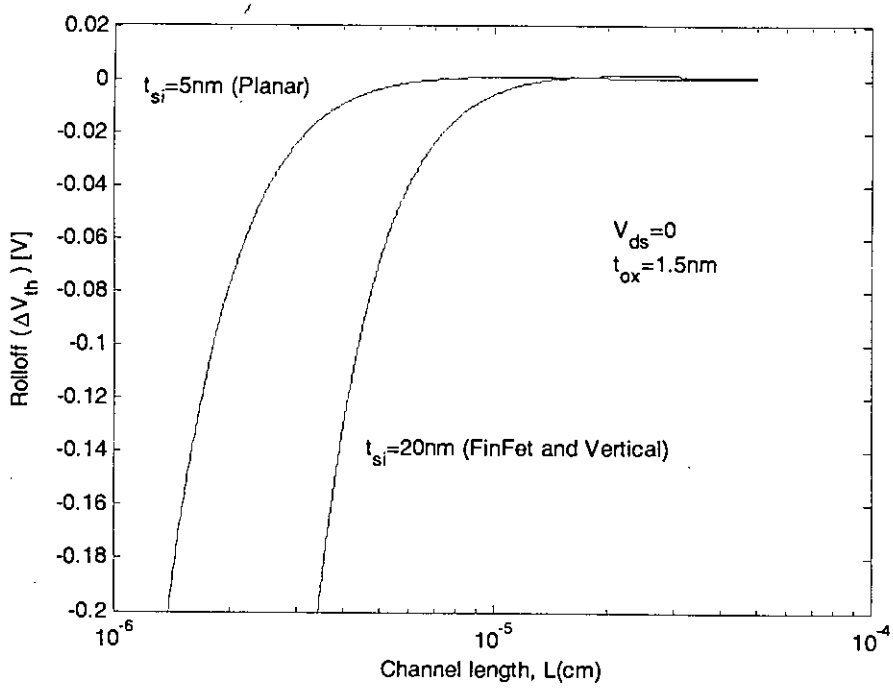

Figure 4.34 Threshold voltage rolloff as a function of channel length for Planar, Vertical and FinFET Architectures.

Chapter 5

Conclusion

5.1 Summary

A continuous *I–V* model is derived from analytic solutions of Poisson's and current continuity equation for long channel DG MOSFETs. No charge sheet approximation is invoked which is a key to the proper depiction of "volume inversion" in subthreshold condition. From the gate to gate (y-direction) potential profile it is found that for thicker silicon film the operation of the device is similar to the operation of two conventional MOSFETs connected in parallel and volume inversion does not occur. Form *I-V* characteristics it is found that subthreshold current increases for increased silicon thickness but the subthreshold slope remains almost the same. So film thickness has little effect on operating current of the device. The effect of drain voltage on volume inversion has also been studied. From the developed I-V model potential profile along the channel (x-direction) has been obtained. The potential profile inside the silicon channel has also been derived. From the potential profile electric field profile along the oxide-silicon interface, as well as that inside the silicon channel has been calculated. These profiles would give valuable information regarding field-constraints in designing sub 100nm devices.

Effects of the channel length on device performance have been analyzed through a quasi 2D analysis. The potential profile calculated through the gradual channel approximation has been used to solve the Poisson's equation along the channel length direction. The solution is then superimposed on a remnant 2D solution to achieve the two dimensional potential profile. The resulting expression of the threshold voltage incorporates the short channel effects. It has been shown that the effect of threshold voltage roll-off, observed in conventional MOSFETs for dimensions below 100nm, can be compensated in the DGFET structure through careful adjustment of the silicon thickness. Improvements in

performance of the DGFET structure in terms of current drivability, Short Channel Effect, Subthreshold Slope, etc. compared to conventional bulk MOSFET has been analyzed. Results obtained through our model are in agreement with published simulation results. The simplified model has been used to critically comment on device parameters of the different configurations of DGFET structures.

5.2 Possible future work

The DG MOSFET is the most promising candidate for CMOS scaling beyond 65nm technology node as strict I_{ON}/I_{OFF} ratios will require deviation from conventional bulk CMOS. In this work, the surface potential profile of a double-gate (DG) MOSFET has been obtained through a quasi 2D analysis. Exact 2D analysis will give more accurate result. We assume a linear variation of source to drain voltage along the channel. More accurate model of source to drain voltage variation can be developed. The analysis has been done assuming a symmetric double gate structure. Analysis can be done for asymmetric double gate MOSFETs.

For a complete analysis of the ultimate scaling limitations of DG MOSFETs down to $10nm$ gate lengths and below, quantum mechanical effects need to be considered. The electrons in the inversion layer are distributed in subbands and more band bending is required to populate the inversion layer, increasing V_t. Inversion layer quantization for body thickness less than $\sim 5nm$ causes a substantial threshold voltage shift that cannot be neglected.

APPENDIX I

Multiplying both sides by $2\frac{d\psi}{dy}$ equation (1) becomes [39]

$$2\frac{d\psi}{dy}\frac{d^2\psi}{dy^2} = 2\frac{d\psi}{dy}\frac{q}{\varepsilon_{si}} n_i e^{\frac{q(\psi - V)}{kT}} \qquad (31)$$

Integrating (31) once with the symmetry boundary condition $d\psi / dy\big|_{y=0} = 0$, one obtains

$$\frac{d\psi}{dy} = \sqrt{\frac{2qkT\, n_i}{\varepsilon_{si}}\left(e^{\frac{q(\psi - V)}{kT}} - e^{\frac{q(\psi_0 - V)}{kT}}\right)} \qquad (32)$$

for $0 \le y \le t_{si}/2$. Here $\psi_0 \equiv \psi(y = 0)$ is the potential at the center of the silicon film.

Rearranging equation (32) one obtains

$$\frac{d\psi}{\sqrt{\left(e^{\frac{q(\psi - V)}{kT}} - e^{\frac{q(\psi_0 - V)}{kT}}\right)}} = \sqrt{\frac{2kT\, n_i}{\varepsilon_{si}}}dy \qquad (33)$$

Let $e^{\frac{q(\psi - V)}{kT}} - e^{\frac{q(\psi_0 - V)}{kT}} = u^2$. So $d\psi = \frac{kT}{q}\frac{2udu}{u^2 + e^{\frac{q(\psi_0 - V)}{kT}}}$ and putting this in equation (33) and rearranging results

$$\frac{du}{u^2 + e^{\frac{q(\psi_0 - V)}{kT}}} = \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}}dy \qquad (34)$$

Integration of equation (34) results

$$u = e^{\frac{q(\psi_0 - V)}{2kT}} \tan\left(e^{\frac{q(\psi_0 - V)}{2kT}} \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}} y \right)$$

$$\text{or, } \sqrt{\left(e^{\frac{q(\psi - V)}{kT}} - e^{\frac{q(\psi_0 - V)}{kT}} \right)} = e^{\frac{q(\psi_0 - V)}{2kT}} \tan\left(e^{\frac{q(\psi_0 - V)}{2kT}} \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}} y \right)$$

$$\text{or, } e^{\frac{q(\psi - \psi_0)}{2kT}} = 1 + \tan^2\left(e^{\frac{q(\psi_0 - V)}{2kT}} \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}} y \right)$$

Finally one obtains

$$\psi(y) = \psi_0 - \frac{2kT}{q} \ln\left[\cos\left(e^{\frac{q(\psi_0 - V)}{2kT}} \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}} y \right) \right] \qquad (35)$$

Now let $\beta = e^{\frac{q(\psi_0 - V)}{2kT}} \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}} \frac{t_{si}}{2}$. So $\psi_0 = V - \frac{2kT}{q} \ln\left(\frac{t_{si}}{2\beta} \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}} \right)$ and putting this in equation (35) and rearranging one obtains equation (2).

APPENDIX II

Let $\psi_0 - V = \phi$ and assuming $V=V_{ds}(x/L)$ equation (14) becomes

$$\frac{d^2\phi}{dx^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{q}{kT}\phi} \qquad (36)$$

with boundary conditions

$$\phi(0) = V_{bi} \qquad (37)$$

$$\phi(L) = V_{bi} \qquad (38)$$

Multiplying both sides by $2\frac{d\phi}{dx}$ equation (36) becomes

$$2\frac{d\phi}{dx}\frac{d^2\phi}{dx^2} = 2\frac{d\phi}{dx}\frac{q}{\varepsilon_{si}} n_i e^{\frac{q}{kT}\phi} \qquad (39)$$

Integrating (39) once with the symmetry boundary condition $d\phi/dx\big|_{x=0} = 0$, one obtains

$$\frac{d\phi}{dx} = \sqrt{\frac{2kT\, n_i}{\varepsilon_{si}}\left(e^{\frac{q}{kT}\phi} - e^{\frac{q}{kT}V_{bi}}\right) + C_1} \qquad (40)$$

Here $\phi(x=0) \equiv V_{bi}$ is the built-in voltage and C_1 is the integration constant.

Rearrangement of equation (40) results

$$\frac{d\phi}{\sqrt{\left(e^{\frac{q}{kT}\phi} - e^{\frac{q}{kT}V_{bi}} + C_2\right)}} = \sqrt{\frac{2kT\, n_i}{\varepsilon_{si}}}dx \qquad (41)$$

Here $C_2 = C_1 \frac{\varepsilon_{si}}{2kTn_i}$. Let $e^{\frac{q}{kT}\phi} - e^{\frac{q}{kT}V_{bi}} + C_2 = u^2$. So $d\phi = \frac{2kTudu}{q\, e^{\frac{q}{kT}\phi}}$ and putting this in equation (41) and rearrangement results

$$\frac{du}{u^2 + e^{\frac{q}{kT}V_{bi}} - C_2} = \frac{1}{\lambda_D} dx \qquad (42)$$

where λ_D is given as $\lambda_D = \sqrt{2kT\varepsilon_{si}/q^2 n_i}$ and can be called intrinsic Debye length. Integrating (42) one obtains

$$\frac{1}{\sqrt{e^{\frac{q}{kT}V_{bi}} - C_2}} \tan^{-1}\left(\frac{u}{\sqrt{e^{\frac{q}{kT}V_{bi}} - C_2}}\right) = \frac{x}{\lambda_D} + C_3$$

$$\text{or, } \sqrt{\frac{e^{\frac{q}{kT}\phi} - e^{\frac{q}{kT}V_{bi}} + C_2}{e^{\frac{q}{kT}V_{bi}} - C_2}} = \tan\left[\sqrt{e^{\frac{q}{kT}V_{bi}} - C_2}\left(\frac{x}{\lambda_D} + C_3\right)\right]$$

$$\text{or, } \frac{e^{\frac{q}{kT}\phi}}{e^{\frac{q}{kT}V_{bi}} - C_2} = \sec^2\left[\sqrt{e^{\frac{q}{kT}V_{bi}} - C_2}\left(\frac{x}{\lambda_D} + C_3\right)\right] \qquad (43)$$

Applying boundary conditions (37) and (38) to equation (43) results

$$C_2 e^{-\frac{q}{kT}V_{bi}} = \sin^2\left[C_3\sqrt{e^{\frac{q}{kT}V_{bi}} - C_2}\right] \qquad (44)$$

$$C_2 e^{-\frac{q}{kT}V_{bi}} = \sin^2\left[\left(\frac{L}{\lambda_D} + C_3\right)\sqrt{e^{\frac{q}{kT}V_{bi}} - C_2}\right] \qquad (45)$$

From equation (44) and (45) one obtains

$$\sin\left[\left(\frac{L}{\lambda_D}+2C_3\right)\sqrt{e^{\frac{q}{kT}V_{bi}}-C_2}\right]\sin\left[\frac{L}{\lambda_D}\sqrt{e^{\frac{q}{kT}V_{bi}}-C_2}\right]=0 \qquad (46)$$

With $C_3=\frac{L}{2\lambda_D}$ and $C_2=e^{\frac{q}{kT}V_{bi}}-\left(\frac{\pi}{\frac{L}{\lambda_D}+2e^{-\frac{qV_{bi}}{2kT}}}\right)^2$ equation (43) becomes

$$\varphi(x)=V_{bi}-\frac{2kT}{q}\ln\frac{2+e^{\frac{qV_{bi}}{2kT}}\frac{L}{\lambda_D}}{\pi}+\frac{kT}{q}\ln\left\{\sec^2\left[B\left(\frac{x}{L}-\frac{1}{2}\right)\right]\right\} \qquad (47)$$

Where $B=\frac{\pi}{1+2e^{\frac{-qV_{bi}}{2kT}}\frac{\lambda_D}{L}}$ and putting relation of ϕ and V in equation (47) one obtains equation (21)

By plugging in the solution (21) of the 1-D Poisson equation, (17) becomes

$$\frac{\partial^2\psi_1}{\partial x^2}+\frac{\partial^2\psi_1}{\partial y^2}=\frac{2kTB^2}{qL^2}\sec^2\left[B\left(\frac{x}{L}-\frac{1}{2}\right)\right]\left[e^{\frac{q}{kT}\psi_1(x,y)}-1\right] \qquad (48)$$

Recalling that $\psi(x,y)$, the sum of $\psi_0(x)$ and $\psi_1(x,y)$, has weak functional dependence in y-direction and the majority of its change in x-direction has been captured by the function $\psi_0(x)$, $\psi_1(x,y)$ thus can be expected to be of small magnitude. Retaining the lowest-order term only in the Taylor expansion of $e^{\frac{q}{kT}\psi_1(x,y)}$, (48) is approximated as

$$\frac{\partial^2\psi_1}{\partial x^2}+\frac{\partial^2\psi_1}{\partial y^2}=\frac{2B^2}{L^2}\sec^2\left[B\left(\frac{x}{L}-\frac{1}{2}\right)\right]\psi_1(x,y) \qquad (49)$$

Equation (49) is then solved by separation of variables, i.e., to seek $\psi_1(x,y)$ in the form of

$$\psi_1(x,y) = G(x)H(y) \qquad (50)$$

Substituting (50) into (49) yields

$$\frac{G''(x)}{G(x)} + \frac{H''(y)}{H(y)} = \frac{2B^2}{L^2}\sec^2\left[B\left(\frac{x}{L} - \frac{1}{2}\right)\right] \qquad (51)$$

which can be separated as

$$\frac{H''(y)}{H(y)} = \rho^2 \qquad (52)$$

$$\frac{G''(x)}{G(x)} = -\rho^2 + \frac{2B^2}{L^2}\sec^2\left[B\left(\frac{x}{L} - \frac{1}{2}\right)\right] \qquad (53)$$

where ρ is the separation constant (i.e., eigenvalue).

The (52) can be solved as

$$H(y) = C_1\cosh(\rho y) \qquad (54)$$

Here C_1 is a constant. From equation (50)

$$\psi_1(x,y) = C_1 G(x)\cosh(\rho y) \qquad (55)$$

Using boundary condition given by equation (20) one obtains

$$\varepsilon_{ox}\frac{V_{GS} - \Phi_{MS} - C_1 G(x)\cosh\left(\rho\frac{t_{si}}{2}\right) - \psi_0(x)}{t_{ox}} = \varepsilon_{si} C_1 G(x)\sinh\left(\rho\frac{t_{si}}{2}\right) \qquad (56)$$

Rearrangement of equation (56) results

$$G(x) = \frac{1}{C_1} \frac{V_{GS} - \Phi_{MS} - \psi_0(x)}{\cosh\left(\rho \frac{t_{si}}{2}\right) + \frac{t_{si}\rho}{\gamma} \sinh\left(\rho \frac{t_{si}}{2}\right)} \tag{57}$$

Here $\gamma = \varepsilon_{ox} t_{si} / \varepsilon_{si} t_{ox}$ and comparing (53) and (57) $\rho = \frac{2B}{L}$. So from (55)

$$\psi_1(x,y) = \frac{V_{GS} - \Phi_{MS} - \psi_0(x)}{\eta} \frac{\cos\left[2\theta\left(\frac{y}{t_{si}}\right)\right]}{\cosh\theta} \tag{56}$$

where $\theta = (Bt_{si}/L)$ and $\eta = 1 + (2\theta/\gamma)\tanh\theta$.

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