Analytical Modeling of Current-Voltage Characteristics of Ferroelectric Tunneling Field Effect Transistor

A thesis submitted in partial fulfillment of the requirement of the degree

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Master of Science in Electrical and Electronic Engineering

by

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DECLARATION

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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ABSTRACT

In this work a modified structure of Tunneling Field Effect Transistor (TFET) has been proposed incorporating Ferroelectric oxide as the gate oxide, called the Ferroelectric Tunneling FET (Fe-TFET). The TFET device is one of the novel devices for a low-power digital application due to their band to band tunneling mechanism and it exhibits a very small leakage current, high drive current and lower subthreshold slope. Fe-FET is also introduced by integrating ferroelectric material operating in the negative capacitance region that acts as a step-up transformer of the surface potential in a traditional MOSFET structure to achieve a steeper subthreshold slope. The proposed device (Fe-TFET) effectively combines the mechanism of TFET and the theoretical concept of Fe-FET. A simple tentative analytical ON current model of the proposed device is also presented here. By using the double gate configuration of this newly modified device named Fe-TFET, it is feasible to achieve much lower SS and can get sufficiently high drive current at a very low operating voltage. Fe-TFET gives ON current as high as 0.02 A/μm for a gate voltage of 0.4V, according to the results yielded from the analytical model. Thus the I_{ON}/I_{OFF} ratio becomes ~ 10^8 which is greater than that of a MOSFET and also for traditional TFET. OFF current exponentially increases with the threshold voltage reduction. So, in order to limit OFF current while maintaining a satisfactory ON current the subthreshold slope has to go down. This work provides physics based reasoning behind the multiplicative improvement in the subthreshold slope for the proposed device which gives ~40mV/dec subthreshold slope. Finally it demonstrates that the device performance can be amended in accordance with the technology of different band gap materials like Si, GaAs, Ge and InAs and different Ferroelectric oxides like $BaTiO_3$ and $SrTiO_3$.

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List of Symbols

A	Area (m^2)
A_{kane}, B_{kane}	Parameter of Kane's Model
C	Constant
C_{inv}	Inversion Layer Capacitance (F/m)
D	Material Dependent Parameter of Kane's Model
$\|E\|$	Electric Field (V)
$\bar{E}_{ext}$	External Electric Field
E_g	Band Gap Energy (eV)
$E_y(avg)$	Average Electric Field
G_{B2B}	Band to band generation rate
I	Band to band tunneling current (A or A/μm)
I_{ON}	On-current (A or A/μm)
I_{OFF}	Off-current (A or A/μm)
k	Boltzmann constant (eV/K)
l_1, l_2	Length (m)
L_g	Gate Length (m)
l_{tpath}	Tunneling Path (m)
m_{eff}	Carrier Effective Mass (kg)
N_a	Hole Doping Concentration (m^{-3})
P	Polarization charge per unit area (Cm^{-3})
Q	Charge (C)
q	Magnitude of the Electronic Charge (C)
R, S	Variable Parameter
SS	Subthreshold Slope (mV/decade)
t_{ox}	Oxide thickness (m)
U	Gibbs free energy
V_D	Supply Voltage (V)
V_{FB}	Flat Band Voltage (V)
V_g	Gate Voltage (V)
V_{ox}	Oxide Voltage (V)

V_{onset}	Onset Voltage (V)
W	Wide Silicon Body (m)
X, Y, Z	Modified Anisotropy Constant
ψ	Surface potential (V)
ψ_v	Valance Band Potential (V)
ψ_c	Conduction Band Potential (V)
$\delta\psi$	Perturbation of the electrostatic potential (V)
ρ	Volume Charge Density
ϵ_s	Permittivity of the Semiconductor
ϵ_{si}	Dielectric Constant of Silicon
α, β, γ	Anisotropy Constant
$\hbar$	Reduced Plank Constant
σ	Ferroelectric dependent parameter

Dedicated

to

My Parents

CHAPTER 1
Introduction

1.1 Preface

The foremost constraint of the conventional MOSFET is that the subthreshold slope (SS) cannot be reduced below 60mV/decade at room temperature due to the theoretical limitation of $ln(10)kT/q$ which is known as Boltzmann tyranny [1]. Besides, the down-scaling of conventional MOSFETs has led to higher static power consumption and exhibits short-channel effects and gate leakages. In addition high SS and thus high operating voltage make power consumption a rising challenge.

Several FET devices have been introduced to overcome these limit. The tunneling FET device is one of the novel devices for a low-power digital application due to their band to band tunneling mechanism [2-7] and it exhibits a very small leakage current, high drive current and SS <60mV/decade [8-10]. By using DG-TFET, we can achieve lower SS and also lower operating supply voltage compared to the conventional MOSFETs. So, they are considered to replace the conventional MOSFET at low operating voltages for low power digital applications. In DG-TFET, electrons move from the highly p doped source to moderately lighter n doped drain by drift diffusion. Here, the drain voltage has no influence in tunneling. Fe-FET is also introduced by integrating ferroelectric material operating in the negative capacitance region [11] that acts as a step-up transformer of the surface potential in a traditional MOSFET structure to achieve a steeper SS [12].

Here we proposed a modified structure of tunneling FET which combines the mechanism of TFET and the theoretical concept of Fe-FET. By using the double gate configuration and the replacement of the gate oxide by ferroelectric material like $BaTiO_3$ of this newly modified device named Fe-TFET, it is possible to achieve much lower SS and can get sufficiently high drive current at a very low operating voltage. Thus the I_{ON}/I_{OFF} ratio becomes greater than that of a MOSFET and also for traditional TFET [13]. Our proposed device shows the tunneling mechanism for the ON Current which use band to band tunneling in their ON-state and show a very small leakage current, in range of femto-amperes due to the large tunneling barrier formed when the device is turned off.

1.2 Literature Review

If the empirical Moore's law [14] holds forever, then by the year of 2025 the dissipative power density in a chip will be ~2MW/cm^2 [15] which is well above the maximum heat removal limit of 1000 W/cm^2 [16] from an IC by using conventional technology. To reduce the power hunger of IC the transistors should be designed such that it can turn on at a very low voltage having significantly low sub-threshold slope with high I_{ON}/I_{OFF} ratio. With the continued miniaturization of MOSFET from micro-meter to nano-meter regime the device geometry such as channel length, junction depth and oxide thickness has been reduced by about 3 orders of magnitude. To maintain a low power density, the power supply voltage V_{DD} should also go down with the scaling of device dimensions. But the mere reduction of the V_{DD} reduces the ON current I_{ON}, so to meet up the I_{ON} requirement the threshold voltage V_{TH} should be scaled with the scaling of the supply voltage. However, I_{OFF} exponentially increases with the threshold voltage reduction, since $I_{OFF} \propto 10^{-V_{TH}/SS}$. So, to limit I_{OFF} while maintaining a satisfactory I_{ON} the SS has to go down. However, for the conventional MOSFET structure the SS cannot be reduced below 60mv/decade at room temperature, even with infinite gate capacitance because a fundamental physical limit of surface potential change of $ln(10)kT$ is required to modulate the subthreshold current by one decade, which is known as Boltzmann Tyranny. In order to circumvent this limit a number of novel devices has recently been proposed to the literature such as Impact Ionization-MOSFET[17]-[19], FeedBack-FET [20], Nanoelectromechanical FET [21], Suspended Gate MOSFET [22], Tunneling FET [23-25], Fe-FET[26].

TFET is a gated reverse biased p-i-n diode which utilizes, unlike MOSFET that uses thermal carrier injection over the potential barrier, band to band tunneling as a source carrier injection mechanism. In the OFF state the tunnel barrier between the valance band of the source to the conduction band of the channel is so wide that effectively no tunneling occurs. But when the gate voltage exceeds the threshold voltage the tunneling barrier between the source and the channel is reduced enough to allow sufficiently high tunneling current. So by the exploitation of BTB tunneling mechanism TFET can supersede the fundamental SS limitation of conventional MOSFET. Zhang *et. al.* [27] theoretically showed that the Sub-threshold slope of TFET can be reduced below 60mv/dec. Choi et. al. [28] demonstrated 70nm n channel

TFET with SS 52.8mv/decade. Ref. [29] presented a vertical Si/SiGe with an SS of 44mv/decade by device simulation.

Salahuddin and Dutta [30] theoretically demonstrated that a ferroelectric material operating in the negative capacitance region could act as a step-up transformer of the surface potential in Metal–Oxide–Semiconductor structure, opening a new way for the realization of transistors with steeper subthreshold characteristics(S< 60 mV/decade) without changing the basic physics of the FET. Chen et. al. [31] demonstrated that with a proper choice of the ferroelectric insulator thickness, the hysteresis shape can be tailored for operating voltages below 0.5 V to obtain a steeper SS.

In this work, we proposed a theoretical framework of combining the aforementioned two techniques of obtaining steeper SS to beat the fundamental physical limit, thus garnering further reduction in SS value.

$$SS = \frac{dV_g}{dlog(I)} = \frac{dV_g}{d\psi}\frac{d\psi}{dlog(I)} = F_1F_2 \quad (1)$$

Here, ψ is the surface potential, F_1 is the variation gate voltage with respect to surface potential and F_2 is the variation of surface potential with respect to logarithmic term of drain current. By utilizing the band-to-band tunneling mechanism, TFET lowers the F_2 in eqn. (1) whereas Fe-FET utilizes negative capacitance to reduce the F_1 factor of eqn. (1).

1.3 Basic Structure of Tunneling FET

TFETs are gated p-i-n diodes. To switch the device on, the diode is reverse biased and a voltage is applied to the gate. In order to be consistent with MOSFET technology, the names of the device terminals are chosen such that voltages are applied in a similar way for TFET operation [32, 33]. Since a reverse bias is needed across the p-i-n structure in order to create tunneling and since an NMOS operates when positive voltages are applied to the drain and gate, the n-region of a TFET is referred to as its drain, and the p+ region as its source for an n-type device.

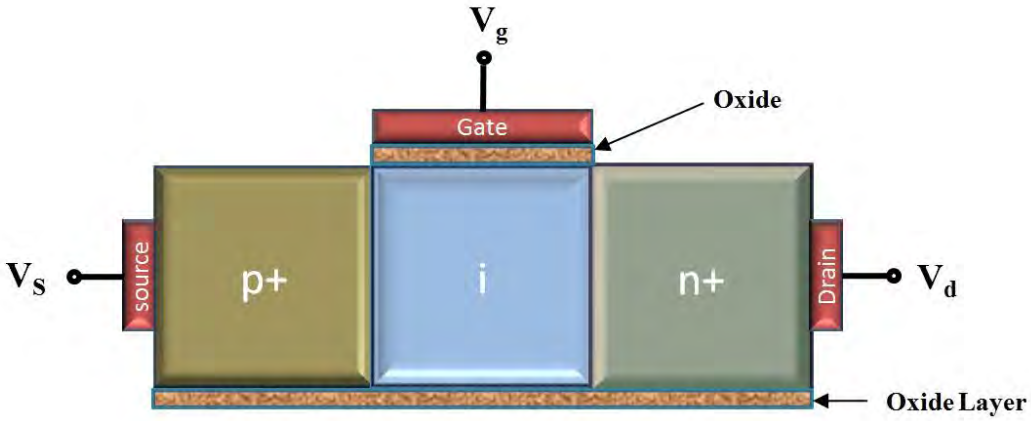


Figure 1.1: A simple TFET device structure, a p-i-n diode with one gate

Figure 1.1 shows the basic device structure for a typical p-i-n TFET. The structure shown is an n-type device with a p+ source and an n+ drain. In a p-type TFET, the source would be doped n+ and the drain would be doped p+.

1.4 TFET Characteristics

TFETs are promising devices to replace conventional MOSFETs for low-power applications. They offer the potential for a very low OFF-current and a small SS. TFETs are interesting as low-power devices because of their quantum tunneling barrier. When the devices are turned on, the carriers must tunnel through the barrier in order for current to flow from source to drain. When the devices are off, the presence of the barrier keeps the OFF-current extremely low, several orders of magnitude lower than the OFF-current of a conventional MOSFET.

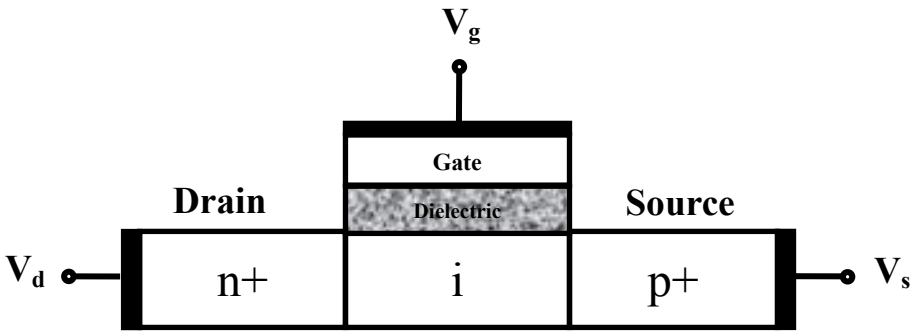


Figure 1.2: A simple TFET device structure, an n-i-p diode with one gate.

1.4.1 Band to Band tunneling

Tunneling is a quantum mechanical process where electrons move through potential energy barriers. Band-to-band tunneling is the effect when electrons travel from the valence band to the conduction band (or vice versa) through the forbidden energy band gap [34]. Understanding the nature of this band-to-band tunneling is important for understanding the approximations made in various simulation models. This understanding is also useful when optimizing design parameters of TFETs for maximum performance.

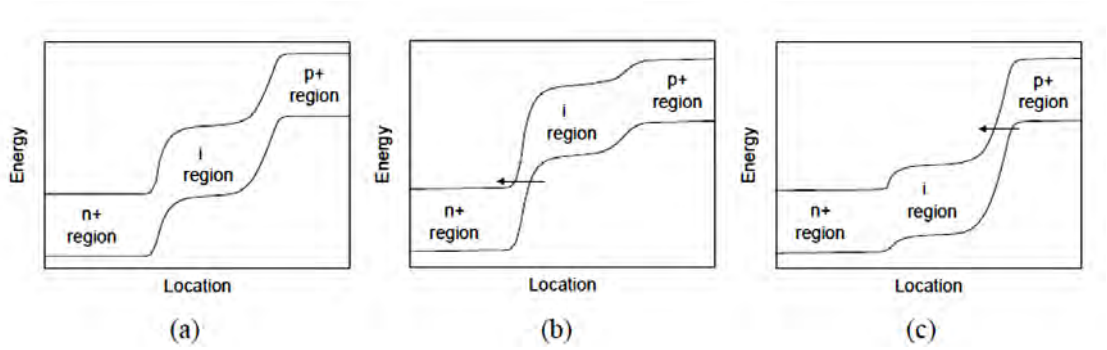


Figure 1.3: Energy band diagrams taken horizontally across the body of a TFET in (a) the OFF-state where the only current comes from p-i-n leakage, (b) the on-state with a negative bias on the gate leading to p-type TFET behavior, and (c) the on-state with a positive bias on the gate leading to n-type TFET behavior.

When a TFET is OFF, only p-i-n diode leakage current flows between the source and drain and this current can be extremely low which is less than a fA/μm. Figure 1.3(a) shows the energy bands horizontally across the body of a TFET in the OFF-state, with a reverse bias applied across the p-i-n junction, but no voltage applied to the gate. If a TFET is designed with similar doping levels and similar gate alignment in the n- and p-sides, then the device exhibits ambipolar behavior. Figure 1.3(b) shows the energy band diagram with a reverse bias applied across the device and a negative voltage applied to the gate. The energy bands in the intrinsic region under the gate are lifted, and the energy barrier is now small enough for band to band tunneling to take place between the valence band of the intrinsic region and the conduction band of the n+-region. When a positive voltage is applied to the gate, on the other hand, the energy bands in the intrinsic region are pushed down, as in Figure 1.3(c), and tunneling takes place between the valence band of the p+-region and the conduction band of the intrinsic region. The energy barrier width for band-to-band tunneling is the single most important factor that determines the amount of drain current through a TFET.

The ON-current of an n-type TFET depends on the width of the energy barrier between the intrinsic and p+ regions, and the current increases exponentially with a reduction in this barrier width. Figure 1.4 shows the dependence of the energy barrier width on the gate voltage for several different gate dielectric constants.

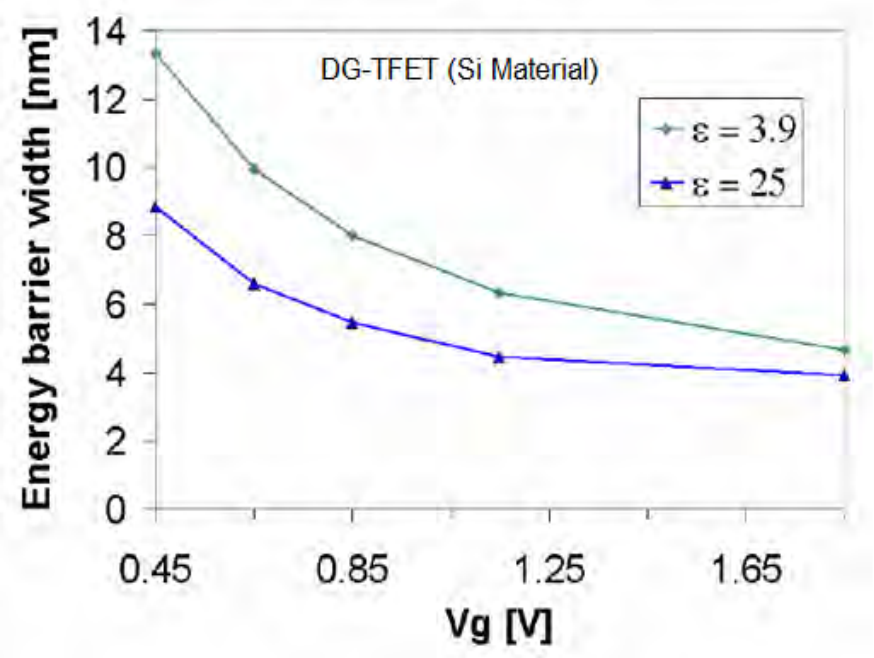


Figure 1.4: Energy barrier width dependence with the variation of gate voltage for several different gate dielectric constants

1.4.2 Subthreshold Slope

The SS is typically defined as the inverse of the rate of change in current as a function of gate voltage and it can be written as [35]:

$$SS = \frac{\partial V_g}{\partial(log_{10} I)} \text{ [mV/dec]} \quad (1)$$

The subthreshold slope of a MOSFET [33] is limited by the diffusion current physics of the device in weak inversion, such that the minimum possible swing in an ideal device is

$$SS_{MOSFET} = ln(10)\frac{kT}{q} \text{ [mV/dec]} \quad (2)$$

which is about 60 mV/dec at room temperature (300 K) known as Boltzmann Tyranny. On the other hand, a TFET does not experience the same physical limitation, because the current mechanism relies on the tunneling-barrier width rather than the formation of an inversion channel. Starting from Hurkx's band-to-band tunneling model [35] the subthreshold slope for a TFET can be expressed in terms of the gate voltage as

$$SS_{TFET} = \frac{{V_g}^2}{5.75(V_g + const)} \text{ [mV/dec]} \quad (3)$$

where the constant is determined by device dimensions and material parameters. Equation (3) shows that, the subthreshold slope is highly dependent on the gate voltage and one should distinguish between the point and the average slopes. This is an important remark for future benchmarking of new abrupt switch solutions, for which most reports currently point to the optimization of the point slope only.

Due to the changing values of slope along the I-V_g curve, it is useful to define two different types of swing that are point swing and average swing. These are illustrated in Figure 1.5. Point swing is the smallest value of the subthreshold swing anywhere on the I-V_g curve, typically found right as the device leaves the OFF-state and tunneling current starts to flow. Average swing is taken from the point where the device starts to turn on, up to threshold, often defined using the constant current technique. Average swing is the more useful value for circuit designers.

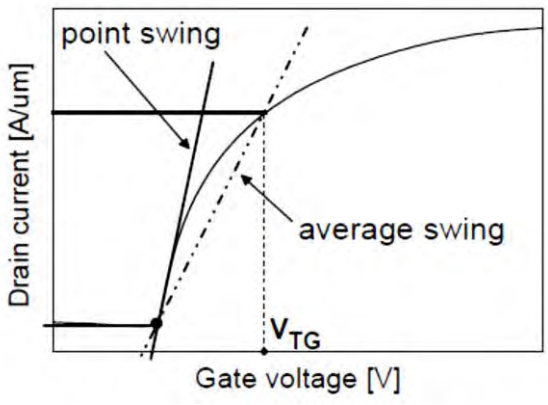


Figure 1.5: Visual definitions of point swing, taken at the steepest point of the I-V_g curve, and average swing, taken as the average from turn-on to threshold.

1.5 Ferroelectric FET (Fe-FET) Structure

It is of significant importance to have a steep subthreshold slope because lowers the supply voltage and hence the power dissipation can be achieved. However, in a traditional MOSFET, a fundamental limit of surface potential change of $2.3k_BT$ is required to modulate the subthreshold current by 10 times, which is known as Boltzmann tyranny. Fe-FET is proposed by integrating ferroelectric material as a voltage amplifier in a traditional MOSFET structure to achieve the fast transition in subthreshold region. On the other hand, the aggressive scaling of CMOS technology inevitably leads to a drastic challenge in process variations, such as channel length variation, channel dopant fluctuations, and other layout-dependent proximity effects.

To enable the early-stage exploration of circuit design and better understand the impact on performance variability, it is necessary to develop an effective model that is able to physically capture the steep subthreshold slope and embed it into standard model parameters for circuit simulation. A new threshold voltage model of Fe-FET is proposed in to capture the steep subthreshold behavior. This model is derived from the first principle and physically captures the subthreshold behavior of Fe-FET such that model scalability is guaranteed for future technology generations.

Fe-FET is proposed in to speed up the transition by stacking a ferroelectric material on top of silicon dioxide as a voltage amplifier to boost surface potential in a MOSFET structure, as shown in the schematic in Figure 1.6. Figure 1.7 illustrates the equivalent capacitance model for a Fe-FET device, where the ferroelectric capacitance (C_{FE}) is in series with the oxide capacitance (C_{ox}) combined to form the insulator capacitance C_{ins} and the substrate capacitance (C_s). V_{int} denotes the internal voltage between C_{FE} and C_{ox}.

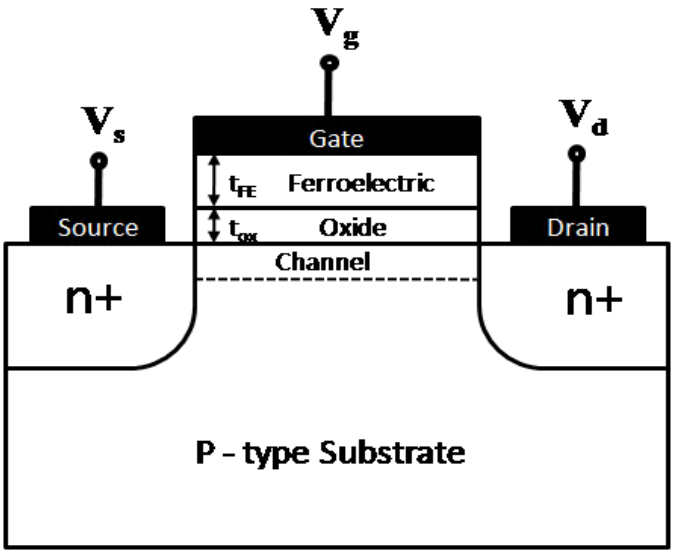


Figure 1.6 Cross-section of Ferroelectric FET proposed by Salahuddin and Datta [9]

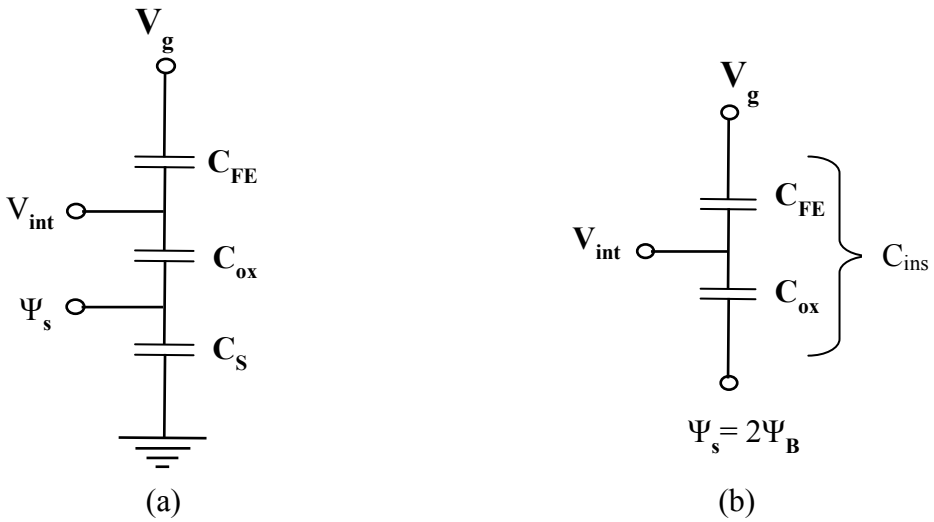


Figure 1.7: (a) The equivalent capacitance model in the substrate to gate region (b) The capacitance model in the ferroelectric and oxide region.

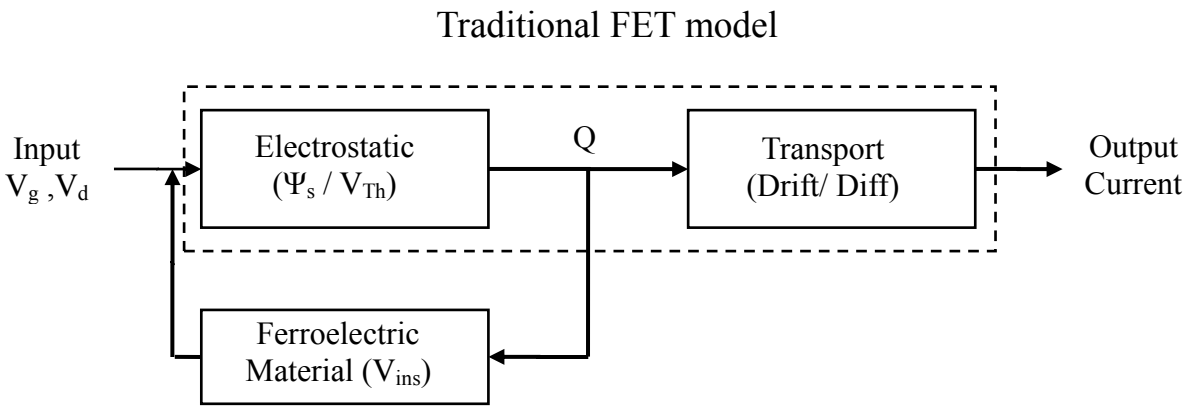


Figure 1.8: The integration of the ferroelectric material into traditional FET model

The negative capacitance of the ferroelectric dielectric originates from the intrinsic feedback mechanism between the induced charge and the voltage drop on the capacitance; it is modeled by inserting an additional feedback path in traditional CMOS model, as shown in Figure 1.8. This feedback between charge and voltage drop is modeled by Eq. (1),

$$V_g - V_{int} \approx \alpha_0 Q + \beta_0 Q^3 + \gamma_0 Q^5 + \rho_0 \frac{dQ}{dt} \quad (1)$$

where α_0 and $\beta_0$are negative to account for the negative capacitance. γ_0 is positive to describe the behavior of normal capacitance. ρ_0 is the resistivity for the voltage drop. Those parameters (α_0, β_0, γ_0 and ρ_0) are proportional to the thickness of ferroelectric dielectric (t_{FE}), and are modeled in the following equations -

$$\alpha_0 = 2\alpha t_{FE} \text{ , } \beta_0 = 4\beta t_{FE} \text{ , } \gamma_0 = 6\gamma t_{FE} \text{ and } \rho_0 = \rho t_{FE}$$

Where, α, β, γ and ρ are material co-efficient of the ferroelectric dielectric. The internal voltage (V_{int}) which accounts for the change of voltage drop in C_{FE}.

SS can be written as the following form incorporate with the effect of surface potential. By incorporating the ferroelectric material the value of SS becomes much lower to overcome the fundamental physical limit -

$$SS = \left(\frac{\partial V_g}{\partial \psi_s}\right)\left(\frac{\partial \psi_s}{\partial (log_{10} I)}\right) \quad (2)$$

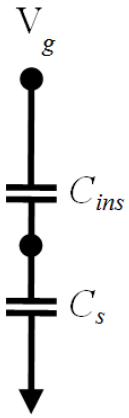


Figure 1.9: The insulator capacitance C_{ins} is in series with another capacitance C_s. C_s comprises of the body capacitance, the channel to source capacitance, the channel to drain capacitance

Here

$$F1 = \frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_s}{C_{ins}} \tag{3}$$

and $$\frac{\partial \psi_s}{\partial (log_{10} I)} = 2.3 k_B T/dec \; = \; 60\, mV/dec$$

From Equation (3), one would see that it is a product of two terms. The first term is often called the 'body factor' *F1* of the FET. The second term, which represents the change of surface potential as a function of drain current, has a fundamental value of 60mV/dec at room temperature for a FET where the transport is dominated by thermionic emission. Eq. (3) shows the expression for *F1*. One would recognize that this is a ratio of the supply voltage V_g to the internal node voltage ψ_s, which is, in the usual case, always larger than 1. This is why the subthreshold slope has the limit of 60mV/dec at room temperature. However, the same reasoning will also tell us that, if one could imagine an insulator with a negative capacitance, then in Eq. (3), *F1* will be less than 1, which will then bring down the subthreshold swing below 60 mV/decade. This negative capacitance is shown by the ferroelectric material like $BaTiO_3$, $SrTiO_3$ and other related material that ensures the value of *F1* is less than 1 by adjusting some parameter which is related to the capacitive term.

1.6 Proposal of Ferroelectric TFET device

Here we proposed a modified device structure of TFET including negative capacitive mechanism which shows some extra beneficial behavior over conventional MOSFET and also traditional TFET. This proposed structure combines the mechanism of tunneling FET and the theoretical concept of Fe-FET. Here we developed the tunneling mechanism for the ON Current which use band to band tunneling in their ON-state and show a very small leakage current, in range of femtoamperes due to the large tunneling barrier formed when the device is turned off. Double gate configuration and the replacement of the SiO_2 by the ferroelectric material like $BaTiO_3$ or $SrTiO_3$ tend to enhance the device performance.

The major crisis of the traditional MOSFET is that, when it aggressively scaled down it suffers high SS and thus high operating voltage which makes the power consumption a rising challenge. But by using DG-TFET, we can achieve SS < 60 mV/dec. It also operates a lower supply voltage than the conventional MOSFET. So, TFET is a excellent replacement of the conventional MOSFET at low operating voltages for low power digital applications. The subthreshold slop (SS) for DG-TFET is possible to achieve ~50 mV/dec [36]. Fe-FET is also a superior alternative device that can achieve much lower SS by using the theoretical concept of negative capacitive mechanism.

So, our proposed device named Fe-TFET combines the both phenomenon of band to band tunneling (BTBT) mechanism and negative capacitance (NC) behavior of ferroelectric material. By using this Fe-TFET, we can achieve much lower SS and get sufficiently high drive current at a very low operating voltage. Thus the I_{ON}/I_{OFF} ratio becomes greater than that of a MOSFET and also for traditional TFET.

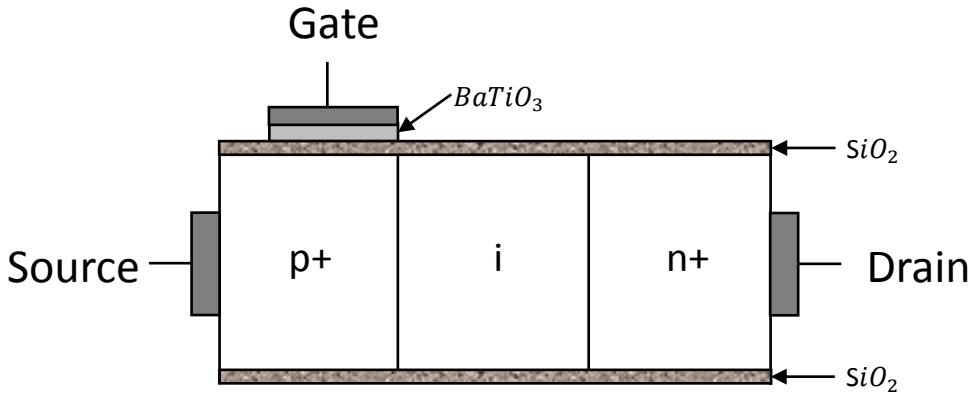


Figure 1.10: Cross section of Ferroelectric Tunneling FET with one gate

1.7 Objective of this Study

The objectives of this work are:

i. Study of a proposed structure of Ferroelectric Tunneling Field Effect Transistor (Fe-TFET).
ii. Analytical modeling of I-V characteristics of the Fe-TFET.

The outcome of this work is to accomplish the following –

i. Analytical modeling of Fe-TFET with different semiconductor material
ii. Establishment of the better performance in terms of SS and I_{ON}/I_{OFF} ratio.

1.8 Thesis Outline

Chapter 2 describes the double gate structure of FET device and initiates the ferroelectric oxide in place of traditional oxide or high k dielectric material. The double gate ferroelectric tunneling FET Structure is considered for the Si, Ge, GaAs and InAs substrate. Reasons of modifications are clarified in this chapter.

Chapter 3 at first 1-D Poisson's Equation is solved to evaluate the surface potential and the electric field. Then the Surface Potential is modeled to develop the relationship between the surface potential and the gate voltage by using Landau-Khalatnikov method. Finally the ON Current equation is modeled considering the onset voltage using Kane's Model.

Chapter 4 presents the new proposed device characteristics in case of Si, GaAs, Ge and InAs. The impact of different Ferroelectric material, oxide thickness variation, source doping concentration and gate length are described with illustrations. Next the device performance of Double gate Ferroelectric TFET is compared with semi classical Double Gate TFET. Finally, optimization of SS and improvement of I_{ON}/I_{OFF} ratio are explained in this section.

Chapter 5 draws the conclusion of this work. This chapter summarizes the findings of the study. It also puts forward suggestions regarding future scopes of works related to this thesis.

CHAPTER 2
Double Gate Ferroelectric TFET

2.1 Introduction

Double Gate Ferroelectric Tunneling Field Effect Transistors (DG Fe-TFET) use the tunneling of electrons as the carrier transport method for device operation. They are generally designed as gated p-i-n diodes, where the gate is used to modulate an effective tunneling barrier height. Ideally, these devices exhibit a very low OFF-state current (proportional to reverse biased diode leakage), a very low subthreshold slope and high ON-current. TFETs can be generally classified as point and/or line tunneling devices. In a point tunneling device, the source does not appreciably deplete, but the gate causes the channel region to invert, resulting in tunneling from the source to the channel. In a line tunneling device, the source is inverted (generally by engineering an overlapped gate with an optimized source doping profile), resulting in tunneling into the inversion layer, similar to Gate-Induced Drain Leakage.

Here, we proposed a point tunneling device structure where gate is located fully top of the source region. Gate voltage allows the band bending of the depletion region under the portion that resides in the interface of the gate and source region. These band bending permits the transport of electron from valence band to conduction band causes the tunneling current. Simulation results show very low subthreshold slope at very low operating voltage in the range of 0.8 V. It also shows high ON current in the range of 0.02 A/μm. Gate leakage was neglected in the device that we propose here, because the thickness of oxide is large enough to limit the OFF-current in fabricated TFETs.
So, it is evident that this device theoretically proves a very efficient. But in case of TFET, the experimental results show very low subthreshold slope at very low currents. However, unless TFETs improve to better match their simulation results, they have limited application for logic devices.

2.2 Double Gate Structure of Fe-TFET

Double Gate TFET is a good consideration to increase the current at least double which is very much beneficial over the TFET with single gate [37-39]. In this way, in case of Fe-TFET, the ON-current is boosted, while the OFF-current, still in the femtoamperes or picoamperes range, increases by the same factor but remains

extremely low. When the device body is thin enough, however, the electrostatic control of the tunnel junction by the gate will be improved with a double-gate configuration, and the current will more than double. The double gate gives an advantage of about two decades of current in subthreshold and about one decade for high V_g. The subthreshold slope and threshold voltage are also reduced with the double-gate configuration.

2.3 Ferroelectric Oxide

Ferroelectric oxide shows different behavior than the traditional oxide SiO_2 and the high k dielectric material. It exhibits negative capacitance in a certain range and this property distinguishes the ferroelectric from the regular capacitor.

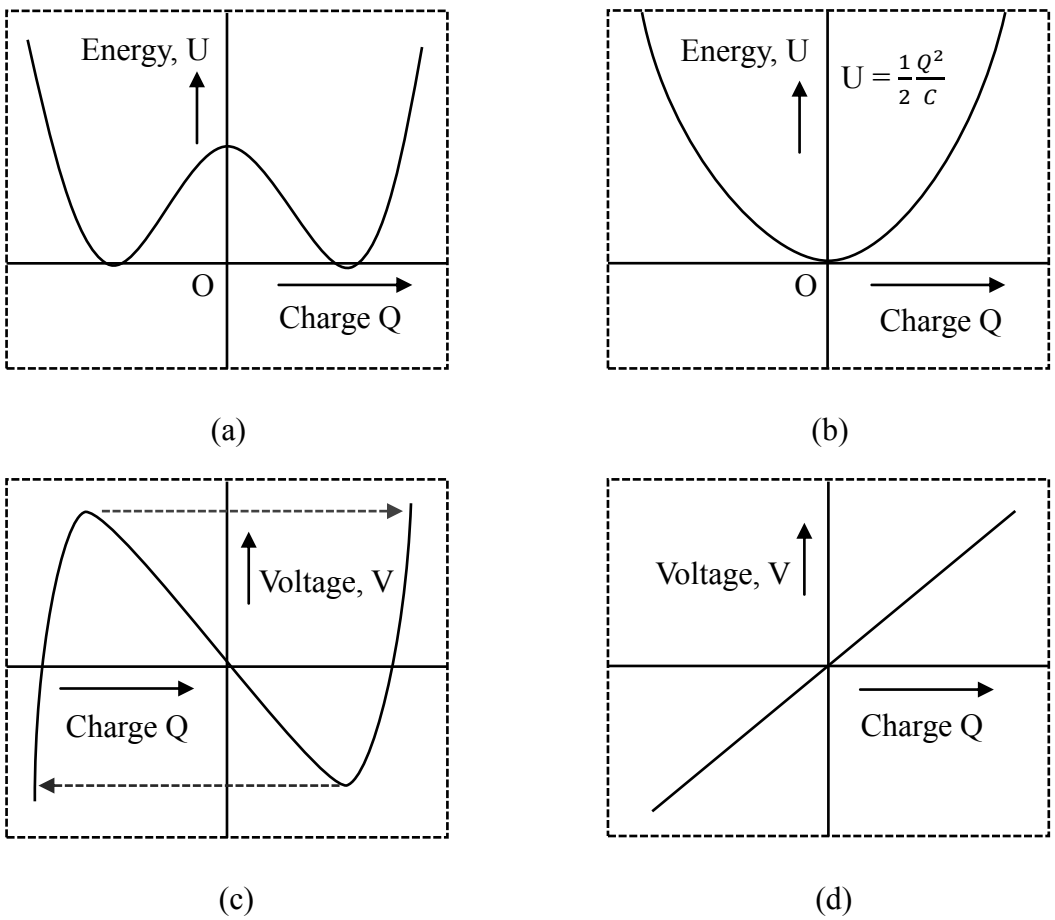
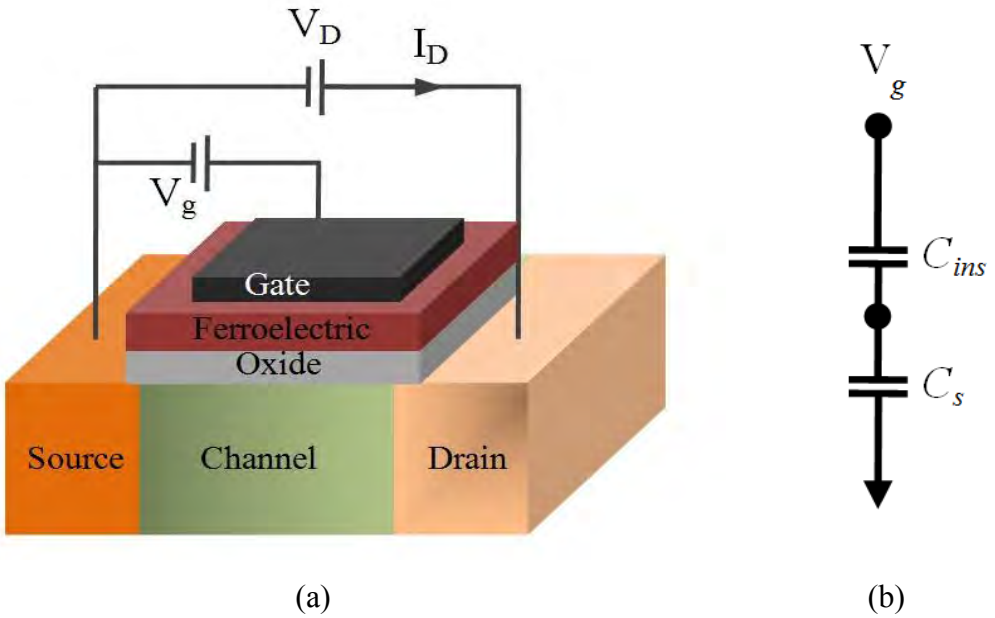


Figure 2.1: (a) The energy landscape of ferroelectric showing negative capacitance. (b) The energy landscape of a usual capacitor. The landscape shows well known $Q^2/2C$ dependence. (c) Derivative dU/dQ vs. Q found from (a). (d) Derivative dU/dQ vs. Q found from (b).

Figure 2.1 (a) and (b) show the energy landscapes of a ferroelectric and regular capacitor respectively. If we look at the region around zero charge, we notice that the curvature of energy landscape is opposite for the ferroelectric insulator in comparison to a regular capacitor. This gives the first hint that, in this region, the capacitance of the ferroelectric is negative. Formally, the capacitance is defined as the inverse slope of the derivative dU/dQ. The derivative plots for Figures. 2.1(a) and 2.1(b) are shown in 2.1(c) and 2.1(d). We see that in the region indicated by the circle, the slope is negative and hence the capacitance is negative. However, one would also notice that in this region, the material is unstable. This is because the arrow indicated region in 2.1(a) is far from the energy minima. One can show that this instability translates to the typical hysteretic behavior of a ferroelectric material (see the dashed lines).



(a) (b)

Figure 2.2: (a) Schematic of a FET with the gate circuit. (b) The insulator capacitance C_{ins} is in series with another capacitance C_s. C_s comprises of the body capacitance, the channel to source capacitance, the channel to drain capacitance.

Now let us consider a combination of capacitances having a positive and a negative capacitor in series as shown in the gate circuit of Figure 2.2(b), so that the total capacitance is given by

$$\frac{1}{C} = \frac{1}{C_s} - \frac{1}{C_{ins}} \tag{1}$$

If this total capacitance of the series combination is positive, then the total system remains stable and will not show any hysteresis. Thus the ferroelectric can be part of a

stable system even though being in an unstable state of negative capacitance by itself. One would also see from Eq. (1) that the total capacitance in this series combination is larger than either of the two constituent capacitances, which means that the total capacitance is enhanced.

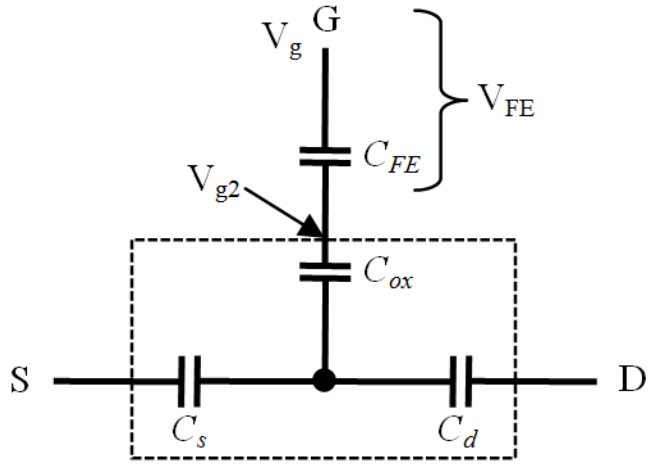


Figure 2.3: The capacitive model shown in Figure 2.2(a) is modified by putting a ferroelectric insulator on top of a SiO_2 layer

The energy landscape of a ferroelectric material shown in Figure 2.1(a) is given by the following expression

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 \tag{2}$$

Where $\boldsymbol{P}$ is the polarization and α, β and γ are anisotropy constants. This is often termed as the Gibb's free energy of the system [7]. α and β are usually negative and γ is positive. One would then see that the low charge region is dominated by α, whereas the intermediate region by β. As a result, for low charge region the system is unstable and in a negative capacitance region. However for higher values of charge density, γ becomes more and more important and at some point overcomes the negative contribution from α and β making the system stable again in a positive capacitance region.

2.4 Double Gate Fe-TFET Device Structure

Our proposed device indicated in the figure is modified structure than the conventional TFET. Here Gate on Source is demonstrated to achieve the good control of the band to band tunneling current. Thus the band to band tunneling current is mostly influenced by the gate voltage and has a little effect on drain voltage. The device can be regarded as an extreme case of the short gate TFET as the gate does not even cover a part of the channel. It is important to note that in this device, the tunneling occurs in the direction orthogonal to the gate. The one-dimensional nature of the band to band tunneling enables an approximate determination of the potential profile in the tunneling region.

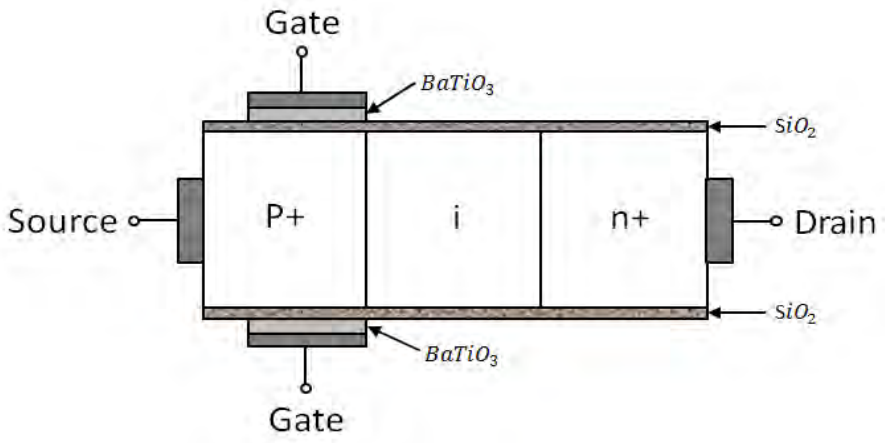
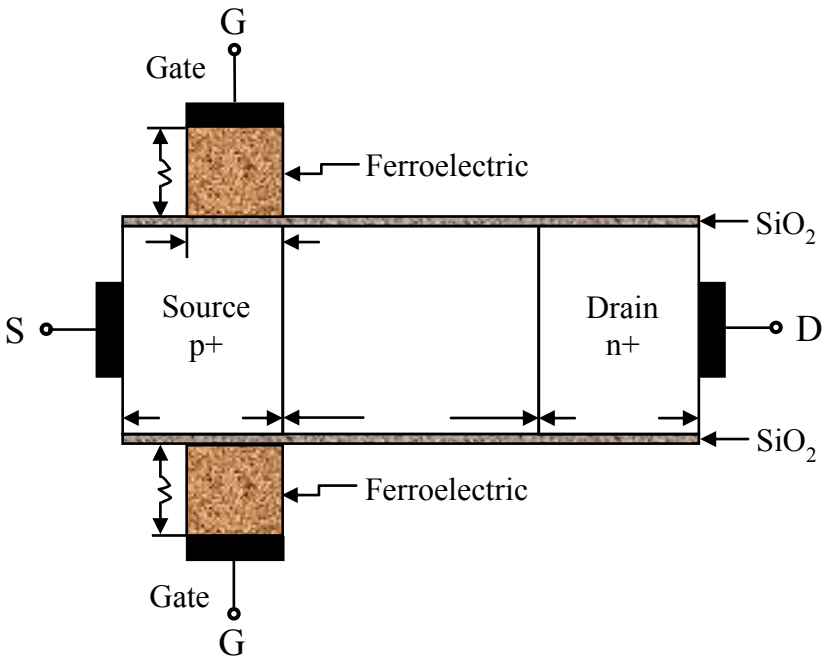


Figure 2.5: Double Gate ferroelectric tunnel field effect transistor with the gate is located fully on top of the source

In this work we propose a modified structure of TFET incorporating Ferroelectric capacitor as the gate oxide, called the Ferroelectric TFET (Fe-TFET). The proposed device effectively combines two different mechanisms of lowering the sub threshold slope (SS) for a transistor garnering a further lowered one compared to conventional TFET. A simple yet accurate ON current model of the proposed device is presented here. Fe-TFET gives ON current as high as 0.02 A/μm for a gate voltage of 0.6 V, OFF current of less than 1pA/μm and an improved lower SS, according to the results yielded from the analytical model. This work also provides physics based reasoning behind the multiplicative improvement in the SS for the proposed device.

2.4.1 Si Tunneling Fe-TFET Scheme

In the following device structure, Si material is used in the source region and barium titanate is used as



ferroelectric oxide in between the metal gate and source interface.

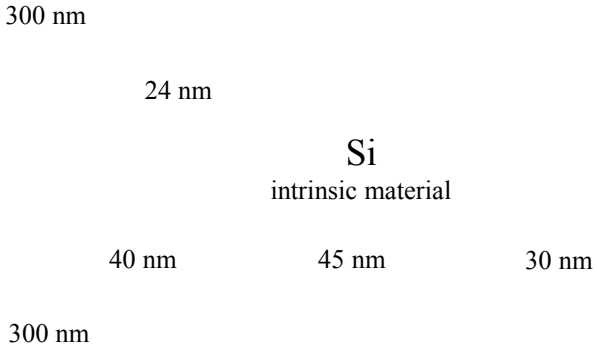


Figure 2.6: Double Gate ferroelectric Si tunneling field effect transistor with the gate is located fully on top of the Source

2.4.2 Ge Tunneling Fe-TFET Scheme

In the following device structure, Ge material is used in the source region and barium titanate is used as ferroelectric oxide in between the metal gate and source interface.

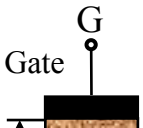


Figure 2.7: Double Gate ferroelectric Ge tunneling field effect transistor with the gate is located fully on top of the Source

2.4.3 GaAs Tunneling Fe-TFET Scheme

In the following device structure, GaAs material is used in source region and barium titanate is used as ferroelectric oxide in between metal gate and source interface.

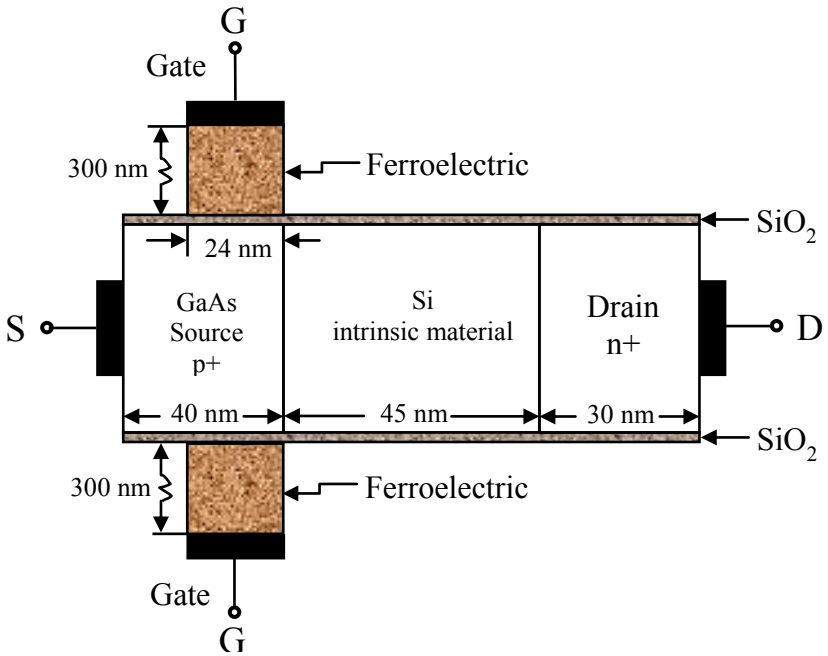


Figure 2.8: Double Gate ferroelectric GaAs tunneling field effect transistor with the gate is located fully on top of the Source

2.4.4 InAs Tunneling Fe-TFET Scheme

In the following device structure, InAs material is used in source region and barium titanate is used as ferroelectric oxide in between metal gate and source interface.

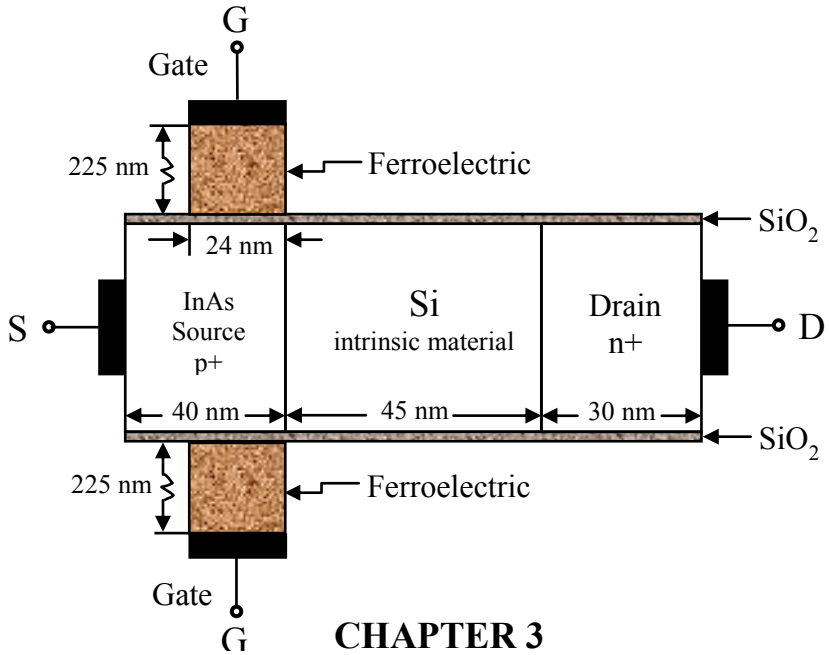


Figure 2.9: Double Gate ferroelectric GaAs tunneling field effect transistor with the gate is located fully on top of the Source

3.1 Introduction

As MOSFETS reach nanometer dimensions, power consumption becomes a major blockage for further scaling. The continued reduction of the MOSFET size is leading to an increased leakage current due to short channel effects, such as Drain Induced Barrier Lowering (DIBL) and the power supply voltage cannot be reduced any further because of the subthreshold slope being limited to 60 mV/decade at room temperature. In this view, the exploration of alternative devices which possibly outperform the MOSFET at these nanometer dimensions is required.

A promising alternative for the MOSFET, which does not suffer from these limitations, is the Ferroelectric tunneling field-effect transistor (Fe-TFET). Throughout the rest of this work the term Fe-TFET will not refer to any specific implementation form, but the Fe-TFET is defined as a semiconductor device in which the gate controls the source-drain current through modulation of Band-to-Band Tunneling (BTBT). Band-to-Band Tunneling is a process in which electrons tunnel from the valence band through the semiconductor band gap to the conduction band or vice versa.

TFETs with a subthreshold slope lower than 60 mV/decade have already been demonstrated and due to their built in tunnel barrier, Si TFETs are expected to maintain low OFF currents for channel lengths down to 10 nm. An advantage of TFETs compared to other alternative device concepts is that their fabrication is compatible with standard CMOS processing since they can be implemented as a reverse biased gated p-i-n diode. So, our proposed device named Fe-TFET concocts the TFET mechanism and negative capacitance of Ferroelectric material. In this work, an analytical model for our novel device is developed. A new modified TFET device structure is presented for which the potential profile can be determined straightforwardly. As a result, the total current through the device can be calculated analytically. In order to obtain a closed expression for the current, an approximation regarding the behavior of the current around the band to band tunneling onset voltage needs to be made, as discussed.

3.2 Solve 1-D Poisson's Equation to evaluate Surface Potential and Electric Field

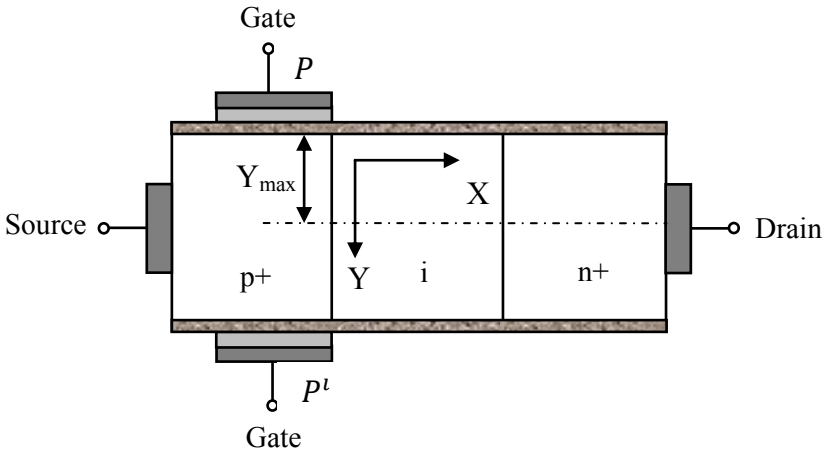


Figure 3.1: DG Fe-TFET with positive gate bias applied such that a depletion region with thickness Y_{max} exists (only upper half shown)

For one dimensional approach, the electrostatic potential in a semiconductor by ψ is given by Poison's equation [40],

$$\frac{d^2\psi_s(y)}{dy^2} = -\frac{\rho(y)}{\epsilon_s}$$

Where $\psi_s(y)$ is the surface potential, $\rho(y)$ is the volume charge density and $\epsilon_s$is the permittivity of the semiconductor. Here, $\rho(y) = -qN_a$

$$\therefore \frac{d^2\psi_s(y)}{dy^2} = \frac{qN_a}{\epsilon_s} \quad \text{(A)}$$

By integrating equation (A) we have that

$$\psi_s(y) = \frac{qN_a}{2\epsilon_s}(y - y_{max})^2$$

As the electric field

$$E(y) = -\frac{d\psi_s(y)}{dy}$$

$$\therefore E(y) = -\frac{qN_a}{\epsilon_s}(y - y_{max})$$

Where, y_{max} is the length of the depletion region which is the function of gate voltage and q is the elementary charge.

3.3 Modeling of Surface Potential using Landau-Khalatnikov Method

Now we need to develop a relation between the gate voltage and surface potential in the highly doped source region.

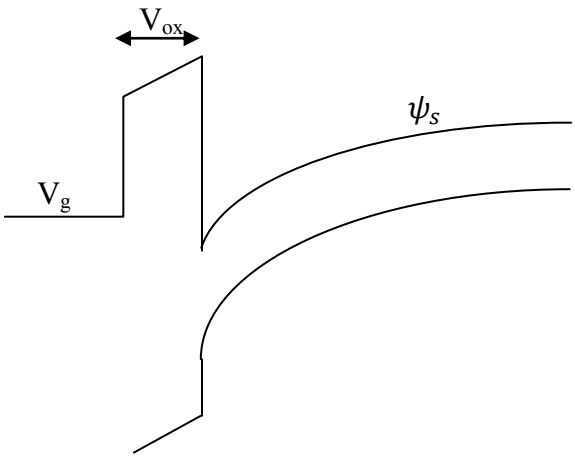


Figure 3.2: Energy band diagram of metal, ferroelectric oxide and semiconductor junction

Here $\psi_s$is the surface potential. So,

$$V_g = V_{FB} + V_{ox} + \psi_s \tag{A}$$

The physics for the traditional MOS Capacitor is well known and needs no mention but the dynamics for the negative capacitor needs clarification to develop a simple linear intuitive model for optimization of device operation.

From LK (Landau-Khalatnikov) equation [41-43] we know

$$e\frac{d\bar{P}}{dt} + \bar{\nabla}_{\mathrm{p}}\mathrm{U} = 0 \tag{1}$$

Where, U is the Gibbs free energy. We can express it in terms of anisotropy energy.

$$\mathrm{U} = \alpha P^2 + \beta P^4 + \gamma P^6 - \bar{E}_{ext.}\bar{P} \tag{2}$$

Where, $\bar{P}$ is the polarization charge per unit area.
Putting equation (2) in (1) we get

$$\rho\frac{d\bar{P}}{dt} + 2\alpha P + 4\beta P^3 + 6\gamma P^5 - \bar{E}_{ext} = 0$$

At steady state

$$\frac{d\bar{P}}{dt} \approx 0$$

$$\therefore\ 2\alpha P + 4\beta P^3 + 6\gamma P^5 = \bar{E}_{ext}$$

Here in this case

$$E_{ext} = \frac{V_{ox}}{t_{ox}}$$

$$V_{ox} = 2\alpha t_{ox}P^2 + 4\beta t_{ox}P^3 + 6\gamma t_{ox}P^5$$

$$V_{ox} = \alpha_0 P + \beta_0 P^3 + \gamma_0 P^5$$

Here

$$\alpha_0 = 2\alpha t_{ox}\ , \beta_0 = 4\beta t_{ox} \text{ and } \gamma_0 = 6\gamma t_{ox}.$$

For Ferroelectric material $P \approx Q$

$$V_{ox} = \alpha_0 Q + \beta_0 Q^3 + \gamma_0 Q^5 \quad (3)$$

If the inversion layer capacitance is C_{inv} and charge is Q

$$\text{Then, } C_{inv} = \frac{Q}{\psi_s} \qquad \therefore\ Q = C_{inv}\psi_s$$

From equation (3) we get

$$V_{ox} = \alpha_0 C_{inv}\psi_s + \beta_0 {C_{inv}}^3 {\psi_s}^3 + \gamma_0 {C_{inv}}^5 {\psi_s}^5$$

$$V_{ox} = X\psi_s + Y{\psi_s}^3 + Z{\psi_s}^5$$

Here, $X = \alpha_0 C_{inv}$, $Y = \beta_0 {C_{inv}}^3$ and $Z = \gamma_0 {C_{inv}}^5$

If we assume the effect of higher order term is negligible then

$$V_{ox} \approx X\psi_s \quad (4)$$

Putting the value of equation (4) to equation (A), we get

$$V_g = V_{FB} + X\psi_s + \psi_s$$

$$\therefore \psi_s = \left(\frac{V_g - V_{FB}}{1 + X}\right)$$

This is the relation between the surface potential and applied gate voltage.

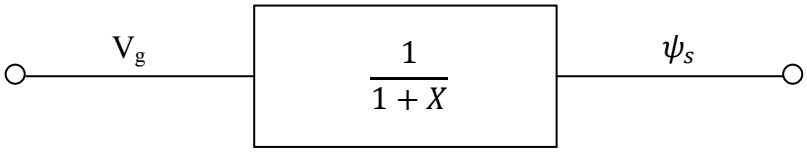


Figure 3.3: Auto-Transformer relationship between gate voltage and surface potential

By making the$(1 + X) < 1$, we can get an amplified surface potential.

Here the functional block acts as if it were a transformer. The amplification phenomena introduced by the negative capacitance gate stack. Significantly reduces the gate voltage requirement for sufficient BTBT current.

3.4 Evaluation of onset voltage, V_{onset}

Thus along the x-direction, no potential change is considered, so the electric field will be changed along the y-direction. Here gate voltage is the function of surface potential and the parameter X which has great significance related to the properties of ferroelectric material. So, the gate voltage

$$V_g = V_{FB} + (1 + X)\psi_s$$

For better understanding the mechanism of tunneling current, onset voltage V_{onset} is evaluated which marks the onset band to band tunneling current in the depletion region [30]. It can also say that the band to band tunneling begins when the band bending is equal to the energy gap.

So

$$V_{onset} = V_{FB} + (1 + X)\frac{E_g}{q}$$

3.5 Evaluation of ON Current Equation using Kane's Model

The current I is found by the integration of the band to band generation rate G_{B2B} on the volume of the device

$$I = q \int G_{B2B}\, dV = qWL_g \int G_{B2B}\, dy \qquad \text{(B)}$$

Where, L_g and W are the gate length and width respectively. By using Kane's Model [2], the band to band generation rate G_{B2B} can be calculated from the following equation

$$G_{B2B} = A_{kane} \frac{|E|^D}{\sqrt{E_g}} exp\left(-B_{kane} \frac{{E_g}^{3/2}}{|E|}\right) \qquad (1)$$

Where, E_g is the band gap, D is the material dependent parameter of Kane's Model and $A_{kane} = \left(e^2 {m_{eff}}^{1/2}\right)/(18\pi\hbar^2)$ and $B_{kane} = \left(\pi {m_{eff}}^{1/2}\right)/(2q\hbar)$ are in general functions of carrier effective mass m_{eff} [3]

Thus neutral region does not contribute to the band to band tunneling current I. So, the current is evaluated considering only a depletion region instead of relying on the local electric field .

The average electric field in the y-direction is given by

$$E_y(avg) = \frac{E_g}{q l_{tpath}} \qquad (2)$$

Where, l_{tpath} is the tunneling path.

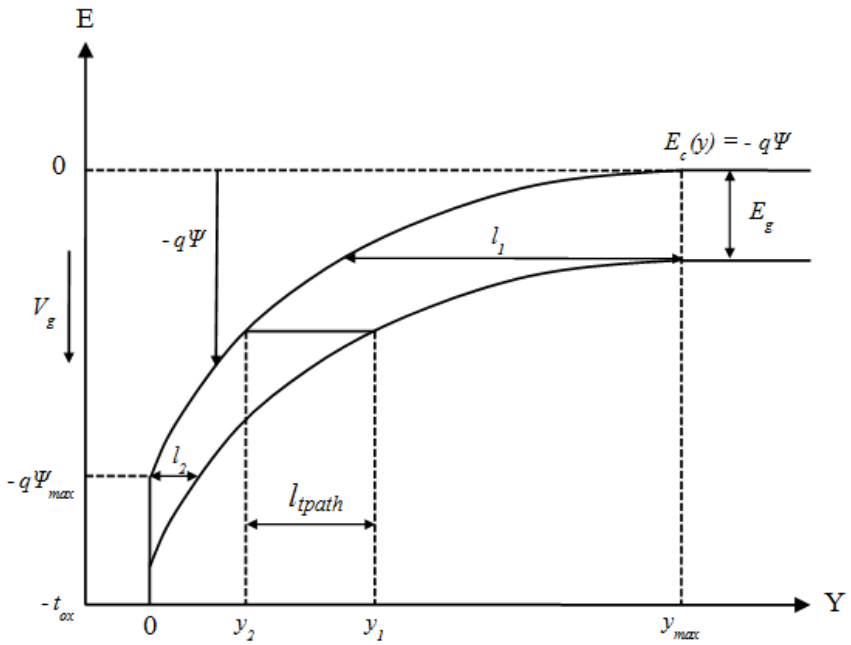


Figure 3.4: Band diagram of the cross-section P-P[1] from Figure 3.1 indicating l_{tpath}

For calculating the tunneling path, two points [y_1 (valance band) & y_2 (conduction band)] in the y direction are considered which are at the same potential

$$\psi_v(y_1) = \psi_c(y_2)$$

Here,

$$\psi_v(y_1) = \frac{qN_a}{2\epsilon_s}(y_1 - y_{max})^2 + \frac{E_g}{q}$$

and $$\psi_c(y_1) = \frac{qN_a}{2\epsilon_s}(y_2 - y_{max})^2$$

$$\therefore (y_2 - y_{max})^2 = (y_1 - y_{max})^2 + C$$

Where $$C = \frac{2E_g\epsilon_s}{q^2N_a} \text{ and } l_{tpath} = y_1 - y_2$$

$$\therefore (y_2 - y_{max})^2 = \left(l_{tpath} + y_2 - y_{max}\right)^2 + C$$

Solving the above equation we get

$$y_2 = y_{max} - \frac{{l_{tpath}}^2 + C}{2l_{tpath}} \quad (3)$$

From the equation (3) we get the following equation for the expression of by

$$\therefore dy = \frac{1}{2}\left(\frac{C}{{l_{tpath}}^2} - 1\right) dl_{tpath} \quad (4)$$

Putting the equation (1), (2) and (4) in equation (A) we get the following expression

$$I = \frac{qWL_gA_{kane}}{2}\int_{l_1}^{l_2} \frac{{E_g}^{D-\frac{1}{2}}}{q^D {l_{tpath}}^D} exp\left(-B_{kane}q\sqrt{E_g}l_{tpath}\right)\left(1 - \frac{C}{{l_{tpath}}^2}\right) dl_{tpath} \quad (C)$$

In case of non-degenerate semiconductor, the equation of l_1 and l_2 are same as in [4]

$$l_1 = \sqrt{C}$$

and $$l_2 = \sqrt{\frac{qC}{E_g}}\left\{\sqrt{\psi_s} - \sqrt{\psi_s - \frac{E_g}{q}}\right\} \quad (5)$$

Where, Φ_s is the electrostatic potential at the end of the depletion region.

Since we have developed necessary equation to calculate the tunneling length l_1 and l_2. Now we need to evaluate the approximate expression of tunneling current. The integral of the band to band tunneling current expression in equation (C) can be assumed by the following approximating expression

$$I \approx -\frac{WL_g A_{kane} {E_g}^{D-1}}{2B_{kane} q^D}\left(\frac{1}{{l_2}^D} - \frac{C}{{l_2}^{D+2}}\right) exp\left(-B_{kane} q\sqrt{E_g} l_2\right) \quad (D)$$

By using equation (5) and (D) for $\psi_s = \frac{E_g}{q} + \delta\psi$, we get the following equation

$$I \approx \frac{WL_g A_{kane}\sqrt{q}}{B_{kane} {E_g}^{3/2}}\left(\frac{E_g N_a}{2\epsilon_s}\right)^{D/2} exp\left(B_{kane} q\sqrt{2\epsilon_s E_g}/\sqrt{qN_a}\left(\sqrt{\delta\psi} - \sqrt{E_g/q}\right)\right)\sqrt{\delta\psi}$$

Where, $\delta\psi$ is a perturbation of the electrostatic potential which is the function of gate voltage as well as onset voltage.

$$\delta\psi = (V_g - V_{onset})/\sigma \text{ , where, } \sigma = 1 + X$$

Considering the value of D is 2 to get an optimized expression for the band to band tunneling current

$$I \approx WL_g R\ exp\left(S\sqrt{V_g - V_{onset}}\right)\sqrt{V_g - V_{onset}}$$

With

$$R = \frac{A_{kane} N_a}{2 B_{kane} \epsilon_s} \sqrt{\frac{q}{E_g \sigma}}\, exp\left(-B_{kane} q^2 E_g \sqrt{2\epsilon_s} / \sqrt{N_a}\right)$$

$$S = B_{kane} \sqrt{\frac{2 q E_g \epsilon_s}{\sigma N_a}}$$

The respective positions of the quasi-Fermi levels also determine the ratio between band to band tunneling generation and band to band tunneling recombination. In the previous treatment for the depletion region the respective positions of the quasi-Fermi levels were ignored and band to band tunneling was entirely attributed to generation. This is an acceptable approximation as long as the valence band is filled and the conduction band is empty.

In the case of a non-degenerate semiconductor, the inversion regime sets in before the electron quasi-Fermi level and the conduction band meet. In the depletion region, only the tail of the Fermi-Dirac distribution occupies the conduction band which is negligible compared to the almost fully occupied valence band. In the inversion layer however, the conduction band is filled and band to band tunneling recombination can no longer be neglected.

Using the previous approach, the total current in the device equals the current generated in the depletion region. The influence of the gate voltage is straightforward, namely increasing the depletion region size and increasing the current accordingly.

In a degenerate semiconductor, the limits l1, l2 of the integration (5) need to be altered such that the integration only extends over the region of tunneling where the conduction band is (approximately) empty and the valence band is (approximately) full.

CHAPTER 4

Optimization of Simulation Parameters

4.1 Introduction

While the basic parameters to optimize in order to have superior Fe-TFET characteristics are known an abrupt doping profile at the tunnel junction, high capacitive coupling from the gate to the tunnel junction, etc. – it is crucial to also understand the sensitivity of device characteristics to parameter fluctuations. This is well-understood for conventional MOSFETs and the principal sources of fluctuation, including random discrete dopants, different dielectric materials, gate and channel length fluctuations and oxide thickness fluctuations, have been thoroughly studied. The same needs to be accomplished with Fe-TFET, so that the main sources of characteristic fluctuation can be pinpointed and then controlled.

The goals of this chapter are twofold: to optimize the device characteristics of the Fe-TFET using the additive booster technique and then to investigate the influence of the parameter fluctuations which are unavoidable in device fabrication and their impact on device characteristics. The critical parameters that will need to be the most tightly controlled when fabricating these devices are identified and the parameter variation is quantified.

Increasing short channel effects like drain induced barrier lowering (DIBL) and roll-off are serious impediments to further scaling of conventional MOSFET. These limitations instigate all researchers to look for innovative devices. Non-scalable sub-threshold slope in MOSFET limits its application in high speed and low power application.

Fe-TFET is a strong candidate in high speed and low power application because of its potential to get low Sub-Threshold Slope (<60 mV/decade). In the previous work it was demonstrated that silicon double gate TFET (DG-TFET) suffers from unacceptable low ON-current. Here we have shown that, by introducing the ferroelectric material in place of SiO_2; layer high ON-current, low OFF-current and very low SS can be obtained in Double Gate Fe-TFET. Device structure is depicted. As doping profile is high band bending narrowing model is included. In both n-channels mode of operation and p-channel mode of operation conduction takes place by tunneling of electron from valance band of source to conduction band of drain region. Band to band tunneling is a strong function of electric field. As V_g increases from 0-0.8 V band bending becomes significant. In the OFF-state (V_g<0.2 V), current flows very low (<10^{-12} A/μm) and then tunneling current increases very sharply. From the input characteristic we can say that Double Gate Fe-TFET is almost free from drain induced barrier lowering problem. After channel length scaling, OFF-current increases and there is no significant increase of ON-current is seen. But in p-channel mode of operation sufficient band bending takes place at higher gate voltage. The ON-current can be improved by careful choice of ferroelectric material. Very low point subthreshold slope (~ $40mv/dec$) is observed and because of that high I_{ON}/ I_{OFF} ratio (~10^{11}) is seen, which is useful to operate the device in low voltage range. In all low Subthreshold Slope, high I_{ON}/ I_{OFF} ratio and low threshold voltage V_{Th} make this device a strong candidate for ultralow power and ultralow voltage application.

4.2 Device characteristics for Si, GaAs, Ge and InAs

Fe-TFET structure is better option for low power application. I_{ON} current is boosted up with the lowering the band gap which can be achieved by using Ge and InAs. Thus the band gap is reduced gradually then the band to band tunneling occurs by applying very low gate voltage V_g at a certain thickness of ferroelectric material. So, it is very much appreciating novel device to operate in a very small range of gate voltage. And the OFF current is hence supposed to be limited forming a large barrier by the forbidden band gap which should prevent tunneling to happen in the OFF-state.

The band gap is one of the most important parameters when considering a TFET, since it determines the “barrier” between valence and conduction band. The ON-current

increases with decreasing band gap, while also V_{onset} is reduced since the voltage required to create a path from valence to conduction band is directly proportional to the band gap. A small band gap is therefore beneficial for a large Fe-TFET ON-current and is desirable as far as it does not jeopardize the Fe-TFET OFF-current.

Table 1.1: Values of V_{onset}, Biasing V_g, I_{ON}, I_{OFF} for different Material at ferroelectric oxide thickness (t_{ox}) = 300 nm

Material	Band Gap (eV)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)	I_{OFF} (A/μm)
GaAs	1.43	0.4776	1.08	0.024	10^{-13}
Si	1.1	0.4400	0.92	0.025	10^{-10}
Ge	0.66	0.1230	0.62	0.033	10^{-8}
InAs	0.36	0.0928	0.416	0.033	10^{-6}

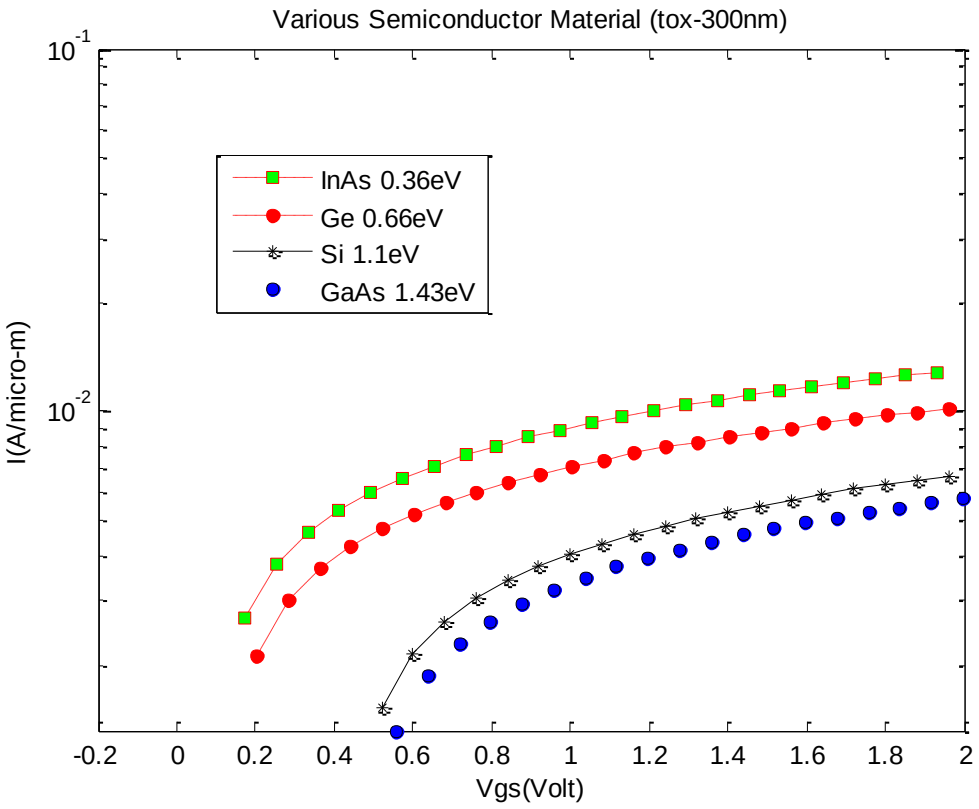


Figure 4.1: I-V_{gs} characteristics curve of DG Fe-TFET for different semiconductor material with fixed ferroelectric oxide thickness, t_{ox} = 300 nm

Table 1.2: Values of V_{onset}, Biasing V_g, I_{ON}, I_{OFF} for different Material at ferroelectric oxide thickness (t_{ox}) = 225 nm

Material	Band Gap (eV)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)	I_{OFF} (A/μm)
GaAs	1.43	0.7157	1.18	0.021	10^{-13}
Si	1.1	0.6050	0.99	0.022	10^{-10}
Ge	0.66	0.2573	0.65	0.0256	10^{-8}
InAs	0.36	0.1596	0.56	0.03	10^{-6}

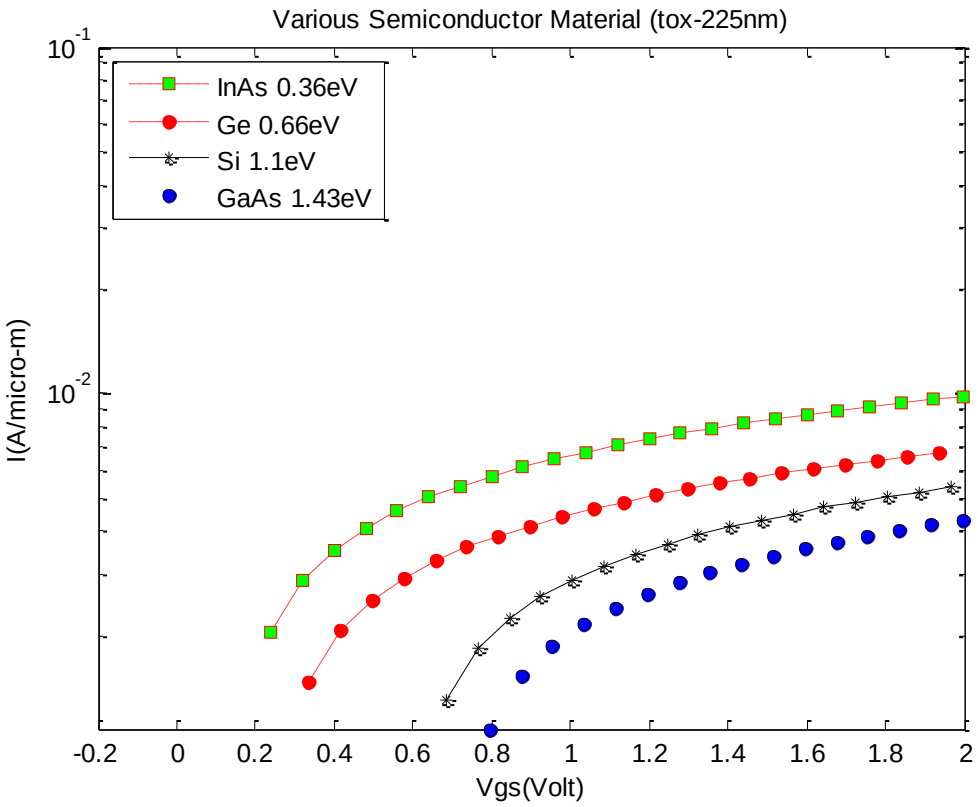


Figure 4.2: I-V_{gs} characteristics curve of DG Fe-TFET for different semiconductor material with fixed ferroelectric oxide thickness, t_{ox} = 225 nm

4.3 Impact of different Ferroelectric material

The impact of different ferroelectric material on the device performance of a n-TFET is studied by varying the anisotropy constants α (-1×10^7 m/F) while keeping its width fixed at 300 nm and 225 nm for the device structure, as shown in Figure 4.3 with L_g = 24 nm. The anisotropy constants α value of the ferroelectric material used are -1×10^7 m/F ($BaTiO_3$) and -5.3×10^8 m/F ($SrTiO_3$). The effects of varying α value of the ferroelectric material on the transfer characteristics of the n-TFET are shown in Figure 4.3 to Figure 4.6. The values of V_{onset} or V_{Th} and I_{ON} are extracted from the transfer characteristics in Figure 4.3 to Figure 4.6.

The α value ferroelectric material of $BaTiO_3$ and $SrTiO_3$ which has been found to improve the device performance of such devices. Moreover, it has also been reported

that the high α value of ferroelectric material deteriorates the performance of an n-TFET, in the presence of such conditions we need to adjust the thickness of ferroelectric material. It may be mentioned here that, in this work, the impact of a α value ferroelectric material on the device performance is investigated for our proposed Double Gate Fe-TFET structure to develop the basic understanding on this subject. Since it is done, it is now open for the researchers to take up a study to investigate the impact of a similar α value ferroelectric material for a p-TFET.

Table 1.3: Values of V_{onset}, Biasing V_g, I_{ON} for different ferroelectric materials (anisotropy constant α) at certain oxide thickness (t_{ox}) in case of GaAs Material

Material GaAs	Ferroelectric Material	α (m/F)	t_{ox} (nm)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)
E_g = 1.43 eV ϵ_r = 13.1 C_s = 0.111 F/m^2	$BaTiO_3$	-1×10^7	300	0.4776	0.782	0.0267
			225	0.7157	0.987	0.021
	$SrTiO_3$	-5.3×10^8	6	0.4205	0.69	0.0264
			4	0.7570	1.043	0.021

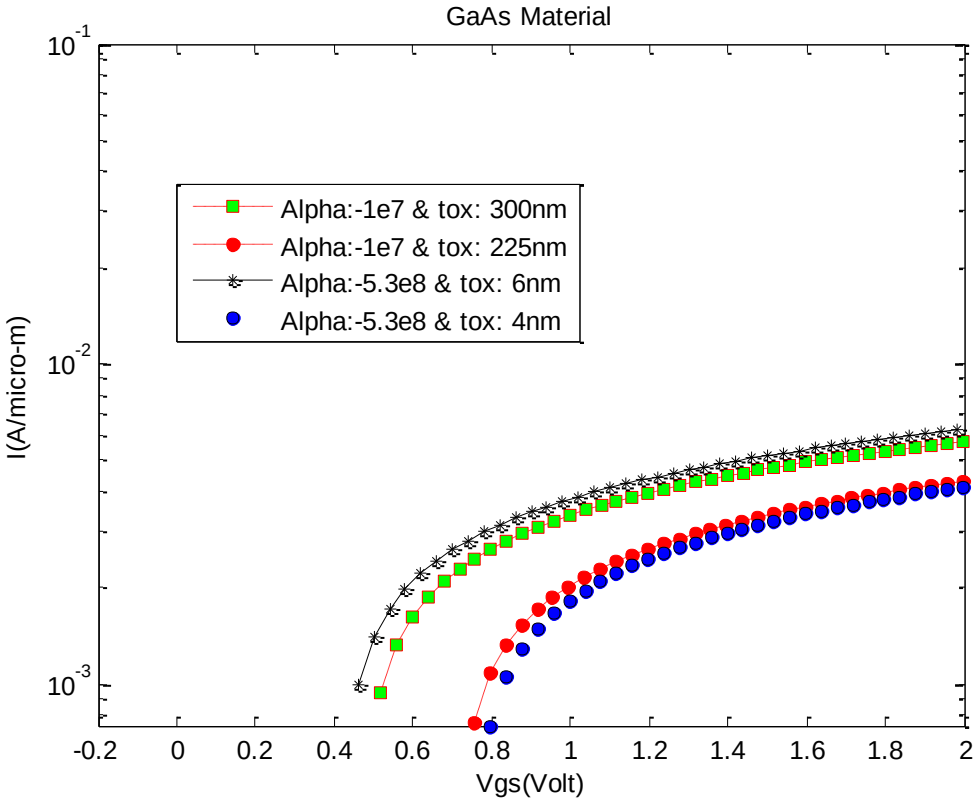


Figure 4.3: Impact of varying the ferroelectric material on the I-V_{gs} transfer characteristics for the DG Fe-TFET with fixed gate length, L_g = 24 nm and also varying the ferroelectric oxide thickness for different consideration in case of GaAs Material.

Table 1.4: Values of V_{onset}, Biasing V_g, I_{ON} for different ferroelectric materials (anisotropy constant α) at certain oxide thickness (t_{ox}) in case of Si Material

Material Si	Ferroelectric Material	α (m/F)	t_{ox} (nm)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)
E_g = 1.1 eV ϵ_r = 11.8 C_s = 0.1 F/m^2	$BaTiO_3$	-1×10^7	300	0.4400	0.666	0.0232
			225	0.6050	0.834	0.0208
	$SrTiO_3$	-5.3×10^8	8	0.1672	0.391	0.034
			4	0.6336	0.885	0.0202

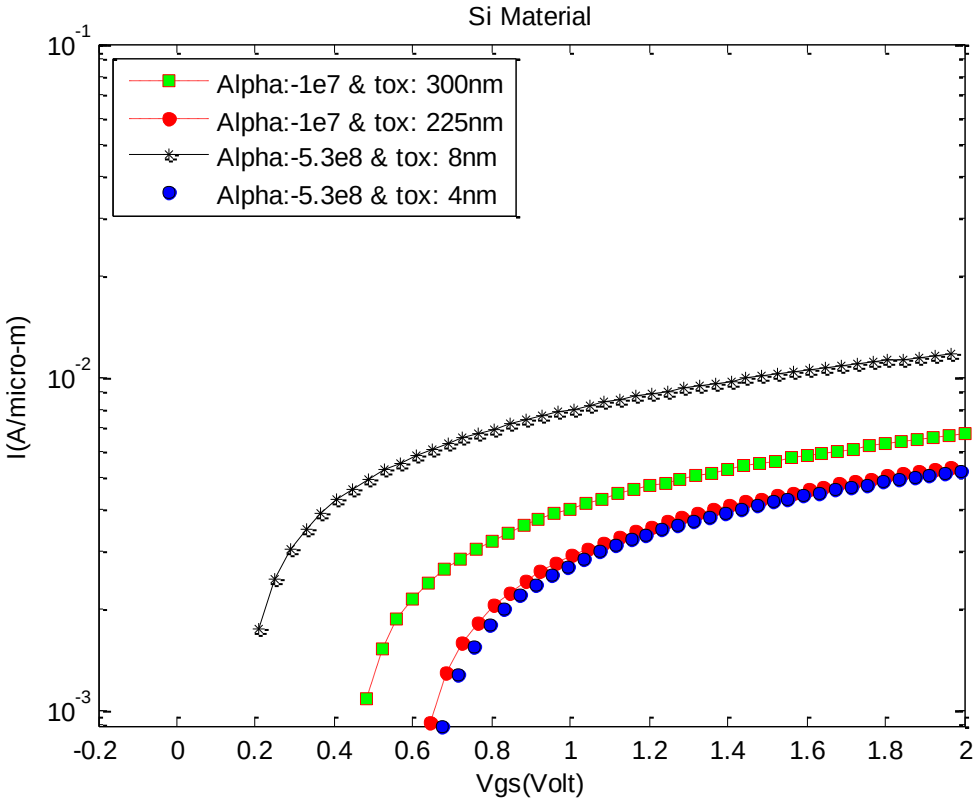


Figure 4.4: Impact of varying the ferroelectric material on the I-V_{gs} transfer characteristics for the DG Fe-TFET with fixed gate length, L_g = 24 nm and also varying the ferroelectric oxide thickness for different consideration in case of Si Material.

Table 1.5: Values of V_{onset}, Biasing V_g, I_{ON} for different ferroelectric materials (anisotropy constant α) at certain oxide thickness (t_{ox}) in case of Ge Material

Material Ge	Ferroelectric Material	α (m/F)	t_{ox} (nm)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)
E_g = 0.66 eV ϵ_r = 16 C_s = 0.1356 F/m^2	$BaTiO_3$	-1×10^7	300	0.1230	0.432	0.03176
			225	0.2573	0.5384	0.023
	$SrTiO_3$	-5.3×10^8	6	0.0908	0.325	0.0326
			4	0.2805	0.589	0.023

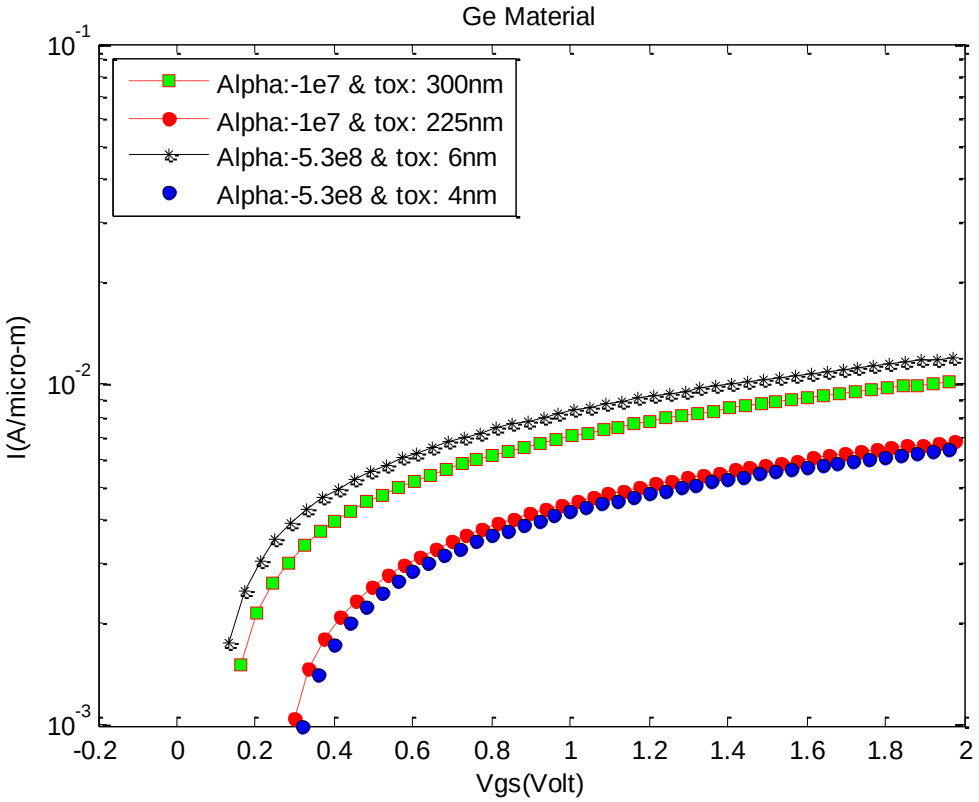


Figure 4.5: Impact of varying the ferroelectric material on the I-V_{gs} transfer characteristics for the DG Fe-TFET with fixed gate length, L_g = 24 nm and also varying the ferroelectric oxide thickness for different consideration in case of Ge Material.

Table 1.6: Values of V_{onset}, Biasing V_g, I_{ON} for different ferroelectric materials (anisotropy constant α) at certain oxide thickness (t_{ox}) in case of InAs Material

Material InAs	Ferroelectric Material	α (m/F)	t_{ox} (nm)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)
E_g = 0.36 eV ϵ_r = 14.6 C_s = 0.1237 F/m^2	$BaTiO_3$	-1×10^7	300	0.0928	0.411	0.03147
			225	0.1596	0.477	0.0262
	$SrTiO_3$	-5.3×10^8	6	0.0768	0.345	0.0324
			4	0.1712	0.528	0.0256

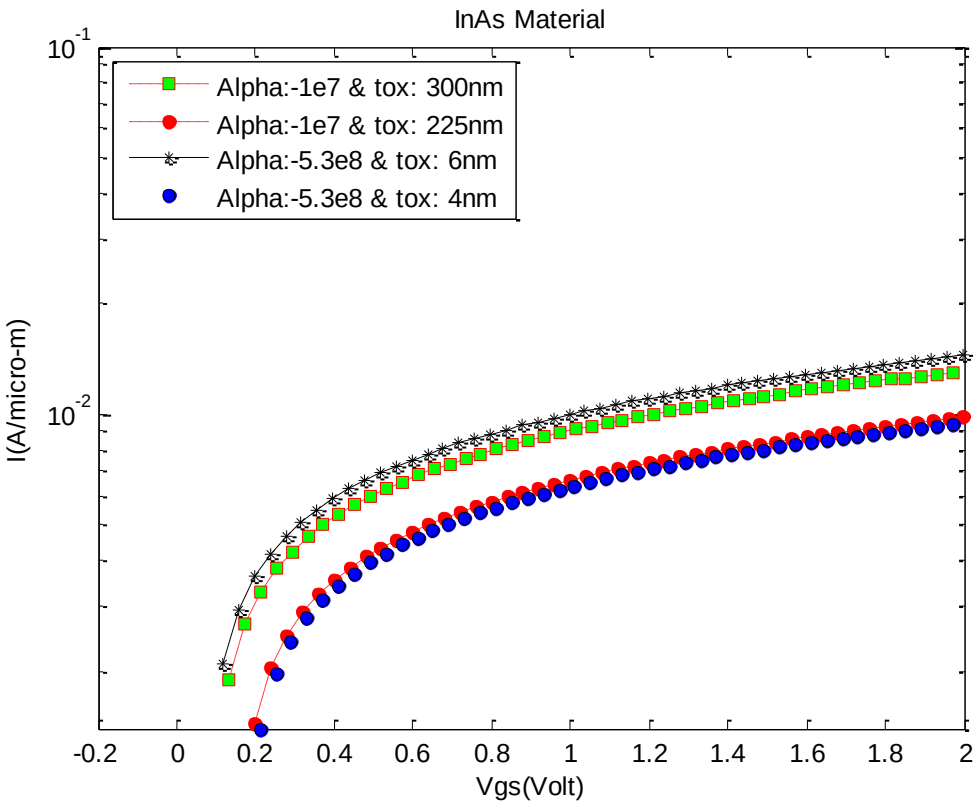


Figure 4.6: Impact of varying the ferroelectric material on the I-V_{gs} transfer characteristics for the DG Fe-TFET with fixed gate length, L_g = 24 nm and also varying the ferroelectric oxide thickness for different consideration in case of InAs Material.

4.4 Impact of Oxide thickness

The oxide thickness has huge impact on the ON-current while its influence on the onset voltage is straightforward. A larger oxide thickness reduces the onset voltage. A large oxide thickness is required to enable the gate to adequately control the source region and it will therefore improve the validity of the approximations.

Capacitive coupling between the gate and channel is a critical parameter for highly-scaled conventional MOSFETs, so oxide thickness variations have been a major focus of studies on parameter fluctuations for this type of device. TFETs are even more sensitive to changes in gate capacitance than conventional MOSFETs, thus it is no surprise that changes in dielectric permittivity and thickness can cause major fluctuations in traditional TFET characteristics. But here we introduce the ferroelectric

material instead of SiO_2 or the high k dielectric oxide. Normally in case of conventional MOSFET and the semi classical TFET, oxide thickness is needed to small as possible to enhancement of the value of capacitance, thus to boost up the tunneling current but there arises the gate leakage at the OFF state of the device. So, it is the fundamental problem of the FET devices. But, here it is a very interesting phenomenon that the ferroelectric oxide thickness is needed to make large to ensure the enhancement of charge storage capacity of ferroelectric material which acts as an auto transformer to increase the ON current at a low supply voltage. Thus ensure the low power dissipation and operate at a very low operating voltage.

The I-V_{gs} of an optimized Double Gate Ferroelectric TFET with varying oxide thickness is shown in Figure. ON-current and Subthreshold Slope are clearly both very sensitive to changes in the oxide thickness with a certain ferroelectric material as oxide.

The variation of the oxide thickness has a drastic influence on all characteristics, especially when changing from a relatively low oxide thickness. For example, when changing from 300nm to 440nm, threshold voltage changing from 0.4776V to 0.0332V and the ON-current goes up from 0.0153 A/μm to 0.0465 A/μm.

Fe-TFETs show high sensitivity to changes in gate dielectric thickness. The gate leakage increases exponentially as the oxide thickness is reduced. This limits the downscaling thickness to about 3.4 nm to 3.5 nm. But to further decrease the effective oxide thickness alternative high dielectric constant material can be used at a limited range. On the other hand, a thick gate oxide of ferroelectric material reduces the leakage current and improves the driving capabilities of a MOS transistor. However a trade off between this benefits and gate leakage is necessary. So optimize value of gate dielectric thickness of ferroelectric material have to choose which will show maximized value of ON-current and limits the gate leakage for this value of thickness.

Table 1.71: Values of V_{onset}, Biasing V_g, I_{ON} for different thickness (t_{ox}) of ferroelectric oxide, $BaTiO_3$ in case of GaAs Material

GaAs Material	t_{ox} (nm)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)
E_g = 1.43 eV ϵ_r = 13.1 C_s = 0.111 F/m^2	440	0.0332	0.228	0.0465
	400	0.1602	0.342	0.0285
	350	0.3189	0.478	0.0197
	300	0.4776	0.64	0.0153

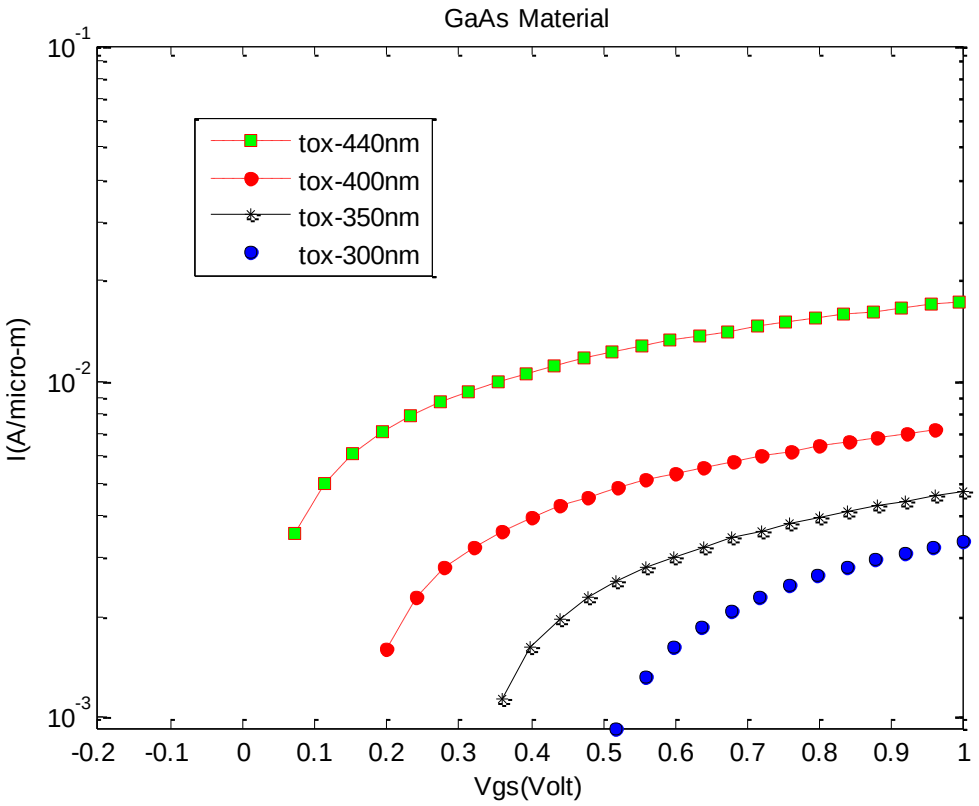


Figure 4.71: Transfer characteristics of showing the impact of varying the thickness of ferroelectric oxide, $BaTiO_3$ on I-V_{gs} curve of DG Fe-TFET in case of GaAs Material with Source Doping Concentration, Na=10^{25} m^{-3}

Table 1.72: Values of V_{onset}, Biasing V_g, I_{ON} for different thickness (t_{ox}) of ferroelectric oxide, $SrTiO_3$ in case of GaAs Material

GaAs Material	t_{ox} (nm)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)
E_g = 1.43 eV ϵ_r = 13.1 C_s = 0.111 F/m^2	8	0.0840	0.2685	0.03941
	7	0.2522	0.4111	0.02559
	6	0.4205	0.6046	0.022
	4	0.7570	0.92	0.015

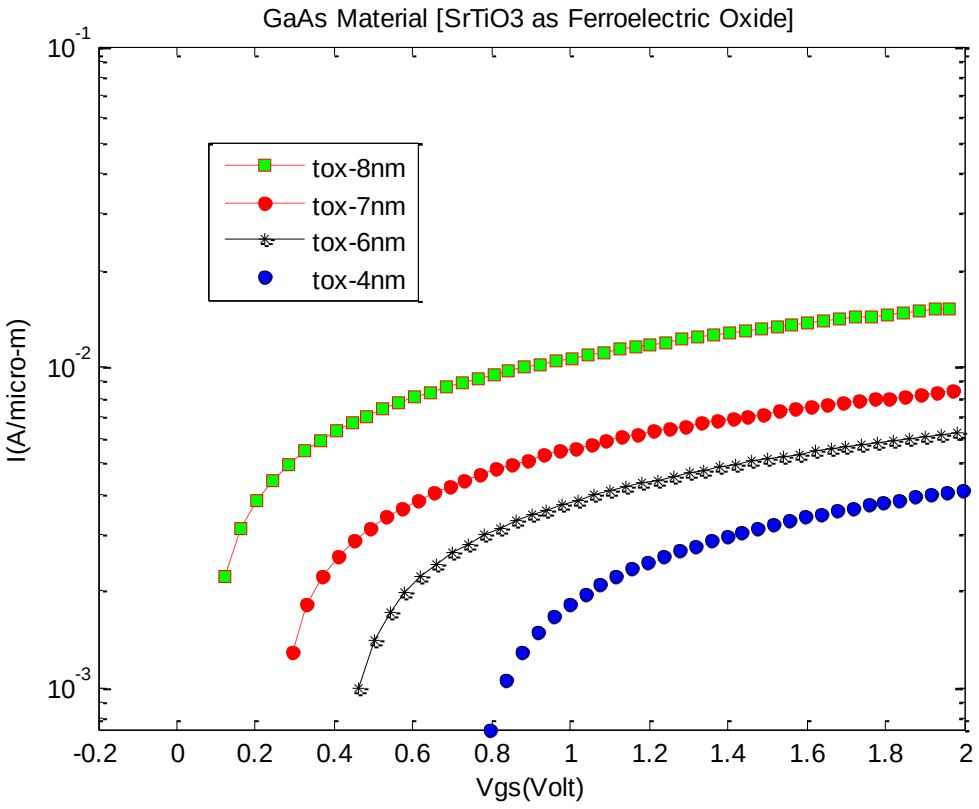


Figure 4.72: Transfer characteristics of showing the impact of varying the thickness of ferroelectric oxide, $SrTiO_3$ on I-V_{gs} curve of DG Fe-TFET in case of GaAs Material with Source Doping Concentration, Na=10^{25} m^{-3}

Table 1.81: Values of V_{onset}, Biasing V_g, I_{ON} for different thickness (t_{ox}) of ferroelectric oxide, $BaTiO_3$ in case of Si Material

Si Material	t_{ox} (nm)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)
E_g = 1.1 eV ϵ_r = 11.8 C_s = 0.1 F/m^2	440	0.1320	0.2905	0.0274
	400	0.2200	0.385	0.02176
	350	0.3300	0.48	0.017
	300	0.4400	0.5787	0.01176

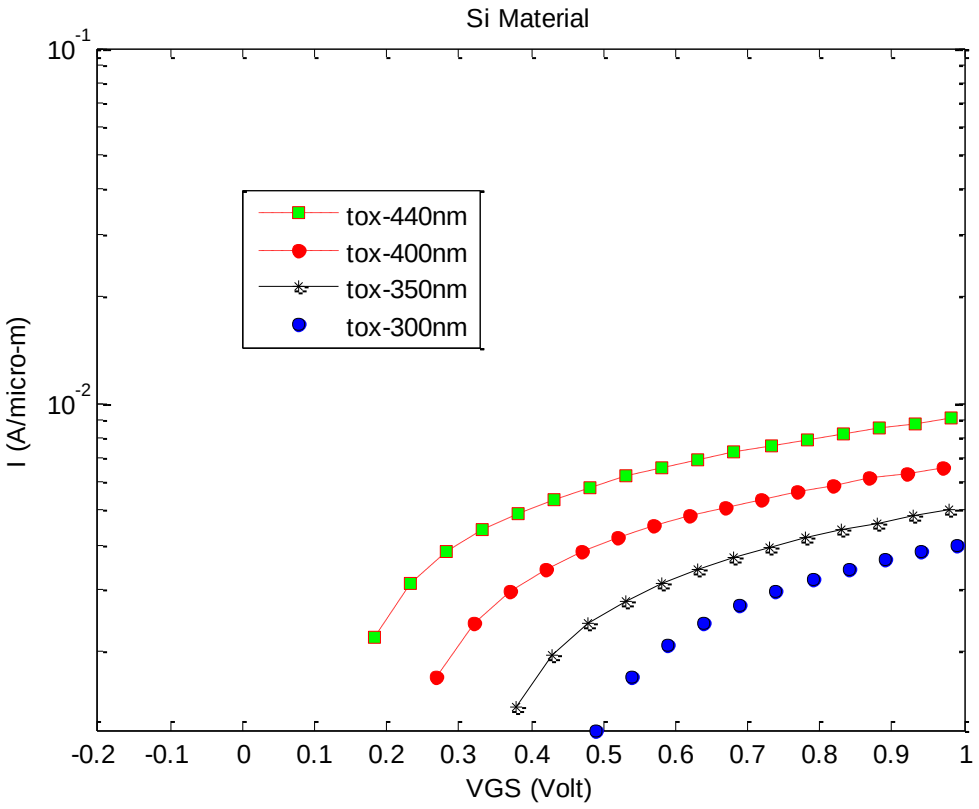


Figure 4.81: Transfer characteristics of showing the impact of varying the thickness of ferroelectric oxide, $BaTiO_3$ on I-V_{gs} curve of DG Fe-TFET in case of Si Material with Source Doping Concentration, Na=10^{25} m^{-3}

Table 1.82: Values of V_{onset}, Biasing V_g, I_{ON} for different thickness (t_{ox}) of ferroelectric oxide, $SrTiO_3$ in case of Si Material

Si Material	t_{ox} (nm)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)
E_g = 1.1 eV ϵ_r = 11.8 C_s = 0.1 F/m^2	8	0.1672	0.3551	0.03382
	6	0.4004	0.569	0.02382
	4	0.6336	0.798	0.01882
	2	0.8668	1.012	0.01412

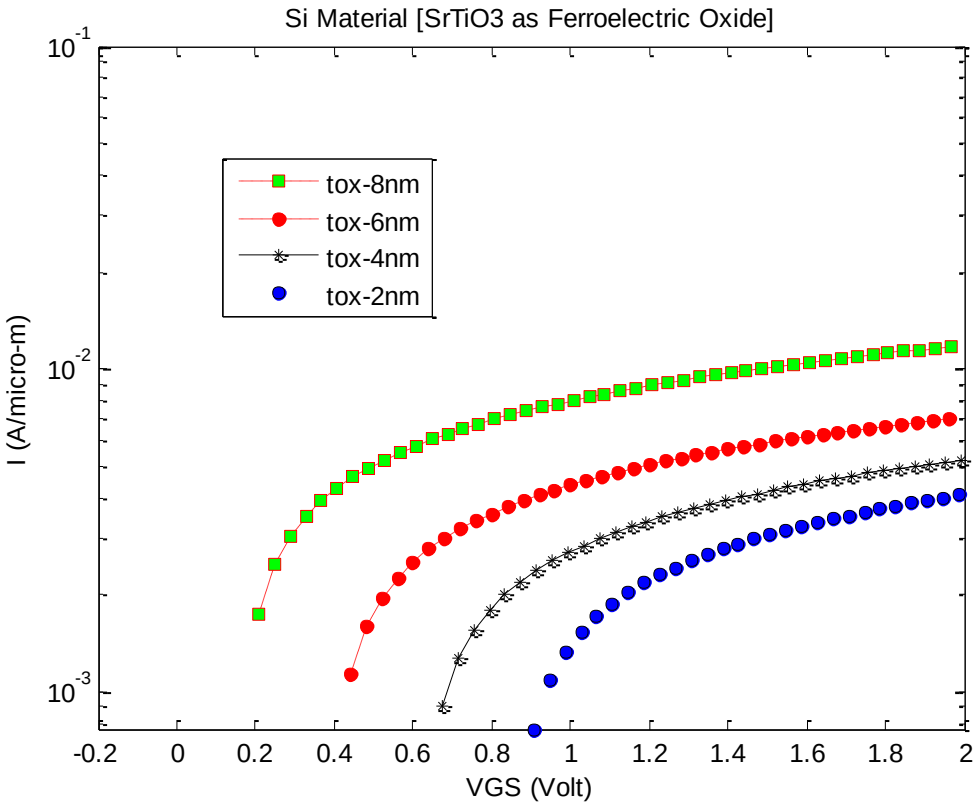


Figure 4.82: Transfer characteristics of showing the impact of varying the thickness of ferroelectric oxide, $SrTiO_3$ on I-V_{gs} curve of DG Fe-TFET in case of Si Material with Source Doping Concentration, Na=10^{25} m^{-3}

Table 1.91: Values of V_{onset}, Biasing V_g, I_{ON} for different thickness (t_{ox}) of ferroelectric oxide, $BaTiO_3$ in case of Ge Material

Ge Material	t_{ox} (nm)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)
E_g = 0.66 eV ϵ_r = 16 C_s = 0.1356 F/m^2	350	0.0335	0.1722	0.0375
	300	0.1230	0.286	0.0252
	225	0.2573	0.397	0.0155
	200	0.3020	0.4388	0.01378

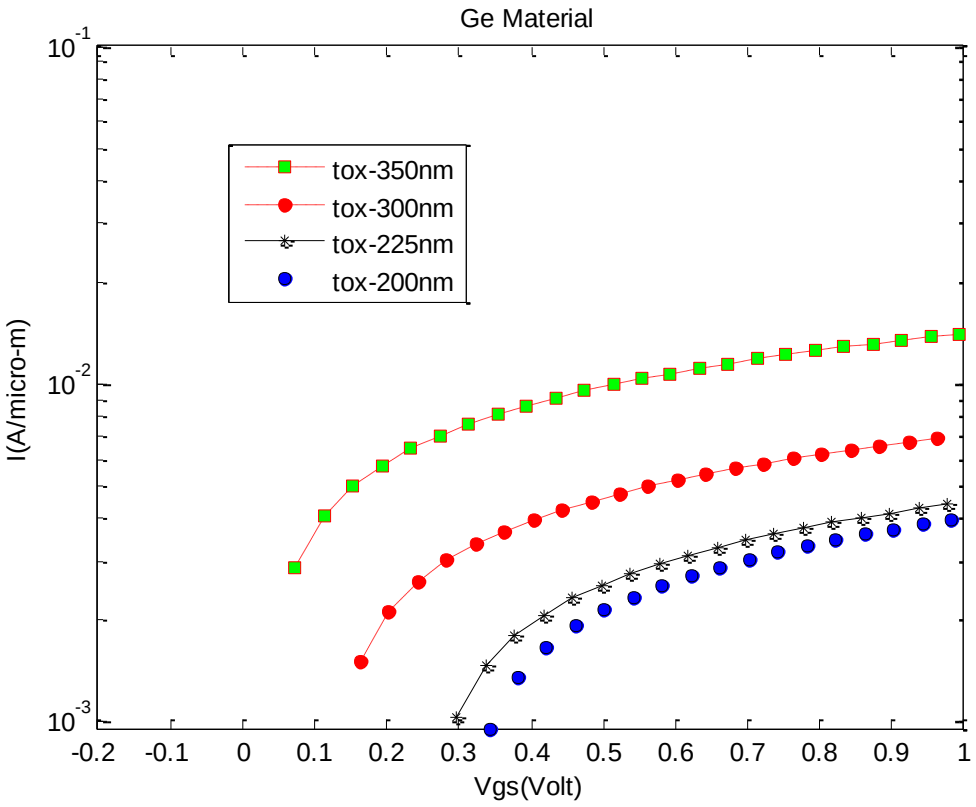


Figure 4.91: Transfer characteristics of showing the impact of varying the thickness of ferroelectric oxide, $BaTiO_3$ on I-V_{gs} curve of DG Fe-TFET in case of Ge Material with Source Doping Concentration, Na=10^{25} m^{-3}

Table 1.92: Values of V_{onset}, Biasing V_g, I_{ON} for different thickness (t_{ox}) of ferroelectric oxide, $SrTiO_3$ in case of Ge Material

Ge Material	t_{ox} (nm)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)
E_g = 0.66 eV ϵ_r = 16 C_s = 0.1356 F/m^2	6	0.0908	0.2634	0.03324
	5	0.1857	0.3653	0.02559
	4	0.2805	0.4569	0.02118
	2	0.4703	0.64	0.01618

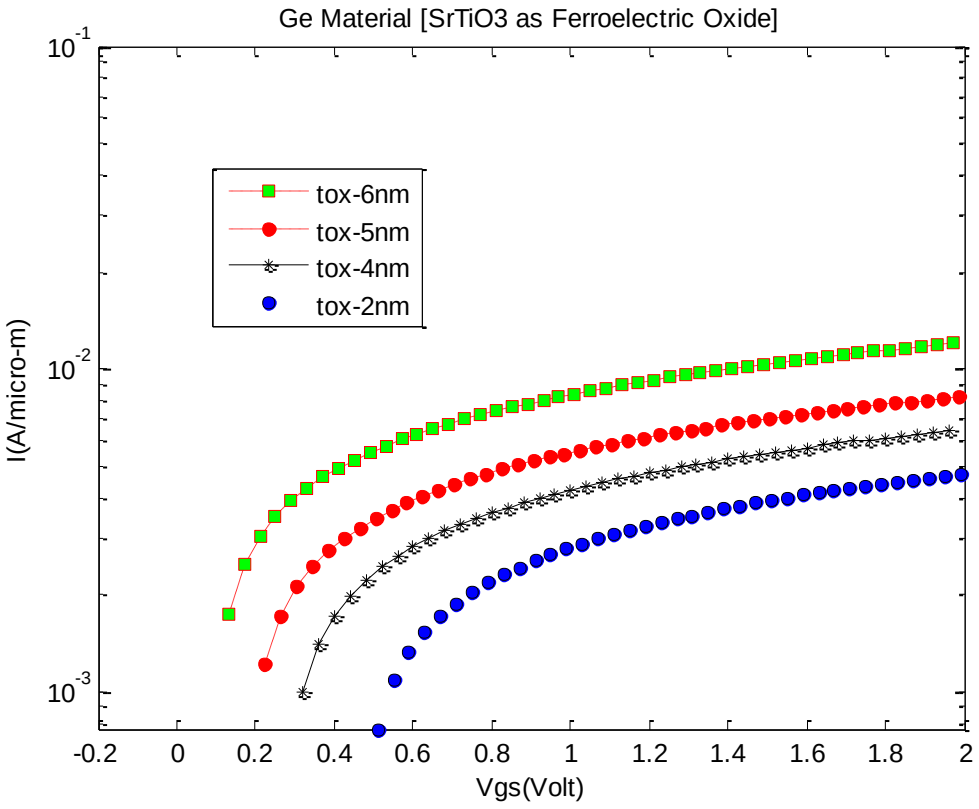


Figure 4.92: Transfer characteristics of showing the impact of varying the thickness of ferroelectric oxide, $SrTiO_3$ on I-V_{gs} curve of DG Fe-TFET in case of Ge Material with Source Doping Concentration, Na=10^{25} m^{-3}

Table 1.101: Values of V_{onset}, Biasing V_g, I_{ON} for different thickness (t_{ox}) of ferroelectric oxide, $BaTiO_3$ in case of InAs Material

InAs Material	t_{ox} (nm)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)
E_g = 0.36 eV ϵ_r = 14.6 C_s = 0.1237 F/m^2	400	0.0037	0.16388	0.06176
	350	0.0483	0.2055	0.030588
	300	0.0928	0.258	0.02382
	225	0.1596	0.3277	0.01764

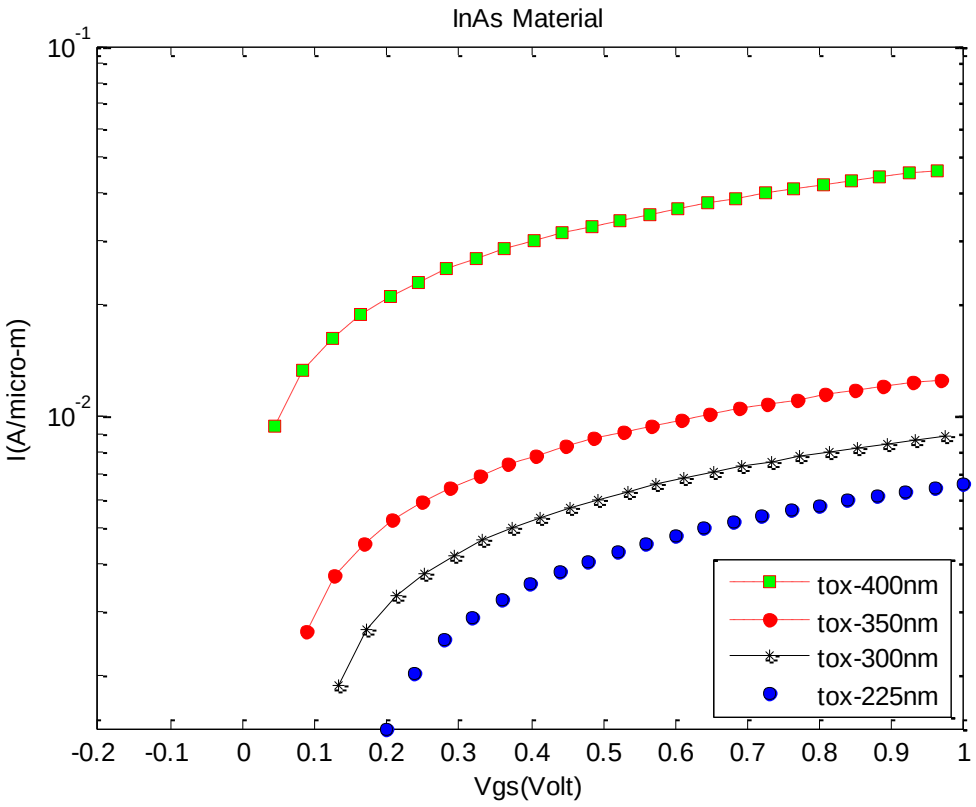


Figure 4.101: Transfer characteristics of showing the impact of varying the thickness of ferroelectric oxide, $BaTiO_3$ on I-V_{gs} curve of DG Fe-TFET in case of InAs Material with Source Doping Concentration, Na=10^{25} m^{-3}

Table 1.102: Values of V_{onset}, Biasing V_g, I_{ON} for different thickness (t_{ox}) of ferroelectric oxide, $SrTiO_3$ in case of InAs Material

InAs Material	t_{ox} (nm)	V_{onset} or V_{Th} (V)	Biasing V_g (V)	I_{ON} (A/μm)
E_g = 0.36 eV ϵ_r = 14.6 C_s = 0.1237 F/m^2	6	0.0768	0.2638	0.03206
	5	0.1240	0.325	0.02676
	4	0.1712	0.342	0.02206
	2	0.2656	0.4388	0.01676

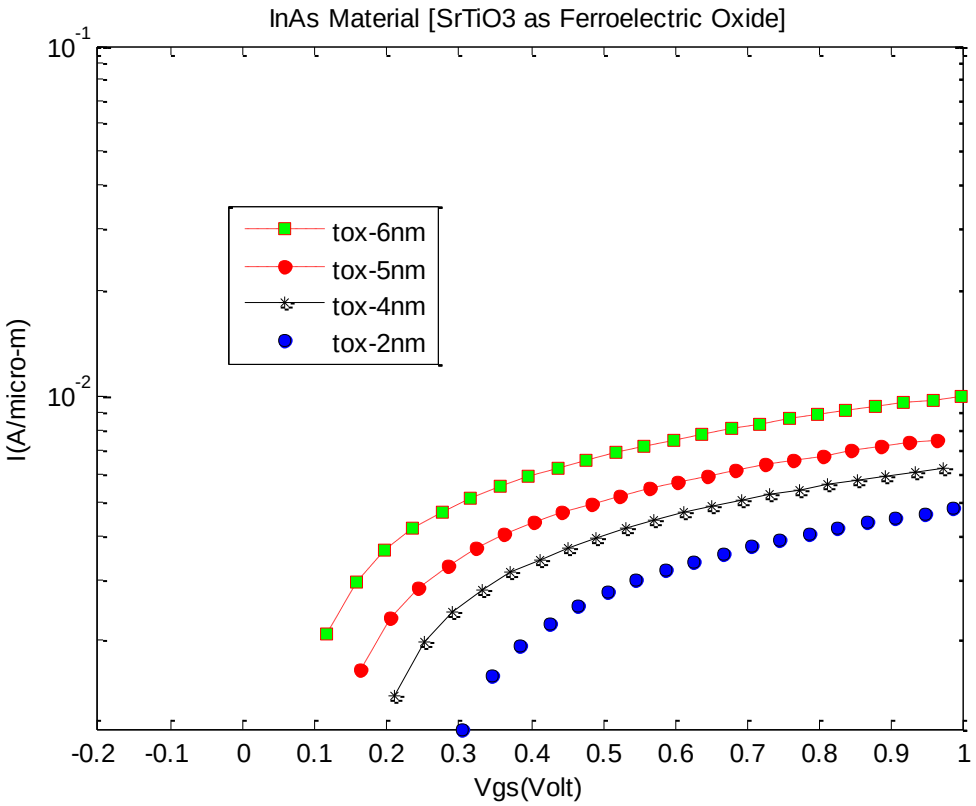


Figure 4.102: Transfer characteristics of showing the impact of varying the thickness of ferroelectric oxide, $SrTiO_3$ on I-V_{gs} curve of DG Fe-TFET in case of InAs Material with Source Doping Concentration, Na=10^{25} m^{-3}

Although it may look as if the fluctuations become less extreme with decreasing t_{ox}, this is because we are looking at units that have not been normalized to the I_{ON} or the V_{th} or not to choose the appropriate ferroelectric material. If we look at fluctuations as percentages, they are significant everywhere in the studied range of dielectric thickness.

4.5 Impact of Source Doping Concentration

A higher doping level of the source increases the ON-current. This can be understood by realizing that the doping level determines the curvature of the potential in the depletion region. A larger doping level will thus decrease the tunnel distance and increase the current. An upper limit on the onset voltage or on the voltage drop over the oxide will limit the doping level.

We now see the impact of varying the source doping concentration on the gate dielectric dependence of the device performance. The device structure with L_g = 24 nm for two different values of the source doping concentration as 1×10^{20} and 2×10^{20} atoms/cm^3. For each of the source doping concentrations, the transfer characteristic is plotted in Figure 4.11 to Figure 4.18 for different thickness of the gate oxide corresponding to $BaTiO_3$. An increase in the source doping concentration results in corresponding improvement in the device performance, as expected. This is simply due to the fact that a relatively higher source doping not only causes more band lowering of the tunnel destination but it also reduces the source depletion and, hence, less depletion width. As a result, the minimum value of the tunnel width is reduced, and the maximum electric field is increased across the tunneling junction. It is, however, interesting to note that, in Figure 4.11 to Figure 4.18. a relatively lower source doping reduces the gate oxide dependence of the device performance, which is in contrast with that intuitively expected. This can be attributed to the combined influence of the following two: First, a decrease in the source doping concentration results in corresponding shift in the location of the tunneling junction toward the source, which is due to larger source depletion for lower source doping. Second, a larger impact of the fringing field arising out of the gate dielectric is observed at the gate edge than the rest of the device. As a result, for a device with higher source doping, the impact of the fringing field across the tunneling junction will be exhibited to be much larger on the tunnel destination, compared with that on the tunnel source. This, in turn, results in significant widening of the tunnel width, thereby degrading the device performance drastically. In contrast, due to a shift in the location of the tunneling junction toward the source for a device with lower source doping, the impact of the fringing field on the tunnel source partly compensates its impact on the tunnel destination. As a result, the gate ferroelectric oxide dependence of the device

characteristics is somewhat reduced when a relatively lower source doping concentration is used.

Table 1.11: Values of I_{ON}, V_{onset}, Biasing V_g for different source doping concentration (N_a) at certain oxide thickness (t_{ox}) in case of GaAs Material

GaAs Material	t_{ox} (nm)	N_a (m^{-3})	I_{ON} (A/μm)	V_{onset} (V)	Biasing V_g (V)
E_g = 1.43 eV ϵ_r = 13.1 C_s = 0.111 F/m^2	350	1×10^{25}	0.05353	0.3189	0.45
		2×10^{25}	0.04353		
		1×10^{26}	0.02		
		2×10^{26}	0.01		
	300	1×10^{25}	0.0535	0.4776	0.73
		2×10^{25}	0.044		
		1×10^{26}	0.02		
		2×10^{26}	0.01		

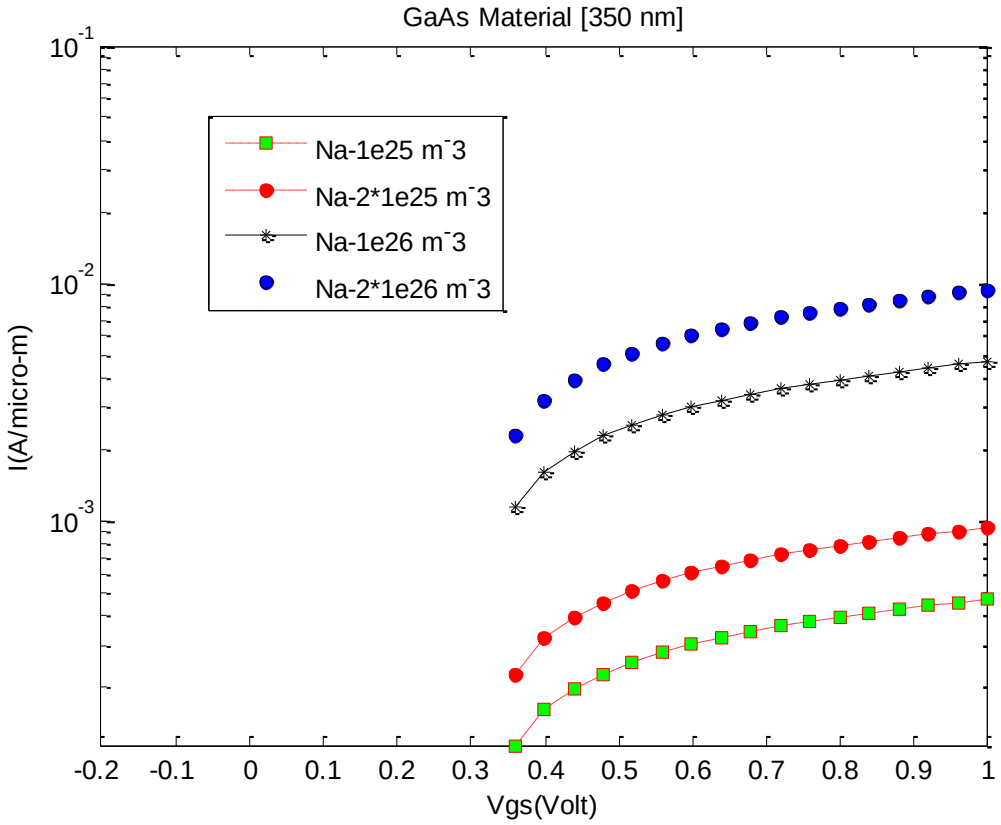


Figure 4.11: Transfer characteristics of showing the impact of varying the source doping concentration on I-V_{gs} curve of DG Fe-TFET in case of GaAs Material with ferroelectric oxide thickness, t_{ox} =350 nm

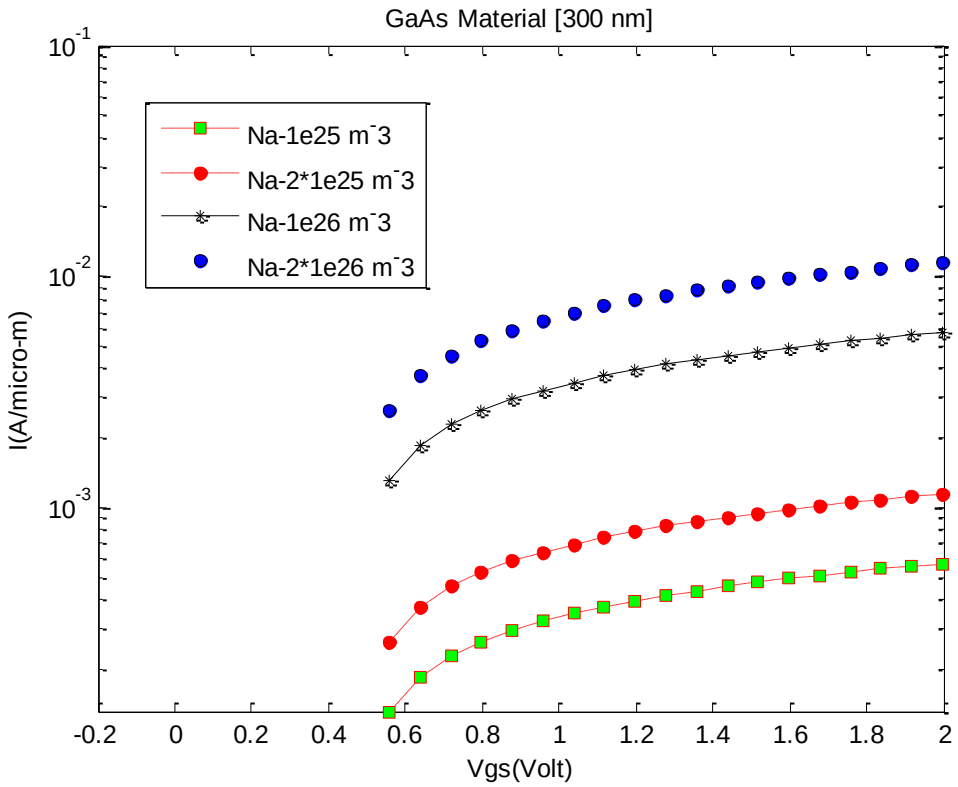


Figure 4.12: Transfer characteristics of showing the impact of varying the source doping concentration on I-V_{gs} curve of DG Fe-TFET in case of GaAs Material with ferroelectric oxide thickness, t_{ox} =300 nm

Table 1.12: Values of I_{ON}, V_{onset}, Biasing V_g for different source doping concentration (N_a) at certain oxide thickness (t_{ox}) in case of Si Material

Si Material	t_{ox} (nm)	N_a (m^{-3})	I_{ON} (A/μm)	V_{onset} (V)	Biasing V_g (V)
E_g = 1.1 eV ϵ_r = 11.8 C_s = 0.1 F/m^2	350	1×10^{25}	0.05382	0.3300	0.45
		2×10^{25}	0.0438		
		1×10^{26}	0.0188		
		2×10^{26}	0.01		
	300	1×10^{25}	0.0521	0.4400	0.56
		2×10^{25}	0.0428		
		1×10^{26}	0.0194		
		2×10^{26}	0.0088		

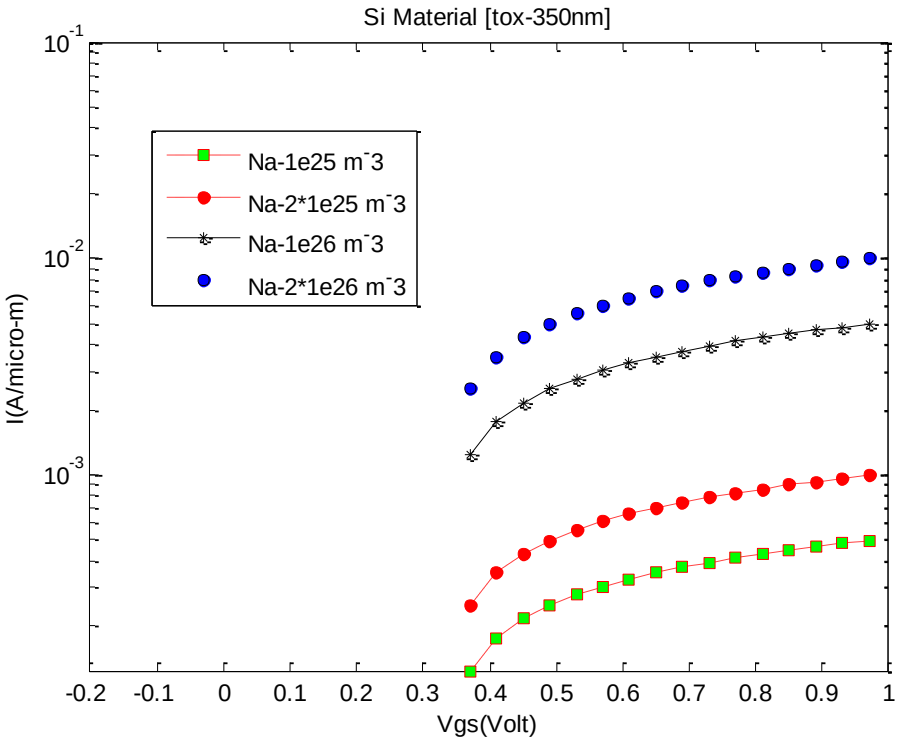


Figure 4.13: Transfer characteristics of showing the impact of varying the source doping concentration on I-V_{gs} curve of DG Fe-TFET in case of Si Material with ferroelectric oxide thickness, t_{ox} =350 nm

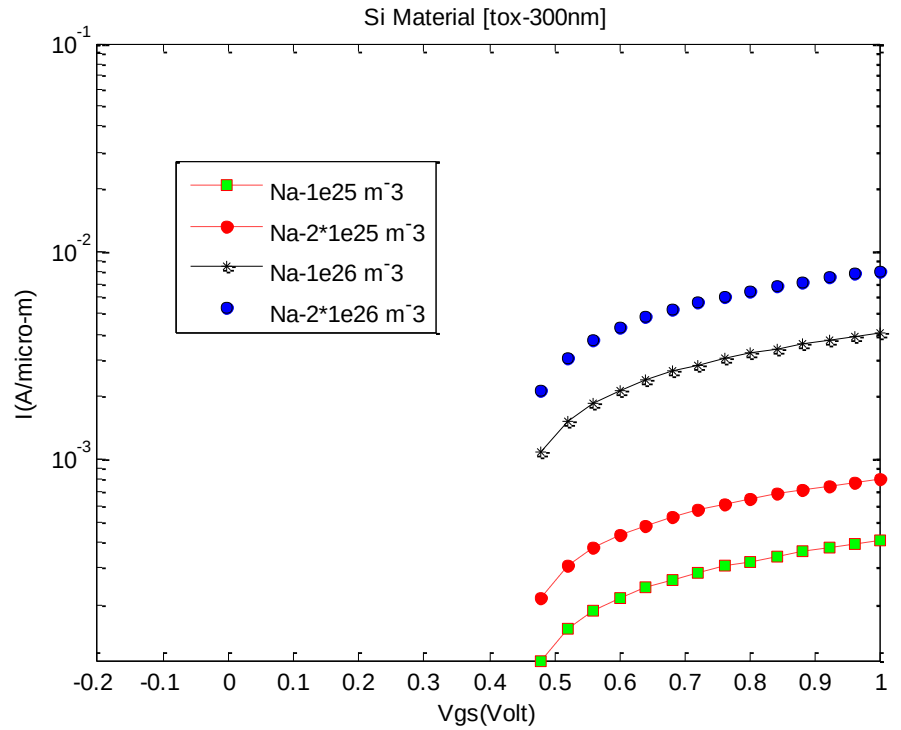


Figure 4.14: Transfer characteristics of showing the impact of varying the source doping concentration on I-V_{gs} curve of DG Fe-TFET in case of Si Material with ferroelectric oxide thickness, t_{ox} =300 nm

Table 1.13: Values of I_{ON}, V_{onset}, Biasing V_g for different source doping concentration (N_a) at certain oxide thickness (t_{ox}) in case of Ge Material

Ge Material	t_{ox} (nm)	N_a (m^{-3})	I_{ON} (A/μm)	V_{onset} (V)	Biasing V_g (V)
E_g = 0.66 eV ϵ_r = 16 C_s = 0.1356 F/m^2	300	1×10^{25}	0.05618	0.1230	0.26
		2×10^{25}	0.04588		
		1×10^{26}	0.02088		
		2×10^{26}	0.01		
	225	1×10^{25}	0.05323	0.2573	0.39
		2×10^{25}	0.04294		
		1×10^{26}	0.02		
		2×10^{26}	0.01		

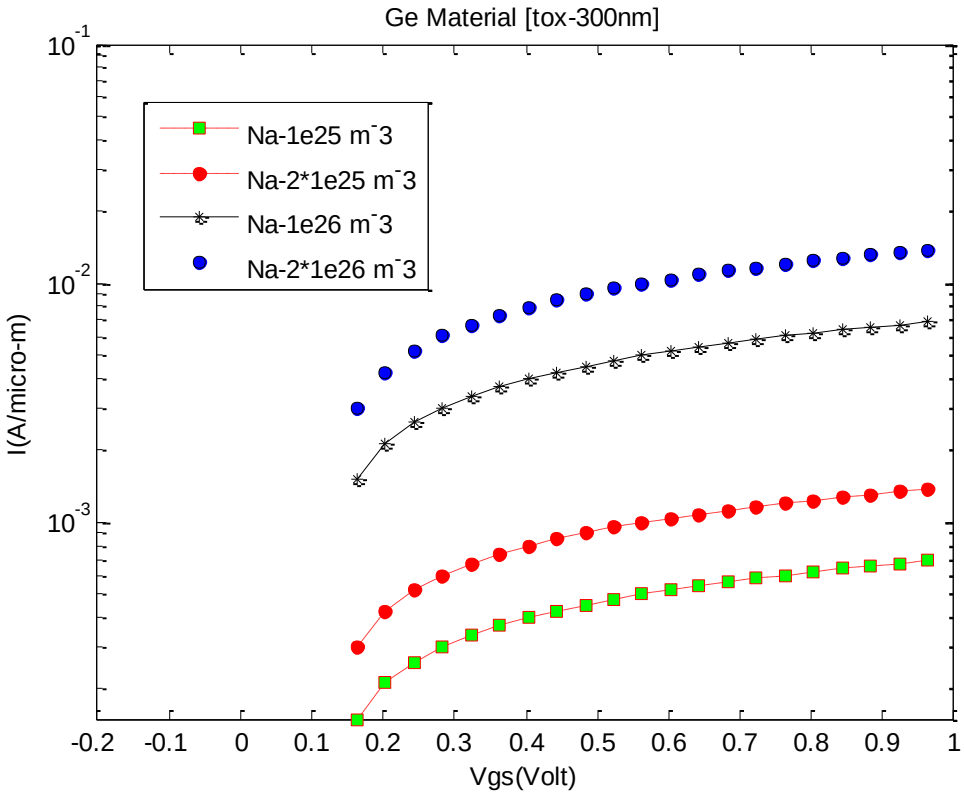


Figure 4.15: Transfer characteristics of showing the impact of varying the source doping concentration on I-V_{gs} curve of DG Fe-TFET in case of Ge Material with ferroelectric oxide thickness, t_{ox} =300 nm

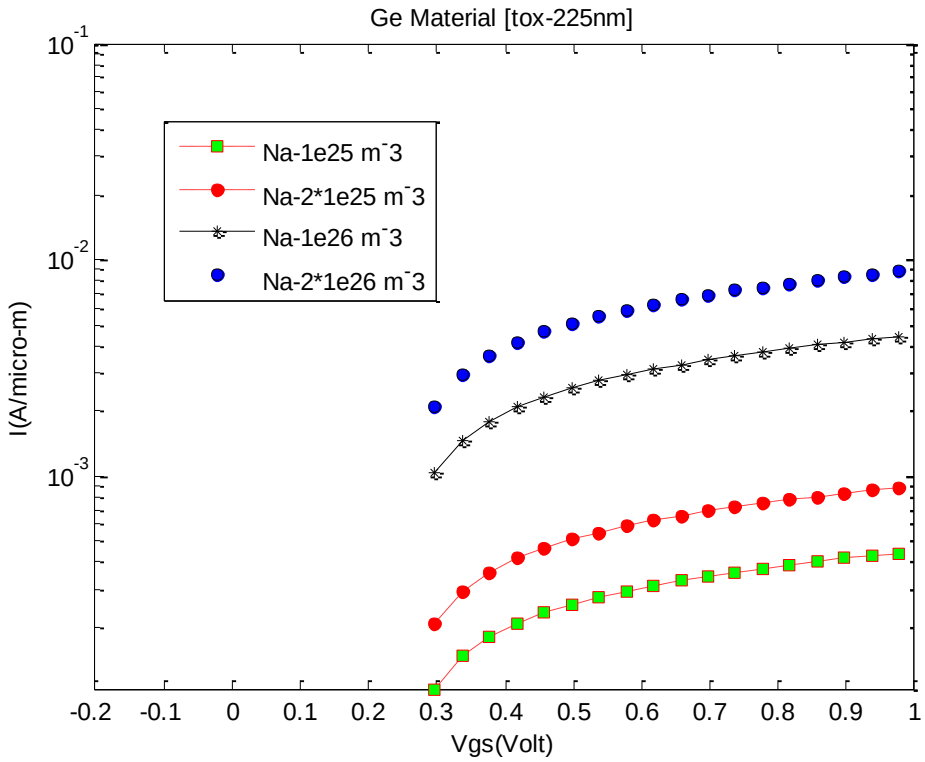


Figure 4.16: Transfer characteristics of showing the impact of varying the source doping concentration on I-V_{gs} curve of DG Fe-TFET in case of Ge Material with ferroelectric oxide thickness, t_{ox} =225 nm

Table 1.14: Values of I_{ON}, V_{onset} and Biasing V_g for different source doping concentration (N_a) at certain oxide thickness (t_{ox}) in case of InAs Material

InAs Material	t_{ox} (nm)	N_a (m^{-3})	I_{ON} (A/μm)	V_{onset} (V)	Biasing V_g (V)
E_g = 0.36 eV ϵ_r = 14.6 C_s = 0.1237 F/m^2	300	1×10^{25}	0.05735	0.0928	0.226
		2×10^{25}	0.0467		
		1×10^{26}	0.02		
		2×10^{26}	0.01		
	225	1×10^{25}	0.0553	0.1596	0.29
		2×10^{25}	0.0444		
		1×10^{26}	0.02		
		2×10^{26}	0.01		

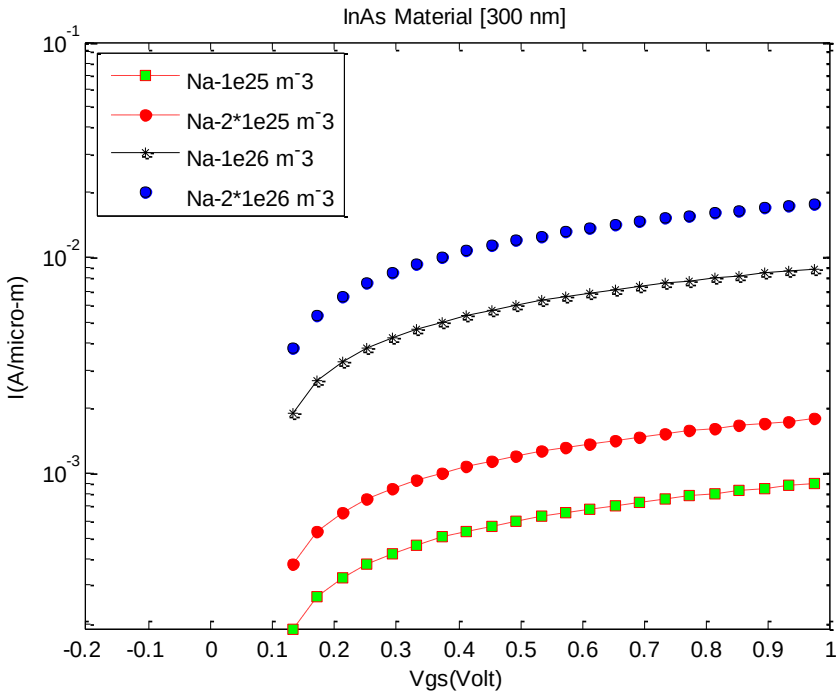


Figure 4.17: Transfer characteristics of showing the impact of varying the source doping concentration on I-V_{gs} curve of DG Fe-TFET in case of InAs Material with ferroelectric oxide thickness, t_{ox} =300 nm

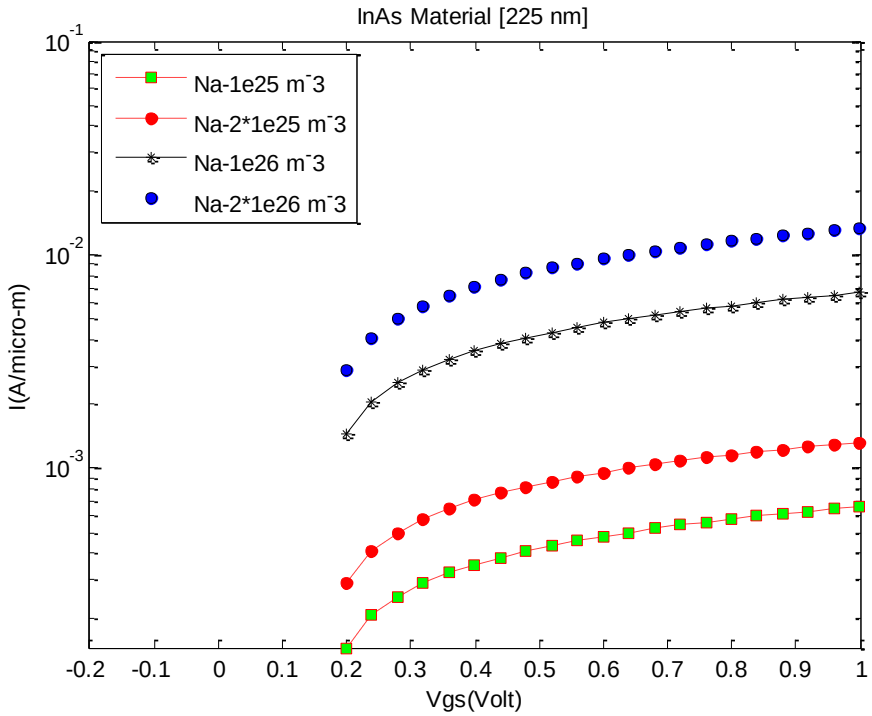


Figure 4.18: Transfer characteristics of showing the impact of varying the source doping concentration on I-V_{gs} curve of DG Fe-TFET in case of InAs Material with ferroelectric oxide thickness, t_{ox} =225 nm

4.6 Impact of Gate Length

Gate alignment is another important booster, and there have been recommendations to align the gate oxide with the tunnel junction in order to take advantage of fringing and to shorten the gate on the source end in order to increase device speed. It is important to understand how such design choices would influence the magnitude of characteristic fluctuations. Here, we present a detailed investigation of gate alignment. Gate on source region demonstrates low fringing field effect [44-47], thus the gate controlling on ON current shows a significant improvement than the conventional MOSFET as well as semi classical TFET.

Figure 4.19 to Figure 4.26 shows that the alignment of the gate oxide has a large influence on characteristics and one that is not necessarily intuitive at first glance. For a gate with large gate length ensures the improvements in ON-current, threshold voltage and swing. But gate length is needed to maintain at a desired and well accepted range. The aligned gate on source region has better characteristics in the important low-voltage region, critical for low-power devices.

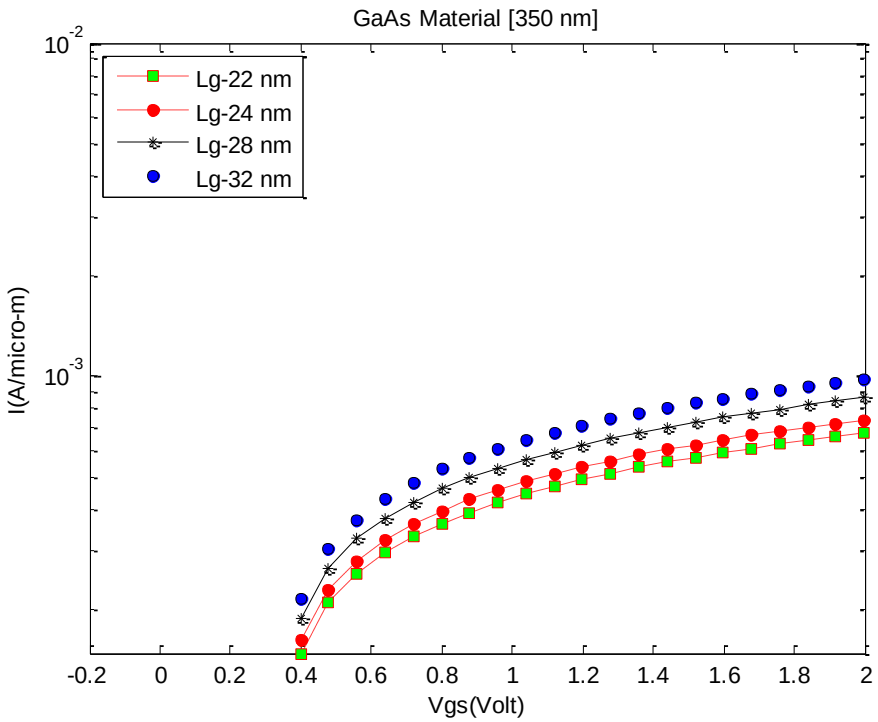


Figure 4.19: Impact of varying gate length (L_g) on I-V_{gs} Curve for the DG Fe-TFET in case of GaAs Material with ferroelectric oxide thickness, t_{ox} = 350 nm

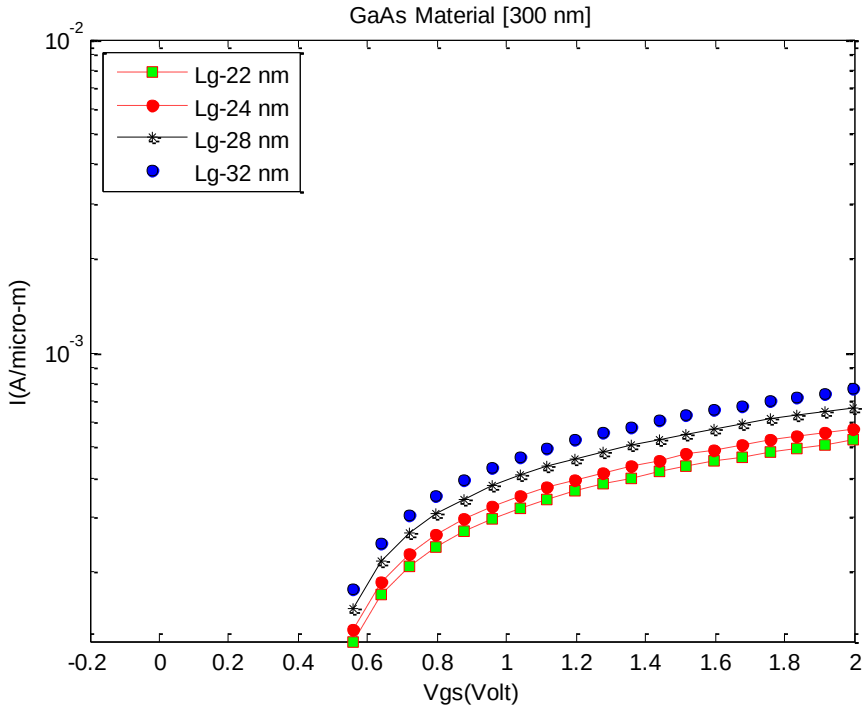


Figure 4.20: Impact of varying gate length (L_g) on I-V_{gs} Curve for the DG Fe-TFET in case of GaAs Material with ferroelectric oxide thickness, t_{ox} = 300 nm

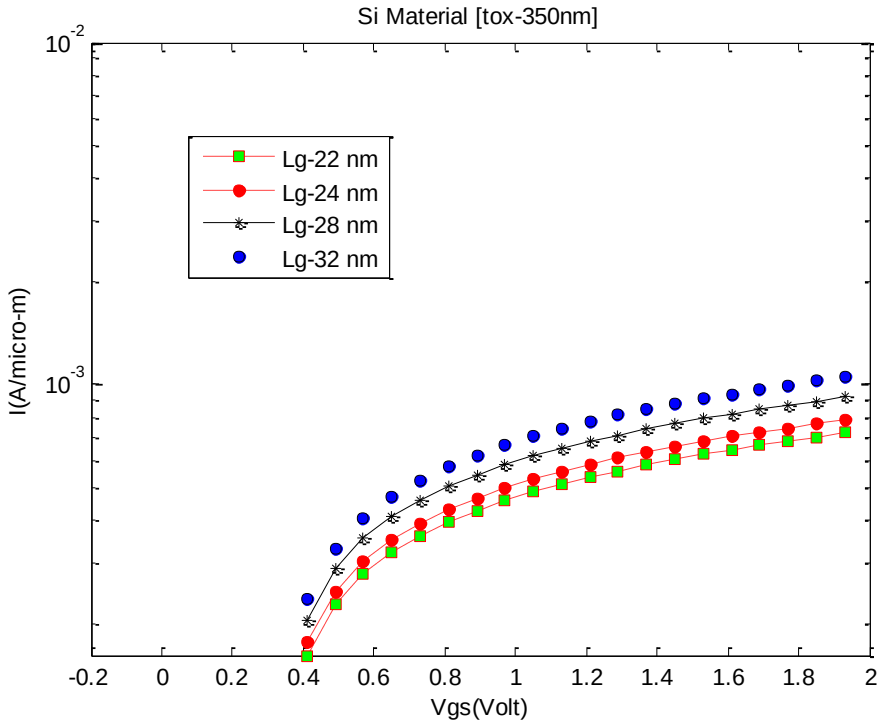


Figure 4.21: Impact of varying gate length (L_g) on I-V_{gs} Curve for the DG Fe-TFET in case of Si Material with ferroelectric oxide thickness, t_{ox} = 350 nm

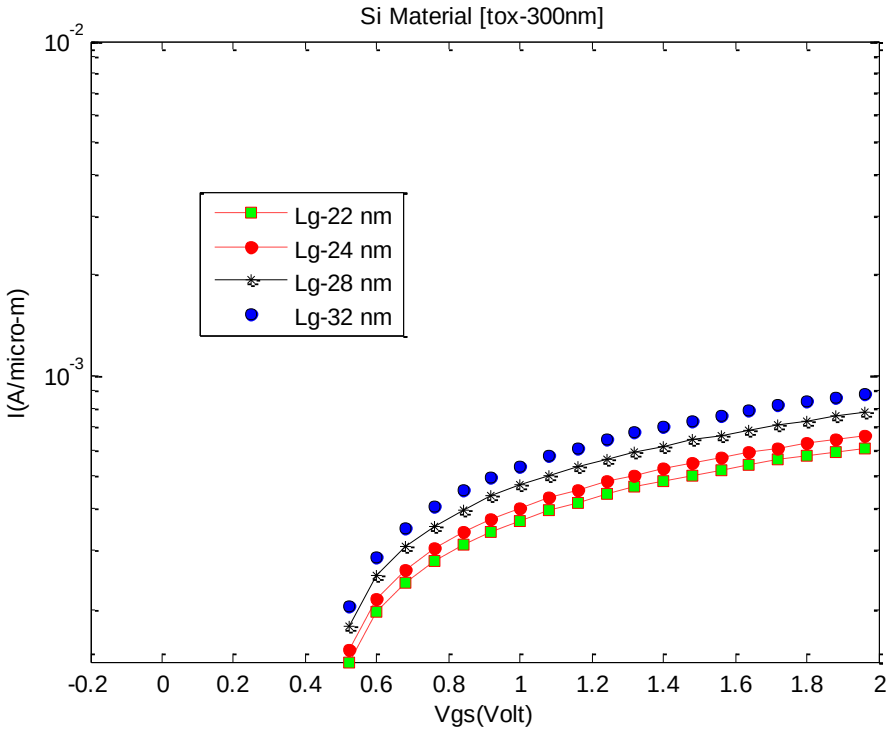


Figure 4.22: Impact of varying gate length (L_g) on I-V_{gs} Curve for the DG Fe-TFET in case of Si Material with ferroelectric oxide thickness, t_{ox} = 300 nm

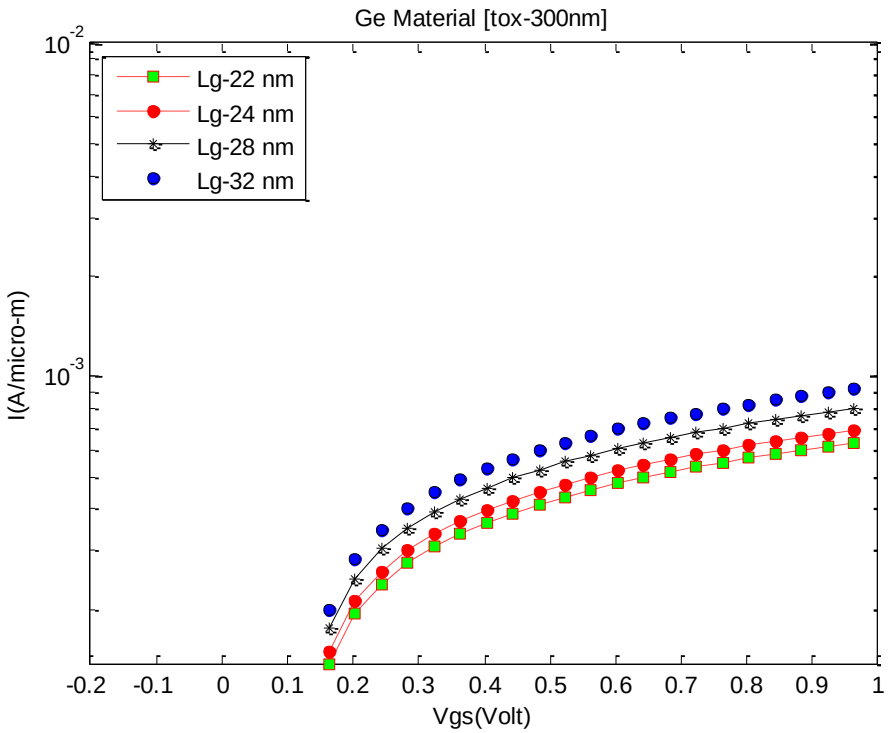


Figure 4.23: Impact of varying gate length (L_g) on I-V_{gs} Curve for the DG Fe-TFET in case of Ge Material with ferroelectric oxide thickness, t_{ox} = 300 nm

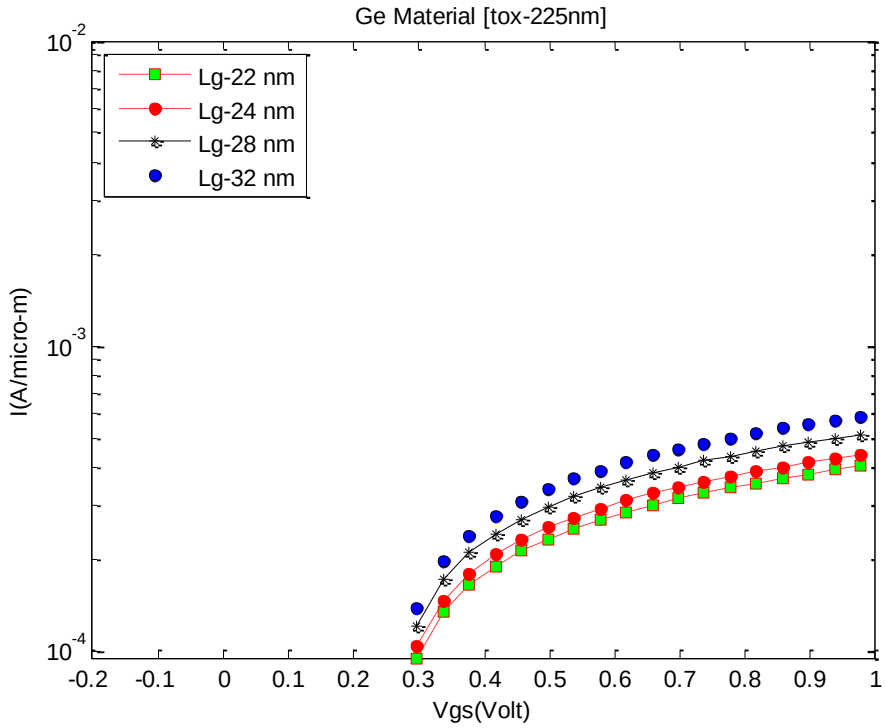


Figure 4.24: Impact of varying gate length (L_g) on I-V_{gs} Curve for the DG Fe-TFET in case of Ge Material with ferroelectric oxide thickness, t_{ox} = 225 nm

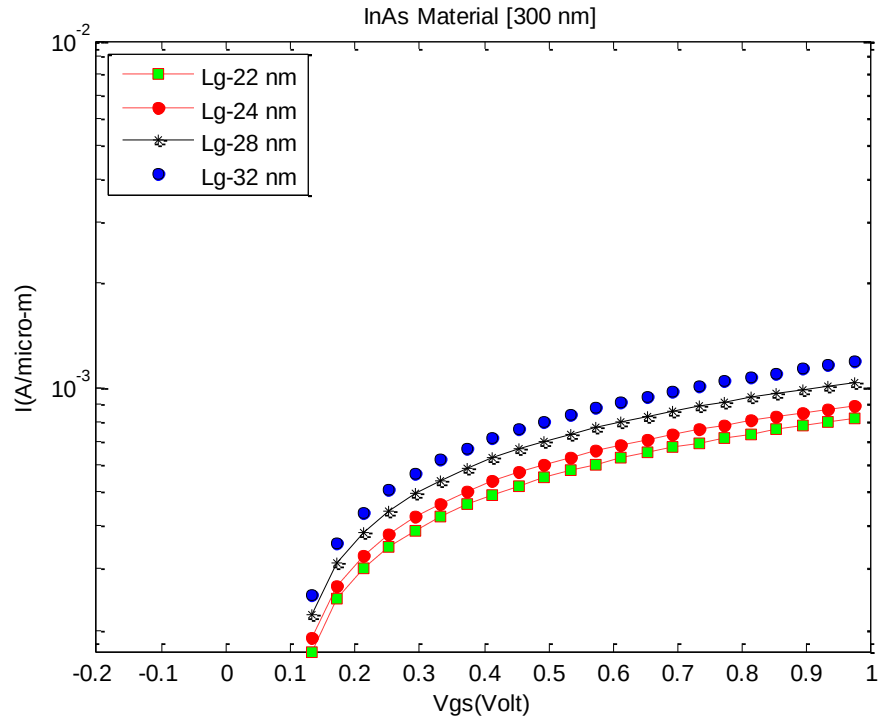


Figure 4.25: Impact of varying gate length (L_g) on I-V_{gs} Curve for the DG Fe-TFET in case of InAs Material with ferroelectric oxide thickness, t_{ox} = 300 nm

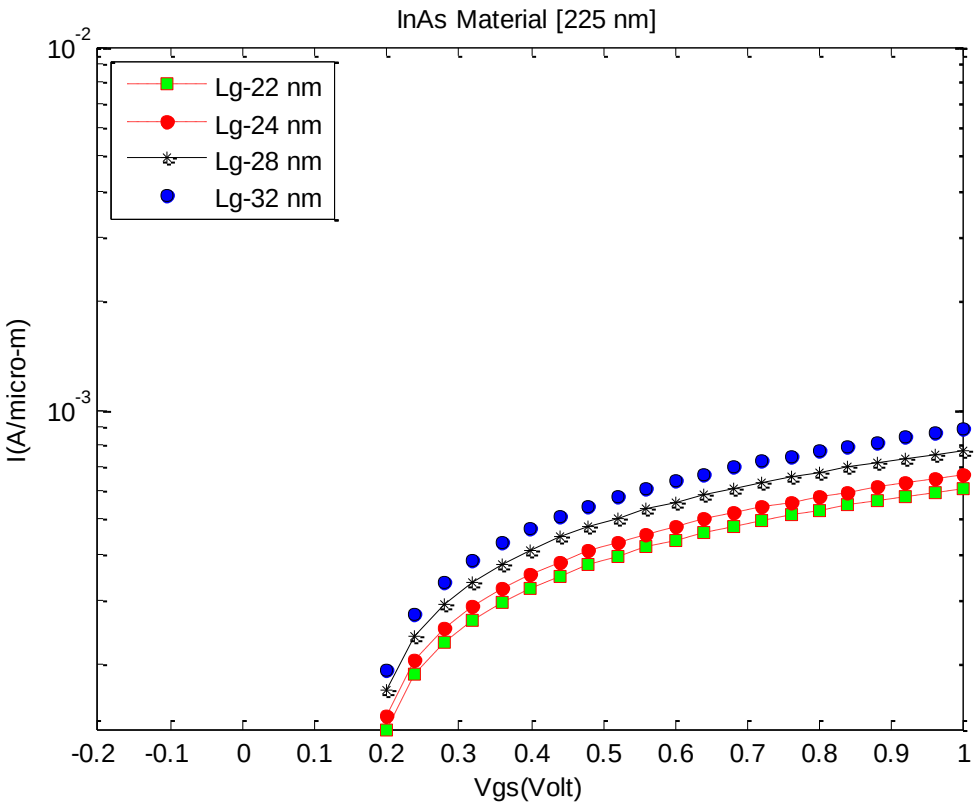


Figure 4.26: Impact of varying gate length (L_g) on I-V_{gs} Curve for the DG Fe-TFET in case of InAs Material with ferroelectric oxide thickness, t_{ox} = 225 nm

4.7 Comparison with semi classical DG-TFET

The magnitudes of the characteristic variations for Double Gate Ferroelectric TFETs can be compared to those for conventional Double Gate TFET, as presented in the Fig 4.27 & Figure 4.28.

For the Double Gate TFET with high k dielectric thickness 2nm, the operating voltage is 1.8V. But in case our proposed device DG Fe-TFET with ferroelectric material, the operating voltage is 0.8V in case of $BaTiO_3$ with thickness 160nm and 0.9V in case of $SrTiO_3$ with thickness 2nm. The changes in characteristics for this change in ferroelectric oxide in place of traditional oxide (high k dielectric) is ΔV_{Th} = 1V which is a huge improvement about 55.55%. This same effect is also shown by $SrTiO_3$ with small oxide thickness which is similar to the conventional TFET, but the behavioral property of SrTiO3 is needed further study to employ into the device structure.

For each characteristic, the variations for Fe-TFETs were higher magnitude than that of conventional TFET. For very thin oxide thickness layers, the changes in threshold voltage and subthreshold slope for conventional MOSFETs and TFETs are comparable with very thick ferroelectric oxide layers, while the fluctuation of ON current for Fe-TFET is higher for traditional TFET. The ON-current of a Fe-TFET depends on the width of the energy barrier between the intrinsic and p+ regions, and the current increases exponentially with a reduction in this barrier width.

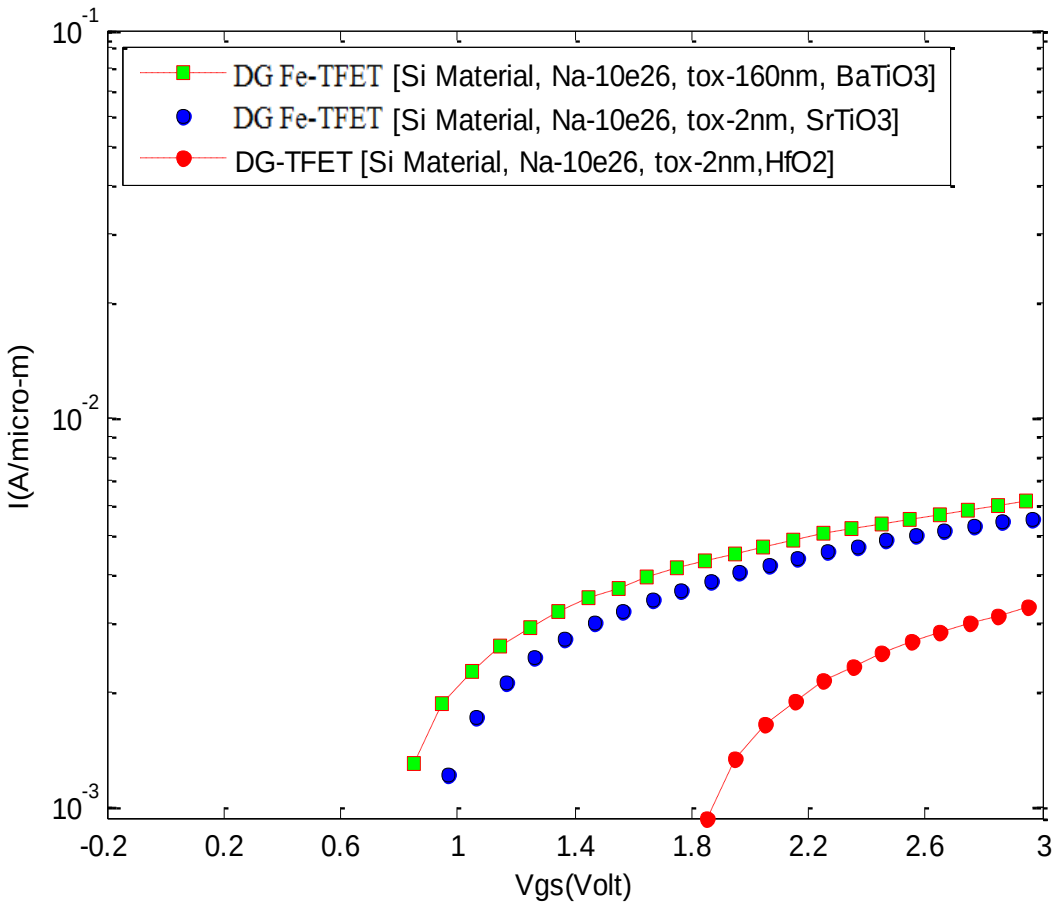


Figure 4.27: Comparison of I-V_{gs} characteristics curve between DG Fe-TFET with $BaTiO_3$ [t_{ox}=160nm] and $SrTiO_3$ [t_{ox}=2nm] as ferroelectric oxide and semi classical DG TFET with HfO_2 [t_{ox}=2nm] as high k dielectric oxide.

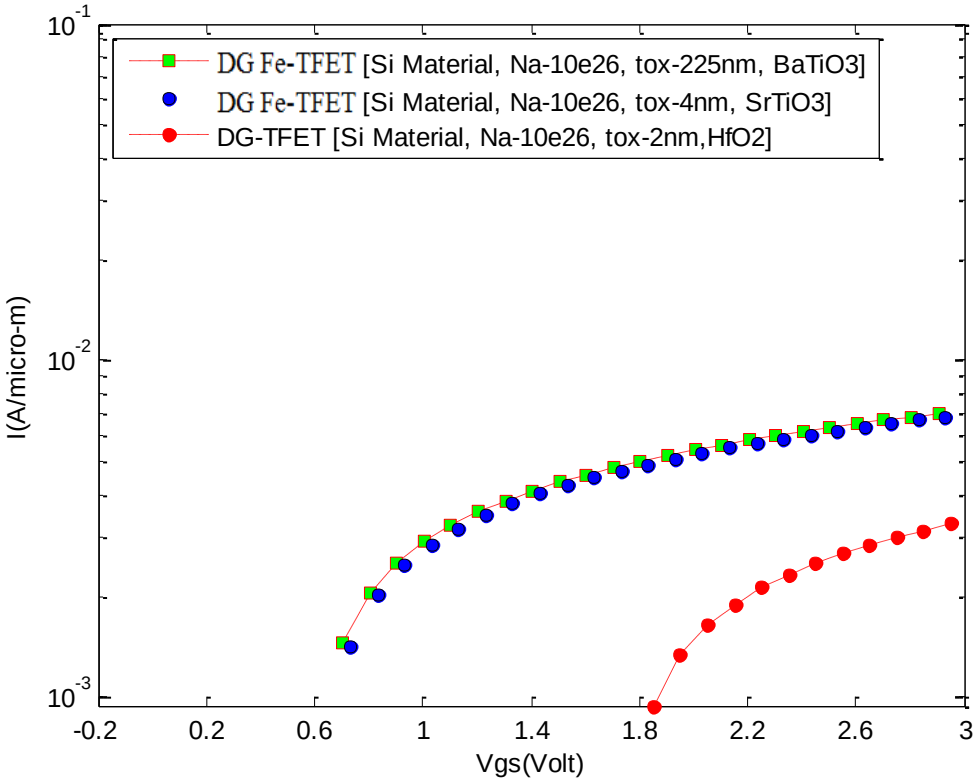


Figure 4.28: Comparison of I-V_{gs} characteristics curve between DG Fe-TFET with $BaTiO_3$ [t_{ox}=225nm] and $SrTiO_3$ [t_{ox}=4nm] as ferroelectric oxide and semi classical DG TFET with HfO_2 [t_{ox}=2nm] as high k dielectric oxide.

4.8 Optimization of Subthreshold Slope (SS)

The benefits of a DG Fe-TFET over a DG MOSFET and DG TFET which compares the I–V_{gs} characteristics of an optimized asymmetrical DG TFET from with those of a analytical model of DG Fe-TFET, being proposed for the first time in this work. The two devices have the same dimensions for channel length (i-region length in the TFET, equal to 45 nm), and body thickness (10 nm) and different value of oxide thickness (225nm for DG Fe-TFET and 4 nm for DG TFET). The optimized DG Fe-TFET uses ferroelectric material ($BaTiO_3$) instead of traditional oxide or high k dielectric material, as will be discussed later. It is important to notice the difference between the subthreshold regions in these two types of devices.

A MOSFET has a constant slope between the OFF-state and threshold. A TFET, however, demonstrates a slope that is steeper (smaller slope) closer to the OFF-state and less steep closer to threshold and varies as a function of the gate voltage. And this effect is much greater for our proposed device that the semi classical TFET.

Table 1.151: Values of Biasing V_g, I_{ON}, I_{OFF} and SS for different thickness (t_{ox}) of ferroelectric oxide, $BaTiO_3$ in case of GaAs Material

GaAs Material	t_{ox} (nm)	Biasing V_g (V)	I_{ON} (A/μm)	I_{OFF} (A/μm)	SS (mV/dec)
E_g = 1.43 eV ϵ_r = 13.1 C_s = 0.111 F/m^2	440	0.228	0.0465	10^{-13}	19.54
	400	0.342	0.0285		29.8
	350	0.478	0.0197		42.3
	300	0.64	0.0153		57.2

Table 1.152: Values of Biasing V_g, I_{ON}, I_{OFF} and SS for different thickness (t_{ox}) of ferroelectric oxide, $SrTiO_3$ in case of GaAs Material

GaAs Material	t_{ox} (nm)	Biasing V_g (V)	I_{ON} (A/μm)	I_{OFF} (A/μm)	SS (mV/dec)
E_g = 1.43 eV ϵ_r = 13.1 C_s = 0.111 F/m^2	8	0.2685	0.03941	10^{-13}	23.15
	7	0.4111	0.02559		36.03
	6	0.6046	0.022		53.3
	4	0.92	0.015		82.31

Table 1.161: Values of Biasing V_g, I_{ON}, I_{OFF} and SS for different thickness (t_{ox}) of ferroelectric oxide, $BaTiO_3$ in case of Si Material

Si Material	t_{ox} (nm)	Biasing V_g (V)	I_{ON} (A/μm)	I_{OFF} (A/μm)	SS (mV/dec)
E_g = 1.1 eV ϵ_r = 11.8 C_s = 0.1 F/m^2	440	0.2905	0.0274	10^{-10}	34.4
	400	0.385	0.02176		46.1
	350	0.48	0.017		58.3
	300	0.5787	0.01176		71.7

Table 1.162: Values of Biasing V_g, I_{ON}, I_{OFF} and SS for different thickness (t_{ox}) of ferroelectric oxide, $SrTiO_3$ in case of Si Material

Si Material	t_{ox} (nm)	Biasing V_g (V)	I_{ON} (A/μm)	I_{OFF} (A/μm)	SS (mV/dec)
E_g = 1.1 eV ϵ_r = 11.8 C_s = 0.1 F/m^2	8	0.3551	0.03382	10^{-10}	41.63
	6	0.569	0.02382		67.9
	4	0.798	0.01882		96.4
	2	1.012	0.01412		124.17

Table 1.171: Values of Biasing V_g, I_{ON}, I_{OFF} and SS for different thickness (t_{ox}) of ferroelectric oxide, $BaTiO_3$ in case of Ge Material

Ge Material	t_{ox} (nm)	Biasing V_g (V)	I_{ON} (A/μm)	I_{OFF} (A/μm)	SS (mV/dec)
E_g = 0.66 eV ϵ_r = 16 C_s = 0.1356 F/m^2	350	0.1722	0.0375	10^{-8}	26.2
	300	0.286	0.0252		44.6
	225	0.397	0.0155		64.1
	200	0.4388	0.01378		71.4

Table 1.172: Values of Biasing V_g, I_{ON}, I_{OFF} and SS for different thickness (t_{ox}) of ferroelectric oxide, $SrTiO_3$ in case of Ge Material

Ge Material	t_{ox} (nm)	Biasing V_g (V)	I_{ON} (A/μm)	I_{OFF} (A/μm)	SS (mV/dec)
E_g = 0.66 eV ϵ_r = 16 C_s = 0.1356 F/m^2	6	0.2634	0.03324	10^{-8}	40.3
	5	0.3653	0.02559		57
	4	0.4569	0.02118		72.22
	2	0.64	0.01618		103

Table 1.181: Values of Biasing V_g, I_{ON}, I_{OFF} and SS for different thickness (t_{ox}) of ferroelectric oxide, $BaTiO_3$ in case of InAs Material

InAs Material	t_{ox} (nm)	Biasing V_g (V)	I_{ON} (A/μm)	I_{OFF} (A/μm)	SS (mV/dec)
E_g = 0.36 eV ϵ_r = 14.6 C_s = 0.1237 F/m^2	400	0.16388	0.06176	10^{-6}	34.2
	350	0.2055	0.030588		45.8
	300	0.258	0.02382		58.9
	225	0.3277	0.01764		77.2

Table 1.182: Values of Biasing V_g, I_{ON}, I_{OFF} and SS for different thickness (t_{ox}) of ferroelectric oxide, $SrTiO_3$ in case of InAs Material

InAs Material	t_{ox} (nm)	Biasing V_g (V)	I_{ON} (A/μm)	I_{OFF} (A/μm)	SS (mV/dec)
E_g = 0.36 eV ϵ_r = 14.6 C_s = 0.1237 F/m^2	6	0.2638	0.03206	10^{-6}	58.5
	5	0.325	0.02676		73.4
	4	0.342	0.02206		78.7
	2	0.4388	0.01676		103.8

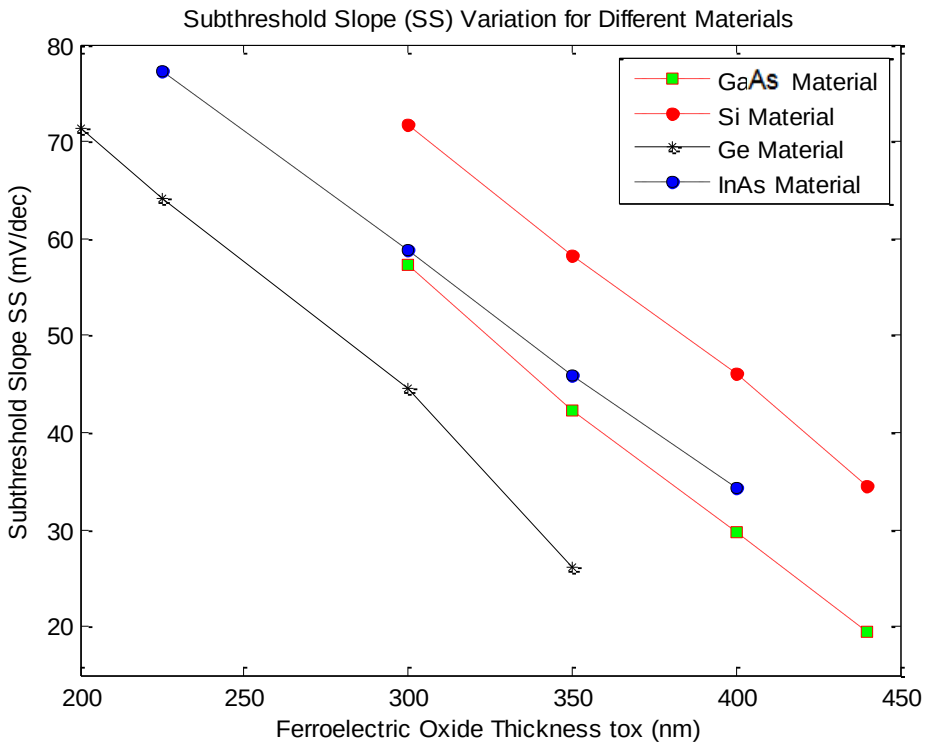


Figure 4.291: Variation of SS as a function of thickness (t_{ox}) of ferroelectric oxide, $BaTiO_3$ for GaAs, Si, Ge, InAs Material.

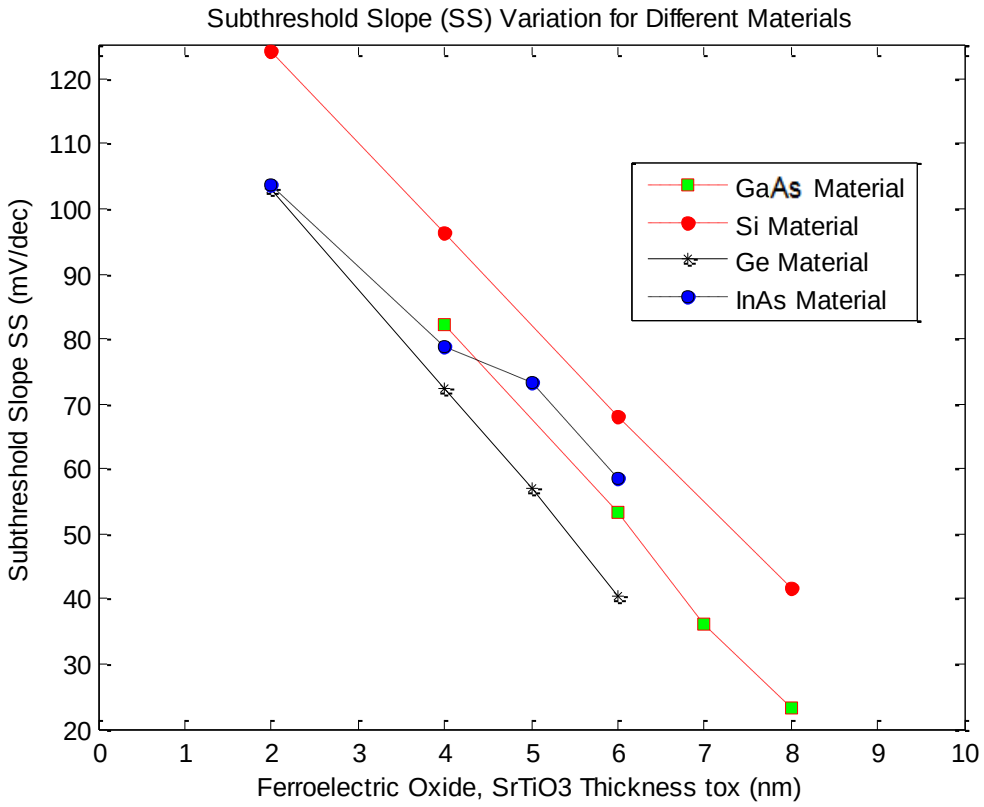


Figure 4.292: Variation of SS as a function of thickness (t_{ox}) of ferroelectric oxide, $SrTiO_3$ for GaAs, Si, Ge, InAs Material.

It is clear that the slope for the Fe-TFET in Figure 4.291 & Figure 4.292 is lower than that of the TFET. The average SS value is calculated between the voltage at which the current begins to increase with increasing gate voltage, and the threshold voltage. These two values are different because SS is a function of V_g. Their extraction is shown in the inset of Figure 4.291 & Figure 4.292.

4.9 Improvement of I_{ON}/I_{OFF}

Several trends can be seen in the figure. First, OFF-current, which depends on the cross section of the p-i-n structure, slightly decreases as expected with thickness. As, the film gets thinner than 10 nm, ON current starts to drop, possibly due to the reduced cross-sectional area available for current flow. Due to these trends, the ratio I_{ON}/I_{OFF} will have a maximum when plotted against ferroelectric oxide thickness. Table 1.19 to Table 1.22 shows that this optimum value occurs when t_{ox} is higher, depending on the

value chosen for E_g means different material. The maximum ratio is about 2×10^{11} in case of GaAs Material and as a comparison, the optimized asymmetrical DG MOSFET from [19] has an I_{ON}/I_{OFF} ratio of 10^6 with I_{ON} taken at Vg = 1.5 V. The order of magnitude of the I_{ON}/I_{OFF} ratio is not dramatically modified by a variation of the oxide thickness, which would be advantageous if there were variations of body thickness in devices on thin films.

Table 1.19: Values of I_{ON}, I_{OFF} and I_{ON}/ I_{OFF} for ferroelectric oxide thickness (t_{ox}) in case of GaAs Material

GaAs Material	t_{ox} (nm)	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/ I_{OFF}
E_g = 1.43 eV ϵ_r = 13.1 C_s = 0.111 F/m^2	440	0.0465	10^{-13}	4.65×10^{11}
	400	0.0285		2.85×10^{11}
	350	0.0197		1.97×10^{11}
	300	0.0153		1.53×10^{11}

Table 1.20: Values of I_{ON}, I_{OFF} and I_{ON}/ I_{OFF} for ferroelectric oxide thickness (t_{ox}) in case of Si Material

Si Material	t_{ox} (nm)	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/ I_{OFF}
E_g = 1.1 eV ϵ_r = 11.8 C_s = 0.1 F/m^2	160	0.0274	10^{-10}	2.74×10^{8}
	150	0.02176		2.176×10^{8}
	140	0.017		1.7×10^{8}
	130	0.01176		1.176×10^{8}

Table 1.21: Values of I_{ON}, I_{OFF} and I_{ON}/ I_{OFF} for ferroelectric oxide thickness (t_{ox}) in case of Ge Material

Ge Material	t_{ox} (nm)	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/ I_{OFF}
E_g = 0.66 eV ϵ_r = 16 C_s = 0.1356 F/m^2	350	0.0375	10^{-8}	3.75×10^6
	300	0.0252		2.52×10^6
	225	0.0155		1.55×10^6
	200	0.01378		1.378×10^6

Table 1.22: Values of I_{ON}, I_{OFF} and I_{ON}/ I_{OFF} for ferroelectric oxide thickness (t_{ox}) in case of InAs Material

InAs Material	t_{ox} (nm)	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/ I_{OFF}
E_g = 0.36 eV ϵ_r = 14.6 C_s = 0.1237 F/m^2	400	0.06176	10^{-6}	6.176×10^4
	350	0.030588		3.0588×10^4
	300	0.02382		2.382×10^4
	225	0.01764		1.764×10^4

Clearly, these values of the average swing depend upon our chosen definition for the threshold voltage. A lower constant current value would lower the threshold voltage and in turn, would advantageously lower the average swing values. It is worth mentioning, however, that qualitatively, all the trends of the curves remain the same.

CHAPTER 5
Conclusion

5.1 Summary of this Study

MATLAB simulations of the analytical model have proven to be an effective means to investigate TFET behavior and the dependence of its static characteristics on changes in dimensions, doping, and other parameters.

The work presented here can be useful to other researchers who will be designing and fabricating Ferroelectric TFETs, and developing analytical and compact models for these devices. The proposed device Fe-TFET had a double gate, a high source doping and lower drain doping to suppress ambipolar behavior, a ferroelectric material is used to boost the I_{ON} without affecting I_{OFF}. The main accomplishments of this work can be summarized as follows:

The optimization of the static characteristics of TFETs by the variation of gate structure (single or double), source, drain, and intrinsic region doping levels, gate dielectric material, and silicon body thickness was carried out. The resulting optimized device had a double gate, a high source doping and lower drain doping to suppress ambipolar behavior, a ferroelectric oxide, and a silicon body thickness of 10 nm. Different dielectric material was investigated and by replacing traditional oxide by ferroelectric oxide there was a significant change in ON current and trans-conductance. An investigation of band gap reduction at the tunnel junction was performed. The best characteristics were attained when band gap was small at the junction where tunneling takes place so that ON-current was improved and large at the other (drain-side) junction so that OFF-current stayed low. The optimization of work function shows that the increasing value of work function decreases the threshold voltage significantly. Channel length variation doesn't show much change in I_{ON} current but by increasing channel length breakdown improves significantly. Ferroelectric oxide thickness enlargement decreases leakage current in our proposed device.

Finally, a parameter variation study was carried out, looking at the effects on important static characteristics: ON-current, threshold voltage and subthreshold slope. The most important finding was that gate dielectric thickness, silicon body thickness, and tunnel

junction doping profile abruptness are the parameters whose tight control is the most critical during TFET fabrication. In addition, above the critical gate length at which p-i-n leakage becomes a concern, gate length variations cause almost no fluctuation in characteristics, unlike the case for conventional MOSFETs. Our proposed FeTFET showed improved characteristics including higher ON-current, .higher trans-conductance and a lower sub-threshold swing after the modifications in the design of previously proposed device. The TFETs promising behavior makes it a strong candidate to complement or replace MOSFET technology, particularly for low power applications.

5.2 Suggestion for Future Works

Recent research relevant to the problem in chapter 1, it can be seen that the majority of TFET work has been done in the past few years but there is still much progress to be made in terms of optimization to achieve superior device characteristics. The biggest future challenge is to successfully design and fabricate fully-optimized TFETs of both n-type and p-type that show low OFF-currents beyond what is possible for conventional MOSFETs, high ON-currents and average SS of less than 60 mV/decade at room temperature. Further work will also be necessary in order to develop most accurate analytical and compact models for TFETs. Although some work has been done in these areas, the theoretical framework which will allow experimental data to be fitted has not yet been developed. More calibration and tuning of the models are required and will become possible once more experimental data is available [48-50].

There are several scopes of future works on the areas of this study. These are as follows.

In this thesis work, 1-D simulation is performed to study the behavior of the ferroelectric TFET but 2-D simulation can be performed to carry out a more comprehensive analysis. Here 1-D analytical model has been performed along the grid line perpendicular to the direction of the carrier transport. Similarly 2-D analytical model can be carried out along a cross section perpendicular to the direction of the charge carrier transport.

The obtained results from the analytical model can be compared with the experimental data and analyzed those results with more alternate material for future study. There are

several topics presented in this thesis which still have some open points, or certain aspects that are not fully understood. These points need further study. This work is mainly focused on the variation of tunneling junction in between the source and intrinsic region. Future work can be conducted with the focus on the impact of the junction in between the intrinsic region and drain region to the ON current.

A more comprehensive study of both tensile and comprehensive strain effects on the electrostatics and transport properties of highly scaled Fe-TFETs can be performed. In this thesis work, substrate capacitance is taken as the variation of the dielectric constant of different materials considering the effective body thickness is around 1 nm, but this is needed to further study and should taken into account the effect of effective body thickness for different materials. The ON-current was seen to have a maximum at some large ferroelectric oxide thickness. The reason for the decrease in ON-current with smaller t_{ox}, but this should be studied further too to fully understand. Once again, more experimental data is necessary in order to choose the optimum value of the ferroelectric oxide thickness. The channel length is considered 45 nm in this work, not showing the effect of variation of channel length to model the ON current equation. So, it is needed to further study.

This study focused on the ON state characteristics of the Fe-TFET. Study can be conducted on the OFF state current and construct an analytical model of the OFF state current to describe the device behavior more accurately which are more important figure of merits of highly scaled devices. In this study, a small layer thickness of SiO_2 is shown in between the ferroelectric material and the substrate, but the effect of SiO_2 layer is neglected to evaluate the analytical model of ON current. So, this can be included to get a more accurate model and investigate the device performance with the experimental data to get a clear view of our proposed model. In this work, the effective oxide thickness (EOT) is not possible to take into account for the comparison our proposed model with the semi classical TFET, because of the different characteristics of the ferroelectric material and the traditional oxide. So, it is needed to find out the alternate relationship to explain and distinguish the material's behavior more accurately.

Finally, I am convinced that once Fe-TFETs have been investigated and developed and once Fe-TFETs with highly optimized characteristics have been fabricated, then these promising devices will live up to their potential. I am optimistic that these devices or some variation upon them will bring lower power consumption and better energy-efficiency to computers, appliances, and devices everywhere.

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