M.Sc. Engineering Thesis

DESIGN OF A UWB TRANSMITTER WITH INTEGRATED ANTENNA FOR ON-CHIP RF WIRELESS INTERCONNECTS

By

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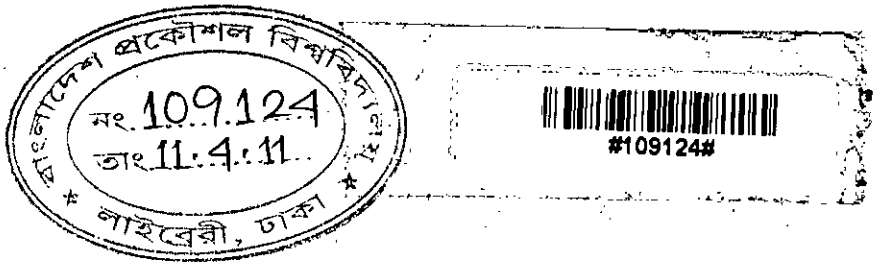

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Candidate's Declaration

This is to certify that the work presented in this thesis entitled **"DESIGN OF A UWB TRANSMITTER WITH INTEGRATED ANTENNA FOR ON-CHIP RF WIRELESS INTERCONNECTS"** is the outcome of the investigation carried out by me under the supervision of Professor Dr. A. B. M. Harun-ur Rashid in the Department of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology (BUET), Dhaka. It is also declared that neither this thesis nor any part thereof has been submitted or is being currently submitted anywhere else for the award of any degree or diploma.

A. Arafat 2.4.2011

Muhammad Abdullah Arafat

Candidate

Dedicated to My Parents

CONTENTS

List of Figures

List of Tables

List of Abbreviations

UWB	Ultra Wideband
IR-UWB	Impulse Radio Ultra Wideband
TR	Transmitted Reference
OOK	On Off Keying
BPSK	Bipolar Phase Shift Keying
PPM	Pulse Position Modulation
FCC	Federal Communication Commission
ITRS	International Technology Roadmap for Semiconductors
RF	Radio Frequency
PCIe	Peripheral Component Interconnect express
SP	Single Pulse
SNR	Signal to Noise Ratio
PSD	Power Spectral Density
LNA	Low Noise Amplifier
LPF	Low Pass Filter
PRR	Pulse Repetition Rate
GMP	Gaussian Monocycle Pulse
DGP	Derivative of Gaussian Pulse
GP	Gaussian Pulse
MP	Monocycle Pulse

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Abstract

With the continued growth in the integration density of CMOS and clock frequency of ultra-large-scale integrated circuits, the wire interconnects technology is emerging as the major bottleneck to the improvement of integrated circuit (IC) technology. The semiconductor industry has sought to address this primary problem by increasing the thickness of the wires, using more exotic substrate materials with lower dielectric loss tangents, and employing more sophisticated input/output drivers. However, all of these potential solutions are costly, thereby making wireless interconnect technology an increasingly attractive alternative. In this thesis, we have proposed a simple impulse radio ultra wideband (IR-UWB) wireless interconnect system with integrated antennas, transmitters, and receivers for inter-chip and intra-chip communications. To avoid complicated inter-chip/intra-chip channel estimation methods and to reduce electronic overhead in terms of circuit components in the receiver transmitted reference ultra wideband (TR-UWB) signaling scheme has been incorporated in the system architecture that provides straight-forward synchronization. Various UWB pulses have been investigated to explore the ultimate pulse shape which satisfies the FCC regulations and also provides the highest data transmission rate. Novel circuit topologies have been proposed to design complete digital OOK/BPSK UWB transmitters in IBM 90nm CMOS technology. For the transmitters, a Gaussian monocycle UWB pulse is generated using triangular impulse generation technique with novel methodology to include TR pulse. A differential operation has been employed to increase the maximum achievable voltage swing and to immunize environmental noise. The circuits have been developed in an integrated fashion with low power requirements desirable for on-chip wireless interconnects. The performance of the proposed transmitters has been evaluated and compared with some other available UWB transmitters, which shows superior performance over the conventional transmitters. The transmitters together with the on-chip dipole antenna have been simulated to confirm the effective reception of the transmitted signal.

CHAPTER 1
INTRODUCTION

1.1 Motivation

Modern electronics technology has changed the world in a short time span. A good share of the credit should go to microelectronics. Since the invention of the integrated circuits in the late 1950s, the development of this remarkable device has been blessed by the laws of physics and the science of materials. The initial material choices – silicon substrates, silicon dioxide gate, intermediate dielectrics, aluminum interconnection and process such as planer technology and photolithography have stood the test of 50 years. In addition, the industry has taken the advantage of the fact that decreasing transistor size not only reduced cost, but also improved performance in terms of speed, functionality and power dissipation. However, the laws of physics and the science of materials are becoming less friendly as we approach 100 nm design regime. Despite remarkable experimental results for transistors well below this dimension, there are growing challenges to our ability to effectively stay on the technology roadmap [1].

From the invention of the first transistor the industries have come a long ways to the brink of integrating billions of components on a single chip. Scaling of device dimensions continues to play an important role. Continuous advancements in technology have resulted in integrated circuits with smaller device dimensions and larger area and complexity. Decrease in minimum feature size has led to a decrease in interconnect cross sectional area and pitch. Increase in chip area has resulted in increase in communication distance (wire length). Increase in chip complexity has demanded more communication channels. This has also resulted in an increase in the number of metal layers. For the foreseeable future the scaling of the device dimensions will continue and IC chips with several billion components will be built in the future. To quantify the magnitude of the problem, the delay associated with an interconnect of length, d, with negligible series

resistance, is proportional to d and the square root of the relative dielectric constant, ε_r, of the inter level dielectric (ILD). The delay time is usually called the time of flight (TOF) across the signal line of the given length. For an ILD of $\varepsilon_r = 4.0$ (SiO_2), the TOF is about 6ps/mm. For an x-direction signal of interest, it is usually surrounded by many y-direction signal lines on an adjacent wiring layer. These orthogonal signal lines will add capacitance and further degrade the TOF to as much 8ps/mm. These numbers can be compared to the delays of a NAND gate with a fan out of 3, which are around 70, 30 and 12 ps for the 250-, 130- and 45- nm technologies respectively [2].

A microprocessor often requires a long interconnection line between the arithmetic logic unit (ALU) and the cache storage. As a first approximation, the length of this 'global' signal line can be assumed to be equal to the edge dimension of the chip- around 15 mm, 20 mm and 30 mm for the 250-, 130- and 45-nm chip generations. The TOFs for such lines would lie in the 125 to 250 ps range, increasing as the lines got smaller and the chips larger. These numbers range from 2 to 20 times the gate delay for the equivalent design rule, and are totally unacceptable burden in the device performance [3].

ULSI designers have identified various measures that could be undertaken to solve some, if not all of the problems being faced. The shift from aluminum to copper for metallization, the use of low k dielectric layer, reverse scaling of wire geometries, the inclusion of repeaters, and standard cell modification are some that already been successfully implemented. Nevertheless, these evolutionary approaches may soon encounter fundamental material limits. Revolutionary methods and techniques must be pursued to carry on the fast progress of future ULSI technology. One of such possibilities is to use "wireless interconnect using Si integrated antenna" [4, 5].

1.2 On-chip Wireless Interconnect Systems

With appropriate designs, RF/microwave signals can be transmitted efficiently through either free space or guided mediums. However, the efficient transmission and receiving of the RF/microwave signals in free space require the size of antennas to be comparable with their wavelengths. As the CMOS device dimensions continue to scale down, operating speeds and cut-off frequencies (f_t and f_{max}) of CMOS devices will exceed 100 GHz in the near future. At 24 GHz, the wavelength of electromagnetic waves in free space is 12.5 mm and in silicon it is 3.7 mm. This means a quarter wave antenna needs to be only 3 and 0.9 mm in free space and silicon respectively. These in conjunction with the increase of chip sizes to 2 cm x 2 cm have made the integration of antenna for wireless interconnection possible.

Based on these considerations, a wireless interconnects system acts as a miniature wireless LAN (local-area network). Compared to global electrical wires, this wireless scheme potentially offers several advantages. First, circuits can be synchronized over much larger chip sizes because wireless approach provides three to ten times' faster transmission of signals, compared to global wires. In addition, the bandwidth of the wireless interconnect system is only limited by the bandwidth of the transmitting and receiving components and not by the transmission medium, as in the case of global wires. Also the cross talk between channels should be much improved using FDMA and CDMA communication technique. Furthermore, wireless approach can provide new flexibility to reconfigure the interconnect system simply by changing the CDMA codes.

1.3 UWB Wireless Communication Systems

To realize the aforementioned advantages of wireless interconnect systems, the potentials of using Ultra Wideband (UWB) communication technology as the signal transmission technique are being investigated [6, 7]. Ultra-wideband (UWB) is regulated for commercial use in the band from 3.1-10.6 GHz by Federal Communication Commission (FCC) with the constraints of spectral mask which determined the maximum average equivalent radiated isotropic power spectral density of –41.25dBm/MHz and a minimum bandwidth of 500 MHz [8]. There are two approaches for UWB applications, which are Multi-band OFDM UWB and Impulse-Radio UWB (IR-UWB). Recently, low-cost, short-range wireless communication applications like radio frequency identification (RF-ID) and wireless sensor network have drawn much attention from the researcher as well as industries [9]. IR-UWB, without carrier signal, is one of the prominent candidates for those applications since circuit implementation is simpler, no up/down conversion or mixer is needed leading to substantial reduction in chip area and power consumption. IR-UWB uses the nano-second monocycle pulses to transmit the data signal over much wider frequency band than any conventional carrier based wireless systems.

These entire features make UWB scheme attractive for wireless interconnects systems. Moreover, it creates less electrical overhead on the existing circuitry of the chip because of its simplified transceiver architecture [10]. It has been shown that on chip antenna can be effectively utilized for UWB pulse generator thus avoiding expensive and power hungry analog components [11]. Also, to achieve a high data rate with low BER using conventional data transmission technique, one needs a substantial amount of transmitted power. Large transmitted power results in increased power consumption, which generates extra heat in the chip. Since UWB systems use ultra short pulses to transmit data, active signal occupies a small fraction of the total transmission time and hence the average power requirement is very low [12]. Thus the problem of heat generation and area penalty that originates from the circuitry of the intra/inter-chip wireless interconnect systems is radically solved by the use of UWB signal transmission technique.

1.4 UWB Transmitter

UWB transmitter is an indispensable part in the IR-UWB transceivers. Since part 15 of the FCC regulation has been revised for UWB systems [8], several types of UWB systems have been proposed, such as Impulse Radio (IR), Direct- Sequence UWB (DS-UWB), and Multi-Band OFDM (MB-OFDM) [10], [13]. Although the DS-UWB and MBOFDM are potential candidates for wireless personal area network (WPAN) applications, IR has been more attractive for UWB wireless interconnects [13]. A several papers about pulse generator have been published [14]-[34]. Some early works show that pulse generation could be performed by direct synthesis, using step recovery diode and transmission line [35] or using BJT characteristic [36], which is not easy for integration, low cost, low complexity purposes. Many of the papers are based on the analog technique since the digital technique circuitry [37] is complicated. In [38]-[40] analog based pulse generator circuits were presented. Recently, some digital UWB transmitters have been proposed [17], [25], [27] but those published works consume much power and can't provide high data rate. To satisfy the bandwidth, many types of pulses can be the candidates [41], but the Gaussian pulse is preferred since it has no side lobes and a sharp roll-off compared to other pulses. The theory analysis shows that, the higher order derivative of Gaussian pulse, the better roll-off we have and the pulse itself can satisfy the FCC spectral mask without using the filter. But increasing the order of derivatives, hence increasing the complexity of the circuit, increases the pulse width which put a severe limitation on the data transmission rate. All the traditional IR-UWB transmitters did not aware of this limitation because they were based on approaches developed for radar, RFID and wireless sensor networks applications emphasizing much on FCC regulations. Therefore, finding the ultimate pulse shape which will satisfy both FCC regulation and high data rate requirement for wireless interconnects applications deserves attention before designing the transmitter. The digital generation of UWB pulses, which can satisfy the FCC spectral mask with low power and low complexity, is still a challenge at present.

1.5 Research Objectives

The ultimate goal of this work is to develop an ultra wideband transmission technology and to design a low power high data rate UWB transmitter to be used for wireless interconnects systems for the future ULSI. The design objectives for this UWB interconnects systems are as follows:

- To develop an appropriate UWB communication scheme suitable for on-chip wireless interconnects.
- To find the most appropriate UWB pulse for chip interconnects for achieving maximum throughput.
- To design a low power high data rate UWB transmitter for on-chip wireless interconnects.
- To assure proper reception of the UWB pulses in the receiver by the on-chip antenna with a power level suitable for the LNA of the receiver.

1.6 Thesis Layout

This thesis comprises of six chapters. In **chapter 1** we gave a brief introduction on the limitations of present day IC technology which has initiated a tremendous research effort to stay on the technology roadmap for the future ULSI. The potentials of using UWB communication technology as the signal transmission technique for wireless interconnects and the present state of UWB transmitter design are discussed. Finally this chapter gives an outline of the objectives of this work.

Chapter 2 provides a detail literature review of the interconnect technology with its future prospect. It was shown that the main design constraint is the interconnect delay aroused due to the constant scaling down of interconnects which requires innovative techniques to solve. Some revolutionary techniques for interconnects such as 3-D

integration, optical interconnects and wireless interconnects are discussed. The chapter also provides some fundamental preliminaries on wireless interconnect and concludes by describing its promising advantages in wireless chip interconnects.

In **chapter 3**, we give an overview of the ultra wideband technology which includes the motivation of using UWB technology, UWB definition, advantages of UWB, UWB signaling and pulse shapes, modulation techniques. This chapter also provides the proposed IR-UWB transceiver architecture for wireless IC interconnects and introduces transmitted reference (TR) scheme for communication. The FCC regulation for UWB communication is then described and the ultimate pulse shape for high speed IR-UWB communication is proposed at the end of this chapter.

In **chapter 4**, we present the complete differential UWB transmitter design with step-by-step demonstration. OOK and BPSK transmitters are devised separately and both include TR scheme. The performances of the transmitters are evaluated and shown with simulation waveforms. A high speed digital clock generator circuit using CMOS inverters is also presented at the end of this chapter.

The on-chip antenna simulation in HFSS is done in **chapter 5** which confirms the successful reception of the transmitted UWB signal. The effect of various parameters of the antenna is also discussed in this chapter.

The thesis is finally concluded in **chapter 7** by presenting a summary of the overall research along with some suggestions for future work.

CHAPTER 2

FUTURE OF INTERCONNECT TECHNOLOGY

2.1 Background

The semiconductor industry has evolved at an incredible rate, particularly in the past two decades. Transistor channel lengths have steadily decreased from 2.0 μm in 1980 to 0.5 μm in 1992 to current (2011) development processes that incredibly have channel lengths as small as 32 nm. Each new generation of devices requires less area and has faster switching speeds than the preceding one. These benefits are reflected at both circuit and chip levels. At the circuit level, a particular function can be computed in less time and implemented in less silicon area. As a result, chips do not have to increase in size to possess more functionality. As a consequence of the transistor scaling, the number of transistors on each chip is increasing, and perhaps more significantly, their density is also increasing. This is a problem when one considers that each device must communicate with other devices, each circuit block needs to talk to other circuit blocks, and so on up the hierarchy. The interconnections required to support this communication grow increasingly more complex. Furthermore, due to the higher clock frequencies, these interconnections need to support higher bandwidths.

It is easy to imagine what problems may occur if this congestion is not addressed. The problem is as familiar as the rush-hour traffic encountered in daily commuting. The obvious solutions of building more highways and widening lanes are prohibitively expensive. Similarly, adding more metal levels and increasing chip size to accommodate more interconnects can significantly add to the overall cost. In short, interconnect design for a high-performance digital system is a growing problem that needs to be addressed early on in a design flow [42].

2.2 Conventional On-chip Wiring

On-chip wires have always been necessary to connect circuits together. While the metal and dielectric materials are undergoing changes, the wires largely have remained the same in function and usage. One significant difference is in their growing number. Figure 2.1 shows a Scanning Electron Microscope (SEM) photo of local interconnect with the dielectric material removed [43]. These on-chip wires are thin and narrow with cross-sectional dimensions typically less than half of a micron.

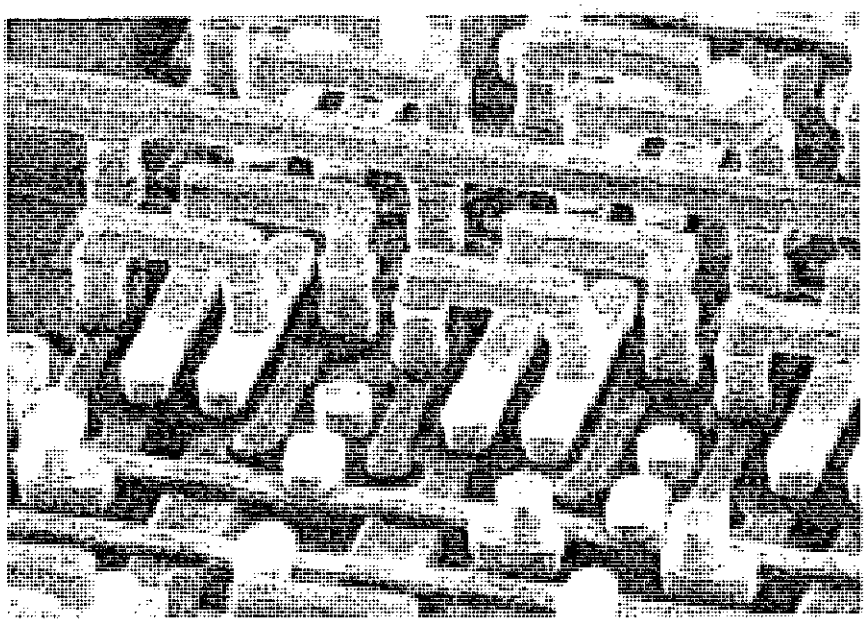


Figure 2.1: SEM photo of lower levels of interconnect (with dielectric material removed) [43]

The three tier architectural hierarchy of high-end microprocessor, shown in Figure 2.2, exhibits three distinct levels of wiring hierarchy. The first tier referred to as "local" comprises logic blocks built using standard cells, inverters and latches. These blocks are referred to hereafter as sub-modules. Approximately 80% of the wires on the chip begin and end within these sub-modules. The defining characteristics of these so-called "**local wires**" are that they are shorter in length and usually carry signals between various layers

of logic within the sub-module. The size of a sub-module is of the order of 10 K to 50 K gates depending upon the design and layout of the microchip.

Sub-modules are used to construct modules that belong to the second tier of the architectural hierarchy. **Intermediate wires** are defined as those that interconnect multiple sub-modules laid out according to a semi-global floor plan. They are usually of lengths between that of local and global wires and are mostly used for signal communications, but may also assist in clock distribution.

Finally, modules are arranged according to a pre-defined global floor plan to construct the third and final tier entity i.e. the chip itself. **Global wires** interconnect the modules and carry signals, clock and power between them.

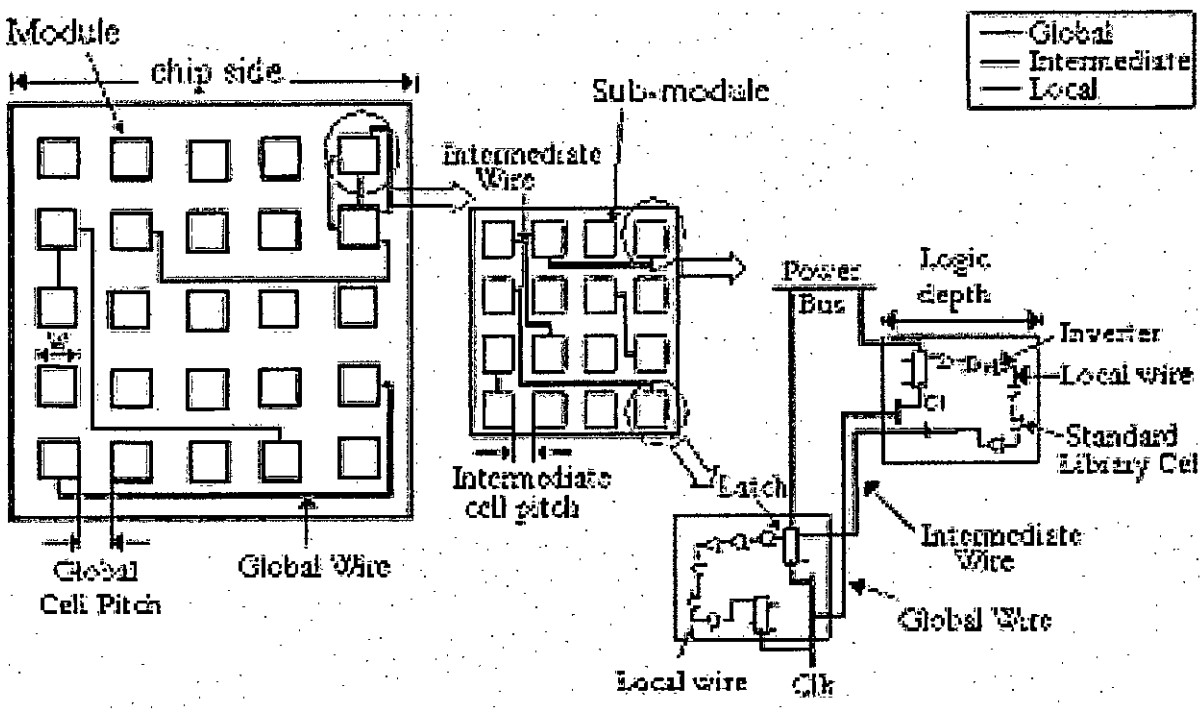


Figure 2.2: Three Tier Architectural hierarchy for VLSI circuit design

A wiring hierarchy is typically used that places the shorter wires nearer to the silicon surface and increasing longer wires on higher layers. Figure 2.3 shows a cross-section of an advanced hierarchical wiring scheme using copper metallization [44]. The lower levels of interconnect are thinner and are used in local routing. Intermediate layers

are of medium thickness and used for semi-global routing. Finally, the top layers are the thickest and are used for global routing. Alternating levels of interconnect are customarily laid out in orthogonal directions to minimize cross-talk between adjacent levels. Furthermore, this convention helps to simplify routing.

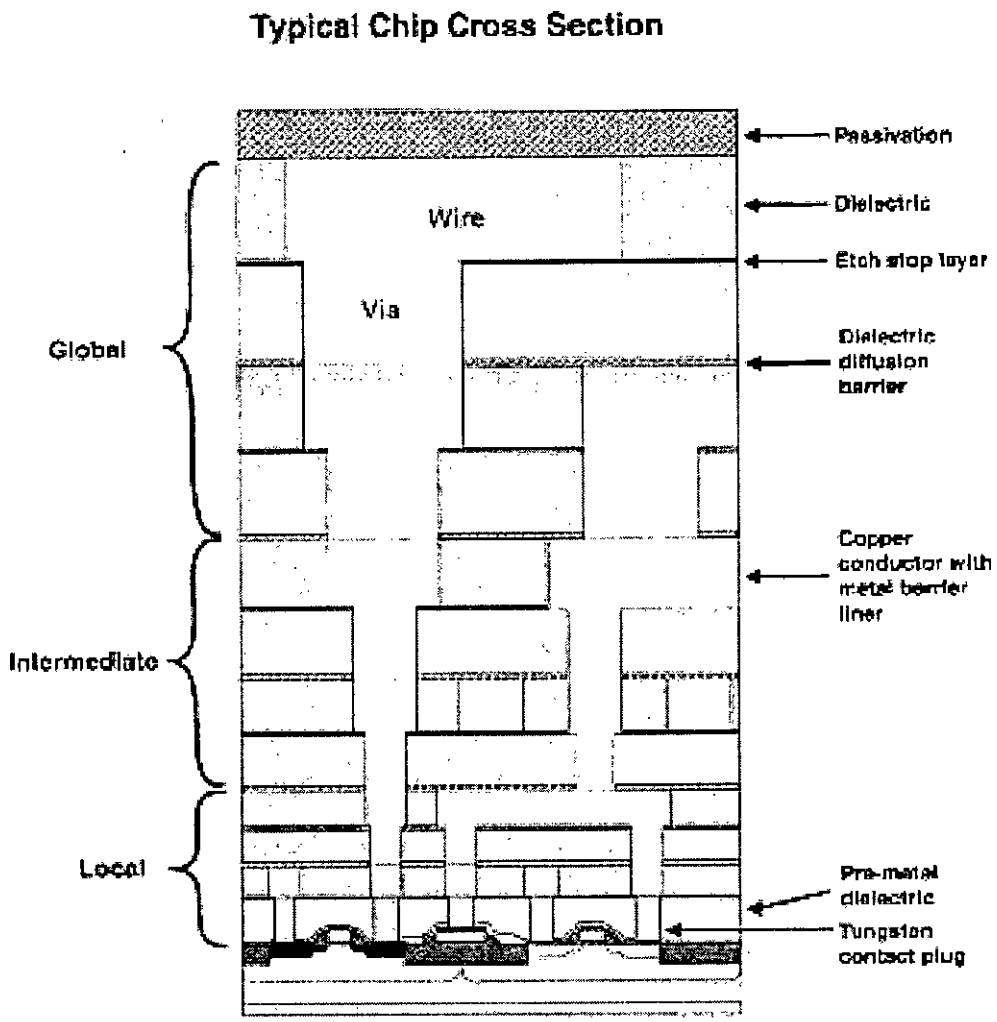


Figure 2.3: Sample cross-section of hierarchical wire scaling [44]

2.3 Logic and Wire Delays

The International Technology Roadmap for Semiconductors (ITRS) illustrates the growing problem of global interconnects delays (Figure 2.4) [44]. As technology continues to scale, the logic delays decrease due to faster transistors. At the same time, local interconnect delays similarly improve because the physical size of circuit blocks decrease, and the local interconnect spans shorter distances. On the other hand, the global interconnect delays rise with technology scaling for one of two different reasons. The first possible reason is that overall chip size increases so that interconnects need to span longer distances. A second, more likely, scenario is, even if chips do not become larger, the increased complexity of circuits requires an increased density of interconnects. This is achieved by reducing the cross-sectional area of wires, which negatively impacts the resistance, and decreasing wire spacing, which adversely impacts the capacitance. The combination of these factors results in global interconnect delays that scale in the wrong direction. Repeaters help alleviate this growing divergence between logic and global interconnect delays, but are not enough to close the performance gap.

Overall circuit performance in the past has depended primarily on device properties. To enhance the circuit and system speed the primary effort had been on improving the device speed through scaling the device dimensions. The parasitic resistance, capacitance and inductance associated with interconnections (Figure 2.5) and contacts are now beginning to influence circuit performance and will be one of the primary factors in the evolution of deep submicron ULSI technology. The results of theoretical modeling indicate that below 1 μm minimum feature size the impact of parasitics seriously hurts circuit and system performance [45]. RC time delay, IR voltage drop, CV^2f power consumption and crosstalk noise due to these parasitics is becoming appreciable.

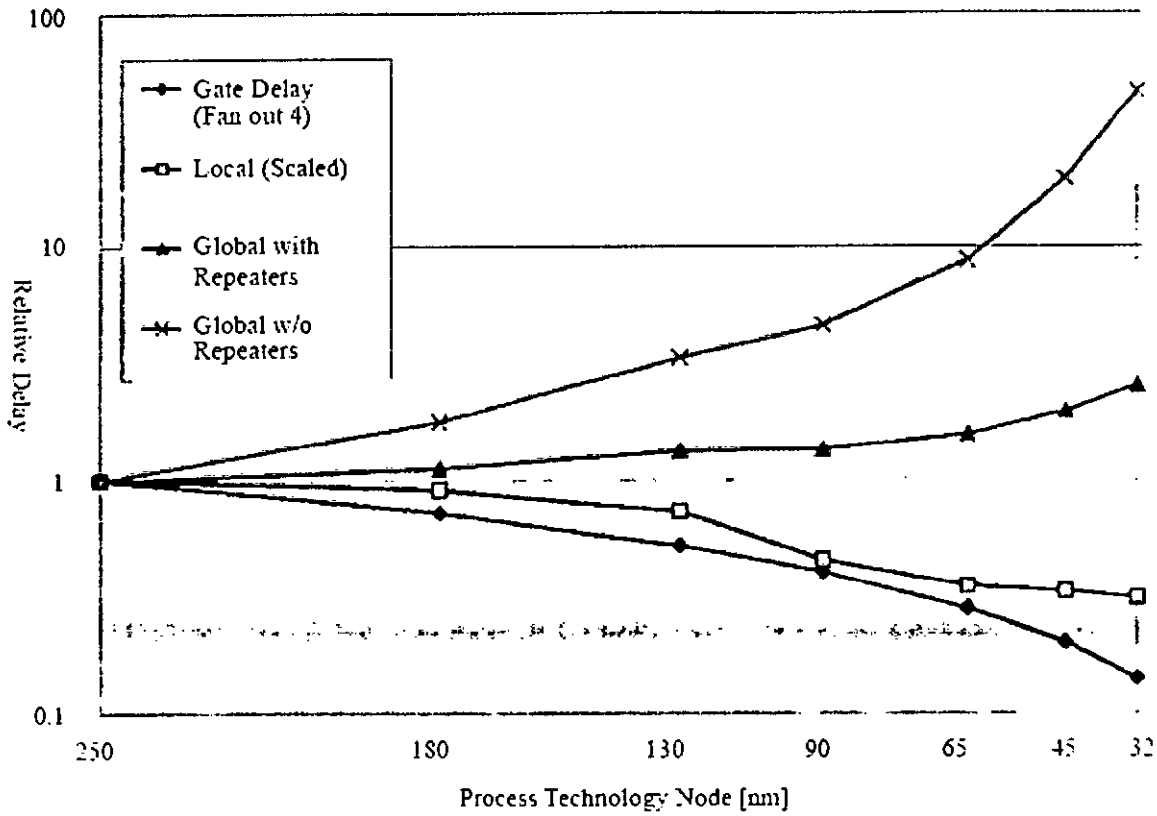


Figure 2.4: International Technology Roadmap for Semiconductors 2001 predictions for device and wire delays [44]

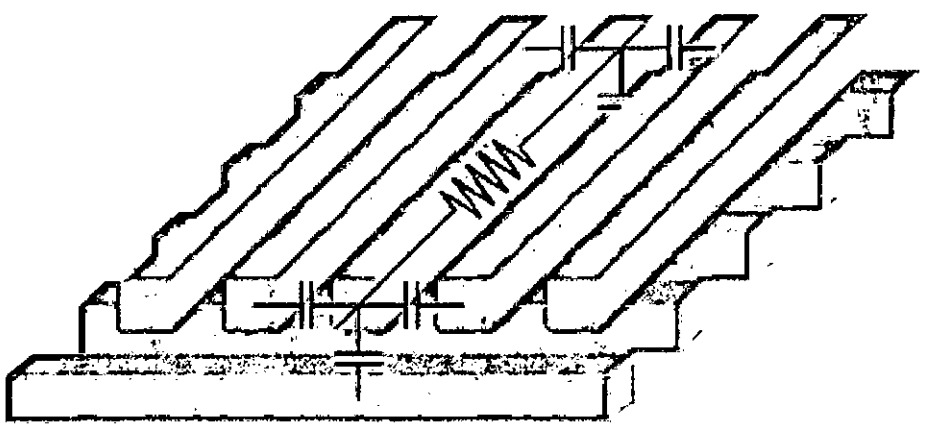


Figure 2.5: Dense mesh of interconnect typical of modern high-performance integrated circuits, with series resistance and shunt capacitance indicated

2.4 Evolutionary Approaches to Global Interconnect

Much of the work related to improving global interconnects is in reducing the resistance and capacitance of the wires. Along these lines, semiconductor fabrication facilities have introduced integration of new materials [46], [47]. Copper metallization provides lower resistance than similarly sized aluminum wires, and lower permittivity dielectrics provide lower capacitance. Introduction of these materials is expensive due to extensive reliability requirements and fabrication tool adaptation. At the circuit level, designers have sought to reduce capacitance by preventing wire switching in opposite directions. These techniques have shown to be effective in reducing the wire delay, but are not enough. Thus even with very fast devices and with copper and low-k dielectrics the overall performance of a large circuit could be seriously affected by the limitations of interconnections and contacts as shown in Figure 2.6 [1].

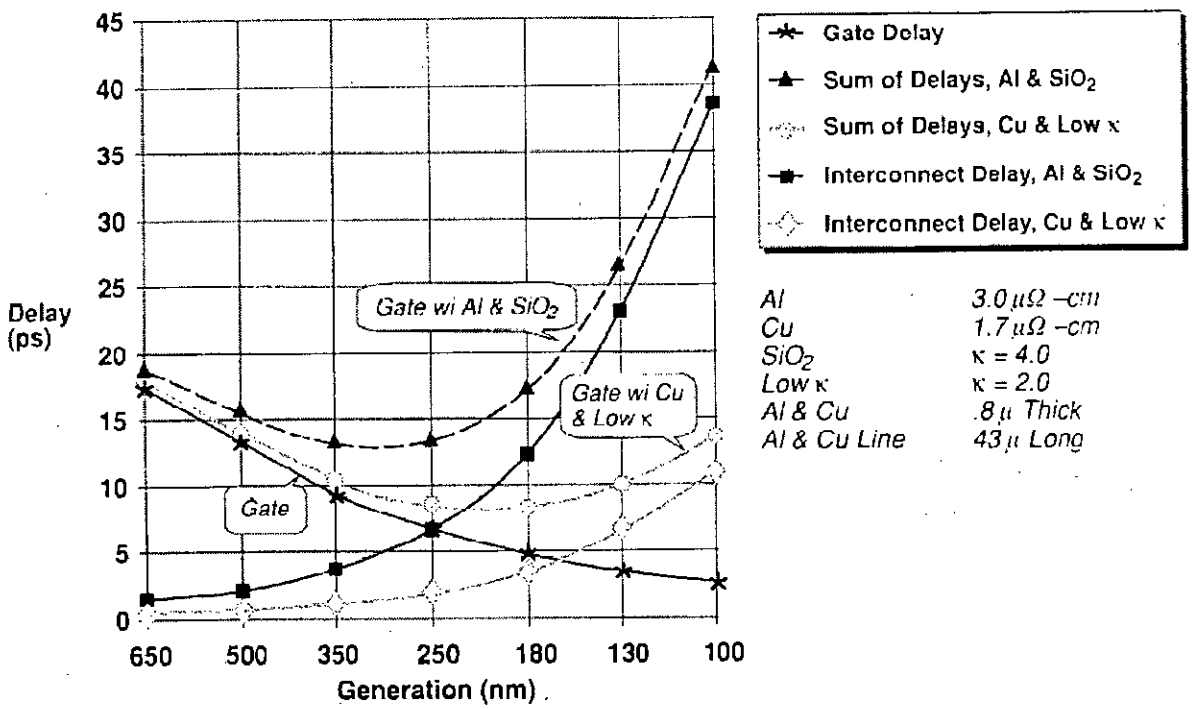


Figure 2.6: Calculated gate and interconnect delay versus technology generation [1]

2.5 Revolutionary Techniques of Interconnection

The evolutionary approaches being used to solve the problems imposed by interconnects eventually encounter fundamental materials limits. Therefore, revolutionary new techniques are needed to provide a paradigm shift to continue the progress in integrated electronics. Examples of such techniques are:

- Three-dimensional ICs with multiple layers of active devices
- Optical interconnects for on-chip and chip-to-chip interconnects
- RF/wireless interconnect for inter- and intra-chip communications

These approaches are briefly discussed and compared below.

2.5.1 3-D Integration

3-D integration of active transistor layers or, as an intermediate step placement of the clock/signal and power/ground wires on opposite sides of a chip, can reduce the number and average length of two-dimensional (2-D) global wires by providing shorter "vertical" paths for connection. A 3-D approach has also been shown to reduce overall chip area when designs are interconnect-limited. Several different schemes have been proposed for implementing 3-D integration for the advanced technology nodes as shown in Figure 2.7 [48].

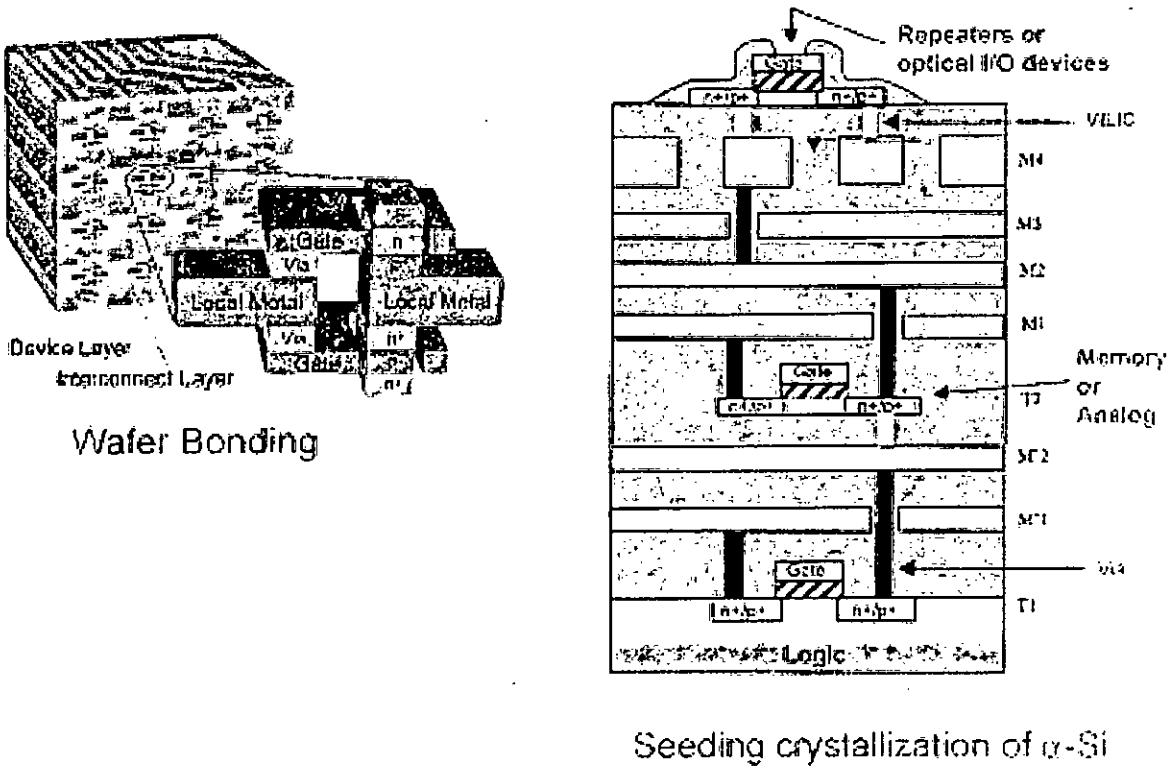


Figure 2.7: Different approaches to fabricate 3-D circuits [48]

3-D integration also offers some attractive advantages related to system performance and enabling of new system architectures. First, it can extend the performance of high-speed transistors to technology nodes where the global wires otherwise are expected to present serious frequency limitations to advanced CMOS. Second, for systems-on-chip (SOC) applications, 3-D integration may provide the means to integrate dissimilar technologies (digital, memory, analog, RF, etc.) in the same cube but on different active layers. For example, power hungry digital circuits could be located on the bottom layer adjacent to the heat sink and lower-power/higher-voltage analog circuits on the top active layer. 3-D approaches could also enable integration of huge amounts of cache memory on top of a high performance microprocessor chip.

Complex and difficult challenges remain, however, including management of thermal dissipation from interior stacked active layers, the need for 3-D routing and

placement tools, development of new systems architectures to exploit 3-D integration, etc. Furthermore, there are diminishing returns for adding more than three or four active layers to a 3-D chip. For this reason, including more than four active layers would provide no further savings in active chip area needed to realize a system function or, therefore, in cost per transistor or function.

2.5.2 Optical Interconnect

Optical interconnect technologies have long been considered as attractive alternatives to providing both inter-chip and, perhaps eventually, intra-chip replacement technology for metal/dielectric global interconnects [49]. Proposed optical approaches can be grouped into **guided wave** and **free space**. Guided wave optics involves the use of waveguides to contain the optical signals within a board, package, or on a chip. Free-space optics utilizes diffractive optics and conventional lenses or micro lens arrays to guide single or multiple parallel optical beams in free space. Figure 2.8 shows a typical view of an optical interconnect system using optical modulator and detector units.

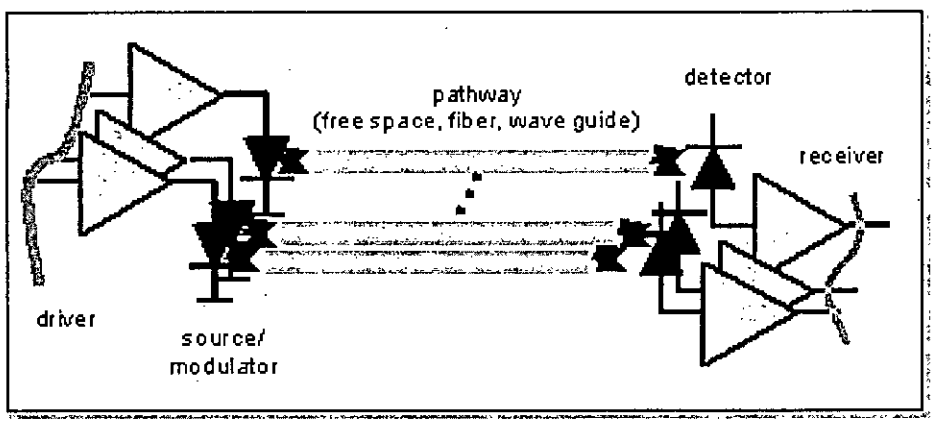


Figure 2.8: Optical interconnect concept

Compared to electrical wires, optical technology offers fundamental advantages to global interconnects, given that the technology can be realized in a simple, cost effective implementation. The bandwidth of electrical interconnects is $\sim A/l^2$, where A is

the cross section area of interconnect and l is the length. Optical interconnects, however, are not bandwidth limited in this way, although they are limited by the propagation delays of optoelectronic components such as transmitters, modulators, and receivers. Optical interconnects must overcome some rather difficult fundamental and technological challenges before they will find application as on-chip interconnects. The first issue, particularly for on-chip guided wave optical interconnects, is the relative size of optical components (particularly waveguides and photo-receiver circuits) required. For this reason, guided wave optical interconnects may require separate active layers in the vertical dimension with via interconnect to the functional blocks to support the required optoelectronic components. Power dissipation for receivers, and, to a lesser extent, transmitters can be prohibitively large. Other issues with optical interconnects are the technologies for fabricating III–V devices on silicon. Hetero-epitaxial growth of III–V vertical-cavity surface-emitting lasers (VCSELs) on silicon CMOS circuits is a very difficult technology limited by reliability concerns.

2.5.3 Wireless Interconnect

A wireless interconnect technology uses a radio technology to provide communications between functions on a large integrated circuit chip (intra-chip) as well as communications between functions on separate chips (inter-chip) located on a multichip module or on a motherboard, where distances are measured in a few to tens of centimeters and data rates are gigabits per second. The wireless interconnect technology has become possible due to the confluence of wireless communications algorithms with RF silicon processes. For example, Floyd *et al.* have demonstrated a wireless interconnect technology with integrated antennas, transmitters, and receivers in a 0.18-um CMOS process for intra-chip clock distribution at 15 GHz [5]. Zhang has evaluated the performance of a wireless interconnect technology for intra-chip data transmission at 15 GHz [50]. Chang *et al.* have implemented a wireless interconnect technology for inter-chip communications using a capacitive coupling technique and Mizoguchi *et al.* using an inductive coupling mechanism [51]. The wireless interconnect technology is a

very new approach, and much work remains to be done before becoming a viable candidate to replace global wires.

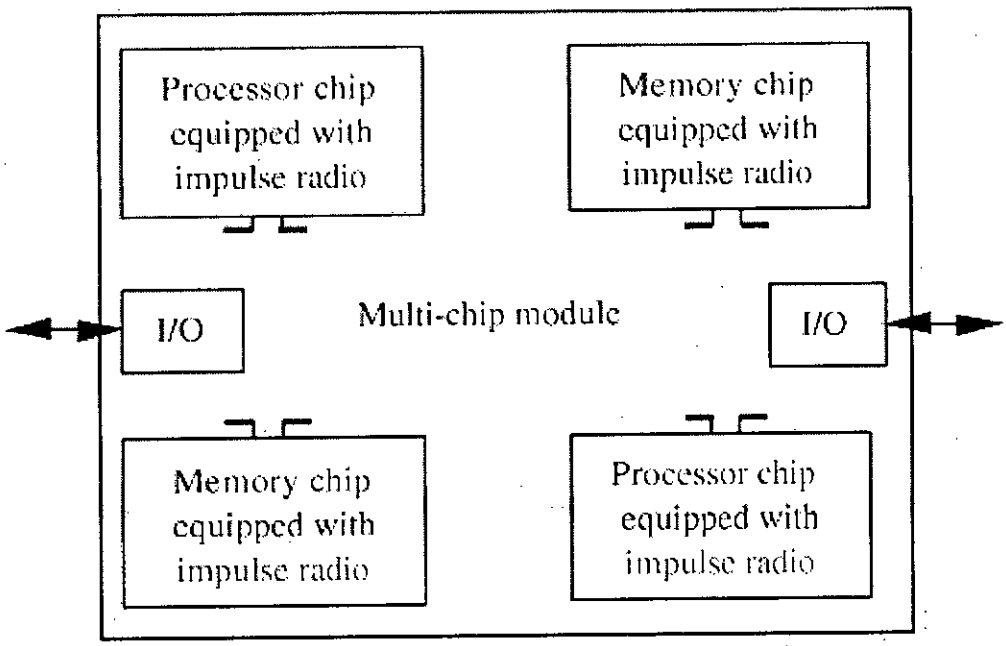


Figure 2.9: Wireless interconnect using impulse radio for interchip communication [52]

Figure 2.9 illustrates the wireless interconnect technology within a multichip module that features the use of impulse radio [52]. Conventionally, a processor chip interconnects with a memory chip in the multichip module using a peripheral component interconnect express (PCIe) circuit. The PCIe circuit is a recent industry standard in which a differential driver and a differential receiver reside on the processor chip, and a differential driver and a differential receiver reside on the memory chip. The differential driver on the processor chip is coupled to the differential receiver on the memory chip through a pair of wires. The differential driver on the memory chip is coupled to the differential receiver on the processor chip through another pair of wires. The pair of wires needs to support a high data rate of 2.5 Gbps. The PCIe standard is intended to provide architecture that can extend into the future to accommodate the ever-increasing requirements for communication performance between chips. The wireless interconnect technology employs an impulse radio to realize a wireless PCIe.

Specifically, an impulse transmitter replaces a PCIe driver, an impulse receiver replaces a PCIe receiver, and an antenna replaces a pair of wires. As compared with the conventional PCIe, the wireless interconnect technology has such advantages as scalability and reconfigurability. It can also be used at the system level to attain fault tolerance, because one can reconfigure the multichip module by software commands to debug and then to eliminate the fault chips via reconfiguration. To fully exploit the capabilities of the wireless interconnect technology for inter-chip communications, the assessment of the theoretical performance of the impulse radio over an inter-chip wireless channel appears desirable. Zheng *et al.* evaluated the performance of the binary phase-shift-keying (BPSK) impulse radio over an inter-chip wireless channel of length 20 cm [52]. The impulse radio operates with the radiated power spectral density < -41 dBm/MHz (or the average transmitted power less than -2.85 dBm) to meet the emission regulation over the UWB from 3.1 to 10.6 GHz [8].

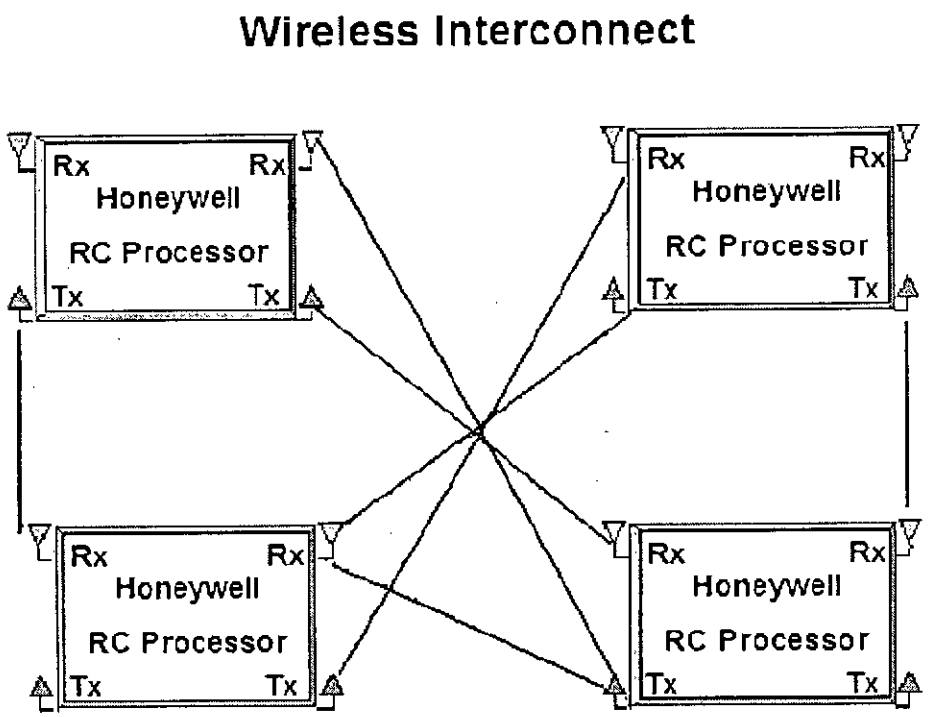


Figure 2.10: Chip-to-chip wireless links [53]

A generic board designed for multiple applications will have to be routed as depicted in Figure 2.10 [53]. Each processor, which is Field Programmable Gate Arrays (FPGAs), now has to communicate through each other if it does not have a direct trace to the device. However, a wireless link will allow the point to point communication link. Mapping new algorithms or systems that have different data rate requirements would be easily achievable with re-configuring the wireless link. With such a configurable wireless link, the data sharing and processing will allow a single device to communicate to multiple devices and vice versa. Distributed process can be easily achieved with the available bandwidth.

Compared to global electrical wires, RF interconnects potentially offer several advantages. First, circuits can be synchronized over much larger areas because wireless approach transmit signals three to ten times' faster compared to global wires. In addition, the bandwidth of the RF approaches, much like optical interconnects, is only limited by the bandwidths of the transmitting and receiving components, and not by the transmission medium, as is the case for global wires. Also, the crosstalk between channels should be much improved, particularly for the approach using FDMA and CDMA communication techniques.

RF interconnect has to overcome some difficult challenges before becoming a viable candidate to replace global wires. First, for package applications, the RF implementation must be cost competitive with conventional interconnect systems. Further, the power dissipated by RF interconnect support circuits must be equal to or less than the power dissipated by the global interconnect wires, and the silicon area consumed by these RF circuits must only be a small fraction of the chip size . Also, the RF power dissipation cannot add a significant amount of heat to an already heavy thermal load. Finally, similar to optical interconnects, RF interconnect systems will likely require adaptation of new system architectures to fully exploit the capabilities of RF interconnects.

Though both optical and wireless interconnect schemes are simultaneously evaluated as a new technology solution for the future ULSI, the later shows a number of promising advantages.

- Optical interconnect requires conversion of electrical signal into optical signal at the transmitter side and optical signal to electrical signal at the receiver end. Optical devices are fabricated using III – V group which are not compatible with existing Si technology and hence costly to implement. On the other hand wireless interconnects provide completely CMOS compatible architecture.

- The relative size of optical components (particularly waveguides and photo-receiver circuits) compared to chip circuitry is a critical design constraint. That is why, optical interconnects may require separate active layers in the vertical dimension with via interconnect to the functional blocks to support the required optoelectronic components. To the contrary, no special guided wave mechanism is required for on-chip wireless interconnect hence it reduces the electronic overhead on the existing circuit components.

CHAPTER 3

UWB WIRELESS CHIP-TO-CHIP COMMUNICATION

Ultra-wideband (UWB) is a promising technology for networks requiring a very high data rate at short distances. Chip to chip, board to board, and box to box interconnects can also make use of an UWB based wireless link. In these cases, the distances are even shorter compared to a networking application, and the UWB designer can take advantage of this fact for high speed link. After providing some basic fundamental definitions on UWB techniques, this chapter describes the proposed architecture for UWB transceiver intended to use for on-chip wireless interconnects. The ultimate shape of the transmitting UWB pulse capable of both carrying high data rate and satisfying the FCC regulations is also investigated at the end of this chapter.

3.1 Motivations for Developing UWB System

Modern integrated circuits require high capacity channel to communicate between chips and also within the chips. According to Shannon's channel capacity theorem [54]. channel capacity C is given by

$$C = B\log_2\left(1+\frac{S}{N}\right) \tag{3.1}$$

where, B is the bandwidth, S is the total signal power, and N is the total noise power. It is clear that the channel capacity (data rate) increases linearly with the bandwidth and logarithmically (and hence weakly) with the signal-to-noise ratio (SNR). For fixed SNR we, therefore, need huge bandwidth for high capacity or bit rate for example, 10-20 Gbps or even more. Since ultra wideband, as its name implies, provides large bandwidth, we

have moved from traditional narrowband system to UWB technology for on-chip wireless interconnects.

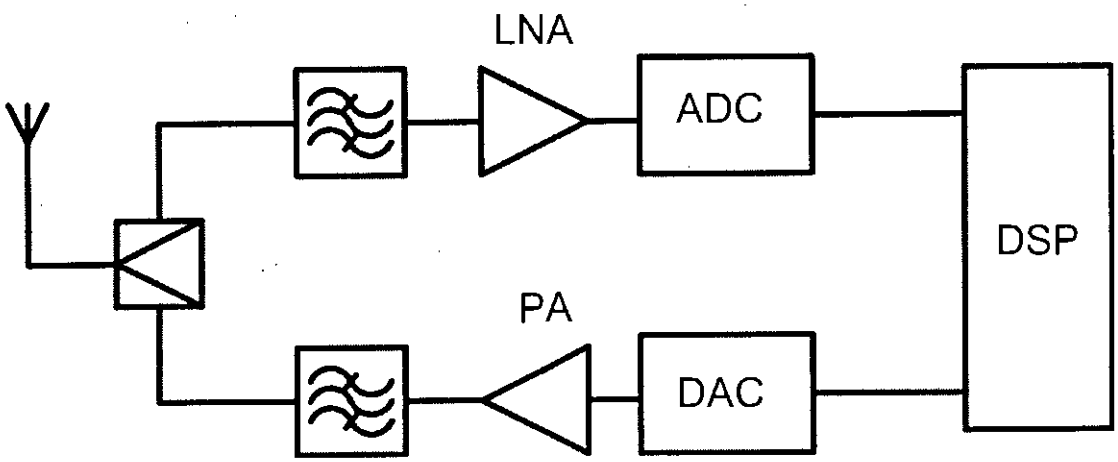


Figure 3.1: Block diagram of the impulse-radio transceiver [55]

The UWB system not only helps achieve high data rates, but also allows operation at a significantly lower signal power than narrowband systems, with only a minor effect on channel capacity [17]. Figure 3.1 shows an ideal UWB transceiver architecture used in an impulse-radio transceiver [55]. Many components, including frequency synthesizers, down-conversion mixers, up-conversion mixers, image-rejection filters, and channel-selection filters, that are used in narrowband transceivers can be eliminated from a UWB transceiver. Signal processing tasks such as modulation, demodulation, channel selection, and filtering that were previously performed by the RF and analog circuits in narrowband transceivers can now be executed in the digital domain by the baseband digital signal processing (DSP) circuits [55]. Many advantages can be achieved by using fewer RF circuits, including reduction in the hardware, power, cost, and number of design cycles, as well as high integration and more flexibility. Also, the low RF signal power of the UWB system further reduces the transceiver's power consumption. The ability of a UWB communication system using modulated short pulses to operate without a carrier signal allows a very efficient use of the signal spectrum [56]. The PSD of UWB systems (Figure 3.2) is so low (lower than -41.3 dBm/MHz) that it does not cause any interference with

existing narrowband communication systems in the same frequency band. For instance, a 802.11.a (5 GHz) system would not be affected at all by UWB signals [57]. All these remarkable properties strengthen our choice for employing UWB system.

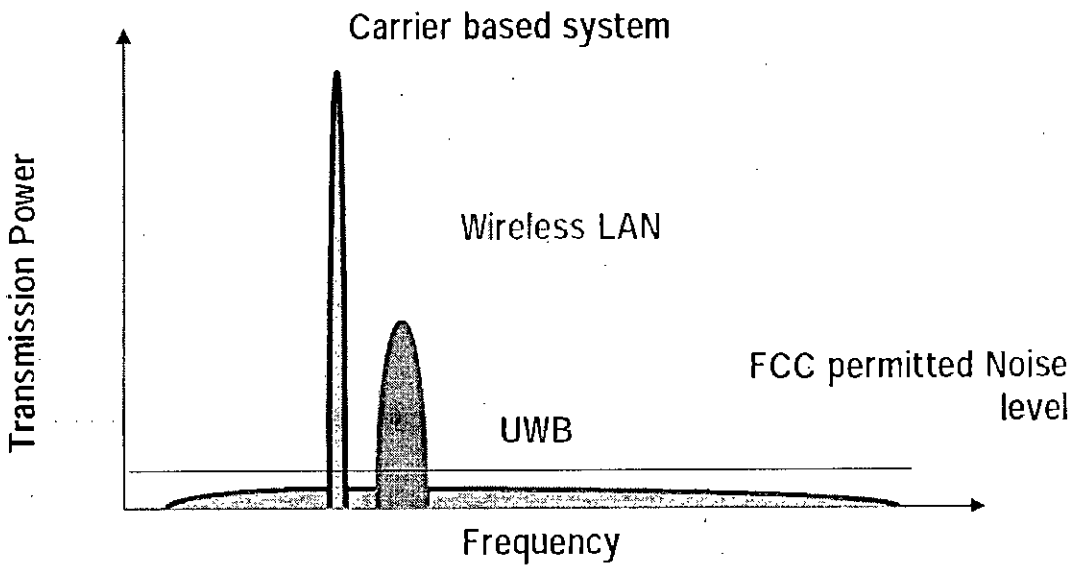
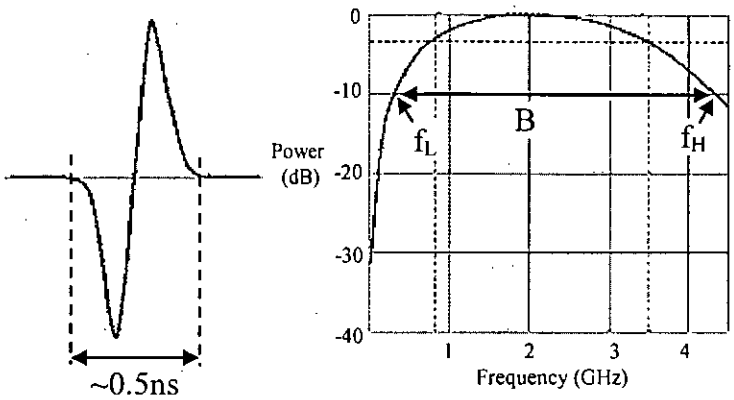


Figure 3.2 PSD of different wireless communication systems

3.2 Fundamentals of Ultra-Wideband System

3.2.1 UWB Definition

UWB technology is generally defined as any wireless transmission scheme where the fractional bandwidth is greater than 20% or occupies 500MHz or more bandwidth. The fractional bandwidth is defined as B/f_c, where $B=f_H - f_L$ denotes the -10 dB bandwidth and center frequency $f_c = (f_H + f_L) / 2$ with f_H being the upper frequency of the -10 dB emission point, and f_L the lower frequency of the -10 dB emission point as depicted in Figure 3.3.



(a) Time domain (b) Frequency domain

Figure 3.3: Ultra wideband signals

The main core of the technology is the usage of the pulse-code modulation of ultra wide band signals for data transmission. Instead of transmitting a continuous carrier wave modulated with information or with information combined with the spread code, which determines the bandwidth of the signal, a UWB radio system transmits a series of very narrow impulses, typically with the pulse widths of about 0.5 ns.

The intervals between these pulses may vary from 0.1 to 100 ns. These short time-domain impulses take the form of a single cycle, or Gaussian monocycle transformed into the frequency domain result in the ultra wideband spectrum. Indeed, the central frequency f_c is roughly inverse to the width τ of the pulse $f_c \sim 1/\tau$, so for the single impulse with the width of 0.5 ns the central frequency is about 2 GHz.

3.2.2 UWB Advantages

UWB is a newly developed carrier less wireless RF technology, and is considered to be a potential solution to a wide range of RF problems. UWB transmitters transmit trains of extremely short pulses at precise time intervals, resulting in a very low power signal that can coexist with other radio systems. Its features can be summarized as:

- Ultra wideband and ultra-low PSD
- Extremely low transmission energy
- Very high data rate
- Base-band communications
- Excellent immunity to interference from other radio systems
- Excellent multipath immunity
- Low probability to intercept
- Nearly 'all digital' architecture with simple CMOS circuitry
- Commonality of signal generation and processing architectures
- Potentially small size and processing power
- Low cost

Ultra Wideband is a promising technique for wireless communications. In contrast with the conventional communication systems using the "sine wave", UWB information is carried in very short pulse, which covers an extremely wide spectrum bandwidth. So, the RF and analog receiver circuitry is reduced to a wide band low-noise amplifier, a correlator and data converters. **No up down conversion is needed**, which results in **substantial reduction of transceiver area, power**, and can be integrated with **low price CMOS circuit**. UWB is a carrier-free (base-band) technique, which will greatly **reduce the complexity and cost** of the transceiver.

A very wide bandwidth means better multipath mitigation, interference mitigation by using spread spectrum techniques, more users and high data rate. Short impulse (typically <1ns) prevents destructive interference from multipath and the multipath components can be individually resolved. Carrier-less nature of waveform results in less fading, even when pulses overlap. This reduces fade margin in link budgets.

This ultra wideband signaling scheme is particularly attractive for wireless interconnect systems for several reasons. **First**, it creates less electrical overhead on the existing circuitry of the chip because of its simplified transceiver architecture. UWB systems can be made nearly "all digital", with minimal RF and microwave electronics. **Second,** on chip antenna can be effectively utilized to transmit UWB pulse thus avoiding

expensive and power hungry analog components. **Third,** to achieve a high data rate with low BER using conventional data transmission technique, one needs a substantial amount of transmitted power. Large transmitted power results in increased power consumption, which generates extra heat in the chip. Since UWB systems use ultra short pulses to transmit data, active signal occupies a small fraction of the total transmission time and hence the average power requirement is very low.

Therefore, low power, low cast and very wide bandwidth make carrier less UWB technology an attractive competitor in wireless interconnect system design.

3.2.3 UWB Signaling and Pulse Shapes

UWB is a base-band technology, and thus the choice of the monocycle shape will affect the performance. Several possible monocycles for UWB are listed below [41].

i. Gaussian pulse

The Gaussian pulse often used to model UWB signal can be represented by

$$p(t) = Ae^{-\frac{(t-\mu)^2}{2\sigma^2}} \tag{3.2}$$

where,

A is the pulse amplitude (volts)

t is time (seconds)

σ is the standard deviation of the Gaussian pulse (seconds)

μ is the mean value of the Gaussian pulse (seconds)

ii. Gaussian Monocycles

The Gaussian monocycle is similar to the first derivative of the Gaussian pulse and is given by

$$p'(t) = -\frac{A}{\sigma^2}(t-\mu)e^{\frac{(t-\mu)^2}{2\sigma^2}} \tag{3.3}$$

iii. Scholtz's Monocycles

This monocycle appears in Dr. Scholtz's papers, so we call it Scholtz's monocycle. It is similar to the second derivative of the Gaussian pulse and can be represented by

$$p'(t) = \left[-\frac{A}{\sigma^2} + \frac{A}{\sigma^4}(t-\mu)^2 \right] e^{-\frac{(t-\mu)^2}{2\sigma^2}} \qquad (3.4)$$

iv. Higher Order Gaussian Monocycles

Higher order derivatives of Gaussian monocycles are also widely used in the design of UWB transmitter depending on the system power spectrum requirements.

The time domain waveforms of Gaussian pulse, Gaussian monocycles, Scholtz's monocycles along with their power spectrum densities are illustrated in Figure 3.4. As shown in figure, Gaussian pulse has dc spectral components, which may reduce the antenna radiating efficiency and, therefore, basic Gaussian pulse is normally not used in UWB systems. **Moreover, Gaussian and its nth-derivative pulses are favored over other waveforms, e.g. rectangular and sinusoidal, for UWB since their side lobes have the smallest energy.**

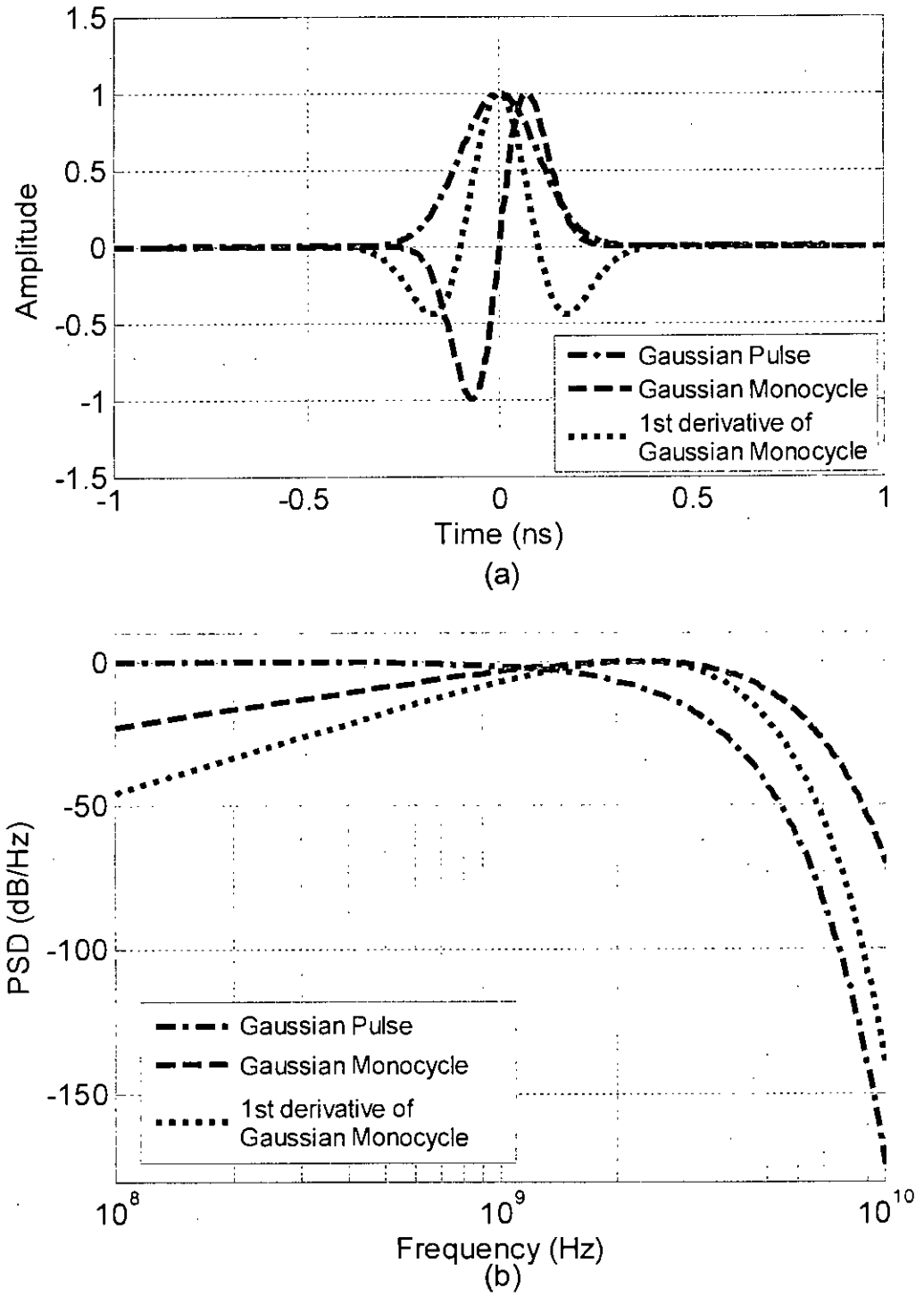


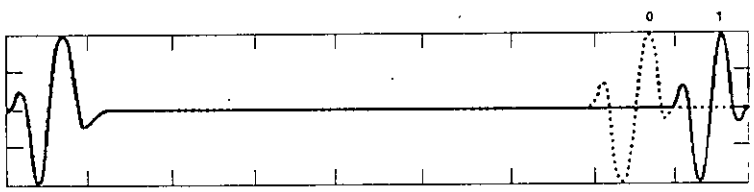
Figure 3.4 (a) Generally adopted Gaussian pulse shapes in UWB communication (σ = 0.1ns)
(b) Fourier transform of the pulse shapes

3.3 Modulation Types

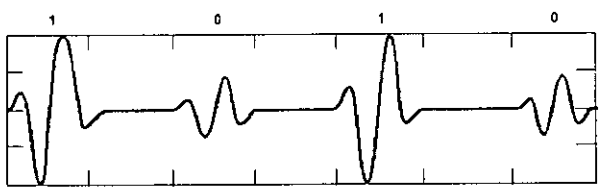
Although numerous modulation techniques are used with impulse-radio UWB, three common schemes are often found in research papers and journals. On-Off Keying (OOK), Bipolar Phase Shift Keying (BPSK), and Pulse Position Modulation (PPM) are popular UWB modulation techniques due to their simplicity and flexibility towards low duty cycle pulsed communication systems. The basic techniques of signal transmission under different modulation schemes are outlined in Figure 3.5.

Binary Modulation:

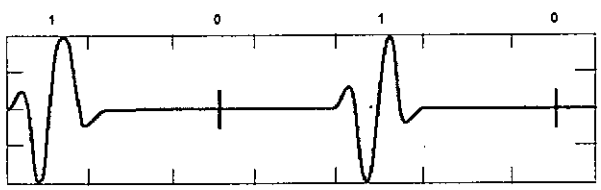
- Pulse Position Modulation (PPM)



- Pulse Amplitude Modulation (PAM)



- On Off Keying (OOK)



- Bipolar Phase Shift Keying (BPSK)

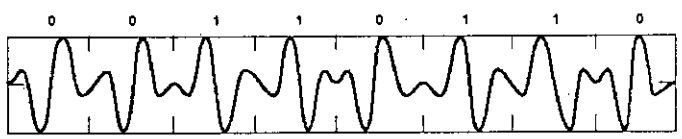


Figure 3.5: Common UWB modulation techniques

3.3.1 On Off Keying (OOK)

On Off Keying is the simplest pulse modulation technique where a pulse is transmitted to represent a binary "1", while no pulse is transmitted for a binary "0", as depicted in Figure 3.5.

One obvious advantage of using OOK is the simplicity of the physical implementation, as one pulse generator is necessary, as opposed to two, as is the case with bi-phase modulation. A single RF switch can control the transmitted pulses by switching on for a "1" data bit and off for a "0" data bit. This effortless transmitter configuration makes OOK popular for less complex UWB systems. Although OOK has a very straightforward implementation, there are some system drawbacks. In either a hardware or software based receiver design, synchronization may be lost if the data contains a steady stream of "0's".

3.3.2 Binary Phase Shift Keying (BPSK)

The most common form of PAM in UWB communications is bipolar phase shift keying (BPSK), where the polarity of a pulse is modulated. In this situation, a positive pulse is transmitted for a "1" and a negative pulse is transmitted for a "0".

One advantage of BPSK modulation is its improvement over OOK in BER performance. Another benefit of bi-phase modulation is its ability to eliminate spectral lines due to the change in pulse polarity. This aspect minimizes the amount of interference with conventional radio systems. A decrease in the overall transmitted power could also be attained, making bi-phase modulation a popular technique in UWB systems when energy efficiency is a priority. A disadvantage of bi-phase modulation is the physical implementation is more complex, as two pulse generators, one of them with the opposite polarity, are normally necessary instead of one, as is the case with OOK. This presents a problem when attempting to transmit a stream of pulses, as the time between pulses can become non-periodic if the pulse generators are not triggered in a timely fashion.

3.3.3 Binary PPM

The last popular UWB modulation scheme to be discussed is PPM, which is a technique where the timing of each pulse is altered to transmit data instead of varying the amplitude. The simplest form of PPM is binary PPM, where a pulse in a uniformly spaced pulse train represents a "0" and a pulse offset in time from the pulse train represents a "1." Conceptually, the binary PPM technique is shown in Figure 3.5.

The most advantageous feature of PPM is the orthogonal signaling present in its data. Each of the pulses in time is independent of one another, meaning the time during the symbol period can be broken up to look for each pulse within a specified time slot. In the case of M-ary modulation schemes, PPM provides better error performance than PAM and also has the advantage of permitting non-coherent reception. One of the disadvantages of PPM is its poor BER performance. Another apparent drawback to PPM is its susceptibility to inter-symbol interference, as multiple positions are required to transmit at a higher data rate. PPM must lower the transmitted pulse rate to account for this effect. Therefore, there is a data rate limitation when using M-ary PPM in impulse-radio UWB applications. Even when the inter-symbol interference is reduced at the transmitter by decreasing the pulse rate, multipath are more likely to overlap with the next data pulse, causing bit errors at the receiver if the reflections are strong. These types of problems lead to a more complex receiver design, which hampers the use of PPM.

3.4 IR-UWB Architecture for Interconnects System

Since UWB wireless interconnects is a new technology, very few system architectures are found in the literature. Zheng *et al.* [52] proposed a block diagram of the UWB impulse-radio transceiver architecture as shown in Figure 3.6. The building blocks of the UWB transmitter comprise a UWB Gaussian pulse generator, modulator, and a UWB driver amplifier (DA). The Gaussian pulse generator generates a UWB Gaussian pulse and the UWB pulse modulator modulates the pulse. The modulated UWB Gaussian pulse is then amplified by the UWB DA. Subsequently, the UWB antenna transmits the

amplified pulse wirelessly. The receiver consists of a UWB low-noise amplifier (LNA), a correlator (including a multiplier and integrator), an analog-to-digital converter (ADC), and clock generation and synchronization circuits. The UWB LNA is matched to the UWB antenna by means of a matching network. The purpose of the UWB LNA is to amplify the received pulses to a suitable level for signal processing as well as to provide enough gain so as to overcome noise in subsequent stages. The data is subsequently recovered by the correlator. The ADC is used to convert the analog demodulated signal into the digital signal. The digital baseband provides control for the clock generation, synchronization, and data processing.

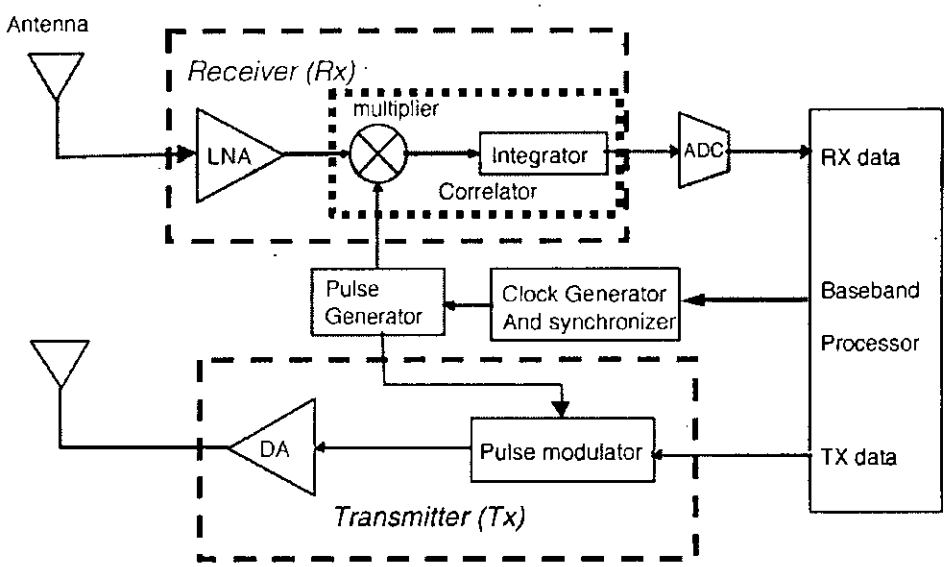


Figure 3.6: Conventional Architecture of UWB wireless transceiver [52]

A similar architecture was also proposed by Jin *et al.* for wireless interconnects [14]. Although these architectures serve the purpose, they have some basic limitations which will be prominent in future high speed communications. First, a reliable technique should be built in order to synchronize the pulses used in the correlator. None of them has mentioned this technique. On the other hand, for coherent demodulation, we need to distribute the same clock among all the chips and also within the chip. This introduces another issue of clock distribution whether it is wired or wireless.

Secondly, the template pulse used for the correlator block is shown the same as the transmitted pulse. But, in general, the received pulses are the derivatives of the transmitted

pulses. Therefore, the effect of antenna on signal transmission is not considered which is clearly discussed in the later sections.

Thirdly, integrator and analog to digital converter (ADC) are used at the receiver. To facilitate the A/D conversion, the integrator should be made as lossless as possible. Also the integration response time should be short so that the ADC would have enough time to perform conversion. This means that the integrator should have a high slew rate and fast settling behavior.

3.5 Proposed Transceiver Architecture

Determining the architecture of UWB transceiver for on-chip wireless interconnects application is a critical issue. Rake, transmitted-reference (TR), differential detector, and energy detector (ED) are the four most popular UWB receiver architectures investigated in the literature. To make a selection among these options, there are several aspects to be taken into account. For instance, UWB Rake receiver provides high data rate (typically up to several Gbps) but with the cost of a highly complex circuitry. On the other hand, the ED receiver architecture provides lower data rate (typically 1-100 Mbps) but with much lower complexity. One of the factors that influence the hardware complexity in a UWB transceiver is the use of either all-digital or mixed analog-digital components. Although all-digital Rake receiver provides reconfigurability, scalability, and a high data rate it is burdensome to implement an all-digital Rake receiver with the current technology. The RF components and digital hardware required to design a Rake receiver are expensive, and designing such components comes with some challenges. Therefore, low-complexity UWB system architecture such as TR transceiver using mixed analog-digital components is considered.

First to solve the last problem mentioned in the previous section, we have replaced the integrator by a low pass filter as shown in Figure 3.7. As shown in the figure, the receiver is based on the correlation between the received pulse and a template pulse. This means that a template signal is to be correlated with the received signal in order to derive

the information from the incoming signal. A general correlator is simply a multiplier circuit (mixer) followed by a low pass filter (LPF) circuit. The output of the LPF is fed to a comparator that monitors the output of the LPF and performs the analog to digital conversion (ADC) for the receiving bit. The remaining first two problems are solved by using TR scheme which is described below.

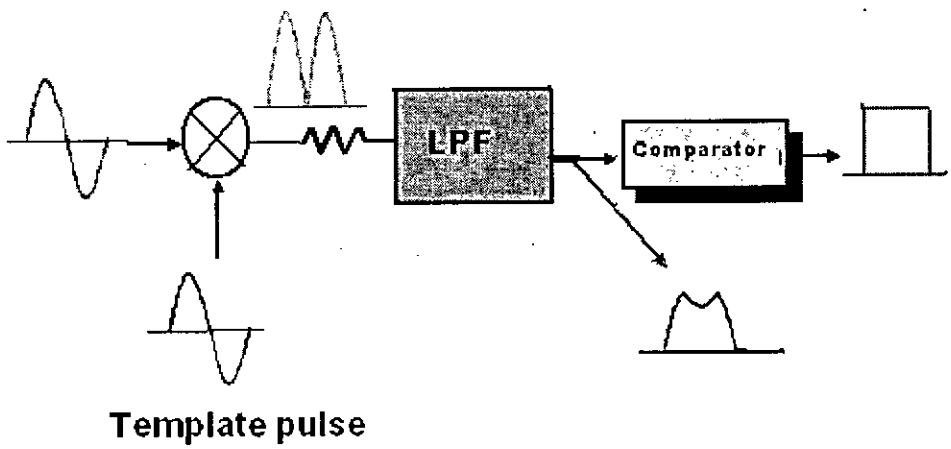


Figure 3.7: Signal demodulation using LPF

3.5.1 Definition of Transmitted reference (TR)

One of the low-complexity forms of transmitted reference (TR) system transmits a pair of pulses in each frame. The first one is not modulated and used to provide the multipath channel's pulse response function to the demodulator, while the second one is data-modulated. The transmitted signals corresponding to data bit '1' and '0' for BPSK and OOK modulations, respectively, are shown in Figure 3.8.

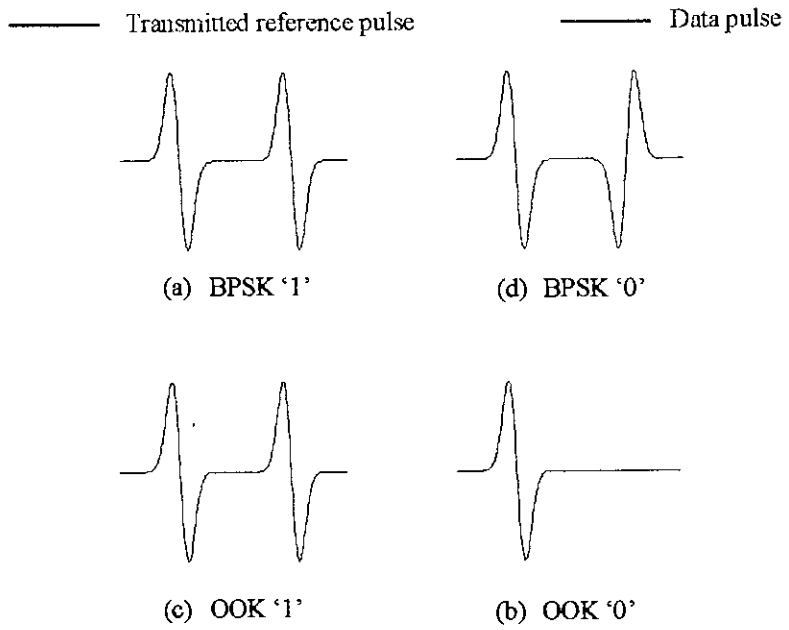


Figure 3.8: Gaussian monocycle pulses with transmitted reference; (a) and (b) represent BPSK '1' and '0' respectively; (c) and (d) represent OOK '1' and '0' respectively

3.5.2 Importance of Transmitted Reference in Wireless Interconnects Systems

When a UWB pulse travels through the RF channel, it usually gets distorted, which leads to the reception of replicas of the pulse with different delays, amplitudes, phases or even different shapes. Usually, distortion is partially compensated for or equalized at the receiver by way of channel estimation and some proper receiver design. However, for highly dispersive channels such as the ones created by UWB radios, effective channel estimation and the associated receiver design to equalize the channel and to collect enough energy for data detection are difficult.

Moreover, it has been found that the received UWB pulse is the time derivative of the transmitted UWB pulse in case of on-chip wireless interconnects through dipole antenna on silicon substrate. For example, Figure 3.9 shows a typical transfer function of a dipole antenna pair formed on silicon substrate. The received UWB pulse through this antenna is seen to be the derivatives of the transmitted pulse as depicted in Figure 3.10.

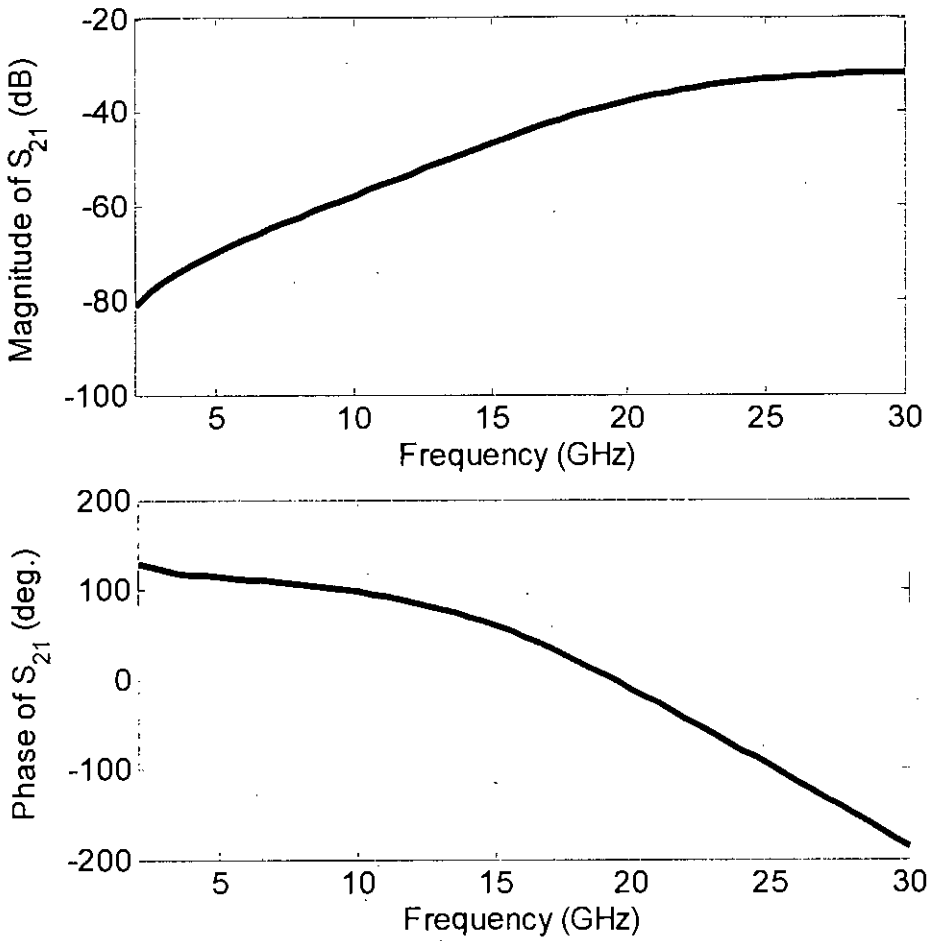


Figure 3.9: A typical transfer function of silicon integrated dipole antenna pair for on-chip wireless interconnects

Therefore, using the transmitted pulse as the template in the mixer circuit one would have erroneous results at the receiver. It is also difficult to predict the shape of the received signal pulse since it varies significantly depending on the transfer function of the channel which in turn depends on the geometry and property of the materials used to develop the channel. To solve the above problems, a radio design philosophy, called transmitted reference signaling scheme, is proposed and utilized in this thesis for on-chip wireless interconnects.

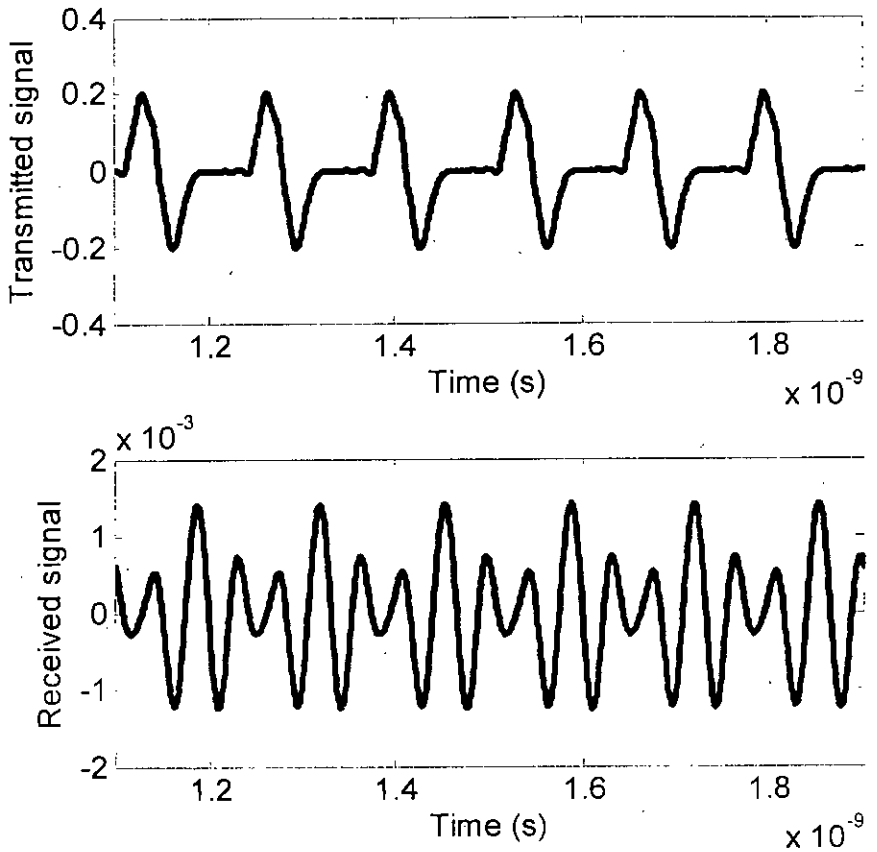


Figure 3.10: Transmitted and received UWB signals through on-chip dipole antenna pair

The advantage of a TR system is its ease of implementation because channel estimation is not required. However, the most significant drawback is the noise-cross-noise signal that appears at the correlator output, which severely degrades the performance at low pulse SNR. TR systems also waste communication resources, i.e., power and time, to transmit reference signals.

3.5.3 UWB Pulse Generator with TR Pulse

A transmitted signal including TR pulses can be generated by delaying the pulse signal and adding the modulated pulse to the original pulse signal as illustrated in Figure 3.11.

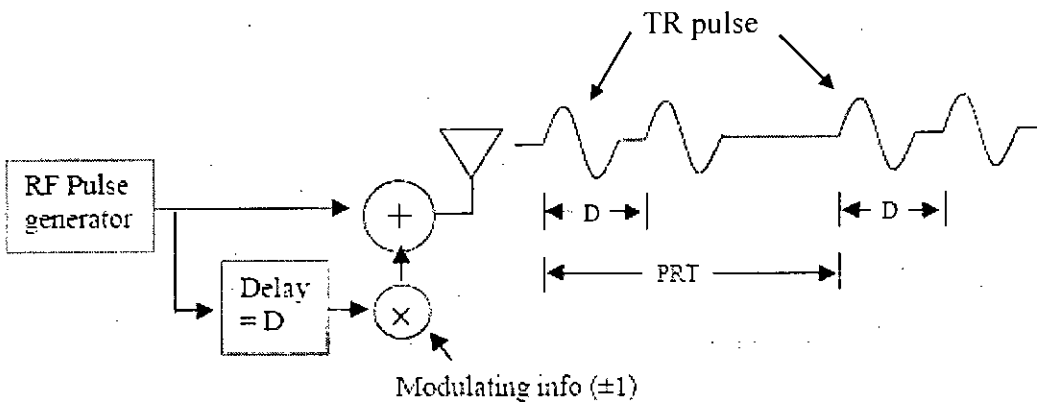


Figure 3.11: Conventional Scheme for generating TR UWB pulse

In the next chapter, we have developed a novel UWB transmitter suitable for on-chip wireless interconnects which transmits a TR pulse along with each data pulse **without employing any delay and adder circuits.**

3.5.4 Receiver Architecture for the Proposed Model

The UWB receiver of the proposed data transmission system is similar to the conventional receiver except for the demodulator circuits. Due to the problem of channel estimation discussed in section, the conventional receiver using an external pulse as template is no longer suitable for on-chip RF wireless interconnects. To solve this problem, a TR pulse is attached to every data pulse and the response of the TR pulse at LNA output is taken as the template pulse. At the receiver side, a simple delay line and a cross-correlator is used to demodulate the data symbols. A delay unit with delay, *D* is used to synchronize the TR pulse with the data pulse and both the pulses are then fed to the mixer

to extract the information bit. Depending on the transmit signal the output signal of the correlator is the correlation of the reference signal with the information signal as shown in Figure 3.12.

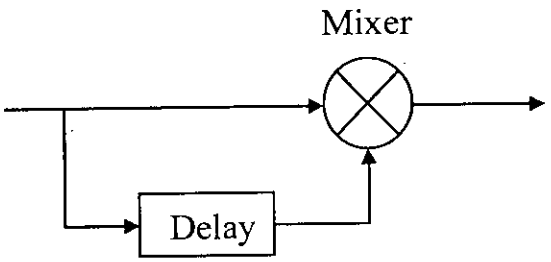


Figure 3.12: Demodulator used in UWB receiver for wireless interconnects

3.5.5 Self Synchronized Complete Transceiver Architecture for on-chip Wireless Interconnects

After gathering some knowledge about the transmitter and the receiver separately, we are now in a position to describe the whole transceiver architecture by combining the two parts. The proposed single link transceiver being designed targeting on-chip wireless interconnects system using ultra wideband communication technology is presented in Figure 3.13. The developed wireless transceiver architecture is based on TR system and UWB pulse is used as transmitting pulse to achieve carrier less high rate data transmission. The system is self synchronized in the way that no clock is required in the receiver.

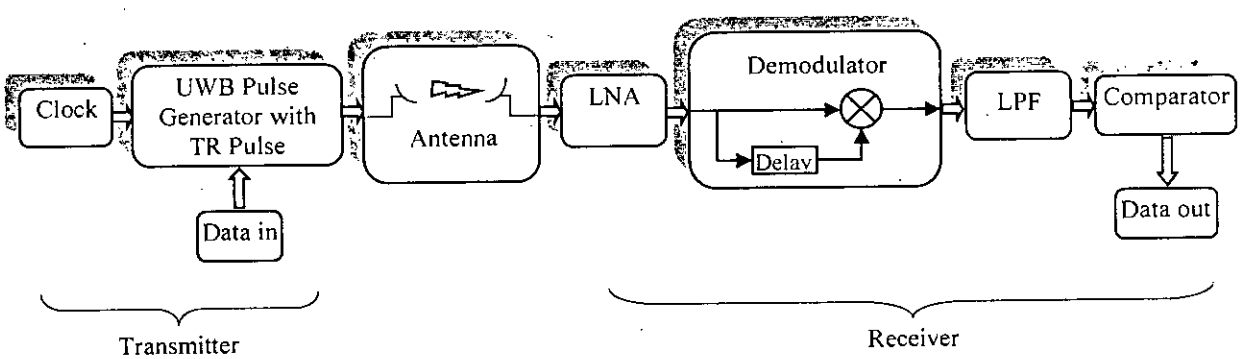


Figure 3.13: Proposed Single Link UWB Communication System Architecture for on-chip Wireless Interconnects

The complete system comprises of the following basic elements:

- Clock generator
- UWB pulse generator with TR pulse
- On-chip wireless antenna
- Low noise amplifier (LNA)
- Demodulator (Delay and Mixer)
- Low pass filter
- Comparator

In our proposed data transmission technique, information is contained in the amplitude or phase of the data pulses. The transmitted signal, *s(t)*, is given by,

$$s(t) = p'(t) + s \cdot p'(t - D) \tag{3.5}$$

where, *p'(t)* denotes the UWB pulse shape (Gaussian monocycle), *s* is the data symbol and *D* is the bit-independent delay between the TR pulse and the data pulse. For BPSK modulation, $s \in \{-1; 1\}$ and for OOK modulation, $s \in \{0; 1\}$ and each corresponding signal already shown in Figure 3.8 represents 1 bit value.

The signal states at different stages of the data communication system are presented in Figure 3.14 and 3.15.

OOK SYSTEM

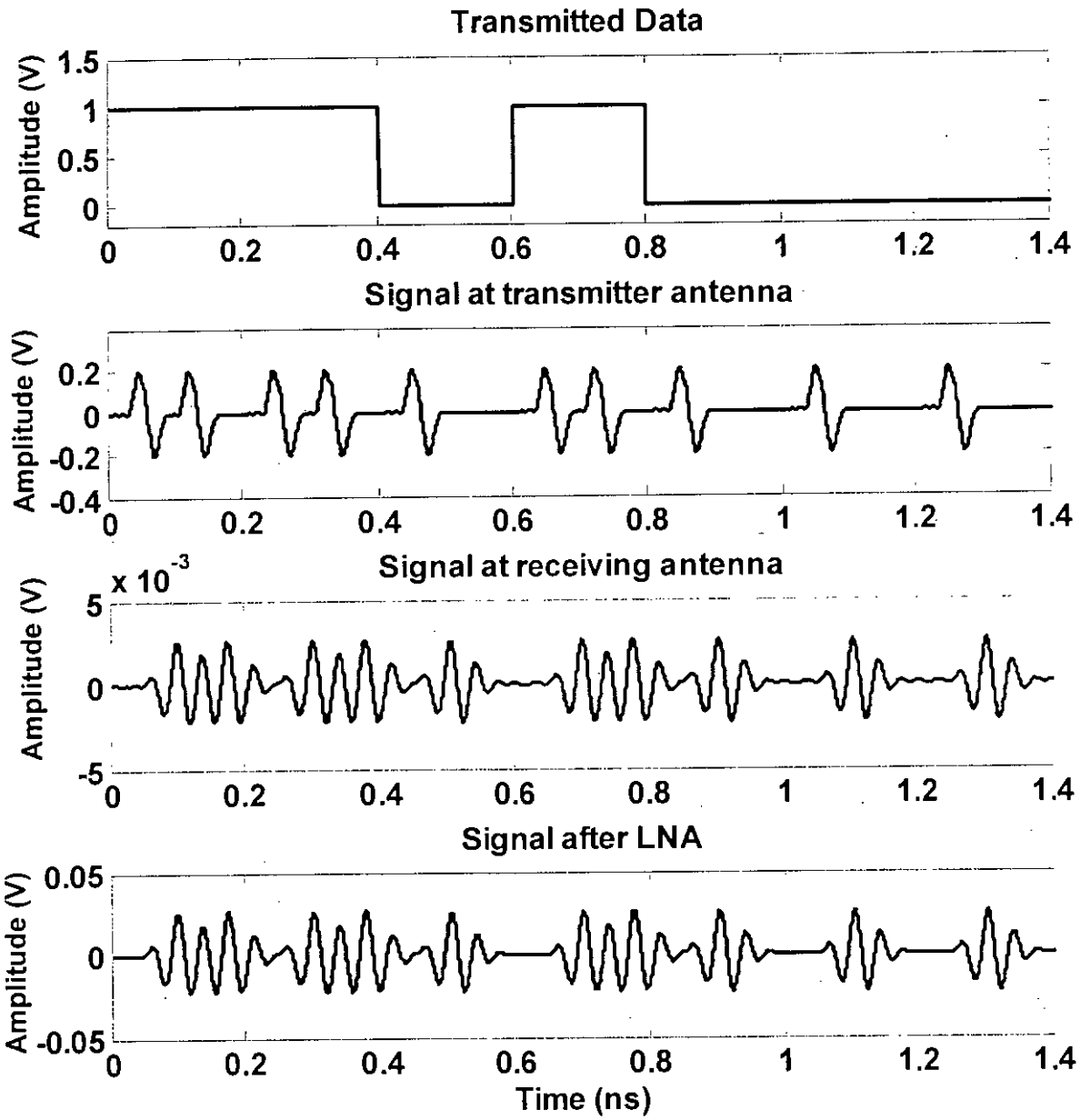


Figure 3.14: Signal conditions at different stages of the proposed transceiver for OOK modulation

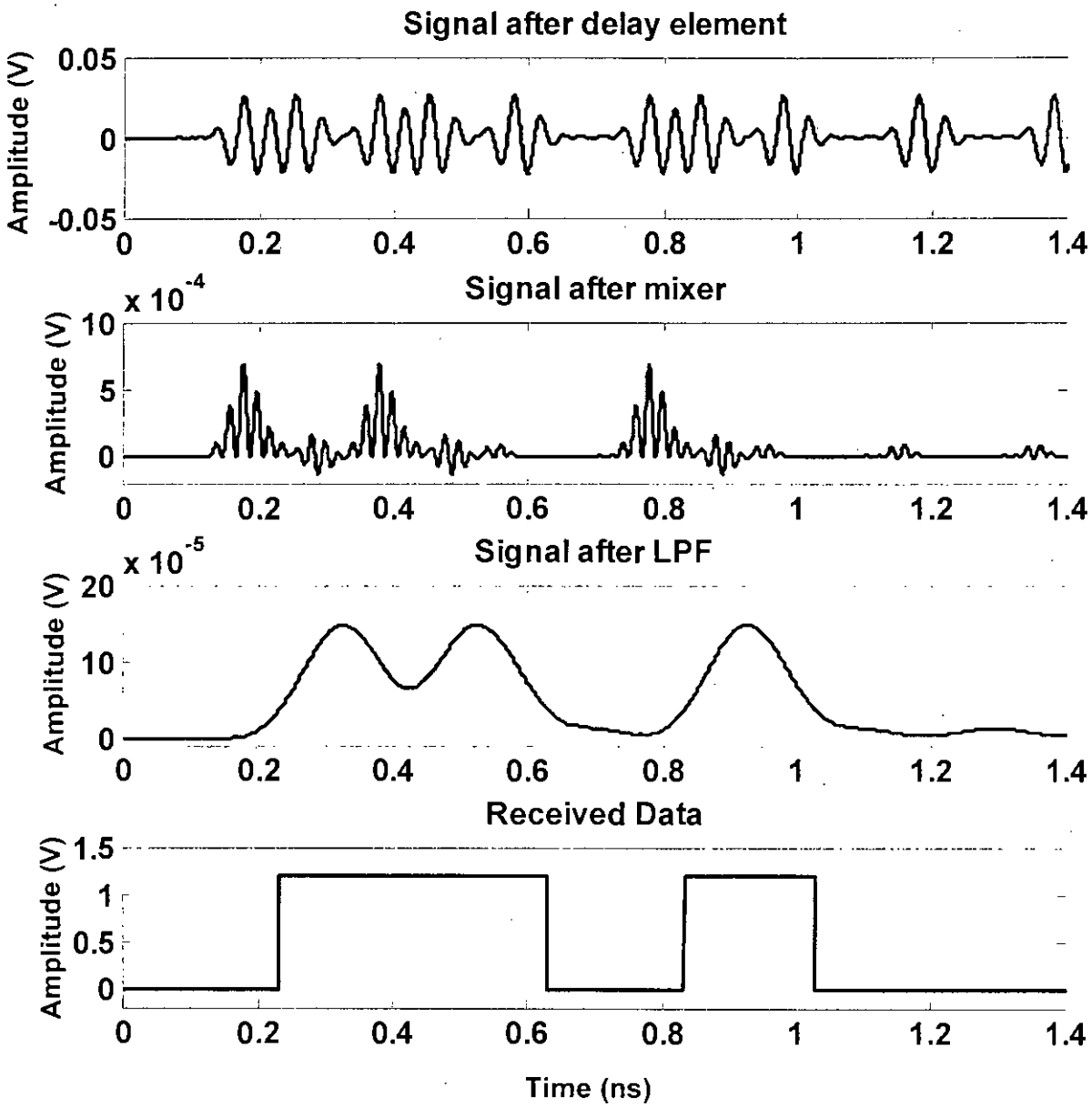


Figure 3.14: Signal conditions at different stages of the proposed transceiver for OOK modulation (continued...)

BPSK SYSTEM

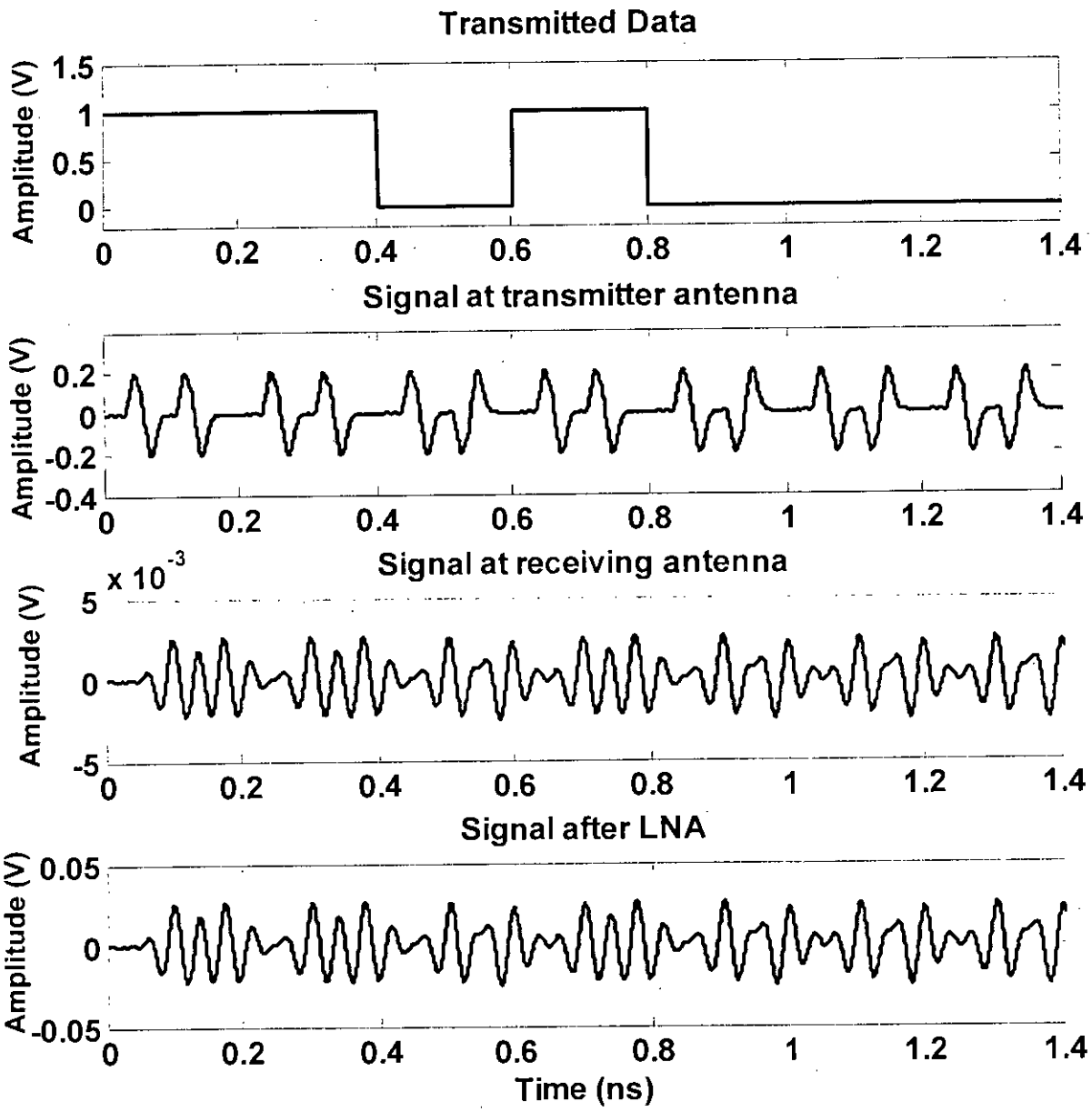


Figure 3.15: Signal conditions at different stages of the proposed transceiver for BPSK modulation

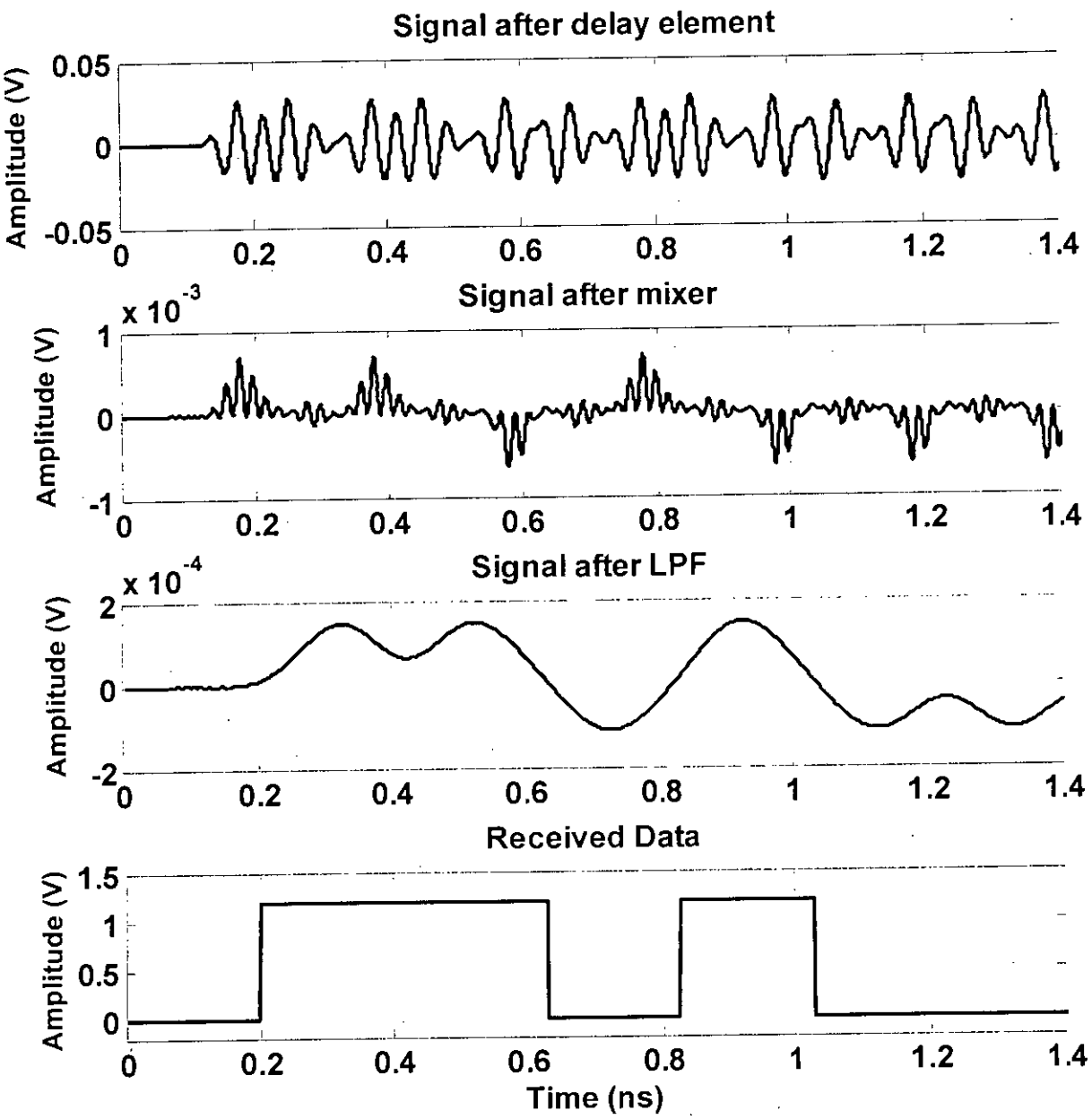


Figure 3.15: Signal conditions at different stages of the proposed transceiver for BPSK modulation (continued...)

3.6 FCC Regulations and UWB pulse Shape for Chip Interconnects

The Federal Communication Commission (FCC) has released an unlicensed 3.1–10.6-GHz frequency band for ultra-wideband (UWB) related applications, where UWB transmission is defined as the occupied fraction bandwidth 20% or larger than 500 MHz of absolute bandwidth [8]. According to FCC, the transmitted power should be under the mask shown in Figure 3.16.

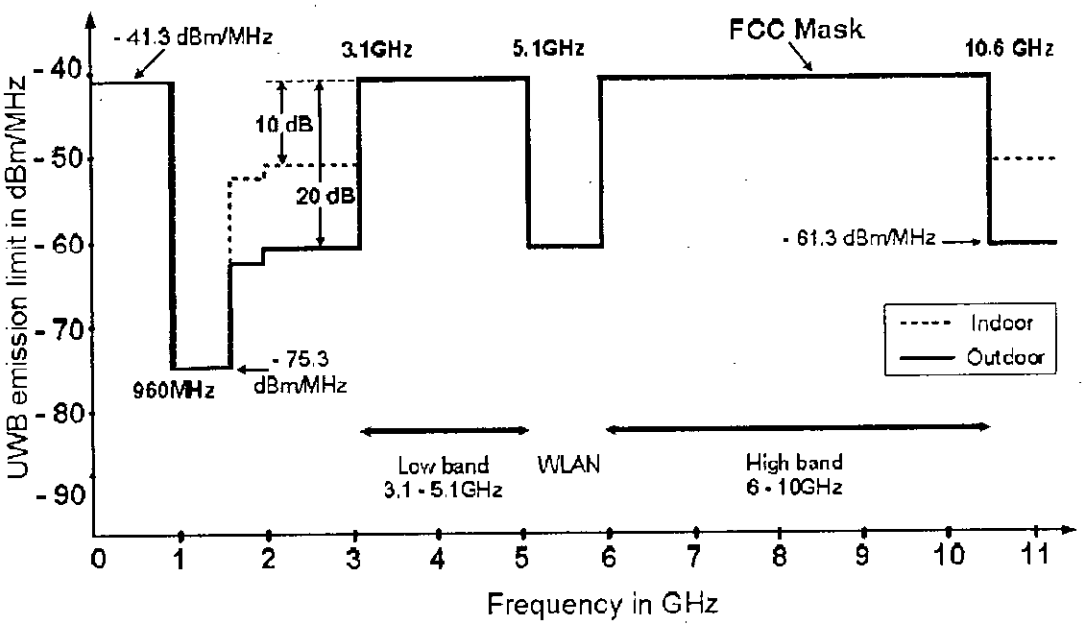


Figure 3.16: FCC spectral mask for UWB communication systems [8]

For the single band (carrier-less) IR-UWB system, the pulse spectrum is designed to occupy the whole allowed 3.1–10.6 GHz frequency band; therefore, the pulse requires a very short duration (less than a nanosecond) with just one or a few cycles of Gaussian function-like waveform. Many types of pulses can be the candidates [41], however to satisfy the wide bandwidth, the Gaussian monocycle pulse and its derivatives are preferred since it contains very small side lobes and provides a sharp roll-off compared to other pulse types. The theoretical analysis shows that, the higher the derivative order (N) of the Gaussian pulses the better the roll-off, so the pulse can satisfy the FCC spectral mask

without requiring additional pulse-shaping filters. Analysis in [15] shows that one needs to take at least the 7-th derivative to the Gaussian pulse in order to fit the pulse power spectral density (PSD) inside the FCC mask shown in Figure 3.17 for the outdoor applications. For indoor application, 5th order derivative of Gaussian pulse can meet the FCC spectral mask. Figure 3.17 shows that the FCC spectral mask for outdoor applications is -10dB more stringent than the indoor one. For these reasons a 5th derivative Gaussian pulse generator is designed in [15], [21], [29] and a 7th derivative Gaussian pulse generator is designed in [26].

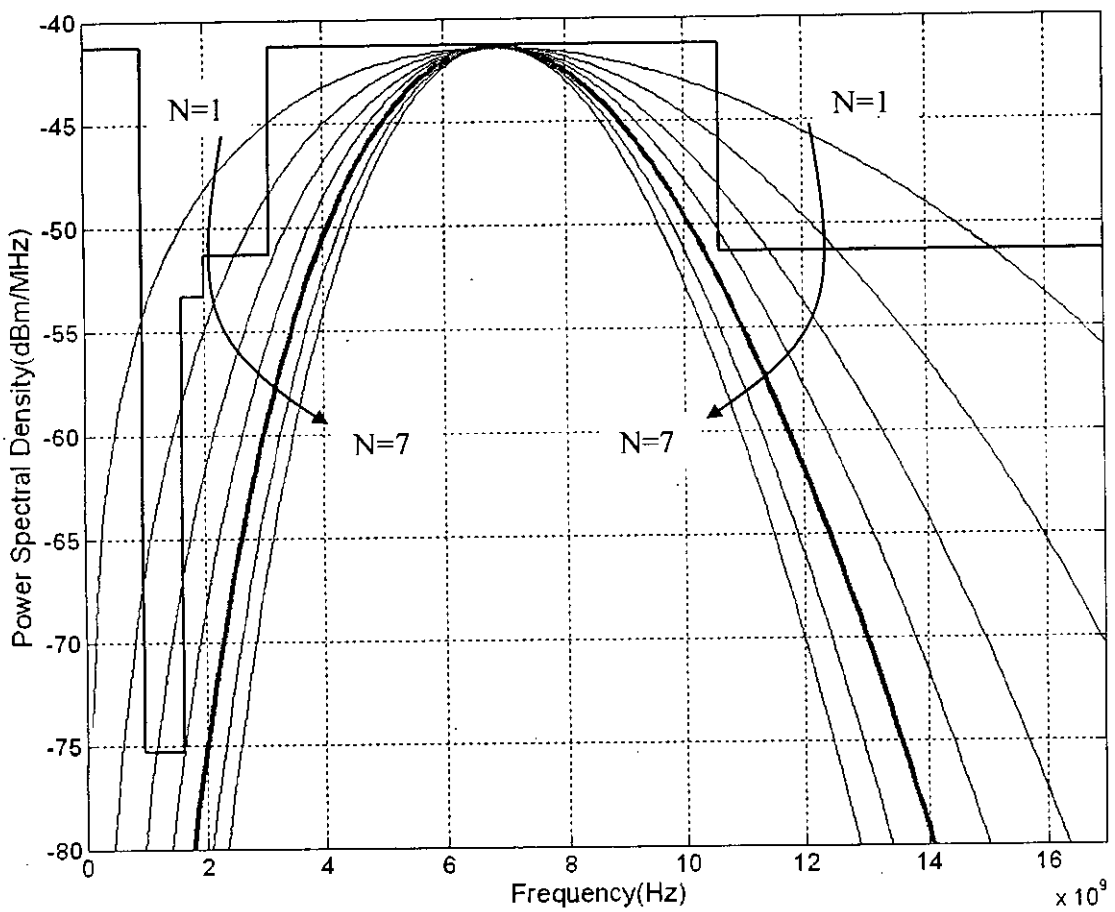


Figure 3.17: PSD of different Gaussian derivatives satisfying FCC mask [15]

But an important thing is that if the pulse widths (or standard deviation) of the Gaussian derivatives are kept same, then the -10 dB bandwidths which is vital for satisfying indoor FCC regulation are also same as revealed from Figure 3.18. Therefore,

the derivative pulses must have increasing widths (or standard deviation) with the increase of the order (N) of derivation which is evident from Figure 3.19. In fact it is a fundamental relation between time domain and frequency domain behavior of signals which states that if the pulse width increases, the frequency spectrum becomes narrower and vice-versa.

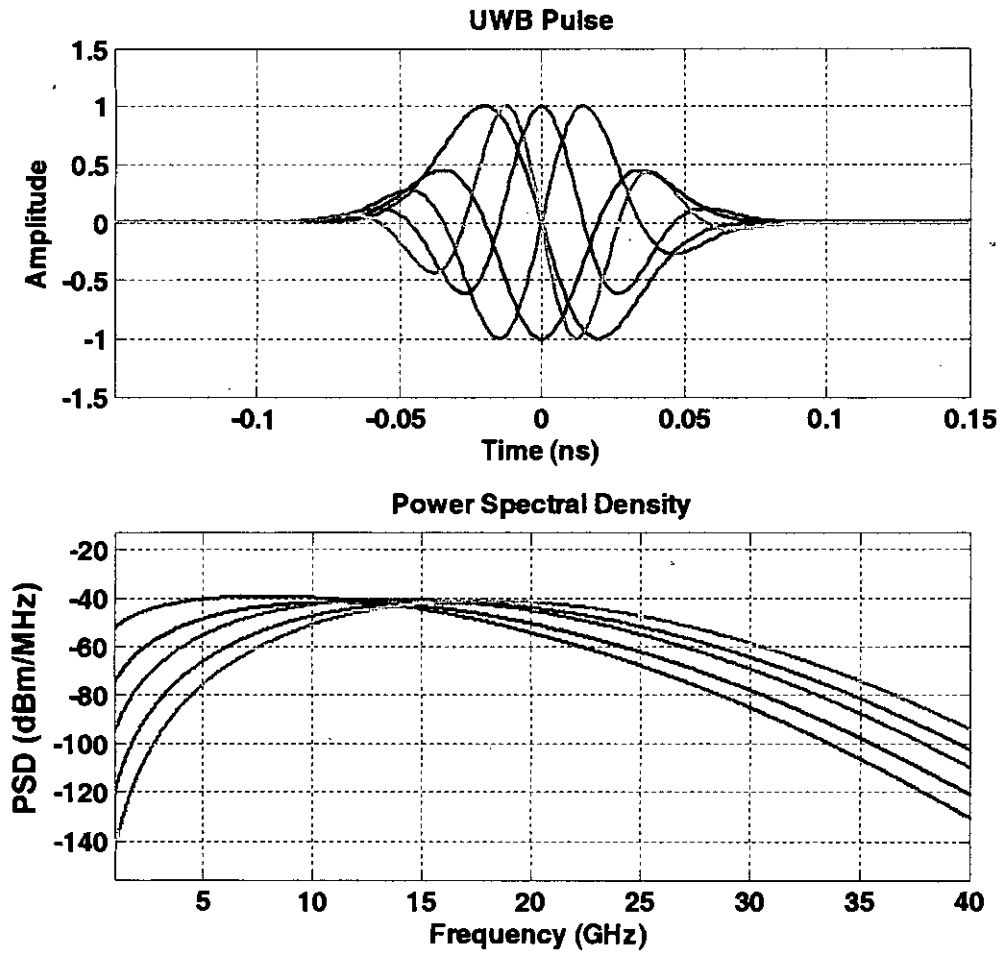


Figure 3.18: PSD comparison for different Gaussian derivatives having the same width

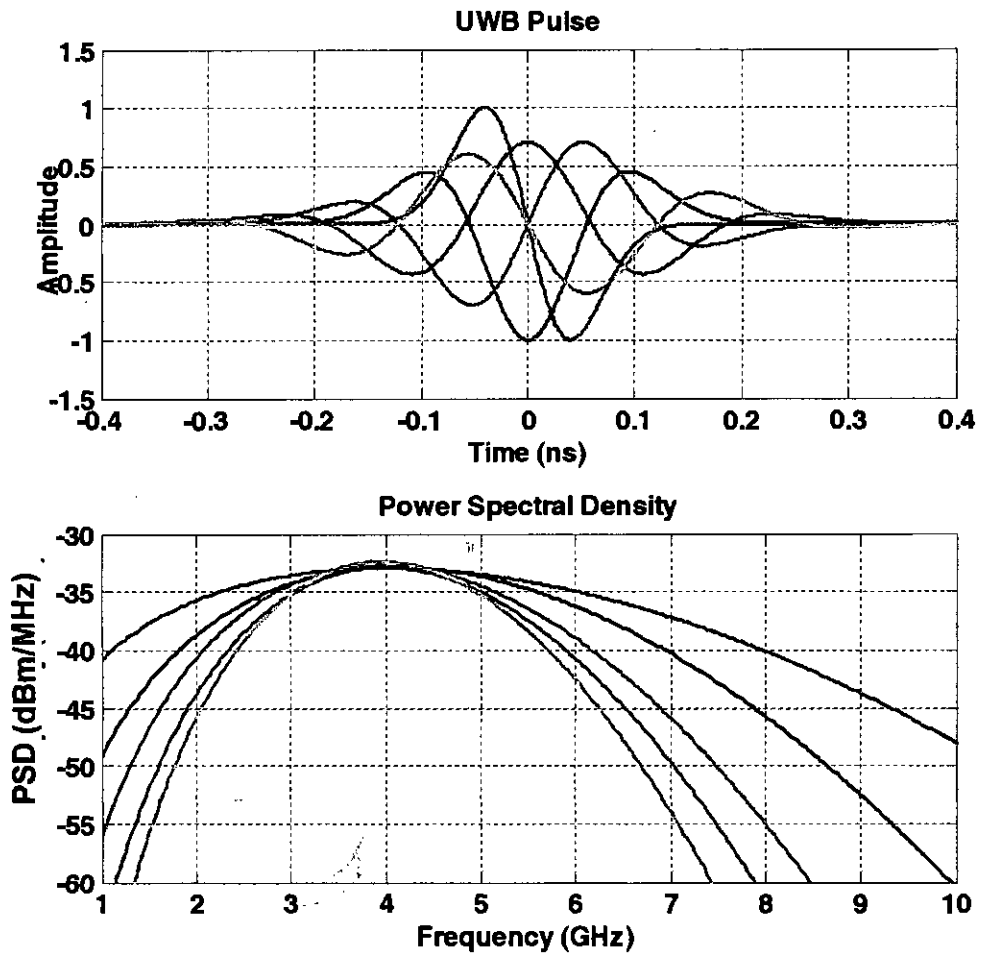


Figure 3.19: PSD comparison for different Gaussian derivatives having different widths

From the above investigations, we have found that to satisfy FCC regulations for indoor communications, researchers have proposed 5th derivative Gaussian pulse which has considerable duration. Since data rate or pulse repetition rate (PRR) is inversely proportional to pulse width, lower data rate is available using 5th derivative pulse. Therefore, although the higher derivative Gaussian pulse generators can be used for data communication in wireless sensor networks, wireless multimedia and video networks and wireless remote controls, none of them can provide high capacity in wireless chip interconnects systems.

To achieve high throughputs in wireless interconnects; we propose Gaussian

monocycle pulse as the transmitted signal instead of any other higher order derivatives of Gaussian pulse because Gaussian monocycle pulse has the smallest width, it is very easy to generate and it also satisfies FCC regulations. Figure 3.20 shows the power spectral density of a Gaussian monocycle pulse with various widths. It is seen that the spectrum becomes more flat as the pulse becomes narrower. Therefore, although the wider GMP pulses do not satisfy the FCC regulations, the GMP pulse whose pulse duration is about 120 ps or less has a power spectrum well below the entire FCC mask without degrading the pulse amplitude.

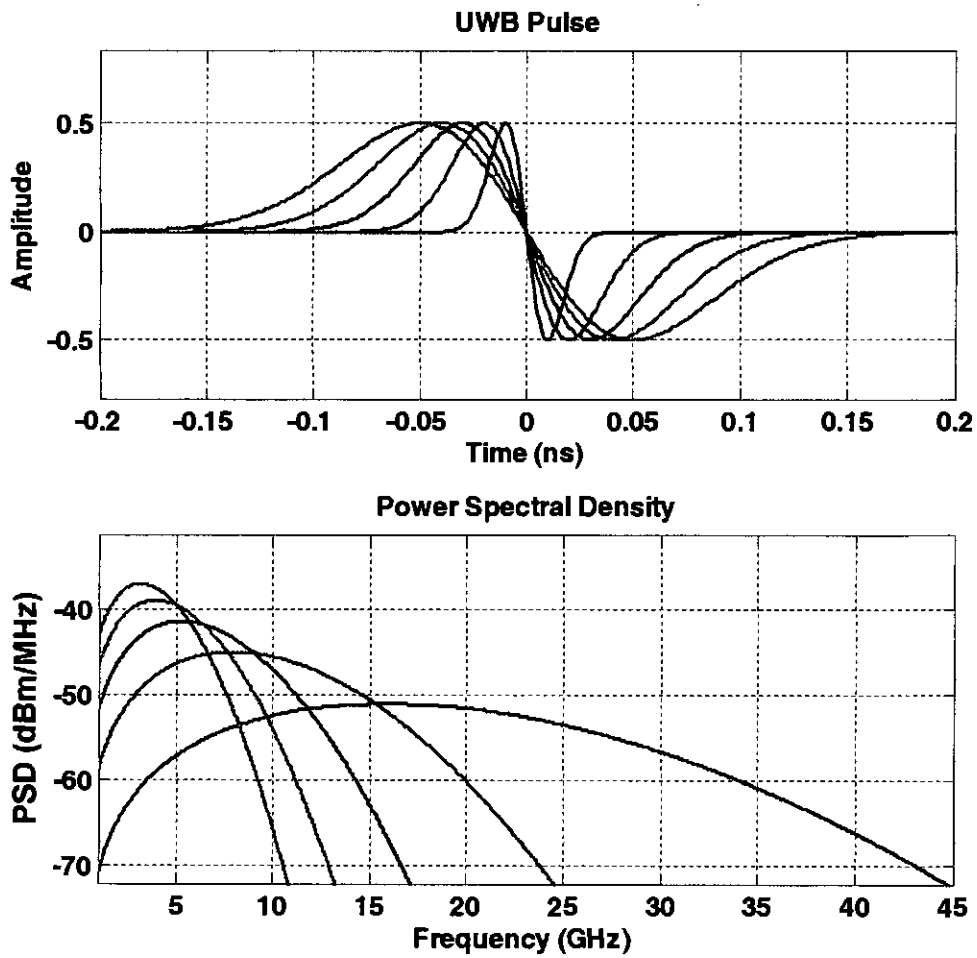


Figure 3.20: PSD of Gaussian monocycle pulses having different widths

From the above discussions we conclude that although in recent IR-UWB communication systems 5^{th} derivative Gaussian pulse is realized to effectively utilize the 3.1-10.6 GHz band under the FCC mask, we propose the Gaussian monocycle pulse as the transmitted signal to serve high data rate by utilizing the whole spectrum under the FCC mask. By spreading the spectrum, the UWB system also achieve better immune to narrow band interference.

CHAPTER 4

UWB TRANSMITTER DESIGN

The generation of monocycle pulses, which can satisfy the FCC spectral mask with low power and low complexity, is still a challenge at present. In this chapter, we have designed a complete digital IR-UWB Gaussian monocycle pulse transmitter for on-chip wireless interconnects applications. The design procedure is illustrated step by step with necessary figures. The performance of the transmitter is evaluated and also compared with other available transmitters found in the literature.

4.1 Design Sequence of UWB Pulse Generator

Our proposed circuit for generating a Gaussian monocycle pulse is shown in Figure 4.1. It consists of two basic parts:

a) Triangular impulse generator and
b) Pulse combination stage

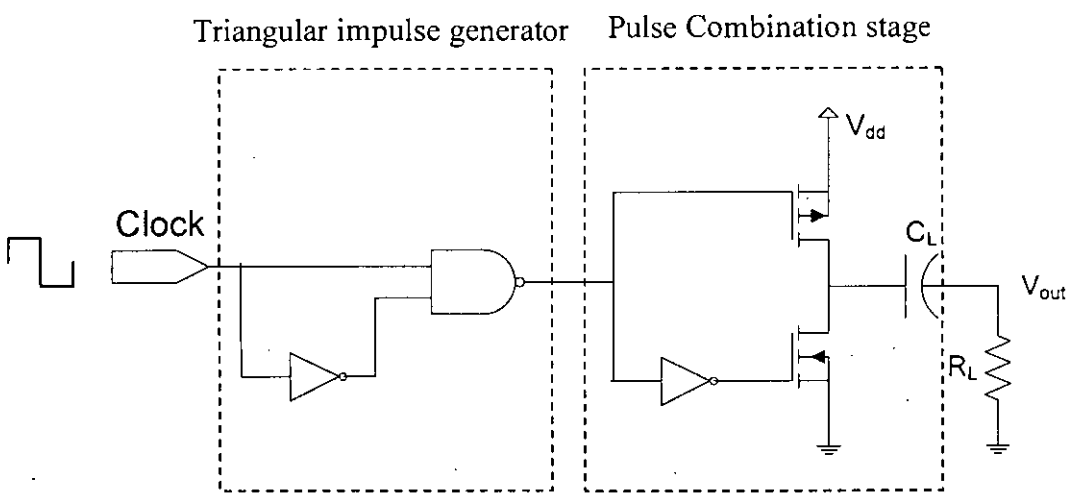


Figure 4.1: Basic circuit for Gaussian Monocycle pulse generation

4.1.1 Basic Principle: Triangular Impulse Generation

The main part of Gaussian monocycle generator is the triangular impulse generator. A digital rectangular clock and its delayed inverted version are fed to a NAND gate and an inverted Gaussian impulse is obtained at the output of the NAND gate as shown in Figure 4.2. The amplitude and the width of the impulse depend on the delay between the two inputs made by the inverter and also on the sizes of the MOS transistors comprising the NAND gate.

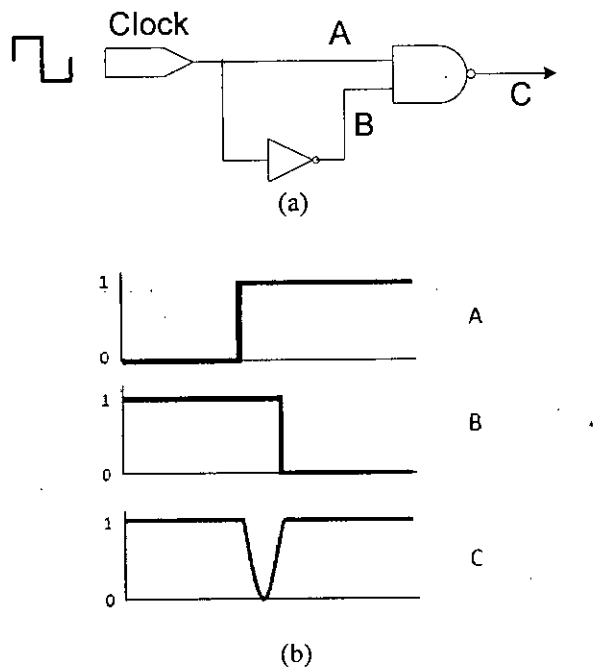


Figure 4.2: Basic triangular impulse generator (a) circuit (b) signal waveform at various nodes

4.1.2 Pulse Combining Stage

The second part of the pulse generator of Figure 4.1 is the output stage which shapes the Gaussian impulse to Gaussian monocycle. The inverted Gaussian impulse generated by a NAND gate drives a PMOS transistor (M1) and a positive Gaussian impulse drives a NMOS transistor (M2). The drain terminals of both the transistors are connected to a load resistance (R_L) through a capacitance (C_L) as shown in Figure 4.3. The capacitor (C_L) is made from a NMOS transistor by shorting drain, source, and substrate terminals all together. The resistance (R_L) represents the input impedance of the transmitting antenna. Although the input impedance may vary with frequency, we

assume a flat impedance of the antenna at first. In chapter 5, we have considered the actual impedance of the antenna in our simulation.

The positive impulse at D is derived from the inverted impulse by using one or more inverters as required. The inverters introduce some delay between the two Gaussian impulses which is the main principle of producing a monocycle pulse from two Gaussian impulses. The two impulses sequentially trigger the two transistors. The PMOS transistor is triggered first and a current flows to the ground through capacitor and resistor. Since the capacitor is being charged by the current, the PMOS transistor gradually goes from saturation to cut off region and the current ceases. In this way, we have the positive half cycle of the Gaussian monocycle pulse. As soon as the charging current dies out, the NMOS transistor is triggered and it creates a path for the capacitor to discharge. A discharging current now flows through the resistor and gradually dies out again. Since the direction of the current through the resistor is now opposite from the direction of current in charging condition, the negative half cycle of the Gaussian monocycle pulse is formed.

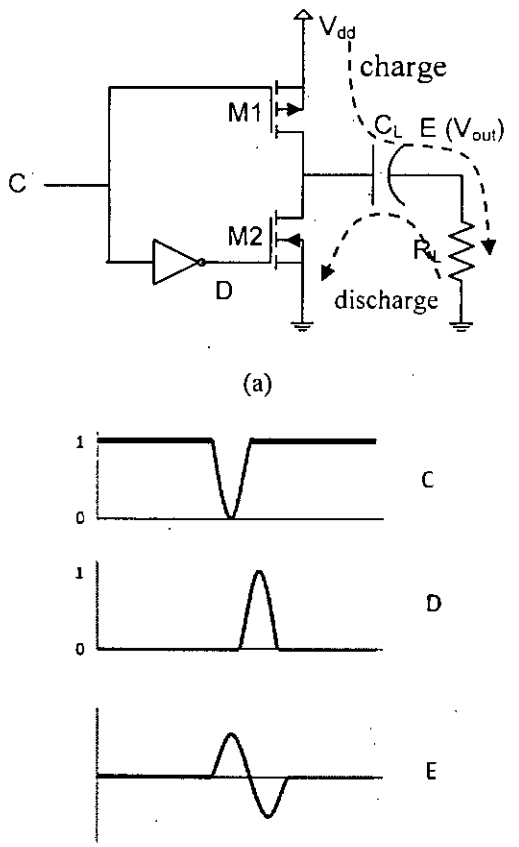


Figure 4.3: Output stage of the pulse generator (a) circuit (b) signal waveforms at various nodes

The shape of the output waveform across the load resistance strongly depends on the delay between the triggers of the two transistors and an accurate timing is the most difficult challenge in the design of such a pulse generator. The delay is governed by both the size and the number of inverters used in the line. Moreover, the amplitude of the monocycle pulse depends on the amplitude of current which in turn depends on the size of the transistors M1 and M2. By adjusting both of them carefully, a complete high quality Gaussian monocycle pulse is finally obtained.

4.1.3 Data Modulation: OOK

After the generation of UWB pulse, the pulses have to be modulated according to the data bits to represent '1' and '0'. First, we have developed an on-off keying (OOK) transmitter and then we have designed a BPSK transmitter.

In order to generate pulses according to the data bits, we have used a three input NAND gate instead of two input NAND gate to get direct control of the pulse generation for OOK as shown in Figure 4.4. If the data bit is '1', only then we get an impulse.

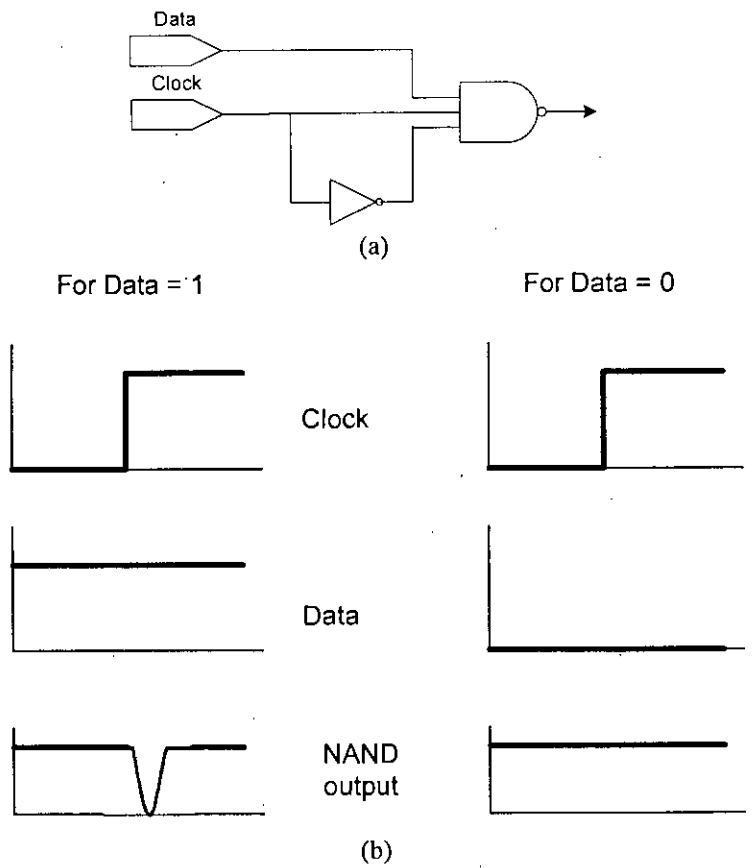
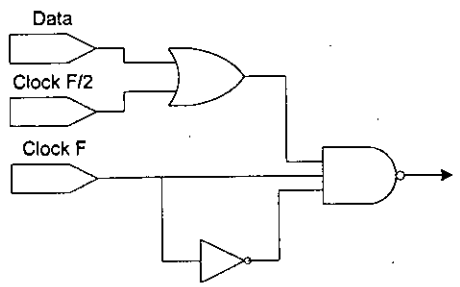


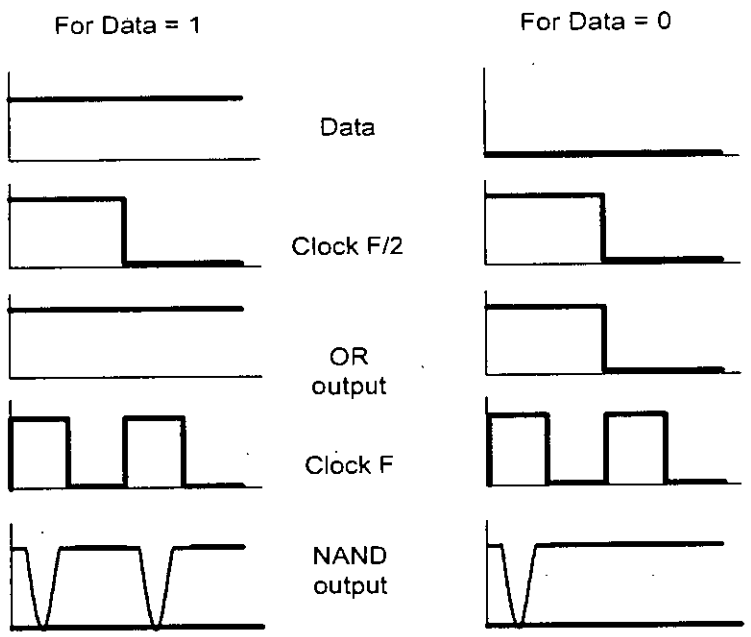
Figure 4.4: Design step to include OOK modulation (a) circuit (b) signal waveforms at various nodes

4.1.4 Data with Transmitted Reference (TR)

Since we are developing this pulse generator targeting to use in the transmitted reference communication scheme, TR pulses are to be transmitted along with the data pulses for all bits. To include this feature in the pulse generator, we have proposed the circuit shown in Figure 4.5, instead of using a delay element and an adder circuit as shown in Figure 3.11 in the previous chapter.



(a)



(b)

Figure 4.5: Design step to include TR scheme (a) circuit (b) signal waveforms at various nodes

Since we need two impulses for data bit '1' and one impulse for data bit '0', the data line (the upper input of the NAND gate) in Figure 4.5 (a) must be high for two clock periods when data bit is '1' and data line must be successively high and low each

for one clock period when the data bit is '0'. This sequence can be achieved from the following logic equation:

$$Y = Data + Clock_{F/2} \tag{4.1}$$

where, $Clock_{F/2}$ is another digital clock whose frequency is the half of the frequency of the original clock and Y is the desired control signal to be fed to the NAND gate. In the circuit of Figure 4.5, two clock pulses with frequencies F and F/2 are shown. In fact, for synchronization between the two clocks, the lower frequency clock must be derived from the main clock using a frequency divider. For this purpose, we have used a simple positive edge triggered D flip-flop effectively as shown in Figure 4.6. The D flip-flop not only eliminates one clock but also provides a mean to operate the transmitter in different modes which is discussed in later sections.

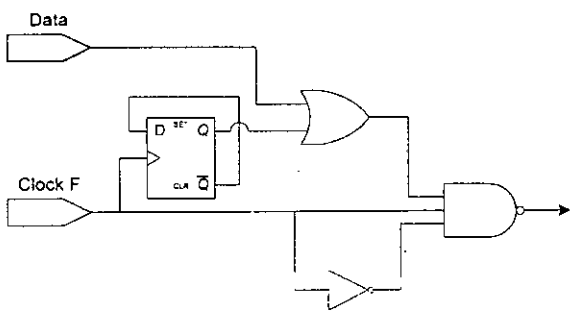


Figure 4.6: Design step employing D flip-flop

The single ended complete circuit diagram of UWB Gaussian monocycle OOK transmitter with TR pulse is given in Figure 4.7. A series of inverters between node 3 and node 5 are inserted to balance the delays required for the signal to travel from node 3 to node 4 and from node 3 to node 5. Also three inverters are placed to make sufficient delay between the two impulses triggering at the transistors M1 and M2.

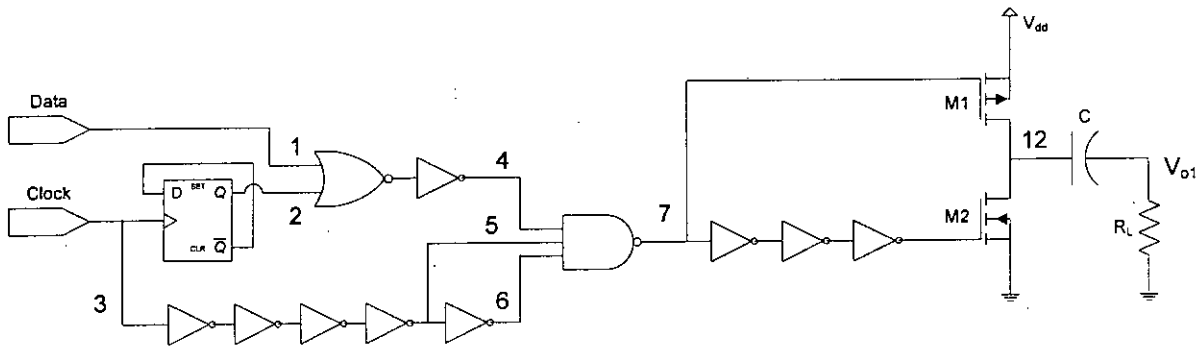


Figure 4.7: Single ended UWB Gaussian monocycle OOK transmitter with TR pulse

4.1.5 UWB Transmitter with Differential Output

The antenna integrated on silicon substrate (discussed in chapter 5) used to transmit the electromagnetic signal in wireless interconnects are usually differential in nature. Therefore, the output signal of the transmitter must be differential. Differential signals also don't have common mode system noise and power supply variation effects. To achieve differential output, we have used another pair of transistors (M3 and M4) along with C_L and R_L in the output stage as shown in Figure 4.8. Since an opposite signal swing is required at the output of the lower stage with respect to the upper stage. the gating impulses of M3 and M4 transistors must have opposite sequence to that of M1 and M2 transistors. The opposite gating impulses are obtained by using two more inverters in the delay line after the NAND gate. The detail timing diagram is illustrated in Figure 4.9. In this way, we have derived two opposite Gaussian monocycle pulses at the outputs. An important task of this design is to confirm sufficient overlapping between the two monocycles since the two monocycles will not completely overlap in this design due to the delay incurred by the inverters between the gating impulses of M1 and M3 transistors and between the gating impulses of M2 and M4 transistors. But by careful designing of inverter $Inv_{8\text{-}9}$ and $Inv_{10\text{-}11}$, we have reduced the delay effect and a nearly ideal Gaussian monocycle pulse is achieved as shown in Figure 4.12 (c).

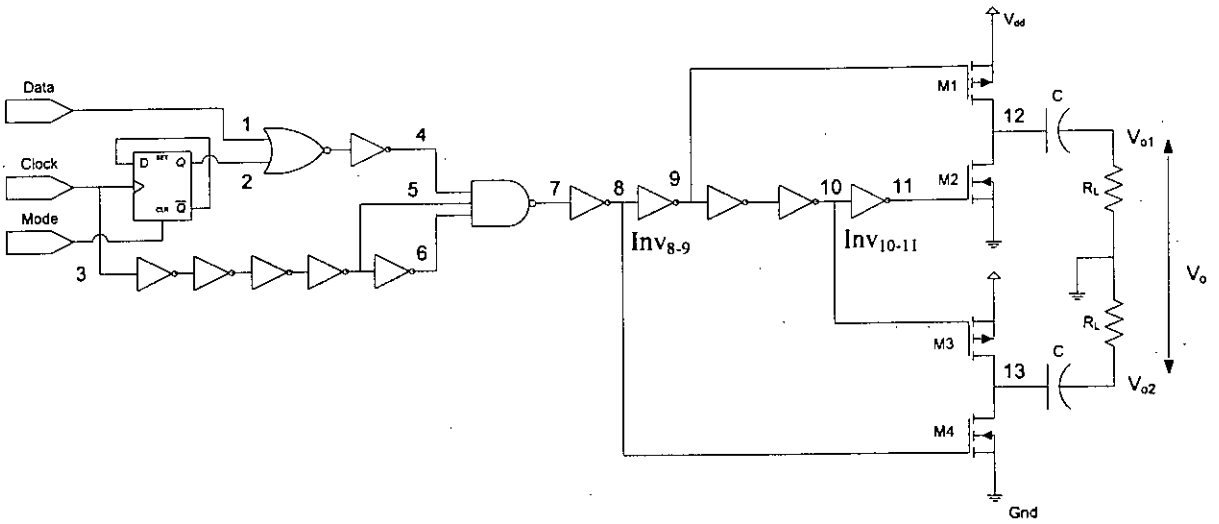


Figure 4.8: Complete schematic of the differential UWB OOK transmitter

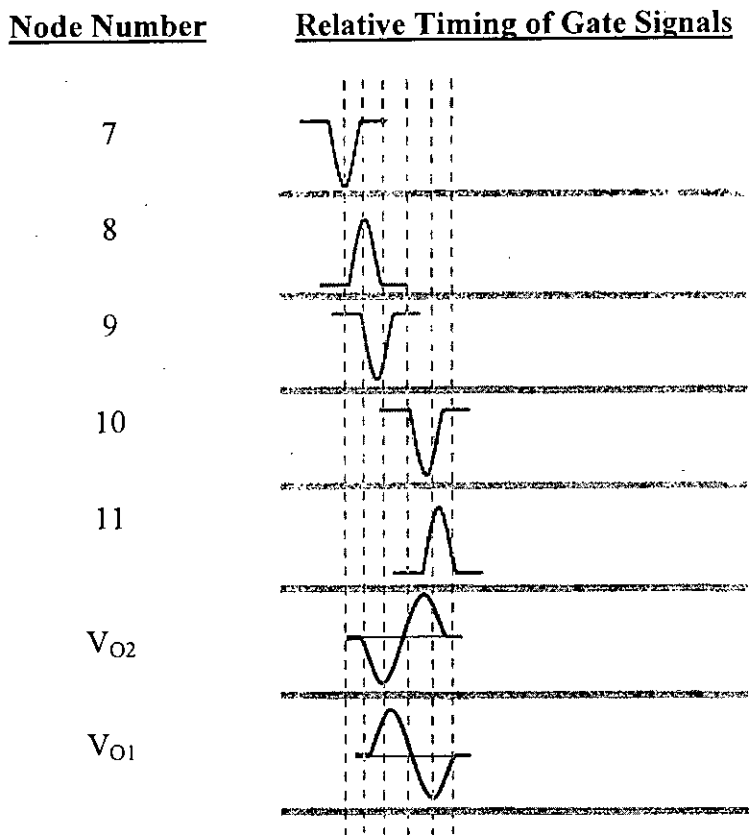


Figure 4.9: Timing waveforms at various nodes of the transmitter circuit of Figure 4.8

4.1.6 Proposed UWB BPSK Transmitter Design

After designing the OOK transmitter, an interesting thing happens when we swap the gate connections of the upper and lower combination stages as shown in Figure. We get an inverted Gaussian monocycle pulse at the differential output. This indicates a way to obtain bipolar pulses at the output by properly switching the gate connections according to data bits.

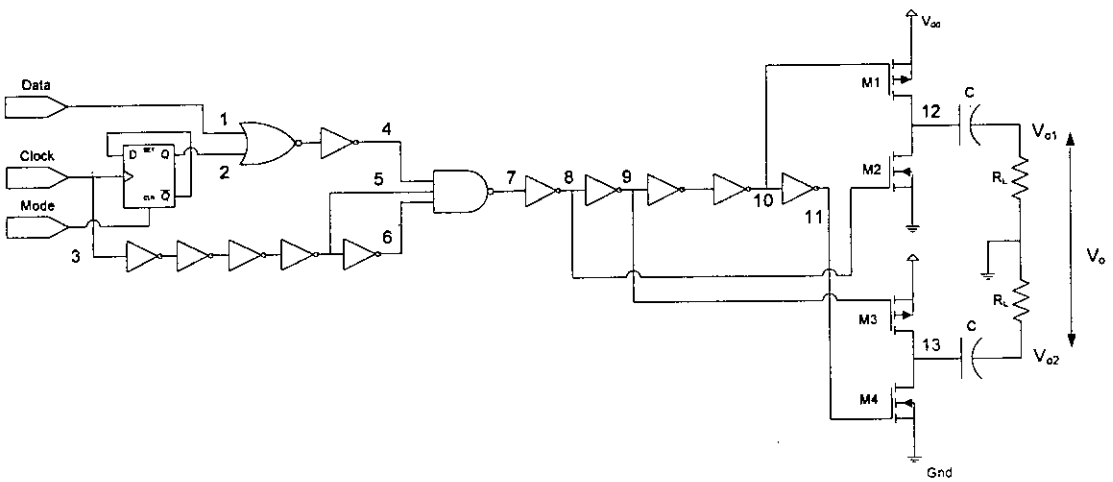


Figure 4.10: Gate connections of UWB transmitter to produce inverted Gaussian monocycle pulse

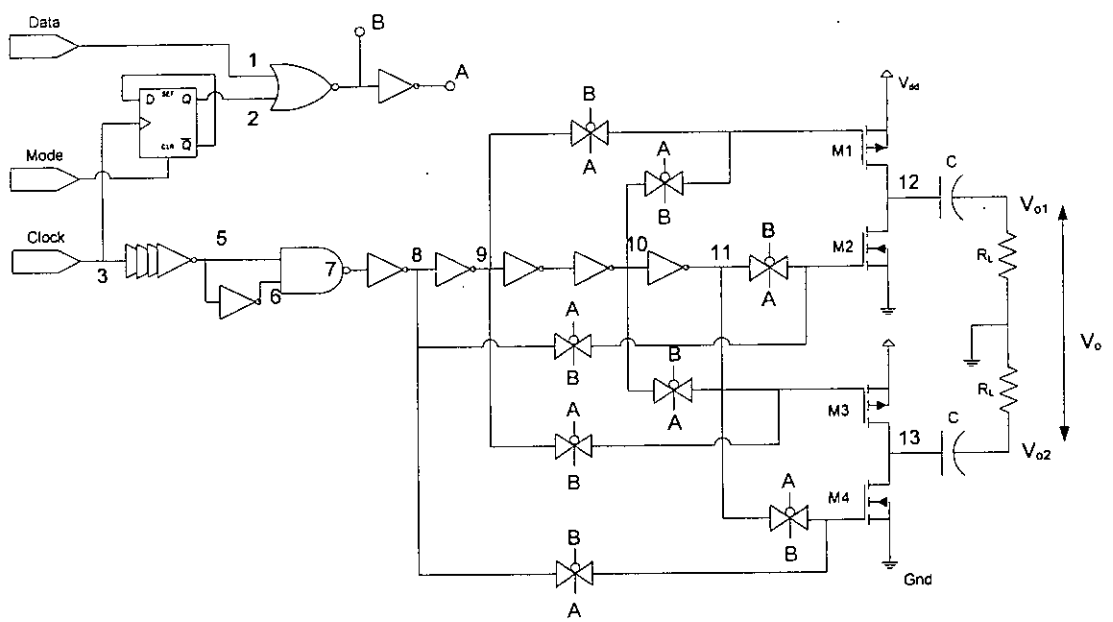


Figure 4.11: Complete schematic of the differential UWB BPSK transmitter

We have proposed a UWB BPSK transmitter where the switching is done through transmission gates as shown in Figure 4.11. For BPSK transmission we have used a two input NAND gate instead of a three input NAND gate since for BPSK we don't have to control the occurrence of the triangular impulses according to data; an impulse is needed for both data bit '1' and '0'. Rather we have to control the polarity of the output pulses. To obtain BPSK pulse with TR pulse, the same synthesized signal which was used for controlling the triangular impulse generation in OOK transmitter is now used to control the transmission gates.

4.1.7 Modes of Operation and Data Rate

The developed UWB transmitter can be operated in two modes:

a) Transmitted reference (TR) mode

b) Single pulse (SP) mode

a) Transmitted Reference Mode

In TR mode, each bit is preceded by a TR pulse and it is successfully achieved in our developed transmitter by utilizing a D flip-flop. The data rate of the transmitting signal is limited by the width of the Gaussian monocycle pulse. From simulation we have found that the pulse width of the monocycle is 140 ps. Therefore, a maximum 7 GHz clock can be used in this transmitter because each clock pulse produces one pulse; otherwise the output pulses will overlap each other and distort the output signal. And since two consecutive clock pulses are needed to represent one data bit, data can be transmitted at a maximum rate of 3.5 Giga bits per second (Gbps) in TR mode.

b) Single pulse mode

Much of the existing RF receivers, for example [58], use PPL for synchronization and a template pulse is generated in the receiver to demodulate the signal. In such systems only single UWB pulse is transmitted to represent each data bit. To make our designed transmitter useful not only for transmitted reference systems but also for traditional receivers, we have included an option

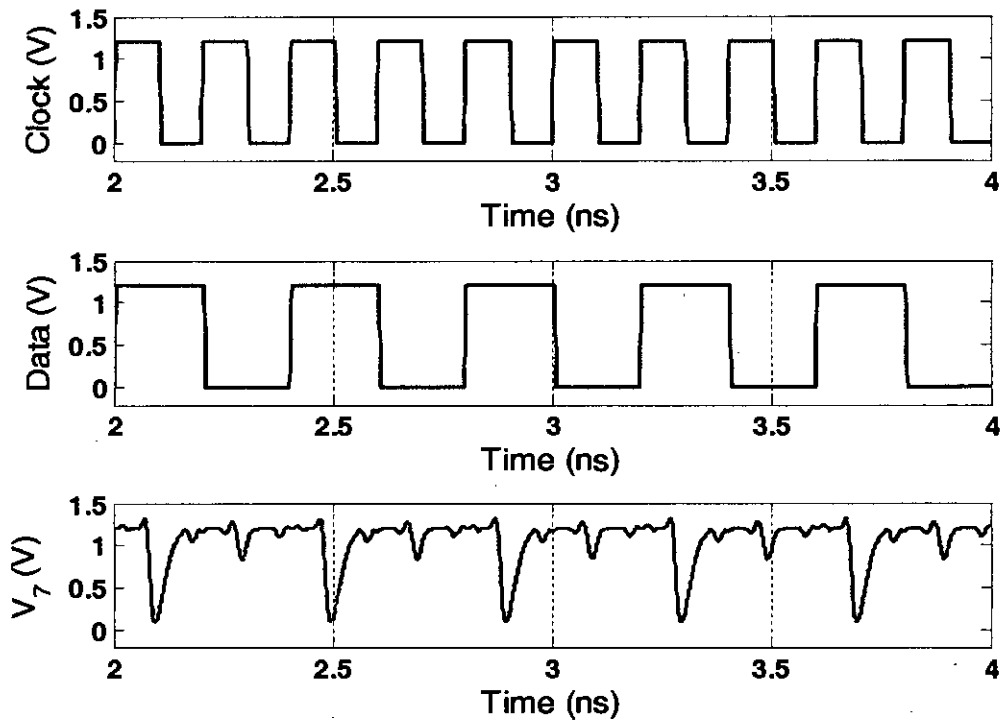
to operate the transmitter in single pulse mode without transmitting TR pulses. This control is done by using $\overline{CLEAR}$ button (active low) of the D flip-flop as mode selector. If $Mode = \overline{CLEAR} = 1$, the pulse generator operates in TR mode. And if $Mode = \overline{CLEAR} = 0$, the pulse generator operates in single pulse (SP) mode by clearing the output of the D flip-flop; the data line now directly controls the NAND output. The data rate in SP mode can be twice the data rate of TR mode since one pulse now represents one bit. Therefore, data can be transmitted at a maximum rate of 7 Gbps in SP mode. The data rates for different modes of operation are summarized in Table 4.1.

Table 4.1: Data Rates for different modes of operation

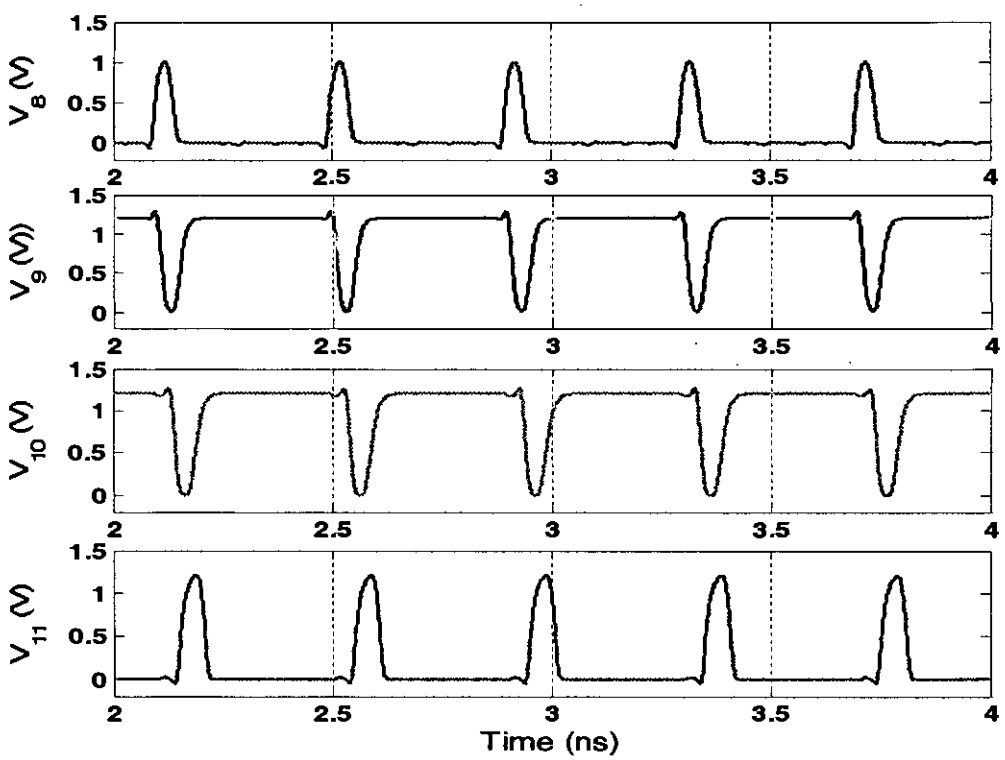
Mode of Operation	Mode signal	Max. Clock Freq.	Max. Data Rate
Single Pulse Mode	**0**	**7 GHz**	**7 Gbps**
TR Mode	**1**	**7 GHz**	**3.5 Gbps**

4.2 Simulated Waveforms

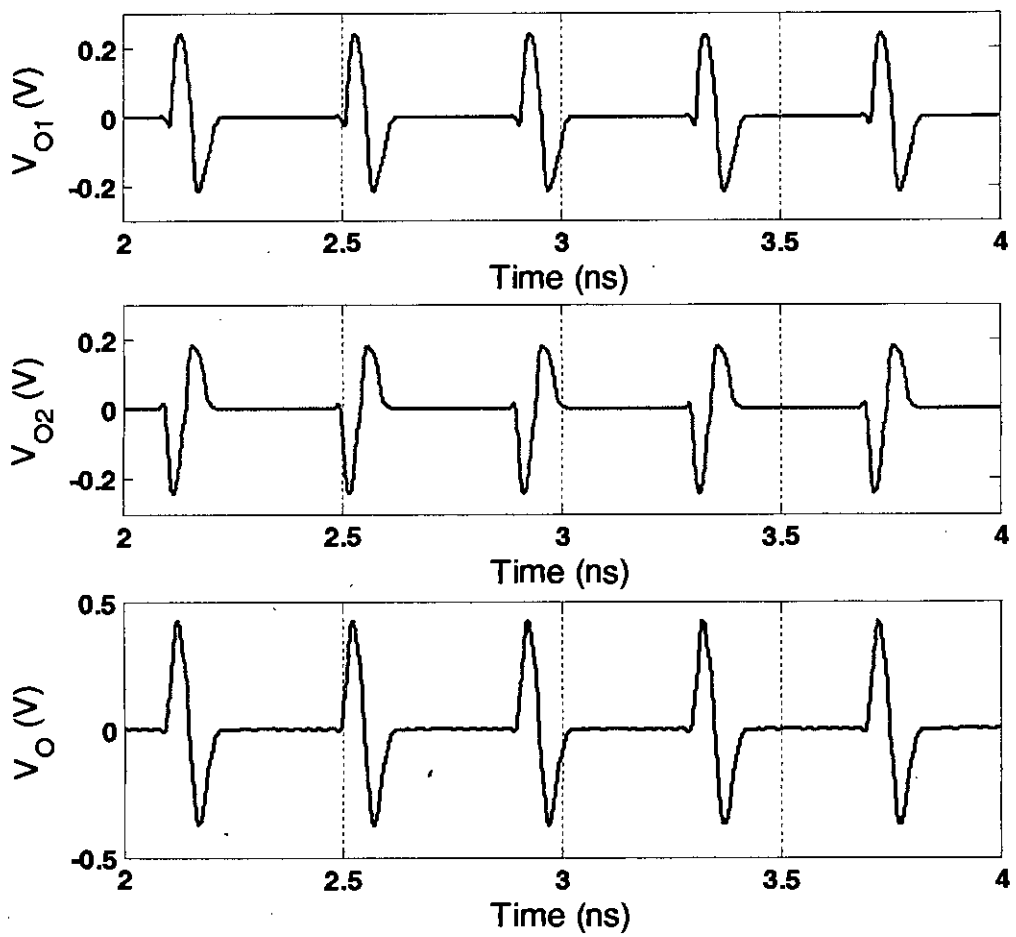
The whole transmitter circuit is designed in **Synopsys, HSPICE** using **IBM 90 nm CMOS** technology and the simulated waveforms at various nodes of the complete differential transmitters are shown in Figures 4.12 and 4.13 for different modes of operation.


Clock (V)
Data (V)
V_7 (V)
1.5
1
0.5
0
2
2.5
3
3.5
4
Time (ns)

(a)


V_8 (V)
V_9 (V)
V_{10} (V)
V_{11} (V)
1.5
1
0.5
0
2
2.5
3
3.5
4
Time (ns)

(b)



(c)

Figure 4.12: (a)-(c) HSPICE Simulated waveforms at various nodes of the complete differential UWB Gaussian monocycle OOK transmitter operated in SP mode
(Clock frequency = 5 GHz, Data rate = 5 Gbps)

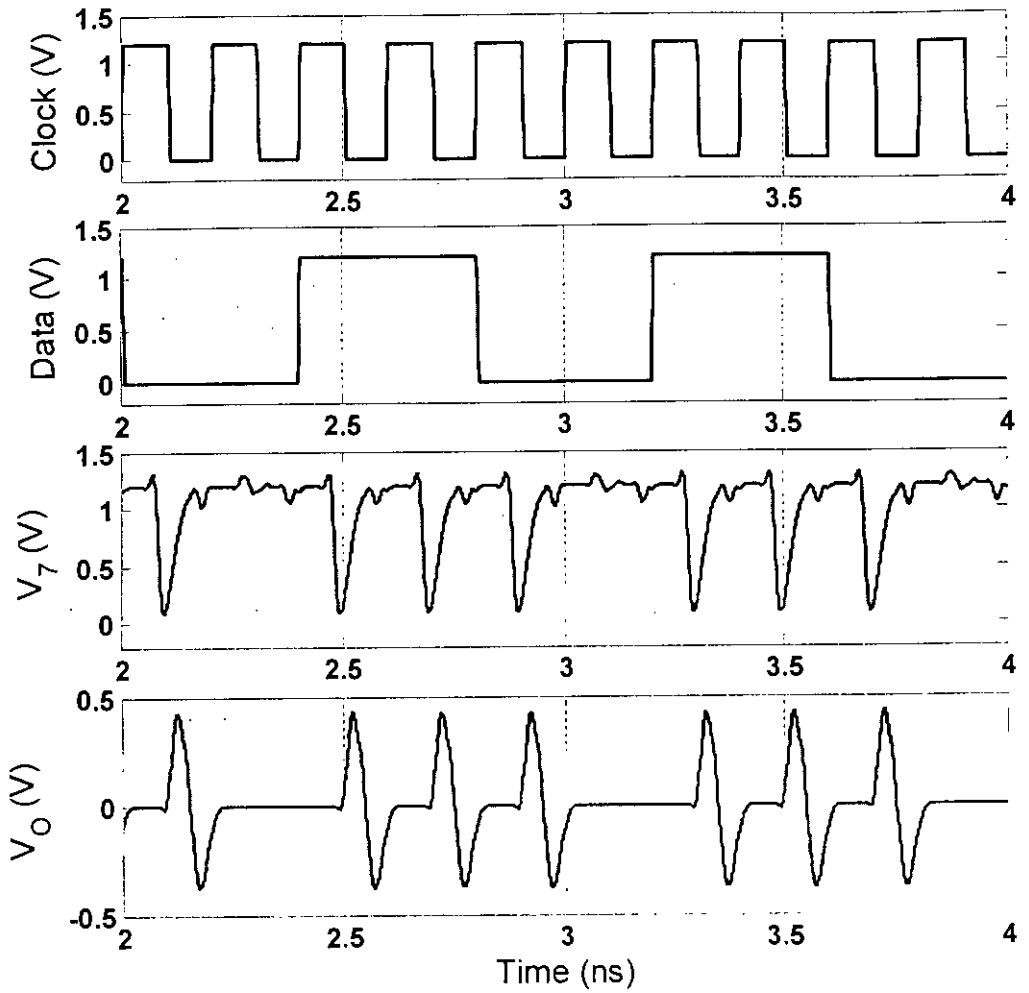
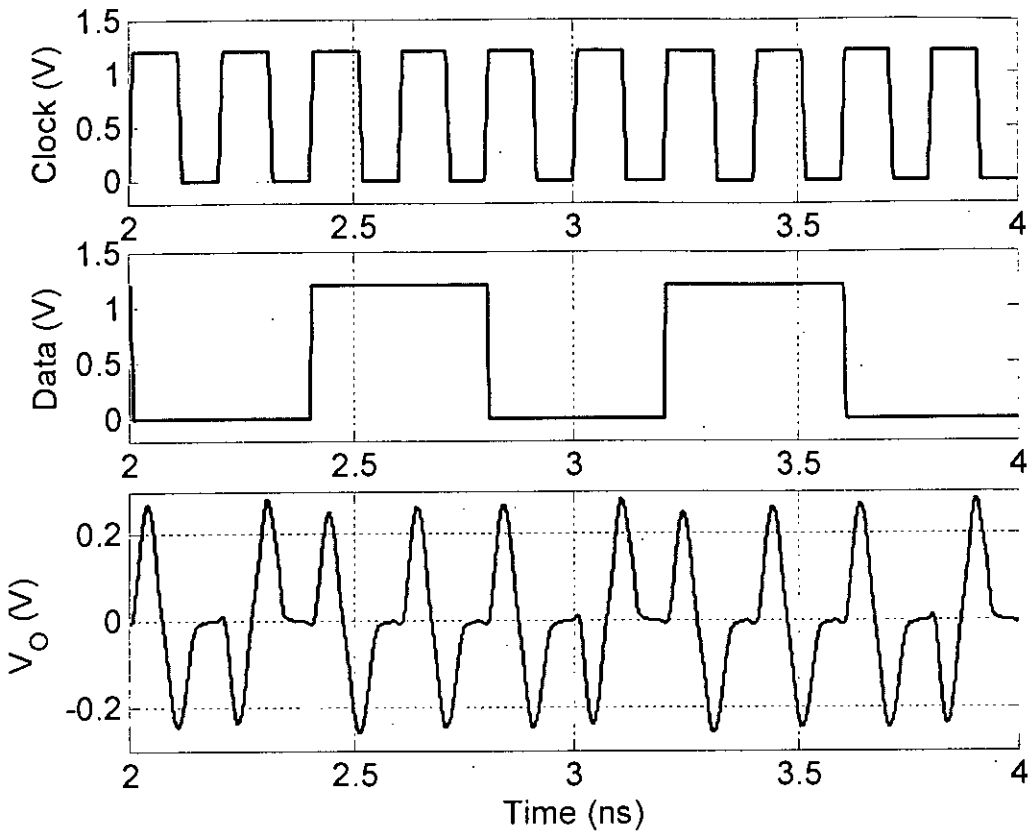
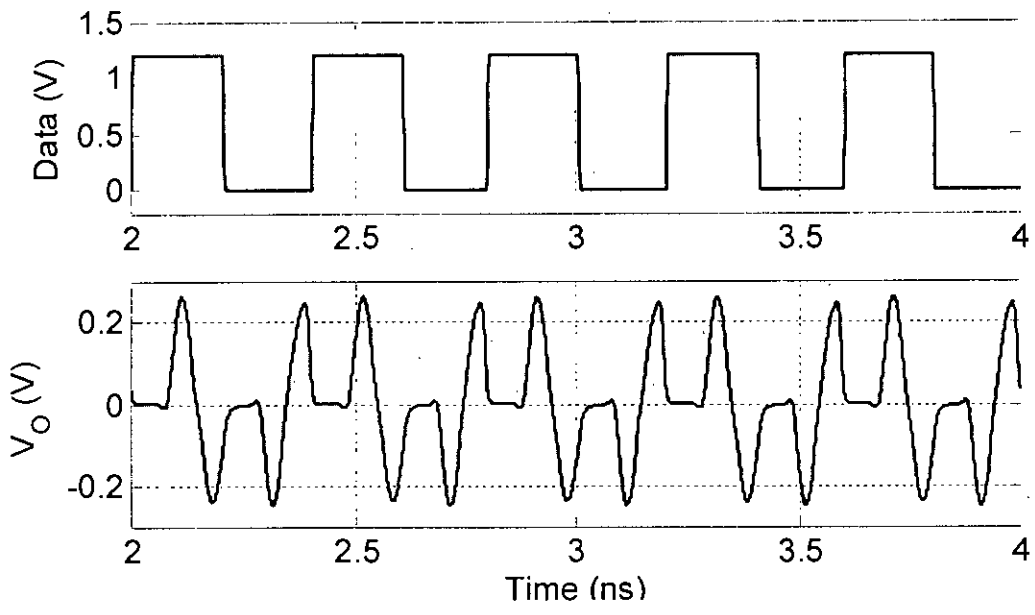


Figure 4.13: HSPICE Simulated waveforms at various nodes of the complete differential UWB Gaussian monocycle OOK transmitter operated in TR mode
(Clock frequency = 5 GHz, Data rate = 2.5 Gbps)



(a)



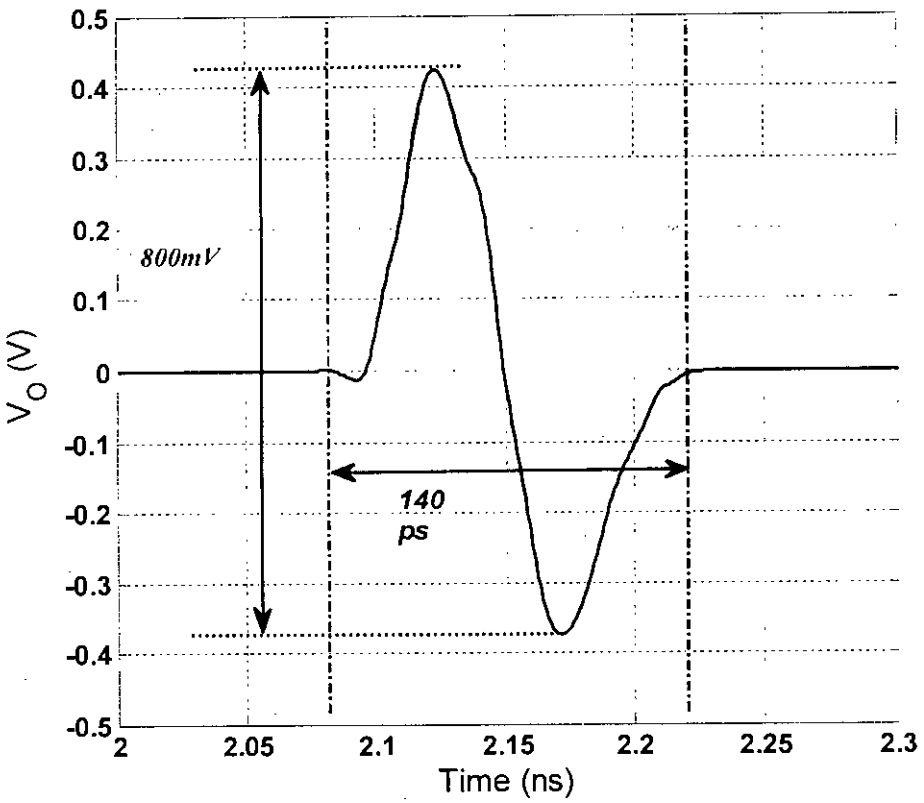
(b)

Figure 4.14: HSPICE Simulated waveforms of the differential UWB Gaussian monocycle BPSK transmitter operated in (a) TR mode and (b) SP mode
(Clock frequency = 5 GHz)

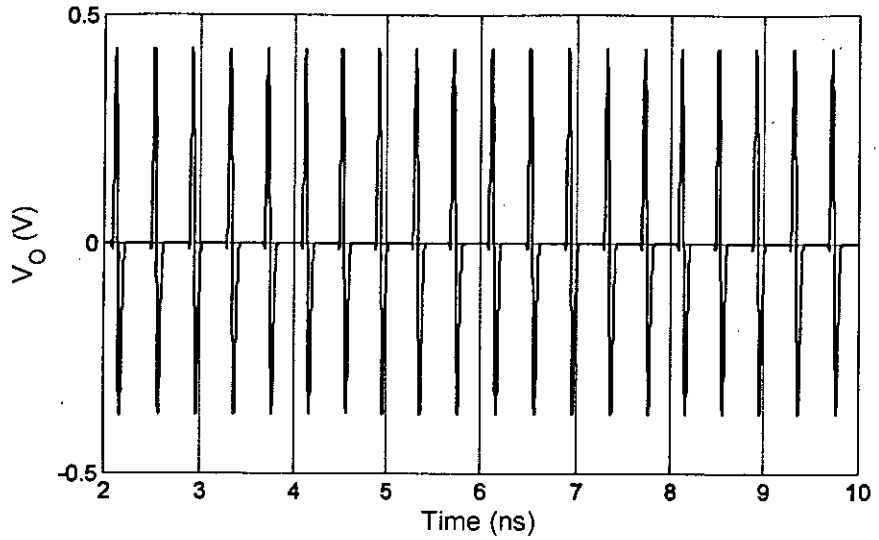
4.3 Performance Evaluation

i) Time Domain

Figure 4.15 (a) examines a single UWB Gaussian monocycle pulse generated by the designed OOK transmitter. The peak-to-peak output pulse amplitude is found to be 800 mV for OOK transmitter and 500 mV for BPSK transmitter and the pulse duration is around 140pico-seconds (ps) for both the transmitters. Figure 4.15 (b) shows a series of pulses generated by the transmitter at a rate of 2.5 Giga pulse per second (Gpps). All the pulses have same amplitude, width and shape.



(a)

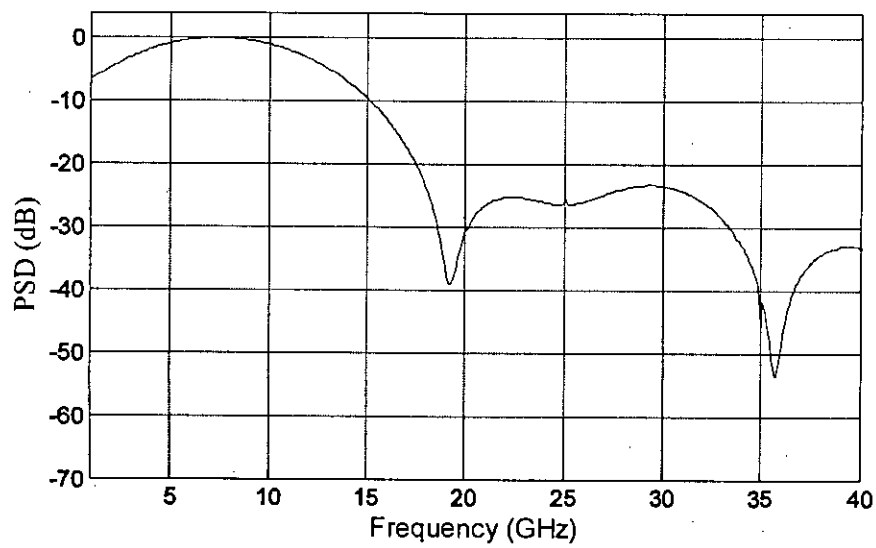


(b)

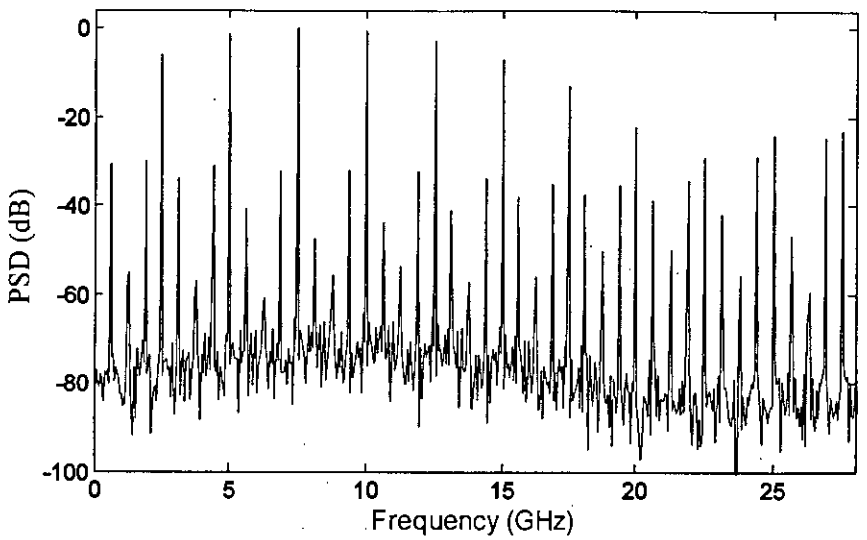
Figure 4.15: (a) A single generated UWB monocycle pulse, (b) a series of pulses at 2.5 Gpps

ii) Frequency Domain

The normalized FFT spectrum of a single pulse and a series of pulses are shown in Figure 4.16. The -3dB bandwidth of the transmitted signal is 9 GHz (from 3.5 GHz to 12.5 GHz).



(a)



(b)

Figure 4.16: Normalized frequency spectrum of generated Gaussian monocycle pulse (a) spectrum of a single pulse, (b) spectrum of a series of pulses at 2.5 Gpps

iii) Effect of Load Resistance on Output Pulse Waveform

All the waveforms shown so far are generated assuming a 100Ω load resistance R_L connected at each output of the differential transmitter which represents the input impedance of the transmitting on-chip antenna. In this subsection we have investigated the effect of the load resistance on the output waveform by simulating the circuit using different values of R_L. Figure 4.17 shows the variations of OOK transmitter pulse amplitude with respect to R_L. It is seen that the peak-to-peak pulse amplitude increases with load resistance.

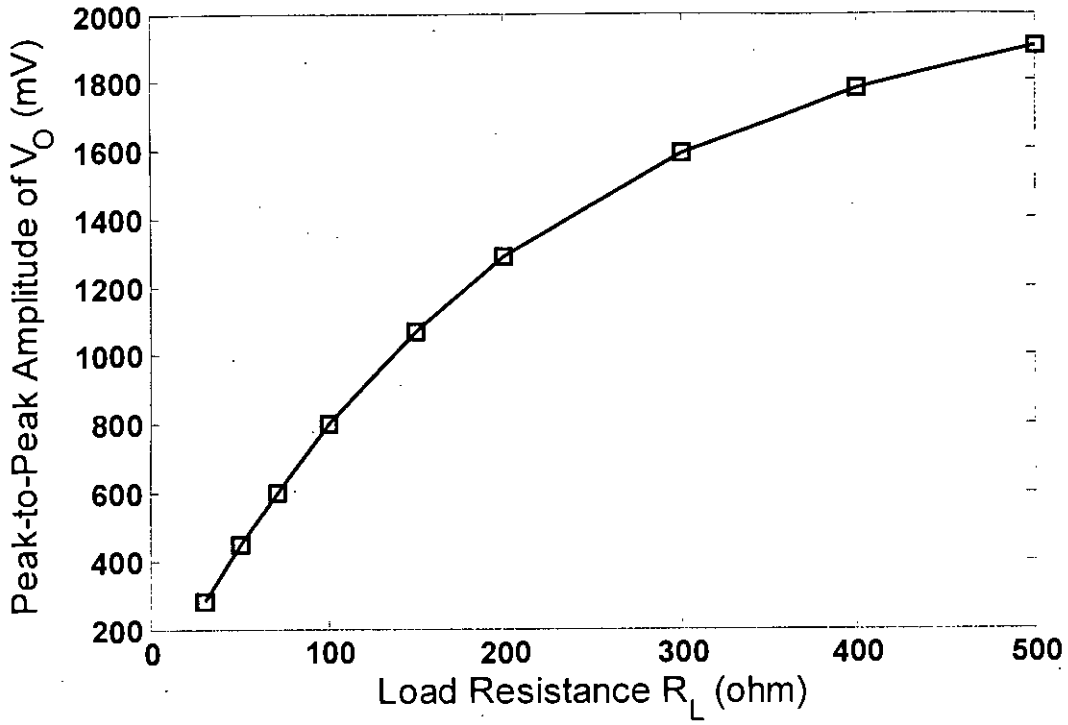


Figure 4.17: Effect of load resistance on OOK transmitter output waveform

iv) Power Consumption

The biggest issue of any on-chip wireless communication is the amount of power consumption. Very low power dissipation is required to reduce the amount of heat generated by the device and to increase battery life. The instantaneous power supplied by the power supply is the product of the instantaneous voltage and current supplied by the source. In our design, power supply voltage is 1.2 V DC. The simulated waveform of instantaneous current and power delivered by the DC power supply to the whole OOK transmitter circuit is shown in Figure 4.18. The calculated value of average power delivered by the DC power supply is only 5.5mW for OOK transmitter and 5.64mW for BPSK transmitter at a pulse repetition rate (PRR) of 5 Gpps. Therefore, only 1.1 and 1.13pico-Joule (pJ) energy are consumed by the OOK and BPSK transmitters, respectively, for each pulse transmission.

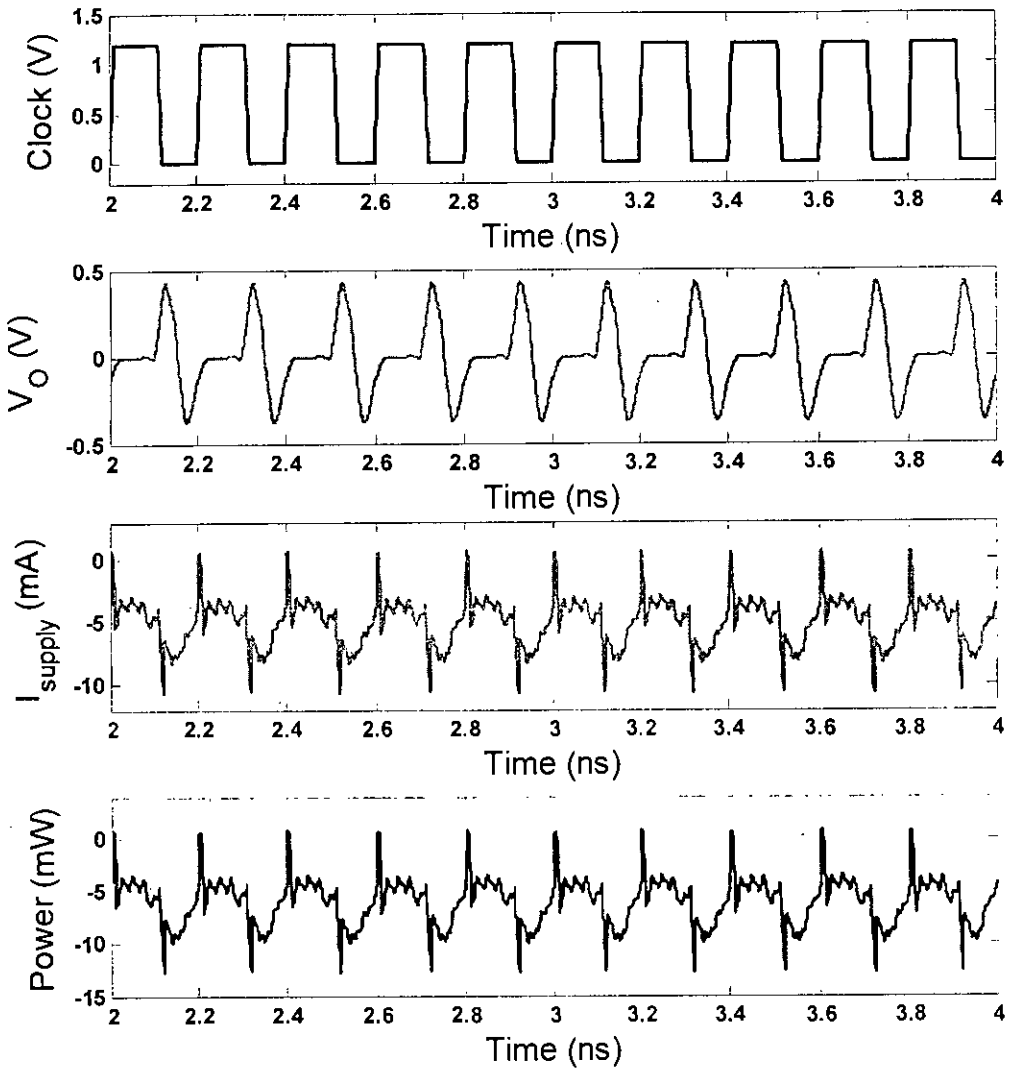


Figure 4.18: Waveforms of instantaneous current and power supplied by the DC power source in OOK transmitter

v) Output Wave shape and FCC Regulation

Let us now examine the power spectral density (PSD) in dBm/MHz of the generated Gaussian monocycle pulse. Figure 4.19 shows the PSD of a single pulse generated from the BPSK transmitter. It is observed from the figure that 500 mV peak-to-peak pulses do not satisfy the FCC regulation. However, if we reduce the pulse amplitude to around 350 mV without increasing the pulse width, it satisfies the FCC regulation. The amplitude of the output pulse is reduced by using smaller size CMOS transistors (M1-M4) in the pulse combination stage of the transmitter. In this way, we

can have a 350mV peak-to-peak (p-p) Gaussian monocycle pulse with 140ps pulse width which also satisfies FCC regulations.

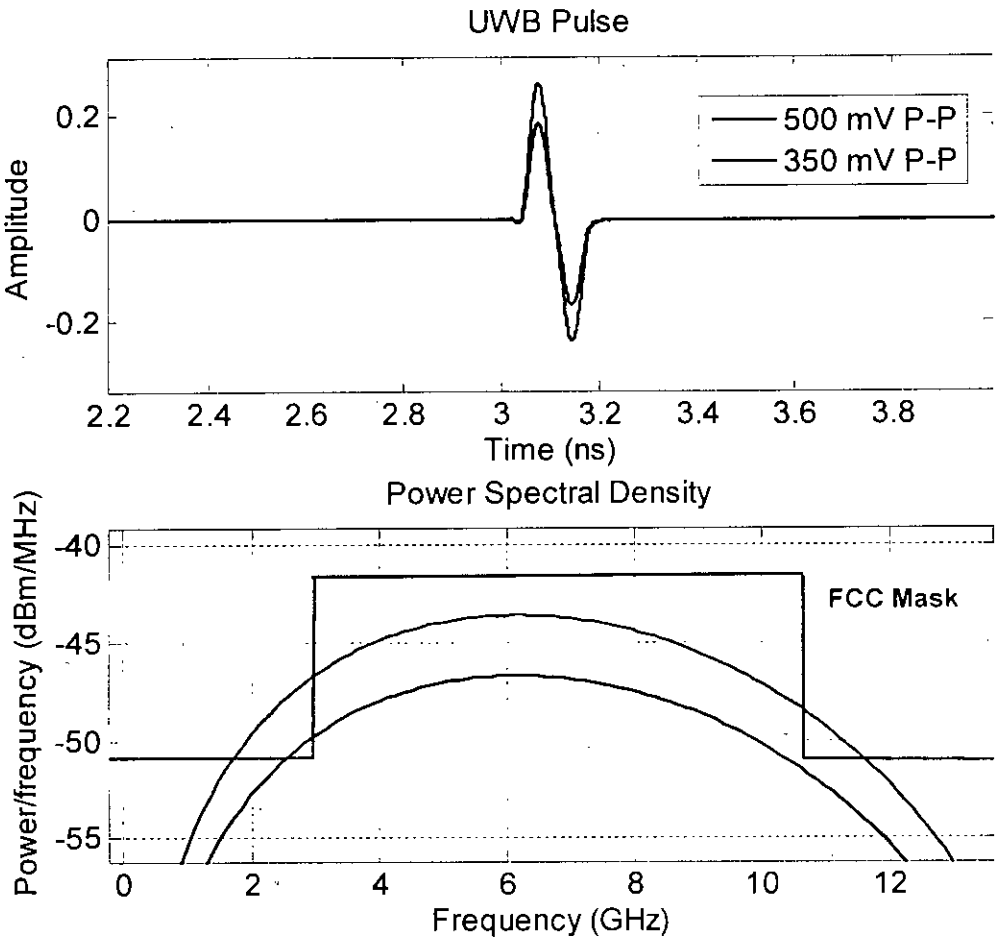


Figure 4.19: Generated UWB Gaussian monocycle pulse and FCC regulations

vi) Summary

The properties of the designed UWB transmitter are summarized in Table 4.2.

Table 4.2: Properties of the designed UWB transmitter

Parameters	Values
Transmitter	IR-UWB
Pulse shape	Gaussian Monocycle
Modulation	OOK/BPSK
Pulse duration	140ps
Peak-to-Peak Pulse Amplitude with R_L=100Ω	800 mV (OOK) 500 mV (BPSK)
Data Rate (Max.)	7Gbps
-3 dB Bandwidth	9 GHz (3.5 -12.5GHz)
Energy consumption	1.10pJ/pulse (OOK) 1.13pJ/pulse (BPSK)
Power Supply	1.2 V
Technology	IBM 90 nm CMOS

4.3.1 Performance Comparison

Table 4.3 compares the designed UWB transmitter with those found in the literature. Energy consumption, pulse amplitude and pulse duration are some of the most important parameters to assess UWB transmitters. It is evident that the proposed pulse generator is appropriate for high frequency UWB pulse generation with large amplitude and very low energy dissipation. Our developed transmitter consumes only 1.13pJ energy per pulse. Although the transmitter designed in [17] consumes less power than our transmitter, the pulse amplitude is only 1.8mV which is not acceptable for practical use. Moreover, no other IR-UWB transmitter provides p-p pulse amplitude as large as 800mV. Table 4.3 also reveals that the generated Gaussian monocycle pulse

has the smallest pulse duration among all the transmitters which is required for high speed data transmission for on-chip wireless interconnects.

Table 4.3: Performance Comparison of UWB transmitters

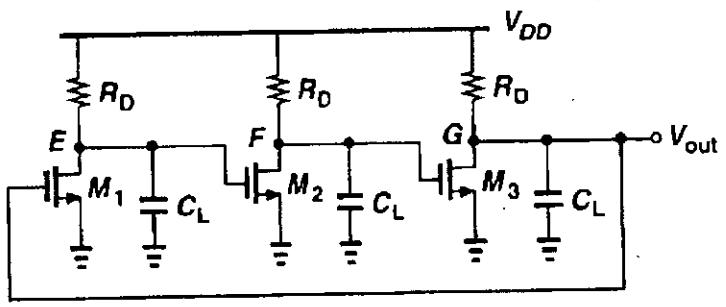
Ref.	Technology (CMOS)	Pulse Shape	Modulation	Energy Consumption (pJ/pulse)	P-P Pulse Amplitude (mV)	Pulse Duration (ps)	Max. Data Rate (Gbps)	Bandwidth (GHz)	Power Supply (V)
This Work	90 nm	GMP	OOK/BPSK	**1.10/1.13**	800/500	140	7	3.5-12.5	1.2
[15]	0.13 um	5th DGP	BPSK	**33**	84	750	1.3	3.1-10.6	--
[16]	0.13 um	GP	BPSK	**30.1**	192	810	1	3-5	1.2
[17]	0.18 um	MP	--	**0.95**	1.8	300	--	--	1.8
[18]	0.18 um	GMP	OOK	**33.8**	160	410	1.4	2.8	1.8
[19]	0.18 um	2nd DGP	BPSK	--	27	250	--	5	1.8
[21]	0.18 um	5th DGP	PPM	**57.5**	154	820	0.4	--	1.8
[22]	0.18 um	--	BPSK	**975**	--	--	0.2	3.1-10.6	1.8
[23]	0.18 um	--	OOK/BPSK	**300**	250	1.4-3.3ns	16-62 Mbps	3-5	1.8
[24]	0.18 um	GMP	--	--	90-140	230-270	--	--	--
[25]	0.18 um	GMP	--	**10.86**	123	280	1.16	4.14	1.8
[26]	0.18 um	7th DGP	--	**4.7**	500	800	--	3.1-5.1	1.5
[27]	0.18 um BiCMOS	MC	BPSK	**(55mW)**	80	1ns	--	3.1-5.1	2.5
[28]	0.18 um	MC	--	**27.6**	673	500	--	5.9-10.4	2.1
[29]	0.18 um	5th DGP	--	**81 (0.38)** **135 (4)**	560 (0.38) 510 (4)	0.38-4ns	10Mbps	3-10	1.8
[30]	0.18 um	GMP	BPSK	**17nJ**	1.8	--	--	3.1-10.6	1.8
[31]	0.18 um	MC	BPSK	**2**	3.6	1ns	100 Mbps	3.1-5	1.8

4.4 Clock Generator

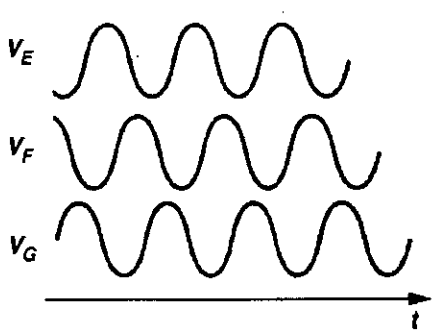
Almost all digital circuits are dependable on at least one clock source, which generates a rail-to-rail square wave. An oscillator is a circuit that produces a periodic signal, without any specific input signal except internal noise. To generate UWB pulses, the designed UWB transmitter also requires a high speed square clock. For each positive rising edge of the clock signal, a UWB pulse is generated. We have designed a high frequency clock circuit following the principle of ring oscillator.

4.4.1 Ring Oscillator

The ring oscillator comprises N amplifiers connected in a feedback loop. To get the ring oscillator to oscillate, there needs to be at least three amplifiers, this to fulfill the first criterion of a sufficient phase shift of 180°. The second criterion for oscillations is met if the closed loop gain is greater than 1. An example of three stage ring oscillator is shown in Figure 4.20.



(a)



(b)

Figure 4.20: Three-stage ring oscillator (a) circuit, (b) waveforms

4.4.2 Single Ended Ring Oscillator with Inverters

A simple digital implementation of ring oscillators is depicted in Figure. 4.21. The basic single-ended topology consists of CMOS inverters. Let us suppose that the circuit is released with an initial voltage at each node equal to the trip point of the inverters, V_{trip}. The trip point of an inverter is the input voltage that results in an equal output voltage. With identical stages and no noise in the devices, the circuit would remain in this state indefinitely, but noise components disturb each node voltage, yielding a growing waveform as shown in Figure 4.21. The signal eventually exhibits rail-to-rail swing.

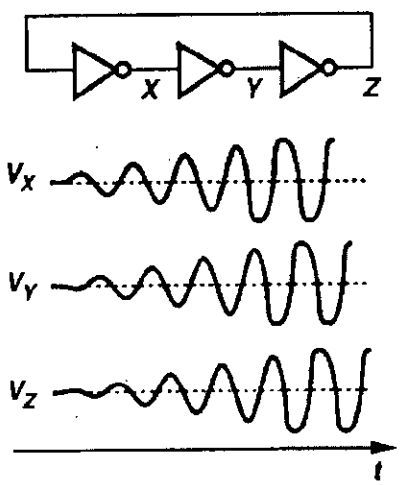


Figure 4.21: Ring oscillator using CMOS inverters

Let us now assume the circuit of Figure 4.21 begins with $V_x = V_{DD}$. Under this condition, $V_Y = 0$ and $V_Z = V_{DD}$. Thus, when the circuit is released, V_X begins to fall to zero (because the first inverter senses a high input), forcing V_Y to rise to V_{DD} after one inverter delay, T_D, and V_Z to fall to zero after another inverter delay. The circuit therefore oscillates with a delay of T_D between consecutive node voltages, yielding a period of $6T_D$ as illustrated in Figure 4.22. T_D is determined by the large signal nonlinear, current drive and capacitances of each stage. When the circuit is released with all inverters at their trip point, the oscillation begins with a high frequency but, as the amplitude grows and the circuit becomes nonlinear, the frequency shifts to $1/(6T_D)$ (which is a lower value). Ring oscillators employing more than three stages are also feasible. The total number of inversions in the loop must be odd so that the circuit does not latch up. A ring incorporating five inverters provides a frequency of $1/(10T_D)$.

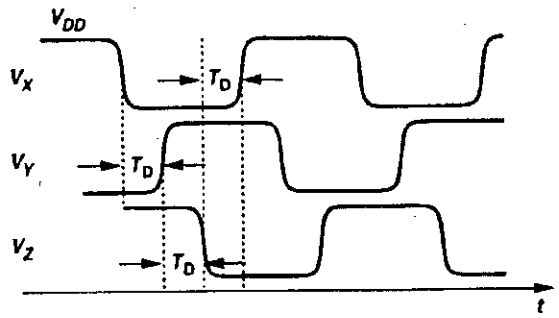


Figure 4.22: Waveforms of ring oscillator when one node is initialized at V_{DD}

In our design, we have used a ring oscillator incorporating three CMOS inverters for achieving a high frequency clock, since the operating frequency decreases with the increase of the number of inverter stages.

4.4.3 Start-up Circuit for Ring Oscillators

It has been seen in the previous section that an initial voltage is required to start the ring oscillator properly. We have devised a circuit to produce this initial voltage by charging a MOS capacitor from a current source. The complete clock circuit is shown in Figure 4.23. Here two inverters 'Inv4' and 'Inv5' are appended at the end as buffers to achieve a good rectangular waveform. The output waveform of the clock is shown in Figure 4.24 and 4.25.

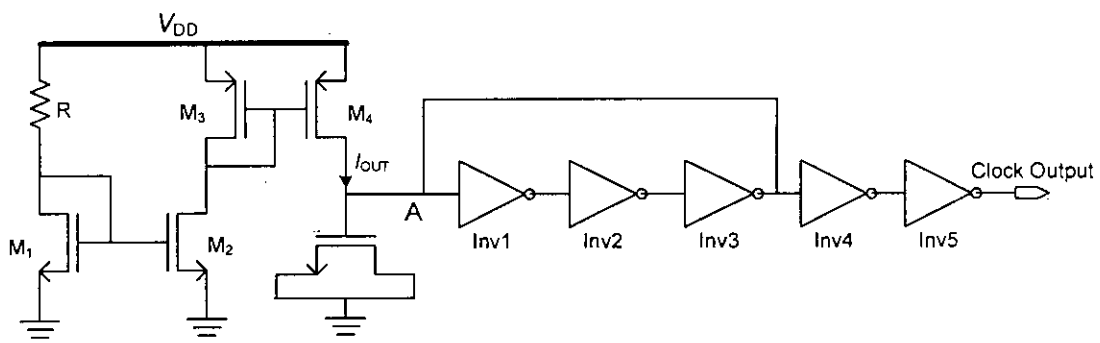


Figure 4.23: Clock generator circuit using current source

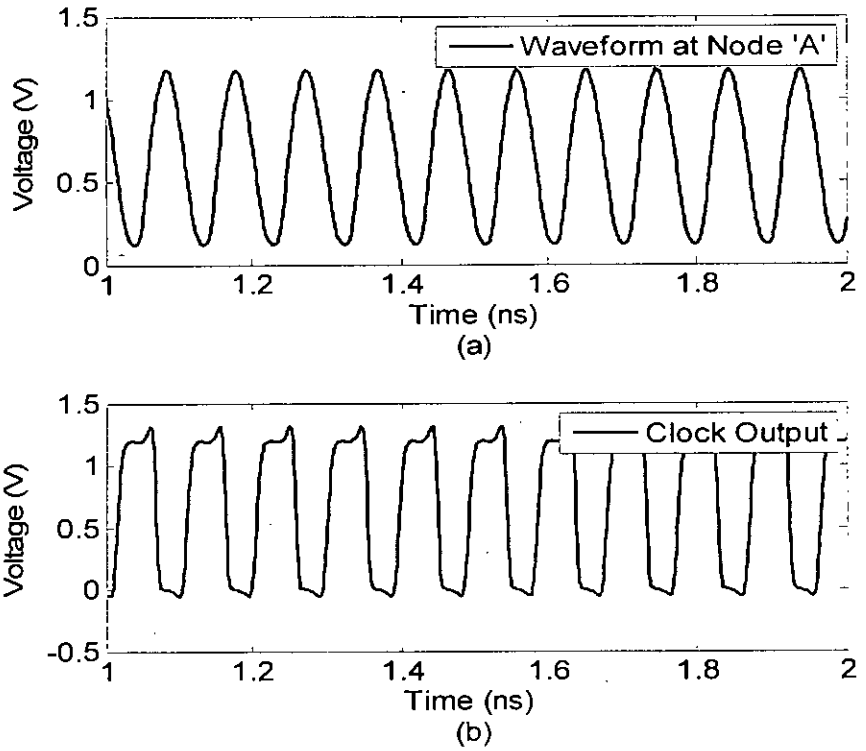


Figure 4.24: Waveform at (a) node A and (b) output of clock generator
(Clock Frequency = 10 GHz)

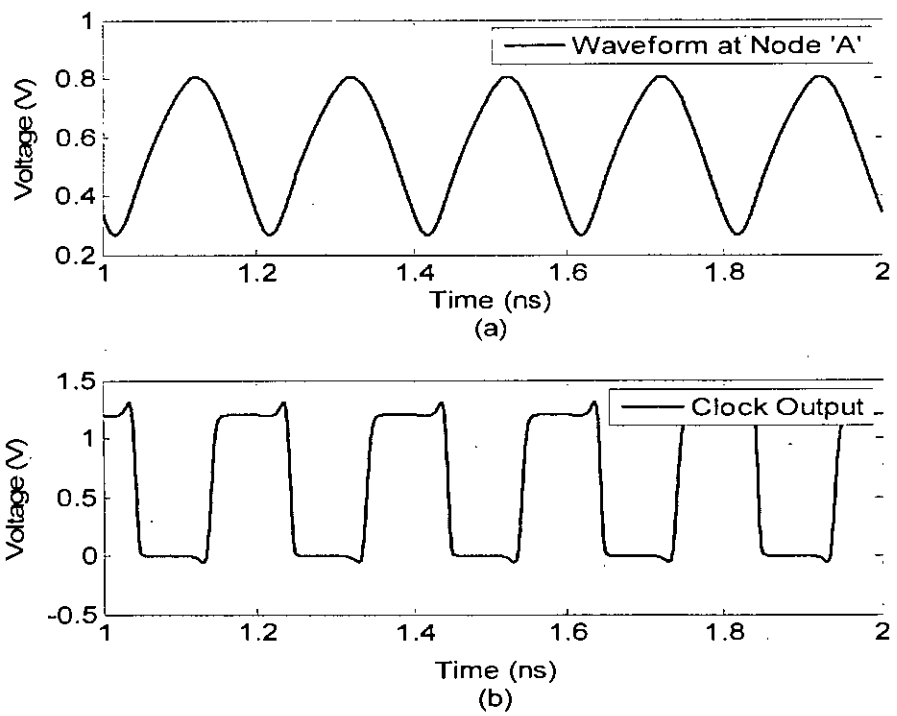


Figure 4.25: Waveform at (a) node A and (b) output of clock generator
(Clock Frequency = 5 GHz)

The operating frequency of the clock depends on the capacitance of the MOS capacitor connected at node A. It can be changed by varying the capacitance. Moreover, a voltage controlled oscillator (VCO) can be used as a variable frequency clock generator to externally control the clock frequency.

CHAPTER 5

ON-CHIP ANTENNA SIMULATION

On-chip antenna is an important component of UWB transceiver for wireless interconnects. Efficient transmission of the generated UWB pulse depends on accurate antenna design. Extensive amount of research have been done for successful wireless signal transmission using Si integrated antenna for on-chip communications along with stacked Si chips [59]-[63]. In this chapter, a dipole antenna is simulated to analyze the received signal and various factors affecting the transmission characteristics of the antenna are explored.

5.1 Transmitting and Receiving Antenna

Several types of antenna such as dipole antenna, loop antenna, patch antenna, micro-strip antenna are used in UWB wireless communications. Among these antenna linear dipole antenna is the simplest form of antenna and also easy to implement.

5.2 Dipole Antenna

A dipole antenna is a straight electrical conductor measuring 1/2 wavelength from end to end and connected at the center to a radio-frequency (RF) feed line. This antenna is one of the simplest types of antenna, and constitutes the main RF radiating and receiving element in various sophisticated types of antennas. The dipole is inherently a balanced antenna, because it is bilaterally symmetrical. The axial length of a dipole antenna can be varied and one usual value is half of the wavelength at the center operating frequency. Figure 5.1 shows a typical sketch of a half wave dipole antenna.

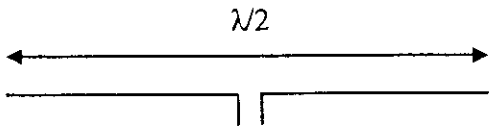


Figure 5.1: Half wave Dipole Antenna

5.2.1 Dipole Antenna Shapes

There are different shapes of dipole antenna such as linear, zigzag and meander dipole antenna as shown in Figure 5.2. In our simulation, we have used linear dipole antenna.

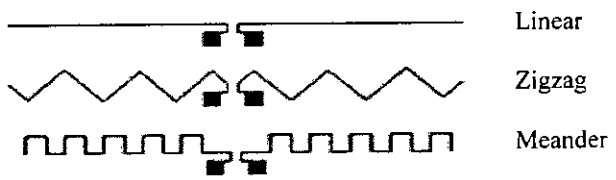
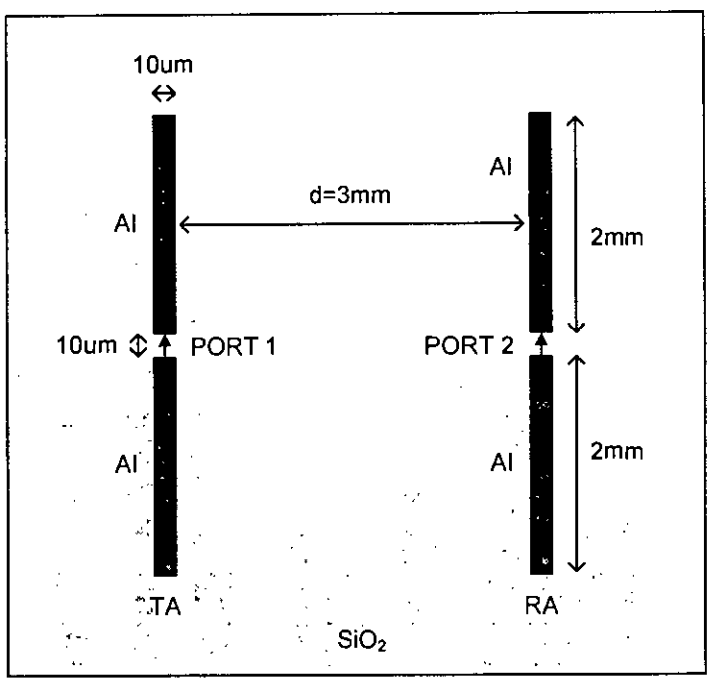
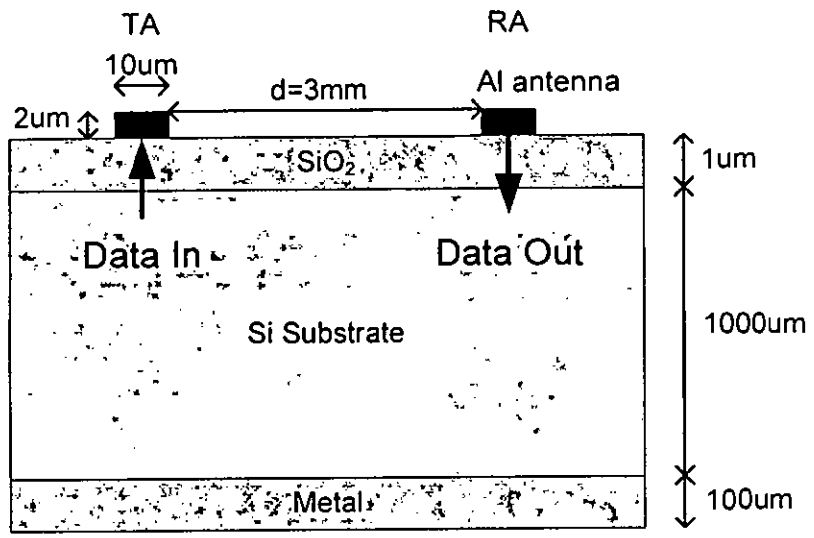


Figure 5.2: Shapes of Dipole Antenna

5.2.2 Device Structure and Simulation Method



(a)



(b)

Figure 5.3: Schematics of the geometry of antenna structure (a) Top view.
(b) Cross section (not to the scale)

Figure 5.3 shows the geometry of a dipole antenna excited horizontally through the plane of the antenna with 1 mm thick Si layer used as substrate. The resistivity of the Si substrate is 10 Ω-cm. A 1 um thick SiO_2 layer is used as insulator on top of the Si substrate. The antenna is formed with first metal layer consisting of 2 um thick Aluminum (Al). A 100 um thick metallic ground is placed at the bottom of the Si substrate.

Simulation is performed with the ANSOFT High Frequency Structure Simulation (ANSOFT HFSS v-9), which is a 3-D full-wave finite element electromagnetic simulator. It divides the simulation regions into a large number of tetrahedral, where a single tetrahedron is basically a four sided pyramid. At each vertex of the tetrahedron, HFSS stores the components of the field that are tangential to the three edges of the tetrahedron. The value of the vector field at points inside each tetrahedron is interpolated from the vertices of the tetrahedron. We have used adaptive meshing in which the simulated structure is initially divided into a coarse number of finite elements of tetrahedral shape. The number of tetrahedrons is increased by 20% between each successive simulation until the simulated s-parameter show a 99.9% match between two successive simulations at every vertex of every tetrahedron in the entire simulated structure.

During the simulation, an axial length (l) of 4mm, and a separation (d) of 3mm between the transmitting antenna (TA) and the receiving antenna (RA) are taken. The permittivity of Si and SiO_2 layers are taken as 11.9 and 4 respectively, and the conductivity of the Al metal layer is $3.8x10^7$ S/m. The frequency is varied from 1 GHz to 30 GHz in 0.5 GHz steps. The 3D structure of the antenna device is shown in Figure 5.4 and the properties of the materials used are listed in Table 5.1.

Table 5.1: Properties of materials used in antenna structure

Materials	Height (um)	Length (mm)	Width (um)	Conductivity (S/m)	Relative Permittivity
Aluminum (Al)	2	4	10	$38x10^6$	1
SiO_2	1	6	14	0	4
Si Substrate	1000			10	11.9
Metal	100			$38x10^6$	1

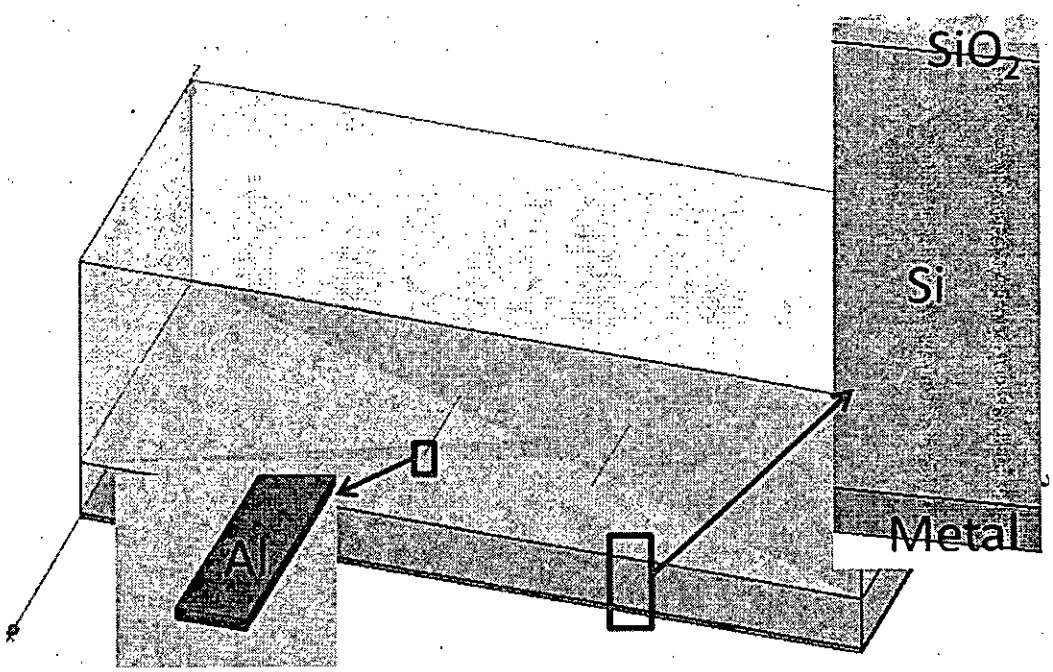


Figure 5.4: 3D structure of the antenna device in HFSS

5.2.3 Transmission Characteristics of Integrated Dipole Antenna

RF networks are usually characterized by a set of simultaneous equations describing the exiting waves from each port in terms of incident waves. Scattering parameters (S-parameters) are the most suitable of them. S-parameters are measured by sending a single frequency signal into the network or "black box" and detecting what waves exit from each port. The four S-parameters are defined as follows (Figure 5.5):

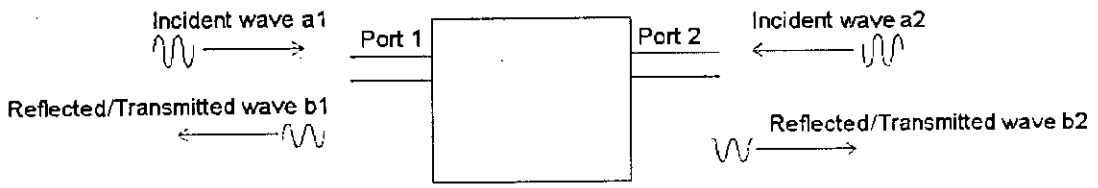


Figure 5.5: Scattering parameter definition

Forward Reflection Coefficient,	S11 = b1 / a1
Backward Transmission Coefficient,	S12 = b1 / a2
Forward Transmission Coefficient.	S21 = b2 / a1
Backward Reflection Coefficient,	S22 = b2 / a2

S-parameters of the dipole antenna system obtained from HFSS simulation is shown in Figure 5.6. Figure 5.6 reveals that the reflection coefficient is minimum around 9 GHz and the transmission coefficient is maximum around 12 GHz. Also the bandwidth of S21 is very wide as required. The power spectrum of the transmitted UWB signal is shown in Figure 4.16 in chapter 4, and the –10 dB bandwidth of the signal is found to be approximately 15 GHz with a center frequency of around 10 GHz. The 4 mm dipole antenna, therefore, can be used for transmitting the UWB signal generated from the pulse generator devised in chapter 4.

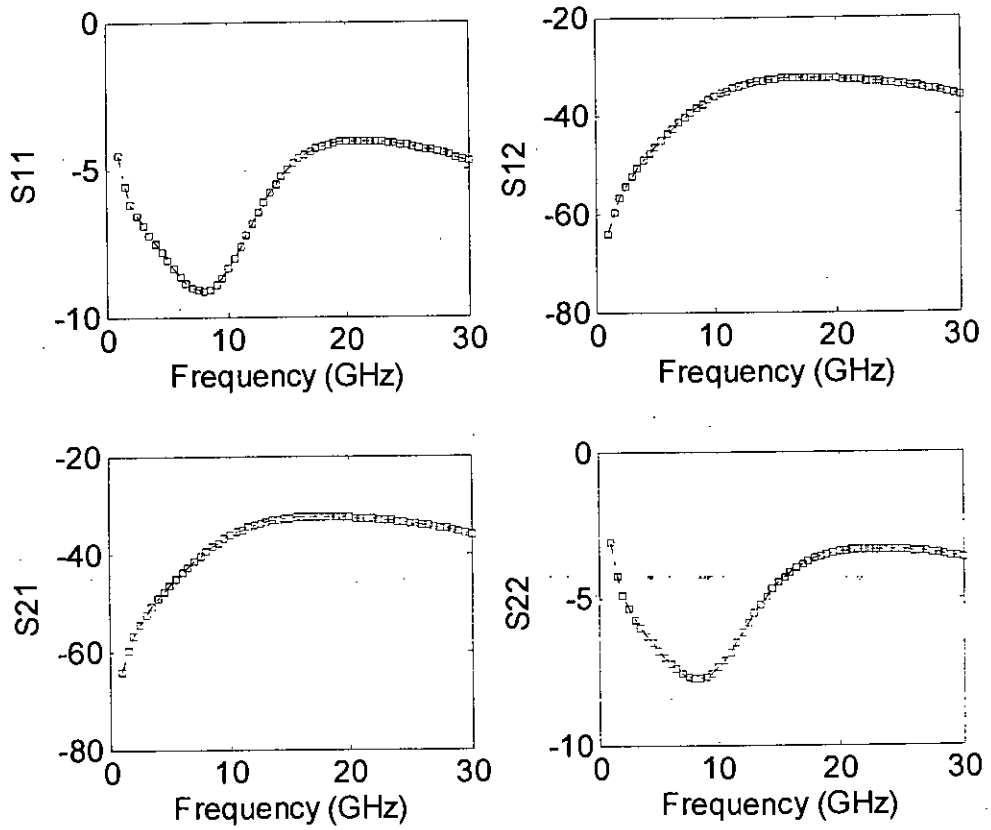


Figure 5.6: Transmission characteristics of integrated dipole antenna (l = 4mm, d = 3mm)

The resonance frequency of a dipole antenna is given by

$$f_{air} = \frac{c}{\lambda} \tag{5.1}$$

and

$$f_{Si} = \frac{f_{air}}{\sqrt{\varepsilon_r}} \tag{5.2}$$

where f_{air} = resonance frequency in air

f_{Si} = resonance frequency on Si chip

c = velocity of light (3 x 10^8 m/s)

λ = wavelength and ε_r = dielectric constant of Si

In our antenna system, $\lambda = 8$ mm , $\varepsilon_r = 11.9$

Therefore, $f_{air} = 37.5$ GHz and $f_{Si} = 10.87$ GHz

To explore the effects of the antenna length (l) on resonance frequency, simulations are done for three different antenna lengths: l = 2mm, 3mm, 4mm and the results are shown in Figure 5.7. Both the resonance frequency and the transmission coefficients shift to higher frequency as antenna length decreases. Much of the transmitter power in the lower frequency region will, therefore, not propagate through the channel if the antenna length becomes smaller than 4 mm.

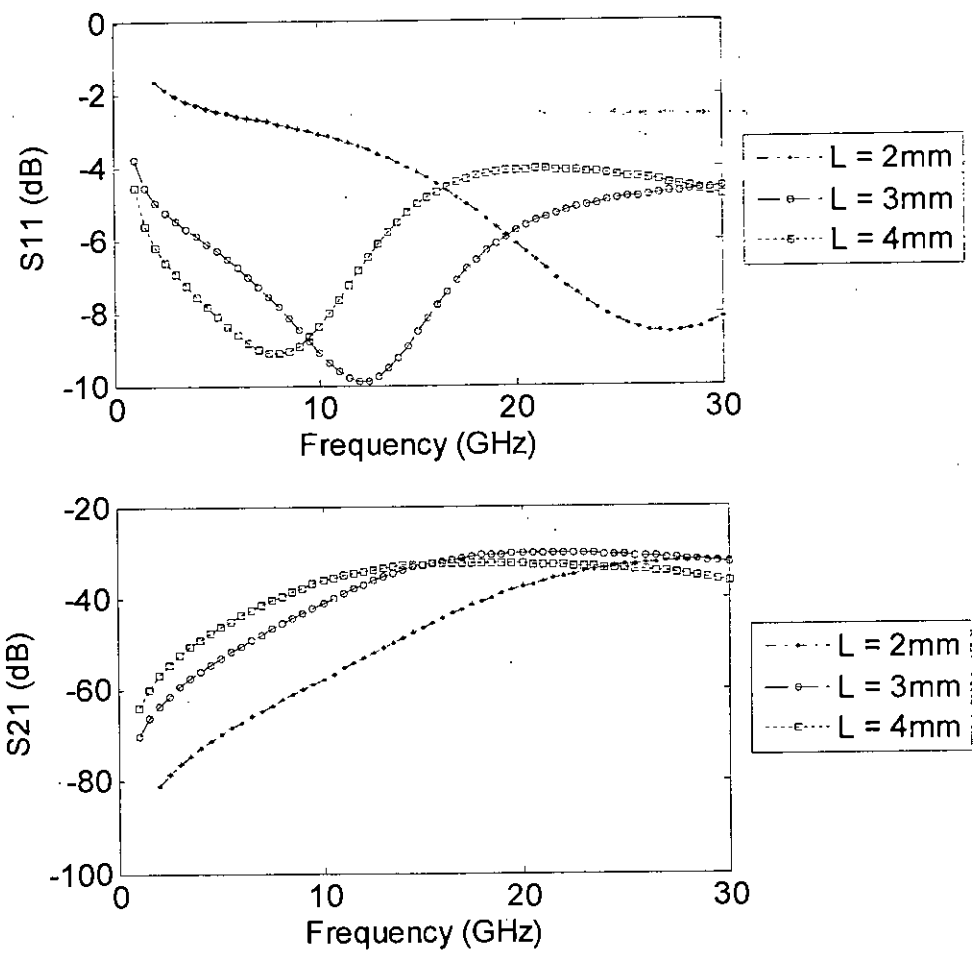


Figure 5.7: Effect of antenna length on transmission characteristics

Antenna gain also depends on the separation (d) between the transmitting and receiving antennas. The antenna pair is placed at three different distances: d = 1mm, 3mm, 5mm and the variations of reflection and transmission coefficients obtained for these distances are shown in Figure 5.8.

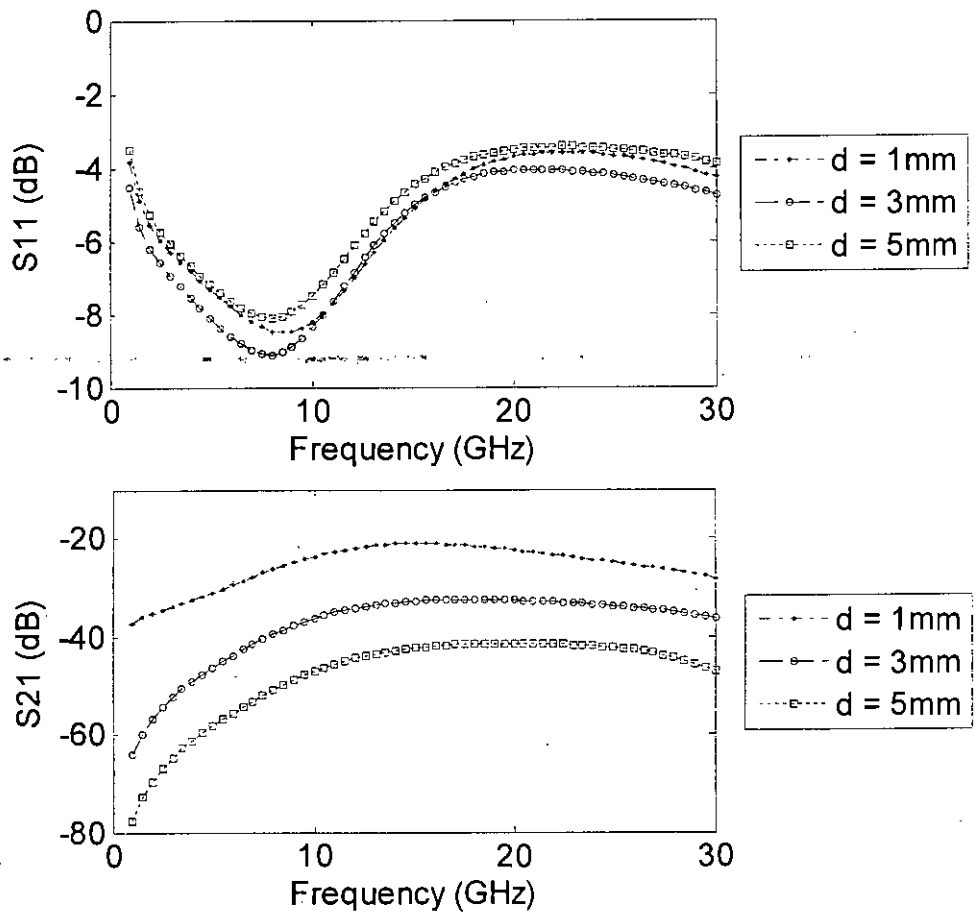


Figure 5.8: Effect of antenna separation on transmission characteristics.

5.3 Received UWB Signal

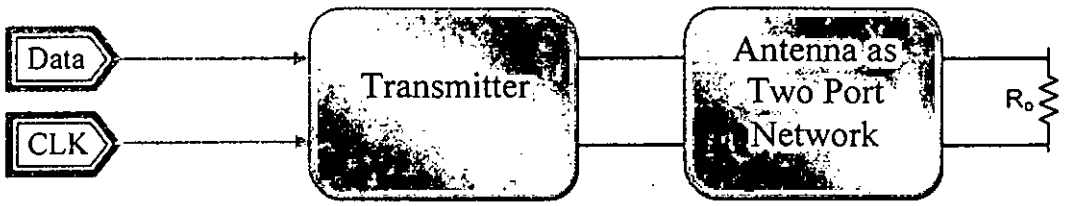
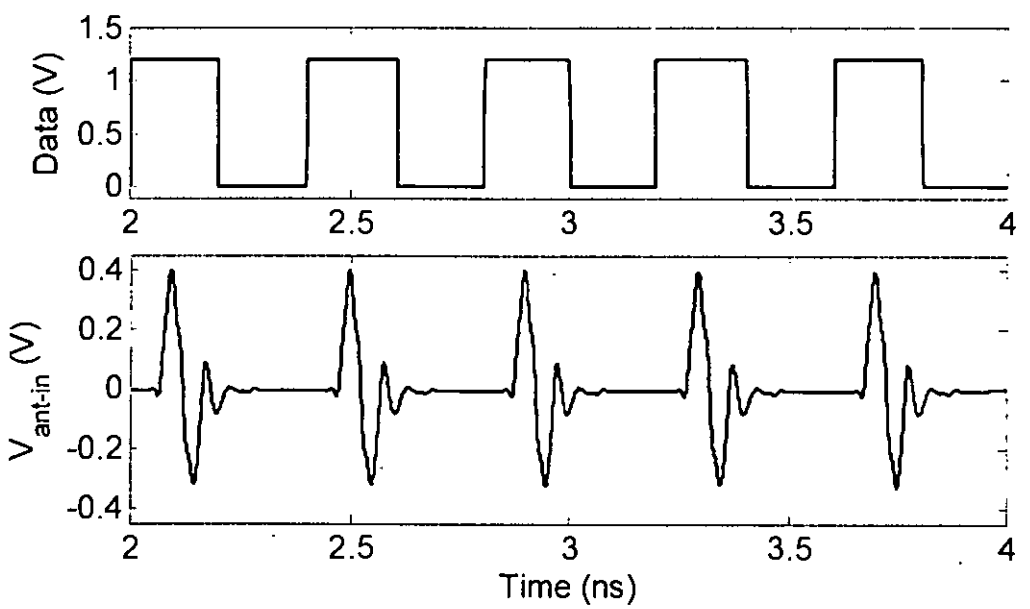
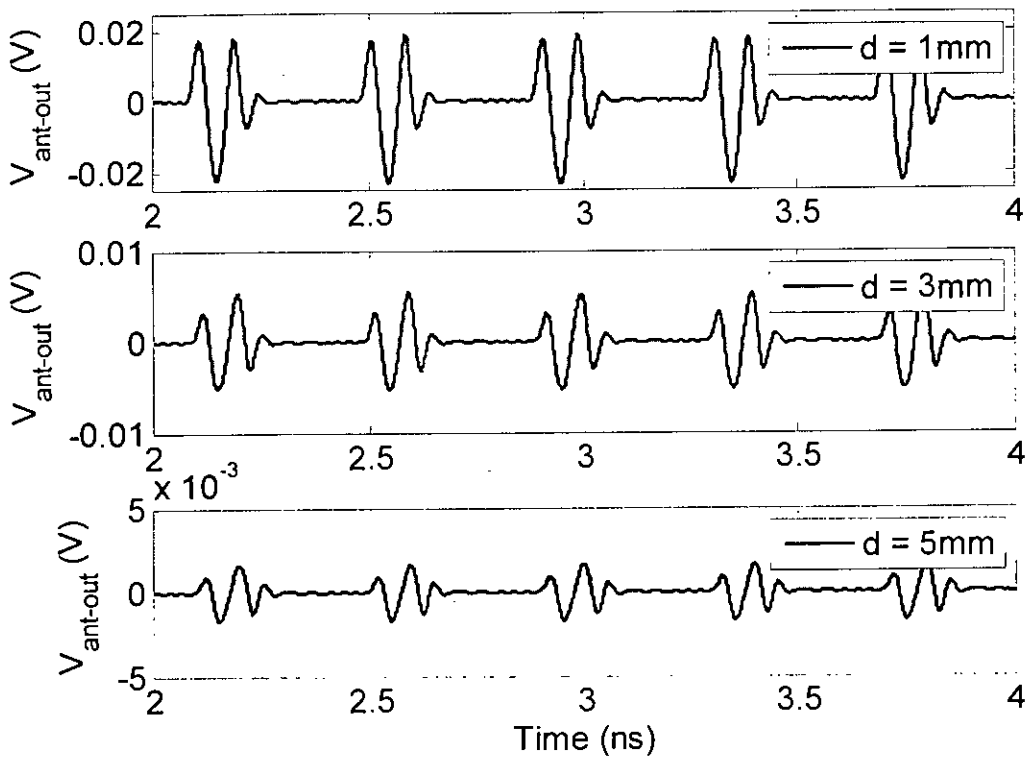


Figure 5.9: Simulation of antenna output signal in Hspice

The extracted S-parameters of the dipole antenna are used to simulate the received UWB signal at the receiving antenna. In Hspice the antenna system is represented as a two port network defined by the scattering parameters of the antenna pair. The input port of the two port network is connected to the end of the transmitter designed in chapter 4 and the output port is terminated by a 100 Ω load resistance as shown in Figure 5.9. The received UWB signal at the output port is shown in Figure 5.10 for three antenna distances. **UWB pulse trains are observed successfully at the receiver with a peak-to-peak voltage of 10.7 mV for a communication distance of 3mm.**



(a)



(b)

Figure 5.10: (a) Transmitted UWB signal (b) Received UWB signal for various distances

It is, therefore, feasible to transmit Gaussian monocycle pulse train generated from the designed transmitter through the on-chip Si integrated antenna and receive successfully at the receiver with sufficient amplitudes.

CHAPTER 6

CONCLUSION

6.1 Summary

In this research, we first investigated the potentials of ultra wideband transmission technology to be used as wireless interconnects system. We proposed a simple UWB wireless transceiver system architecture for on-chip implementation. The system exploits transmitted reference scheme which allows a straight-forward synchronization technique by giving proper delay to the reference pulse and also avoids complicated intra-chip channel estimation for the detection unit. Therefore, the system behaves like a self synchronous system. We then explored the ultimate UWB pulse shape to be used for data transmission which simultaneously satisfies the FCC regulations and the requirement of high throughput. Although in several publications higher order derivatives of Gaussian pulse are proposed only for satisfying the FCC mask without any consideration about data rate, we projected for using Gaussian monocycle pulse to support high speed data transmission.

We then devised two low power high speed fully digital differential UWB transmitters for our designed wireless system: one for OOK system and the other for BPSK system. Both the transmitters can be operated in either single pulse mode or transmitted reference mode. The whole circuit is simulated in HSPICE using IBM 90nm CMOS technology. The performances of the transmitters are evaluated and compared with some other available transmitters in the literature. The generated pulse is Gaussian monocycle and it has a width of 140ps and peak-to-peak amplitude of 500mV in case of BPSK transmitter. The output pulse with reduced amplitude can satisfy FCC regulation. The transmitters can transmit data at a rate of 3.5 Gbps in TR mode and 7 Gbps in SP mode. It provides the highest data transmission rate among previously reported pulse generators.

The design also requires less number of gates and, thus, reduces the cost. The major advantage of the proposed transmitter is its low power consumption. 'Energy consumption per pulse' is the figure of merit of any UWB wireless transmitter. Our BPSK transmitter consumes only 1.13pJ/pulse which is lower than any other UWB transmitter. High data rate, simple design and low power consumption make the proposed UWB TR transmitters appropriate for on-chip implementations.

Finally, successful signal reception at the output of on-chip dipole antenna was confirmed by the simulation of Si integrated dipole antenna together with the developed transmitter.

6.2 Future Works

- We bypass the need for channel estimation by using TR technique; but comparisons between TR and non TR systems in terms of data rate, bit error probability and system complexity are still to be done.

- Throughout this work, we have designed two UWB transmitters for wireless inter-chip communication. The circuits were designed at the schematic level. The other steps required for fabrication - layout drawing, parasitic extraction, post layout simulation etc. still need to be completed.

- In this research, we used IBM 90nm CMOS technology. More recent technology may be used for achieving higher bit rates.

- This developed UWB transmitter may now be connected to a suitable UWB receiver to analyze the performance of the complete transceiver system.

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