A Simulation Based Comparative Analysis of Performance Limits of High Mobility MOSFETS of Alternate Structures

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Declaration

It is hereby declared that this dissertation is the result of my own work except where explicit reference is made to the work of others, and has not been submitted elsewhere for the award of any degree or diploma.

____
(Mahmudur Rahman Siddiqui)

To my beloved parents.

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I would like to express my sincere gratitude to my supervisor, Dr. Quazi Deen Mohd Khosru, Professor, Department of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, for his generous help, warm encouragement and support throughout my graduate thesis. Throughout my life I will benefit from the experience and knowledge I have gained working with him.

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Abstract

After dominating the the semiconductor logic industry for decades the reign of Si is coming to an end. Aggressive scaling of MOSFETs have pushed Si towards its physical performance limits. By the end of this decade the Si MOSFETs will reach their theoretical limits. To continue the scaling of logic devices and improve performance of integrated circuits researchers must find a suitable replacement for Si. To meet the high current demands the replacement must have high carrier mobility. III-V semiconductors appear as perfect candidates for nMOS materials as they have very high electron mobility. But there are many possible III-V materials. Also the aggressive scaling of Si has given birth to some very innovative structures which solves very critical problems of nano-scale fabrication. Few of such innovative structures are Double gate MOSFETs, Semiconductor On Insulator MOSFETs, FinFETs etc. These structures might be utilized to achieve further performance enhancement of the III-V based MOSFETs. Researchers all around the world are searching for the best possible alternative using III-V materials. But fabrication of III-V materials pose some difficult challenges. One such challenge is the gate dielectric. The III-V materials do not have aa natural oxide dielectric like Si and thus growth of a dielectric with acceptable interface quality is very difficult and perfecting one process is time and resource consuming. A theoretical study of all the possible options of III-V MOSFETs will shed some light on how to choose the most optimum path of device development and ensure perfect utilization of resources and time. Thus theoretical evaluation of different performance markers of a MOSFET using III-V material has become very important. There are several performance markers for a MOSFET. The On current denotes the current driving capability of a MOSFET which in turn decides the speed of a logic circuit. The subthreshold swing decides the power loss of a MOSFET. The on/off current ratio also is a performance parameter of a MOSFET. As integrated circuits are being shrunk down the speed of a transistor needs to increase while the power consumption must decrease. Thus a systemic study of the On current of a MOSFET will provide the engineers with one basis of selection or even lead to early elimination of

some device structure that will not be able to sustain performance improvement in the long run without wasting valuable time and resources. In this study a comparative picture of the transistor On current for four different structures utilizing five different III-V semiconductor is presented. The calculation has taken into account the quantum mechanical effects active at the operating device dimensions. Only the limiting current is considered here and all imperfections are ignored as the objective is to draw a comparative picture of the ultimate performances of these devices.

Chapter 1

Introduction

1.1 Introduction

Silicon (Si) has dominated the semiconductor industries for decades. The performance of Si Metal Oxide Semiconductor Field Effect Transistors (MOSFET) have been improving with the gradual scaling of the devices as per Moor's Law. With scaling of MOSFETs the oxide thickness has gone down to facilitate lower operating voltage but at the same time increasing gate leakage current. Also the channel lengths have been reduced thus increasing the drain current. But gradually this scaling is pushing Si MOSFETs to their performance limits. SiO_2 was the preferred gate dielectric material for Si based MOS devices as SiO_2 is the natural oxide of Si and the fabrication process is very simple. Also the interface quality is very good. But due to the high tunneling current at nano-scale the gate dielectrics of current Si MOSFETs are high-κ materials. Also current carrying capability of Si is approaching the target drain current [1]. The limiting performance of Si MOSFETs is presented in [2]. The typical bulk Si MOSFET has already reached its best performance and to achieve further improvement Si MOSFETs with different structures is being considered.

Different device architectures have been explored utilizing Si to improve performance and achieve continuous scaling. Multiple gate structures stirred the most attractions. Different multiple gate structures have been investigated such as Double Gate (DG) and triple gate MOSFETs [3, 4, 5]. Other structures using Si for high performance nano- MOSFETs that have undergone extensive research are Si On Insulator (SOI) MOSFETs and FINFETs [6, 7].

These alternate structures have brought certain improvement to the characteristics of the MOSFET compared to the bulk MOSFET. But the current carrying capability of Si is limited due to the low electron mobility and also high electron effective mass. As a result, Si will not be able to provide the required drain current in future technology nodes. To meet the drain current requirements materials with higher electron mobilities are essential [8, 9].

Research community is searching for high mobility alternative materials for the future high speed logic devices to continue the predicted performance enhancement [10]. Carbon nanotubes [11], Si nanowires [12], Graphene [13], Ge [14] and III-V compound semiconductors such as InSb [15, 16] and InGaAs [17, 18] are among the materials studied as they have high electron and hole mobility. As the mobility becomes higher the maximum drain current also increase as well as the speed of the device.

III-V compound semiconductors shows good promise as the building block of the future high speed and low power nMOSFETs as they have very high electron mobility. But there are many different possibilities both in material composition and device structures. As research community improves the fabrication process of compound semiconductor devices, effects of imperfections such as interface traps and oxide traps are reducing. These impurities have to be reduced to an acceptable value before these devices are ready for industrial production. Under these conditions the performances of these devices will approach their limiting values. A comparative study of the limiting performance of these devices can shed some light on the most preferable path of evolution of compound semiconductor based devices.

1.2 Literature Review

III-V compound semiconductors have very high electron mobility compared to Si. As a result the drain currents in III-V material based n-MOSFETs are much higher compared to Si. From transport viewpoint, ternary InGaAs has its advantages over binary materials (GaAs, InAs etc.) as its larger inter-valley separation (0.5 eV for $In_{0.53}Ga_{0.47}As$) ensures lower degradation of electron transport under high drain bias. One of the major challenges in the development of III-V semiconductor MOSFETs is the development of suitable gate

dielectrics. Ren et al. have fabricated enhancement-mode n-channel InGaAs MOSFETs for the first time using Ga_2O_3 and Gd_2O_3 as gate dielectrics [19]. Passlack et al. also reported enhancement mode nMOSFETs with high mobility channel material [21]. Researchers have also reported other different MOSFETs using III-V compound semiconductors that provide enhanced drain current and high speed.

Structural change can further improve the performances of the MOSFETs. Xuan et al. have reported increased drain current in surface channel InGaAs MOSFETs with surface layer enriched with In [20]. These surface channel MOSFETs have relatively long channel. They use atomic layer deposited (ALD) Al_2O_3 as gate dielectric. The interface quality of this dielectric is very poor [22]. The performance enhancement under ideal condition is still unexplored.

In case of Si based devices, the Semiconductor On Insulator structure has shown better performance. Thus similar structure also caught the interest of researchers. The III-V on insulator structure has already found important use in photonic circuits and LASERs. But their application as high performance MOS devices also shows promise [23]. Researchers are also investigating the possibilities of double gate and SOI MOSFETs using III-V materials as channel [25]. The impact of variation in material composition of the constituting III-V semiconductor is yet to be explored. Also the impact of the channel width on the drain current is still under study. The fabrication of III-V material based devices are complicated by oxide growth and appropriate substrate fabrication. As a result nano scale device fabrication is quite complicated. Thus theoretical studies are required until fabrication techniques are perfected.

The FinFET structure has achieved very good success for Si based MOSFETs. The FinFET structure is an evolved from of the double gate structure but it provides better performance than double gate MOSFETs and also provides easier fabrication options. The use of FinFET structure for III-V based nano MOSFETs might also avail the same advantages that have been observed for Si. Wu et al. have successfully fabricated III-V based FinFET

[24]. The possible improvements of performance with change of material and with scaling is still under research.

Another innovative structure that has caught attention of the research community is the Quantum Well FET (QWFET). The QWFET is inspired by the High Electron Mobility Transistor structure (HEMT). These devices are still under fabrication research statge. InGaAs and InSb based quantum well FETs have been reported for ultra-high speed and low power operation [15, 16, 17, 18]. These QWFETs show very promising results for future high performance applications.

1.3 Objective of The Thesis

The interest of research community in high mobility semiconductors has intensified due to the limitations of Si devices at sub 16 nm nodes [1]. Researchers are investigating the prospects of MOSFETs of different structures using compound semiconductors. As mentioned in the previous section the fabrication process of III-V based transistors are complicated due to the oxide interface quality and substrate growth. Thus significant efforts are necessary to perfect the fabrication procedure of these devices. A theoretical study of performance limits of each structure and the variation of performance with the constituting material composition will give a direction to focus all our efforts on perfecting the fabrication process of the most attractive III-V based MOS structure.

The most important performance indicators of a transistor are the On current, subthreshold swing and the on-off current ratio. The determination of On current requires the analysis of the device under strong inversion. For determination of the off current and sub-threshold swing the device has to be analyzed under low bias. For different structures different boundary set ups are required for the theoretical study. The two analysis require different algorithms. In this thesis the On current is determined and compared for different material and structure combinations. This study portrays a comparative picture of the On current of these devices and provides a basis of selection. The subthreshold characteristics

will also play a role in making the most optimized selection but the sub-threshold region is outside the scope of this work.

The bulk MOSFET structure has been taken as the basis of comparison for this study. The on current of the bulk MOSFETs will be calculated for different III-V materials. Then the drain currents for DG MOSFETs, SOI MOSFETS and Surface Channel MOSFETs will be compared with the bulk device to investigate the impact of the structural change on the device performance. Also the currents will be compared among each device to understand the impact of change in material on the drain current. Here, the FinFET structure and the QWFET structure is excluded. Because the FinFET structure requires a 2D analysis environment while bulk, surface channel, DG and SOI MOSFETs can be analyzed in a 1D environment. While the QWFET structure uses very thin quantum well layer as channel. The thin layer changes the energy-momentum relationship of electron in the channel. As a result, the effective mass approximation is not valid for QWFETs. The analysis of such devices requires eight band k-p method for determination of effective mass of electrons of different energies. Thus the QWFET structure does not comply with the simulator used for the other four structures.

In this thesis, performance limits of MOSFETs of several different structures will be determined using numerical simulation. The simulation involves using the electrostatic solutions of the devices to determine the ballistic currents. Electrostatic solutions for different biases will be acquired by solving the coupled Schrdinger's and Poisson's equations self-consistently [26]. The Poisson's equation will be solved using finite difference method and the Schrdinger's equation will be solved using Hamiltonian matrix formalism [34]. The obtained electrostatic solution will be used to determine the ballistic current of the device using the over-the-barrier model [27, 28]. The equation system will be modified according to the physical structure of the device with appropriate boundary conditions. As compound semiconductors will be used for the devices under study, an appropriate determination of material parameters according to the composition of the semiconductor is required. All the

necessary material parameters will be adjusted according to the material compositions using appropriate equations.

This thesis will shade light on the impact of change in material parameters such as electron effective masses, band gap etc. on the drain current of a device. Also, we will gain insight on the impacts of changing in device structures on drain current which will provide a better understanding of the impacts of quantization and strain.

Chapter 2

Ballistic Current

The carrier transport in long channel devices can be accurately modeled by using carrier mobility as the channel length is much larger than the scattering length or mean free path. Thus an electron or a hole experiences many collisions before reaching its destination. As a result the statistical parameter mobility gives an accurate picture of the carrier transport. But as the device is scaled down, the number of collisions experienced by carriers while moving from source to drain reduces. As a result the assumption of mobility becomes less effective. A Monte Carlo simulation done by a IBM group [29] showed that near ballistic transport is reached for Si Semiconductor On Insulator (SOI) MOSFETs for a channel length of 30 nm. III-V materials such as GaAs and InAs has much higher mean free path for electrons compared to that of Si. Thus it is expected that the electron transport in III-V MOSFETs will be ballistic in future devices where physical channel length is expected to be in the sub 15 nm range [1].

The ballistic current for different devices has been determined using the Over-the-barrier model. The Over-the-barrier model was first proposed by Kenji Natori in [27]. The same model was adopted by Asad et al. [28] with slight modification. The model used by Asad has been adopted in this work. In this chapter the Over-the-barrier model is discussed at length. The algorithm for calculating the current is also discussed.

2.1 Physics of the Over-the-barrier model

In ballistic transport no scattering occurs while the carrier travels from the source to the drain. The current is given by the net charge flow from the source to the drain that is the difference between carriers flowing from source to drain and those flowing from drain to source. The potential energy for electron from the source to the drain forms a barrier. When no voltage is applied across the the source and drain the potential at both the source and the drain is same. But due to difference in dopant types between the source and drain diffusions and the channel region, the channel potential forms the barrier. When a positive voltage is applied between the drain and the source the potential of the drain goes down. Thus the drain end of the barrier goes lower. Thus the potential rises sharply from the source end to a maximum value and from the top of the barrier the potential gradually decreases towards the drain end. This is depicted in Fig. 2.1. The picture shows that the top of the barrier energy does not change with the drain voltage.

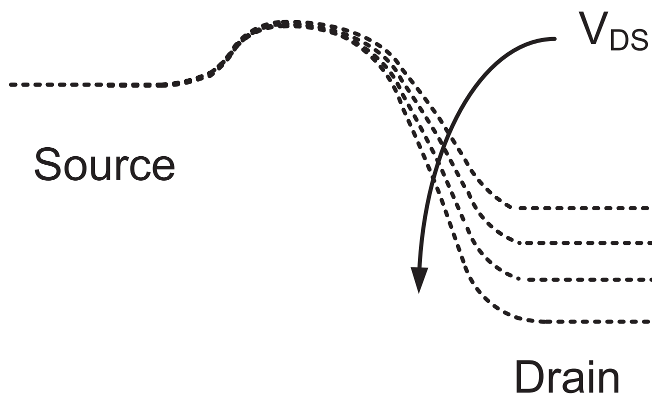

Figure 2.1: Schematic diagram showing bottom of the conduction band variation with increasing drain bias under a fixed gate bias.

The maximum energy of the potential barrier plays a significant role in Over-the-barrier model. This point is denotes as Top-of-the-barrier. In Over-the-barrier model it is assumed that all the carriers injected from the source that have lower energy than the Top-of-the-

barrier energy is reflected back towards the source by the barrier. The carriers contributing in the drain current are those that have energy equal or higher than the Top-of-the-barrier energy. Thus the carrier concentration at the position of Top-of-the-barrier is required to determine the ballistic drain current.

The states at the Top-of-the-barrier are filled according to the source and drain fermi levels depending on the momentum of the state. This is shown in Fig. 2.2. The positive k states are filled according to the source Fermi level and the negative k states are filled according to the drain Fermi level. When no voltage is applied across the drain and source the Fermi levels are at the same energy for both the source and the drain. As a result the carrier distribution around the k-space is symmetric. Thus the numbers of carriers traveling along the +x direction and the -x direction are equal resulting in a zero current. When a voltage is applied between the drain and the source the drain Fermi level becomes lower compared to the source Fermi level. Thus the number of carriers occupying the -k states becomes lower. As a result the carrier distribution changes. The number of carriers traveling towards the source (-x direction) becomes lower compared to the carriers traveling towards the drain (+x direction).

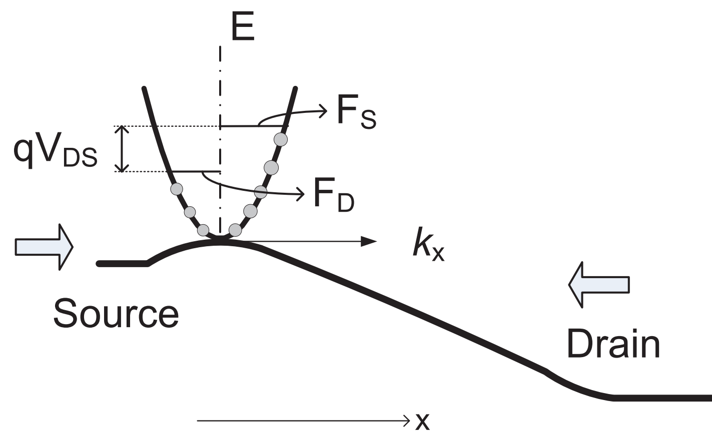

Figure 2.2: Schematic diagram shows over-the-barrier transport in an n-MOSFET under drain bias.

As the drain voltage increase and the drain Fermi level goes down the number of -k state carriers decrease. To maintain the gate voltage the total number of inversion carriers needs

to stay constant. This is an important assumption of the Over-the-barrier model. To keep the total inversion charge constant the source Fermi level has to be adjusted accordingly. Thus the carrier concentration remains the same as the equilibrium concentration but the distribution of the carriers around the k-axis changes as the drain voltage is increased. Once the drain voltage reaches a high enough value all the carriers occupy the +k states. As a result the current reaches a maximum value at this drain voltage. If the drain voltage is further increased the current stays constant.

The total number of carriers is controlled by the applied gate voltage. As the gate voltage is increased the barrier height reduces that is the Top-of-the-barrier energy reduces. This is shown in Fig. 2.3. The increase in gate voltage results is an overall increase in carrier concentration. The number of carriers for a given gate voltage can be calculated by solving the equilibrium electrostatic of the device. The determination of the equilibrium electrostatics of the device is discussed in the next chapter.

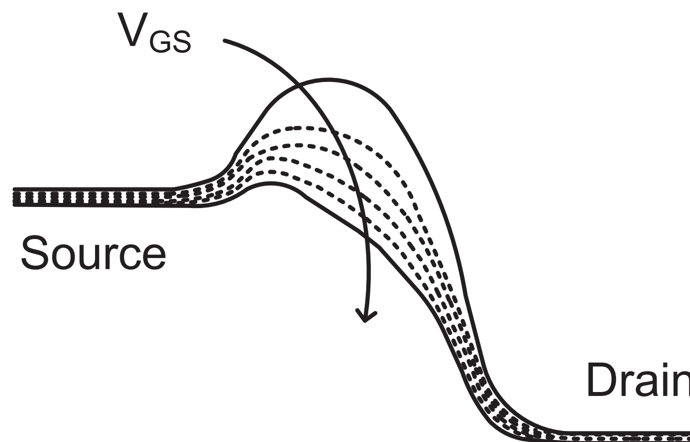

Figure 2.3: Schematic diagram showing bottom of the conduction band variation with increasing gate bias under a fixed drain bias.

It is apparent from the discussion that the Top-of-the-barrier plays a significant role in the Over-the-barrier model. The electron potential energy reaches a maximum value a small distance away from the source. To determine the Eigen states at the Top-of-the-barrier the

gate voltage at this position is required. The distance of the Top-of-the-barrier from the source is very small and it is neglected for this study. This assumption does not affect the ballistic current as the ballistic current only considers the carriers flowing above the Top-of-the-barrier energy. Thus the gate voltage at the source end can be used to determine the equilibrium carrier concentration for the device which is equal to V_{GS}. The current due to carriers tunneling trough the barrier is ignored in this study. This component of the current is ignored as it does not contribute to the limiting current of the device.

2.2 Mathematical formulation and algorithm

As discussed in the previous section the ballistic current is determined from the difference between carriers flowing in the +x direction and -x direction. To find the carrier distribution in the k-space, first the total carrier concentration must be determined for the equilibrium condition at the Top-of-the-barrier. This is done by solving the coupled one dimensional Poisson-Schrödinger equations for the applied V_{GS}. This solution process is discussed in the next chapter. The solution of the coupled Poisson-Schrödinger equations gives the equilibrium carrier concentration N_{inv} and the Eigen energies ε.

From the Eigen energies and the drain Fermi level for a given drain to source voltage V_{DS} the number of -k state carriers can be determined. From the total number of inversion carriers obtained from the electrostatic solution and the number of -k state carriers the position of the source Fermi can be adjusted. The adjusted source Fermi level gives the total number of carriers in the +k states. The number of carriers in i-th sub band N^i_{inv} can be calculated using the source and the drain Fermi levels with Eq. 2.1 and the total number of carriers can be calculated by summing N^i_{inv} for all the sub bands (Eq. 2.2)

$$
\begin{aligned}
N^i_{inv} \;=\; & \left[\frac{m_{Di}}{\pi\hbar^2}\frac{K_BT}{2}\right]\{\ln\left(1+exp\left(\frac{E_F-\varepsilon_i}{K_BT}\right)\right) \\
& +\ln\left(1+exp\left(\frac{E_F-\varepsilon_i-qV_{DS}}{K_BT}\right)\right)\}
\end{aligned}
\tag{2.1}
$$

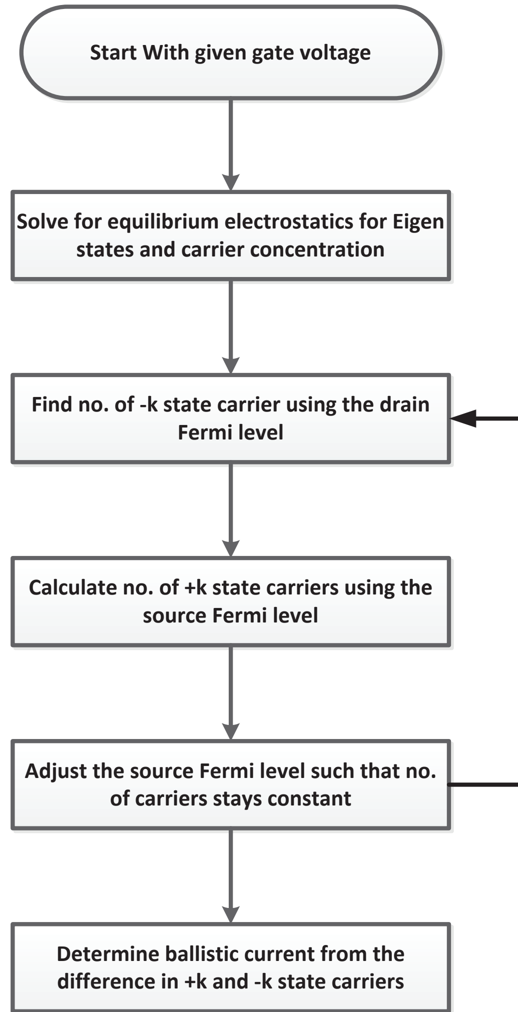

Figure 2.4: Algorithm for calculating the ballistic current for a given gate voltage.

$$N_{inv} = \sum N_{inv}^{i} \tag{2.2}$$

Here, m_{Di} is the density of states effective mass and E_F is the Fermi level at the source end and E_F - V_{DS} gives the drain Fermi level. E_F is adjusted so that the total number of carriers N_{inv} is equal to the carrier concentration obtained from the electrostatics solution.

The adjusted source Fermi level and the calculated Eigen states are used in Eq. 2.3 to calculate the current for the i-th sub band. The total current is then determined by summing the sub band currents for all the sub band.

$$\frac{I_D^i}{W} = \left[\frac{q}{\hbar^2}\sqrt{\frac{m_{Ci}}{2}}\left(\frac{K_B T}{\pi}\right)^{3/2}\right]\{F_{1/2}\left[\frac{(E_F-\varepsilon_i)}{K_B T}\right] -F_{1/2}\left[\frac{(E_F-\varepsilon_i-qV_D)}{K_B T}\right]\} \tag{2.3}$$

Chapter 3

Equilibrium Electrostatics

The Top-of-the-barrier plays a significant role in the Over-the-barrier model. It has been assumed in this work that the Top-of-the-barrier is at the source end of the device thus assuming an abrupt increment of the CBM at the source. This assumption plays little role in determination of the ballistic current of the device as the ballistic current is not dependent on the channel length. But this assumption will result in an under estimation of the short channel effect. This study only focuses on the limiting ballistic currents of MOSFETs with different structures and materials. Thus this assumption will not incur any significant errors in this study. The equilibrium charge concentration at the source end might be determined from the equilibrium electrostatic solution of the device. This solution can be obtained by a self-consistent simulator. In this chapter the self-consistent simulator has been discussed. The boundary conditions for this simulator has to be adjusted according to the different device structures used for study here. The required adjustments are discussed in later chapter.

3.1 Algorithm of the self-consistent simulator

The the electrostatic solution of a MOSFET consists of a potential well and its corresponding charge distribution for a given gate voltage. Self-consistent modeling is a tool that finds the equilibrium electrostatic solution of a MOSFET by iterative methods. The MOSFET is described by two coupled differential equations: Poisson's Equation and Schrödinger's

equation. There are two different ways of acquiring the self-consistent solution depending on the starting point:

- Gate Voltage.
- Number of Inversion Carriers.

The process described here uses the gate voltage as a starting point. The following sections present the solution process for a bulk nMOS in inversion region. Only the inversion region is discussed here as this objective of this study includes the determination of the On current of MOSFETs.

A flow diagram given in figure 3.1 shows the basic steps of a self-consistent model. The model starts with a given gate voltage which is used to calculate the potential profile inside the semiconductor with the aid of an assumed charge density. This assumption might be obtained from the solution for a lower gate voltage or it might also be guessed as the ionized impurity concentration. For the later assumption the simulator will take higher number of iterations to converge. The potential profile obtained is then converted into an energy band diagram by using the physical parameters of the device. This energy band profile is used in the Schrödinger equation to obtain Eigen functions. These Eigen functions and corresponding Eigen energies are used to calculate the charge density. The charge density obtained is used in place of the assumed charge density of the first iteration to obtain a new potential profile and the process continues until two successive iterations produce results within the tolerance limit. The whole process in explained elaborately in the following sections with the aid of necessary figures. A typical bulk Si nMOS with 1nm thick SiO_2 gate and an uniform 10^{18} cm^{-3} impurity concentration is used for this discussion. The algorithm stays the same for different materials and structures.

3.1.1 Initialization

Initialization provides the data required for solving the Poisson's equation for the 1_{st} iteration. Poisson's equation requires two parameters: gate voltage and distribution of charge

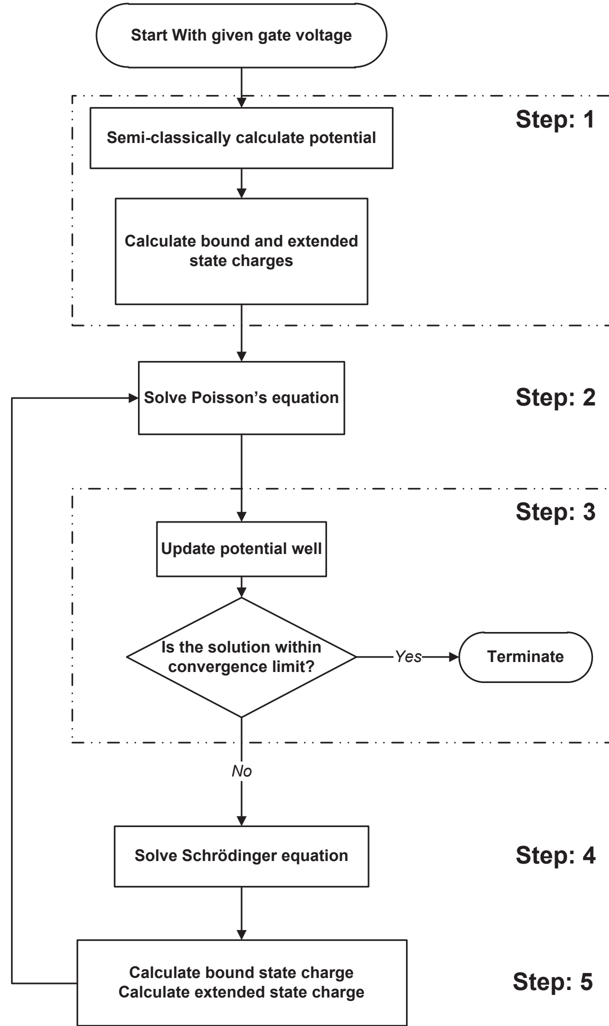

Figure 3.1: Flow diagram of self-consistent simulator

density with space. The process starts with a given gate voltage. The overall charge density can be divided into two parts: Depletion Charge and Inversion Charge. A zero inversion charge density is assumed for the 1_{st} iteration or the inversion charge determined by the self-consistent simulator for a closer gate voltage. Any initial condition should be alright theoretically. But an absurd initial condition might lead to slow convergence or even cause failure to converge. So it is advised to use the inversion charge profile obtained for a lower gate voltage as an initial condition. The gate voltage and the inversion charge density profile are used to solve the Poisson solver.

3.1.2 Solving Poisson's Equation

To solve Poisson's equation distribution of the total charge density is required which consists of both inversion charge and depletion charge. The mathematical process is discussed in Section 3.2. The depletion charge changes with the gate voltage for lower gate voltages. When the device reaches deep inversion the depletion charge distribution becomes constant. To obtain the appropriate depletion charge for a given inversion charge, a depletion width is assumed and total charge density is calculated as follows

$$\begin{aligned} \rho_{dep}(z) &= -e(N_A - N_D); \qquad & 0 < z < z_d \\ &= 0; & z > z_d \end{aligned} \tag{3.1}$$

where z_d is the depletion layer thickness.

$$\rho_{total}(z) = \rho_{dep}(z) + \rho_{inv}(z) \tag{3.2}$$

Using the total distribution of charge density the Poisson's equation is solved to obtain a potential profile. The objective is to find the maximum depletion width for which the potential does not go below the bulk potential for an nMOS for a given inversion charge density. That is the potential should not have any local maxima or minima inside the semiconductor. Depletion width is varied until an acceptable solution is obtained. Different potential profiles for different Z_D is shown in Fig. 3.2. Through iterative method the appropriate Z_D is determined which gives the solution of the Poisson's equation.

From the solution of the Poisson equation we obtain a depletion width and a potential profile. Depletion charge can be calculated by multiplying the depletion width with impurity concentration and electrons charge. Figure 3.3 shows the potential profile and the corresponding depletion width obtained from the solution of the Poisson equation for a gate voltage of 1 volt. The potential profile is used to determine the energy band profile for the device. The energy band profile is calculated by multiplying the potential profile with the charge of electron and then offsetting the oxide and semiconductor part of the profile by the

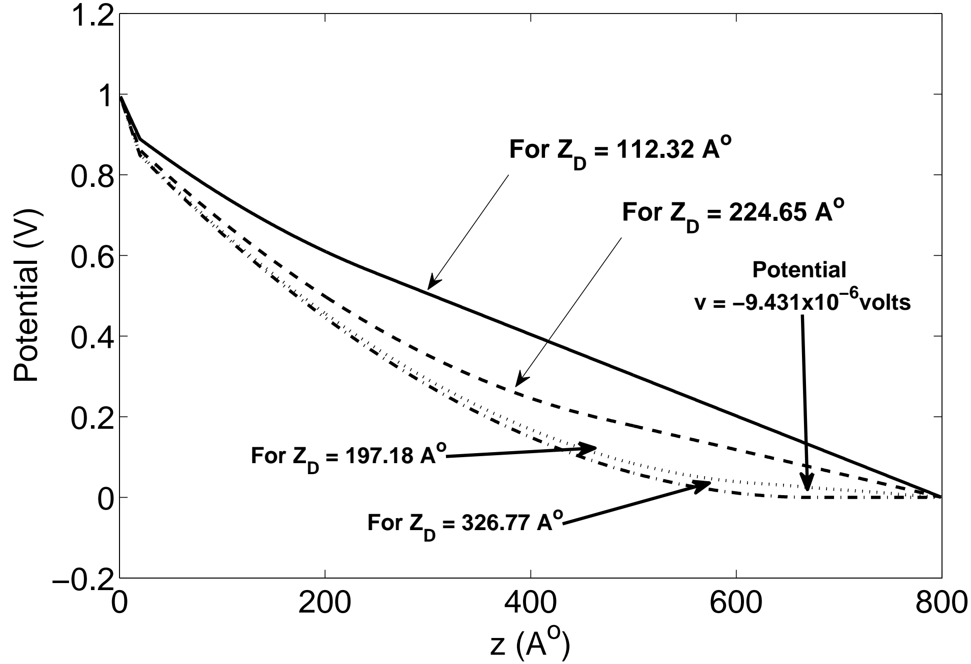

Figure 3.2: Potential profile obtained from Poisson solver for different Z_D for $V_{GS} = 1$ V.

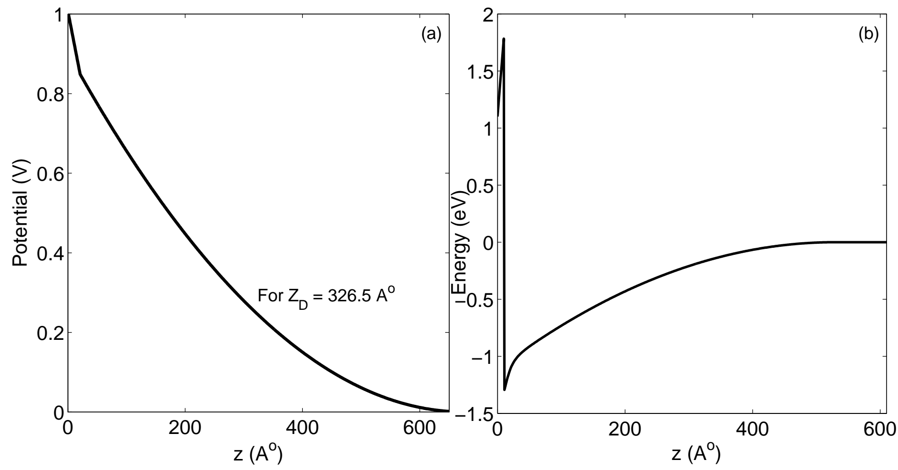

Figure 3.3: (a)Solution of the Poisson equation for $V_{GS} = 1$ V. (b) Calculated energy band profile from the potential profile.

appropriate differences in their work functions (Fig. 3.3). This energy band profile is used in the Schrödinger's equation solver.

The solution obtained from the Poisson solver might require some post processing under some specific circumstances. It is evident that if inversion charge is underestimated then depletion width is overestimated and vice versa. So, if the self-consistent loop is initialized with a low assumption for inversion charge the first iteration will result in a high overestimation of depletion width. A higher depletion width means a broader potential well. The resulting inversion charge density becomes highly overestimated due to the broad potential well. For the second iteration, the inversion charge is heavily overestimated. Hence even a zero depletion width provides a unacceptable solution. The situation is portrayed in figure 3.4.

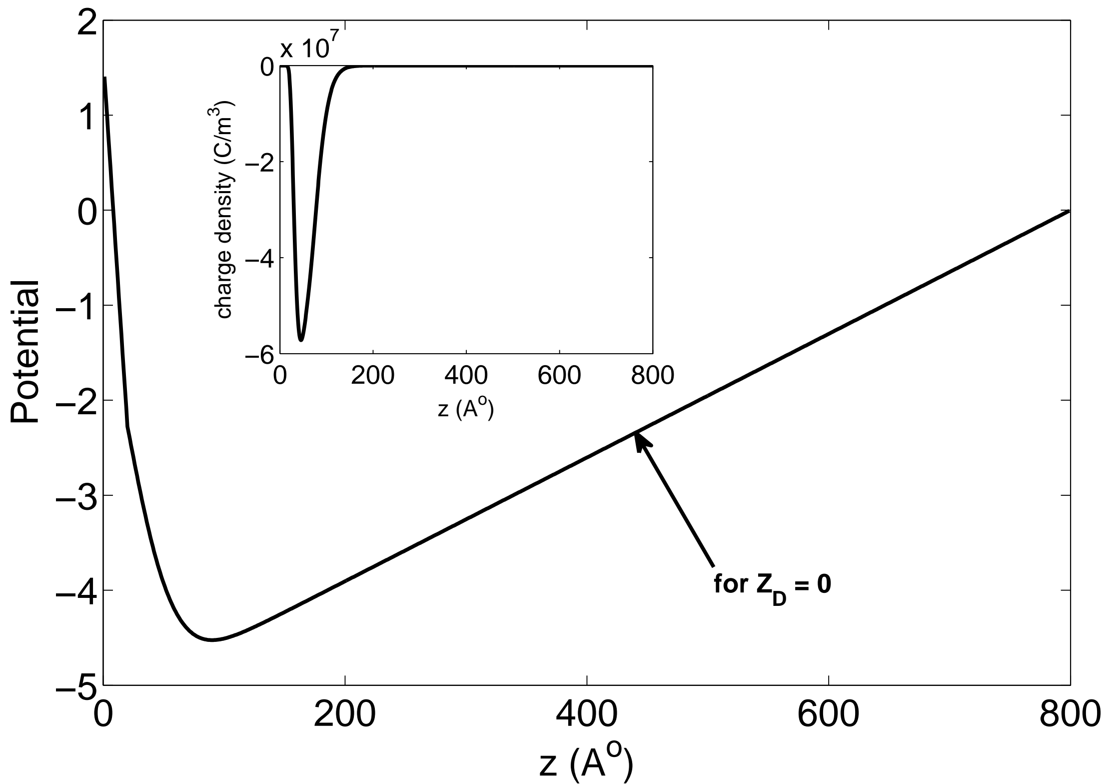

Figure 3.4: Solution obtained from Poisson solver for heavily overestimated inversion charge density.

The potential profile obtained here is not physically possible. This situation is very common if an iteration is initialized with zero inversion charge density for a gate voltage

high enough to push the device into deep inversion. For such situations the negative values of the potential profile are replaced by zeros.

3.1.3 Solving Schrödinger's Equation

The Schrödinger equation is solved following the precess discussed in Section 3.3. The solution of the Schrödinger equation provides us with some Eigen energies and corresponding normalized wave function ($|\Psi|_n^2$) or Eigen functions. These Eigen energies and Eigen functions are used to calculate the inversion charge density. There is a small probability of obtaining an erroneous solution from the Schrödinger solver. The matrix based solver that is used in this study has an accuracy that is dependent upon the step size of the mesh. As the frequency of the wave function becomes higher the accuracy of the solver goes down. That is the solver can calculate lower Eigen energies and their corresponding Eigen functions accurately but the higher Eigen energies will require a finer mesh which compromises computational efficiency. At energies very near to the bulk energy level an Eigen energy might reside which is difficult to obtain accurately while keeping acceptable computational efficiency. The normalized wave function obtained for these Eigen energies does not decay down to a zero value in the bulk due to the error introduced by the computational inaccuracy. Such a wave function is shown in figure 3.5.

The impact of this error is negligible while calculating for an inverting gate voltage as the contribution of the first few Eigen energies heavily dominate the proceedings and the higher Eigen energy being further away from the Fermi level contributes little to the inversion charge. But this erroneous wave function can have a profound impact in the accumulation region. These erroneous states are neglected completely.

3.1.4 Charge Calculation

The inversion charge density is calculated using the Eigen energies and their corresponding normalized wave functions with the aid of the following formulas.

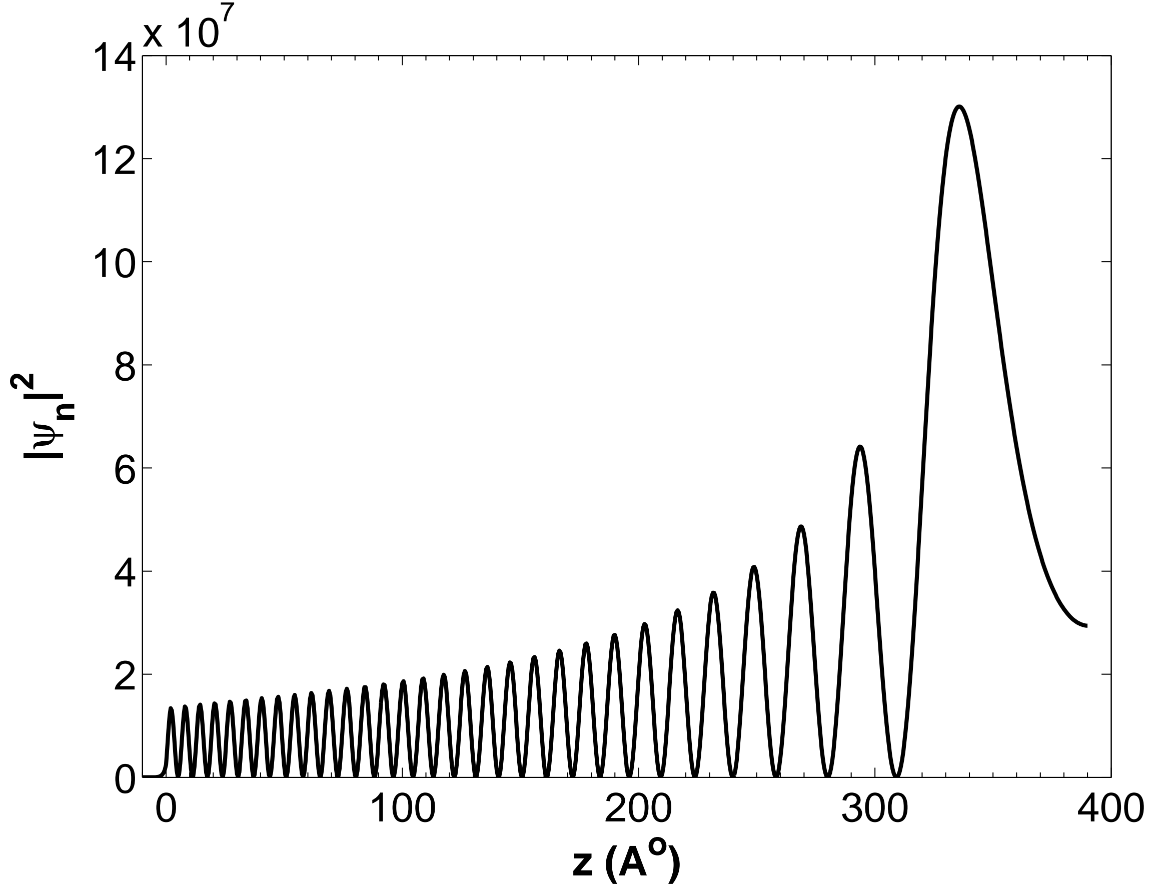

Figure 3.5: Erroneous $|\psi_n|^2$ obtained from Schrödinger equation solver for Eigen energy of $-0.0043eV$

$$N_{ij} \;=\; \frac{n_{vi} m_{di} kT}{\pi \hbar^2} \ln\left[1 + exp\left(\frac{E_F - E_{ij}}{kT}\right)\right] \tag{3.3}$$

Here N_{ij} denotes carrier concentration in the jth subband in the ith valley, n_{vi} is the valley degeneracy, m_{di} is the density of states effective mass of the ith valley, E_F is the fermi energy level and E_{ij} is the Eigen energy.

$$\rho_{inv}(z) \;=\; -e \sum_{ij} N_{ij} |\psi_{ij}(z)|^2 \tag{3.4}$$

here ρ_{inv} is the inversion charge density.

3.1.5 Updating and error check

At higher gate biases when deep inversion is achieved, the inversion charge calculated from the Eigen energies and the Eigen functions become very sensitive to small changes in the potential profile. As a result the self-consistent simulator becomes divergent if the potential profile is changed significantly after each iterations. This gives rise to the necessity of containing the change in the potential profile to ensure small change in every iteration. To contain the change in inversion charge the potential profile is controlled by updating the previous potential profile rather using the newly obtained potential profile. The update equation is given below where u denotes potential.

$$u_{new} = u_{old} + update\ coeff \times (Poisson\ solution - u_{old}) \tag{3.5}$$

The value of the update coefficient might vary from 0.06 to 0.03 depending on the impurity concentration.

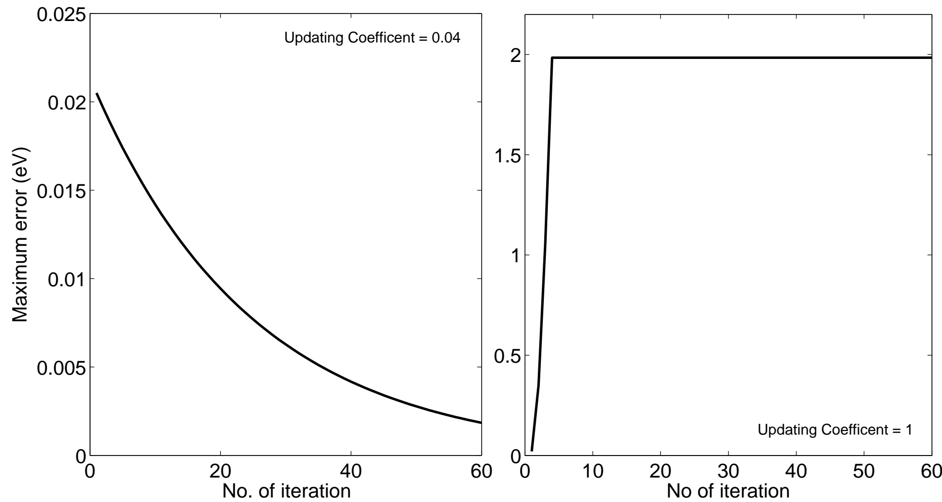

Figure 3.6: Maximum error for different iterations for different updating coefficients

Figure 3.6 shows maximum difference between two consecutive energy band profile in electron volts where gate voltage is 2 volts for two self-consistent solutions one adapting an update coefficient and another without any updating. It is obvious that use of appropriate

update coefficient is essential for successful and fast convergence. The newly obtained inversion charge profile is compared with the previous one. If the difference lies within the tolerance limit then the self-consistent solution is obtained and the loop is terminated.

3.2 Poisson's Equation Solver

In this section we discuss discuss the use of finite difference method to solve Poisson equation. In this method the derivatives in the partial differential equation are approximated by combinations linear equations by using the discrete differentiation methods. There are several discrete differentiation processes.

Three discrete differentiation forms are commonly considered for approximation of first order derivatives.

Forward difference

$$\left(\frac{\partial u}{\partial x}\right)_i \approx \frac{u_{i+1} - u_i}{\Delta x} \tag{3.6}$$

Backward difference

$$\left(\frac{\partial u}{\partial x}\right)_i \approx \frac{u_i - u_{i-1}}{\Delta x} \tag{3.7}$$

Central difference

$$\left(\frac{\partial u}{\partial x}\right)_i \approx \frac{u_{i+1} - u_{i-1}}{2\Delta x} \tag{3.8}$$

A second order derivative can be approximated with the aid of first order derivatives. Using the discrete approximations discussed before a second order derivative may be approximated by the following equation.

$$\left(\frac{\partial^2 u}{\partial x^2}\right)_i \approx \frac{u_{i+1} - 2u_i + u_{i-1}}{(\Delta x)^2} \tag{3.9}$$

Generalized Poisson's equation can be written as

$$\frac{\partial^2 V(z)}{\partial z^2} = f \tag{3.10}$$

$$where, f = -\rho_{inv}(z)/\epsilon_0\epsilon_{ox}, \qquad -t_{ox} < z < 0 \tag{3.11}$$

$$= -(\rho_{inv}(z) + \rho_{dep}(z))/\epsilon_0\epsilon_{si}, \qquad z > 0 \tag{3.12}$$

Now, the value of the voltage at the metal end of the gate is the applied voltage V_GS. This is used as a boundary condition for solving the Poisson equation. The other boundary is taken at the other physical end of the device. This boundary is deep in the semiconductor body for a bulk MOSFET or the second gate metal for a double gate MOSFET. Here, we are using a bulk MOSFET. Thus the potential will be zero deep inside the bulk.

$$V_1 = V_GS \tag{3.13}$$

and

$$V_{end} = 0 \tag{3.14}$$

Open boundary condition at material interfaces are necessary to relate their Electric fields. For a bulk MOSFET with the oxide field F_{ox} and semiconductor field should be related as shown in the equation below. This relationship is held at every material boundaries.

$$\epsilon_{ox}F_{ox} = \epsilon_{semiconductor}F_s \tag{3.15}$$

So, using the discrete differentiation technique the Poisson equation can be approximated as the set of following linear equations.

$$
\begin{aligned}
&i = 1 && V_1 && = V_g \\
&i = 2 && \frac{V_1 - 2V_2 + V_3}{(\Delta z)^2} && = f_2 \\
&i = 3 && \frac{V_2 - 2V_3 + V_4}{(\Delta z)^2} && = f_3 \\
&\cdots \quad \cdots && \cdots && \cdots \\
&At\ SiO_2/Si\ interface && -\epsilon_{ox} V_{i-1} + (\epsilon_{ox} + \epsilon_{si}) V_i - \epsilon_{si} V_{i+1} && = 0 \\
&\cdots \quad \cdots && \cdots && \cdots \\
&i = N-1 && \frac{V_{N-2} - 2V_{N-1} + V_N}{(\Delta z)^2} && = f_{N-1} \\
&i = N && V_N && = 0
\end{aligned}
$$

Solving this set of linear equations we can obtain the solution of the poisson's equation for the MOSFET.

3.3 Schrödinger's Equation Solver

The Schrödinger equation can be solved utilizing two different methods which are

- Retarded Green's function formalism using transmission line analogy.
- Hamiltonian matrix formalism

A detailed comparison of these two methods has been presented in [33]. The model used in this study uses the Hamiltonian Matrix formalism. This method has been chosen because of the faster execution of matrix based algorithm while maintaining the required level of accuracy with the use of larger matrices. The Hamiltonian Matrix formation is discussed at length here for a bulk MOSFET.

The Hamiltonian matrix is the energy matrix for any system. The energy band levels around the conduction band minimum can be described by [34]

$$h(\vec{k}) = E_c + \frac{\hbar^2 k^2}{2m^*} \tag{3.16}$$

where E_c is the conduction band minimum energy and m^* is the effective mass. A differential equation can be formed that that will yield energy eigenvalues replacing $\vec{k}$ with $-i\vec{\nabla}$ in the Eq. 3.16.

$$\left[E_c - \frac{\hbar^2}{2m^*}\nabla^2\right]\psi(\vec{r}) = E\psi(\vec{r}) \tag{3.17}$$

For one dimension Eq. 3.17 can be written as

$$\left[E_c - \frac{\hbar^2}{2m^*}\frac{d^2}{dx^2}\right]\psi(x) = E\psi(x) \tag{3.18}$$

Finite difference method is used to convert Eq. 3.18 into a Hamiltonian matrix. This conversion is done by choosing a discrete lattice. We can represent the wave function $\psi(x)$ by a column vector("T" denotes transpose)

...

$$\{\psi(x_1)\ \psi(x_2)\ \ldots\ \psi(x_{i-1})\ \psi(x_i)\ \psi(x_{i+1})\ \ldots\ \ldots\}^T$$

Then the matrix representing the hamiltonian operator(H_{op}) is obtained.

$$H_{op} \equiv E_c - \frac{\hbar^2}{2m^*}\frac{d^2}{dx^2}$$

Using finite difference method it can be written

$$\left(\frac{d^2}{dx^2}\psi\right)_{x=x_i} = 2\frac{(x_i - x_{i-1})\psi_{i+1} - (x_{i+1} - x_{i-1})\psi_i + (x_{i+1} - x_i)\psi_{i-1}}{(x_{i+1} - x_{i-1})(x_{i+1} - x_i)(x_i - x_{i-1})}$$

For uniform mesh size of $\triangle x = a$ which reduces to

$$\left(\frac{d^2}{dx^2}\psi\right)_{x=x_i} = \frac{\psi_{i+1} - 2\psi_i + \psi_{i-1}}{a^2} \tag{3.19}$$

and

$$(E_c\psi)_{x=x_i} \rightarrow E_c(x_i)\psi_i \tag{3.20}$$

If we assume

$$t_o = \frac{\hbar}{2m^* a^2}$$

then

$$[H_{op}\psi]_{x=x_i} = -t_o\psi_{i-1} + (E_c(x_i) + 2t_o)\psi_i - t_o\psi_{i+1} \tag{3.21}$$

and the matrix,

$$[H_{op}] = \begin{bmatrix} E_c(x_1)+2t_o & -t_o & 0 & 0 & 0 & 0 \\ -t_o & E_c(x_2)+2t_o & -t_o & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & -t_o & E_c(x_{n-1})+2t_o & -t_o \\ 0 & 0 & 0 & 0 & -t_o & E_c(x_n)+2t_o \end{bmatrix} \tag{3.22}$$

For spatially varying effective mass the correct/modified version of Eq. 3.18, 3.21 and 3.22 are Eq. 3.23,3.24 and 3.25 respectively.

$$\left[E_c - \frac{\hbar^2}{2}\frac{d}{dx}\left(\frac{1}{m^*(x)}\frac{d}{dx}\right)\right]\psi(x) = E\psi(x) \tag{3.23}$$

$$[H_{op}\psi]_{x=x_i} = -t_{i-1}\psi_{i-1} + (E_c(x_i) + t_{i-1} + t_i)\psi_i - t_i\psi_{i+1} \tag{3.24}$$

where

$$t_i = \frac{\hbar^2}{2m_i^*}$$

$$[H_{op}] = \begin{bmatrix} E_c(x_1)+2t_1 & -t_1 & 0 & 0 & 0 & 0 \\ -t_1 & E_c(x_2)+t_1+t_2 & -t_2 & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & -t_{n-2} & E_c(x_{n-1})+t_{n-1}+t_{n-2} & -t_{n-1} \\ 0 & 0 & 0 & 0 & -t_{n-1} & E_c(x_n)+2t_{n-1} \end{bmatrix} \tag{3.25}$$

To solve the Schrödinger's equation the following steps should be followed to calculate Eigen energies and normalized wave function.

1. The potential well was approximated with multi step function.
2. The hamiltonian matrix is formed using Eq. 3.22 or 3.25
3. Eigenvalues and eigenvectors are determined of that matrix.
4. Eigen energies are calculated from eigenvalues.
5. Eigenvector are normalized to determine normalized wave function.

Chapter 4

Material Parameters

The devices under study here have III-V compound semiconductor materials. The material parameters vary with composition of the material. The parameters also vary under the effect of strain. In this chapter we discuss the variation of material parameters with composition and strain.

4.1 Variation With Material Composition

The variation of different material parameters such as electron effective, hole effective mass, band gap etc. with material composition have to be calculated appropriately. All the material parameters associated with this studies is discussed in this section. The exact calculation of a variation of a material parameter with its composition is impossible due to the large uncertainty. Thus the value of the required parameter in calculated using interpolation technique. Thus the parameter for the new material is determined from the corresponding known values of the parameter for the end semiconductors. For this study the ternary material $In_xGa_{1-x}As$ has been used. The required material parameters of $In_xGa_{1-x}As$ can be calculated from the known values of InAs and GaAs. If $A_xB_{1-x}C$ is the ternary material of interest and the material parameters of binary material AC and BC are known then we can calculate the value for $A_xB_{1-x}C$ using Equation 4.1.

$$T_{ABC(x)} = xB_{AC} + (1-x)B_{BC} - x(1-x)W_{ABC} \tag{4.1}$$

Here, T is the parameter for the ternary material while B is the same parameter for binary materials. W is the bowing parameters. The value of W changes for different material parameters. All the parameters of interest have been calculated using Equation 4.1.

If the bowing parameter W becomes zero then this interpolation becomes linear. According to Vegrad's Law the bowing parameter for calculating lattice constant is zero. Thus calculation of lattice constant is necessarily a linear interpolation between the lattice constants of InAs and GaAs. The lattice constants of InAs and GaAs are given in Table 4.1. Several parameters can be calculated using the linear interpolation that is assuming their bowing parameters as zero. These parameters are density of states effective masses, quantization effective masses and transport effective masses for both electrons and holes, elastic stiffness constants C11 and C12, deformation potential b, a_v and a_c, relative permittivity, Luttinger parameter. All these parameters for the material $In_xGa_{1-x}As$ system have been listed in in Table 4.1.

One of the device parameters that depends on a bowing parameter is band gap. Also, parameters related to spin orbit splitting and electron affinity also depend on a bowing parameters. These values of these parameters along with their bowing parameters are also mentioned in Table 4.1 and 4.2.

To describe the physics of the device with different compound semiconducting material the band alignment of the layers of semiconductors have to be calculated according to the material composition and the resulting strain from mismatch between two different semiconductor materials if any. Fig. 4.1 shows a typical heterogenous band structure.

Here the effects of material composition on band alignment is discussed. The effects of strain is discussed in the next section. There are two band offsets associated with band alignment: the conduction band offset and the valance band offset. Both these offset changes with the material composition. The model-solid theory is employed here to estimate the band edge offsets of cubic semiconductors [31]. The model lines up the band structure of different semiconductors by introducing an average valence band energy $E^0_{v,av}$. $E^0_{v,av}$ can be expressed with Equation 4.2 for unstrained semiconductors.

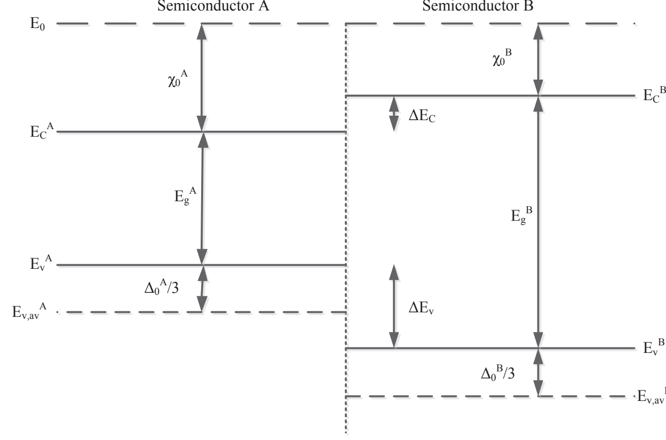

Figure 4.1: Band diagram for a typical heterostructures.

$$E^0_{v,av} = E^0_v - \frac{\Delta_0}{3} \tag{4.2}$$

Here E^0_v denotes valence band edge and Δ_0 denotes spin orbit splitting. Values for $E^0_{v,av}$ are given in Table 4.1. These values are obtained by calculating the average electrostatic potential for model-solids of neutral atoms and are taken from [32]. The conduction band edge can be calculated from these data as shown in Equation 4.3.

$$E^0_c = E^0_v + E_g = E^0_{v,av} + \frac{\Delta_0}{3} + E_g \tag{4.3}$$

Here, E^0_c denotes conduction band edge and E_g denotes the band gap of the material. For interpolating $E^0_{v,av}$ for a ternary material $A_xB_{1-x}C$ it has to be taken into account that the lattice parameter a_{ABC} is different form the binary lattice constants a_{AC} and a_{BC}. The bowing parameter for $E^0_{v,av}$ can be calculated from the binary deformation potential a_v and binary lattice parameters using Equation 4.4

$$C_{ABC}(E^0_{v,av}) = 3[a_v(AC) - a_v(BC)]\frac{a_{AC} - a_{BC}}{a_{ABC}} \tag{4.4}$$

The binary deformation potential a_v is also dependent on the composition but as mentioned before the bowing parameter for it is zero. Under strain, the average energy $E_{v,av}$ is shifted from its unstrained value $E^0_{v,av}$ as shown in Equation 4.5

$$E_{v,av} = E^0_{v,av} - P_\epsilon = E^0_v - \frac{\Delta_0}{3} - P_\epsilon \tag{4.5}$$

Here, P_ϵ is an energy associated with strain which is required to include strain in the two band Hamiltonian matrix. More on P_ϵ has been discussed in the following section.

By comparison with fully self-consistent interface calculations, the error bar on band offsets determined from the model-solid theory extends up to 0.1 eV [36]. Many other theoretical and experimental investigations of heterostructure band offsets have been published, leading to a list of typical values for the valence band edge E^0_v in unstrained bulk material (4.1). The absolute energy scale is arbitrary, here the InSb valence band edge is used as origin. Known bowing parameters are listed in Table 4.2. The implementation of the effects of strain are discussed in the next section.

An alternate way to determine the band offset is to take vacuum level as the reference and using the electron affinity (χ_0) as shown in Equation 4.6.

$$E^0_c = E_0 - \chi_0 \tag{4.6}$$

Bowing parameters for the affinity can be calculated by weighting the band gap bowing parameter $C(E_g)$ with the average conduction band offset ratio $\Delta E_c/\Delta E_g$ of the binary endpoint materials for the same symmetry point (Equation 4.7).

$$C(\chi_0) = -C(E_g)\frac{\Delta E_c}{\Delta E_g} \tag{4.7}$$

This study uses the valence band edge method for band edge alignment.

4.2 Effects of Strain

The fabrication of materials with different lattice parameters on each other results in a strained layer at the top of the device. The strain changes material parameters like electron affinity, transport effective mass etc. The variation of parameters with strain is discussed here. Strain deforms the crystal lattice. However, it is assumed to be still periodic such that Bloch functions are still applicable. Since the elementary crystal cell is deformed, potential and Bloch lattice functions now have a period equal to the strained elementary cell. The relative change of the lattice period gives the strain.

$$\epsilon_{ij} = \frac{\Delta a_i}{a_j} \tag{4.8}$$

This strain can be different in different directions. With small strain, the strained Hamiltonian can be given as perturbation of the unstrained Hamiltonian [37]. Only bi-axial strain is considered in this work. For mismatched super lattice grown along the z-axis the strain components can be calculated as

$$\begin{aligned} \epsilon_{xx} &= \epsilon_{yy} \neq \epsilon zz \\ \epsilon_{ij} &= 0 for i \neq j \end{aligned} \tag{4.9}$$

The two strain components are related by the elastic stiffness coefficient C_{11} and C_{12} as sown in equation below:

$$\begin{aligned} \epsilon_{zz} &= -2\frac{C_{12}}{C_{11}}\epsilon_{xx} \\ \epsilon_{xx} = \epsilon_{yy} &= \frac{a_{st} - a_0}{a_0} \end{aligned} \tag{4.10}$$

where a_{st} and a_0 are the lattice constant of the strained and unstrained crystal, respectively. For compressive strain, $a_{st} < a_0$, $\epsilon_{xx} = \epsilon_{yy} < 0$, and $\epsilon_{zz} > 0$.

Additions of P_ϵ and Q_ϵ are required to the diagonal elements of the two-band Hamiltonian matrix to incorporate the effects of crystal deformations on the Bloch functions. P_ϵ and Q_ϵ is given below.

$$P_\epsilon = -a_v(\epsilon_{xx} + \epsilon_{yy} + \epsilon_{zz})$$
$$Q_\epsilon = -\frac{b}{2}(\epsilon_{xx} + \epsilon_{yy} - 2\epsilon_{zz}) \tag{4.11}$$

As a result of this modification, the strain is found to cause the following shifts of the band edges at the Λ point. According to the two band model which assumes that the interaction with the spin orbit can be neglected the band edge shifts can be expressed as:

$$E_{hh}(0) = E_{hh}^0 = E_v^0 - P_\epsilon - Q_\epsilon$$
$$E_{lh}(0) = E_{lh}^0 = E_v^0 - P_\epsilon + Q_\epsilon \tag{4.12}$$

The conduction band edge is given by

$$E_c(0) = E_c^0 = E_v^0 + E_g + a_c(\epsilon_{xx} + \epsilon_{yy} + \epsilon_{zz}) \tag{4.13}$$

The factors a_c and a_v are hydrostatic deformation potentials; b is the shear deformation potential. The separation of the total hydrostatic deformation potential in conduction (a_c) and valence band (a_v) contributions is important at heterointerfaces.

Due to the deformation of crystal structures under strain, the E-k relationship changes. Thus the effective mass changes with strain. To calculate the change is effective mass the two band model can be used which assumes that there are no coupling with the spin orbit band or the three band model which includes the spin orbit but neglects the effects of the coupling with conduction band. According to the two band model the bands along the z-axis remains parabolic thus the effective mass stays the same along the z direction. But the x-y E-k relationship deforms from the parabolic band thus resulting in a k dependent effective mass. Near the Λ point which is the point of interest in simulation studies the transverse effective masses can be expressed as:

$$m_{hh}^t = \frac{m_0}{\gamma_1 + \gamma_2}$$

$$m_{lh}^{t} = \frac{m_0}{\gamma_1 - \gamma_2} \tag{4.14}$$

Here, γ_1 and γ_2 are Luttinger parameters for cubic solids. The two band model is discussed here. A more detailed discussion along with the three band model can be found in [32]. All the related data for determination of change in material parameters due the composition and strain is given in Table 4.1 and 4.2.

Table 4.1: Required material parameters for $In_xGa_{1-x}As$ material system.

Parameter	**InAs**	**GaAs**
E_g	0.36 eV	1.42 eV
m_c^{Γ}	$0.023m_0$	$0.063m_0$
m_c^X(t/l)	$0.16/1.13m_0$	$0.23/1.3m_0$
m_c^L(t/l)	$0.05/0.64m_0$	$0.075/1.9m_0$
m_{hh}	$0.57m_0$	$0.50m_0$
m_{lh}	$0.025m_0$	$0.076m_0$
m_{so}	$0.14m_0$	$0.14m_0$
γ_1	20.0	6.98
γ_2	8.5	2.06
γ_3	9.2	2.93
a_0	6.0583	5.65325
C_{11}	832.9	1221
C_{12}	452.6	566
b	-1.8	-2.0
a_v	1.0	1.16
a_c	-5.08	-7.17
E_v^0	-0.59	-0.8
Δ_0	0.39	0.341
$E_{v,av}^0$	-6.67	-6.92
χ_0	4.90	4.07

Table 4.2: Bowing parameters for $In_xGa_{1-x}As$ material system.

Bowing Parameter	**(In,Ga)As**
$C(E_g^{\Lambda})$	-0.127+1.31x
$C(E_g^{X})$	0.055
$C(E_g^{L})$	0
$C(E_v^{0})$	
$C(\Delta_0)$	0

Chapter 5

Results and Discussions

III-V semiconductors have shown promise to become the material of choice for future high performance devices. As discussed before number of different structures with different III-V semiconductors have come under consideration. In this study bulk MOSFETs, Surface Channel MOSFETs, Double Gate MOSFETs and SOI MOSFETs have been taken for theoretical evaluation of their limiting performance. The devices fabricated to this day suffer from different processing issues such as oxide-semiconductor interface traps. Thus the experimentally reported drain currents does not provide a clear picture of the limiting performance of each devices and their variation with material compositions. $In_xGa_{1-x}As$ was taken as the material of choice for this study. The obtained results are presented here. Also the device parameters are presented in Table 5.1

Table 5.1: Parameters for the devices used for simulation in this study.

Device Type	**EOT (nm)**	**Doping Concentration cm^{-3}**	**Thickness nm**
Bulk	0.53	7.5×10^{18}	
Surface Channel	0.53	7.5×10^{18}	5-20
Double Gate	0.77	1×10^{17}	5,8
SOI	0.6	1×10^{17}	5.5

5.1 Bulk MOSFETs

Bulk MOSFETs are typical Si MOSFET like structures only the semiconductor material is III-V.

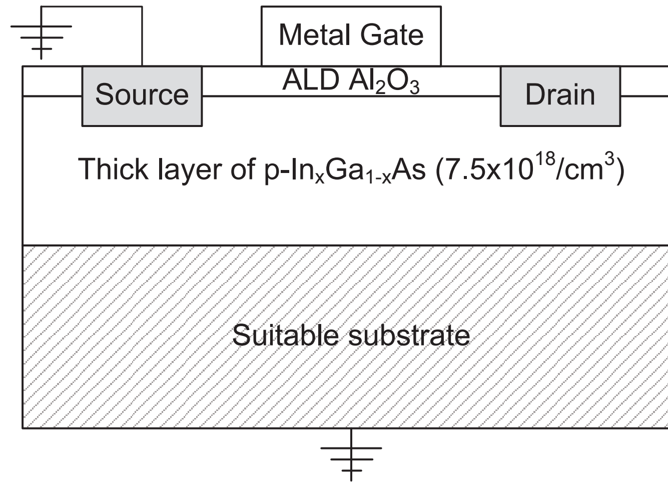

Figure 5.1: Schematic diagram of a bulk MOSFET used for the simulation.

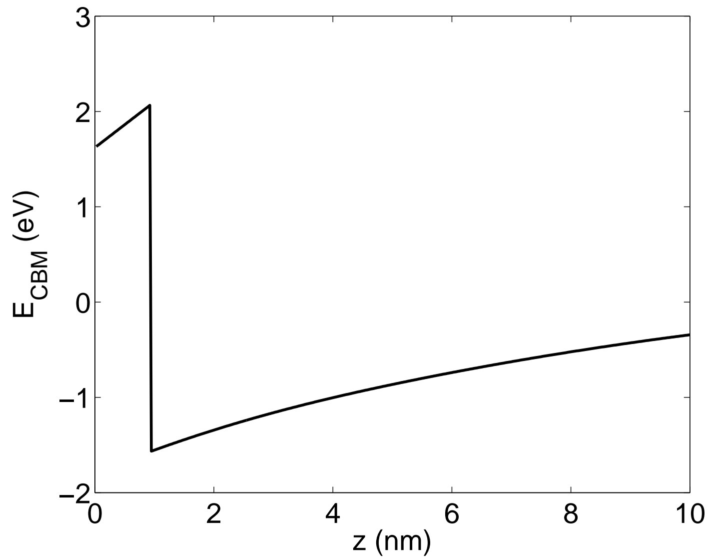

Figure 5.2: Energy band diagram portraying the conduction band minima (CBM) energy for InAs bulk MOSFET at V_{GS} = 2.0 V.

But III-V MOS fabrication rises some issues. InP is the material of choice as the substrate for the fabrication of $In_xGa_{1-x}As$ MOSFETs. Thus a buffer layer of $In_{0.53}Ga_{0.47}As$ has to be fabricated to reduce strain on the active layer. This buffer layer is not suitable for the end binary semiconductors that is GaAs and InAs. To provide a comparative picture for this study a hypothetical substrate is assumed which does not cause any strain on the active material. Also the active layer is taken to be thick such that the substrate does not play any role on the device performance. This is shown in the schematic diagram of a bulk III-V MOSFET in Fig. 5.1. The EOT of the oxide is 0.53 nm and the doping concentration is $7.5 \times 10^{18} cm^{-3}$ according to [1]. The device parameters are also summarized in Table 5.1. The energy band diagram for an InAs bulk MOSFET under applied gate to source voltage V_{GS} = 2.0 V is shown in Fig. 5.2. Here, the oxide-semiconductor conduction band offset will change with material composition. The oxide offsets for GaAs, $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$, $In_{0.75}Ga_{0.25}As$ and InAs for Al_2O_3 are 2.80 eV, 3.34 eV, 3.42 eV, 3.5 eV and 4.23 eV respectively. The ballistic currents for devices with different material composition have been calculated using the methods discussed in Chapter 2. As a comparison between different materials is presented the comparison over the over drive voltage (V_{OV}) is more appropriate. Here V_{OV} = V_{GS} - V_{th}. The threshold voltage (V_{th}) is defined such that the drain current is 1 (μA/m). Fig. 5.3 shows the currents for five different materials for V_{OV} 0.5 V, 0.65 V and 0.8 V respectively.

These results may present themselves as counter intuitive as we know that InAs has much higher electron mobility compared to GaAs. Thus it is expected that the drain currents will increase as the In composition in the material increases. Similar conclusion can be reached if the transport effective masses are taken into account for ballistic transport. The effective masses are shown in Table 4.1. The effective mass decreases as In composition increases in the material thus increasing the injection velocity. But the ballistic currents also depend on the inversion charge density. The number of inversion carriers are shown in Fig. 5.4

As the density of states effective mass reduces from GaAs towards InAs the inversion charge density is expected to reduce. Fig. 5.4 shows the inversion charge density for five

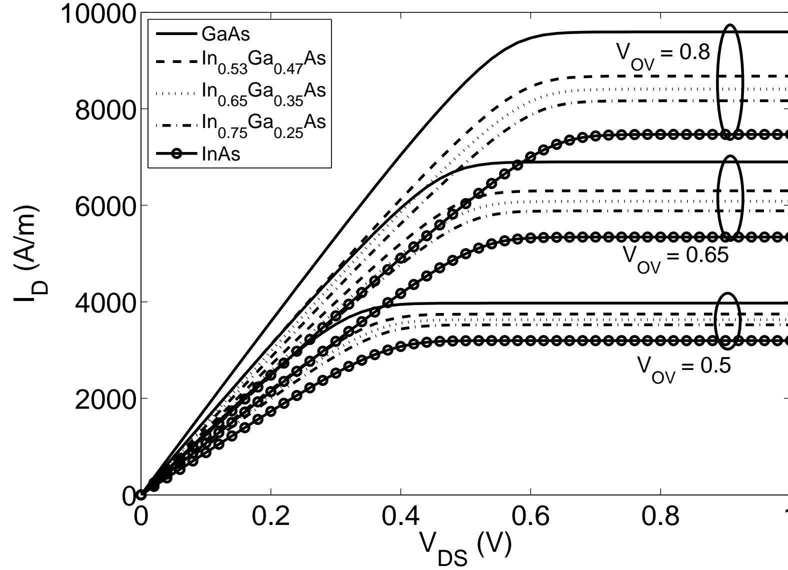

Figure 5.3: Simulated ballistic drain current for bulk MOSFETs at V_{OV} = 0.5, 0.65 and 0.8 V.

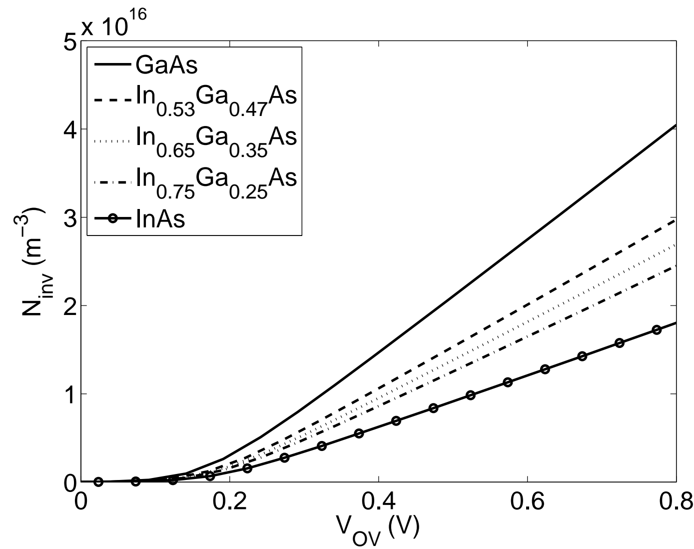

Figure 5.4: Number of inversion carriers N_{inv} for different bulk MOSFETs.

different materials. The figure shows a significant decrease in inversion charge density. Another factor in determining the ballistic current is the position of the Eigen energies ε_i. From Chapter 2 we observe that as ε_i goes closer to the source Fermi level the number of

+k carriers increase. Fig. 5.5 shows the position of first Eigen energies with respect to the equilibrium source Fermi level.

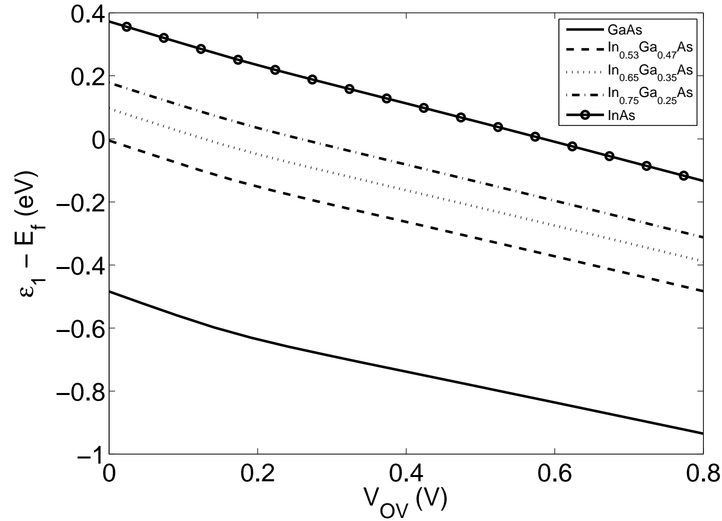

Figure 5.5: Position of first Eigen state ε_1 with respect to the equilibrium source Fermi level for different bulk MOSFETs.

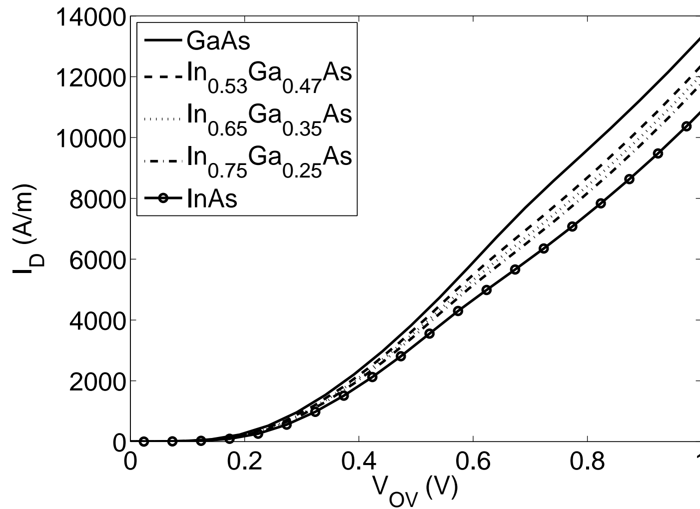

Figure 5.6: Simulated ballistic on current for bulk MOSFETs at V_{DS} = 1.5 V.

As GaAs has higher quantization effective mass the Eigen energy is lower than that of InAs. Also the potential well formed in the GaAs device will be narrower as the Eigen

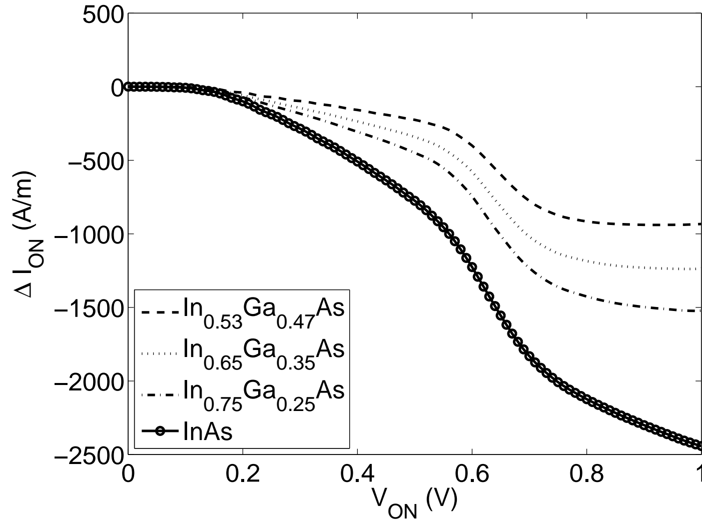

Figure 5.7: Change in simulated ballistic on current for bulk MOSFETs with respect to GaAs bulk MOSFET at V_{DS} = 1.5 V.

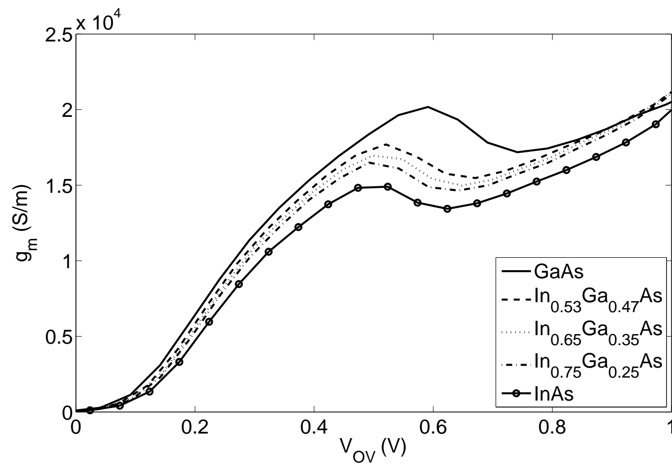

Figure 5.8: Simulated transconductance for bulk MOSFETs at V_{DS} = 1.5 V.

energy is low. Due to the low Eigen energy the number of +k state carriers are higher for GaAs. This argument is also applicable to the -k states. As the Eigen energies are lower the energy state will be closer to the drain Fermi level thus resulting in a comparatively higher number of -k state carriers. But the drain Fermi level resides much lower than the Eigen states and slight variation of the Eigen states does not change the number of -k state carriers significantly as the drain Fermi is further away. But due to the close proximity of the source

Fermi a slight variation in the position of the Eigen states results in significant change in the number of +k state carriers and thus is the drain current. Fig. 5.6 shows the On current I_{ON} for different bulk MOSFETs at different V_{OV}. Also, the change in I_{ON} is depicted in Fig. 5.27 which shows the change is I_{ON} with respect to GaAs bulk MOSFET. A negative value denotes that current is decreasing from GaAs to InAs.

Table 5.2: Change in inversion charge (V_{OV} = 0.5 V), transport effective mass and drain current (V_{OV} = 0.5 V, V_{DS} = 1.5 V) for bulk MOSFETs.

Parameter	**GaAs**	**$In_{0.53}Ga_{0.47}As$**	**$In_{0.65}Ga_{0.35}As$**	**$In_{0.75}Ga_{0.25}As$**	**InAs**
m_t (m_0)	0.067	0.0453	0.0403	0.0362	0.0260
% change		-32.39%	-39.85%	-45.97%	-61.19%
N_{inv} ($\times 10^16$ m^{-3})	2.1052	1.5331	1.3817	1.2523	0.91433
% change		-27.18%	-34.37%	-40.51%	-56.57%
I_D (A/m)	3972	3745	3631	3523	3196
% change		-5.72%	-8.59%	-11.3%	-19.5%

Table 5.2 shows the increase in drain current and decreases in transport effective mass and inversion charge density. The transconductance g_m of the devices can be calculated from Fig. 5.6. The calculated g_m for these devices are shown in Fig. 5.8. It is evident that there are very little difference in the transconductance of these devices.

5.2 Surface Channel MOSFETs

Xuan et el. first reported enhanced performance for long channel MOSFETs whose surface layers have increased In component [20].

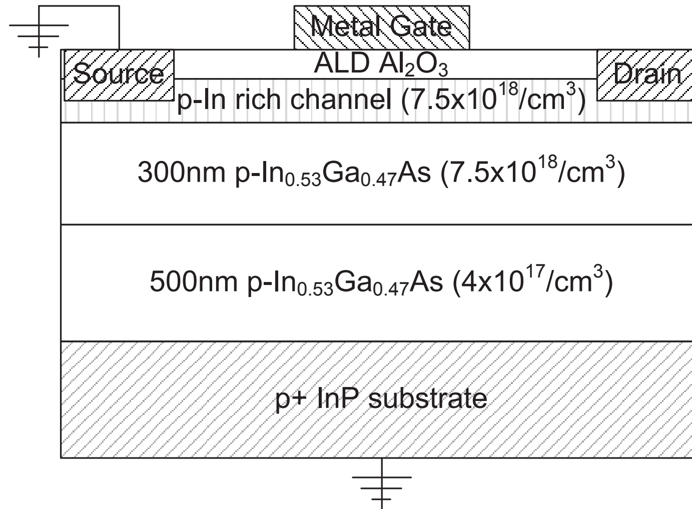

Figure 5.9: Schematic diagram of a surface channel MOSFET used for the simulation.

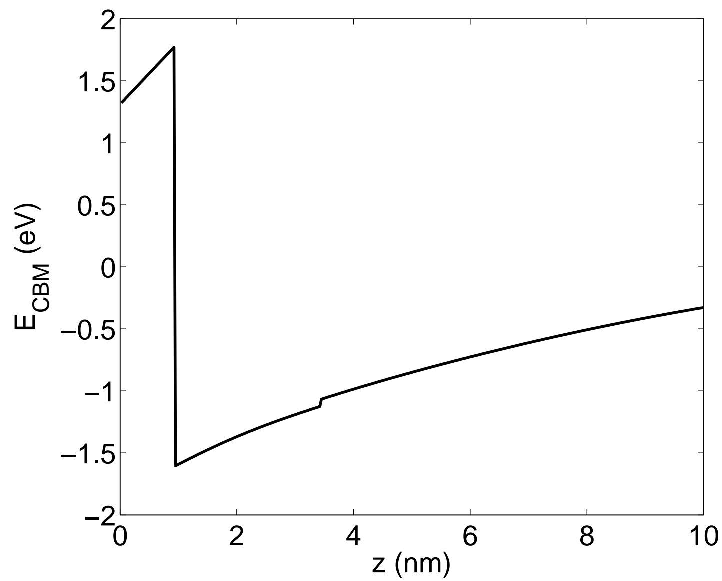

Figure 5.10: Energy band diagram portraying the conduction band minima (CBM) energy for $In_{0.65}Ga_{0.35}As$ surface channel MOSFET at $V_{GS} = 2.0$ V.

The schematic diagram for such a surface channel MOSFET is shown in Fig. 5.9. The energy band diagram is shown in Fig. 5.10 for a 65% In rich surface channel MOSFET with a 2.5 nm thick surface layer for $V_{GS} = 2.0$ V. The device parameters are not yet specified for surface channel MOSFETs in ITRS, so the device parameters for bulk MOSFETs are taken for the simulation of surface channel MOSFETs. The surface layer thickness is also not specified. The fabricated long channel devices have a surface layer thickness of 20 nm. But for the doping concentration of 7.5×10^{18} cm^{-3} as specified in [1] the thickness of 20 nm makes the surface layer so thick that the under lying layer has no other effects on the performance of the MOSFET other than strain. To investigate the effects of the thickness of the surface layer, drain currents are calculated for four different surface layer thickness: 2.5 nm, 5 nm and 10 nm. The oxide offsets of $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$ for Al_2O_3 are 3.34 eV, 3.38 eV and 3.42 eV respectively. Also the conduction band offset between $In_{0.53}Ga_{0.47}As$ and $In_{0.65}Ga_{0.35}As$ is -0.055 eV. For $In_{0.53}Ga_{0.47}As$ and $In_{0.75}Ga_{0.25}As$ interface the conduction band offset is -0.104 eV.

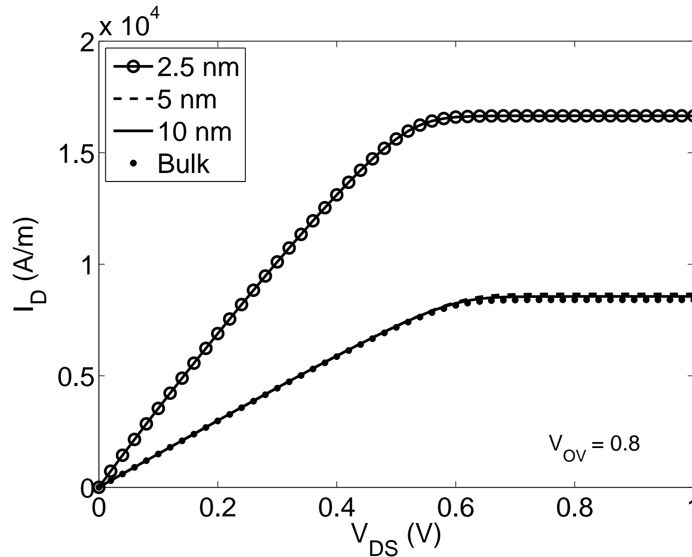

Figure 5.11: Ballistic drain current for $In_{0.65}Ga_{0.35}As$ surface channel MOSFETs for $V_{OV} =$ 0.8 V for different surface layer thickness.

Fig. 5.11 show the ballistic currents for a surface channel MOSFET with $In_{0.65}Ga_{0.35}As$ as the surface layer and different surface layer thickness. We observe that for thick surface layer

the drain current is independent of the surface layer thickness. But the current increases as the surface layer becomes 2.5 nm thick. This phenomenon can be explained by the narrower quantum well for the 2.5 nm device and also the with the aid of the change in effective mass due to narrow thickness of the surface layer [38] (Fig. 5.12). Also we can take the aid of number of inversion carriers and the position of the first Eigen state to explain this increment in the current for narrow surface layer.

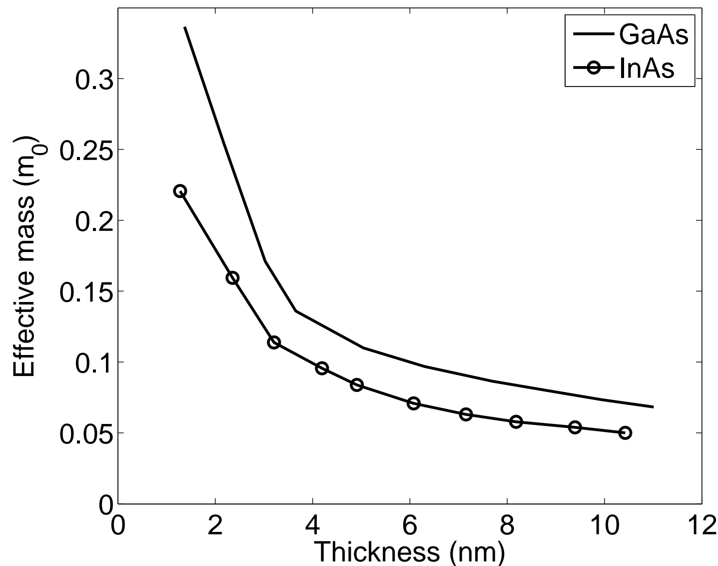

Figure 5.12: Change in value of effective mass with the thickness of semiconductor layer [38].

From Fig. 5.13 and 5.14 we can observe that there is very little difference in inversion charge concentration or the first Eigen energy for higher channel thickness. But as the channel grows thinned the conduction band offset is pushed inside the inversion charge layer and the surface layer thickness starts to play a more important role. Also the increment in quantization effective mass contributes in the increase of drain current. But from the figures we see that thin surface layer results in an elevated inversion charge concentration. On the other hand the position of the first Eigen energy goes slightly lower as surface layer thickness is reduced .This lower Eigen energy can be explained by the fact that as channel layer is made thinner the carriers of the lowest energy states becomes trapped inside a thinner potential

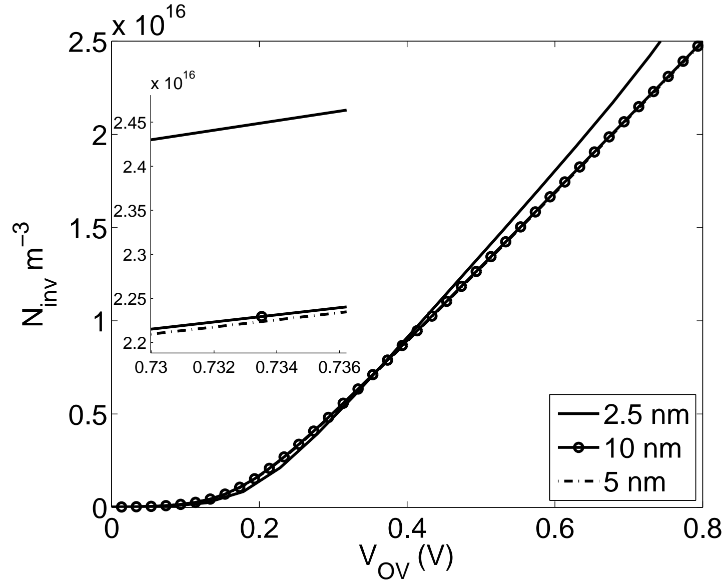

Figure 5.13: Number of inversion carriers N_{inv} for $In_{0.65}Ga_{0.35}As$ surface channel MOSFETs of different channel thickness. Inset shows a magnified vision.

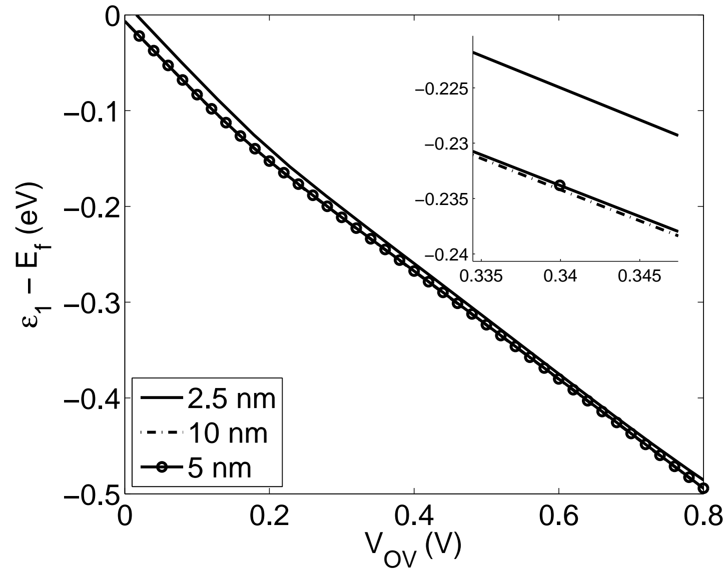

Figure 5.14: Position of first Eigen state ε_1 with respect to the equilibrium source Fermi level for $In_{0.65}Ga_{0.35}As$ surface channel MOSFETs of different channel thickness. Inset shows a magnified vision.

well. We know that majority charge in the inversion is contributed by the first two Eigen energies. As the well becomes narrower the wave function of the first Eigen state becomes

trapped inside a ever narrower well resulting in early truncation of the first Eigen function. As the result the Eigen energy becomes slightly lower to maintain the required equilibrium charge concentration. But for the 2.5 nm device we observe that the Eigen energy lies above the other devices. This is due to the change is effective mass from the narrow surface layer. This change of effective mass occurs below 5 nm thickness. We observe that the thinner device portrays a better current capability.

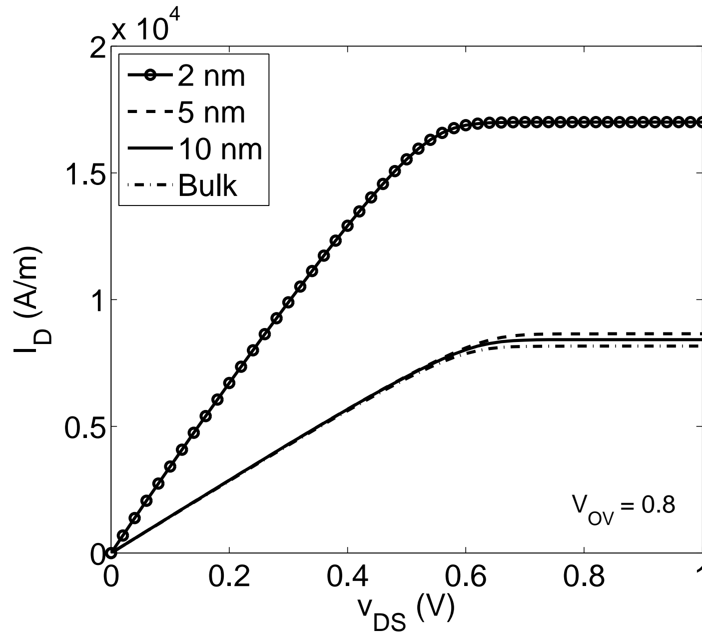

Figure 5.15: Ballistic drain current for $In_{0.75}Ga_{0.25}As$ surface channel MOSFETs for V_{OV} = 0.5 V for different surface layer thickness.

Using similar reasoning an increase in drain current is also expected in the $In_{0.75}Ga_{0.25}As$ devices. Fig. 5.15 shows the drain currents of devices with $In_{0.75}Ga_{0.25}As$ as the surface layer. We observe the increase in current for the 5 nm thick surface layer.

It is also evident from Fig. 5.11, 5.15 that the performance of the surface channel devices are better than the bulk devices with the same material as the surface layer. This increase in performance can be attributed to effects of strain. Strain plays two roles in the performance of devices. Due to strain both the transport and density of states effective masses becomes lower. Due to the decrease in transport effective mass the injection velocity increases. On

the other hand the decrease in density of state effective mass decreases the inversion carrier density. Which has a detrimental effect on the drain current. But an positive effect over all is observed due to strain. The significant improvement in current in 2.5 nm devices can be explained by the changed effective mass.

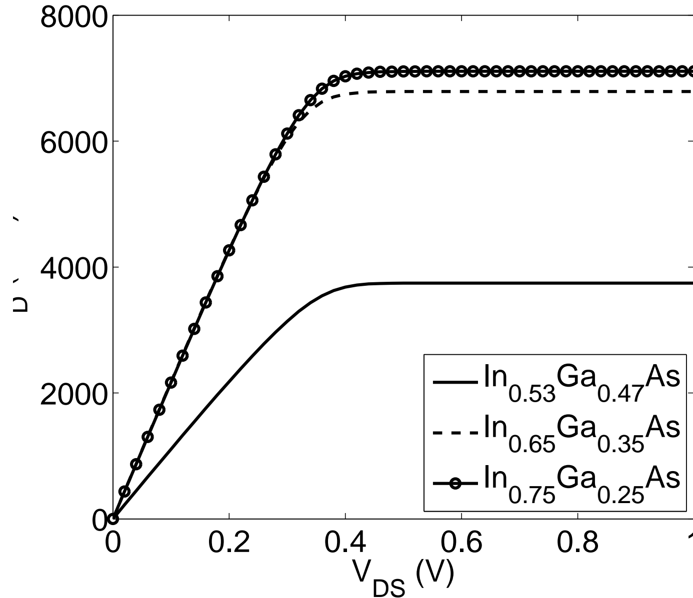

Figure 5.16: Ballistic drain current for different surface channel MOSFETs for $V_{OV} = 0.5$ V and surface layer thickness of 2.5 nm.

These surface channel devices have the same material for the layer under the top surface layer which is $In_{0.53}Ga_{0.47}As$. Thus we also compare the performance with bulk $In_{0.53}Ga_{0.47}As$. Fig. 5.17 and 5.16 shows the drain currents of the surface channel MOSFETs for 2.5 nm, 5 nm and 10 thick surface layers accordingly along with the current of bulk $In_{0.53}Ga_{0.47}As$ MOSFET for 0.5 V over drive voltage.

We observe that though surface channel MOSFETs show performance increase compared to the bulk devices with the same material as the surface layer but their performance does not improve compared to the bulk $In_{0.53}Ga_{0.47}As$ device for 10 nm and 5 nm thickness. The reasons of a better performance of bulk $In_{0.53}Ga_{0.47}As$ has already been discussed in the previous section. We also observe that the surface channel MOSFET with thin surface layer shows

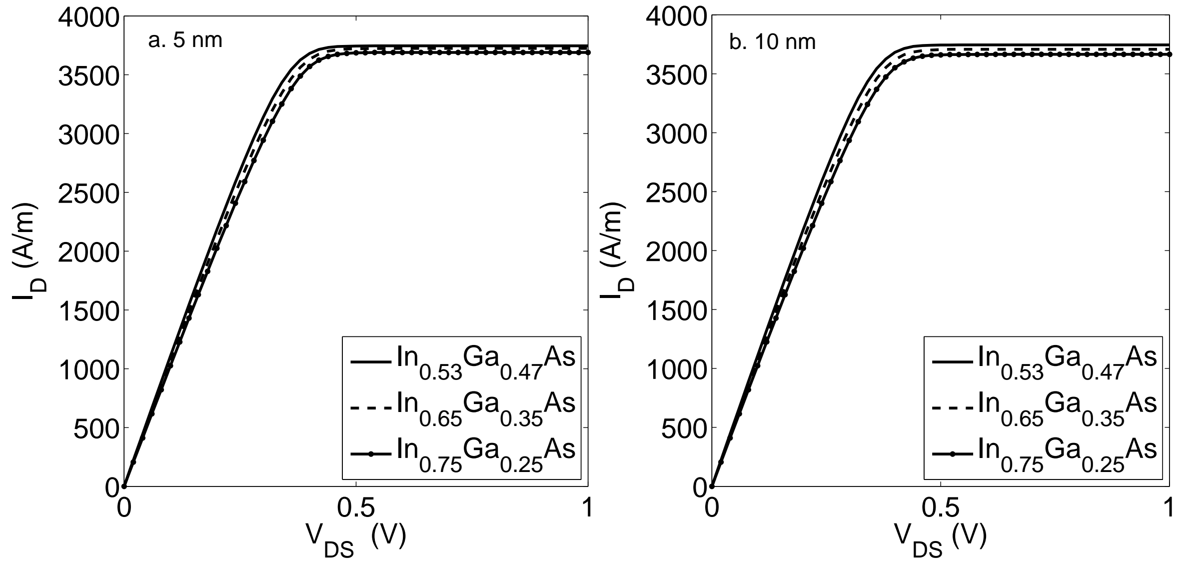

Figure 5.17: Ballistic drain current for different surface channel MOSFETs for $V_{OV} = 0.5$ V and surface layer thickness a. 5 nm and b. 10 nm

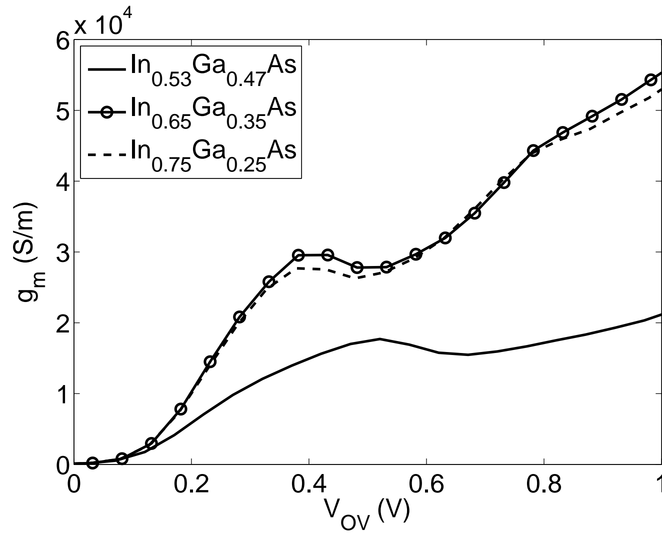

Figure 5.18: Transconductance for different surface channel MOSFETs for surface layer thickness of 2.5 nm.

better performance compared the bulk $In_{0.53}Ga_{0.47}As$ device. Also the transconductance for these devices are shown in Fig. 5.19 and 5.18.

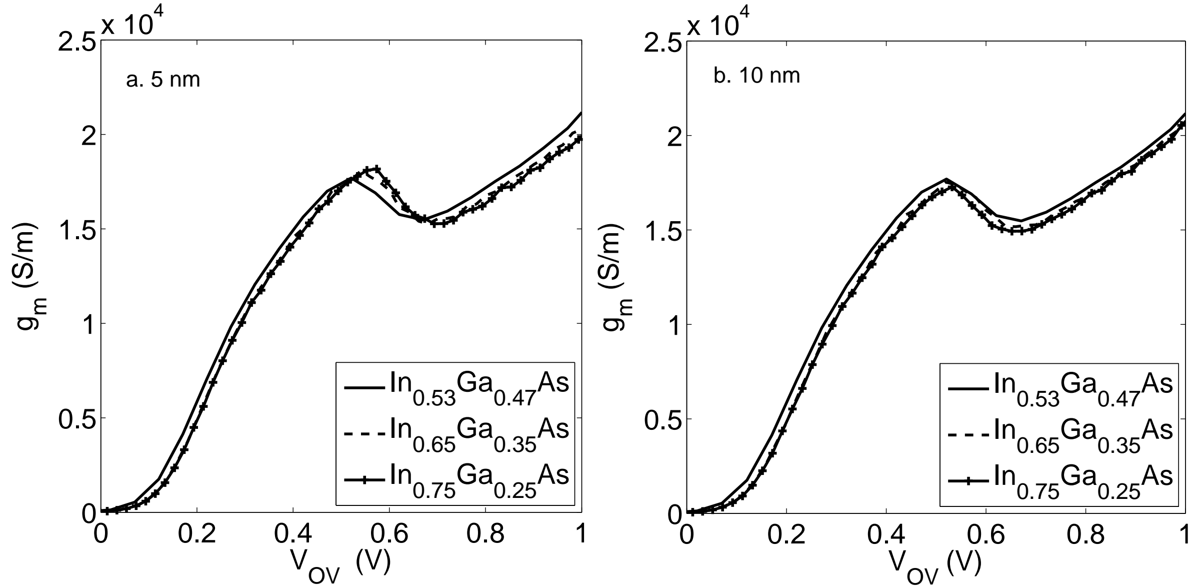

Figure 5.19: Transconductance for different surface channel MOSFETs for surface layer thickness a. 5 nm and b. 10 nm.

From the figures we observe that like the bulk MOSFETs, transconductance does not show any significant change in the surface channel MOSFETs. The on current of all the surface channel devices under study have been summarized in Table 5.3

Table 5.3: On current (I_{ON}) for V_{OV} = 0.5 V for for different surface channel MOSFETs.

Surface Layer Composition	**Layer Thickness nm**	**I_{ON} A/m**
$In_{0.65}Ga_{0.35}As$	2.5	6787
	5	3724
	10	3708
$In_{0.75}Ga_{0.25}As$	2.5	7109
	5	3689
	10	3665

5.3 Double Gate MOSFETs

Double Gate (DG) MOSFETs have shown promise as nano-scale device with Si as the channel material. In this section the performance of III-V material based DG MOSGETs are investigated using the similar technique used for bulk and surface channel MOSFETs. The schematic diagram of a DG MOSFET is shown in Fig. 5.20. We have taken the five materials that were used for the bulk MOSFET for the double gate MOSFET. This should give a comparative picture that would qualitatively predict the performance of III-V DG MOSFETs also shed some light on the underlying physics.

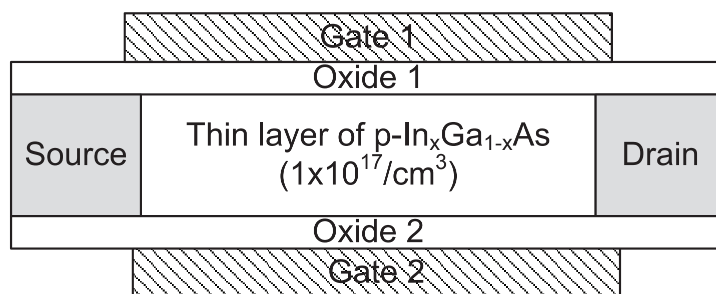

Figure 5.20: Schematic diagram of a Double Gate MOSFET used for the simulation.

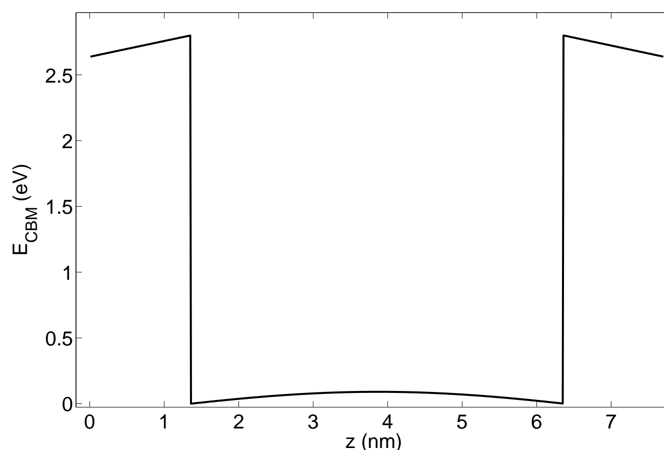

Figure 5.21: Energy band diagram portraying the conduction band minima (CBM) energy for GaAs double gate MOSFET at $V_{GS} = 2.0$ V at both gates.

The DG MOSFETs used for simulation in the work have an EOT of 0.77 nm. The channel layer thickness is taken to 5 nm and 8 nm. The oxide offsets for GaAs, $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$, $In_{0.75}Ga_{0.25}As$ and InAs for Al_2O_3 are 2.80 eV, 3.34 eV, 3.42 eV, 3.5 eV and 4.23 eV respectively for both gate dielectrics. We have taken a balanced DG MOSFET that is same voltage is applied in both gates. Also the EOT of both gate dielectrics are equal.

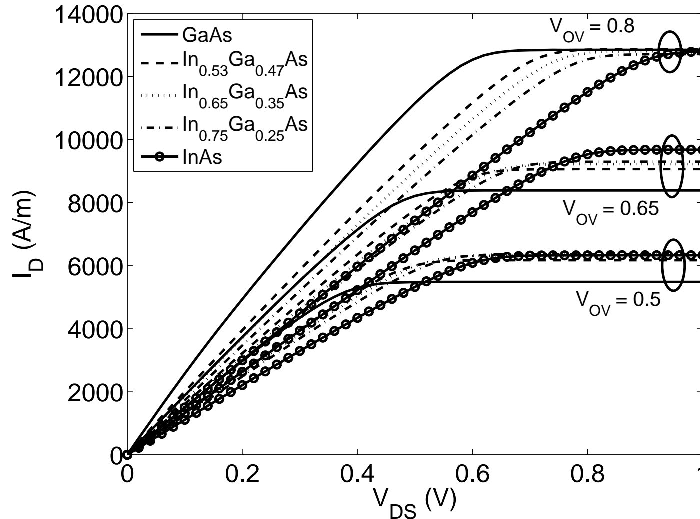

Figure 5.22: Simulated ballistic drain current for different Double Gate MOSFETs with 5 nm thin channel layer for $V_{OV} = 0.5$, 0.65 and 0.8 V simulation.

The calculated ballistic drain current is shown in Fig. 5.22 for a DG MOSFET with 5 nm thin channel layer. We observe a completely opposite performance compared to the bulk MOSFET and also the surface channel MOSFET. Both for bulk MOSFET and surface channel MOSFET the material with higher density of states effective mass prevailed. But for 5 nm DG MOSFET we obtain the best performance for InAS at low overdrive voltage. To further investigate the phenomenon we calculate the inversion charge and also look into the Eigen states of the system. The inversion carrier density is shown in Fig. 5.23 and the first Eigen energy is shown in Fig. 5.24

The inversion carrier concentration portrays expected behavior. As the density of states effective mass is higher for GaAs, it is expected that GaAs devices will show higher inversion charge density. But the Eigen states does not behave as seen for bulk MOSFET. In case of

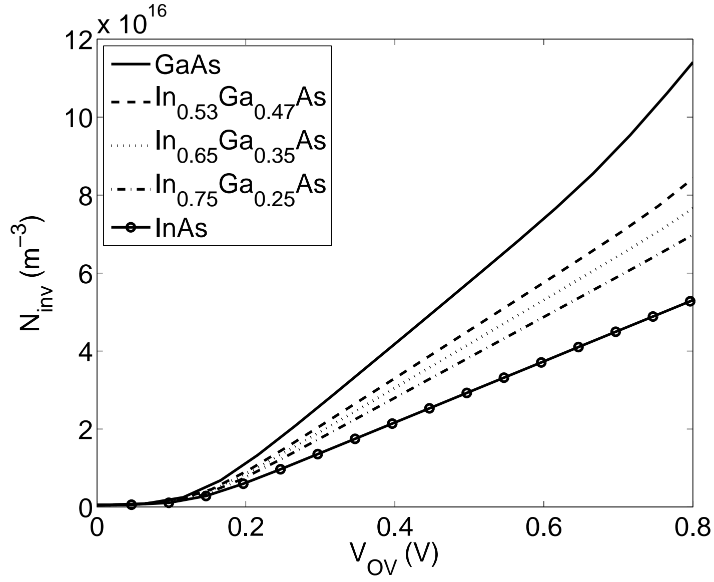

Figure 5.23: Number of inversion carriers N_{inv} for different DG MOSFETs.

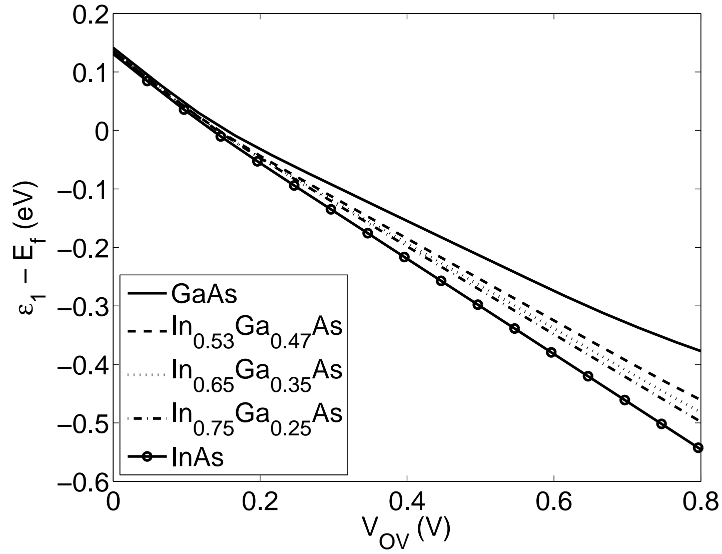

Figure 5.24: Position of first Eigen state ε_1 with respect to the equilibrium source Fermi level for different DG MOSFETs.

bulk MOSFET we have seen that the lower quantization effective mass results in a higher Eigen state for In rich materials. But in double gate structure we observe that the Eigen state for InAs lies below that of GaAs. It should be noted that, for surface channel MOSFETs we

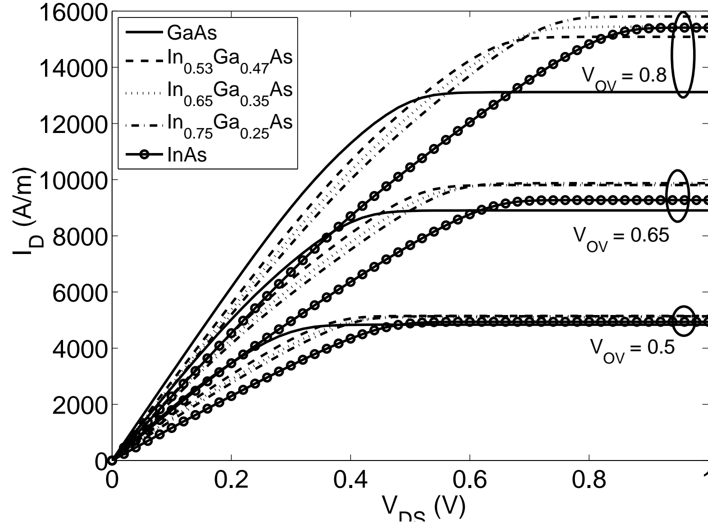

Figure 5.25: Simulated ballistic drain current for different Double Gate MOSFETs with 8 nm thin channel layer for $V_{OV} = 0.5$, 0.65 and 0.8 V simulation.

also observed this sort of behavior when the surface channel was shrunk to 5 nm. But the extent of this deviation was very low. This is because the quantum well in surface channel MOSFET has very small potential barrier created by the difference in the work functions of two semiconductors. But for DG MOSFET the potential well is formed by the difference in the work functions of the semiconductor and oxide which is very large. As a result all the inversion charge is localized within the narrow channel. As a result the Eigen energies of the materials with low density of states effective mass must go lower to accommodate enough charge to achieve inversion.

It is noteworthy, that the inversion charge of GaAs increases very steeply with V_{OV}. While the higher Eigen state of GaAs affects the drain negatively, the higher inversion charge plays a positive role and increases the drain current. Thus in DG MOSFET contradictory phenomenon are in act. This is visible in the drain currents of the devices. While other MOSFET structures show very consistent trend in increase or decrease of drain current such as for bulk MOSFET GaAs produce higher currents than InAs at all gate voltages, DG MOSFET does not show any distinct trend. For low bias InAs provides higher on current while at higher gate voltage GaAs and InAs gives equal drain current. Similar behavior is

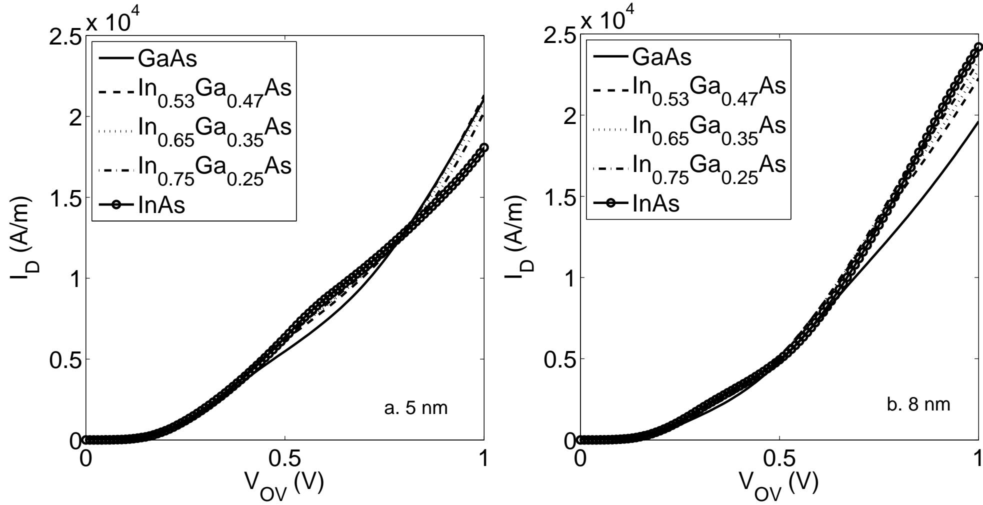

Figure 5.26: Simulated ballistic on current for DG MOSFETs at V_{DS} = 1.5 V for a. 5 nm and b. 8 nm thin channel.

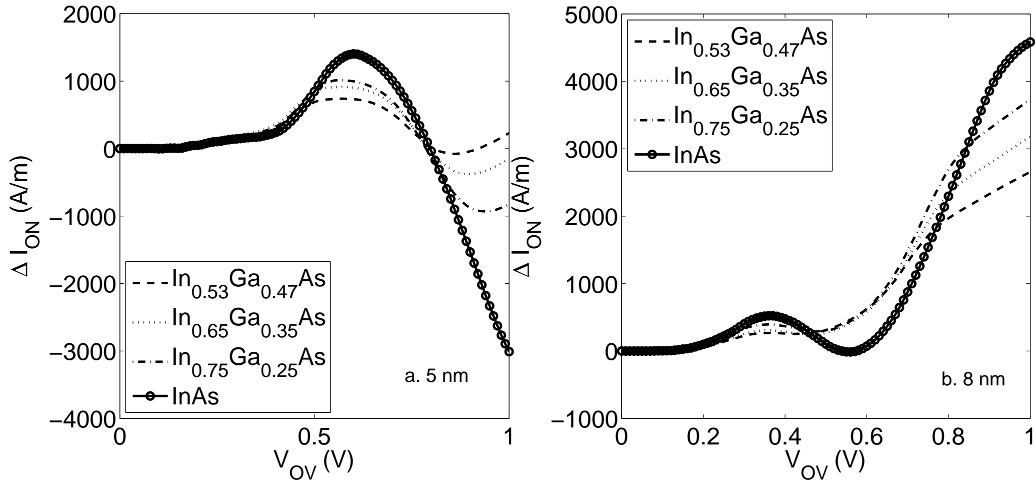

Figure 5.27: Change in simulated ballistic on current for DG MOSFETs with respect to GaAs DG MOSFET at V_{DS} = 1.5 V for a. 5 nm and b. 8 nm thin channel.

observed at the ITRS advised semiconductor thickness of 8 nm. This is shown in Fig. 5.25. For 8 nm thin channel GaAs provides lowest current for all bias conditions. But InAs still performs differently at different gate bias.

In Fig. 5.26 the on current for different over drive voltages is shown for both 5 nm and 8 nm thin channel DG MOSFETs. The shifting performance is very clear form this picture.

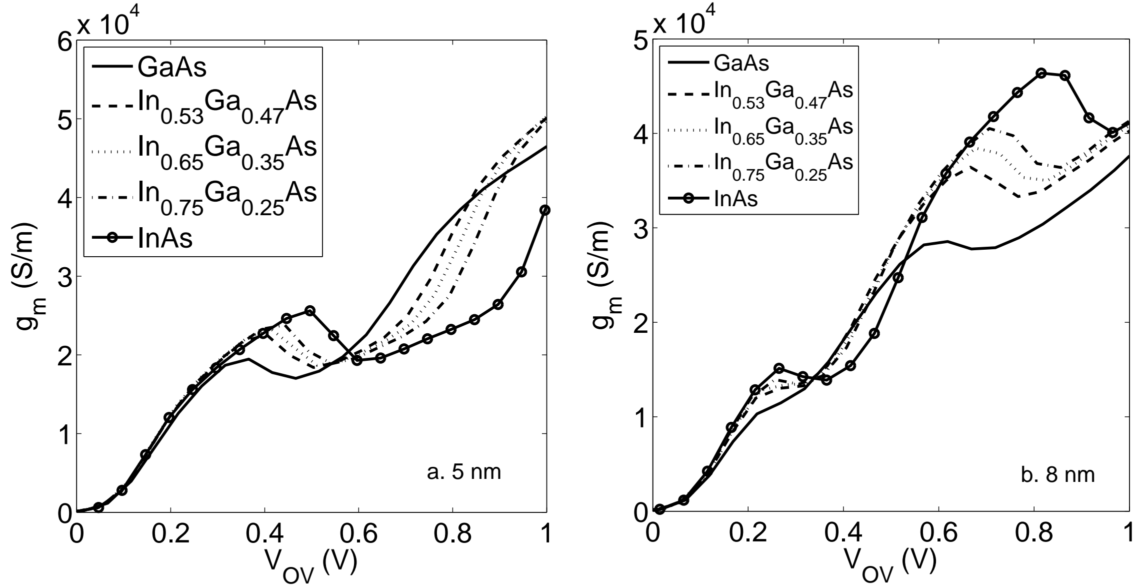

Figure 5.28: Transconductance for different DG MOSFETs for channel layer thickness a. 5 nm and b. 8 nm.

We also calculated the change in On current due to change in material for both DG MOSFET structures. This is shown in Fig. 5.27. Also the transconductance of these devices might be calculated from Fig. 5.26. The transconductance is shown is Fig. 5.28. Similar to the previous devices, no specific trend is observed in the change of transconductance. Also the change in transconductance is not as significant as the change in current.

5.4 SOI MOSFETs

SOI structures have been very successful in optoelectronic devices. They have also shown very high promise as logic devices with Si as the active material. The SOI structure is used as the base for different structures such as FinFETs and DG FETs. The structure we have considered is given in Fig. 5.29. Also the band diagram showing the conduction band minima for GaAs SOI MOSFET under V_{GS} = 2.0 V is shown in Fig. 5.30.

Here, we have assumed a 5.5 nm thin channel layer and 0.6 nm EOT for the gate dielectric as per [1]. The oxide offsets for GaAs, $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$, $In_{0.75}Ga_{0.25}As$ and InAs for Al_2O_3 are 2.80 eV, 3.34 eV, 3.42 eV, 3.5 eV and 4.23 eV respectively for both

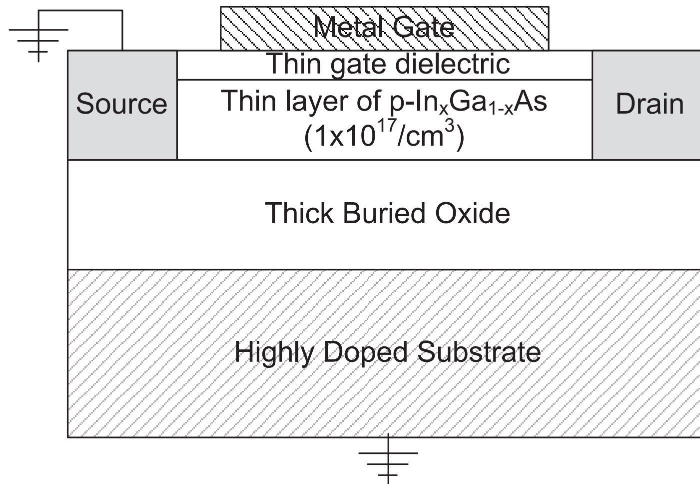

Figure 5.29: Schematic diagram of a SOI MOSFET used for the simulation.

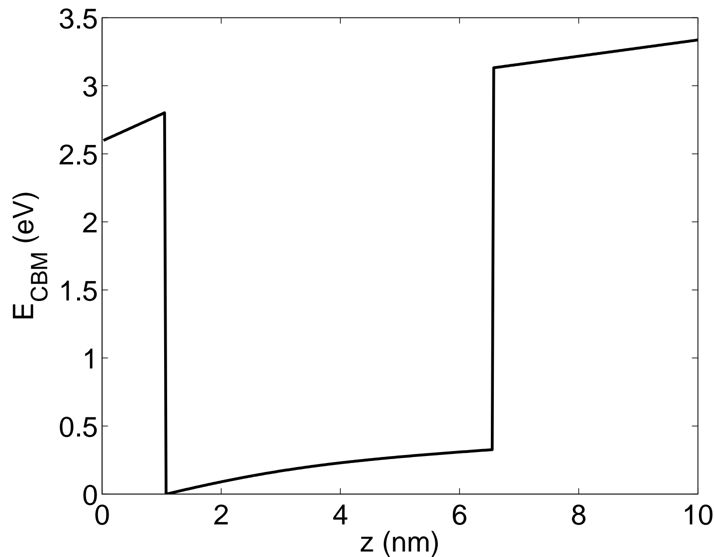

Figure 5.30: Energy band diagram portraying the conduction band minima (CBM) energy for GaAs SOI MOSFET at $V_{GS} = 2.0$ V.

semiconductor oxide interface. Also the substrate is assumed to be highly doped such that it behaves like poly under bias. This assumption neglects the voltage that will be dropped in the substrate if a lightly doped substrate is used. As a result the performance under a certain gate voltage will be overestimated. But it this study the comparison is strictly done on the over drive voltage level. Thus the impact of this assumption will be minimal. Also

this reduces simulation domain to the ultra thin layer of semiconductor thus ensuring very high accuracy and computational efficiency.

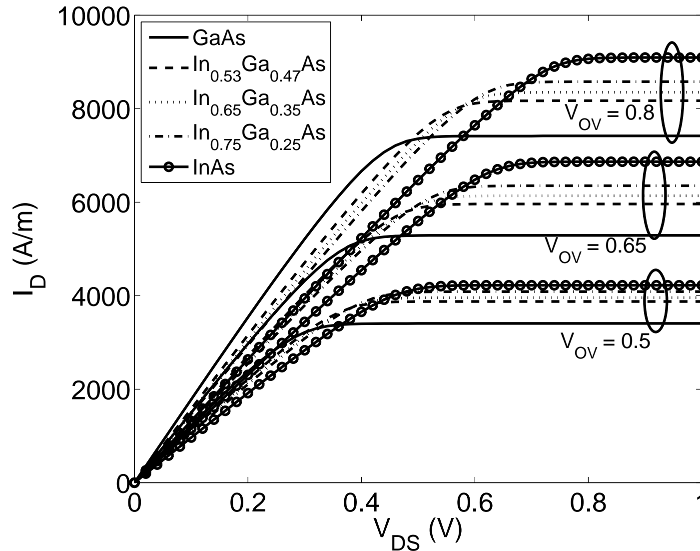

Figure 5.31: Simulated ballistic drain current for different SOI MOSFETs with 5.5 nm thin channel layer for $V_{OV} = 0.5$, 0.65 and 0.8 V simulation.

Fig. 5.31 shows the simulated ballistic drain currents for SOI structure using the five materials under consideration. For SOI MOSFET we see that the trend of DG MOSFET is followed rather than that of the bulk MOSFET. This is because SOI structure like DG MOSFET, creates a quantum well with high boundary potentials which pushes the Eigen energies of the light electrons towards the bottom of the quantum well. Similar behavior as DG MOSFETs is portrayed in the inversion charge density and first Eigen energy profiles shown in Fig. 5.32 and 5.33, respectively.

We can see that the inversion charge density again is maximum for GaAs. But the first Eigen energy of InAs is at the lowest position. Thus like DG MOSFETs, in SOI MOSFETs two contradictory process determines the drain current. The variation of on current with over drive voltage is shown in Fig. 5.34.

We observe that SOI MOSFET shows more consistent behavior in On current compared to DG MOSFETs. The InAs SOI MOSFET provides the best performance for all overdrive

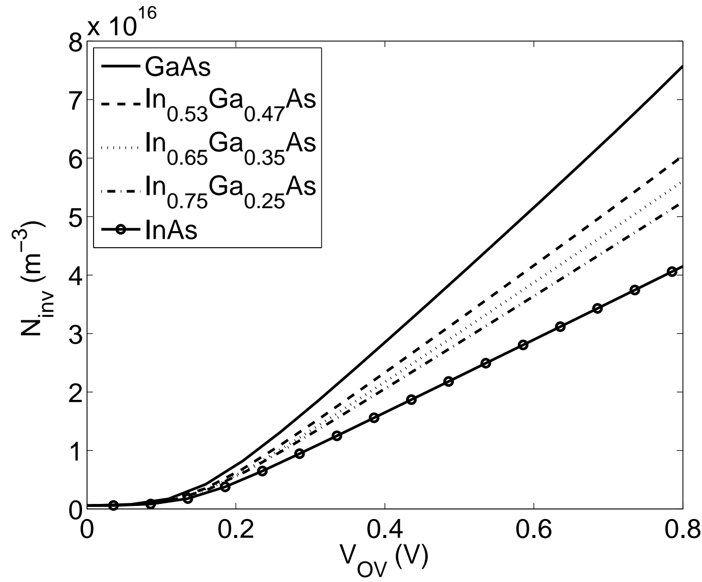

Figure 5.32: Number of inversion carriers N_{inv} for different SOI MOSFETs.

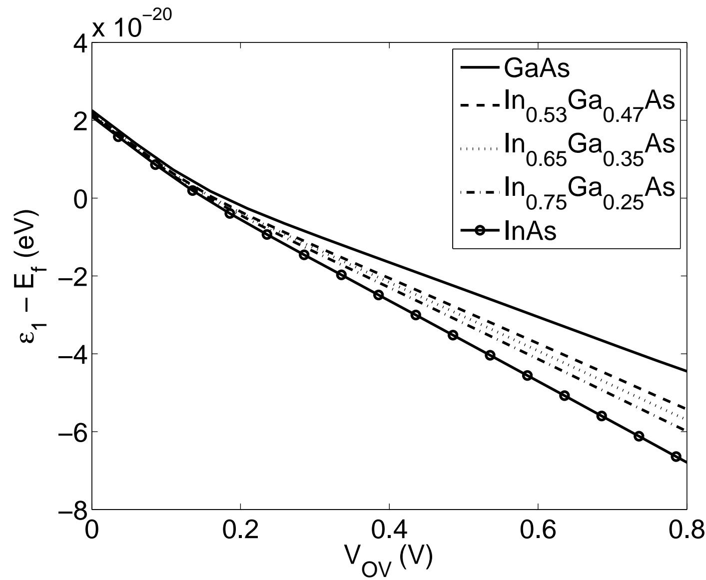

Figure 5.33: Position of first Eigen state ε_1 with respect to the equilibrium source Fermi level for different SOI MOSFETs.

voltages. The difference in on current is shown in Fig. 5.35. Also we can calculate the transconductance for the SOI MOSFETs from Fig. 5.34. The calculated transconductance is shown in Fig. 5.36. Again no significant trend is observed in the transconductance profile.

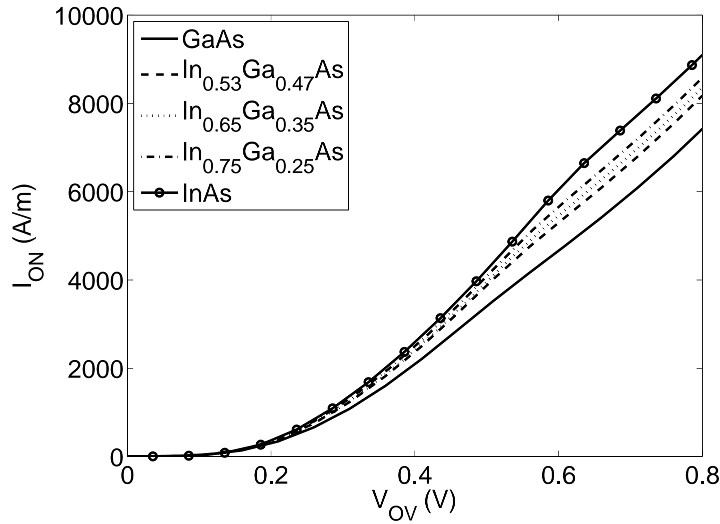

Figure 5.34: Simulated ballistic on current for SOI MOSFETs at V_{DS} = 1.5 V.

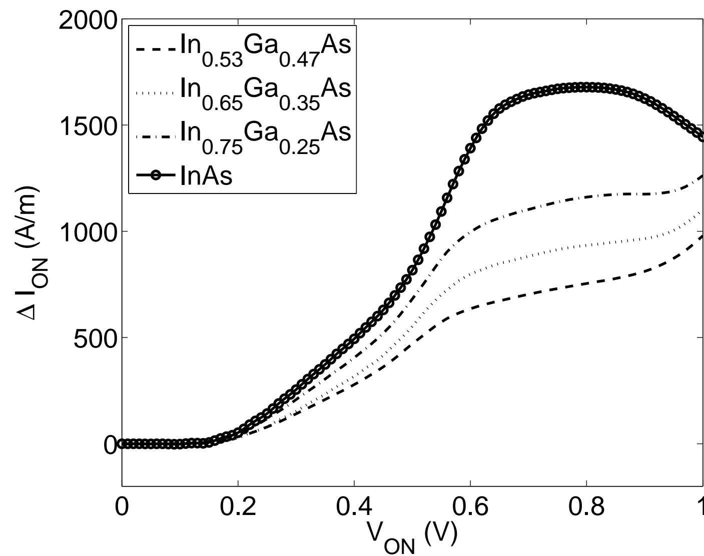

Figure 5.35: Change in simulated ballistic on current for SOI MOSFETs with respect to GaAs SOI MOSFET at V_{DS} = 1.5 V.

5.5 Comparison Among Different Structures

In this section we summarize the calculated On currents of all the devices and the materials. We have taken the bulk MOSFET, the 5 nm channel surface channel MOSFET, the 8

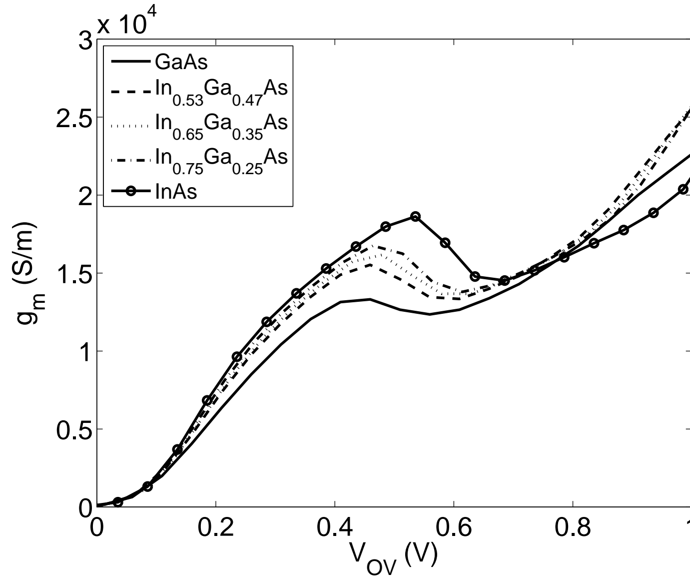

Figure 5.36: Transconductance for different SOI MOSFETs.

nm thin Double Gate MOSFET and the 5.5 nm thin SOI MOSFET. The 5 nm channel surface channel MOSFET is selected as it showed the best performance among the surface channel MOSFETs without any change in the effective masses of the carriers. The 8 nm DG MOSFET is chosen as the 8 nm shows higher current than the 5 nm device and also ITRS suggests 8 nm channel thickness 21 nm half pitch length. Over drive voltage of 0.5 V is taken for comparison as this is the operating voltage according to ITRS. The On currents are summarized in Table 5.4.

Table 5.4: Comparison of On current of different device structures utilizing different III-V compound semiconductors at $V_{OV} = 0.5$ V.

Semiconductor Type	**Bulk (A/m)**	**Surface Channel (A/m)**	**Double Gate (A/m)**	**SOI (A/m)**
GaAs	3972		4837	3405
$In_{0.53}Ga_{0.47}As$	3745		5149	3875
$In_{0.65}Ga_{0.35}As$	3631	3724	5103	3957
$In_{0.75}Ga_{0.25}As$	3523	3689	5137	4087
InAs	3196		4938	4222

According to Table 5.4 the only structure that provide significant improvement in drain current over the bulk MOSFETs is the DG structure. The surface channel structure does not provide any significant benefit and thus promise little towards further progress. The SOI structure performs as well as the bulk structure or even better than the bulk MOSFETs for elements with low electron effective mass. SOI and DG structure also enjoys the added advantage of lower short channel effects which is outside the scope of this study.

For bulk structure materials with high density of states effective mass should be chosen for better current carrying capability. For structures that have quantum well with high boundary potentials, materials with lower effective mass are desirable.

Chapter 6

Conclusion

6.1 Result Summary

The ballistic currents of bulk, surface channel, double gate and semiconductor on insulator MOSFETs have been calculated using over-the-barrier model. For over-the-barrier model the electrostatic solution of the device is required at the top-of-the-barrier. It was assumed that the top-of-the-barrier resides at the source end of the device. The electrostatic solution of the device at the source end was calculated by solving a coupled 1D Schrödinger-Poisson equation with open boundary condition to incorporate the wave function penetration effect. This self-consistent simulator accounts for all the quantum mechanical effects arising from carrier energy quantization and wave function penetration. The currents obtained through these calculation give a comparative picture of bulk, surface channel, DG and SOI MOSFETs using III-V materials.

It has been found that bulk III-V MOSFETs have relatively good current carrying capabilities. Only the double gate structure provides current that is significantly higher than that of a bulk MOSFET. Bulk MOSFET matched the performance of SOI MOSFETs with the surface channel MOSFETs came up short in current driving capability. Also, the analysis shows that for bulk devices or devices without quantum wells should use semiconductors that have high density of states effective mass. For bulk MOSFET, GaAs outperformed all other III-V materials due to the high inversion charge density.

The study shows that surface channel MOSFET is not the way to go. These structures might provide good performance boost in a long channel device but at nano-scale this structure will not be able to live up to the expectation. Also, as the surface channel MOSFET does not have any deep quantum wells the high effective mass materials showed better performance that the materials with low effective mass.

The double gate structure did not see the light of fabrication with Si as the active material due to the inherent complications in fabrication of these devices. But these structure show the most promising results. They produced the highest drain currents. Still this needs more rigorous studies before a concrete statement can be made. As for Si double gate structure, the FinFET which is based on the idea of double gate provided a easier fabrication choice and also better performance. Thus without further inspection a statement might prove to be immature. But, this result shows that DG structure for III-V MOSFETs is a journey worth venturing. Also, as the double gate structure has a deep quantum well the materials with low density of states effective mass showed better performance. Though the advantages of the lower effective mass materials are fluctuating. Further study might shed more light on the topic.

The Semiconductor On Insulator structure was outperformed by the DG structure but it came out as second best. The SOI structure shows promise and also it does not pose many fabrication challenges which is a great drawback of the DG structure. For the SOI structure materials with low effective mass consistently performed well for all gate biases.

6.2 Future Scope of the Work

Further study is required to complete this vast picture that compares several semiconductor materials using several different structures and over a number of performance parameters. This study only determined the on current of the device which dictates the speed of operation. Another very important aspect of a MOSFET is the subthreshold swing. This decides the power consumption of the MOSFET which must be low as ICs using nano-MOS have several billions of transistors on the chip. If power consumption is not managed the chip will over

heat and fail. Very accurate analytical models are present for the calculation of subthreshold characteristics of Si based MOSFETs but they are not very accurate for nano-scale high mobility materials. A Non Equilibrium Green's Function based model will provide a good physical picture of these devices.

Two very important structures have been omitted from this study because they ill fit to the mathematical model used here. These are the FinFET structure and the Quantum Well FET structure. FinFETs have shown very good performance for highly scaled Si based MOSFETs. They might prove very useful a III-V material environment. The simulation of FinFET requires a 2D environment. This can be achieved by changing the 1D Schrödinger-Poisson system to a 2D system. Couple of algorithms are widely used. They are: mode space approximation and real space representation.

The QWFET follows the structure of a HEMT. These structures are strained and also uses a channel that is 2 nm thick. At this scale the constant effective mass approximation breaks down and the effective mass has to be calculated for every energy using a eight band k-p method. The QWFET and FinFET structures might prove very promising.

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