BALLISTIC CURRENT-VOLTAGE MODEL IN DEPLETION ALL AROUND OPERATION OF SILICON ON INSULATOR FOUR-GATE TRANSISTOR

A thesis submitted for the partial fulfillment of the requirement of the degree
of
Master of Science in Electrical and Electronic Engineering

By

Shafat Jahangir

Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology

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Certification

The thesis titled **"Ballistic Current-Voltage Model in Depletion All Around Operation of Silicon on Insulator Four-gate Transistor"** submitted by Shafat Jahangir, Roll No: 100706201P, Session: October 2007, has been accepted satisfactory in partial fulfillment of the requirement for the degree of Master of Science in Electrical and Electronic Engineering on April 24, 2010.

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Declaration

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

_____

Shafat Jahangir

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BUET, Dhaka,
April, 2010 Author

Dedication

To my Parents

Sikder Jahangir Rashid and Sayeda Sultana

Abstract

Two dimensional Poisson-Schrödinger equation is solved numerically in depletion all around (DAA) operation of n-channel four gate transistor (G4-FET) by *finite element method*. Potential distribution is obtained by solving 2-D Poisson equation. The influence of different gate bias voltages on the location and size of the conducting channel is studied, which also includes fully depleted condition for certain gate bias voltages. The developed model is used to investigate the gradual change of the size of the conducting channel from drain to source, when drain is positively biased. Conduction band profile is studied and shallow n-well region is found. By solving 2D Schrödinger equation, Eigen energy at various cross sections between drain and source, subband profiles from source to drain and wave function distribution are observed. Weak energy quantization is found by observing small energy difference (less than kT) between subsequent subband profiles and noticing wave function distribution extending beyond neutral n-well and into the depletion region. Using the outputs of 2D Poisson-Schrödinger solver, a ballistic current-voltage model is developed by mode-space approach and modified Tsu-Esaki equation. Finally, effect of gate bias on current-voltage characteristics is investigated.

Chapter 1

Introduction

Transistors are the key components in practically all modern electronics [1], [2]. The importance of transistors in today's society rests on the ability to be mass-produced using a highly automated fabrication process achieved with astonishingly low per-transistor costs. Since the invention of the bipolar junction transistor in the late 1940's, semiconductors replaced vacuum tube electronics and provided an enormous increase in speed. The electronic circuits made with vacuum tubes were heavy, power-hungry, and unreliable. On the other hand, semiconductor devices are lightweight, low power, and reliable. Semiconductor circuits became popular due to the introduction of the Integrated Circuit (IC) concept, introduced in 1958 independently by Jack St. Clair Kilby and Robert Norton Noyce [3], [4]. Since the introduction of the Integrated Circuit (IC) concept, the number of circuit components that can be placed on an IC has increased exponentially with time. In order to accommodate more transistors in same area device sizes need to be scaled down. Decreasing the device size reduces the area. It also provides a faster transistor with a lower power requirement. In 1965, Gordon Moore, co-founder of INTEL, observed that the number of transistors in an integrated circuit (IC) would double every two years [5], [6]. This observation, known as Moore's Law after Gordon Moore, has been successful in making predictions since 1965. Moore's Law has been the primary driving factor for over the last 40 years for the enhancement of device performances by continuously scaling down the feature sizes of the devices. The competitive drive for improved performance and cost reduction has resulted in the scaling of circuit elements to smaller dimensions [7].

Over time, the process technology has been improved. The Bulk-Si devices have emerged as the unprecedented active element for very large scale integration (VLSI), but a number of fundamental physical limits now hamper the growth of performance of the Bulk-Si

devices. The problems include decreasing carrier mobility due to impurity scattering and increasing gate tunneling current as the junction becomes shallower. These trends make conventional scaling less feasible. As a result, the operating voltage tends to be set higher than that needed by a scaled-down device in order to achieve the desired speed performance [8]. In the Bulk-Si technology, multiple transistors are isolated from each other by reverse biased p-n junctions. With the rapid progress and the evolution of microelectronics, the junction isolation is not always the best approach for integrated circuits. These junctions introduce extra capacitance and reduce the density of the transistors in the circuits.

In search of new process technology, researchers probed for a substrate that would meet the necessary requirements of low junction capacitance, low leakage current, and high breakdown voltage. The requirements are fulfilled by utilizing Silicon-on-Insulator (SOI) wafers. Historically, there were three reasons for developing and using SOI. In the 1970s and 1980s, the radiation hardness of SOI circuits was the primary motivator for choosing new substrates. Thin, active Si films minimized the impact of ionizing radiation on device performance. For the same supply voltage, digital logic circuits, such as microprocessors, run faster in SOI than in the Bulk-Si. Alternatively, it is possible to reduce power consumption of the SOI chips by lowering their operating voltages, while still keeping the clock rate and their performance the same as in more power-hungry Bulk-Si circuits. However, the advantages of SOI technology are not limited to the areas of speed and power. They also include good radiation hardness, the ability to withstand high temperatures, the ability to handle high voltage, contain steep subthreshold characteristics, and have small, short-channel effects [8].

The SOI technology opens up the possibility of having more than one gate for each transistor due to the presence of two oxide layers. Because of the two oxide layers, Double Gate MOSFET (DGMOSFET) is now attracting attention. DGMOSFET utilizes the two oxide layers as independent gates to control conduction. This offers more control over the channel and completely or partially, eliminates the drawbacks of the Bulk-Si technology. However, the maximum number of gates in a transistor is not limited to just

two [9]. The number of gates can be extended to four for SOI technology includes two junction gates in addition to the two oxide gates. The transistor with four gates is called a Four Gate Field Effect Transistor (G^4FET) [10].

The International Roadmap for Semiconductors forecasts a transition from bulk to silicon-on-insulator (SOI) and then to multiple-gate SOI for high-performance digital integrated circuits [11]. Considering this technology trend, it is highly desirable to incorporate analog circuits into CMOS SOI. The four gate transistor (G4FET), which was first introduced in 2002 [10], features the maximum number of gates that can be accommodated in a single device. Preliminary investigations confirm the potential of the G^4FET for innovative analog circuits that can be conceived within a standard partially depleted SOI technology [12]–[15]. Due to its multiple independent gates, the use of the G^4FET enhances circuit design flexibility while reducing transistor count as compared to standard CMOS implementations [14], [15]. The G^4FET combines an accumulation-mode SOI MOSFET and a lateral double-gate JFET in a single transistor. The four gates can be independently biased, enabling the optimization of the electrical characteristics related to one gate by the bias on the remaining gates. In the G^4FET, depending on the bias on the four gates, surface and/or volume conduction modes are available [16]. This work is focused on a specific operation mode of the G^4FET providing volume conduction and called depletion-all-around (DAA) [17], [18]. DAA operation is more versatile than that of a JFET because the use of the extra MOS gates results in superior electrical characteristics. In addition, the DAA operation benefits from the high-density integration advantage enabled by the SOI CMOS technology, which is not available in bulk JFET technology.

1.1 Literature Review

Cristoloveanu et al. [19] proposes and describes the unique four-gate transistor G^4FET. They show experimental results that reveal that each gate can modulate the drain current. Simulations, using commercial tools like Silvaco/Atlas, are presented to clarify the mechanisms of operation. The new device shows enhanced functionality, due to the combinatorial action of the four gates, and opens rather revolutionary applications.

Dufrene et al. [20] proposes a new saturation current model for the n-channel G^4FET, a novel 4-gate transistor. The model is verified against measurement results from G^4FETs fabricated using a standard 0.35-micron partially depleted SOI process. Since the G^4FET is an accumulation-mode device, in case of surface conduction, the conventional first-order JFET model provides the basis for the G^4FET saturation current model. The JFET gate-to-source voltage is replaced by V_{JG}, the bias voltage applied to the G^4FET's junction (or lateral) gates. Then, to include the additional MOS gate bias effects exhibited by the G^4FET's saturation I-V characteristics, the new model develops hierarchical equations for the JFET zero-bias saturation current parameter, I_{D0}, and the pinch-off voltage, V_P. Parameter values for the new model are extracted using curve-fitting techniques.

Akarvardar et al. [21] presents systematic measurements in four-gate SOI transistors (G^4-FET). Methods of extraction for the threshold voltage, sub-threshold swing, and mobility in the linear region are discussed and results are shown. The extracted parameters demonstrate the complex dependence of the multi-gate biases, which is explained. A new extraction technique for the carrier mobility and effective width of devices with isolated multiple gates is proposed.

Dufrene et al. [22] presents simulations, using commercial tools like Silvaco, that are used to better understand the conduction flow caused by the interaction of multiple gates. With a non-uniform doping profile, they have achieved simulations that reproduce the channel characteristics measured in fabricated experimental devices. 3-D simulations are done to further explore the role of the multiple gates of the device.

Dufrene et al. [23] presents the operational performance of the 4-gate transistor (G^4-FET) from the low voltage to the high voltage regime. Measured results show the complexity of threshold voltage, sub-threshold swing, and breakdown voltage due to the multiple gate control utilized with the G^4FET. Devices fabricated in a 0.35µm 3.3V partially-

depleted SOI Honeywell technology can achieve a breakdown voltage of 15V, excellent sub-threshold and high mobility.

Dufrene et al. [24] describes the operation of the novel SOI four-gate transistor (G^4-FET) in the subthreshold region. The sub-threshold slope, which may be defined with respect to either the junction gates or MOS gates, is adjustable using the remaining gates. A comparison of conventional MOSFET swings and G^4-FET swings shows improved subthreshold slope. Systematic experimental data and simulations show the bias conditions for optimized performance.

Dufrene et al. [16] analyzes the various operation modes of the G^4-FET based on the measured current–voltage, transconductance and threshold characteristics. The main parameters (threshold voltage, swing, mobility) are extracted and shown to be optimized for particular combinations of gate biasing. Numerical simulations, using commercial tools like Silvaco, are used to clarify the role of volume or interface conduction mechanisms. Besides excellent performance (such as subthreshold swing and transconductance) and unchallenged flexibility, the new device has the unique feature to allow independent switching by its four separate gates, which inspires many innovative applications.

Akarvardar et al. [25] shows that the operation of the 4-gate transistor (G^4FET) is governed by the charge coupling between front, back and lateral gates. They derive a 2D analytical relation for the fully-depleted body potential. The front-interface threshold voltage is expressed as a function of the back and lateral gate voltages for all possible back interface conditions.

Akarvardar et al. [26] proposes a model for two-dimensional channel potential and threshold voltage of the silicon-on-insulator (SOI) four-gate transistor (G^4FET). The 2-D analytical body potential is derived by assuming a parabolic potential variation between the lateral junction–gates and by solving Poisson's equation. The model is used to obtain the surface threshold voltage of the G^4FET as a function of the lateral gate bias and for all

possible charge conditions at the back interface. The body-potential model is extendable to fully depleted SOI MOSFETs and can serve to depict the charge-sharing and drain-induced barrier-lowering effects in short-channel devices.

Akarvardar et al. [27] reports low frequency noise characteristics of the silicon-on-insulator four-gate transistor. The noise power spectral density as a function of biasing conditions is presented and compared for surface and volume conduction modes. It is shown that, for the same drain current, the volume of the transistor generates less noise than its surface. The possible transition from carrier-number fluctuations to mobility fluctuations as the conducting channel is moved away from the surface toward the volume is also discussed.

Akarvardar et al. [28] shows that in the silicon-on-insulator four-gate transistors, the conducting channel can be surrounded by depletion regions induced by independent vertical metal–oxide–semiconductor gates and lateral JFET gates. This unique conduction mechanism named depletion-all-around (DAA) enables majority carriers to flow in the volume of the silicon film far from the silicon/oxide interfaces. Especially when the interfaces are driven to inversion, the control of the lateral JFET gates on the conduction is maximized, while the sensitivity of the volume channel to the oxide and interface defects is minimized. This leads to excellent analog performance, low noise, and reduced sensitivity to ionizing radiation. G^4FET properties in DAA mode are presented from multiple perspectives: experimental results, 3-D device simulations using commercial tool, and analytical modeling.

Akarvardar et al. [14] presents a novel analog multiplier using SOI four-gate transistors. It is due to the multiple inputs of the G^4FET that may be biased independently; the number of transistors in the proposed circuit is dramatically reduced, compared to conventional single gate MOSFET based multipliers. Only four G^4FETs are needed to build the multiplier core. The circuit is feasible with a standard SOI CMOS process. Two different configurations, both based on the linear modulation of the front-gate threshold

voltage by the junction-gates, are presented. They address the theoretical analysis as well as the preliminary measurement results.

Akarvardar et al. [29] introduces the fully-depleted version of the SOI four-gate transistor (G^4-FET) and its characteristics are systematically investigated. It is shown that the thinning-down of the silicon film promotes vertical coupling between the front and the back gates while mitigating the horizontal coupling between the lateral gates. As a consequence the direct influence of the lateral junction-gates on the body potential distribution is reduced. However, by biasing the back interface in inversion the junction-gates can indirectly modulate the body potential. This provides a very efficient control of the front-channel conduction parameters – such as threshold voltage, sub-threshold swing and trans-conductance – by the junction-gates regardless the device width. The experimental results are clarified by 3-D device simulations using commercial tool and analytical modeling.

In some literature, I-V characteristics and various conduction parameters such as threshold voltage, trans-conductance, sub-threshold slope, etc have been observed mainly in surface conduction mode along with some volume conduction operation using commercial tools like Silvaco/Atlas for large devices (in context to nano-scaling) [17], [26], [28]. In surface conduction mode, surface scattering is unavoidable and in case of larger devices, quantum mechanical effect is not that much pronounced. Ballistic current-voltage model in volume conduction using modified Tsu-Esaki equation [30] and mode-space approach [31] (when channel dimension is comparable to silicon nano-wire and scattering throughout the channel is neglected) utilizing the results from a physics based 2-D Poisson-Schrodinger solver that can take into account the inevitable quantum mechanical effects due to device down-scaling is still not reported in the literature.

1.2 Objective of this Work

In this work, the objective was to develop a ballistic current-voltage model in depletion all around operation (DAA) for silicon on insulator n-channel four gate transistor. On the

way to achieve this goal, a two dimensional Poisson-Schrödinger equation is solved numerically in depletion all around (DAA) operation of n-channel four gate transistor (G^4-FET) by *finite element method*. The influence of different gate bias voltages on the location and size of the conducting channel is investigated, which also includes fully depleted condition for certain gate bias voltages. The developed 2D Poisson-Schrödinger solver is used to observe the gradual change of the size of the conducting channel from drain to source, when drain is positively biased.

Conduction band profile is studied. By solving 2D Schrödinger equation, eigen energy at various cross sections between drain and source, subband profiles from source to drain and wave function distribution are observed. Using the outputs of physics based 2D Poisson-Schrödinger solver, a I-V characteristics simulator considering quantum ballistic transport is developed by mode-space approach [31] and modified Tsu-Esaki equation [30]. Finally, effect of gate bias on current-voltage characteristics is investigated.

1.3 Organization of the Thesis

The first chapter deals with the literature review and objective of the thesis. The second chapter deals with 2D Poisson-Schrodinger equation and I-V characteristics simulator developed by mode-space approach using modified Tsu-Esaki equation. The third chapter presents simulation results and physics based explanations of various observations. Finally summary of this work and suggestions for future works are made in the fourth chapter.

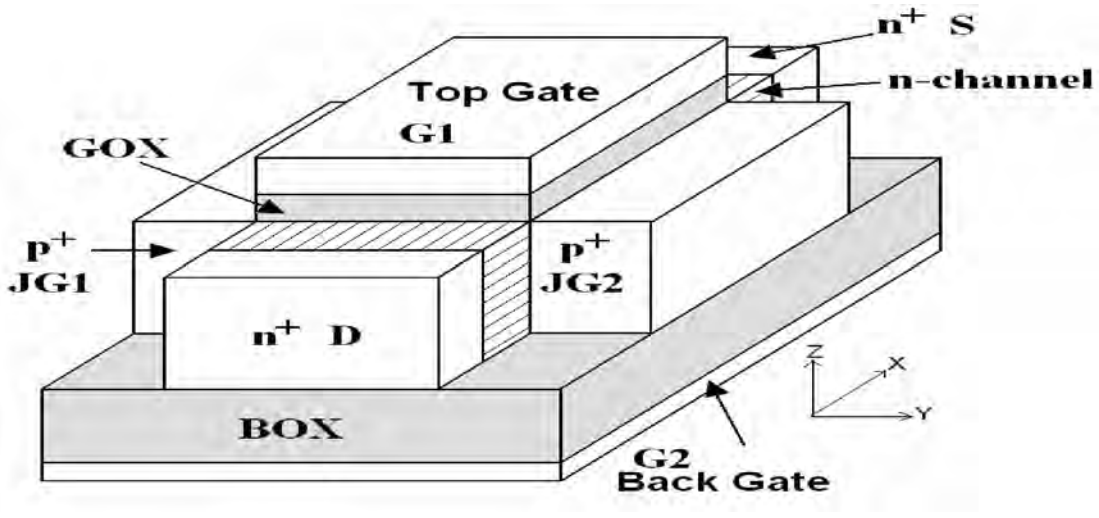
Chapter 2

Depletion-All-Around Operation and Ballistic Current-Voltage Model

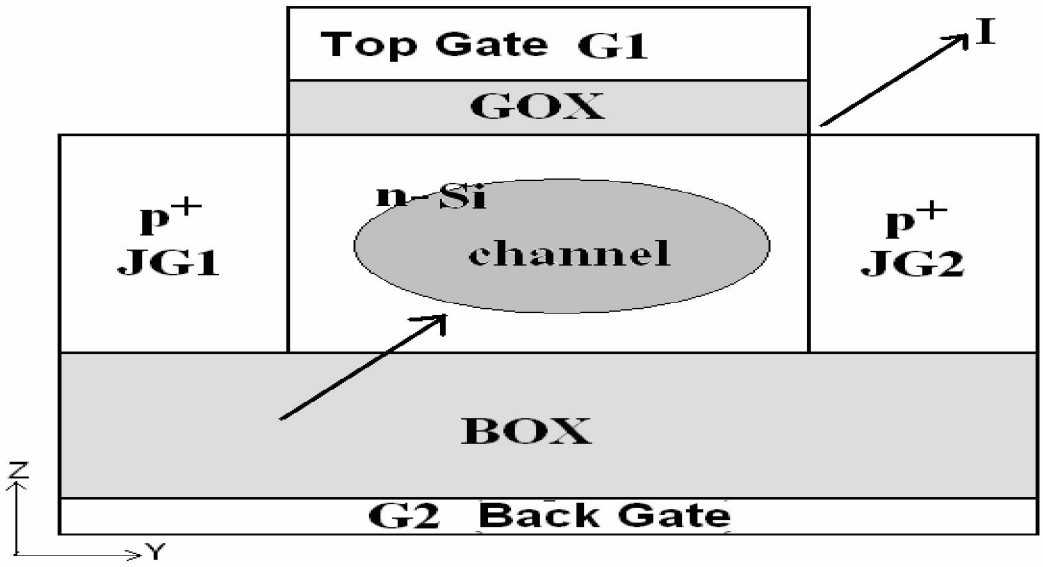
This section describes depletion-all-around operation in an n-channel G^4-FET and ballistic current-voltage model. Physics based numerical models for solving two dimensional Poisson and Schrodinger equations have also been presented considering open boundary condition.

2.1 G^4-FET Structure

The G^4-FET [10], [16] is a double-gate MOSFET comprising two lateral junction-gates (JG1 and JG2) or reciprocally it is a lateral double-gate JFET comprising two vertical MOS gates (poly silicon top-gate G1 and back-gate G2) (Fig. 2.1). G^4-FET comprises four gates in a single transistor. No extra fabrication steps are needed to incorporate G^4-FET-biased circuits with a standard partially or fully depleted (FD) SOI process. In G^4-FET, conduction parameters such as threshold voltage, trans-conductance, sub-threshold slope, etc. related to a single gate can be adjusted by the biases on the remaining gate when the device is driven from one gate keeping the other gates at constant voltages. When G^4-FET is driven from multiple gates simultaneously, multiple-input circuits with much reduced transistor count is obtained compared to the standard CMOS procedure. Thus multiple independent gates of the device enhance circuit design flexibility. In G^4-FET, both surface and volume conduction modes can be achieved applying appropriate bias on the four gates.



(a)



(b)

Figs. 2.1: (a) Schematic structure of the n-channel G^4-FET, (b) Cross section of the device (drain and source are not shown in this case)

2.2 Depletion-All-Around Operation

This work is focused on a specific operation mode of the G4-FET providing volume conduction and called depletion-all-around (DAA) [17], [28]. Because of the use of extra MOS gates, this volume conduction mode gives rise to some better features than that of a single JFET. These include some enhanced electrical characteristics such as high intrinsic dc gain [17], low-noise operation [27], [32] and radiation hardness [18], [33]. Hence it is

very attractive for analog circuits, where low-noise and/or radiation-hard operation is required.

In depletion-all around (DAA) operation of SOI four-gate transistor (G^4-FET), the conduction channel is surrounded by depletion regions induced by independent vertical MOS gates and lateral JFET gates. This enables majority carriers i.e. drain current I_D to flow through the volume of the silicon film far from both silicon/oxide and p+ gate/n-film interfaces. This configuration is achieved by applying appropriate voltages to all four gates of an n-channel G^4-FET. Under appropriate gate bias voltages, the cross-section of the channel can be made sufficiently narrow to invoke quantum mechanical effects. Adjusting bias to all four gates, fully depleted (FD) structure is attained and the proposed current-voltage model is extendable to the FD structure as well. In G^4-FET, volume conduction can also be achieved while the regions near top and bottom gates are populated by inversion charges, thereby creating a bridge between two p+ junction gates. This happens when sufficiently large negative bias is applied to top and back gates. The device performance and properties in DAA mode are remarkably affected by the presence of inversion layers. This work is restricted to depletion-all-around mode of volume conduction and various characteristics are observed accordingly.

2.3 Device Dimension

In this work 2-D simulation is done on a partially depleted DAA n-channel G^4-FET device structure with a channel width of w_si = 90 nm, a film thickness of t_si = 60 nm, a gate oxide thickness of t_gox = 15 nm, channel length of 150 nm and a buried oxide thickness of t_box = 40 nm. The channel doping density is $N_D = 5 \times 10^{17}$ cm^{-3} in the n-type device. The doping density in p+ junction gates is $N_A = 2 \times 10^{20}$ cm^{-3}.

2.4 Ballistic Current-Voltage Model

Two dimensional Poisson-Schrödinger equation is solved numerically in depletion-all-around (DAA) operation of n-channel four-gate transistor (G^4-FET) by finite element

method using COMSOL with MATLAB. Ballistic drain current is calculated by mode-space approach [31] using modified Tsu-Esaki equation [30].

2.4.1 2D Poisson Solver

Since the profile of the depletion region for any given set of gate bias voltages is not known, hence initially an arbitrary depletion charge profile as shown in Fig. 2.2 is assumed in the n silicon film as input to the 2-D Poisson solver. Usual analytical semi-classical equations of depletion width for reverse biased p+-n junction and MOS capacitor cannot be used in this work because those equations cannot take into account 2-D effects such as charge sharing between the junction gates and the MOS gates.

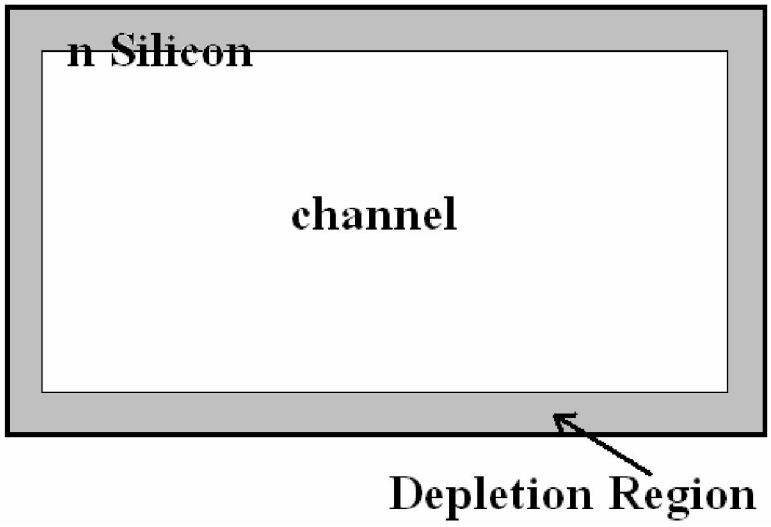


Fig. 2.2: Initially assumed box like channel and depletion charge distribution in the silicon film

From this charge profile, initial potential profile is obtained numerically by solving 2-D Poisson equation as given in Eq. (1).

$$-\in_0 \in_r \left[\frac{\partial^2 V(y,z)}{\partial y^2} + \frac{\partial^2 V(y,z)}{\partial z^2} \right] = \rho_{depl} \qquad (1)$$

Where, *V(y,z)*= Potential profile at any yz cross section.

ρ_{depl} = Depletion charge density (qN_D) within the depletion region and zero within the neutral channel.

$\in_0$ = Permittivity of free space.

$\in_r$ = Relative dielectric constant.

COMSOL with MATLAB is used to solve Eq. (1) using finite element method. COMSOL [34] provides a powerful, interactive environment for modeling and solving scientific and engineering problems using finite element method. Classical PDE in multi-physics mode is used for solving 2-D Poisson equation which is given in coefficient form in COMSOL as,

$$-\nabla \cdot (c\nabla u) = f \tag{2}$$

Comparing Eq. (2) with Eq. (1),

$c \equiv \in_0 \in_r$ = material dielectric constant,

$u \equiv V(y,z)$ = Potential profile at any yz cross section,

and $f \equiv \rho_{depl}$ = Depletion charge density.

From this initial potential profile, a new depletion charge profile is attained which is again fed to Eq. (1) to get a new potential profile. From this second potential distribution a new charge profile is obtained and the whole process is repeated again. Actual voltage profile is reached through this Gauss-Seidel iterative technique when the error converges i.e. when error becomes lass than a predefined value. Here, error is the absolute value of the maximum difference in potential at any point between new and old potential profiles. According to Gauss-Seidel numerical technique, in each loop, new charge profile is obtained from a weighted new potential profile.

Weighted new potential profile = V_old × weightage + V_new × (1-weightage)

Where, V_old = old potential profile

V_new = new potential profile

Weightage = 0.85

Using this Poisson solver, potential profile at any yz cross section between drain and source is achieved by defining the corresponding voltage of the neutral n-channel for various cross sections in the Gauss-Seidel iterative technique. It is assumed that voltage applied at the drain is degraded linearly as shown in Fig. 2.3 from drain to source which is at 0V.

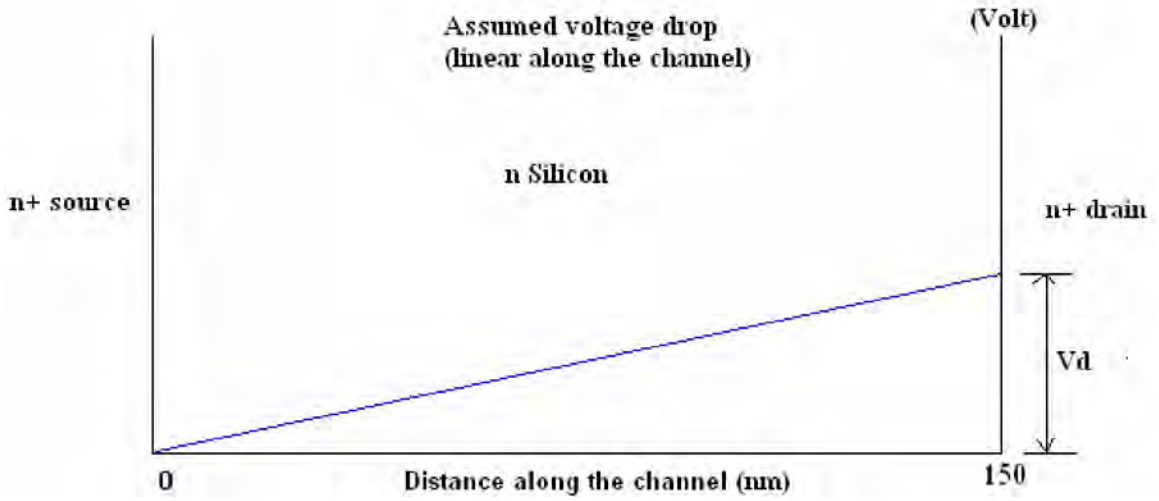


Fig. 2.3: Linear voltage drop from drain to source.

While modeling 2D Poisson solver, Dirichlet i.e. fixed voltage boundary condition is used at the external boundaries of the four gates. Neumann i.e. continuous electric flux boundary condition is used at all internal boundaries. It is assumed that *flat band voltage* (V_{FB}) is zero. As p+ junction gates are heavily doped ($N_A = 2\times10^{20}$ cm^{-3}) and since the applied bias voltages to poly silicon gates are quite small, it is assumed that depletion regions of reverse biased p+ junction/n-film do not extend into p+ gates and poly silicon *depletion effect* is neglected.

2.4.2 2D Schrodinger Solver

Conduction band profiles at various yz cross sections are achieved from corresponding potential distributions. Conduction band change at silicon/oxide interface is 3.1eV. This conduction band profile is fed as input to 2-D Schrodinger Eq. (3). COMSOL [34] with

MATLAB is used to solve 2-D Schrodinger Eq. (3) by finite element analysis under effective mass approximation and open boundary condition.

$$-\frac{\hbar^2}{2m^*_{yi}}\frac{d^2}{dy^2}\varphi_{ij}(y,z)-\frac{\hbar^2}{2m^*_{zi}}\frac{d^2}{dz^2}\varphi_{ij}(y,z)+v(y,z)\varphi_{ij}(y,z)=E_{ij}\varphi_{ij}(y,z) \quad (3)$$

Where, *v(y,z)*= conduction band profile at various yz cross section.

E_{ij} = eigen energy at ith valley of jth subband

Φ_{ij} = wave function distribution at ith valley of jth subband

m_{yi}, m_{zi} = directional effective masses of ith valley at yz cross section.

Classical PDE in multi-physics mode is used for solving 2-D Schrodinger equation which is given in coefficient form in COMSOL as,

$$-\nabla\bullet(c\nabla u)+au=\lambda u \quad (4)$$

Comparing Eq. (3) and Eq. (4),

$u\equiv\varphi_{ij}(y,z)$ = wave function distribution at ith valley of jth subband

$a\equiv v(y,z)$ = conduction band profile at various yz cross section

$\lambda\equiv E_{ij}$ = eigen energy at ith valley of jth subband

$$c\equiv\begin{bmatrix}\frac{\hbar^2}{2m^*_{yi}} & 0\\ 0 & \frac{\hbar^2}{2m^*_{zi}}\end{bmatrix}$$ = directional effective masses of ith valley at yz cross section

This work is done on 100 Silicon wafer with transport (x) along 110 direction, junction gate confinement (y) along -110 direction and top/bottom gate confinement (z) along 001 direction. Directional effective masses are calculated using Ref. [35] and are shown in Table 1.

Table 1: Directional effective masses in terms of m_l and m_t

Valley	m_x	m_y	m_z
Δ_1 [100]	$2\times m_l\times m_t/(m_l+m_t)$	$2\times m_l\times m_t/(m_l+m_t)$	m_t
Δ_2 [010]	$2\times m_l\times m_t/(m_l+m_t)$	$2\times m_l\times m_t/(m_l+m_t)$	m_t
Δ_3 [001]	m_t	m_t	m_l

Where, longitudinal effective mass, $m_l = 0.91 \times m_0$

Transverse effective mass, $m_t = 0.19 \times m_0$

Rest mass of electron, $m_0 = 9.11 \times 10^{-31}$kg

Solving Eq. (3), eigen energies and wave function distribution corresponding to various eigen energies are obtained. Also by solving Eq. (3) for conduction band profiles at various cross sections between drain and source eigen energies at various cross sections are achieved. From these, different subband profiles from source to drain are reached. While modeling 2D Schrodinger Eq. (3), Neumann condition i.e. open boundary condition (Φ_{ij} is continuous across the boundary) is considered at all boundaries.

2.4.3 Ballistic Current-Voltage Equation

In this device, electron faces 2-dimentional confinement (one along top/bottom gate and another along lateral gates) and is able to move along one direction only (source to drain / drain to source). Scattering phenomena is neglected and channel length is less than 200 nm. Hence ballistic approach is taken while calculating drain current. Both *over the barrier* electrons and *tunneling* electrons are taken into account in this ballistic current model.

Ballistic current, calculated using mode space approach [31] by modified Tsu-Esaki model [30] for jth mode (subband), is given by

$$I_{DSj} = [\int q \times V_S(E) \times D_S(E) \times f_S(E) \times dE - \int q \times V_D(E) \times D_D(E) \times f_D(E) \times dE] \times T(E) \qquad (5)$$

Here, E = electron energy and limit of electron energy are considered in such a way that both over the barrier electrons and tunneling electrons are taken into account.

Electron charge, $q = 1.602 \times 10^{-19}$Coulomb

Carrier group velocity of a one-dimensional electron wave propagating towards the drain/source through a certain subband, $V(E) = \text{sqrt}(2 \times (E - E_j)/m_c)$

Density of states of 1D electron wave, $D(E) = 1/(\text{pi} \times \text{hcut}) \times \text{sqrt}(2 \times m_{di}/(E - E_j))$

Fermi-Dirac distribution function, $f(E) = 1/(1 + \exp((E - E_F)/k \times T))$

Transmission coefficient T(E) is obtained using Ref. [36] for various subband profiles from drain to source mentioned in Section 2.4.2.

E_j = stands for the bottom of jth subband.

Conductivity effective mass, $m_c = m_x$.

Density of states effective mass, $m_{di} = m_{x.}$

hcut = h/(2×pi).

h = Plank's constant = 6.625×10^{-34} J-s.

k = Boltzmann constant =1.38×10^{-23} J/K.

E_F = Fermi level energy.

'S' subscript stands for source end, 'D' subscript stands for drain end. Total drain current is simply the sum of all mode currents obtained using Eq. (5). This I-V model is valid for pinch off condition as well. Apart from volume conduction this model is extendable to fully depleted structure and surface conduction mode as well.

Chapter 3

Results and Discussions

In this chapter, simulation results and physics based explanations of effect of gate bias on current-voltage characteristics are presented. Beside that, potential distribution, conduction band profile, eigen energy profile and wave function distribution are observed. Effect of gate bias on the location and size of the conducting channel is studied. Gradual change of the size of the conducting channel from drain to source is also observed when drain is positively biased.

3.1 Effect of Gate/Drain Bias on Conducting Channel

Top gate, back gate, junction gate1 and junction gate2 biases are represented as V_tg, V_bg, V_jg1 and V_jg2 respectively. Built in potential at p+gate/n-Si is about 1V and corresponding depletion width is 52nm. Hence positive bias is applied to p+ junction gates, so that effective junction gate voltage Veff= -1V+V_jg (where V_jg is positive bias voltage to p+ junction gates) and volume conduction is possible. Fig. 3.1 shows a structure, where depletion regions from all gates overlap and a *fully depleted* structure is found, leaving no conducting channel from drain to source and the device goes to *off-state*.

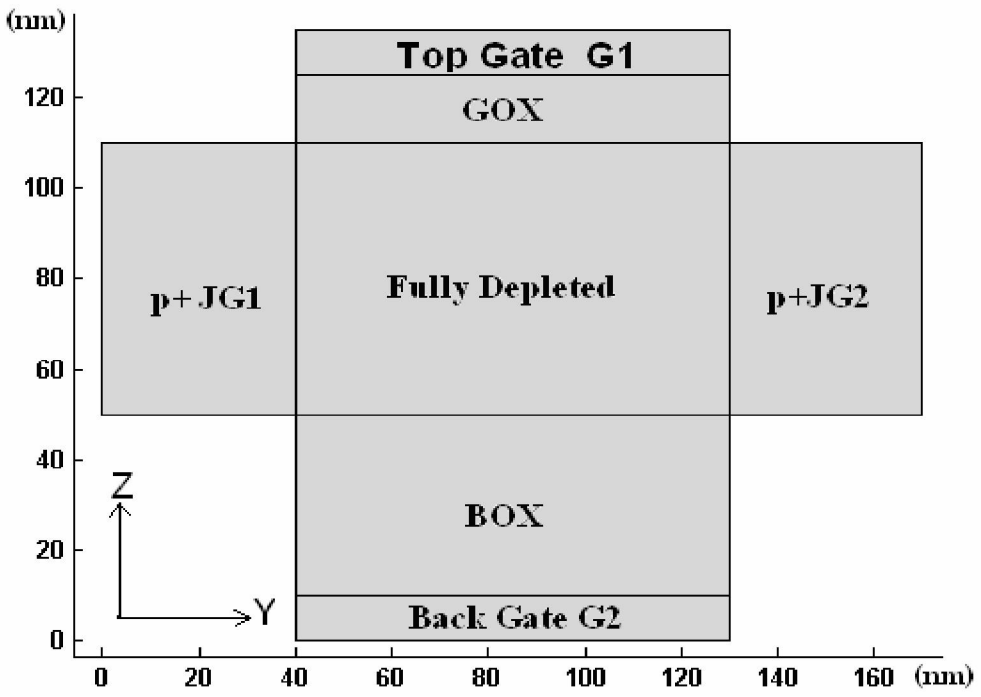


Fig. 3.1: 2-D simulation result showing fully depleted (FD) structure at any cross-section between drain and source with bias conditions: V_tg= -0.6V, V_bg= -0.6V, V_jg1= V_jg2 = 0.1 V, Veff= -0.9V and V_D = 0.25 V, V_S = 0 V.

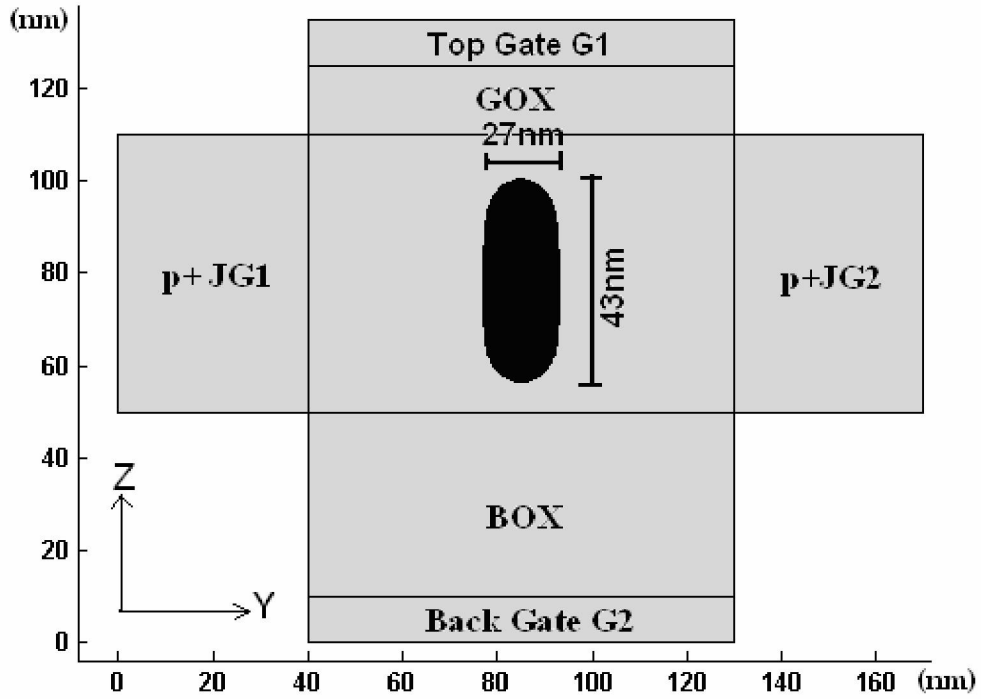
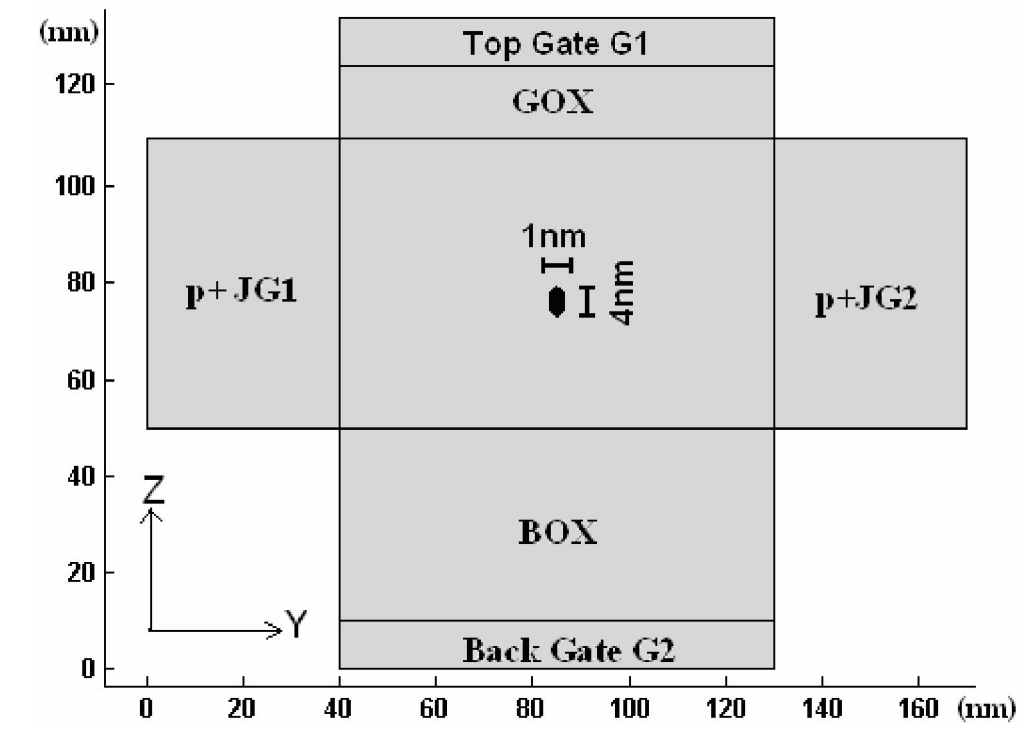


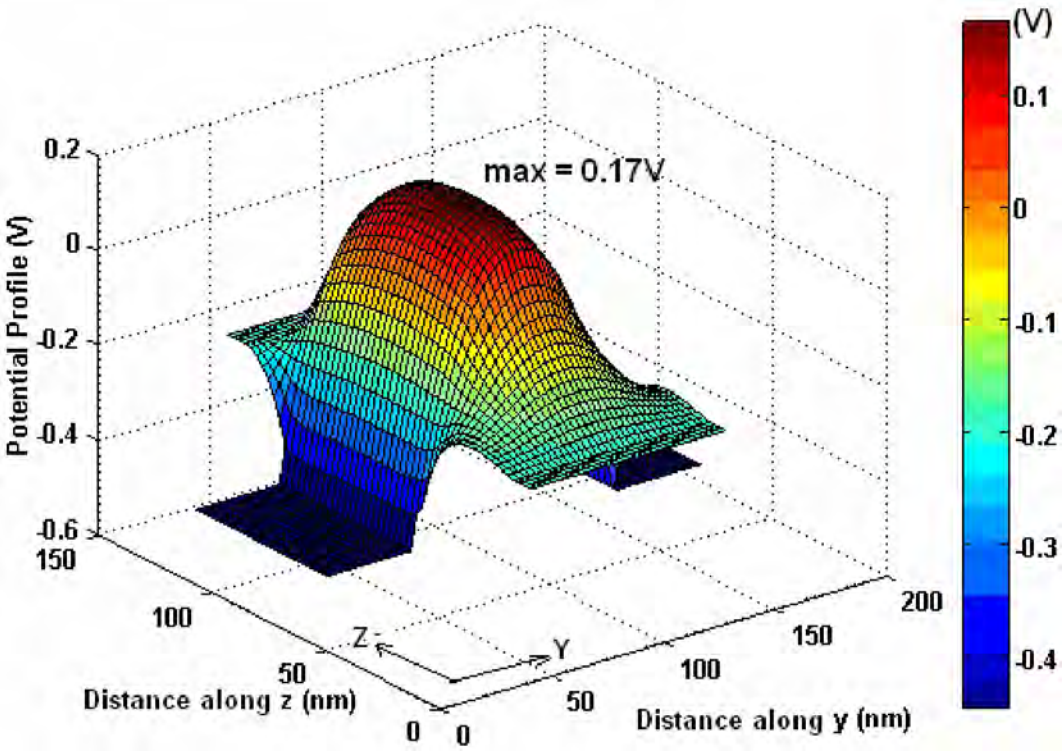
Fig. 3.2: 2-D simulation result showing position of channel (black region) at source end with bias conditions: V_tg = -0.2V, V_bg = -0.2V, V_jg1=V_jg2= 0.45V, Veff = -0.55V and V_D = 0.25 V, V_S = 0 V. Channel is at 0 V.

By applying appropriate bias on all four gates, the conducting channel is confined at the center of the silicon film, thereby avoiding unwanted surface scattering and improving carrier mobility. Such a structure is shown in Fig. 3.2.

Similar channel structure as Fig. 3.2 is observed in Fig. 3.3(a) near the pinch off point of the channel with V_D = 0.25 V and V_S = 0V. In this case the channel is contracted near the pinch off point than before as shown in Fig. 3.2 because the n-film/p+ junction near the pinch off point is more reverse biased than before. From the pinch off point up to the drain end the channel is *pinched-off*. Moving forward towards source from pinch off point, keeping the bias conditions as stated above, gradually expanding channel is observed at each subsequent cross-section and finally reach the structure as Fig. 3.2 at source terminal. This is because the voltage applied at the drain is dropped gradually as one travels from drain to source and becomes zero at the source. Fig. 3.3(b) shows corresponding potential distribution where the channel (black region) is near pinch-off point (0.17V) and all of the four gates are at negative bias required for depletion all around operation.

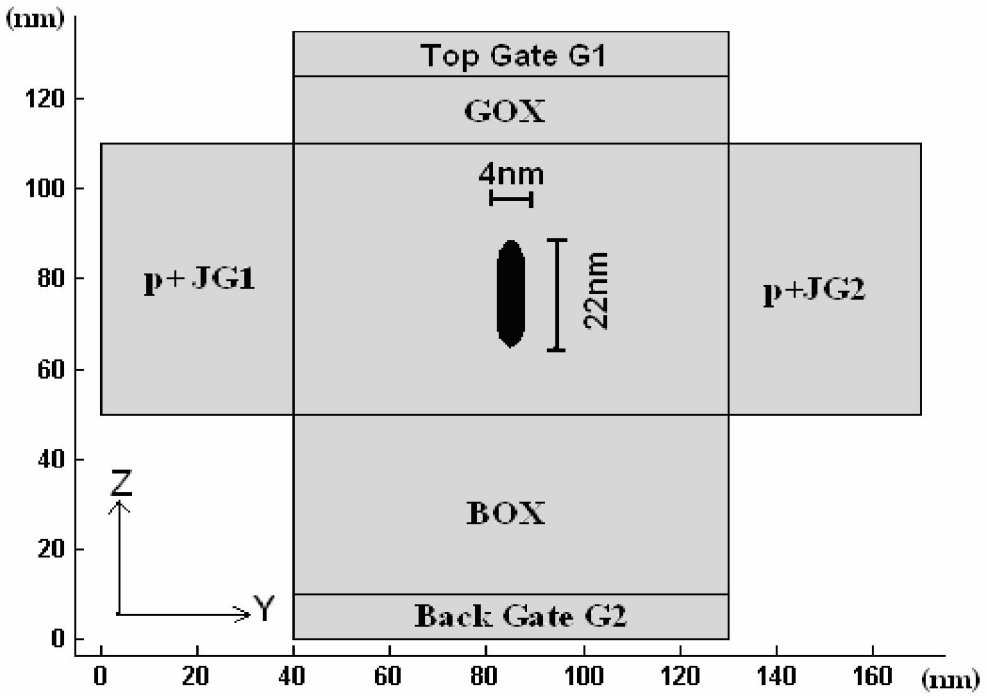


(a)

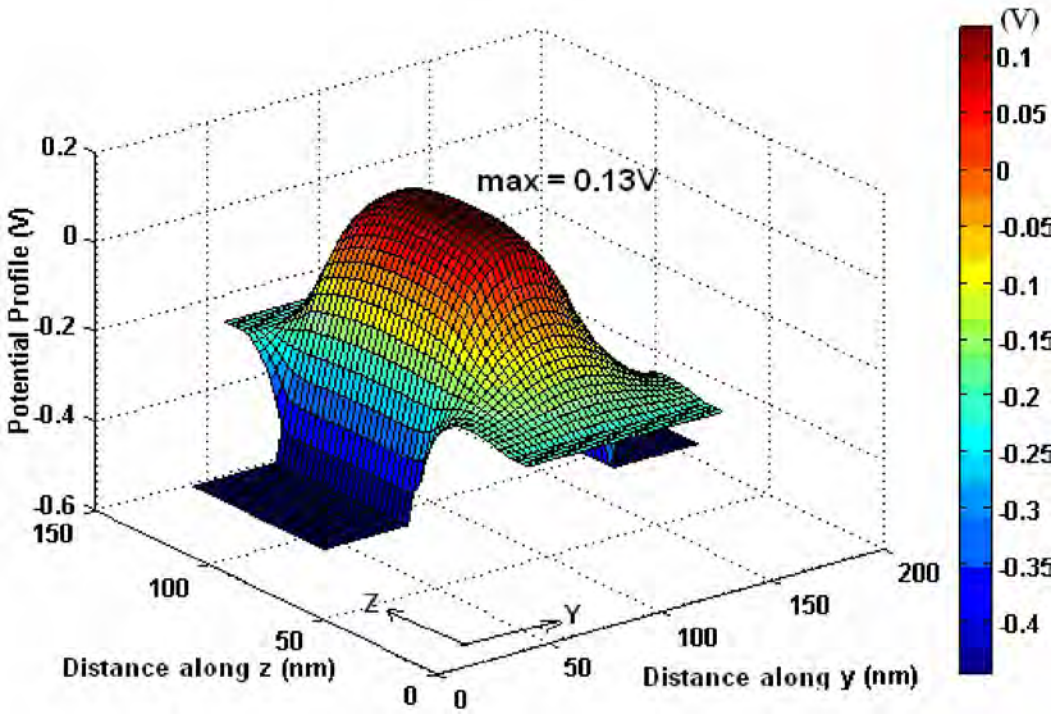


(b)

Figs. 3.3: (a) 2-D simulation result showing position of channel (black region) near pinch off point with bias conditions: V_tg = -0.2V, V_bg = -0.2V, V_jg1=V_jg2= 0.45V, Veff= -0.55V and V_D = 0.25 V, V_S = 0 V, (b) Corresponding potential distribution where the channel is at 0.17 V.



(a)



(b)

Figs. 3.4: (a) 2-D simulation result showing position of channel (black region) at a cross-section between source and pinch off point, with bias conditions: V_tg = -0.2V, V_bg= -0.2V, V_jg1=V_jg2= 0.45V, Veff= -0.55V and V_D = 0.25 V, V_S = 0 V, (b) Corresponding potential distribution where the channel at the cross section is at 0.13 V.

Keeping the bias conditions as above, Fig. 3.4 presents a depletion-all-around channel structure in between drain and source where the channel is at 0.13 V. It is noticeable that this time the channel is larger than that at the pinch off point but smaller than that at the source.

For a given gate bias, Fig. 3.5 shows that 2D channel cross section is gradually reduced from source end (which is at 0V) to pinch off point (which is at 0.17V).

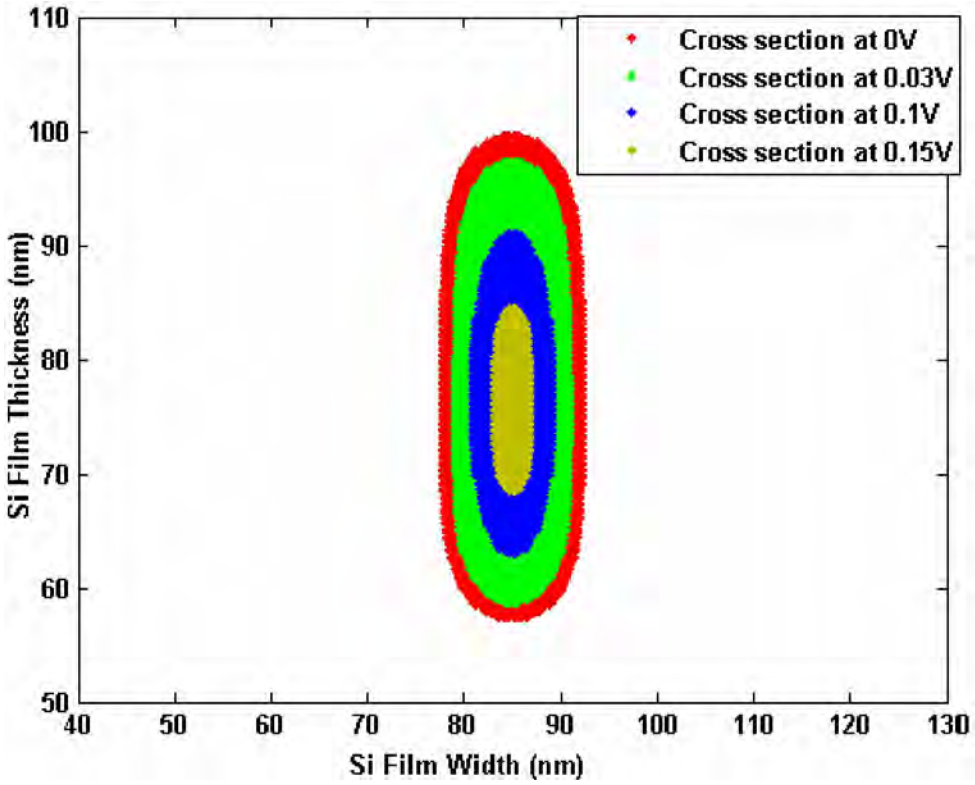


Fig. 3.5: Channel area at different cross section from source up to pinch off point overlapped on each other in Si film of width 90 nm (from 40 nm to 130 nm according to the co-ordinate of this work) and thickness 60 nm (from 50 nm to 110 nm according to the co-ordinate of this work) with bias conditions: V_tg= -0.2V, V_bg= -0.2V, V_jg1= V_jg2= 0.45V, Veff= -0.55V and V_D = 0.25 V, V_S =0V.

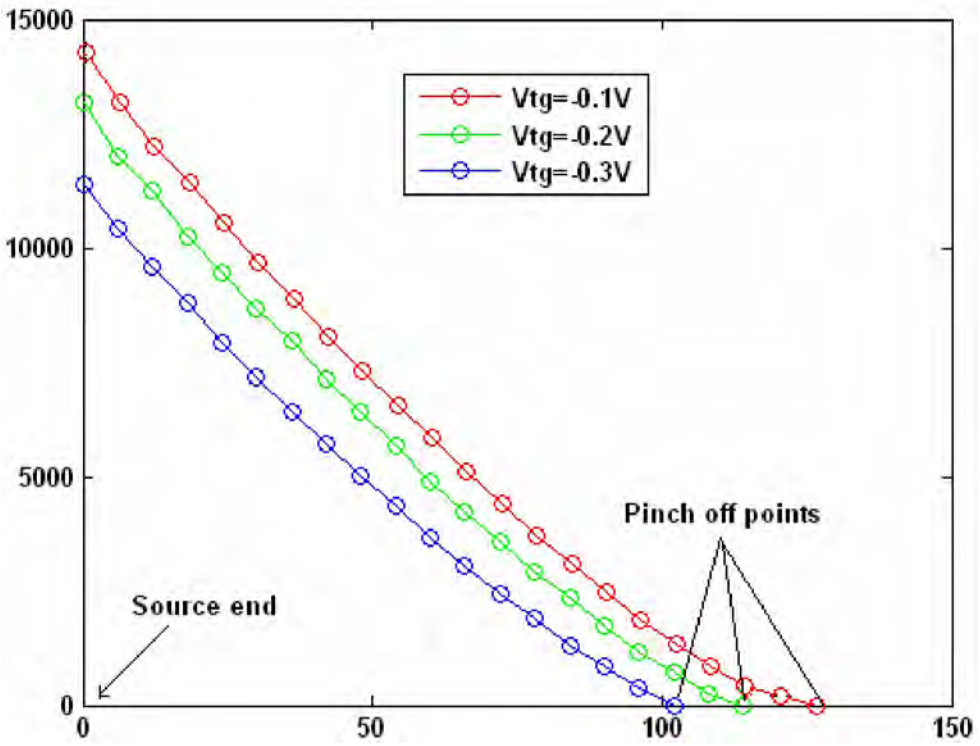
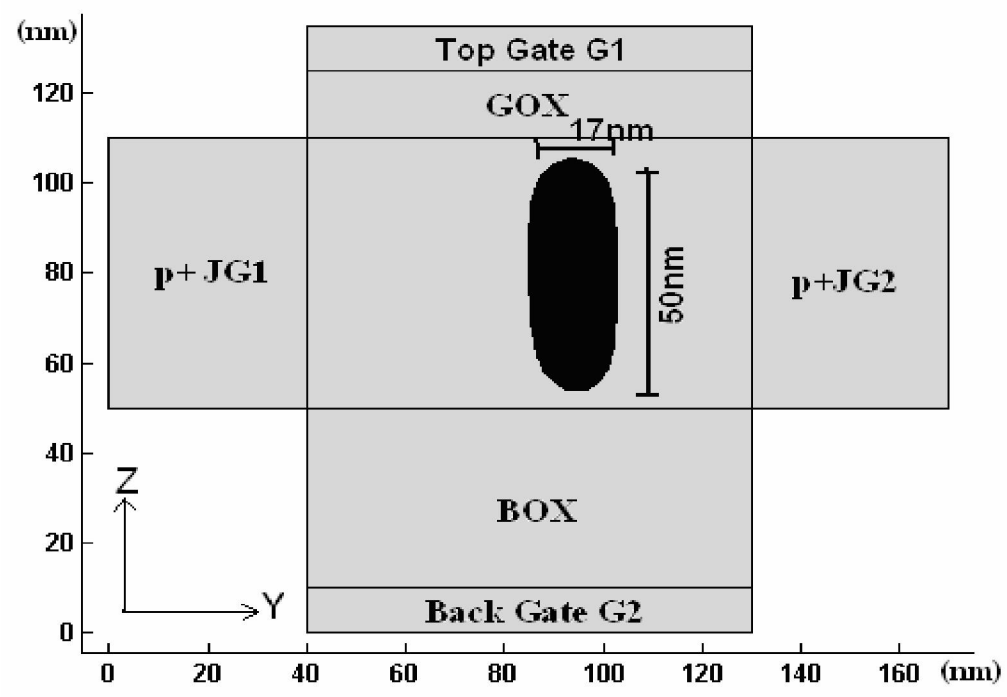
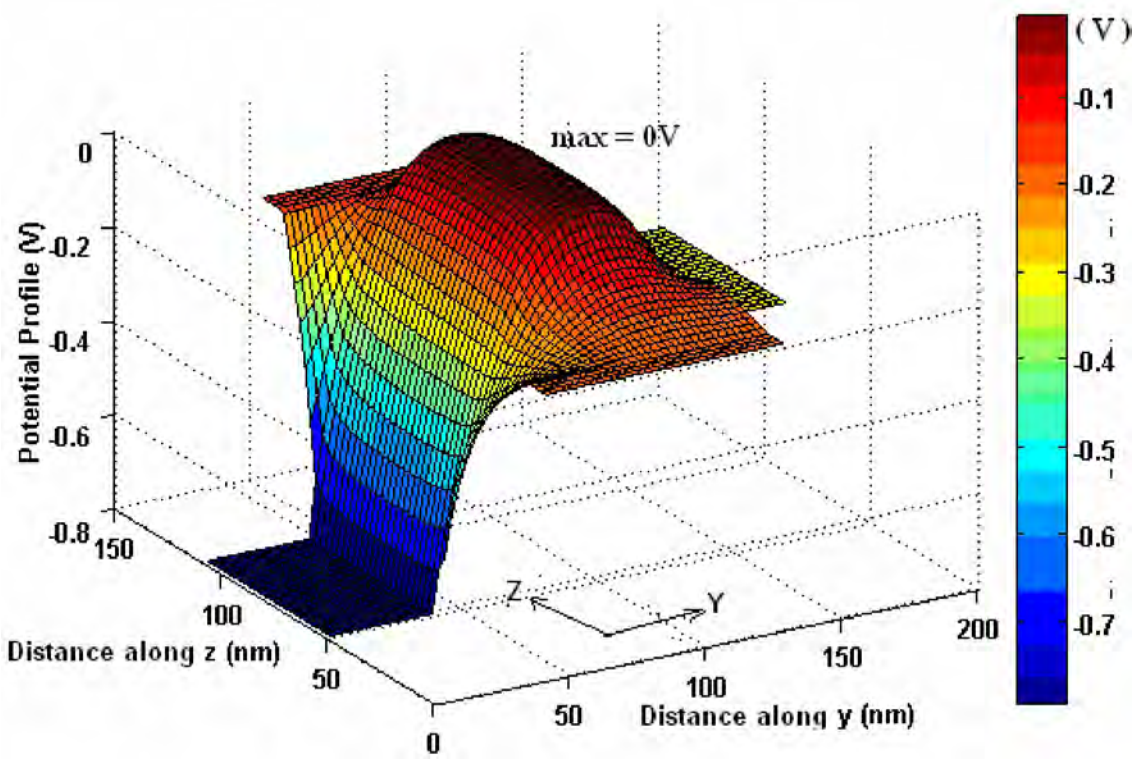


Fig. 3.6: No. of grid points in the channel vs distance from source for different gate bias combination with V_bg= -0.4V, V_jg1=V_jg2= 0.45V V, Veff= -0.55V are fixed, but top gate voltage V_tg is varied.

In Fig.3.6, for all gate bias combinations, channel area becomes zero before drain end i.e. pinch off condition is reached before drain end in all cases. It is noticed that as top gate voltage is increased negatively with other gate bias remaining fixed, initial channel area at source end (at 0 nm) decreased due to the increased depletion region near the gates. It is assumed that voltage applied to drain end is linearly reduced towards the source end where it finally becomes zero. Hence, it is also observed that for a given gate bias combination, as one travels from source end to drain end, channel area is decreased gradually, because the n-film/p+ junction at any subsequent cross section is more reverse biased than that of previous cross section. The more negative the top gate voltage, the more far away is the pinch off point from the drain end.



(a)



(b)

Figs. 3.7: (a) 2-D simulation result showing position of channel (black region) at source end with bias conditions: V_tg = -0.15 V, V_bg = -0.2 V, V_jg1= 0.2V, V_jg2 = 0.5 V, and V_D = 0.25 V, V_S = 0 V, channel is shifted to the right and it is at 0V, (b) Corresponding potential distribution.

The position of the channel within the silicon film can be adjusted by adjusting the different gate bias voltages. Fig. 3.7 shows such a scenario where the channel is shifted to the right. Pinch-off region is defined as the region where number of grid points in the channel is zero.

Using this model in DAA operation, size and location of the conducting channel can be controlled through appropriate gate bias to increase carrier mobility, thereby enhancing device performance. Besides, the dimensions of the channel can be confined to less than 20 nm. For such dimension, electron energy gets quantized which gives rise to various new and interesting quantum mechanical effects.

3.2 Conduction Band Profile

Conduction band profile is obtained from the potential profile. From Fig. 3.8, it is observed that n-well (neutral channel region) is very shallow as compared to the well-known n-well near silicon-oxide surface for a single gate enhancement type MOSFET and hence electron energy quantization is actually influenced by the well, formed by the barriers at oxide/semiconductor interfaces and p+gate/n film junctions. Hence weak energy quantization is expected. Conduction band barrier height at silicon-gate oxide interface is 3.1 eV.

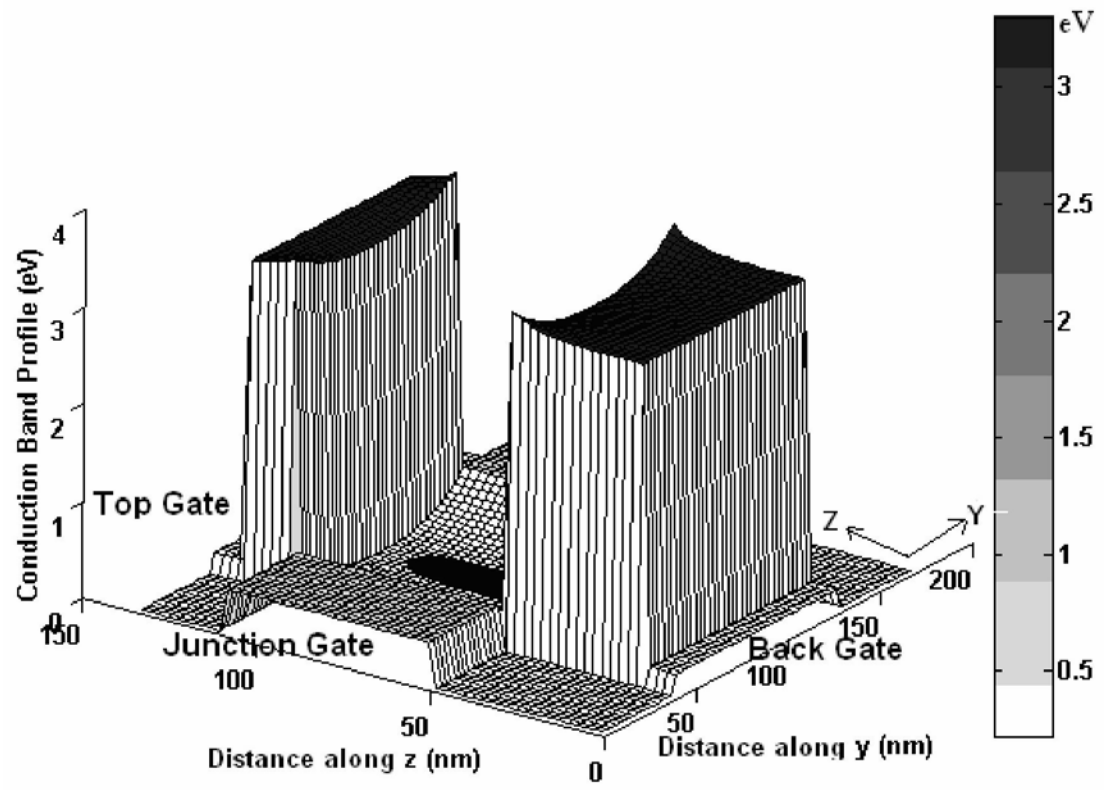


Fig. 3.8: Conduction band profile with bias conditions: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V and channel (black region at the bottom) is at 0V

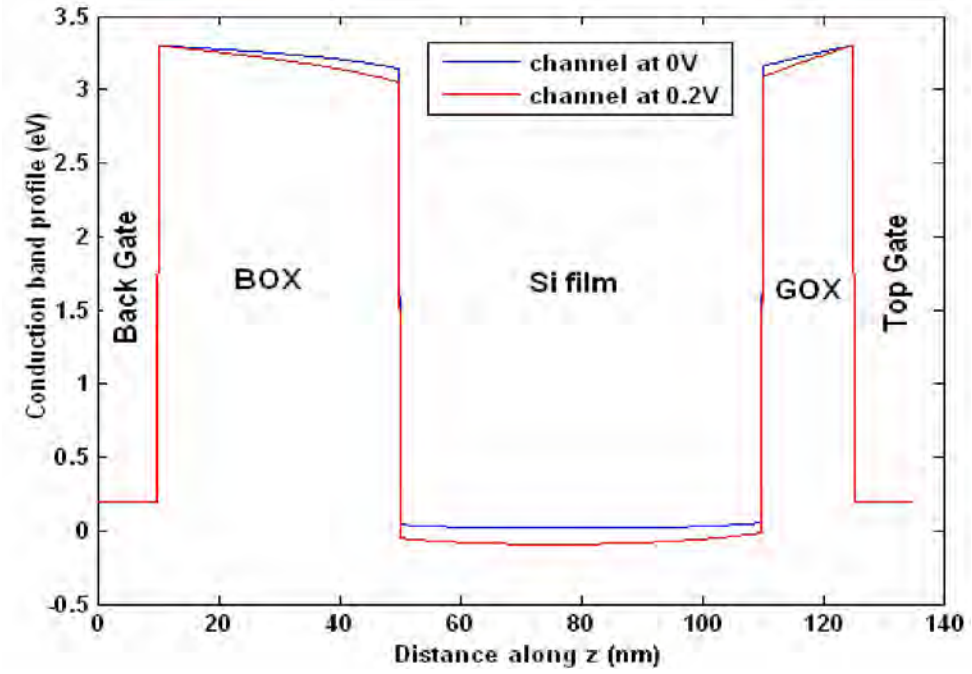


Fig. 3.9: Cross-section view of conduction band profile with bias conditions: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V.

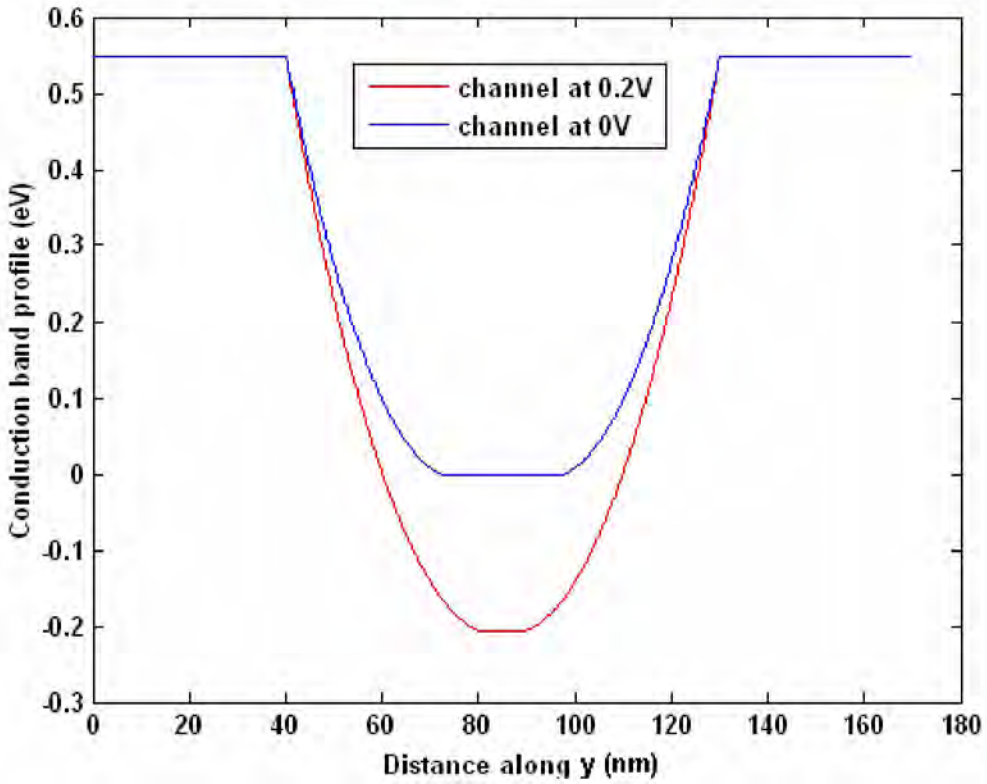


Fig. 3.10: Cross-section view of conduction band profile with bias conditions: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V.

3.3 Subband Profile and Wave Function Distribution

Fig. 3.11 shows first five subband profiles from source to drain for a given gate bias combination and drain voltage. It is seen that subband profiles are reduced almost linearly from source end to pinch off point. After pinch off up to the drain end, eigen energy profiles are reduced parabolically. Difference in conduction band profile between n+ source and n-Si film is calculated to be 0.0954 eV according to previously assumed doping density. Debye length/diffusion length at the n+ source/n-Si junction is neglected.

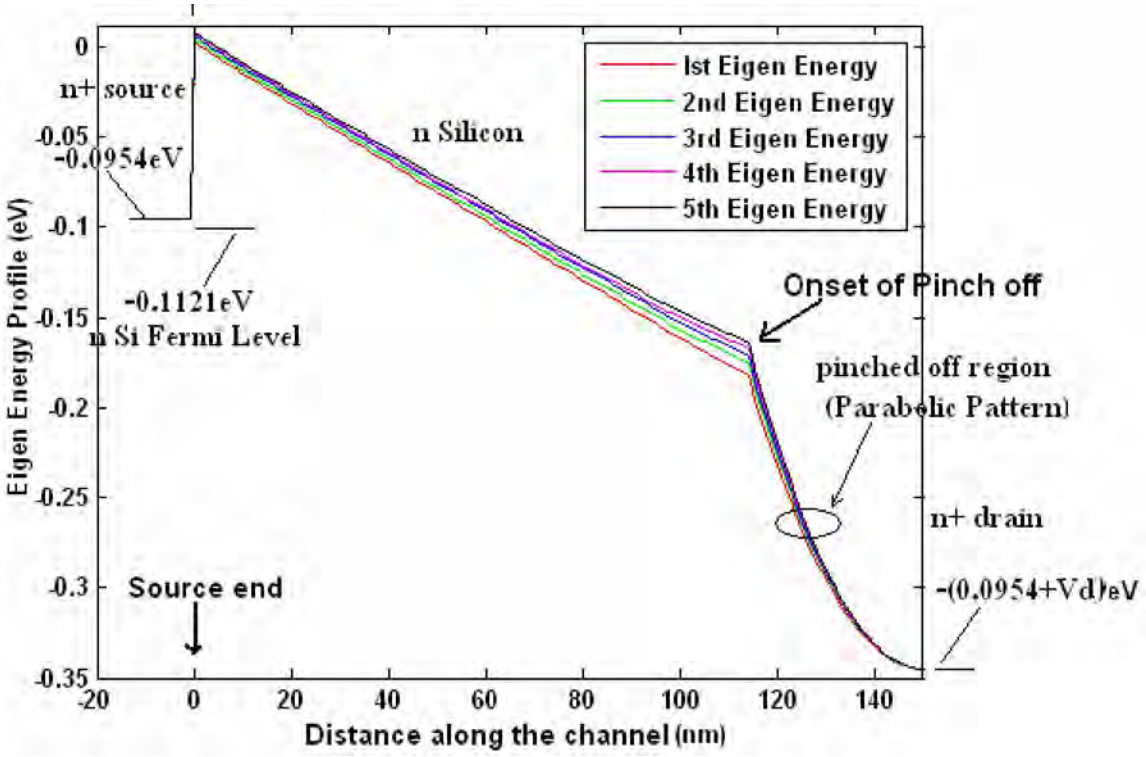


Fig. 3.11: First five eigen energies vs distance along the channel from source end, with bias: V_tg = -0.15 V, V_bg = -0.4 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V and V_D = 0.25 V.

For better understanding, Fig. 3.12 shows first five subband profiles from source end to the pinch off point for the above gate bias combination and drain bias. From Fig. 3.12 it is found that difference between successive subbands i.e. eigen energies is less than kT (in eV) and in some cases successive subband profiles become almost degenerate. This result gives a picture of weak energy quantization.

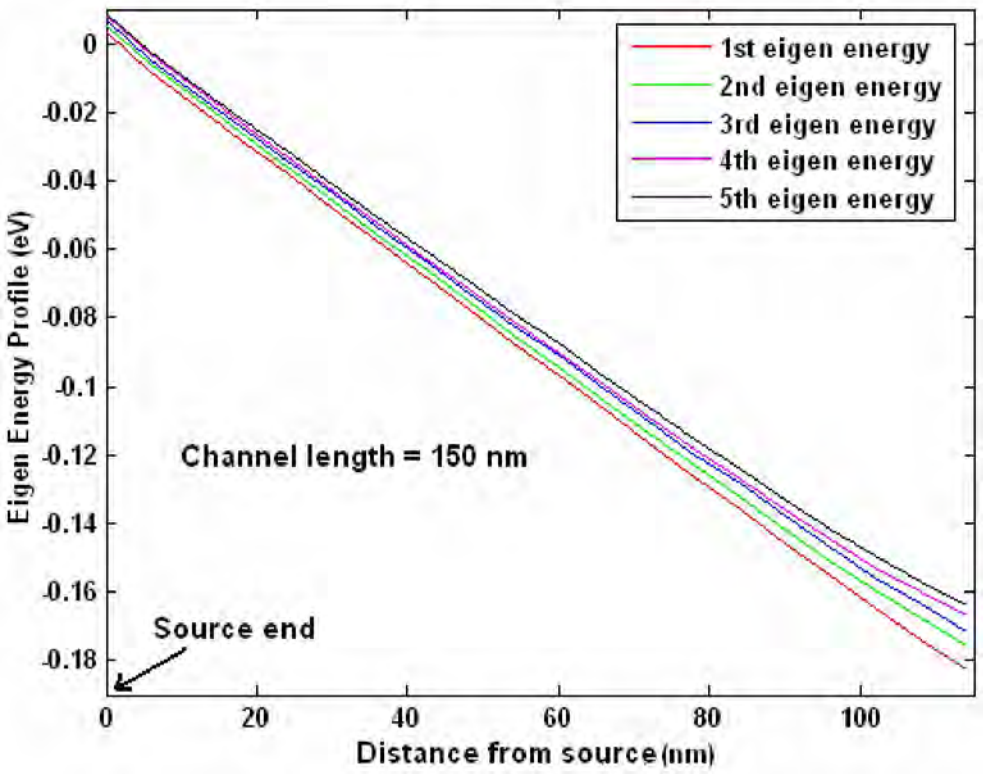


Fig. 3.12: First five eigen energies vs distance from source end up to pinch off point with bias: V_tg = -0.15 V, V_bg = -0.4 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V and V_D = 0.25 V.

Fig. 3.13 shows first eigen energy profile from source to drain, as top gate voltage is increased negatively with other gate biases kept at fixed voltages. From Fig. 3.13 it is visible that as top gate voltage is increased negatively, pinch-off of channel occurs farther away from the drain end. Fig. 3.14 shows the same result as Fig. 3.13, but near pinch off point only, for better understanding. Fig. 3.14 shows first eigen energy vs channel length with bias: V_bg= -0.4V, V_jg1=V_jg2=0.45V, Veff= -0.55V. Here, X1, X2 and X3 are pinch off points along the channel for different top gate voltages.

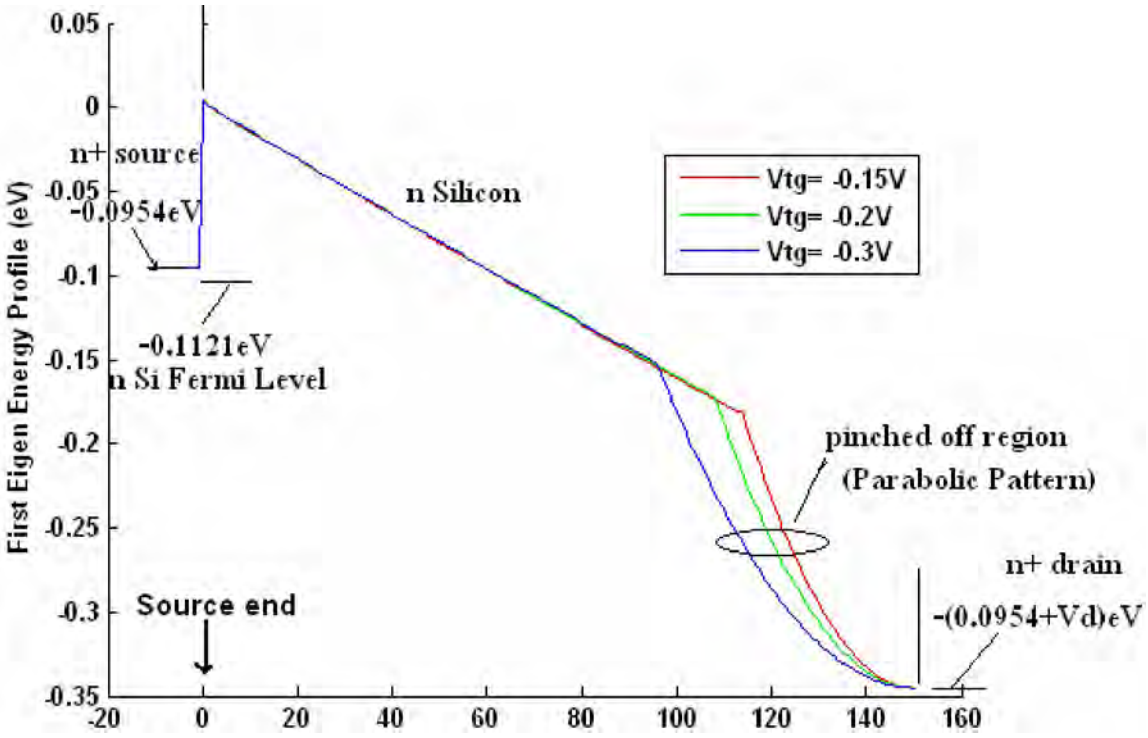


Fig. 3.13: First eigen energy profile vs distance along the channel, with bias: V_bg= -0.4V, V_jg1=V_jg2=0.45V, Veff= -0.55Vand V_D = 0.25 V, where top gate bias is varied in each case.

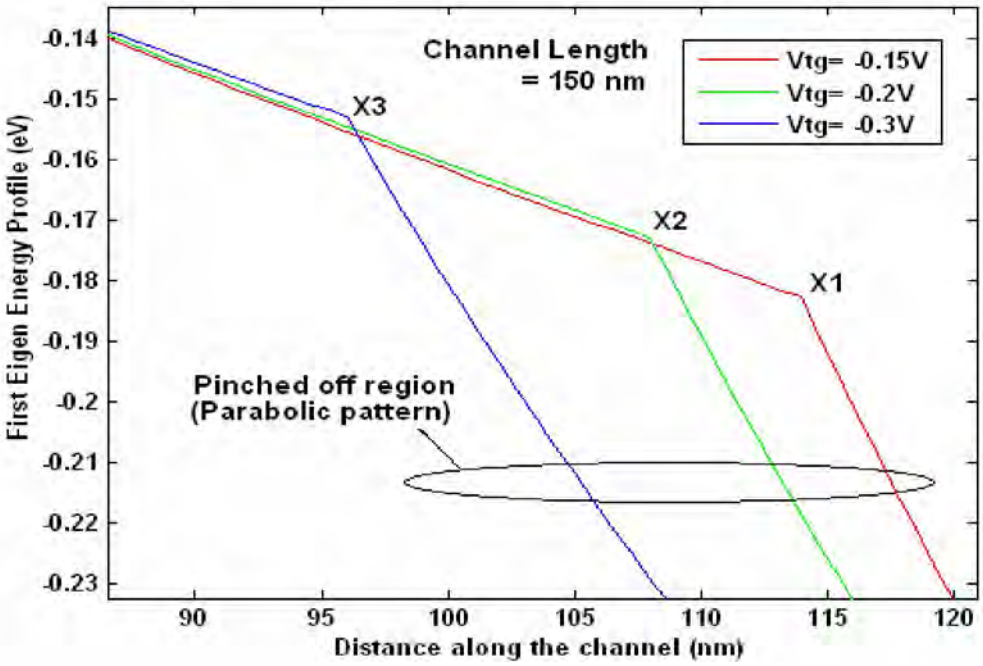
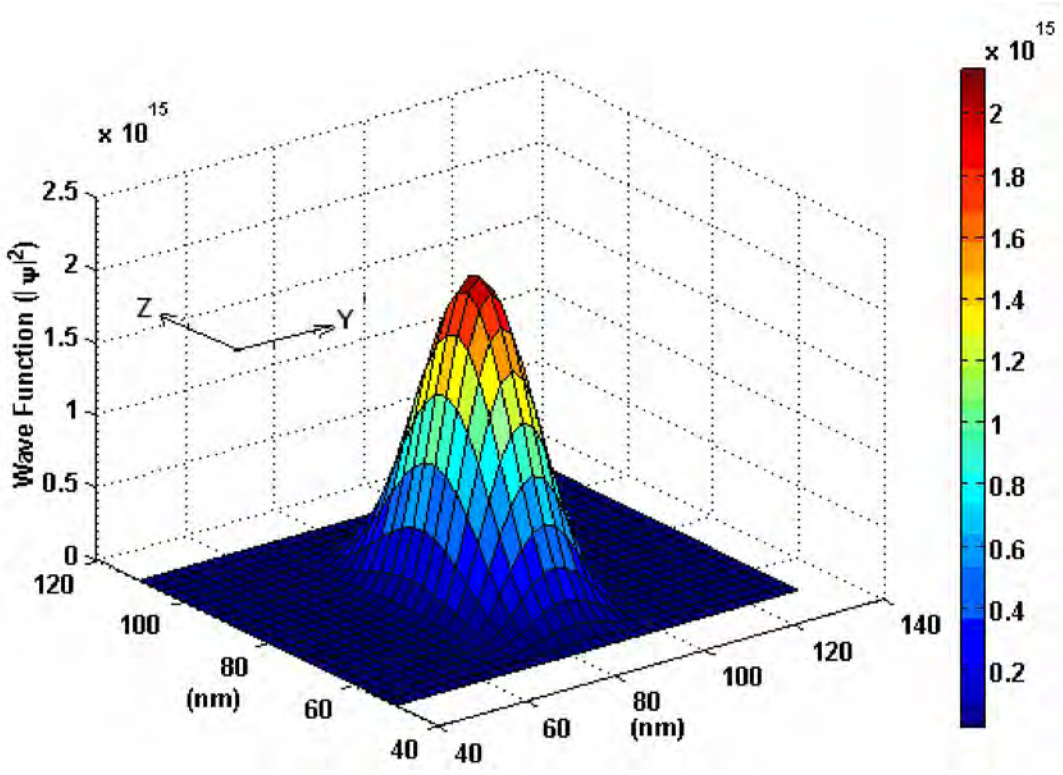


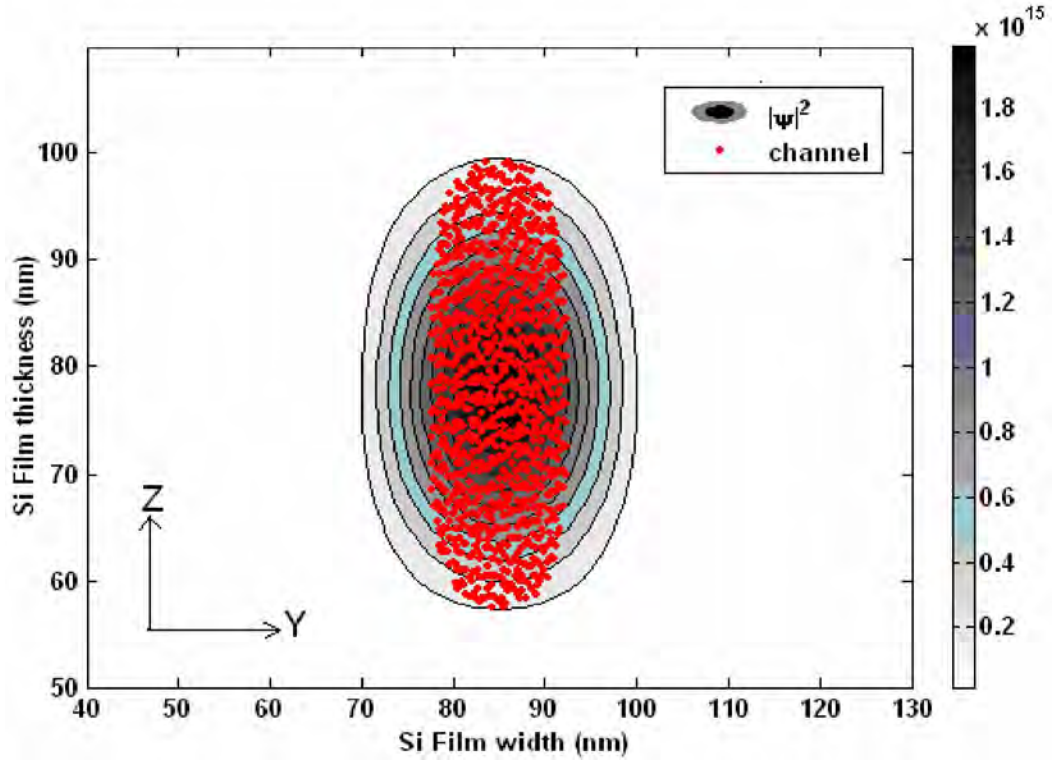
Fig. 3.14: First eigen energy profile vs distance along the channel, with bias: V_bg= -0.4V, V_jg1=V_jg2=0.45V, Veff= -0.55V and V_D = 0.25 V. X1, X2 and X3 are pinch off points along the channel for different top gate voltages.

Fig. 3.15 shows 3D plot and corresponding contour plot of wave functions regarding first eigen energy for a certain gate bias combination and a certain cross-section. It is observed that wave function $|\Psi|^2$ i.e electrons are not confined within the n-channel, rather it extends into the depletion region but never into gate-oxide or p+ junction gates. This result also represents weak energy quantization. This is because electron energy quantization is actually influenced by the well, formed by the barriers at oxide/semiconductor interfaces and p+/n junctions, not by the shallow n-well alone. In these cases only the silicon film is shown, not the whole device.

Fig. 3.16 shows 3D plot and corresponding contour plot of wave functions regarding second eigen energy for the same gate bias combination and cross-section. Similarly, Fig. 3.17, Fig. 3.18 and Fig. 3.19 show 3D plot and corresponding contour plot of wave functions regarding third, fourth and fifth eigen energies respectively, for the same gate bias combination and cross-section. In each case, it is observed that wave function $|\Psi|^2$ is not confined within the n-channel, rather it extends into the depletion region representing weak energy quantization.

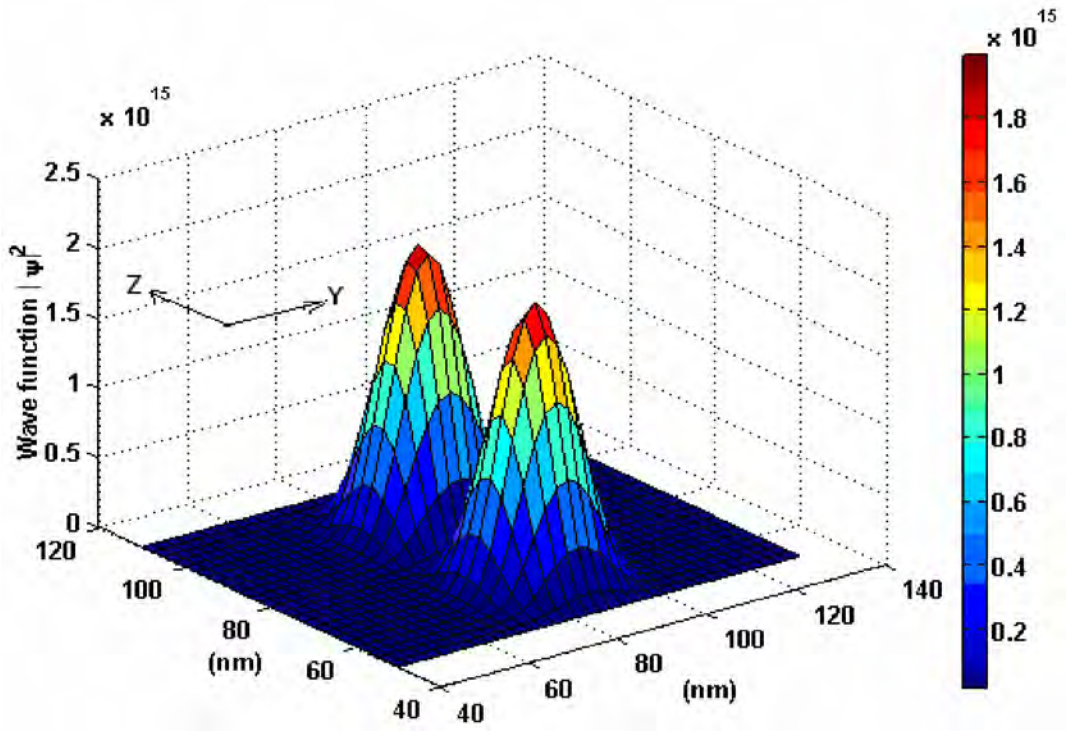


(a)

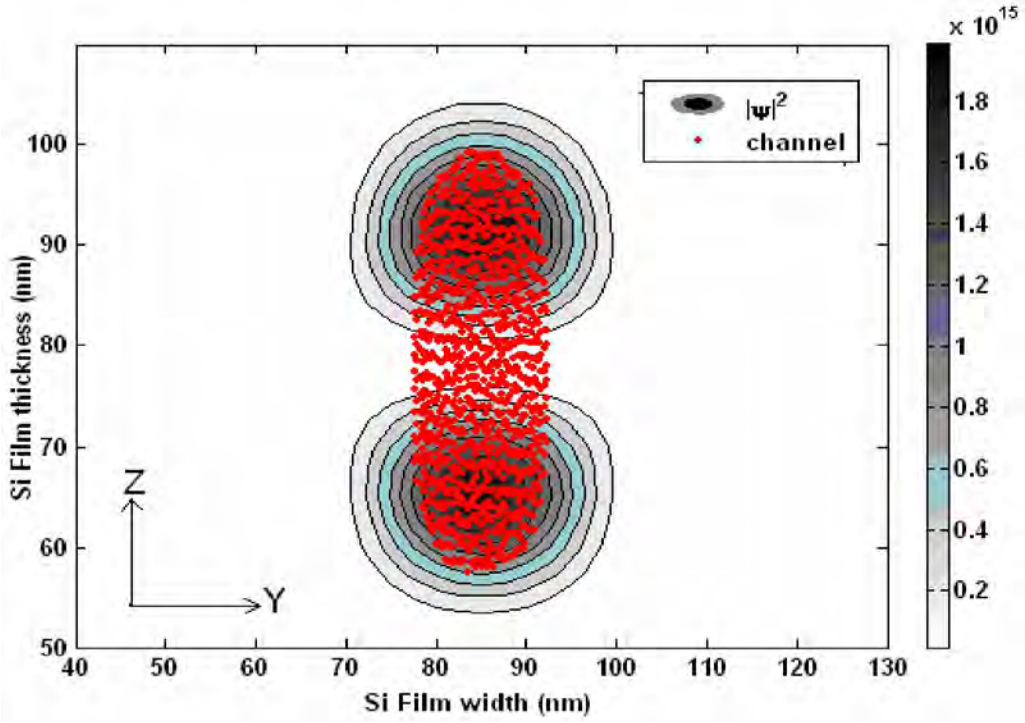


(b)

Figs. 3.15: (a) 3-D plot and (b) contour plot of normalized wave function corresponding to 1st eigen energy showing channel (red spotted region). Gate bias: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V; channel is at 0V.

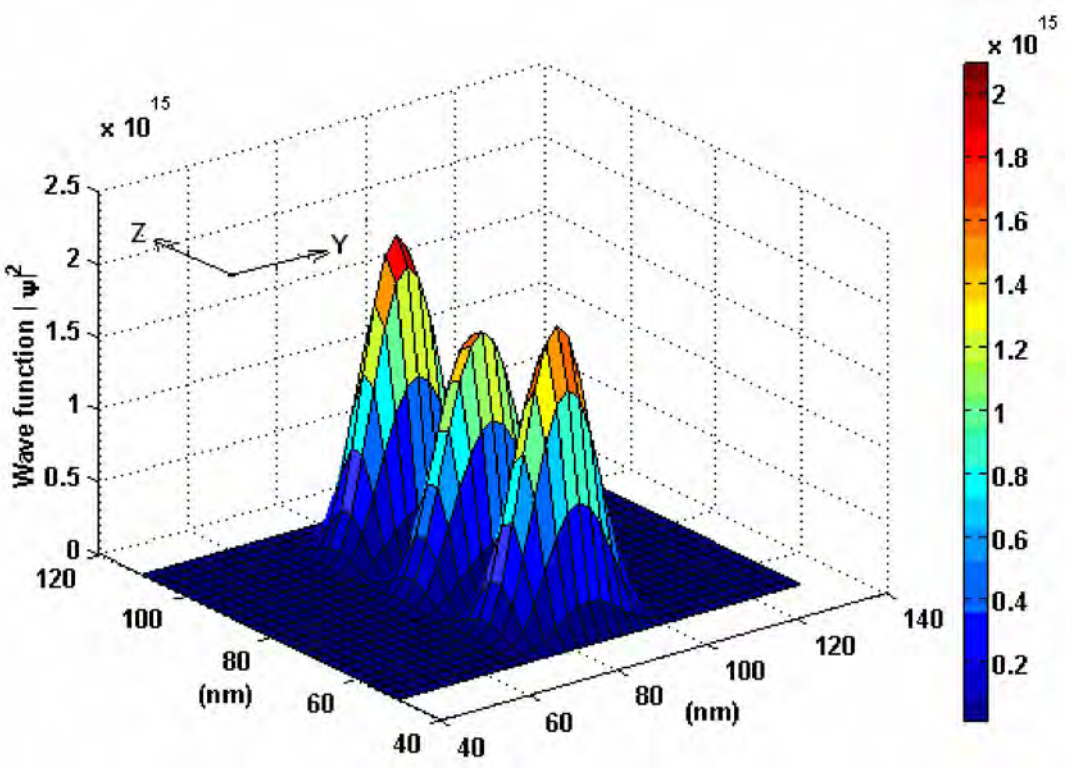


(a)

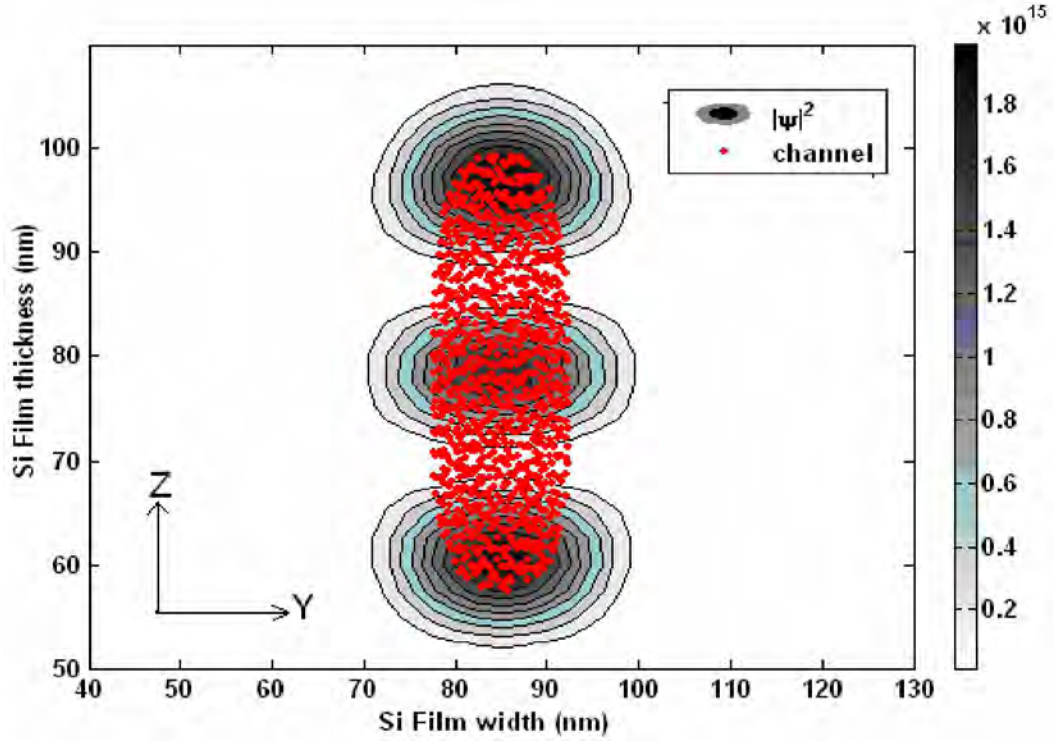


(b)

Figs. 3.16: (a) 3-D plot and (b) contour plot of normalized wave function corresponding to 2nd eigen energy showing channel (red spotted region). Gate bias: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V; channel is at 0V.

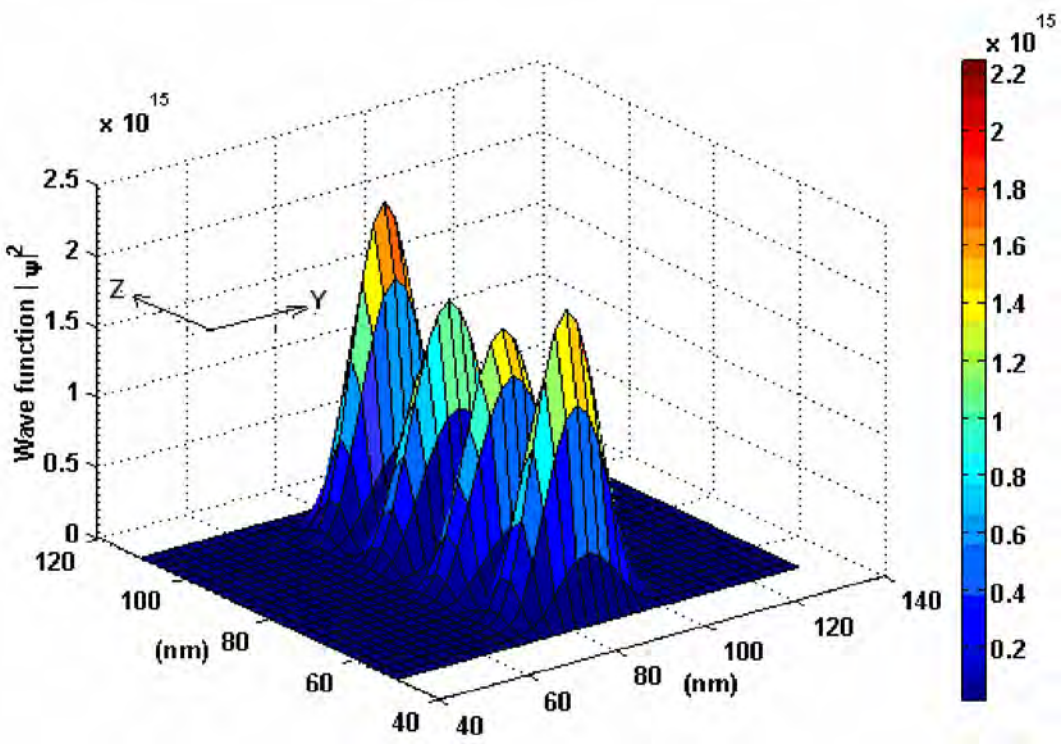


(a)

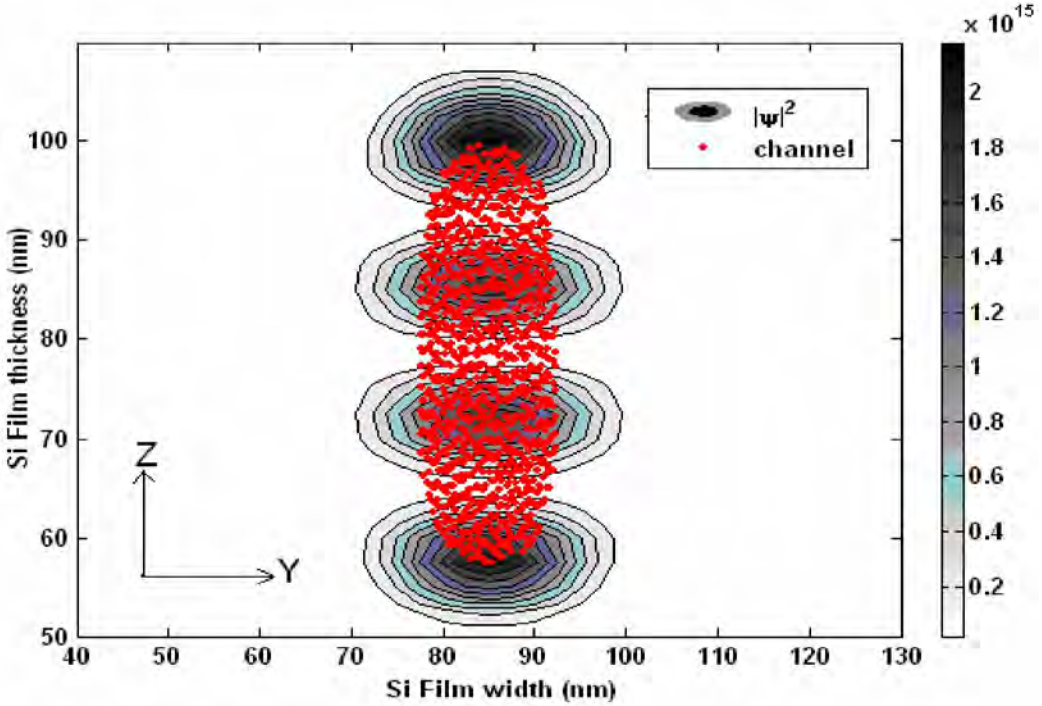


(b)

Figs. 3.17: (a) 3-D plot and (b) contour plot of normalized wave function corresponding to 3rd eigen energy showing channel (red spotted region). Gate bias: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V; channel is at 0V.

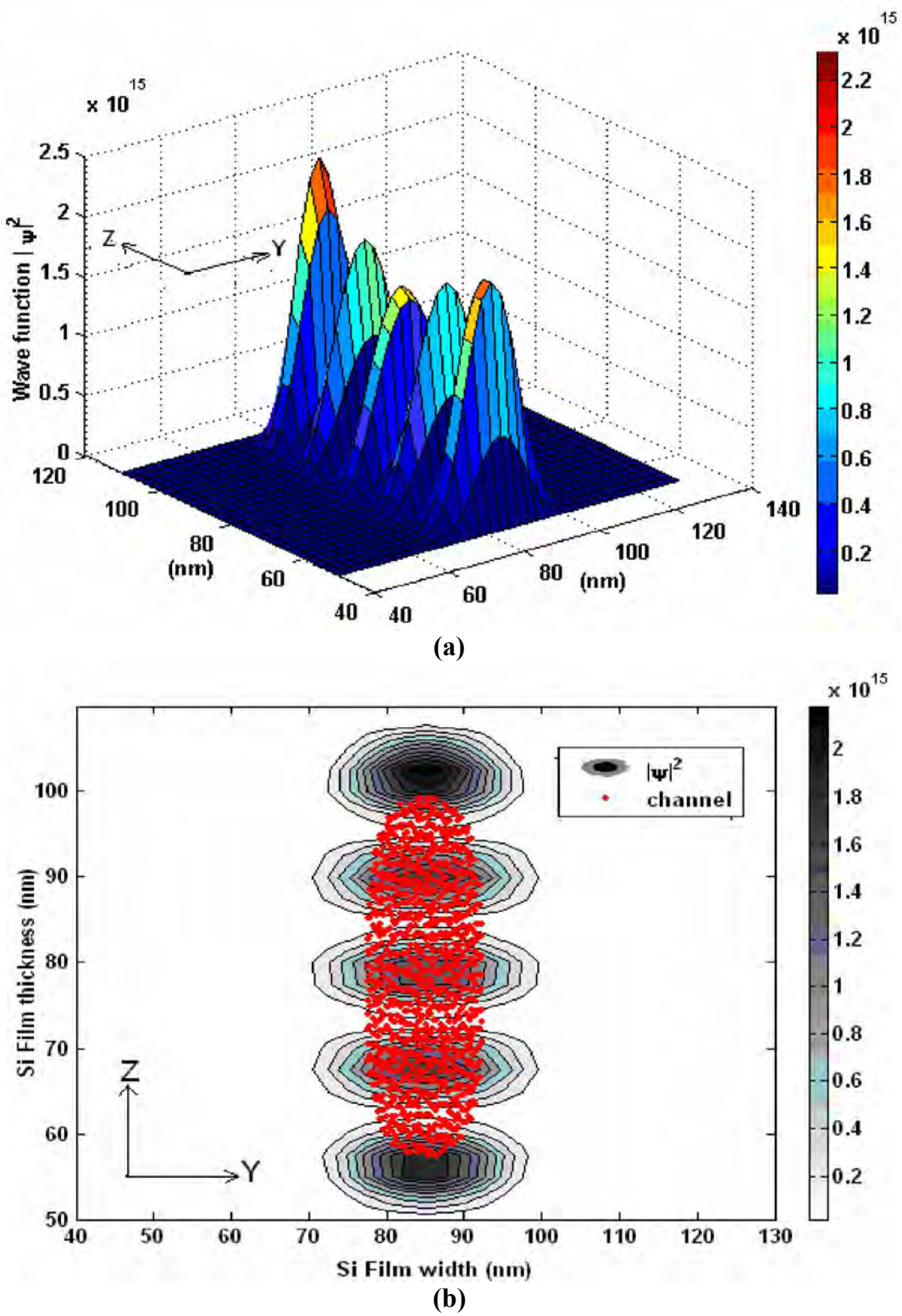


(a)



(b)

Figs. 3.18: (a) 3-D plot and (b) contour plot of normalized wave function corresponding to 4th eigen energy showing channel (red spotted region). Gate bias: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V; channel is at 0V.



Figs. 3.19: (a) 3-D plot and (b) contour plot of normalized wave function corresponding to 5th eigen energy showing channel (red spotted region). Gate bias: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V; channel is at 0V.

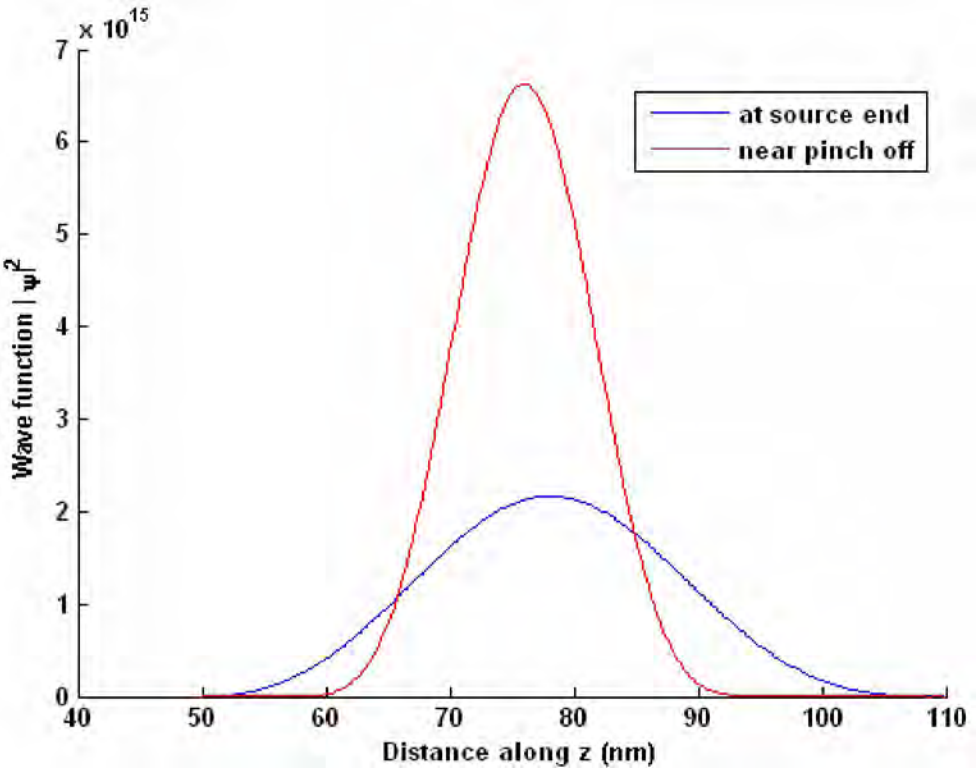


Fig. 3.20: Cross section view of normalized wave function corresponding to 1st eigen energy. Gate bias: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V.

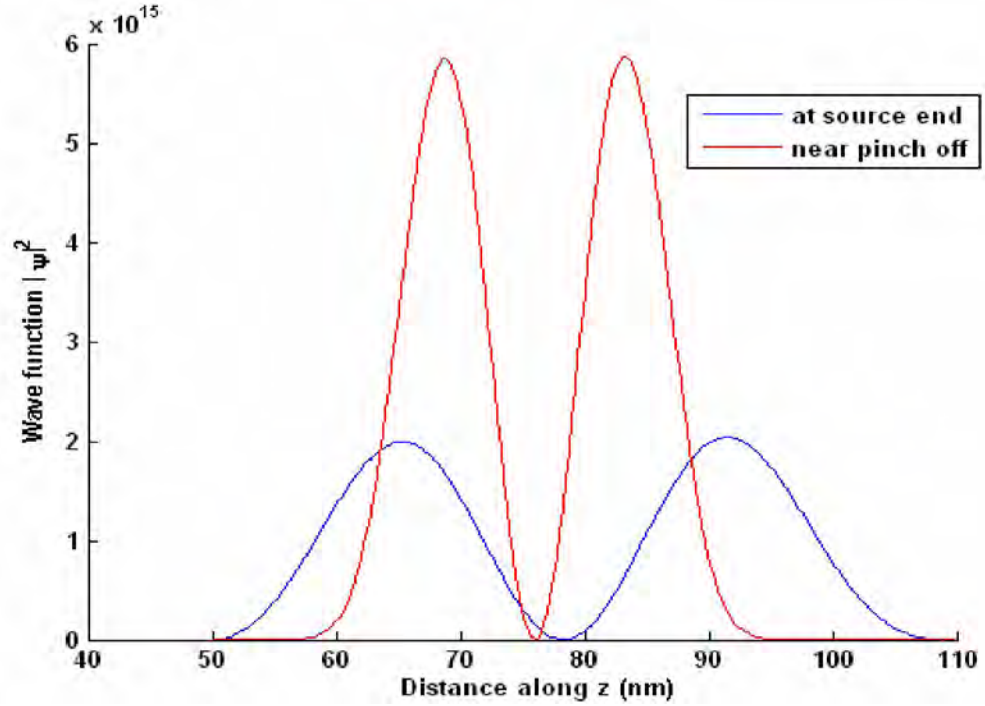


Fig. 3.21: Cross section view of normalized wave function corresponding to 2nd eigen energy. Gate bias: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V.

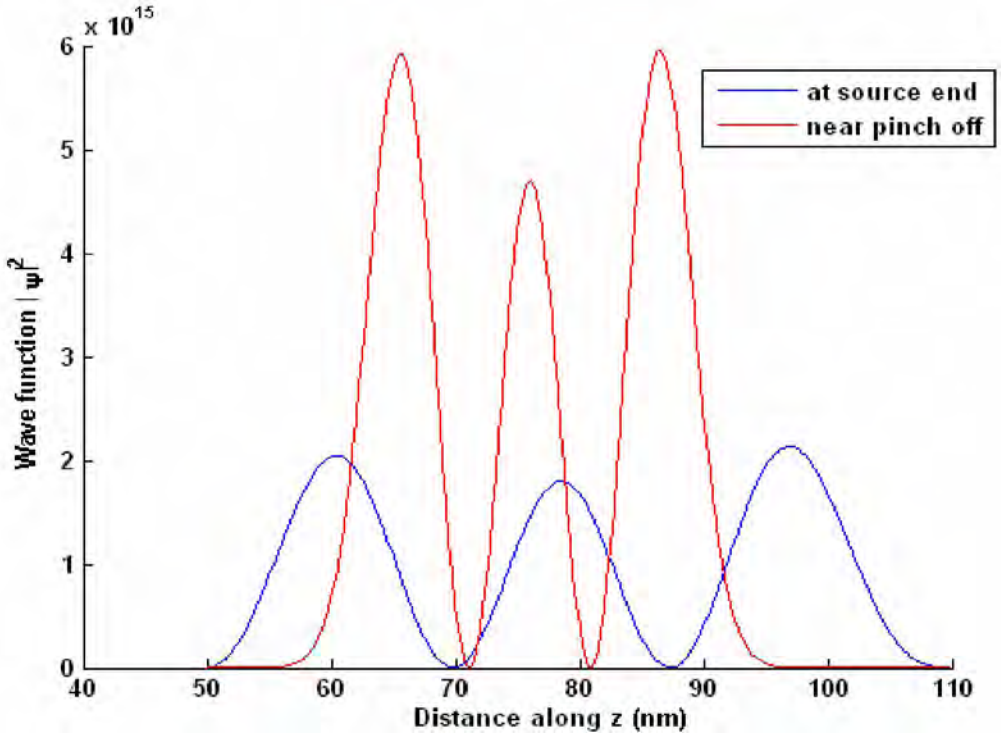


Fig. 3.22: Cross section view of normalized wave function corresponding to 3rd eigen energy. Gate bias: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V.

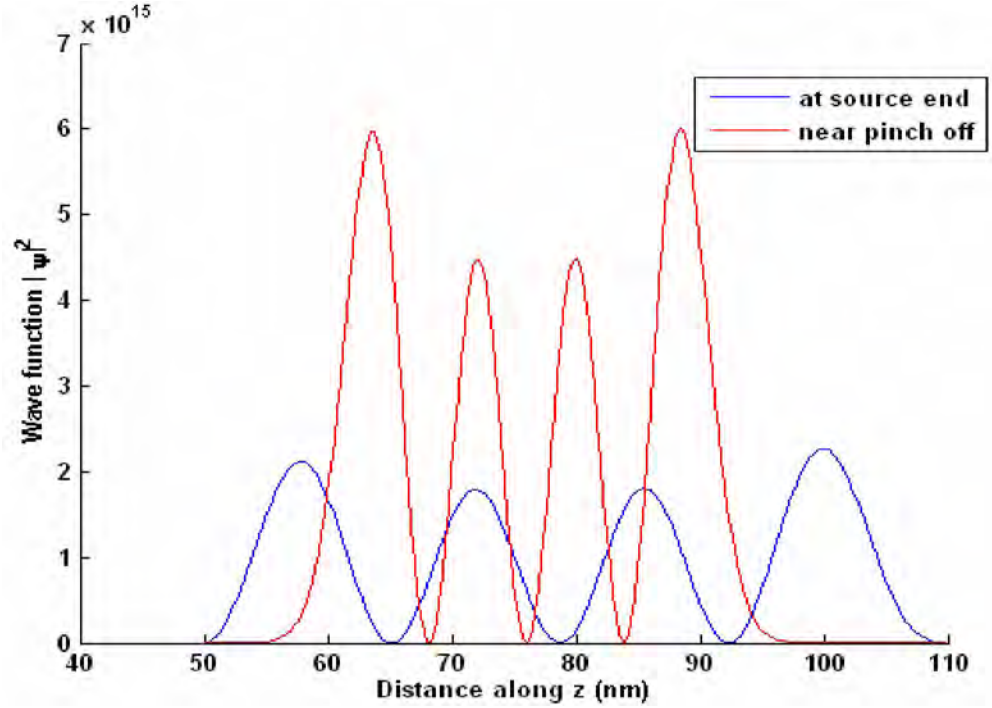


Fig. 3.23: Cross section view of normalized wave function corresponding to 4th eigen energy. Gate bias: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V.

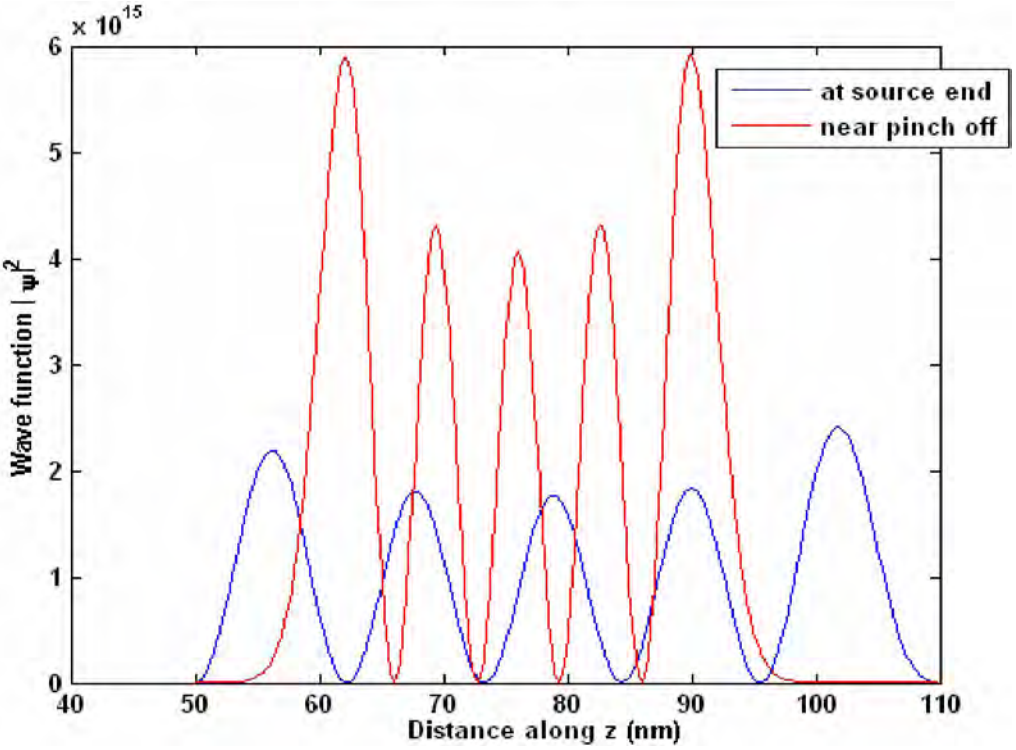


Fig. 3.24: Cross section view of normalized wave function corresponding to 5th eigen energy. Gate bias: V_tg = -0.2 V, V_bg = -0.2 V, V_jg1 = V_jg2 = 0.45V, Veff= -0.55V.

Fig. 3.20, 3.21, 3.22, 3.23 and 3.24 show that wave functions at the cross section near source end, corresponding to various eigen energy, change gradually as they appear at the cross section near pinch off. Hence, between any two subsequent cross sections, wave functions corresponding to an eigen energy remain almost similar and transmission coefficient can be calculated from subband profile using impedance approach.

3.4 Current-Voltage Characteristics

Using modified Tsu-Esaki [30] Equation given in Eq. (5), ballistic current is measured by mode-space approach [31]. Scattering throughout the channel is neglected. In modified Tsu-Esaki approach, for calculating ballistic current, carrier group velocity of a one-dimensional electronic wave propagating towards the drain/source through a certain subband i.e. v(E), density of states for that electronic wave i.e. D(E), Fermi-Dirac distribution function i.e. f(E) and Transmission coefficient i.e. T(E) are required.

Following figures show change of v(E), D(E), f(E) and T(E) with electron energy E. Fig. 3.25 shows change of carrier group velocity v(E) at source end with electron energy E for the first eigen energy at a given gate bias combination.

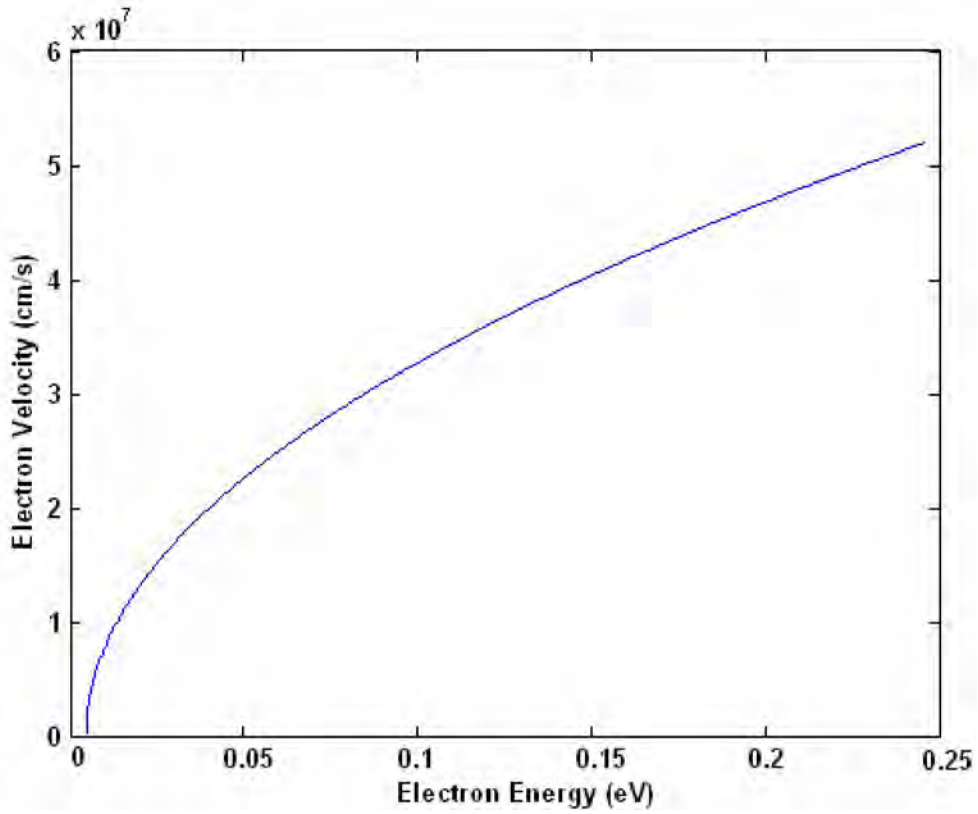


Fig. 3.25: Carrier group velocity v(E) at source end vs electron energy E, for first eigen energy.

Fig. 3.26 shows change of density of states D(E) at source end with electron energy E for first eigen energy at a given gate bias combination.

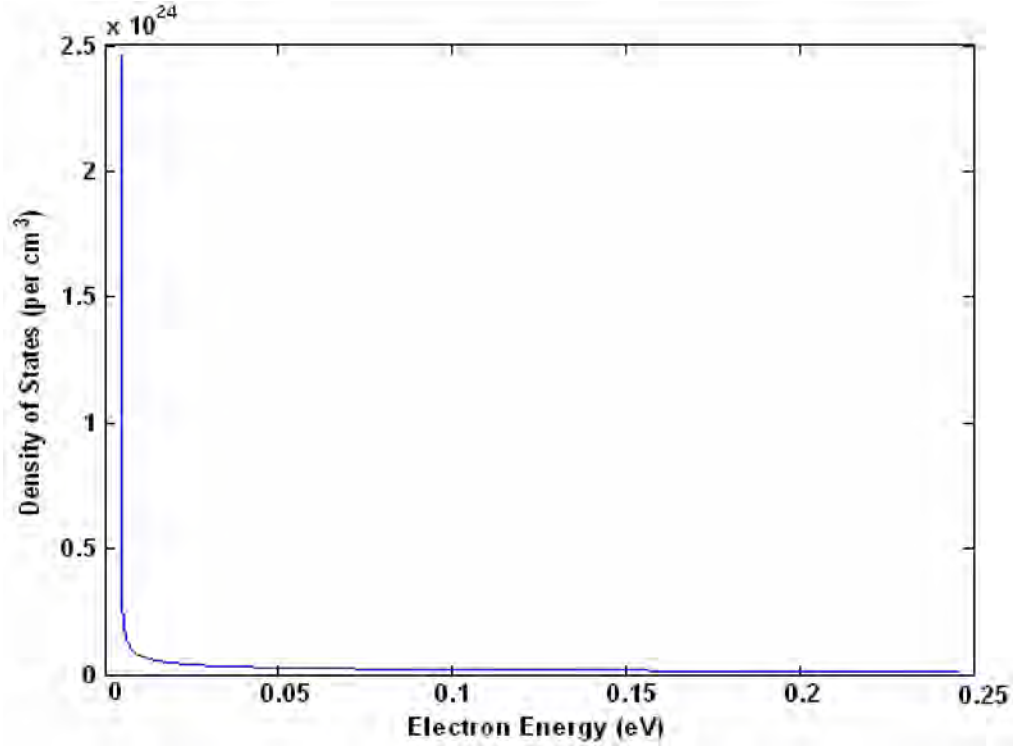


Fig. 3.26: Density of states D(E) at source end vs electron energy E, for first eigen energy.

Fig. 3.27 shows change of Fermi-Dirac distribution function i.e. f(E) at source end with electron energy E.

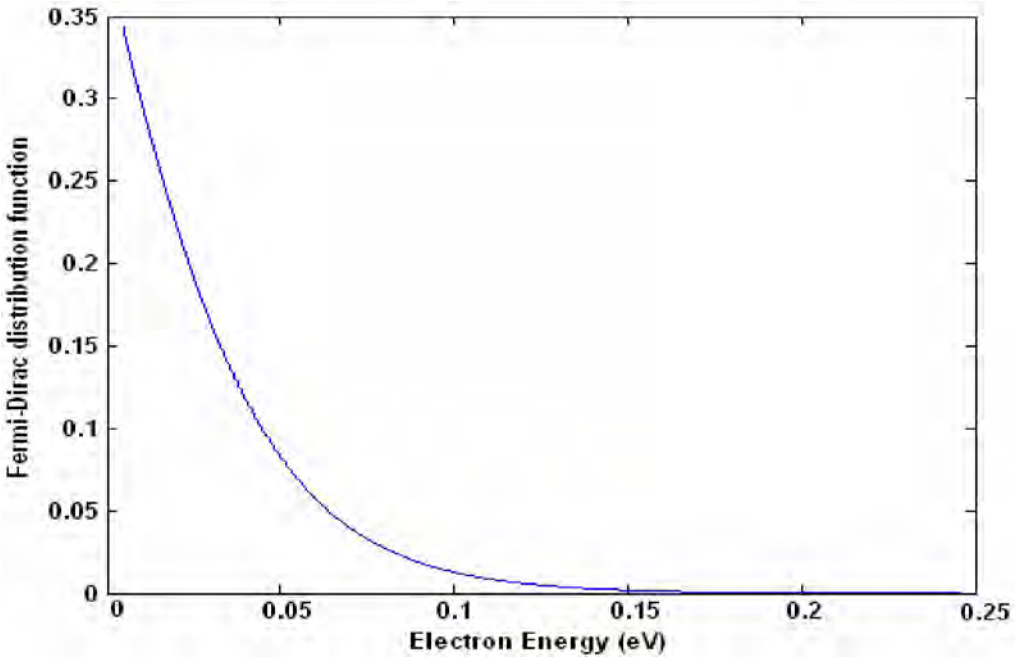


Fig. 3.27: Fermi-Dirac distribution function f(E) at source end vs electron energy E.

Fig. 3.28 shows change of transmission coefficient i.e. T(E) with electron energy E for first, second and third subbands at a given gate and drain bias combination.

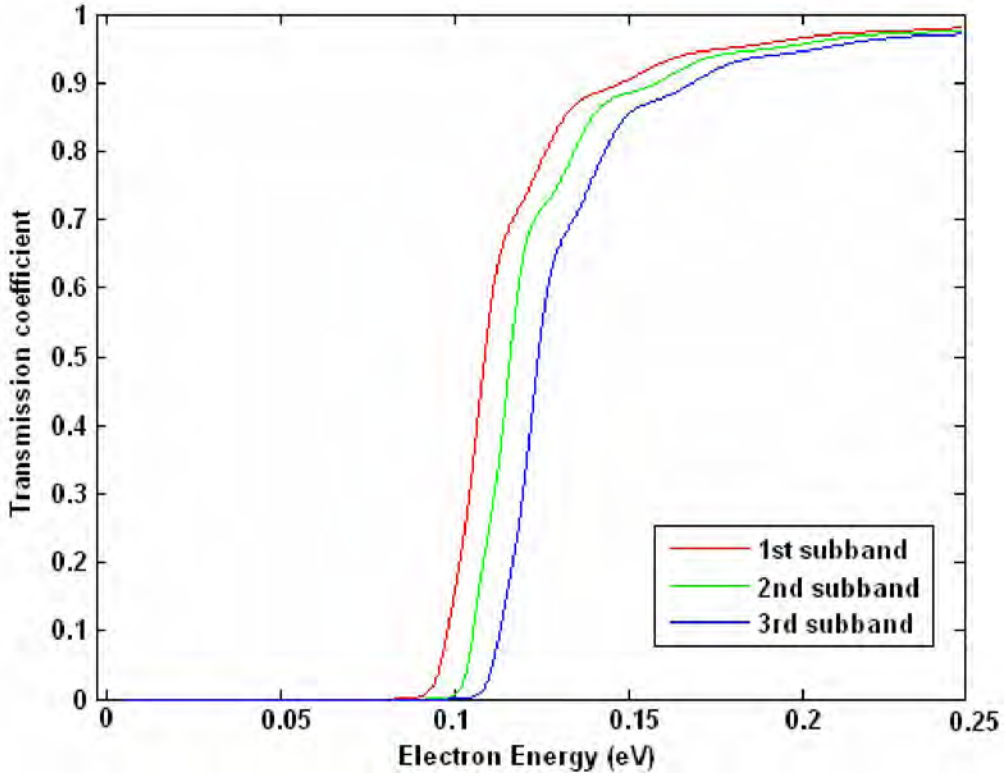


Fig. 3.28: Transmission coefficient i.e. T(E) vs electron energy E, for first, second and third subbands, with gate bias: V_tg = -0.15V, V_bg = -0.2V, V_jg1 = V_jg2 = 0.4V, Veff= -0.6V and V_D= 0.25V.

In Fig. 3.29 top gate bias is varied, while back-gate and junction gate biases are kept constant. It is found that with the negative increase in top gate bias, ballistic current reduces. Because the more negative the top gate bias the smaller is the channel cross-section i.e. the larger is the depletion region.

In Fig. 3.30 back gate bias is changed, while top-gate and junction gate biases are kept constant. Fig. 3.31 shows change of drain current with junction gate voltage, when top-gate and back-gate biases are kept constant. Fig. 3.29, Fig. 3.30 and Fig. 3.31 show multiple gate dependence of ballistic drain current in G^4FET.

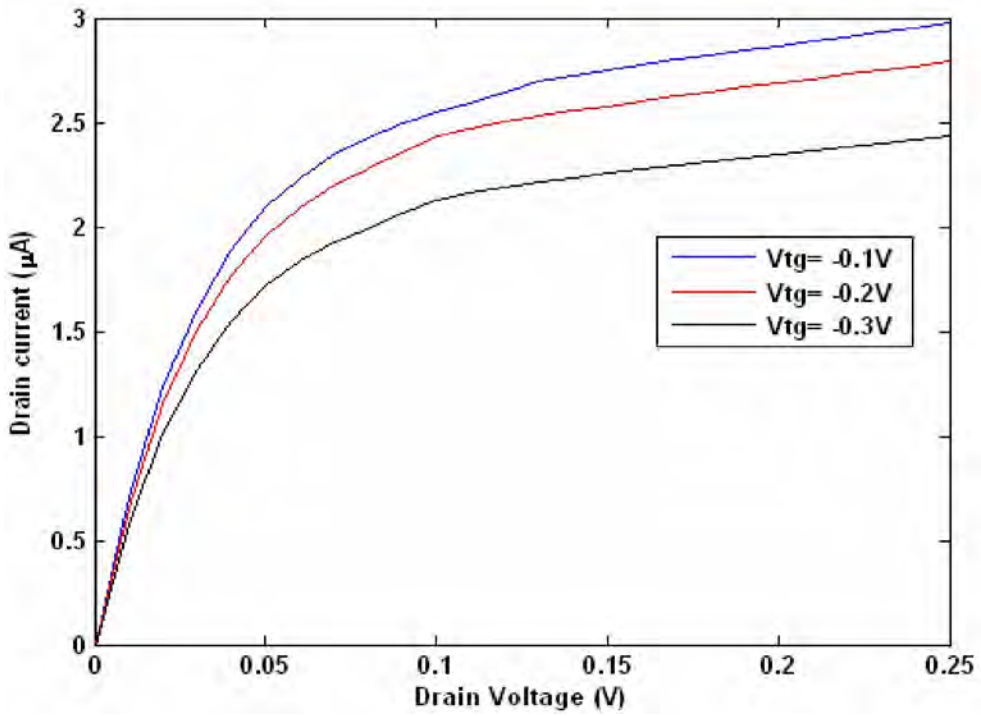


Fig. 3.29: Drain current vs. Drain voltage at different top gate bias while other gate biases remaining constant at V_bg= -0.2V, V_jg1=V_jg2= 0.4V, Veff= -0.6V.

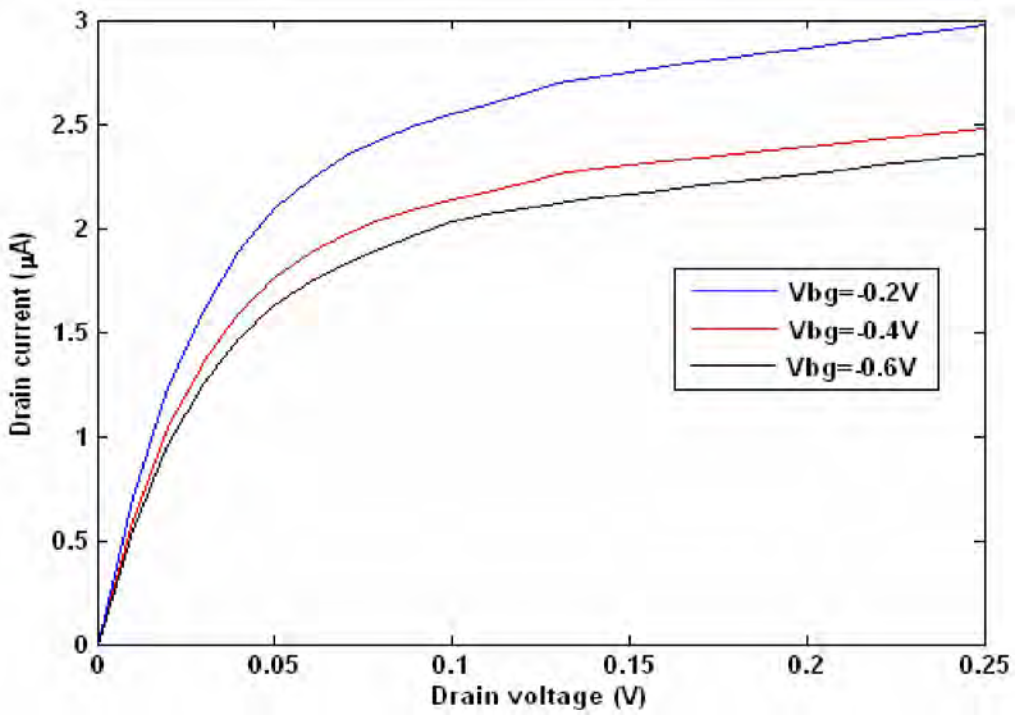


Fig. 3.30: Drain current vs. Drain voltage at different back gate bias while other gate biases remaining constant at V_tg= -0.15V, V_jg1=V_jg2= 0.4V, Veff= -0.6V.

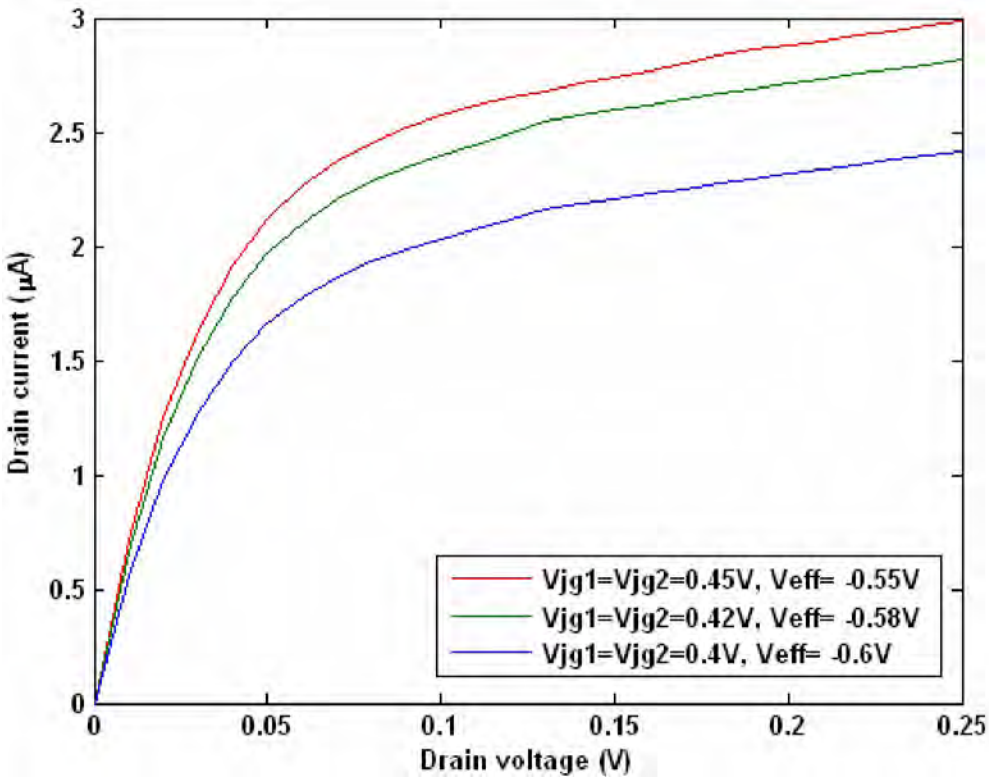


Fig. 3.31: Drain current vs. Drain voltage at different junction gate bias while other gate biases remaining constant at V_tg = -0.2 V, V_bg = -0.2 V.

Chapter 4

Conclusion

4.1 Summary

Two dimensional Poisson-Schrödinger equation is solved numerically in depletion all around (DAA) operation of n-channel four gate transistor (G^4-FET) by *finite element method*. Potential distribution is obtained by solving 2-D Poisson equation. The influence of different gate bias voltages on the location and size of the conducting channel is studied, which also includes fully depleted condition for certain gate bias voltages. The developed model is used to investigate the gradual change of the size of the conducting channel from drain to source, when drain is positively biased. It is also found that by applying appropriate bias voltages on the four gates, the conducting channel can be narrowed down to less than 20 nm yielding various new quantum mechanical effects in carrier transport like weak quantization effect.

Conduction band profile is studied and shallow n-well region is found. By solving 2D Schrödinger equation, eigen energy at various cross sections between drain and source, subband profiles from source to drain and wave function distribution are observed. Weak energy quantization is found by observing small energy difference (less than kT) between subsequent subband profiles and noticing wave function distribution extending beyond neutral n-well and into the depletion region. Using the outputs of physics based 2D Poisson-Schrödinger solver, a ballistic current-voltage model is developed by mode-space approach using modified Tsu-Esaki equation. Finally, effect of gate bias on current-voltage characteristics is investigated.

4.2 Suggestion for Future Research Works

With negative bias applied to all gates, this work is focused on a specific operation mode of the G^4-FET providing volume conduction and is called depletion-all-around (DAA) mode. Hence this work is confined to depletion-all-around mode of volume conduction and various characteristics are observed accordingly. If this ballistic current-voltage model is further extended to inversion region by applying sufficiently strong negative bias, the device performance and properties in DAA mode are remarkably affected by the presence of inversion layers under MOS gates because then both the junction gates get interconnected through the inverted silicon film.

In this work, effect of multiple gate bias on current-voltage characteristics is observed. Adjustment of various significant transport parameters such as threshold voltage, trans-conductance, sub-threshold slope, etc. related to a single gate, when the device is driven from one gate keeping the other gates at constant voltages can also be observed using the proposed current-voltage model.

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Appendix A

Flow Chart for I-V Characteristics Simulator Considering Quantum Ballistic Transport

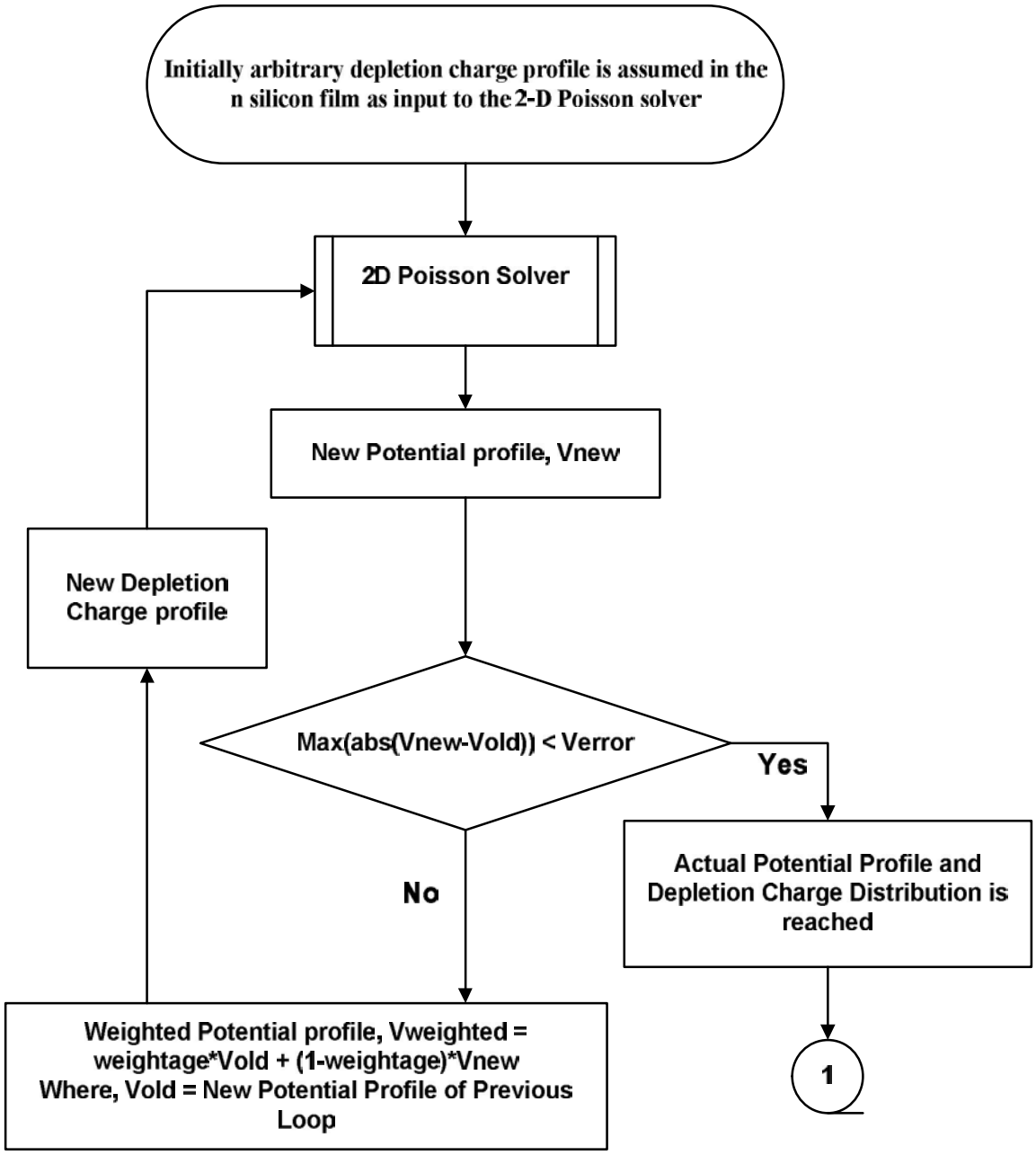

Fig. A.1 : Flowchart

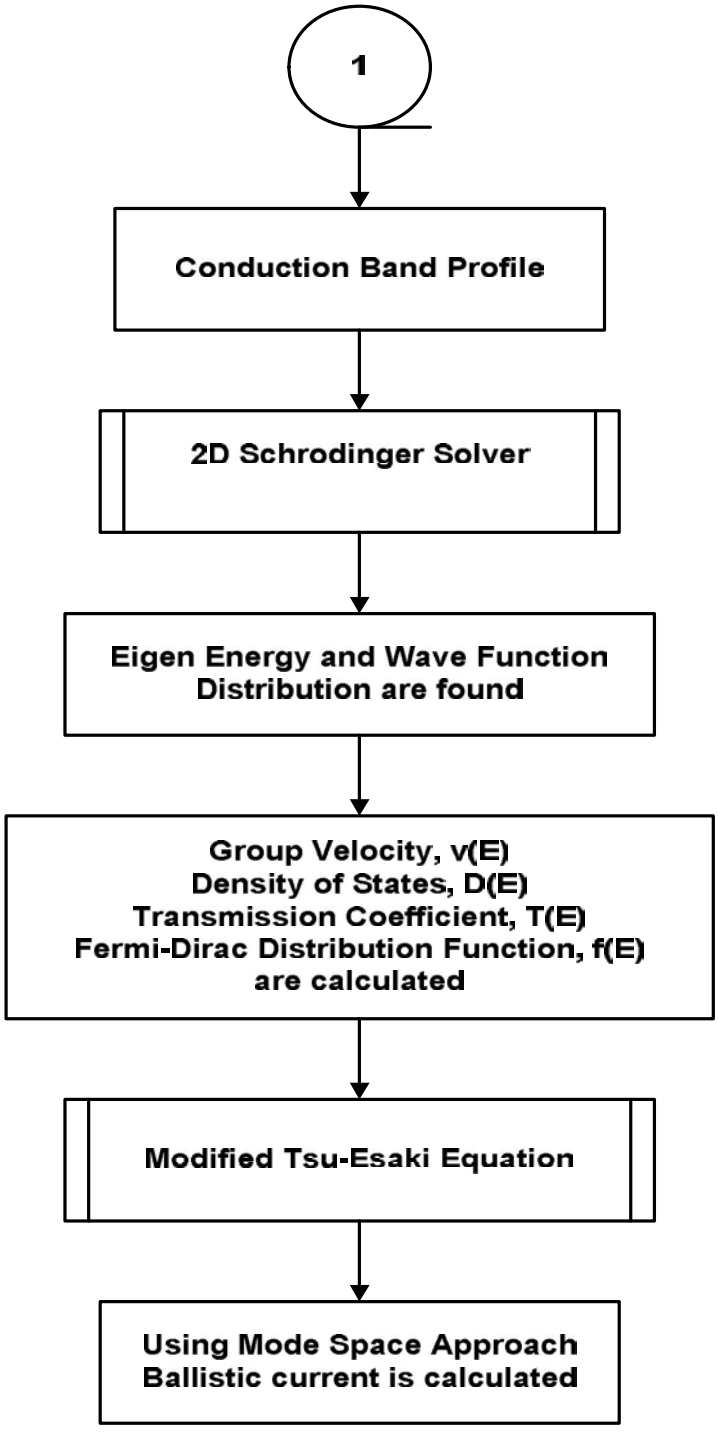

Fig. A.1 : Flowchart (Continued)