DESIGN AND OPTIMIZATION OF A FULLY INTEGRATED HIGH DATA RATE TRANCEIVER IN 90nm CMOS TECHNOLOGY FOR ON-CHIP UWB WIRELESS INTERCONNECT SYSTEM

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by

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The thesis titled "**DESIGN AND OPTIMIZATION OF A FULLY INTEGRATED HIGH DATA RATE TRANCEIVER IN 90nm CMOS TECHNOLOGY FOR ON-CHIP UWB WIRELESS INTERCONNECT SYSTEM**" submitted by S. M. Shahriar Rashid, Student ID.: 0409062238 P, Session: April 2009 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on October 30, 2011.

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_____

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Dedication

To my parents

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Acknowledgement

All praises and gratitude belong to almighty Allah, without whose consent nothing is achievable. This is He, who gave me enough physical and mental strength to invest in this thesis that was of prime importance for completing this work.

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Abstract

Modern submicron transistors are capable of offering unity gain bandwidths as high as hundred GHz. Still, circuit modules of next generation integrated circuits will not be able to utilize this high speed, if the parasitic issues associated with the interconnecting copper wires continue to increase as technology shrinks down. That is why; forthcoming ultra high speed ICs have to come up with a whole new interconnect systems replacing traditional copper interconnects. One of the approaches to overcome this limitation could be the use of on-chip wireless interconnection with integrated antenna. However, being sensitive to interference and multipath fading, this kind of short distance wireless data transmission necessitates the communication scheme to be carefully chosen. UWB topology, offering low power spectral density, has proved itself as one of the wise choices for this application. It has a lot more bright sides. Large bandwidth available for high speed data transmission, multiplexing capabilities, interference tolerances etc. are to name a few. TR-UWB (Transmitted Reference- Ultra Wide Band) version of this topology is gaining much interest in literature, especially for its simple transceiver architecture.

It this thesis, a number of RF circuits were designed, they are- square law up-conversion mixer, low noise amplifier, direct conversion folded mixer, low pass filter and comparator. The circuits were fully integrated i.e. no off chip circuit elements, in IBM 90 nm CMOS technology and were simulated both in Cadence Spectre & HSPICE. They were optimized in terms of speed, power, area etc. and were characterized thoroughly so as to investigate their viability of incorporating in the intended TR-UWB on-chip wireless interconnects systems. Finally, the circuits were assembled to form a complete system, included with on-chip integrated antenna pair to transmit and eventually to recover digital data where the system worked very successfully. A system level investigation was also carried on at the end to identify its overall performance limits. The maximum achievable speed of the system was found as 2.5 gbps with a minimum detectable receiving power level of -27 dBm. A new signaling scheme is also proposed to reduce the minimum

detectable power level to -33 dBm sacrificing about 1 gbps speed. The receiver burns only 40 mW power from a 1.2 V power supply and occupies 0.67 mm^2 area on silicon chip.

Therefore, overall performance of the system is outstanding and its commitment for being a viable replacement of traditional wired interconnects is really appreciating. In literature, there are only handful of circuit level designs of such intra-chip interconnects systems, which are capable of communicating random digital data wirelessly.

CHAPTER 1
INTRODUCTION

1.1 Motivation

The unity gain frequency (f_T) of modern submicron CMOS transistors are in around 100 GHz. But, this benefit is yet to be utilized in high speed ICs, because the parasitic issues associated with the traditional interconnects i.e. copper wire, limits the speed of their internal data transmission. This problem aggravates as the technology shrinks, because as the process scales down, the width of the metal wires also follow giving rise to an increase in wiring resistance. Moreover, smaller transistors need less space to create circuits that need more number of metal layers to account wiring difficulties. In other words, metal wires are coming closer ending up to larger parasitic capacitances. Thus, RC delay is waxing for both reasons and the consequence is the data transmission speed limitation to severe extent [1-2].

The delay of interconnecting wires can be quantified in terms of time of flight (TOF), which is defined as the delay experienced by a signal as it propagates through a wire of unit length. This TOF can be as high as 8 ps/mm. In comparison, gate delay of a NAND Gate of fan out 3 is about 30 and 12 ps in 130 nm and 50 nm technologies respectively [3].

Now, consider the edge dimension of modern microprocessors, which is in between 20 mm to 30 mm. These ICs need long interconnections between their arithmetic logic units (ALU), registers, cache storages etc. So, TOF of those long interconnect would range from 125 to 250 ps, meaning- speed of those microprocessors has to be less than 8 GHz. And this delay is 2 to 20 times of the gate delay of modern submicron technologies [4].

More alarming, limitation of interconnecting speed will be the bottleneck in the emerging age of nano-transistors, when several hundreds of GHz bandwidth will be available, if this issue is not addressed properly. So, fending off the interconnecting delays will be one of the major challenges in future ULSI technologies. That is why; this problem invokes a lot of research in parallel with technological advancement and a corner edge solution is to be invented.

1.2 Overview of the Interconnects:

History of interconnects in ICs started with aluminum wire. Almost all the transistors and modules of the ICs in 1950s, when the technology was in it's infancies, were connected by aluminum wires. Later, as the process advanced, increased resistances of those wires due to scaling down began to bother. Peoples tried to overcome the problem by using wider wires or by using repeaters to connect modules. But, the first technique increased capacitance in long wires and second one yielded when the total delay of large number of repeaters over long distance summed up to be inconvenient. These factors put engineers in quest of alternative connecting metal like copper.

Copper wires were lucrative because of it's lower resistivity (60% of Aluminum). However, what factors took it so long to come in to ICs includes- difficulties of fabrication, diffusion through silicon, formation of silicon dioxides and it's toxicity. Fortunately, most of those problems could be avoided after the incorporation of complicated and costly copper damascene process.

Today, 40% improvement of resistivity of copper wires over aluminum is no longer sufficient for large modern ICs in submicron technologies, especially which aspire for operation in a speed of tens of GHz. So, this is the time to invent next generation interconnect techniques, that will not only reduce the interconnection delay considerably, but also will be simple, will occupy less space, will be usable both in intra-chip and inter-chip applications and will be cheap as well.

In response to this urge, the approaches proposed so far include:

1. Three Dimensional (3D) Integration
2. Optical Interconnect
3. RF/Wireless Interconnect

Let us put some light on their pros and cons.

1.2.1 Three Dimensional (3D) Integration

Usually, in ICs, transistors are created in a single layer i.e. in 2D. Three dimensional integration proposes that, transistors will be formed in two or more layers, so that, more number of modules can be accommodated in small space and thus, long lateral interconnect could be avoided [5].

This technique in effect implies a whole new fabrication process, that will be difficult to implement since the foundry will be complicated and costly. Again, incorporation of more than four layers would be impractical. Finally, transistors of upper layers will find difficulties in heat dissipation process. For these reasons, this scheme has not received much attention yet.

1.2.2 Optical Interconnect

Optical interconnect could be one of the possible solutions [6]. Concept of this technique is depicted in Fig. 1.1. Merits of this approach are- several THz of bandwidth will be available in optical carrier signal and optical propagation velocity is much higher than the signal propagation velocity of electrical interconnects. In fact, optical interconnect could be the next generation interconnects unanimously, if was not for the following demerits:

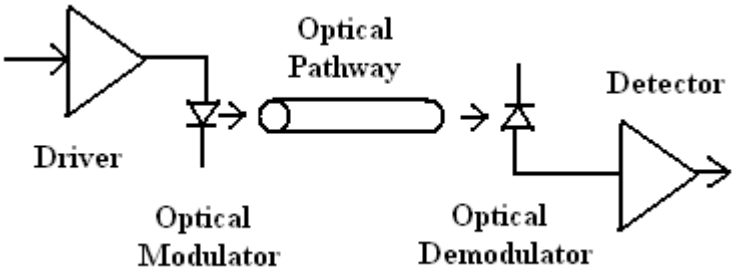

Figure 1.1: Transceiver architecture of the Optical Interconnect

Although, the optical bandwidth is enormous, but the limitation would be imposed by the slower transmitter, modulator, demodulator and receiver circuitry. Next, incorporation of active pathway in chip is difficult, transceiver circuits would be power hungry and space consuming, above all, it could not be fabricated without complex and costly III-V foundry. Still, peoples are working to make the process feasible [6].

1.2.3 RF/Wireless Interconnect

RF and wireless interconnect is relatively a latest idea that is getting attention in literature as one of the promising savior of speed limitation problem of the interconnects in future generation high speed ICs [7]. This technique will be using on-chip integrated antennas for intra-chip and inter-chip wireless data transmission at high speed [8-9]. A block diagram is shown in Fig. 1.2, where a transmitter (Tx) is transmitting clock signal and four receiver (Rx) modules are receiving. [7] used this scheme for high speed clock distribution.

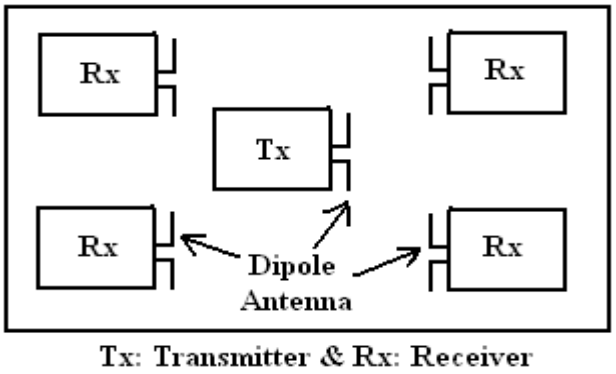

Figure 1.2: Block diagram of a typical RF/Wireless Interconnect

In this work, we chose this method of data transmission because of several other advantages those will be discussed in the next section.

1.3 Why do we prefer RF/Wireless Interconnect

RF/Wireless interconnect will exchange data wirelessly by means of RF signal. That is why, unlike optical interconnect, it will not require complex fabrication process like those for active guiding medium or for III-V device on silicon chip. This will make the transceiver compact and cheaper. Power dissipation will be within reasonable limit as well.

Next, similar to optical interconnect; bandwidth of this scheme is limited only by the delays associated with the transceiver circuits, not by the channel itself. So, it has inherent capability of supporting multiplexing and multiple access topologies like FDMA and CDMA, which might enhance its data transmission ability by manifolds. Interference, crosstalk etc. will also reduce dramatically.

Several other achievements, such as, low power spectral density i.e. low interference, wider bandwidth, simple transceiver architecture, thus viable to be fully integrated on silicon chip and so on, will be annexed if UWB (Ultra Wide Band) communication technique is adopted [10-11].

Therefore, to us, this simpler methodology could be the future generation high speed interconnects for ICs, if it gets proper attention and research.

1.4 Current State of the Problem

First of the challenges in this arena was to design fully integrated on-chip transmitter-receiver antenna pair for RF/Wireless interconnect system, when the proposition was in its embryonic state in 1990's. Design of some good antenna pairs can be found in [8-9]. They also demonstrated the feasibility and competence of those integrated antennas on silicon chip. There were other works like [5], [13] who studied the merits and demerits of this technique.

Later, peoples were interested in UWB transceiver architecture for these kind of short distance communication due to its innate advantages discussed earlier. [10-11] and [14-16] studied the signal and system in depth. They also proposed a few feasible communication and transceiver topologies. [17-21] are the recent works in this field who investigated signal propagation loss, leakage loss, interference, fading, scattering, BER etc.

But, complete integrated RF/Wireless interconnects or UWB RF circuits designed especially for these kinds of on-chip wireless interconnect system are yet to appear in literature. The best that can be found is- distribution of periodic signal like monolithic clock within ICs, such as that in [7]. Those designs are inapplicable for random data streams. Apparently, incorporation of RF circuitry in those systems is still to be. Receiver front ends for such wireless applications are designed in [22-23], but are partial. In fact, a complete on-chip wireless interconnects system with UWB transmission has not showed up yet. Therefore, this is our opportunity to design them to help the system incarnate.

1.5 Thesis Overview

Designing a series of high frequency circuits with short channel devices is very difficult because of low trans-conductance per unit current of the transistors, low quality factors of the energy storage elements, short channel effects, parasitic elements, matching issues to name a few. In this thesis, a few RF circuits will be designed in IBM 90 nm CMOS process. So, being involved with short channel devices, all the aforementioned difficulties can be expected to be present.

At first, a square law up-conversion mixer will be designed for the transmitter with improved matching technique which will elevate the lower frequency signal, to K-frequency band (above 20GHz). This frequency up-lifted TR-UWB signal will be transmitted and subsequently will be received by a pair of on-chip integrated antenna. The system will be optimized so that the signal strength at the receiving antenna is well above the minimum detection level.

Then a low noise amplifier (LNA) will be designed and will be optimized in terms of power gain, noise figure, power consumption and at the same time in terms of area by reducing the number of on-chip inductors- those are major area occupying elements in silicon chips.

Next, A direct conversion folded mixer will be annexed to the LNA. Both the current pushed and voltage fed folded mixers will be simulated and their features will be evaluated. An inter-stage matching will be incorporated to merge the LNA with mixer that will help warding off using separate LNA and mixer. Fruition of this clever technique will be less power, low noise, reduced number of on-chip inductors e.g. saving of chip area, simpler architecture, thus better reliability and so forth. The system will be characterized in frequency domain, as well as from linearity standpoint and then time domain simulation will be invoked to confirm the successful detection of transmitted 5gbps bit streams by BPSK and DPSK.

The system will be re-designed to detect TR-UWB pulses. A new TR-UWB modulation technique will be proposed for the case when the digital circuits of transmitter and receiver will be slow to process excessive high speed data streams. A comparator will be designed as well to enrich the detected binary signals and thus for retrieving the transmitted information bits.

Circuits will be designed in HSPICE, fully integrated in IBM 90nm CMOS technology e.g. no external circuit elements and then will be assembled in Cadence Spectre for complete chip level simulation. After optimizing the system up to satisfactory level, layout will be drawn for estimating the area budget of the system on chip.

1.6 Layout of the Thesis

This thesis will consist of **Eight** chapters. **Chapter 1** introduced the topic, mentioning the challenges and problems of the next generation ULSI technology, what are the techniques under research to remain in the technology roadmap, what are their pros and cons etc. This chapter also discussed what was the motivations in preferring on-chip wireless interconnect with UWB communication technique. An overview of the literature was presented to give an idea about the current state of the art. And lastly, the objective and methodology of this thesis work was outlined.

Chapter 2 will present the transceiver architecture which is to be implemented. This chapter will discuss on how the UWB signals will be generated, how the digital signal will be modulated, what are the issues involved in transmitting those signals through the silicon channel, how the received signal will be amplified, how they will be demodulated etc. The benefits and shortcomings of the scheme will also be included in this chapter.

Chapter 3 will explain the design of a square law up-conversion mixer after mentioning why it is needed in the transmitter. This chapter will show the design steps in detail that will include an improved input-matching technique which makes this circuit superior comparing to the other mixers of same topology of literature. Time domain response of the circuit will be demonstrated after characterizing the circuit thoroughly.

Chapter 4 will discuss on designing the low noise amplifier (LNA) for the receiver. After mentioning the design objectives, this chapter will describe how the LNA could be optimized in terms of gain, power dissipation, input-output matching and space requirement. What features had to sacrifice in return will also be noted in this chapter. Layout of the LNA will be included to find out the area requirement.

Chapter 5 will describe the design of fully integrated direct conversion mixer. This chapter will mention what types of mixers are available in the literature, why they need to be optimized before being used in this application and then, will explain how those limitations were addressed in this work. After that, two types of feeding technique to the mixer, namely- current pushed and voltage fed, will be analyzed, their relative merits will be compared and then the mixer will be merged with the LNA designed in chapter 4. Thus the receiver front end will consist of a single circuit, which will perform the functions of both LNA and Mixer. This circuit will be optimized in frequency domain as well as in time domain. Finally, the circuit will be used to detect 2gbps bpsk and dpsk signals. Layout of the circuit will also be given.

Chapter 6 will demonstrate how the receiver front end of chapter 5 was re-designed to detect the UWB signal successfully. A new technique will be incorporated in the circuit that will help avoiding otherwise bulky and power hungry circuits of the state of the art. This circuit will be used to detect the UWB transmitted signal and will be compared with the ideal scenario depicted in chapter 2. Then, a new TR-UWB modulation method will be introduced in response to a practical difficulty. Merits and demerits of the

circuit and the modulation technique will be investigated. At last, area budget of this receiver front end will be estimated from the layout.

Chapter 7 will be comprised of the design of a CMOS comparator for the regeneration of high speed digital bit streams, detected in chapter 6. The circuit will be explained and its performance will be evaluated. This chapter will discuss on a basic limitation of designing such circuits in modern sub-micron CMOS technologies like IBM 90 nm Process- that was the foundry used throughout this work.

Chapter 8 will conclude the thesis work summarizing and evaluating them judiciously. Suggestions for the future works required to finish the design of complete UWB on-chip wireless transceiver will also be included in this chapter.

CHAPTER 2

UWB ON-CHIP WIRELESS TRANCEIVER ARCHITECTURE

2.1 Bright Sides of the UWB Communication

Merits of the UWB communication was mentioned briefly in previous chapter. First, its large bandwidth can support data transmission in very high speed. From time domain standpoint- larger the bandwidth, shorter the pulse duration. That means, more data can be transmitted over the same period of time using these sharper pulses. This represents the main idea of the high speed communication, since pulse width has to be briefest possible if highest possible communication speed is to attain. However, excessively large bandwidth can not be obtained because of the practical issues related to the transceiver circuits.

Secondly, power spectral density (psd) of a signal reduces as its bandwidth increases, because the signal power is distributed over the whole bandwidth. That is why; psd of the UWB signal is very low and so is less likely to interfere with other communication channels. Thus provision for multiplexing and multiple access such as FDMA or CDMA is ensured. Also, the effect of multipath fading, colored noise etc. can be expected to be minimum. Moreover, this scheme is especially suitable for these kinds of short distance communication, because the low psd signal will not be able to travel much longer out of the chip and will not interfere with the regular terrestrial communication signal, which would violate the FCC (Federal Communications Commission) rules.

Third, as the UWB signals themselves are of high frequency, they do not need the assistance of any other high frequency carrier for modulation. So, modulation techniques of the UWB signals are easier. In fact, UWB communication is sometimes referred as carrier less communication. These short duration pulses can be modulated using simpler

techniques like PAM (Pulse Amplitude Modulation), PPM (Pulse Position Modulation), OOK (On Off Keying) etc [10-11], [14], [16]. However, in our application, we would prefer TR-UWB (Transmitted Reference- UWB) modulation method, where at least a couple of pulses will be transmitted for each bit- one will serve as the reference pulse for synchronization, no other information, while the other will carry the information about the bit i.e. '1' or '0'. So, no bulky and power hungry synchronizing circuits like PLL (Phase Locked Loop) will be needed. In other words, the system will be self synchronized [15].

Lastly, the transceiver architecture will be simplest possible, as there is no need for synchronization, carrier generation i.e. local oscillator, frequency up or down conversion etc. Again, simple modulator in turn implies a simple de-modulator. All that will be needed in the receiver is a simple correlator, consisting of only a few circuitries. There will be a number of achievements in return- reliability, easy design, less power, limited footprint etc. are a few of them. In fact, design of high frequency circuits is always troublesome and this simple architecture will save us from designing too much of them. Next section presents such a transceiver system which enjoys almost all the benefits mentioned above.

2.2 The On-Chip UWB Wireless Transceiver Architecture

Block diagram of the on-chip UWB wireless transceiver is given in Fig. 2.1 and the transmitted TR-UWB signal is shown in Fig. 2.2.

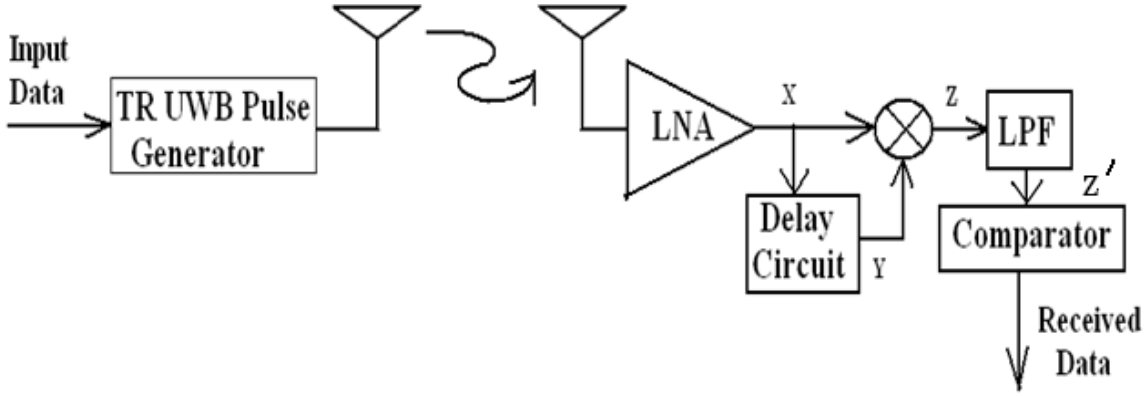

Figure 2.1: Block diagram of the on-chip UWB wireless transceiver

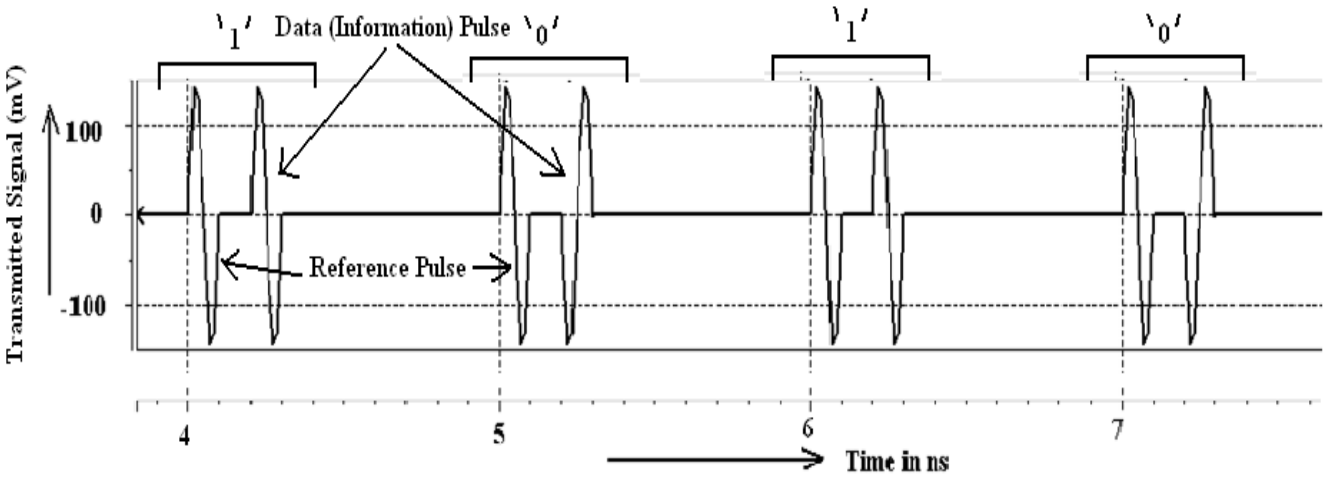

Figure 2.2: Transmitted TR-UWB Signal

In Fig. 2.2, the transmitted TR-UWB signal consists of a couple of pulses for each bit. The leading pulses are always in the same phase, known as reference pulse that is required for synchronization, will be described later. The trailing pulse is the information signal, because it is in the same phase or out of phase with respect to the reference pulse, denoting '1' and 'o' respectively.

Now, in Fig. 2.1, the transmitter is necessarily a TR-UWB pulse generator, that will generate streams of TR-UWB pulses depending on the input data. Its internal structure can be shown like that in Fig. 2.3 and the corresponding signals at all the nodes are given in Fig. 2.4. Those figures are self explanatory, so let us avoid unnecessary details.

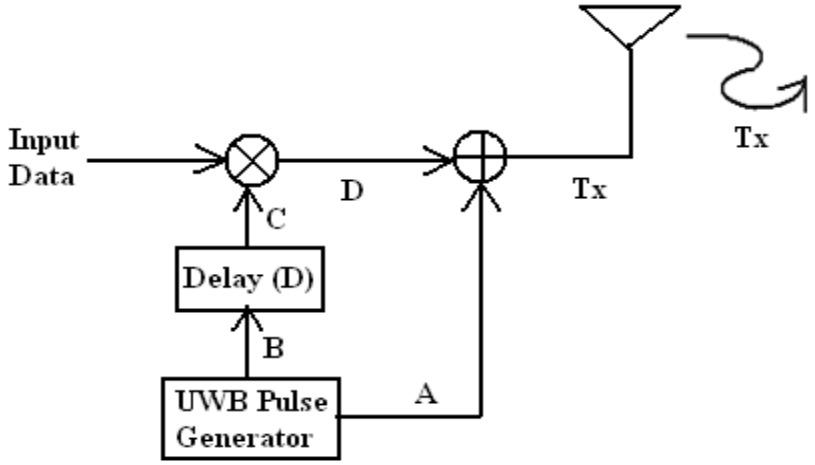

Figure 2.3: Internal block diagram of the TR-UWB pulse generator

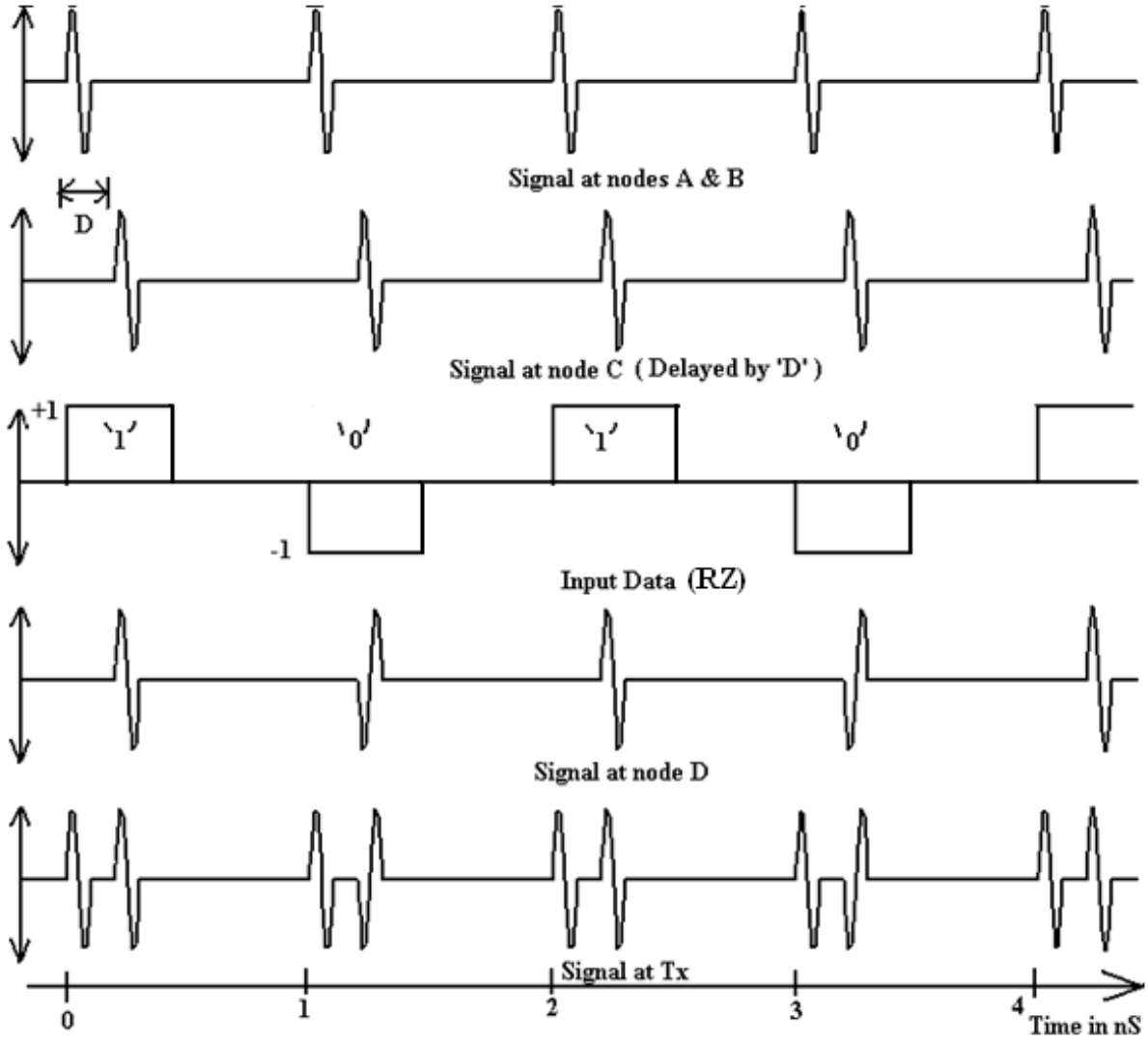

Figure 2.4: Signals at nodes of Fig. 2.3

However, instead of using separate pulse generator, delay element, multiplier and adder as can be found in Fig. 2.3, the whole transmitter circuit can be designed only by a single mixed signal circuit, where the input will be digital bit streams and the output will be TR-UWB pulses of Fig. 2.2. Such one can be found in [24].

Now, the signal received by the receiving antenna will have to be amplified, because it will experience much attenuation on its way through the silicon channel. This is the job of the low noise amplifier (LNA). LNA, being the first element of the receiver,

plays a very important role on the overall performance of the receiver, because according to Frii's formula, overall noise figure of any receiver like that of Fig. 2.5 is given by:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots \quad 2.1$$

Where, 'F' and 'G' are the noise factor and the gain of the corresponding blocks.

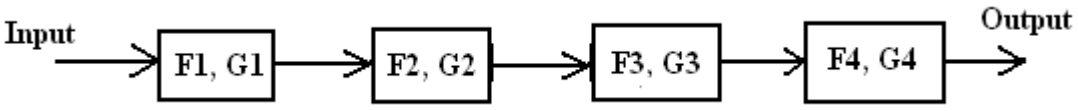

Figure 2.5: Block diagram of a typical receiver.

Usually, the first blocks of the receivers are an LNA. So, $F_1=F_{LNA}$ and $G_1=G_{LNA}$ are the noise factor and the gain of the LNA. In that case, (2.1) reduces to:

$$F_{receiver} = F_{LNA} + \frac{(F_{rest} - 1)}{G_{LNA}} \quad 2.2$$

Where, F_{rest} is the overall noise factor of the rest of the receiver after the LNA. Both from (2.1) and (2.2), it is clear that, total noise factor of the receiver will be minimum if F_{LNA} is minimum and G_{LNA} is maximum. This is the main reason, why LNA is one of the most vital elements in the receiver. However, designing such LNAs for high frequency UWB applications is very complicated because of other constrains such as- low trans-conductance per unit current of the transistors of the sub micron technologies, low quality factors of the energy storage elements, necessity of wide band input-output matching, area and power budget etc. Therefore, careful design and judicious optimization is obvious for getting a satisfactory overall performance of the receiver.

The detection of the received signal by the receiver of Fig. 2.1 is depicted in Fig. 2.6. The amplified signal of node X is delayed by 'D' in node Y and then is multiplied to get the signal like that in node Z. Signal at node Z $'$ is obtained after removing the high frequency components by the LPF (Low Pass Filter) i.e. after integration. Finally, the comparator regenerates the transmitted RZ bit streams and thus the input data (RZ) of Fig.

2.4 are retrieved. This is how this UWB wireless transceiver will work without the assistance of any explicit carrier or synchronizing circuit. Note that, a sample and hold circuit could be incorporated in between the LPF and comparator if the data were NRZ instead; that would sample the signal at node Z′ once in every bit.

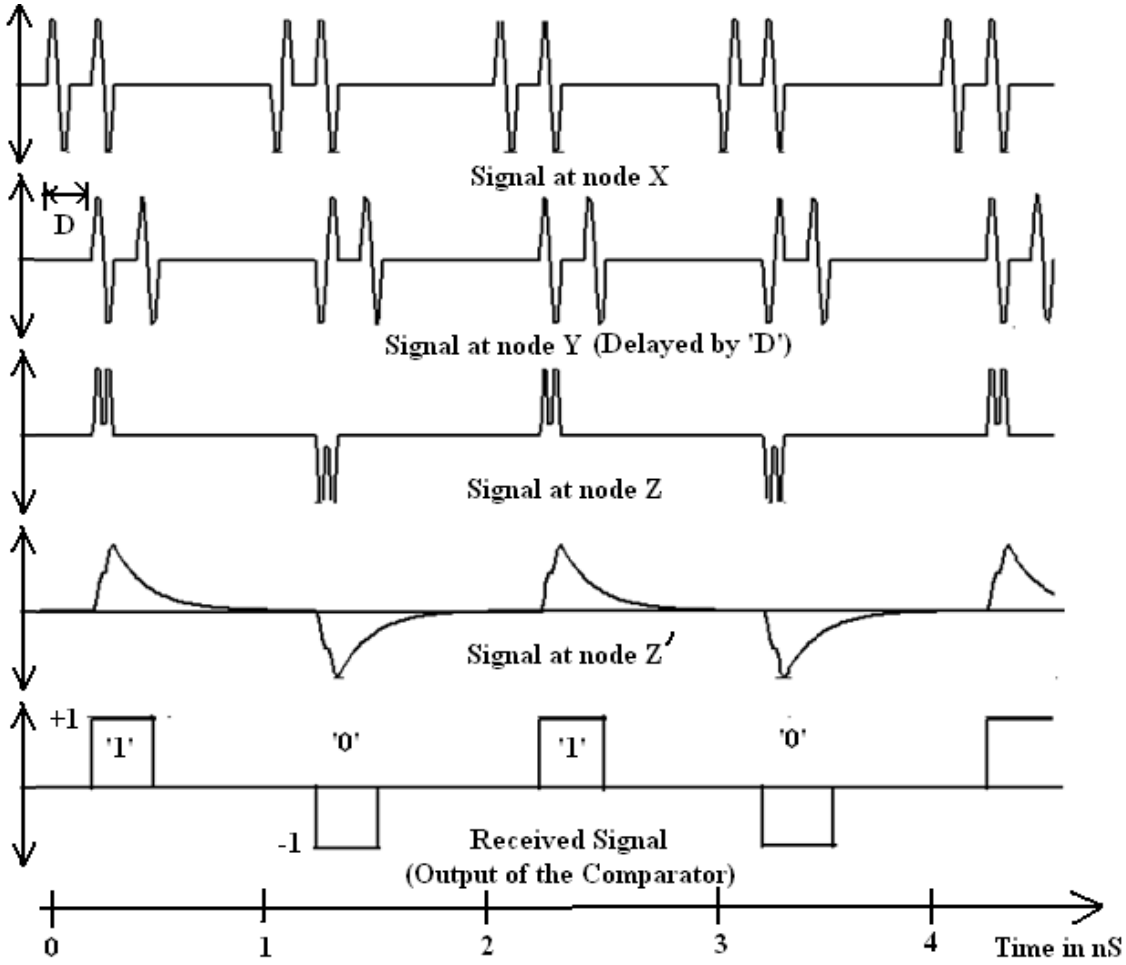

Figure 2.6: Signals at the nodes of the receiver of Fig. 2.1

In this transceiver architecture, one should expect that, the high frequency UWB signal will not appear after the LPF. Knowing that, designing RF circuits is a tedious job; this system would appear especially attractive, because only a few circuits (LNA, Delay Block, Mixer and LPF) have to work with those RF signals. Nevertheless, as mentioned earlier, a complete receiver like that of Fig. 2.1 is not yet reported. In subsequent chapters, we would like to explain how we tried to design the system in circuit level to detect the transmitted data conveniently.

CHAPTER 3

DESIGN OF A DOUBLE BALANCED SQUARE LAW CMOS FREQUENCY UP-CONVERSION MIXER FOR THE TRANSMITTER

When the TR-UWB pulse generator of the transmitter of Fig. 2.1 was being designed, it appeared that, involved with digital signal, more than a few GHz speed in this 90 nm technology would not be available due to the signal integrity constraints and compounded by the non-ideal effects of the devices. On the other hand, the antenna pair works in around 20 GHz that necessitated the incorporation of a frequency up-conversion mixer in between the pulse generator and the transmitting antenna.

This chapter will mention the design objectives of the up-conversion mixer for the transmitter. Then, the reason of choosing square law topology will be discussed, together with its limitations. A square law up-conversion mixer will be designed next with a new input isolation technique which will eliminate the problem of this topology in high frequency applications. The circuit will be analyzed thoroughly in frequency domain as well as in time domain. At last a transient simulation will be carried on to up-convert a 1 GHz sinusoidal signal to 20 GHz and then the signal will be transmitted and will be received to observe the performance of this part of the system.

3.1 Design Objectives of the Frequency Up-Conversion Mixer

Detection of short duration pulses like TR-UWB signals introduced in previous chapter is very complicated. So let us start the design with traditional digital signal like BPSK (Binary Phase Shift Keying) or DPSK (Differential Phase Shift Keying). A BPSK transceiver is given in Fig. 3.1 and the corresponding signals are shown in Fig. 3.2, where the LO (Local Oscillator) signal is a 1 GHz Sinusoid. These figures are self explanatory.

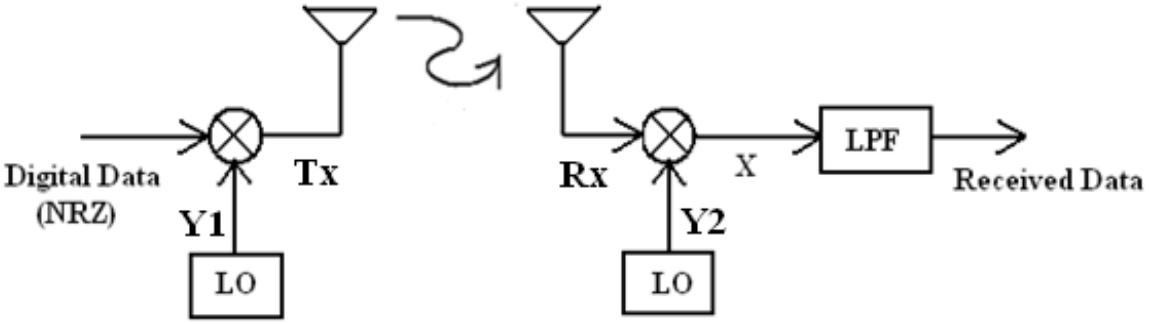

Figure 3.1: Block diagram of the bpsk transceiver

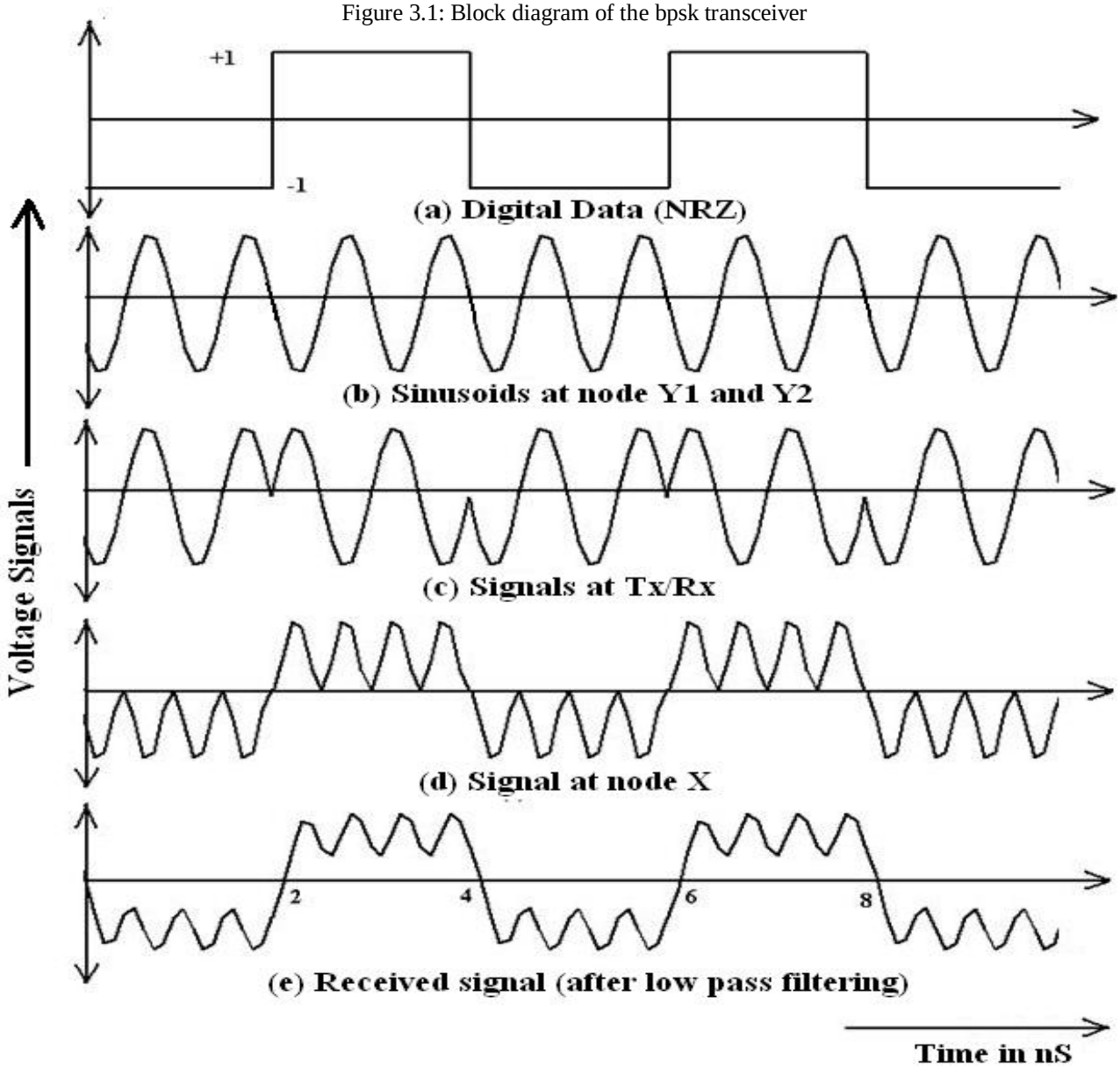

Figure 3.2: Signals at the nodes of Fig. 3.1

Since, eventually the transmitter of Fig. 3.1 will be replaced by the TR-UWB pulse generator, so the bpsk generator will be modeled as ideal whenever needed. But now, let us work with continuous '1' or '0' for further simplification at this starting level. Note that, in this case continuous '1' or '0' will be 1 GHz sinusoidal signals, but in phase with respect to the carrier for '1' or out of phase otherwise.

In summary, the frequency up-conversion mixer will up-lift the 1 GHz sinusoidal signal to about 20 GHz i.e. in K-frequency band, so that the signal frequency falls within the pass band of the on-chip integrated antenna. The mixer has to be simple, compact, low power, it should have good input and output matching, lowest possible harmonic distortion, good port to port isolation etc. Next sections will explain what the constraints in choosing proper mixer topology were and how the circuit was designed to satisfy all the design objectives mentioned.

3.2 Selection of the Mixer Topology

Choice of the mixer topology is very important for designing transceivers, especially for high frequency conditions. Compromises among the conversion gain, noise figure, power consumption and the linearity are involved. Though, CMOS low noise amplifiers operating in K-frequency band have received good attention, but the up-conversion mixers have not got that much [25]. In fact, a design whose features match exactly to this system could not be found in literature. That is why, a fresh one was to design.

Passive mixer like that of [26] is one of the choices, but is subject to high conversion losses. Gilbert mixer is probably the most popular choice, but is usually power hungry. For example, 40.5mW and 93mW power consumptions are reported in [22] and [27] respectively. Folded mixers are familiar for their better linearity, but are noisy. 12.9 NF of such one is reported in [28].

On the other hand, square law mixers are simple, consists of least number of transistors. So, low power, less noisy and are less susceptible to harmonic problems [29], but are criticized for their poor input port isolation, which makes it less appropriate for high speed transceivers. The square law mixer designed in this thesis work incorporated a new input isolation technique that suppressed the leakage problem satisfactorily. The circuit was designed in IBM 90 nm CMOS process, whereas most of the modern MMwave circuits are implemented in costly technologies like SiGe, SOI etc. Therefore, the mixer will be cheap as well. After all, this mixer could up-convert a 1 GHz sinusoidal signal to K-frequency band successfully.

3.3 Description of the Circuit

If principle of superposition is applied to the square law mixer of Fig. 3.3, then it can be shown that, $v_{IN}=V_B+v_{lo}+v_{if}$, where v_{lo} and v_{if} are the ac components of v_{IN}. Their frequencies are same as those of v_{lo} and v_{if} respectively, but the amplitude is scaled by the corresponding impedance of the coupling capacitor, Cc. Again, when the transistor is in saturation, then

$$I_D = \frac{1}{2}\beta(v_{IN} - V_t)^2 \qquad 3.1$$

Where, $\beta=\mu_n C_{ox}\frac{W}{L}$, μ_n = mobility of the electron, C_{ox}=oxide capacitance per unit area, W and L are the width and the length of the transistor respectively, V_t it the threshold voltage.

From (3.1), $I_D = \frac{1}{2}\beta(V_B+v_{lo}+v_{if} - V_t)^2$,

$$= \frac{1}{2}\beta(V_B - V_t)^2 + \frac{1}{2}\beta v_{lo}^2 + \frac{1}{2}\beta v_{if}^2 + \beta(V_B - V_t)v_{lo} + \beta(V_B - V_t)v_{if} + \beta v_{if}v_{lo} \qquad 3.2$$

(‘ ⁄ ’ are dropped for simplicity)

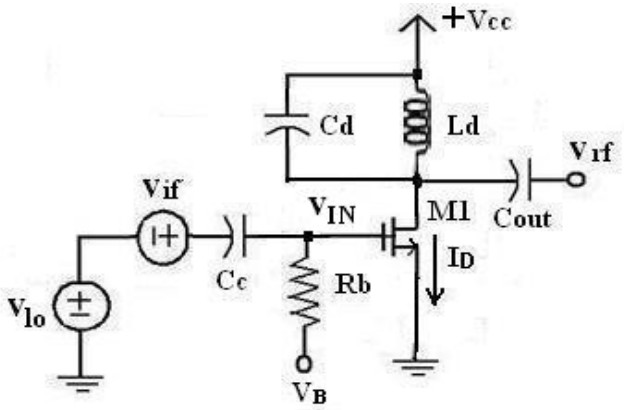

Figure 3.3: A simple square law mixer

Now, in Fig. 3.3, $v_{rf} = -I_D R_{load}$, where R_{load} is the equivalent impedance at the output of the circuit. Apparently, the circuit will work as a balanced mixer if the I_D can be made equal to $\beta v_{if} v_{lo}$ filtering other frequency components of (3.2). Advantages of the circuit would be the simplicity, low power consumption, low noise and less area requirement. However, this circuit is criticized for its lack of isolation between the input ports. Another limitation is, only one input source can have a ground reference in this circuit.

The later problem can be addressed in the circuit of Fig. 3.4, where the principle of superposition can be used again to show that, the circuit works in the similar way to that of Fig. 3.3. Still, low input isolation is the critical issue of this circuit, which makes it unattractive especially in high frequency applications.

In this work, the circuit is modified further and is drawn in Fig. 3.5. This circuit was derived from the popular cascode low noise amplifier topology, where M2 improves the gain and input-output isolation. The resonant tank, consisting of L1 and C1 is designed to resonate at f_{lo}, where f_{lo} is the frequency of v_{lo}. So, it will block v_{lo} on its way to the IF input port. On the other hand, v_{if} will see different impedance through this parallel combination as long as $f_{if} \neq f_{lo}$, where f_{if} is the frequency of v_{if}. It will reach the gate of the transistor conveniently, but will be blocked by the series combination of Lg and Cg as they are matched for f_{lo} i.e. series resonance only at the frequency f_{lo}. In this way, the isolation between the input ports was improved. Note that, the resonant tank could be placed in the LO input path as well, with necessary modifications.

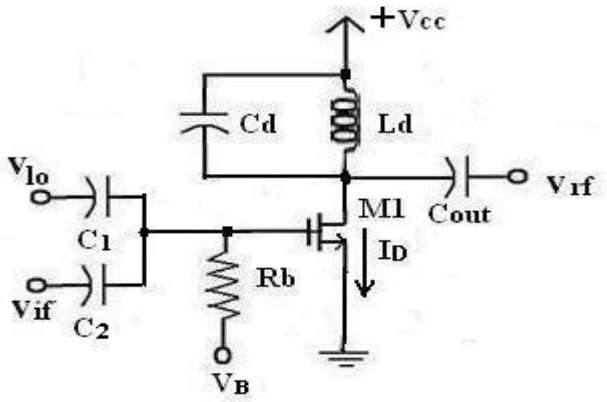

Figure 3.4: Modified circuit of a square law mixer

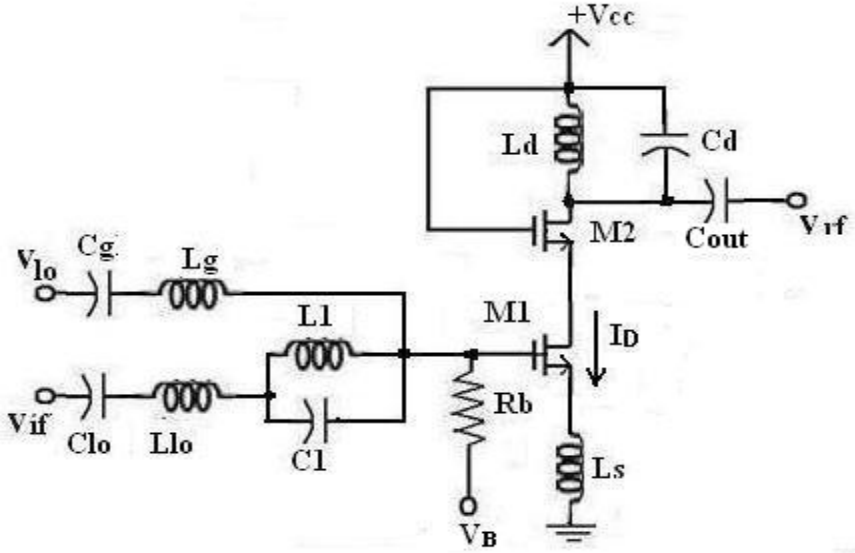

Figure 3.5: Square Law Mixer with improved input isolation technique

To demonstrate the performance of the mixer as a frequency up-converter, the f_{if} and f_{lo} was chosen as 1GHz and 19GHz respectively. Now, the impedance of the resonant tank is theoretically infinite for f_{lo} if L1=1nH and C1=70.2fF. But, it is about 6.3j Ω for the f_{if}. Similarly, v_{lo} encounters zero impedance on its way to the gate of the transistor if Lg and Cg are 1.2nH and 58.5fF respectively, whereas, the v_{if} sees this series path as -2700j Ω. In this way, a good isolation could be ensured. Rb is a large resistor, used for preventing both v_{if} and v_{lo} from bypassing the transistor gate. Clo is the dc blocking capacitor, while Llo and Ls match the input side like LNA. Input matching of LNA will be discussed in detail in next chapter. Anyways, Cd and Ld are chosen so that, the centre frequency of the gain is 19GHz, since the USB and the LSB of the v_{rf} would be 20GHz and 18GHz respectively. Voltage gain is plotted in Fig. 3.6.

Though, all the frequency components of (3.2) except f_{lo} and $f_{lo}\pm f_{if}$ are expected to be attenuated much because of falling out of the band, still v_{if} (f_{if}=1GHz) manifests itself significant, as seen in Fig. 3.7, because of its much higher magnitude than the $v_{if}v_{lo}$. For example, if the magnitude of v_{lo} and v_{if} are 1mV and 10mV respectively, then those of the USB and LSB of $v_{if}v_{lo}$ would be 5μV and a gain of about 1000 would be required to bring up this term in the range of mV for making it comparable to v_{rf}, which is infeasible in this high frequency. That is why; v_{if} will be quite large comparing to $v_{if}v_{lo}$ even after experiencing out of band attenuation.

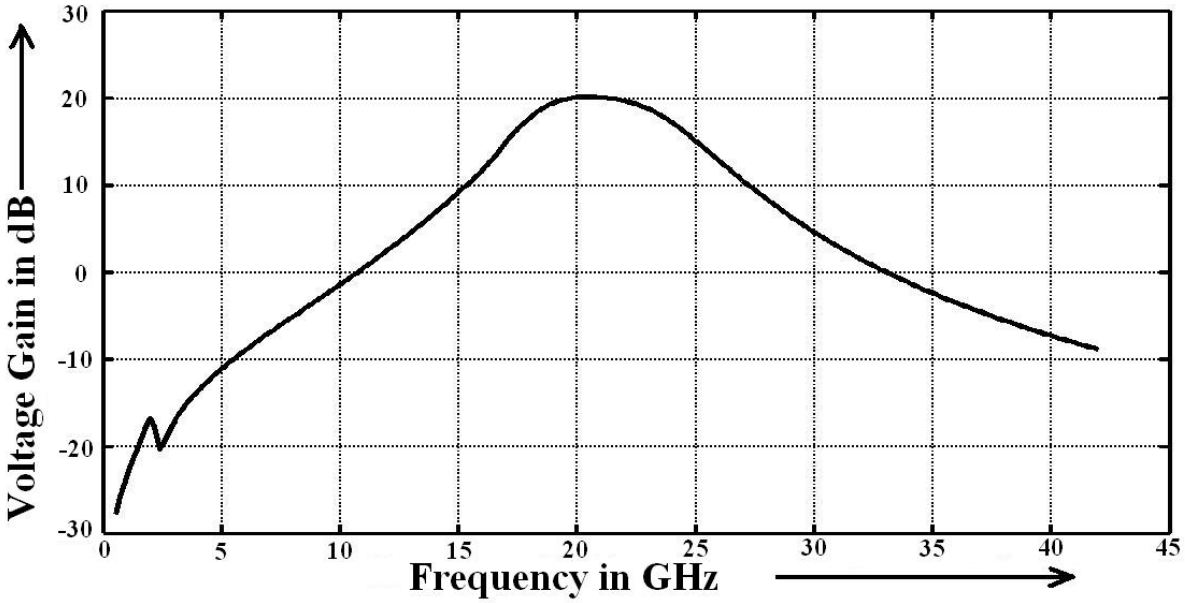

Figure 3.6: Voltage Gain of the circuit of Fig. 3

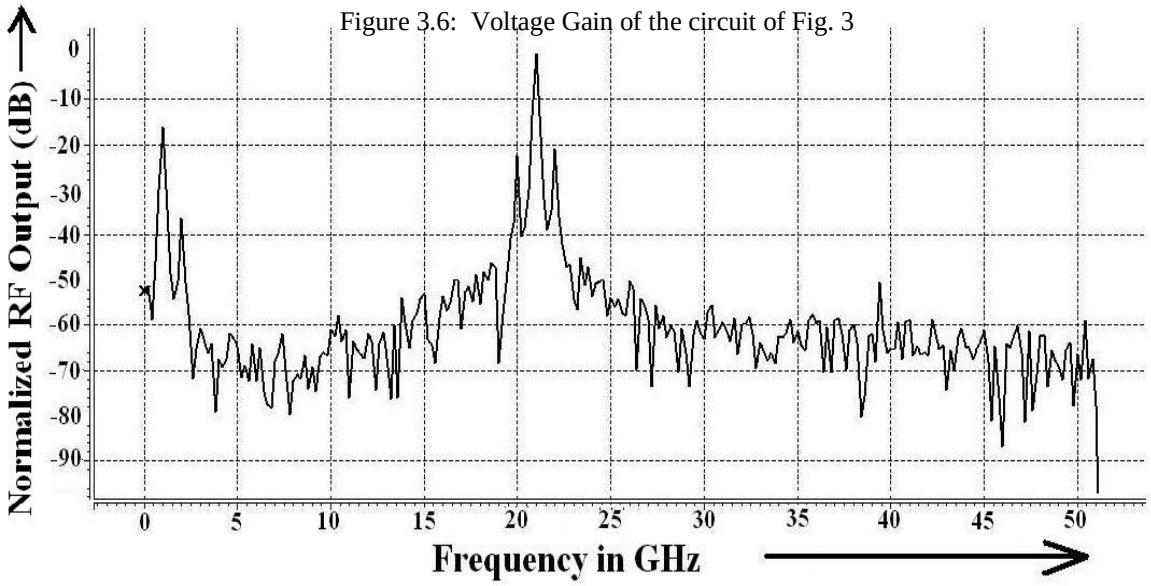

Figure 3.7: Normalized FFT of v_{rf} of the mixer in Fig. 3.5

To mitigate the issue, further modification was obvious. The circuit of Fig. 3.8 is the complete double balanced square law up-conversion mixer, where the inputs were fed differentially. In this case, (3.2) can be used to show:

$$I_{D1} = \frac{1}{2}\beta(V_B - V_t)^2+\frac{1}{2}\beta v_{lo}^2+\frac{1}{2}\beta v_{if}^2+\beta(V_B - V_t)v_{lo} +\beta(V_B - V_t)v_{if}+\beta v_{if}v_{lo} \quad 3.3$$

$$I_{D2} = \frac{1}{2}\beta(V_B - V_t)^2+\frac{1}{2}\beta v_{lo}^2+\frac{1}{2}\beta v_{if}^2 - \beta(V_B - V_t)v_{lo} - \beta(V_B - V_t)v_{if}+\beta v_{if}v_{lo} \quad 3.4$$

and

$$I_D = I_{D1} + I_{D2} = \beta(V_B - V_t)^2+ \beta v_{lo}^2+\beta v_{if}^2+2\beta v_{if}v_{lo} \quad 3.5$$

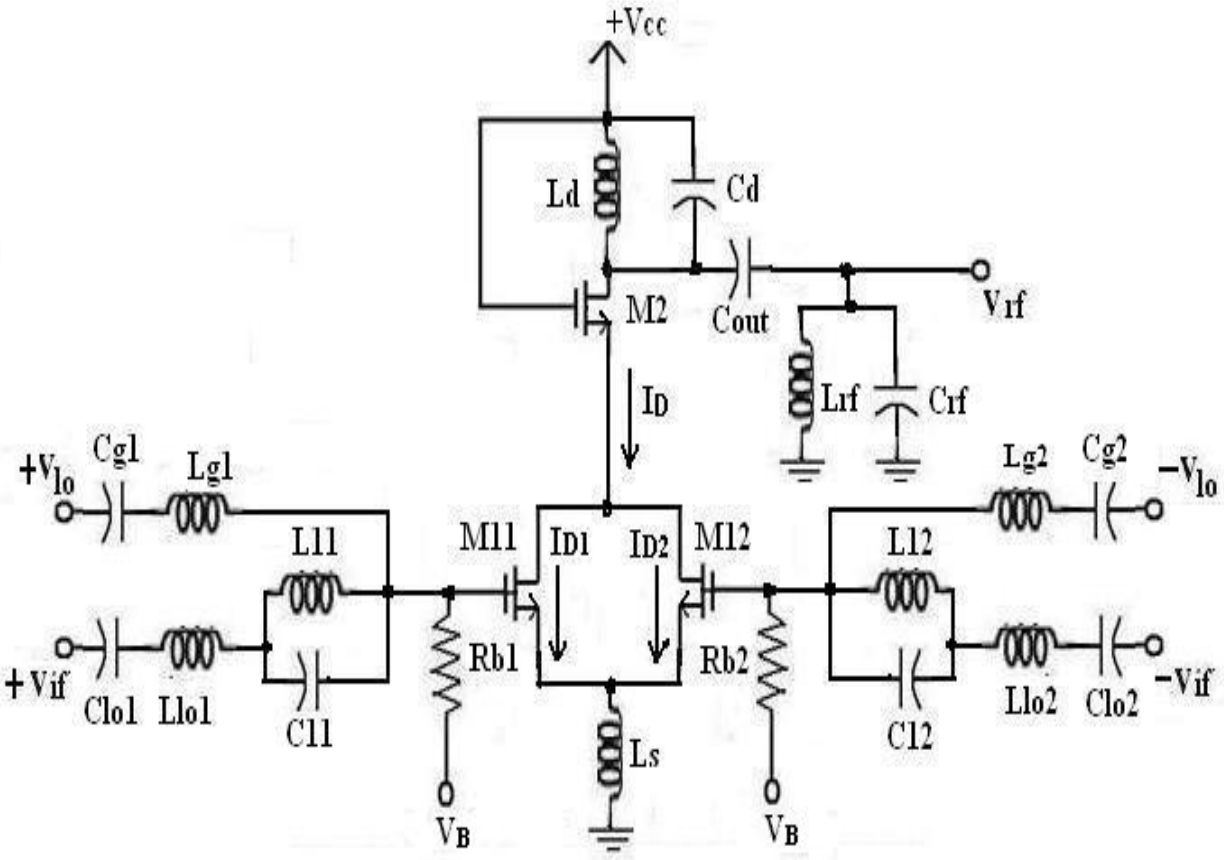

Figure 3.8: The double balanced square law CMOS up-conversion mixer

Now, in (3.5), magnitudes of v_{lo}^2, v_{if}^2 and $v_{if}v_{lo}$ are comparable. Still all the frequency components of (3.5) except $v_{if}v_{lo}$ falls out of the band and suffers sufficient attenuation. This is how, the circuit works as a double balanced mixer i.e no carrier signal at the output. Lrf and Crf forms the RF band pass filter and improves the SNR of v_{rf}. However, this filter could be designed to pass only the USB or the LSB to the output if desired. But, both were used in this system because, that will make the detection of binary bits easier. FFT of v_{rf} and corresponding time domain signal are shown in Fig. 3.9 and Fig. 3.10 respectively.

Use of only three transistors makes the circuit less noisy and power starved. Another advantage is, the circuit can work in single balanced mode i.e. carrier is one of the constituents of the output signal, simply when the – v_{lo} input port is grounded, because $\beta(V_B - V_t)v_{lo}$ augments (3.5) in that case. Therefore, this square law mixer can work as well in applications where the carrier is needed. FFT and the time domain signal of the single balanced configuration are given in Fig. 3.11 and Fig. 3.12 respectively.

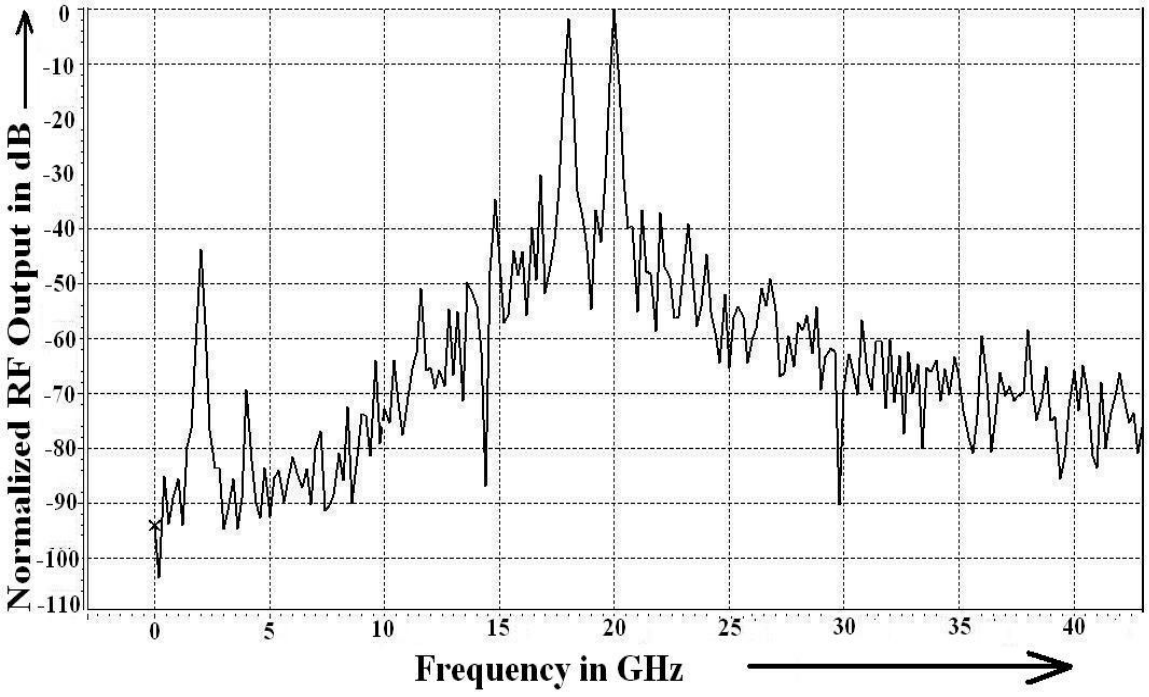

Figure 3.9: Normalized Frequency Constituents of the Double Balanced Output

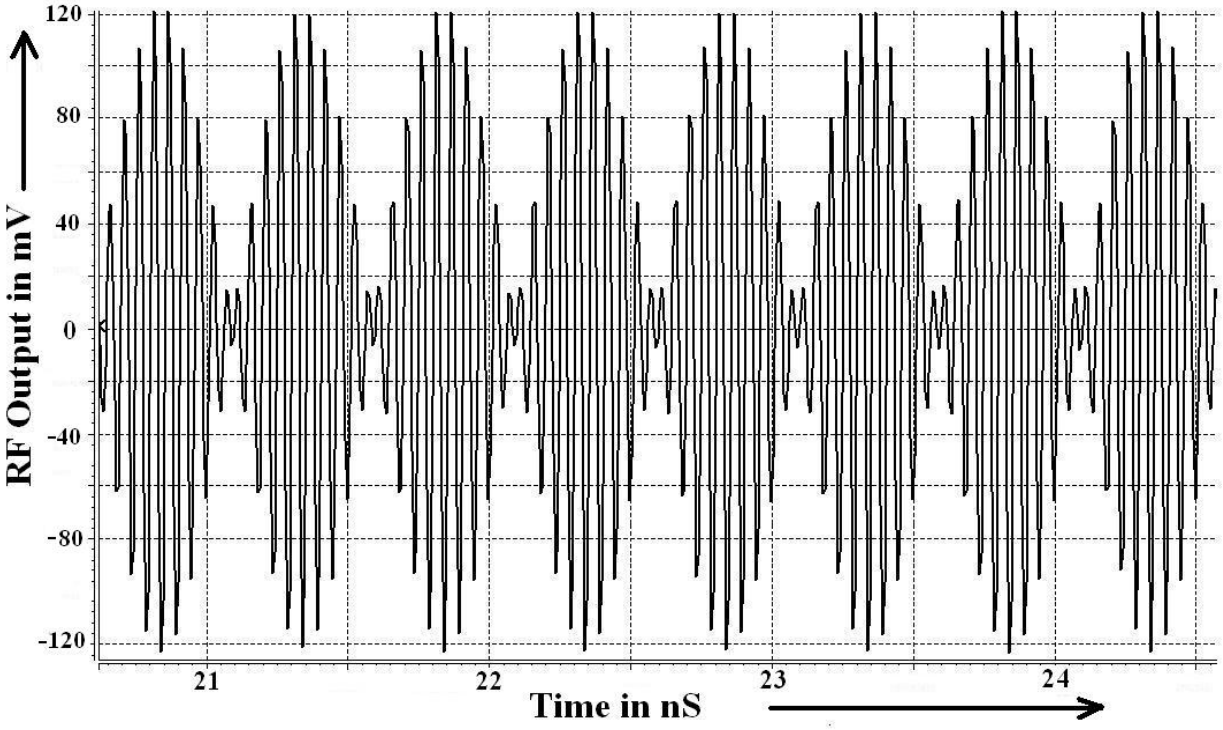

Figure 3.10: Double Balanced Output Vs Time

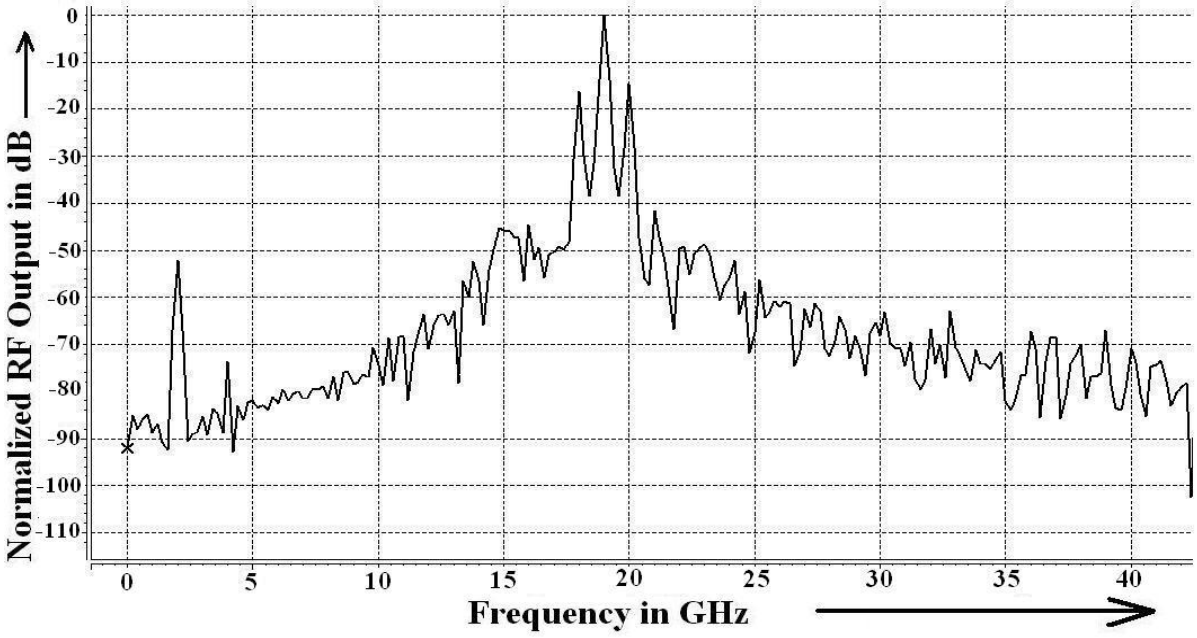

Figure 3.11: Normalized Frequency Constituents of the Single Balanced Output

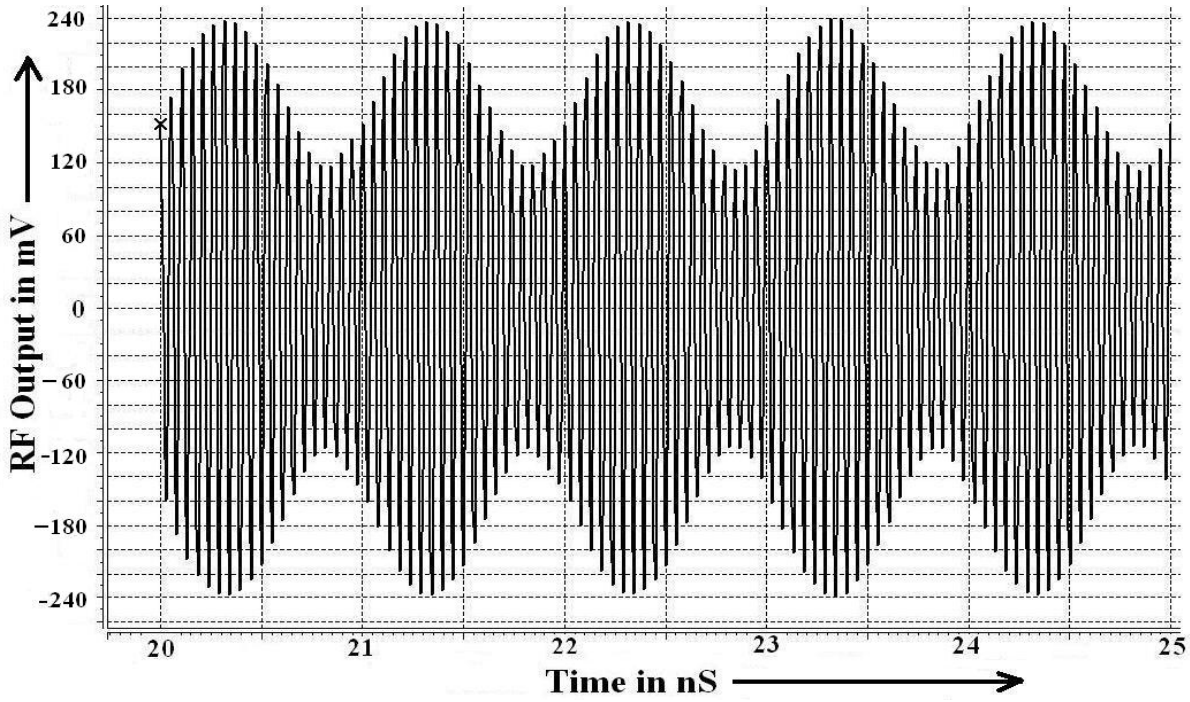

Figure 3.12: Single Balanced Output Vs Time

3.4 Other Simulated Responses

The mixer was designed in IBM 90nm CMOS process, fully integrated i.e. no off-chip circuit component, and was simulated in HSPICE. A 1GHz signal was up converted by a 19GHz carrier. This RF circuit was matched for 50Ω system. The RF filter at the output was designed to pass both the sidebands. The simulated responses exhibit a conversion gain (S21) of 11.4dB from the LO to the RF port and the reverse isolation (S12) is -30.5dB. They are plotted in Fig. 3.13. Input-Output matching parameters (S11 and S22) are depicted in Fig. 3.14 and are -18dB and -18.8dB respectively. LO to IF port isolation is shown in Fig. 3.15 and is less than -15dB in the input frequencies of interest (f_{if} and f_{lo} in this case), which is quite high for a square law mixer. Noise figure of the mixer is 6.1dB and is plotted in Fig. 3.16 together with the minimum noise figure. Input referred 1dB compression point and the IIP3 are -10.8dBm and about 0dBm respectively. They are respectively in Fig. 3.17 and in Fig. 3.18.

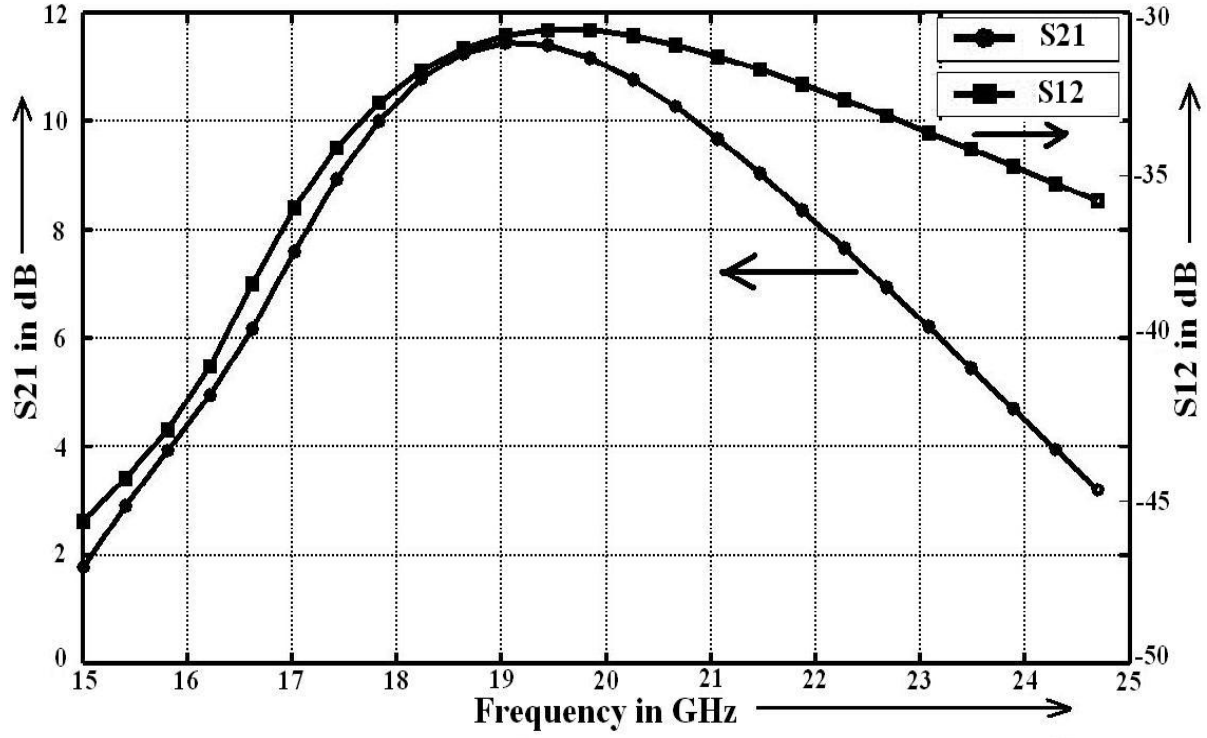

Figure 3.13: S21 and S12 Vs Frequency

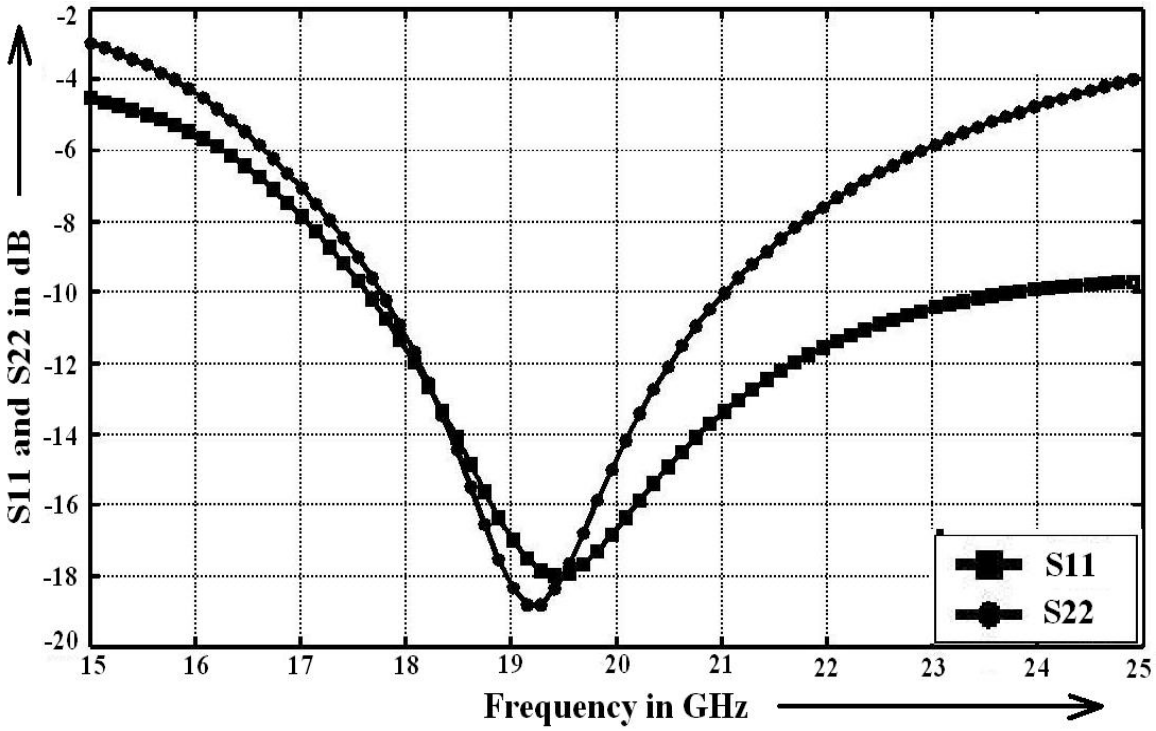

Figure 3.14: S11 and S22 Vs Frequency

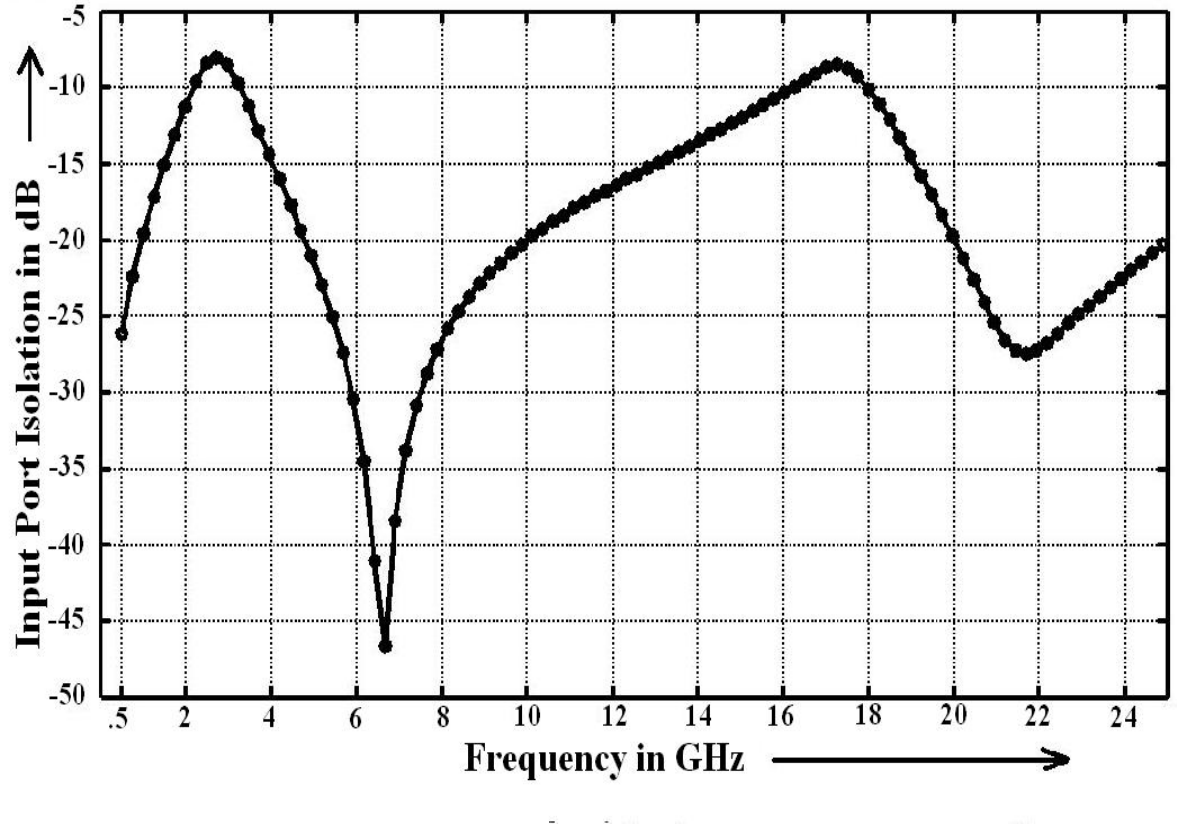

Figure 3.15: Input Isolation Vs Frequency

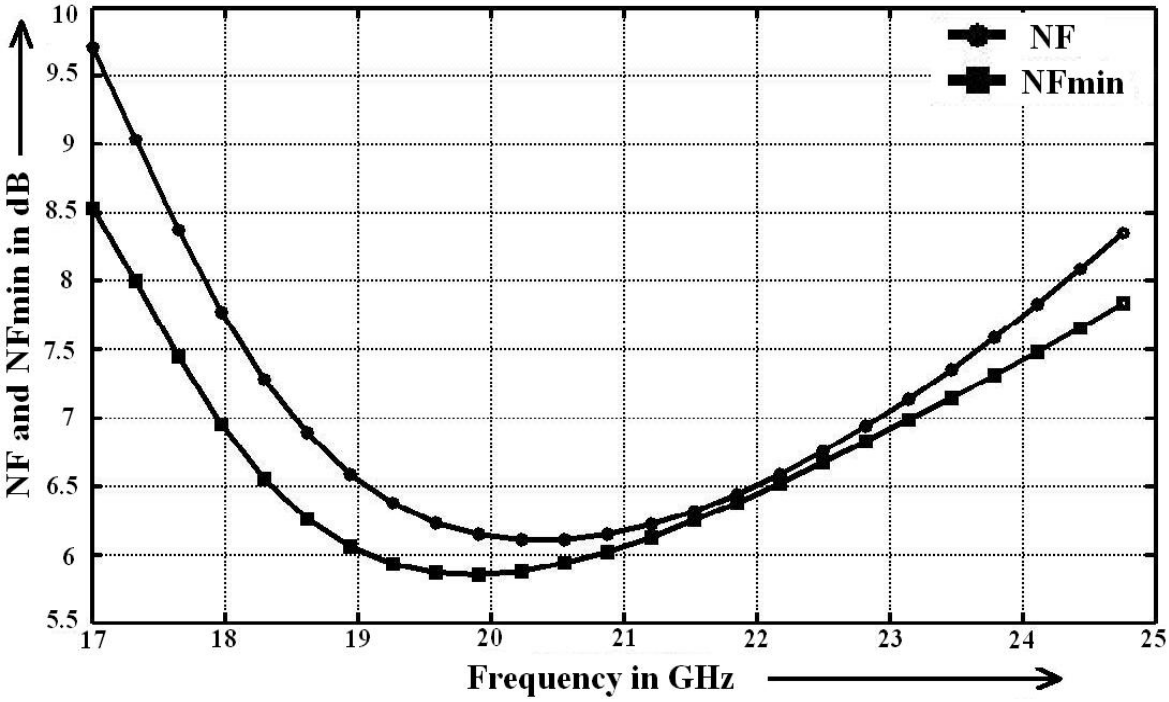

Figure 3.16: Noise Figure and Minimum Noise Figure Vs Frequency

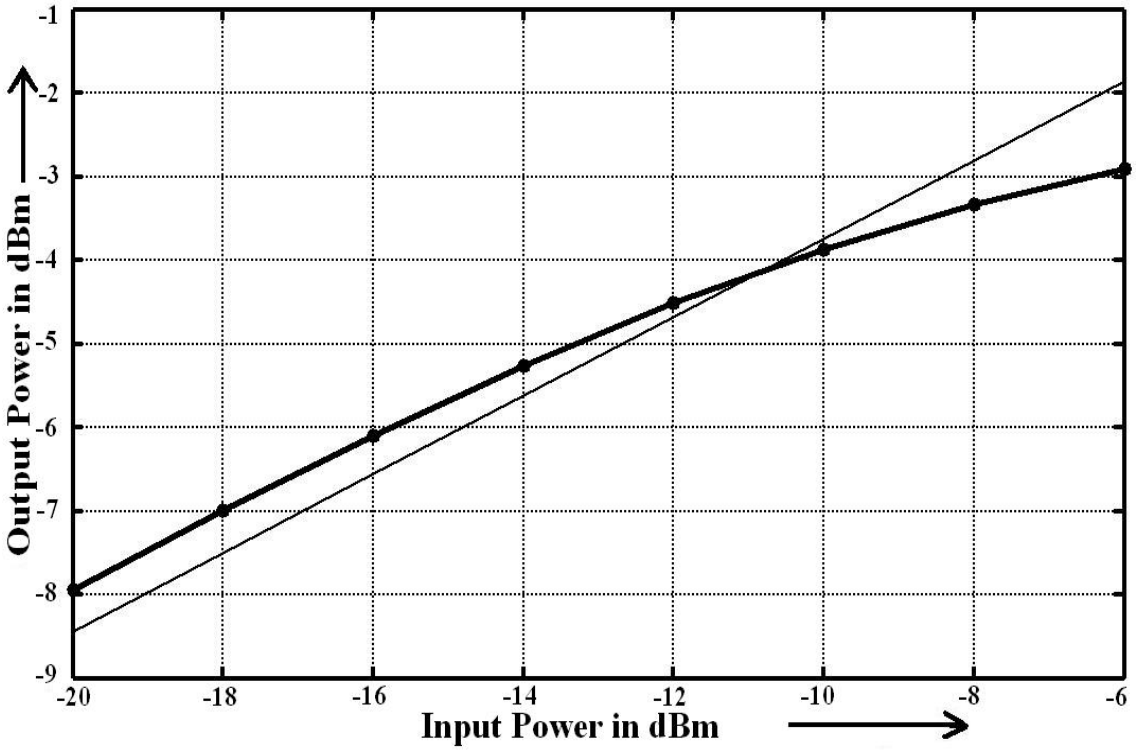

Figure 3.17: Input referred 1dB Compression Point

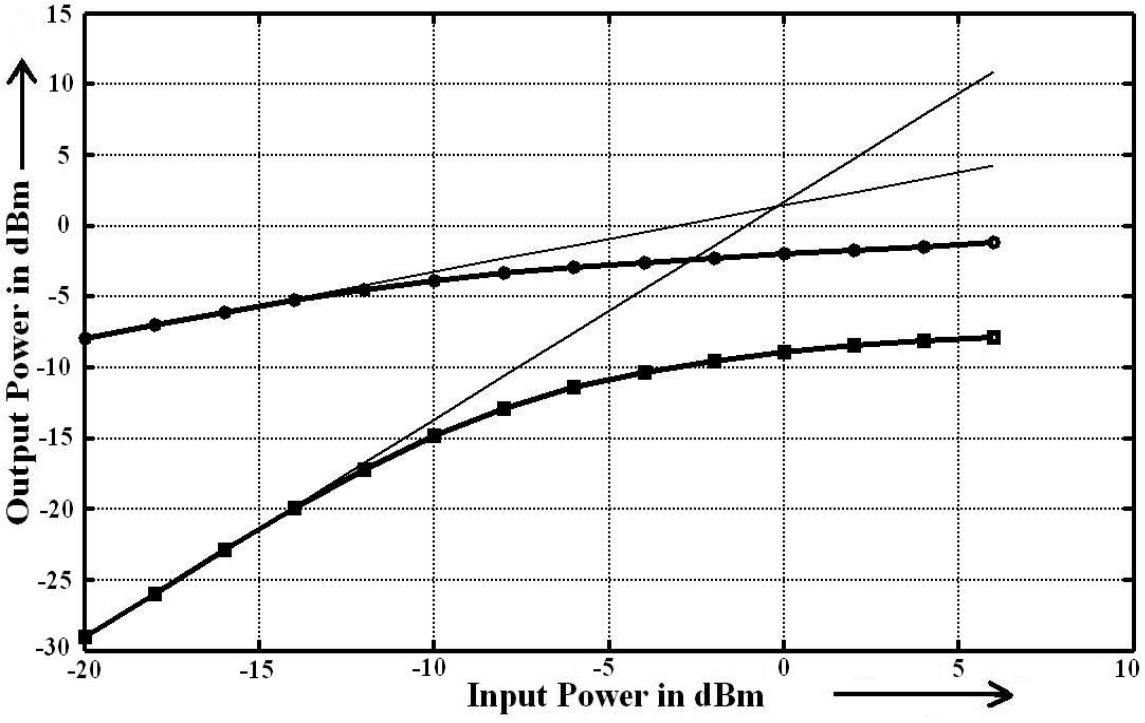

Figure 3.18: Input referred IP3 (IIP3)

Group delay of the mixer is shown in Fig. 3.19 and it varies from .07 nS to .11 nS within the operating band. Time period relative to the centre frequency (19GHz) is .053 nS. So, group delay variation is about 75.5% ($\frac{0.11-0.07}{0.053}$X100%) with respect to the centre frequency. This <100% group delay ensures that, there will be no Inter Symbol Interference due to the dispersion if the mixer is employed in digital applications. Moreover, the variation of the group delay, as can be seen in Fig. 3.19, is almost symmetric with respect to the centre frequency. That is why $f_{lo}+ f_{if}$ and $f_{lo}- f_{if}$ can be expected to experience almost same delay on their way to the output, resulting in very low distortion. To demonstrate this issue, the mixer was fed by a three tones IF input, i.e. $v_{if} =A_1\sin(2\pi f_1 t)+A_2\sin(2\pi f_2 t)+ A_3\sin(2\pi f_3 t)$, where f_1, f_2 and f_3 are 1, 2 and 0.2 GHz respectively. The corresponding RF output can be found in Fig. 3.20, where the mixer was in single balanced mode. To compare with, Fig. 3.21 plots:

$$V_{rf}=Ac[1+A_1\sin(2\pi f_1 t)+A_2\sin(2\pi f_2 t)+A_3\sin(2\pi f_3 t)]\sin(2\pi f_{lo} t) \quad 3.6$$

using MATLAB, where, f_{lo}=19GHz. As, there is no group delay variation, thus no distortion in (3.6), so the resemblance between Fig. 3.20 and Fig. 3.21 justifies the aforementioned argument.

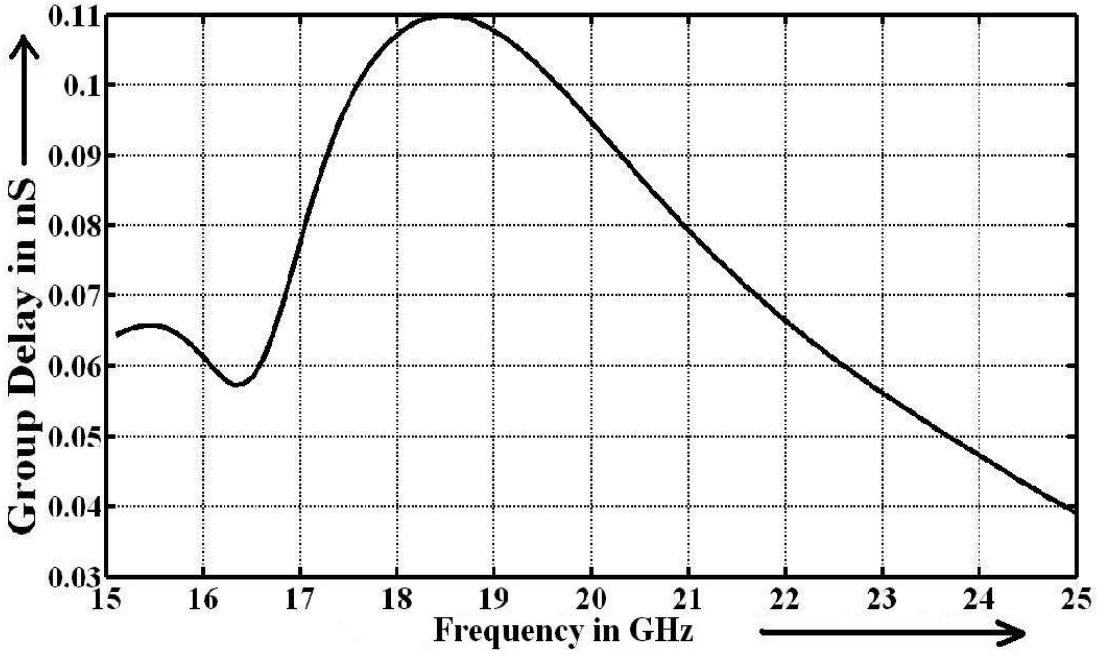

Figure 3.19: Group Delay Vs Frequency

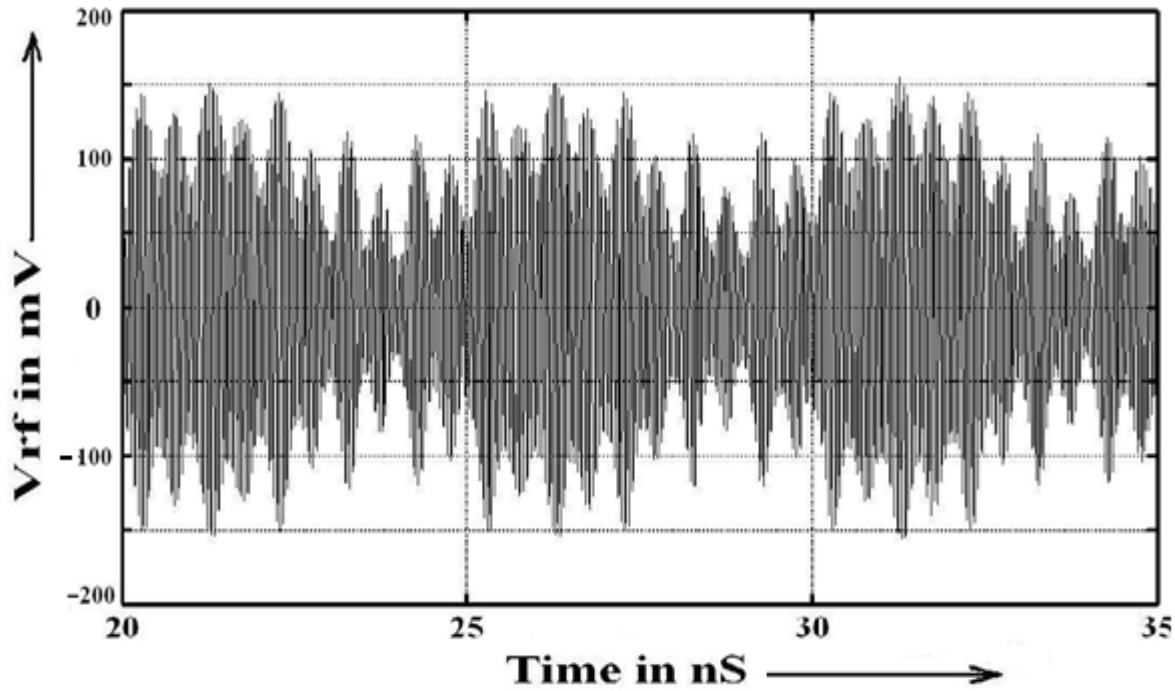

Figure 3.20: RF Output for the three tone input signal

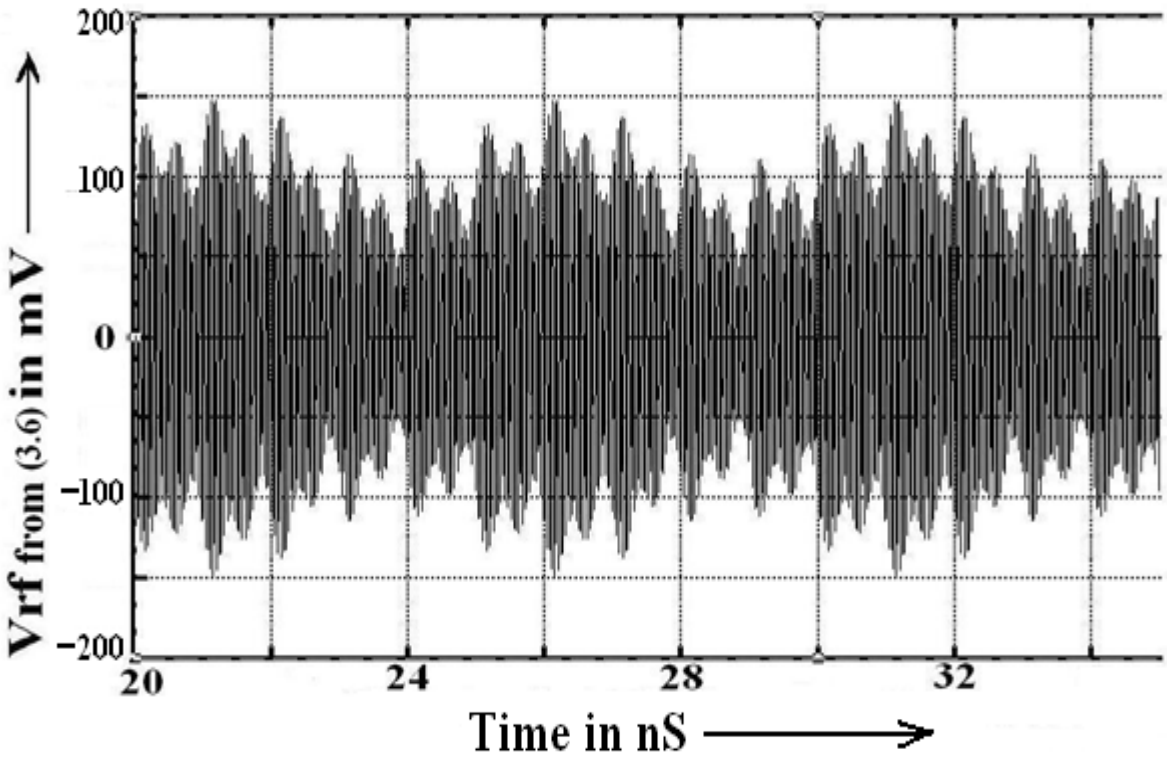

Figure 3.21: Ideal RF Output from (3.6) Vs Time

The circuit consumes only 9.25mW power from a 1.2V power supply. Therefore, commitments of this simple square law mixer are quite lucrative comparing to the state of the art. The design was accepted in 17 th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2010), Athens, Greece, December 12-15, 2010 [30].

Lastly, the double balanced signal of Fig. 3.10 was transmitted and received by the on-chip antenna pair. The simulated responses can be found in Fig. 3.22. The signal experienced about -18 dB attenuation on its way through the wireless channel. Negligible distortion of the received signal indicates that, the signal frequencies matched well with the transmission bandwidth of the antenna and thus, optimum performance was obtained.

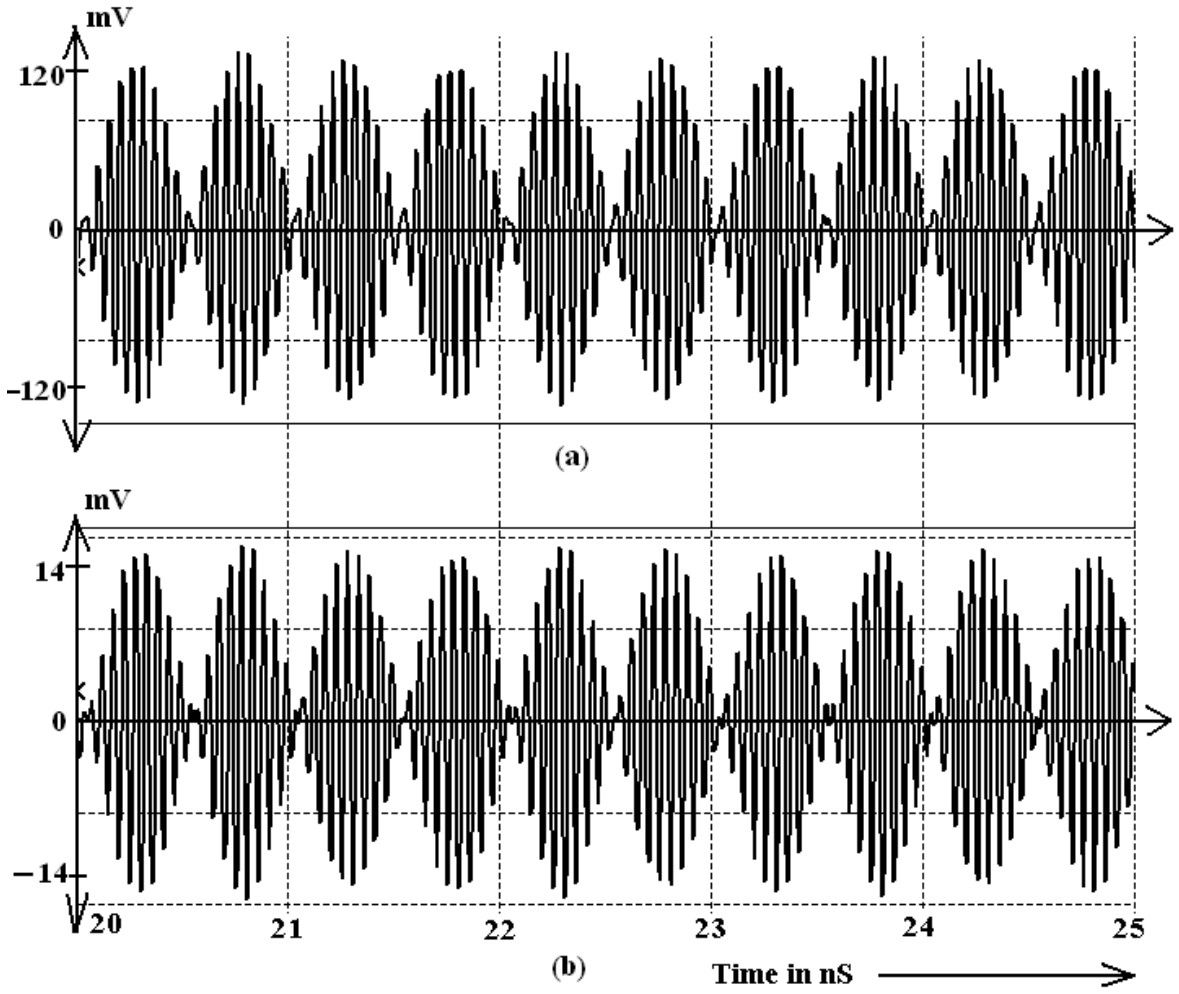

Figure 3.22: (a) Transmitted signal of Fig. 3.10 (b) Received signal

A suitable mixer topology was chosen in this chapter considering the design requirements and also its limitations were identified. The needs for employing an up-conversion mixer were mentioned as well. Then, a 1 to 20 GHz square law CMOS up-conversion mixer was designed with new input isolation technique to get rid of its problem of signal leakage in the input ports. No off-chip circuit components were used in designing this circuit i.e. the mixer was fully integrated. The circuit was analysed thoroughly and was showed that, it can work both as balanced and un-balanced mixer. Its simulated response appeared lucrative. At last, a 20 GHz DSB signal was created up-converting a 1 GHz sinusoidal signal by this mixer. That signal was transmitted and was received successfully by an on-chip integrated antenna pair. Thus, the performance of this section of the system was verified.

However, this circuit was matched for sinusoidal signal. So, wideband matching would be needed for using it in UWB applications. But, at the end no up-converter was required in the system, because high frequency UWB pulse generator appeared afterward that made frequency up-conversion unnecessary.

CHAPTER 4

DESIGN OF A 20 GHz DIFFERENTIAL LOW NOISE AMPLIFIER

Since a differential dipole antenna pair will be used in this wireless interconnect system, so the following LNA has to be differential as well. Differential circuits usually perform better than their single ended counterpart. They are more immune to power supply and environmental noises. They also have high common mode rejection ratio (CMRR) that makes them robust against common mode noise. But differential circuits are criticized for their power and space requirement.

In this chapter, at first the design of a 21 GHz source degenerated differential LNA will be described. This circuit was designed in our BSc thesis [31]. Its limitations will be discussed after a through analysis of the circuit. Then a 20 GHz differential LNA will be designed without any source degeneration. The merits and demerits of the circuit will be analyzed in detail. The circuit will be optimized for this particular application. Simulated responses of the circuit will be presented together with the layout. Lastly, the time domain performance of the LNA will be verified by observing how the received DSB signal of previous chapter, shown in Fig. 3.22, is handled by this amplifier.

4.1 Description of A 21 GHz Source-Degenerated Differential Low Noise Amplifier

Schematic diagram of a 21 GHz source degenerated differential low noise amplifier is given in Fig. 4.1. The reason of choosing a common source structure was to achieve a better noise performance, because in this structure the input is fed to the gate of a MOSFET. So the input side is free from substrate noise that would have picked up if it was fed to any diffusion body e.g. to the source of the driving transistor if it were a common gate structure.

4.1.1 Design of the Source-Degenerated Differential LNA

Operation of the circuit can be described with the help of its half circuit sketched in Fig. 4.2, where Ld forms a parallel tuning network with the gate to drain capacitance of M2 and the resonant frequency of this parallel resonator is the center frequency of the amplifier. M2, being a part of the cascode structure, not only improves the gain of the amplifier by acting as a common gate stage, but also isolates the output from the input breaking the Miller capacitance of M1 between the input-output nodes that would be present otherwise.

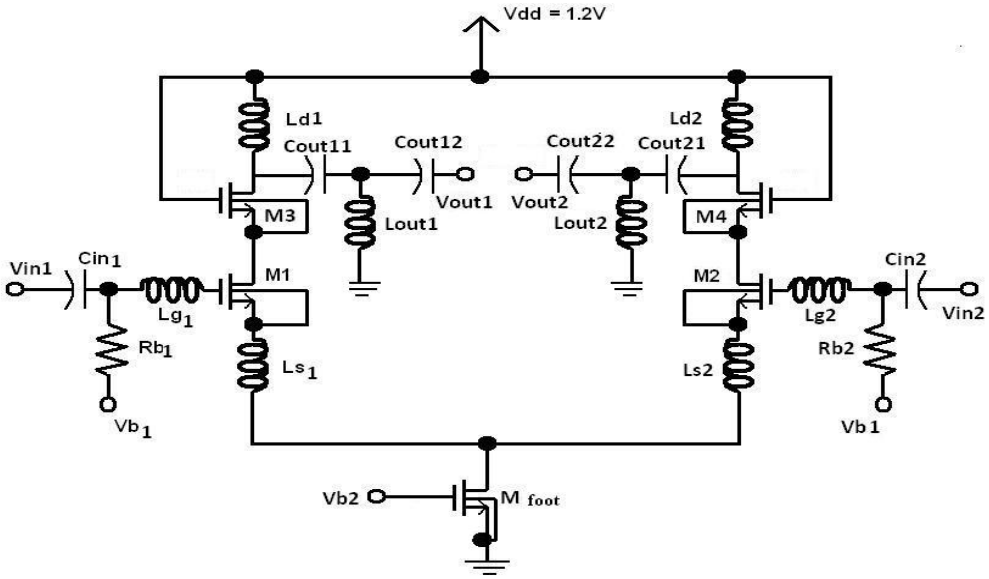

Figure 4.1: A 21GHz source-degenerated differential low noise amplifier

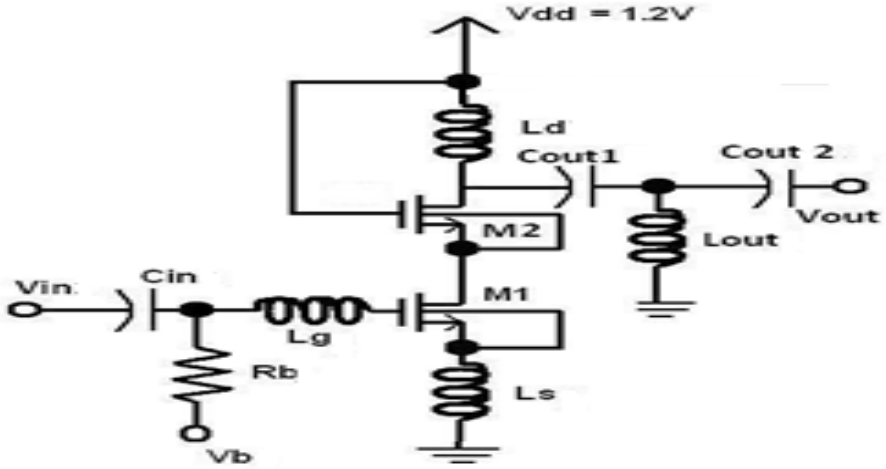

Figure 4.2: Half circuit of the differential LNA of Figure 4.1

Sizing the M1 transistor was a critical issue for it had to take part both in power and noise matching, which are independent. That is why; power matching and noise matching of the input port are different. Fortunately, there are techniques to achieve both type of input matching simultaneously in this common source LNA topology, although each has corresponding merits and demerits. Ref. [32] is a good work, where four types of matching techniques are discussed in detail, namely- Classical Noise Matching (CNM), Simultaneous Noise and Input Matching (SNIM), Power Constrained Noise Optimization (PCNO) and Power Constrained Simultaneous Noise and Input Matching (PCSNIM) techniques. Among them, the SNIM and PCSNIM techniques are relevant in this condition, so let us compare them in brief.

The core LNA are redrawn in Fig. 4.3 and Fig. 4.4 for SNIM and PCSNIM matching respectively, where the only difference is the presence of an external capacitor, C_{ext} in the later one. Now, it can be easily shown that [32], in Fig. 4.3,

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + \frac{1}{sC_{gs}} + sL_s \qquad 4.1$$

Where, g_m and C_{gs} are trans-conductance and the gate to source capacitance of the transistor M1 respectively and $s=j\omega$.

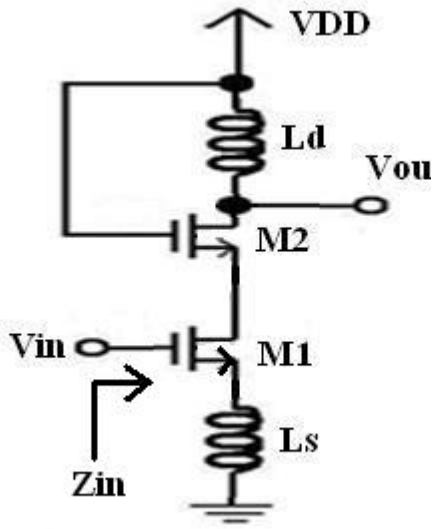

Figure 4.3: Core amplifier for SNIM matching

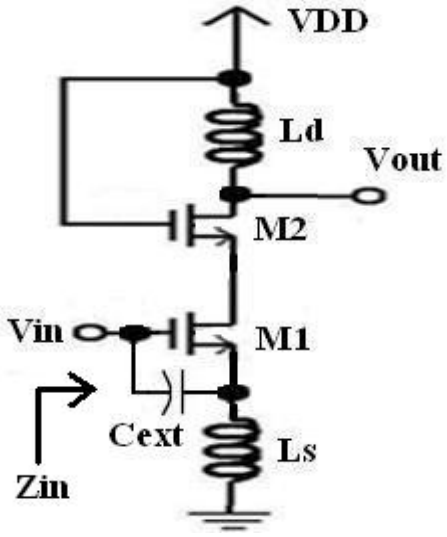

Figure 4.4: Core amplifier for PCSNIM matching

Condition for simultaneous input noise matching of the circuit is [32],

$$Z_{in} = Z_{opt}^{*} \qquad 4.2$$

Z_{opt}^{*} being the conjugate of the optimum impedance for input noise matching and can be deduced to [32],

$$Z_{opt} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma\left(1-|c|^2\right)}} + j\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma\left(1-|c|^2\right)} + \left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - sL_s \qquad 4.3$$

Again, (4.3) can be reduced to $Z_{opt} = \mathrm{Re}\left[Z_{opt}\right] - m\frac{1}{sC_{gs}} - sL_s$ 4.4

Where, γ and δ are drain and gate noise parameters such that,

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \qquad 4.5$$

And

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \qquad 4.6$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \qquad 4.7$$

g_{d0} is the drain-source conductance at zero drain-source voltage (V_{DS}), k is the Boltzman constant, T and Δf are absolute temperature and the bandwidth respectively. In (4.3), 'c' is the correlation coefficient between the gate and drain noise currents, $\alpha = g_m / g_{d0}$ and m≈1 in (4.4) for submicron technologies [32]. So, $Im[Z_{in}]=Im[Z_{opt}^{*}]$ from (4.1) and (4.4).

Now, (4.2) will be satisfied if $Re[Z_{in}] = Re[Z_{opt}^{*}]$

Or

$$\frac{g_m L_s}{C_{gs}} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma\left(1-|c|^2\right)}}}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma\left(1-|c|^2\right)} + \left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} \qquad 4.8$$

Here, $Re[Z_{in}] = \frac{g_m L_s}{C_{gs}}$ = 50 Ω at the center frequency to match the input port for a 50 Ω system i.e. source resistance is 50 Ω, that needs the right hand side of (4.8) to be equal to 50 Ω at the same frequency. In 90nm technology, $\alpha \approx 0.9$, $\delta/\gamma \approx 2$ and $c \approx 0.6$ (taken from the model files of IBM 90 nm PDK). Then, after choosing the center frequency, ω, the only parameter that can be varied to make the right hand side of (4.8) equal to 50 Ω is C_{gs} and it can be controlled by sizing the driving transistor M1. For LNAs operating with lower center frequencies, value of C_{gs} is to be quite large. For example, if ω = 2π5GHz (f=5GHz), then a C_{gs} of about 200fF is required, that in turn needs the width of M1 to be around 350μm. Such a large device will not only occupy significant space but also will burn excessive power. That is why; SNIM technique is not much attractive in low frequency applications and a better matching scheme is to be called up for power constrained noise matching which gives way to the PCSNIM technique.

The circuit for PCSNIM technique is given in Fig. 4.4, where an external capacitor, C_{ext} is introduced. Then, (4.1) and (4.3) changes to [32],

$$Z_{in} = sL_s + \frac{1}{sC_t} + \frac{g_m L_s}{C_t} \qquad 4.9$$

and

$$Z_{opt} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|c|^2)}} + j\left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - sL_s \qquad 4.10$$

respectively, where $C_t = C_{gs} + C_{ext}$, since C_{gs} and C_{ext} are parallel. Note that, (4.9) and (4.10) reduces to (4.1) and (4.3) respectively simply when $C_t = C_{gs}$. However, condition stated in (4.2) still holds and like (4.8) it can be shown that, this condition will be satisfied when,

$$\frac{g_m L_s}{C_t} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|c|^2)}}}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2)}+\left(\frac{C_t}{C_{gs}}+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} \qquad 4.11$$

Now, appropriate C_{ext} can be chosen to keep the width of M1 within 100 µm. Thus power constraint of the LNA can be met up in this matching technique. That is why PCSNIM is a popular input matching scheme, especially in low frequency LNAs and a lot of designs relied on this method like [33-34] etc.

But, in 21 GHz center frequency, C_{gs} can be decreased by a factor by which the center frequency increased i.e. more than 4 times in this case. So, right hand side of (4.8) can be made equal to 50 Ω with a C_{gs} less than 50 fF, in other words width of M1 can be less than 100 µm. It implies that, in this range of frequency SNIM technique will surpass PCSNIM and external capacitor C_{ext} will no longer be needed. Most of the LNAs operating in this band of frequencies, such as [7], [22] used this benefit without any explanation.

SNIM technique was preferred in this design. Width of M1 was chosen as 80 µm with 20 fingers. C_{gs} was found as 46 fF after simulation and $Re[Z_{opt}]$ was calculated as 50.9 Ω using (4.8). Then, the bias voltage, Vb of Fig. 4.2 was set so that maximum g_m of M1 can be obtained and still operates in saturation region. Simulation result showed that g_m=30 mA/V. So about 80 pH source degenerating inductor, L_s was needed for getting $Re[Z_{in}]$ = 52 Ω. $Re[Z_{in}]$ versus frequency is shown in Fig. 4.5 and Noise Figure, NF together with Minimum Noise Figure, NF_{min} was plotted in Fig. 4.6. Note that, NF_{min} shows the best noise performance that could be obtained from a circuit if the noise matching was perfect. Fig. 4.6 points that, perfect noise matching was in 22.5 GHz where both curves touched each other. The reason why this point shifted further from 21 GHz is the internal resistance of L_g and L_s were neglected in the analysis discussed above.

However, noise figure of the LNA is 4.4 dB at the center frequency and is less than 5 dB in the entire bandwidth which is quite satisfactory comparing to the state of the art.

In Fig. 4.2, Rb is a large resistor so that, the input signal does not bypass to ground through Vb, while C_{in} is the input coupling capacitor for dc blocking and L_g is to eliminate the capacitive reactance of the input impedance, since the source impedances are purely resistive in 50 Ω system. That is why, Z_{in} has to be purely resistive as well for minimum reflection from the input port.

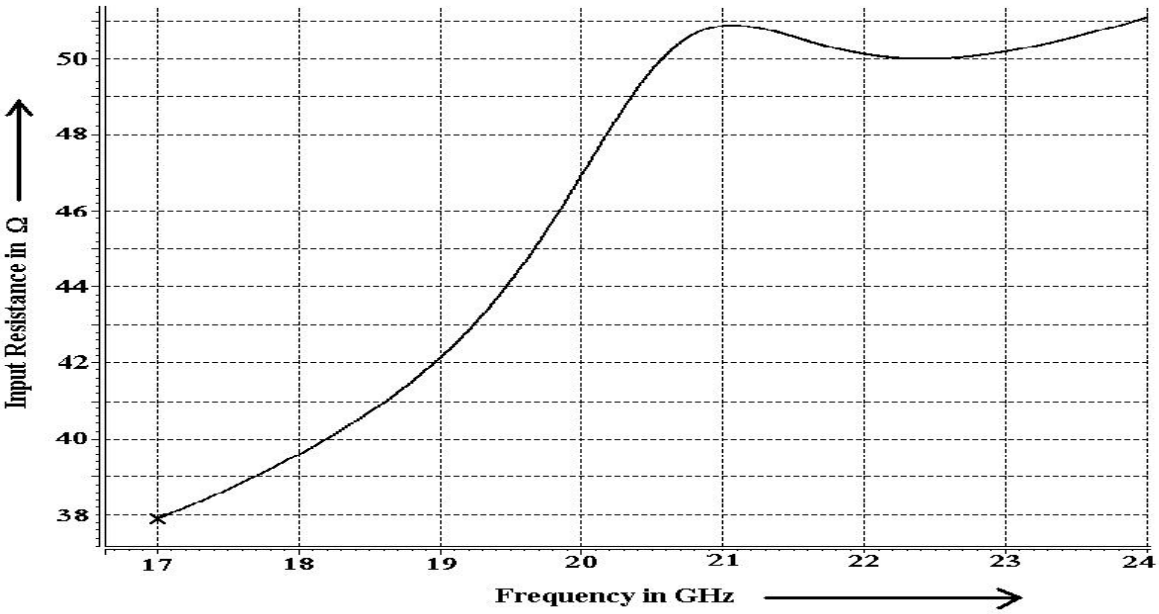

Figure 4.5: Input resistance versus frequency for the circuit of Fig. 4.1

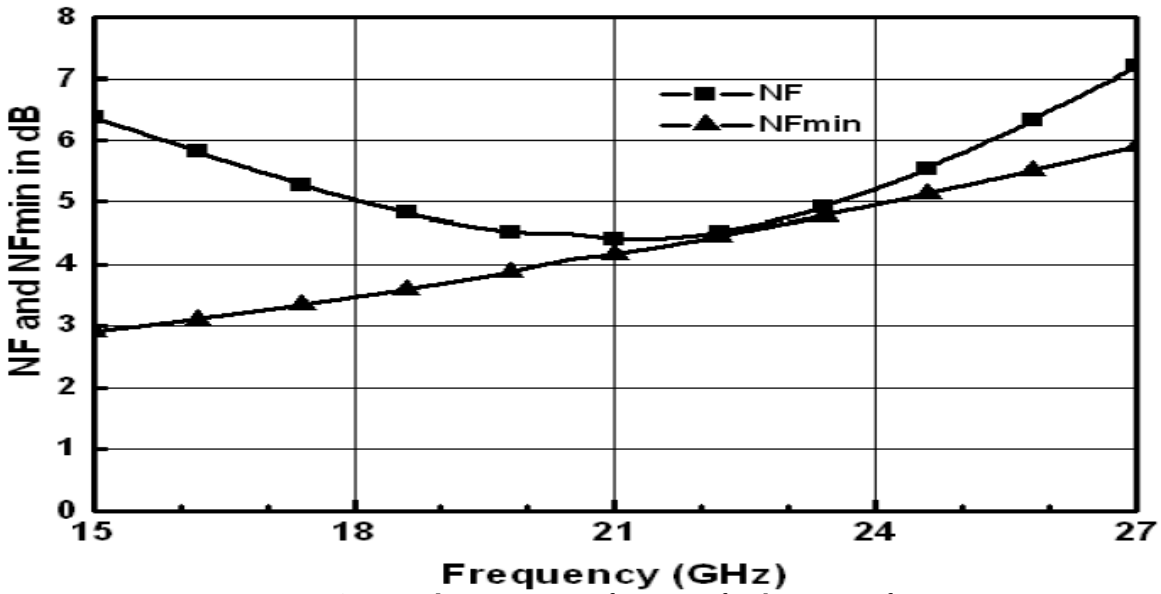

Figure 4.6: NF and NFmin versus frequency for the circuit of Fig. 4.1

In this circuit, C_{out1}, C_{out2} and L_{out} formed the output matching network. It was a tricky circuit and was the contribution of this design. Detail of this network can be found in [35-38] and let us avoid that here since it was not used in the 20 GHz differential LNA, which will be used in this work and will be explained in the next section.

4.1.2 Simulated Responses of the Source-Degenerated Differential LNA

Simulated power gain, S21 of the source-degenerated differential LNA is depicted in Fig. 4.7 that peaks to 9.7 dB at 21 GHz with a bandwidth of 4.4 GHz (18.8-23.2 GHz). Input and output matching parameters (S11 and S22) are shown in Fig. 4.8 and Fig. 4.9 respectively. Input referred 1 dB compression point of the circuit is -4.26 dBm and can be found in Fig. 4.10. It consumes 20.7 mW power from a 1.2V source.

Simulated response of the circuit was lucrative. This work was accepted in the proceedings of 12th International Symposium on Integrated Circuits (ISIC 2009), Singapore [38]. Also, its half circuit was fabricated in 2009 from IBM under MOSIS Education Program (MEP). A photograph of the lot of chips is given in Appendix A.

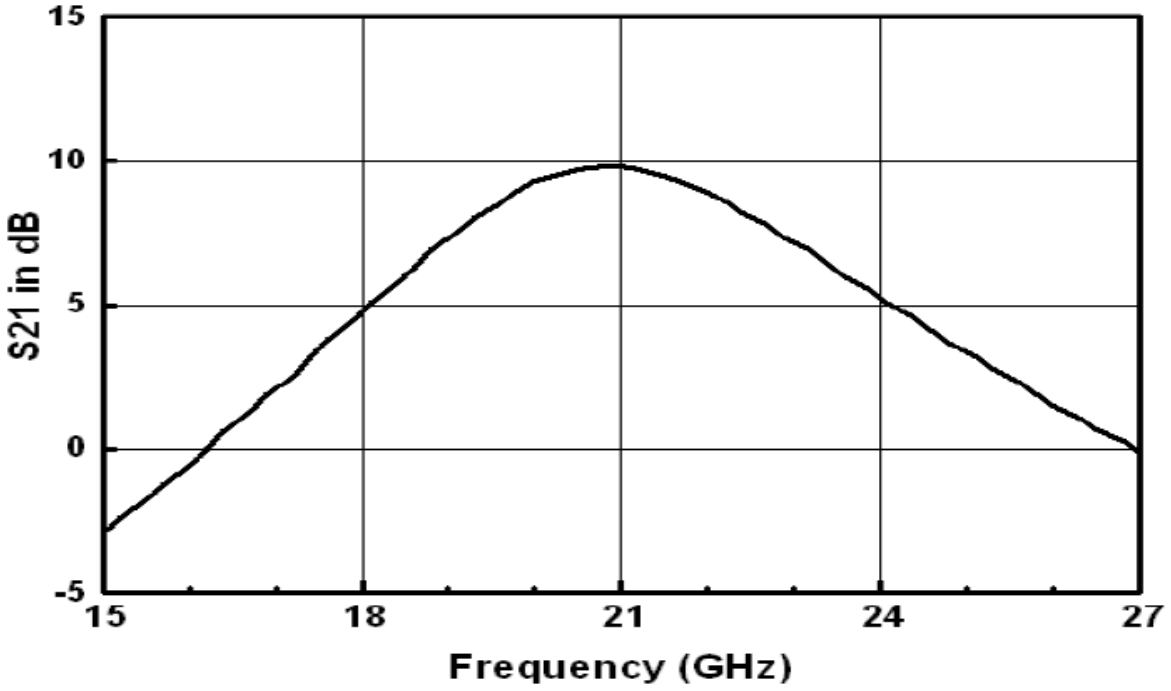

Figure 4.7: S21 versus frequency for the circuit of Fig. 4.1

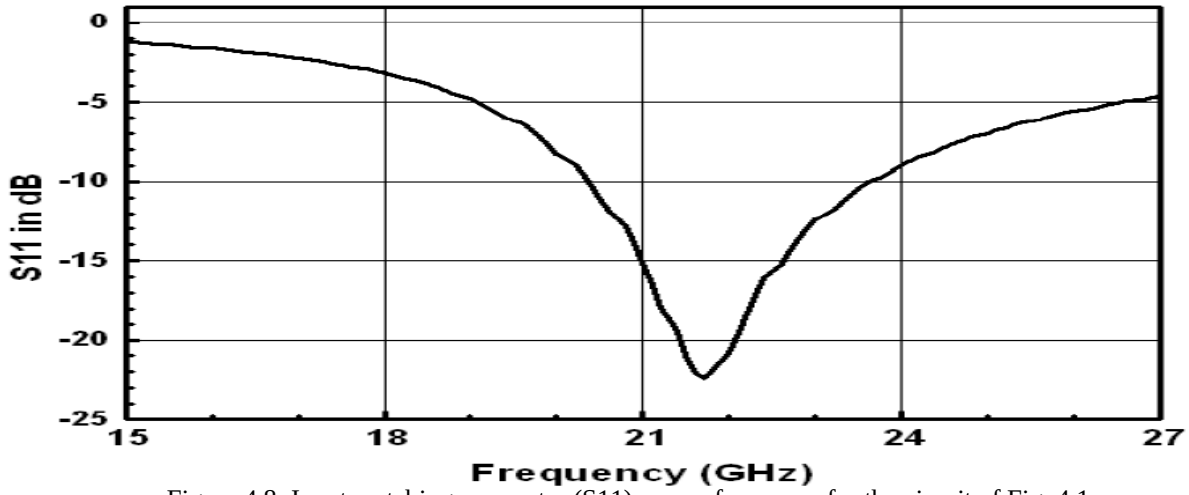

Figure 4.8: Input matching parameter (S11) versus frequency for the circuit of Fig. 4.1

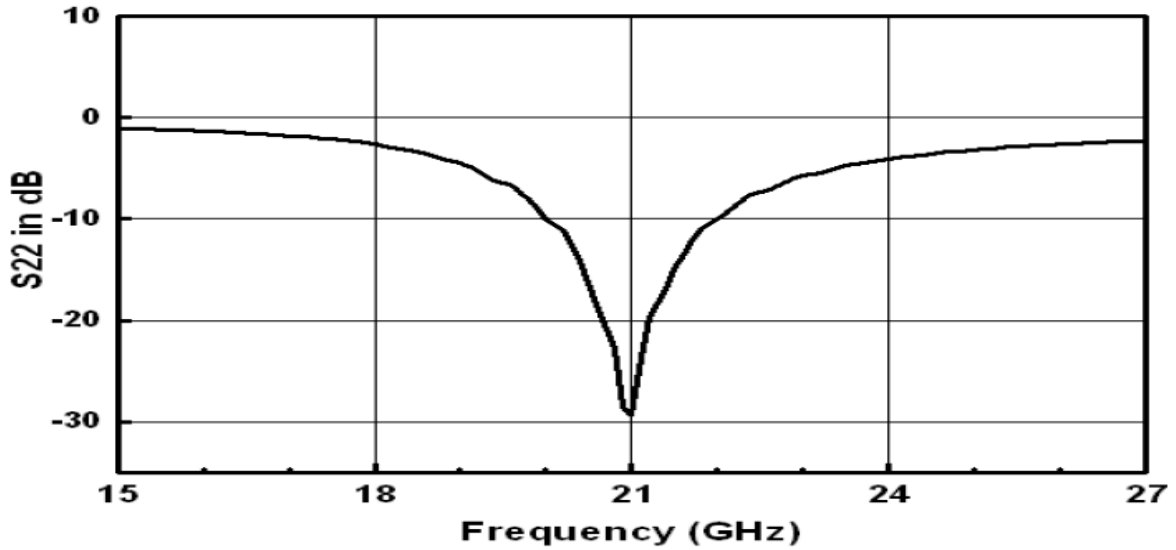

Figure 4.9: Output matching parameter (S22) versus frequency for the circuit of Fig. 4.1

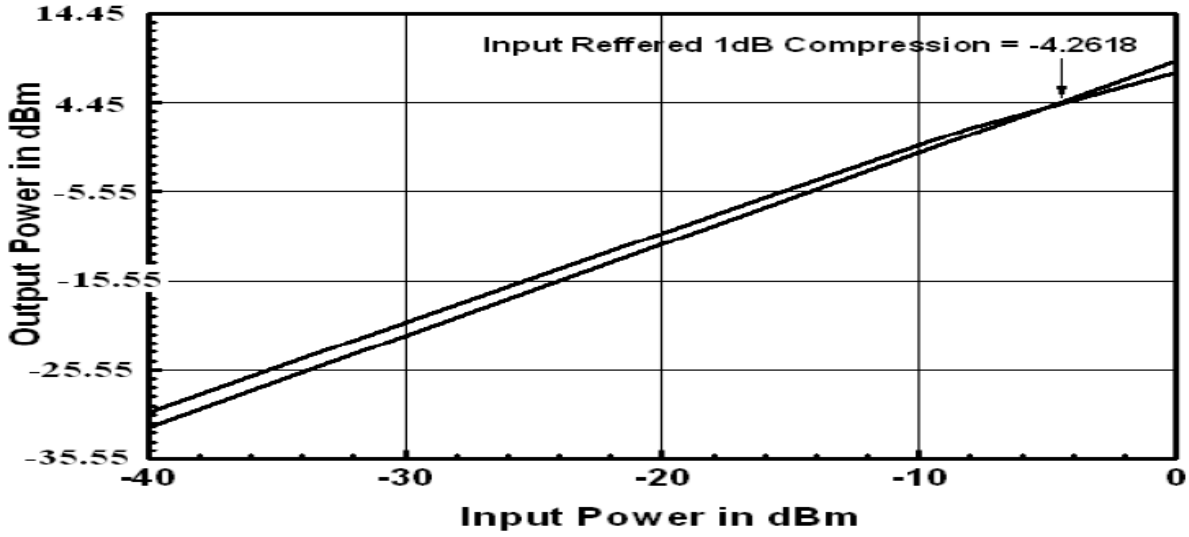

Figure 4.10: Output versus input power for the circuit of Fig. 4.1

4.2 Design of A 20 GHz Differential Low Noise Amplifier

The circuit described in previous section has a few shortcomings. First, the source degenerating inductor degrades the gain much. Secondly, on-chip inductors in sub-micron technologies are accompanied with significant amount of resistance and that is why their Q-factors are usually less than 20. So, internal resistance of that source degenerating inductor contributes considerable noise to the circuit. Note that, according to (2.2) both gain and noise performances of the LNA have to be best for getting optimum response from the receiver front end. Apparently, a differential LNA devoid of the source degenerating inductor would offer better commitments in this application. Moreover, the area requirement of the LNA would decrease significantly since inductors are the area consuming elements on silicon chip. Therefore, in this work a new input matching technique was incorporated in designing a 20 GHz differential LNA to optimize the performance of the LNA discussed in previous section by avoiding aforementioned shortcomings.

4.2.1 Description of the 20 GHz Differential LNA

The half circuit of the 20 GHz differential low noise amplifier is portrayed in Fig. 4.11. The biasing resistor, Rb is not shown in the figure. Here, L_{RF} and C_{RF} match the input side without any assistance of source degenerating inductor, while Ci blocks dc voltage. Now, let us explain how the input matching network works. The circuit is redrawn in Fig. 4.12 without any input-output matching and corresponding input impedance is shown in Fig. 4.13.

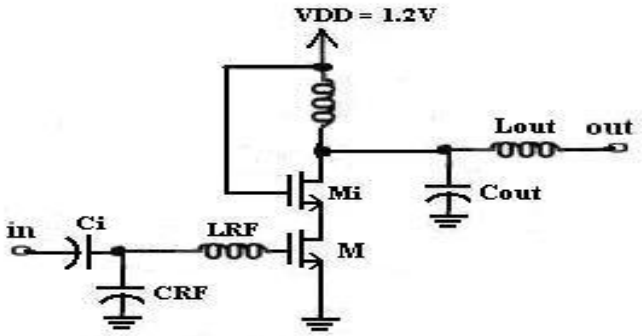

Figure 4.11: Half circuit of the 20 GHz differential LNA

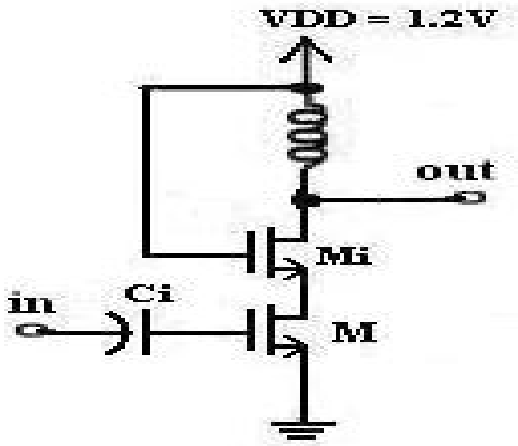

Figure 4.12: Half Circuit of the 20 GHz differential LNA without input-output matching

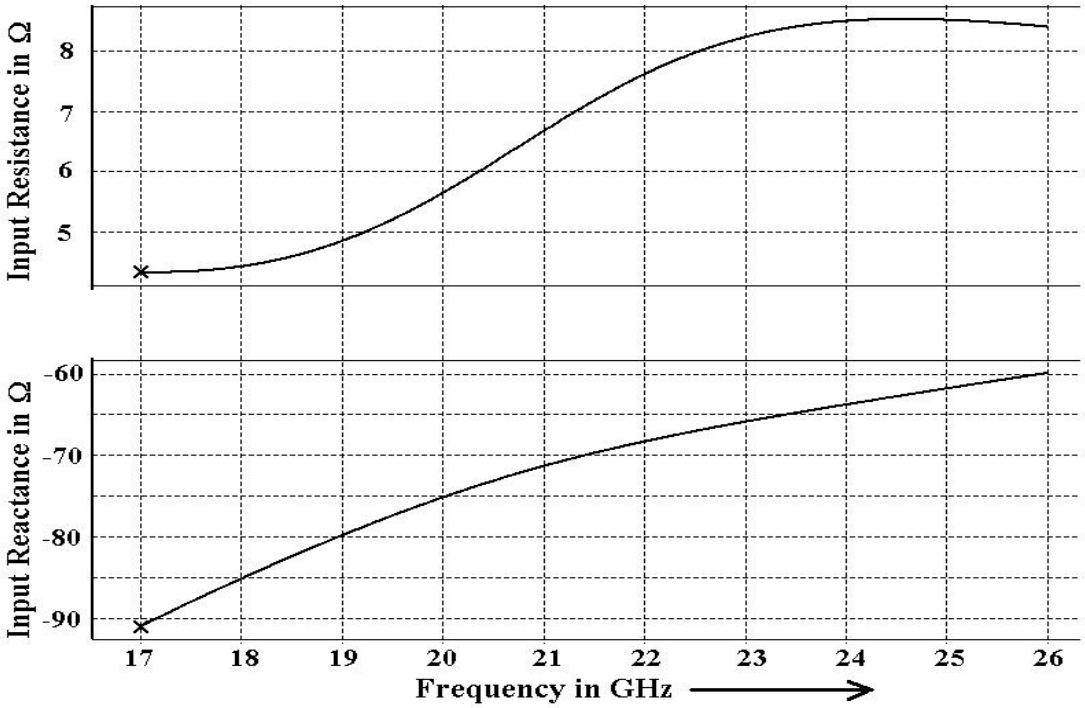

Figure 4.13: Input resistance and reactance of the circuit of Fig. 4.12

Fig. 4.13 shows that, the input resistance and reactance of the amplifier are about 5.5 Ω and -75j Ω (106 fF) respectively at the center frequency of 20 GHz. The reason of such a small gate resistance can be understood with the help of MOSFET high frequency model. Such one is given in Fig. 4.14, which is the high frequency model of the RF type of MOSFET of IBM 90 nm Technology. So, the 106 fF input capacitance is contributed by the parasitic capacitors of the driving transistor, M and the 5.5 Ω resistance comes from its

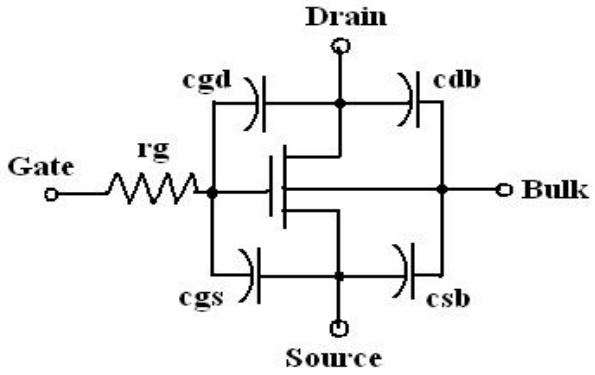

Figure 4.14: High frequency model of the NMOS Transistor

gate resistance r_g. Here, r_g is the equivalent resistor of all the internal resistances of those parasitic capacitors. Note that, in low frequencies, the capacitors will act as very high impedances and then the effect of r_g will be insignificant. In other words, this transistor model will offer very high input impedance at low frequencies as one should expect.

Again, the internal resistances of the on-chip inductors are substantial in sub-micron technologies. That is why, Q-factors of such inductors are quite low and this is one of the reasons for which designers try to avoid them in their design. For example, Q-factors of the octagonal spiral inductors of IBM 90 nm Technology are in the range of 10-15. Knowing this, it can be expected that, the resonant impedance of a parallel resonator like that of Fig. 4.15 will be much small, not infinity which would be if not for the non-ideal internal resistances ($R_{Lon\text{-}chip}$) of those on-chip inductors. Moreover, the degraded Q-factor will extend the bandwidth of the resonator of Fig. 4.15 and it no longer will act as a narrow-band band pass filter. Now, this network can serve the purpose of input matching if Z_{eq} is approximately 50 Ω at the resonant frequency.

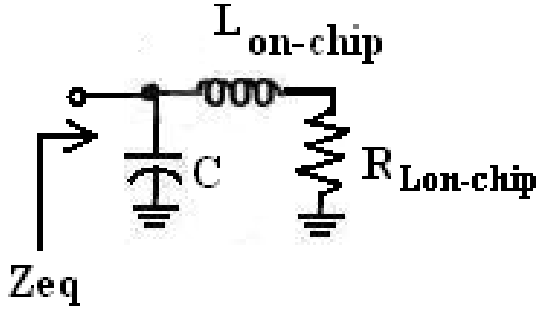

Figure 4.15: Schematic diagram of a parallel resonator

An 820 pH on-chip octagonal spiral inductor was included to the gate of the driving transistor, M of Fig. 4.12 and the resulting circuit is shown in Fig. 4.16. The corresponding input resistance and reactance are plotted in Fig. 4.17. Comparison of Fig. 4.17 with Fig. 4.13 reveals that, the inductor came up with an internal resistance of about 10 Ω. However, now the input impedance of the circuit is (16+28j) Ω. So, a -28j Ω (0.28 pF) C_{RF} would resonate with this impedance to make Zin equal to (52-24j) Ω that would match the

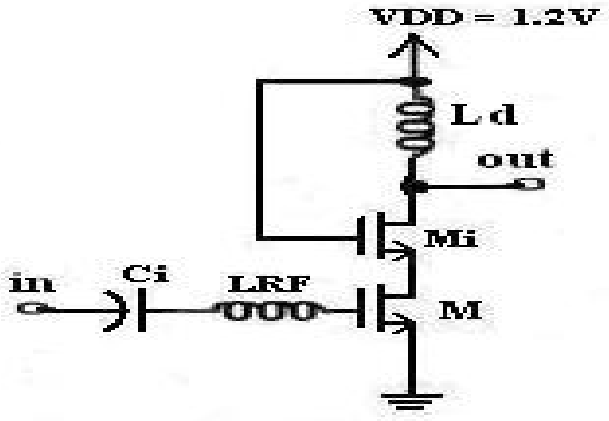

Figure 4.16: Half Circuit of the 20 GHz differential LNA with a gate inductor

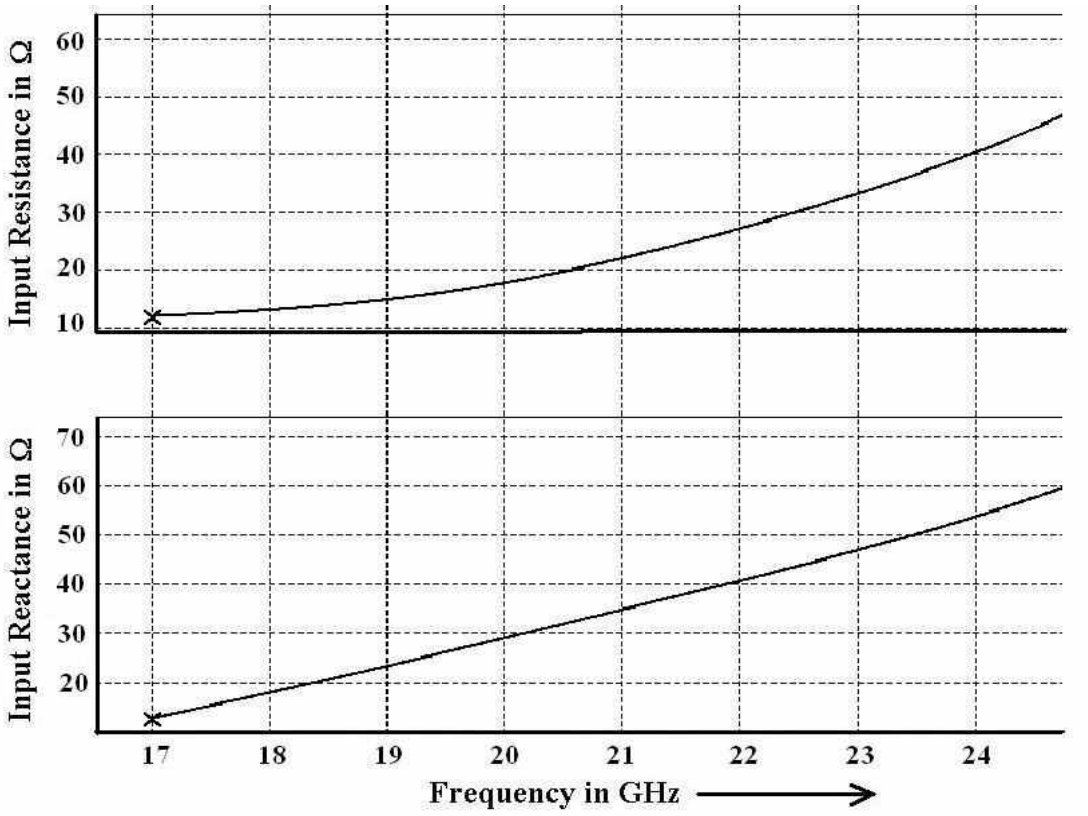

Figure 4.17: Input resistance and reactance of the circuit of Fig. 4.16

real part of Zin approximately with the 50 Ω source resistance, but the reactive part would be non-zero i.e. -24j Ω. The circuit and the correspoding input impedance can be found in Fig. 4.18 and in Fig. 4.19 respectively. To make the input reactance zero at the center frequency 20 GHz, the input port was matched at slightly higher frequency so that, the zero-crossing point of the input reactance of Fig. 4.19 shifts to the desired point. Also, the value of C_{RF} was adjusted to make the resonant impedance greater than 50 Ω at the new resonant frequency so that, the trailing edge of the input resistance curve goes through 50 Ω point at 20 GHz. The input resistance and reactance of the final circuit are given in Fig. 4.20, where they are about 50 Ω and close to 0 Ω respectively at 20 GHz. This is how the input port of the 20 GHz LNA was matched. Note that, the center frequency of the LNA is still 20 GHz, because it is governed by the drain inductor, Ld and the gate-drain capacitor of the isolating transistor, Mi, whereas input matching is only for reducing the signal reflection from the input port of the amplifier.

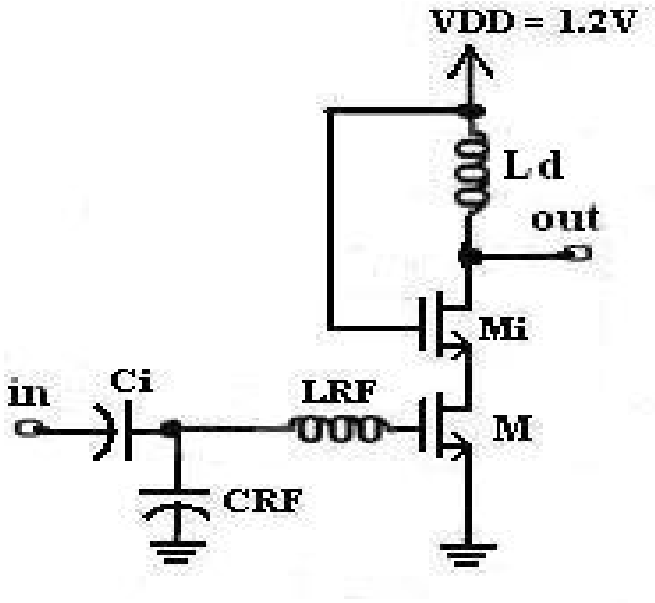

Figure 4.18: Half Circuit of the 20 GHz differential LNA with input matching

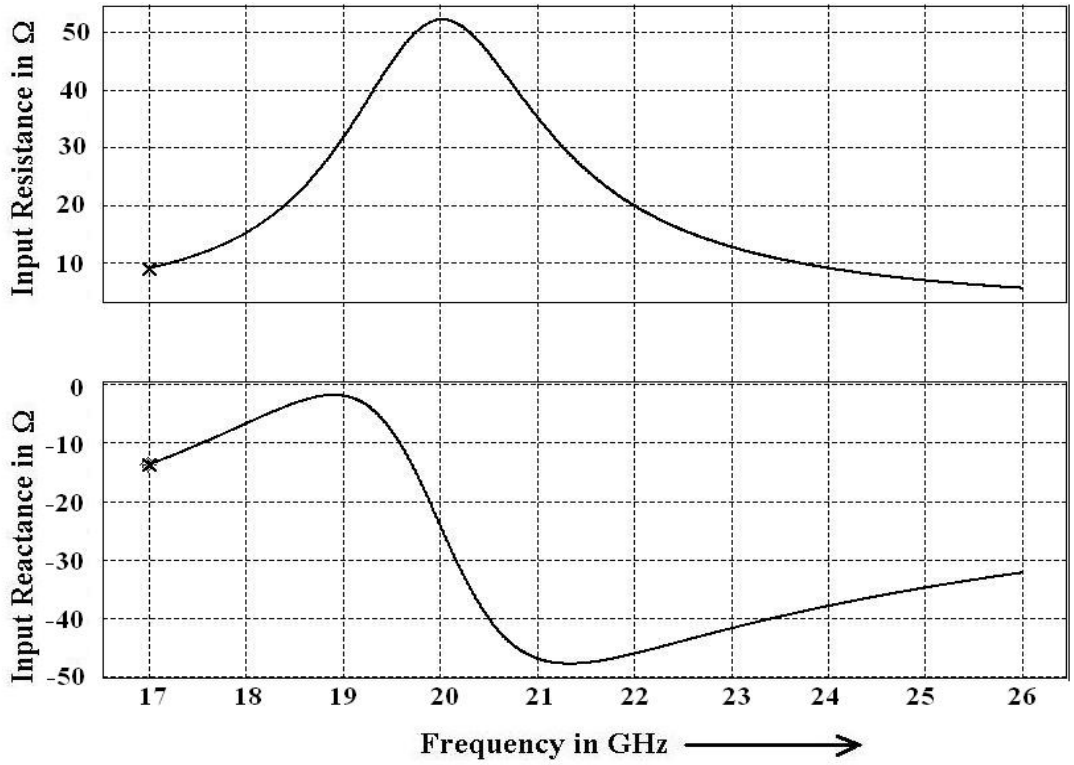

Figure 4.19: Input resistance and reactance of the circuit of Fig. 4.18

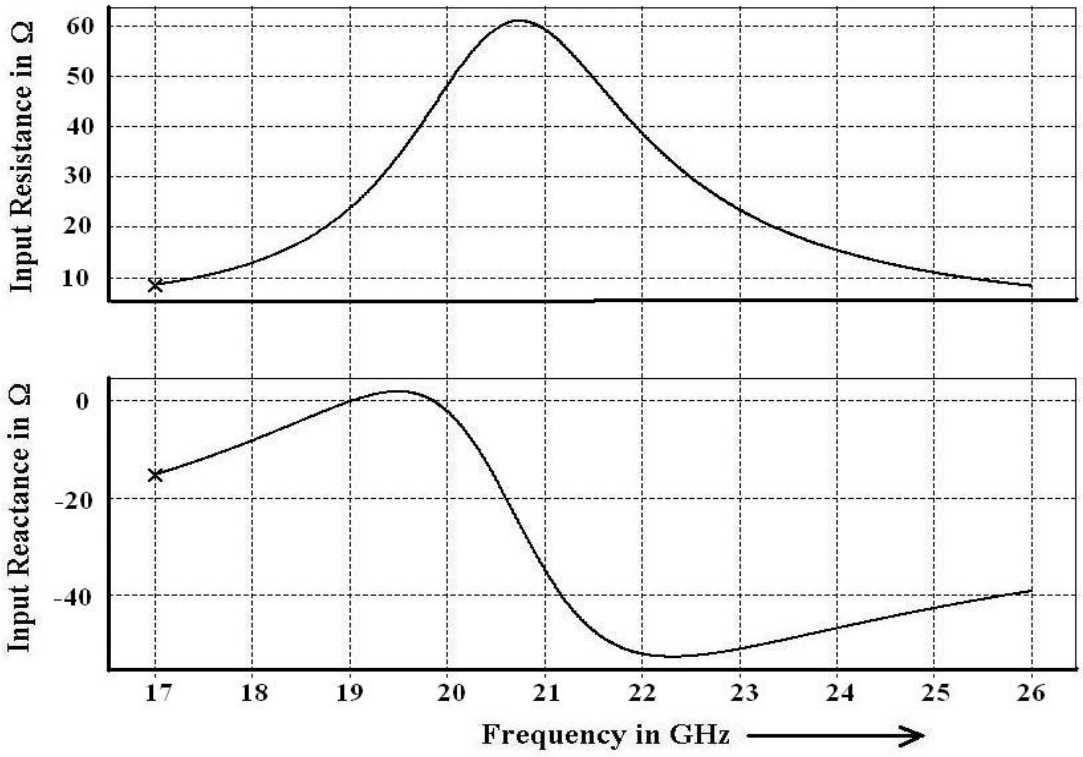

Figure 4.20: Input resistance and reactance of the circuit of Fig. 4.18 after the adjustment of C_{RF}

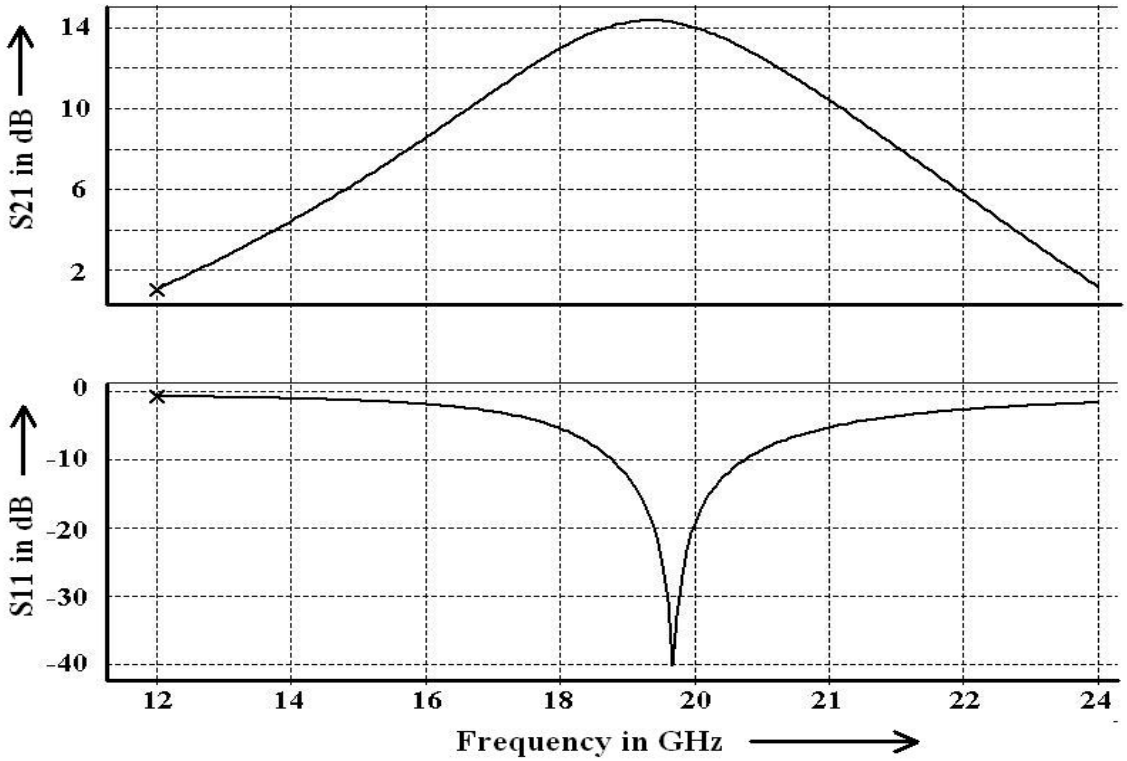

Figure 4.21: S21 versus frequency of the circuit of Fig. 4.18

Gain and input matching parameters (S21 and S11) are plotted in Fig.4.21. S21 is now more than 14 dB. It can be compared with the gain response of Fig. 4.7 to realize that, exclusion of the source degenerating inductor improves the gain by more than 4 dB. S11 is -40 dB near the center frequency. So, S21 and S11 of Fig. 4.21 assures good input matching of the circuit.

Now, let us come to the question of input noise matching. Noise figure (NF) and the minimum noise figure (NF_{min}) of the circuit is plotted in Fig. 4.22. NF and NF_{min} never touched each other, unlike the noise responses of the source degenerated LNA depicted in Fig. 4.6. It implies that, the input noise matching is not as good as it was when there was source degeneration. NF is now 3.8 dB at the center frequency, whereas it was 4.4 dB in Fig. 4.6 and the NF_{min} curve also dropped by about 1.5 dB. Both NF and NF_{min} decreased because the noise contribution of the internal resistance of the source degenerating inductor is no longer present. So, the minimum noise figure that can be reached now has to be lower.

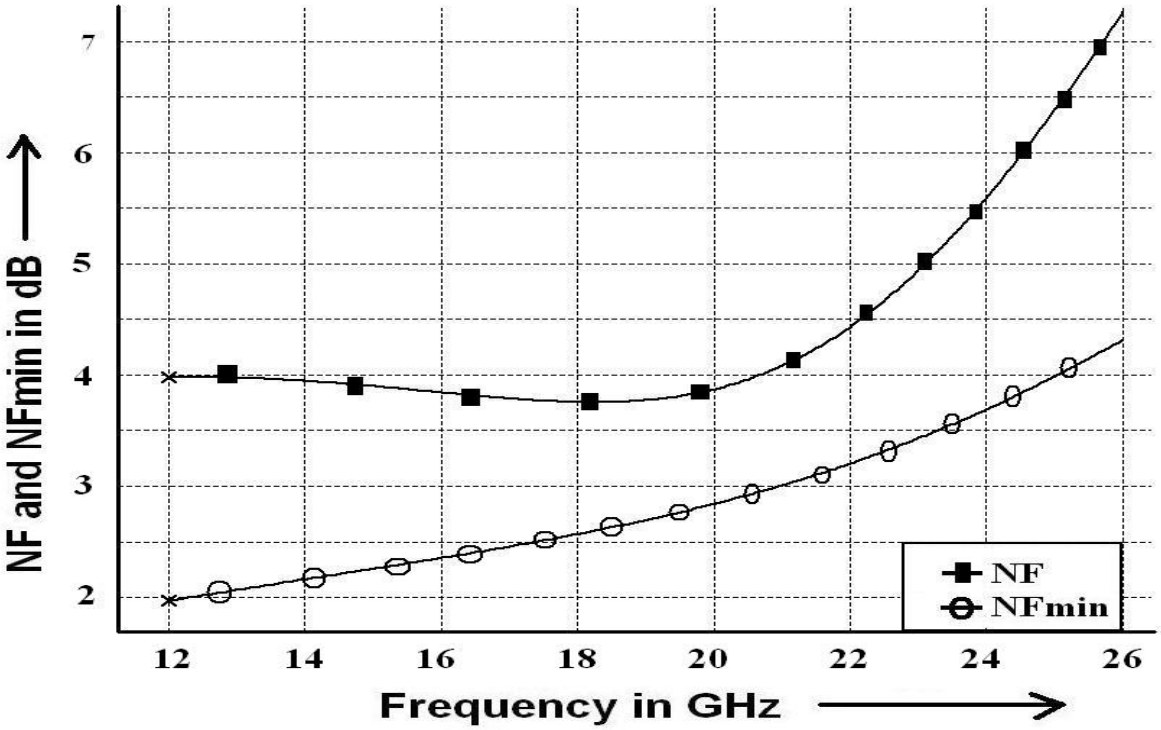

Figure 4.22: NF and NF_{min} versus frequency of the circuit of Fig. 4.18

On the other hand, NF curve did not reach NF_{min} because, now $L_s = 0$ in (4.4). That is why the new optimum impedance, Z_{opt}(new) for noise matching is now,

$$Z_{opt}(\text{new}) = \text{Re}\left[Z_{opt}(\text{old}) \right] - m\frac{1}{sC_{gs}} \qquad 4.12$$

This implies,

$$\text{Im}\left[Z_{opt}(\text{new}) \right] = \text{Im}\left[Z_{opt}(\text{old}) \right] + sL_s \qquad 4.13$$

Here, Z_{opt}(old) is the optimum impedance of (4.4).

A 160 pH source degenerating inductor was used in previous circuit. Since, $\text{Im}[Z_{opt}(\text{old})] = \text{Im}[Zin^*] = 0$, so, $\text{Im}[Z_{opt}(\text{new})] = sL_s = 20j\ \Omega$ at 20 GHz. L_{RF} and C_{RF} of the half circuit of Fig. 4.18 was adjusted to get an input reactance of 20j Ω at 20 GHz and it is shown in Fig. 4.23. The corresponding noise response can be found in Fig. 4.24, where again the NF reached NF_{min} at the center frequency. So, now the noise matching is good in that point as argued here.

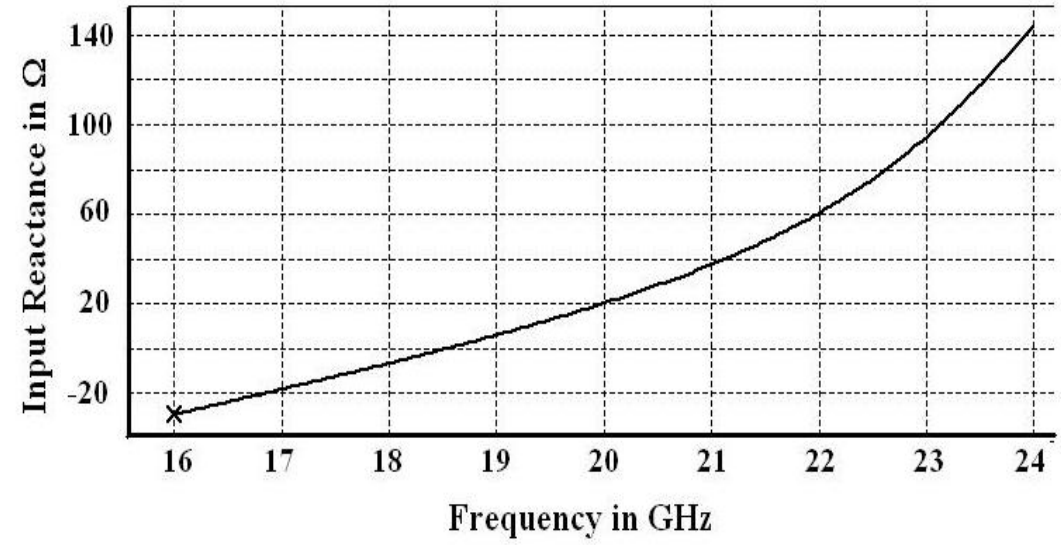

Figure 4.23: Input reactance of the circuit of Fig. 4.18 versus frequency

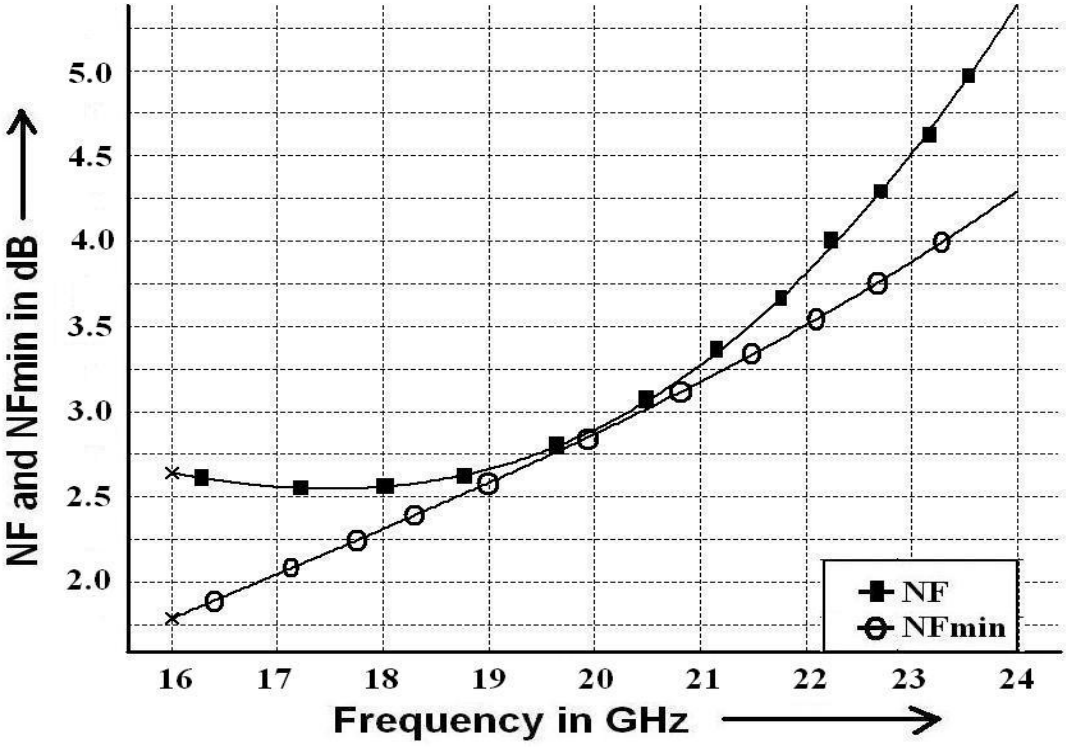

Figure 4.24: NF and NF_{min} of the circuit of Fig. 4.18 versus frequency after noise matching

S21 and S11 of the noise matched circuit are given in Fig. 4.25, where S21 decreased by about 3 dB comparing to Fig. 4.21 and -4.5 dB S11 indicates poor input matchig. It implies that, noise matching spoiled the power matching of the input side of the amplifier. So, it can be concluded that, the assistance of external gate-source capacitance is

not required for simultaneous noise and power matching of a K-band LNA. But both type of matching is not possible at the same time excluding the source degenerating inductor, although it offers several other advantages. Some other issues regarding the source degenerating inductors are discussed in [39] from different perspective.

In this design, noise matching was traded off for good input power matching for the receiver has to work with very small signal, which will be needed to be amplified enough. Moreover, no matter the NF could reach the NF_{min} , about 4 dB NF will not be problemetic in this application since this receiver opts for detecting digital signal. That is why, the input port was matched for maximum power transfer. The input matching technique discussed here is used in some of the recent works such as [40] without detail explanation.

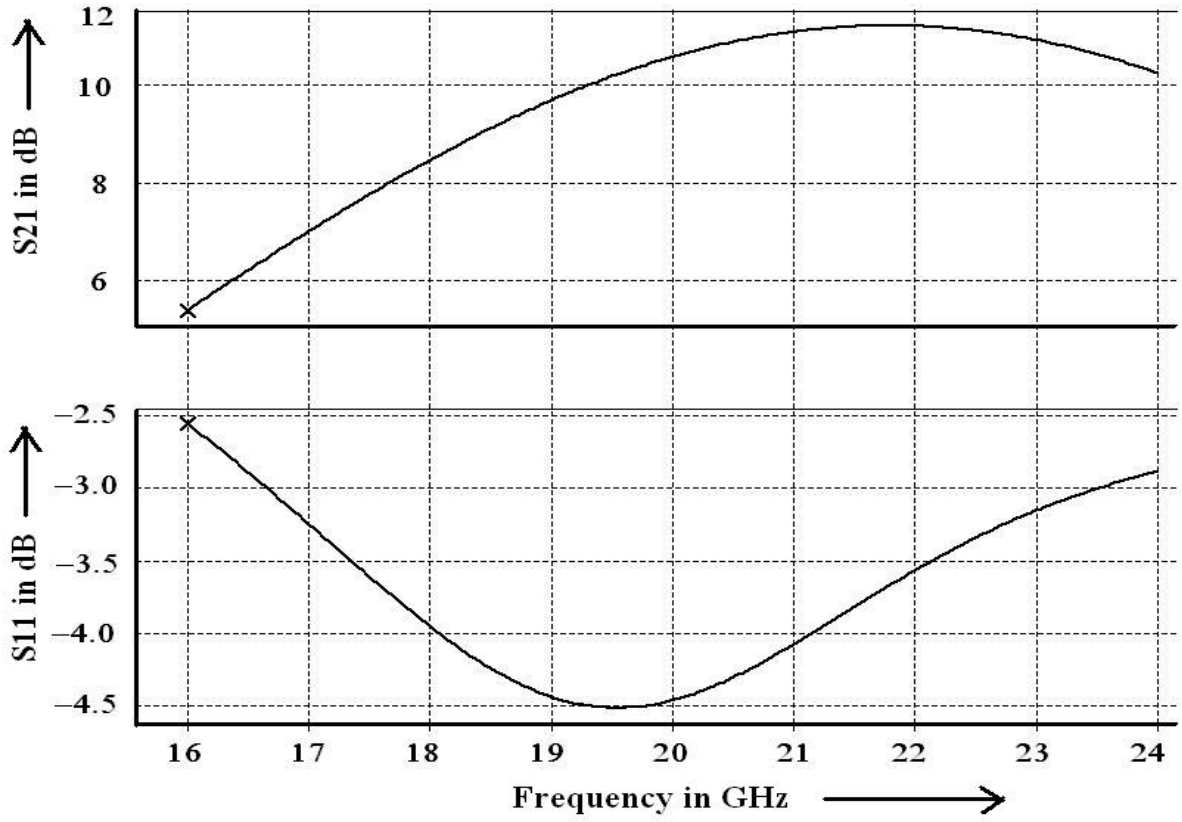

Figure 4.25: S21 and S11 of the circuit of Fig. 4.18 versus frequency after noise matching

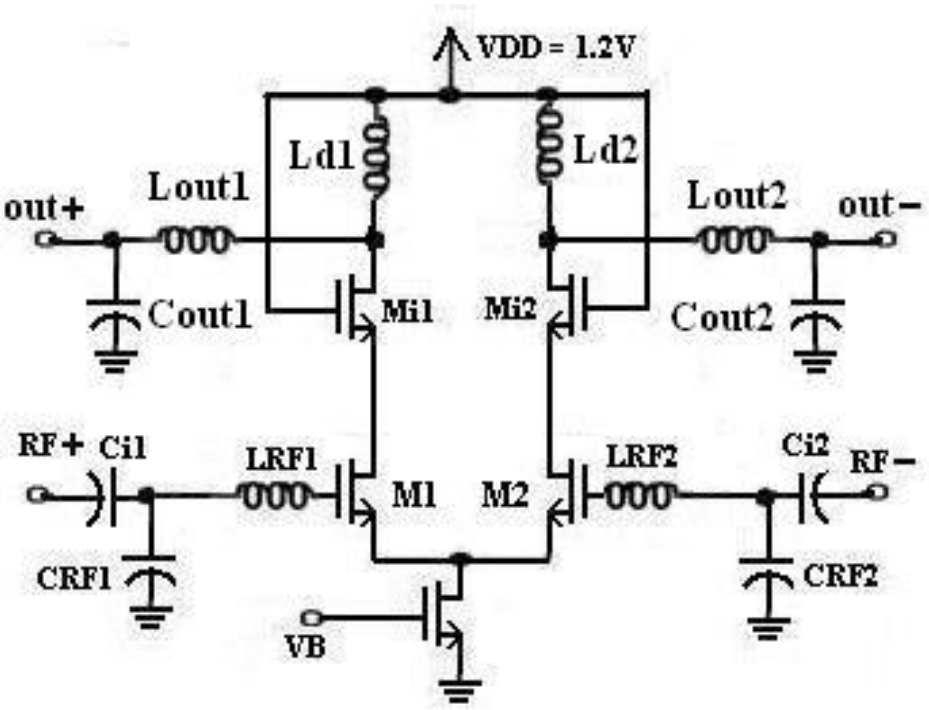

Figure 4.26: Complete 20 GHz differential low noise amplifier

Schematic diagram of the complete 20 GHz differential low noise amplifier is portrayed in Fig. 4.26. Here, L_{out1}, L_{out2}, C_{out1} and C_{out2} matches the output port by the similar fashion the input matching networks did. No dc blocking capacitor was used at the output because this port will be feeding dc biasing current to the following mixer circuit. This part will be discussed in more detail in the next chapter. Anyway, rest of the elements of this circuit performs the same function as those of 21 GHz differential low noise amplifier discussed in the previous section.

4.2.2 Frequency Response and Linearity of the 20 GHz Differential LNA

The 20 GHz differential low noise amplifier was designed and simulated in Cadence Spectre. Frequency responses and linearity of the circuit are shown in this section. The power gain (S21) is plotted in Fig. 4.27. The maximum gain is 14 dB at the center frequency 20 GHz with 2.9 GHz bandwidth (18.4 GHz - 21.3 GHz). Reverse isolation of the amplifier (S12) is less than -26 dB as can be found in Fig. 4.28. Input-output matching parameters (S11 and S22) are shown in Fig. 4.29. They are -28 dB and -26 dB respectively near the center frequency. These low values of matching parameters assure that, the signal reflections from the input and output ports of the amplifier will be very low. Fig. 4.30 justifies this argument where the VSWR from the input and output ports (VSWR1 and VSWR2) are shown and both are close to zero at 20 GHz. Also in Fig. 4.31, the values of available power gain (GA), transducer power gain (GT) and the overall power gain (GP) are close in the center frequency which is an indicator of good matching. So, based on these responses, it can be inferred that the power matching of the amplifier was quite satisfactory.

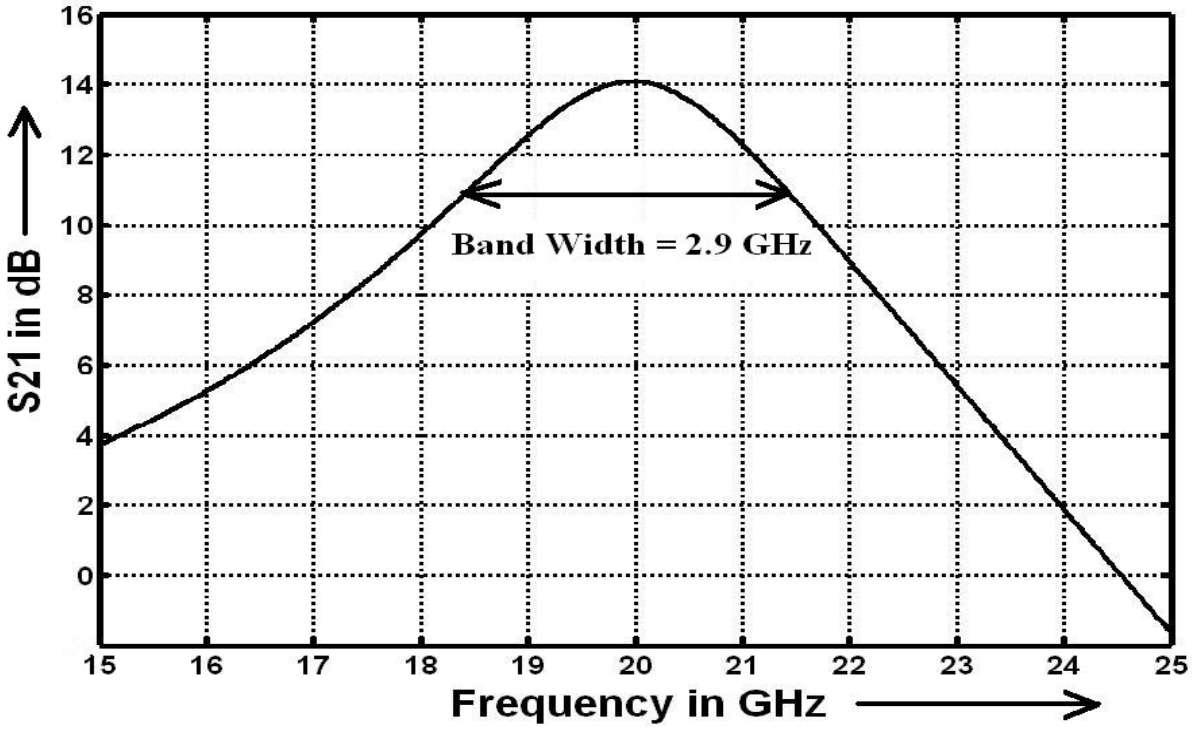

Figure 4.27: S21 versus frequency of the 20 GHz differential LNA

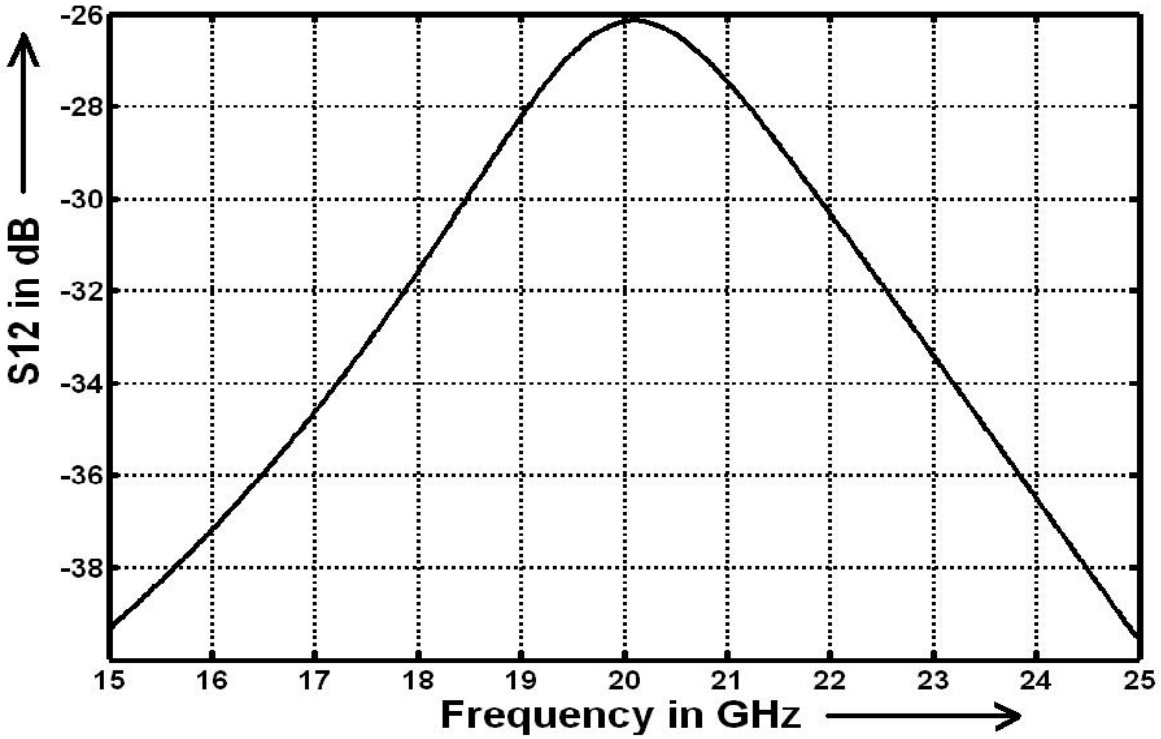

Figure 4.28: S12 versus frequency of the 20 GHz differential LNA

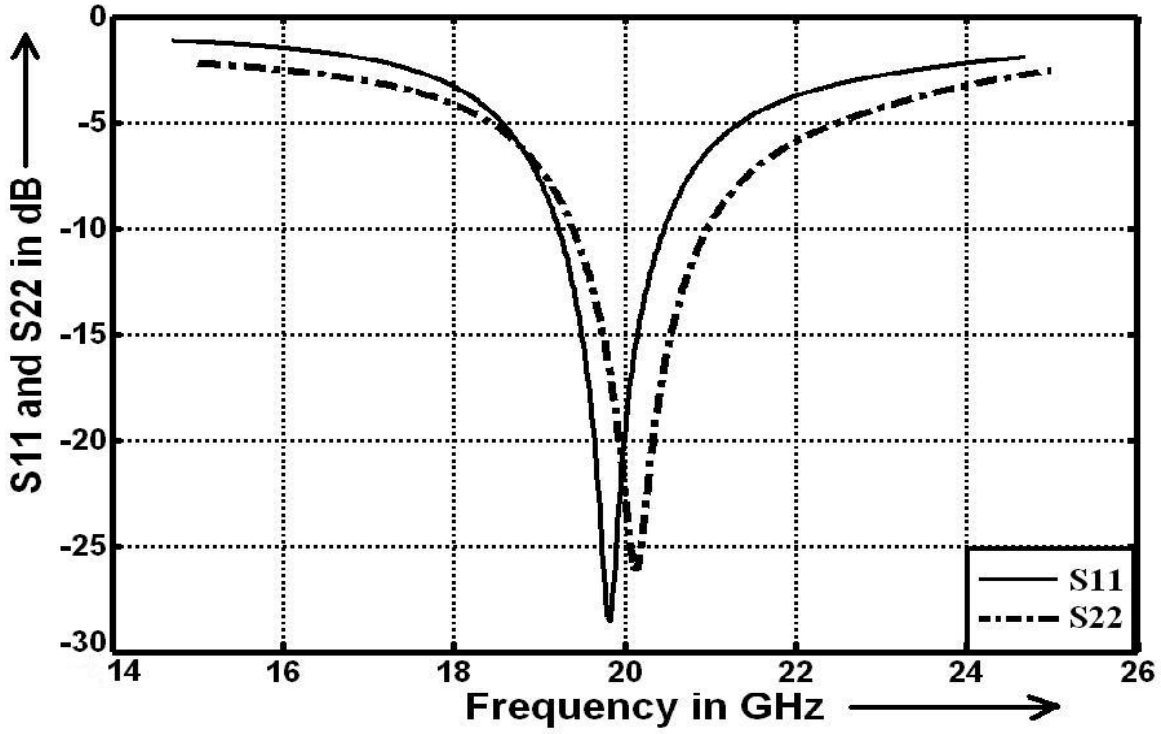

Figure 4.29: S11 and S22 versus frequency of the 20 GHz differential LNA

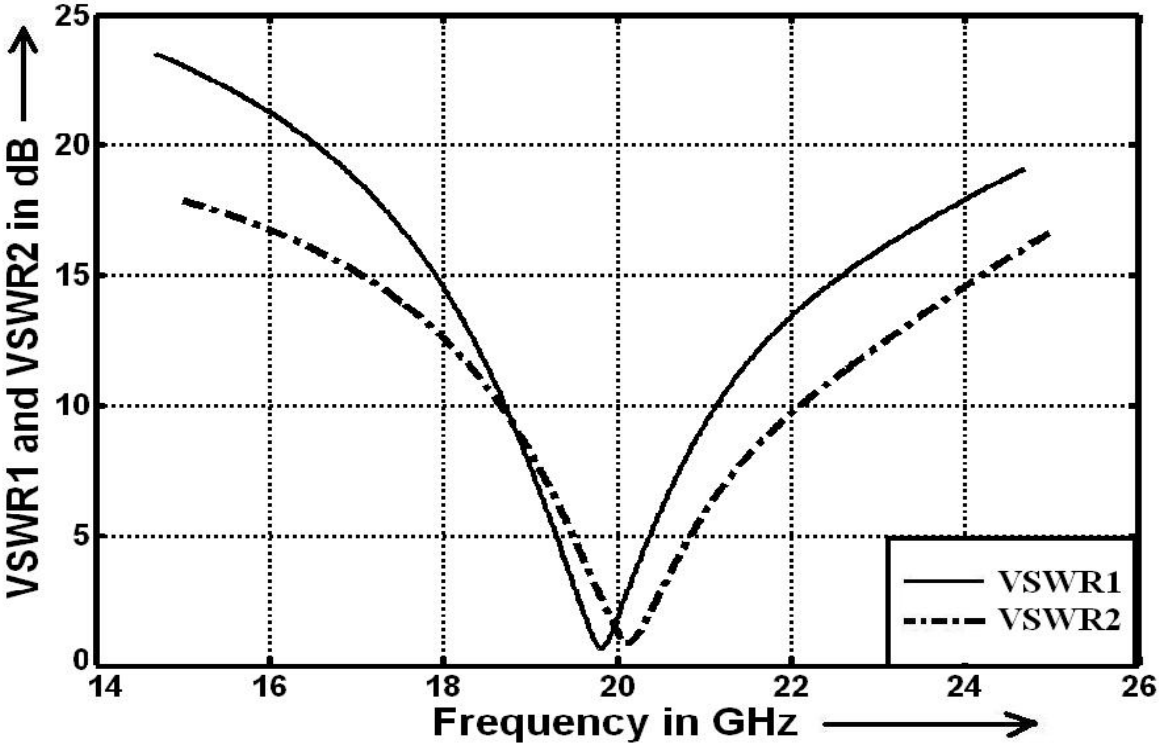

Figure 4.30: VSWR1 and VSWR2 versus frequency of the 20 GHz differential LNA

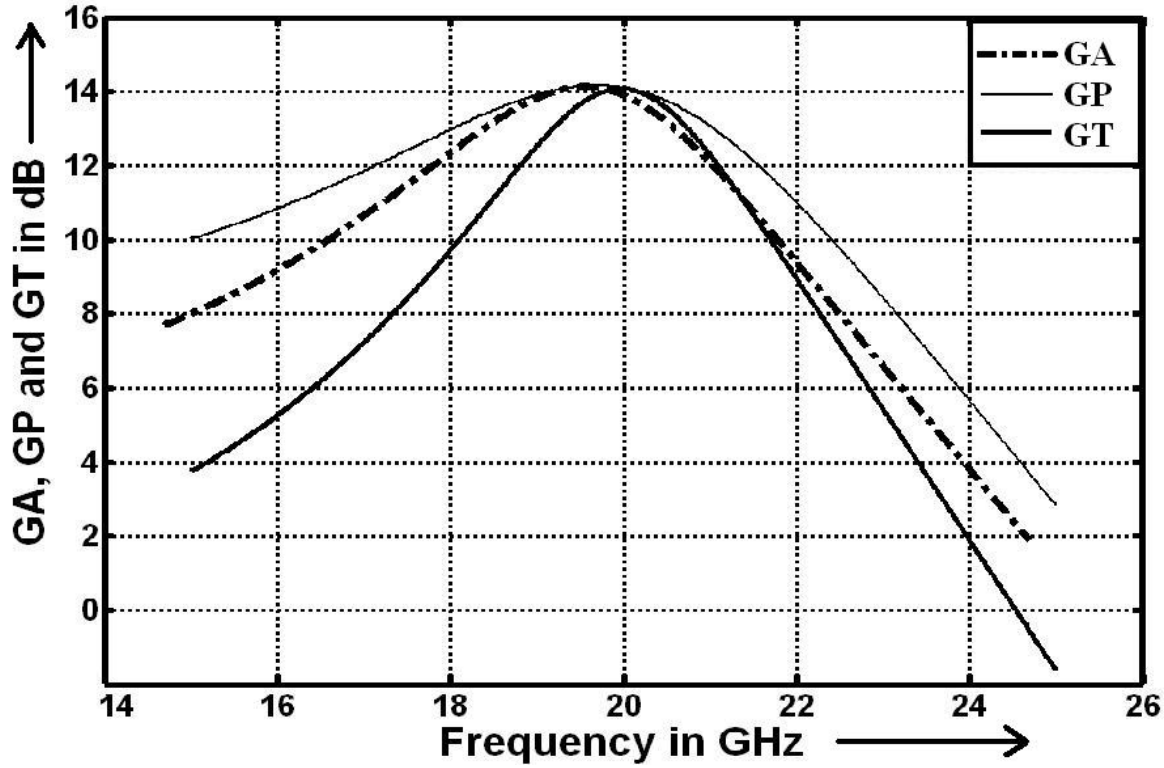

Figure 4.31: GA, GP and GT versus frequency of the 20 GHz differential LNA

Noise figure (NF) and the minimum noise figure (NFmin) of the amplifier are plotted in Fig. 4.32. They are 4.6 dB and 3.4 dB respectively at the center frequency, slightly higher than those of Fig. 4.22 because now the tail current source transistor is adding some noise to the circuit. The input referred 1 dB compression point of the circuit is shown in Fig. 4.33. It is about -14 dBm, lower than that of the source degenerated LNA showed in Fig. 4.10. This is because; the compression point depends on both the output signal headroom and on the gain of the amplifier. If the later one increases with the former limit unchanged, then the output signal limit will be reached at lower input power. This is what happened in this case. Although linearity improvement techniques are proposed in some of the recent works like [41-42], but that will not be required in this application for the amplifier will be working with very small signal. So the linearity limit is less likely to be reached. The 3rd harmonic distortion point of the amplifier can be found in Fig. 4.34. The input referred 3rd order intercept point (IIP3) is about -5 dBm, about 9 dBm higher than the compression point that ensures that, linearity of the amplifier is limited by the gain compression point, not by the harmonic distortion limit. The Rollet stability factor (Kf) is plotted in Fig. 4.35. It is greater than one in all frequencies. That means, this circuit will be unconditionally stable in all frequencies of interest. Thus, possibility of instability due to higher gain is eliminated.

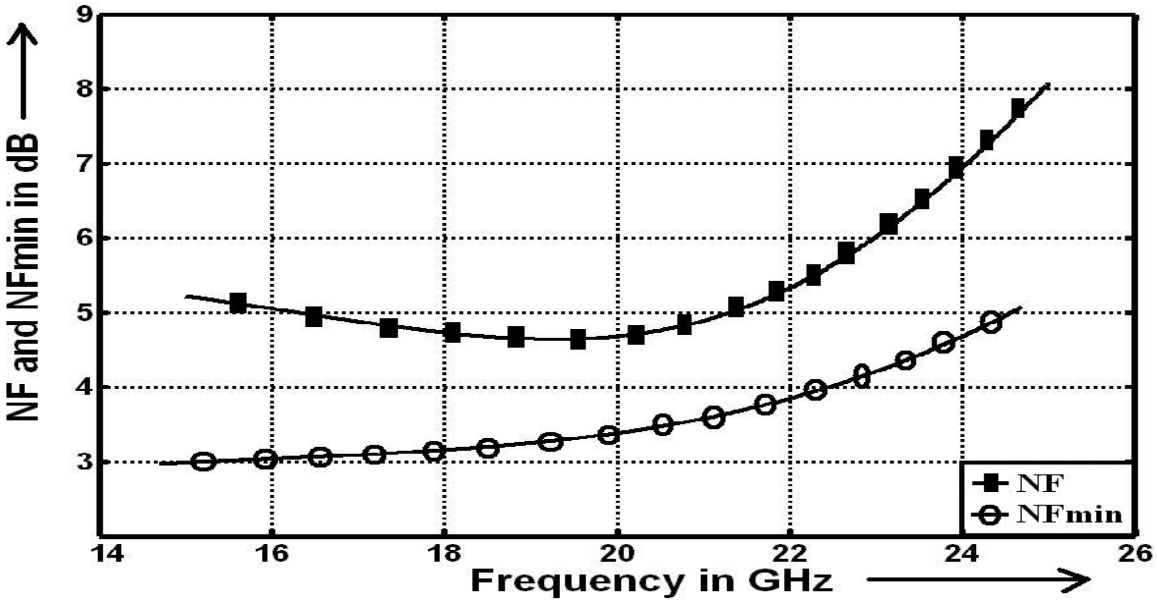

Figure 4.32: Noise Figure (NF) and Minimum Noise Figure (NF_{min}) versus frequency of the 20 GHz differential LNA

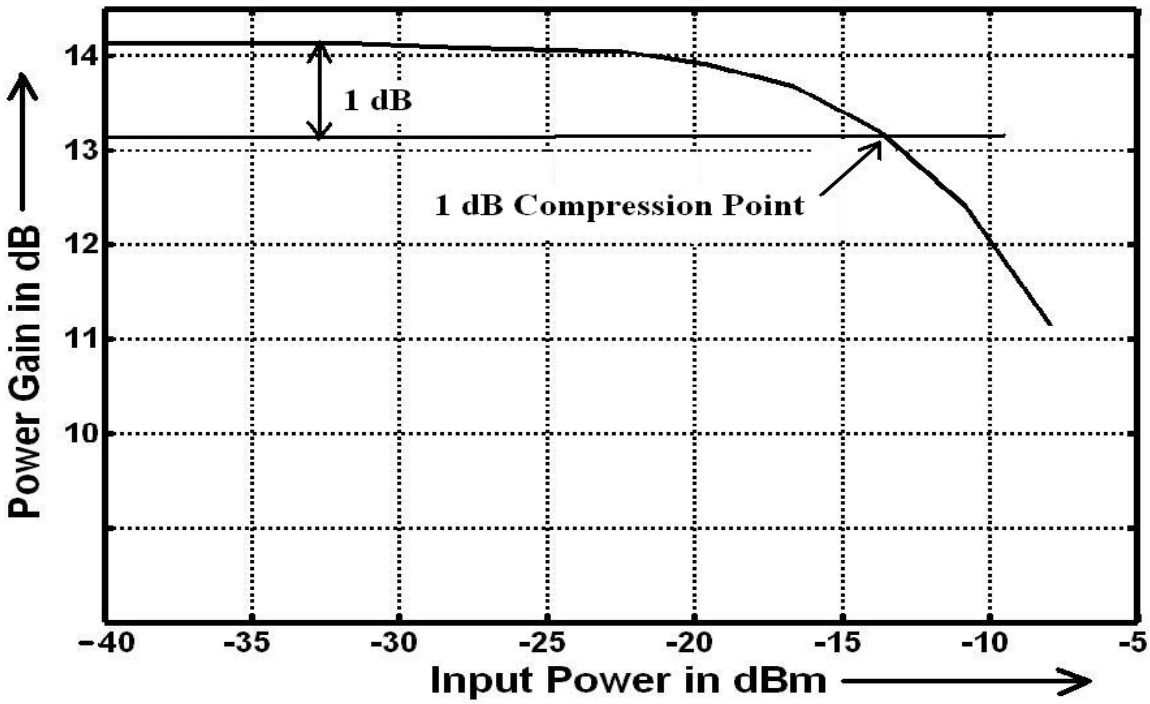

Figure 4.33: Gain versus input power of the 20 GHz differential LNA

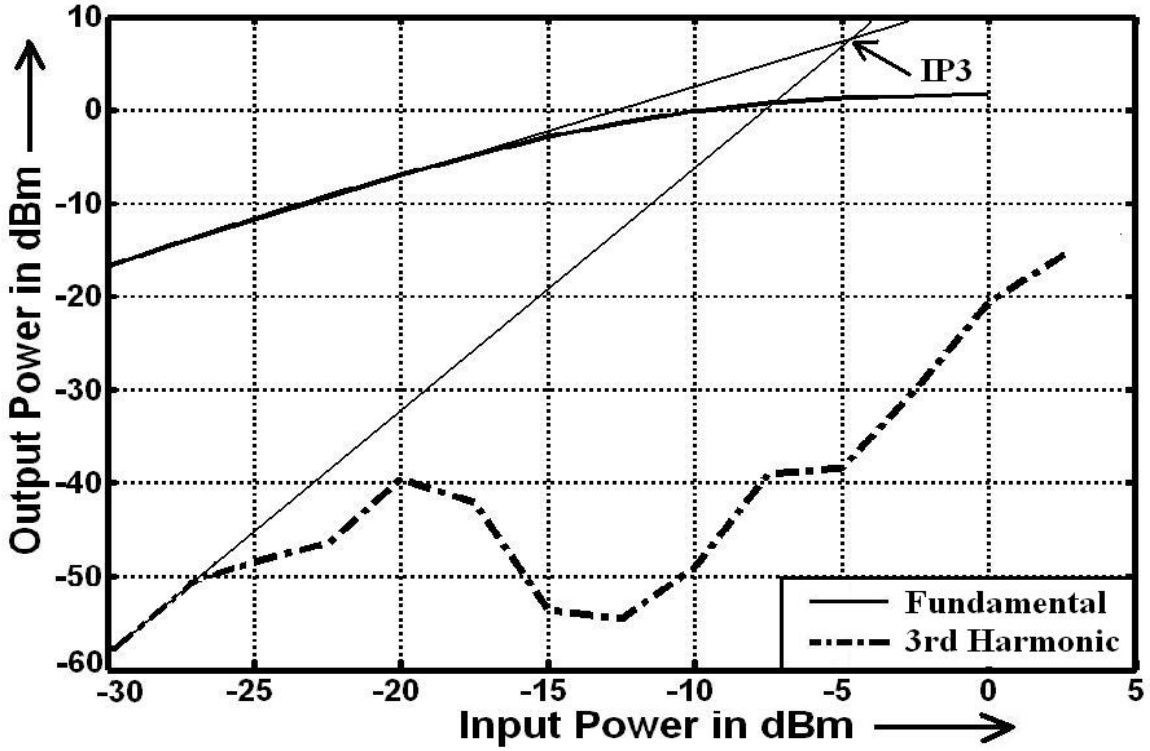

Figure 4.34: Illustration of the 3rd order intercept point (IP3) of the 20 GHz differential LNA

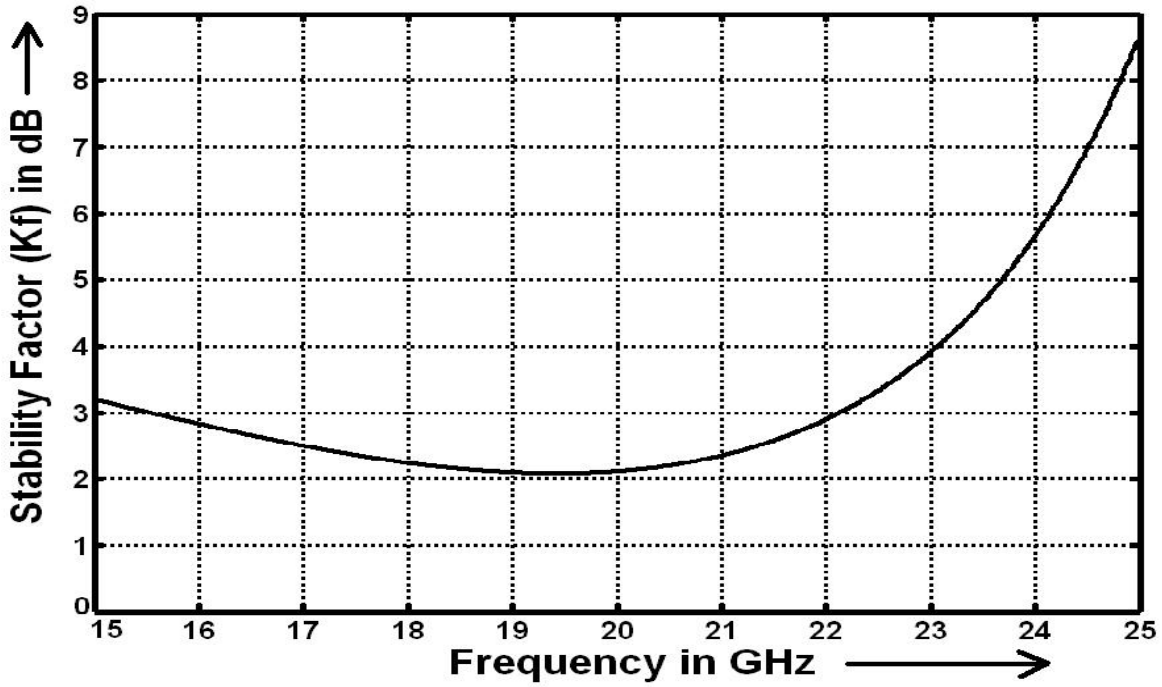

Figure 4.35: Rollet stability factor (Kf) of the 20 GHz differential LNA

4.2.3 Transient Response of the 20 GHz Differential LNA

To observe the time domain response of the amplifier, the double balanced up-converted signal generated in previous chapter was transmitted and received by a pair of on-chip integrated antenna which was then amplified by the 20 GHz differential LNA designed in this chapter. The system is drawn in Fig. 4.36 and the corresponding signals are shown in Fig. 4.37. Note that, the transmitted and received signals were plotted in Fig. 3.22, where the signal experienced about -18 dB attenuation on its way through the channel. Now, this received signal enjoys about 14.5 dB gain offered by the LNA. Delays at different nodes can be observed in the figure. But, insignificant distortion ensures that, the performance of this LNA will be quite promising in this application.

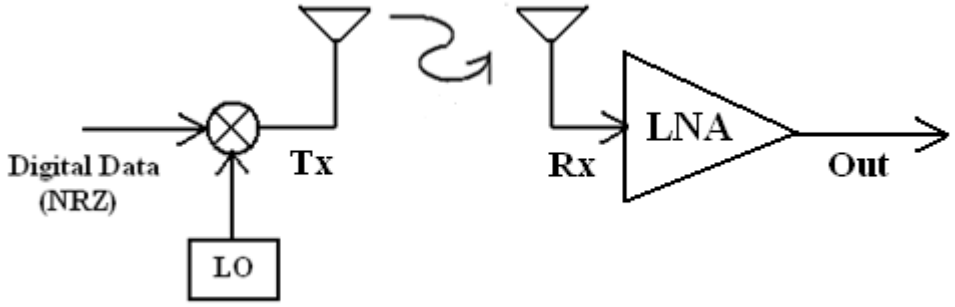

Figure 4.36: System for observing Transmitted (Tx), Received (Rx) and Amplified (out) signals in time domain

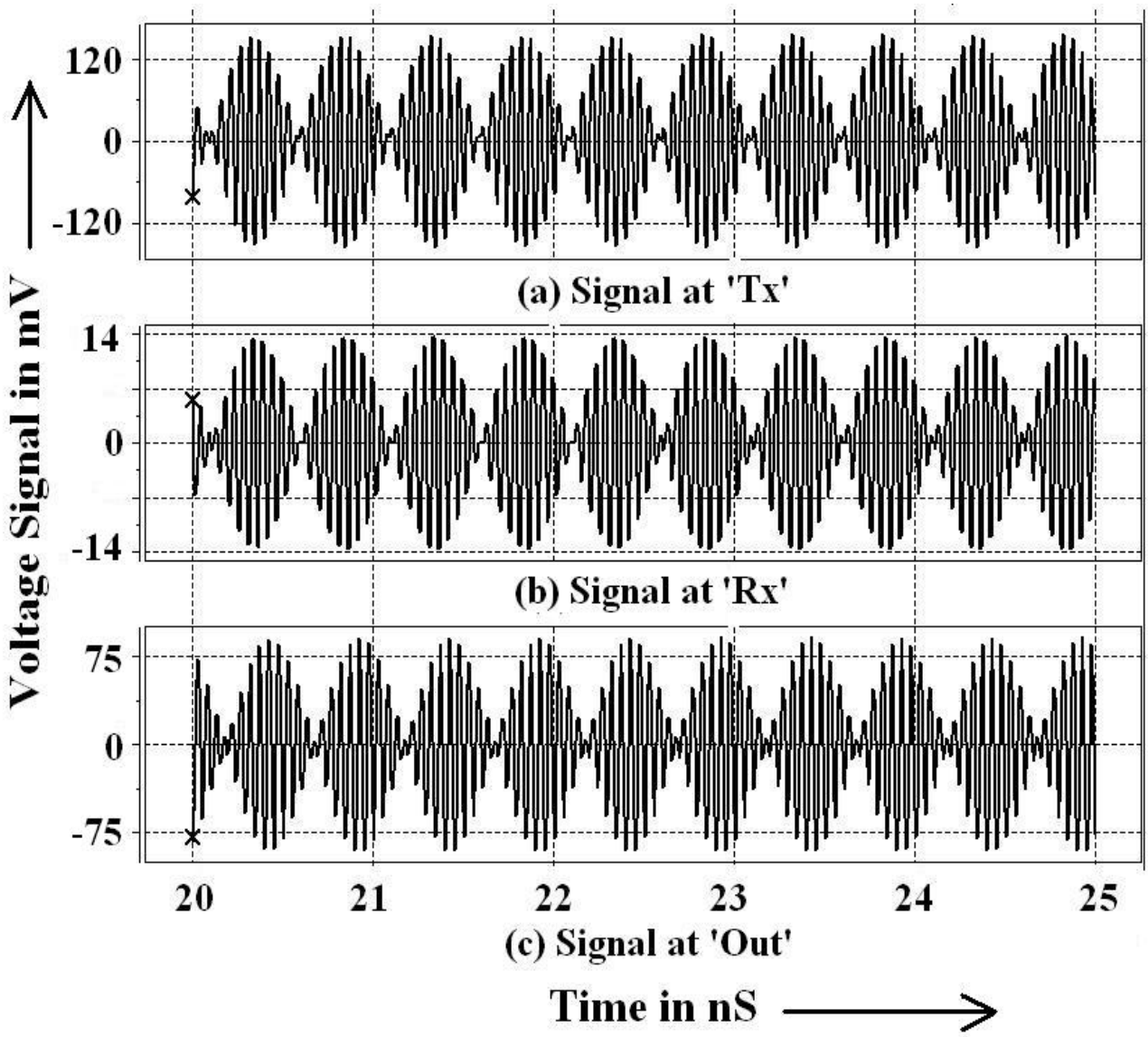

Figure 4.37: Signals at the nodes of Fig. 4.36

4.2.4 Area and Power Requirements of the 20 GHz Differential LNA

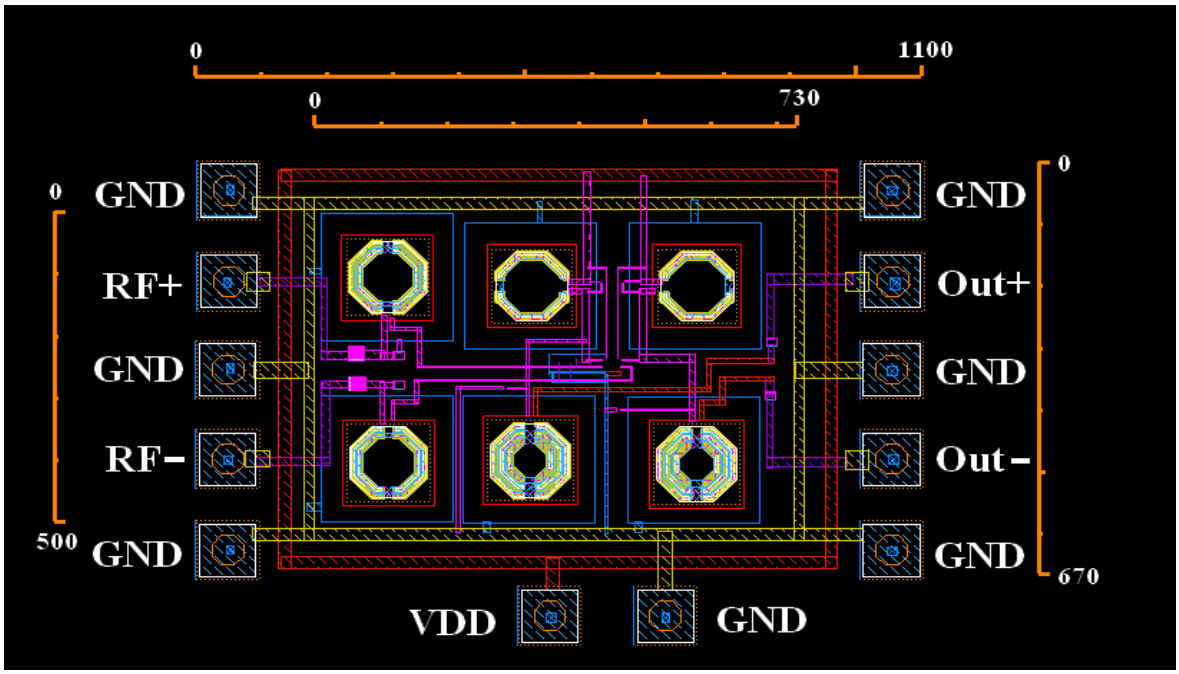

Figure 4.38: Layout of the 20 GHz differential low noise amplifier

The layout of the 20 GHz low noise amplifier is given in Fig. 4.38. Total six on-chip inductors were required including the input-output matching networks, as can be found in the schematic circuit of Fig. 4.26. It occupies 0.73mm X 0.5mm = 0.365mm^2 and 1.1mm X 0.67mm = 0.737mm^2 area excluding and including probe pads respectively. This circuit consumes about 17 mW power from a 1.2 V power supply with the biasing circuitry included. Therefore, space and power requirements together with the simulated responses of this 20 GHz differential low noise amplifier ensure its commitments for this on-chip wireless interconnect system. Performance of this circuit is compared with state of the art in Table 4.1.

Table 4.1: Comparison of the 20 GHz differential LNA with state of the art LNAs

Reference	This Work*	[22]	[38]*	[84]	[108]*
Technology	90 nm CMOS	0.18 µm CMOS	0.13 µm CMOS	0.18 µm BiCMOS	0.35 µm CMOS
No. of Stages	1 (diff.)	3	1 (diff)	2	1 (diff)
Peak Gain (S21)	14 dB at 20 GHz	15 dB at 21.8 GHz	9.72 dB at 21 GHz	12 dB at 27 GHz	3.62 dB at 18.2 GHz
Bandwidth (GHz)	2.9	N/A	4	9	7.9
Reverse Isolation (S12 in dB)	-26	N/A	-26.4	N/A	-6.47
Input Matching (S11 in dB)	-27.5	-21	-21.3	< -12	-16.3
Output Matching (S22 in dB)	-26	N/A	-20	< -20	-7.72
NF in dB	4.8	6	4.4	4.5	0.42
1 dB Compression Point in dBm	-14	N/A	-7.24	-6.3 (IIP3)	-14.6
Power Consumption (mW)	17	24	20.75	13	0.5
Area Requirement (mm^2)	0.365	0.5	N/A	0.25	N/A

*schematic simulation results

This chapter discussed on the design of a 21 GHz source-degenerated differential LNA and its simulated responses were also demonstrated. After identifying its merits and demerits, a 20 GHz differential LNA was designed with a new input matching to optimize performance for this application. Response of the circuit was found quite promising. This circuit will be employed in the receiver front-end in subsequent chapters to detect the transmitted UWB bit streams.

CHAPTER 5

UNIFYING LNA AND MIXER FOR THE RECEIVER FRONT-END

The receiver front-end can be defined as the part of the receiver, which deals with received high frequency signals i.e. before down conversion. In that sense, the LNA, mixer, the delay circuit and the low pass filter (LPF) of Fig. 2.1 forms the receiver front-end for that self synchronized TR-UWB system. But, generally most of the receivers are not self-synchronized, so a local oscillator (LO) usually replaces the delay circuit. That is why, traditionally receiver front-end means the combination of LNA, mixer and LPF after the receiving antenna and this terminology will be used in this work as well.

This chapter will discuss on the merits and demerits of different types of mixer topologies, will choose the most suitable one for this particular application and will explain its operations in detail. Then a direct conversion or zero IF (Intermediate Frequency) mixer will be designed which will down convert the received high frequency signal directly to its baseband without any intermediate down conversion. More specifically, this mixer will be capable of multiplying two small signals of same frequency, as needed in the receiver of Fig. 2.1, where delayed version of a signal is multiplied with the original signal. After designing the mixer, the LNA and the mixer will be unified to end up to a single-circuit receiver front-end. The achievements and the trade offs will be examined. Performance of the circuit will be verified judiciously based on simulated responses of the circuit. At last, this receiver will be employed to detect a BPSK (Binary Phase Shift Keying) signal and then to a self synchronized system such as DPSK (Differential Phase Shift Keying) receiver. Thus, the commitment of the circuit will be verified in time domain as well.

5.1 Choosing a Suitable Mixer Topology

Employing a number of RF circuits, in most of the cases, this is the receiving section of the transceiver which is bulky and power hungry. In implies that, judicious design of the receiver front ends is a good way to make these transceivers economical in terms of power and space. Again, choosing a suitable mixer topology is a very important design step since; other important issues are involved here like conversion gain, noise, linearity, isolations within and between input-output ports and so on. So, let us put some light on the merits and demerits of different mixer topologies to weigh them for this application.

The square law mixer designed in chapter 3 can not be used here, because it was designed to multiply two signals of significantly different frequencies so as to up or down convert one of them. Matching networks of each input ports were designed to pass the input signal but to block signals of different frequencies to improve input port isolation. So, if that square law mixer is to multiply a couple of signals of same frequency, then both the input ports will have to be matched for the same frequency and that is why they will be transparent to each other. Thus, there will be too much leakage problems in the input side. Moreover, designing the input matching networks will be complicated because of the loading effects.

Passive mixer and bulk-driven mixers are among other choices. Schematic diagram of the core of passive mixer is given in Fig. 5.1. Here the major problem is lack of isolation between ports for they are isolated only by gate-source or gate-drain capacitors of the transistors, which is poor in high frequencies such as in 20 GHz. Although, this problem is encountered in some of the recent works by using on-chip baluns or transformers, but again, these are area consuming elements and are inconvenient in silicon chip. Such one can be found in [26]. Still, another major problem of this mixer is high conversion loss. This is obvious because, passive circuits can never provide any gain. Conversion loss of [26] is in between 7 to 10 dB. That is why; this topology will not be suitable in this application because, this receiver will have to handle very small signals which will be fed

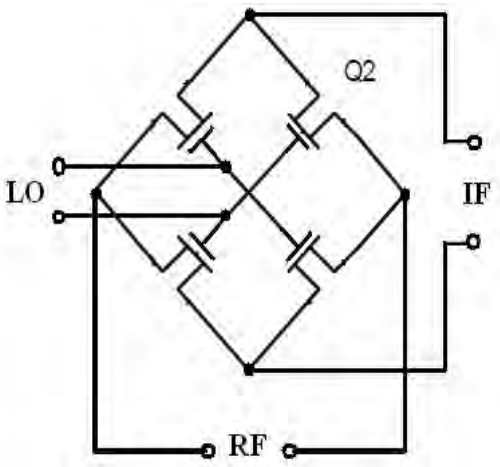

Figure 5.1: Core of a passive mixer

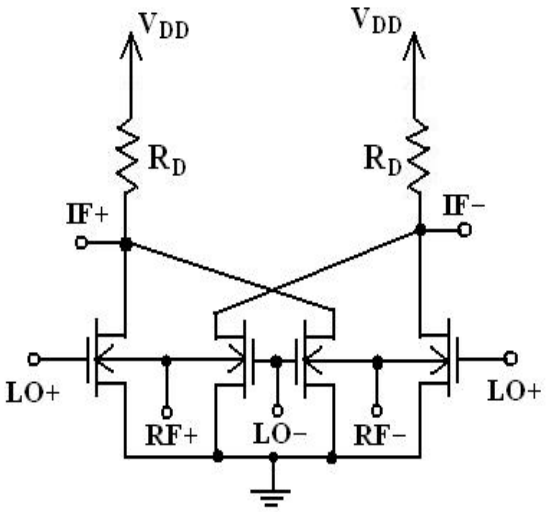

Figure 5.2: A basic bulk-driven mixer

to a comparator. So, largest possible signal will drive the comparator if highest possible conversion gain is available and then, the comparator will be able to offer its optimum performance. Usually passive mixers are used in large signal applications.

Schematic diagram of the core of bulk-driven mixer is shown in Fig. 5.2. Although, these types of mixers can provide good conversion gain [43-46], but again, they are criticized for their poor input port isolation, as they are isolated only by the parasitic capacitors of the driving transistors. Another problem of this topology is high noise figure, because one of the input is fed to a diffusion body i.e. substrate terminal of the transistor. For example, NF of [44] and [45] are 17 dB and 26 dB respectively while their gains are 13 dB and 13.6 dB in order. In small signal applications, this high noise may mask the information signal. These limitations make the topology inappropriate for this application.

Next option is the Gilbert's mixer. Schematic diagram of a basic Gilbert's mixer is drawn in Fig. 5.3. Although, this topology needs more space and power than other topologies discussed earlier, but it offers good conversion gain, moderate noise figure, good isolation and so on. In short, Gilbert's Mixer is most convenient to design for high frequency applications. That is why; most of the mixers in this frequency range, like those of [22] and [47-55] preferred this topology. This structure will also be preferred in this work to multiply two small signals. Note that, Gilbert's mixers can be used either for

frequency conversion or as small signal multipliers. Before, moving to the detail of circuit design, let us discuss on the differences between these two applications of the Gilbert's mixer.

5.2 Analysis of Gilbert's Mixer

As mentioned in previous section, Gilbert's mixers can be used either as frequency up or down converters or as small signal multipliers. Unlike the later case, one of the inputs of the former one is a large signal, most of the time generated by local oscillators. So the corresponding input transistors are not biased, while all the input transistors are to be biased properly in later application. This is the main difference between those two configurations. But, unfortunately, most of the relevant texts like [29], [56-57] analyze Gilbert's mixer as frequency converter. Analysis of this circuit as small signal multiplier is rare. However, both types of analysis will be archived in this section.

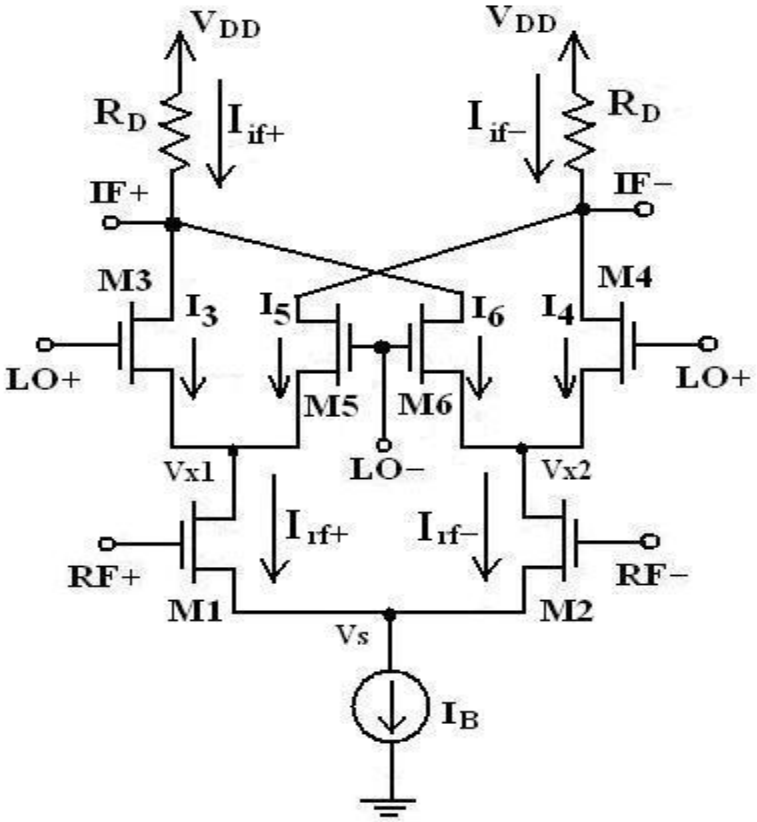

Figure 5.3: A basic Gilbert's mixer

5.2.1 Gilbert's Mixer as Frequency Converter

In Fig. 5.3, local oscillator signal, LO+ and LO- are large signals when the mixer is employed as frequency converter. That means, at a time M3, M4 or M5, M6 are 'ON', when LO+ or LO- is 'High' respectively, thus M3-M6 form a switching stage.

Here, $$Irf+ = \frac{IB}{2} + g_{m,rf}v_{rf+} \qquad 5.1$$

$$Irf- = \frac{IB}{2} + g_{m,rf}v_{rf-} \qquad 5.2$$

$g_{m,rf}$ is the trans-conductance of M1 and M2 transistors, v_{rf+} and v_{rf-} are differential RF inputs.

Now, output signal, $v_{out} = v_{IF+} - v_{IF-} = (V_{DD} - I_{if+}R_D) - (V_{DD} - I_{if-}R_D)$

$$= (I_{if-} - I_{if+}).R_D \qquad 5.3$$

Where, v_{IF+} and v_{IF-} are the voltages at nodes IF+ and IF- respectively. Again, M3 and M4 are 'ON' when LO+ is 'High' i.e. LO- is 'Low'. Then, I_{if+} and I_{if-} equal to I_{rf+} and I_{rf-} respectively and so from (5.3),

$$v_{out} = (I_{rf-} - I_{rf+}).R_D = g_{m,rf} .(v_{rf-} - v_{rf+}).R_D \qquad 5.4$$

Similarly, M5 and M6 are 'ON' when LO- is 'High' i.e. LO+ is 'Low'. In that case, I_{if+} and I_{if-} equal to I_{rf-} and I_{rf+} respectively and from (5.3),

$$v_{out} = (I_{rf+} - I_{rf-}).R_D = - g_{m,rf} .(v_{rf-} - v_{rf+}).R_D \qquad 5.5$$

note that, outputs of (5.4) and (5.5) are just phase shifted by 180^0 . This situation is shown in Fig. 5.4, where a 1 GHz sinusoidal signal at RF port was mixed with a 10 GHz bipolar LO signal and the resulting output is given in Fig. 5.4 (c). This output can be expressed simply as, $v_{out}(t) = G. v_{rf}(t).v_{lo}(t)$ 5.6

where, G is the gain of the circuit.

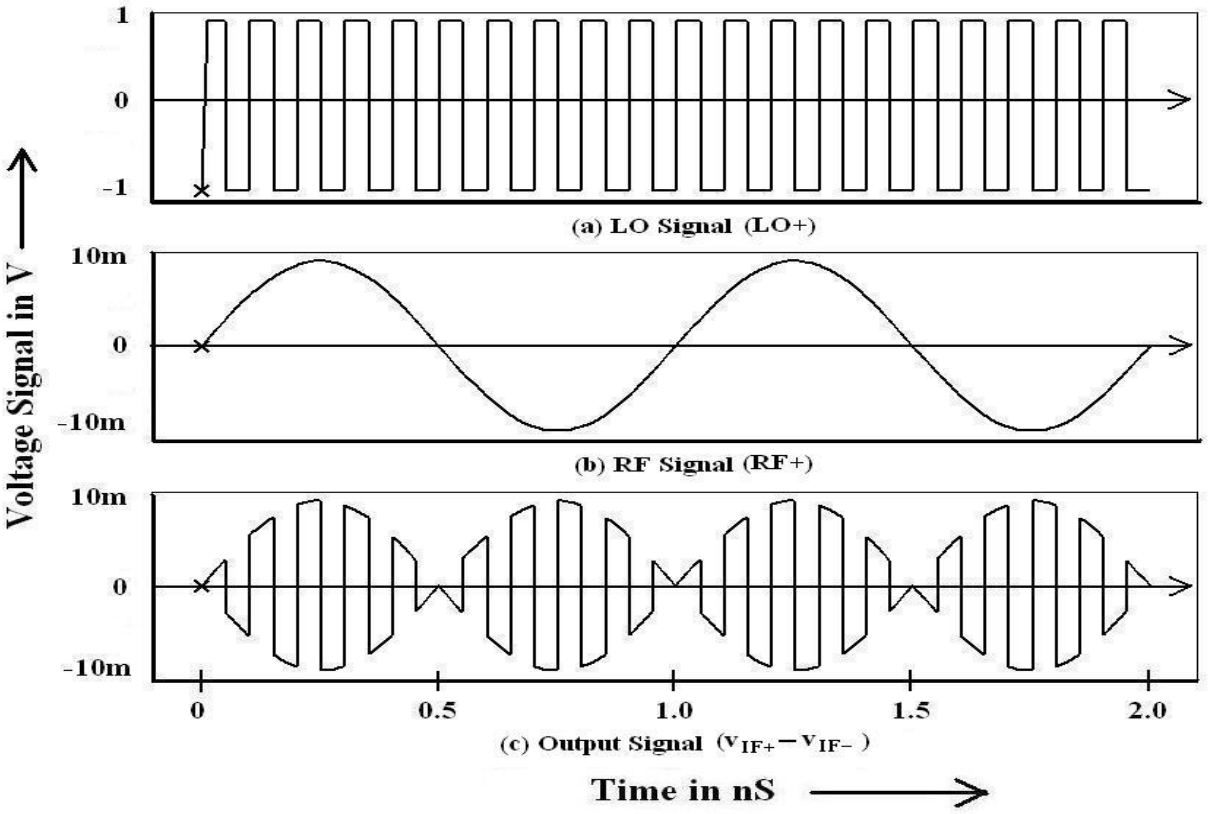

Figure 5.4: Input-Output signals of a Gilbert's mixer when working as frequency up-converter (only LO+ and RF+ are shown here. LO- and RF- are just 180^0 phase shifted)

Since, $v_{lo}(t)$ is a square wave, so application of Fourier's series expansion on (5.6) gives rise to,

$$v_{out}(t) = G.\,A_{rf}.\sin(\omega_{rf}.t).\left[\frac{Alo}{2} + \frac{2Alo}{\pi}.\cos(\omega_{lo}.t) - \frac{2Alo}{3\pi}.\cos(3\omega_{lo}.t) + \ldots..\right]$$

Or,

$$v_{out}(t) = G.\,A_{rf}.\left[\frac{Alo}{2} + \frac{Alo}{\pi}.\sin(\omega_{lo}.- \omega_{rf}).t + \frac{Alo}{\pi}.\sin(\omega_{lo}.+ \omega_{rf}).t - \frac{2Alo}{3\pi}.\sin(3\omega_{lo} - \omega_{rf}).t - \frac{2Alo}{3\pi}.\sin(3\omega_{lo} + \omega_{rf}).t + \ldots..\right] \quad 5.7$$

Here, A_{rf} and A_{lo} are amplitudes of RF and LO signals respectively while ω_{rf} and ω_{lo} are angular frequencies of them in same order. Frequency constituents of the signal of Fig. 5.4(c) are plotted in Fig. 5.5 which agrees with (5.7). Now, both the sidebands of the up-converted signal will be available if a low pass filter blocks all frequencies higher than $(f_{lo} - f_{rf})$ and $(f_{lo} + f_{rf})$, while upper or lower sideband will be at the output if only either one of them are passed. Note that, a dc blocking capacitor will block the dc part of (5.7).

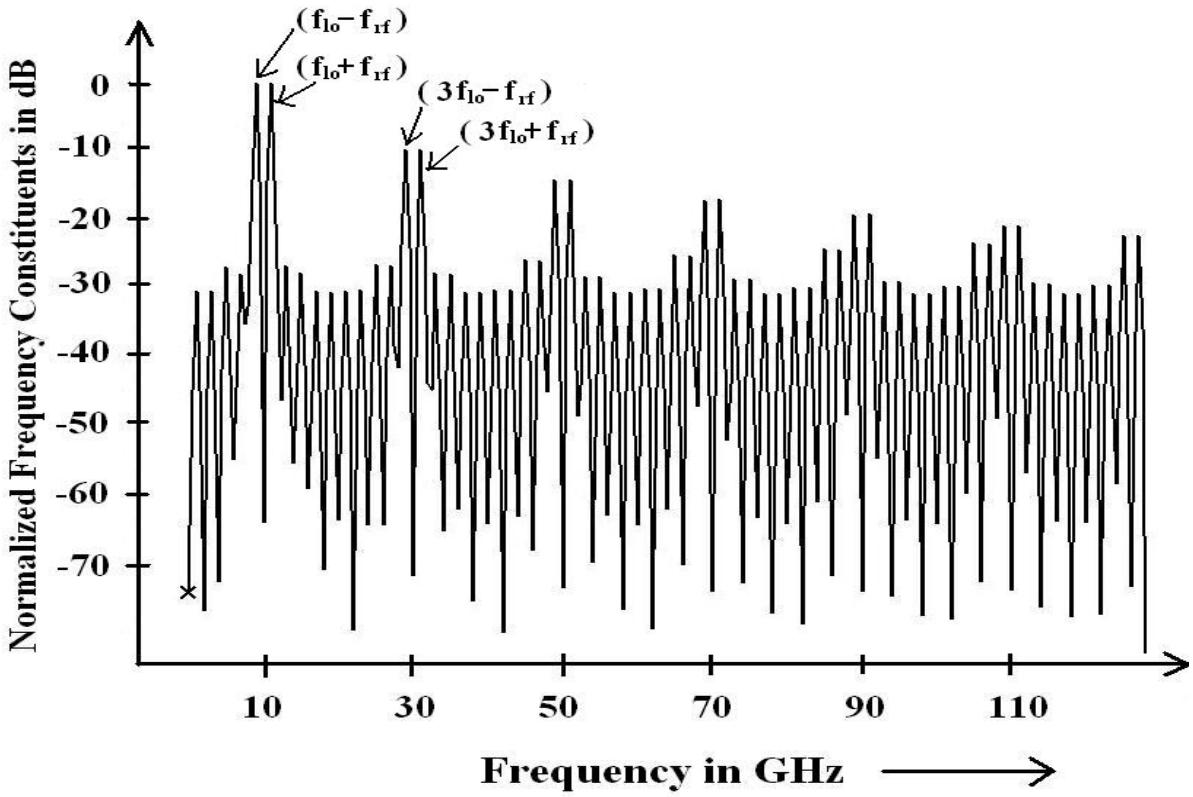

Figure 5.5: Frequency constituents of the output signal of Fig. 5.4(c)

The mixer works as a frequency down converter simply when f_{lo} is less than f_{rf}. So, in summary, a Gilbert's mixer works as frequency up or down converter when one of its inputs, usually local oscillator signal (LO), is a large signal and then the high frequency parts are to be eliminated by a low pass filter. Next section will explain how this same mixer can work as a small signal multiplier as well.

5.2.2 Gilbert's Mixer as a Small Signal Multiplier

To use Gilbert's mixers as small signal multipliers, both RF and LO inputs of the circuit of Fig. 5.3 are to be biased and then, both RF and LO are small signals. So, no switching functions anymore in M3-M6 stage. In that case,

$$I_3 = I_5 = \frac{Irf+}{2} = \frac{\beta}{4}.(V_{RF} + v_{rf} - V_t)^2 \qquad (5.8)$$

And $$I_4 = I_6 = \frac{Irf-}{2} = \frac{\beta}{4}.(V_{RF} - v_{rf} - V_t)^2 \qquad (5.9)$$

because, $I_{rf+} = \frac{\beta}{2}.(V_{RF} + v_{rf} - V_t)^2$, $I_{rf-} = \frac{\beta}{2}.(V_{RF} - v_{rf} - V_t)^2$. Here, $\beta = \mu_n C_{ox}\frac{W}{L}$, v_{rf} is the RF signal and V_{RF} is gate to source dc voltage of the transistors M1 and M2. Note that, according to the nature of differential circuit, the common-source voltage, Vs will change to adjust V_{RF} in such a way that, the sum of the dc currents through the transistors M1 and M2 is equal to the biasing current, I_B. However, since the trans-conductance of a transistor in saturation is given by, $g_m = \sqrt{2\beta Id}$, where Id is the current flowing through that transistor, so the trans-conductance of the transistors M3 and M5 are,

$$g_{m,3\text{-}5} = \sqrt{2\beta.\frac{\beta}{4}.(V_{RF} + v_{rf} - V_t)^2}$$

Or $$g_{m,3\text{-}5} = k.(V_{RF} + v_{rf} - V_t) \qquad 5.10$$

Where, $k = \frac{\beta}{\sqrt{2}}$. Similarly, trans-conductance of the transistors M4 and M6 are,

$$g_{m,4\text{-}6} = k.(V_{RF} - v_{rf} - V_t) \qquad 5.11$$

Now, $$i_{f+} = g_{m,3\text{-}5}.v_{lo} + g_{m,4\text{-}6}.(-v_{lo})$$
$$= k.(V_{RF} + v_{rf} - V_t).v_{lo} - k.(V_{RF} - v_{rf} - V_t).v_{lo}$$

Or $$i_{f+} = 2k.v_{rf}.v_{lo} \qquad 5.12$$

Where, v_{lo} is the small signal of LO input ports.

Similarly, $$i_{f-} = g_{m,4\text{-}6}.v_{lo} + g_{m,3\text{-}5}.(-v_{lo})$$
$$= k.(V_{RF} - v_{rf} - V_t).v_{lo} - k.(V_{RF} + v_{rf} - V_t).v_{lo}$$

Or, $$i_{f-} = -2k.v_{rf}.v_{lo} \qquad 5.13$$

Again, for this ac condition, modified version of equation (5.3) can be used to express the ac output signal as, $v_{out} = (i_{f-} - i_{f+}).R_D = -4k.v_{rf}.v_{lo}.R_D$

Or, $$v_{out} = G.v_{rf}.v_{lo} \qquad 5.14$$

Where, G is the conversion gain of the mixer and is equal to $-4kR_D$. So, equation (5.14) shows that, the mixer can work as a double balanced i.e. no carrier component at the output, small signal multiplier. This is the configuration which will be used in this

work to multiply a couple of signals of same frequency. Next section will describe the circuit in detail.

5.3 Design of the Receiver Front-End

A basic receiver front end is depicted in Fig. 5.6. As mentioned earlier in this chapter, judicious design of the receiver front ends is a good way to make these transceivers economical in terms of power and space. The receiver proposed in [22] consists of a 3 stage LNA and a 2 stage differential mixer. That circuit burns 64.5 mW of power in total and uses a number of slab inductors, which is inconvenient to integrate. On the other hand, [47-48] employed on-chip transformers, so their performance depends much on the coupling co-efficient of those transformers that vary considerably on silicon chip. Moreover, the area budget needs to be extended as well.

To minimize both space and power burden simultaneously, one has to come up with a design with minimum possible number of stages and with no on-chip transformer thing. In that sense, a better one is reported in [49]. But it uses a cascode structure, so is not suitable in applications where the supply voltage is as low as 1.2 V. Design of [50] is comprised of a 1 stage LNA and a 1 stage mixer to operate in 2.14 GHz frequency. But, in this circuit the mixer loads the LNA directly. So, at higher frequencies, it will have to employ an inter stage matching to counter the diminishing gain of the amplifier, when the input impedance of the mixer will precipitate due to its input parasitic capacitances. Recently, the concept of inter stage matching was incorporated in [51]. But again, it used an integrated transformer for that purpose, so is accompanied by the shortcomings mentioned earlier.

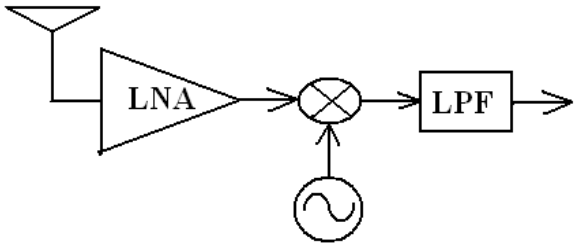

Figure 5.6: An example of a receiver front end

In this design, a simple passive inter stage matching was adopted to unify the LNA and the mixer that gives rise to a simple 2 stage receiver front end. This design is free from any off-chip circuit element i.e. fully integrated. The circuit was designed in IBM 90 nm CMOS technology, whereas most of the modern high frequency MM-wave mixers are designed in costly processes like SiGe, SOI etc. They also use transmission line based matching techniques those are area consuming. Since, lumped elements will be used in this design, so area requirement of this circuit will be lower. This section will describe how the LNA and the mixer was unified to end up to a receiver front end that is simple, less noisy, power starved, compact as well as cheap.

5.3.1 Design Issues

To design the receiver front end of Fig. 5.6, let us start from the mixer. In section 5.1, it was argued that, Gilbert's mixer will be most appropriate in this application. But, the problem is, this topology will not be able to maintain good isolation in high frequencies. Isolations were improved in [52] by using RF transformers. A better way to improve isolation is by placing isolating transistors in between the ports. Then the Gilbert's cell would look like that in Fig. 5.7, where Mi1-Mi4 are isolating transistors. Again, it would be difficult to keep all the transistors in saturation if there are more than three transistors in

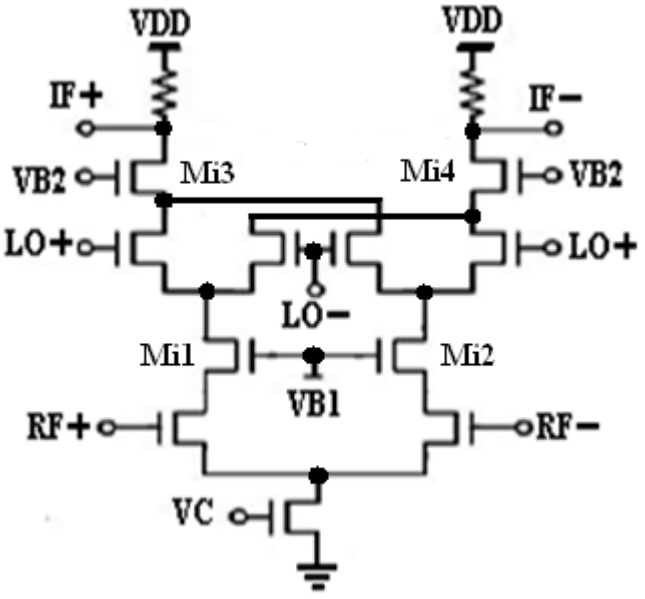

Figure 5.7: Gilbert's mixer for high frequency applications

series between the supply rails, especially when the supply voltage is low for submicron devices. For instance, [53] had to discard the isolating transistor between the LO-IF ports and the tail current source while [48] used on-chip inductors as isolators. That is why, isolation between the LO-IF ports and the CMRR of the former one will degrade whereas the later one will occupy large space.

One of the solutions of this problem would be to fold the circuit like that in Fig. 5.8. Note that, in this figure, the load resistors are replaced by inductors to set the centre frequency at 20 GHz like the LNA of previous chapter. Operation of the circuit is same as that described in section 5.2.2, since still now, the small signal currents generated by the RF transistors will be steered to the next stage. This is because; the output of the first stage is a high impedance node as both the parallel tuned path and the cascode branch offers high impedance at that node. This folded circuit has other advantages to offer like better headroom, improved linearity, higher gain etc. [54]. However, this configuration is criticized for its space and power demand, which would be compensated if its first stage could act as an LNA, because in that case a separate LNA would not be required in the receiver front end. In other words, the LNA and the mixer would be unified.

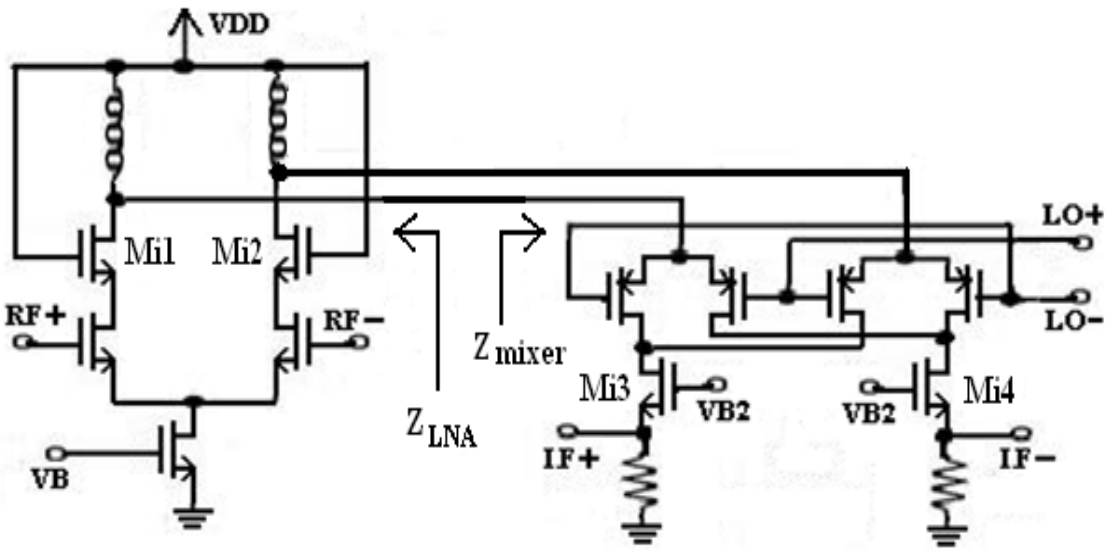

Figure 5.8: A folded Gilbert's mixer

The first stage of Fig. 5.8 is in fact an LNA [50], but its gain will fall down in high frequencies, because the input impedance of the second stage will be quite low in those frequencies. Input resistance and reactance of the second stage, Z_{mixer} is plotted in Fig. 5.9, which is (94-30j) Ω at 20 GHz. Note that, the real part is near to 100 Ω instead of 50 Ω since this is a differential system now. This resistance would be lower if the driving transistors were NMOS instead of PMOS. Output impedance of the LNA, Z_{LNA} can be found in Fig. 5.10 and it is (380+100j) Ω at 20 GHz. Gain (S21) and the output matching parameter (S22) of the first stage are given in Fig. 5.11, where the gain reduced by about 5 dB and the output matching nearly spoiled comparing to similar responses of the LNA of previous chapter shown in Fig. 4.27 and Fig. 4.29 respectively, where the output port was matched for a 50 Ω system. This is the effect of mismatch between Z_{mixer} and Z_{LNA}.

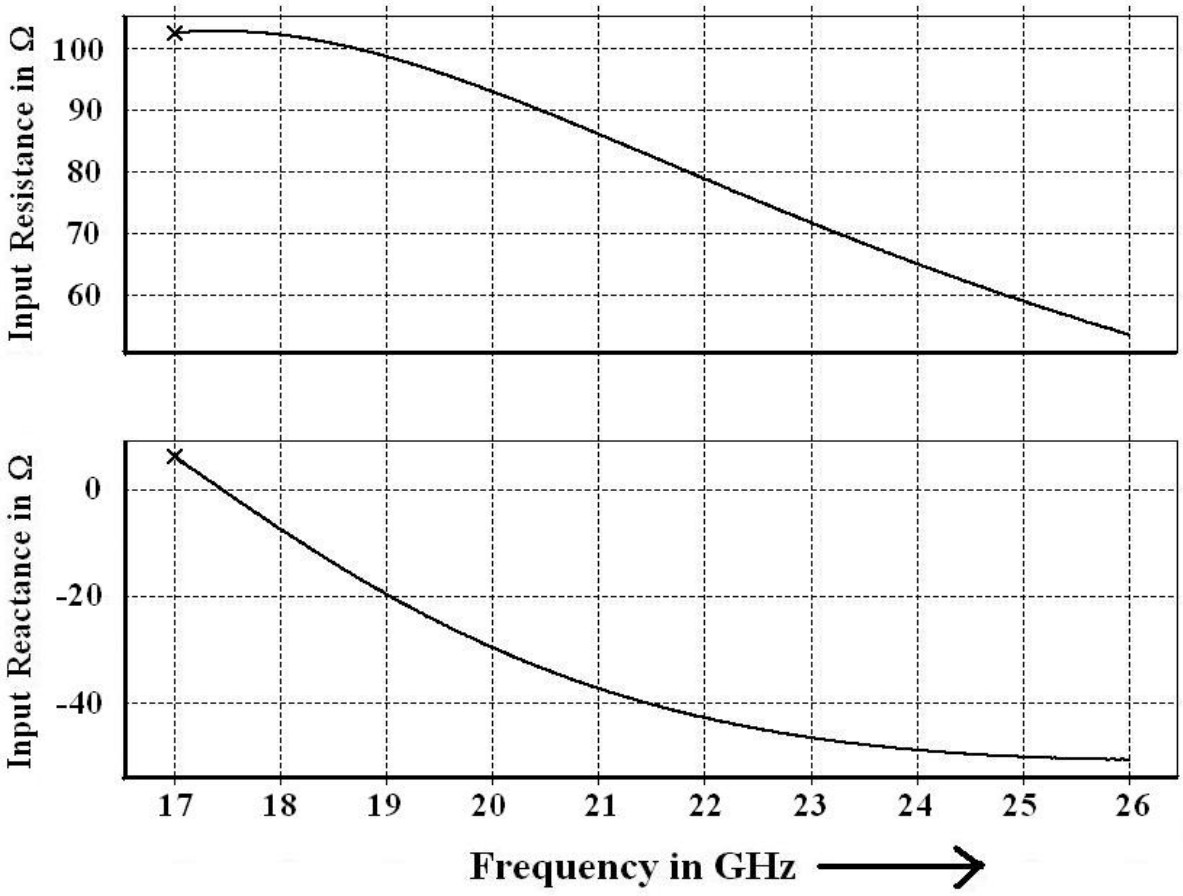

Figure 5.9: Input resistance and reactance versus frequency of the mixer stage (Z_{mixer})

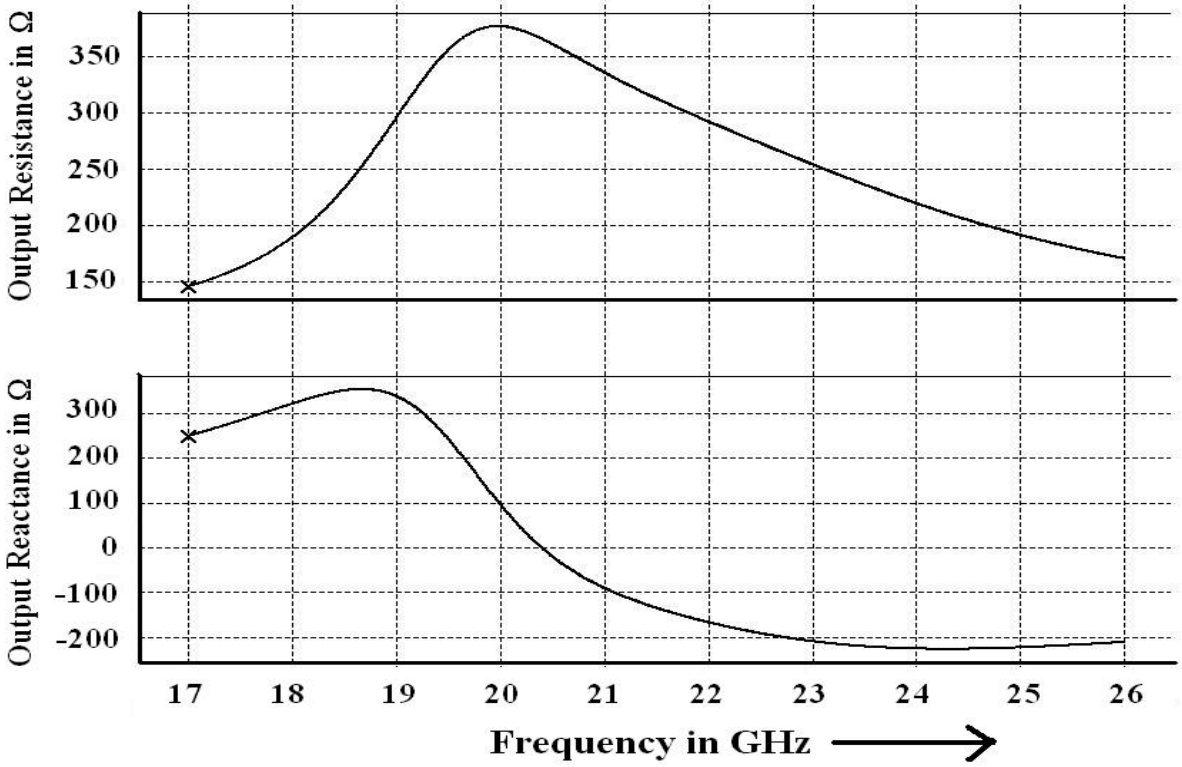

Figure 5.10: Output resistance and reactance versus frequency of the first stage (Z_{LNA})

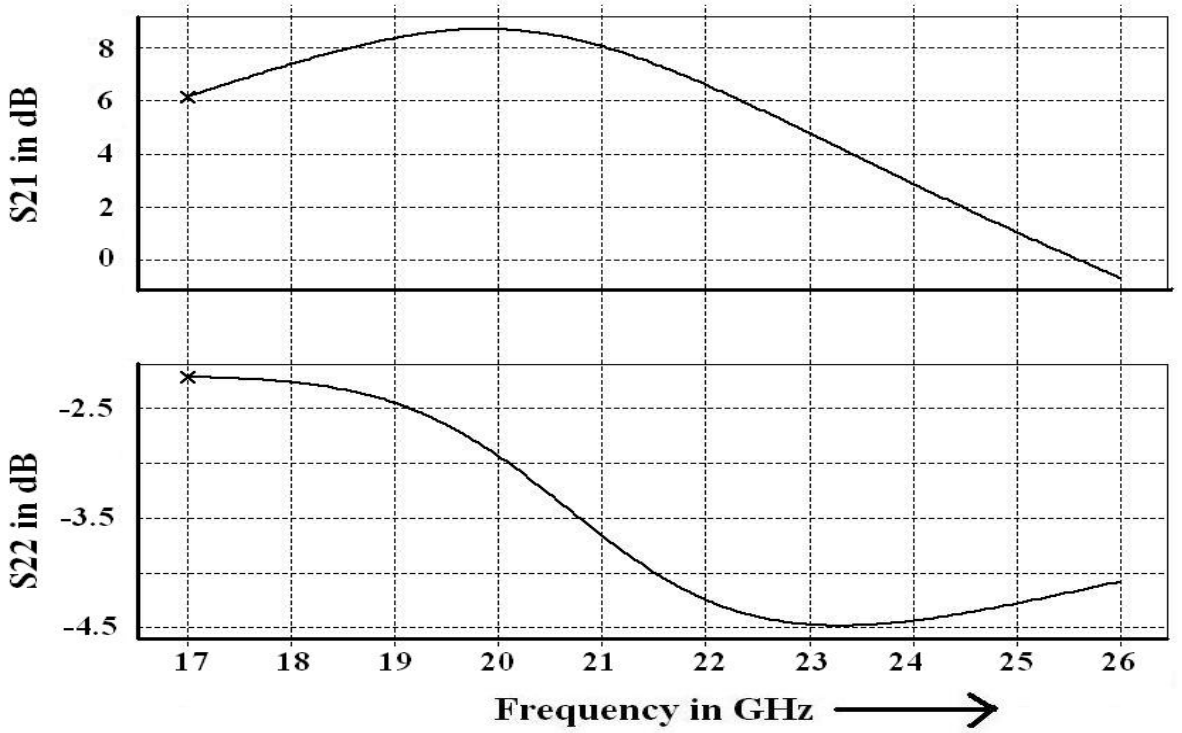

Figure 5.11: S21 and S22 versus frequency before inter-stage matching

Gain of the LNA is of prime importance for the receiver, because according to Frii's formula given in (2.2):

$$F_{receiver} = F_{lna} + \frac{(Frest-1)}{Glna}$$

Where, $F_{receiver}$, F_{lna} and F_{rest} are the noise factors of the whole receiver, LNA and of the rest of the receiver after LNA, whereas G_{lna} is the Gain of the LNA. So, overall noise factor of the receiver can be minimized by reducing the noise factor of the LNA and by increasing its gain. Now let us see, how the gain of the first stage was improved in this work by incorporating a simple passive inter-stage matching to unify the LNA and mixer of the receiver front end.

5.3.2 Unification of LNA and Mixer

Gain of the first stage can be improved by using an inter-stage matching between two stages. [47] and [51] used on-chip transformers for that purpose. In this work, a simpler passive matching technique was preferred to end up to the circuit of Fig. 5.12. Here, L_{int1}, L_{int2}, C_{int1} and C_{int2} forms the differential inter-stage matching network and works in the same way the input matching network did for the 20 GHz LNA described in previous chapter. Note that, any passive matching network would not work here because, most of the matching circuits need capacitors in series patch which would block the dc biasing currents of the second stage.

To examine the matching for this particular case, the inter-stage was modeled in Fig. 5.13, where R_{mixer} and X_{mixer} are the total gate resistance and the capacitive reactance of the half circuit of second stage and are 47 Ω & -15j Ω respectively at 20 GHz such that, differential version of this impedance is equal to 2 X (47-15j) Ω or (94-30j) Ω, so as to agree with Fig. 5.9. Similarly, R_{LNA} and X_{LNA} are 190 Ω and +50j Ω respectively, which are half of Z_{LNA}, where Z_{LNA} was the differential output impedance of the first stage and was (380+100j) Ω in Fig. 5.10. In Fig. 5.13, 'h' subscripts denote half circuit versions of the impedances.

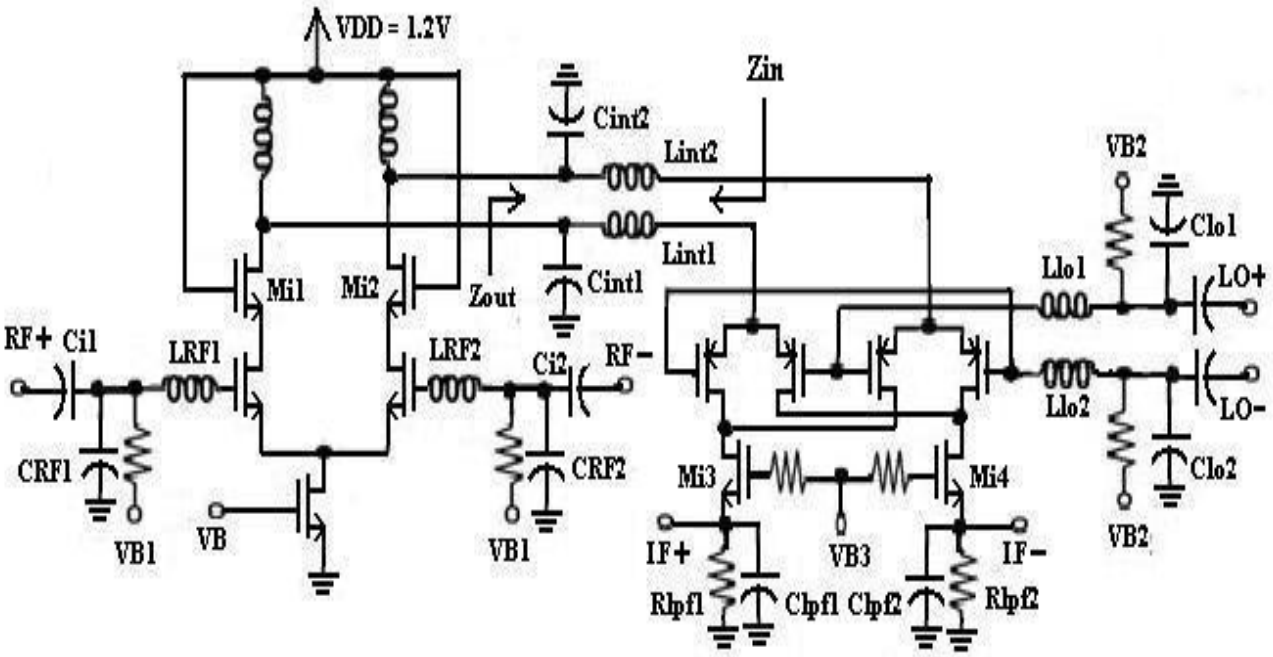

Figure 5.12: The complete circuit of unified LNA and mixer

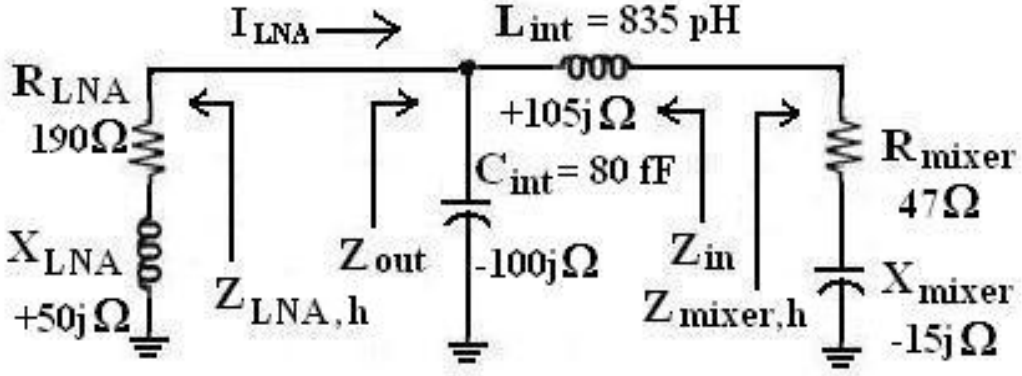

Figure 5.13: Model of inter-stage matching. Here, 'h' subscripts denote half circuit versions of the impedances. All impedances are calculated in 20 GHz frequency

Now, the Z_{out} of this parallel resonator will peak up at its resonant frequency, 20 GHz in this design, but the peak value can be controlled by choosing suitable L_{int} and C_{int} . Again, R_{mixer} in effect reduces the Q-factor of L_{int} . Thus, it reduces the resonant impedance of the parallel resonator. That means, peak value of Z_{out} can also be controlled by sizing the input transistors of the second stage to get a suitable value of R_{mixer}. The higher it is, easier it will be to match (note that, no matching would be required if R_{mixer} was equal to 190 Ω), although getting too high a value is difficult in this band of high frequency. On the

other hand, a drawback of choosing high input resistance is- increased noise figure. But, according to Frii's formula given in (2.2), this effect can be minimized if the gain of the first stage can be increased much.

In this design, based on simulation, size of the PMOS transistors of the second stage was chosen so that, its input resistance is near to 50 Ω. This was the highest resistance that could be obtained with reasonable transistor sizes. Differential version of the input impedance can be found in Fig. 5.9. L_{int} and C_{int} were selected next as 835 pH and 80 fF respectively using Smith's chart. All the impedances are shown in Fig. 5.13 which are calculated in 20 GHz frequency. Now, Z_{out} and Z_{in} can be easily calculated as (208-55j) Ω and (47+17j) Ω respectively. So, these two impedances match nearly with $Z_{LNA,h}$ = (190+50j) Ω and $Z_{mixer,h}$ = (47-15j) Ω in the same order. Differential versions of Z_{out} and Z_{in} of the original circuit of Fig. 5.12 are plotted with frequency in Fig. 5.14 and Fig. 5.15 respectively, where they are (380-150j) Ω and (110+4j) Ω at 20 GHz. Note that, half of these values does not match exactly with those theoretical calculations above. This is because of the parasitic issues associated with those on-chip inductors and capacitors. For the same reason, Z_{in} and Z_{out} of Fig. 5.14 and Fig. 5.15 do not match perfectly with corresponding impedances of Fig. 5.9 and Fig. 5.10 at 20 GHz, but still they are pretty close and so can be accepted. This argument can be justified by considering the improvement of gain (S21) and output matching parameter (S22) of the first stage shown in Fig. 5.16. Comparison of these curves with corresponding responses of Fig. 5.11 reveals that, gain increased by about 5 dB and the output matching improved a lot. Now, the gain and output matching of the first stage are comparable to those of the 20 GHz LNA designed in previous chapter and were shown in Fig. 4.27 and Fig. 4.29 respectively (Corresponding curves are not exactly the same due to the differences in load impedances. In previous chapter the LNA was matched for a 50 Ω system, whereas in this chapter both the resistance and the capacitive reactance of the mixer stage are loading the first stage, although both the circuits are same). So, this first stage can work now as a low noise amplifier conveniently. This is how the output of the first stage can be matched to employ it as a low noise amplifier. In short, the LNA and Mixer are unified.

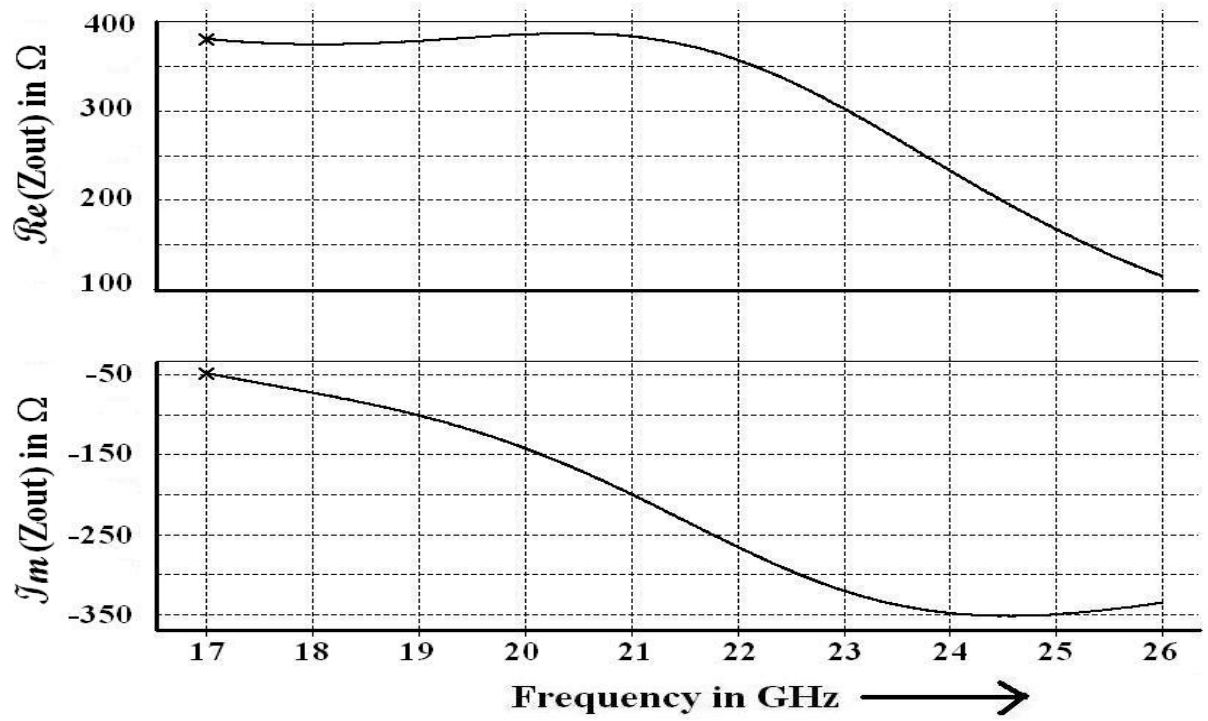

Figure 5.14: Resistance and reactance of Zout of the circuit of Fig. 5.12

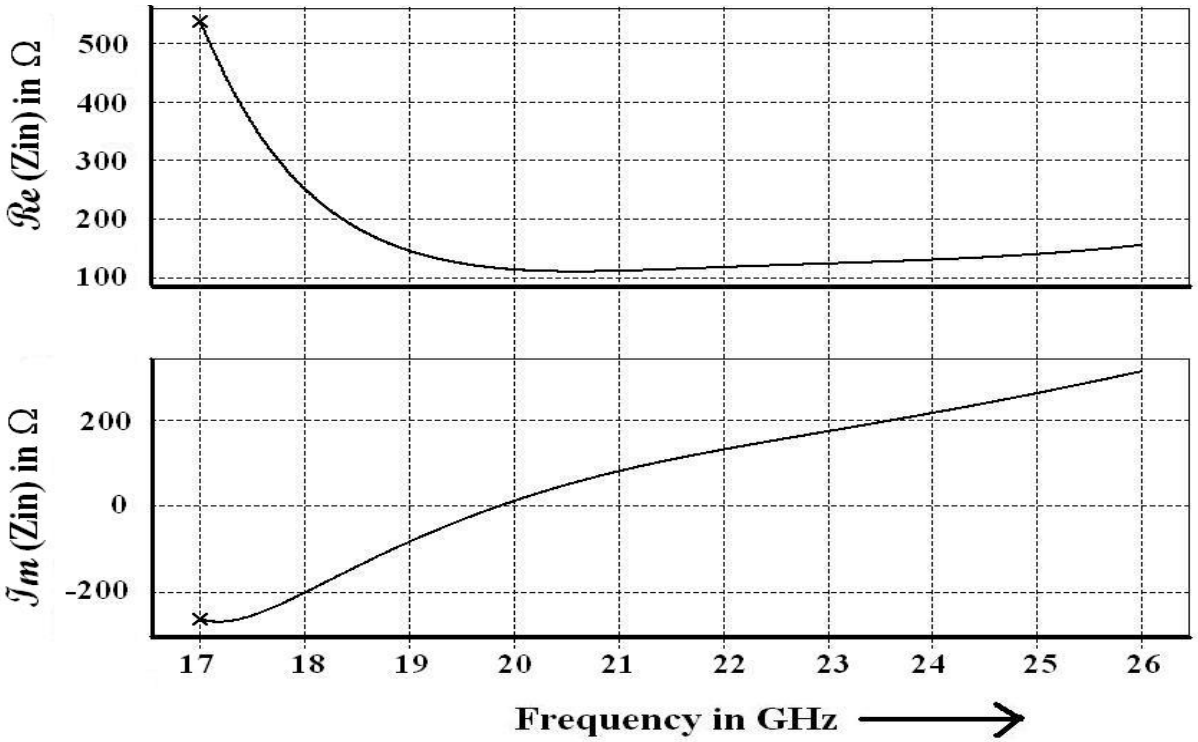

Figure 5.15: Resistance and reactance of Zin of the circuit of Fig. 5.12

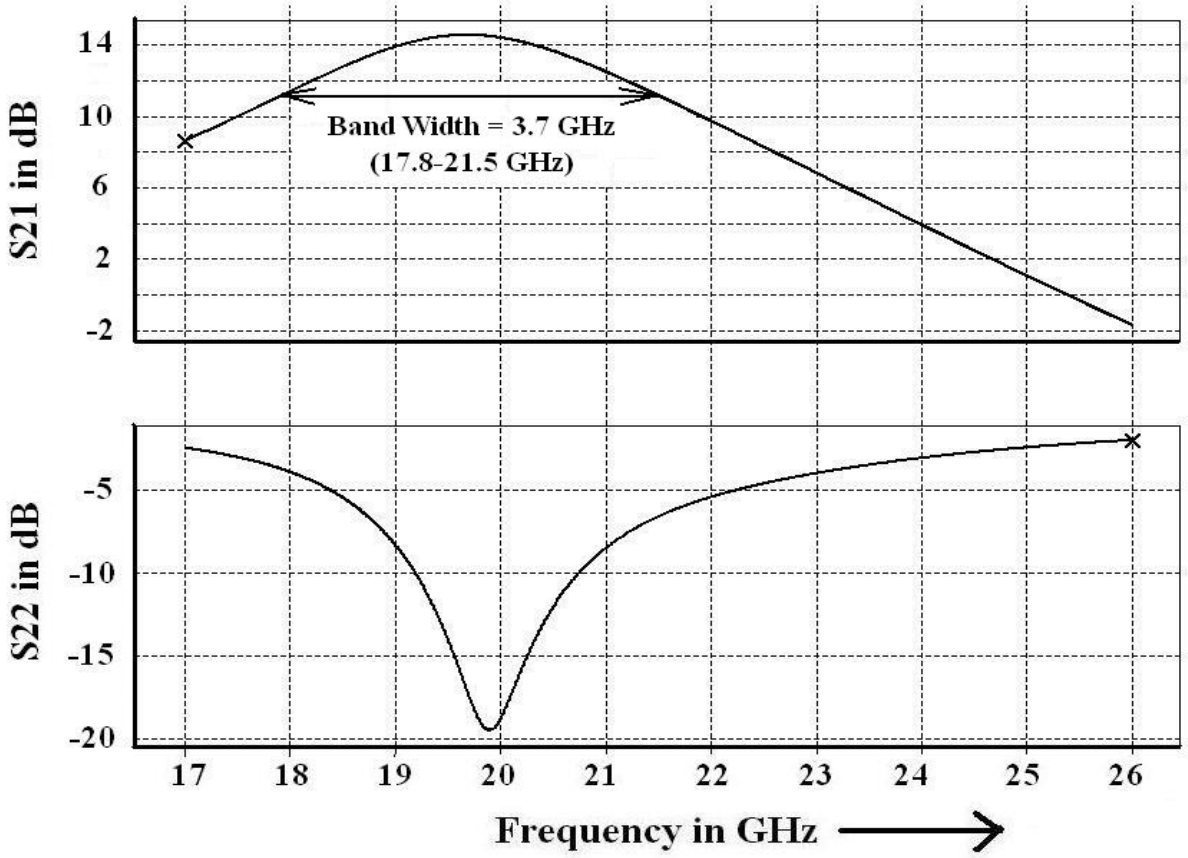

Figure 5.16: Gain (S21) and the output matching parameter (S22) of the first stage of Fig. 5.12 after the inter-stage matching employed

Another advantage of incorporating inter-stage matching is improved input port isolation (RF and LO inputs). Additional isolation is required in direct conversion (zero-IF) receiver because; here the frequencies of both the inputs are same i.e. both the inputs are matched for the same frequency. So, input signal through one port finds it easier to leak to another input port that would be difficult if those ports were matched for different frequencies. In fact, this was the reason why the square law mixer of chapter 3 could not be used in this receiver. Anyways, zero-IF mixers can be found in [58-59], they used additional active buffer stage to improve isolation. They also used split-phase architecture where space and power requirements are almost twice. In that sense, the simple passive inter-stage matching used in this work is much economical.

In the unified receiver front end, portrayed in Fig. 5.12, L_{RF1}, L_{RF2}, C_{RF1}, C_{RF2} and L_{lo1}, L_{lo2}, C_{lo1}, C_{lo2} match the RF and LO input ports respectively by the same way the input matching did in previous chapter. Also, dc blocking capacitors are present in both the input ports. M_{i1}-M_{i4} are the isolating transistors, whereas R_{lpf1}, R_{lpf2}, C_{lpf1} and C_{lpf2} forms the low pass filter (LPF) that should pass only zero frequency i.e. dc signal. All the resistances of that circuit are biasing resistors and are of high value, so do not interfere in matching issues. This is how the circuit is composed. However, incorporation of the inter-stage matching was not without any cost. Next section will explain what had to sacrifice in exchange.

5.3.3 Limitation of this Unification Technique

The limitation of this unification technique is- slower response. This is because in Fig. 5.13, a fraction of I_{LNA} is charging the C_{mixer} that decreases when Z_{out} is increased by using the inter stage matching. So, the charge up process takes more time. This effect is depicted in Fig. 5.17, where two sinusoidal signals of same frequency were multiplied by the circuit of Fig. 5.12 and then the high frequency components were removed by the low pass filter to observe only the dc transient response. Here, $v_{rf} = v_{lo} = A.\sin(2\pi ft)$, so from (5.14), $v_{if} = G.(A^2/2).\ [1- \cos(2\pi 2ft)]$, where v_{rf}, v_{lo} and v_{if} are the small signals at RF, LO and IF ports respectively, ‘A’ is the magnitude of the input signal and ‘f’ is 20 GHz frequency. Then, the LPF removed the 2f or 40 GHz frequency and only $(A^2/2)$ was suppose to remain in the IF output port. Anyways, the 40 GHz part was not removed completely from the output, as can be seen in Fig. 5.17 and that is why the steady state region has a dc part super-imposed by a 40 GHz sinusoid. But, its presence will not be harmful for the receiver performance because that small magnitude signal is far above the zero-level, so will be ignored by the following zero-threshold comparator.

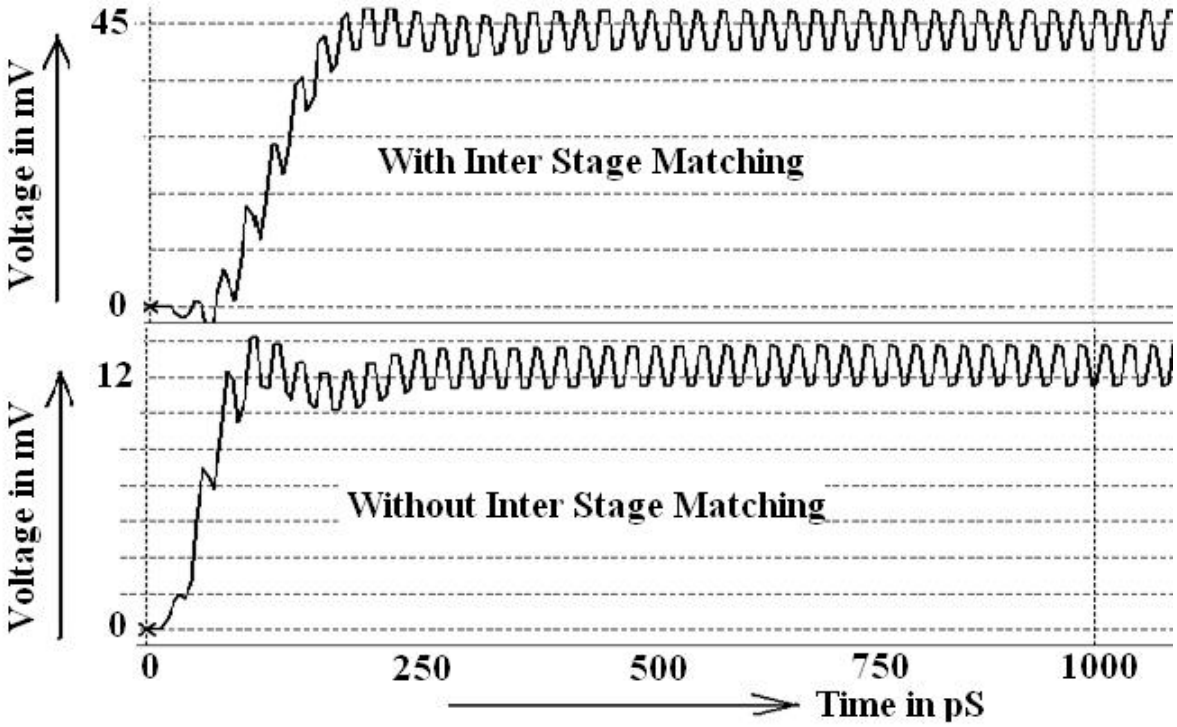

Figure 5.17: Transient response of the receiver front-end when detecting a dc signal (with and without inter-stage matching)

Although, higher gain is evident in Fig. 5.17, but the rise time increased from 200 ps to 250 ps after using the inter stage matching. So, data speed is to fall back from 5 gbps to 4 gbps. Therefore, 1 gbps speed was traded off in this design for saving space & power and for simplicity.

5.3.4 Frequency Responses and Linearity of the Receiver Front-End

The Circuit was designed in IBM 90 nm CMOS technology with no off-chip element and was simulated in Cadence Spectre. 15.2 dB conversion gain was attained at 20 GHz with a bandwidth of 2.7 GHz (18.7 GHz to 21.4 GHz), as can be seen in Fig. 5.18. Comparing to the bandwidth of the first stage shown in Fig. 5.16, overall bandwidth of the receiver front-end decreased by 1 GHz because, a couple of gain stages i.e. LNA and mixer, are cascaded here. Note that, conversion gain of a mixer is defined as the ratio of the output signal, v_{if} to the small signal input, v_{rf}. This definition is applicable for

frequency conversion mixers without any confusion, where the large signal LO port is biased by a reasonable dc voltage with no ac signal super-imposed (since, LO stage is a switching stage in that case) i.e. there is only one input signal. But, confusion arises when the mixer works as small signal multiplier, since there are a couple of small signal inputs, unlike frequency conversion mixer. In this simulation both the RF and LO ports were fed with small signals of same amplitudes (A) and frequencies (f) after proper biasing. So, if conversion gain of the mixer was unity, then v_{if} was supposed to be $A^2/2$ after the removal of the high frequency parts by the LPF as noted in previous section. Based on this argument, the conversion gain in Fig. 5.18 was calculated as $20 \log_{10}(2v_{if}/A^2)$, where v_{if} is the dc part of the differential output signal.

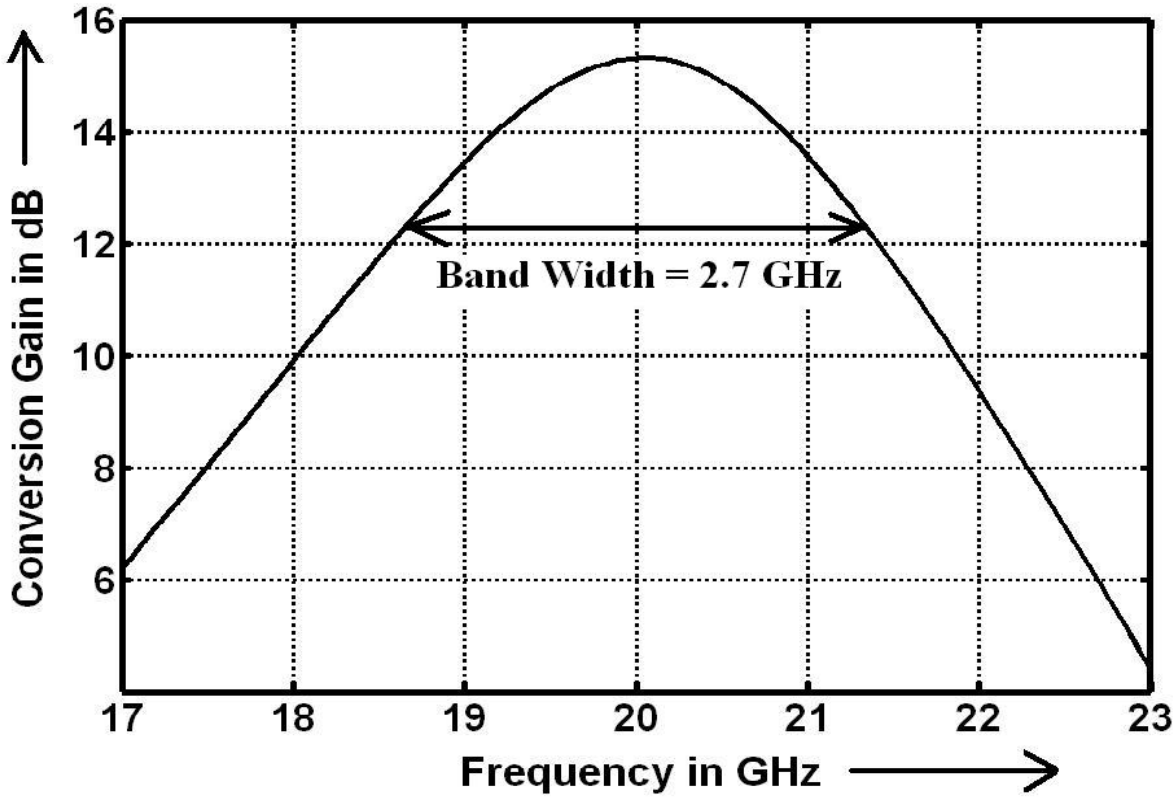

Figure 5.18: Conversion gain of the receiver front-end versus frequency

Noise figure of the circuit is 7.6 dB. Fig. 5.19 shows the noise figure versus frequency response. Noise analysis of mixers can be found in [60]. Although, the noise performance of this circuit is quite satisfactory comparing to the state of the art [47-55], but it could be improved further by using sophisticated current reuse bleeding or switched biasing techniques proposed in [61-66] at the expense of simplicity and area. Those schemes were not tried in this digital environment where the noise immunity is well reputed.

Fig. 5.20 plots the RF and LO port matching parameters (S11). They are -26 dB and -24 dB respectively and were matched for 100 Ω differential system. Input port isolation and feed through versus frequency are presented in Fig. 5.21 and Fig. 5.22 respectively. RF to LO isolation is much higher (less than -10 dB) than the LO to RF isolation (less than -42 dB) because the RF signal goes through a gain stage unlike the LO signal, which also experiences the reverse isolation of the first stage. Similarly, RF to IF feed through is better (less than -80 dB) than LO to IF feed through (less than -50 dB), since LO input is closer to the IF output than the RF port is.

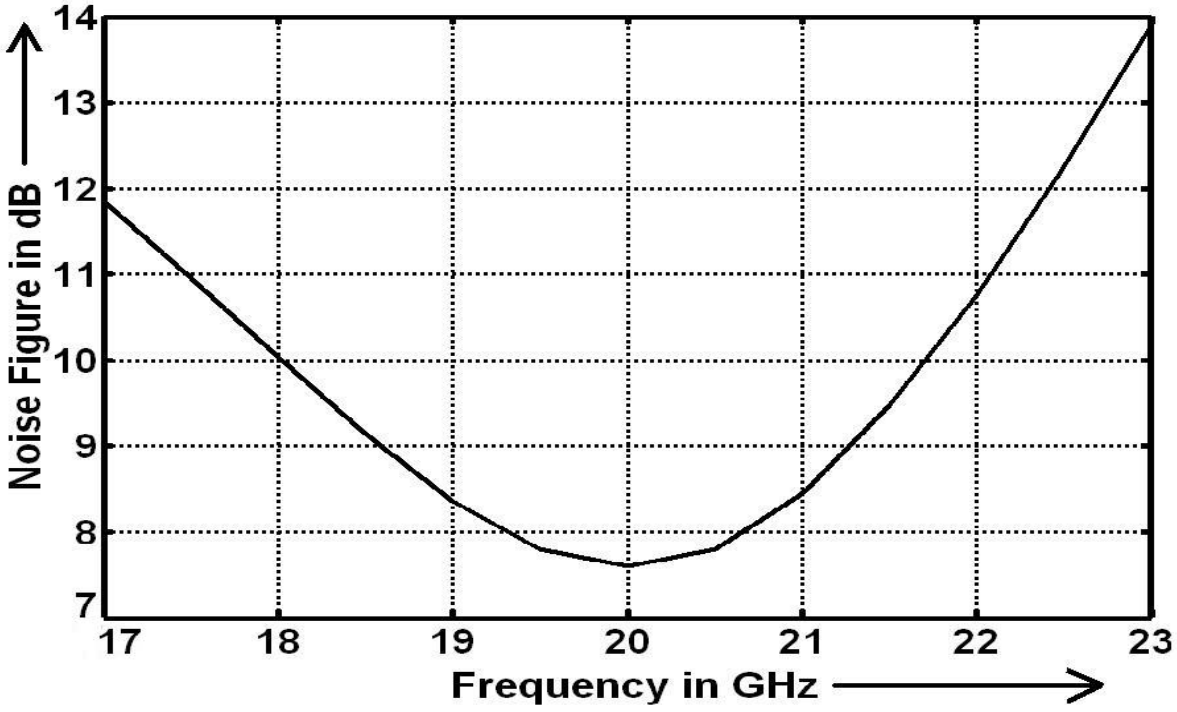

Figure 5.19: Noise Figure (NF) versus frequency

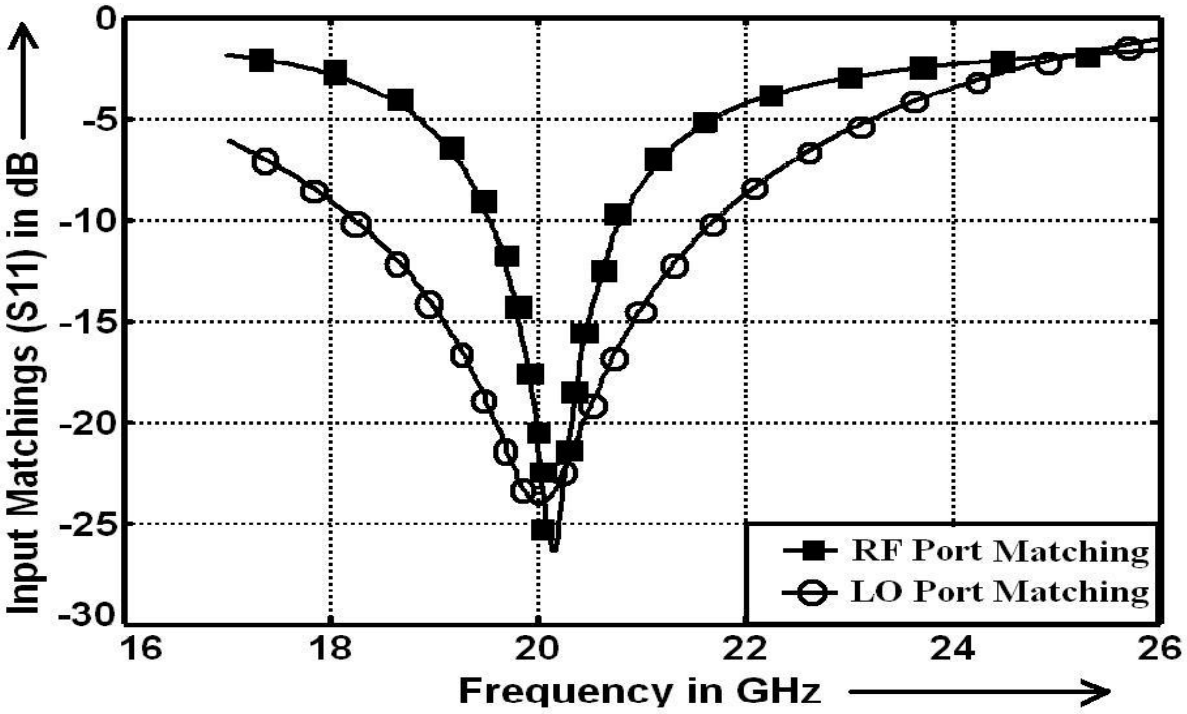

Figure 5.20: Input port matching parameters (S11) versus frequency

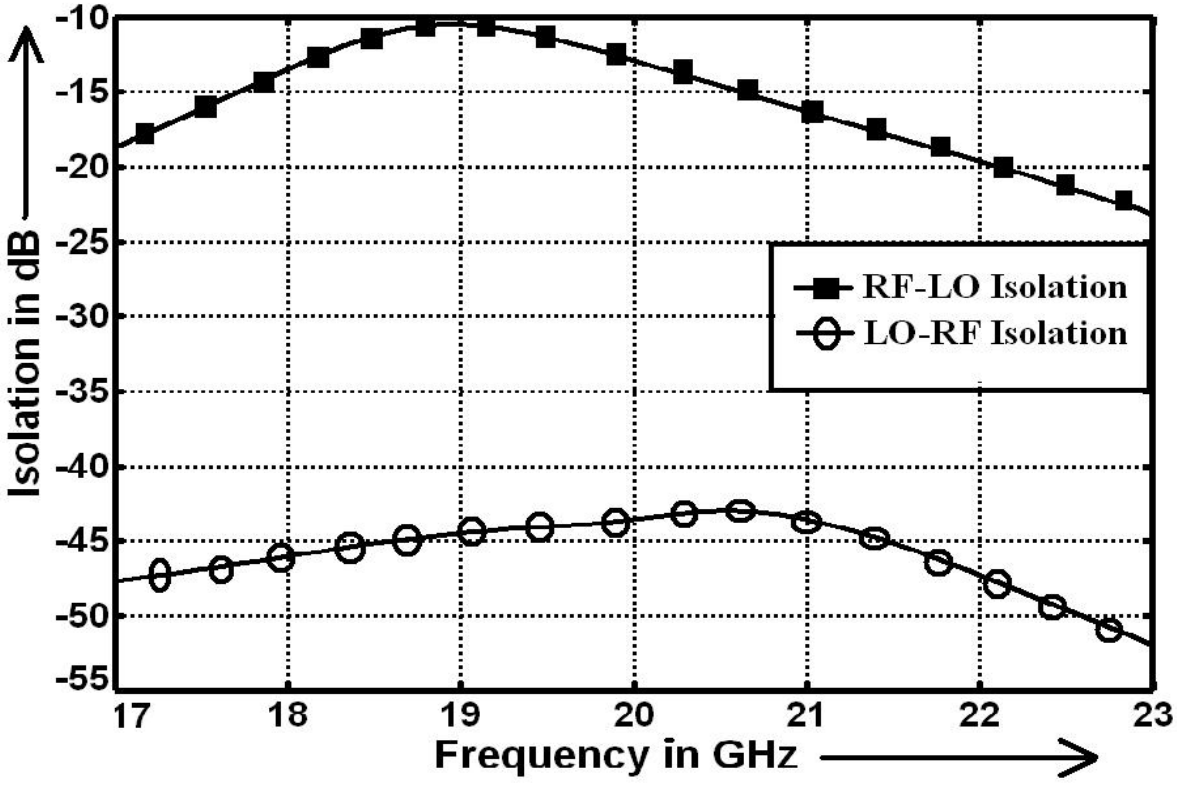

Figure 5.21: Input port isolations versus frequency

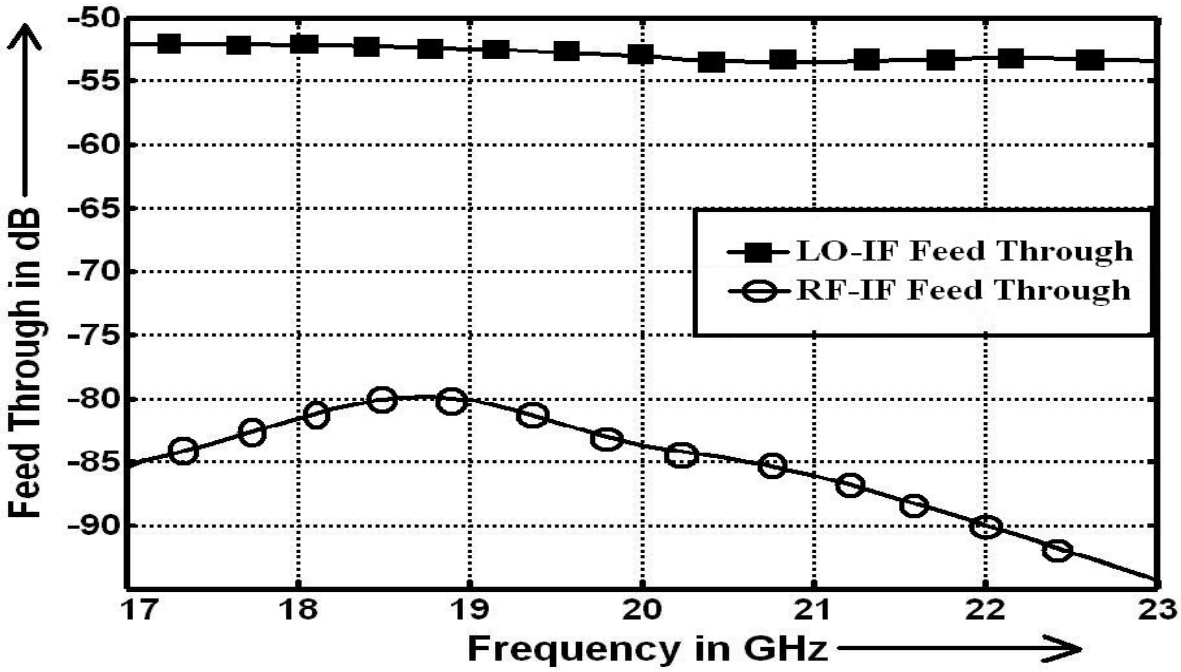

Figure 5.22: Input to output feed-through versus frequency

Input referred 1 dB compression point of the circuit is -18 dBm. This linearity response can be found in Fig. 5.23, where again, calculation of the gain needs some explanation. In case of up-conversion mixers, the output and input powers are given by $(G.A^2)/(2R)$ and $A^2/(2R)$ respectively, where G is the power gain and R is 100 Ω for a differential 50 Ω system. These terms can be expressed in dBm in the following way:

$$\text{Output Power (dBm)} = 10.\log_{10}(G) + 20.\log_{10}(A) - 10.\log_{10}(2R) + 10.\log_{10}(10^3) \quad 5.15$$

And

$$\text{Input Power (dBm)} = 20.\log_{10}(A) - 10.\log_{10}(2R) + 10.\log_{10}(10^3) \quad 5.16$$

Where, $10.\log_{10}(10^3)$ appeared to convert the powers in mW.

Now, the gain can be found simply by subtracting (5.16) from (5.15), as the gain is equal to $10.\log_{10}(G)$ when expressed in dB. This curve is a straight line parallel to X-axis in low signal power region where the gain is constant and will start bending downward after the circuit enters its saturation region. Gain of the LNA shown in Fig. 4.33 was calculated in this way.

But the scenario is different in case of zero-IF small signal multiplier, because then the output is a dc signal of amplitude proportional to $A^2/2$, although the input will be same as before. So, the output power would be $G.(A^2/2)^2/R = (G.A^4)/(4R)$, where again G is the power gain. Now, the expression of the output power in dBm would be:

$$\text{Output Power (dBm)} = 10.\log_{10}(G) + 40.\log_{10}(A) - 10.\log_{10}(4R) + 10.\log_{10}(10^3) \qquad 5.17$$

The expression of input power will remain same as 5.16. So, the gain can be calculated using (5.16) and (5.17) by,

$$\text{Power Gain} = \text{Output Power (dBm)} - 2 \text{ X Input Power (dBm)} + 10 \qquad 5.18$$

Where, R was considered as 100 Ω. This power gain was plotted in Fig. 5.23 versus input power and the gain was found as 15 dB in the linear region, which agrees with Fig. 5.18, thus, the analysis is justified.

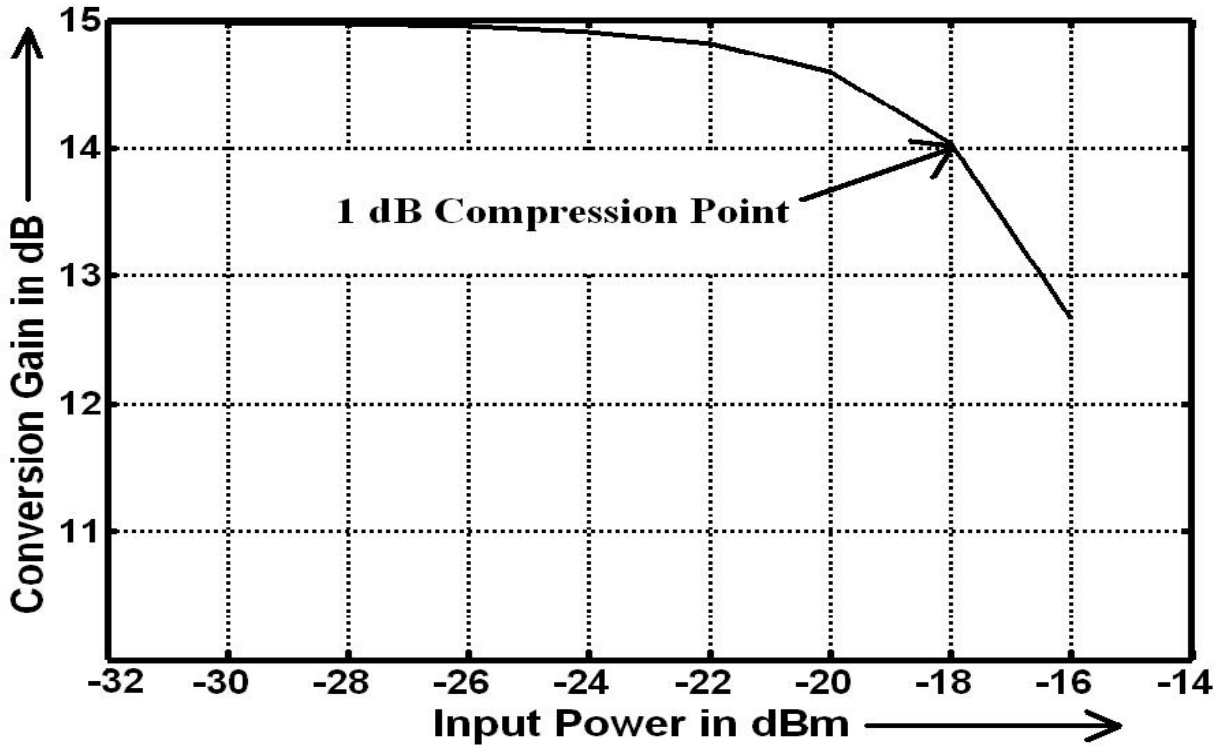

Figure 5.23: Conversion gain versus input power

Although, linearity improvement techniques are available in literature [67-68], but again they incur additional complicacy and space burden, whereas -18 dBm i.e. input signal limit is maximum 56.3 mV (peak), compression point will work fine in this receiver for it will work only with small signals.

Therefore, responses of the circuit in frequency domain and its linearity issues speak well of it. Now, to verify the performance of this circuit in time domain, it will be employed to detect a BPSK signal at first synchronously and then differentially. Next section will demonstrate those time domain responses of the receiver front-end.

5.4 Detection of Traditional Digital Signals by this Receiver Front-End

Before employing this receiver front-end in UWB system, let us verify the time domain response of the circuit by detecting traditional digital signals. Here, a BPSK (Binary Phase Shift Keying) signal will be detected- at first synchronously then differentially. Basic block diagram of the system is shown in Fig. 5.24 and the corresponding signals are shown in Fig. 5.25, where a 2 gbps bipolar NRZ digital bit stream is to be transmitted and detected. The local oscillator and the multiplier of the transmitter are modeled as ideal since these are not going to be part of the UWB system. On the other hand, a real on-chip dipole antenna pair was used for the transmission and reception of the signal with a silicon channel in between. The received signal (Rx) experienced about 23 dB attenuation on its way through the channel, although the distortion is insignificant. Note that, the carrier frequency shown in Fig. 5.25 is reduced to 2 GHz for clarity, whereas the actual frequency is 20 GHz. Next couple of sections will describe how the transmitted data can be recovered from this received signal using the receiver front-end designed in this chapter.

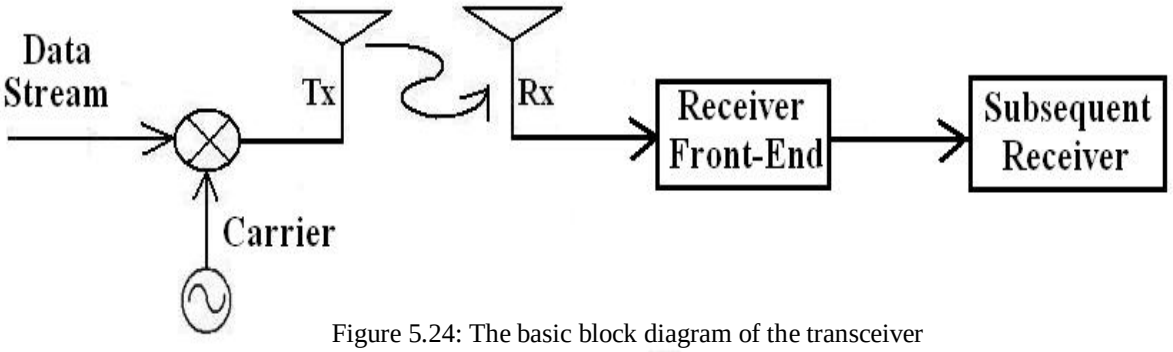

Figure 5.24: The basic block diagram of the transceiver

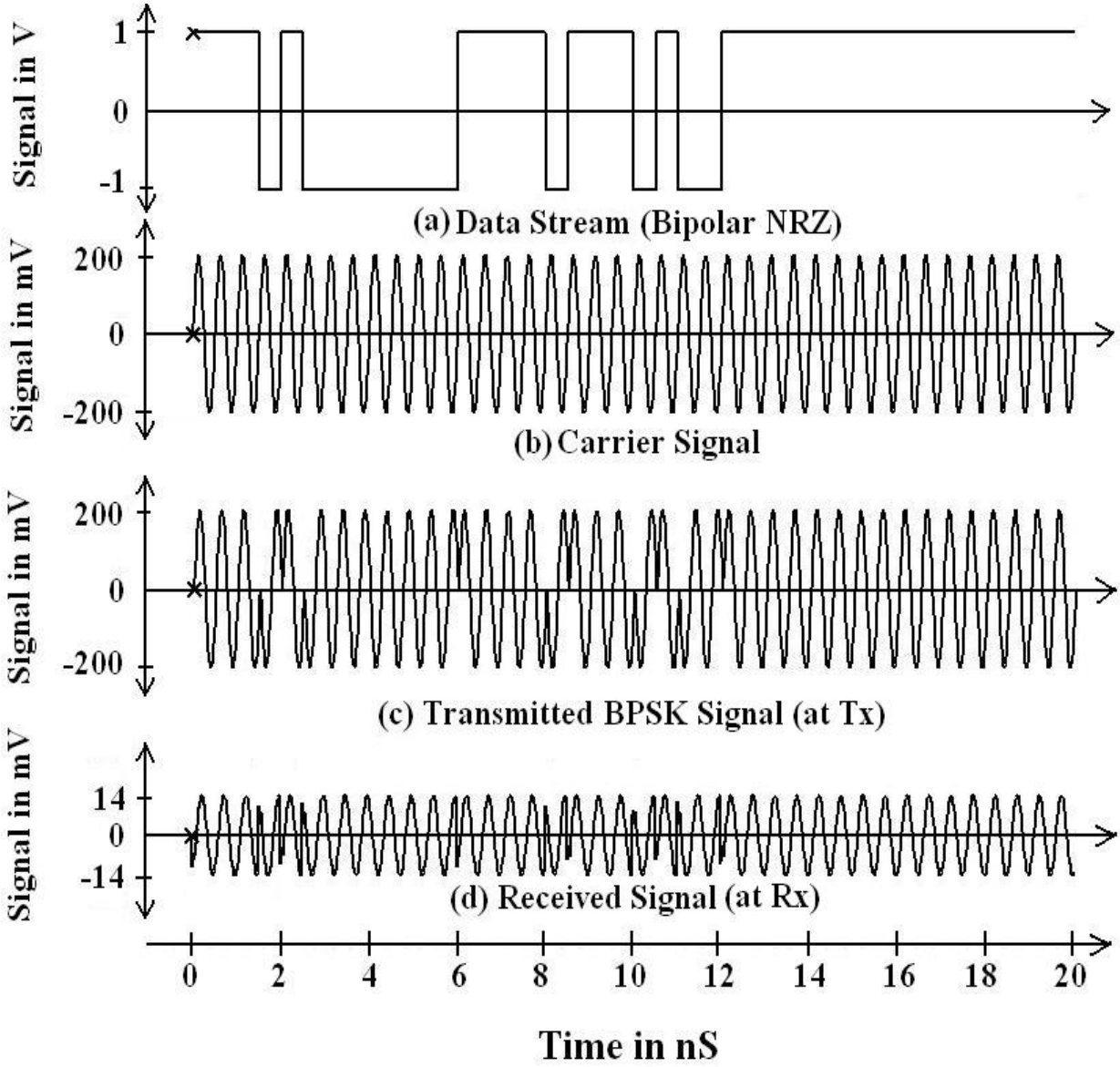

Figure 5.25: Signals at different nodes of the system of Fig. 5.24

5.4.1 Synchronous Detection of the Signal

Receiver diagram for the synchronous detection of the signal is given in Fig. 5.26, where the receiver front-end consists of the LNA, Multiplier and the LPF. Here, the local oscillator (LO) generates the same 20 GHz carrier as the transmitter of Fig. 5.24 did (shown in Fig. 5.25(b) with reduced frequency) and will also be modeled as ideal since it will not be part of the UWB receiver. The detection process is pretty straight forward. Since, the carrier signal and the received signal are in-phase and 180^0 out of phase when there are '1' and '0' respectively, so the multiplier of the receiver will multiply $A_{LO.}\sin(2\pi ft)$ with $A_{RX.}\sin(2\pi ft)$ and $A_{RX.}\sin(2\pi ft+180^0)$ for '1' and '0' respectively. Here, f is the 20 GHz carrier frequency, while A_{LO} and A_{RX} are the amplitudes of the LO signal and received signal. So, after removal of the high frequency parts of the multiplier output by the LPF, input to the comparator will be $CG.(A_{LO.}\ A_{RX})/2$ for '1' and $-CG.(A_{LO.}\ A_{RX})/2$ for '0', where CG is the conversion gain. Transmitted bit stream and the detected signal at the output of the LPF (v_{if}) can be found in Fig. 5.27. Again, although the high frequency (40 GHz) part was not removed completely by the LPF, but its low magnitude will not affect the performance of the following comparator i.e. will be ignored.

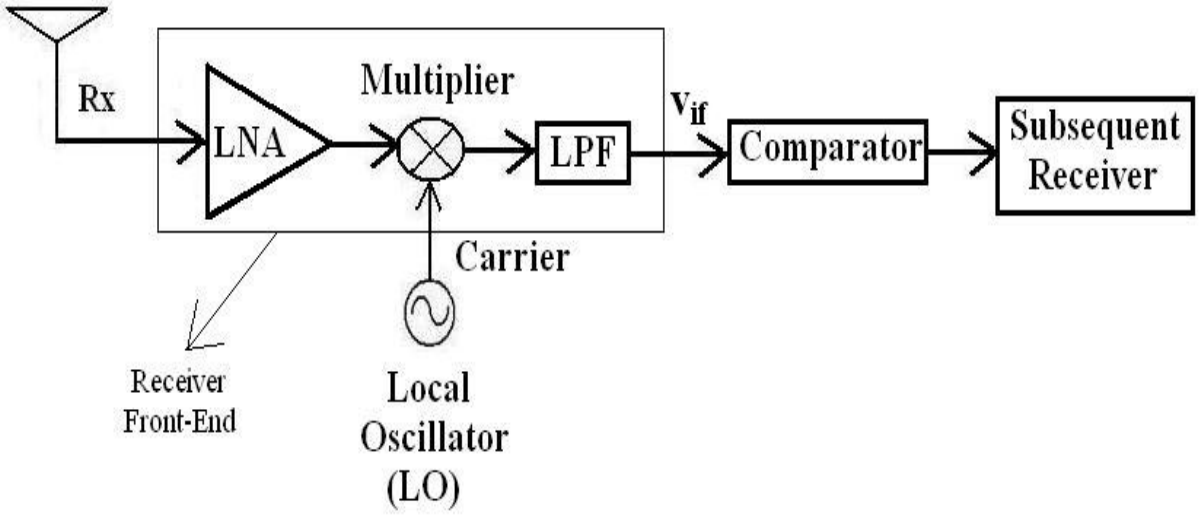

Figure 5.26: Receiver diagram for synchronous detection of the signal

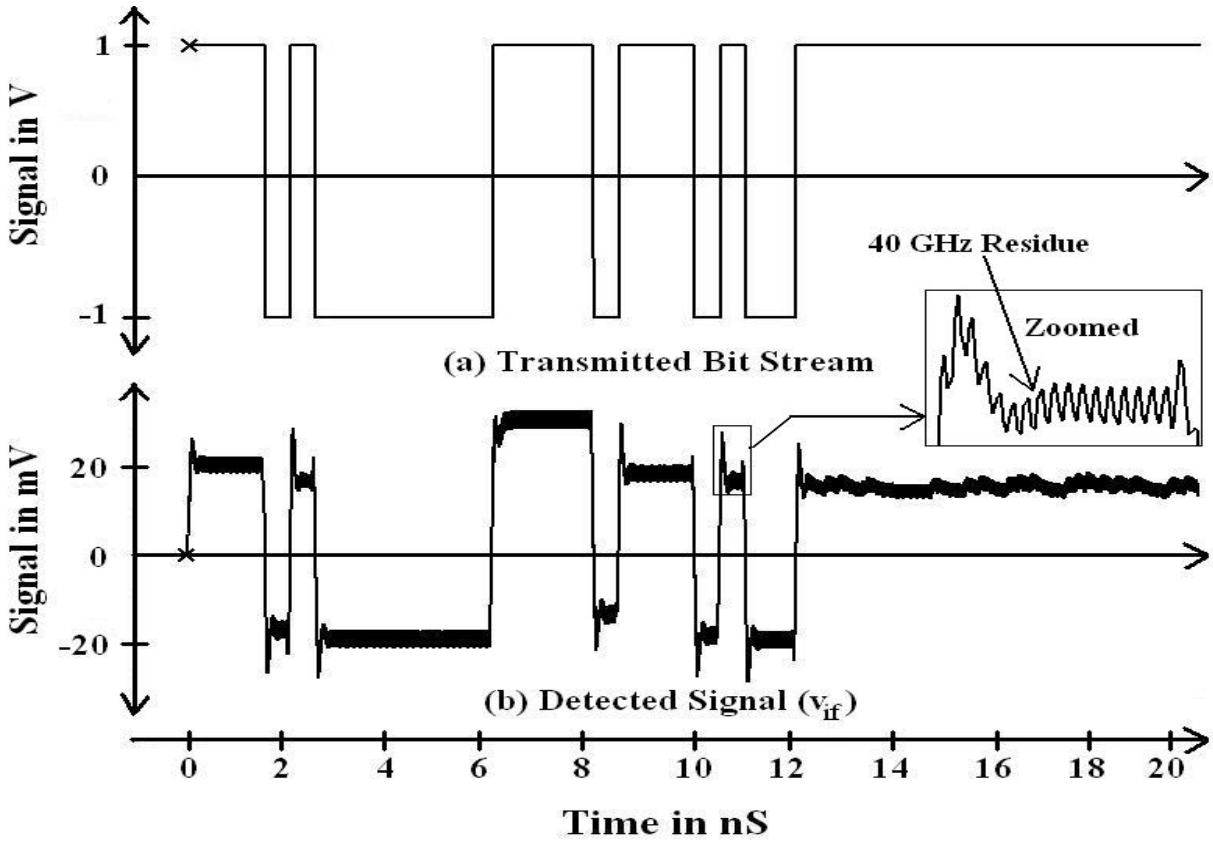

Figure 5.27: Transmitted and detected digital bit streams

Although, the synchronous detection process is easy in ideal condition, but practically it is quite difficult for the local oscillators of the transmitter and the receiver has to be synchronized. If there is any phase difference (Φ) between those couple of carrier signals, then the multiplier output will be ± $[\cos(\Phi).CG.A_{LO.}\ A_{RX}]/2$, where Φ was considered as zero in this analysis i.e. output was maximum that would be possible. That is why, carrier synchronization is very important for these kind of synchronous receivers. There are sophisticated circuits like Phase Locked Loop (PLL) which are commonly used for the purpose of synchronization, but those circuits are power hungry, bulky and complicated.

The alternative approach is to use asynchronous detection methods like differential detection, which will be preferred in this work. Next section will explain how the receiver front-end can be employed in an asynchronous receiver to detect the transmitted BPSK data differentially.

5.4.2 Asynchronous Detection of the Signal

Asynchronous detection scheme does not need any oscillator at the receiver, thus no synchronization issue. Rather, it detects the signal differentially i.e. '1' in the output of the receiver front-end (v_{if}) means a difference in previous output. That means, whenever there is a '1' in v_{if}, the latest bit will be '1' or '0' if the previous bit was '0' or '1' respectively. A diagram of this receiver is shown in Fig. 5.28, where an ideal delay element replaced the oscillator of the synchronous receiver of Fig. 5.26. It delays the output of the LNA by one bit duration (0.5 ns in this case). So, at any moment the multiplier multiplies the signals corresponding to present bit with previous bit to identify the difference in input bit stream.

Mathematically, if both the present bit and the previous bit are '1' or '0', then $G_{LNA}.A_{RX}.\sin(2\pi ft)$ and $G_{LNA}.A_{RX}.\sin(2\pi ft)$ or $G_{LNA}.A_{RX}.\sin(2\pi ft+180^0)$ and $G_{LNA}.A_{RX}.\sin(2\pi ft+180^0)$ will be multiplied, where G_{LNA} is the gain of the LNA. In both cases, the v_{if} will be $CG.(A_{LO.}\ A_{RX})/2$. On the other hand, $G_{LNA}.A_{RX}.\sin(2\pi ft)$ and $G_{LNA}.A_{RX}.\sin(2\pi ft+180^0)$ will be multiplied if there is any transition, in which case the v_{if} will be $- CG.(A_{LO.}\ A_{RX})/2$. Note that, since the comparator will generate a '1' in the former case and a '0' in the later one, so it might contradict the concept of differential detection process introduced in earlier this section. This problem can be avoided simply taking inverted output from the receiver front-end i.e. v_{if} = (IF-) – (IF+). Signals at different nodes of the receiver are given in Fig. 5.29.

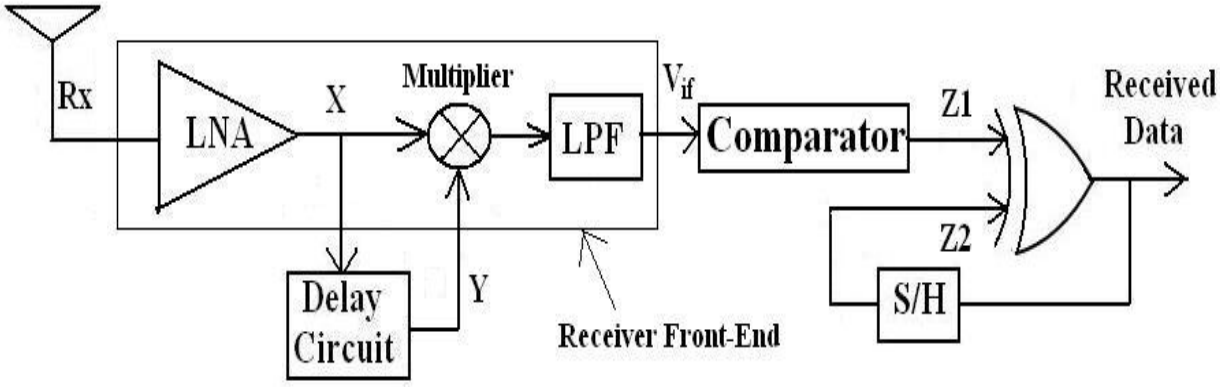

Figure 5.28: Receiver diagram for asynchronous detection of the signal

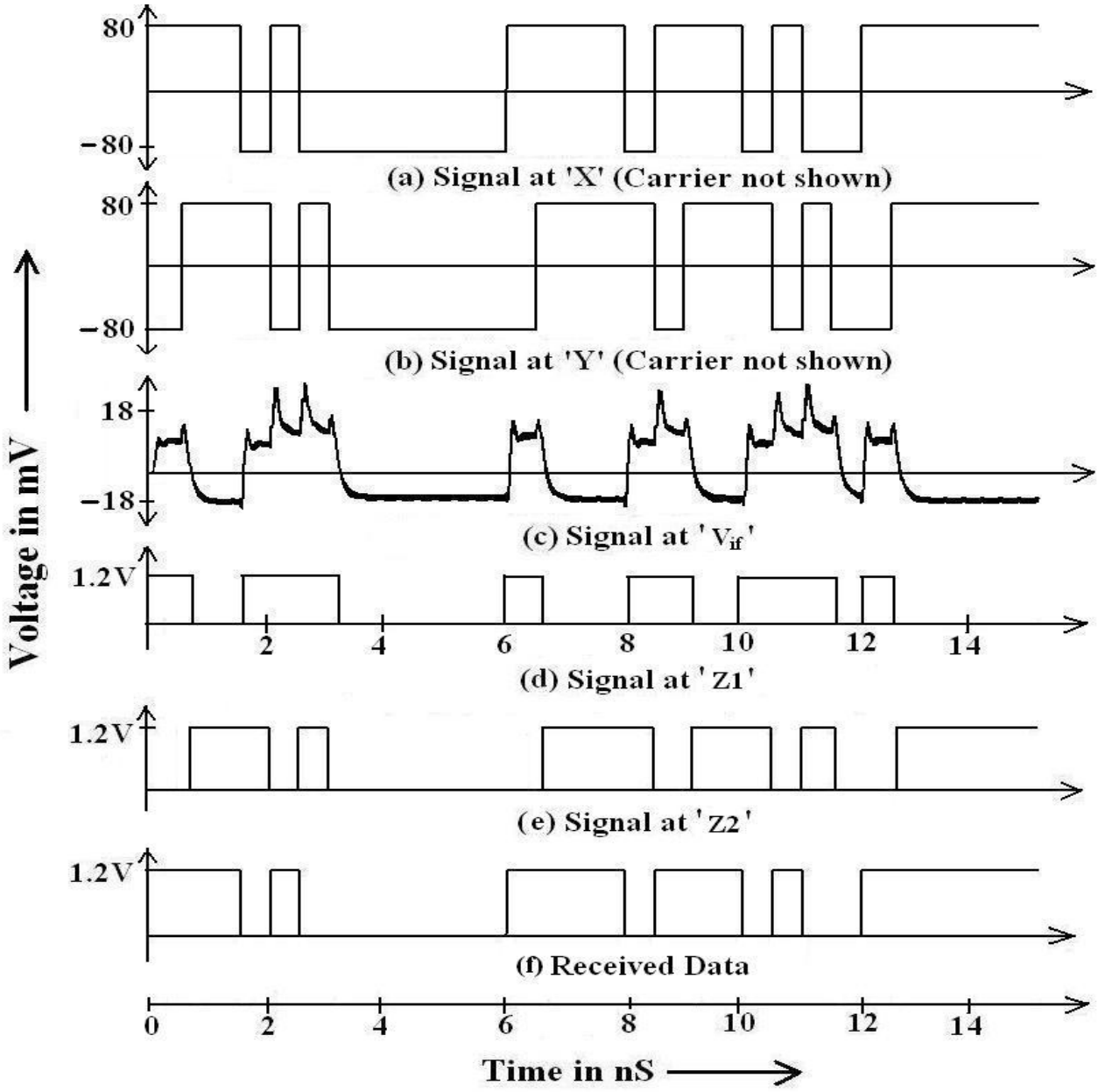

Figure 5.29: Signals at different nodes of the receiver of Fig. 5.28

Note that, only digital information is shown in Fig. 5.29(a) and (b) excluding the BPSK carrier for clarity. Here, the signal at node 'X' is in fact the transmitted data which is to be detected. But remember, only envelop is shown in the figure whereas, it is actually a BPSK signal and so, still to be detected. The ideal delay element delayed the signal at node 'X' by one bit duration to node 'Y'. Output of the receiver front-end (v_{if}) can be found in Fig. 5.29(c). It can be related to the transmitted bit stream of Fig. 5.29(a) to

realize that, a '1' in v_{if} means a transition in received data. So, this signal can conveniently be considered as the differential information. Thus, the performance of the receiver front-end is verified.

Now, an ideal differential to single ended comparator with zero-threshold level will generate the bit-streams of Fig. 5.29(d) (at node Z1). On the other hand, the sampling and hold circuit, S/H will sample the received data at the output of the XOR gate and will hold it for one bit duration. The signal at node Z2 can be found in Fig. 5.29(e) where zero initial condition was assumed and the circuit was considered as ideal. Finally, the received data can be found at the output of the XOR gate, which is shown in Fig. 5.29(f) and it is merely the unipolar form of the transmitted data shown in Fig. 5.25(a). So, the detection process was successful.

This circuit consumes only 27 mW power including biasing circuitry from 1.2 V power supply. Layout of the unified receiver front end of Fig. 5.12 is given in Fig. 5.30. It occupied 0.94 X 0.5 = 0.47 mm^2 and 1.3 X 0.66 = 0.86 mm^2 areas without and with probe pads respectively. Layout of the whole chip (2 X 2 = 4mm^2) can be found in Fig. 5.31, where a lot of floating metal layers can be seen which were used for metal density requirement (filling).

Therefore, the unification technique proposed in this chapter gave rise to a simple, low power and compact unified receiver front-end. Other features of the circuit is quite attractive especially for low signal power applications such as on-chip wireless interconnect system. The circuit could detect traditional digital signals synchronously as well as asynchronously. However, the circuit is to be modified further to work with UWB signals. Next chapter will discuss on the modified receiver front-end and will show how well that modified circuit can extract digital information from UWB pulse stream. But, before moving onward, performance of this folded mixer is compared with state of the art in Table 5.1.

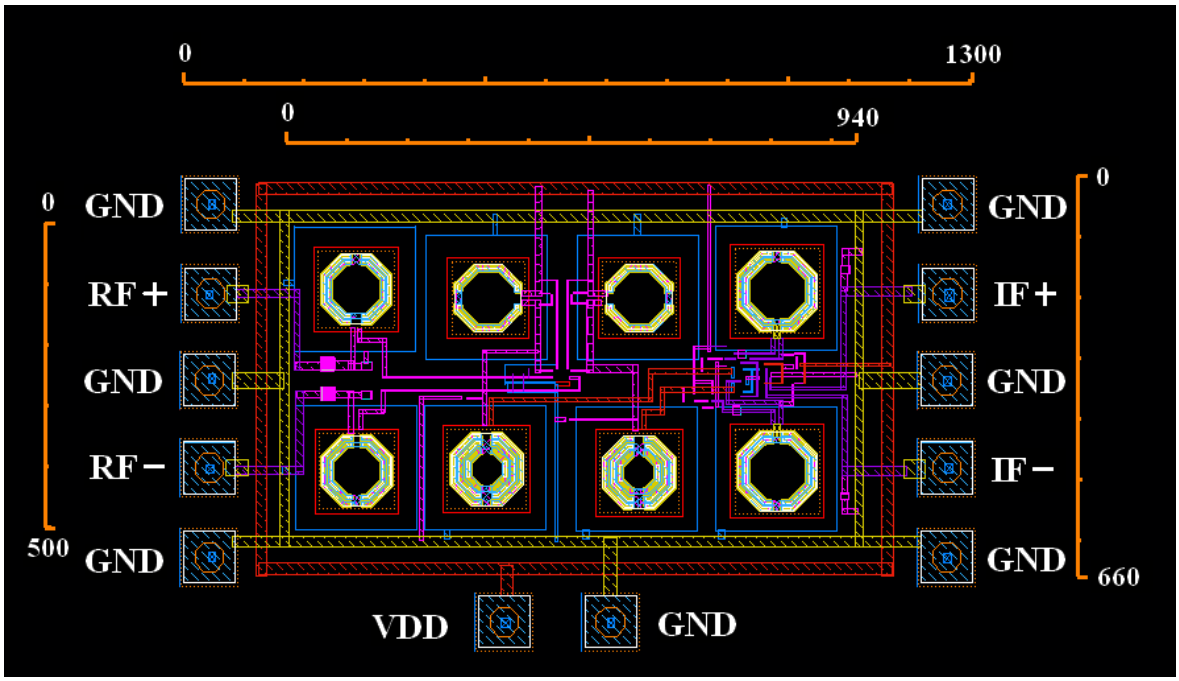

Figure 5.30: Layout of the receiver front-end of Fig. 5.12

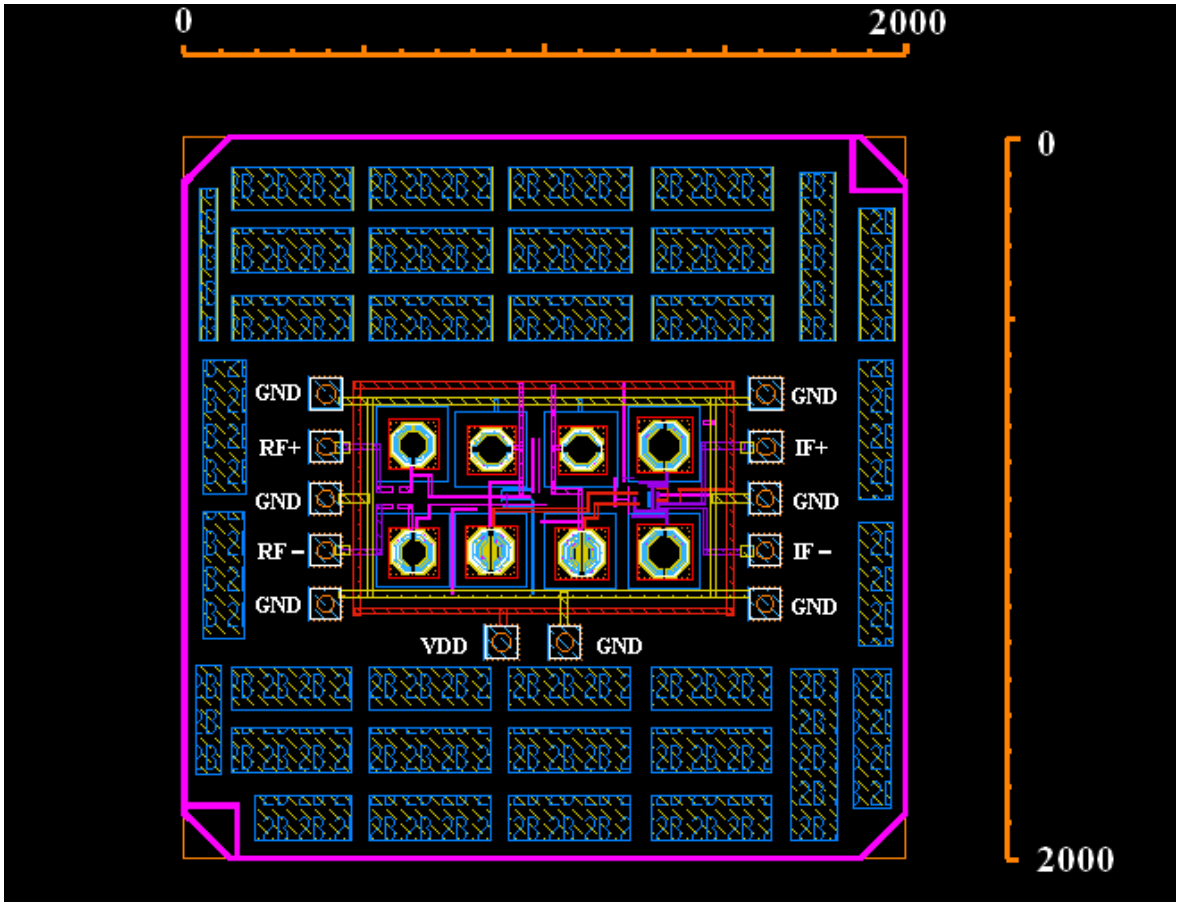

Figure 5.31: Layout of the whole chip

Table 5.1: Comparison of the folded mixer with state of the art:

Reference	**This Work***	**[22]**	**[23]**	**[25]**	**[53]**
Technology	90 nm CMOS	0.18 µm CMOS	0.13 µm CMOS	0.13 µm CMOS	0.18 µm CMOS
Topology	Folded Mixer (LNA+Mixer)	2-Stage Gilbert's Mixer	Sub-Harmonic	Dual Gate	Gilbert's Mixer with Gain Enhancement
Operating Frequency (GHz)	20	24	24	25	24
Conversion Gain (dB)	15	13	12.5	5.2	9.12
Bandwidth (GHz)	2.7	N/A	0.44	10	4
RF Port Matching (dB)	-26	-21	-10	-25	-20
LO Port Matching (dB)	-24	-10	-10	-20	-20
Input Ports Isolation (dB)	< -10	N/A	< -65	< -33	< -26
Input-Output Feedthrough (dB)	< -50	< -31	N/A	< -52	N/A
NF in dB	7.8	17.5	7.4	N/A	~10
1 dB Compression Point (dBm)	-18	-23	-6 (IIP3)	-5.8	-11
Power Consumption (mW)	27	40.5	76.8	8	16.2
Area (mm^2)	0.47	1.5	3	0.47	1.3

*****schematic simulated responses

CHAPTER 6

OPTIMIZING THE RECEIVER FRONT-END TO DETECT HIGH SPEED DIGITAL DATA USING UWB TRANSMISSION

The receiver front-end designed in previous chapter detected traditional digital signals successfully. Now, this is the time to work with UWB signals for detecting high speed digital data using TR-UWB transmission introduced in chapter 2. The transceiver architecture of Fig. 2.1 is recalled in Fig. 6.1. The idealistic picture of the detection process was portrayed in Fig. 2.6 and is showed again in Fig. 6.2.

Now, design of any receiver depends substantially on the received signal, which in turn depends on the transmitter system. In this chapter, at first the transmitter and the received signal will be analyzed to determine the design objectives of the receiver. Then, the receiver front end designed in previous chapter will be modified accordingly and will be examined. Then that circuit will be employed in the receiver to detect the received TR-UWB pulse stream. Finally, the communication topology will be optimized so as to encounter all technological limitations.

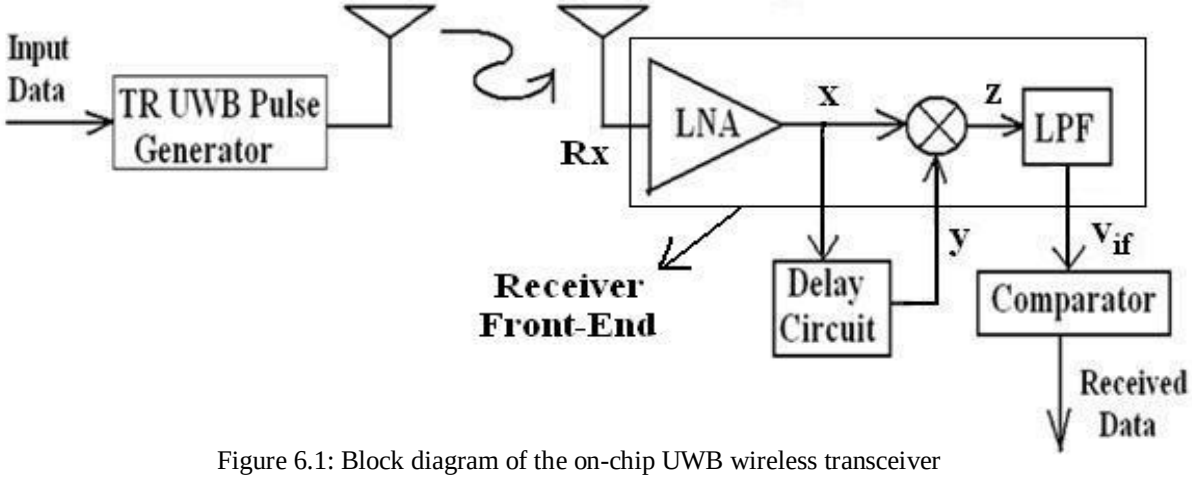

Figure 6.1: Block diagram of the on-chip UWB wireless transceiver

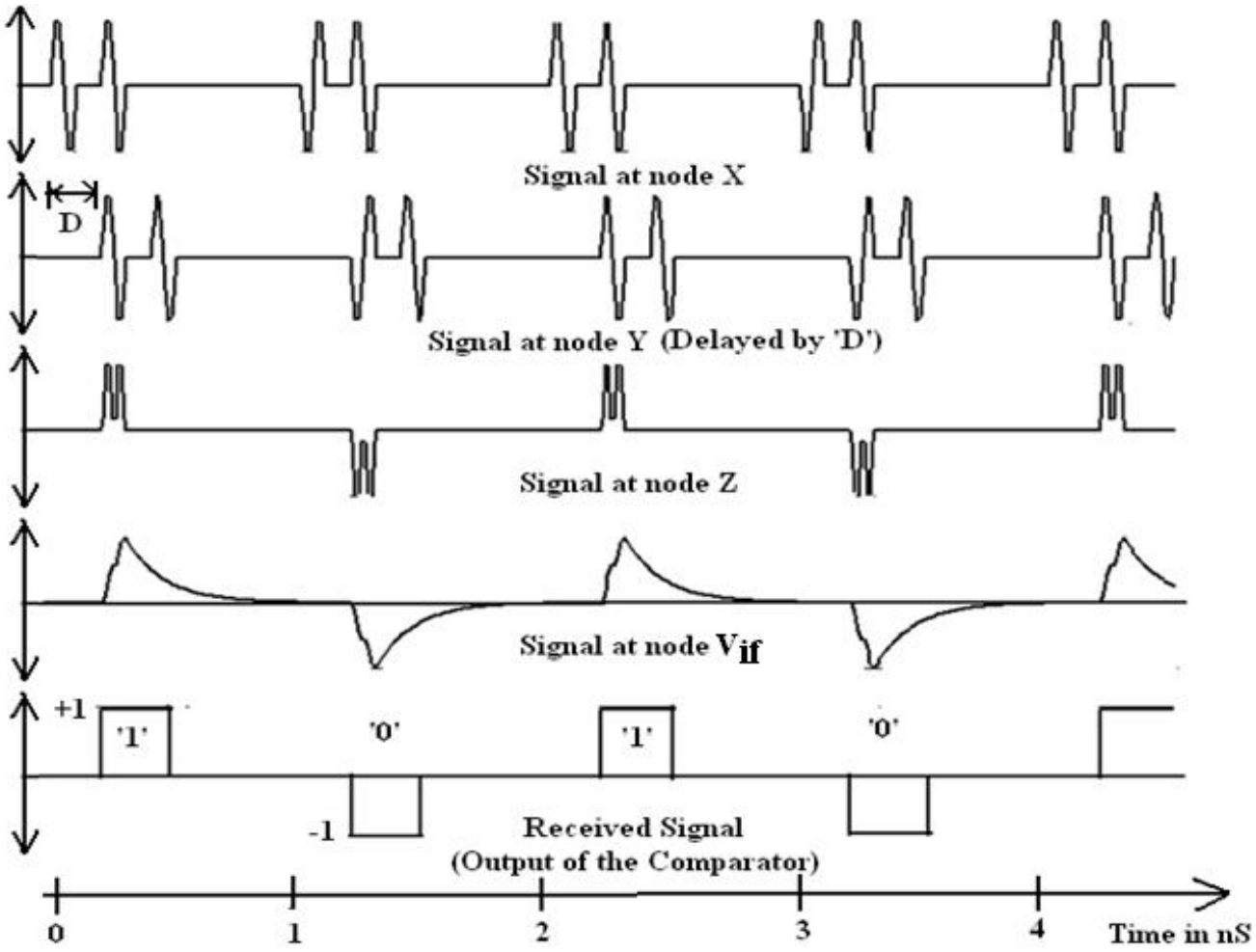

Figure 6.2: Signals at the nodes of the receiver of Fig. 6.1

6.1 Design Objectives of the Receiver Front-End

As mentioned earlier, design objectives of the receiver front end depends on the received signal. In this system, the received signal resembles the signal generated by the pulse generator of the transmitter. Such a pulse generator can be found in [24] that was designed particularly for this system. Detail discussion of that circuit is available in [69].

However, in this work the TR-UWB pulse stream generated by that pulse generator was modeled using the block diagram of Fig. 2.3 considering all the circuit elements as ideal. The resulting signal is depicted in Fig. 6.3 and its frequency constituents are shown in Fig. 6.4.

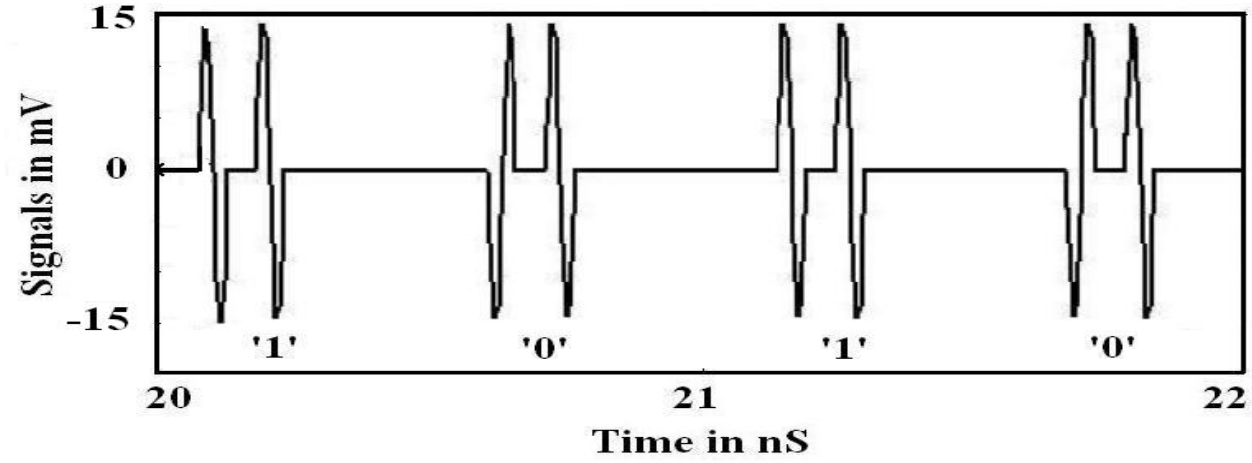

Figure 6.3: Received signal at node 'Rx' of the block diagram of Fig. 6.1

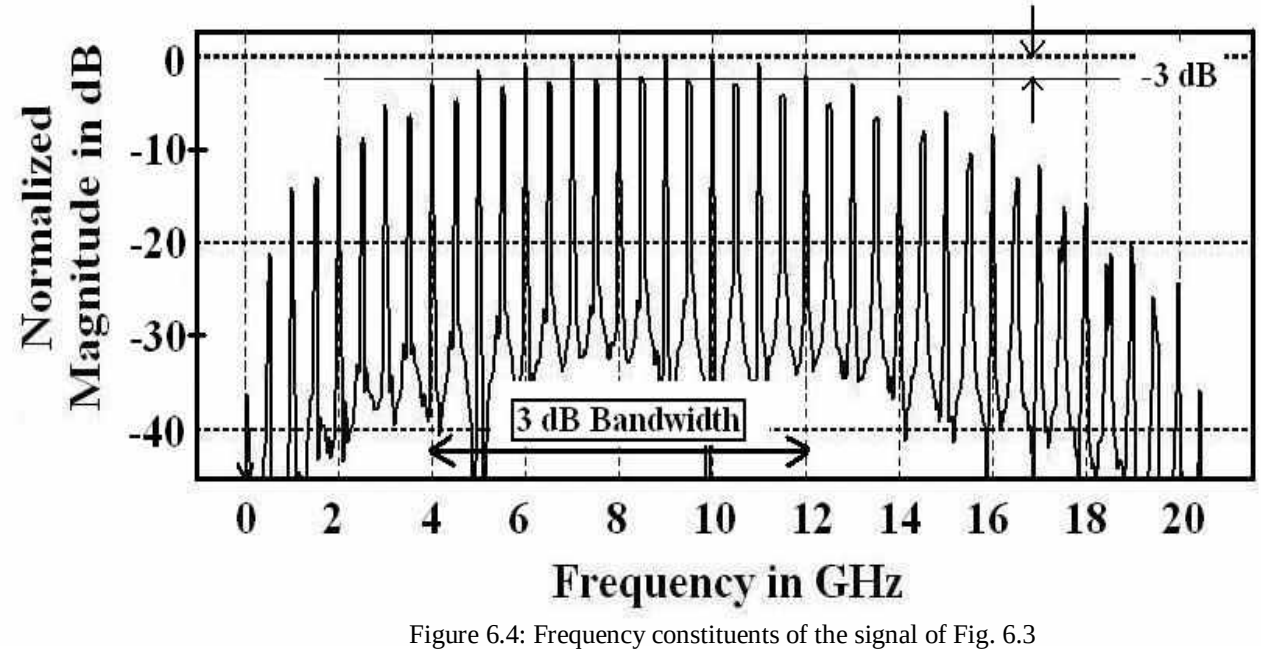

Figure 6.4: Frequency constituents of the signal of Fig. 6.3

Observation of Fig. 6.4 indicates that, the center frequency of the antenna pair used in previous chapters is to be reduced from 20 GHz to 10 GHz band. Although quite possible, but this is beyond the scope of this work. That is why; a 23 dB attenuation will be imposed here on the transmitted signal, which was experienced by the transmitted signals of previous chapters. Again, since 10 GHz band is pretty high and the antenna pair can be redesigned to handle this signal conveniently, so no up-conversion will be required in the transmitter i.e. square law up-conversion mixer designed in chapter 3 will not be used.

Now, about the design objectives of receiver circuitry- Fig. 6.4 shows that, the signal of Fig. 6.3 occupies a bandwidth of 8 GHz (4 GHz - 12 GHz). So, there will be a couple of major design objective for the circuits of receiver front-end. First, they should have bandwidths of nearly 8 GHz and second, with the center frequency preferably at 8 GHz. Next section will describe how the circuit designed in chapter 5 can be optimized to satisfy aforementioned design objectives.

6.2 Optimizing the Receiver Front-End

Extension of bandwidth and shifting of the center frequency will involve input-output matching issues. So, the receiver front end is to be modified judiciously to optimize the circuit in terms of power, space and simplicity that is pretty complicated. This section will describe the optimizing technique in detail. At first, let us extend the bandwidth of the receiver front end.

6.2.1 Extension of Bandwidth

To extend the overall bandwidth of the receiver front end, at first the bandwidth of the LNA is to be increased. There are several techniques available in literature. Most popular is- using multiple stages, each centered in slightly different frequencies, so as to get a wider bandwidth as whole. This topology can be found in [70-71]. But, as one should expect, their space and power requirement multiplies by the same scale as the number of stages. Another way of increasing bandwidth is the use of resistive or reactive feedback [72-75], but at the expense of gain. Moreover, matching and isolation becomes complicated. Next comes concurrent topology [76-79], where notch filter is used at the input or output or in between stages to eliminate a band of frequency from the total bandwidth of the LNA. This is in fact dual band scheme popular for band selection, can not provide ultra wide bandwidth and getting more than a couple of frequency band from this topology is quite difficult since it in effect cleaves a bandwidth rather than increasing

it. Current reuse technique was used in [80] to increase the power gain in conjunction with inter-stage matching between a couple of stages each tuned at slightly different frequencies to increase the bandwidth as well. On the other hand, concept of trans-impedance filter was introduced in [81] for bandwidth extension. However, none of this couple of design is straight forward. They involve a lot of design issues. Yet, another interesting technique is to use inductive peaking [82-84] in output side or input side or in both. But again, this method relies on coupling co-efficient of on-chip inductors, thus complicated, less predictable and space consuming.

In this work, a simpler technique [85] was used to increase the bandwidth sacrificing gain, simplicity, noise, power and space by minimum extent. The modified circuit is portrayed in Fig. 6.5. Here, the bandwidth was increased by using a stacked tuning network at the load end of the LNA. This technique was used in [85] without any detail. However, in the circuit of Fig. 6.5, L1, C1 and L2, C2 are tuned at 7.5 GHz while L3, C3 and L4, C4 are tuned at 10.5 GHz. The voltage gain of LNA i.e. first stage, is shown in Fig. 6.6, where the bandwidth extension is clearly visible. Since, the power gain parameter (S21) is closely related to voltage gain, so the bandwidth of S21 can be expected to increase if the matching of the circuit is good. Matching issues of this circuit is not so easy for all the input, output and inter-stage matching have to be over a wide bandwidth. Next few sections will explain how the matching issues were dealt with to optimize the receiver front end.

6.2.2 Inter-Stage Matching

Inter-stage matching is of prime importance in this scenario, because the wide bandwidth of the LNA will be fruitless if it has to drive a poorly matched mixer stage. So, matching network between the stages has to be well designed not to spoil the gain response of the LNA. Output impedance of the LNA is shown in Fig. 6.7, where the reactive part looks good, but the resistive par needs much attention. Inter-stage matching would be perfect if high order filters such as Chebyshev filters [86-87] could be used as matching

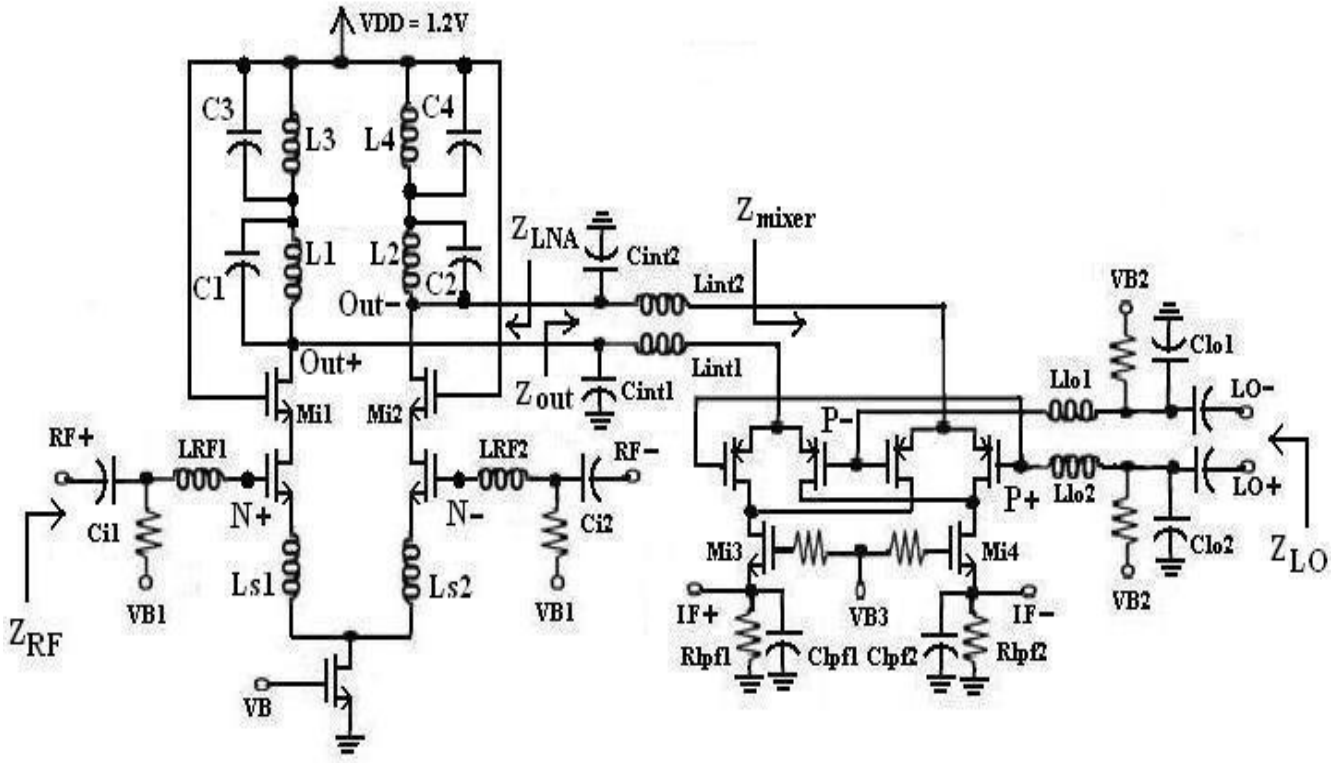

Figure 6.5: Receiver front-end to work with TR-UWB signal

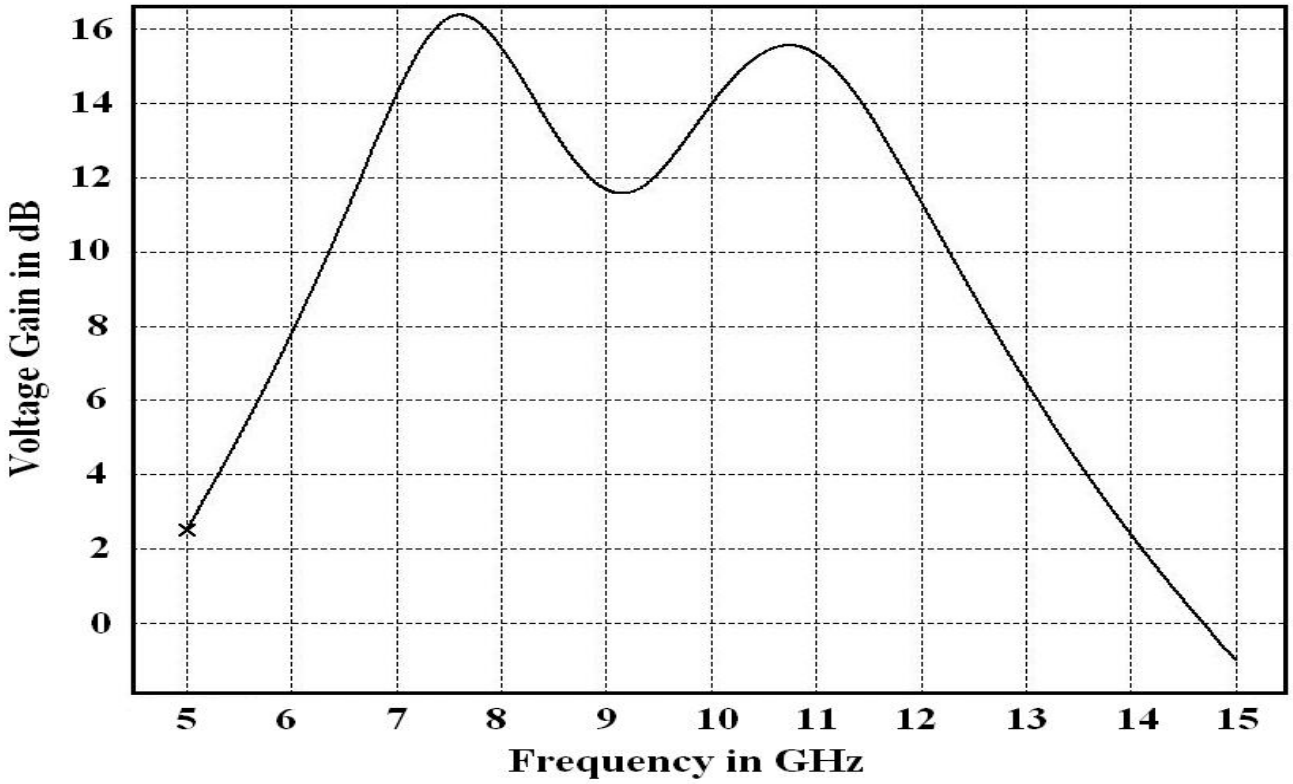

Figure 6.6: Voltage gain of the first stage of the receiver front-end

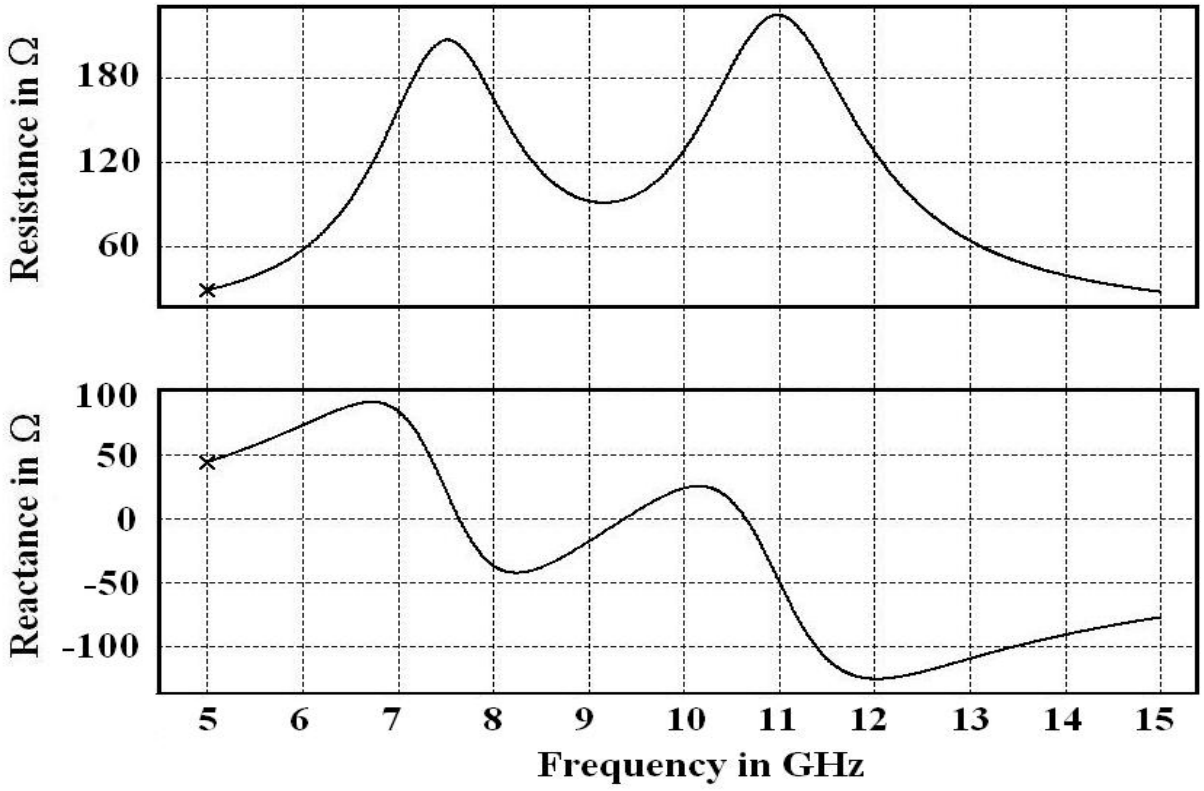

Figure 6.7: Z_{LNA} of Fig. 6.5 versus frequency

network to get a two prong real part similar to the $Re[Z_{LNA}]$ of Fig. 6.7, but again, those high order filters need number of on-chip inductors, so are area consuming and thus is to be optimized.

To investigate further, gain (S21) and output matching parameter (S22) of the LNA are plotted respectively in Fig. 6.8 and Fig. 6.9 for three different load impedances, viz. Z_{out} = 100 Ω, 110 Ω and 120Ω. Output matching (S22) widens when Z_{out} increased, whereas effect of Z_{out} on S21 is insignificant. Anyways, this couple of figures reveals that, gain and output matching is satisfactory even for flat load impedances. That is why, to optimize in terms of space, the first order inter-stage matching technique of previous chapter can safely be used in this condition as well.

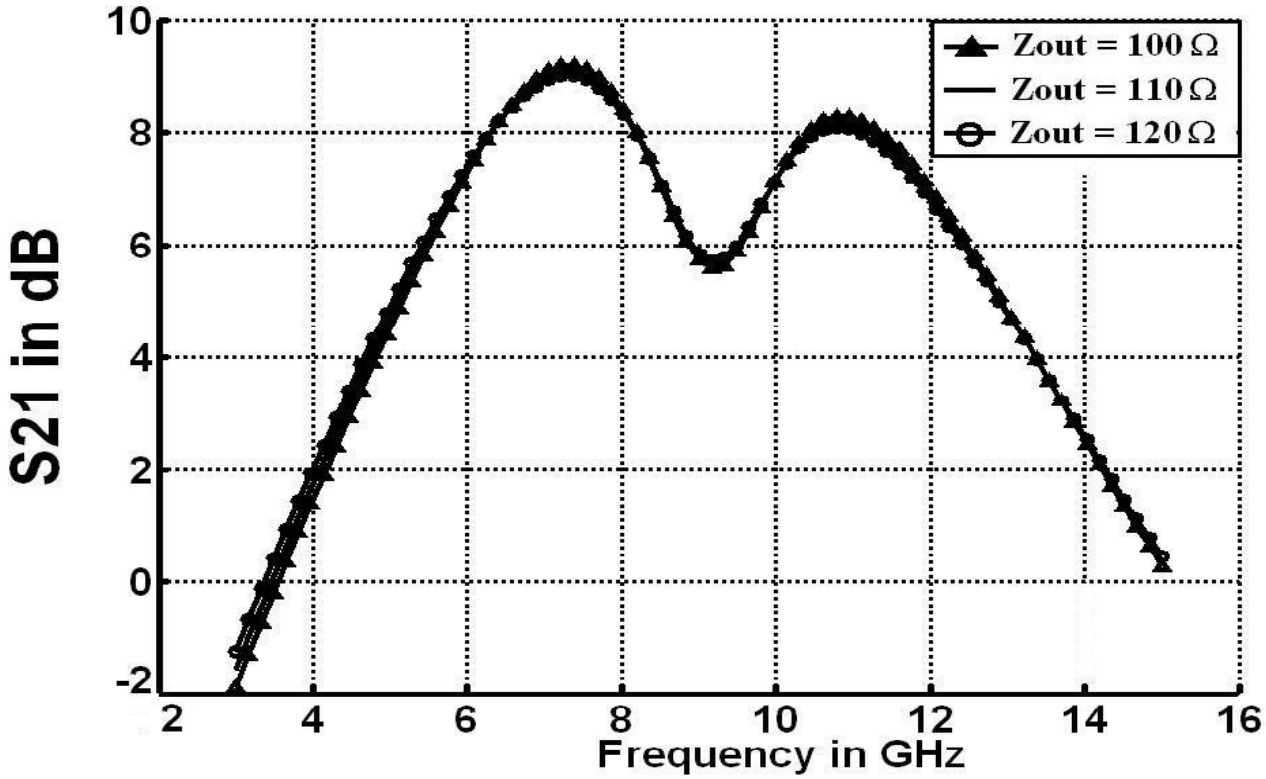

Figure 6.8: Gain (S21) of the LNA versus frequency for three different load impedances

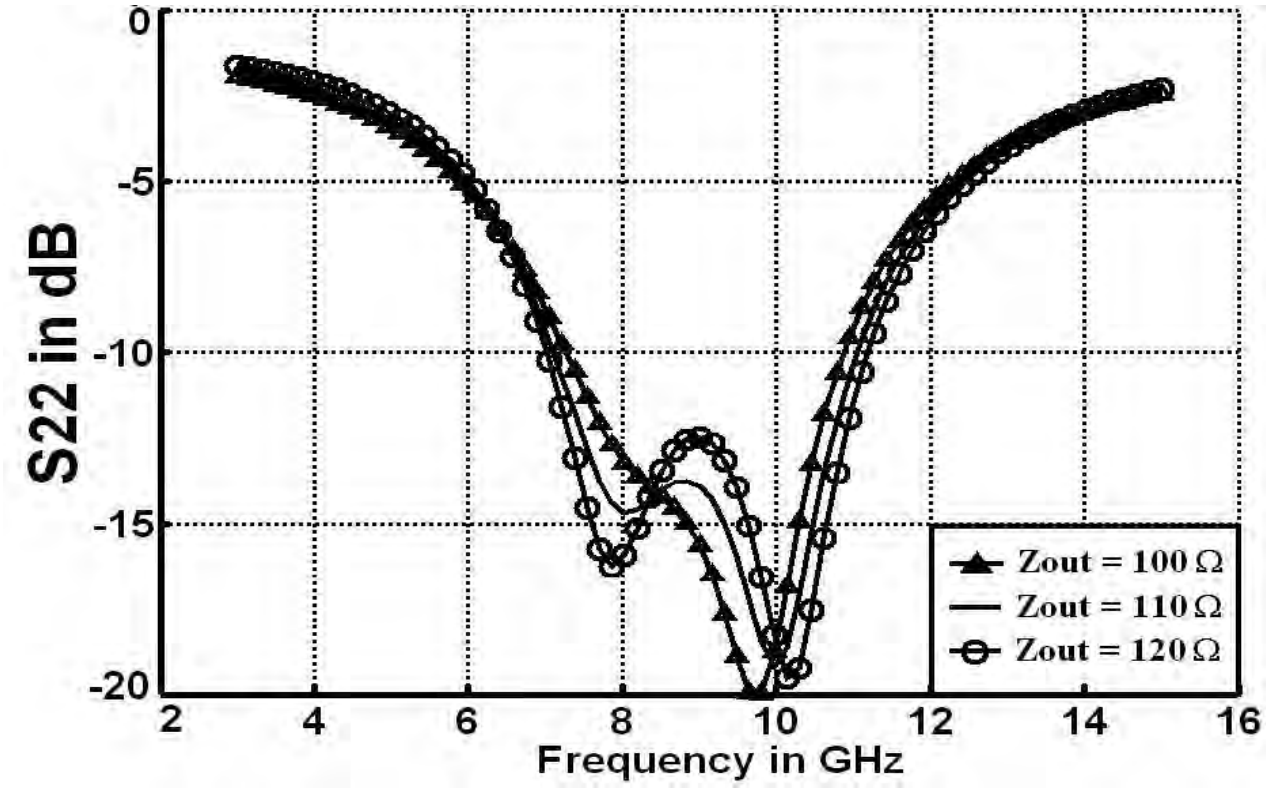

Figure 6.9: Output matching (S22) of the LNA versus frequency for three different load impedances

Input impedance of the mixer stage, Z_{mixer} is shown in Fig. 6.10, where Z_{mixer} = (92-20j) Ω at 10 GHz. Suitable values of L_{int1}, L_{int2}, C_{int1} and C_{int2} were chosen using Smith's chart, like what was done in previous chapter. Load impedance of the LNA, Z_{out} was plotted in Fig. 6.11 after matching and it is Z_{out} = (120-3j) Ω at 10 GHz. Note that, getting more than 120 Ω real part would need larger inductors, so was avoided. However, the corresponding input matching parameter (S11) of the second stage after matching is also shown in Fig. 6.12. Since, gain & output matching of the LNA and the input matching of the mixer (Fig. 6.8, 6.9 and 6.12) are over wide band, so the inter-stage matching can be considered as satisfactory for this application.

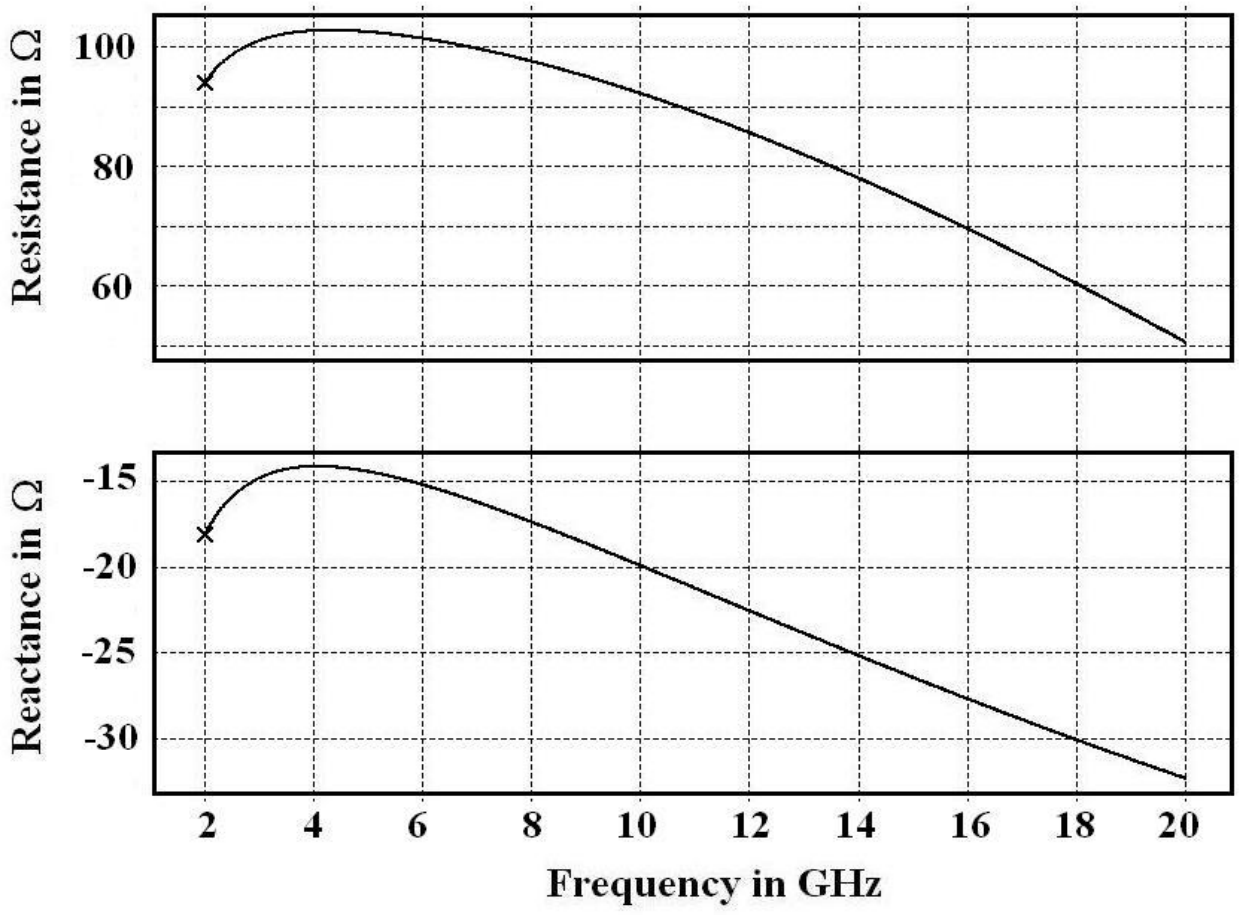

Figure 6.10: Z_{mixer} of Fig. 6.5 versus frequency

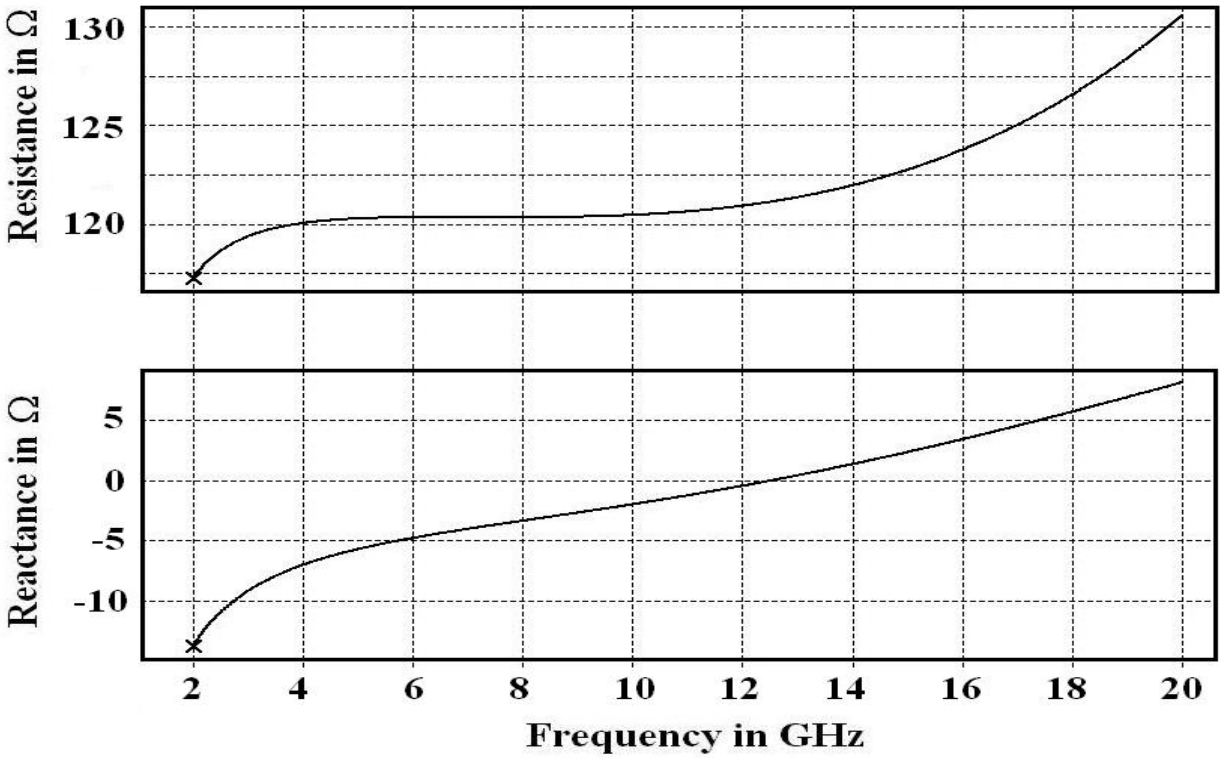

Figure 6.11: Z_{out} of Fig. 6.5 versus frequency

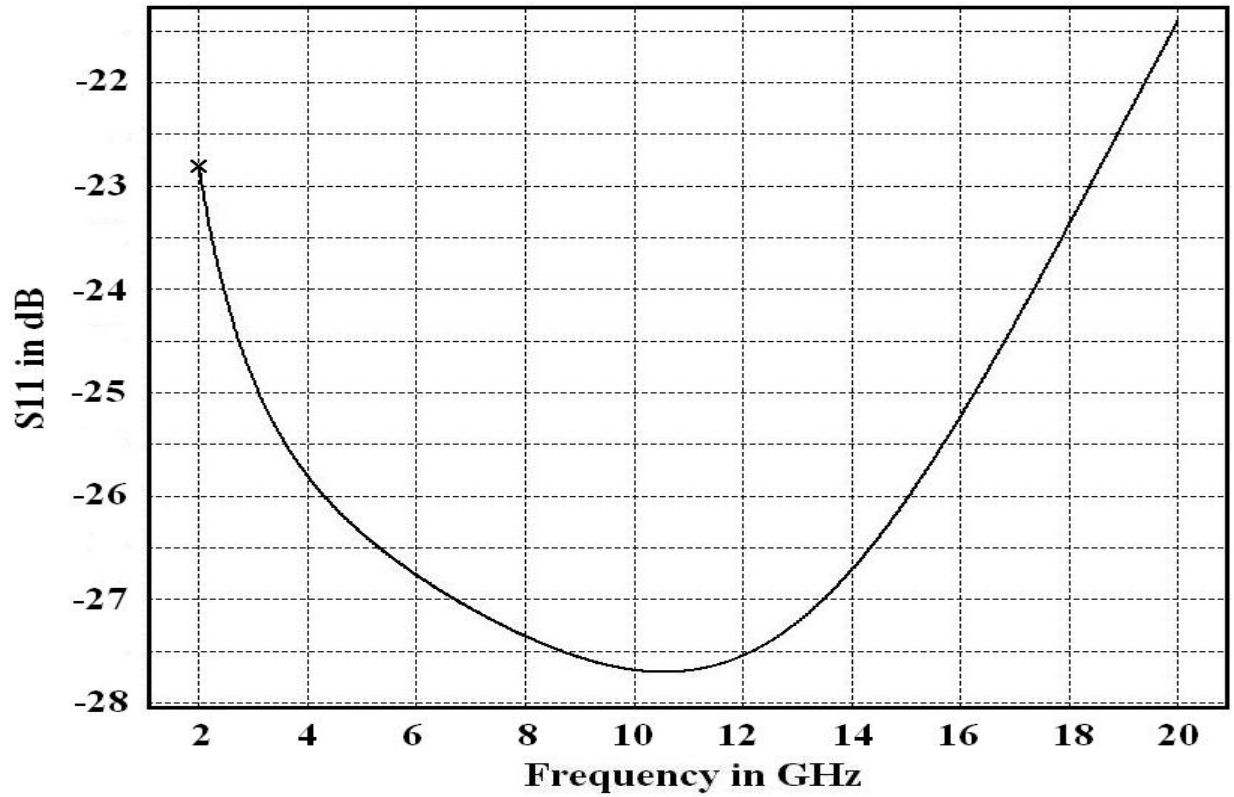

Figure 6.12: S11 of the second stage of Fig. 6.5 versus frequency

Anyways, benefit of this good inter-stage matching will not be available if the signal distorts much in the input ports i.e. RF and LO inputs, before reaching the inter stage. It emphasizes on good input matching. Wideband matching techniques are available in literature. For instance, [86-87] used 3rd order Chebyshev filter for input matching. Again, [88] used ladder based matching for the input side. Another interesting way of input matching is by using split input technique [89-90] where, input signal was fed simultaneously to a couple of parallel input ports, each matched for slightly different frequencies. This technique would suit pretty well for this circuit. However, all the wideband matching schemes mentioned here involve much complicacy. Also, area budget is to be considered at the same time, especially where the circuit is differential.

On the other hand, it will be shown that, distortion due to narrowband matching will not vitiate the performance of this digital system. In other words, input matching of this receiver front end will be optimized only for digital application and so, it may not be applicable for analog system where least possible distortion is desired. Next couple of sections will explain the input matching of this receiver front-end.

6.2.3 Matching of LO Input Port

Narrow band matching was preferred here, as mentioned above. The input impedance of the LO port, Z_{LO} is shown in Fig. 6.13 before the matching network consisting of L_{lo1}, L_{lo2}, C_{lo1} and C_{lo2} was included. Note that, Z_{LO} = (15-320j) Ω at 10 GHz, where the capacitive reactance is much higher than they were at 20 GHz e.g. -75j Ω in Fig. 4.13. So, big inductors were needed (L_{lo1} = L_{lo2} = 5.5 nH) for the LO port input matching network. This matching technique is same as that used in the LNA of Fig. 4.26. Input impedance after matching can be found in Fig. 6.14 and the corresponding matching parameter (S11) can be found in Fig. 6.15, which evinces that the matching is over narrow band. Next section will discuss on the matching of RF input port.

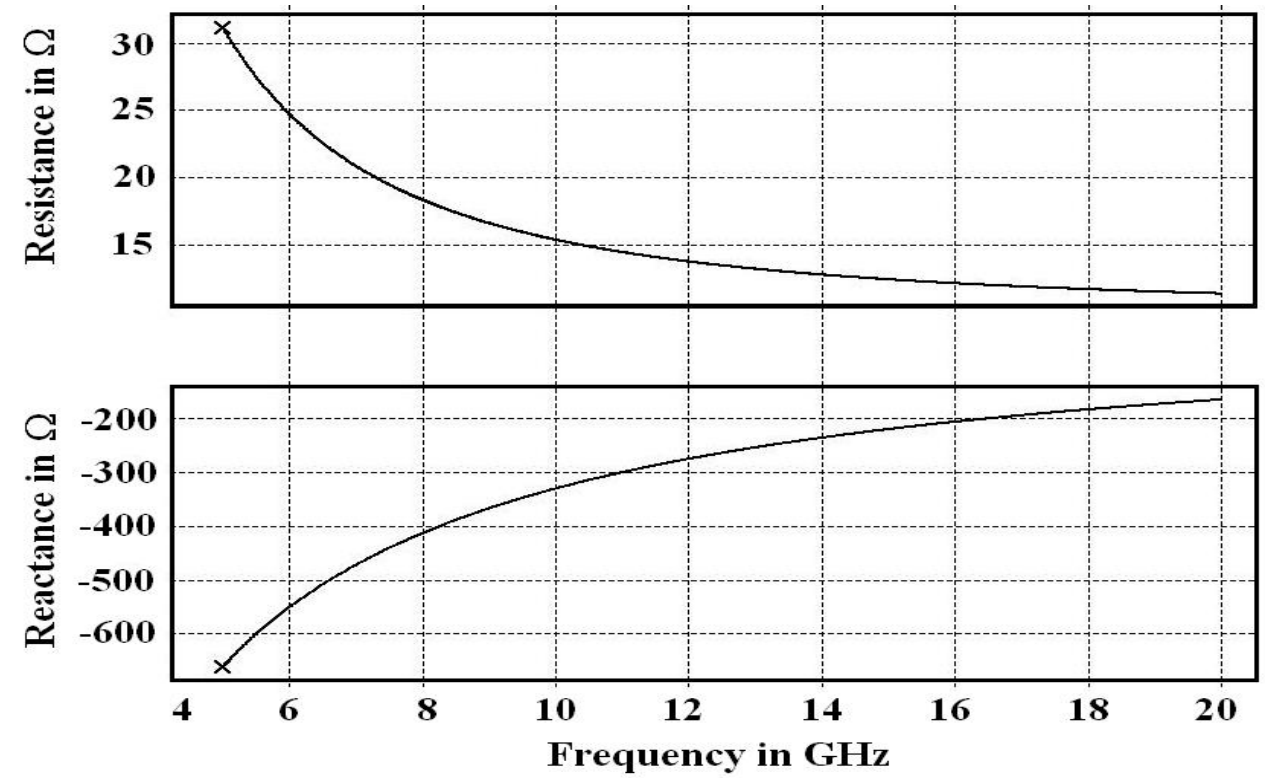

Figure 6.13: Z_{LO} of Fig. 6.5 versus frequency (Before matching)

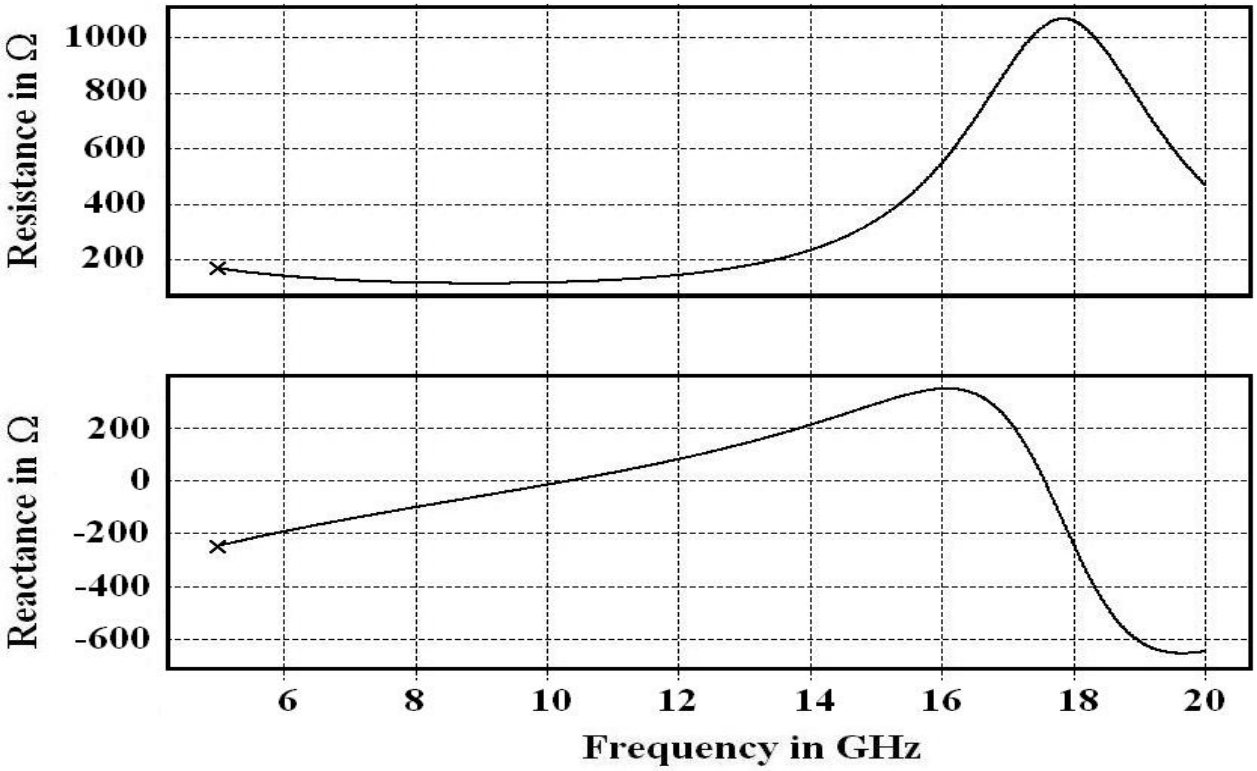

Figure 6.14: Z_{LO} of Fig. 6.5 versus frequency (After matching)

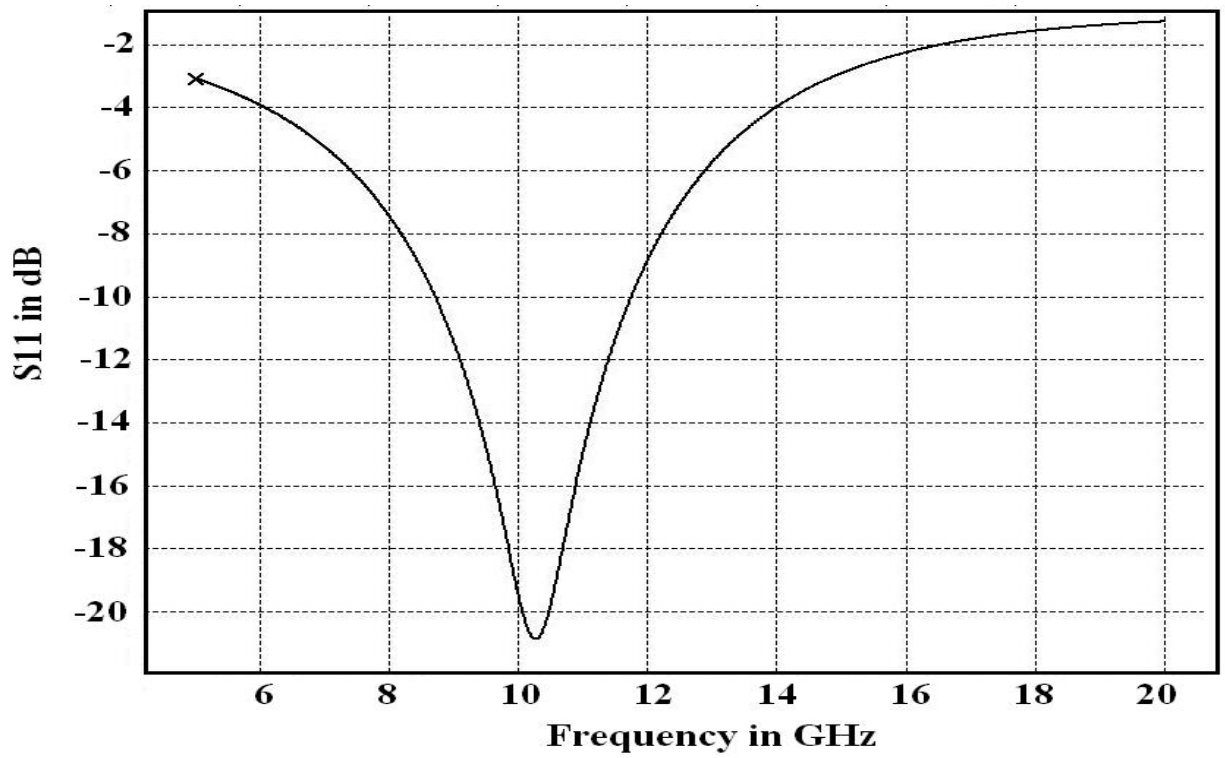

Figure 6.15: Input matching parameter (S11) of the LO port versus frequency

6.2.4 Matching of RF Input Port

Narrow band matching will be preferred for the RF input port as well. Input impedance, Z_{RF} is plotted in Fig. 6.16 versus frequency before matching, i.e. before L_{RF1}, L_{RF2}, Ls1 and Ls2 were included. Here, Z_{RF} = (25-360j) Ω at 10 GHz. Besides too high capacitive reactance, the resistive part is also large. That is why, the matching scheme used for LO port will be difficult to use here, because an inconveniently big inductor would be required then not only to compensate the input capacitance, but also to achieve a reasonable quality factor. Moreover, the self resonant frequency of such high on-chip inductors drops drastically to a few GHz that complicates the design further.

In quest of alternative, the source degenerated matching mentioned in section 4.1.1 was preferred for this RF input port. This technique is very popular in low frequencies (<10 GHz) and detail of this method can be found in [31].

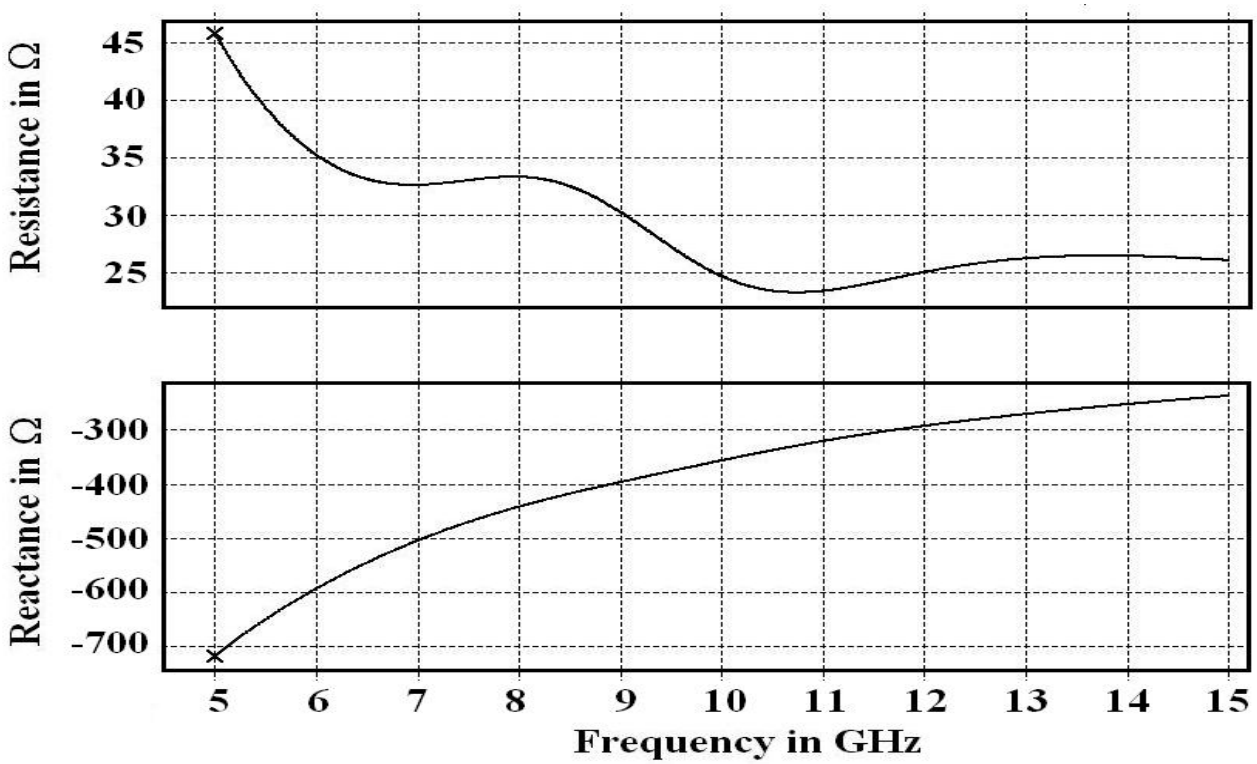

Figure 6.16: Z_{RF} of Fig. 6.5 versus frequency (Before matching)

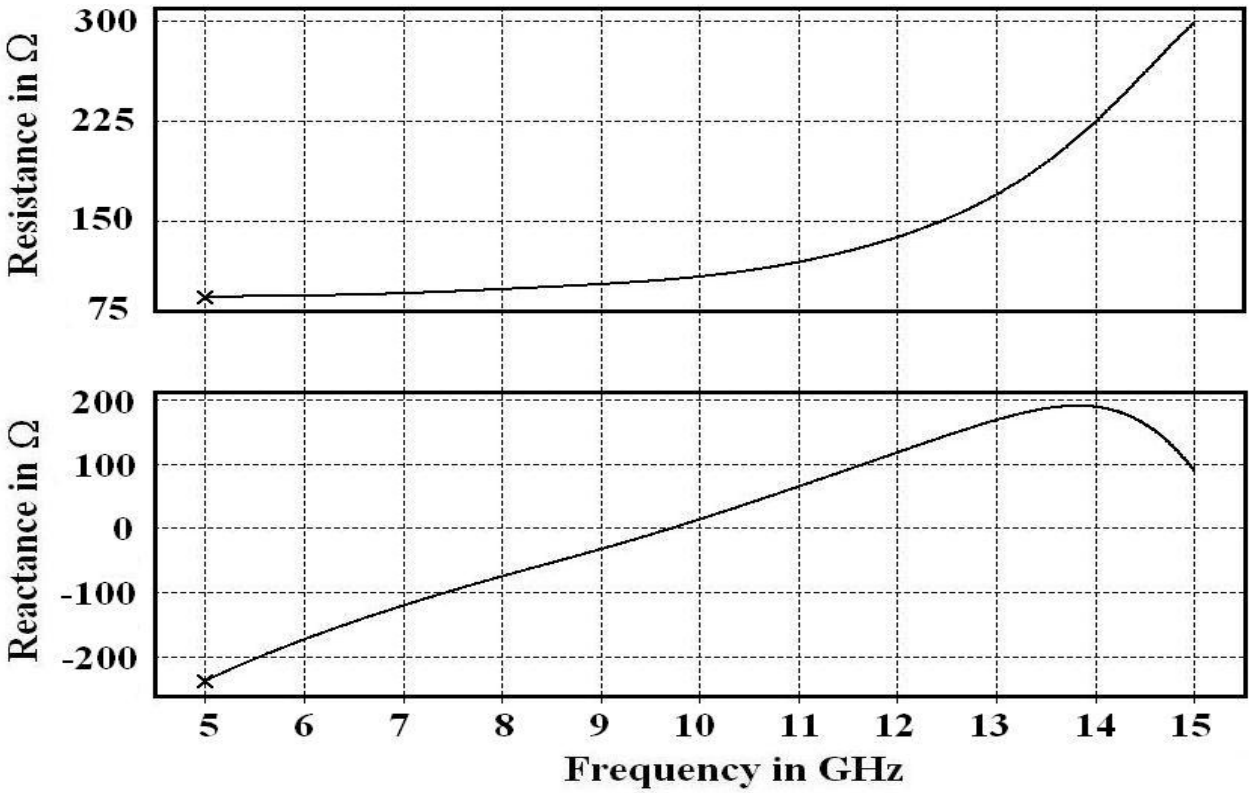

Figure 6.17: Z_{RF} of Fig. 6.5 versus frequency (After matching)

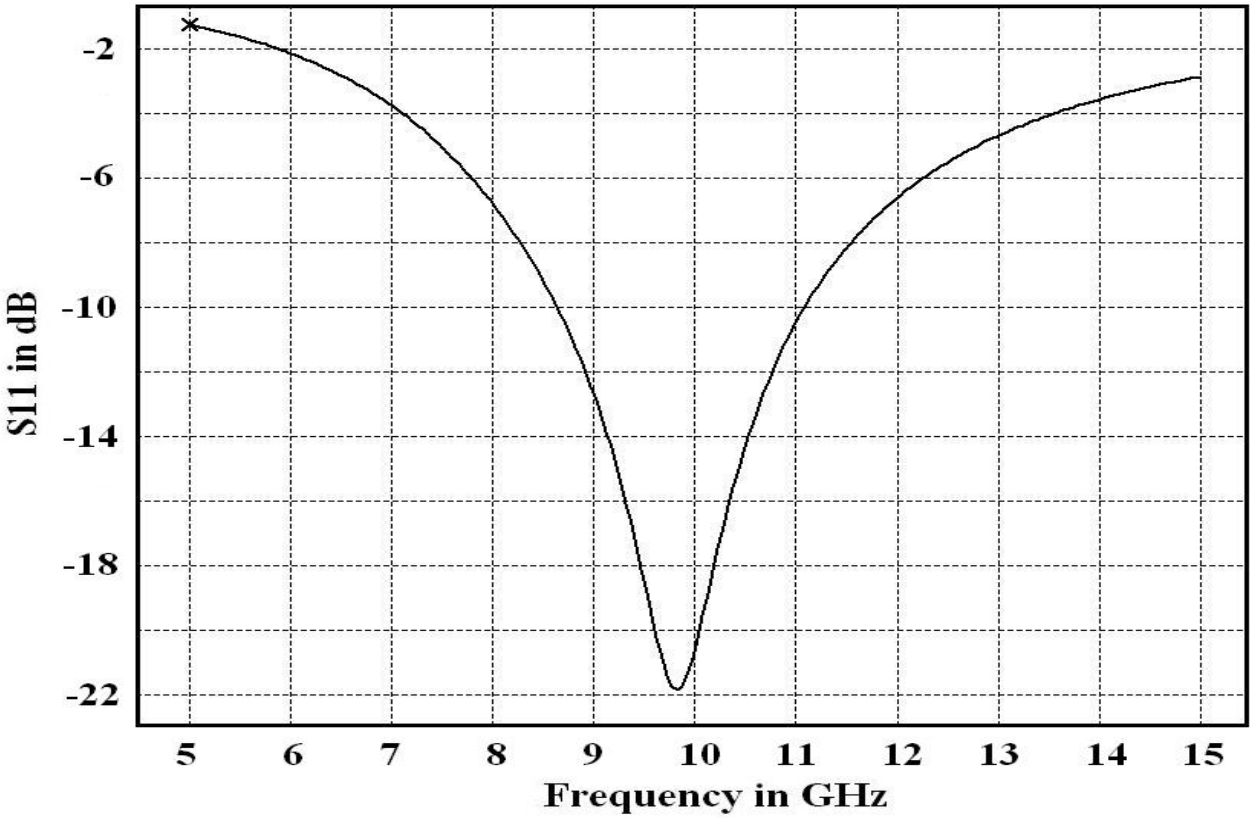

Figure 6.18: Input matching parameter (S11) of the RF port versus frequency

Input impedance of RF port is plotted again in Fig. 6.17, but this time after matching and the matching parameter (S11) is shown in Fig. 6.18, which points this matching as narrow band, as expected.

Now, let us examine what is the effect of this narrow band input matching on the performance of the receiver front end in this digital environment.

6.2.5 Justification of the Narrow Band Input Matching

At first, scattering parameters (S21, S12, S11 and S22) of the first stage i.e. LNA, are shown in Fig. 6.19 and Fig. 6.20. Cost of returning to source degeneration is the degradation of gain by about 5 dB. The peak gain is now 9 dB (Fig. 6.19) whereas it was about 14 dB in Fig. 4.27. But, its 7 GHz bandwidth exceeds well the minimum limit of ultra wideband in this condition (20% of center frequency; 2 GHz in this case). Reverse

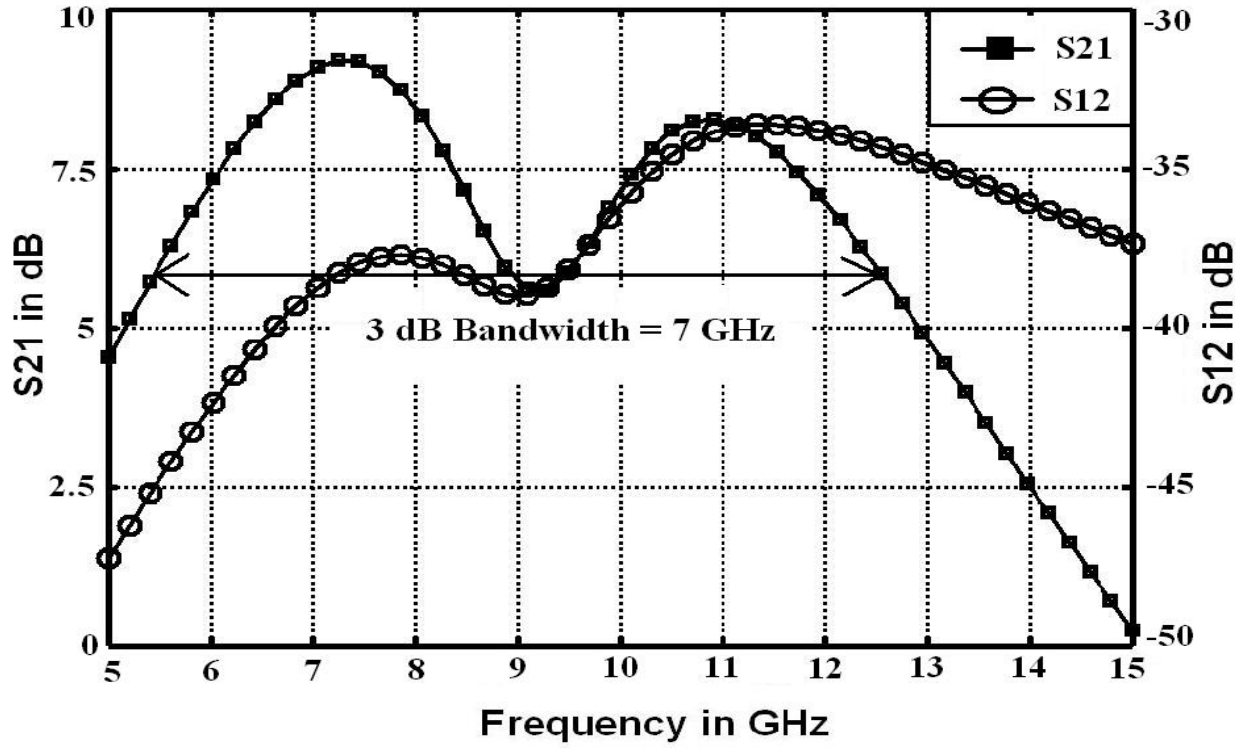

Figure 6.19: S21 and S12 of the first stage of Fig. 6.5 (LNA) versus frequency

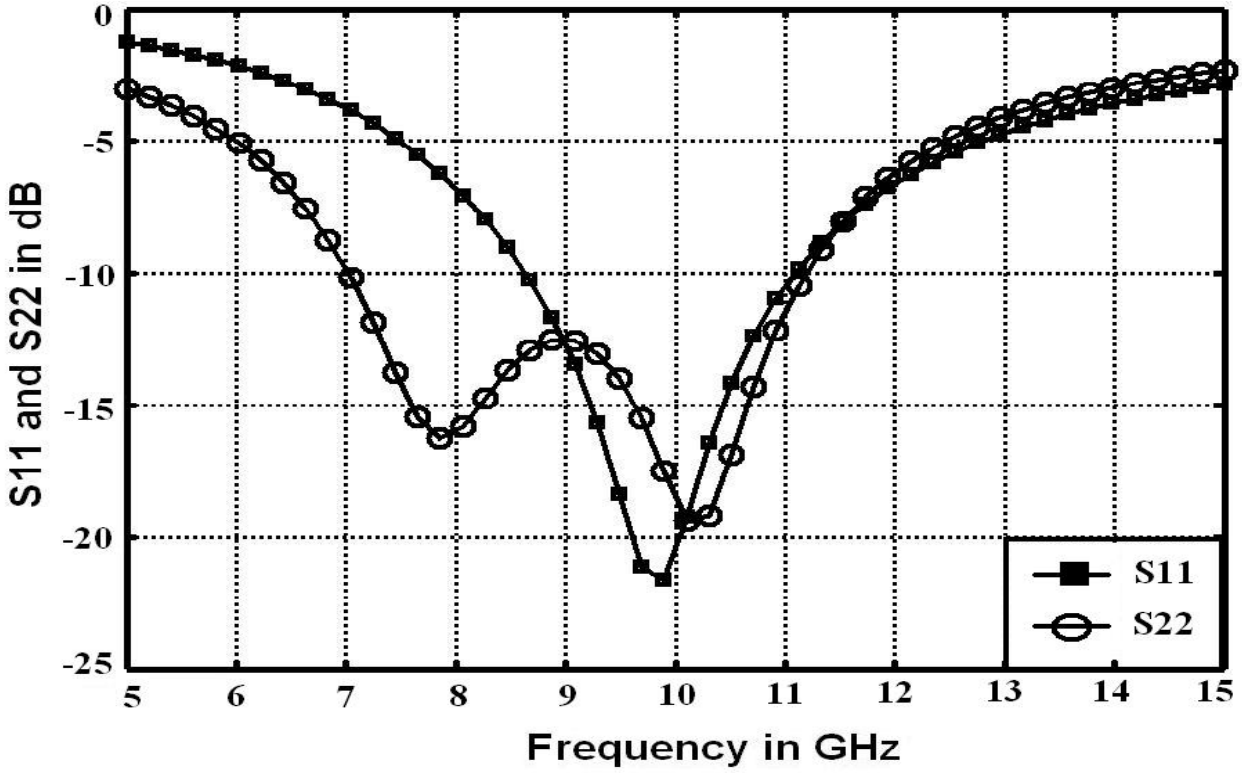

Figure 6.20: S11 and S22 of the first stage of Fig. 6.5 (LNA) versus frequency

isolation is less than -33 dB. On the other hand, although the output matching (S22 in Fig. 6.20) is over wide band, but the input matching (S11 in Fig. 6.20) is not. So, how much will it affect the performance of the circuit?

The UWB pulse stream of Fig. 6.3 was fed to the RF input port (Fig. 6.21(a)). The signal at the gate of the driving transistor (node 'N+' of Fig. 6.5) is shown in Fig. 6.21(b) and the amplified signal at the output of the LNA can be found in Fig. 6.21(c). The similarity between these last couple of signal proves that, the signal is distorted from the input side, not in the output. To investigate further, frequency constituents of the input signal and the gate signal (Fig. 6.21(a) and (b)) are depicted in Fig. 6.22, which can be compared to realize that, the reason of distortion was the attenuation of out of band signals.

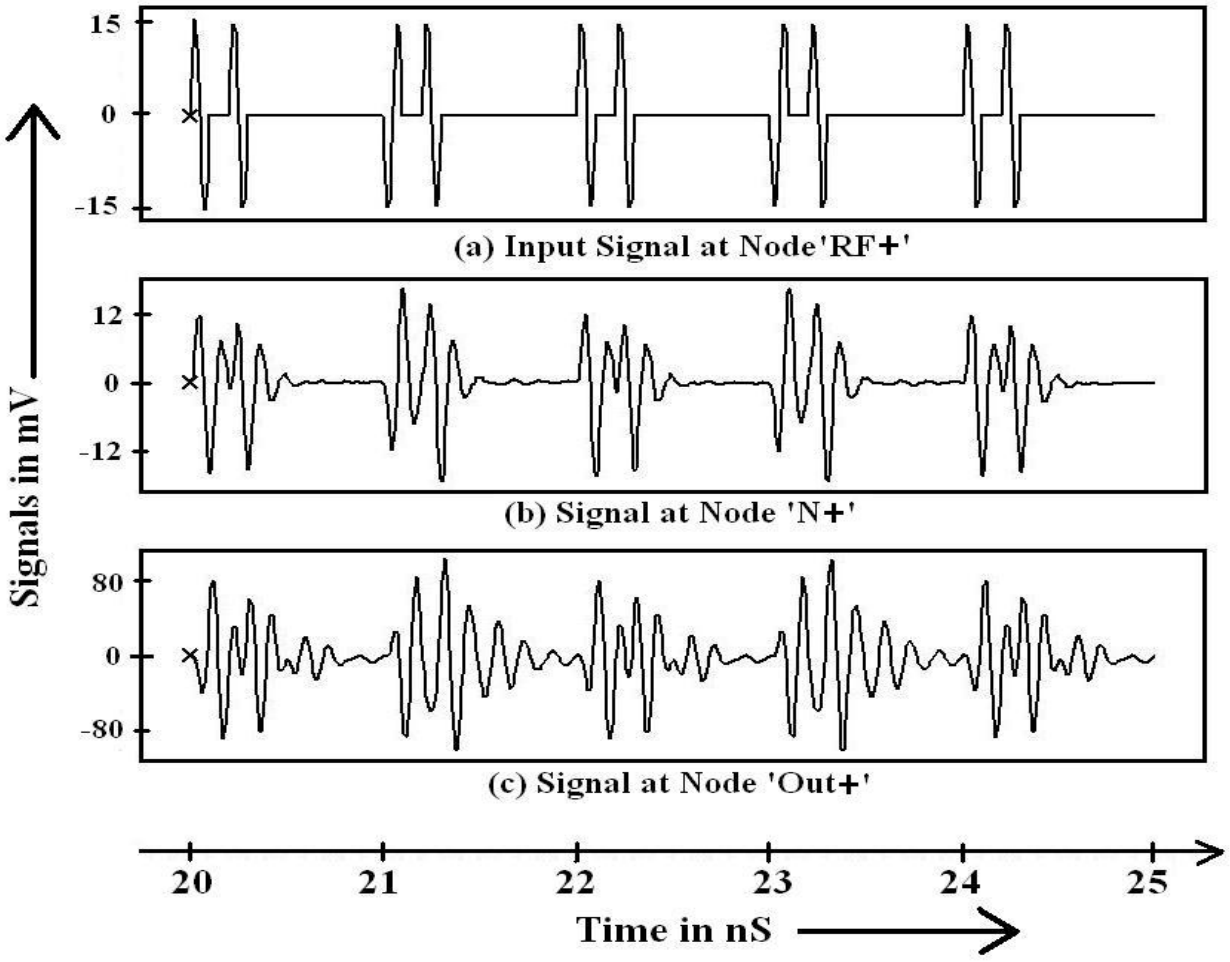

Figure 6.21: Signals at three different nodes of the circuit of Fig. 6.5 (dc quantities are eliminated)

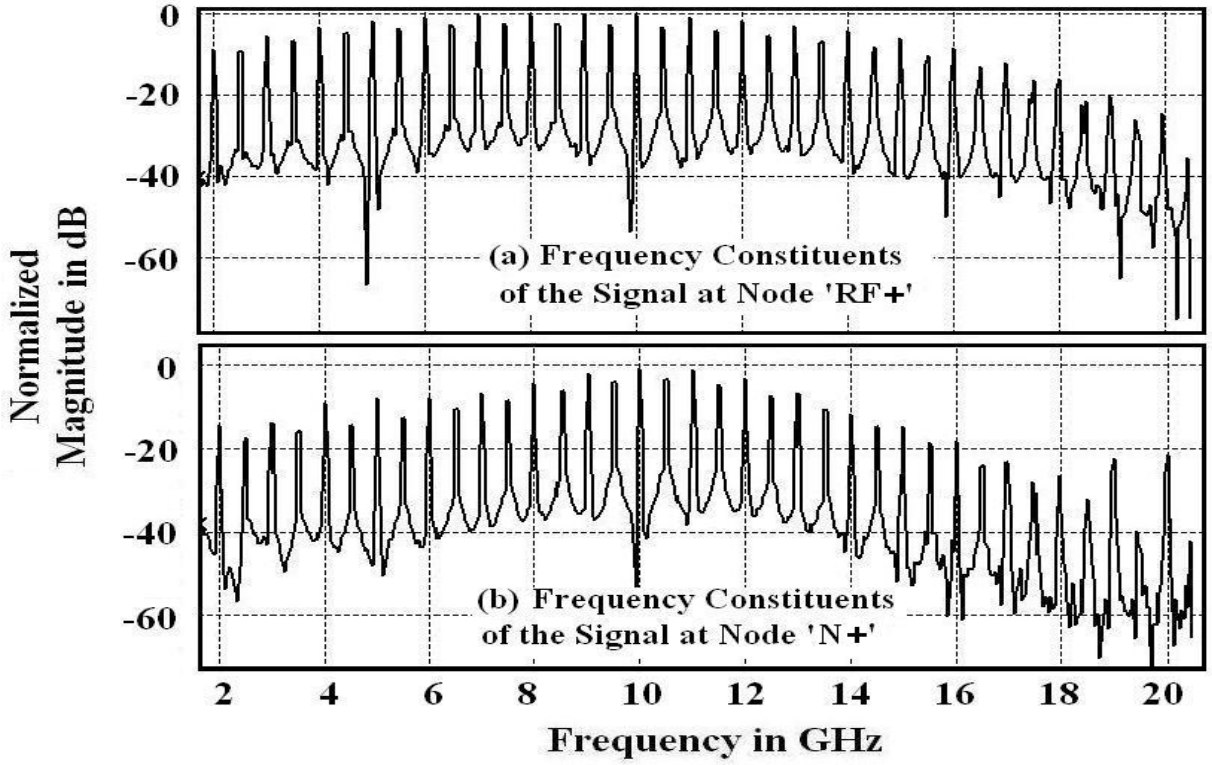

Figure 6.22: Frequency components of the signal of Fig. 6.21(a) and (b)

However, the TR-UWB signal and its delayed version was fed to the RF and LO ports respectively as shown in Fig. 6.23. The resulting gate signals are available in the same figure. Though, both are distorted but still maintain their supposed phase difference. The output of the multiplier, at node 'IF+' of Fig. 6.5, can be found in Fig. 6.23(e) where the C_{lpf1} and C_{lpf2} were removed to skip filtering for the time being. It is apparent that, those distorted signals were multiplied correctly by the multiplier and so, surely this receiver front end will work well for this digital system.

This circuit burns only 26 mW power from the 1.2 V power supply. Anyways, now, let us put some light on the noise issues of this circuit.

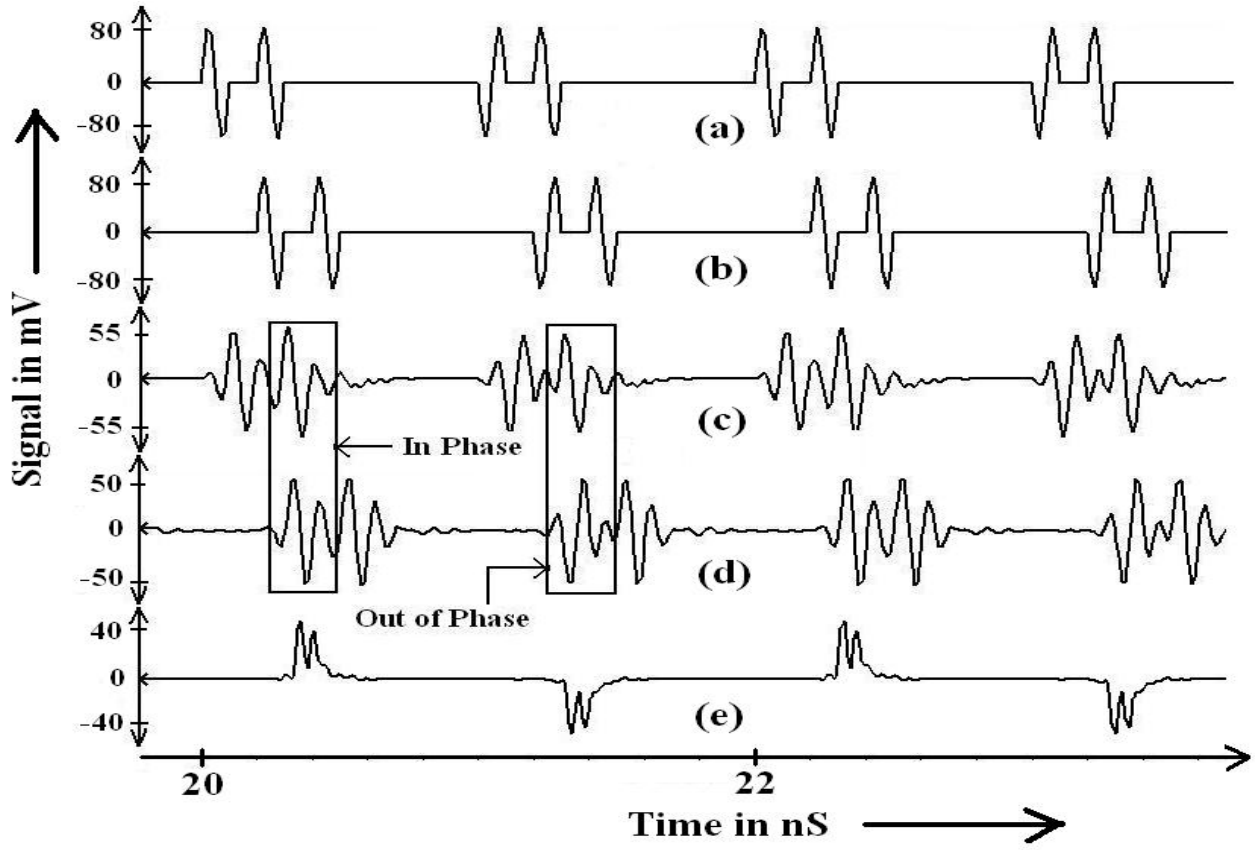

Figure 6.23: Signals at different nodes of the circuit of Fig. 6.5 (dc quantities are eliminated) (a) TR-UWB signal at node 'RF+' (b) delayed TR-UWB signal at node 'LO+' (c) distorted signal at node 'N+' (d) distorted signal at node 'P+' (e) multiplied signal at node 'IF+' (no filtering)

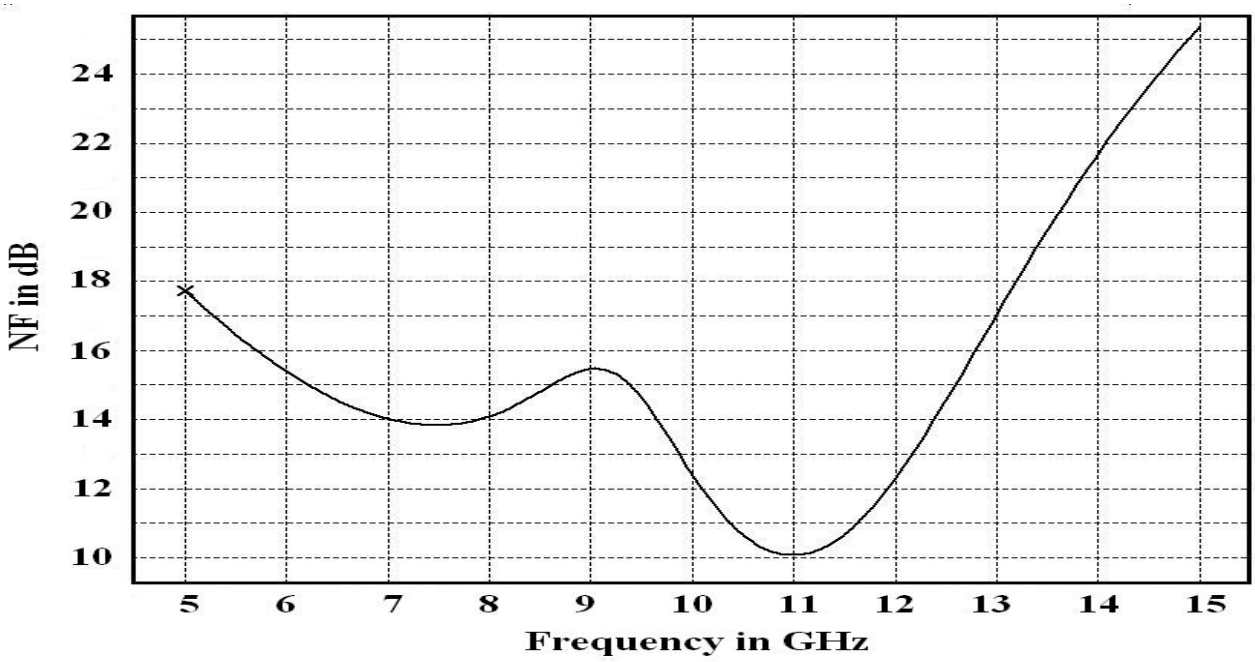

Figure 6.24: Noise figure of the receiver front end versus frequency

6.2.6 Noise Issues of the Receiver Front-End

Noise figure of the receiver front end is plotted in Fig. 6.24 with frequency. It is not less than 10 dB now, whereas the minimum was 7.8 dB in previous chapter. NF increased because of the internal resistances of the couple of additional inductors between the supply rails of the first stage. Noise issues of such wideband circuits are discussed in [91-92]. However, like the circuits of earlier chapters, no noise minimization techniques were adopted.

Coming to this point, now this is the time to employ this receiver circuit to detect the UWB pulse stream of Fig. 6.3. Next sections will demonstrate the performance of this circuit in time domain.

6.3 Detection of TR-UWB Pulse Stream by this Receiver Front-End

The ideal receiver front-end of Fig. 6.1 was replaced by the circuit designed in this chapter and the signals of Fig. 6.2 were reproduced by this new system. But here it recovered 2 gbps digital bit streams those can be found in Fig.6.25. Indubitably, the receiver front end performed well in the detection process, since the digital data was recovered successfully. Anyways, note that the delay element and the comparator were modeled as ideal in this simulation.

Now, although this system detected digital data successfully, but an ideal comparator was incorporated. In next chapter, it will be shown that, detection of such short duration pulses will be difficult for real high speed comparators. That is why, a new TR-UWB communication scheme will be proposed in next section to increase the signal energy for the real comparators.

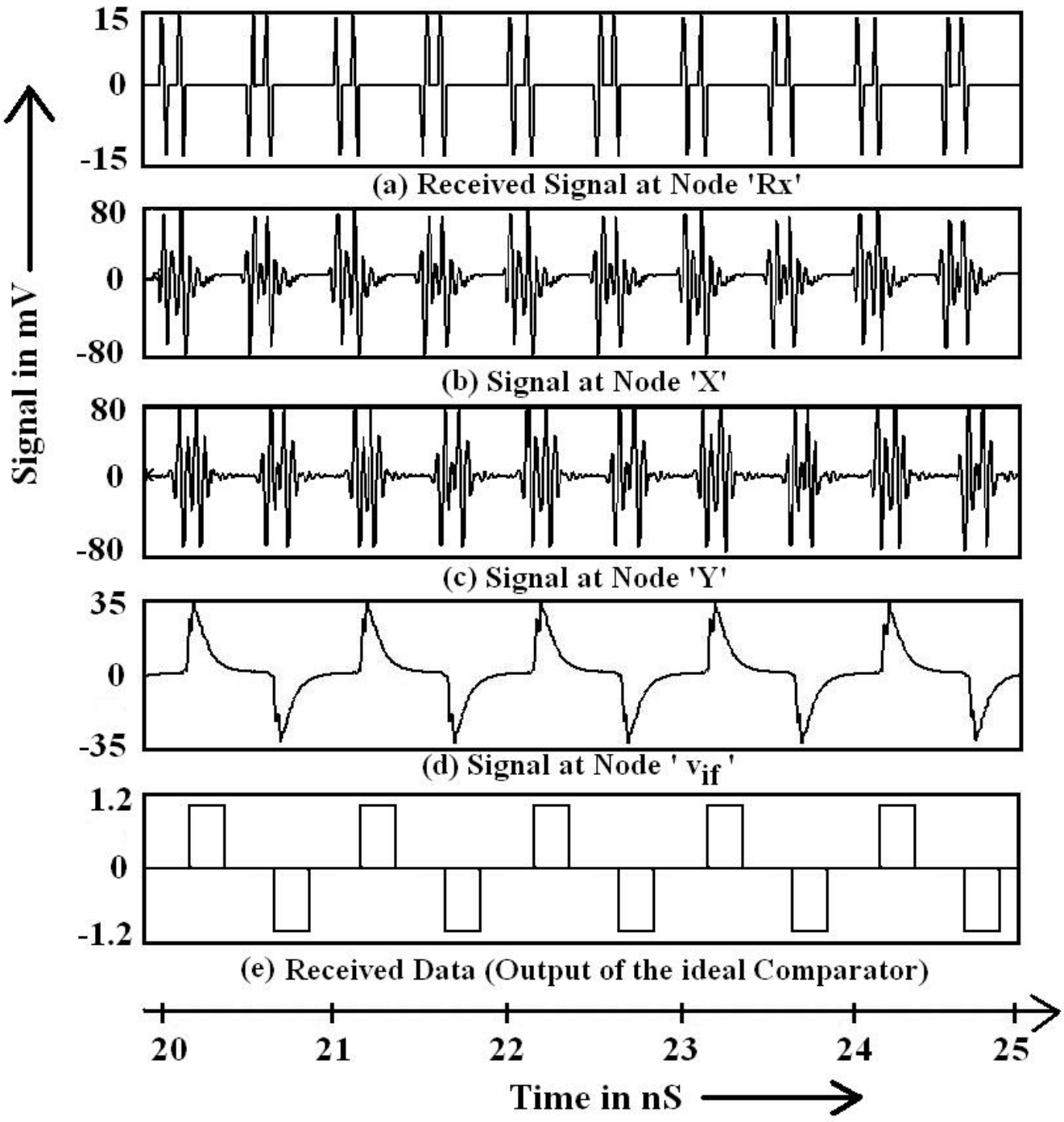

Figure 6.25: Signals at different nodes of the UWB receiver of Fig. 6.1 when detecting 2 gbps digital data with real receiver front-end of Fig. 6.5 employed

6.4 Modified TR-UWB Communication Scheme

To increase the signal strength for real comparators, the new proposal is to use three consecutive pulses for each digital bit instead of two, where only the middle one will be the reference pulse. This reference pulse will be in phase or out of phase with other couple of information pulses for '1' and '0' respectively. The transmitted pulse stream is shown in Fig. 6.26. Its frequency constituents, shown in Fig. 6.27, assure that it can be

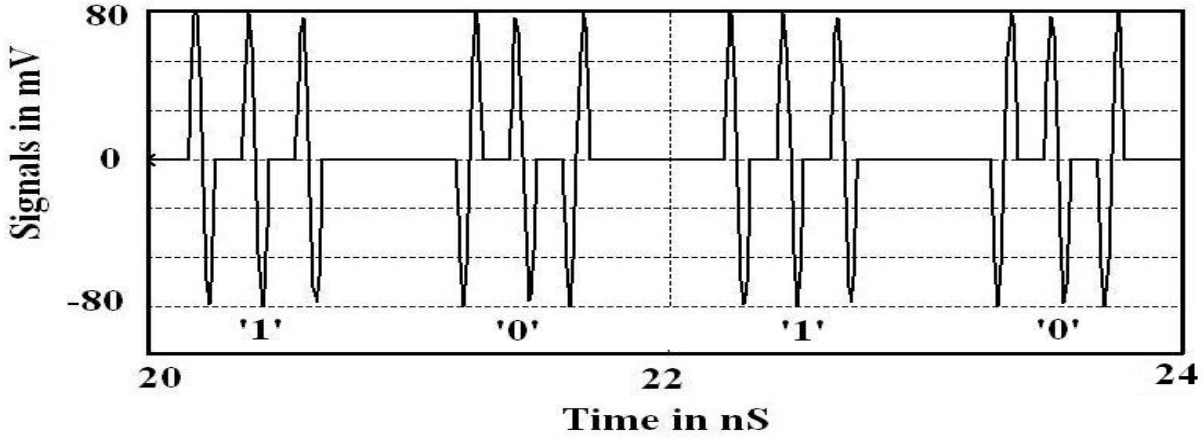

Figure 6.26: Proposed three pulse TR-UWB signal for on-chip wireless interconnect

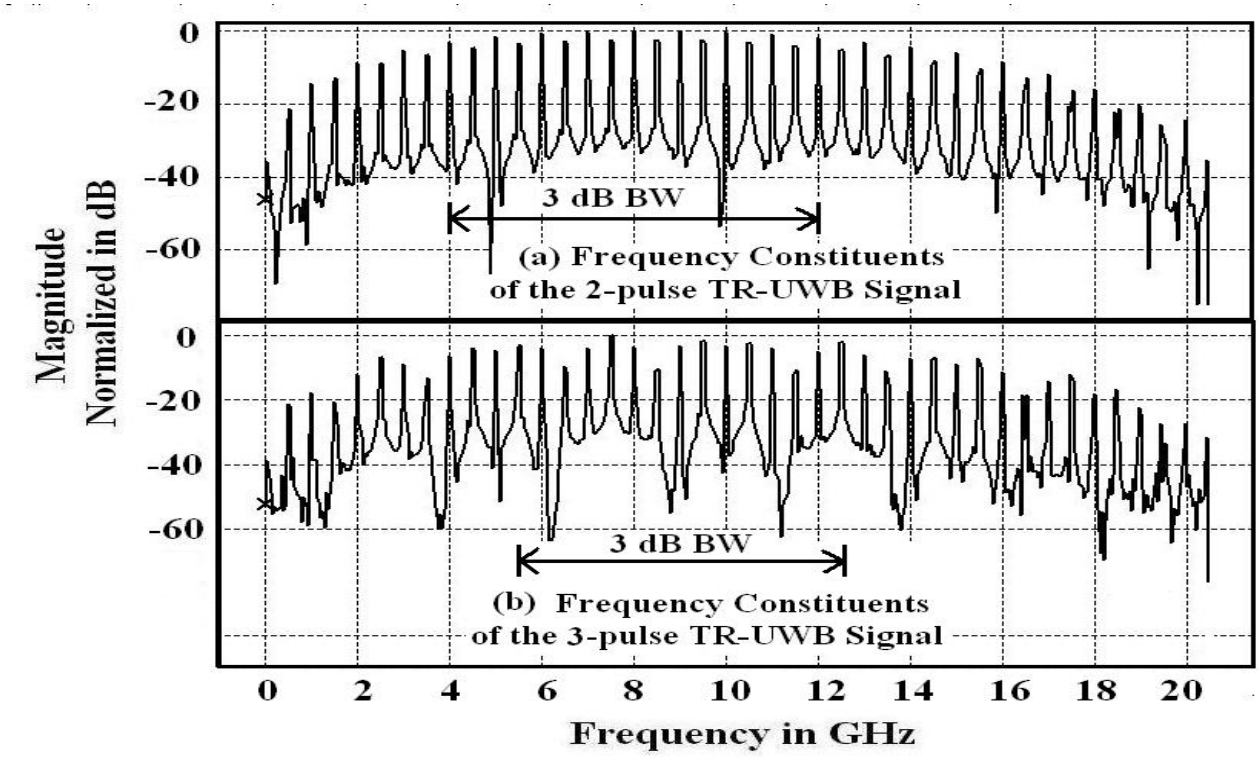

Figure 6.27: Frequency components of the 2-pulse and 3-pulse TR-UWB signal

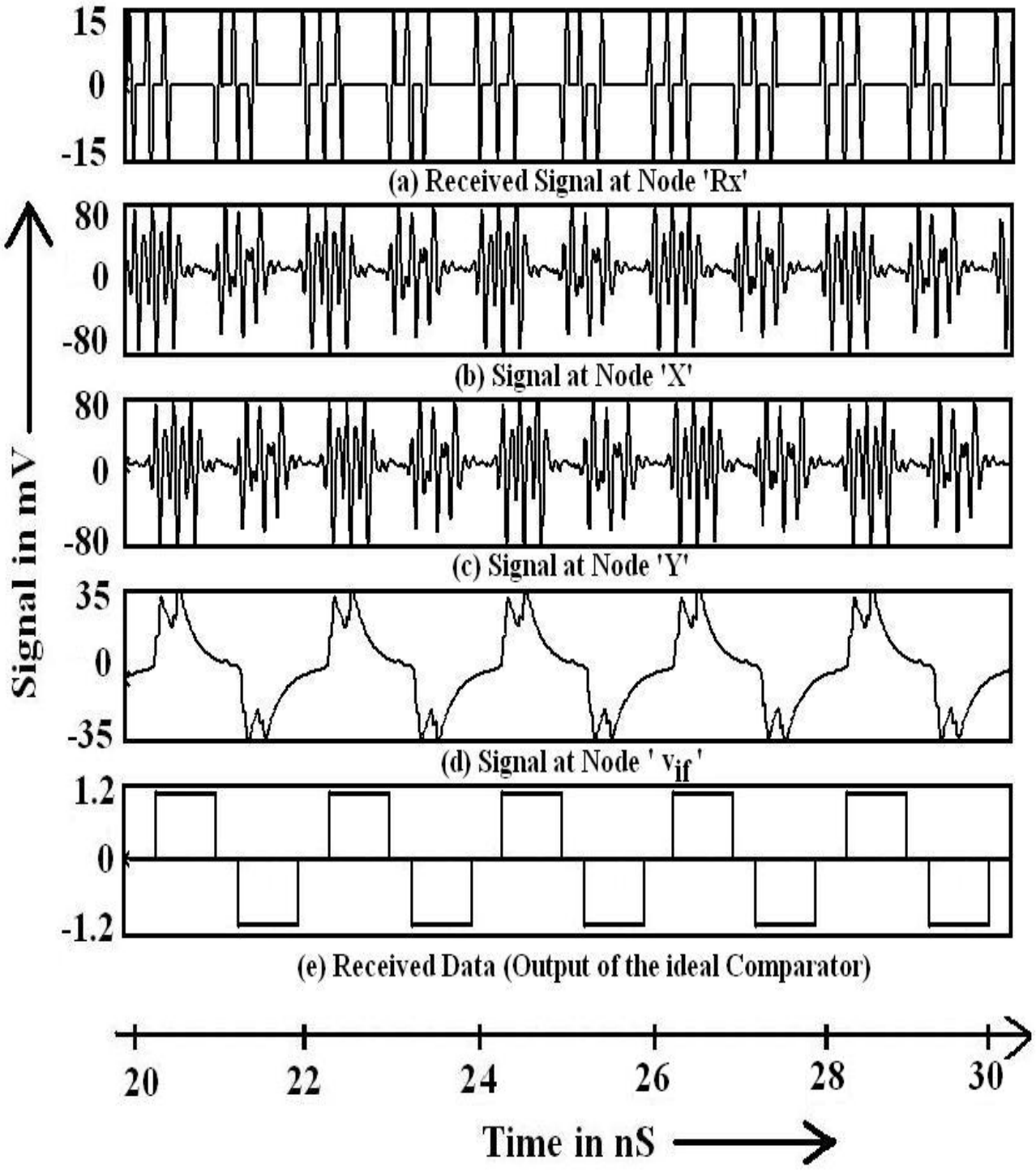

Figure 6.28: Detection of the 1 gbps digital data using 3-pulse TR-UWB transmission scheme

handled conveniently by the receiver front end of this work without any change, because its frequency distribution is not much different than the two pulse counterpart.

This modified TR-UWB pulse stream was fed to the receiver of previous section at 1 gbps and corresponding signals are portrayed in Fig. 6.28. It is clear that, signal energy in v_{if} increased by approximately twice, so will be easier to detect by the following comparator. Of course, the maximum number of bits per second will decrease by approximately 33%, but it is for the limitation of the real high speed comparators, especially in modern sub-micron technologies. Another advantage of increased signal strength for the comparator will be lower minimum detectable power level for the receiver. It in turn will allow increasing the communication distance for same transmitted power level, or the transmitted power level could be decreased for the same communication distance.

This chapter modified the receiver front end of previous chapter to make it suitable for working with UWB signals. The circuit was optimized considering intricate practical issues. Then it was used to recover the digital data from TR-UWB pulse stream. Finally, a new TR-UWB communication scheme was proposed considering the limitation of real high speed comparators. The receiver front end performed satisfactorily with both types of signaling schemes.

To the best of our knowledge, a complete system for on-chip wireless interconnect is yet to be reported. There are a few works like [93-94], who discussed on the system with circuit blocks, but no transistor level design. On the other hand, there are some works like [95], which designed complicated transceiver circuit for wireless communication, but not for on-chip wireless interconnect. In that sense, the receiver front end designed in this work expects enough evaluation.

However, the delay element and the comparator of the receiver used in this chapter were modeled as ideal. A real delay element can be found in [96], but that is based on charging-discharging mechanism, so applicable only for large signal conditions i.e. for digital signals. Anyways, designing the delay element is beyond the scope of this work. But, let us investigate the design issues of high speed comparators of sub-micron technologies. Next chapter will discuss on the challenges of those circuits.

CHAPTER 7

DESIGN OF A HIGH SPEED COMPARATOR FOR THE RECEIVER

The delay circuit and the comparator of earlier chapters were modeled as ideal, it has already been mentioned. This chapter will discuss on designing high speed comparators and will evaluate the performance of the circuit. Designing such circuits in modern sub-micron technologies is a challenge because of their short channel effects. Especially, getting a very high gain is quite difficult due to the low output resistance of those transistors.

On the other hand, higher the gain of the comparator will be, lower will be the minimum detectable power level for the receiver. In other words, if the gain of the comparator is higher, then the receiver will be able to recover digital data correctly even if the signal received by the receiving antenna is weaker. Its advantage will be- increased allowable distance between the transmitter and receiver or lesser transmitted power. Besides, the comparator has to be fast enough so that, it can regenerate the high speed digital data. For example, it was mentioned in chapter 5 that, the receiver front end can work at maximum speed of 4 gbps. But, the overall speed of the receiver will not be so high if the comparator is slower. In this way, comparator plays an important role in governing the communication speed and distance of the whole transceiver system. After all these, this circuit should consume limited power and must not occupy excessive space. Therefore, there are a number of intricate design objectives for this part of the receiver.

This chapter opts for describing how the aforementioned design objectives were addressed in designing a high speed comparator for the receiver of UWB on-chip wireless interconnect system. The circuit will be employed in the receiver to regenerate the 2 gbps digital data of previous chapter. Finally the performance of the whole receiver will be evaluated to determine its maximum allowable speed and minimum detectable receiving

power level. Thus, a brief ideal about the capability of this receiver will be available at the end of this chapter.

7.1 Design of the Comparator

Comparators are nothing but high gain amplifiers. Gains of these amplifiers are so high that, even a small difference between its differential inputs is amplified enough for its output to reach its saturation limit. Higher the gain of the amplifier, better it will be as a comparator, whereas gains of ideal comparators are infinite.

In practice, highest possible gain from any amplifier stage is $|g_m r_o|$, where g_m is the trans-conductance of the driving transistor and r_o is its non-ideal small signal resistance. This gain is actually available from active loaded common source amplifier and it decreases if the current source is non-ideal. Such one is shown in Fig. 7.1, where the gain is $|g_m.(r_{o1} \| r_{o2})|$, r_{o1} and r_{o2} being the output resistance of transistor M1 and M2 respectively. So, for a given g_m, r_{o1} and r_{o2} are to be highest for the gain to be highest as well.

But designing a very high gain amplifier in modern sub-micron technologies is not very easy. This is because, r_o of those short channel devices are at best a few hundred ohms. Anyways, r_o can be increased by increasing the length of the devices, since $r_o \propto \frac{W}{L}$,

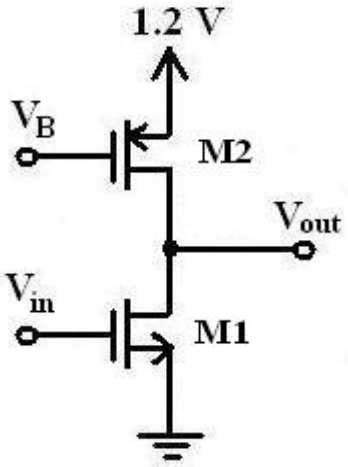

Figure 7.1: A real active loaded common source amplifier

where W is the width of the devices. But, it will have an effect on the trans-conductance of the driving transistor, as $g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})(1+\lambda V_{DS})$ where the symbols have their usual meaning. Moreover, V_{DS} also increases with L and its impact will not be insignificant for the λ of the short channel devices are pretty high. Anyways, L can not be increased indefinitely since its increased input capacitance will pose a risk of filtering high frequency signals at the input, pulling the gain down in those frequencies. In contrary, λ of long channel devices are very small, which makes their r_o very high as $r_o \propto \frac{1}{\lambda}$. So, secondary effects can be ignored all together in those technologies, whereas choosing a suitable aspect ratio involve much work when the technology shrinks.

I-V curves of both NMOS and PMOS transistors are plotted in Fig. 7.2, 7.3, 7.4 and 7.5 respectively for different gate to source voltages, V_{GS} and channel lengths, L. A few r_o are also mentioned there which increased with L as expected. Fig. 7.6 shows how r_o of NMOS and PMOS devices vary with channel length, where the width was 100 μm for both types of transistors.

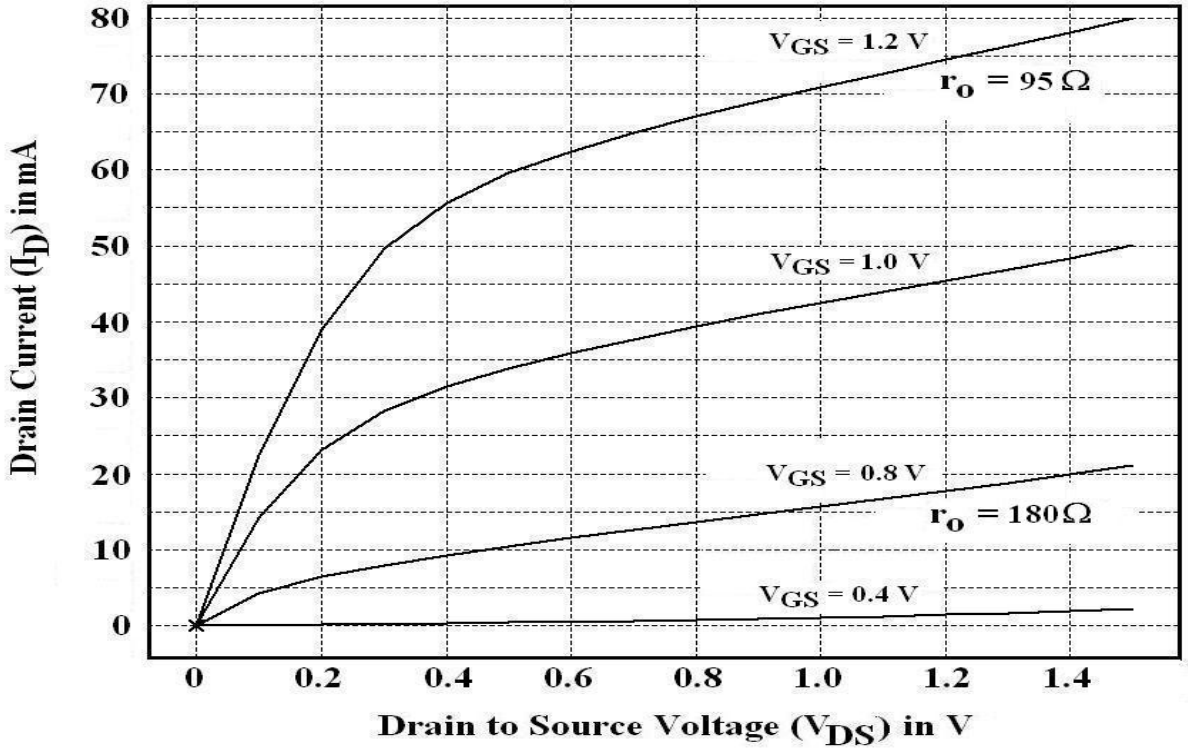

Figure 7.2: I-V curve of NMOS transistors with W=100 μm and L=100 nm

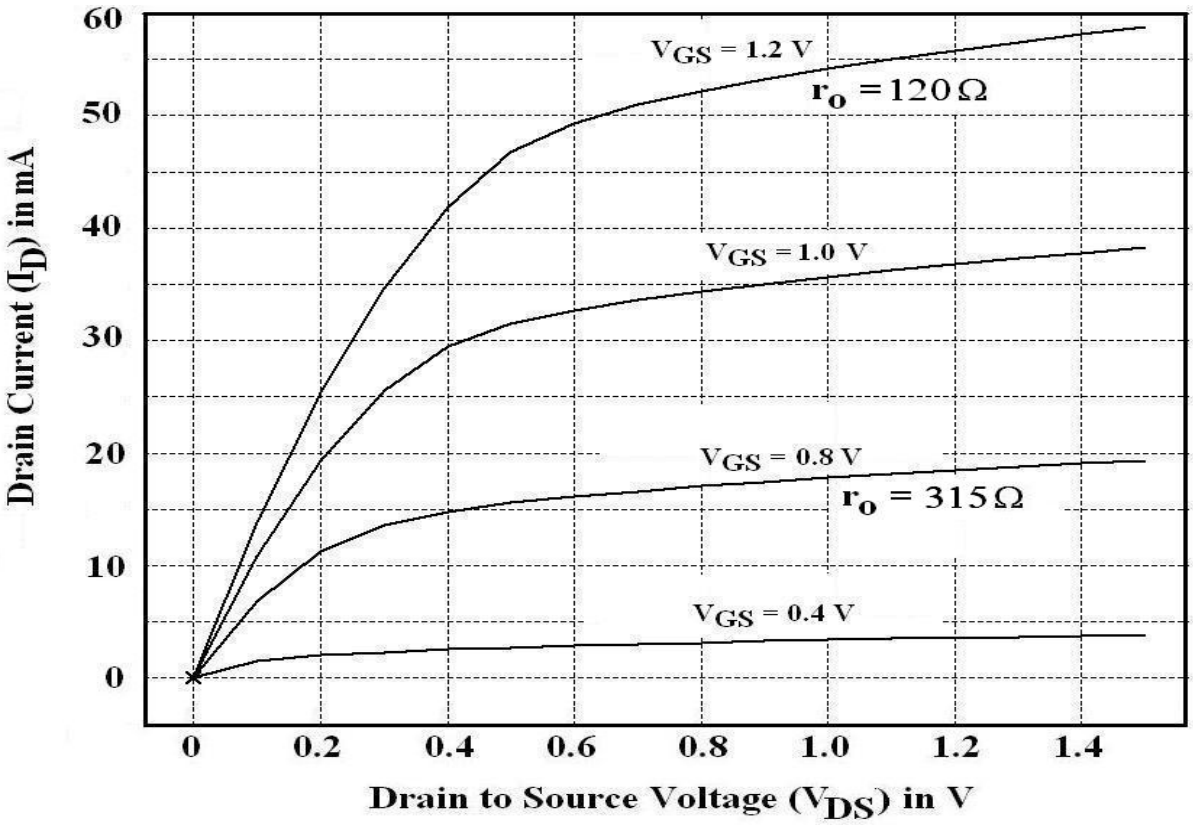

Figure 7.3: I-V curve of NMOS transistors with W=100 μm and L=200 nm

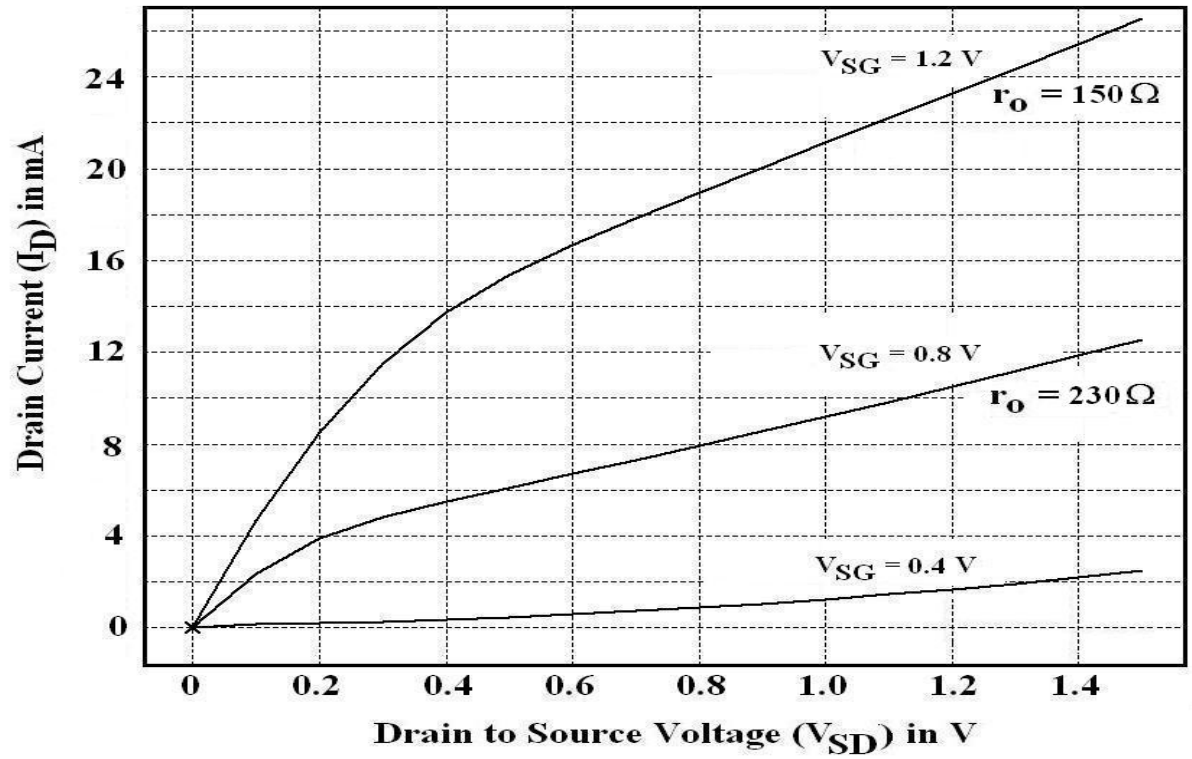

Figure 7.4: I-V curve of PMOS transistors with W=100 μm and L=100 nm

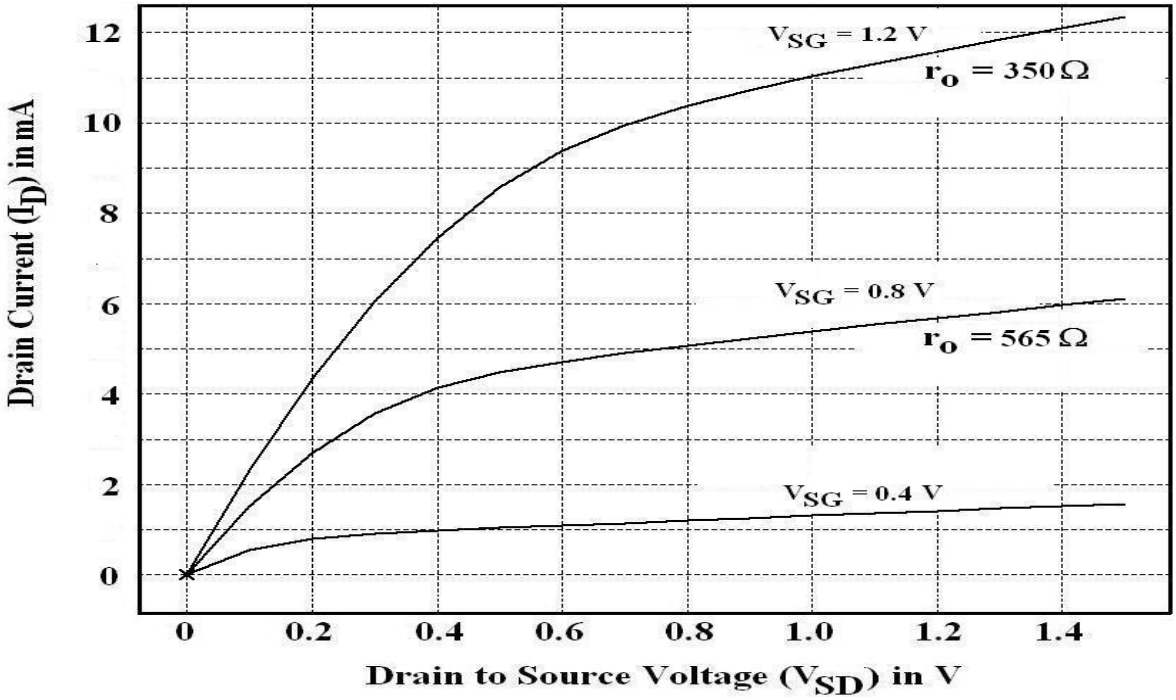

Figure 7.5: I-V curve of PMOS transistors with W=100 μm and L=200 nm

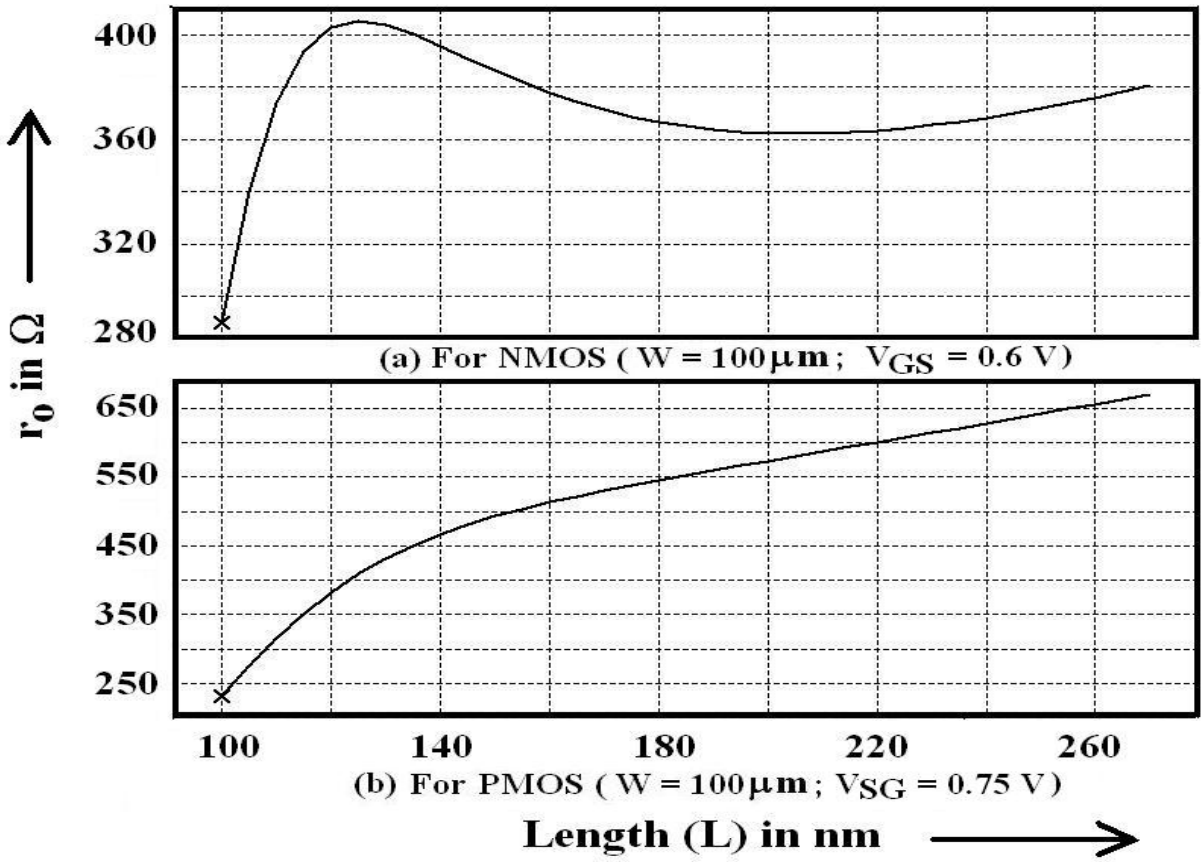

Figure 7.6: r_o of NMOS and PMOS transistors versus channel length

Now, to get an idea about the maximum gain that can be obtained in this IBM 90 nm CMOS technology, $|g_m r_o|$ of ideal current source loaded common source amplifier is plotted in Fig. 7.7 versus V_{DS} for channel lengths, L = 100 nm, 150 nm, 200 nm, 250 nm, 300 nm with W = 100 µm. The circuit which was used for this purpose is also drawn in Fig. 7.8. A negative feedback was used to maintain the desired drain to source voltage, V_{DS} that was varied. The op-amp of gain 200 V/V generated the required gate voltage, V_{GS} so as to keep the bias current constant, 4 mA in this simulation.

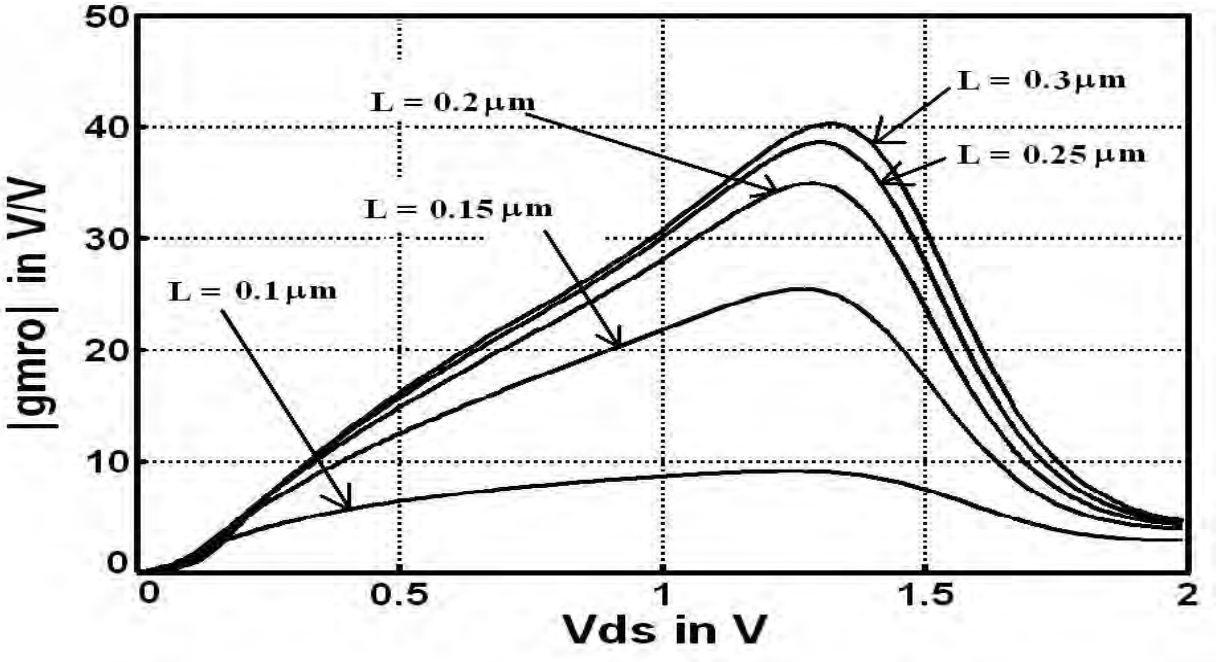

Figure 7.7: Gain of an ideal current source loaded common source amplifier for various L (W=100µm)

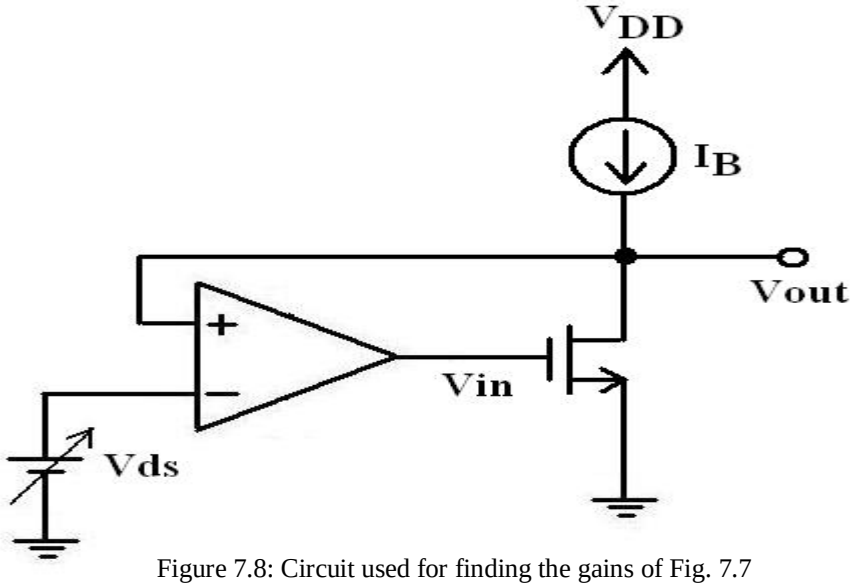

Figure 7.8: Circuit used for finding the gains of Fig. 7.7

4 mA bias current was not arbitrarily chosen. Although, the gain efficiency, $|g_m r_o|/I_d$ was found increasing significantly with decreasing I_d, but it could not be minimized further because the dc gate voltage of the comparator will be governed by the dc voltage at the output of the receiver front end of chapter 6 and it was 0.6 V. So, the width of the driving transistor is to be decreased if the bias current is to minimize. But, Fig. 7.9 shows another contradicting issue, where $|g_m r_o|$ decreases with decreasing width. That is why; too low a width will not be able to give a good gain. In Fig. 7.7, width was chosen as 100 µm, as increasing it further did not increase gain too much in Fig. 7.9. Similarly, gain of Fig. 7.7 increases less after L=200 nm. Also, input capacitance increases if anyone or both of L and W increases. So, all these constraints prevailing, optimum aspect ratio and the resulting bias current for the driving NMOS transistor are W/L=100 µm/0.2 µm and 4 mA respectively. The maximum gain ($|g_m r_o|$) of corresponding common source amplifier is expected to be 14 V/V (22.9 dB) from Fig. 7.7.

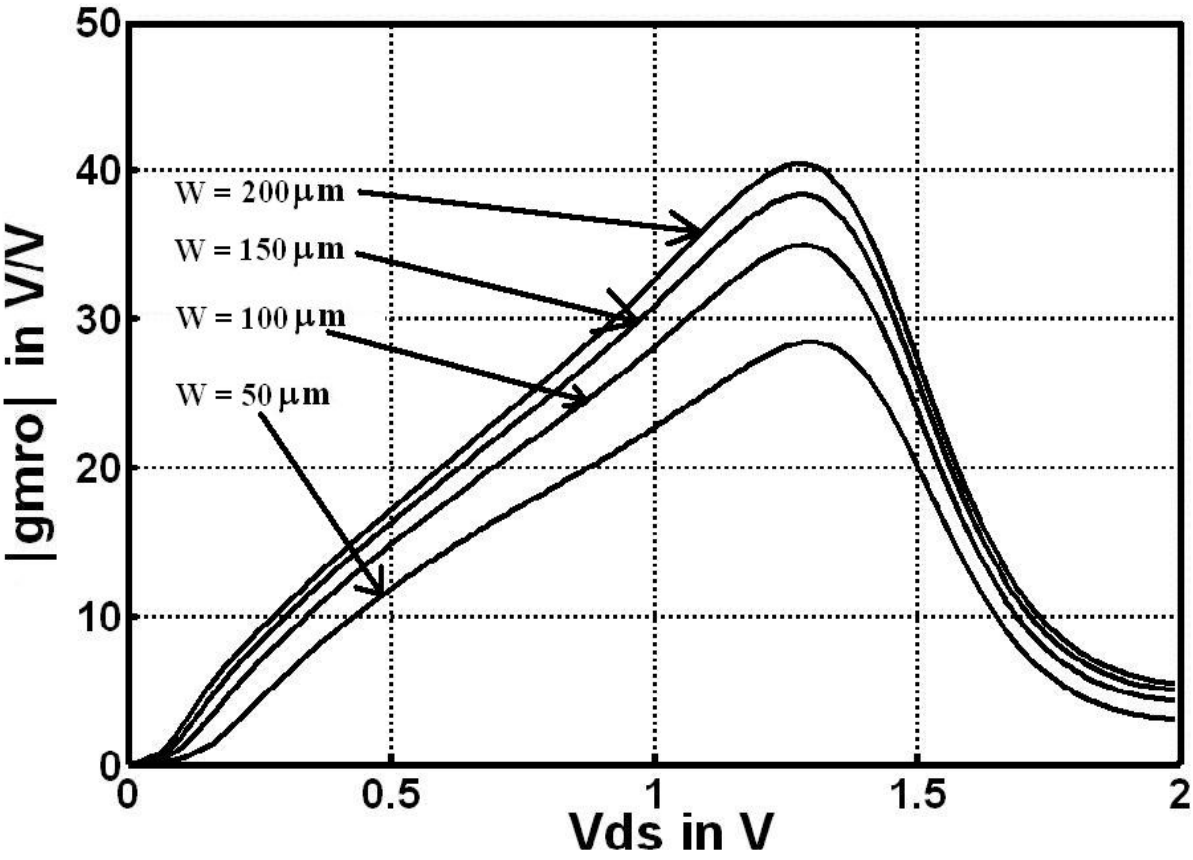

Figure 7.9: Gain of the ideal current source loaded common source amplifier for various W (L=0.2 µm)

Next, the common source amplifier of Fig. 7.1 was designed with the aspect ratio of the PMOS transistor as W/L=100µm/0.25µm. The resulting transfer curve can be found in Fig. 7.10. Gain of the amplifier was calculated by finding the slope of the curve in the transition region and it is $\frac{\Delta Vout}{\Delta Vin}$ = 9.2 V/V (19.3 dB), much less than the maximum possible gain of 14 V/V, as expected earlier. To investigate further, corresponding r_o of NMOS and PMOS transistors can be read from Fig. 7.6 as 360 Ω and 640 Ω respectively. Trans-conductance of the driving transistor can be calculated as $|g_m r_o|/r_o$ = 39 mA/V and the gain would be $|g_m.(r_{o1} || r_{o2})|$ = 9 V/V (19.1 dB), pretty close to the simulated value of Fig. 7.10.

Another observation of Fig. 7.10 is- its transition is not exactly at Vin = 0.6 V, that would be optimum for getting maximum output swing with the power supply being 1.2 V. The reason is, r_o of the PMOS transistor is much higher than that of the NMOS transistor. To justify this argument, aspect ratio of the PMOS transistor was increased to get r_o = 380 Ω, close to that of the NMOS transistor (360 Ω) and the resulting shift in transfer

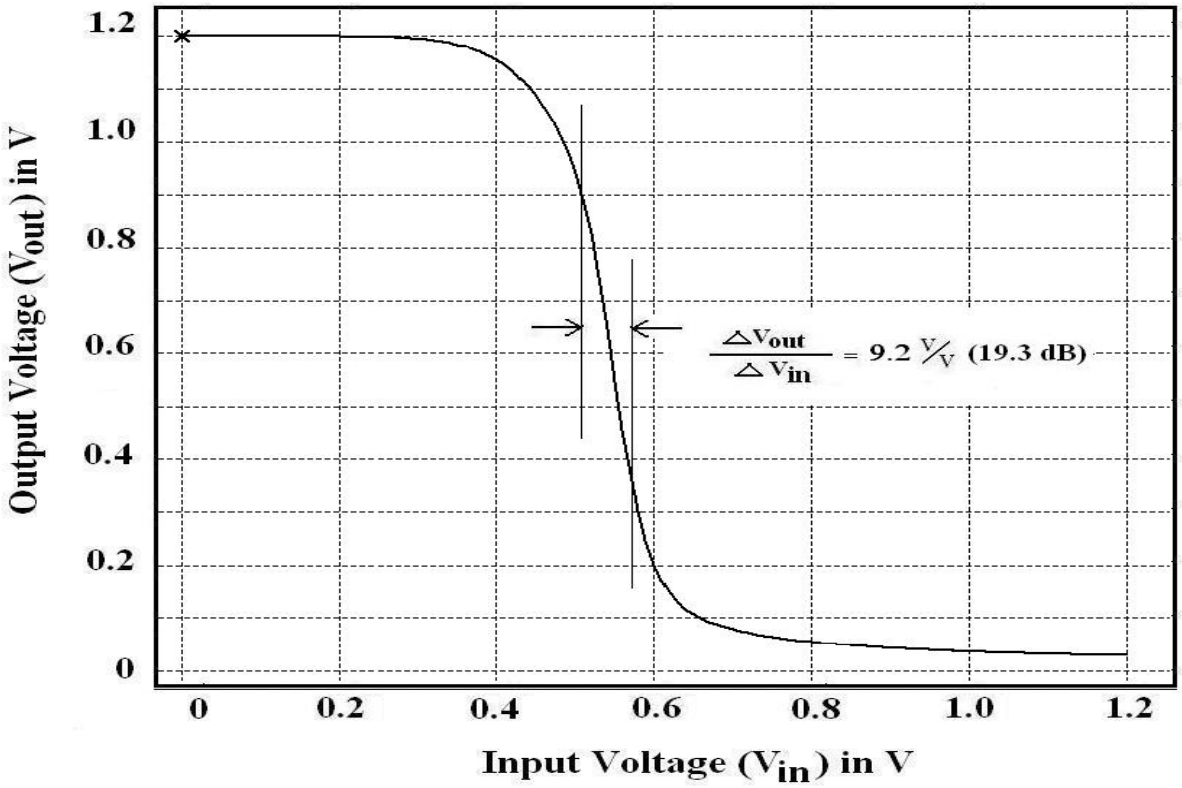

Figure 7.10: Transfer curve of the active loaded common source amplifier of Fig. 7.1

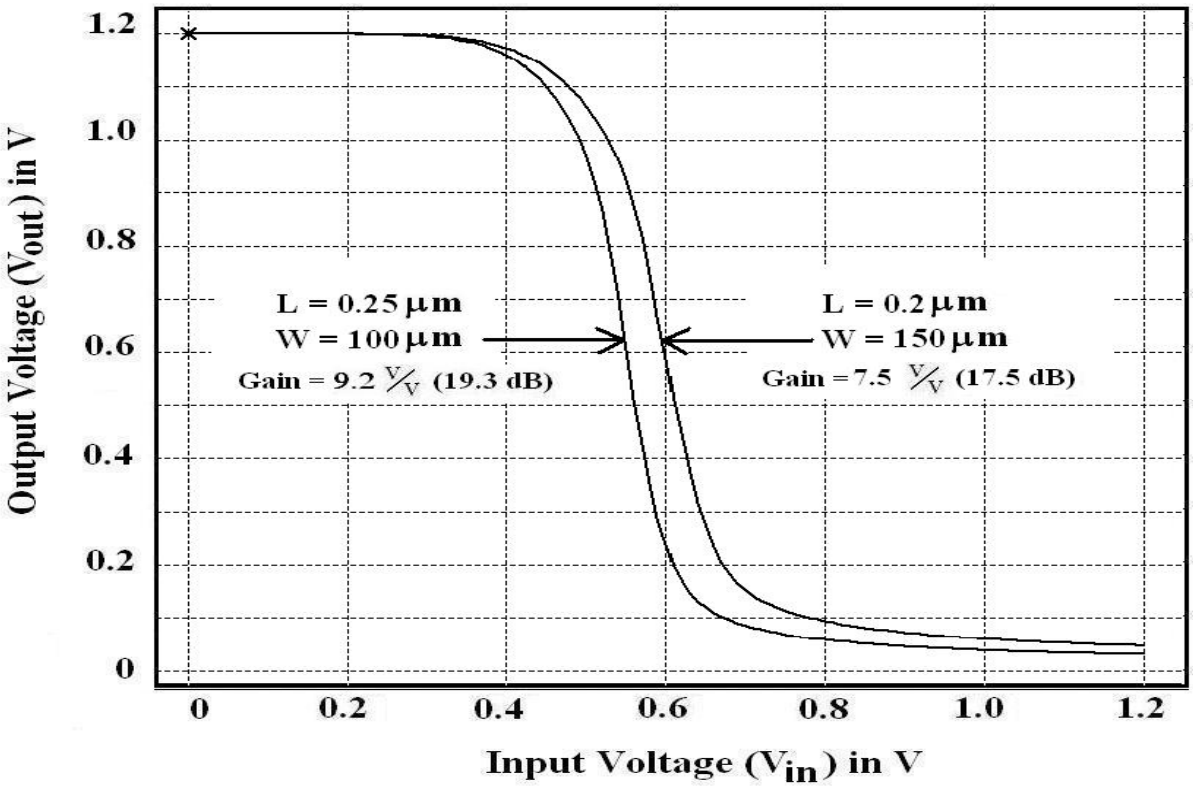

Figure 7.11: Transfer curve of the common source amplifier of Fig. 7.1 for two different sizes of the active load

curve can be seen in Fig. 7.11, where in later case the transition is exactly at Vin = 0.6 V. But, the gain dropped to 7.5 V/V (17.5 dB) due to the decreased output resistance, r_o of the PMOS load. It means optimum aspect ratios are to be chosen carefully depending on applications.

By the way, a similar analysis was carried on in MIC 1.2 µm CMOS technology and the gain was found as 52 V/V (34.3 dB) with r_o in around 10 kΩ for NMOS devices and with a bias current of 25 µA. So, both the gain and gain efficiency of this IBM 90 nm technology is comparatively very low.

Anyways, there are a lot of comparator architectures proposed in literature for sub-micron technologies [97-102]. But a simple one was designed in this work. It is the popular two stage differential to single ended op-amp, but followed by a CMOS inverter. The

schematic diagram is portrayed in Fig. 7.12. Gains of all three individual stages are shown in Fig. 7.13, where the first stage is a non-inverting stage and the following two are inverting. Total gains of those stages are also available in Fig. 7.14. Note that, overall gain of the comparator is the gain after all three stages and it is 685 V/V (56.7 dB) as mentioned in Fig. 7.14(c). Again, a similar kind of two stage comparator was designed in MIC 1.2 µm CMOS technology excluding the third stage of this design and the overall gain was 3700 V/V (71.4 dB). This huge difference speaks for the technological constraints in designing such high gain amplifiers in this CMOS process, as argued earlier this section.

Note that, none of the driving transistors of Fig. 7.12 were biased externally. DC voltages of the output of previous stages biased them well. Again, though the third stage is a CMOS inverter, but it works as an amplifier stage in this circuit. In fact, inverters and amplifiers are not much different structurally. They work both as inverter or amplifier when are fed with large and small signals respectively. Of course biasing issues are involved. In this situation, the output of the comparator has to generate a large signal which will swing rail to rail and its input is also a large signal (V_{out2}). A CMOS inverter works best in this condition, triggering to anyone of its supply rail whenever there is a significant change in its input i.e. large signal input. This technique actually borrows the concept of so-called sense amplifier of digital memory blocks.

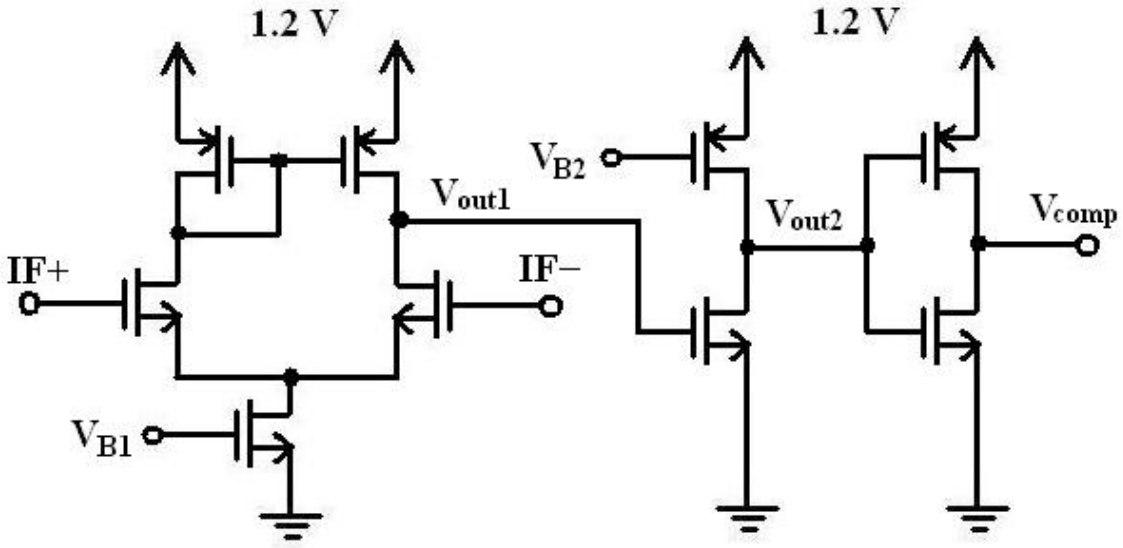

Figure 7.12: Schematic diagram of the three stage comparator

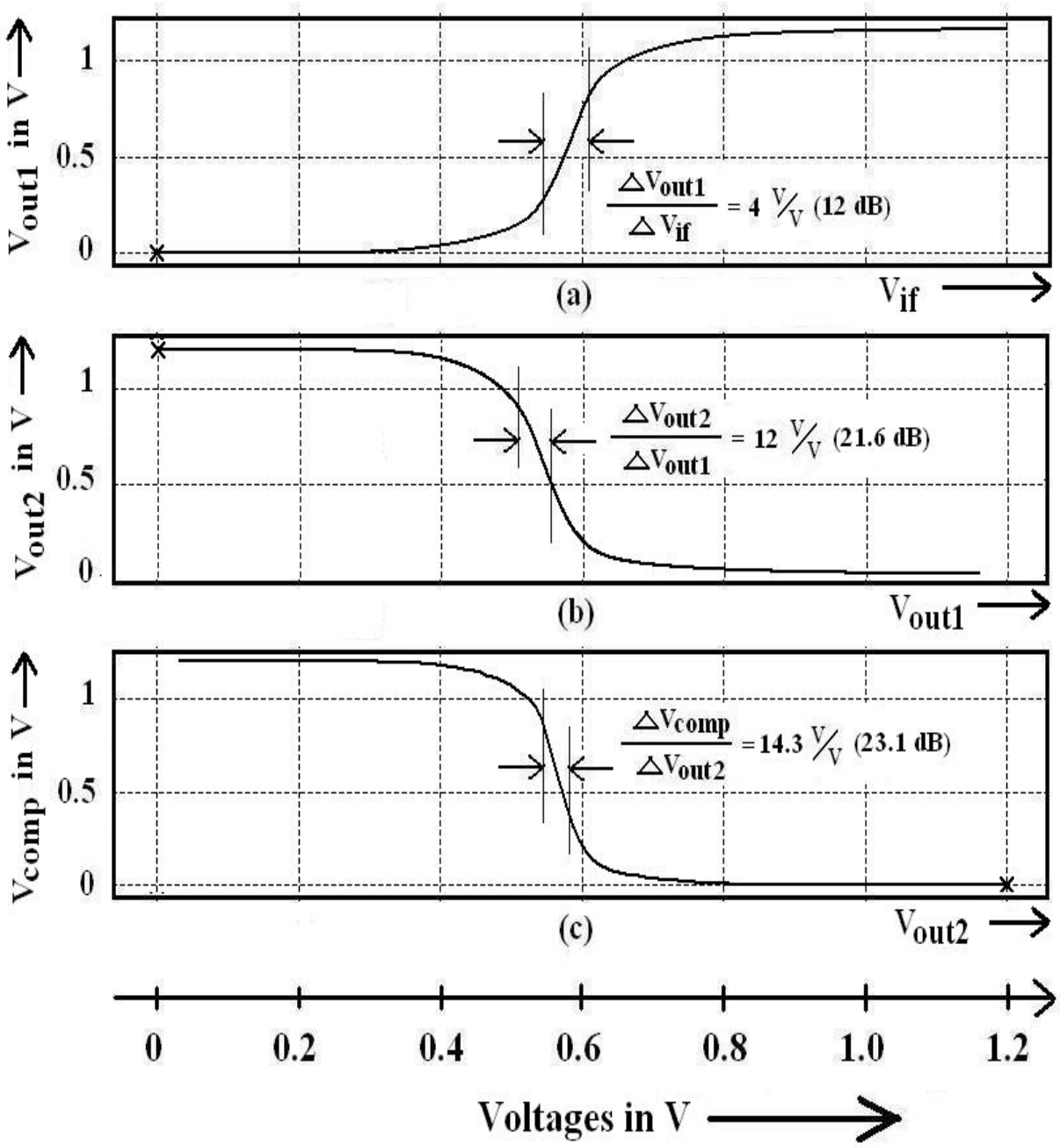

Figure 7.13: Transfer curves of all three individual stages of the comparator of Fig. 7.12

(a) Vout1 versus Vif = IF+ - IF- (b) Vout2 versus Vout1 (c) Vcomp versus Vout2

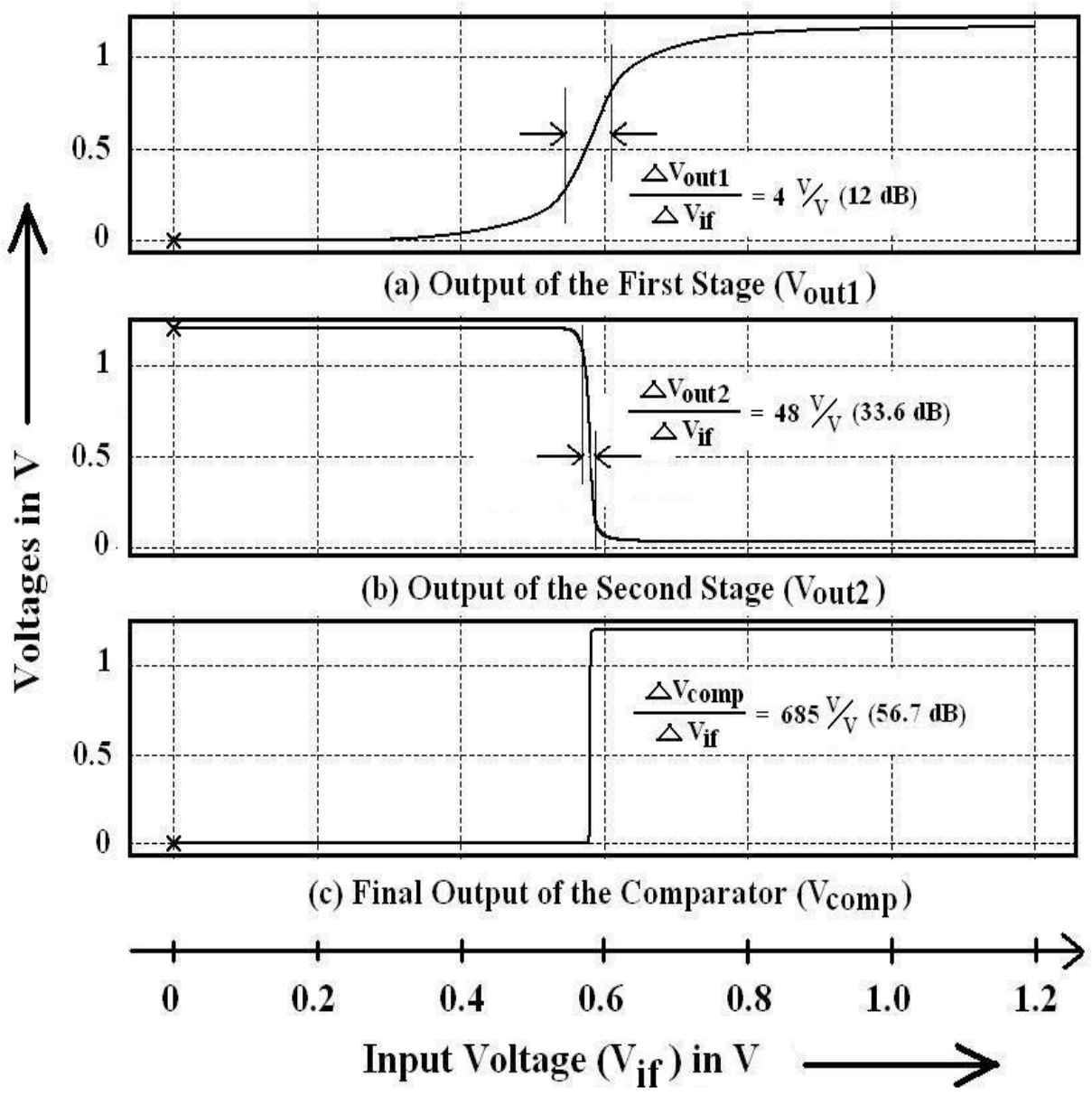

Figure 7.14: Overall transfer curves of all stages of the comparator of Fig. 7.12 (Vif = IF+ - IF-)

(a) Vout1 versus Vif (b) Vout2 versus Vif

(c) Vcomp versus Vif (transfer curve of the whole comparator)

This comparator was employed in threshold detection and the results can be found in Fig. 7.15, where it satisfactorily detected the threshold voltages of 0.6 V and 0.7 V. Also its offset was found as 51.4 μV using the circuit of Fig. 7.16. The effect of this offset is tampered threshold level when working as threshold detector. Offset cancellation techniques are available in literature [103-107], but since, the comparison is not to be very precise in this digital application, so those techniques were not tried here. Anyways, this circuit consumes 13.7 mW power from 1.2 V power supply.

Next sections will investigate the performance of this comparator in detecting high speed digital data for the on-chip wireless interconnect system using TR-UWB pulse stream.

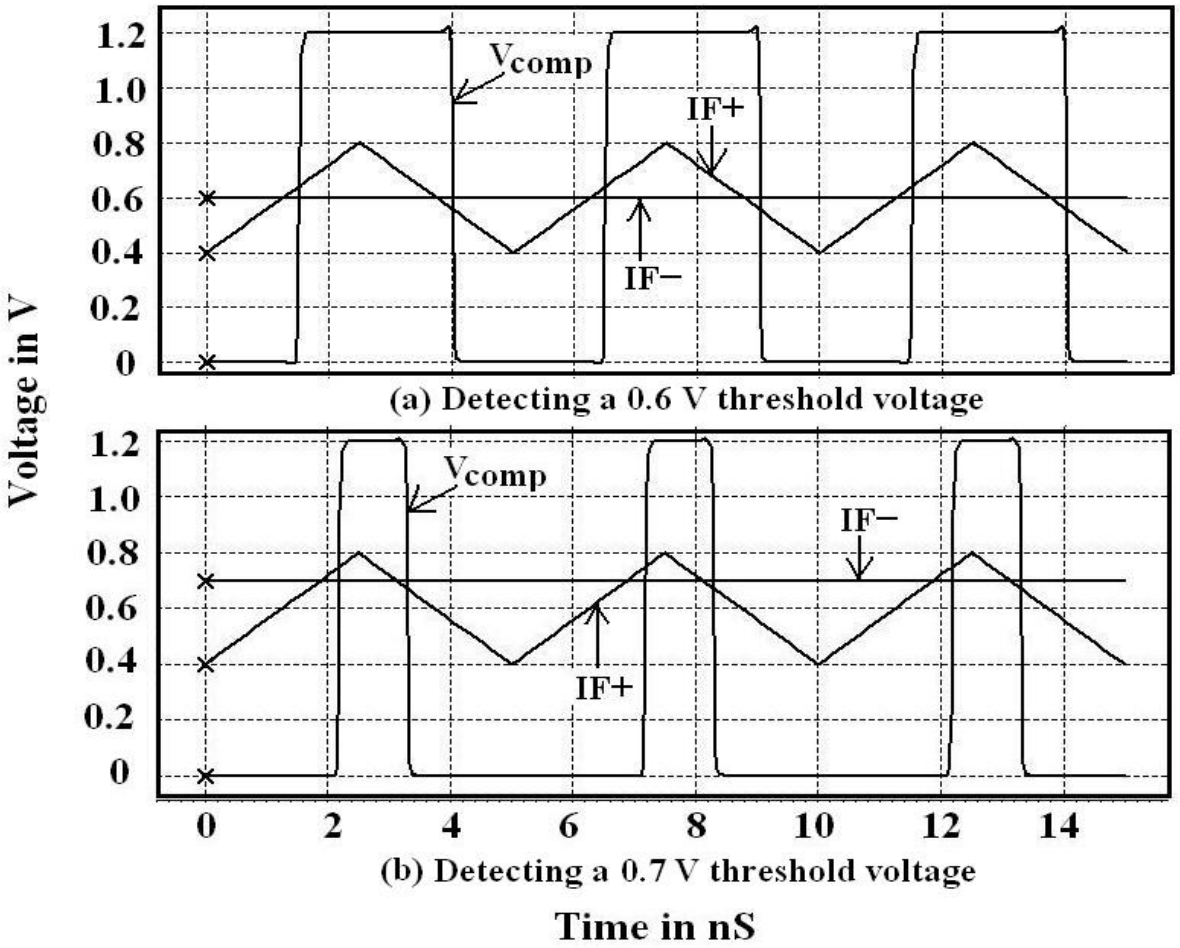

Figure 7.15: Performance of the comparator as a threshold detector

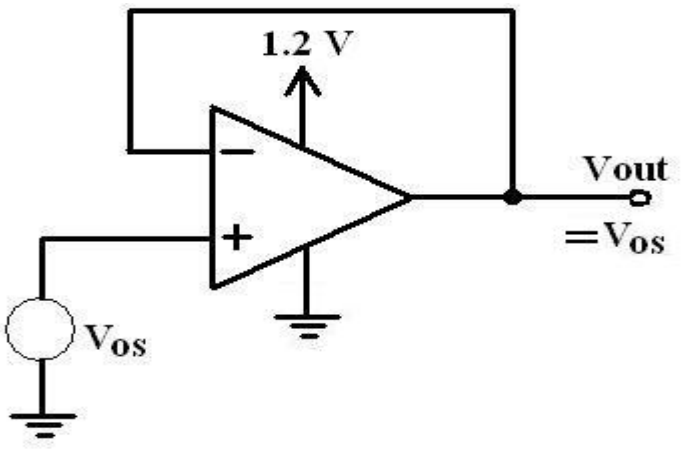

Figure 7.16: Circuit used for finding offset voltage (Vos = offset voltage)

7.2 Detection of High Speed Digital Data

To evaluate the commitment of this comparator, its performance in regenerating the transmitted digital data will be investigated, given the output of the receiver front end of previous chapter, v_{if} as its input. But, unfortunately the simulator could not simulate the receiver as a whole. That is why, both 3-pulse and 2-pulse versions of v_{if} were modeled for this comparator. The corresponding responses of this circuit can be found in Fig. 7.17 and 7.18 respectively, where output of all the three stages were included to demonstrate the gradual improvement of the signal. Transmitted data are also shown in those figures for convenience. Although, signal delay is clearly visible between the transmitted and received bit streams, but the detection process was indubitably successful. Note that, v_{if} of Fig. 7.17(a) and Fig. 7.18(a) are the 1 gbps and 2 gbps signals of Fig. 6.28(d) and Fig. 6.25(d) respectively.

However, next section will scrutinize this circuit more objectively so as to identify its constraints and performance limits.

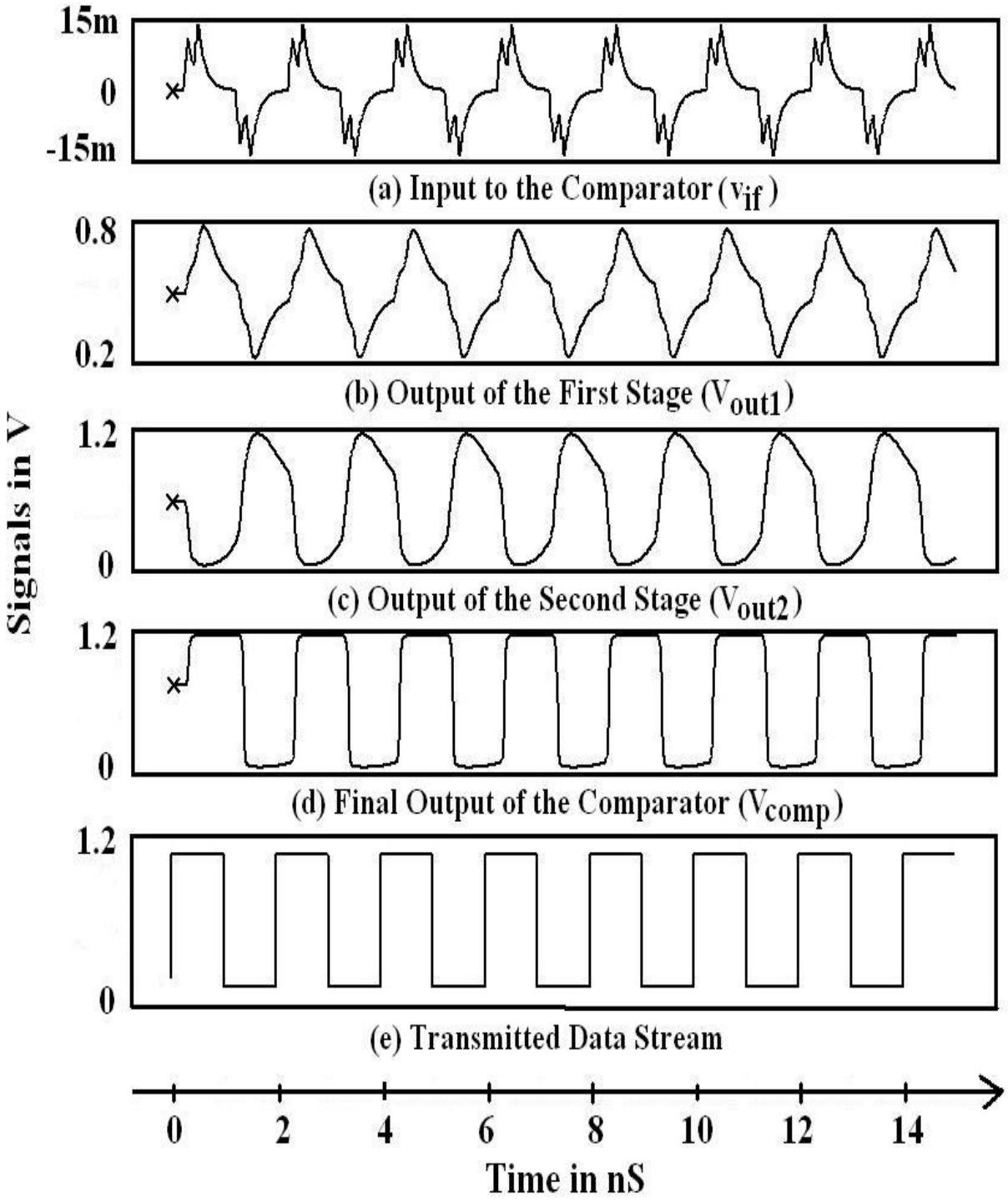

Figure 7.17: Regeneration of 1 gbps digital data in 3-pulse TR-UWB transmission scheme

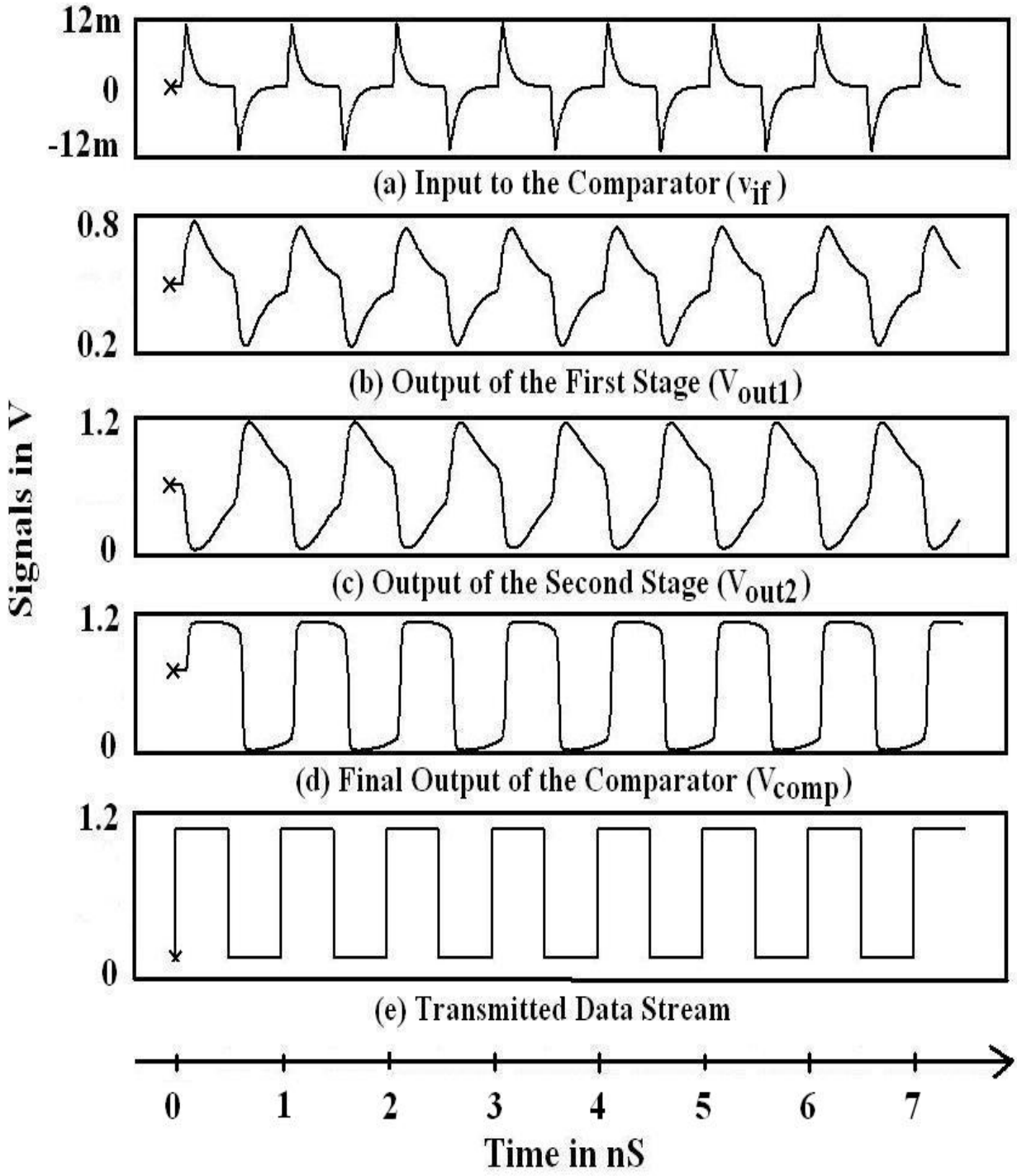

Figure 7.18: Regeneration of 2 gbps digital data in 2-pulse TR-UWB transmission scheme

7.3 Commitments of this Comparator

Commitments of this comparator will be determined in terms of maximum speed and the minimum input power level at which it can work satisfactorily. At first, zoomed version of the V_{comp} of Fig. 7.18(d) is shown in Fig. 7.19, where the rise time and fall time were found as 0.22 ns and 0.2 ns respectively. With this constraint, the maximum speed at which this circuit can work is (1/0.22) GHz or approximately 4.5 GHz.

So, in this system, the speed limit will not be imposed by the comparator. For instance, since the pulse width is 0.1 ns, so minimum bit duration for 3-pulse signaling is 0.1 X 3 (for 3 pulses) + 0.1 X 3 (for 3 inter-pulse pauses) = 0.6 ns. So the data speed can not be more than (1/0.6) = 1.67 gbps. Similarly, for 2-pulse signaling, the minimum bit duration is 0.1 X 4 = 0.4 ns and it sets the maximum speed limit to (1/0.4) = 2.5 gbps. As

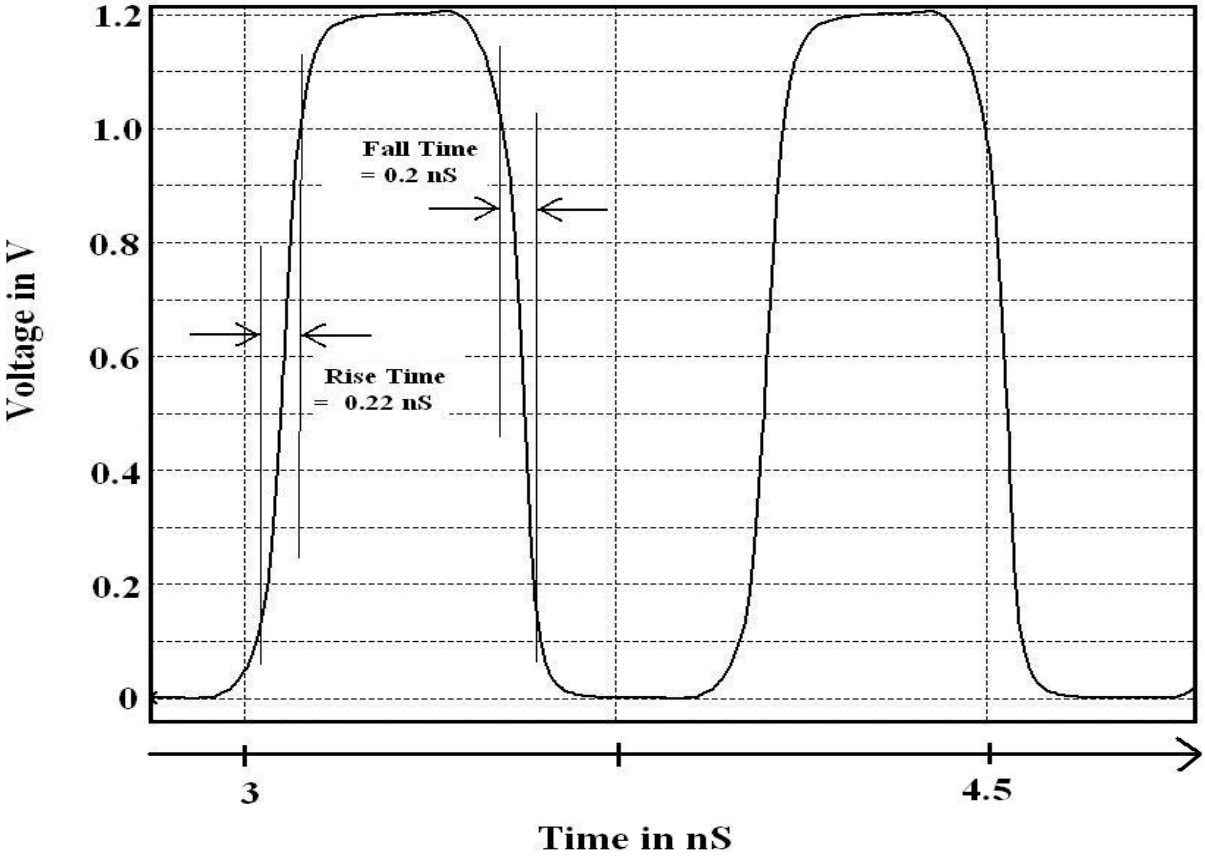

Figure 7.19: Finding maximum operating speed of the comparator

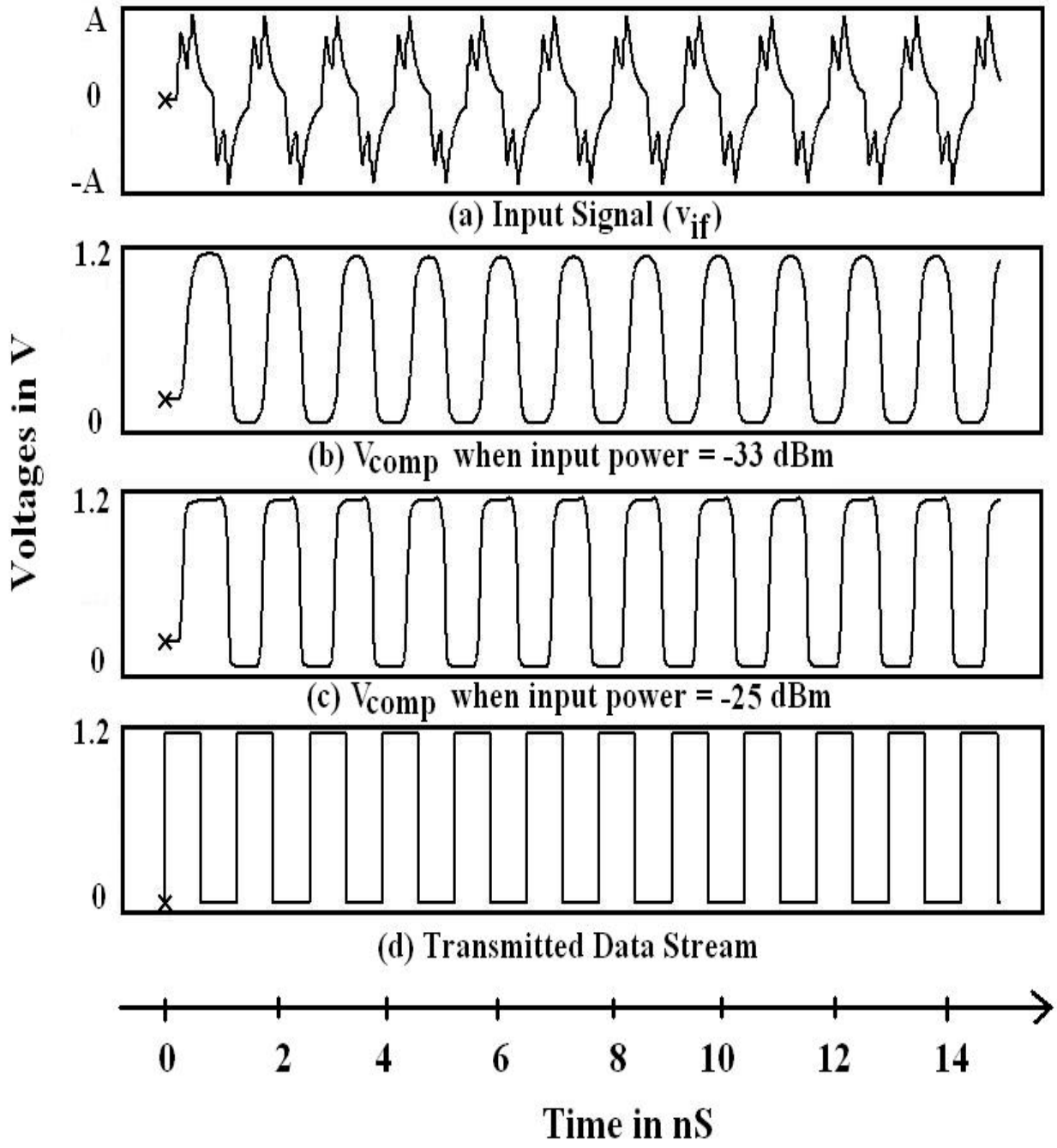

Figure 7.20: Finding minimum detectable received power level for 3-pulse signaling at the maximum data speed of 1.5 gbps

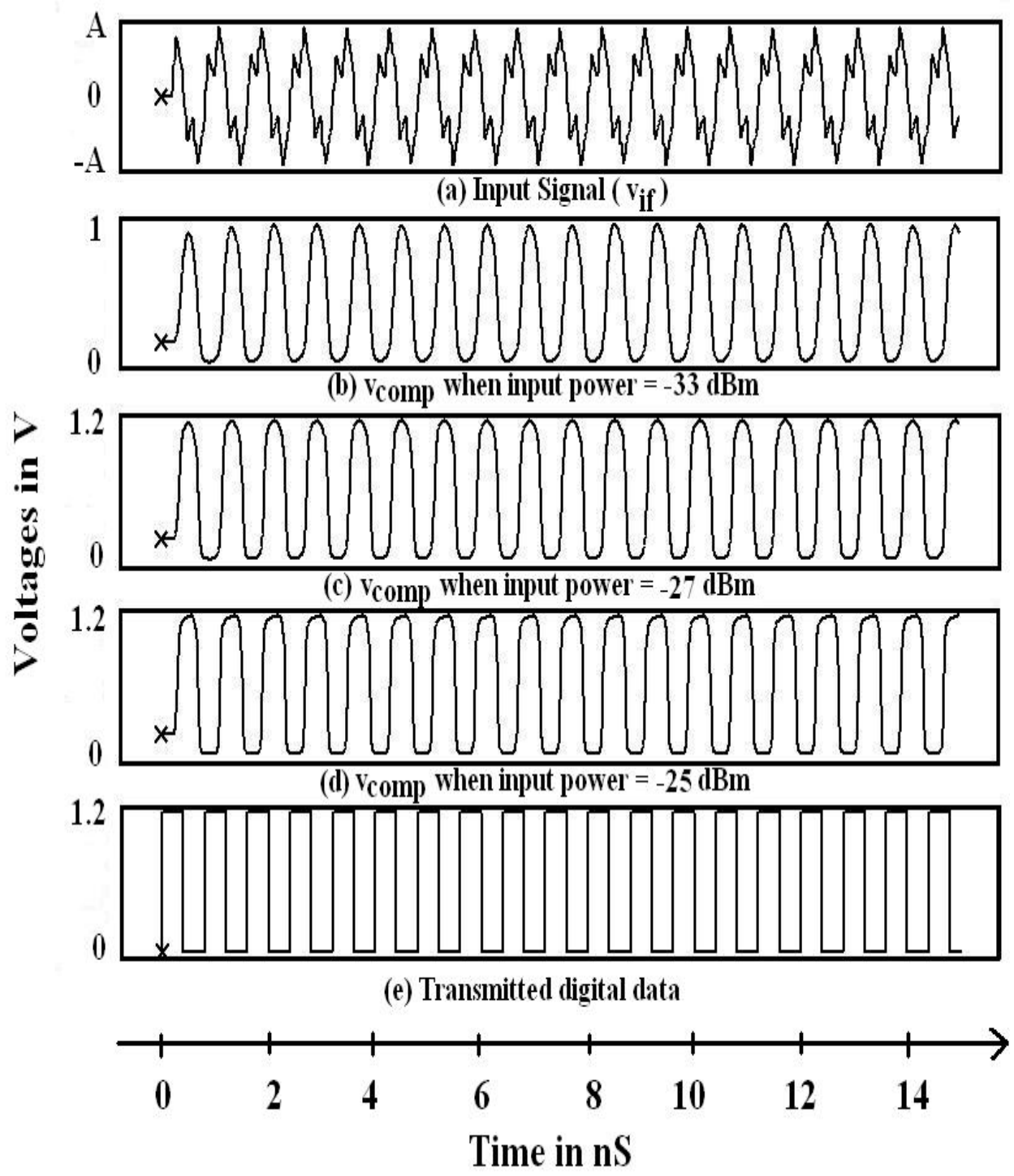

Figure 7.21: Finding minimum detectable received power level for 2-pulse signaling at the maximum data speed of 2.5 gbps

both of these limits are less than the maximum speed of the comparator i.e. 4.5 gbps, so maximum communication speed of this system is in fact governed by the communication scheme.

Now, to find the minimum input power of the receiver at which the comparator can work barely fine, the input power level at the receiving antenna were varied with maximum allowable data speed to identify the worse case scenario and the output of the comparator was found not reaching its rails for input power levels less than -33dBm (~10 mV) and -27 dBm (~20 mV) for 3-pulse and 2-pulse signaling respectively. These responses can be found in Fig. 7.20(b) and Fig. 7.21(c) in respective order. Fig. 7.20 and Fig. 7.21 also show the responses for a few other power levels for convenience. Note Fig. 7.21(b), where -33 dBm received power level could not make the output reach its rails for 2-pulse signaling. Actually, 3-pulse version performs better in terms of power limit because of its increased signal strength, as argued in previous chapter. But the communication speed has to be traded off. So, this scheme can be preferred in situations when circuit modules have to communicate over long distance or the transmitter has a low output power limit.

Anyways, allowable power limit decreases when signal speed degrades. In fact, it is not much hard to realize that, with 685 V/V gain, minimum differential input signal to the comparator can be as low as 1.2/685 = 1.75 mV for its output to barely reach its 1.2 V rail. Then the corresponding input to the receiver front end will be 1.75/5.7 = 0.31 mV (-63 dBm), where 5.7 V/V is the gain of the receiver front end. However, from simulation it is found that, the detected signal does not look good when the received signal is less than a few mV. Anyways, in this system with 23 dB attenuation through the silicon channel, the transmitter has to transmit maximum (-27+23) = -4 dBm power or about 230 mV signal, which is quite feasible. Therefore, from holistic point of view, the commitment of this transceiver is very lucrative. Performance of this comparator is compared with state of the art in Table 7.1.

Table 7.1: Comparison of the high speed comparator with state of the art

Reference	This Work*	[99]*	[100]*	[101]*	[105]*
Technology	90 nm CMOS	90 nm CMOS	0.13 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
No. of Stages	3	3	3	3	2
Supply Voltage	1.2	1.0	1.2	+1.8/-1.8	1.8
Power Consumption (mW)	13.7	4.3	0.265	0.3	0.6
Maximum Speed (gbps)	4.5	0.528	0.5	N/A	0.5
Speed/Power Metric (GHz/W)	328.5	122.8	1886.8	N/A	833.3

*schematic simulated responses

This chapter designed a simple three stage high speed comparator after discussing on all its challenges. The objectives of the circuit were clearly identified and the design was evaluated rigorously. Then it was employed in the receiver to regenerate the transmitted bit streams, where it detected those signals very successfully. Finally the whole receiver was characterized to point out its performance limit so as to justify its commitment for this on-chip wireless interconnect system. This system fulfilled all its design objectives exceedingly.

CHAPTER 8
CONCLUSION

8.1 Summary of Contributions of this Work

This thesis endeavored to devise a new on-chip interconnects system for fending off traditional copper interconnecting wires which would impose a severe constriction on the data communication speed among the modules of next generation high speed integrated circuits. Devices of upcoming technologies are expected to offer even hundreds of GHz of bandwidth, which will not be relishable unless a whole new interconnects systems, replaces the traditional copper interconnecting wires. Chapter 1 of this thesis mentioned the major contributing factors of copper wires those make them incapable of supporting high speed data transmission. The alternative interconnecting techniques were discussed in brief to explain why RF/Wireless interconnects would be superior, especially when it will come up with UWB signaling topologies. The objectives and the challenges of the system were clearly identified.

Chapter 2 described a transceiver architecture that could be used to satisfy all design objectives. It showed how TR-UWB communication scheme can be used to end up to a self synchronized receiver where bulky and power hungry circuits like PLL (Phase Locked Loop) will not be needed. So, the system could be expected to be compact, low power and simple.

A square law up-conversion mixer was designed in chapter 3, which would be required in case the pulse width of the UWB pulse stream was not much brief i.e. bandwidth of the transmitted signal is much lower than the bandwidth of the on-chip antenna pair. This circuit had a number of advantages over other square law mixers of literature. First, it uses a new input isolation technique which makes it usable in high frequencies, that was one of the main reasons why this topology is not much popular in

those frequencies. Second, it is a single branch circuit and so consumes power as low as 9.25 mW. Third, the circuit was analyzed theoretically, that was another contribution of this work. And after all, this circuit could up-lift a 1 GHz signal to 20 GHz band conveniently. However, this circuit was not required at the end because high frequency UWB pulse generator appeared by that time.

Chapter 4 designed a 20 GHz differential low noise amplifier (LNA) and optimized it for this particular application. The design started from a 21 GHz source degenerated differential LNA, by identifying its shortcomings and modifying it accordingly. A latest matching technique was incorporated there to shed off source degenerating inductors that not only improved gain, but also reduced the space requirement significantly. The technique was described in detail and it was showed how it affects noise matching. This matching scheme is used in some of the latest works without any investigation like this. So, the analysis was another contribution of this work. Time domain response of the circuit was satisfactory and it consumed 17 mW power occupying 0.365 mm^2 area on silicon chip.

Chapter 5 included a theoretical analysis of the Gilbert's mixer as frequency converter and small signal multiplier, where the later one is contributed by this work. That chapter also discussed on the limitations of traditional mixer topologies in modern low power circuits and showed a way out. Then a new unifying technique was proposed to merge LNA and mixer to end up to a compact receiver front end. Such a simple one has not been reported yet in literature. The receiver front end designed there could detect traditional BPSK signal synchronously as well as differentially, consuming only 27 mW power and occupying 0.47 mm^2 chip area.

Chapter 6 modified the receiver front end of previous chapter so as to prepare it for handling TR-UWB signal. Design objectives and challenges were clearly sorted out. The bandwidth extension method incorporated there was used in [85] but without much explanation, whereas detail design issues, advantages and shortcomings of that method can be found in that chapter. The modified circuit processed the received signal satisfactorily

for feeding it to the following high speed comparator. Then a new signaling scheme was proposed to increase the signal strength for increasing the communication distance of the transceiver or for reducing transmitted power level. All the features of this new proposal were evaluated judiciously and the circuit also satisfied all its objectives when working with those new TR-UWB pulse streams.

Finally, a simple three stage differential to single ended comparator was designed which had a number of issues relative to the short channel effects of this 90 nm technology. At first, the design challenges and constraints were reckoned. Then, all the design steps were showed clearly to demonstrate how the technological difficulties were dealt with. The comparator borrowed the concept of sense amplifier in its last stage. Anyways, after the in depth characterization of the circuit, it was employed to regenerate the transmitted bit streams from the output of the receiver front end. Its performance was outstanding. The operational limits of the whole receiver were quantified at the end, in terms of maximum allowable speed and minimum detectable power level. Its range of operation conformed to the signaling budget of the transmitter. The whole receiver consumed about 40 mW power from 1.2 V power supply, occupying 0.9 X 0.74 = 0.67 mm^2 and 1.3 X 0.89 = 1.16 mm^2 area without and with probe pads respectively. Layouts of the whole receiver and of the full chip are shown in Fig. 8.1 and Fig. 8.2 in respective order.

There are a few works in literature, concentrated on subsidiary issues of such on-chip wireless interconnects systems like channel estimation, signaling schemes, communication issues, bit error rates and so on. But a complete transistor level design for interconnecting circuit modules wirelessly on silicon chip is not reported yet, especially for communicating random digital bit streams. It that sense, designing such system was the major achievement of this work. However, this design is still in simulation level, has a few short comings and so has a long way to go.

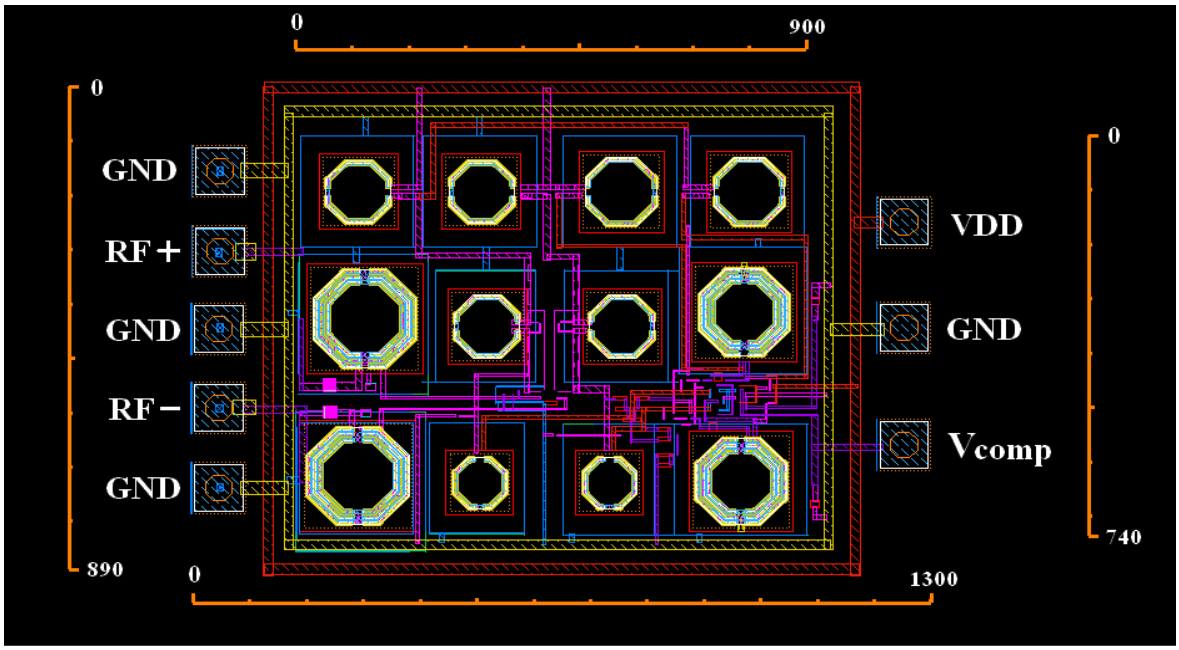

Figure 8.1: Layout of the whole receiver (dimensions are shown in μm)

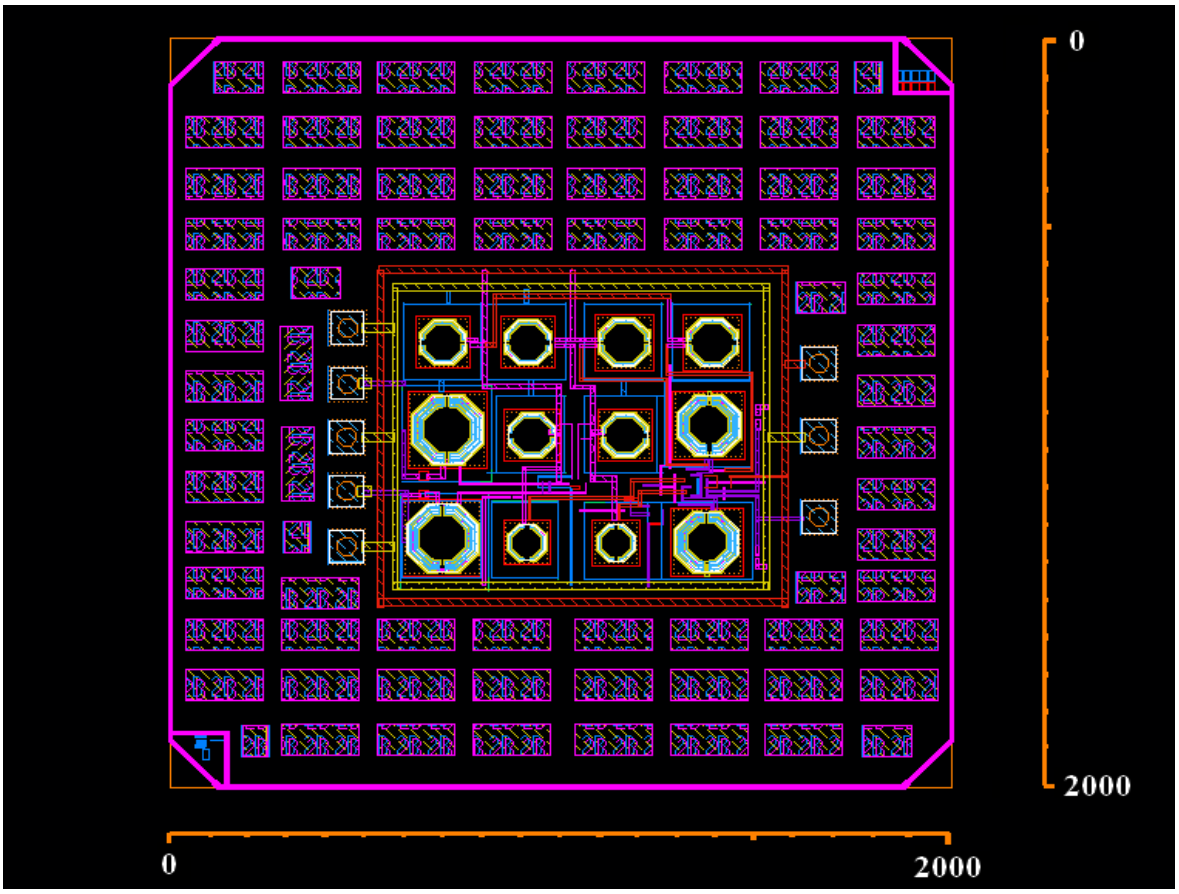

Figure 8.2: Layout of the full chip (dimensions are shown in μm)

8.2 Future Works

As mentioned in last section, design of this transceiver system is not finished yet. It awaits a few immediate advancements. Firstly, the delay element used in this system was modeled as ideal. Actually, it was the only circuit block of this system which is yet to be designed. Designing this thing will not be so easy. All the delay circuits available in literature are for large signal i.e. for digital applications; whereas the system will need to delay small amplitude UWB pulses by a few ps. So, designing this circuit should be of first priority.

Secondly, the antenna pair has to be re-designed to pull its center frequency down to 10 GHz from 20 GHz. Also, a through analysis can be carried on to investigate the maximum communication distance that can be maintained for successful detection by the receiver for a given transmitted power level. Or the minimum transmitted power that can be allowed for successful operation of the system over a given distance etc.

Thirdly, this system will need to be fabricated and tested. This will be the most crucial and challenging part, since behavior of such high-frequency circuits change a lot after they are integrated on silicon chip. Myriads of design issues may pop up in this step.

Next, a wideband matching technique can be tried for the RF and LO inputs of the receiver front end. In chapter 6, it was pointed that, peoples use high order Chebyshev filter for that purpose, but narrow band matching was preferred in this work for saving significant space, since this digital system worked fine with that. However, it will not do without wideband input matching if this receiver front end is employed in any analog system.

More advanced design objectives will appear next like incorporation of multiplexing for simultaneous communication of multiple data streams, design and inclusion of high speed ADC (Analog to Digital Converter) for converting random analog signal to digital data for the transmitter, finding BER (Bit Error Rate) etc.

In short, although a complete on-chip wireless transceiver was assembled here after designing, improving and optimizing the transistor level circuit blocks, which was able to detect the transmitted digital data successfully, but it still awaits a lot of research for moving onward. Therefore, the beauty of this thesis is to open up a window for research that will eventually lift off the noose from the neck of communication channels enabling them support next generation ultra high speed integrated circuits.

Appendix A

Photograph of the Fabricated Low Noise Amplifier

Half circuit of the 21 GHz source degenerated differential low noise amplifier of chapter 4 was fabricated from IBM under MOSIS Education Program (MEP), in co-ordination with Mr. Ashraf Islam, Phd. Student, Department of EECE, UTK, Knoxville and Dr. Syed Kamrul Islam, Professor, Department of EECE, UTK, Knoxville. Photograph of the lot of 40 chips are given bellow.

Figure A.1: Photograph of the lot of 40 chips of 21 GHz source degenerated LNA

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