COMPACT MODELING OF INVERSION CARRIER EFFECTIVE MOBILITY FOR NANOSCALE FinFET

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by

Md. Zakir Hossain

BUET
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
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This thesis titled "COMPACT MODELING OF INVERSION CARRIER EFFECTIVE MOBILITY FOR NANOSCALE FinFET" submitted by Md. Zakir Hossain, Roll No: 0409062213P, Session: April 2009 has been accepted as satisfactory in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on July 9, 2011.

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BUET, Dhaka Md. Zakir Hossain

July, 2011

ABSTRACT

As the device feature size enters into the nanoscale, the modeling and simulation of carrier transport in FinFETs devices becomes challenging. FinFETs technologies under development have channel lengths well below 100 nm where near-ballistic operation becomes feasible. In this thesis an easy approach to model carrier transports in terms of effective mobility in nanoscale FinFETs is presented. The inversion carrier effective mobility has been analyzed for nanoscale n-channel FinFET. The effective mobility has been simulated by considering the phonon scattering, coulomb scattering and surface roughness scattering mechanisms. Mobility due to each scattering phenomenon has been modeled in terms of effective electric field. In order to determine the effective electric field in the FinFET channel, the inversion layer charge density and the depletion layer charge density have been calculated by using semi-classical expression. By using this effective mobility, current-voltage characteristics have been studied for different operating regions of FinFETs of different channel lengths and also for different oxide thickness. The effect of channel length on mobility in nanoscale devices has been considered and found that the effective mobility decreases with the shrinking of the channel length. To eliminate this discrepancy of mobility the "Mathiessen-like" semi-classical expression has been used with appropriate modification by incorporating a parameter. The range of this parameter has been specified by several simulation works of different FinFET devices for a specific range of channel length. The decrease of threshold voltage with decrease in gate length is a well-known short channel effect called the *"threshold voltage roll-off"* has been investigated. Channel conductance and output transconductance has also been calculated for nanoscale FinFETs for different operating regions. In order to test the validity of the proposed model the simulation results have been compared with the available experimental and/or simulation data. The analytical expressions derived in the present model can be a useful tool in device design and optimization.

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LIST OF FIGURES

LIST OF SYMBOLS

a	Regression coefficient
b	Regression coefficient
BOX	Buried oxide
C_{ox}	Oxide capacitance
D_n	Diffusion constant
DIBL	Drain Induced Barrier Lowering
E	Electric field
E_{eff}	Effective electric field
Ec	Vertical electric field
H_{fin}	Fin Height
h	Plank's constant
I_{ds} /I_d	Drain-source current
$I_{d,sat}$	Saturation drain current
J_n	Diffusion current density
k	Boltzmann constant
L_G	Gate length
L_{eff} / L_{ch}	Effective channel length/ Electrical channel length
m	Body effect coefficient
m_a	Effective mass of electron
n_i	Intrinsic electron concentration
N_{inv}	Inversion layer carrier concentration
N_{sub}	Surface concentration
N_a	Substrate impurity concentration
n_p	Minority carrier concentration
n_{p0}	Minority carrier concentration at equilibrium
q	Electron Charge
Q_n	Inversion layer charge per unit area
SOI	Silicon-on-Insulator

S/D	Source/Drain
t_{ox}	Oxide thickness
T_{fin} / t_{fin} / W_{fin}	Fin-width
V_{th}	Threshold voltage
V_{gs}	Gate to Source voltage
V_{ds}	Drain to Source voltage
V_{si}	Voltage at Si fin
V_{ox}	Voltage at oxide layer
$v_{d,sat}$	Saturation voltage
v	Drift velocity
v_{th}	Average thermal velocity
x_{dp}	Position of depletion layer edge
V_t	Thermal voltage
W/ W_{eff}	Gate width / Channel width
X_d	Depletion layer thickness
$\psi(x)$	The surface potential in x-direction
μ_n	Electron mobility
φ_s	Surface potential
$\Delta\Phi_f$	Surface potential difference
μ_{eff}	Effective mobility
μ_{ph}	Mobility due to phonon scattering
μ_{col}	Mobility due to coulomb scattering
μ_{sr}	Mobility due to surface roughness scattering
μ_{bal}	Ballistic mobility
μ_{teff}	Long channel mobility
τ_c	Mean free time
ϕ_{ms}	Work function difference
ε_{si}	Permittivity of Si
φ_b	Bulk Fermi Energy

CHAPTER 1

INTRODUCTION

1.1 Introduction

The invention of the metal-oxide-semiconductor field-effect transistor (MOSFET) in early 1960's broke the barrier to the large-scale integration (LSI) that the initial integrated circuits (IC) with bipolar transistors could not reach [1]. MOSFET has since then become the fundamental semiconductor component of almost all modern electronic circuits. And the steady dimensional downscaling of the MOSFET has been the main drive of the IC technology and information technology, since shrinking the size especially the distance between the source and drain of a MOSFET means increasing the circuit speed, makes more space available to bringing more transistors on the same area, and reduces the manufacturing cost. As shown in Fig.1.1 [2], the downscaling of the MOSFETs has been kept in pace with Moore's law quite well, and the number of transistors on a chip has indeed been doubled about every two years. The key dimension that is reduced from one transistor generation to the next is the gate length (L_G). However, scaling of conventional MOSFET devices is limited due to short channel effects (SCE), gate insulator tunneling and limited control of doping concentrations. An important short channel effect is the so called Drain Induced Barrier Lowering (DIBL). DIBL becomes more prominent as the length of the device is reduced. DIBL is a secondary effect in MOSFETs referring to a reduction of threshold voltage at higher drain voltages. Due to the higher drain voltage the depletion region between the drain and body increases in size and extends under the gate. Gate tunneling is reduced by using thicker gate oxides of insulators with a higher dielectric constant, the so called high-k materials, which increases the barrier width between the gate and the channel. The short channel effects can also be suppressed by developing multigate devices [3-4]. In a multigate device, the channel is surrounded by several gates on multiple surfaces, so the control over the channel is improved. Various types of multigate devices are under research such as double gate transistors, FinFETs and gate-all-around FETs.

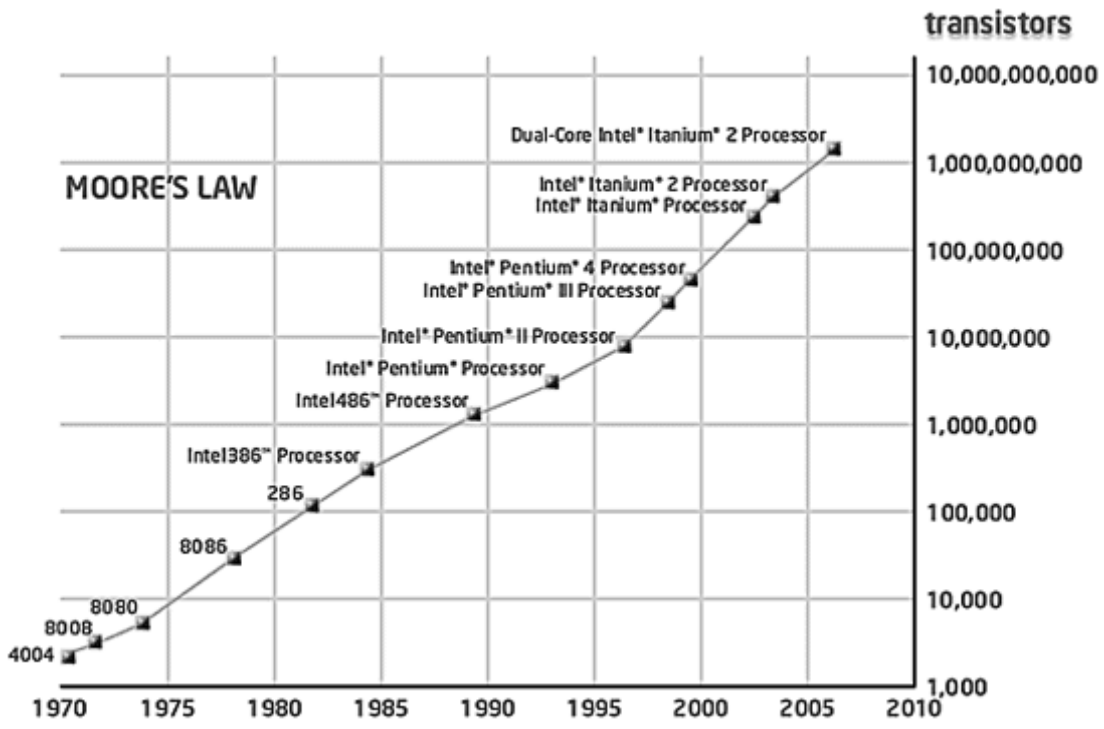

Fig.1.1: Number of transistors integrated in Intel's microprocessors vs. the production year [2].

1.2 Literature Review

There are two primary device structures that have been widely studied and used in complementary MOS (CMOS) technology. The first one is the bulk structure, where a transistor is directly fabricated on the semiconductor substrate and the second is called SOI (silicon-on-insulator) structure, where a transistor is built on a thin silicon layer which is separated from the substrate by a layer of insulator which may be a buried oxide (BOX) layer. The SOI technology has several advantages over the bulk structure [5], such as:

- Simple IC processing (isolation)
- No latch-up
- Higher density
- No body effect
- Reduced S/D junction capacitance
- Better sub-threshold slope.

In a continuous effort to increase current drive and better control short channel effects, silicon-on-insulator MOS transistors have evolved from classical, planar, single-gate devices into three-dimensional devices with a multi-gate structure (double-, triple- or quadruple- gate devices). These devices offer a higher current drive per unit silicon area than conventional i.e., bulk MOSFETs. In addition, they offer optimal short-channel effects (reduced DIBL, Fig.1.2, and subthreshold slope degradation). Fig.1.2 shows that the SOI devices allow the acceptable DIBL values (e.g. bellow 100 mV) for shorter channel length.

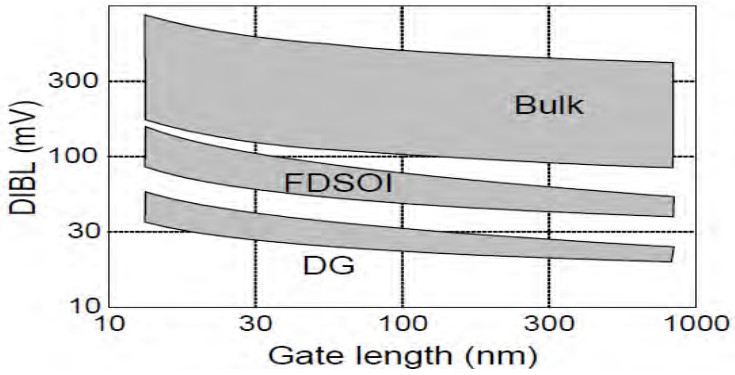

Fig. 1.2: Typical drain-induced barrier lowering in bulk, fully depleted SOI (FDSOI) and double-gate (DG) MOSFETs [6].

As a result, various alternate device structures have been studied. The FinFET is one such novel emerging device which is considered to be a suitable successor to the conventional MOSFET winning-over many of the hurdles.

In November 1999, C. Hu et al [7] in the USA first proposed the idea of FinFET. This makes it possible to form four hundred times as many transistors on a semiconductor chip compared to conventional methods. At the next year, Hisamoto et al reported a self-aligned double-gate MOSFET, FinFET, along with simulation results of electrical characteristics [8].

The effects of a nonuniform source/drain (S/D) doping profile on the FinFET characteristics was investigated by D. S. Woo et al [9] in 2002 using three-dimensional device simulation with vertically nonuniform source/drain(S/D) doping profile and it was shown that with a fixed S/D doping profile, larger SOI thickness can suppress short-channel effect due to the effect of a longer channel region.

G. Kathawala et al in 2003 analyzed the performance of *n*-channel FinFET and compared to double-gate MOSFET by a full-band Monte Carlo simulator [10] and observed that quantum-corrections have only a small effect on the total sheet charge in the channel, even though the charge distributions are quite different. The volume inversion effect becomes more prominent when quantum effects are applied counter balancing the depletion of charge near the interface.

A physics based model was studied by H. R. Khan et al in 2004 [11] using semi-classical 3D Monte Carlo device simulator to investigate important issues in the operation of FinFETs. Fast Multipole Method (FMM) has been integrated with the EMC (*Ensemble Monte Carlo*) scheme to replace the time consuming Poisson equation solver. Effect of unintentional doping for different device dimensions has been investigated and from the result it was shown that the effect of unintentional doping becomes dominant near sub-threshold regime where number of mobile carriers is very few.

A methodology was proposed by A. Bansal et al [12] in 2005 to optimize the gate sidewall spacer thickness simultaneously minimize leakage current and drain capacitance to on-current ratio in FinFET devices for robust and low-power SRAMs. In this approach, the spacer thickness was optimized to reduce the leakage current of a FinFET while minimizing the performance degradation. The proposed technique also reduced the sensitivity of threshold voltage of the device to fluctuations in process parameters such as silicon thickness and gate length. Independent control of front and back gate in double gate (DG) FinFET for low-power logic options was also proposed by A. Datta et al [13] and developed a semi analytical model for different FinFET logic gates to predict their performance as an efficient circuit synthesis methodology.

The behavior of nanoscale FinFET device in the ballistic regime of operation was investigated by H. R. Khan et al [14] in 2006 using fully quantum mechanical simulator based on Contact Block Reduction (CBR) method. Simulation results showed that the transformation from multiple channels into a single merged channel as the fin width was reduced gradually and short channel effects also could be minimized by reducing the fin width. Later in 2007, J. Song et al [15] reported a compact model for DG FinFETs, where quantum mechanical effect and short channel effects were considered for a undoped body

and channel lengths from 10μm to 90nm FinFET. The simulation showed that quantum mechanical effects played significant roles in ultra short devices.

As the device feature size enters into the nanoscale, the modeling and simulation of carrier transport in FinFETs devices becomes challenging. FinFETs technologies under development have channel lengths well below 100 nm where near-ballistic operation becomes feasible. However, most of these studies are devoted to technological aspects and short-channel performance. Mobility is an important parameter for carrier transport because it describes how strongly the motion of an electron is influenced by an applied electric field. Mobility is directly related to the mean free time between collisions, which in turn is determined by the various scattering mechanisms. M. M. Chowdhury et al [16] in 2006 had proposed a physics-based model for double-gate (DG) MOSFET to contemporary nanoscale undoped n-channel DG FinFET. It showed that about three-times higher strong inversion electron mobility in the DG FinFET could be achieved, compared to that in a contemporary bulk-silicon planar MOSFET, and only about 20% lower than that in planar DG MOSFET. At the next year V. V. Iyengar et al [17] proposed a simple methodology for the extraction of the top and sidewall mobility in FinFET like triple-gate device architectures. By this model top and sidewall mobility on both n- and p-channel FinFETs, fabricated with various fin-patterning processes and gate dielectrics, was extracted. This method was then applied to study the effect of different hard-mask processes for fin patterning and the impact of corner-rounding processes. But how to measure the mobility was not described and no expression for mobility was given in both works [16, 17].

M. Poljak et al. [18] in 2008 studied SOI and bulk FinFET by a three dimensional numerical device simulator and their electrical characteristics were compared for different body doping and bias conditions. From this simulation higher drain current in case of SOI FinFET was shown, but classical mobility model was used for this work.

J. Song et al [19] in 2009 reported the experimentally measured strain effect on electron and hole transport in FinFETs. It was found that the hole mobility was enhanced while the electron mobility reduced as channel length decreases. Later in 2010 J. Song et al [20] published another paper where an analytic potential model for symmetric double gate MOSFET was verified and calibrated with experimental n- and p-channel FinFET

data over a wide range of gate lengths and bias regions. Here the long-channel mobility was measured by considering only phonon scattering and coulomb scattering mechanisms. But the short channel mobility is not the same as that of long channel devices [21]. Moreover, mobility was measured in terms of the scattering mechanism which strongly depends on the channel length and other parameters which are missing in literature.

1.3 Objective of the Thesis Work

FinFETs have been widely studied because of their tremendous potential for nano CMOS technologies [8-15]. However, most of these studies are devoted to technological aspects and short-channel performance, while physical properties of FinFETs still lack extensive experimental investigations. The purpose of this work is to gain knowledge and understanding of physical properties of FinFETs, using extensive simulations. The main attention is concentrated to the important characteristics of FinFETs, namely, *the carrier effective mobility*. The effective mobility is the key parameter for any CMOS technology, nevertheless, only a few measurements or models of the effective mobility in FinFETs up to now have been reported [16-20].

Objectives of this work are briefly mentioned below:

i) To model the effective mobility incorporating the impact of different scattering mechanisms in inversion layer of nanoscale SOI n-channel FinFETs.

ii) Analysis of various electrostatic characteristics of nanoscale FinFETs using the developed model and to compare the results to the available simulation and/or experimental data to justify the compatibility of the model.

1.4 Organization of the Thesis

Chapter 2 contains a discussion on the structure and some remarkable feature of FinFET. The current-voltage relationship, different scattering mechanisms and the mobility in the inversion channel based on these scattering mechanisms, the existing effective mobility model for nanoscale FinFETs are also included in this chapter. The mathematical analysis of the proposed mobility model for nanoscale FinFETs are described in the chapter 3. In chapter 4, the mobility and I-V characteristics of short channel FinFETs for different channel lengths, oxide thickness and bias voltage are plotted. The results are discussed and compared with the available experimental and/or simulation data. Chapter 5 contains summary and conclusions of this work with some suggestions for future work.

CHAPTER 2

FinFET THEORY

2.1 Introduction

FinFETs are the most promising device structures to address short channel effects and leakage issues in deeply scaled CMOS, as FinFETs can be fabricated using conventional CMOS processes. Moreover the FinFET is an ultrathin body device which eliminates the need of channel doping, thereby reducing parametric spread due to dopant fluctuations and reducing junction leakage due to high electric fields [22]. As the device dimension is scaled down aggressively, however, additional physical effects such as short-channel effects, namely, threshold voltage roll-off, drain-induced barrier lowering (DIBL), subthreshold current slope and effective mobility degradation become important

In this chapter, we present some basic background information that would help in following the rest of this report. We first give a brief overview of DGFETs and FinFETs and their operation. Then I-V characteristics, scattering mechanisms and mobility of FinFETs will be described systematically.

2.2 FinFET Structure

2.2.1 Double-gate MOSFETs (DGFETs)

Double gate MOSFETs (DG-FET) is a MOSFET that has two gates to control the channel. In a DGFET the channel is under the control of two gates, viz. the front and back gates. This helps in reducing the effect of the drain field in reaching the source, and thus results in reduced SCE.

There are 2 kinds of DG-FETs:

Symmetric

Asymmetric

Symmetric DG-FETs have identical gate electrode materials for the front and back gates (ie. top and bottom gates). When symmetrically driven, the channel is formed at both the

surfaces. In an asymmetric DG-FET, the top and bottom gate electrode materials can differ (eg. n+ poly and p+ poly). When asymmetrically driven this would end up forming a channel on only one of the surfaces. Both have their advantages and disadvantages

2.2.2 FinFET

The structure of a FinFET is shown in Fig. 2.1. Even though current conduction is in the plane of the wafer, it is not strictly a planar device. Rather, it is referred to as a quasi-planar device, because its geometry in the vertical direction (viz. the fin height) also affects device behavior. Amongst the DG-FET types, the FinFET is the easiest one to fabricate. It is so called because the thin channel region (body) stands vertically like the fin of a fish between the source and drain regions. The gate wraps around the body from three sides, and this is responsible for higher gate-channel control and therefore reduced SCE. In strong inversion, conduction predominantly occurs close to the sidewalls, whereas in sub-threshold it occurs along the fin center (ie. midway between the sidewalls).

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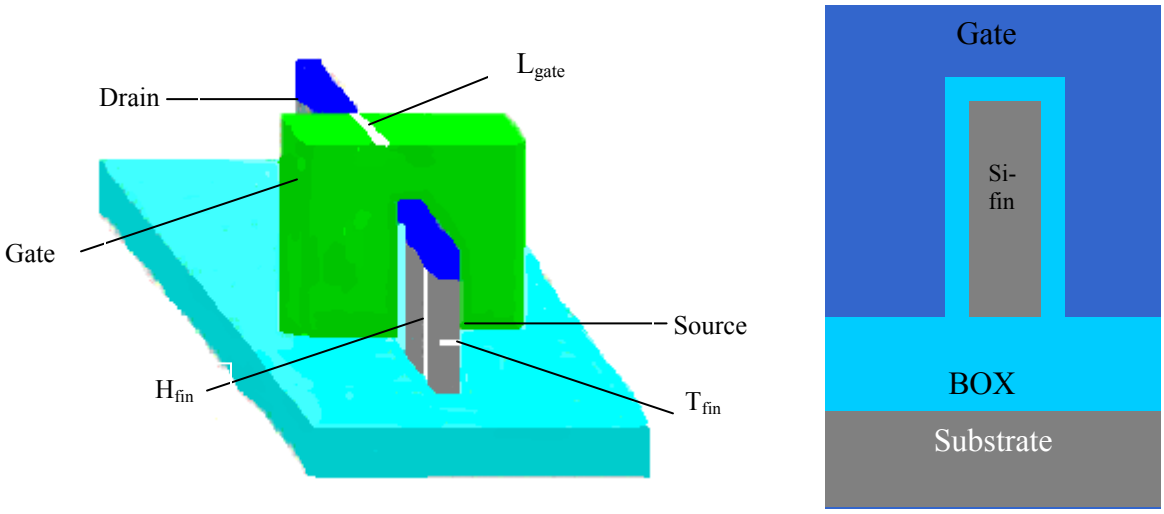

(a) (b)

Fig. 2.1: FinFET structure: (a) with dimensions marked [23] and (b) 2D cross-section along transistor gate (SOI).

The dimension T_{fin} shown in the Fig. 2.1 is the fin-width and is alternately referred to as t_{si} or W_{fin} in the literature. H_{fin} is the height of the fin. L_{gate} is the gate length or channel length of

the device. As shown in Fig. 2.1, sufficiently narrow FinFETs (t_{si} << H_{fin}) can be approximated as a SDG MOSFET [20].

Because the channel is wrapped around the surface of the fin, the gate width of a triple gate FinFET is commonly assumed to be twice the fin height (H_{fin}) plus the fin width (W_{fin}), i.e., $W=2H_{fin}+W_{fin}$, at strong inversion mode [24]. In many cases, W_{fin} is small in order to have acceptably small SCE. Moreover, in a DG-FinFET, the top gate is anyway ineffective. As a result, W is approximately 2 H_{fin}. As a result, the physics of a FinFET becomes largely similar to that of a DGFET. Thus, most of the literature that discuss compact model development for DGFETs can be applied to FinFETs with a minor parameter (H_{fin}) adjustment, as done in [25]. The electrical or effective channel length L_{eff} is defined as the spacing between the electrical source and the drain depletion layers inside the channel region. An important note is that in this work we assume that the designed gate length (design on layout, DOL) equals the physical gate length L_g (design on silicon, DOS). In reality the difference between these two parameters could be considerable and induce a ΔL. Also we neglect the effect of line-edge roughness (LER). The maximum gate width of a FinFET is determined by the technological limit of the aspect ratio (H_{fin} / W_{fin}). The width can also be increased by placing multiple fins in parallel, which results in an integer number of possible gate widths.

Main Features of FinFET are:

1) Ultra thin Si fin for suppression of short channel effects
2) Raised source/drain to reduce parasitic resistance and improve current drive
3) High-k gate dielectrics
4) Symmetric gates yield great performance, but can built asymmetric gates that target $V_{th.}$

2.2.3 Applications of FinFETs

DG devices like Fin FETs offer unique opportunities for microprocessor design compared to a planar process in the same technology node; FinFETs have reduced channel and gate

leakage currents. This can lead to considerable power reductions when converting a planar design to FinFET technology. Utilizing FinFETs would lead to a reduction in total power by a factor of two, without compromising performance. Another possibility to save power arises when both gates can be controlled separately. The second gate can be used to control the threshold voltage of the device, thereby allowing fast switching on one side and reduced leakage currents when circuits are idle.

Finally, separate access to both gates could also be used to design simplified logic gates. This would also reduce power, and save chip area, leading to smaller, more cost-efficient designs. However chip designs using FinFETs must cope with quantization of device width, since every single transistor consists of an integral number of fins, each fin having the same height.

2.3 I-V Characteristics of FinFET

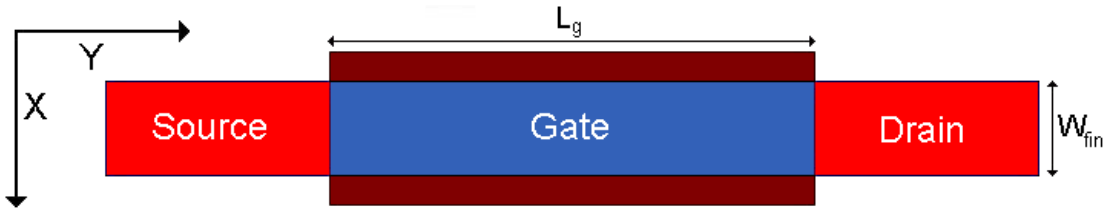

Fig. 2.2: A 2D cross-section of the FinFET.

From the literature [20, 25] it is found that the operation of FinFETs are similar to that of DG-MOSFETT, and especially to the SDG MOSFET. Hence after the inversion layer is formed by applying appropriate gate voltage, if drain current is applied, the charges in the inversion layer start to flow from the source to the drain. Current flows from the drain to the source through the channel. The FinFET is operated in three regions like MOSFET: subthreshold, linear and saturation regions, depending on the value of bias voltages. When the gate voltage is below the threshold voltage ($V_{gs} < V_{th}$), the semiconductor surface is weakly inverted and the device is turned off, and there is no conduction between drain and source. In reality, the Boltzman distribution of electron energies allows some of the more

energetic electrons at the source to enter the channel and flow to the drain, resulting in a subthreshold current that is an exponential function of gate- source voltage. This region of FinFET operation is called subthreshold region.

To model the subthreshold current, only the diffusion component is considered, as in subthreshold the drift component of the current is negligible. By applying low gate-source voltages, electrons diffuse from the source to the drain yielding the electron injection at the edge of the source-fin depletion layer for a NMOS being [26]:

$$n_p\left(x_{dp}\right) = n_{p0} = \frac{n_i^2}{p} \approx n_i\, e^{\frac{\psi(x)}{v_t}} \tag{2.1}$$

And at the drain side:

$$n_p\left(x_{dp} + L_{eff}\right) = n_{p0} e^{\frac{\left(-V_{ds}\right)}{v_t}} \tag{2.2}$$

The carrier density in the y-direction (Fig.2.2), i.e. perpendicular to the gate dielectric, is presumed constant, since the surface potential in the subthreshold regime is constant. n_p is the minority concentration (in this case electrons), x_{dp} the position of the depletion layer edge at the source side of the channel, n_i the intrinsic carrier concentration, p the hole concentration, $\psi(x)$ the surface potential, V_t the thermal voltage (kT/q) and L_{eff} the electrical or effective channel length, defined as the spacing between the electrical source and the drain depletion layers.

The diffusion current density can be expressed as [26]:

$$J_n(x) = qD_n \frac{dn}{dx} \tag{2.3}$$

Where n is the electron density at the source and drain side given by Eq. (2.1) and (2.2) respectively and D_n the diffusion constant, as [26]:

$$D_n = \mu_n \frac{kT}{q} \tag{2.4}$$

Where μ_n is the carrier mobility. Combining Eq.(2.1), (2.2) and (2.3) (assuming no recombination between the source and the drain) results in:

$$J_n(x) = qD_n \frac{n_p(x_{dp} + L_{eff}) - n_p(x_{dp})}{L_{eff}} \tag{2.5}$$

$$= qD_n \frac{n_i}{L_{eff}} e^{\frac{\psi(x)}{v_t}} \left(1 - e^{\frac{(-V_{ds})}{v_t}} \right) \tag{2.6}$$

Now the drain-source current (I_{ds}) can be calculated from the current density, since the distribution of the electron concentration is constant perpendicular to the gate dielectric (volume inversion):

$$I_{ds} = J_n W H_{fin} \tag{2.7}$$

Where J_n is the current density and W is the channel width or effective channel width and H_{fin} the height of the fin, respectively. The formula for the drain current in subthreshold becomes:

$$I_{ds} = qD_n \frac{n_i W H_{fin}}{L_{eff}} e^{\frac{\varphi_s}{v_t}} \left(1 - e^{\frac{(-V_{ds})}{v_t}} \right) \tag{2.8}$$

The potential φ_s relates to the applied gate voltage V_{gs}. The gate-source voltage is distributed over the oxide and the silicon: $V_{gs} = V_{si} + V_{ox}$, with V_{ox} the charge over C_{ox} and V_{si} is $\varphi_s + \Delta\Phi_f$, because the inversion carrier concentration in subthreshold is generally negligible, we could state that the gate voltage falls only over the Silicon: $V_{gs} = \varphi_s + \Delta\Phi_f$, i.e. the surface potential is equal to $V_{gs} - \Delta\Phi_f$ [27]. However, because of the depletion capacitances from the source- and drain-body junctions the subthreshold current is less controlled by the gate. This is modeled with the so-called ideality factor, (m) as well be explained later. Implementing this in Eq. (2.8) becomes [28]:

$$I_{ds} = qD_n \frac{n_i W H_{fin}}{L_{eff}} e^{\frac{\left(V_{gs} - \Delta\Phi_f\right)}{mVt}} \left(1 - e^{\frac{\left(-V_{ds}\right)}{Vt}}\right) \tag{2.9}$$

Substituting the value of D_n, the drain current of Eq. (2.9) in subthreshold region becomes [29]:

$$I_{ds} = \mu_{eff} \frac{W}{L_{eff}} t_{si} n_i kT\, e^{\frac{\left(V_{gs} - \Delta\Phi_f\right)}{mVt}} \left(1 - e^{\frac{\left(-V_{ds}\right)}{Vt}}\right) \tag{2.10}$$

Here μ_{eff} is the effective mobility. The ideality factor or body effect coefficient m, is given by [30]:

$$m = 1 + \frac{3t_{ox}}{X_d} \tag{2.11}$$

X_d is the depletion layer thickness and t_{ox} is the oxide thickness.

When gate voltage is larger than the threshold voltage ($V_{gs} > V_{th}$) the channel acts as a resistor. The drain current is proportional to the drain voltage. This is called the linear region of operation. In linear region, the drain current is modeled as [29]

$$I_{ds} = 2\mu_{eff} C_{ox} \frac{W}{L_{eff}} \left(v_{gs} - v_{th} - \frac{v_{ds}}{2}\right) v_{ds} \tag{2.12}$$

Where v_{th} is the threshold voltage. The minimum gate voltage is required to create strong inversion is called *threshold voltage*, given as [6]:

$$V_{th} = \phi_{ms} + \frac{kT}{q} \ln\left(\frac{2C_{ox} kT}{q^2 n_i t_{si}}\right) + \frac{h^2 \pi^2}{2m t_{si}^2} \tag{2.13}$$

The first term of Eq.(2.13) is the work function difference between the gate and the silicon film. The second term represents the potential Φ in the channel. It is inversely proportional to the silicon film thickness $t_{si.}$ The third term of the Eq. (2.13) is the lowest subband energy above conduction band minima. It is a quantum mechanical term which varies depending on the splitting of the conduction band energy level into subbands.

After the strong inversion, when the drain voltage is increased, current starts to flow between the drain and source. Since the drain voltage is higher than the gate voltage,, the electrons spread out and conduction is not through a narrow channel but through a broader, two or three dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as pinch-off to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon the drain voltage and controlled primarily by the gate-source voltage. After the pinch-off occurs, the drain current reaches to its saturated value. At this point, the drain voltage is called saturation voltage and operating region is called saturation region. These voltage and current can be given as [30]:

$$I_{ds} = I_{d,sat} = \mu_{eff}\, C_{ox} \frac{W}{L_{eff}} \frac{\left(v_{gs} - v_{th}\right)^2}{2m} \tag{2.14}$$

Saturation Voltage $V_{d,sat}$ is:

$$v_{d,sat} = \left(v_{gs} - v_{ds}\right)/\, m \tag{2.15}$$

2.4 FinFET Mobility

2.4.1 Mobility

Mobility is a measure of scattering, low mobility indicates a high level of scattering. The inversion layer mobility is the key parameter for any CMOS technology which describes the drain current and a probe to study the electrostatic properties of a two dimensional carrier system.

Mobility describes how strongly the motion of an electron is influenced by an applied electric field. When electric field is applied to the semiconductor, carriers experience a force from the field (in the opposite direction to the field) during the between collisions. The movement of charges under the influence of an electric field is termed drift. Therefore an additional velocity component is superimposed upon the thermal motion of carriers. This additional component is called *drift velocity*. The drift velocity is proportional to the applied electric field (E) and is given by the expression [26]:

$$v = -\frac{q\tau_c}{m_a}E \tag{2.16}$$

Here τ_c is the mean free time (or electron state life time), define as the average time between collisions, and m_a is the effective mass. The proportionality factor between the drift velocity and electric field is called mobility in unit cm^2/V-s and given as:

$$\mu = -\frac{q\tau_c}{m_a} \tag{2.17}$$

Mobility is directly related to the mean free time between collisions, which in turn is determined by the various scattering mechanisms. Mobility is measured in terms of effective electric field is given as [31]:

$$E_{eff} = \frac{1}{2}\frac{q}{\varepsilon_{si}}\left(\frac{N_{inv}}{2} + N_{sub} \times t_{si}\right) \tag{2.18}$$

Here ε_{si} is the permittivity of Si, N_{sub} is the surface concentration of the depletion charge and N_{inv} is the inversion layer carrier concentration. The Carrier concentration of inversion layer is defined by the following expression [32]:

$$N_{inv} = Q_n / q \tag{2.19}$$

Where Q_n the inversion layer charge per unit area, is a function of gate voltage and can be found by semi-classical expression [32]:

$$Q_n = -\left[v_{gs} - v(y) - 2\varphi_b\right]C_{ox} + \sqrt{\left(2\varepsilon_{si}\, q\, N_a \left[2\varphi_b + v(y)\right]\right)} \qquad (2.20)$$

Here $v(y)$ is the reverse bias applied between a point in the y direction (Fig. 2.2) along the channel and the source electrode (which is grounded). N_a is the substrate impurity concentration and φ_b is the Bulk Fermi Energy given as [28]:

$$\varphi_b = \frac{kT}{q}\ln\left(\frac{Na}{n_i}\right) \qquad (2.21)$$

2.4.2 Scattering Mechanism

Scattering is a general physical process whereby moving particles (electrons or holes) are forced to deviate a straight trajectory by one or more localized non-uniformities in the medium through which they move. The important scattering mechanisms affecting carrier transport in MOS devices are:

i. Phonon scattering
ii. Coulomb scattering
iii. Surface roughness scattering

2.4.3 Phonon Scattering

Phonon are an important source of scattering in carrier transport. Collective vibrations of electrons are known as *phonons.* These processes are strongly dependent on phonon occupation. In phonon scattering a carrier through the channel is scattered by a vibration of the lattice by finite temperature. The phonon scattering depends on the effective electric field and temperature. Mobility due to phonon scattering decreases at higher electric field. The mobility limited by phonon scattering can be determined by the following expression [20]:

$$\mu_{ph} = \frac{\mu_0^{ph}}{\left(1 + E_{eff} \Big/ E_c^{ph}\right)^{V^{ph}}} \tag{2.22}$$

Here, μ_0^{ph} and v^{ph} are constants. In this work, μ_0^{ph}= 755 cm^2/V-s and v^{ph} = 1.2 [20] are taken. E_c^{ph} the vertical electric field at some point along the channel on the semiconductor side of the interface between the gate dielectric and the semiconductor body. The value of E_c^{ph} has been taken as 0.5 MV/cm from the literature [33].

2.4.4 Coulomb Scattering

Coulomb scattering occurs due to the substrate doping impurities, interface state densities and charges trapped in gate oxide. Coulomb scattering results when a charge carrier travels past an ionized dopant impurity (donor or acceptor). The charge carrier path is deflected by owing to coulomb force interaction. The probability of coulomb scattering depends on the total concentration of ionized impurities, which is the sum of the concentration of negatively and positively charged ions. Coulomb scattering is less significant at higher temperature. Because, at higher temperature, the carriers move faster and they remain near the impurity atoms for a shorter time and are therefore less effectively scattered.

The mobility due to coulomb scattering can be determined by the following expression [20]:

$$\mu_{col} = \mu_0^{col}\left(1 + \frac{E_{eff}}{E_c^{col}}\right)^{V^{col}} \tag{2.23}$$

Here, μ_0^{col} and V^{col} are constant. In this work, the values of μ_0^{col} and V^{col} are taken as 213 cm^2/V-s and 1.4 respectively [20]. And the value of E_c^{col} has been taken as 0.65 MV/cm from the literature [33].

2.4.5 Surface Roughness Scattering

Surface roughness scattering or interface roughness scattering is the scattering of a charged particle by an imperfect interface between two different materials. In DG-MOSFET or FinFET devices, surface roughness scattering occurs due to spatial nanoscale heterogeneity of Si/SiO_2 interface. Scaling CMOS devices to smaller dimensions while maintaining good control of the short-channel effects make it necessary to reduce the gate oxide thickness in close proportion to the channel length. Thus, for devices with gate lengths below 100 nm, gate oxide thickness near to 2 nm is needed [34]. The use of such thin oxides leaves inversion layer electrons very near to the interface formed by the gate material (metal or polycrystalline silicon) and the oxide, SiO_2 and SiO_2/Si interface. This proximity is sufficient for the imperfections of this interface. The mobility due to surface roughness scattering can be evaluated by the following expression [35]:

$$\mu_{sr} = \mu_{sr0}\left(E_{eff}/E_{eff\,0}\right)^{\delta} \tag{2.24}$$

Where μ_{sr0} a constant, and $\delta = 2$ [35]. In this work, we adopt the same expression, making μ_{sr0} as a fitting parameter, and using $\delta = 1.9$ that is the value commonly derived from DG-MOSFETs.

2.4.6 Effective Mobility

The effective mobility is the total mobility that considers the effect of all the scattering mechanisms. The effective mobility for the above mentioned scatterings can be determined by the Matthiessen's rule:

$$\frac{1}{\mu_{teff}} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{col}} + \frac{1}{\mu_{sr}} \tag{2.25}$$

The curves of effective mobility versus effective electric field at different biasing conditions follow the universal relationship [36- 37]. The mobility curves have been shown in the next chapter, where the phonon scattering and surface roughness scattering dominate at the higher value of electric field and coulomb scattering at low value of electric field.

2.4.7 Mobility Reduction in Nanoscale FinFET

The dramatic reduction of the mobility measured as decreasing the gate length has been experimentally observed by many groups by different techniques [38-40]. The concept of mobility, resulting from an analysis of stationary transport where carrier velocity is limited by scattering phenomena, has been widely used till today in microelectronics as a measurable factor of merit and as a parameter of analytical models developed to predict device performance. If scatterings are still playing a major role in decananometer MOSFET and cannot be neglected [41-42], ballistic transport in the channel takes a growing importance as the gate length of MOSFETs tends to the nanometer scale.

The effective mobility determined by the Eq. (2.25) is said to be apparent mobility. Shur based model can be useful to describe the apparent decrease of extracted mobility with channel length. According to Shur's approach, the effective mobility μ_{eff} can be given by the "Mathiessen-like" following relation [43]:

$$\mu_{eff} = \frac{1}{\mu_{teff}^{-1} + \mu_{bal}^{-1}} \tag{2.26}$$

Where μ_{teff} is the long channel or apparent mobility and μ_{bal} is the “ballistic mobility” as defined by Shur [43].

The model developed by Shur introduces a parameter μ_{bal}, homogeneous to mobility and proportional to channel length, rewritten as [43]:

$$\mu_{bal} = K_{bal} L_{ch} \tag{2.27}$$

Here L_{ch} is the channel length or effective channel length and K_{bal} is a parameter defined by the relation [43]:

$$K_{bal} = \frac{2q}{\pi m_a v_{th}}, v_{th} = \sqrt{\frac{8kT}{\pi m_a}} \tag{2.28}$$

where q is the electron charge, m_a the conduction effective mass, v_{th} the average thermal velocity, k the Boltzmann constant and T the temperature. Combining Eq.(2.27) and (2.28) with the "Mathiessen-like" relationship (2.26), we can rewrite the effective mobility as a function of channel length [21]:

$$\mu_{eff} = \frac{\mu_{teff}}{1 + \frac{\mu_{teff}}{K_{bal} L_{ch}}} \tag{2.30}$$

CHAPTER 3

MOBILITY MODELING

3.1 Introduction

The effective mobility is the key parameter for any CMOS technology, nevertheless, only a few measurements or models of the effective mobility in FinFETs up to now have been reported [16-20]. A semi-classical model of inversion carrier effective mobility by incorporating the impact of the different scattering mechanisms for SOI n-channel nanoscale FinFET has been developed. Detailed description of the procedure is given in subsequent sections.

3.2 Mobility Model

As describe in Sec.2.4.7, the effective mobility according to Shur based model as the function of channel length is rewritten as:

$$\mu_{eff} = \frac{\mu_{teff}}{1 + \frac{\mu_{teff}}{K_{bal} L_{ch}}} \tag{3.1}$$

From the above expression, it is found that the effective mobility decreases with the decrease in channel length. But from the simulation result it has observed that the above "Mathiessen-like" expression can not accurately define the mobility degradation. This is because, for the occurrence of some additional scattering phenomena‟s and some other physical effects. The major reasons of this discrepancy are as follows:

- Remote surface roughness scattering,
- Silicon-thickness fluctuation-induced scattering,
- Doping pockets,
- Charge and neutral defects; and
- Some other unknown physical effects.

For all of these effects, the experimental measurements or analytical models have not clearly defined till now in short channels [21]. All these effects have defined by a parameter „p" for this work. Hence, for more accurate result the fitting parameter „p" has been introduced to the above relationship (Eq. 3.1). Then the modified expression of the effective mobility:

$$\mu_{eff} = \frac{p\mu_{teff}}{1 + \frac{\mu_{teff}}{K_{bal} L_{ch}}} \tag{3.2}$$

The value of „p" is < 1. This means that the actual mobility degradation is larger than the value defined by the Shur based model (Eq.3.1). The relation between the fitting parameter „p" and the channel length can be determined by the *Regression analysis*, written as:

$$p = a + bL_{ch} \tag{3.3}$$

Here a and b are the regression coefficients. The value of the regression coefficients have found, a = 0.614 and b = 2.81×10^{-3} nm^{-1} respectively, from the simulation result of channel lengths 32 nm, 85.8 nm, 90 nm and 102.2 nm for the values of p are 0.704, 0.85, 0.865 and 0.904 respectively. Now the value of p can be determined for any value of channel length by using the Eq.(3.3). The channel length must in nanometer. This relationship is valid for the channel length of 30 nm ~ 102.2 nm. The mobility model proposed by the above expression Eq.(3.2 and 3.3) has been used throughout the work.

Mobility is calculated with respect to effective electric field which depends on the inversion carrier concentration (N_{inv}) and gate bias, which creates this inversion carrier. Hence the effect of gate bias on inversion carrier concentration and the inversion carrier concentration on effective electric field has been observed by using the Eq.(2.18, 2.19 and 2.20) in the next chapter.

Since the effective mobility depends on the different scattering mechanisms, the individual mobility"s due to different scattering mechanisms has been observed with

respect to effective electric field, and also the effect of temperature on phonon scattering. After calculating the individual mobility"s, the effective mobility has been simulated by using the expression Eq.(3.2). The effect of gate bias and drain bias on effective mobility has been observed. The effective mobility changes with the change in inversion carrier concentration. The variation of effective mobility with the inversion carrier concentration has also been observed. As experimentally observed elsewhere, the mobility extracted from electrical characteristics decreases with the shrinking of the channel length which has described in Sec.2.4.7. The relationship between the effective mobility and the channel length for n-channel FunFET has been observed.

3.3 Current-Voltage Characteristics

The current–voltage (I-V) are the most important characteristics for any CMOS technology either experimental or analytical studies. Hence the current–voltage is simulated for the test device for different operating regions.

The drain current in subthreshold region by using the proposed mobility model, rewritten as [Eq.(2.10)]:

$$I_{ds} = \mu_{eff} \frac{W}{L_{eff}} t_{si} n_i kT\, e^{\frac{\left(V_{gs} - \Delta\Phi_f\right)}{mVt}} \left(1 - e^{\frac{\left(-V_{ds}\right)}{Vt}}\right) \tag{3.4}$$

When gate voltage is larger than the threshold voltage ($V_{gs} > V_{th}$) the channel acts as a resistor. This is called the linear region of operation then the drain current is [Eq.(2.12)]:

$$I_{ds} = 2\mu_{eff} C_{ox} \frac{W}{L_{eff}} \left(v_{gs} - v_{th} - \frac{v_{ds}}{2}\right) v_{ds} \tag{3.5}$$

After the pinch-off occurs, the drain current reaches to its saturated value. This operating region is called saturation region. The saturation current then becomes [Eq.(2.12)]:

$$I_{ds} = I_{d,sat} = \mu C_{ox} \frac{W}{L_{eff}} \frac{\left(v_{gs} - v_{th}\right)^2}{2m} \tag{3.6}$$

The I-V characteristics can be divided into two categories namely: the transfer characteristics or I_D-V_G characteristics and the output characteristics or I_D-V_D characteristics.

3.3.1 Transfer Characteristics

The transfer characteristics have been observed for low and high drain voltages and compared to the experimental data in both the linear and semi log scales. In order to observe the effect of drain voltage on transfer characteristics, drain current versus gate voltage are plotted for different drain voltages.

Drain current strongly depends on oxide thickness. The oxide capacitance increases with the decrease in oxide thickness and the oxide capacitance is directly proportional to the drain current. Hence the effect of oxide thickness on transfer characteristics has been simulated by using the proposed mobility model for different oxide thickness. As the channel length is reduced voltage required to turn on the device is less and hence current increases. For this, the variation of transfer characteristics with the variation of the channel length has also been observed.

All these transfer characteristics have been simulated by using the Eq.(3.4 and 3.5) with the variation of different parameters and shown systematically in the next chapter.

3.3.2 Output Characteristics

The output characteristics of any CMOS devices represent the important performances. For device design the effect of different parameters on output characteristics are needed. The effect of gate voltage on the output characteristics has been observed by using the proposed mobility model and compared to the experimental data in both the linear and semi log scales. The saturation current increases at higher gate bias.

The effect of channel length on output characteristics has been observed. As the channel length is decreased, the drain current increases. The saturation drain current for shorter channel length is higher. The effect of oxide thickness on output characteristics has been observed for n-channel FinFET of channel length of 85.5 nm. It is seen that drain current is highly dependent on oxide thickness.
All these output characteristics have been simulated by using the Eq.(3.5 and 3.6) with the variation of different parameters for n-channel SOI FinFET and shown in the next chapter.

The output characteristics also depend on channel conductance. Hence the channel conductance and transconductance of n-channel FinFET of channel length 90 nm have been simulated and compared to the experimental results. The channel conductance of gate length 85.8 nm FinFET devices has been extracted from the output characteristics and transconductance from the transfer characteristics, and compared with the simulation results of this work.

CHAPTER 4

RESULT AND DISCUSSION

4.1 Introduction

Impact of different gate biases on the mobility characteristics will be studied in this chapter with the help of simulation results. These will illustrate the effects of different gate biases on the mobility and other electrostatic characteristics of the n-Channel FinFET.

The device structure that has been examined is shown in Fig.4.1.The device is a simplified and ultra-scaled version of FinFET. L_{ch} is the channel length or effective channel length (gate length) of 102.2 nm, 85.8 nm and 32 nm are considered, t_{si} is the silicon thickness value of 30 nm, t_{ox} the oxide (SiO_2) thickness of 2 nm and H the fin height of 60 nm. The substrate doping is selected ($N_a = 2\times10^{16}$ cm^{-3}) such that the threshold voltage is practical value.

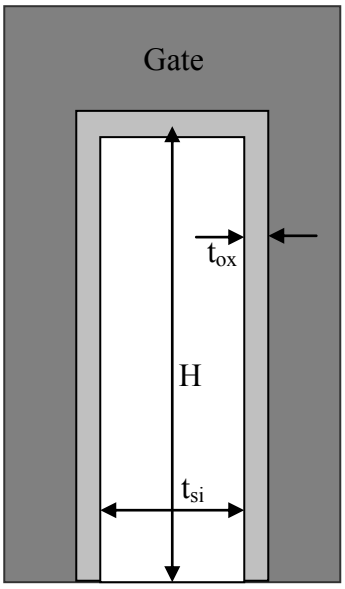

Fig.4.1: Test device of an n-Channel FinFET (Cross section perpendicular to the channel direction).

4.2 Inversion Layer Carrier Concentration

When a positive voltage is applied to the gate of the n-channel FinFET, electrons are induced in the Si- SiO_2 layer. When the gate voltage is increased, carrier concentration also increases. As a result, a channel is formed in between the source and drain through the p-type body or substrate. The device starts to operate when strong inversion is occurred. Concentration of the inversion layer depends upon the gate voltage as well as the drain voltage. The electron concentration in the channel as a function of gate voltage is shown in Fig.4.2 and electron concentration as a function of effective electric field in Fig.4.3 in semi log scale.

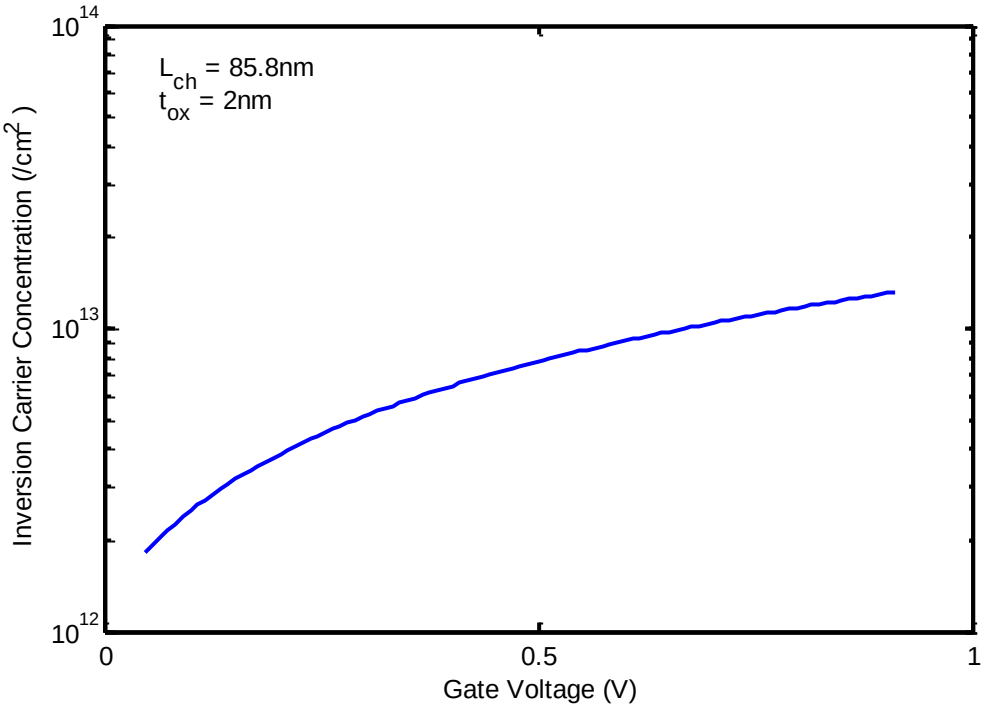

Fig.4.2: Inversion Carrier Concentration versus gate voltage.

From the Fig.4.2, it is seen that the carrier concentration increases with the increase in electric field, i.e., gate voltage. Carrier concentration increases higher at low electric field. This is because the pinch-off occurs and charge remains constant even if the gate voltage is increased beyond the saturation value. At gate voltage 0.5V, the carrier concentration 8×10^{12} cm^{-2} and it varies 3×10^{12} cm^{-2} ~ 10^{13} cm^{-2} for gate voltage 0V ~ 1.0V

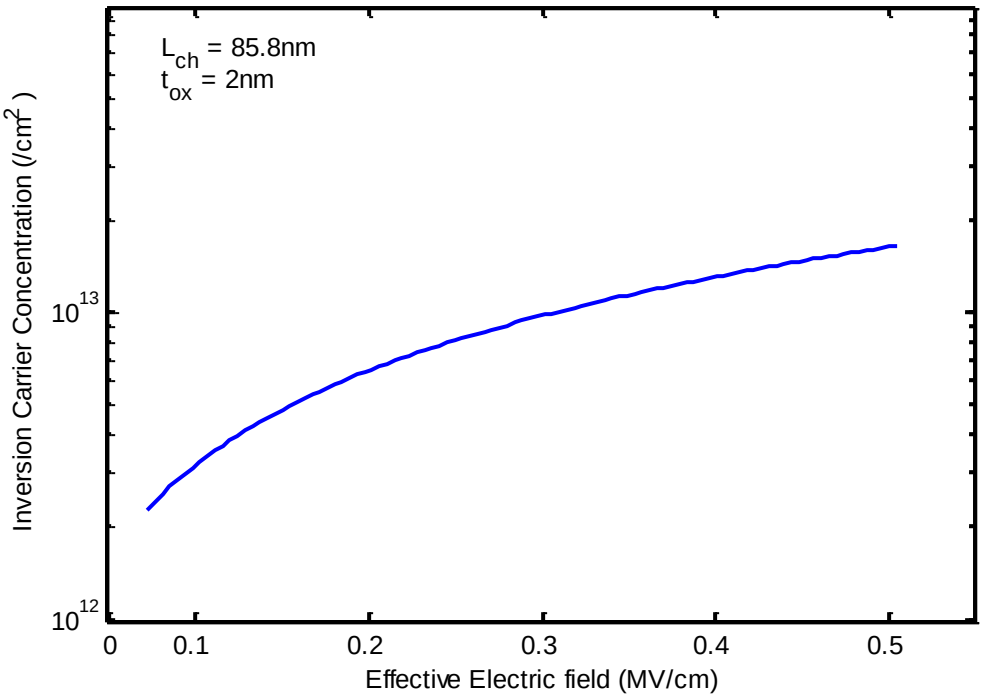

Fig.4.3: Inversion Carrier Concentration versus effective electric field.

4.3 Threshold Voltage Roll-Off

As the dimensions of MOS devices are shrunk, the close proximity between the source and the drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region, and undesirable effects, called the "short-channel effects" start plaguing MOSFETs. The decrease of threshold voltage with decrease in gate length is a well-known short channel effect called the *"threshold voltage roll-off"*. As the channel of the device is reduced to nanoscale region, the charge distribution in the channel is influenced by the field originating from the source/drain. The critical geometry parameters which determine device short-channel behaviors spatially threshold voltage roll-off are gate length, fin thickness, fin height, oxide thickness and channel doping [6]. Threshold voltage fluctuation for channel length reduction can be found by the following expression [26]:

$$\Delta V_{th} = -\frac{qN_a W_m r_j}{C_{ox} L_{ch}} \left[\sqrt{1 + \frac{2W_m}{r_j}} - 1 \right] \tag{4.1}$$

Where r_j is the depth of the source and drain junction, W_m the maximum width of the depletion layer.

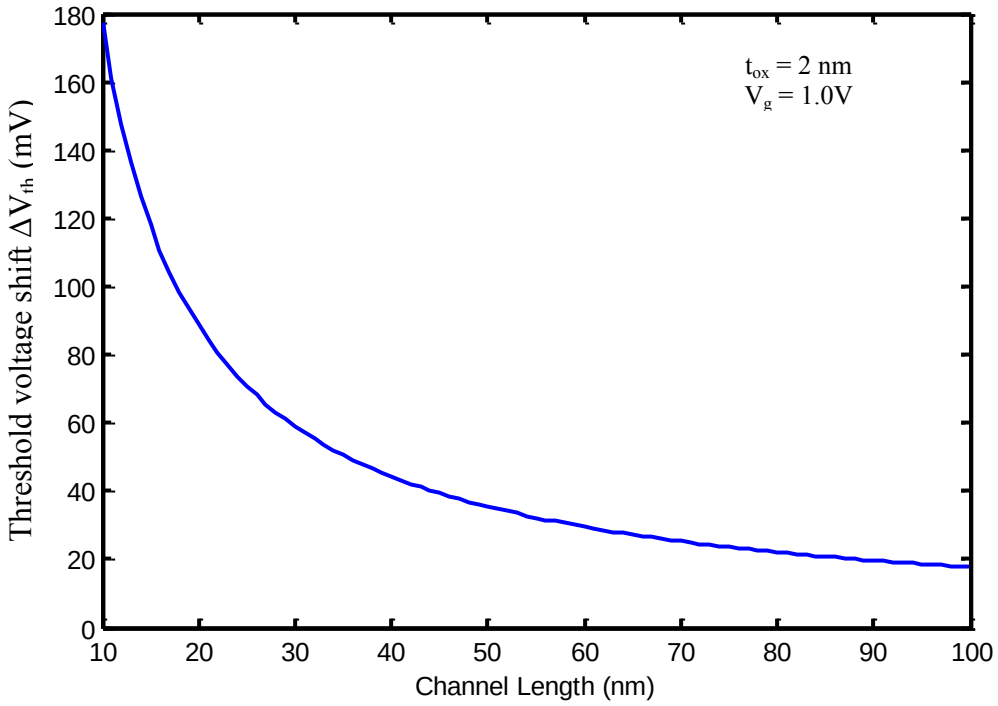

Fig.4.4: Threshold voltage shift (ΔV_{th}) with channel length.

Threshold voltage shift with respect to channel length is shown in Fig.4.4. It is seen that threshold changes sharply above channel length of 60 nm, after this the fluctuation of threshold voltage is comparatively less. Threshold voltage changes due to the reduction of charges in the depletion layer for reduction of channel length. From the Eq.(4.1), threshold voltage roll-off also depends on oxide layer substrate impurity doping concentration (N_a). As the thickness of oxide is decreased, less gate voltage is required for strong inversion. Threshold voltage roll-off can be found by subtracting ΔV_{th} from the threshold voltage, V_{th} as:

Threshold voltage roll-off = $V_{th} - \Delta V_{th}$ (4.2)

Threshold voltage roll-off is shown in Fig.4.5. For shorter channel lengths, the value of threshold voltage reduces.

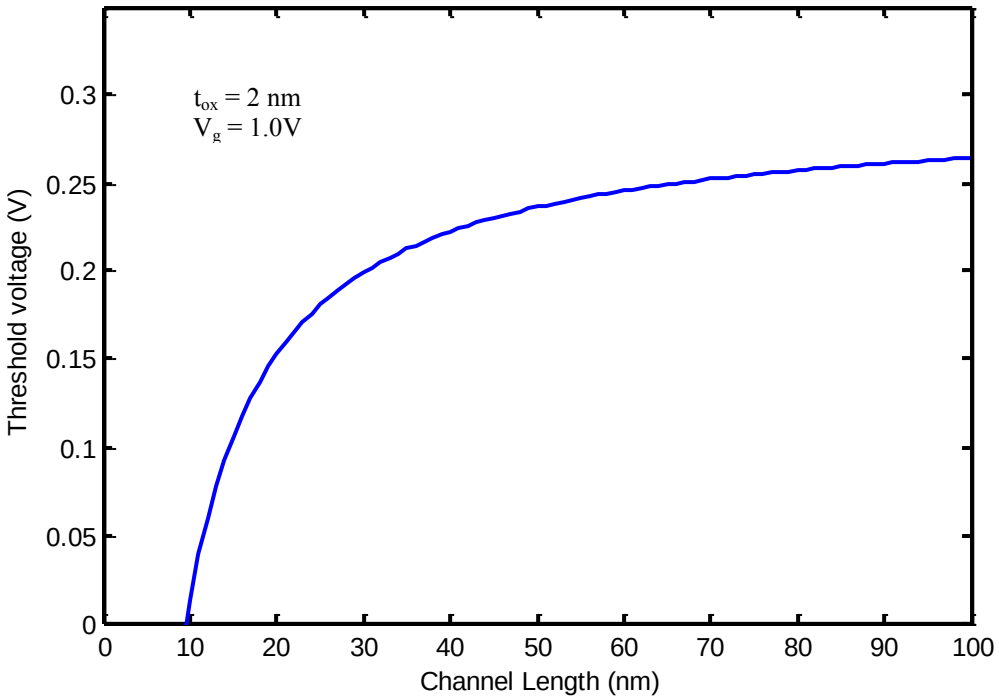

Fig.4.5: Threshold voltage roll-off for nanoscale FinFET.

4.4 Mobility due to Phonon scattering

Figure 4.6 shows the Mobility limited by the Phonon scattering mechanism versus effective electric field. Here mobility due to phonon scattering mechanism decreases gradually with the increase in effective field. Phonon scattering depends on temperature. Mobility limited by the Phonon scattering is very high at lower temperature as shown in Fig.4.7. Phonon scattering also depends on silicon thickness. As silicon thickness is reduced, the phonon limited mobility increases gradually [6]. For the same inversion charge concentration, the phonon scattering rate is greater in thinner films than in thicker ones.

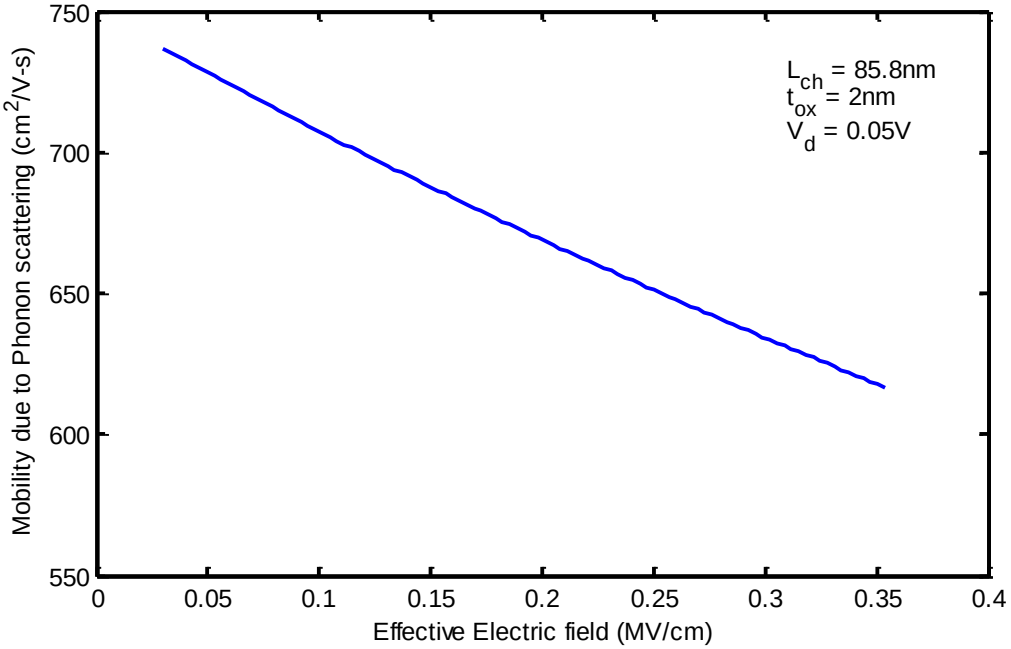

Fig.4.6: Mobility due to Phonon scattering versus Effective Electric Field.

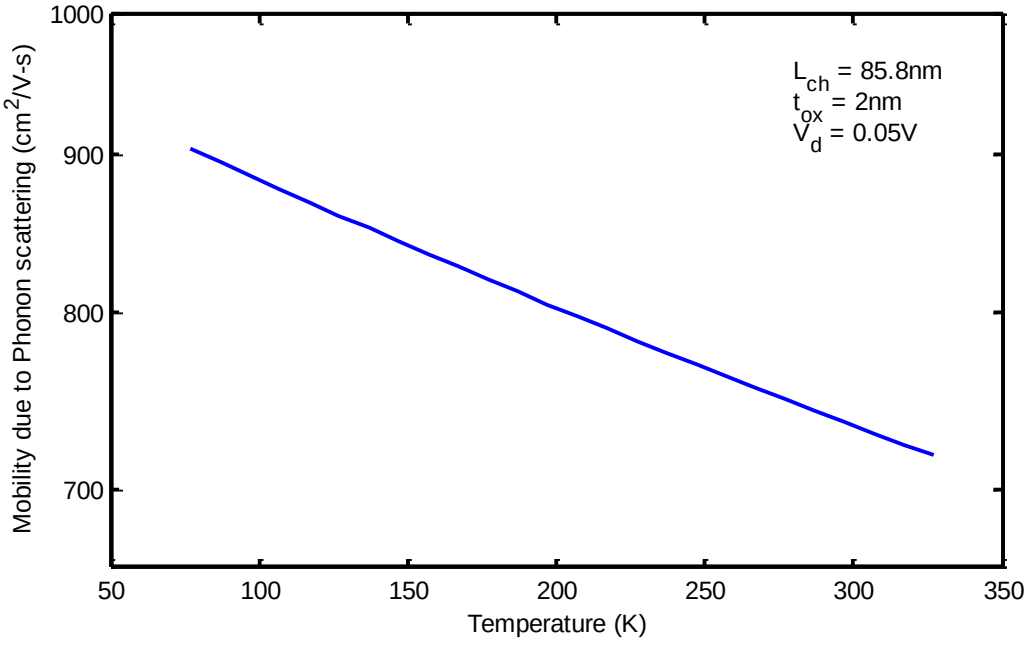

Fig.4.7: Mobility due to Phonon scattering versus Temperature.

4.5 Mobility due to Coulomb scattering

Coulomb scattering occurs due to the substrate doping impurities, interface state densities and charges trapped in gate oxide. The coulomb interaction between the inversion layer electrons and the charges localized near the interface such as interface states or trapped charges become stronger with an increase in N_{inv}, because the average position of electrons approaches the interface more. This effect can compensate the screening effect to some extent and as a result, the N_{inv} dependence becomes weaker. Coulomb scattering as a function of electric field has shown in Fig.4.8. It is seen that at higher electric field coulomb scattering is lower, because the rise in the screening of the charged centers as mobile-carrier density increase. On substrate with higher impurity concentrations, the electron and hole mobilities significantly deviate from the universal mobility curve at lower surface carrier concentrations because of coulomb scattering by the substrate impurity. Coulomb scattering as a function of inversion carrier concentration is plotted in Fig.4.9. Mobility due to Coulomb scattering increases with the increase in $N_{inv.}$

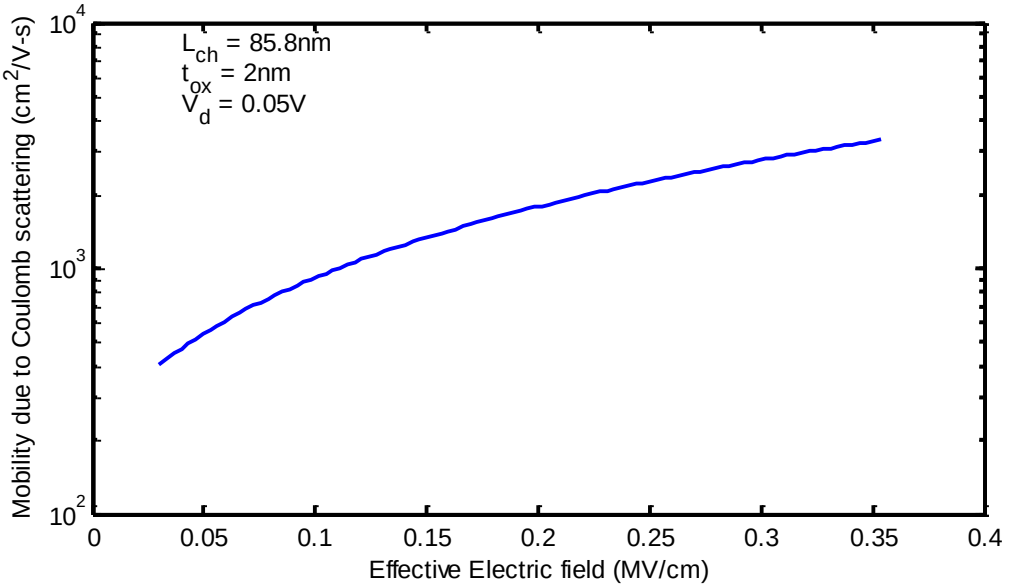

Fig.4.8: Mobility due to Coulomb scattering versus effective electric field.

L_{ch}=85.8nm
t_{ox}=2nm
V_d=0.05V

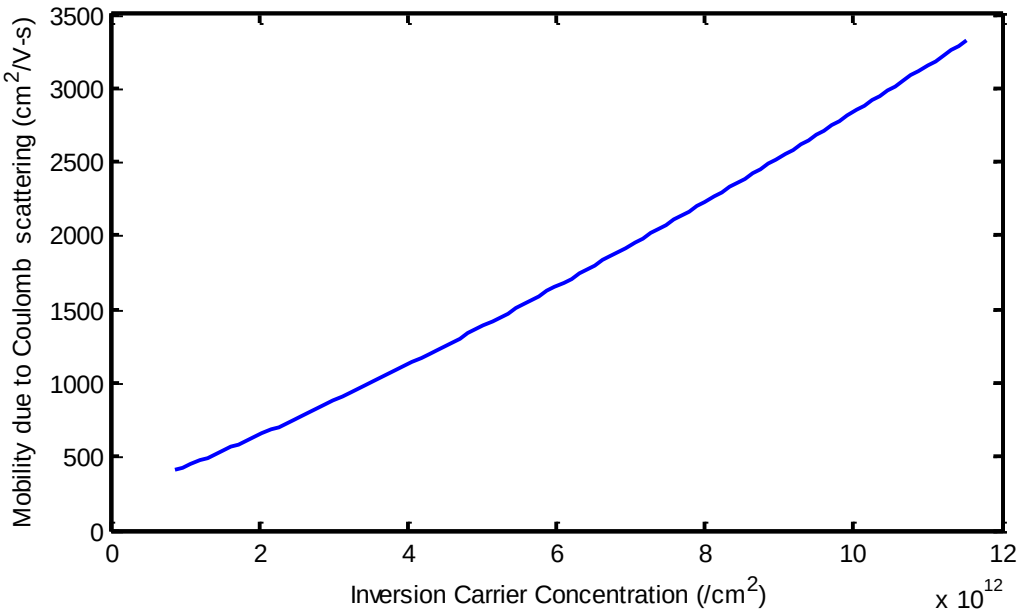

Fig.4.9: Mobility due to Coulomb scattering versus Inversion carrier concentration.

4.6 Mobility due to Surface Roughness scattering

Mobility limited by surface roughness scattering versus effective field is shown in Fig.4.10. It is seen that mobility decreases at higher effective field. This degradation is due to the potential modification due to imperfect interface. These potential modifications produce the electron scattering and consequently degradation in the mobility. The surface roughness scattering is affected by the screening of the mobile electrons in the inversion layer.

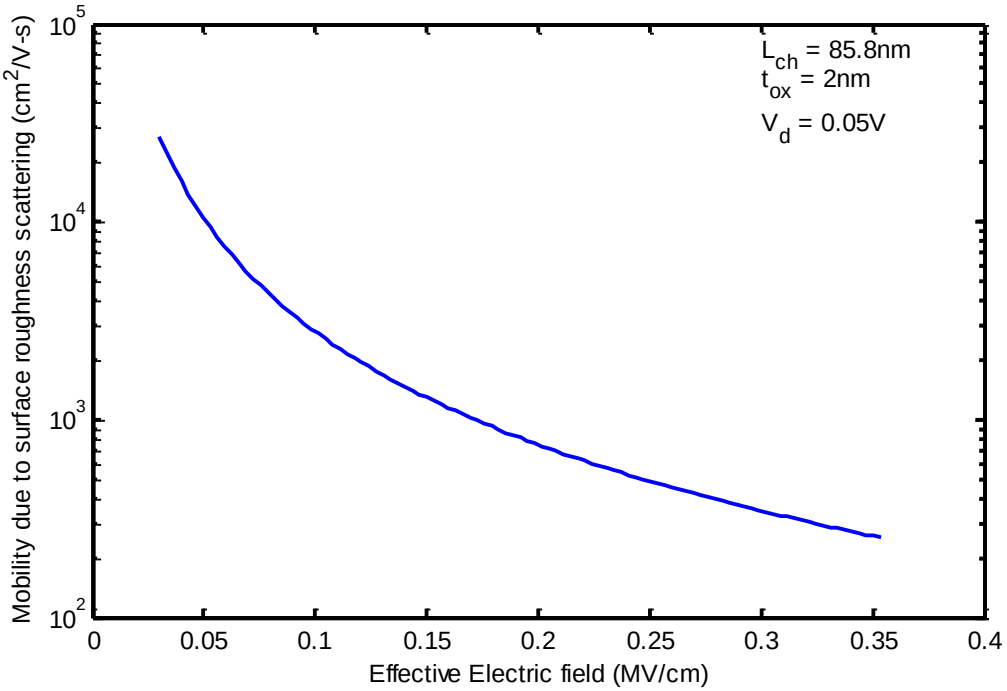

Fig.4.10: Mobility due to surface roughness scattering versus effective electric field.

4.7 Effective Mobility

The effective mobility is obtained considering the phonon scattering, coulomb scattering and surface roughness scattering mechanisms. At the lower value of electric field, coulomb scattering is responsible for the deviation of the effective mobility curve. Because the surface inversion charge concentration is low at this region. As the field increase, charge concentration increases (Fig.4.3), the coulomb scattering increases (Fig.4.9), but the surface roughness scattering and phonon scattering become stronger than coulomb scattering at the higher value of carrier concentration, as the effective field is increased in proportion to the charge concentration. The effective mobility at higher electric field is due to the phonon scattering and surface roughness scattering.

If the nanoscale device physics is not considered in the mobility curve, the mobility is termed as the *ballistic or apparent* mobility. For FinFET with nanoscale channel length, the mobility thus obtained has to be modified. As experimentally observed elsewhere, the mobility extracted from electrical characteristics decreases with the shrinking of the

channel length which has described in Sec.2.4.7. Hence the effective mobility is determined for nanoscale channel length by using the proposed mobility model Eq.3.2 The validity of this model is checked by the transfer characteristics in the next section.

In order to understand the dependency of E_{eff} quantitatively, it is necessary to characterize the mobility curve in terms of scattering mechanism. The dependence of E_{eff} on the basis of a general understanding of the inversion layer mobility is shown in Fig.4.11 and 4.12 by the schematic diagram. The individual and effective mobility curves are plotted as a function of effective electric field. The electric field is a function of gate and drain biases. The electric field is a function of gate voltage as shown in Fig.4.11, when drain voltage is kept constant. Figure 4.12 is plotted when electric field is a function of drain voltage, gate voltage is kept constant. The effective mobility of Fig.4.11 and 4.12 are gradually increases at lower value of effective field. It starts to degrade after the effective field value of 0.1 MV/cm because of the degradation of the mobility due to phonon scattering and surface roughness scattering.

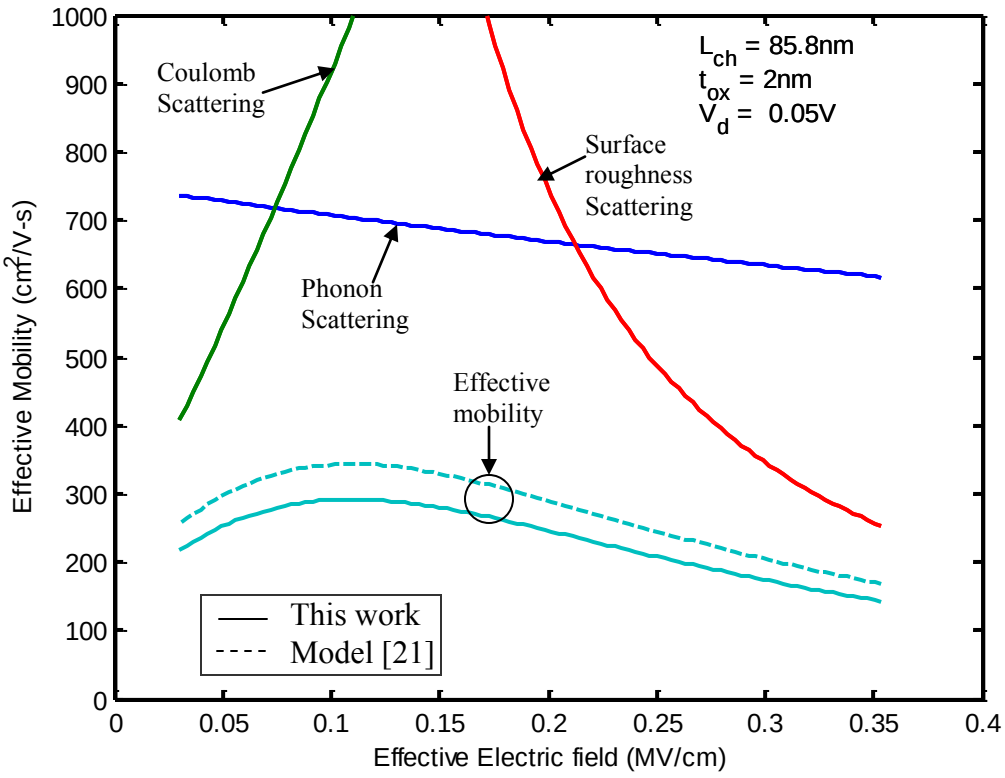

Fig.4.11: Effective mobility versus effective electric field as a function of gate voltage.

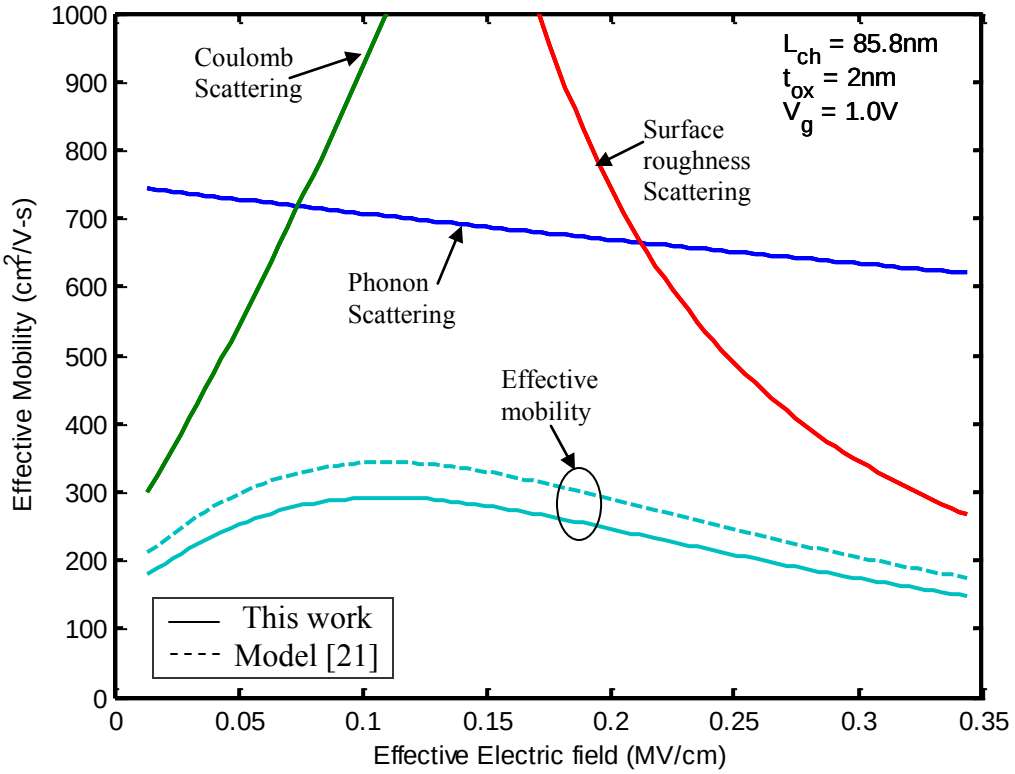

Fig.4.12: Effective mobility versus effective electric field as a function of drain voltage.

The continuous lines of the Fig.4.12 and 4.13 represent the simulation result of the proposed model and the dash lines represent the simulation result of the existing model [21]. The effective mobility of this work is lower than the model [21]. This is because, for the occurrence of some additional scattering phenomena's and some other physical effects not considered in the model [21] as describe previous chapter.

Effective mobility is observed against the inversion carrier concentration as shown in Fig.4.13. It is seen that at comparatively low carrier concentration the effective mobility increases and after this it decreases very sharply. It is the maximum at inversion carrier concentration value of $4*10^{12}$ /cm^2. The continuous curve is for this model and the circle marked line the simulation result by S. Agarwal [44]. The result of this model is nearly in good agreement with the S. Agarwal simulation result.

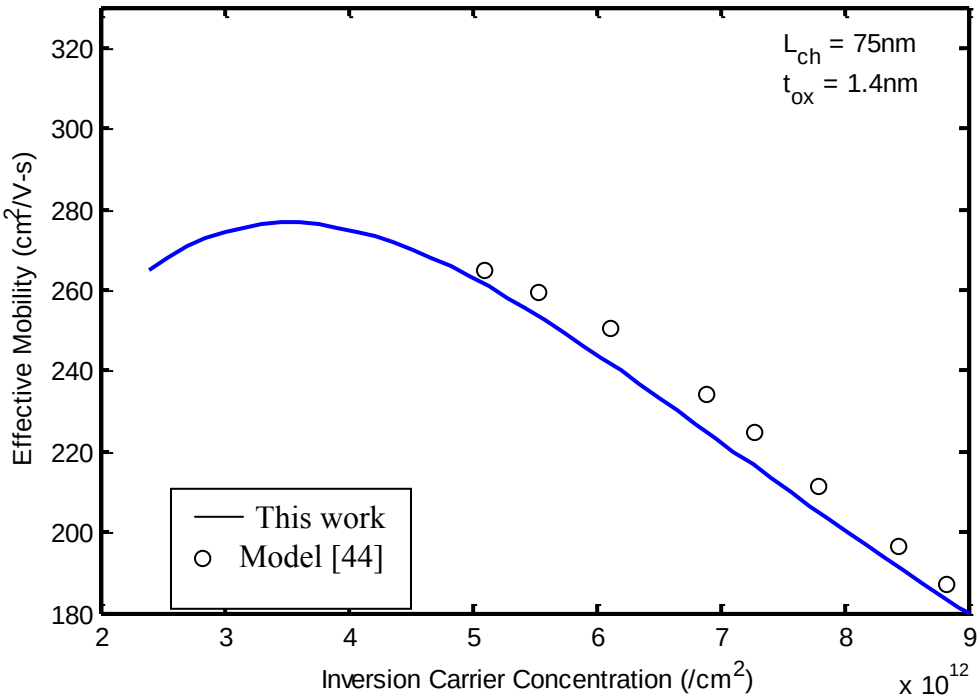

Fig.4.13: Effective mobility versus inversion carrier concentration.

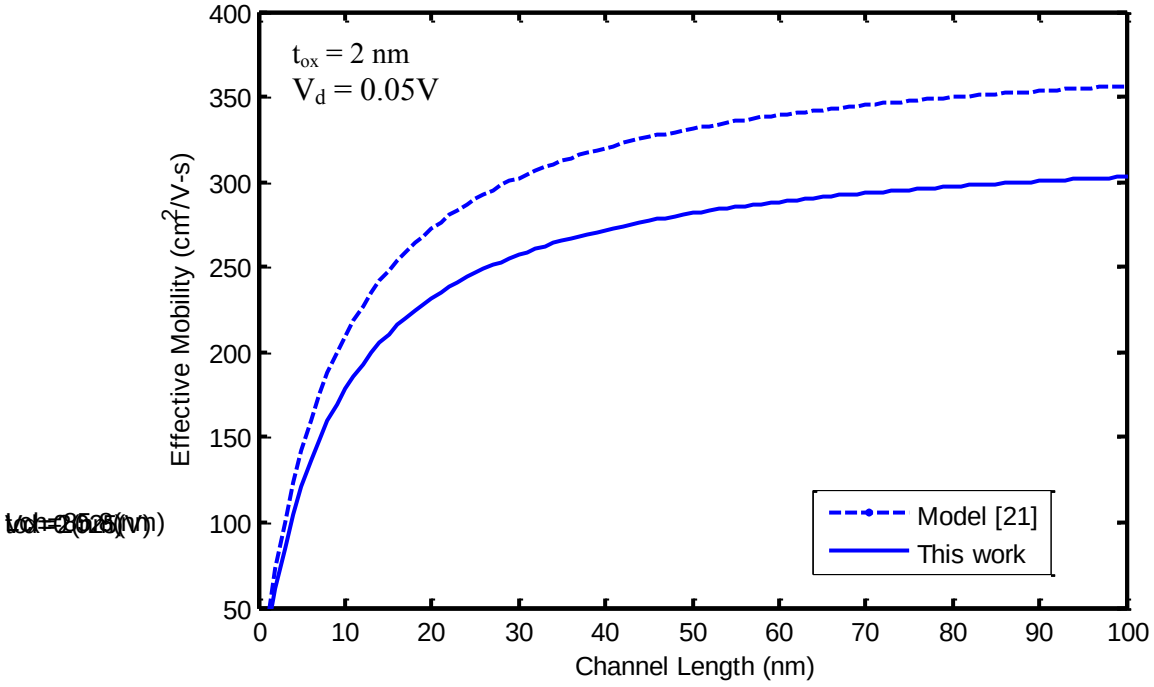

Fig.4.14: Effective mobility versus channel length.

The relationship between the effective mobility and the channel length for n-channel FunFET is observed for channel length 0 ~ 100 nm as shown in Fig.4.14. The effective mobility decreases with the decrease in channel length and the mobility degradation rate is lower beyond 60 nm. The effective mobility represents by the dash line for model [21] is higher than the result of this work.

The effective mobility has been shown in Fig.4.15 for the channel lengths of 102.2nm, 85.8nm, 70nm and 32nm with respect to effective field. It is seen that the effective mobility curve shifts downward for shorter channel length.

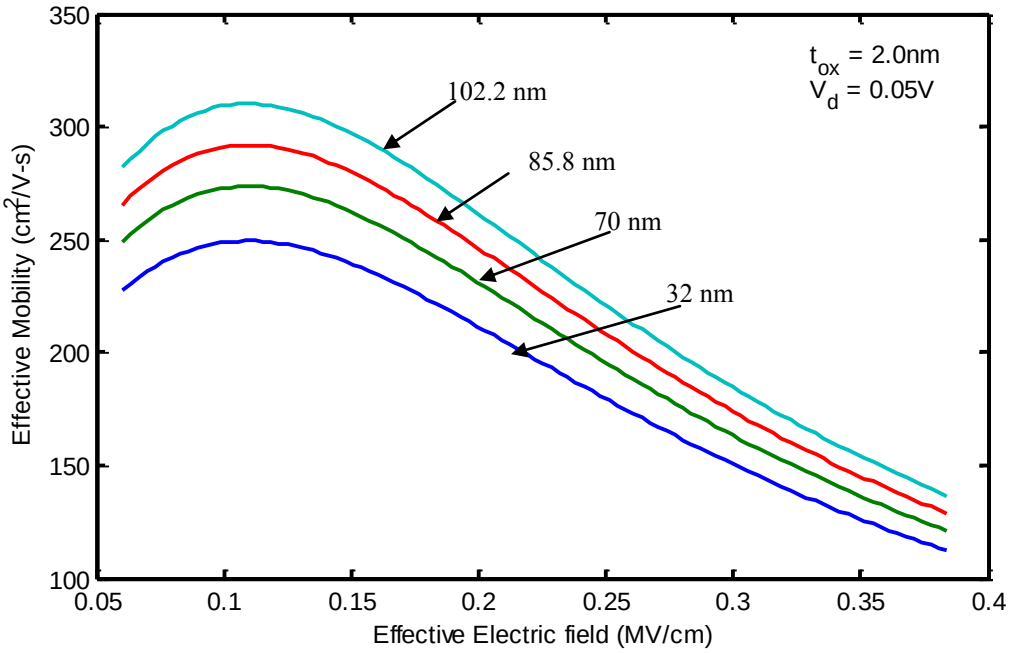

Fig.4.15: Effective mobility versus effective electric field.

4.8 Current-Voltage Characteristics

The drain current is directly proportional to the mobility. Mobility depends on the effective electric field in the inversion layer and effective field is created by the applied gate voltage and drain voltage. The transfer characteristics or I_D-V_G characteristics and the output characteristics or I_D-V_D characteristics will be described in this section.

4.8.1 Transfer Characteristics (I_D-V_G)

If there is no voltage at the gate, the source and drain region are separated by reverse biased pn junction, and no current flow between the source and drain of the device (the off impedance is normally of the order of thousands of mega ohms). When gate voltage is increased, the charges in the inversion layer increase and as a result the electric field increases. The effective mobility increases with the increase in gate voltage is shown in Fig.4.16. At the higher value of gate voltage effective mobility curve degrades due to the phonon and surface roughness scattering. The continuous line represents the simulation result of the proposed model and the dash line represents the simulation result of the existing model

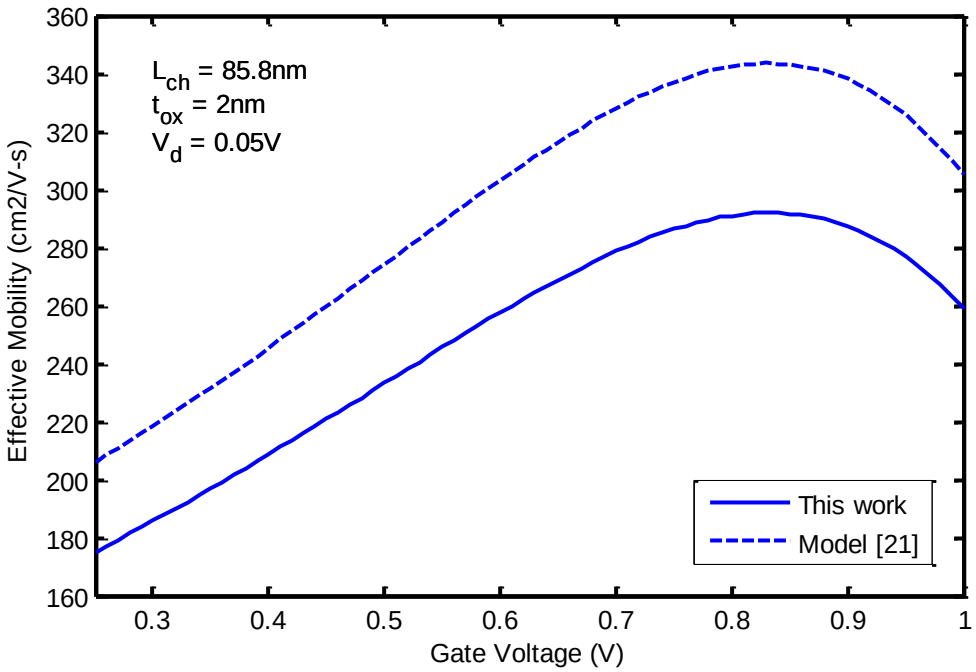

Fig.4.16: Effective mobility versus gate voltage.

The drain current versus gate voltage are shown in Fig.4.17. The continuous lines for this work and the circles represent the experimental results obtained by J. Song et al [20]. Drain current are plotted for 50mV and 1.0V of drain voltages and compared with the experimental data. It is seen that the transfer characteristics lies very close to the experimental results both for low and high drain voltages. The drain current versus gate voltage in semi log scale is shown in Fig.4.18.

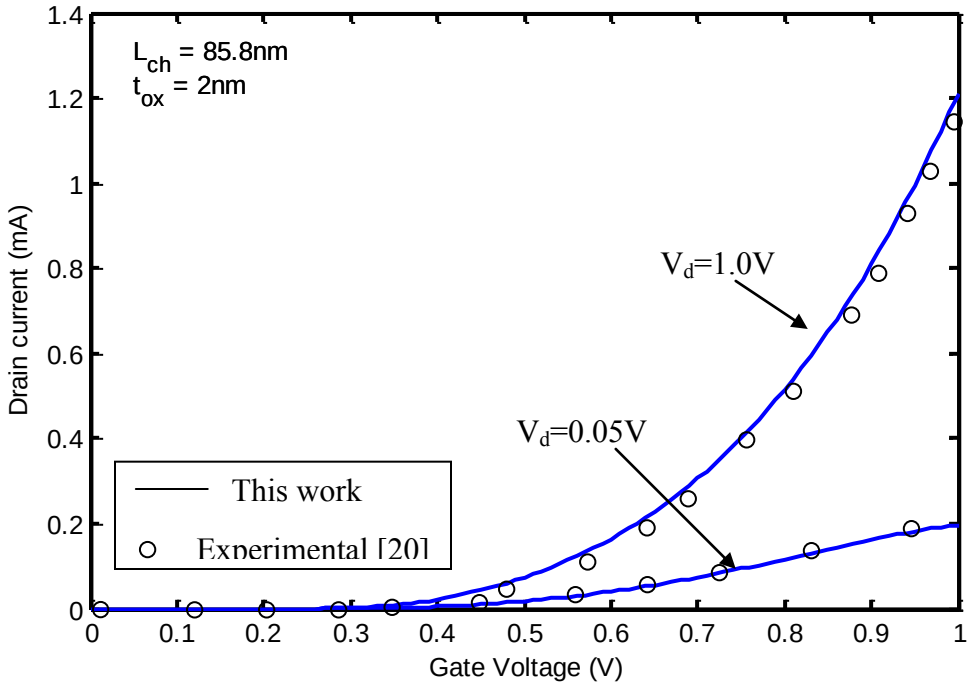

Fig.4.17: Drain current versus gate voltage.

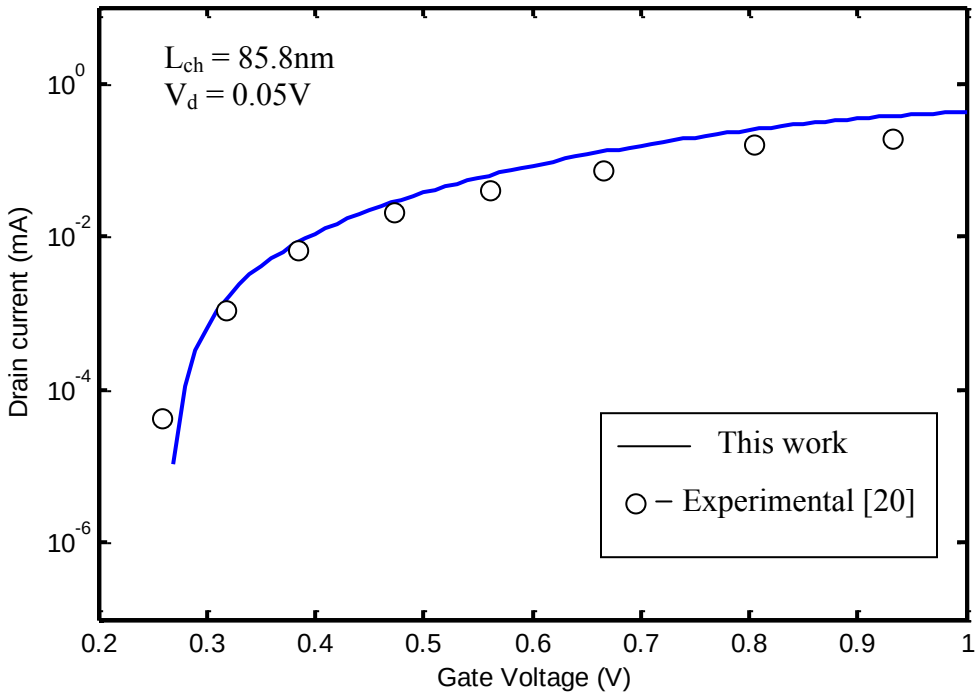

Fig.4.18: Drain current versus gate voltage in semi log scale.

4.8.2 Effect of Drain Voltage

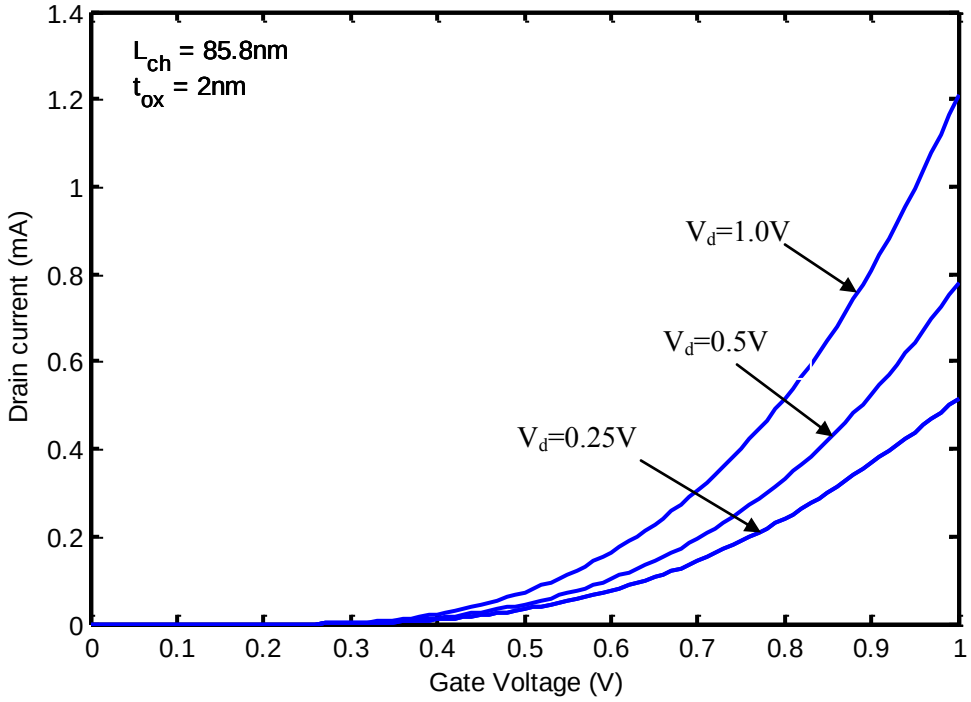

Fig.4.19: Effect of drain voltage on drain current versus gate voltage.

The effect of drain voltage on drain current versus gate voltage is shown in Fig.4.19. Drain currents for drain voltages of 1.0V, 0.5V and 0.25V are plotted with a channel length of 85.8nm. As the drain voltage is increased drain current also increases.

4.8.3 Effect of Oxide Thickness

The effect of oxide thickness on drain current versus gate voltage is plotted in Fig.4.20. It is seen that when the oxide thickness is increased, the drain current decreases and the curves move downward. This is because, the oxide capacitance increases with the decrease in oxide thickness and the oxide capacitance is directly proportional to the drain current.

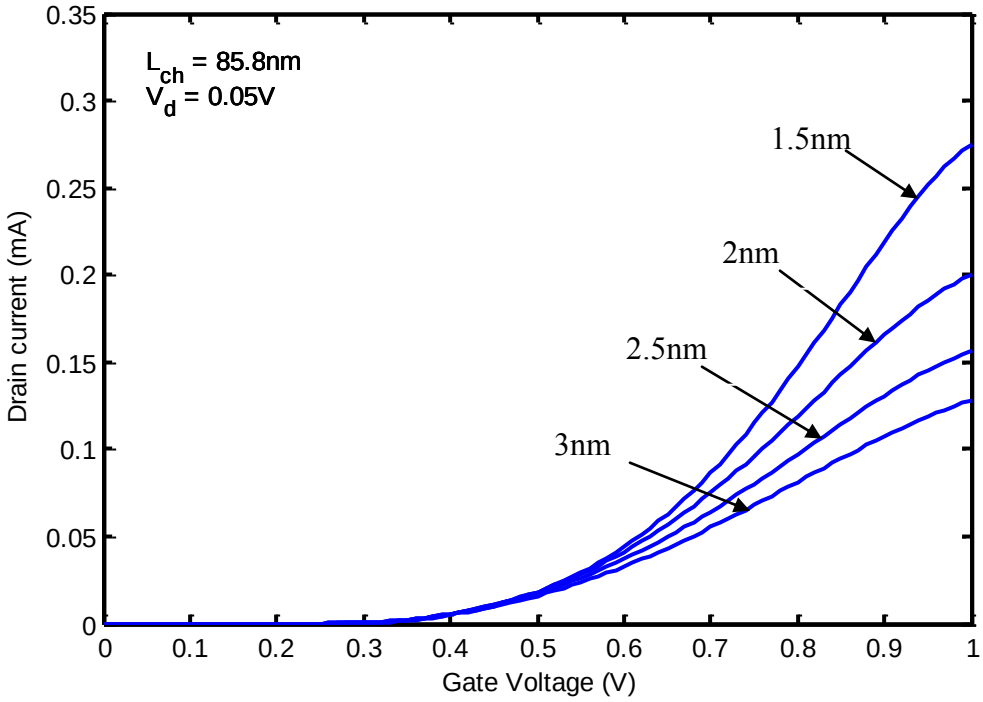

Fig.4.20: Effect of oxide thickness on drain current versus gate voltage.

4.8.4 Effect of Channel Length

As described previous chapter with mathematical expression is that the effective mobility strongly depends on the device channel length. Hence the drain current varies with the variation of the channel length. Drain current versus gate voltage is plotted against different channel length in Fig.4.21. As the channel length is reduced voltage required to turn on the device is less and hence current increases.

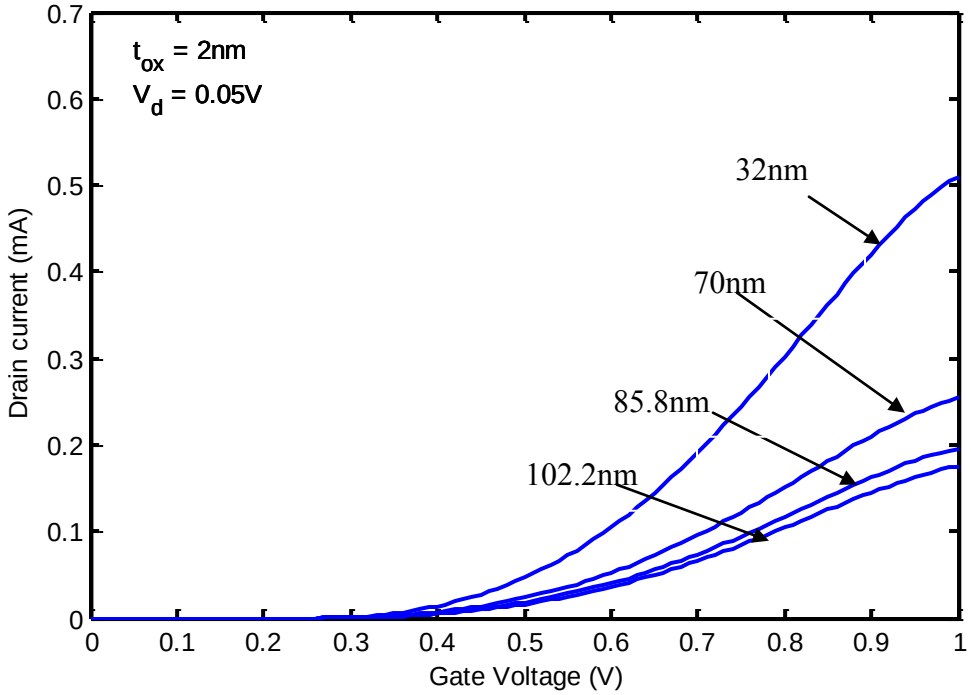

Fig.4.21: Effect of channel length on drain current versus gate voltage.

4.9 Output Characteristics (I_D-V_D)

The effective mobility of the inversion layer is plotted against the drain bias in Fig.4.22. Scattering of carriers at low drain voltage is very low which plays an important role in the device on-sate current. As the drain voltage is increased, the carrier scattering becomes stronger and the mobility due to carrier scattering is limited. The continuous line represents the simulation result of this work and the dash line represents the simulation result of the existing model

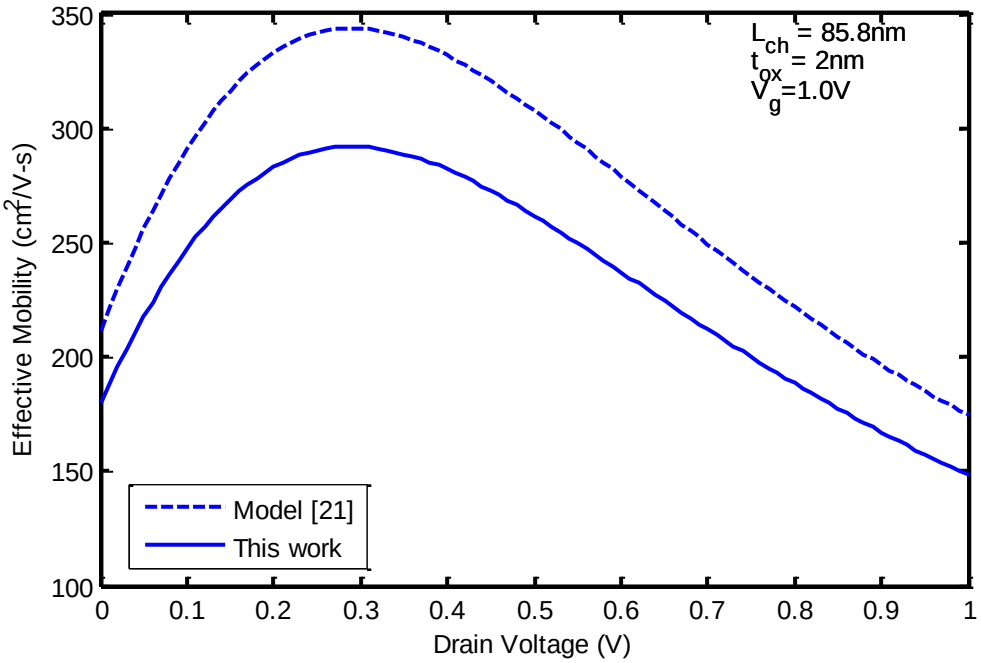

Fig.4.22: Effective mobility versus drain voltage.

The drain current versus drain voltage of channel length 85.8 nm FinFET with oxide thickness 2 nm is plotted in Fig.4.23. The continuous lines indicate the simulation result of this work and the symbols represent the experimental result obtained by J. Song et al. [20]. The Fig.4.23 shows a very good agreement of the drain current of this model with the experimental result. The effect of gate voltage on the output characteristics has also observed. It is seen that as the gate voltage is decreased, the drain current curves move downward. The saturation current increases at higher gate bias.

The output characteristic in semi log scale is plotted in Fig.4.24. The threshold voltage is at the point in the curve where the current I_D changes sharply and its value of 0.265V.

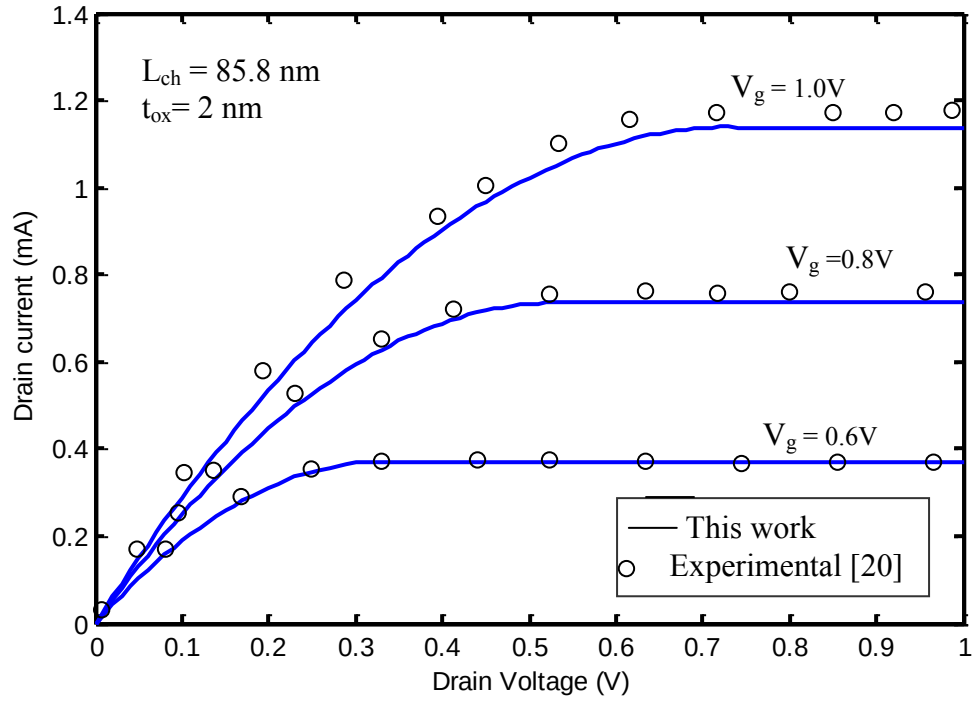

Fig.4.23: Drain current versus drain voltage.

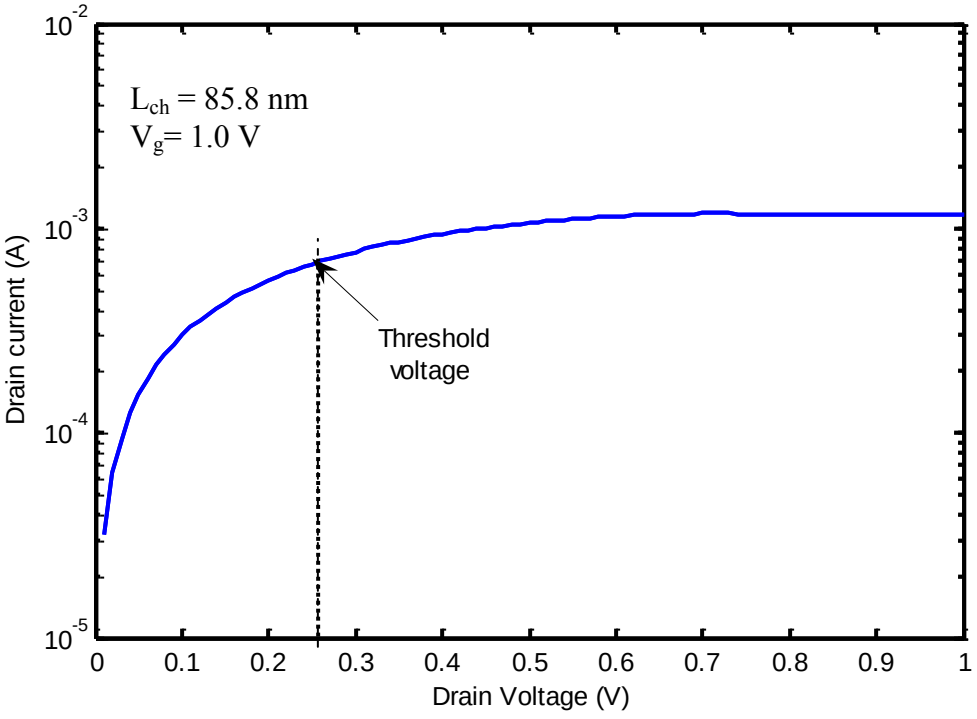

Fig.4.24: Drain current versus drain voltage in semi log scale.

4.9.1 Effect of Channel Length

The effect of channel length on drain current versus drain voltage is plotted as shown in Fig.4.25. As the channel length is decreased, the drain current increases. Here the degradation of effective mobility with channel length is considered. Drain currents are plotted for channel length value of 32 nm, 50 nm, 85.5 nm and 102.2 nm. The saturation drain current for shorter channel length is higher as shown in Fig.4.26. Here drain current is plotted against channel length. For the same dimensions the saturation current can be determined for a wide range of channel length.

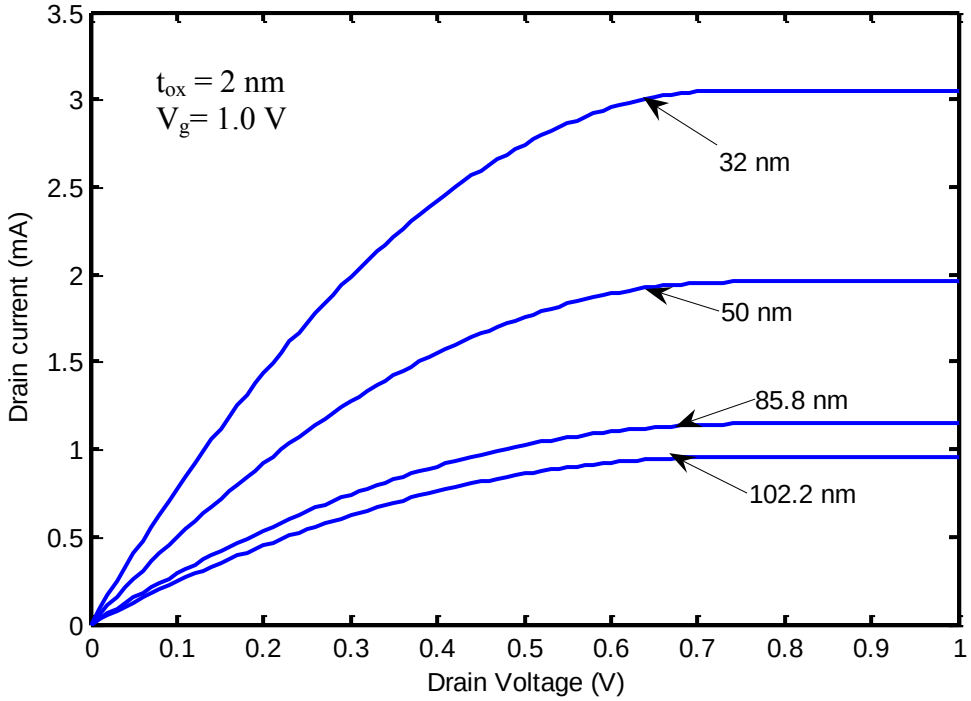

Fig.4.25: Effect of channel length on output characteristics.

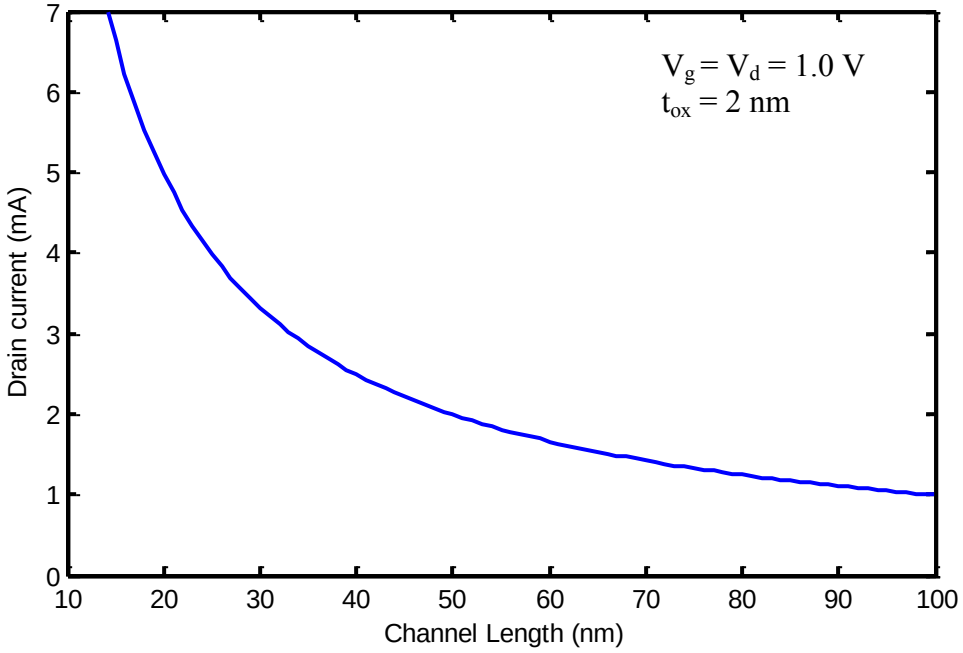

Fig.4.26: Saturation drain current versus channel length.

4.9.2 Effect of Oxide Thickness

Effect of oxide thickness on output characteristics is observed for n-channel FinFET of channel length of 85.5 nm. It is seen that from the Fig.4.27, drain current is highly dependent on oxide thickness. As the oxide thickness decreases more charges are gathered in the Si/SiO_2 interface. So the inversion layer charge concentration increases, resulting an increase in drain current.

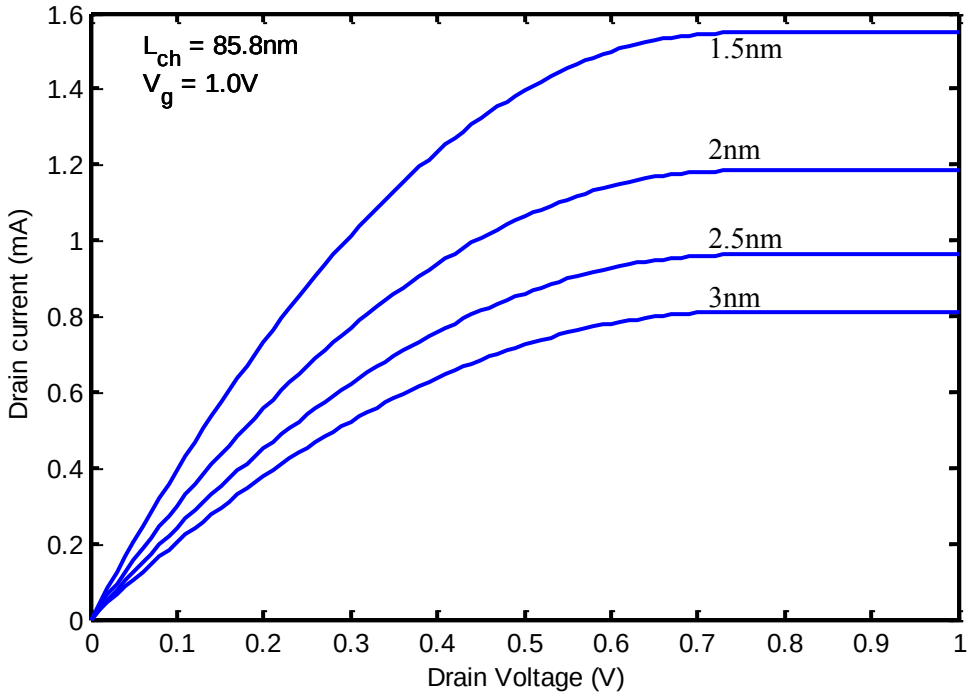

Fig.4.27: Effect of oxide thickness on output characteristics.

4.10 **Channel Conductance**

The channel conductance of MOSFET is defined by the following expression [32]:

$$g_d = \frac{W_{eff}\ \mu_{eff}\ C_{ox}}{L_{ch}}\left(V_{gs} - V_{th}\right) \tag{4.3}$$

The transfer characteristics of a FinFET device gate length of 90nm is simulated and compared with the experimental result. The other dimensions of this device are available in the literature [6].

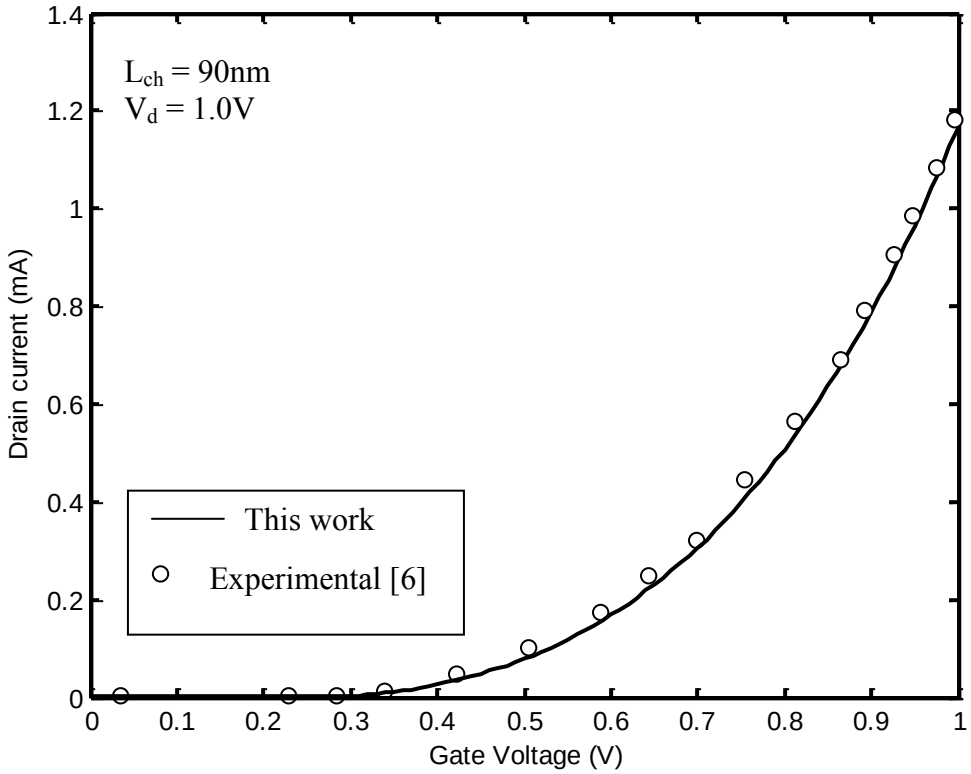

Fig.4.28: Darin current versus gate voltage of 90 nm gate length FinFET.

The channel conductance or output conductance is observed with respect to drain voltage. The channel conductance versus drain voltage curve is shown in Fig.4.29 in semi log scale. When gate voltage, V_g is larger than V_{th}, channel inversion charge density increases, which increases the channel conductance. At saturation, the increment of channel conductance at the drain becomes zero, which means that the slope of I_D versus V_D curve is zero. Hence at this region conductance remain constant.

The channel conductance is plotted for channel length of 85.8nm in Fig.4.30 and compared with the extracted value from the out put characteristics observed by J. song et al [20]. It is seen there is a good agreement between the model and extracted results.

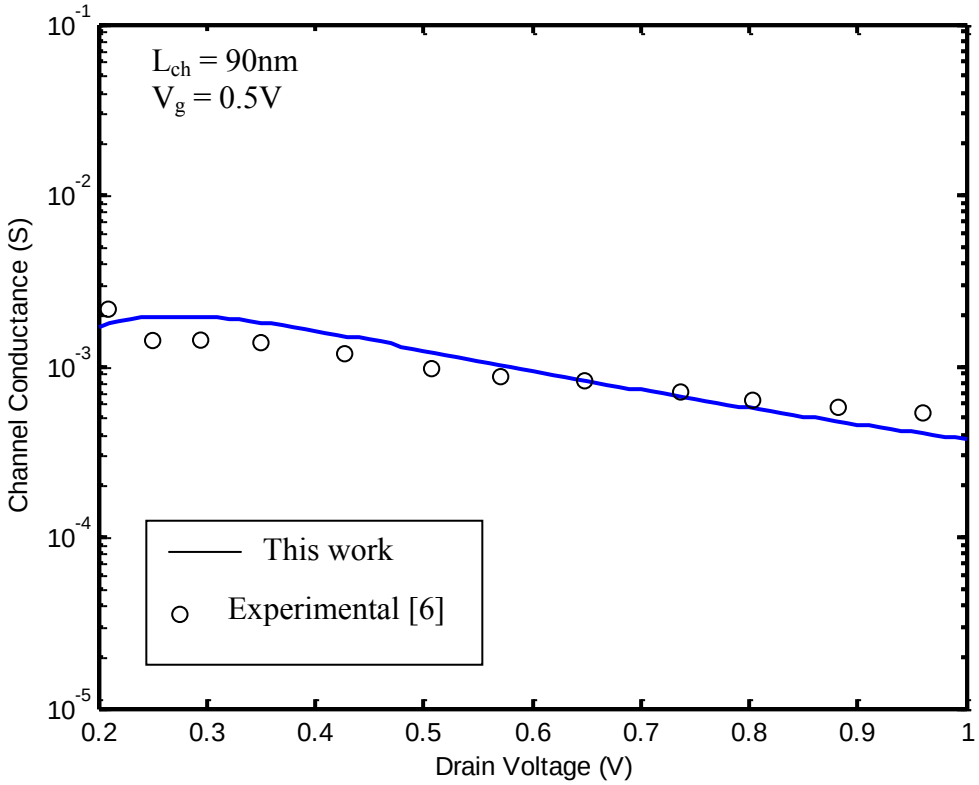

Fig.4.29: Channel conductance versus drain voltage of 90 nm gate length FinFET.

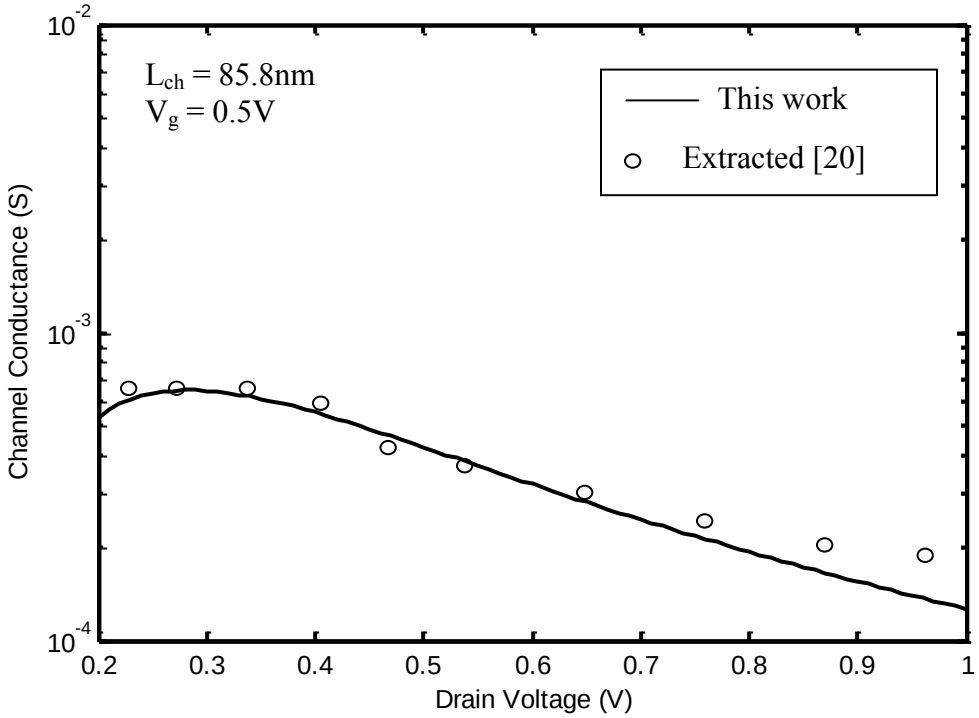

Fig.4.30: Channel conductance versus drain voltage of 85.8 nm gate length FinFET.

4.11 **Transconductance**

The MOSFET transconductance is defined as the change in drain current with respect to the corresponding change in gate voltage. The transconductance for an n-channel MOSFET operating in the linear region is given as [26]:

$$g_m = \frac{W_{eff}\ \mu_{eff}\ C_{ox}}{L_{ch}} V_{ds} \tag{4.4}$$

The transconductance for the saturation region can be found as [26]:

$$g_m = \frac{W_{eff}\ \mu_{eff}\ C_{ox}}{L_{ch}} \left(V_{gs} - V_{th}\right) \tag{4.5}$$

The transconductance of n-channel FinFET of channel length 90 nm versus gate voltage is plotted in Fig.4.31. Here the drain voltage is kept constant for both the linear and saturation regions in order to observe the effect of effective mobility. As the effective mobility increases linearly with the increase in gate voltage as shown in Fig.4.16, transconductancs also increases. At higher value of gate voltage, effective mobility decreases hence transconductancs also decreases. The transconductance for channel length 85.8 nm versus gate voltage is simulated in Fig.4.32 and compared with the extracted value from the transfer characteristics observed by J. song et al [20]. It is seen that there is a good agreement between the model and extracted results.

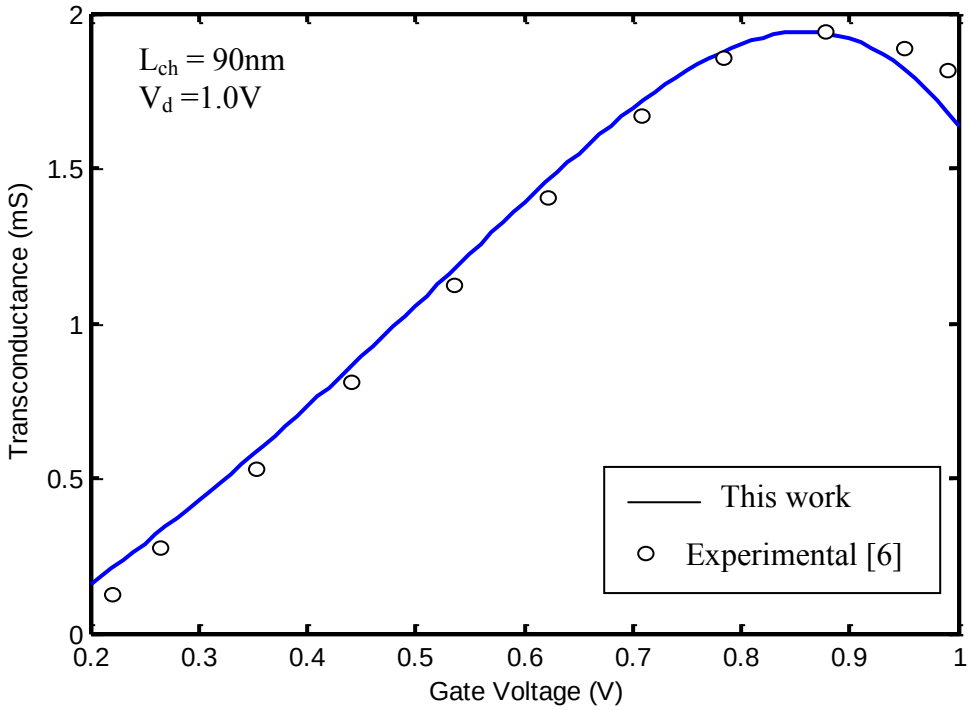

Fig.4.31: Transconductance versus gate voltage of 90 nm gate length FinFET.

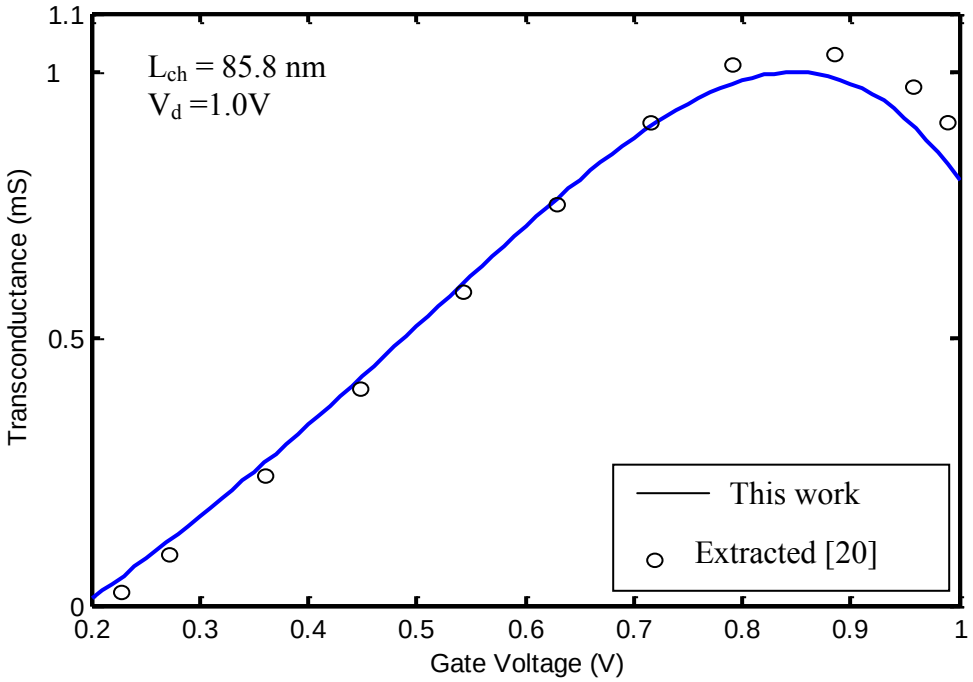

Fig.4.32: Transconductance versus gate voltage of 85.8 nm gate length FinFET.

4.12 Validity of the Model

In order to test the validity of the proposed model, three n-channel FinFET devices with channel length of 32 nm, 85.8 nm and 102.2 nm are simulated. The other dimensions of 32 nm devices are available at S. Agarwal [44]. The device dimensions of 85.8nm and 102.2 nm are same as described in Sec. 4.1. Since the dramatic reduction of effective mobility with decreasing the channel length as describe in previous chapter, the "Mathiessen-like" expression [21] can not accurately define the mobility degradation. The actual mobility degradation is larger than the value defined by this expression. For this compensation, a parameter p is introduced to the "Mathiessen-like" expression Eq. (3.1). The validity of this modification is observed by the transfer characteristics of the above mentioned three devices. The transfer characteristics of 85.8 nm, 102.2nm and 32nm FinFETs are plotted in Fig.4.33, 4.34 and 4.35 respectively. In these figures, the continuous curves are the results of this work, the circle marked curve are the experimental and/or simulation results and the triangles represent the simulation results using the model without fitting parameter [21]. It is seen that there are quite deviation between the experimental data and the results of without fitting parameter in Fig.4.33 and 4.34. Similarly, the simulation result of this work is compared with simulation result for channel length of 32 nm in Fig.4.35 and also found the deviation between the simulation result obtained by S. Agarwal [44] and the results of without fitting parameter. The values of p are taken as 0.704, 0.85 and 0.904 for the channel length of 32 nm, 85.8 nm and 102.2 nm respectively. As the channel length increases the value of p tends to unity, i.e., the influence of p becomes less. This means that the less degradation of mobility, which is required. Hence from these observations, the value of the fitting parameter p can be selected as 0.7~0.9, is valid for the channel length range of 30nm~100nm.

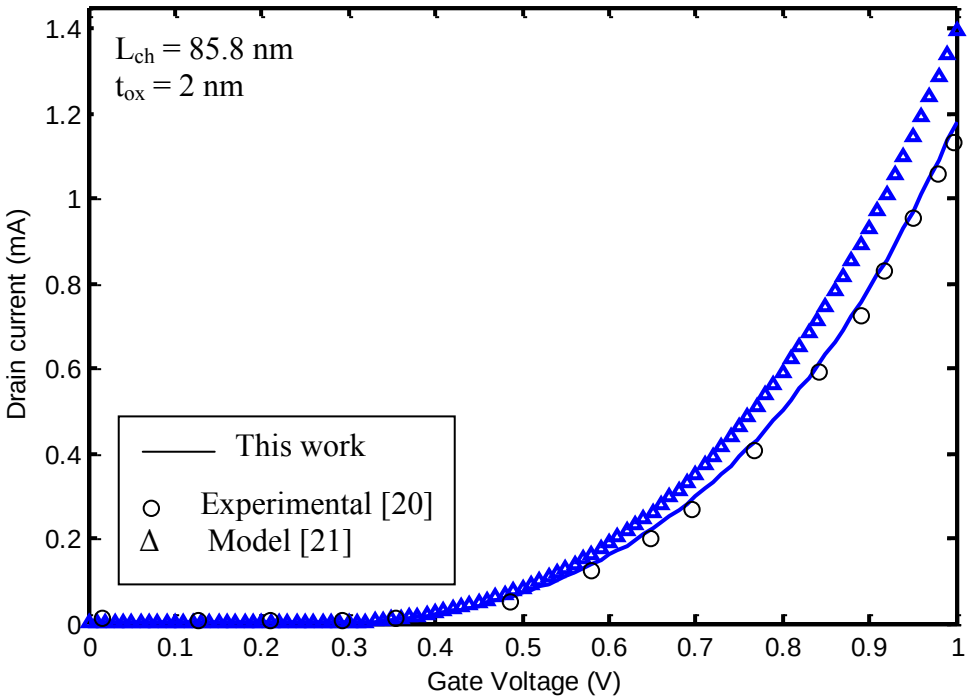

Fig.4.33: Effect of fitting parameter of effective mobility on drain current for 85.8 nm n-channel FinFET.

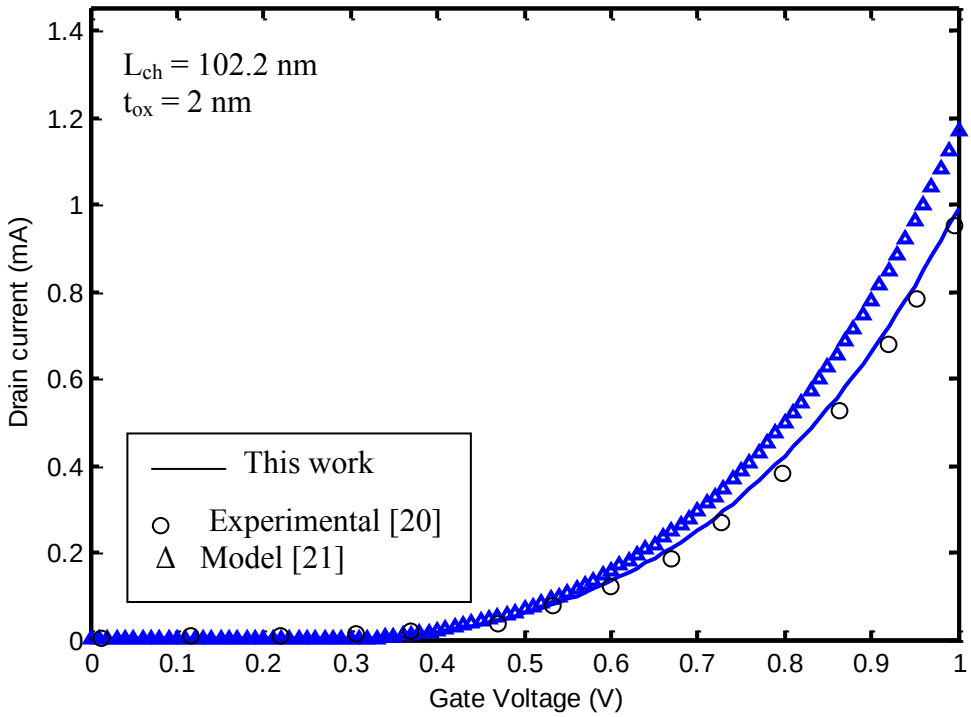

Fig.4.34: Effect of fitting parameter of effective mobility on drain current for 102.2 nm n-channel FinFET.

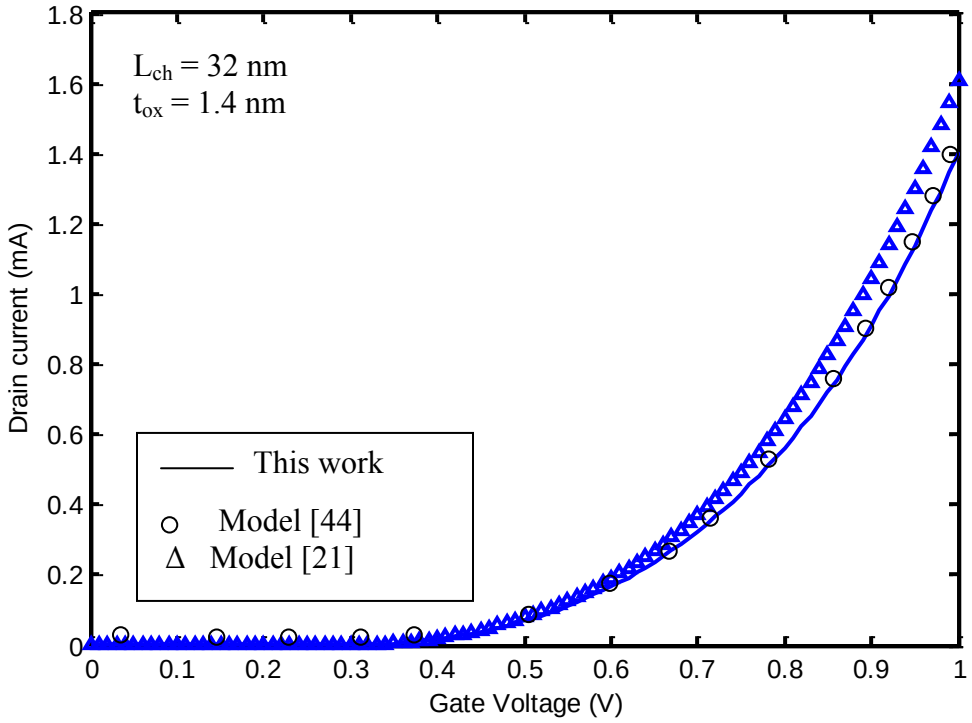

Fig.4.35: Effect of fitting parameter of effective mobility on drain current for 32 nm n-channel FinFET.

CHAPTER 5

CONCLUSION

5.1 Summary

As the dimension of CMOS devices is scaled down to several tens of nanometers in gate length, FinFET presents an effective solution to controlling the short channel effect. This thesis shows a simple approach of drain current model by considering the carrier transport mechanisms in terms of effective mobility in inversion layer of SOI FinFET.

The effective mobility in the inversion channel for nanoscale n-channel FinFET was simulated with respect to effective electric field by considering phonon scattering, coulomb scattering and surface roughness scattering mechanisms as the function of gate bias and drain bias. The effective mobility was observed with respect to the channel length and it was found that it decreases with the decrease in channel length. Hence the effective mobility was modeled for nanoscale channel length by using the "Mathiessen-like" relationship with some modification for better result.

The short-channel behaviors spatially threshold voltage roll-off was investigated with respect to channel length and it was found that threshold changes sharply above channel length of 60 nm, after this the fluctuation of threshold voltage is comparatively less.

The device studied with extremely scaled channel lengths (102.2nm, 90nm, 85.8nm, 70nm, 32nnm) and oxide thickness (1.4nm to 3nm). A good fit is obtained with the available experimental and/or simulation results for the subthreshold, linear and saturation regions of the I-V and other electrostatic characteristics. The validity of this model was done and specified the modification parameter range 0.7~0.9 for the channel length range of 30nm~100nm. The analytical expressions derived in the present model can be a useful tool in device design and optimization.

5.2 Recommendation for Future Works

In this work, three scattering mechanisms were considered for effective mobility measurement. Other scattering mechanism can be included to this model. The scattering mechanisms can be classified into the phase breaking scattering and the coherent scattering mechanism. The phonon scattering considered in this work is one of the phase breaking scattering mechanisms, whereas the coulomb scattering and surface roughness scattering are coherent scattering mechanisms. The remote surface roughness can be considered to the mobility modeling, specially when the oxide thickness is less than 2nm. As a SOI devices silicon-thickness fluctuation-induced scattering ($\mu_{\delta tsi}$) can also be included for silicon thickness is less than 4nm.

The effect of strain and crystal orientation can be included to enhance the performance of the device. The C-V characteristics can also be studied for further improvement of this model.

To further development of this model, other realistic effects can be accounted, such as quantum mechanical effects (gate leakage, inversion layer quantization, and quantization due to structural confinement in case of ultra-thin fins), parasitic series resistance, junction leakage, gate induced drain leakage (GIDL), 3D parasitic effects that are especially severe in FinFETs, gate resistance models for accurate RF simulations, velocity overshoot.

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