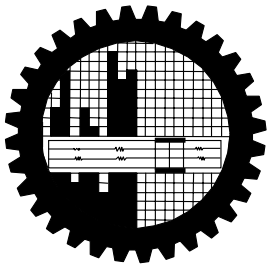
QUANTUM MECHANICAL MODELING AND IMPLEMENTATION OF SINGLE ELECTRON TRANSISTOR CIRCUIT

A thesis submitted to the Department of Electrical and Electronic Engineering of Bangladesh University of Engineering and Technology in partial fulfillment of the requirement for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

by

Mohammad Riazur Rahman Mazumder



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DEDICATION

To My Parents,

To my wife Bushra and our dearest Nehan

Acknowledgement

I am grateful to the Almighty Allah for giving me the strength, courage and potentiality to complete this thesis.

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Abstract

Different models of nano-electronic quantum device Single Electron Transistor (SET) are studied in this work, a modified macro model is proposed and at the end its application in a communication circuit is presented. In the modified macro model it is shown that an inherent problem in the earlier model like unwanted DC offset has been successfully eliminated. I-V characteristics curve of the SET has been studied very closely with the modified macro model. It is shown that how coulomb oscillation of SET can be used to form variable transconductance region of operations. The variable transconductance region of SET consists of a positive and a negative part and a new phenomenon named 'negative transconductance' is observed which is very unique to SET. It is also described how to bias a circuit to achieve that condition with the operating principle described, a phase modulator circuit is proposed in this work which utilizes negative transconductance. The circuit exploits the unique characteristics of SET of having bi-polar transconductance for the proper operating point. The biasing of the circuit is the one of the most critical parts since the region of operation is very narrow. Different biasing conditions are also discussed for the SET bases phase modulator circuit. Since almost every form of communication signal handing systems always convert the original signal to a modulated signal for further processing and increase gain of the transmitted signal, Phase modulator is one of the most common of all elementary communication circuit configurations. The SET based digital signal phase modulator circuit proposed in this work is the most simplified for such circuits used so far. It is seen from the simulation data that SET based digital signal phase modulator circuit performs very efficiently to convert digital pulse to modulated signal.

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List of Symbols

m_0 electron effective mass
ϵ dielectric constant
e charge of an electron
d barrier thickness
μ electrochemical potential
h Plank's constant
k_B Boltzman's constant
f frequency
I current
Γ tunnel rate
τ waiting time
C capactitance
V_{gs} gate voltage
V_{ds} drain voltage
V_b biasing voltage
E_c charging energy
n electron density

CHAPTER 1

INTRODUCTION

1.1 Introduction

With increasing demand of higher processor speed and power efficient integrated circuit components scientist are in pursuit of newer devices. Although few works had been done in the similar field earlier [1]-[5], for the last few years tremendous advancement has been made on nano-electronics circuits and devices. Single Electron Transistor (SET) is one of those unique devices which hold promise to dominate the future world of minuscule circuitry. This chapter focuses on the history of this quantum device, discusses the basic physics of the transistor and finally explains the motivation of this thesis work.

1.2 History of Single Electron Transistor

The effects of charge quantization were first observed in tunnel junctions containing metal particles as early as 1968 [6]. Later, the idea that the Coulomb blockade can be overcome with a gate electrode was proposed by a number of authors [7-10], and Kulik and Shekhter [11] developed the theory of Coulomb-blockade oscillations, the periodic variation of conductance as a function of gate voltage. Their theory was classical, including charge quantization but not energy quantization. However, it was not until 1987 that Fulton and Dolan [12] made the first SET, entirely out of metal and observed predicted oscillation. They made a metal particle connected to two metal leads with tunnel junctions, all on top of an insulator with a gate electrode underneath. Since then, the capacitances of such metal SETs have been reduced to produce very precise charge quantization.

The first semiconductor SET was fabricated accidentally in 1989 by Scott-Thomas *et al.* [13] in narrow Si field effect transistors. In this case the tunnel barriers were produced by interface charges. Shortly thereafter Meirav *et al.* [14] made controlled devices, albeit with an unusual hetero structure with AlGaAs on the bottom instead of the top. In these and similar devices the effects of energy quantization were easily observed. [15]-[17] Only in the past few years have metal SETs been made small enough to observe energy quantization. [18] Foxman *et al.* [13] also measured the level width Γ and showed how the energy and charge quantization are lost as the resistance decreases toward h/e^2. In most cases the potential confining the electrons in a SET is of sufficiently low symmetry that one is in the regime of quantum chaos: the only quantity that is quantized is the energy. In this case there is a very sophisticated approach, based in part on random matrix theory, for predicting the distributions of peak spacing and peak heights [19]-[21]. There are challenging problems in this area that are still unsolved. In particular, there is

great interest in how the interplay of exchange and level spacing determines the spin of a small metal SET [22].
In a SET of sufficiently high symmetry, angular momentum in the plane of the 2DEG is conserved, so shell structure is apparent. Another way to eliminate the scattering that destroys angular momentum conservation is to apply a magnetic field perpendicular to the 2DEG. At sufficiently high fields elegant patterns are seen in the single-electron-peak positions as a function of field [23].

The evolution of Coulomb charging peaks with magnetic field has been interpreted with various degrees of sophistication, imitating the development of the theory of atoms. First one tries the "constant interaction model" in which electrons are treated as independent except for a constant Coulomb charging energy. This gives only a qualitative picture of the physics. In order to be quantitative, one needs to at least treat the electron-electron interactions self-consistently (analogous to the Thomas – Fermi model) [24], and for some cases one needs to include exchange and correlations.

In particular, it is found that electrons in an SET undergo a series of phase transitions at high magnetic field [25]. One of these is well described by Hartree-Fock theory, but others appear to require additional correlations.

The future of research on SETs looks very bright. There are strong efforts around the world to make the artificial atoms in SETs smaller, in order to raise the temperature at which charge quantization can be observed. These involve self-assembly techniques [26] and novel lithographic and oxidation methods [27] whereby artificial atoms can be made nearly as small as natural ones. This is, of course, driven by an interest in using SETs for practical applications. However, as SETs get smaller, all of their energy scales can be larger, so it is very likely that new phenomena will emerge.

1.3 Basic Physics of Single Electron Transistor

A conventional field-effect transistor, the kind that makes all modern electronics work, is a switch that turns on when electrons are added to a semiconductor and turns off when they are removed. These on and off states give the ones and zeros that digital computers use for calculation. Interestingly, these transistors are almost completely classical in their physics. Their behaviors are rarely affected by quantum mechanics. However, if one makes a new kind of transistor, in which the electrons are confined within a small volume and communicate with the electrical leads by tunneling, all this changes. One then has a transistor that turns on and off again every time one electron is added to it; we call it a single electron transistor (SET). Furthermore, the behavior of the device is entirely quantum mechanical.

The manipulation of single electrons was demonstrated in the seminal experiments by Millikan at the very beginning of the century, but in solid state circuits it was not implemented until the late 1980s, despite some important earlier background work [1]-[5]. The main reason for this delay is that the manipulation requires the reproducible

fabrication of very small conducting particles, and their accurate positioning against external electrodes. The necessary nanofabrication techniques have become available during the past two decades, and have made possible a new field of solid state physics,

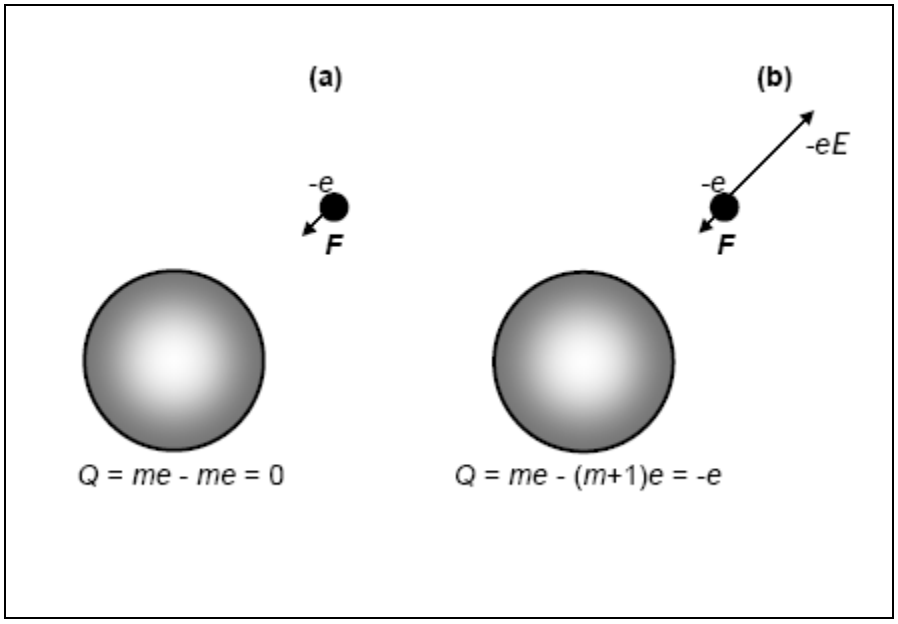

Fig 1.1: The basic concept of single-electron control: a conducting island (a) before and (b) after the addition of a single electron. The addition of a single uncompensated electron charge creates an electric field ***E*** which may prevent the addition of the following electrons.

The basic concept of single-electronics is illustrated in Fig. 1.1. Let a small conductor (traditionally called an *island*) be initially electro-neutral, i.e. have exactly as many (*m*) electrons as it has protons in its crystal lattice. In this state the island does not generate any appreciable electric field beyond its borders, and a weak external force ***F*** may bring in an additional electron from outside. (In most single-electron devices, this injection is carried out by tunneling through an energy barrier created by a thin insulating layer). Now the net charge *Q* of the island is (*-e*), and the resulting electric field *E* repulses the following electrons which might be added. Though the fundamental charge $e \approx 1.6\text{x}10^{-19}$ Coulomb is very small on the human scale of things, the field *E* is inversely proportional to the square of the island size, and may become rather strong for nanoscale structures. For example, the field is as large as ~ 140 kV/cm on the surface of a 10-nm sphere in vacuum. The theory of single-electron phenomena shows that a more adequate measure of the strength of these effects is not the electric field, but the *charging energy*

$$E_c = e^2/C \qquad (1.1)$$

where *C* is the capacitance of the island (For a two-electrode capacitor, the elementary charging energy is of course $e^2/2C = E_c/2$, rather than E_c. However, if a single small conductor is charged with electrons from a source kept at a fixed electrochemical potential μ, this is E_c which gives the electrostatic contribution to the energy necessary for the transfer of one additional electron to the conductor: $e\Delta\mu \equiv E_a \approx E_c$ + kinetic energy – in Eqn. (1.2) this relationship is established.

When the island size becomes comparable with the de Broglie wavelength of the electrons inside the island, their energy quantization becomes substantial. In this case the energy scale of the charging effects is given by a more general notion, the *electron addition energy* E_a. In most cases of interest, E_a may be well approximated by the following simple formula:

$$E_a = E_c + E_k. \qquad (1.2)$$

Here E_k is the quantum kinetic energy of the added electron; for a degenerate electron gas, $E_k = 1/g(\varepsilon_F)V$, where V is the island volume and $g(\varepsilon_F)$ is the density of states on the Fermi surface.

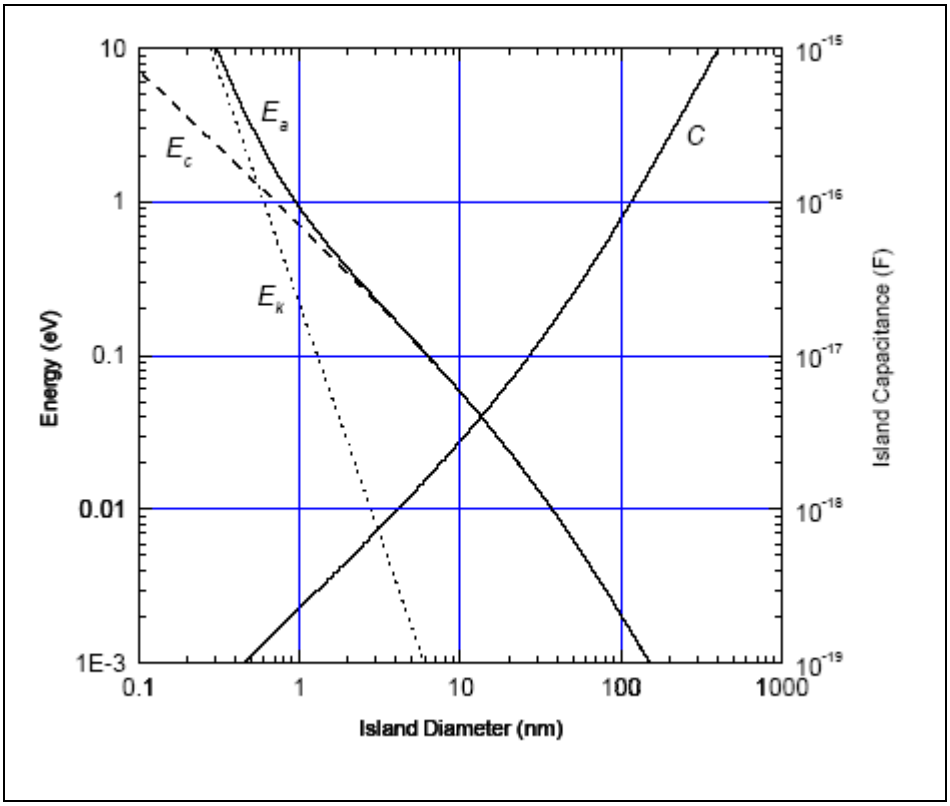

Fig. 1.2: Single-electron addition energy E_a (solid line), and its components: charging energy E_c (dashed line) and electron kinetic energy E_k (dotted line)

Fig. 1.2 shows the total electron addition energy as a function of the island diameter, as calculated using Eqn. (1.2) for a simple but representative model. For 100-nm-scale devices which were typical for the initial stages of experimental single-electronics, E_a is dominated by the charging energy E_c and is of the order of 1 meV, i.e. ~ 10 K in temperature units. Since thermal fluctuations suppress most single-electron effects unless $E_a \gtrsim 10\ k_BT$ these experiments have to be carried out in the sub-1-K range (typically, using helium dilution refrigerators). On the other hand, if the island size is reduced below ~10 nm, E_a approaches 100 meV, and some single-electron effects become visible at room temperature. However, most suggested digital single-electron devices require even higher values of E_a (~ 100 k_BT) in order to avoid thermally-induced random tunneling

events, so that for room temperature operation the electron addition energy E_a has to be as large as a few electron-volts, and the minimum feature size of single-electron devices has to be smaller than ~1 nm (Fig. 1.2). In this size range the electron quantization energy E_k becomes comparable with or larger than the charging energy E_c for most materials; this is why islands this small are frequently called *quantum dots*. Their use involves not only extremely difficult nanofabrication technology (especially challenging for large scale integration), but also some major physics problems including the high sensitivity of transport properties to small variations of the quantum dot size and shape. This is why it is very important to develop single-electron devices capable of operating with the lowest possible ratio E_a/k_BT . As we will see below, some devices may work in the size range where $E_c > E_k$ even at room temperature, thus avoiding complications stemming from the energy quantization effects.

1.4 Motivation

SET is continually being tested by researchers and engineering scientist in various applications. Being a nano-electronic device, SET is a potential candidate for components of molecular computing, quantum computing and nano-electro-mechanical devices (NEMS). SET island is also explained to behave like artificial atom because electrons are confined in the quantum dot island.

This work introduces a new type of application of SET that will eventually open many other doors to the different branches of nano-electronics.

Recent trends in electronics circuits focus on combining multiple features in a single die. The addition of features can be achieved at the cost of increment of power consumption and the complexity of size. However, scientists and engineers are focusing on innovative design topologies and circuits to reduce both the power consumption and design complexity while adding more and more features. Communications circuits are one of the major research arena where significant efforts are given. From consumer electronics to mobile medical applications to space technology, a communications circuit plays major roles. Reducing the power is a great achievement for any mobile system on the surface of earth and in space, since power storage and power generations are limited. The fundamental motivation of this work arose from the awareness of reducing the circuit complexity while decreasing the power consumption for a communication system through designing a unique and novel phase modulation circuit that will consist only one SET and SET being very low power consuming device the circuit’s operation power will be very small.

1.5 Organization of the thesis

History of SET is described in chapter 1. Basic concept and physics of SET is also explained in this chapter.

Chapter 2 begins with a discussion of physical structure of SET. One of the major phenomena of SET is Coulomb Blockade which is also explained in this chapter. Theory of operation of SET, I-V characteristics, stability plots are also discussed in this chapter. At the end of this chapter different techniques of SET fabrication are discussed.

Chapter 3 focuses on modeling of SET. One of the quantum mechanical models is SECS which is discussed in detail in this chapter. A macro model is also studied. Some modifications are proposed for the improvement of the macro model. At the end of this chapter, simulation results of the both modified model and the reference model are compared.

A new phenomenon called negative transconductance is explained in the Chapter 4. This unique feature of SET is utilized to propose a simplified SET based phase modulation circuit in this chapter. Circuit description, biasing conditions and results are also discusses in this chapter.

Chapter 5 is contains concluding remarks of the thesis. Some possible future works are also discussed at the end.

CHAPTER 2

SET STRUCTURE, OPERATION AND FABRICATION

2.1 Introduction

Single electron transistor is unique in its structure, operation and characteristics. The fabrication process of SET requires delicate methodology and machinery. This chapter describes the physical structure of SET. The equivalent circuit is also discussed with simplified transistor view. The theory of Coulomb blockade which is the heart of the transistor operation is discussed which is followed by the operating principle of the transistor itself. Later, a brief discussion on SET fabrication technology is presented.

2.2 Physical Structure of Single Electron Transistor

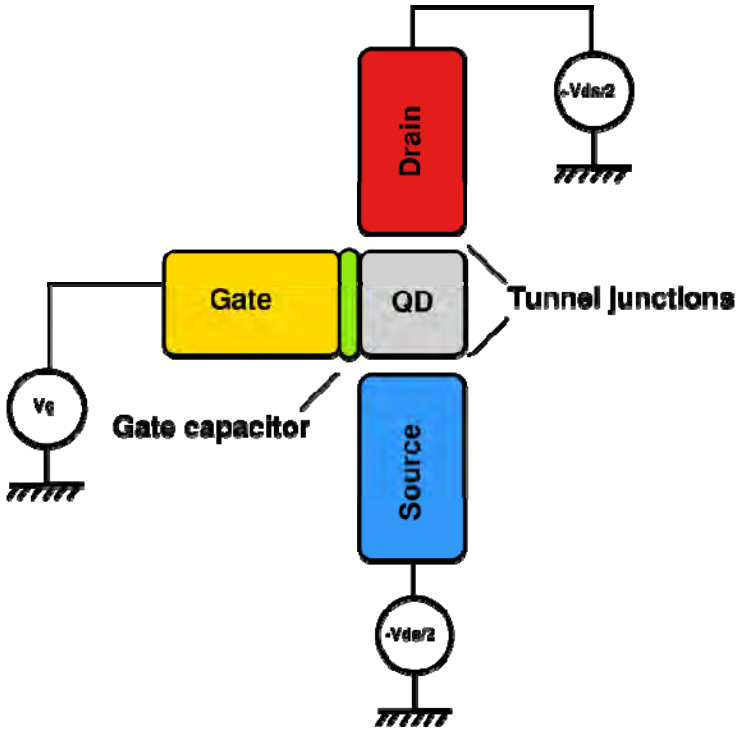

Fig. 2.1: Structural view of SET

The SET transistor can be viewed as an electron box that has two separate junctions for the entrance and exit of single electrons (Fig. 2.1). It can also be viewed as a field-effect

transistor in which the channel is replaced by two tunnel junctions forming a metallic island. The voltage applied to the gate electrode affects the amount of energy needed to change the number of electrons on the island.

The SET transistor comes in two versions that have been nicknamed "metallic" and "semiconducting". These names are slightly misleading, however, since the principle of both devices is based on the use of insulating tunnel barriers to separate conducting electrodes.

In the original metallic version fabricated by Fulton and Dolan, a metallic material such as a thin aluminum film is used to make all the electrodes. The metal is first evaporated through a shadow mask to form the source, drain and gate electrodes. The tunnel junctions are then formed by introducing oxygen into the chamber so that the metal becomes coated by a thin layer of its natural oxide. Finally, a second layer of the metal - shifted from the first by rotating the sample - is evaporated to form the island.

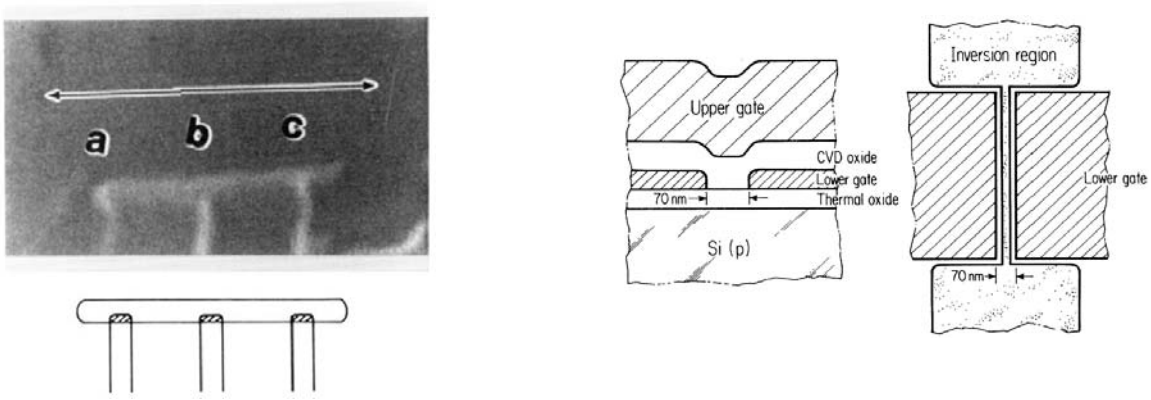

Fig. 2.2: Different types of SET proposed earlier (a) metallic SET [12] (b) semiconducting SET [13]

In the semiconducting versions, the source, drain and island are usually obtained by "cutting" regions in a two-dimensional electron gas formed at the interface between two layers of semiconductors such as gallium aluminum arsenide and gallium arsenide. In this case the conducting regions are defined by metallic electrodes patterned on the top semiconducting layer. Negative voltages applied to these electrodes deplete the electron gas just beneath them, and the depleted regions can be made sufficiently narrow to allow tunneling between the source, island and drain. Moreover, the electrode that shapes the island can be used as the gate electrode.

In this semiconducting version of the SET, the island is often referred to as a quantum dot, since the electrons in the dot are confined in all three directions. In the last few years researchers at the Delft University of Technology in the Netherlands and at NTT in Japan have shown that quantum dots can behave like artificial atoms. Indeed, it has been possible to construct a new periodic table that describes dots containing different numbers of electrons [28].

A simplified schematic representation of SET may look like as shown in Fig. 2.3, where drain, source and the gate electrodes are shown capacitively coupled to the quantum dot island. In this model all isolation barriers are replaced by capacitor including the gate dielectric.

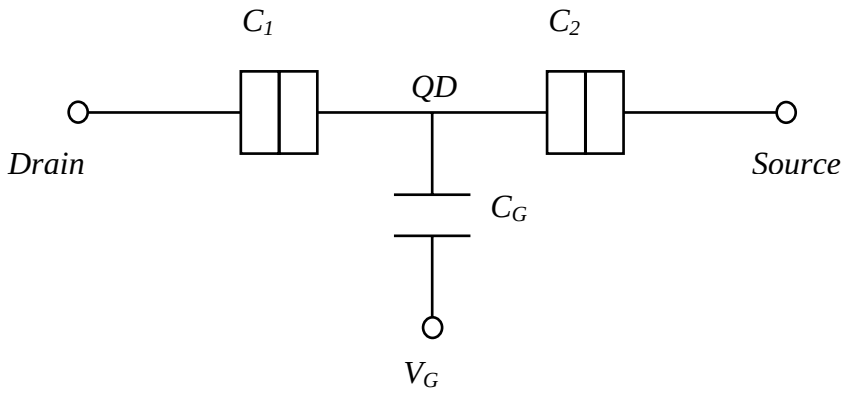

Fig. 2.3: Schematic representation of SET

The following figure shows a possible 3-D view of a SET where quantum dot island is exaggerated for illustration purposes. In reality, the island is usually 35~50nm in length/width.

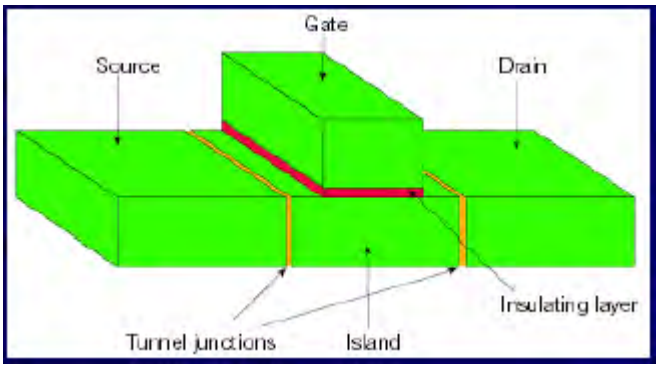

Fig. 2.4: A 3-D representation of SET [29]

An atomic force microscopy image of a fabricated SET is shown in Fig. 2.5. This fabricated SET is demonstrated to operate at room temperature [30].

2.3 Coulomb Blockade

In physics, a Coulomb blockade, named after Charles-Augustin de Coulomb, is the increased resistance at small bias voltages of an electronic device comprising of at least one low-capacitance tunnel junction.

A tunnel junction is, in its simplest form, a thin insulating barrier between two conducting electrodes. If the electrodes are superconducting, Cooper pairs with a charge of two elementary charges carry the current. In the case that the electrodes are normal-conducting, i.e. neither superconducting nor semiconducting, electrons with a charge of one elementary charge carry the current. The following reasoning is for the case of tunnel junctions with an insulating barrier between two normal-conducting electrodes (NIN junctions).

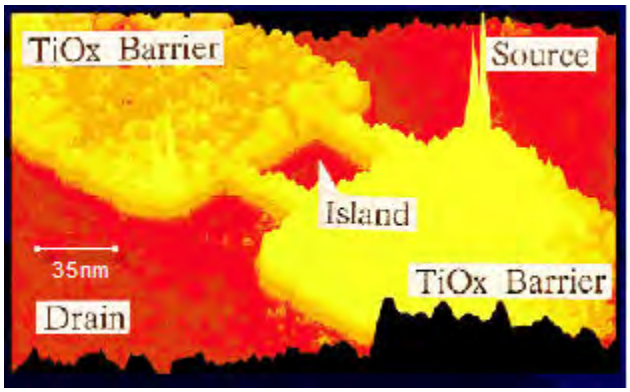

Fig. 2.5: An AFM (atomic force microscopy) image of a SET built by the STM (scanning tunneling microscope) nano-oxidation process. The TiOx tunneling barrier shown here surrounds the quantum dot island which is 35nm X 35nm in area, the width of the TiOx dielectric is 20nm with a relative permittivity of ε_r=24 and barrier height of 285meV. With the 3-nm thick Ti blanket layer this structure ensures small tunneling junction area and corresponding tunnel capacitance becomes as small as 10^{-19} F, which allows the set to be operated at room temperature [30].

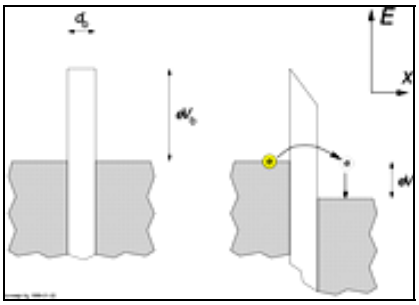

Fig. 2.6: Schematic representation of an electron tunneling through a barrier [31]

According to the laws of classical electrodynamics, no current can flow through an insulating barrier. According to the laws of quantum mechanics, however, there is a nonvanishing (larger than zero) probability for an electron on one side of the barrier to reach the other side which is generally known as quantum tunneling. When a bias voltage

is applied, this means that there will be a current flow. In first-order approximation, that is, neglecting additional effects, the tunneling current will be proportional to the bias voltage. In electrical terms, the tunnel junction behaves as a resistor with a constant resistance, also known as an ohmic resistor. The resistance depends exponentially on the barrier thickness. Typical barrier thicknesses are on the order of one to several nanometers.

An arrangement of two conductors with an insulating layer in between not only has a resistance, but also a finite capacitance. The insulator is called dielectric in this context, as the tunnel junction behaves as a capacitor.

Due to the discreteness of electrical charge, current flow through a tunnel junction is a series of events in which exactly one electron passes (tunnels) through the tunnel barrier (We neglect events in which two electrons tunnel simultaneously). The tunnel junction capacitor is charged with one tunneling electron (elementary charge unit), causing a voltage buildup $U = e / C$, where e is the elementary charge of 1.6×10^{-19} Coulomb and C the capacitance of the junction. If the capacitance is very small, the voltage buildup can be large enough to prevent another electron from tunneling. The electrical current is then suppressed at low bias voltages; the resistance of the device is no longer constant. The increase of the differential resistance around zero bias is called the Coulomb blockade.

In order for the Coulomb blockade to be observable, the temperature has to be low enough so that the characteristic charging energy (the energy that is required to charge the junction with one elementary charge) is larger than the thermal energy of the charge carriers. For capacitances below 1 femto-farad (10^{-15} farad), this implies that the temperature has to be below about 1 degree K. This temperature range is routinely reached for example by dilution refrigerators.

To make a tunnel junction in plate condenser geometry with a capacitance 1 femto-farad, using an oxide layer of electric permeability 10 and thickness one nanometer, one has to create electrodes with dimensions of approximately 100 by 100 nanometers. This range of dimensions is routinely reached for example by electron beam lithography and appropriate pattern transfer technologies, like the Niemeyer-Dolan technique, also known as shadow evaporation technique.

Another problem with the observation of the Coulomb blockade is the relatively large capacitance of the leads that connect the tunnel junction to the measurement electronics.

The simplest device in which the effect of Coulomb blockade can be observed is the so-called single electron transistor. It consists of two tunnel junctions sharing one common electrode with a low self-capacitance, known as the *island*. The electrical potential of the island can be tuned by a third electrode (the *gate*), capacitively coupled to the island.

In the blocking state, as shown in the Fig. 2.7 (top portion), no accessible energy levels are within tunneling range of the electron on the source contact. All energy levels on the island electrode with lower energies are occupied.

In Fig. 2.7 (bottom portion), when a positive voltage is applied to the gate electrode the energy levels of the island electrode are lowered. The electron (marked 1.) can tunnel onto the island (marked 2.), occupying a previously vacant energy level. From there it can tunnel onto the drain electrode (marked 3.) where it inelastically scatters and reaches the drain electrode Fermi level (marked 4) [31].

The energy levels of the island electrode are evenly spaced with a separation of ΔE. ΔE is the energy needed to each subsequent electron to the island, which acts as a self-capacitance C. The lower the C, the bigger ΔE gets. It is crucial for ΔE to be larger than the energy of thermal fluctuations $k_B T$, otherwise an electron from the source electrode can always be thermally excited onto an unoccupied level of the island electrode, and no blocking can be observed.

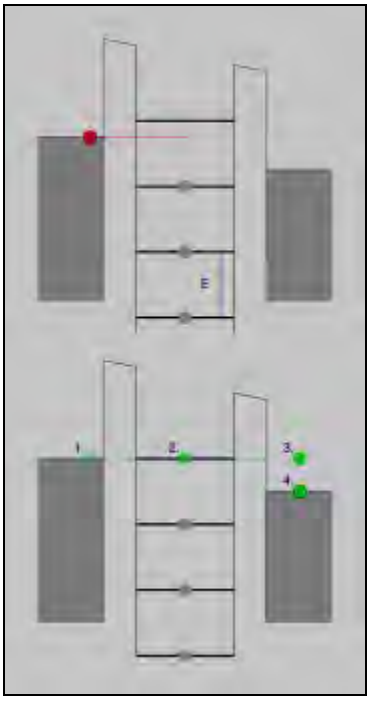

Fig. 2.7: Energy level of source, island and drain of a SET (left to right). (top) blocking stage and (bottom) transmitting stage [31]

2.4 Theory of Operation

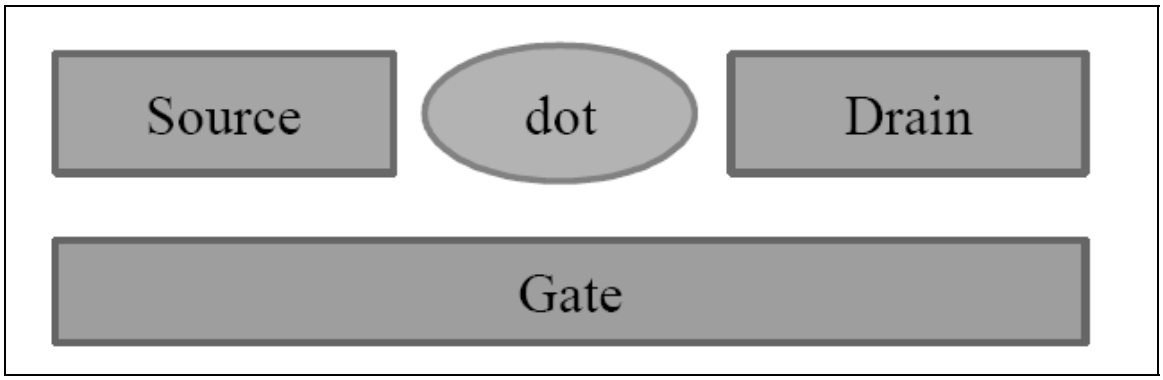

Fig. 2.8: The single electron transistor. A small dot is separated from the source and drain electrodes by tunnel barriers. It is also coupled to the gate electrode capacitively.

Fig. 2.8 shows a device schematic of a single electron transistor, where a dot is surrounded by three electrodes. All three electrodes are coupled to the dot capacitively; a Potential change in any of them can cause an electrostatic energy change in the dot. Only two electrodes (source and drain) are tunnel coupled to the dot and electron transport is allowed only between the dot and these two electrodes. Since the dot is connected to the source and drain electrodes by a tunnel barrier (meaning an electron is either on the dot or one of the electrodes), the number of electrons on the dot, N is well defined. We assume that all interactions between an electron on the dot and all other electrons on the dot or on the electrodes can be parameterized by the total capacitance C. We also assume that C does not depend on different charge states of the dot. Then the total electrostatic energy for a dot with N electrons will become $Q^2/2C = (Ne)^2/2C$. When N electrons reside on the dot, the total energy is

$$U(N) = \sum_{i=1}^{N} E_i + \frac{(Ne)^2}{2C} \tag{2.1}$$

After an additional electron is added to the dot, the total energy increases to

$$U(N+1) = \sum_{i=1}^{N+1} E_i + \frac{[(N+1)\cdot e]^2}{2C} \tag{2.2}$$

Here E_i is the chemical potential of the dot with i electrons. This is the energy of the orbital of the dot that the i-th electron would occupy if there were no electron-electron interactions. The electrochemical potential μ_N is then,

$$\mu_N = E_N + \left(N + \frac{1}{2}\right)\cdot\frac{e^2}{C} \tag{2.3}$$

By definition, the electrochemical potential μ_N is the minimum energy required for adding N-th electron. As long as μ_N is below both μ_S and μ_D , the N-th electron will be added to the dot. Likewise, to add one more electron to a dot with N electrons,

$$\mu(N+1) = \mu_N + \frac{e^2}{C} + \Delta E \tag{2.4}$$

needs to be lower than both μ_S and μ_D, where $\Delta E = E_{N+1} - E_N$. For simplicity, we will assume that ΔE does not change for different charge states of the dot.

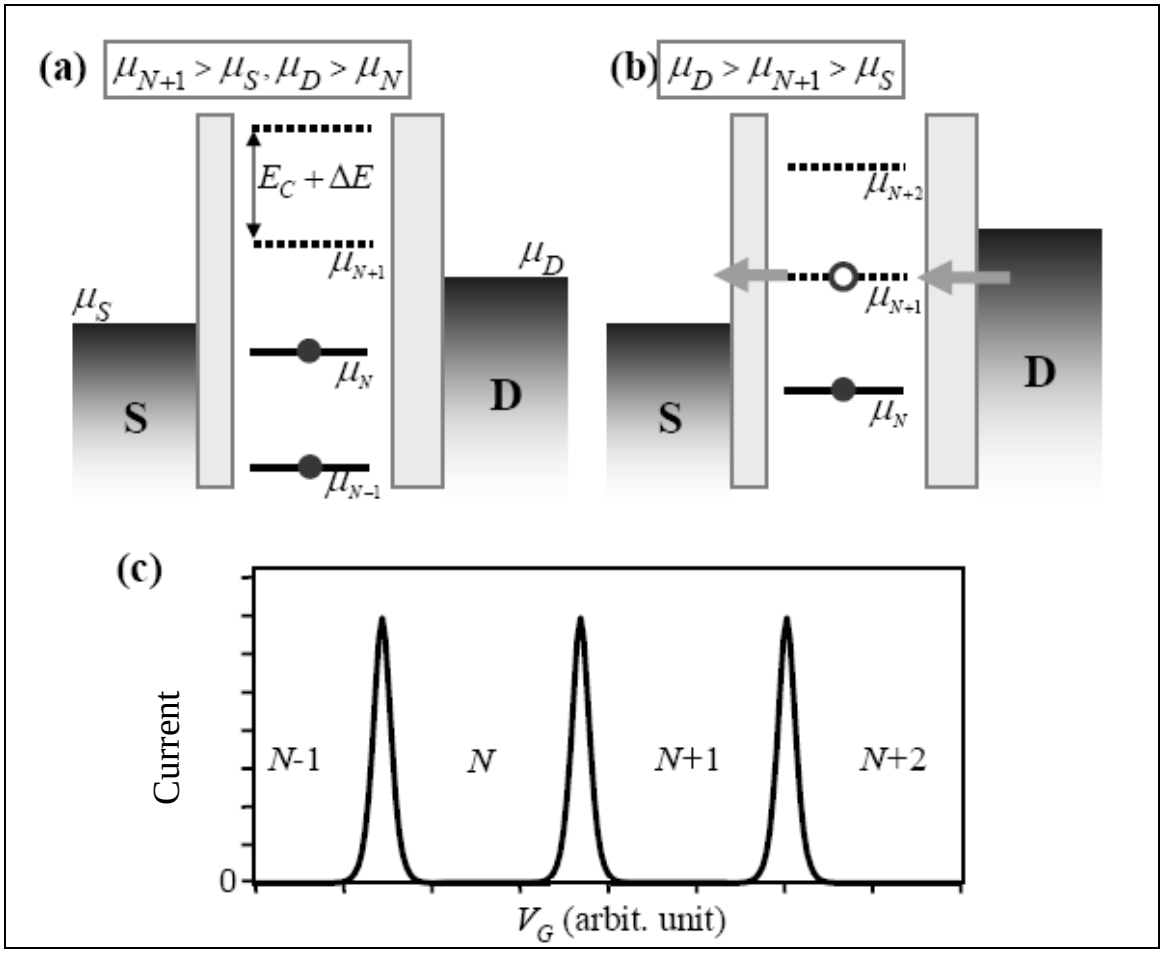

Fig. 2.9: Electron transport in a single electron transistor and I-V characteristics of SET. Energy diagrams for two different energy configurations are shown. In (a), the number of electrons on the dot is fixed at N ("off"-state) and the current is blocked. In (b), the electron number on the dot oscillates between N and N+1 ("on"-state). (c) The drain-source current as a function of the gate bias (V_G) displays the Coulomb oscillation. Each valley of current is labeled by the number of electrons on the dot.

This allows us to drop the subscript N for ΔE . Therefore, the N+1-th electron needs to have an energy larger than the one for the N-th electron by $e^2/C + \Delta E$. This is the charge addition energy. The first term $e^2/C \equiv E_C$, which is called the charging energy, is the energy that is required to overcome the Coulomb repulsion among different electrons.

The second term ΔE is the result of quantized excitation spectrum of the dot. Fig. 2.9(a) illustrates the energy diagram of a single electron transistor with $\mu_{N+1} > \mu_S$ *and* $\mu_D > \mu_N$. The dot will have N electrons and the solid lines below μ_N represent all the filled electrochemical levels. The lowest dotted line represents μ_{N+1} and it cannot be occupied since it is above the electrode Fermi levels. Therefore, the dot is stable with N electrons and hence the current cannot flow through the dot. In other words, the current is "blocked" due to the charge addition energy. Fig. 2.9(b) illustrates another case where $\mu_D > \mu_{N+1} > \mu_S$. In this case, the $N+1$-th electron can be added from the drain and then it can leave the source electrode. This process allows electric current to flow, constantly switching the charge state of the dot between N and $N+1$.

When we sweep the gate voltage V_G, the electrochemical potential of the dot changes linearly with V_G and this allows one to change the number of electrons on the dot. The drain source current as a function of V_G at a low bias is illustrated in Fig. 2.9(c). The current characteristic shows a series of peaks as well as valleys. In the valleys, the number of electrons on the dot is fixed and the current is blocked by the charge addition energy $e^2/C + \Delta E$. This corresponds to the case depicted in Fig.2.9(a). The dot has a well-defined electron number in each valley; N, N+1, N+2 and so on. The conductance peak in this plot corresponds to the case depicted in Fig. 2.9(b), where the dot can oscillate between two adjacent charge states. For example, the conductance peak located between the N-electron valley and the (N+1)-electron valley represents the dot carrying current by oscillating between N and N+1 electron states. These conductance peaks are called Coulomb oscillations. To be able to observe Coulomb oscillations, the charge addition energy should be much larger than the thermal energy k_BT. Otherwise, thermal fluctuation effect will be dominant and the Coulomb oscillation will disappear. Also the electron number on the quantum dot should be a well-defined observable, which requires the contact between the dot and the leads to be resistive. Quantitatively, the contact resistance needs to be larger than the resistance of a single conductance channel (*e.g.* a point contact),$h/e^2 \sim 25.81k\Omega$. These conditions are summarized below.

$$e^2/C + \Delta E. >> k_BT \qquad (2.5)$$

$$R_{contact} >> he^2 \qquad (2.6)$$

To date, single electron transport behavior has been observed from many different nanostructures. They include metallic nanoparticles [12], semiconductor heterostructures [13, 32], carbon nanotubes [33, 34] and semiconducting nanocrystals[34]. More recently, similar behaviors were observed from devices made from single molecules [24-25, 35].

2.4 Stability Plot, Regions of Operation and I-V characteristics

Proper operation of the SET requires proper biasing of gate and drains electrodes with respect to the gate electrode. Depending on the biasing, the SET can exhibit continuous oscillation characteristics in the drain current or a static ON state operation or a static OFF condition. Different regions of operation based on different level of biasing are best studied via stability plots. Depending on the biasing level, stability plot identifies the operating point of the SET describing whether the transistor will remain ON or OFF

Fig. 2.10 shows a typical stability plot with Coulomb diamonds. The diamond shaped shaded regions shown in the middle of the figure is called Coulomb diamond. These shaded regions correspond to particular value of gate and drain biasing (V_G and V_D respectively). These shaded diamonds are also known as stable regions for SET operation. While inside the region, there is always an excess amount of electron in the quantum dot island and so electron transport is effectively suppressed by the Coulomb blockade. Outside the stable region, there are numerous operating points where SET can be operated in a mode when it allows tunneling. In this mode of operation, the tunneling is not suppressed by the Coulomb blockade energy. The operating point, hence the mode of operation is defined both by the gate voltage (V_G) and the drain-source voltage difference (V_D).

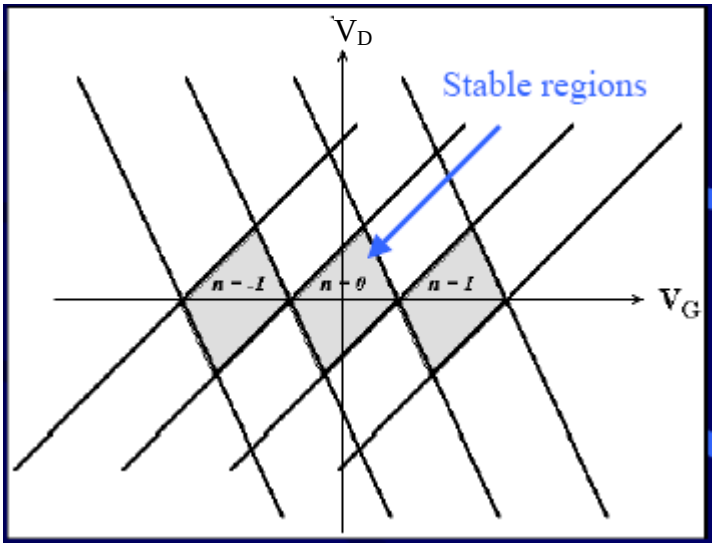

Fig. 2.10: Stability plot. Shaded diamonds corresponds to stable region where electron transportation is effectively suppressed by Coulomb blockade.

Two separate conditions are described below to clarify the operating regions.
<u>Condition 1:</u> Gate voltage fixed, Drain bias swept.

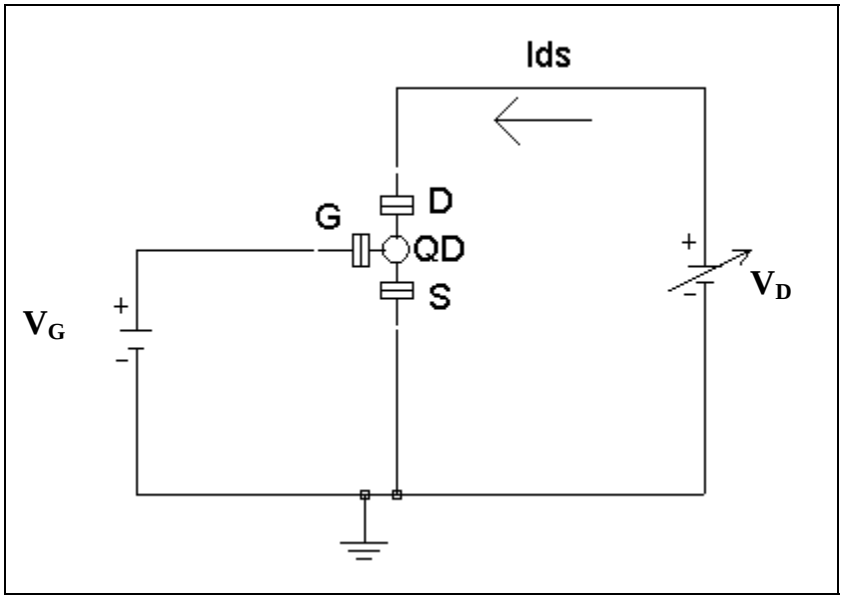

Fig. 2.11: A circuit setup for stability plot

Fig. 2.11 shows a typical circuit setup for stability plot. As shown in Fig. 2.12, the gate voltage is fixed at some level and the drain-source voltage is swept from one direction to the other. One can observe three distinct regions of operation. Internal shaded region, where the electron tunneling is suppressed by the Coulomb blockade is surrounded by the regions where tunneling is allowed. This region pattern doesn't repeat. Once the transistor is out of the stable region in either side, if the bias voltage continues to move in the same direction, it will never get another stable region.

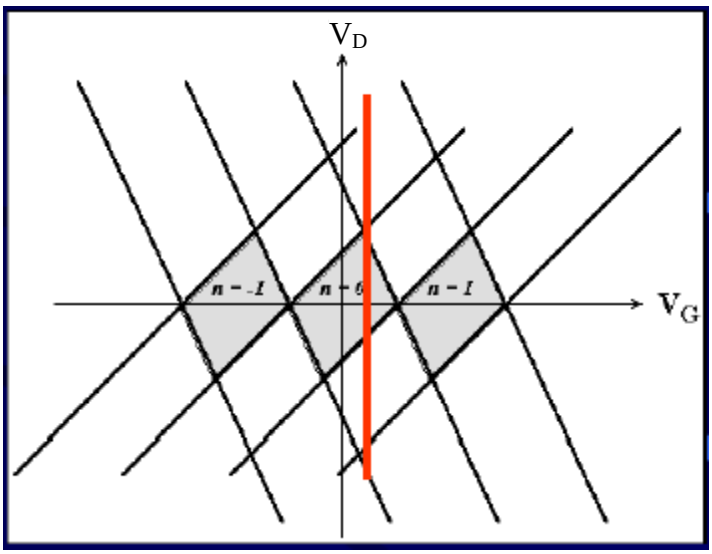

Fig. 2.12: Stability plot. V_D (connected to drain electrode) is being swept while gate bias is kept constant

Thus at this condition the transistor has only one stable region (OFF state) which is bounded by two unstable regions (ON state). The resulting current voltage characteristic is shown in Fig. 2.13.

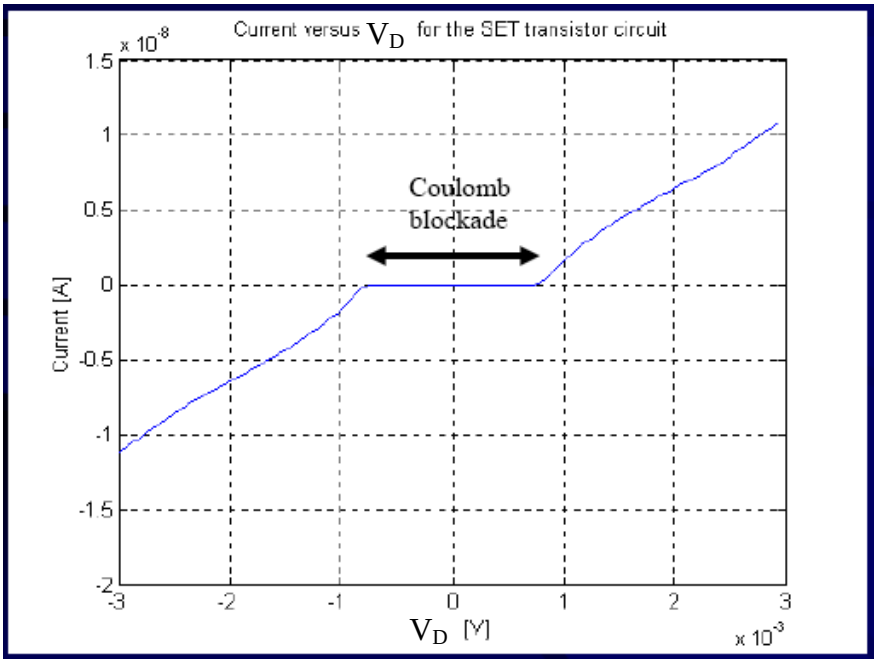

Fig. 2.13: I_D vs V_D characteristics for a fixed gate bias. Two unstable (tunneling allowed) and stable (tunneling blocked) region are obvious.

<u>Condition 2:</u> Drain bias fixed, Gate voltage swept.

Similarly, if we can now setup the circuit as shown in Fig. 2.14, where the drain bias is fixed and the gate bias is being swept.
This condition is much more interesting than the earlier condition. It is clearly seen from Fig. 2.15 that sweeping the gate potential from left to right while keeping the V_D fixed, traverses the transistor into alternating stable (OFF state) and unstable regions (ON state) of operation repeatedly. This condition gives a clear idea, how the changing potential at gate electrode creates OFF and ON states alternatively. Also it shows that, the V_D potential must be leveled to a certain value so as to ensure the successive ON-OFF regions of operations. If V_D is kept at zero level, the transistor will always remain in stable (OFF) condition. This happens as it enters a diamond immediately after coming out of another diamond-ensuring guaranteed OFF state. On the other hand if V_D is leveled too high so as not to intersect any shaded diamond, it keeps the transistor in permanent ON state. By carefully choosing V_D one can get alternative ON and OFF state by sweeping V_G. Such a level of V_D is illustrated in the Fig. 2.15.

As the gate voltage moves, the transistor experiences successive stable and unstable regions. This results, oscillating drain to source current. The result is shown in Fig. 2.16 depicting successive current peaks and valleys.

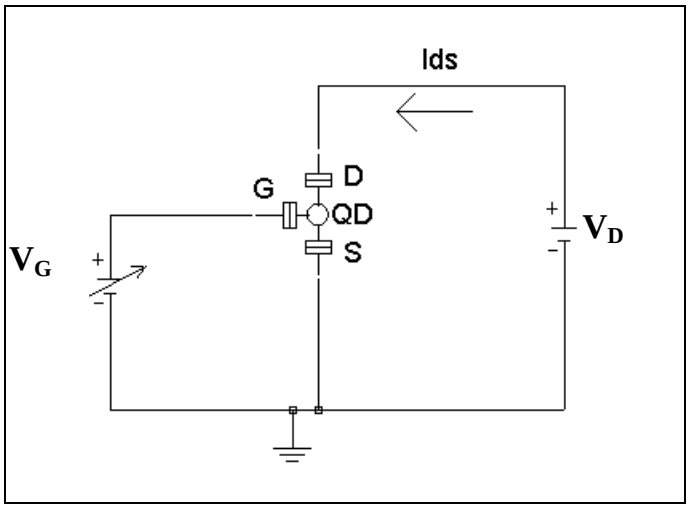

Fig. 2.14: Modified circuit setup for stability plot

Stability plot (also called stability diagram) gives a clear insight of the region of operation as well as better understanding of the I-V characteristics of the SET. By selecting biasing voltages the desired region of operation of the SET can be chosen which will deliver predicted current voltage characteristics.

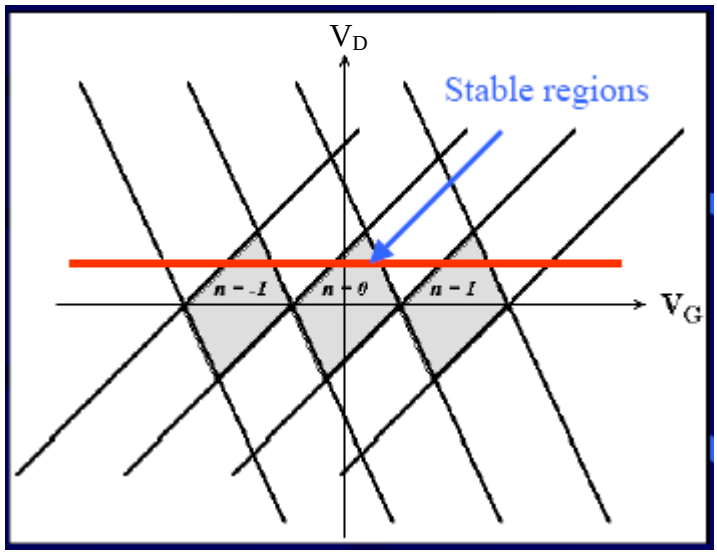

Fig. 2.15: Sweeping V_G while V_D is kept constant. The transistor undergoes repetitive stable and unstable regions resulting oscillation drain current.

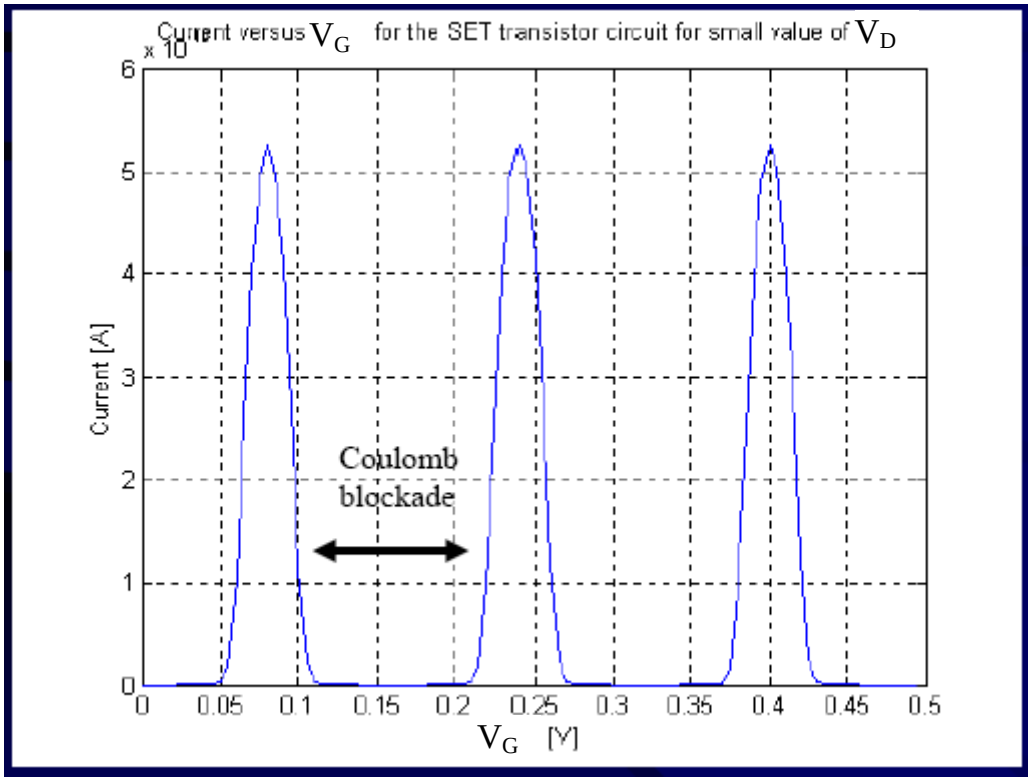

Fig. 2.16: I-V characteristics of SET. Coulomb oscillation with successive peaks and valleys resulting from the repetitive traversing of the transistor through unstable and stable regions

2.5 SET Fabrication Technique

SET, being a novel device, still has major fabrication challenges. The ultra small quantum dot island requires tremendously expensive and accurate fabrication facility. Basic limitation comes even from the operation itself. To be able to observe Coulomb oscillations, the charge addition energy should be much larger than the thermal energy k_BT. Otherwise, thermal fluctuation effect dominates and the Coulomb oscillation will disappear. This can be expressed through the relationship stated $e^2/C >> k_BT$. This is a fundamental barrier of SET operation. Either the capacitance of the total system has to be small enough so that the Coulomb blockade energy is larger than the thermal energy or the operating condition has to be cryogenic. For a typical example at room temp (T=300K) the capacitance has to be ~ 3aF with an island diameter less than 50nm.

Scientists are in constant pursuit of fabricating SET that is able to operate at room temperature. Fig. 2.5 shows an atomic force microscopy image of a fabricated SET. This fabricated SET is demonstrated to operate at room temperature.

An artificial pattern formation method based on the scanning tunneling microscope (STM) which avoids the control problems in self- organized structures[35]. Using this

technique, a group of scientist have succeeded in fabricating an SET. The SET operates at room temperature, showing a clear Coulomb staircase with a ~150 mV period at 300 K [30].

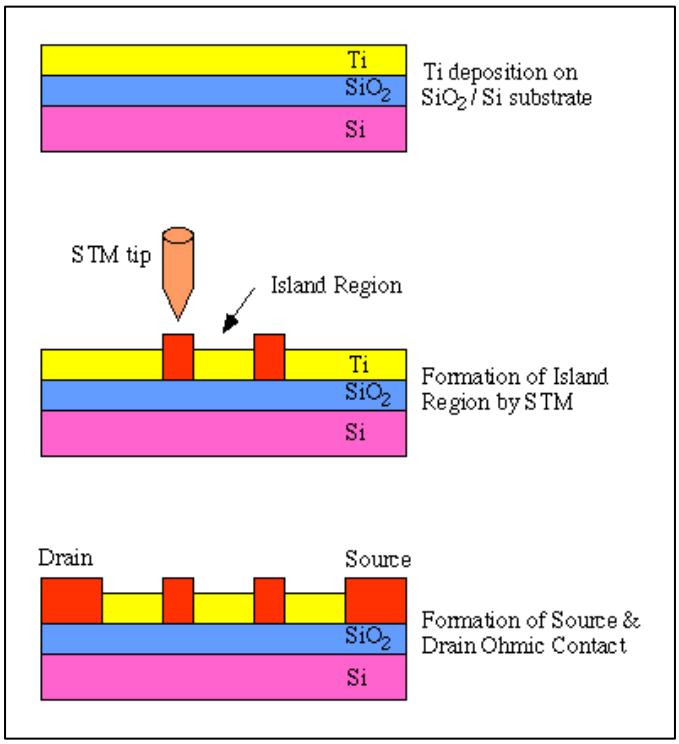

Fig. 2.17: Fabrication of the Ti/TiOx SET by the STM nano-oxidation process [36].

A description of the STM nano-oxidation process is shown in Fig. 2.17. A 3 nm thin titanium (Ti) metal film is deposited on a 100 nm thermally oxidized SiO_2/n-Si substrate. The Ti surface was oxidized by anodization through the water adhered to the surface of the Ti from the atmosphere, using the STM tip as a cathode, forming nanometer size Ti oxide (TiOx) lines. The barrier height of the TiOx/Ti junction has been found to be 285 meV for the electron from the temperature dependence of the current. The relative permittivity of the TiOx has been determined as e_r = 24 from the electric field dependence of the TiOx barrier height [36].

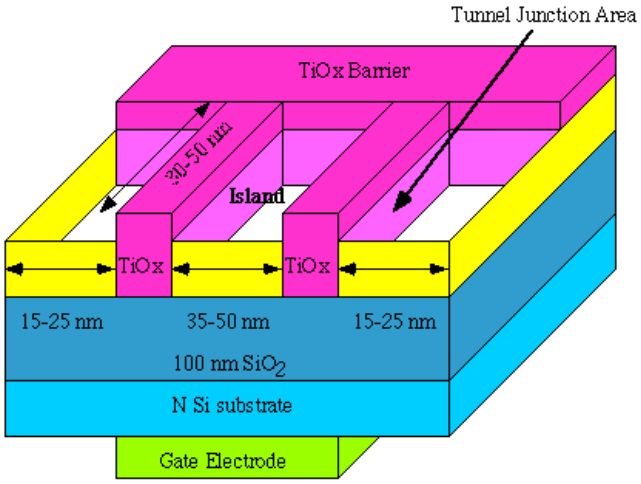

Fig. 2.18: Schematic of a single electron transistor [36]

A schematic illustration of the SET made by the STM nano- oxidation process is shown in Fig. 2.18. At both ends of the 3 nm thick Ti layer the source and drain ohmic contacts are formed, and on the back side of the n-Si substrate, the gate ohmic contact is formed. At the center region of the Ti layer, formed the island region, surrounded by two parallel, narrow TiOx lines, that serve as tunneling junctions for the SET, and two large TiOx barrier regions. Fig. 2.5 is an atomic force microscopy (AFM) image of the island region of a fabricated SET.

Typical sizes of the TiOx lines are 15-25 nm widths and 30-50 nm lengths. Typical island sizes are 30-50 nm by 35-50 nm. The most important feature of this structure is the small tunnel junction. The junction area corresponds to the cross section of the TiOx line, and is as small as 2-3 nm (the thickness of the Ti layer) by 30-50 nm (the length of the TiOx line). The deposited Ti layer is as thin as 3 nm, and the surface of the Ti layer is naturally oxidized to a depth of ~1 nm. Thus, the intrinsic Ti layer thickness is considered to be less than 3 nm. Owing to this small tunneling junction area, the tunnel capacitance becomes as small as 10^{-19} F, which allows the SET to be operated at room temperature.

The drain current-voltage characteristics of the SET were measured at room temperature and are shown in Fig. 2.19. The gate bias was set to 2 V. In Fig. 2.19, the solid line shows the current of the SET, and the dashed line shows the conductance of the SET. Between the drain bias of 0 V and -0.75 V, four clear Coulomb staircases with a 150 mV period are observed. The conductance oscillates with the increase of the drain bias with almost the same 150 mV period. The lower peaks of the conductance oscillation correspond to the flat regions of the current of the Coulomb staircase.

The Coulomb staircase shown in Fig. 2.19 may be attributed to the asymmetrical structure of the two tunneling junctions. One TiOx tunneling junction has a width of 18 nm, while the other junction is 27 nm wide. Due to this difference in junction widths, each tunneling junction has different values of conductance and capacitance, which produces the Coulomb staircase.

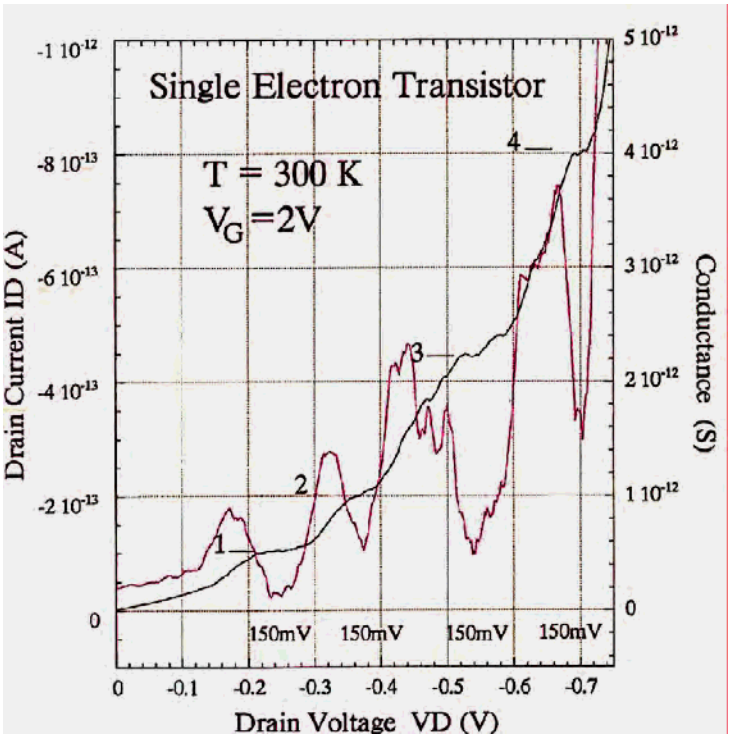

Fig. 2.19: Drain current v. drain voltage characteristics of the SET at 300 K [36]

The height of the Coulomb steps becomes larger with larger drain bias. This may be attributed to the increase of the tunneling probability of the electron through the TiOx tunneling barrier. The Fowler-Nordheim tunneling current increases as the applied drain bias lowers the height of the TiOx tunneling barrier.

The drain current v. gate bias characteristics with 150 mV drain bias at room temperature exhibit clear current oscillations with a period of ~460 mV, implying a periodic Coulomb oscillation of the current. The tunneling capacitance (C_t) and gate capacitance (C_g) could be roughly estimated from the period of the Coulomb staircase and oscillation. Their values were found to be C_t = ~3.6 x 10^{-19} F and C_g = ~3.5 x 10^{-19} F. These estimated values of the capacitances coincide well with the calculated capacitances from the SET's structural parameters. These results confirm the existence of Coulomb blockade phenomena at room temperature, and are due to the small dimensions of the SET island formed by the STM nano-oxidation process.

The fabricated SET shows a Coulomb staircase with periods of 150 mV at a temperature of 300 K. The Coulomb gap and staircase observed at high temperatures are attributed to the small tunneling junction area made by the STM nano- oxidation process. The fabrication process is quite easy and could be applicable to many kinds of devices.

Besides the AFM nano-oxidation process there are several other existing processes. A group of scientists from the University of Manchester has reported that they have

manufactured a single electron transistor out of graphene sheet [37]. These researchers have used the world's thinnest material to create the world's smallest transistor – a breakthrough that could spark the development of a new type of super-fast computer chip. Graphene is a single planar sheet of sp2 – bonded carbon atoms that are densely packed in a honeycomb crystal lattice – shown in Fig. 2.20. The carbon-carbon bond length in graphene is approximately 1.42 angstrom. This sheet is only one-atom thick. The research team suggests that future electronic circuits can be carved out of a single graphene sheet. Such circuits would include the central element or 'quantum dot', semitransparent barriers to control movements of individual electrons, interconnects and logic gates – all made entirely of grapheme as can be seen in Fig. 2.21.

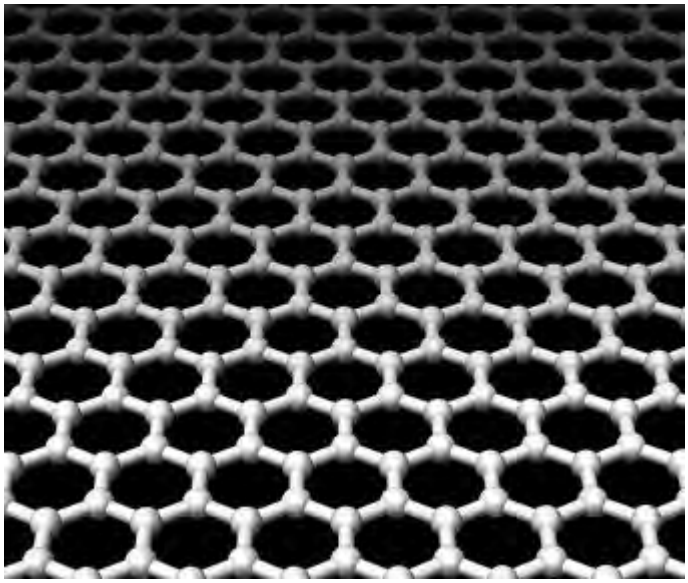

Fig. 2.20: Graphene sheet. Graphene is an atomic scale chicken wire made of carbon atoms [37].

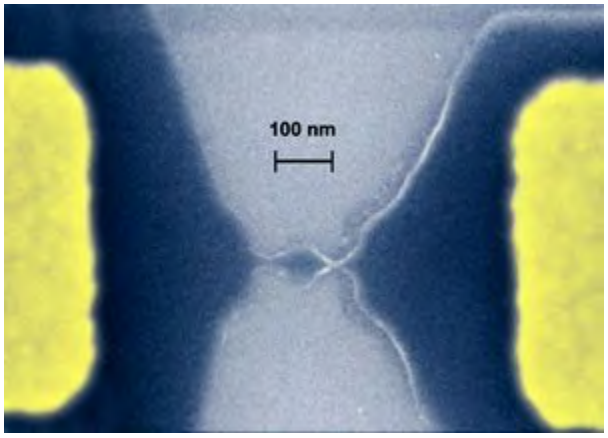

Fig. 2.21: Single-electron transistors carved entirely in a graphene sheet. The central elements are so-called quantum dots allowing electrons to flow one by one. The dots are connected to wider regions (contact pads by nm-wide constrictions) that work as tunnel barriers [37].

CHAPTER 3

SINGLE ELECTRON TRANSISTOR MODELING- QUANTUM & MACRO MODELS

3.1 Introduction

Single Electron Transistor consists of an island in between a source and drain, with a gate voltage exerted on the island. SET operate in single electronics regime where only one electron can tunnel from the source to drain via the island. The processes that take place in this nanostructure are Coulomb blockade and single electron tunneling. In this mesoscopic area, the charge discretization and energy contribution from a single electron are not negligible and leads to non-linear I-V characteristic for the device. A number of modeling methods have been used to study and investigate the phenomena of single electron transistor. Monte Carlo (MC) method has been implemented by several groups [38] whilst Master Equation (ME) formalism has been used to simulate the static and dynamic behavior of the single electron circuit. A combination of MC and ME methods have also been used in order to facilitate the study of rare events like co-tunneling and to eliminate the burden of state finding [39]. Besides these, there are few other methods were used according to the results.

3.2 Modeling the SET: SECS and SPICE models

In this chapter some of the reported models are discussed along with the proposed model. First a quantum mechanical model is discussed. The model is based on physics of electron tunneling and hence incorporates quantum effects. Later a macro model is discussed. A proposed model based on the discussed macro model is presented along with the simulation comparison of the discussed models.

3.2.1 SECS (Single Electron Circuit Simulator)

Downscaling of the devices of integrated circuits (ICs) has reached the verge of nanometer scale. On this scale, new phenomena of a quantum nature are starting to appear in ICs. The necessity of the development of new tools for studding the behavior of such circuits that take into account these phenomena is evident. For this reason, a new system for the design and simulation of single electron circuits called SECS has been developed. The operation of single electron circuits is based on the tunneling effect. The stochastic nature due to tunneling is incorporated in the simulation of single electron circuits using the Monte Carlo method. The novelty of the SECS system is that it provides the behavior of single electron circuits in an actual time scale, making thus easier and more complete the study of the phenomena that take place at an arbitrary single electron circuit.

The Single Electronics together with the carbon nanotubes, the quantum dots and the molecular electronics comprise the broader field of nanoelectronics. Single electron circuits owe their name to the fact that their operation is based on the localization or transfer, of a single electron (hole), or a small number of electrons (holes). In single electron circuits the body of a conductor or semiconductor is interrupted by thin layers of insulator. Therefore, contrary to the continuous charge transfer inside a conductor or semiconductor, the movement of charge is prohibited in single electron devices. However, charge is accumulated at the boundary surfaces of conductor – insulator (or semiconductor – insulator) and under certain conditions it can tunnel through the insulating material giving thus rise to an inconsecutive charge transfer. With the help of tunneling effect it is possible to control the transfer of charge, electron by electron. The area between insulated layers is called an island. Charge can enter or exit the islands only by tunneling effect. An isolated island can be described as an artificial atom, due to the fact that it can contain a small number of electrons, usually of the order of 100, resembling an atom. The charging energy is of prime importance for the operation of a single electron devices or circuits. An essential condition is that, the thermal energy must be very small compared to the island coulomb charging energy. Otherwise, electrons can acquire thermally the necessary energy in order to enter or exit the islands and therefore move in an uncontrolled way. As the size of the island get smaller, the charging energy grows bigger. In order for a single electron device to operate in room temperature the island capacitance must be of the order of aF and its dimensions must be of the order of nanometers. The realization of nano sized components needs a corresponding resolution in fabrication processes and techniques which are still lying far from reproducible mass production nano patterning.

3.2.1.1 BEHAVIOR OF SINGLE ELECTRON DEVICES

The operation of single electron devices is based on the characteristic behavior of small conducting particles surrounded by insulating material [40]. These particles are called islands and,

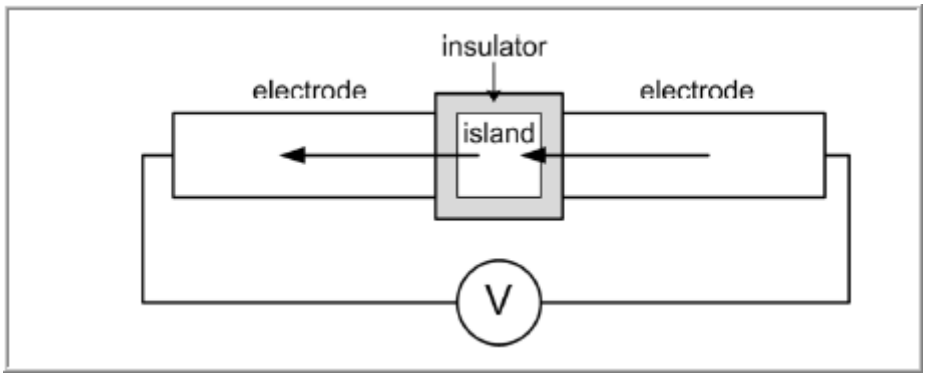

Fig.3.1: Electrons tunneling through an island give rise to an electric current.

due to their size, they can be charged only by a small number of electrons. The transport of electrons to and from each island is possible only by the tunneling effect because of the insulating layer that surrounds the island. The voltage of each island takes quantized values because it can only contain an integer number of elementary charge [41]. Respectively, the island charging energy is also quantized. The quantum nature of effects that take place in SET device operation introduces unique behaviors such as Coulomb blockade and Coulomb oscillations.

If an island is biased by a voltage source, then, for a range of voltage values, electrons tunnel from one electrode to the island and then to the other electrode, as seen in Fig. 1, thus giving rise to an electric current. In this case, the island is conducting. If the voltage is changed, it is possible to stop the flowing of current. This phenomenon is explained by the fact that, due to the discrete charging energies, the electrons do not have enough energy to charge the island and hence they are prevented from passing through the island to the other electrode. This state is known as a Coulomb blockade.

Between each electrode and the island, a tunnel junction is formed, as seen in Fig. 3.1. The current that flows, when the conditions are appropriate, is not a continuous charge transfer but successive tunneling events. In general, if a tunnel junction is biased with a constant current *I*, then the periodic phenomenon of charge transfer by tunneling is called Coulomb oscillations. Knowing the current *I*, the frequency of Coulomb oscillations is, f=*I*/e, where e is the elementary charge [42].In order to charge an island with electrons, the energy required is-

$$\boldsymbol{E_c = \frac{(ne)^2}{2C}} \qquad (1)$$

It is easily seen that the distance between the charging energy levels has a direct dependence on the capacitance of the island. The capacitance itself is a function of the dimensions of the island. The total capacitance of the island to its environment should be small, so that the charging energy is much greater than the thermal energy k_BT [43]. The Coulomb blockade effect can be observed at very low temperatures around 4.2 Kor less, and the operating temperature can be raised by scaling down the structures to a smaller size [43]. In order to observe the Coulomb blockade effect at room temperature, the island capacitance should be less than 1 aF and, hence, the size of the island has to be less than 5 nm [43].

3.2.1.2 TUNNEL JUNCTION

The elemental structure beneath every SET device is the tunnel junction. It is formed by two conductors or semiconductors that are separated by a thin insulating layer. The insulating layer creates a potential barrier that the electrons can cross with the tunnel effect, when the proper conditions are met. When the conditions are not fulfilled, there is no electron transfer, the tunnel junction is in Coulomb blockade, and it behaves as a capacitor.

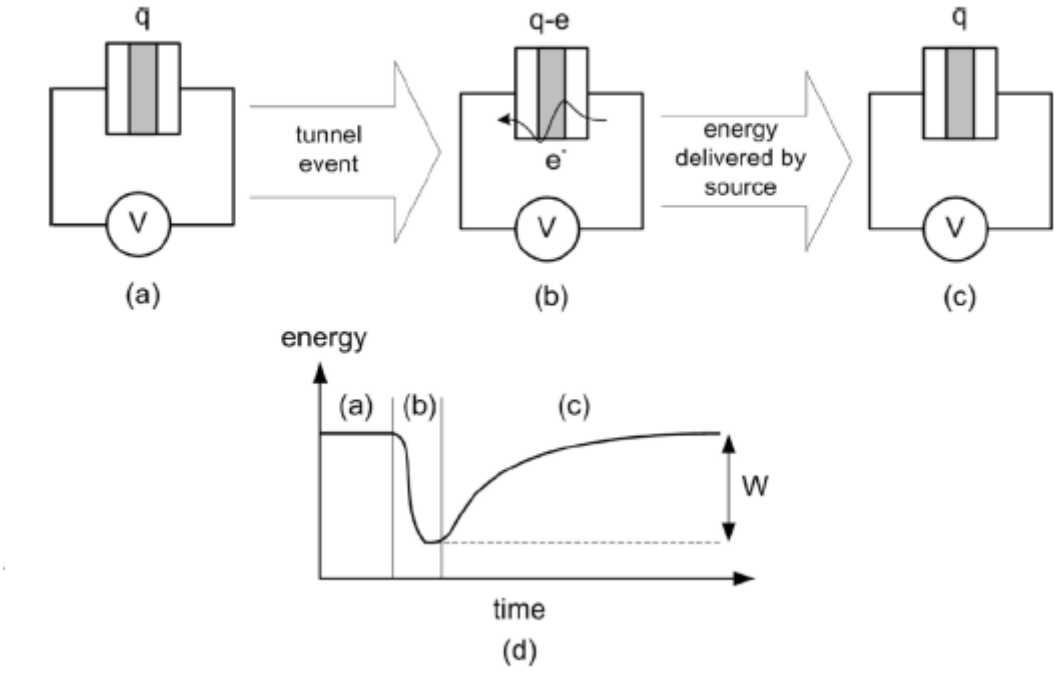

Fig. 3.2 (a)–(c): When a tunnel event occurs, the source restores the tunneling electron. (d) Qualitative plot of the energy of the tunnel junction during the procedure of a tunnel event.

The occurrence of tunnel events is the first thing that must be determined in order to describe the operation of SET devices and circuits. When a tunnel event takes place, the total energy change of all tunnel junctions equals the change of free energy F. The free energy is equal to the stored electrostatic energy E_c minus the energy that is delivered to the tunnel junctions by the sources W, that is $F= E_c-W$ [2], [44]. Consider the elemental SET circuit of a tunnel junction and a constant voltage source, as shown in Fig. 3.2(a), where charge is stored in the capacitance of the tunnel junction and the electrostatic energy is $Ec=q^2/2C$. If the tunnel conditions are met, it is possible for an electron to tunnel from the fermi energy level on one side of the junction only if there is a free energy level on the other side of the junction. Immediately after the tunnel event, the charge is altered to q-e and the stored energy, to $Ec=(q-e)^2/2C$as seen in Fig. 3.2(b). Eventually, the voltage source will restore the charge on the tunnel junction to Fig.3.3.2(c), producing work W. In Fig. 3.2(d), a qualitative plot of the stored energy is shown as a function of time. The probability of a tunnel event depends on the change of the free energy ΔF of the tunnel junction. Before the tunnel event, the free energy Fi equals the electrostatic energy Ec_i. The final free energy provides us with the stored energy before the source drives the circuit to equilibrium, that is, before the charge q is restored. Thus, F_f equals the final electrostatic energy minus the work done by the voltage

source F_f= Ec_f-W. The tendency of a physical system to occupy states of lower energy applies in this situation due to the fact that the greater the change of the free energy ΔF caused by a tunnel event is, the greater the possibility is for the tunnel event to happen.

For the simplification of the model we assume that the duration of tunneling is negligible, hence there is no energy transfer during the tunnel event, something that should be taken into account in a more detailed analysis [45]. The condition for a tunnel event to take place in the simple circuit of the tunnel junction is
ΔF <=0, that is,

$$\boldsymbol{F_f - F_i <= 0} \qquad (2)$$

The initial and final electrostatic energies of the tunnel junctionare equal

$$\boldsymbol{E_{ci} = E_{cf} = \frac{q^2}{2C}} \qquad (3)$$

The energy delivered to the tunnel junction by the voltage source is the difference in the electrostatic energy immediately after the tunnel event and when equilibrium is restored, that is,

$$\boldsymbol{W = \frac{q^2}{2C} - \frac{(q-e)^2}{2C}} \qquad (4)$$

Applying (3) and (4) to (2), the condition for the tunneling event follows:

$$\boldsymbol{q \geq \frac{e}{2}} \qquad (5)$$

or, in the case of negative charge, $\boldsymbol{q \geq -\frac{e}{2}}$. Hence, the Coulomb blockade condition is $\boldsymbol{|q| \geq \frac{e}{2}}$.

3.2.1.3 MODELING THE OPERATION OF SINGLE ELECTRONCIRCUITS

The single electron circuit is basically a system of tunnel junctions and islands. When a single electron circuit operates, it toggles between a number of states. These states are characterized by the number of electrons that occupy each island and by the potential of the nodes where the sources are connected (potential nodes). Each time a tunnel event occurs, the single electron circuit toggles to another state and that is the reason why, as mentioned before, the occurrence of tunnel events is the first thing that must be determined in order to describe the circuit's operation. Therefore, in order to model the

operation of a single electron circuit, we must define these states and the transition from one state to another.

There are two widely used methods for the modeling of single electron circuits, the Master Equation (ME) method and the Monte Carlo (MC) method. A system such as a single electron circuit can be described by the ME[46] as

$$\frac{\partial P_i(t)}{\partial t} = \sum_{j \neq i} (\Gamma_{ij} P_j(t) - \Gamma_{ji} P_i(t)) \quad (6)$$

The above equation expresses that the rate of change of the probability of the circuit being in state is analogous to the probability of being in a state j and toggle to state I and analogous to the probability of being in state i and toggle to some other state j . The analogy factor Γij is the rate of transition from state i to state j .For single electron circuits, this rate is called the tunnel rate.

The disadvantage of the ME method is that the number of states that have to be considered becomes often very large. Consequently, the matrix operations involved in calculating the tunnel rates are time-consuming, and the approximations do not converge quickly.

The MC method is a statistical method where the sampling from probability distribution functions is used and can be applied for the modeling of the behavior of single electron circuits [48]–[50]. In order to use the MC method, a probability distribution must be calculated for each one of the tunneling events that can occur in a single electron circuit. Each one of the tunneling events is related to a different change of the free energy ΔF and, thus, to a different tunnel rate Γ given by [49], [50]

$$\Gamma = \frac{\Delta F}{e^2 R_T \left(\exp\left(-\frac{\Delta F}{k_B T}\right)\right)} \quad (7)$$

where RT is the tunnel junction resistance (or tunnel resistance) and kBT is the thermal energy. The tunnel resistance must be sufficiently large, RT >>h/e2 =26kΩ , in order for the quantum fluctuations to become negligible so the electrons can be localized on the islands[46]. Each tunnel rate corresponds to a probability distribution that expresses the probability of a tunnel event to occur as a function of time

$$P(t) = e^{-\Gamma t} \quad (8)$$

Therefore, each possible tunnel event is described by a unique probability distribution. The time until each one of the possible tunnel events occurs is determined by sampling

from the probability distributions (8). In this way, a waiting time until each possible tunnel event is calculated by

$$\tau = -\frac{\ln(r)}{\Gamma} \tag{9}$$

where r is an evenly distributed random number from the interval [0, 1]. The tunnel event with the smallest waiting time τ will happen first, and thus we can determine the next state of the single electron circuit. By iteration of the procedure described above, we can describe the behavior and simulate the single electron circuits.

A number of simulators and simulation methods have been implemented for the single electron circuits. One such simulator is SIMON [51]. This simulator uses the MC method or a combination of MC and direct calculation. The direct calculation is used in order to include rare events, such as co-tunneling, in the simulation. MOSES is another simulator which is also based on the MC method [52]. A simulation method based on ME is SENECA, which is a computer algorithm suitable for studies of the dynamics and statistics of single electron systems. This method follows the numerical solution of a linear matrix equation for the vector of probabilities of various electric charge states of the system, with iterative refining of the operational set of states [53]. A simulator for single electron tunnel devices and circuits based on simulated annealing [54] uses the ME for the description of the transitions taking place in the circuit. Another proposed method for single electron digital circuit design (SECD) is based on a regular cellular structure [55]. The results are acquired by numerical simulation. For this application, an electron gas has been created, which precisely mimics the lattice gas. A great deal of work has also been done on the simulation of single electron circuits using SPICE models[56], [57].

3.2.1.4 SECS SIMULATION SYSTEM

The transitions of a single electron circuit during its operation occur between neighboring states, that is, when a tunnel event takes place, one electron is transferred. A system that evolves in such a way can be described by the Poisson process, as seen in Fig. 3.3. The single electron circuit in state toggles to the next state i with a tunnel rate Γi+1 . According to this process, the circuit can stay on the same state, toggle to a new state, or toggle to a state that has already been before. The SECS simulation system is based on the Poisson process and, apart from the number of electrons on each island, each state is associated with a time instance, in this way incorporating the actual time in the simulation environment. Thus, states with the same number of electrons are also described by time, and therefore the Poisson process evolves monotonically.

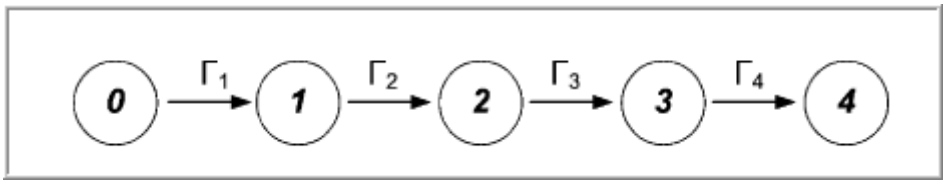

Fig. 3.3: Poisson process. Each state of the SET circuit corresponds to a different time instance. The transition between neighboring states is described by a tunnel rate Γ.

The SECS simulation system incorporates the stochastic nature of tunneling into its model by using the MC method. We may not know exactly when a tunnel event will occur, but we can determine through the probability distribution (8) the time interval until the next tunnel event via random sampling (9). This time interval is the actual time that the single electron circuit will remain in state before toggling to state i+1. Fig. 3.4 shows the flowchart of the SECS simulator. The first step is to design the single electron circuit and to define all of the necessary parameters such as the background charge of the islands, the temperature of the circuit, and the duration of the operation of the circuit.

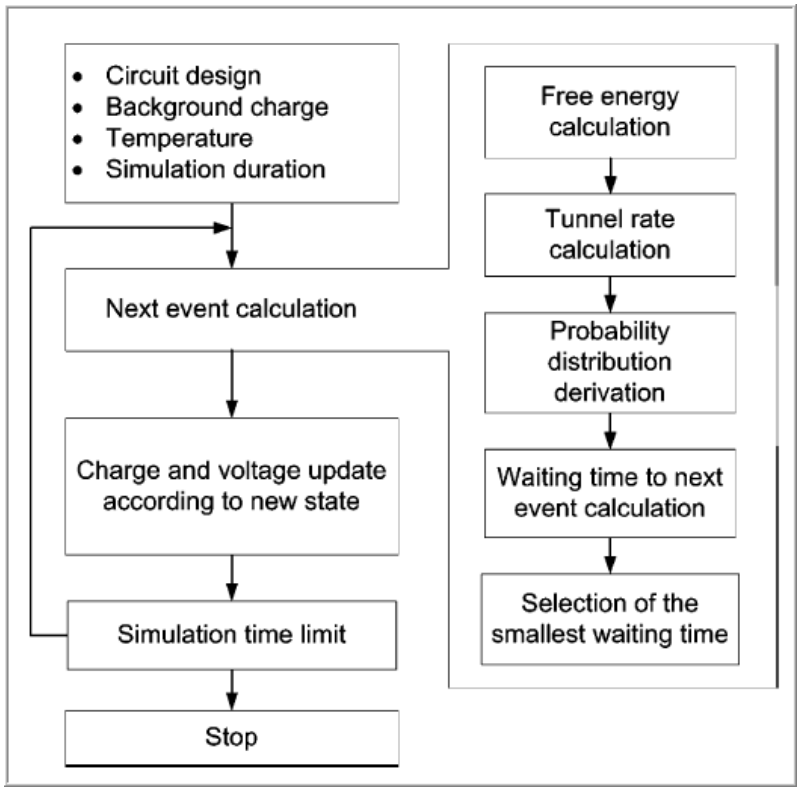

Fig. 3.4(a): Flowchart of the SECS simulator system.

Considering a circuit that can toggle between number of states, as seen in Fig. 4(b).

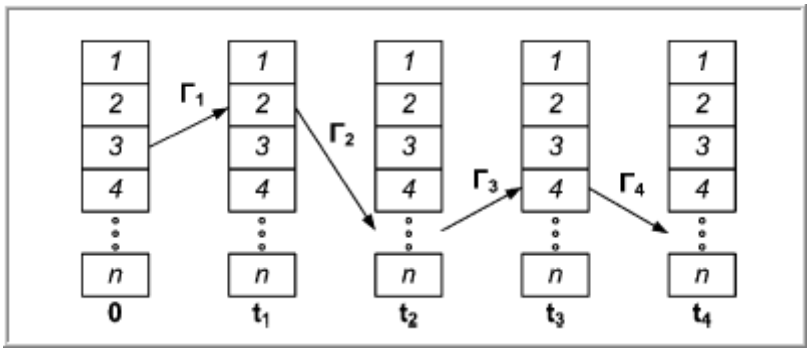

Fig 3.4(b): Application of the Poisson process for the description of the behavior of single electron circuits. SECS determines each successive state of the circuit, from all of the possible neighboring states. The waiting time during which the circuit stays at each state $t_{i+1} - t_i$ is the actual time that results from the probability distributions.

Starting at t=0 from state 3, the circuit can toggle to neighboring states. Each one of these transitions is characterized by a tunnel rate Γ_k and obeys to a different probability distribution. By sampling from these distributions, we determine time k intervals τ_1, τ_2.. τ_k until the next tunnel event. The transition that will take place is the one with the smallest time interval, for example, the transition to state 2. The waiting time $\tau_2 = t_1 - 0$ is the actual time according to which the simulation advances. Being the circuit to the new state 2, it can toggle to the kl states. The new probability distributions are calculated, and again the smallest time interval is chosen. If, for example, this time interval corresponds to state 15, then $\tau_{15} = t_2 - t_1$, and the simulation advances according to the actual time τ_{15} , that is, the time increment in the simulation is the waiting time for the next tunnel event. The novelty of the SECS simulation system is that it provides an actual time increment simulation of the behavior of single electron circuits.

3.2.1.5 SINGLE ELECTRON CIRCUIT SIMULATOR

SECS (single electron circuit simulator) [61] simulation system has been developed for the study of the behavior of nano electronic single electron devices and circuits. The simulation part is neatly combined with a graphical environment and a designing tool, providing a complete system for the research on single electron circuits. SECS is divided into two main parts, the designing part and the simulation part. The design of single electron circuits is being done with the OrCad capture environment, where a single electron component library has been developed. After the circuit design is complete, the netlist file is fed to the simulation part. The simulation algorithm and the graphical user interface have been developed in Matlab.

3.2.2 Macro model

Figure 3.5 shows the schematic diagram of an SET and its equivalent circuit.

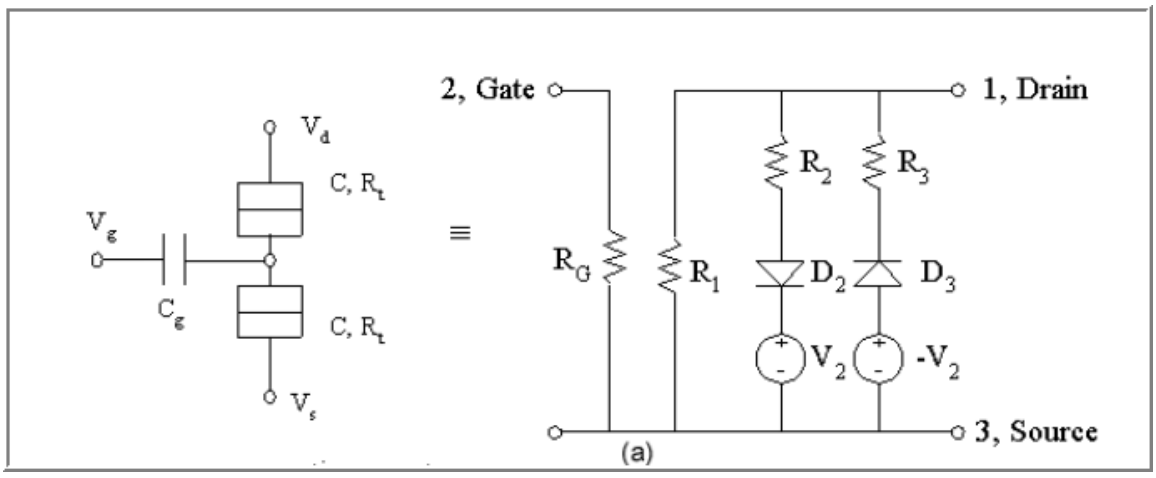

Fig 3.5: Macro-model of an SET

The macro-model representation of the equivalent circuit is summarized below.

In the circuit description presented below, R_1, R_2, and R_3 is expressed with a cosine function to describe the Coulomb oscillation and D_2, D_3, Vp, and -Vp is expressed to describe the Coulomb staircase. The parameter values, CF_1 = 60, CVp = 0.015, CI2 = 0.2x10-9, CR1 = 300 x 106 and CR2 = 100x106, give the best fit of the current-voltage characteristics when C = 1.6 aF, Cg = 4.8 aF, R_t = 100MΩ, and T = 30^0K.

```
.macro SET   node1   node2   node3
.param
+ pi= 3.14159265358979323846264338327 95
+CF1=60
+CI2=0.2E-9
+CR1=300E6
+CR2=275E6
+CVP=0.015

VVPP N_4 N_7 'CVP'
VVPN N_5 N_6 '-1 * CVP'
RG  SOURCE GATE 100G

R1 DRAIN SOURCE R='CR1+CR2*COS(CF1*PI*V(GATE,SOURCE))'
R2 DRAIN N_4 R='CVP/(CI2-2*CVP/(CR1+CR2*COS(CF1*PI*V(GATE,SOURCE))))'
R3 DRAIN N_5 R='CVP/(CI2-2*CVP/(CR1+CR2*COS(CF1*PI*V(GATE,SOURCE))))'

DD2 SOURCE N_6 DLED
DD1 N_7 SOURCE DLED
```

```
.MODEL DIODE D(N=0.01)
.EOM
```

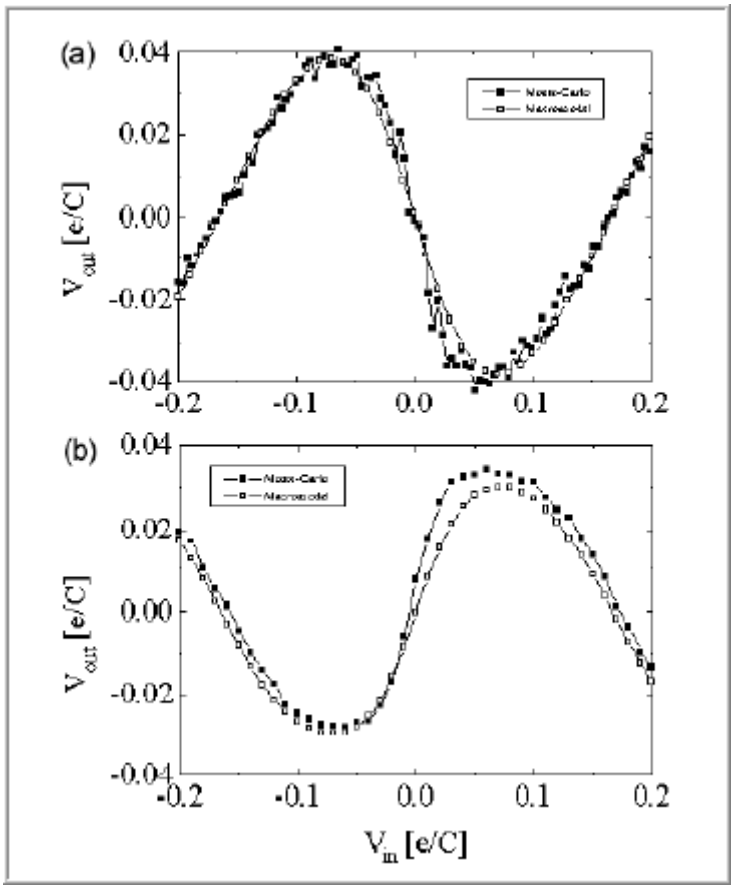

Fig. 3.6 The voltage transfer characteristics of SECs in Figs. 7(a) and (b).

In the Fig.3.6 the simulation results are obtained from the SPICE macro model and Monte-Carlo method. The filled symbols are Monte-Carlo results and the empty symbols are obtained from the SPICE macro-model. The macro-model results (empty symbols) are in agreement with the Monte Carlo simulation results (filled symbols) within 15 %, demonstrating the validity of the macro-model technique.

Simulation result for given Macro model:

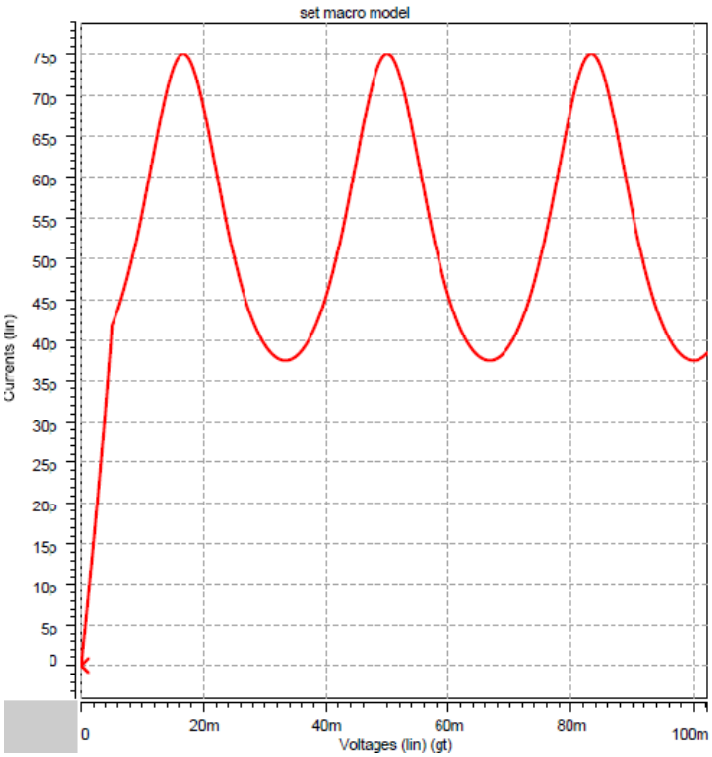

Fig. 3.7: Macro model. I-V profile of SET

3.3 The Proposed Modification

The macro model has been modified to exhibit the coulomb oscillation of the single electron transistor (SET).In the original model the crest and trough are not distinctly visible. So we have suitably chosen the arbitrary model parameter CF1as as shown below.

.SUBCKT SET drain gate source

.param
+ pi= 3.14159265358979323846264338327 95

```
+CF1=20
+CI2=0.2E-9
+CR1=300E6
+CR2=275E6
+CVP=0.015

VVPP N_4 N_7 'CVP'
VVPN N_5 N_6 '-1 * CVP'
RG  SOURCE GATE 100G

DD2 SOURCE N_6 DLED
DD1 N_7 SOURCE DLED

R1 DRAIN SOURCE R='CR1+CR2*COS(CF1*PI*V(GATE,SOURCE))'
R2 DRAIN N_4 R='CVP/(CI2-2*CVP/(CR1+CR2*COS(CF1*PI*V(GATE,SOURCE))))'
R3 DRAIN N_5 R='CVP/(CI2-2*CVP/(CR1+CR2*COS(CF1*PI*V(GATE,SOURCE))))'

.ENDS SET
```

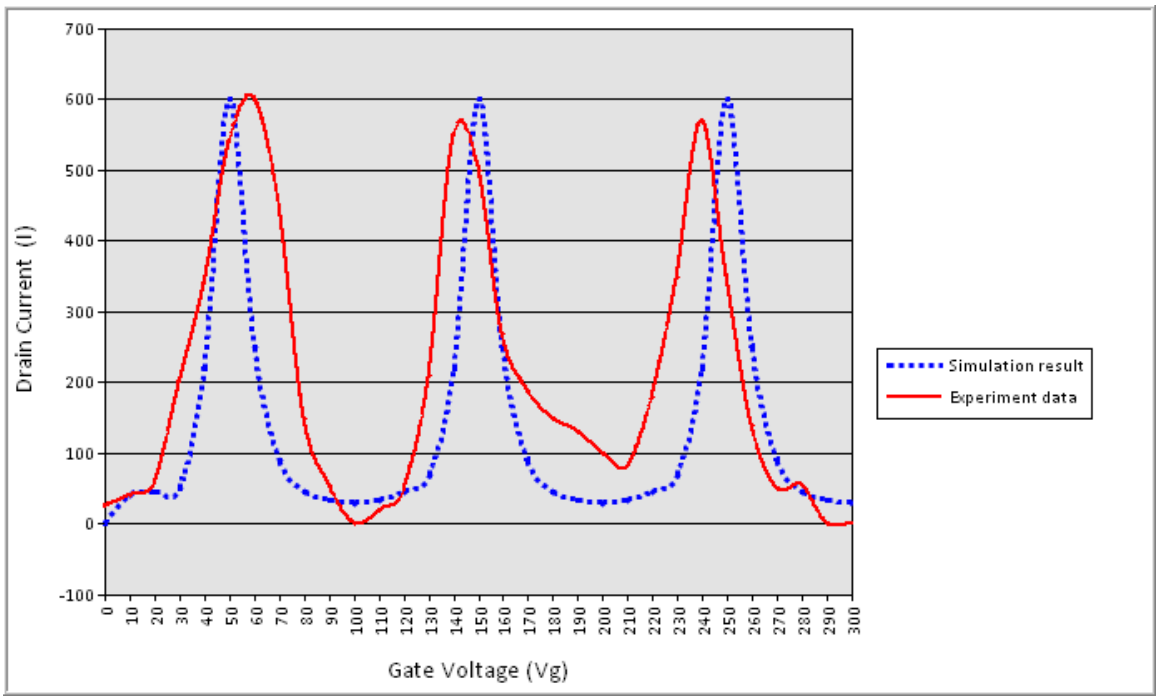

Fig. 3.8: I-V profile comparison of proposed model with experiment data [62].

Simulation result of Modified SET model parameter:

The resultant characteristics curve of SET is shown in the figure 8. It is clearly seen that the modified model produce a more realistic coulomb oscillation with distinct peaks and troughs unlike the previous models.

3.4 I-V characteristics comparison

In modeling the Single Electron Transistor the main motive is to find a suitable simulation result that produce distinct coulomb oscillation with sharp peaks and smooth valleys. The simulation results in Fig. 3.7 and Fig. 3.8 show the difference in existing macro model and the proposed model, respectively. In the existing macro model there are two issues with the I-V profile of SET-

a) The large DC offset of current and
b) The absence of sharp peaks.

In Fig. 8, the simulation result with the proposed model, the peaks are sharper compared to the existing model and the DC offset has been effectively minimized.

Throughout the next chapters of this dissertation the model used is the proposed model that produces sharp peaks with only a very small DC offset.

CHAPTER 4

NOVEL APPLICATION OF SET- A PHASE MODULATION CIRCUIT SIMULATION RESULTS AND DISCUSSION

4.1 Introduction

In this chapter it will be described how coulomb oscillation of Single Electron Transistor (SET) can be used to form variable transconductance region of operations. The variable transconductance region of SET consists of a positive and a negative part. In this chapter it will be also described how to bias a circuit to achieve that condition and at the end circuit setup and results will be discussed.

4.2 Transconductance and Negative resistance application of SET

Transconductance is a property of certain electronic components like transistors, is the ratio of the current change at the output port to the voltage change at the input port. It is written as g_m. For DC signal, transconductance is defined as follows:

$$g_m = \frac{\Delta I_{out}}{\Delta V_{in}}$$

For small signal alternating current, the definition is more simple:

$$g_m = \frac{i_{out}}{v_{in}}$$

The transconductance curve (transfer characteristics) of industry used typical MOSFET is shown in figure below

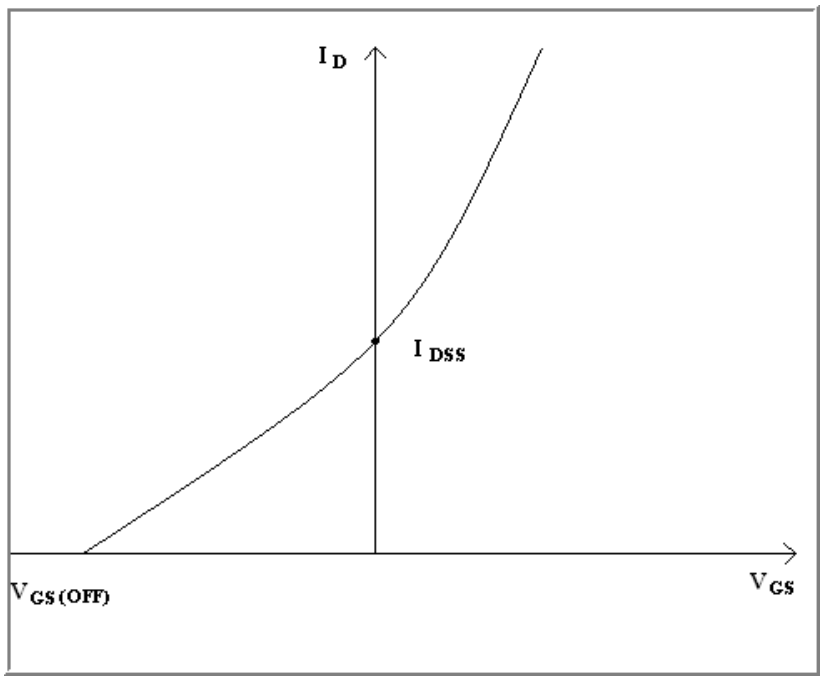

Fig : 4.1 (a) Transconductance of MOSFET

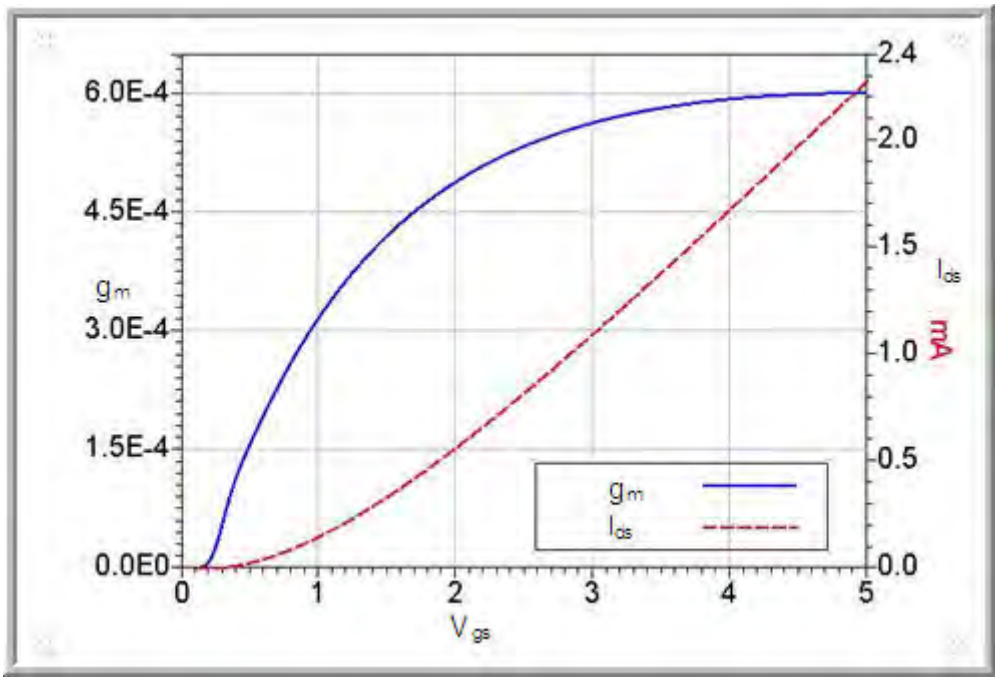

Fig : 4.1 (b) Transconductance of MOSFET from simulation

The characteristic curve shows the variation of I_D with V_{GS}. I_{DSS} denote the drain current with shorted gate. The curve extends on both sides i.e. V_{GS} can be negative as well as positive.

A transistor has three regions of operation- the ohmic region, active region and breakdown region. The rising position of the drain characteristics is the ohmic region. The device acts as resistor. The drain current is nearly constant in the active region. When V_{DS} exceeds the rated value, avalanche breakdown occurs. This device has two applications i.e. as a resistor or a current source.

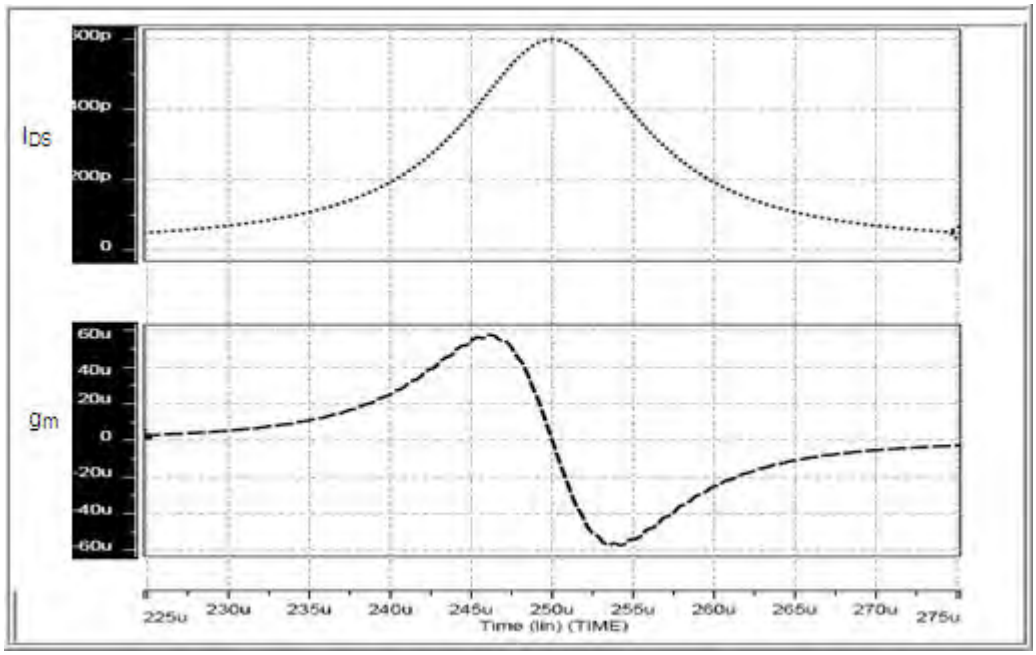

Fig. 4.2 : Coulomb oscillation and negative transconductance of SET

Fig. 4.2 shows the simulation result of one event of the coulomb oscillation along with the derivative of current with respect to gate voltage which is actually the transconductance (g_m) of the Single electron transistor. As shown in top graph in figure 4.2, the drain current (I_{DS}) varies with respect to the gate voltage and shows a maxima because of the Coulomb oscillation. In the second graph of the Fig. 4.2 shows the dv/dt of I_{ds} and shows both maxima and minima.

If we may compare the transconductance curve of a typical MOS transistor shown in Fig. 4.1(b) and that of a SET shown in the Fig 4.2 it is very much evident that the transconductance curve of SET is extended forward significantly both in positive and negative sides of the axis. This means there is a completely new dimension added in the SET g_m curve.

If we have a close looks at the first half of one cycle of coulomb oscillation, we find current is increasing during this period, which resulted a positive slope in the Fig 4.2,

hence positive transconductance for this half cycle. As the peak of the current (I_{ds}) is reached the derivative become zero and transconductance will be zero at the point.

In the second half of the coulomb oscillation cycle current starts to decrease which means transconductance become negative. During this 2nd half cycle of the curve transconductance goes a negative peak and remains negative in the complete period. This is a completely new and unique phenomena of the Single Electron Transistor (SET)

The circuit is suitably chosen to set the operating point Q so that it traverses between points of maximum g_m (positive) and minimum g_m (negative).

4.3 Circuit descriptions and theory of operation

The circuit setup for an application of SET with theory of operation is discussed in this section. Fig 4.3 shows the circuit setup for the phase modulation circuit implemented with a Single Electron Transistor.

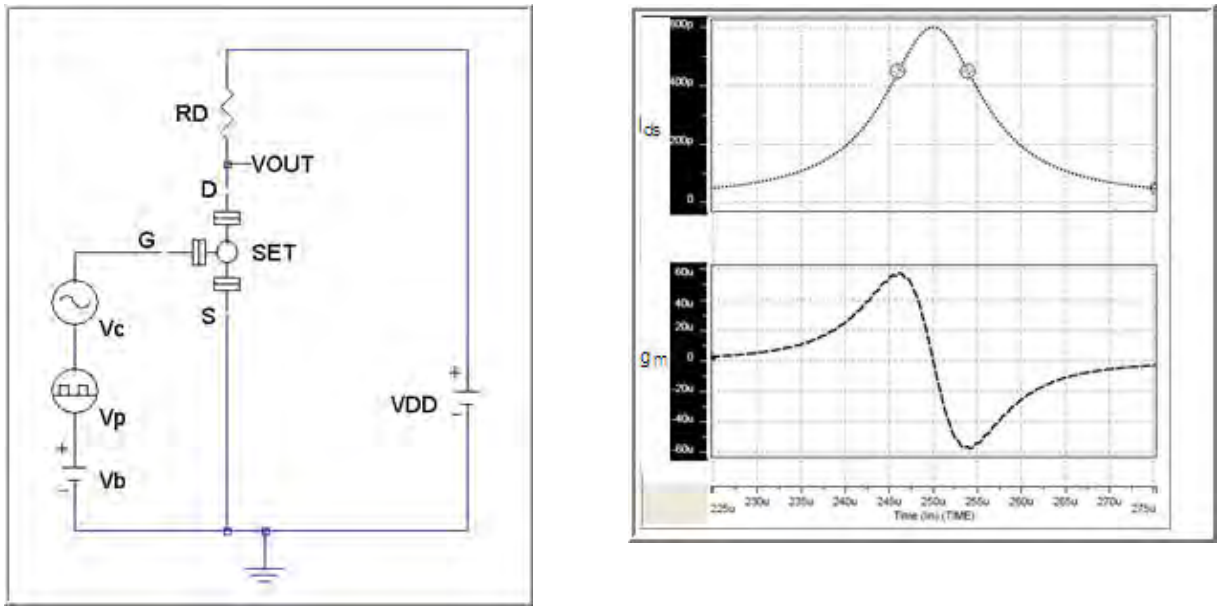

Fig: 4.3 : circuit setup for the phase modulation circuit and simulation results

The SET is biased with V_B so as to operate at the rising or negative slope of the i_{ds} namely particularly at operating points Q1 and Q2 . The Vp is the information signal is to be modulated. Information signal is connected with a high frequency carried signal for the modulation of V_p. Now, considering digital modulation, the rail to rail difference of

the information signal pulses has to be perfectly scaled down to match the difference between operation points Q1 and Q2 instead of the conventional rail to rail difference of 5V. This can be achieved through various mechanisms. When the information bit contains a '0' (zero) the transistor will operate at Q1 and when the information bit contains '1' the transistor will jump to the new operate point at Q2. It's worth mentioning here that the Q1 lies at the positive slope (hence positive g_m) side of the i_{ds} and the point Q2 lies on the negative slope (and hence negative g_m) side of the i_{ds} curve.

The carrier signal V_c has to of very small peak to peak value so as to ensure that when the SET operates at Q1 [information bit contains a '0'] the signal can be properly amplified by the transistor, that is, the variation of carrier signal at that point should be small enough so that the variation of g_m can be considered negligible over the full swing of the carrier signal. The same is true when SET is operating at the point Q2[information bit contains a '1'].

The drain of the SET is connected to a high impedance node shown as a resistance in the Fig 4.3. The value of the resistance can be adjusted to choose the expected gain of the system.

4.4 Biasing Sensitivity

The biasing of the circuit is the most critical part since the region of operation is very narrow. There are three major concerns.

a) DC biasing of the gate voltage
b) Amplitude of the carrier signal
c) Amplitude of the information signal

a) DC biasing of the gate voltage

The SET is biased with V_B so as to operate at circuit at the rising slope of the coulomb oscillation which is shown as operating point Q1 in Fig. 4.3.The biasing is crucial since shifting the bias point either way will reduce the gm of the circuit and hence reduce the gain.

b) Amplitude of the carrier signal

It is required for the circuit to operate properly that amplitude of the carrier signal is chosen properly. The carrier signal V_C has to of very small peak to peak value so as to ensure that when the SET operates at Q1, the peak to peak variation of the carrier signal remains confined not to cross the peak of the coulomb oscillation. Because on the other side of the peak of coulomb oscillation the g_m becomes negative. Moreover, for maximum performance the gm variation of an amplifier has to small, for which is it better to keep the peak to peak variation small enough so that within the variation of carrier signal the

gm doesn't vary too much. In this specific simulation setup we have kept the amplitude of the carrier limited to ±1mV.

c) Amplitude of the information signal

The amplitude of the information signal is of critical importance. Usually the amplitude of the digital information signal varies between 0 and 5V. But for this SET based phase modulation circuit the binary pulse height has to scaled down to the difference of the operating points Q1 and Q2. With this pulse amplitude, the SET will be operating at point Q1 when the binary pulse is '0' and when the binary pulse is '1' the transistor will operate at point Q2.

The scaling down of binary pulse amplitude can be achieved by creating a different rail to rail voltage reference. Different level shifting circuits are available to perform this particular task.

4.5 Simulation Results and Discussion

The simulation is done using the model described in Chapter 3 (SPICE model for SET) in HSPICE software. The circuit shown in Fig. 4.3 used with proper biasing condition so as to satisfy different requirements stated in previous section (section 4.3). As shown in Fig 4.4 (a) signal is the modified digital data pulse that is intended to be modulated.

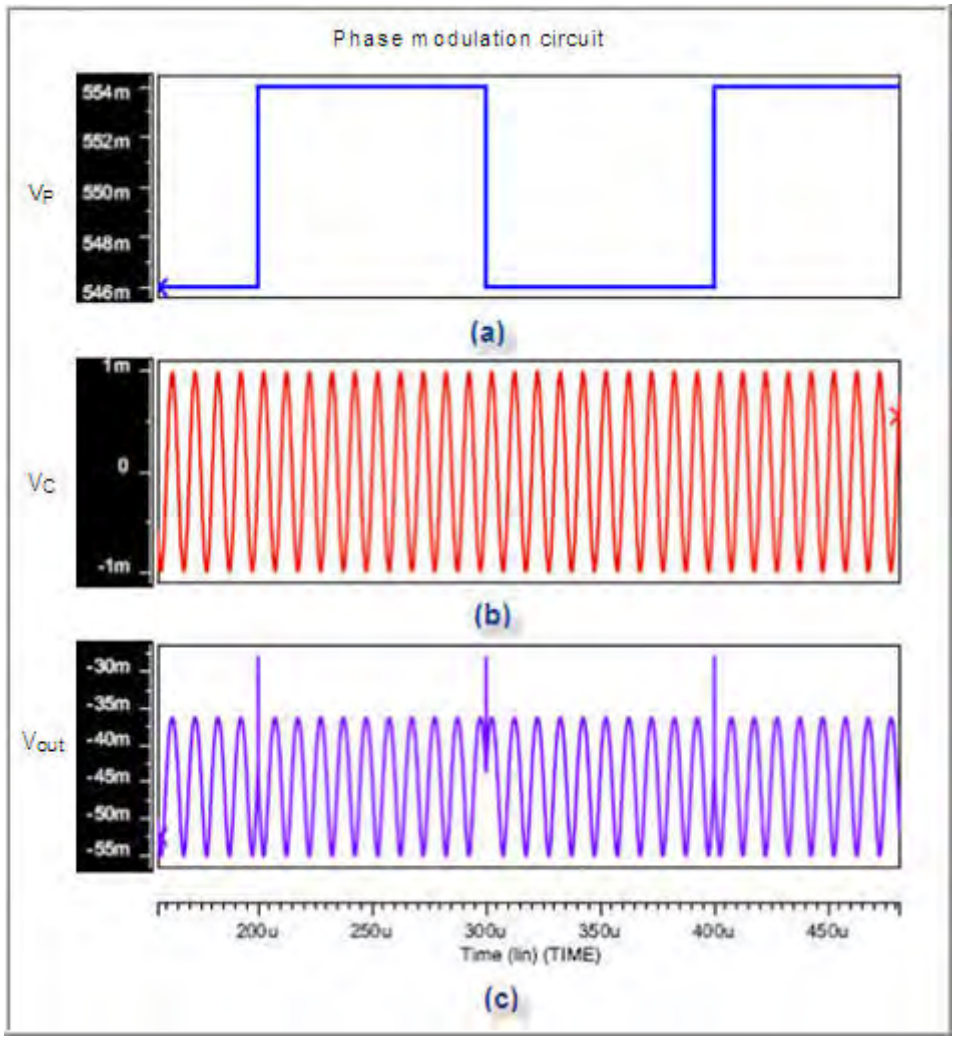

Fig. 4.4 : output of the SET based phase modulation circuit

Fig 4.4(b) is the carrier signal whose phase is being modulated according the information bit. The output of the phase modulator is shown in the Fig 4.4(c) that the phase of the carrier is actually modulated at the transition of the data pulse. The rail to rail movement of the data bit shown in the top portion is scaled down suitably to ensure that complementary operating points of the SET I-V profile so as to generate positive and negative g_m values at bits '0' and '1', respectively.

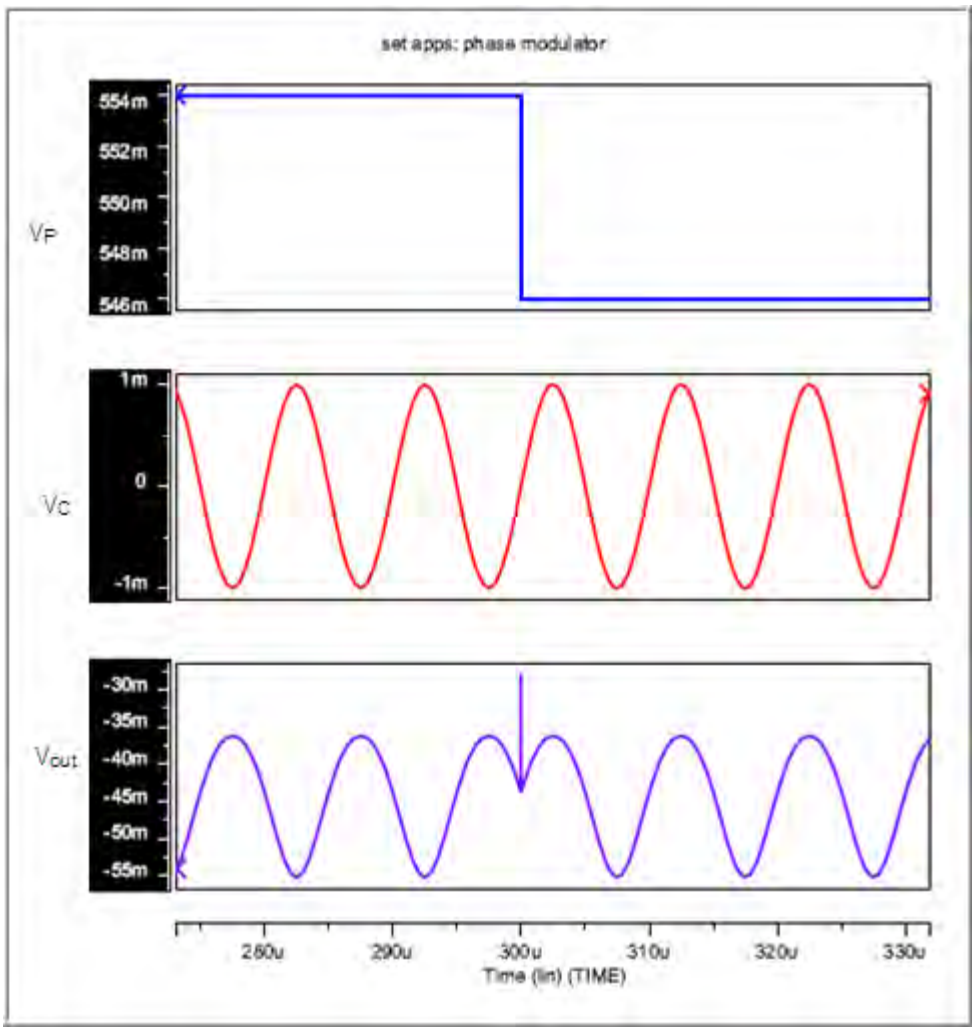

Fig. 4.5: output of the SET based phase modulation circuit (zoomed in view)

In the magnified view in Fig 4.5 it is shown very clearly that as the information bit goes from state '1' to state '0', the output of the circuit is phase modulated career signal to achieve the goal of this SET application circuit.

CHAPTER 5

CONCLUSION

This work focuses on modeling of a Single Electron Transistor and application of the single electron transistor which is considered as a promising nano-electric device to meet the ever increasing demand of the new millennium. A quantum mechanical model and a macro have been studied and finally the macro model has been modified to exhibit the coulomb oscillation of the single electron transistor (SET). In the original model the crest and trough are not distinctly visible.

A novel circuit application of SET is proposed and simulated. The circuit exploits the unique characteristics of SET of having bi-signed transcoductance (g_m) nature by wisely choosing the operating point. Here a specific circuit setup is proposed using single electron transistor which will act as a phase modulator. The main function of the phase modulator will be to detect the change of signal level of the incoming signal (high & low) that is fed to the gate of the SET device and able to produce phase modulation of the career signal.

The novel SET bases phase modulator will find its application in many communication circuits and will be equally possible to use in high end research projects. Such an application is also focused in this work. Since almost every form of communication signal handing system always convert the original signal to a modulated signal for further processing and increase gain of the transmitted signal, phase modulator is one of the most common of all elementary communication circuit configurations. The SET based digital signal phase modulator circuit proposed in this thesis work is the most simplified for such circuits used so far. It is seen from the simulation data that SET based digital signal phase modulator circuit performs very efficiently to convert digital pulse to modulated signal.

Single electron transistor is being studied extensively all over the world – in universities and in industries. The potential it possesses has merely been started to be revealed. The outstanding characteristics of this quantum device will be uncovered soon.

Phase modulation is one the most common type of modulation techniques used in communication engineering. In the advanced communication circuits there are more complex type of modulations are used to have higher efficiency in the bit rate or symbol rate like QPSK. One very useful work would be designing of phase modulation circuit using SET for higher degree of modulation for better throughput.

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