DESIGN AND ANALYSIS OF AN ACTIVE LOW LOSS TECHNIQUE FOR SERIES ELECTROLYTICS TO MAINTAIN HIGH DC BUS VOLTAGE OF A CONVERTER

By

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The thesis titled **"Design and analysis of an active low loss technique for series electrolytics to maintain high dc bus voltage of a converter",** submitted by Muhammad Mohsiul Haque, Roll No. 040506103P, Session April 2005 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of Master of Science in Electrical and Electronic Engineering on 21st September 2010.

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Declaration

I, do, hereby declare that neither this thesis nor any part of it has been submitted elsewhere for the award of any degree or diploma.

Signature of the candidate

Muhammad Mohsiul Haque

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Acknowledgement

At first, I would like to dedicate all my regards to Almighty Allah (swt), the most kind, for allowing me to complete the work successfully.

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Abstract

In this thesis, analysis of an active low loss approach to maintain the DC voltages across series connected electrolytic capacitors used in a converter is presented. The proposed design mitigates the impact of leakage current dispersion, which causes voltage imbalance among capacitors. In traditional method, a passive balancing circuit is often used, where balancing resistors are usually connected in parallel with the capacitors. However, the current flowing through the resistors is much higher than the leakage current of the capacitors and cause high dissipative loss. An active balancing circuit is proposed in this thesis, which ensures the capacitor voltages at desired values without unreasonable increase in the power loss. The circuit is designed using both two and four electrolytic capacitors in series connection to divide the dc bus voltage. For the ease of design and analysis, an application of both two and four equal voltages across capacitors is considered. Here, the control circuit is designed using op amps to compensate the voltage imbalance occurred among capacitors. Simulation results for impacts of various leakage currents as well as load variation and improvements after applying the proposed technique are discussed.

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Chapter3

Introduction

1.1 Introduction

Presently, applications of voltage converters using electrolytic capacitors are common in electronic equipments such as process control, manufacturing, factory automation, telecommunications,UPS,drives and server power supplies.To maintain fullDC bus voltage of these converters, the electrolytic capacitors areequipped with an arrangement of two ormore series-connected electrolytic capacitors rated at lower voltage.But, an electrolytic capacitor is not an ideal capacitor and has significant leakage current.The leakage current of capacitors typically differ from one to another,which mean that the supply voltage is not divided proportionately across the capacitors.To compensate the large dispersion of the leakage current and ensure desired sharing of the total dc bus voltage among the series-connected capacitors, a passive balancing circuit is often used, in which balancing resistors are usually connected in parallelwith the capacitors.But,the current flowing through the resistors ismuch higher than the leakage current of the capacitors and cause high dissipative loss.These balancing loss results into a considerable additional energy cost.So,ordinary balancing circuits have disadvantages such as large weight, size and loss.Another drawback of the ordinary passive balancing circuit is the standby power consumption. For example, a 400V 10kW converter equipped with the ordinary balancing circuit consumesmore than 200kWh standby energy over one year.The standby consumption nowadays becomesmore and more in the focus.Developpment engineers are permanently looking for some new andmore efficient circuit.

1.2 Electrolytic Capacitor

An electrolytic capacitor is a type of capacitor that uses an electrolyte, an ionic conducting liquid, as one of its plates, to achieve a larger capacitance per unit volume than other types. They are often referred to in electronics usage simply as "electrolytics". They are used in relatively high current and low frequency electrical circuits, particularly in power supply filters, where they store charge needed to moderate output voltage and current fluctuations in rectifier output. There are two types of electrolytic: aluminum and tantalum.

Electrolytic capacitors are capable of providing the highest capacitance values of any type of capacitor. However they have drawbacks which limit their use. The voltage applied to them must be polarized; one specified terminal must always have positive potential with respect to the other. Therefore, they cannot be used with AC signals without a DC bias. They also have very low breakdown voltage, higher leakage current and inductance, poorer tolerances and temperature range, and shorter lifetimes compared to other types of capacitors.

By combining small size and very low cost per unit capacitance, electrolytic capacitors (hereafter called electrolytics) are the only cost-effective choice for high-value applications like power supply filtering in most consumer devices. However, electrolytics have huge leakage and dielectric absorbtion. With regular use, electrolytics fail with age by drying out or leaking electrolyte following internal corrosion.

There are two types of leakage; physical and electrical. Since the electrolyte is a liquid or paste, when an electrolytic catastrophically fails it usually oozes some corrosive goop called physical leakage. Unlike an ideal capacitor, electrolytics slightly conduct when there's voltage across the plates called electrical leakage. Other than being a deviation from ideal behavior, the small leakage in new electrolytic causes no major problems; as the electrolytic ages, the leakage increases[1].

1.2.1 Electrical behavior of electrolytic capacitor

A common modeling circuit for an electrolytic capacitor has the following schematic:

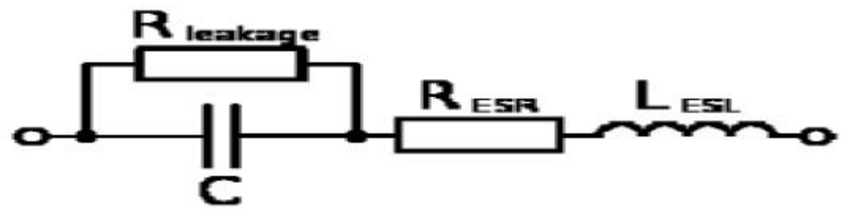


Fig 1.1: Schematic circuit for an electrolytic capacitor.

Where, $R_{Leakage}$ is the leakage resistance, R_{ESR} is the equivalent series resistance (ESR), L_{ESL} the equivalent series inductance (L being the conventional symbol for inductance).

R_{ESR} must be as small as possible since it determines the loss power when the capacitor is used to smooth voltage. Loss power scales quadratically with the ripple current flowing through and linearly with R_{ESR}. Low ESR capacitors are imperative for high efficiencies in power supplies. Low ESR capacitance can sometimes lead to destructive LC voltage spikes when exposed to voltage transients.

This is only a simple model and does not include dielectric absorption and other non-ideal effects associated with real electrolytic capacitors.

1.3 Series Connected Capacitors and Leakage current discussion

Insufficient voltage ratings can be a problem, and series-connection may be the only way to obtain electrolytics with a high enough voltage rating. Few modern styles electrolytic are available with voltage ratings above 450V, including LCRs (500V) and Sprague Atoms (600V). Series-connection requires addition of so-called "bleeder" or *voltage balancing resistors*, one across each capacitor, conducting a current that keeps the voltage across the series capacitors balanced. Even brand new high quality electrolytic capacitors conduct to some degree.

This leakage current depends on the quality of the electrolyte, temperature and condition of the capacitor, and can be represented by a resistance in parallel with the capacitor. In the Fig 1.2, series-connected capacitors C_1 and C_2 have some leakage resistance R_{L1} and R_{L2}. Because of the wide tolerances of electrolytics, this leakage current varies from sample to sample, and by Ohm's law, affects the voltage balance between electrolytic capacitors connected in series.

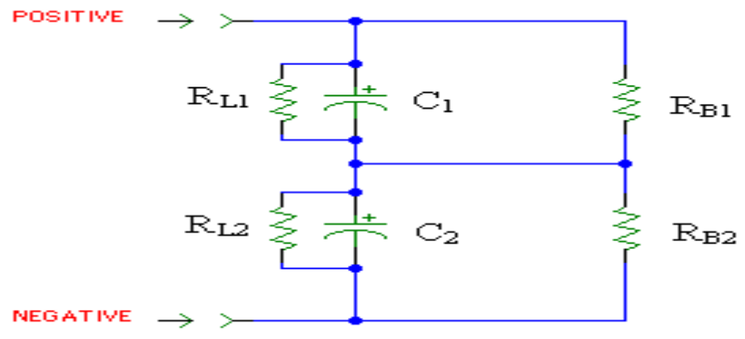


Fig 1.2: Voltage balance between the series capacitors.

Balance resistors R_{B1} and R_{B2} keep the voltage balance between the series capacitors within tolerance by including another larger current in parallel with the leakage current. The balancing current is chosen large enough to overwhelm any leakage imbalance and thereby to guarantee safe operation. To calculate the value of the balancing resistors, the approximate maximum leakage of the series-connected capacitors is determined first. The leakage current in µA ranges from 1/5* $\sqrt{}$(CV) to 1/2* $\sqrt{}$(CV) according to Nichicon, with C in µF, V in volts and current in µA. Leakage specifications can also be available from capacitor's data sheet. One common rule-of-thumb for the balancing current is 10x the leakage current, thus for two 100µF/350V capacitors connected in series to form a 50µF capacitor, maximum leakage of 1/2* $\sqrt{}$(100*350) = 94µA, times 10 is about 1 mA. If the applied voltage is considered to be 650V, then R_{B1} and R_{B2} = 325K? . Power dissipation of I*V = 0.325W, so a minimum 1W resistor would give an adequate safety margin. It is required to check the voltage rating of any balancing resistors too.

It could be thought that two 350V electrolytics connected in series would have a voltage rating of 700V, but the loose tolerances of electrolytics again interferes. As pointed out in the Evox Rifa electrolytic capacitor application note, series capacitors act as a capacitive voltage divider, and N electrolytics connected in series with a capacitance tolerance range of C_{min} to C_{max} have a maximum divided voltage (at the junction of the two capacitors) $V_{div} = (V_{applied} * C_{max}) / (C_{max} + (N - 1) * C_{min})$. In this example, with a ± 20% capacitance tolerance, C_{max} = 1.2*100 and C_{min} = 0.8*100, with V_{div} = (650*120)/ (120 + (2-1)*80) = 390V. This exceeds the voltage rating of the electrolytics by 40 volts; with some algebra it is found that 350+350 gives a 583V maximum when the capacitive tolerance is 20%. For the applied voltage of 650V, the minimum voltage rating for each capacitor would need to be 400V.

In the application note, Nichicon presents a more precise calculation of the balancing current than the 10x-leakage rule given above. Let, $V_{diff} = (V_{max} - V_{min})$ be the difference in operating voltage resulting from leakage imbalance for the two electrolytics in series and $I_{diff} = (I_{max} - I_{min})$ is the maximum difference in leakage current between the two capacitors, then $R_{B1} = R_{B2} = V_{diff} / I_{diff}$. Using the current range given above, $I_{diff} = 0.3* \sqrt{(CV)}*T_c*F$, where T_c is a temperature coefficient and F is a fudge factor. Electrolytics conduct more as the temperature increases, with T_c at 20^0C of 1, increasing to 2 at about 60^0C and 5 at about 85^0C. Again, this characteristic can be found in capacitor's data sheet. The fudge factor is an arbitrary safety factor of an extra 40%, thus for our example at 60^0C, I_{diff} $0.3*\sqrt{(100*400)}*2*1.4$ = 168µA. Nichicon picks an arbitrary V_{diff} of 10% of the capacitor rating, but by knowing the intended application a better worst case estimate can be made.

If it is considered that, the worst case voltage imbalance due to leakage current between the series capacitors increases with decreasing balance resistor current. Thus the larger an imbalance can be tolerated, the smaller balance current can be applied. If the capacitive tolerance is not ignored, it is must to add the capacitive and leakage effects to get a valid worst case estimate of the voltage imbalance. Using two 400V/100µF series connection operating at 650V, the worst case voltage imbalance due to the capacitive tolerance of 20% is 390 - 260 = 130V. This imbalance can increase due to leakage by 20V to (400 –

250) = 150V, and balancing resistance = V_{diff}/I_{diff} = 20V/168µA = 120K? or balancing current = (320/120K) = 2.7mA. This indicates 0.9W per balance resistor requiring two 2W or larger power resistors. A better solution would be to increase the voltage rating to 450V, resulting in a small increase in leakage current difference (10µA) with an increase in voltage imbalance tolerance by 100V. Then, balancing resistance = V_{diff}/I_{diff} = 120V/178µA = 675K? or balancing current = 320/675K = 480µA at 0.16W. It may also be worthwhile to match devices to minimize capacitive imbalance, although some tolerance should remain to accommodate possible changes in the characteristics of ageing capacitors.

Since 450V is the highest readily available electrolytic voltage rating, for voltages much over 650V the number of series-connected capacitors should be increased. With three 450V series-connected capacitors and 20% capacitive tolerance, the maximum operating voltage is 450*(120 + 2*80)/120 = 1050V. Choosing an operating voltage of 900V, with a nominal 300V across each capacitor, if two capacitors operate at their lowest voltage and one at its highest, then V_{max} = 1.2*900/ (1.2 + 0.8 + 0.8) = 346V. Here V_{diff} = 2*(450-346) and I_{diff} is still 178µA, thus, balancing resistance = V_{diff}/I_{diff} = 1.2M? or balancing current = 300/1.2M = 250µA.

For multiple identical series-connected electrolytic capacitors:

- The sum of the voltage ratings should be 30-40% higher than the applied voltage.
- A voltage-balancing resistor network is required, and the balance current need be no more than about 1mA.

The 10 times of leakage rule makes no assumptions about the voltages of the capacitors in use, providing a conservative requirement, although not considering the voltage imbalance due to capacitance and leakage current tolerances. A more thorough analysis will guarantee that the voltage ratings of the series connected capacitors are safely within worst case limits. The manufacturer's recommendations point out the factors that affect the capacitor balance e.g. temperature, range of leakage current, capacitive tolerance, voltage range and these factors should be considered in selection and installation [1].

Finally, as an effect of the "electro-chemical origin" of electrolytic capacitors, the leakage current is largely dependent on operating temperature and aging conditions of the component. It should be noted that if the capacitor voltage is increased to values being higher than the specified surge voltage, the "leakage" current increases rapidly due to the re-starting of the reforming process (growing of the oxide layer) which will take place [2]. Furthermore, at normal operation conditions (voltages below the surge level) the leakage current may be much higher than the specified value for the first minutes after the voltage is applied ("inrush current"). This is especially true after a longer period of voltage-free storage of the component (oxide layer deterioration). But also the normal operation leakage current approximately doubles its value for each 20°C temperature increase. The typical operating leakage current of power electrolytic capacitors can be calculated using the formula as below [2]

$$I_{l,op} = 0.0005\mu A \cdot \frac{C}{\mu F} \cdot \frac{V_R}{V} + 1\mu A \qquad \ldots\ldots\ldots \quad (1.1)$$

(V_R is the rated voltage) valid for long-life (LL) types at 20°C. The maximum leakage current ("acceptance test" according to standard EN 130 300), however, is limited to

$$I_{l,\max} = 0.3\mu A \cdot \left[\frac{C}{\mu F} \cdot \frac{V_R}{V}\right]^{0.7} + 4\mu A \qquad \ldots\ldots\ldots (1.2)$$

valid also for 20°C (for 35°C this permissible limit has to be multiplied by a factor of 2.5).

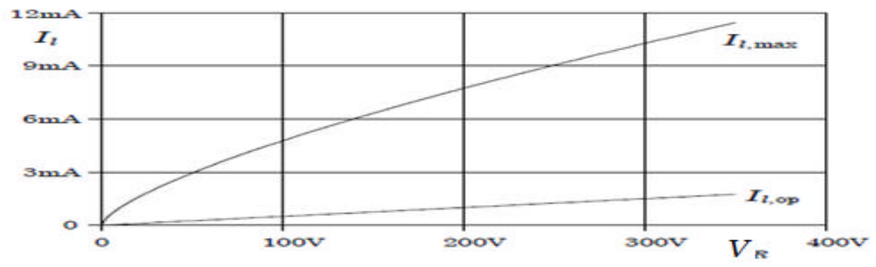


Fig 1.3: Typical and maximum leakage currents of a 10000µF LL-grade electrolytic capacitor according to Equations (1.1, 1.2).

1.4 Specified leakage current and operating leakage current

In the ideal case the leakage current I_L of an electrolytic capacitor depends on the capacitance value of the capacitor, the applied voltage, a constant adder and, particularly important, on the measuring time. Normally the leakage current of an electrolytic capacitor is therefore specified with a formula that contains the capacitance C_R and the rated voltage V_R and which defines the limit value of the leakage current after a certain measuring time (in this case 2 and 5 minutes), for example using the following formulae:

- $I_L (2\,min) < (0.01 * V_R * C_R) + 3\,\mu A$
- $I_L (5\,min) < (0.002 * V_R * C_R) + 3\,\mu A$, for $V_R = 100\,V$
- $I_L (5\,min) < (0.01 * V_R * C_R) + 3\,\mu A$, for $V_R > 100\,V$
- or, in accordance with EN 130300

  $I_L (5\,min) < (0.3 * V_R * C_R) 0.7) + 4\,\mu A$

However, every manufacturer uses his own calculation formulae, most of which also differ from series to series. The leakage current value calculated with the relevant formula defines the maximum value after the elapse of the measuring time after the rated voltage has been applied. Normally the value of the leakage current will be much smaller [3].

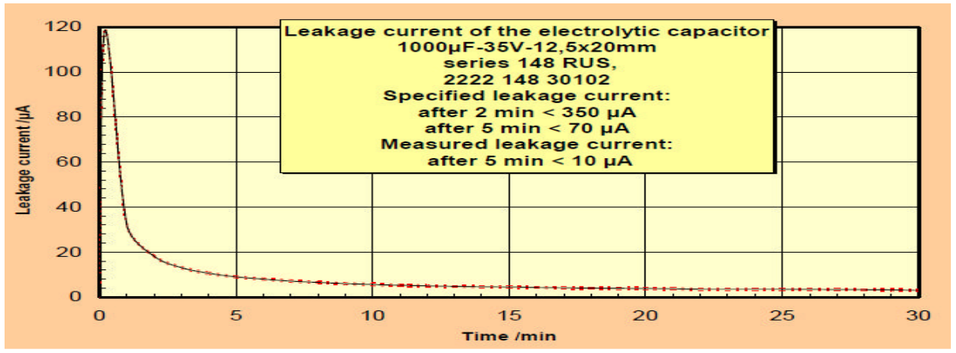


Fig 1.4: Typical time behavior of the leakage current of an aluminium electrolytic capacitor after switching on.

As shown in the curve in Fig 1.4 shows, the leakage current after 5 minutes is far lower than the 5 minute acceptance limit value of 70 µA. And in this example the measured leakage current

value approaches a constant, small value of around 5 to 10 µA on an asymptotic basis. This final value is known as the operating leakage current and has usually established itself after around one hour. After this time all the weaknesses in the dielectric of the electrolytic capacitor of the modern professional electrolytic capacitor supplied today have been healed and the leakage current has declined to a permanent low value. The leakage current value after 2 or 5 minutes, the so-called acceptance value, is relatively high compared to the curve shown in Fig 1.3.

Users expect and generally also receive relatively stable electrolytic capacitors today in terms of their leakage current properties. "Relatively" because the leakage current values of film capacitors or ceramic capacitors can obviously not be achieved by electrolytic capacitors. The leakage current of an electrolytic capacitor is generally considered to be at a much higher level. This is due to the fact that the 5 minute value for the leakage current specified in data sheets is generally several factors higher than the actual operating leakage current. And the operating leakage current will not be reached, of course, until the capacitor has been operating for a certain length of time, until in fact the weaknesses in the dielectric have been healed properly. The longer the voltage is applied to the capacitor, the lower the leakage current will be as shown in Fig 1.5. How remarkably low the leakage current may be on good quality professional goods these days is shown clearly by a simple test. First of all, an electrolytic capacitor is charged to its rated voltage and then it is disconnected from the power source. Then the remaining voltage on the electrolytic capacitor is measured at hourly intervals. Since the leakage current ensures that the capacitor suffers constant trickle discharge, after a certain time the measured voltage should have fallen to zero.

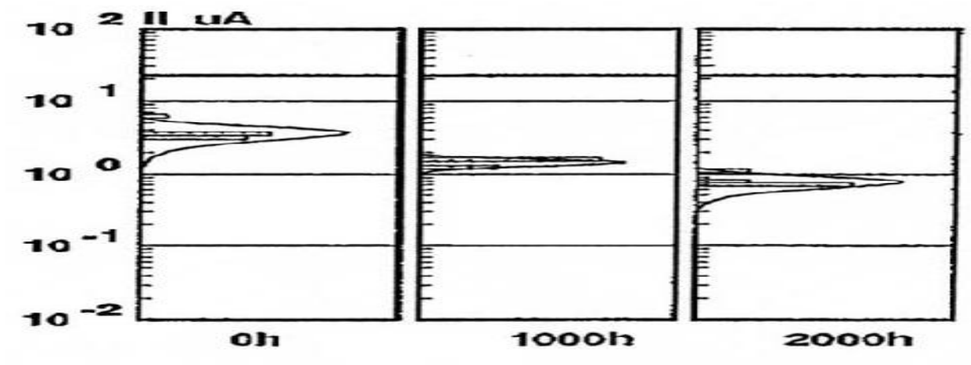


Fig 1.5: Leakage current properties of electrolytic capacitors during a 2000 hours life test. The longer the voltage is applied to the capacitor, the lower the leakage current becomes.

1.5 Voltage and temperature dependence of the operating leakage current

As the example described above shows, the operating leakage current is several factors lower than the acceptance value specified in the relevant data sheets. General specifications for the operating leakage current in the form of formulae in the literature contain massive fluctuations. But this is hardly surprising when we consider that the quality of professional electrolytic capacitors has improved massively in terms of leakage current over the last 20 years.

A leakage current value of around 10 µA for a 1000 µF electrolytic capacitor at 35V (as shown in Fig 1.3) is therefore by no means uncommon. However, this value is also not stable. The operating leakage current of an aluminium electrolytic capacitor with non-solid electrolyte is extremely dependent on the temperature and voltage. These properties are understandable and can be explained easily using the model of the activation energy. The level of the operating leakage current under operating conditions can be calculated in approximate terms using the factors I_{op} / I_L shown in Fig 1.6 and Fig 1.7 below [3].

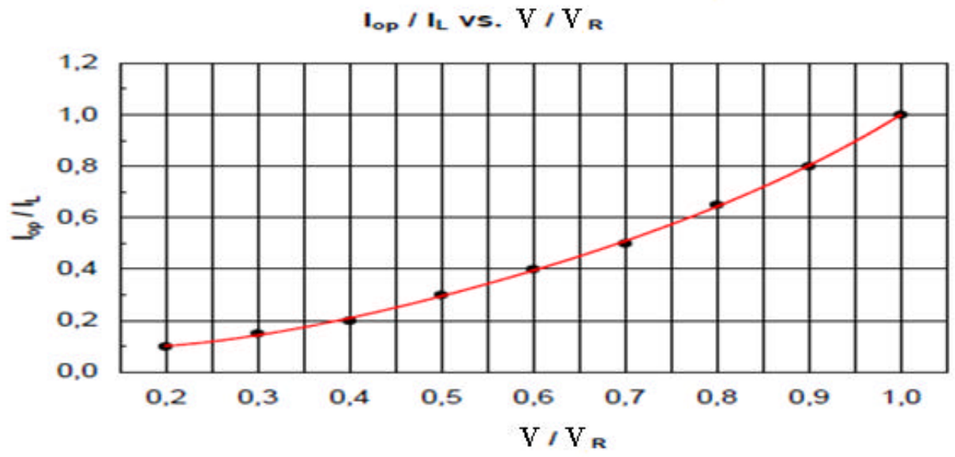


Fig 1.6: Typical multiplier of the leakage current as a function of the voltage applied

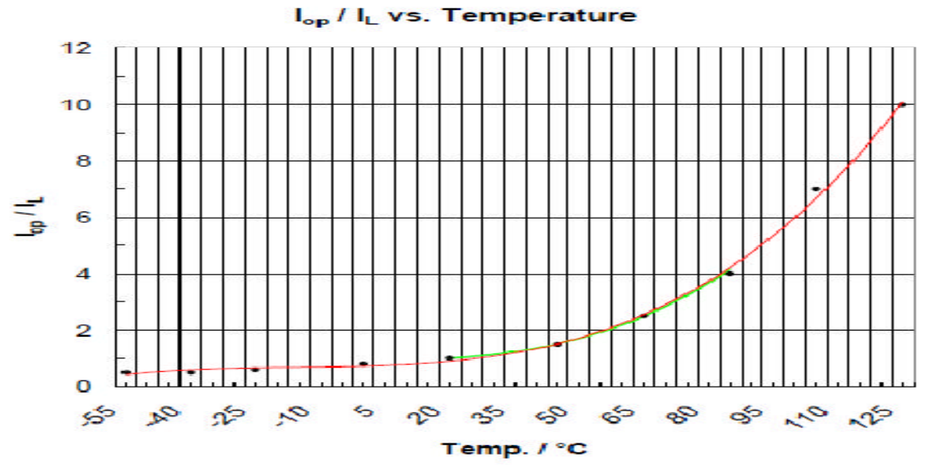


Fig 1.7: Typical multiplier of the leakage current as a function of the capacitor temperature

1.6 Three main causes that damage the electrolytic capacitor

1. Overvoltage: If the specified voltage is exceeded, current will leak through the isolation, not in a slow way that might regenerate weak areas, but violently, creating hot spots where additional break-down occurs. The danger of explosion is imminent.

2. Reversed polarity: As described, the inverse of regeneration i.e. self destruction will occur. If the applied voltage is near the normal (right polarity) working voltage, break down is quick and violent. The effect of a low inverse voltage might be reversible.

3. Temperature: Temperature shortens the life of an electrolytic capacitor. A good rule of thumb is that every $10^{0}C$ over $85^{0}C$ will cut the life expectancy in half[4].

1.7 Influence of Leakage current on electrolytic capacitor

Many manufacturers also issued instructions and even formulae that describe the influence of the level of the applied voltage on the expected useful life. Since we now know that the level of the applied voltage co-determines the level of the leakage current, it can certainly be assumed that voltage influences useful life. After all, the leakage current is also a measure of the forming work that takes place over the entire life time of the capacitor. Since this forming work ultimately withdraws oxygen from the electrolyte and uses it to repair damaged or weakened oxide layers, the electrolyte is therefore consumed. And the loss of electrolyte determines the useful life of the electrolytic capacitor on the basis of the conventional model. On a purely theoretical basis, therefore, if the full rated voltage is applied to the electrolytic capacitor, the component should offer a shorter useful life than if a lower voltage was to be applied. However, if it is considered the physical causes of the electrolytic capacitor leakage current, it is likely that only part of the leakage current will be found in the form of forming work. The remainder of the electrons will tunnel through the dielectric using tunnelling effects or will flow in the form of cross current through electrolyte films around the rubber seal, in other words they will have no influence whatsoever on the possible loss of electrolyte. If the level of the leakage current is taken into account it can be concluded that the influence of leakage current on useful life is in fact rather low. This certainly applies to electrolytic capacitors in the voltage range up to around 100 V (low voltage) and for electrolytic capacitors with solvent, non aqueous electrolytes. For these capacitors the small mechanical variations in the sealing capacity of the gaskets and

therefore the distribution of the expected electrolyte loss over the useful life is definitely more significant than the level of the applied voltage and the leakage current related to it.

Connecting electrolytic capacitors in series results in the voltage being split between the components and in turn this is influenced by the leakage current difference between the individual capacitors in a series. It is therefore very important that the leakage current differences are balanced in the circuit design since even very small differences can cause problems. These differences normally become apparent when the circuits are activated in the form of overvoltage on the component with the lowest leakage current. Since considerable fluctuations can be found between individual capacitors from the same production batch in terms of their leakage currents, it is also possible that large voltage differences may occur. It is observed that voltage increases across the capacitor with lower leakage current. If this results in exceeding the rated voltage of a capacitor, under certain circumstances this can result in premature failure [3].

1.8 Traditional Method

1.8.1 Passive Voltage Balancing

For passive capacitor voltage balancing the two resistors R_B form a voltage divider and a perfect voltage distribution $V_{C1} = V_{C2}$ would be given in case of zero output current ? $I = 0$ (Fig 1.8). The output current, however, is defined by the leakage current difference ? $I = I_{lC2} - I_{lC1}$ of the DC link capacitors. This leads to the consequence that for practical applications R_B has to be selected such that the expected leakage current difference is small in comparison to the quiescent current I_q of the voltage divider to achieve a good voltage distribution $V_{C1} \sim V_{C2} \sim V_D / 2$, i.e. a voltage deviation ? V ? 0. Here, the most significant drawback of the passive voltage balancing becomes obvious. The quiescent current which determines the dissipative losses has to be a multiple of the worst case leakage difference of the capacitors, and also if the actual value of ? I is much smaller or even ? I ? 0 is valid, considerable losses remain permanently.

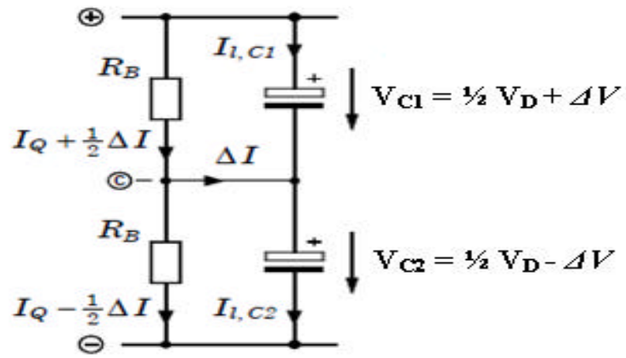


Fig 1.8: Passive Voltage Balancing network.

Using the output resistance $R_B/2$ of the voltage divider, the capacitor voltage deviation is calculated to $\Delta V = \Delta I \cdot R_B/2$; normalization by the nominal voltage $V_D/2$ of the capacitors leads to

$$\Delta v = \frac{\Delta V}{\frac{1}{2} V_D} = \frac{\Delta I \cdot \frac{1}{2} R_B}{I_Q \cdot R_B} = \frac{1}{2}\frac{\Delta I}{I_Q} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.3)$$

Consequently, if the capacitor voltages shall be balanced to $\Delta v = \pm 10\%$, then a quiescent current of $I_Q = 5 \cdot \Delta I$ have to be chosen. Using Equation (1.1), the total losses of the two balancing resistors ("balancing losses") sum up to

$$P_B = \underbrace{2 R_B \cdot I_Q^2}_{P_Q} + \frac{R_B}{2} \cdot \Delta I^2 = P_Q \left[1 + \Delta v^2\right] \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.4)$$

For relevant values $\Delta v < 0.1$ the balancing losses are dominated by the quiescent current losses $P_B \sim P_Q$.

1.8.2 Design Example

To give an example for the dimensioning of a passive balancing network, it should be assumed that the 500V DC voltage link of a 10kVA AC drive system equipped with two 10000µF/350V capacitors (e.g., EPCOS type B 43 564). The leakage current of this component according to equations (1.1, 1.2) for the relevant capacitor operating voltage (Fig 1.3, V_R ~ 250 V) is in the range between I_{opp} ~ 1.3 mA (typical) and I_{max} ~ 9 mA. Due to the fact that the output current ?I of the balancing network is formed by the leakage current difference of the two capacitors, but on the other hand the values given before are valid for 20°C only, a maximum value of ?I = 5 to 10 mA shall be assumed. Choosing I_q = 10 to 5 · ?I leads to a quiescent current of I_q = 50 mA which limits using equation (1.3) the center point voltage deviation to ?v = 5%. Now the resistance value of the balancing resistors can simply be calculated to $R_B = V_C / I_q$ = 250V / 50mA = 5 kΩ. The calculated dimensioning coincides very closely with a guideline given by the manufacturers. In the data sheets or application recommendations ([2] or [5]) it is frequently specified that the balancing resistors shall be calculated using the relation $R_B \cdot C$ ~ 50 sec = T_B. For the case at hand this again leads to R_B = 5 kΩ. The relation used before implies also that the balancing process ?V ? 0 of the (first order) system has a time constant of T_B. If the capacitors are charged up to ?v = ±20% at the power-up of the converter (e.g., caused by ±20% different capacitance values), it will take approximately 3 minutes until ?V ? 0 is valid. A quiescent current of I_q = 50 mA at V_D ~ 500 V results in balancing losses of P_B = 25 W. If the converter is permanently powered by the mains, these losses will sum up to a considerable energy consumption of approximately 220kWh per year. Considering the product life cycle of the converter, the balancing energy costs are many times higher than the costs for the passive balancing network itself. This suggests the development of an advanced balancing method.

1.8.3 Active Voltage Balancing – Basic Concept

The basic idea of the proposed active balancing concept is to separate the dimensioning of the voltage divider's quiescent current from the leakage currents of the electrolytic capacitors. In an

optimal case the voltage divider only would define the potential of the center point "C" to V_C $=V_D/2$ acting as the input reference level of an idealized voltage follower stage. With this, R_B ? 8 , I_L ? 0 would be possible and the balancing loss (appearing in the output stage of the amplifier) are now determined only by the actual leakage current difference and not by worst case conditions as this is true for the passive balancing network [6].

Although the ideal case I_L ? 0 now is not valid any more, the losses can be considerably reduced because a much lower quiescent current as compared to the passive case is possible considering the current gain ß of the transistors? I? ? Iß . Neglecting the losses of the voltage divider itself (i.e., I_L ? 0 ,ß ? 8) the losses of the active balancing are calculated to

$$P_B = ½ V_D ? I \quad \ldots\ldots\ldots\ldots\ldots\ldots . (1.5)$$

1.9 Literature Review

To overcome this critical impact of leakage current, different techniques have been introduced time to time. To avoid the malfunctioning and ensure expected sharing of the bus voltage, a passive resistive balancing circuit is used in traditional methods [2], [5] - [7]. The balancing circuit is principally a resistive divider whose midpoint is connected to the capacitors midpoint. To compensate the maximum leakage current dispersion, the divider is designed so that the bias current is the multiple of the maximum leakage current. Such a large bias current multiplied by the dc bus voltage causes a significant power loss. Then, as an alternative, the active voltage balancing techniques with reduced power loss for series-connected high-power electrolytic capacitors have been introduced [6]-[8]. The losses in these methods are by far lower in comparison to the passive balancing method.

Furthermore, the active circuit also gives a stiffer balancing characteristic ($V_{C1} = V_{C2} = V_D/2$ for the idealized case ß ? 8). For realization of the emitter-follower bipolar transistors which show a maximum collector-emitter voltage of at least $V_D/2$ are required. Considering DC link over voltages, no balanced operating conditions and safety margins to guarantee a robust and reliable operation of the active balancing, at least 400V to 500V semiconductor devices seem to be necessary in practice for a DC link with 500V nominal voltage. However, high-voltage bipolar transistors are characterized by a comparatively low ß due to their wide effective base region. General-purpose 400V NPN / PNP transistor pairs, e.g., MPSA44/MPSA94 are characterized by a current gain of typically only ß ~ 40 and, therefore, are not suited well for realizing the proposed concept.

Although "high-gain" high voltage bipolar transistor pairs are available in the 400V region (e.g., ZETEX ZTX458/ZTX558, ß ~ 200 [9]), it has to be considered that the transistor types mentioned before are "low-power" devices, i.e., limited to typically P = 1W. In the case of ? I> 4mA these elements would be thermally overloaded. On the other hand, real high-voltage bipolar power transistors are hardly available as complementary pairs and/or show very low current gain. Consequently, an implementation using complementary power MOSFET transistors would be of advantage. But also here the availability of high-voltage p-channel devices is very limited (e.g. 500V transistor MTP2P50E by ON Semiconductor); furthermore, these semiconductor devices are rather expensive.

The balancing circuit is based on a bipolar junction transistor (BJT) high-voltage push–pull amplifier whose output is connected to the midpoint of the dc bus capacitors, while the input is connected the midpoint of a resistive voltage divider. Since the amplifier input impedance is quite high, the voltage divider bias current and the related losses could be quite low. A similar circuit based on a high-voltage MOSFET push–pull amplifier is proposed in [8]. A few active dissipative and non-dissipative voltage balancing techniques that are used in super capacitor modules are discussed in [9] and [11]. Active non-dissipative balancing circuits for series-connected lithium-ion and lead–acid batteries are analyzed in [12]–[16]. All these balancing methods, with some minor modifications, could be applied to the series-connected high-power electrolytic capacitors.

Considering the cost effectiveness, simplicity and range of voltage application, op amps can be employed as voltage comparator to design the proposed regulating method [17],[18].

Therefore, the leakage current differences are balanced with importance in the circuit design because even very small difference can cause problems. In this thesis, a novel approach to improve the impacts of leakage current dispersions for both two and four series connected electrolytic capacitors have been analyzed.

1.10 Objective and Methodology

1.10.1 Objective

To improve the shortcomings of a traditional resistive balancing method, the objective of this thesis is to propose a new regulating strategy which will keep the voltage across series connected electrolytic capacitors at desired level in spite of various leakage currents dispersion. The objectives and outcome can be summarized as below:

- Analyze the impact of leakage current dispersion for both two and four series connected capacitors.
- Design a technique that replaces traditional balancing resistances.
- Regulate the impact of leakage current dispersion and maintain voltage balancing among series capacitors at specified level despite leakage current dispersion.
- Facilitate multiple outputs and verify the regulating circuit by applying varied loads.

1.10.2 Methodology

The objective will be approached through two and four electrolytic capacitors of equal voltage connected in series across DC bus. Key challenge of this thesis will be to design a proper regulating technique to alleviate voltage imbalance between series electrolytic capacitors due to leakage current dispersion. Op amps will be used for the push-pull of the required current to compensate the voltage imbalance occurred due to leakage current dispersion among capacitors. Suitable op amps will be selected with the consideration of the voltage compatibility. So, this design to balance voltage across capacitors will fully substitute the balancing resistors. The midpoint of the capacitors will be connected to the offered active less dissipative circuitry so that the impact of capacitor leakage current dispersion is canceled out. The proposed circuit will also regulate the impact of load variation which causes asymmetric voltages across capacitors. As a result, the capacitor voltages will be controlled and maintained at the desired level.

1.11 Organization of the Thesis

The thesis is organized as follows:

Chapter 1 includes introduction, background, basics of capacitors leakage current and its influences, traditional method, objective and methodology of the thesis.

Chapter 2 includes analysis of the impacts of leakage current dispersion for two and four series connected capacitors. Simulation results are also reported in this chapter.

Chapter 3 includes design of the proposed technique and improvements after applying the regulating technique. Simulation results are also reported in this chapter.

Chapter 4 includes conclusions of the thesis with some recommendation for further research.

Chapter 2

Analysis of the Impact of Leakage Current Dispersion

2.1 The impact of leakage current dispersion

The voltage being split between the electrolytic capacitors while connected in series and in turn this is influenced by the leakage current difference between the individual capacitors in a series. Even a large voltage differences may occur due to this leakage current differences. It is observed that voltage increases across the capacitor with lower leakage current. If this results in exceeding the rated voltage of a capacitor, under certain circumstances this can result in premature failure.

2.2 Analysis of the impact of leakage current dispersion

2.2.1 Observation of the impacts

The simulation setup for the analysis of the impacts of leakage current dispersion is shown in Fig 2.1. The impacts because of leakage current dispersion are shown in Fig 2.2. Here, different leakage currents with different values are applied for capacitors C_1, C_2, C_3 and C_4 respectively given in Table 2.1 and corresponding graphs are shown in Fig 2.2 (a), (b), (c) and (d). In Fig 2.2 (a) the emergence of leakage currents are considered abrupt at time 2ms and linear for other instant as shown in Fig 2.2 (b), (c) and (d).

It is observed from the simulation results that voltage decreases across the capacitor in which leakage current is higher and on the other hand, voltages relatively goes high across other capacitors with lower or no leakage currents as shown in Fig 2.2 (a'), (b'), (c') and (d'). This voltage imbalance begins among the capacitors at the instant of leakage current dispersion is applied.

In Fig 2.3 (a) equal leakage current i.e. no dispersion ($I_{L1} = I_{L2}$) is applied and load resistances were also kept equal $R_{L1} = R_{L2}$. As a result there is no voltage imbalance is observed as shown in Fig 2.3 (b).

The impact of leakage current dispersion for two capacitors in series, where simulation setup as given in Fig 2.4 (a) and Fig 2.5 (a) respectively with leakage current applied in C_1 (i.e. I_{L1}) and in C_2 (i.e. I_{L2}) and corresponding voltage imbalance across capacitors are shown in Fig 2.4 (b) and Fig 2.5 (b) respectively. Then, Leakage Current dispersion for four capacitors in series, where simulation setup with varied leakage current applied in four capacitors (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}) is given in Fig 2.6 (a) and as the effect of different dispersion among applied leakage currents voltages became imbalanced which are shown in Fig 2.6 (b), Fig 2.7, Fig 2.8, Fig 2.9 and Fig 2.10.

Then, applying simulation setup with varied loads (i.e. R_1, R_2, R_3 and R_4) as shown in Fig 2.11 (a) and as a result voltage level became asymmetric across capacitors such as higher voltage for higher load Fig 2.11 (b). Also, applying both varied loads and leakage current dispersion as given in Fig 2.12 (a) and resulted asymmetric voltages and imbalance in voltages are shown in Fig 2.12 (b).

Table 2.1

Applied Leakage Currents

Time	**I_{L1} (C_1)**	**I_{L2} (C_2)**	**I_{L3} (C_3)**	**I_{L4} (C_4)**
2ms	10mA	5mA	6mA	2mA
4ms	3mA	10mA	5mA	2mA
5ms	3mA	5mA	10mA	2mA
8ms	3mA	0mA	6mA	10mA

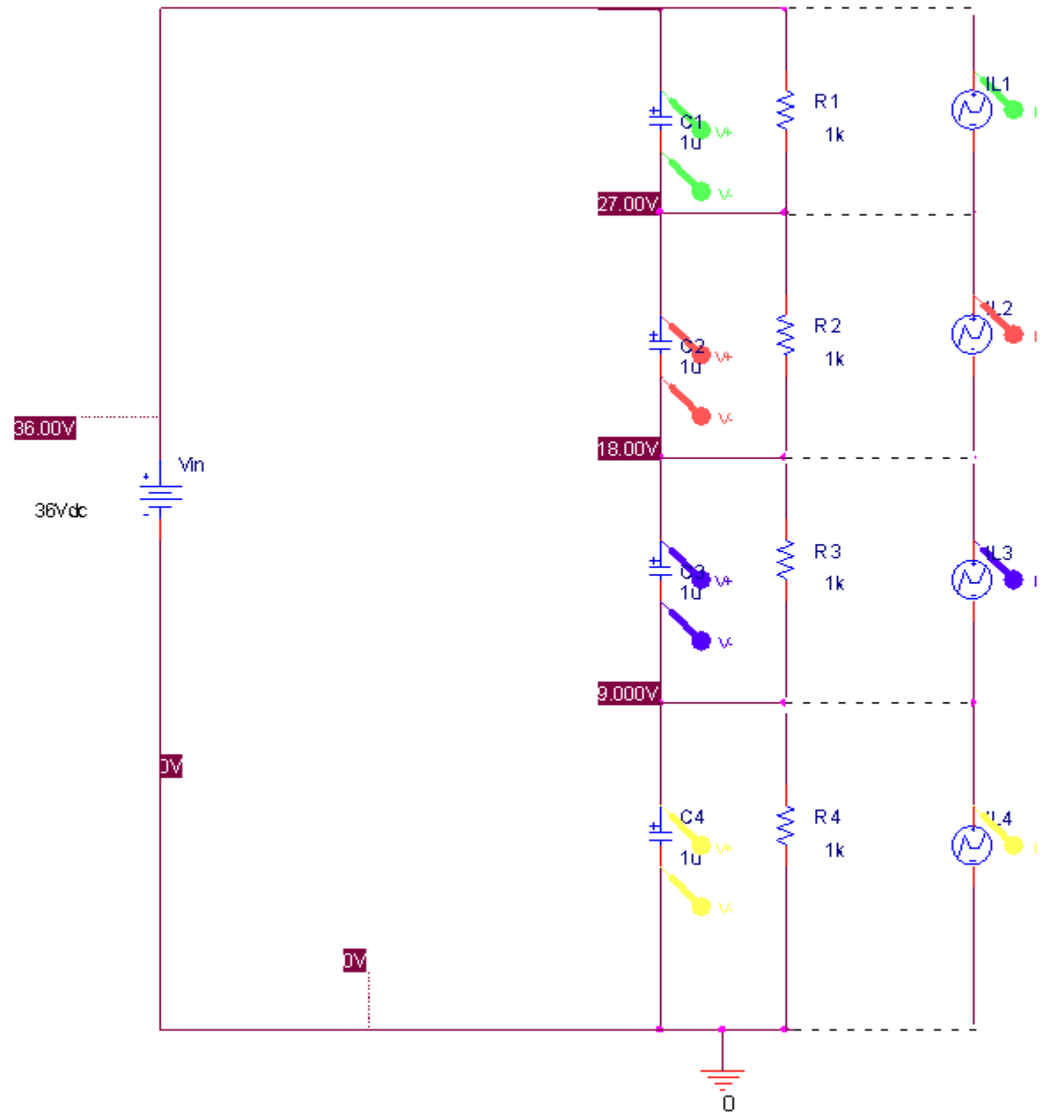
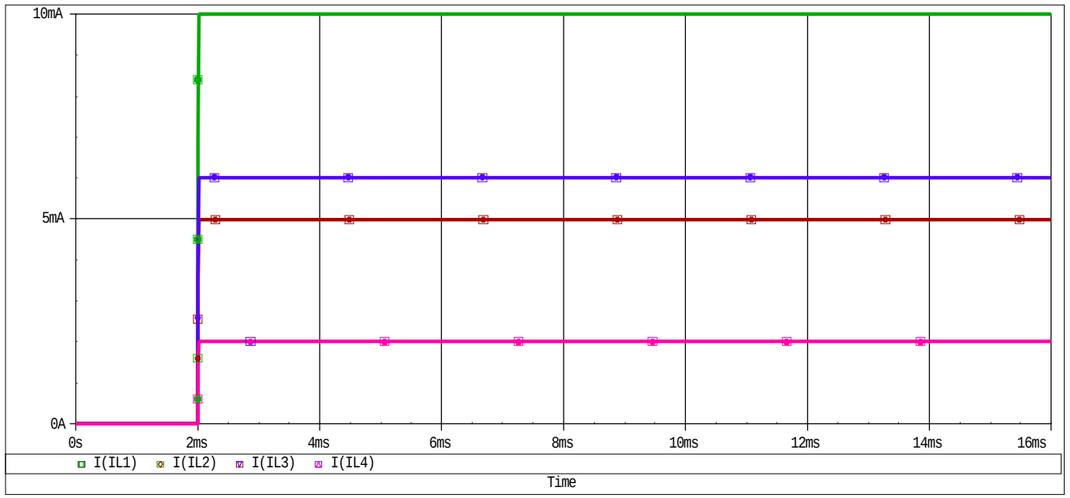
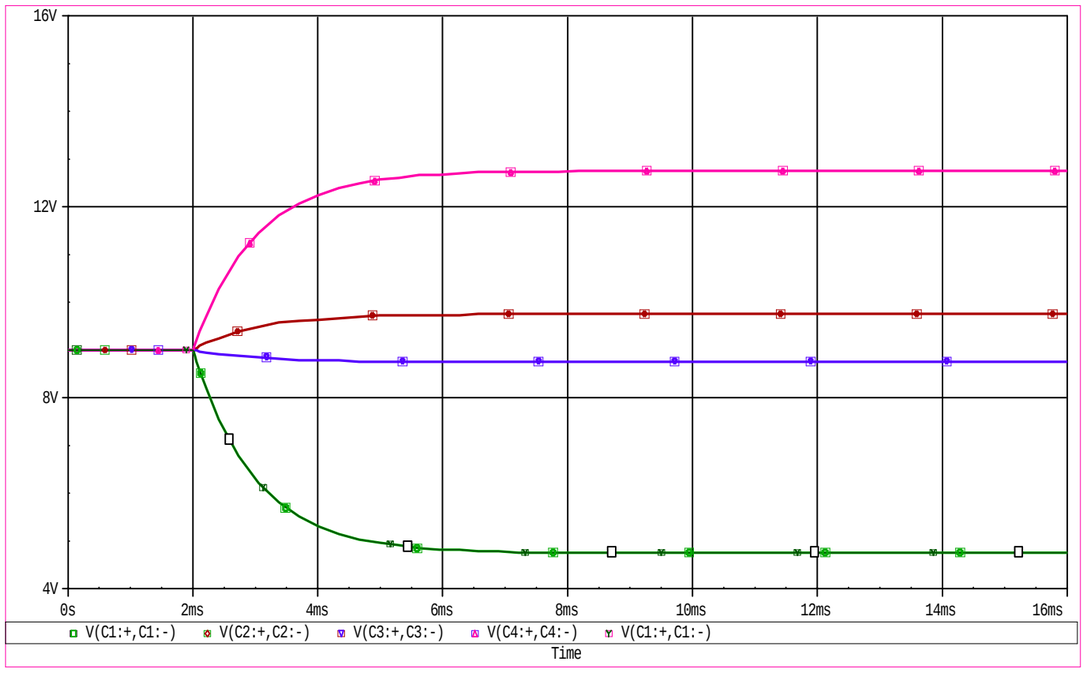


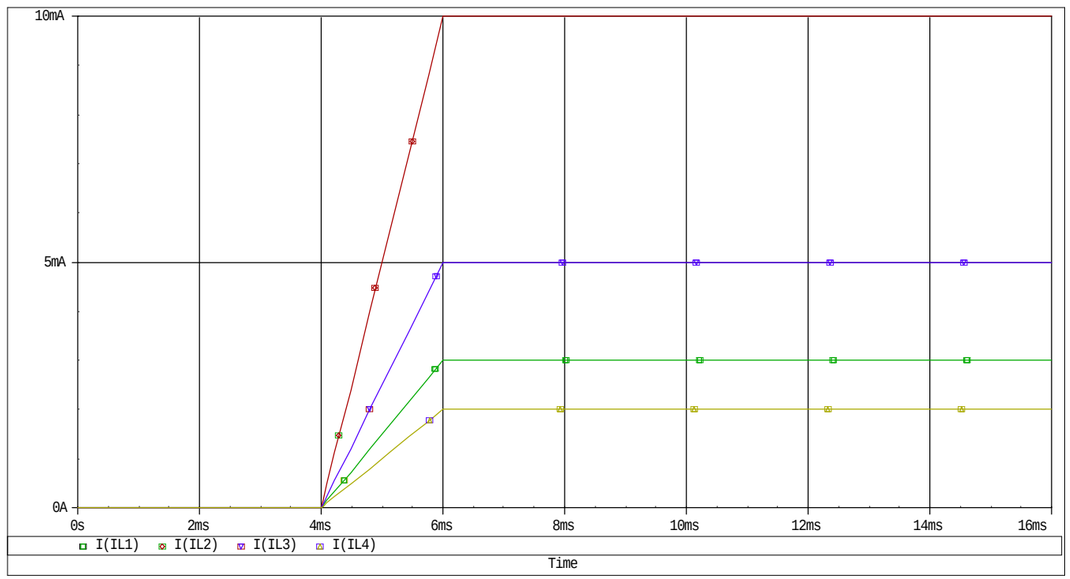
Fig 2.1: The simulation setup for the analysis of the impacts of leakage current dispersion.


10mA
5mA
0A
0s
2ms
4ms
6ms
8ms
10ms
12ms
14ms
16ms
I(IL1)
I(IL2)
I(IL3)
I(IL4)
Time

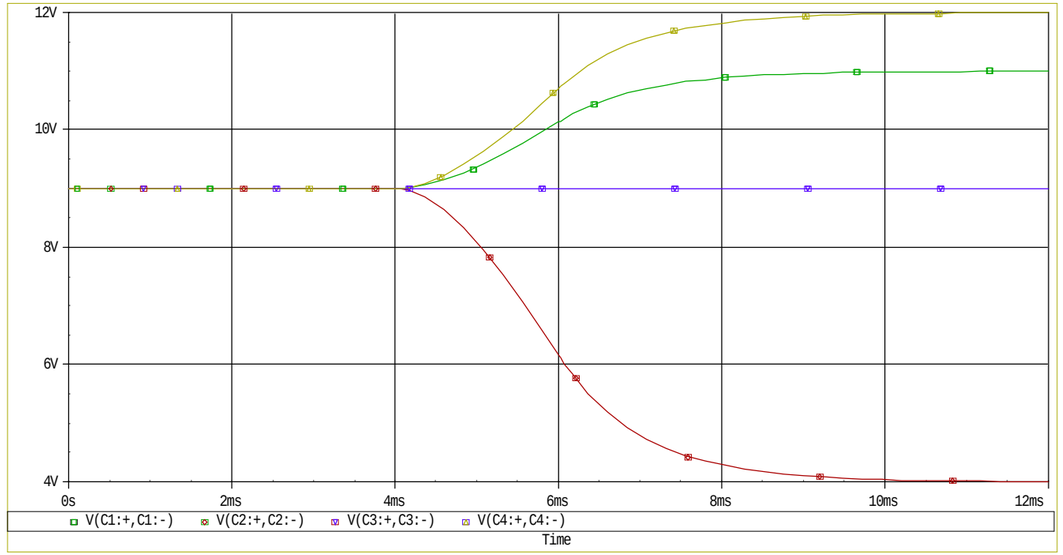
(a)


16V
12V
8V
4V
0s
2ms
4ms
6ms
8ms
10ms
12ms
14ms
16ms
V(C1:+,C1:-)
V(C2:+,C2:-)
V(C3:+,C3:-)
V(C4:+,C4:-)
V(C1:+,C1:-)
Time

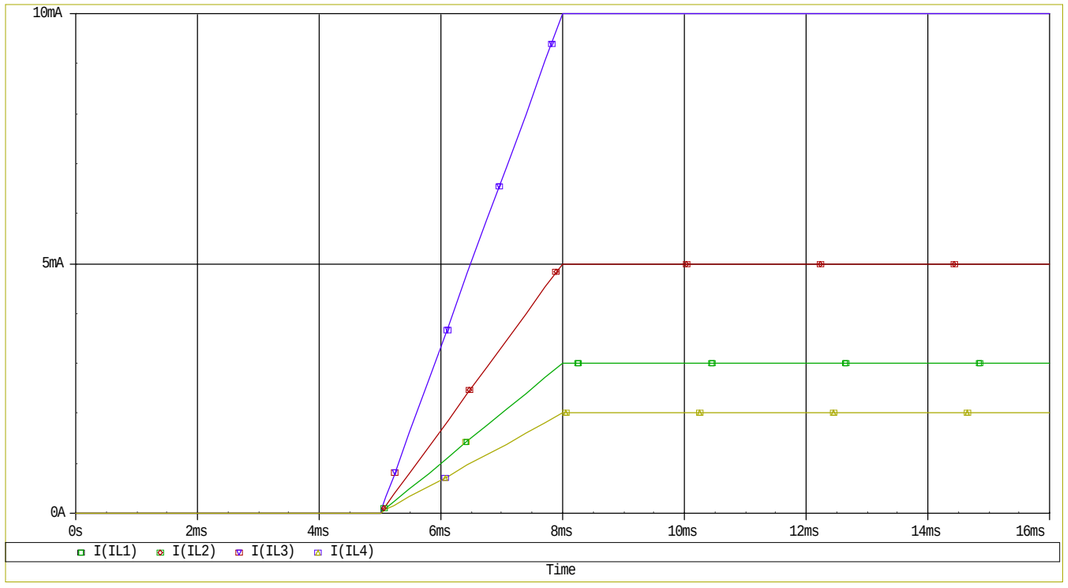
(a?)


10mA
5mA
0A
0s
2ms
4ms
6ms
8ms
10ms
12ms
14ms
16ms
I(IL1)
I(IL2)
I(IL3)
I(IL4)
Time

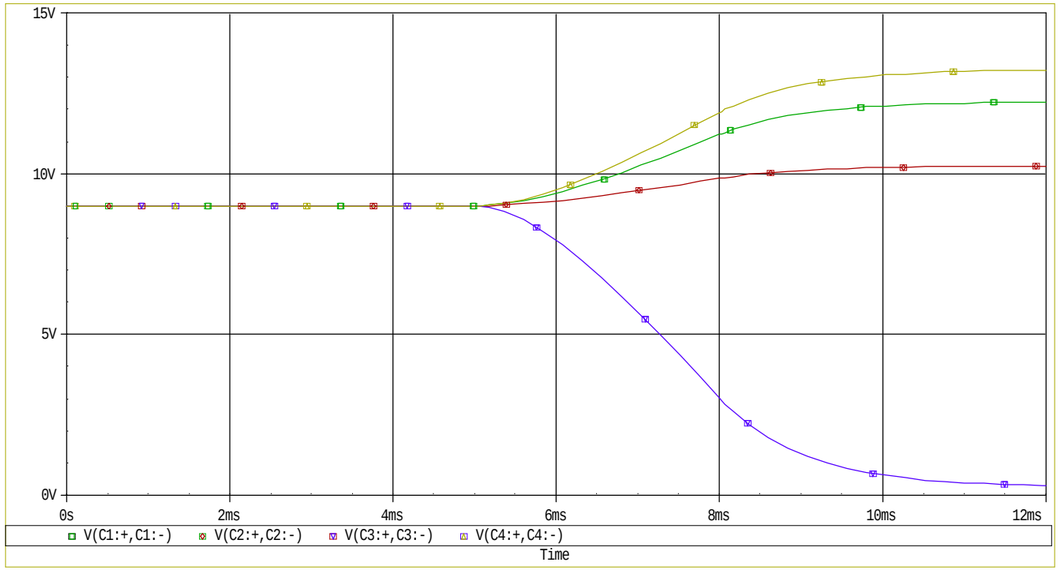
(b)


12V
10V
8V
6V
4V
0s
2ms
4ms
6ms
8ms
10ms
12ms
V(C1:+,C1:-)
V(C2:+,C2:-)
V(C3:+,C3:-)
V(C4:+,C4:-)
Time

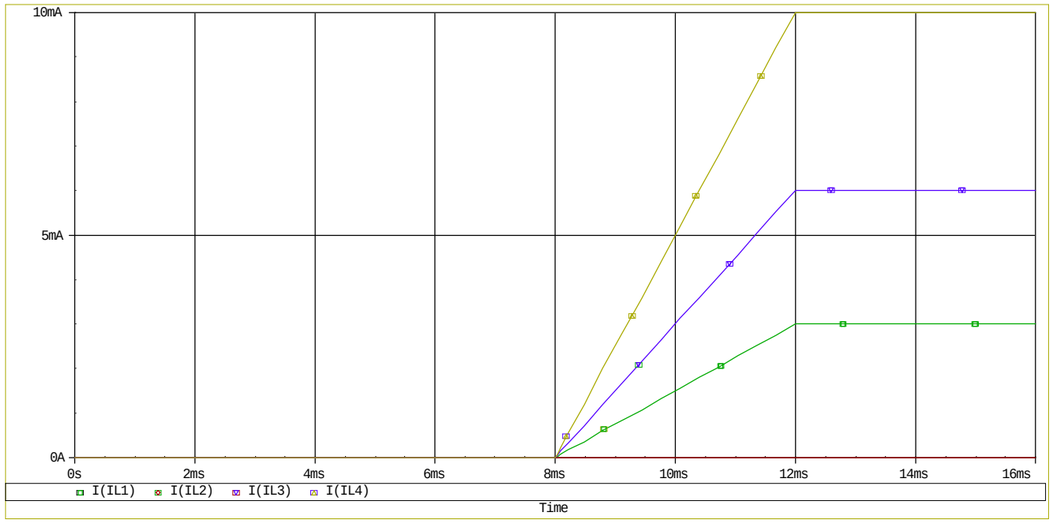
(b?)


10mA
5mA
0A
0s
2ms
4ms
6ms
8ms
10ms
12ms
14ms
16ms
I(IL1)
I(IL2)
I(IL3)
I(IL4)
Time

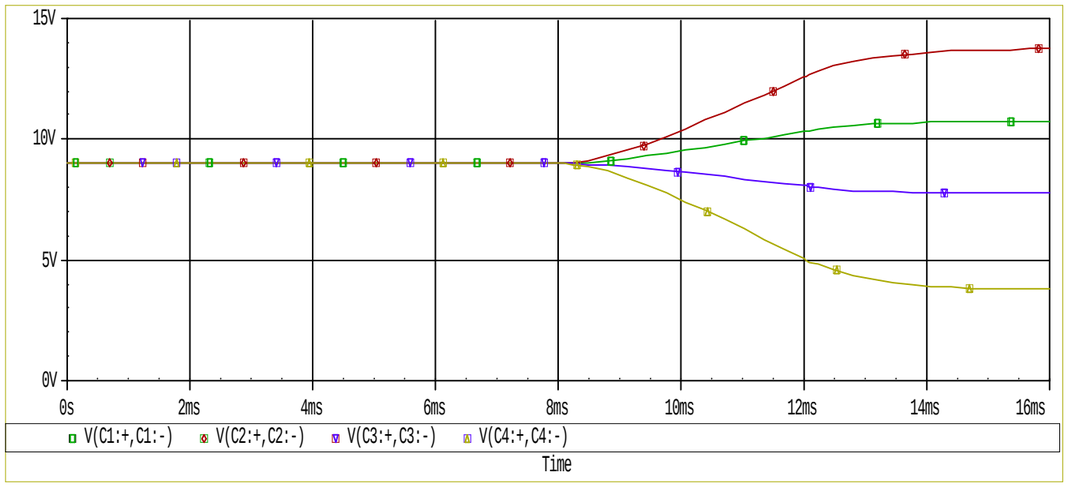
(c)


15V
10V
5V
0V
0s
2ms
4ms
6ms
8ms
10ms
12ms
V(C1:+,C1:-)
V(C2:+,C2:-)
V(C3:+,C3:-)
V(C4:+,C4:-)
Time

(c?)



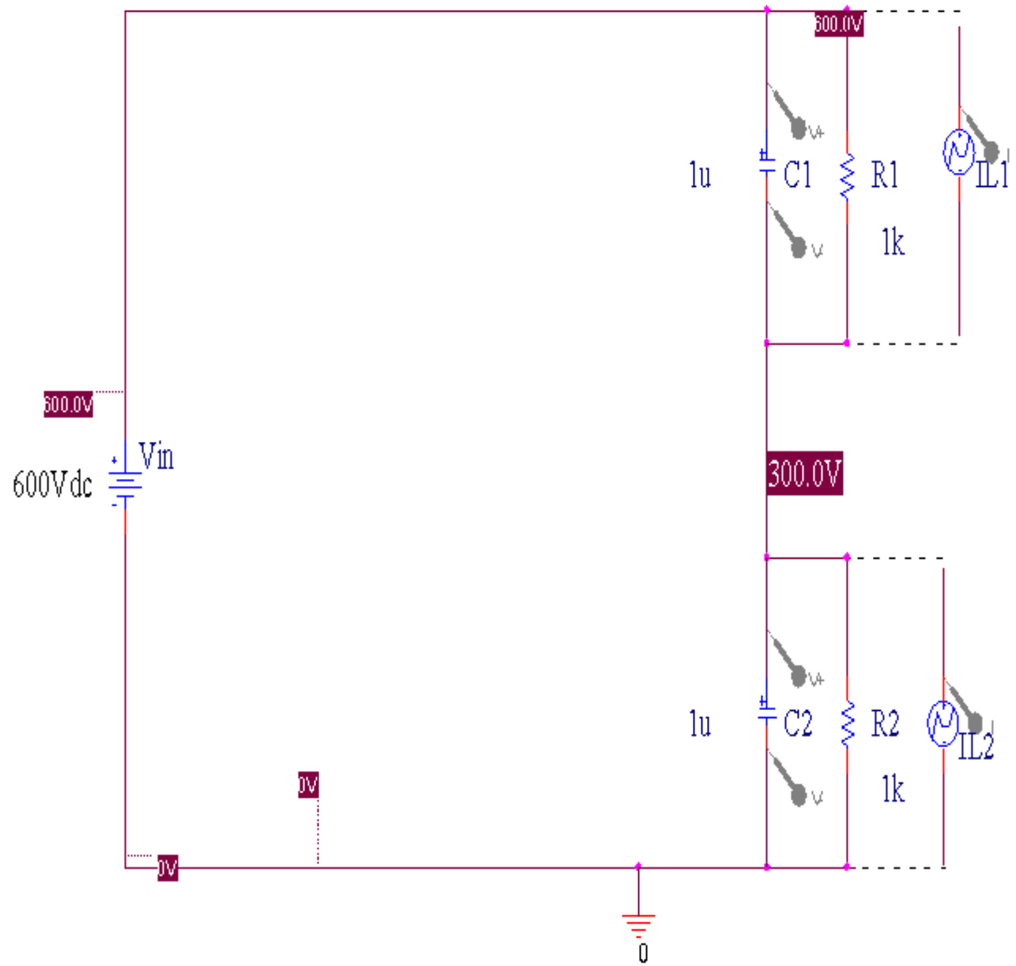
(d)



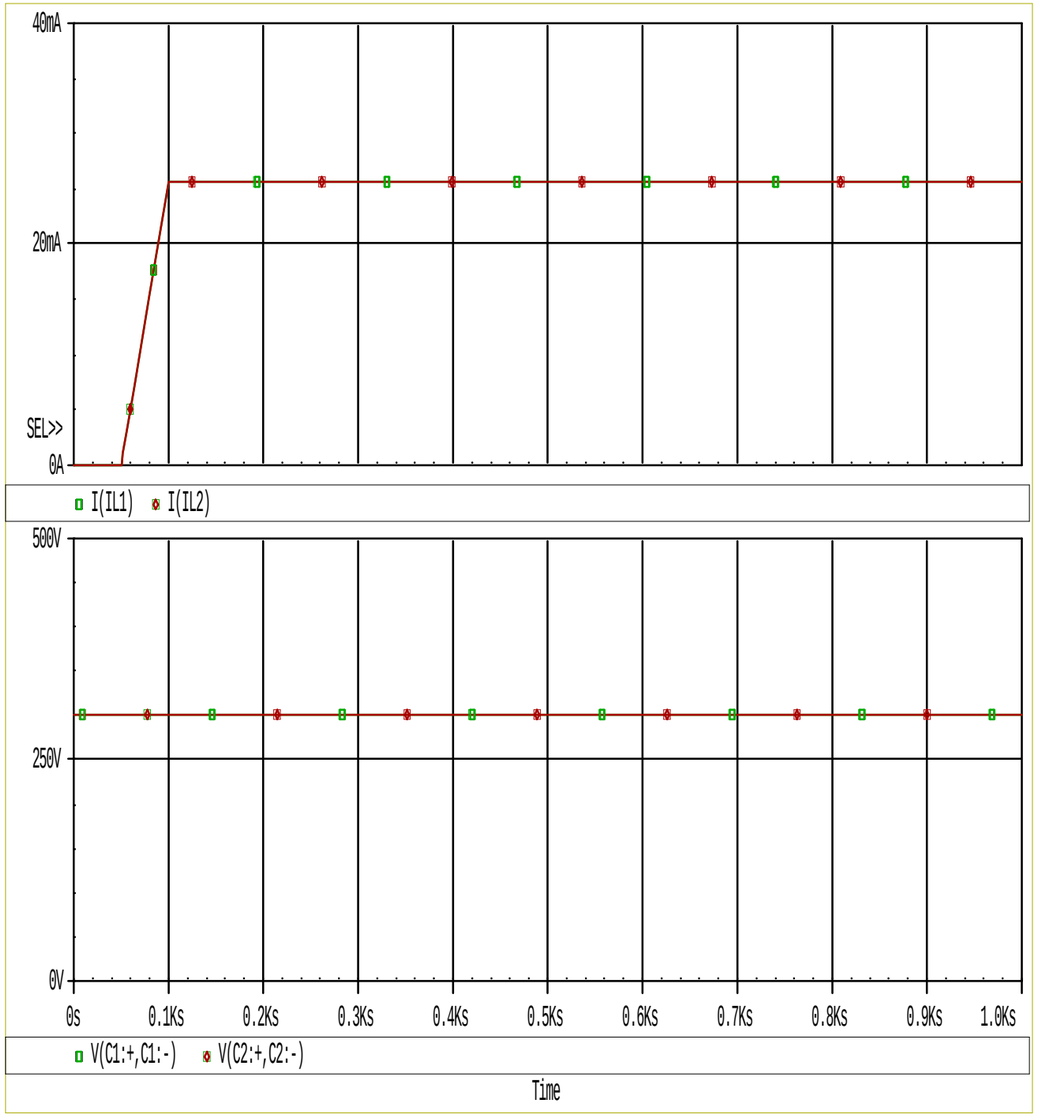
(d')

Fig 2.2: Impacts of various leakage current dispersions for the Fig 2.1, (a) $I_{L1} > \{I_{L2}, I_{L3}, I_{L4}\}$, (a') Voltage decreases for C_1 and relatively higher for others, (b) $I_{L2} > \{I_{L1}, I_{L3}, I_{L4}\}$, (b') Voltage decreases for C_2 and relatively higher for others, (c) $I_{L3} > \{I_{L1}, I_{L2}, I_{L4}\}$, (c') Voltage decreases for C_3 and relatively higher for others, (d) $I_{L4} > \{I_{L1}, I_{L2}, I_{L3}\}$, (d') Voltage decreases for C_4 and relatively higher for others.

2.2.2 Applying Equal Leakage current (i.e. no dispersion)



(a)

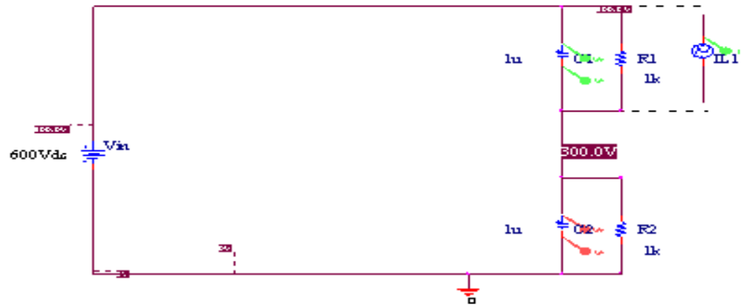


(b)

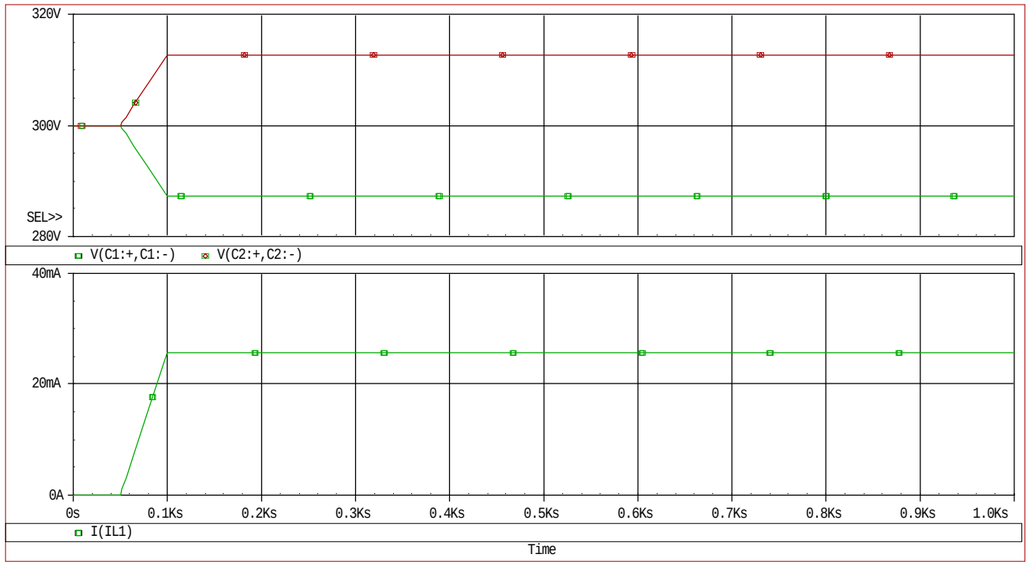
Fig 2.3: (a) Shows the simulation setup, (b) applied equal leakage current of 25mA (i.e. $I_{L1} = I_{L2}$) in both capacitors (upper) i.e. no dispersion, so there is no voltage imbalance observed (lower) i.e. $V_{C1} = V_{C2} = 300$ V.

2.2.3 Realizing the impact for two capacitors in series

2.2.3.1 Leakage Current in C_1



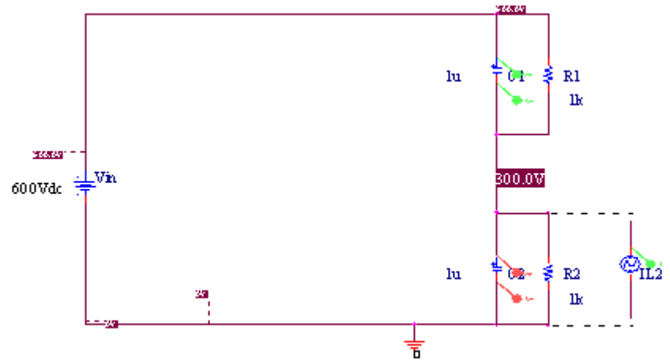
(a)



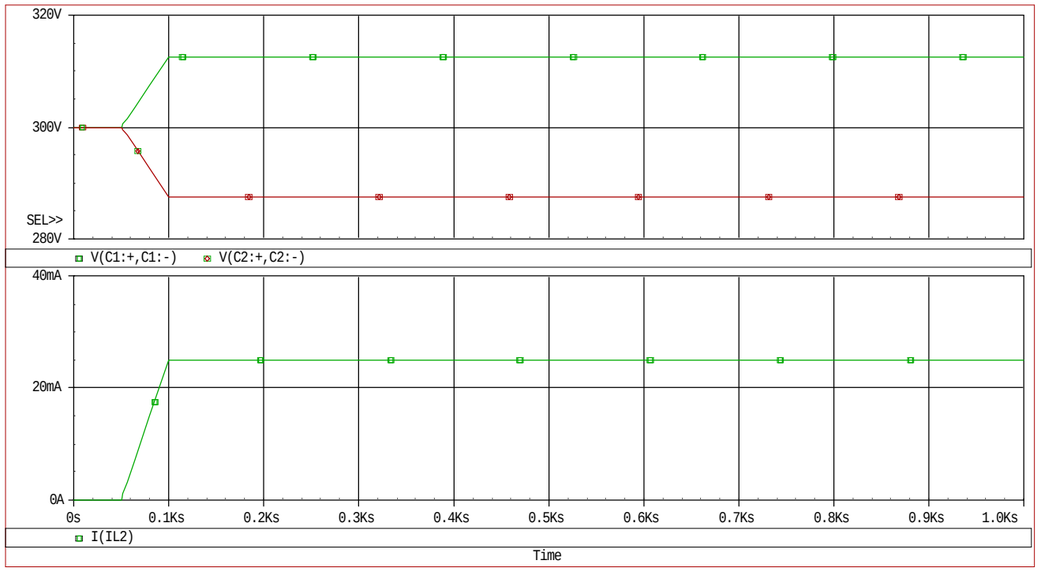
(b)

Fig 2.4: (a) Shows the simulation setup with leakage current applied only in C_1 (i.e. I_{L1}); (b) Voltages became imbalanced e.g. V_{C1} decreased and V_{C2} increased (upper) after applying leakage current dispersion (lower) i.e. I_{L1} = 25mA and no leakage current for C_2.

2.2.3.2 Leakage Current in C_2



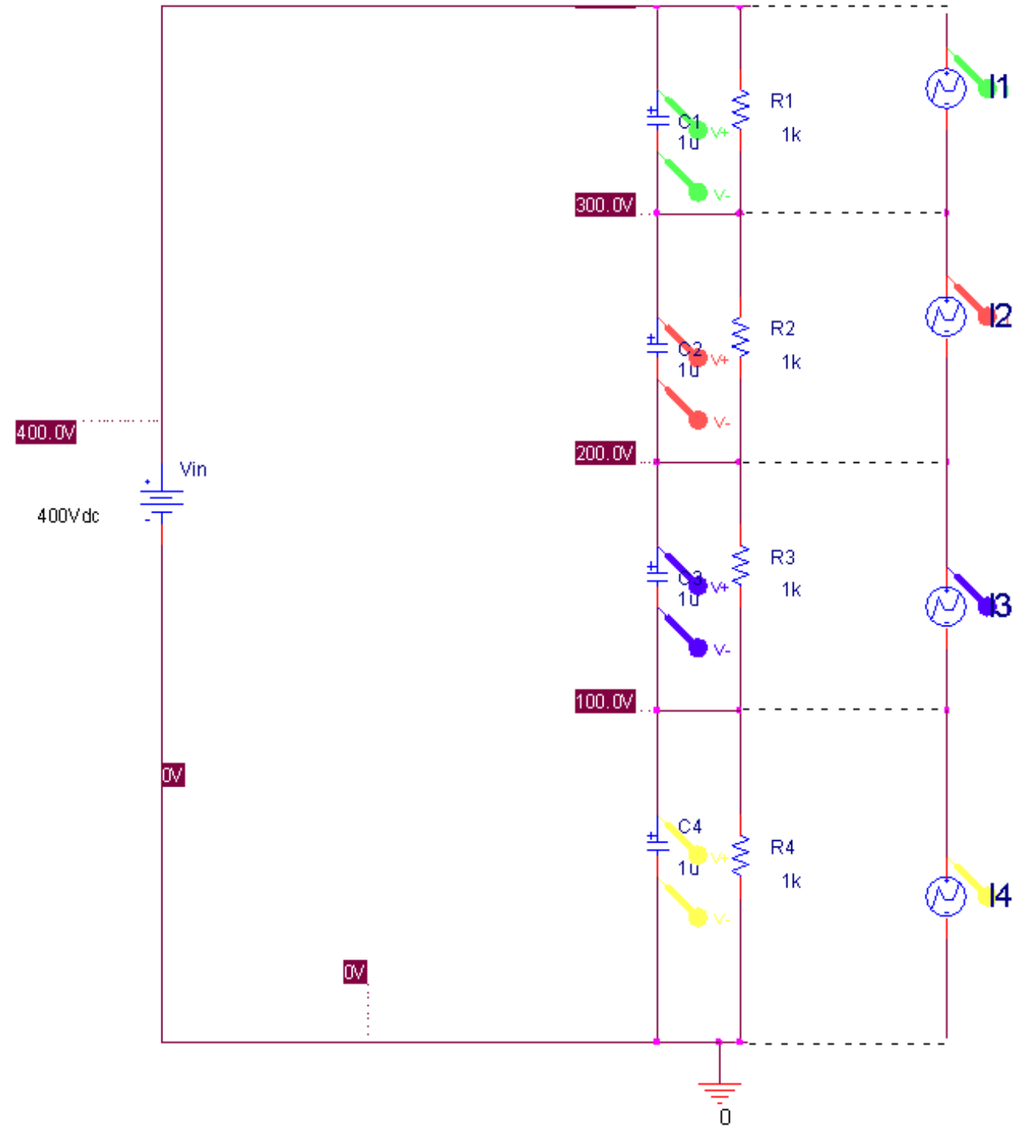
(a)



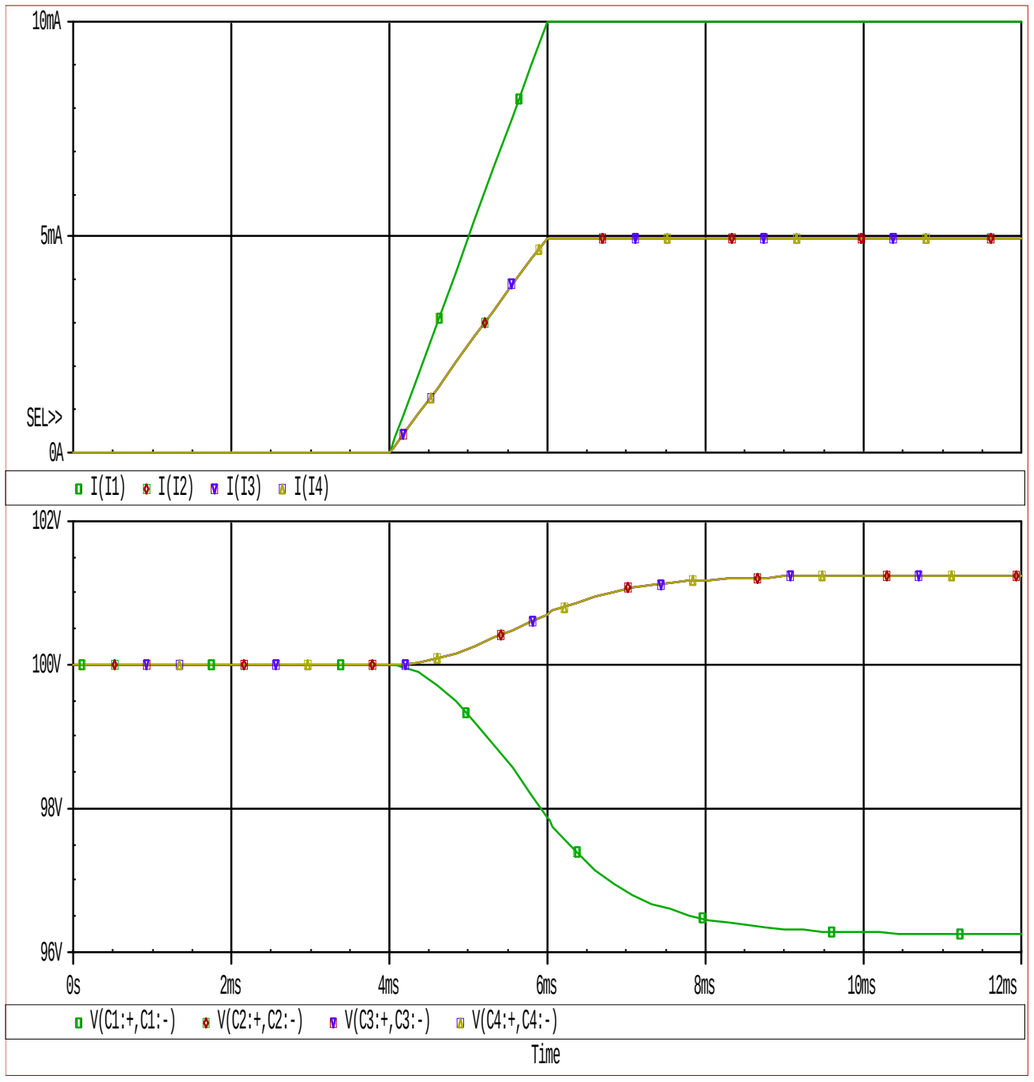
(b)

Fig 2.5: (a) Shows the simulation setup with leakage current applied only in C_2 (i.e. I_{L2}); (b) Voltages became imbalanced e.g. V_{C2} decreased and V_{C1} increased (upper) after applying leakage current dispersion (below) i.e. I_{L2} = 15mA and no leakage current for C_1.

2.2.4 Leakage Current dispersion for four capacitors in series



(a)



(b)

Fig 2.6: (a) Shows the simulation setup with varied leakage current applied in four capacitors (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}), (b) Here, voltages became imbalanced e.g. V_{C1} decreased and V_{C2}, V_{C3}, V_{C4} increased (lower) after applying leakage current dispersion (upper) i.e. I_{L1} = 10mA and I_{L2} = I_{L3} = I_{L4} = 5mA.

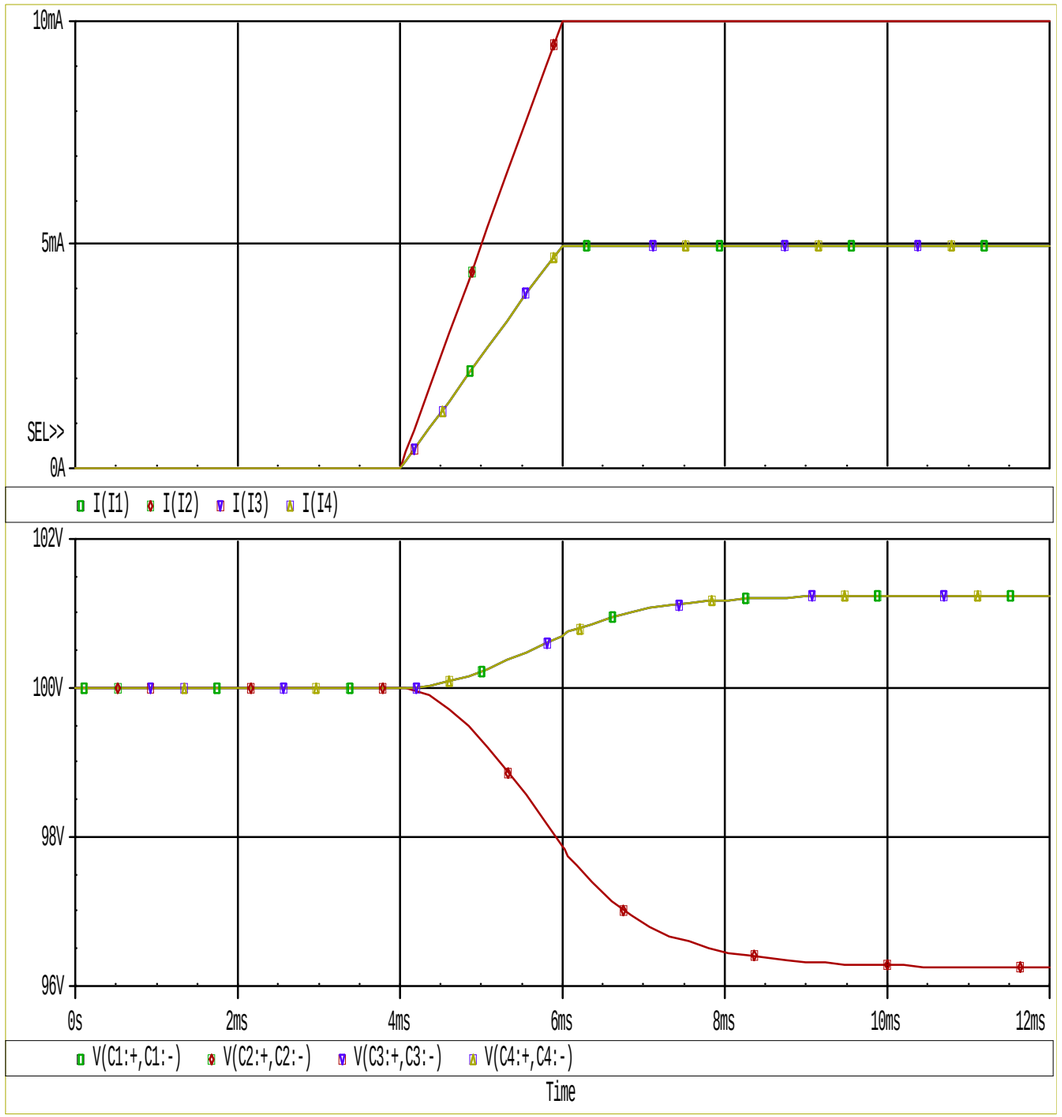


Fig 2.7: The simulation setup with varied leakage current applied in four capacitors (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}) as shown in Fig 2.5 (a). Here, voltages became imbalanced e.g. V_{C2} decreased and V_{C1}, V_{C3}, V_{C4} increased (lower) after applying leakage current dispersion (upper) i.e. I_{L2} = 10mA and $I_{L1} = I_{L3} = I_{L4}$ = 5mA.

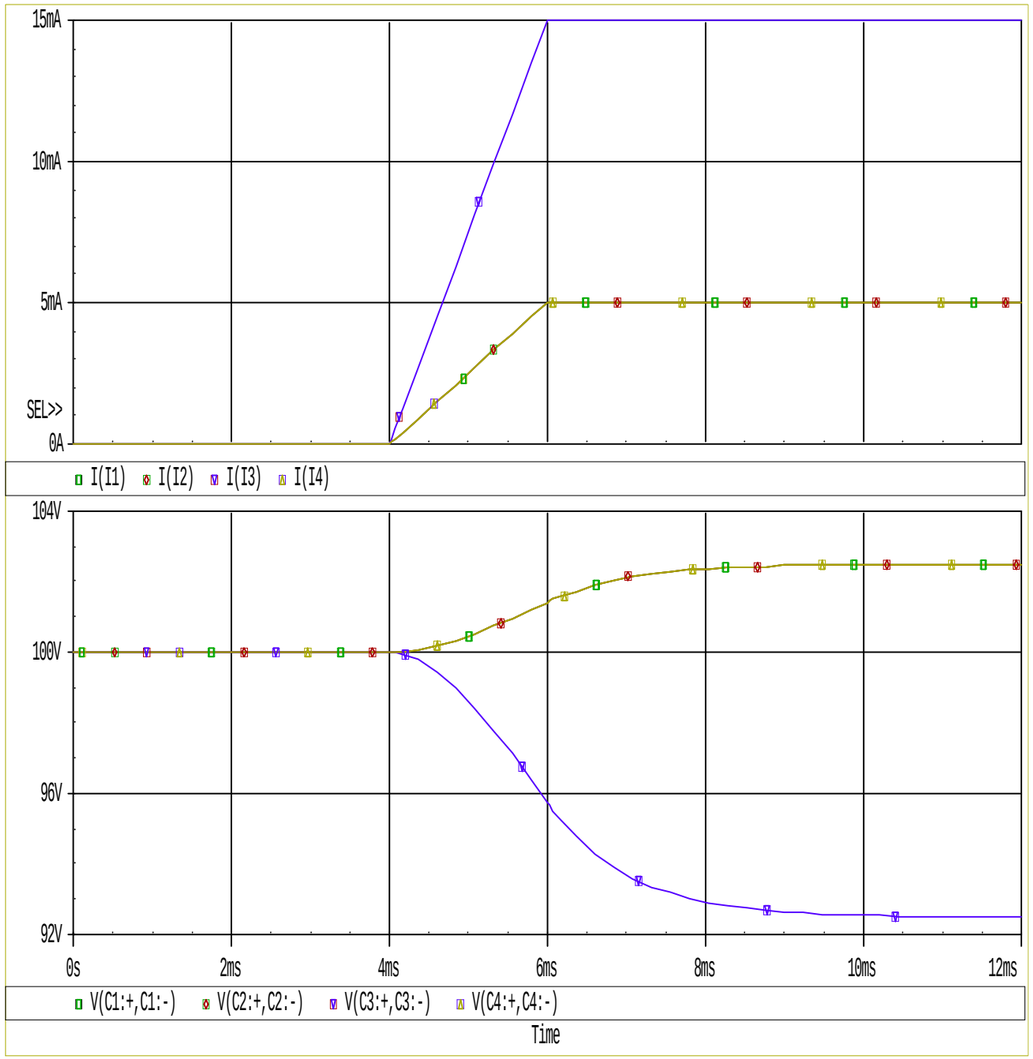


Fig 2.8: The simulation setup with varied leakage current applied in four capacitors (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}) as shown in Fig 2.5 (a). Here, voltages became imbalanced e.g. V_{C3} decreased and V_{C1}, V_{C2}, V_{C4} increased (lower) after applying leakage current dispersion (upper) i.e. I_{L3} = 15mA and I_{L1}= I_{L2} = I_{L4} = 5mA.

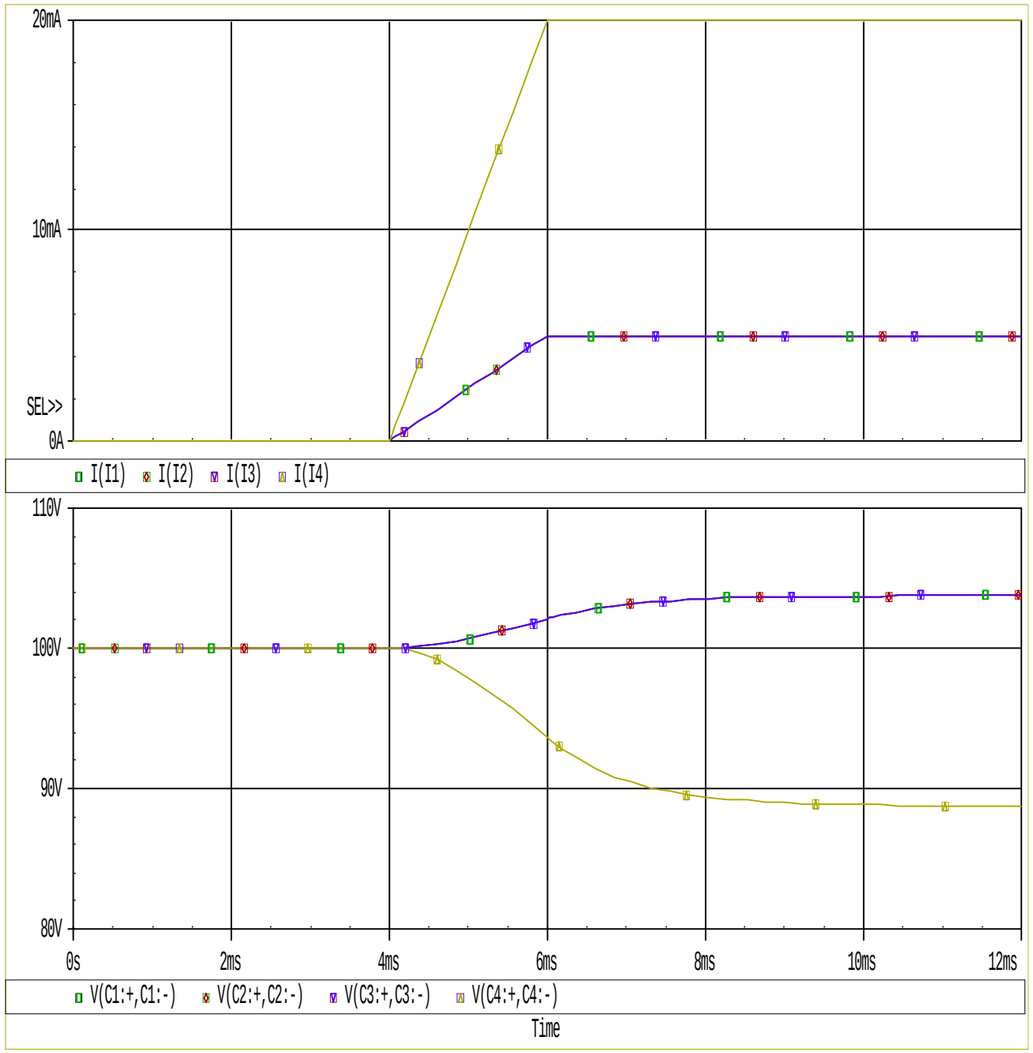


Fig 2.9: The simulation setup with varied leakage current applied in four capacitors (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}) as shown in Fig 2.5 (a). Here, voltages became imbalanced e.g. V_{C4} decreased and V_{C1}, V_{C2}, V_{C3} increased (lower) after applying leakage current dispersion (upper) i.e. I_{L4} = 20mA and I_{L1} = I_{L2} = I_{L3} = 5mA.

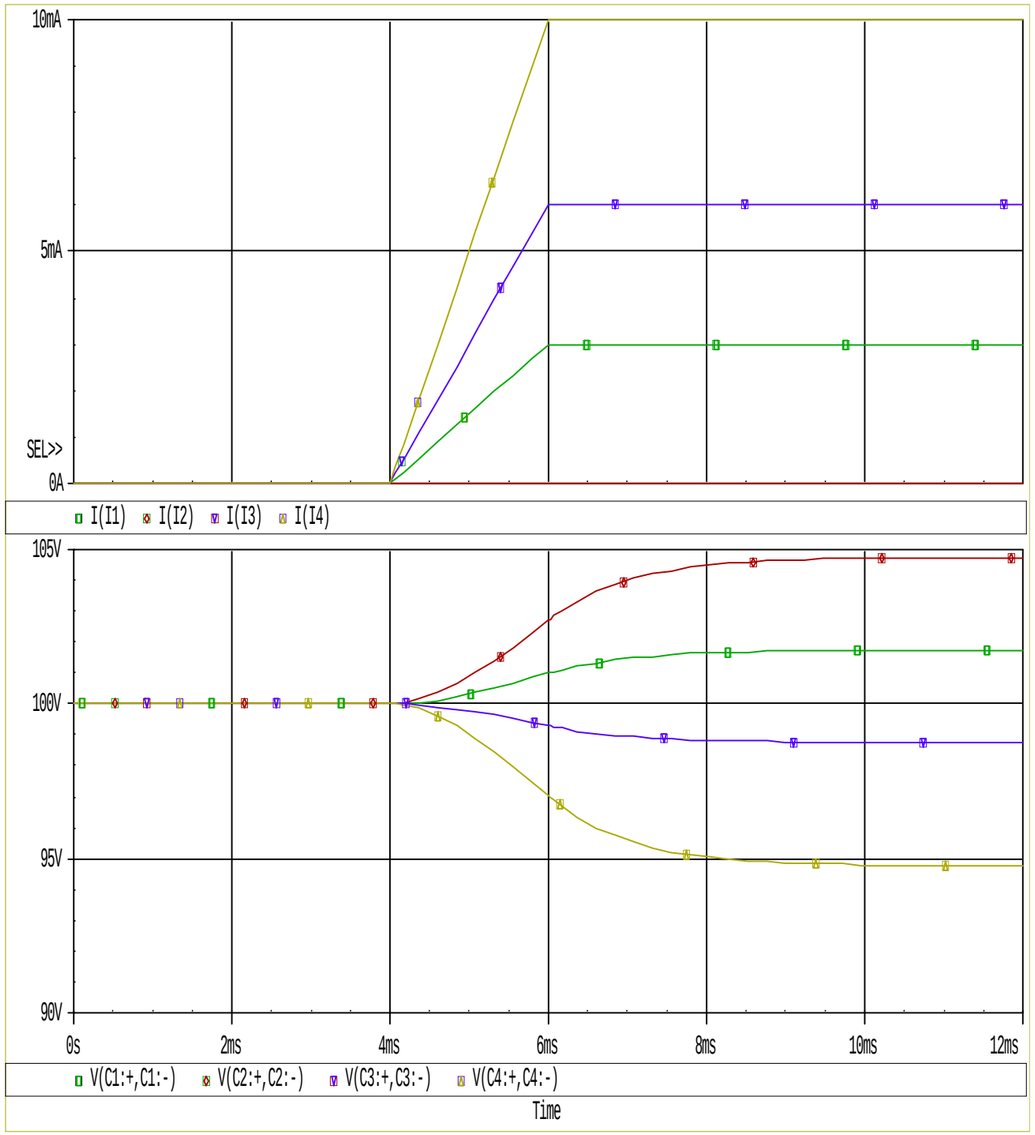
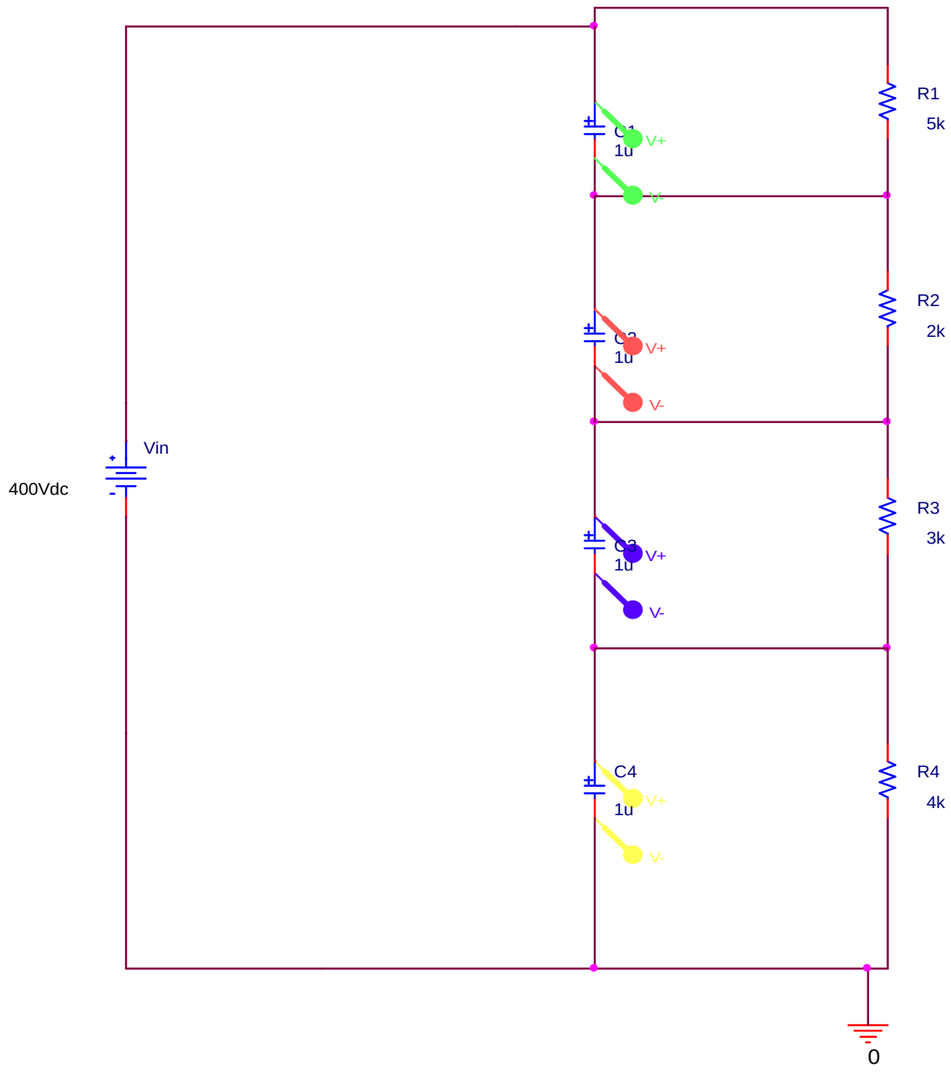
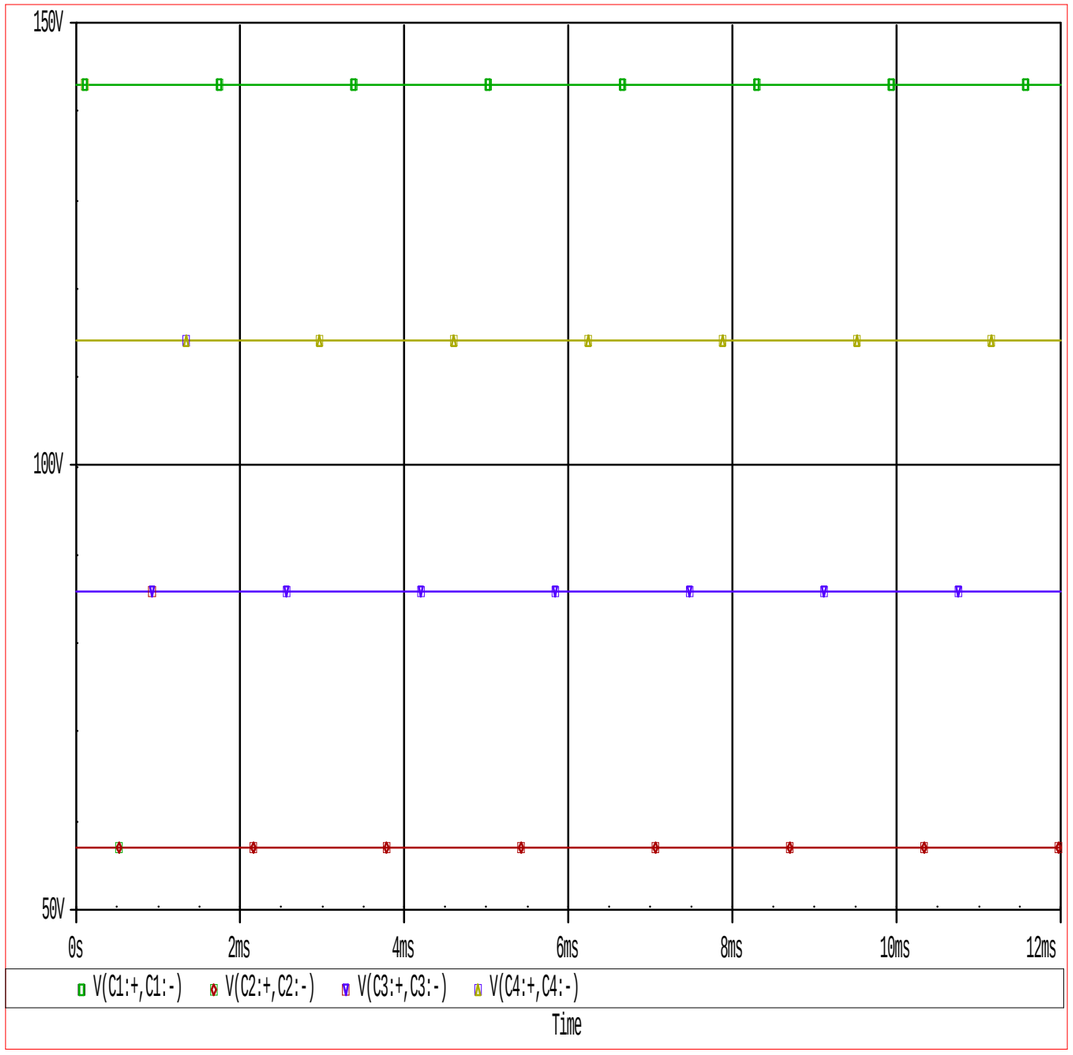


Fig 2.10: The simulation setup with varied leakage current applied in four capacitors (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}) as shown in Fig 2.5 (a). Here, voltages became imbalanced e.g. V_{C3} and V_{C4} decreased and V_{C1}, V_{C2} increased (lower) after applying leakage current dispersion (upper) i.e. I_{L1} = 3mA, I_{L2} = 0mA, I_{L3} = 6mA and I_{L4} = 10mA.

2.2.5 Impact of Load Vary



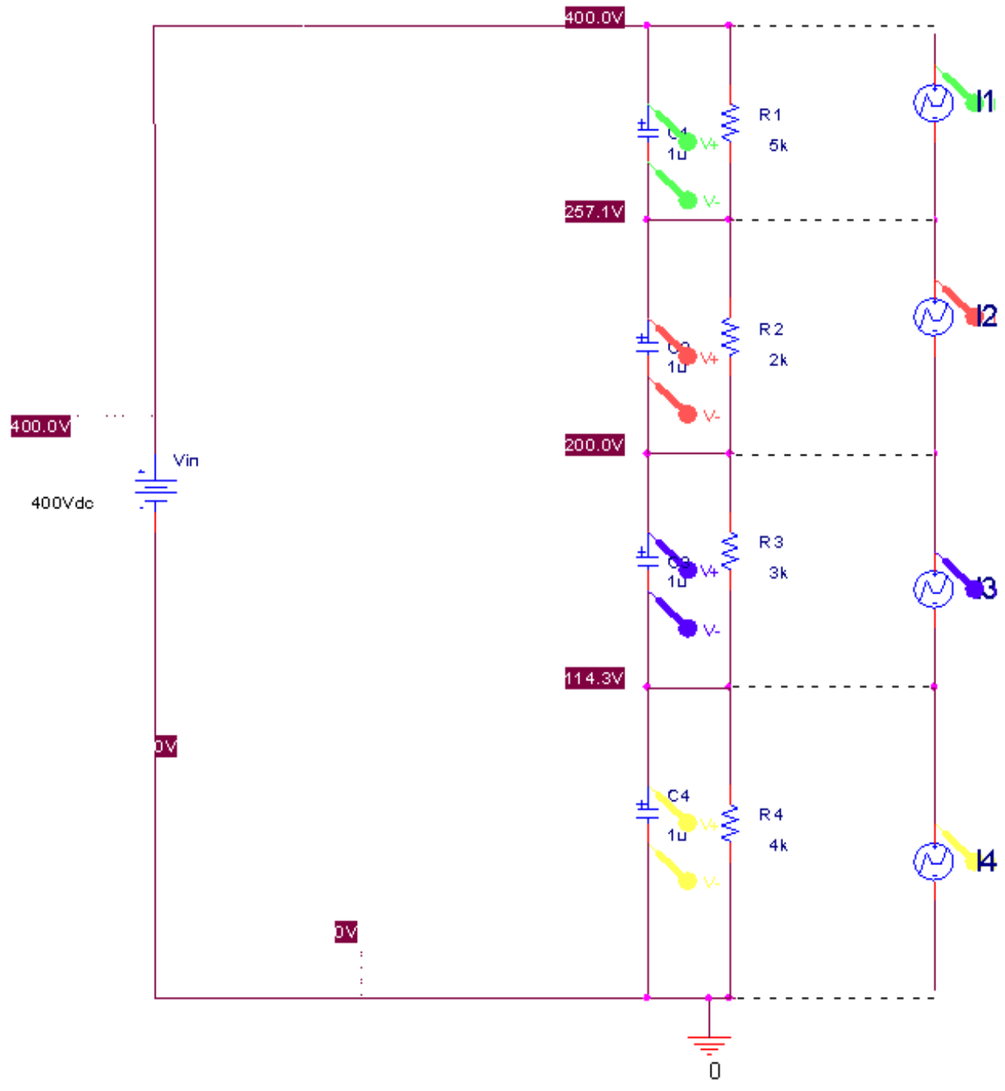
(a)



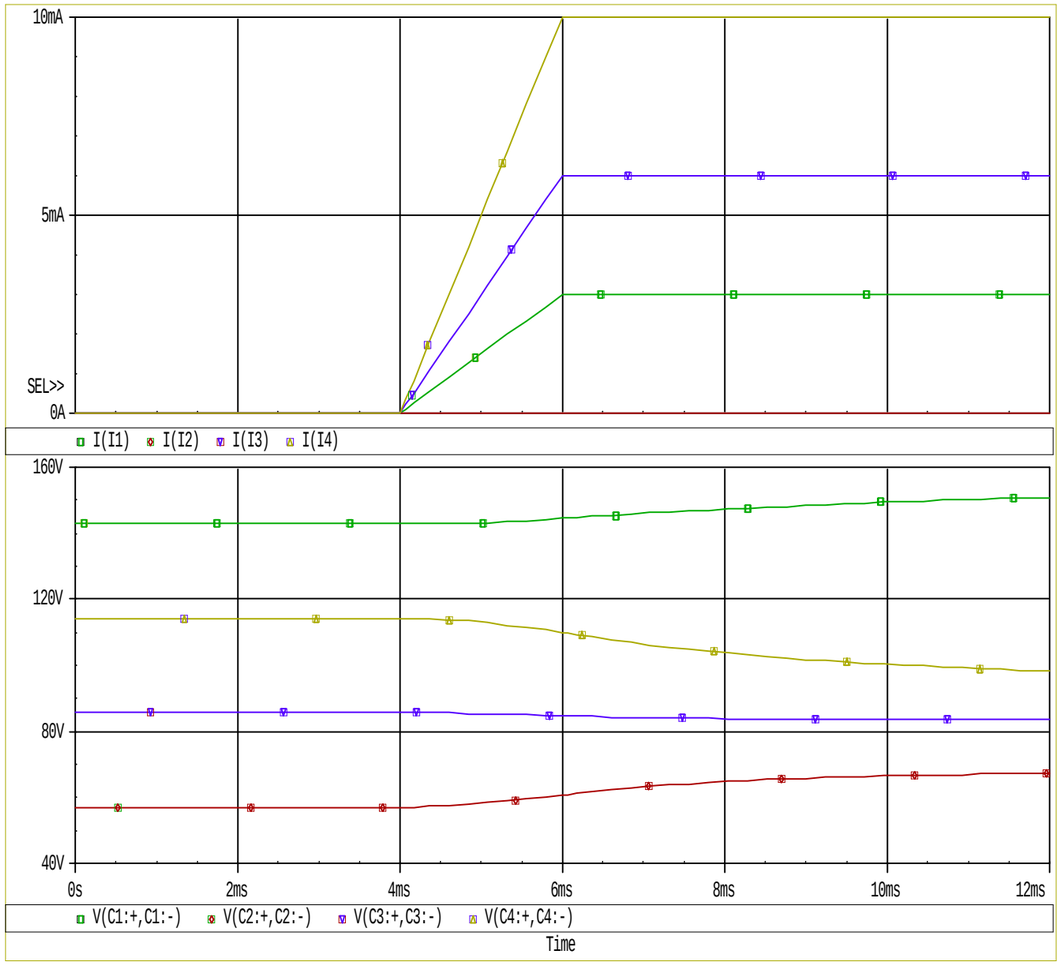
(b)

Fig 2.11: (a) The simulation setup with varied loads (i.e. R_1, R_2, R_3 and R_4). (b) Here, voltages became imbalanced i.e. voltage level became asymmetric across capacitors such as higher voltage for higher load (lower). So, for $R_1>R_4>R_3>R_2$ corresponding voltage is $V_{C1}>V_{C4}>V_{C3}>V_{C2}$.

2.2.6 Impact of Loads vary and also Leakage current dispersion



(a)



(b)

Fig 2.12: (a) The simulation setup with varied loads (i.e. $R_1>R_4>R_3>R_2$) and different leakage currents (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}) applied in four capacitors. (b) Here, voltages became imbalanced i.e. voltage level became asymmetric across capacitors such as higher voltage for higher load (lower) when load varies; besides, V_{C3} and V_{C4} showing decreasing trend and V_{C1}, V_{C2} showing increasing trend (lower) when applying leakage current dispersion (upper) i.e. and I_{L1} = 3mA, I_{L2} = 0mA, I_{L3} = 6mA and I_{L4} = 10mA.

Chapter 3

Design of Regulating Circuit and Improvement Analysis

3.1 Design of the Regulating Circuit

The designed control circuit is shown in Fig. 3.1. The control method is established based on the use of op amps.

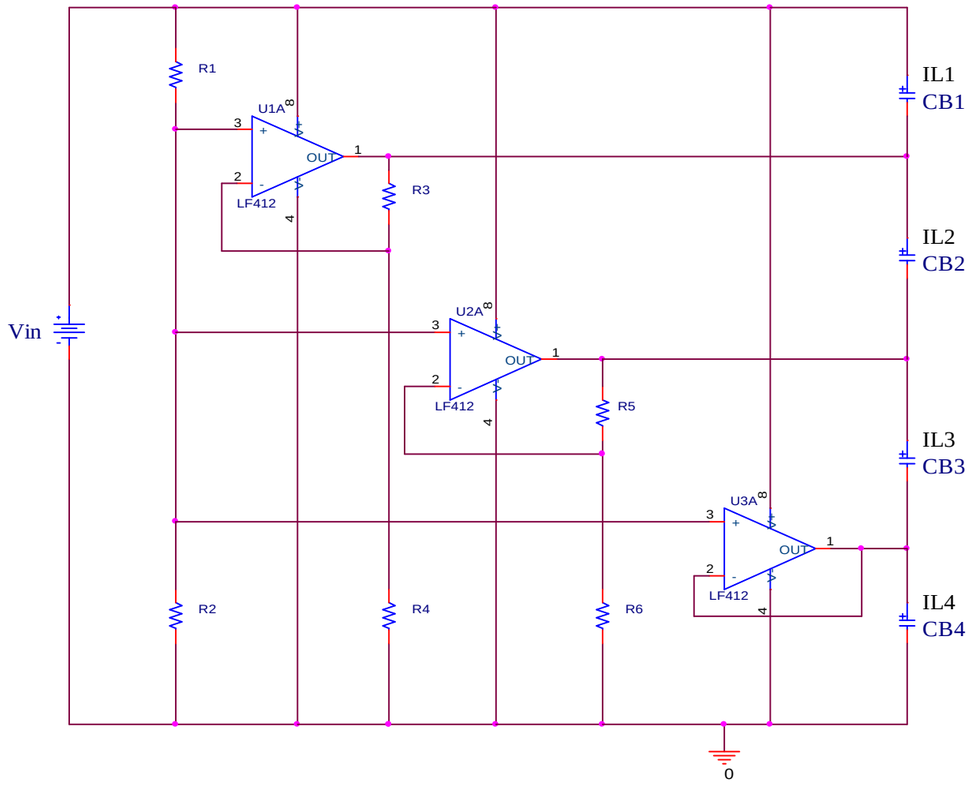


Fig 3.2: The proposed circuit to compensate the voltage imbalance due to leakage current dispersion for a four electrolytic capacitors in series connection.

Op amps are used for the push-pull of the required current to compensate the voltage imbalance occurred due to leakage current dispersion among capacitors. Suitable op amp LF412 is selected for the voltage compatibility [19]. Both bias current and offset voltage are assumed to be negligible. The reference voltage is set to 9 volts for each of the op amps at (+) inputs and voltage feedback is taken from corresponding capacitors at (-) inputs. In this design, the required number of op amps is equal to the number of junction points between two capacitors. The output pin of op amps are connected with each junction points between two capacitors.

To facilitate the dividing of bus voltage, four electrolytic capacitors are connected in series. For the simplicity of analysis, 36 V_{dc} (V_{in}) is divided into four equal 9 volts. The leakage currents are denoted as I_{L1}, I_{L2}, I_{L3} and I_{L4} and voltage as $V_{CB1,}$ V_{CB2}, V_{CB3} and V_{CB4} across capacitors C_{B1}, C_{B2}, C_{B3} and C_{B4} respectively. (Note: here B is used as subscript for the circuit with balanced condition).

3.1.1 Various Electrolytic Capacitors

There are wide verities of electrolytic capacitors of different values ranging from few pF (pico farad) to thousands of µF (micro farad). These capacitors are also available for various voltage ratings e.g. few volts to thousands of voltages [20].

3.1.2 Making the regulating circuit using op amps

In this thesis, the op amps will be used to mitigate the voltage imbalances caused by the leakage current dispersion as well as load variation. Op amps are biased from the dc bus as designed as shown in Fig 3.1. It is apparent that for the voltage compatibility for the proposed circuit it may become a challenge to find the appropriate op amps. But there are several ways to build a circuitry based on basic components for the op amp functionality. In chapter 1, different ways have been mentioned for the design consideration for the op amp functionality. Also, data sheet for high voltage op amps are also available to consult for necessary information, for example in [21].

Moreover**,** to minimize the quiescent losses the resistance value of the voltage divider should be chosen as high as possible.

3.2 Improvements after applying the control technique

To overcome the voltage imbalance occurred due to leakage current dispersion among capacitors the designed method is applied (Fig 3.2) and the improvements are shown in Fig 3.3. The results are found satisfactory for all sorts of leakage current dispersion as considered in Table 2.1 and for corresponding graphs as shown in Fig 2.2 (a), (b), (c) and (d).

With the application of control technique, the voltages across four capacitors are maintained at 9 volts as desired, despite impacts of leakage current dispersions, shown in Fig 3.2 (a) to (d). A negligible variation in voltages levels is observed. In Fig 3.3 (a) an oscillation is found for abrupt appearance of leakage currents as given in Fig 2.2 (a).

Improving the impact of leakage current dispersion for two capacitors in series, where simulation setup as given in Fig 3.4 (a) and Fig 3.5 (a) respectively with leakage current applied in C_{B1} (i.e. I_{L1}) and in C_{B2} (i.e. I_{L2}) and corresponding voltage maintaining at desired level across capacitors are shown in Fig 3.4 (b) and Fig 3.5 (b) respectively. Then, to improve the impact of leakage current dispersion for four capacitors in series, where simulation setup with varied leakage current applied in four capacitors (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}) and the regulating circuit is given in Fig 3.5 (a) and as the effect of deploying the regulating circuit voltages remained balanced despite different dispersion among applied leakage currents which are shown in Fig 3.6 (b), Fig 3.7, Fig 3.8, Fig 3.9 and Fig 3.10.

Now, applying simulation setup with designed circuit to maintain the voltage symmetry for varied loads (i.e. R_1, R_2, R_3 and R_4) as given in Fig 3.11 (a) and as a result voltage level remained symmetric across capacitors as shown in Fig 3.11 (b). Also, applying the regulating technique for both varied loads and leakage current dispersion as given in Fig 3.12 (a) and therefore keeping the symmetry of voltages and maintaining the balance in voltages are shown in Fig 3.12 (b).

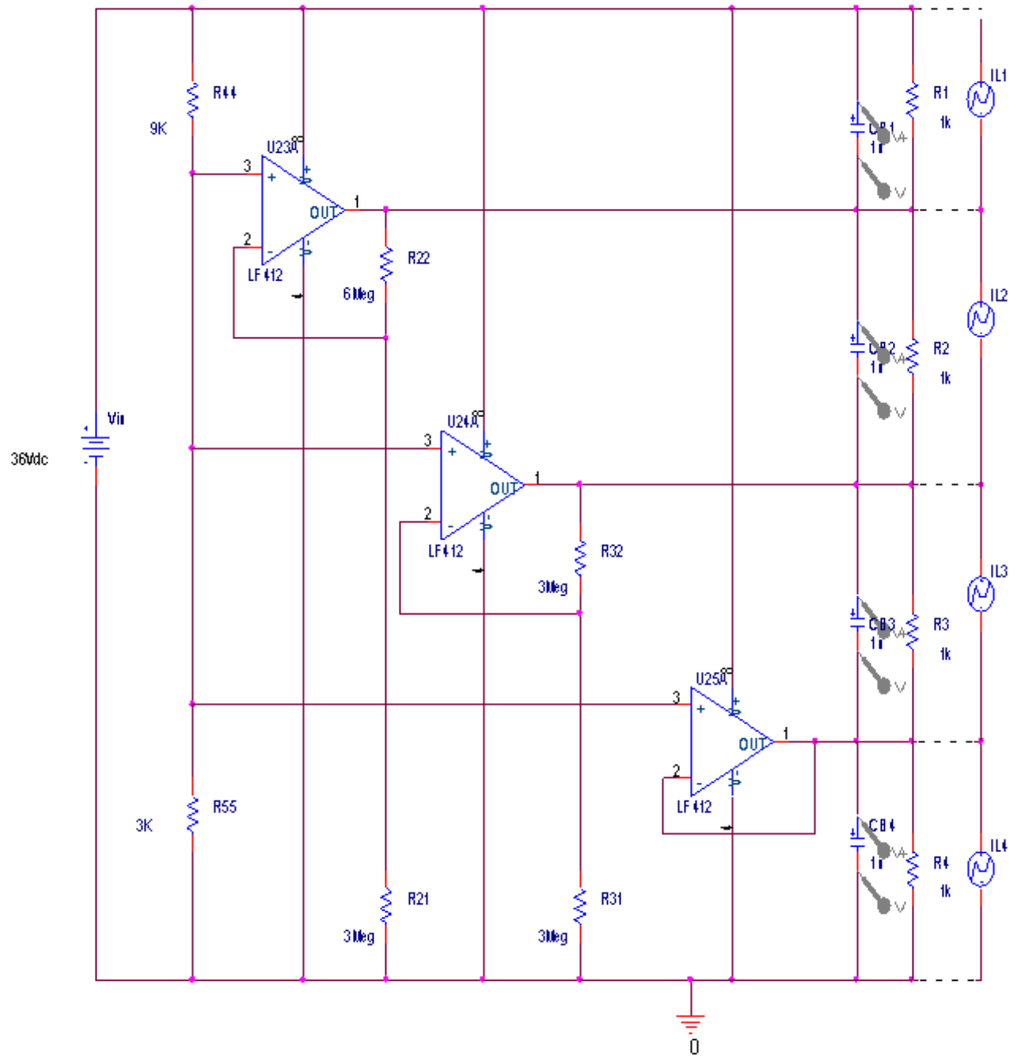
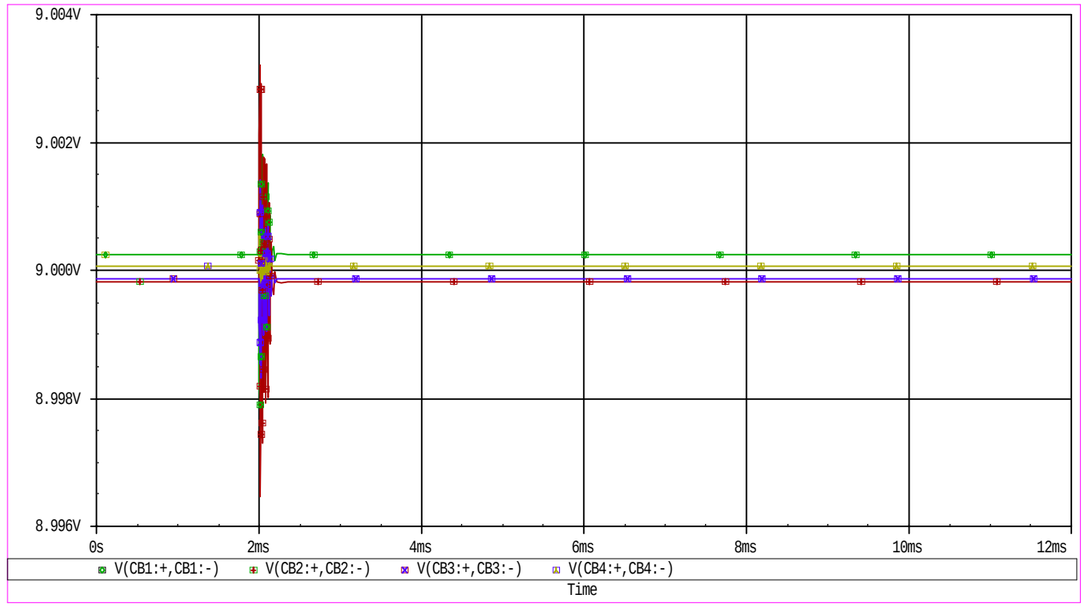
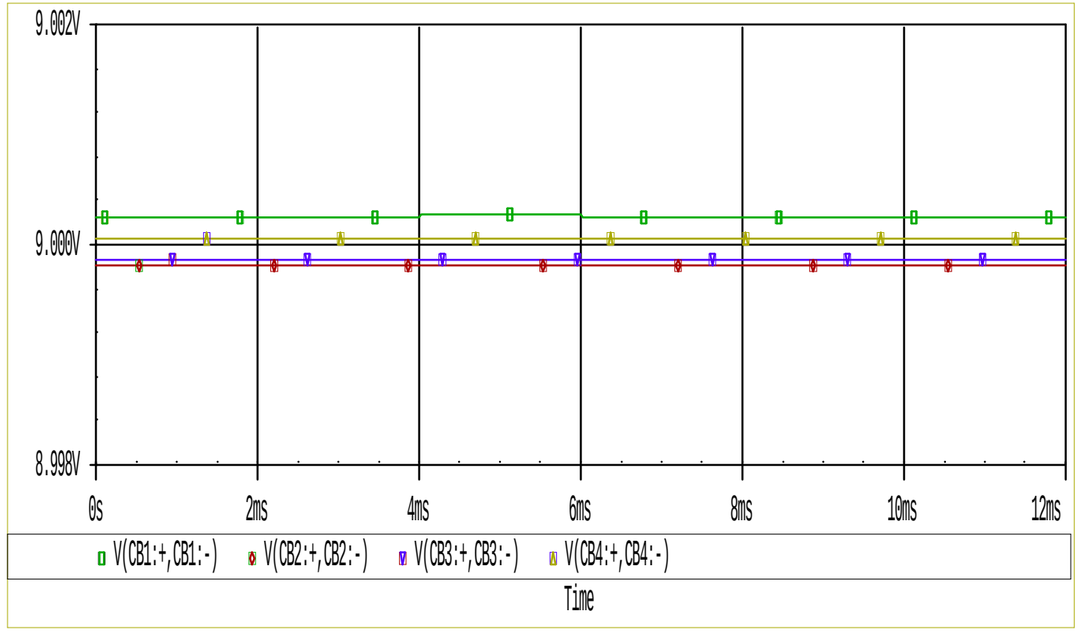


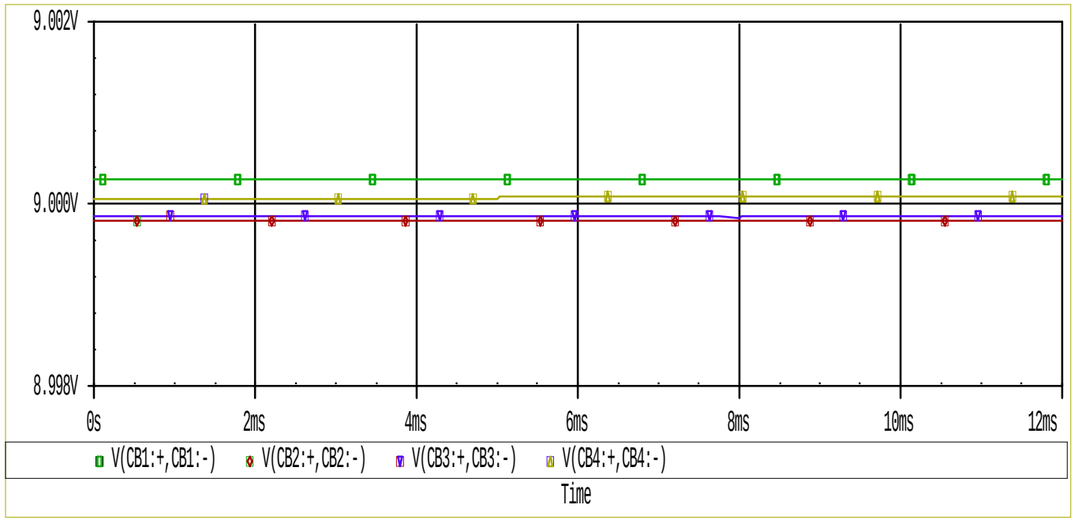
Fig 3.2: The simulation setup for the circuit to compensate the voltage imbalance due to leakage current dispersion for four electrolytic capacitors in series connection.


9.004V
9.002V
9.000V
8.998V
8.996V
0s
2ms
4ms
6ms
8ms
10ms
12ms
V(CB1:+,CB1:-)
V(CB2:+,CB2:-)
V(CB3:+,CB3:-)
V(CB4:+,CB4:-)
Time

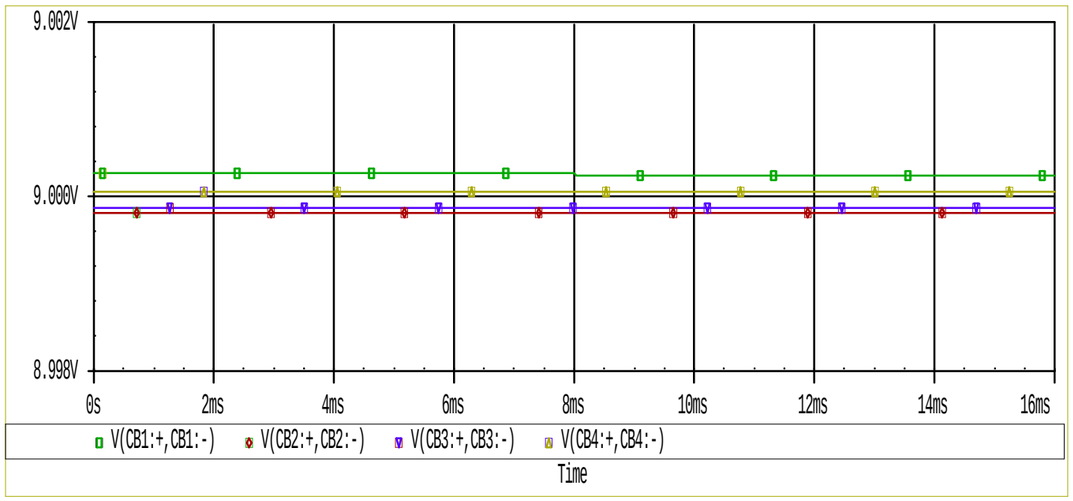
(a)


9.002V
9.000V
8.998V
0s
2ms
4ms
6ms
8ms
10ms
12ms
V(CB1:+,CB1:-)
V(CB2:+,CB2:-)
V(CB3:+,CB3:-)
V(CB4:+,CB4:-)
Time

(b)



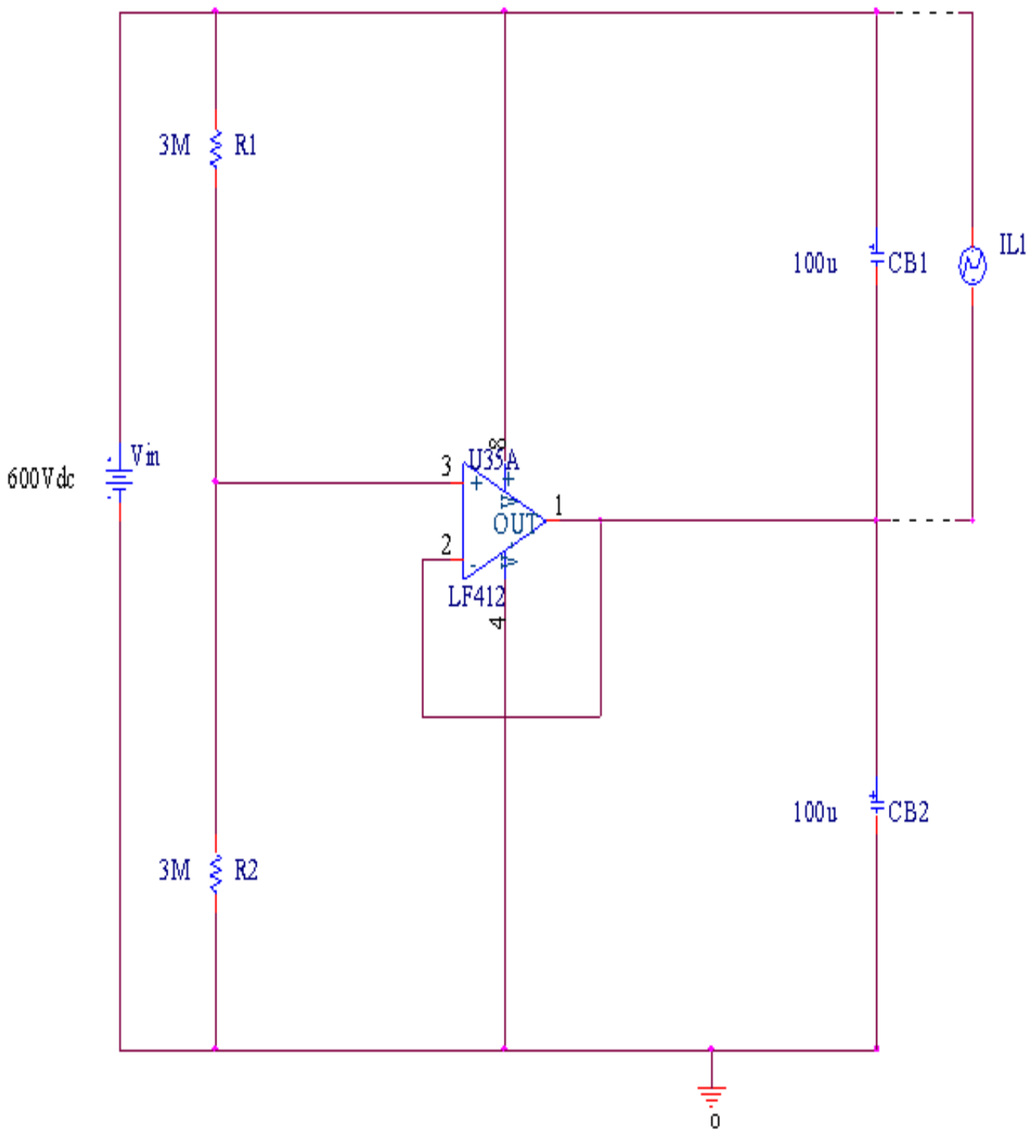
(c)



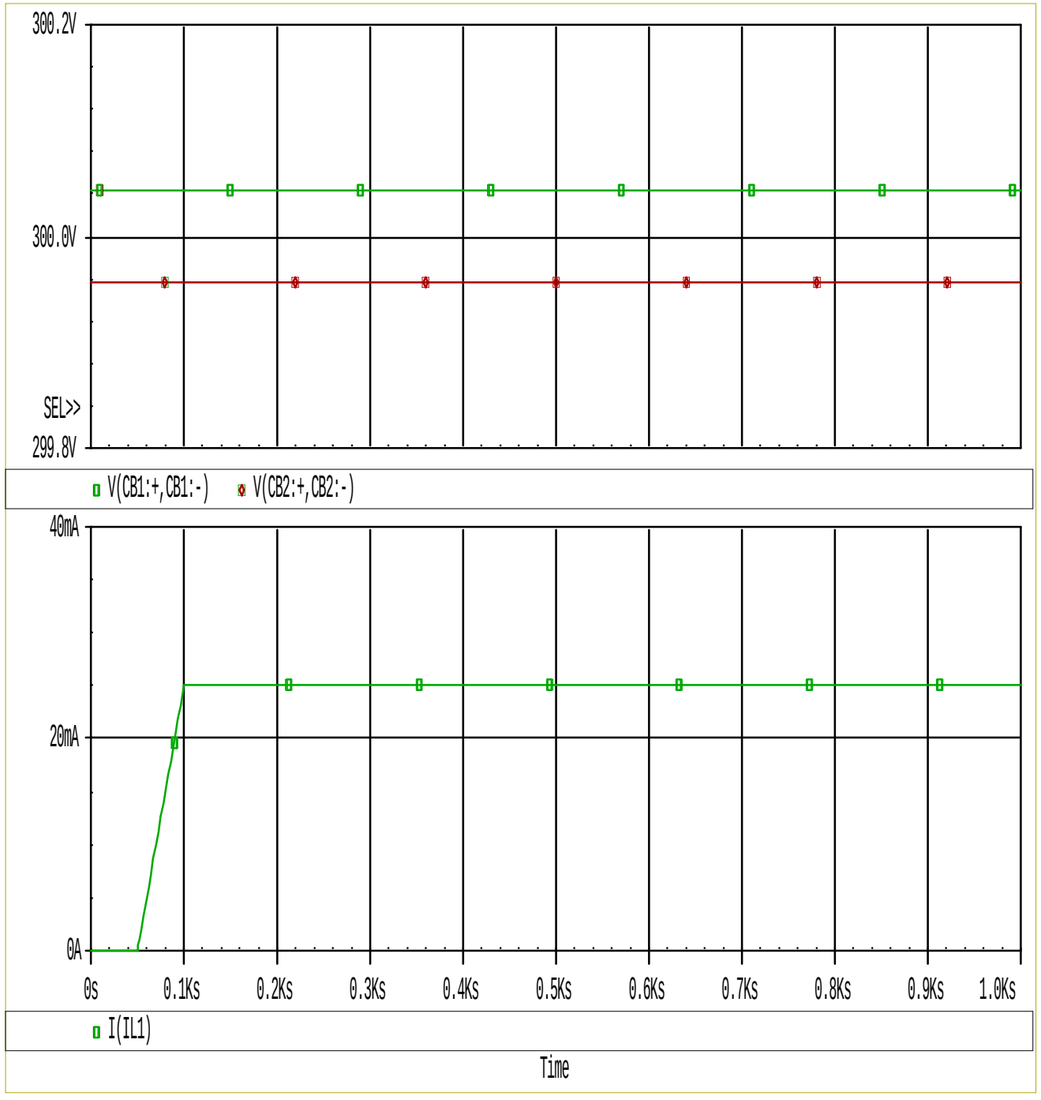
(d)

Fig 3.3: Improvements after applying the control technique, here in (a) to (d) shows that voltages are maintained at $V_{CB1} = V_{CB2} = V_{CB3} = V_{CB4} = 9$ volts across four capacitors despite leakage current dispersion (shown in Fig 2 (a), (b), (c) and (d)) impacts with a negligible deviation in voltage levels; also, in (a) Zoomed view of the simulation result shows an oscillation for abrupt appearing of leakage currents.

3.3 Improving the impact for two capacitors in series

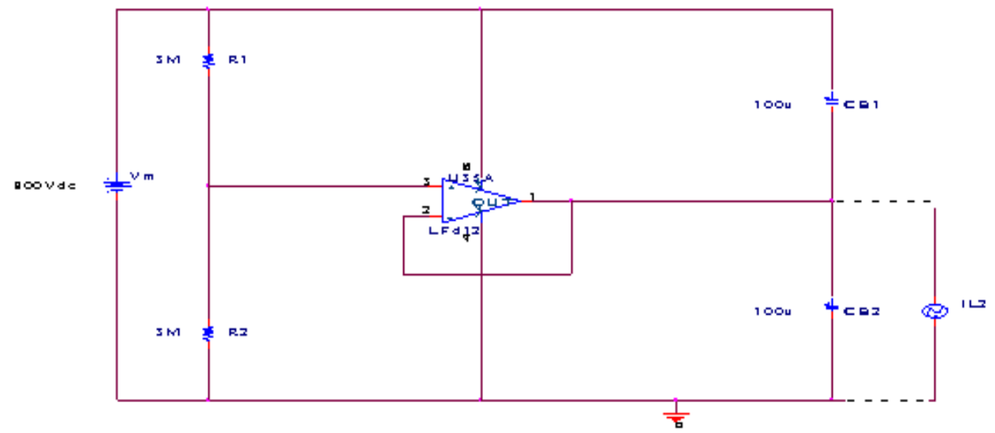


(a)

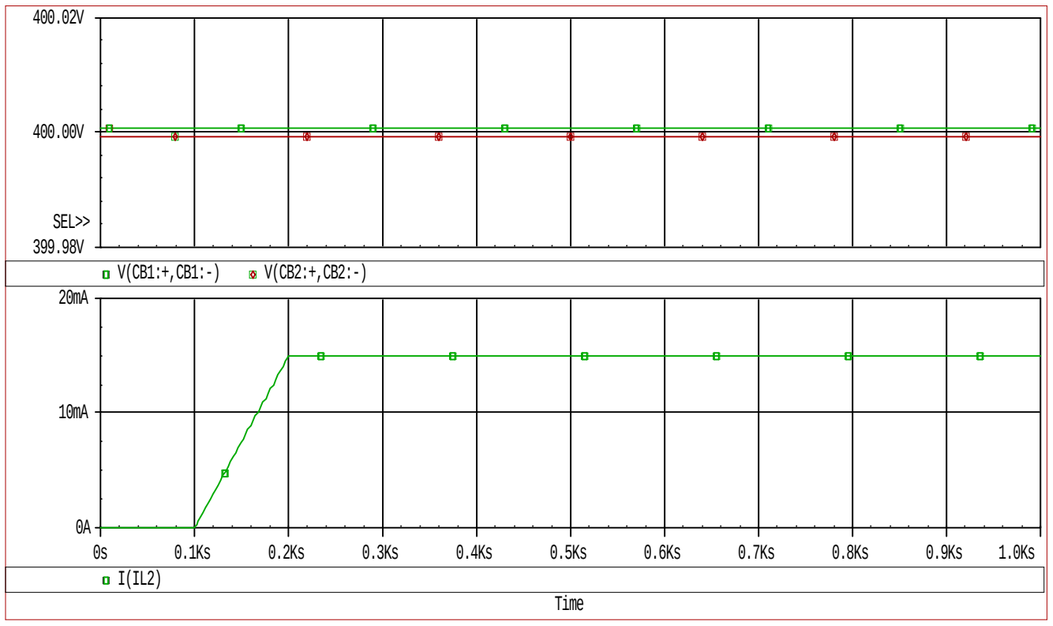


(b)

Fig 3.4: (a) Shows the simulation setup with leakage current applied only in C_{B1} (I_{L1}); (b) Voltages are maintained at V_{CB1} = V_{CB2} = 300 volts across two capacitors with a negligible deviation in voltage levels (upper), despite leakage current dispersion (lower) at I_{L1} = 25mA and no leakage current for C_2.



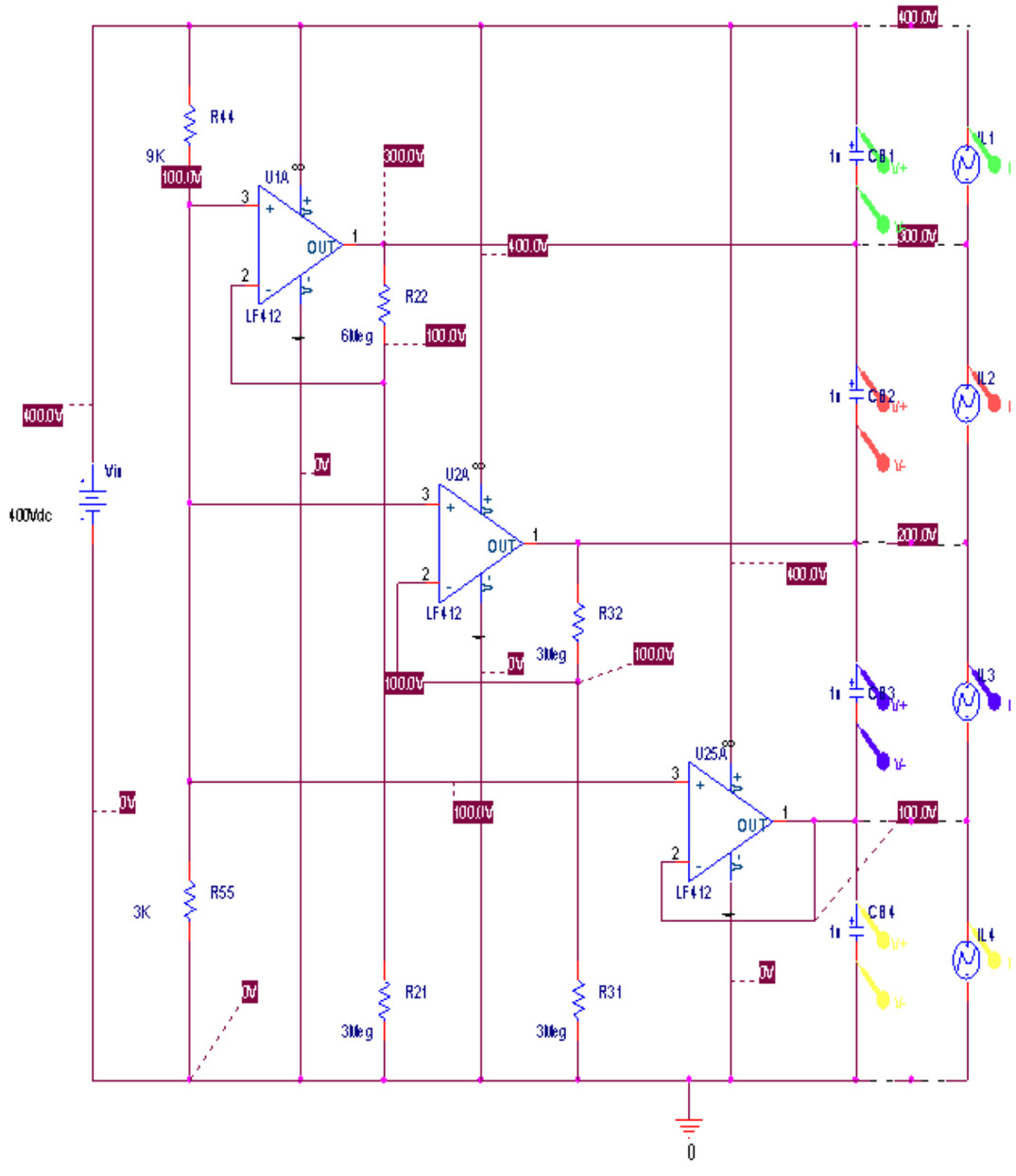
(a)



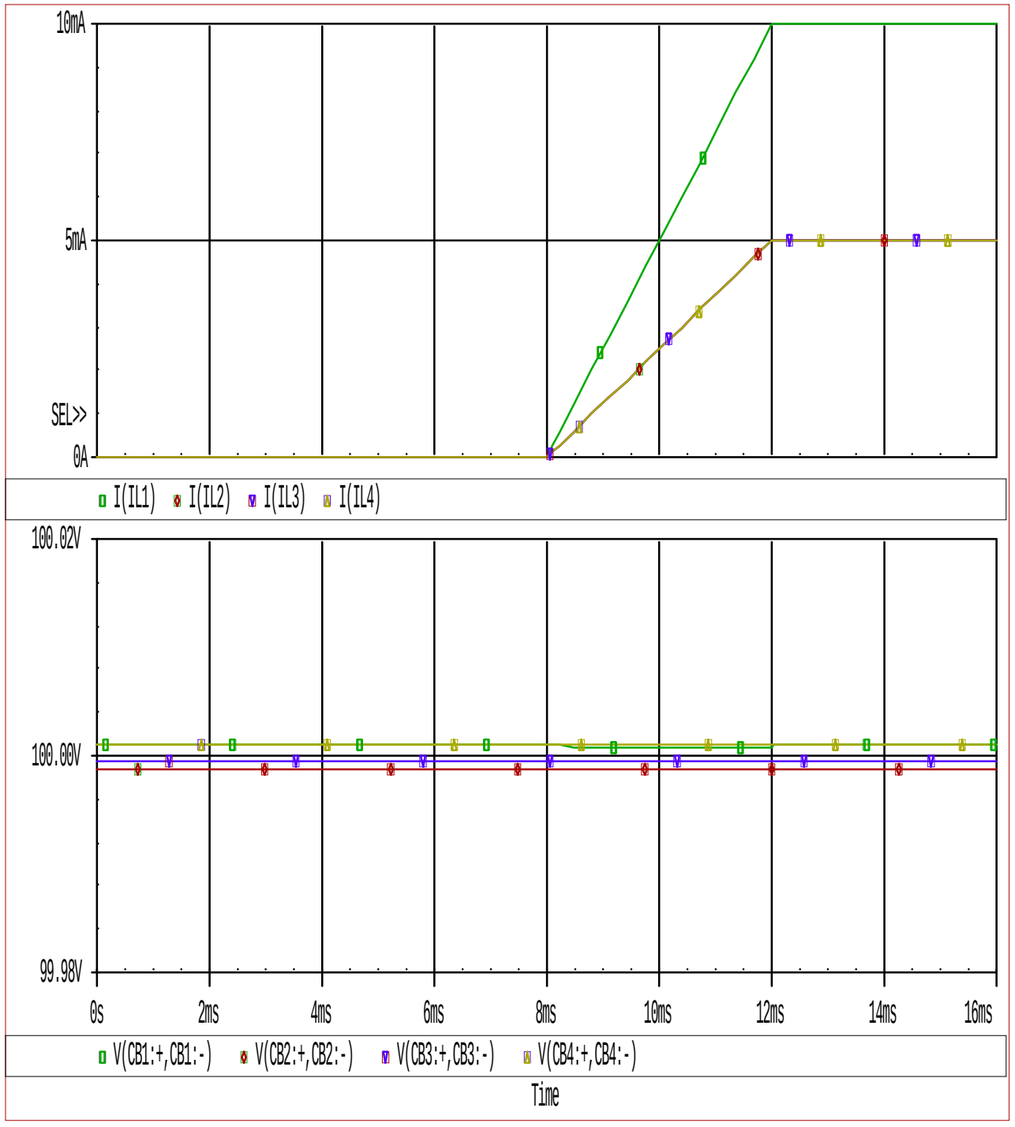
(b)

Fig 3.5: (a) Shows the simulation setup with leakage current applied only in C_{B2} (I_{L2}); (b) Voltages are maintained at V_{CB1} = V_{CB2} = 400 volts across two capacitors with a negligible deviation in voltage levels (upper), despite leakage current dispersion (lower) at I_{L2} = 15mA and no leakage current for C_1.

3.4 Improving the Impact for four capacitors in series



(a)



(b)

Fig 3.6: (a) Shows the simulation setup for the improvement for the impact of varied leakage current applied in four capacitors (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}); (b) Voltages are maintained at V_{CB1} = V_{CB2} = V_{CB3} = V_{CB4} = 100 volts across four capacitors with a negligible deviation (lower), despite leakage current dispersion (upper) i.e. I_{L1} = 10mA and I_{L2} = I_{L3} = I_{L4} = 5mA.

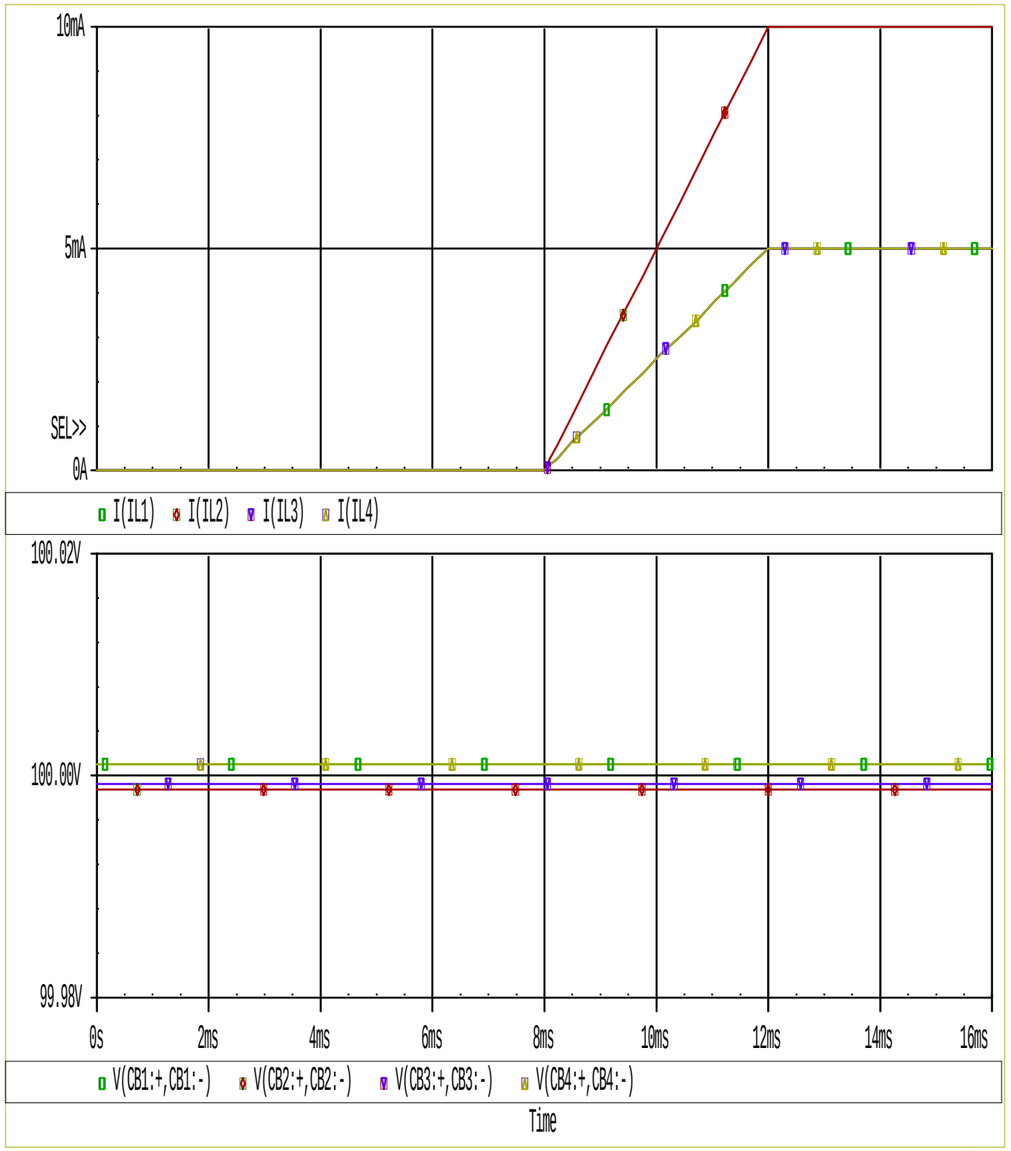


Fig 3.7: The simulation setup for the improvement for the impact of varied leakage current applied in four capacitors (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}) as shown in Fig 3.5 (a). Here, voltages are maintained at $V_{CB1} = V_{CB2} = V_{CB3} = V_{CB4} = 100$ volts across four capacitors with a negligible deviation (lower), despite leakage current dispersion (upper) i.e. $I_{L2} = 10mA$ and $I_{L1} = I_{L3} = I_{L4} = 5mA$.

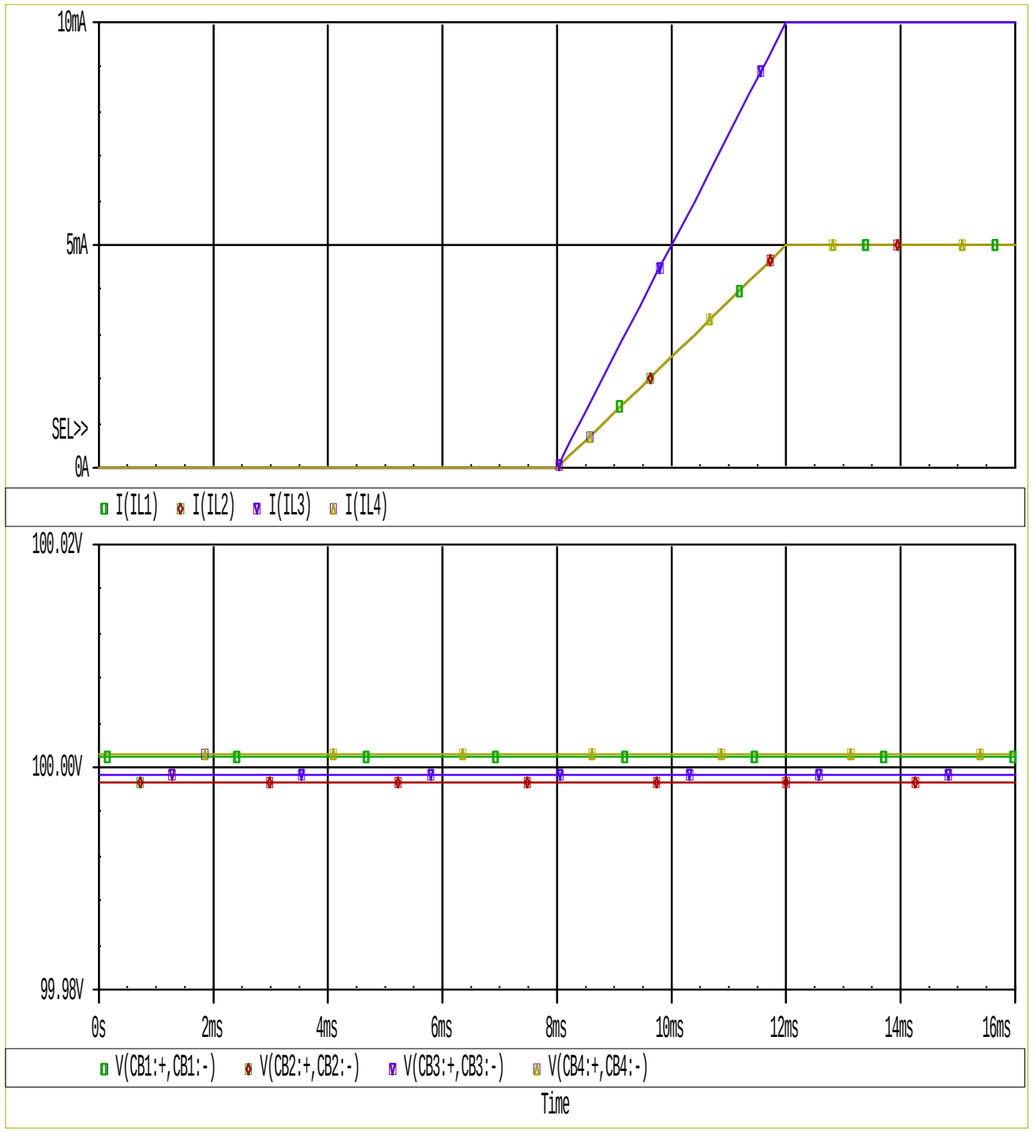


Fig 3.8: The simulation setup for the improvement for the impact of varied leakage current applied in four capacitors (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}) as shown in Fig 3.5 (a). Here Voltages are maintained at $V_{CB1} = V_{CB2} = V_{CB3} = V_{CB4} = 100$ volts across four capacitors with a negligible deviation (lower), despite leakage current dispersion (upper) i.e. $I_{L3} = 10mA$ and $I_{L1} = I_{L2} = I_{L4} = 5mA$.

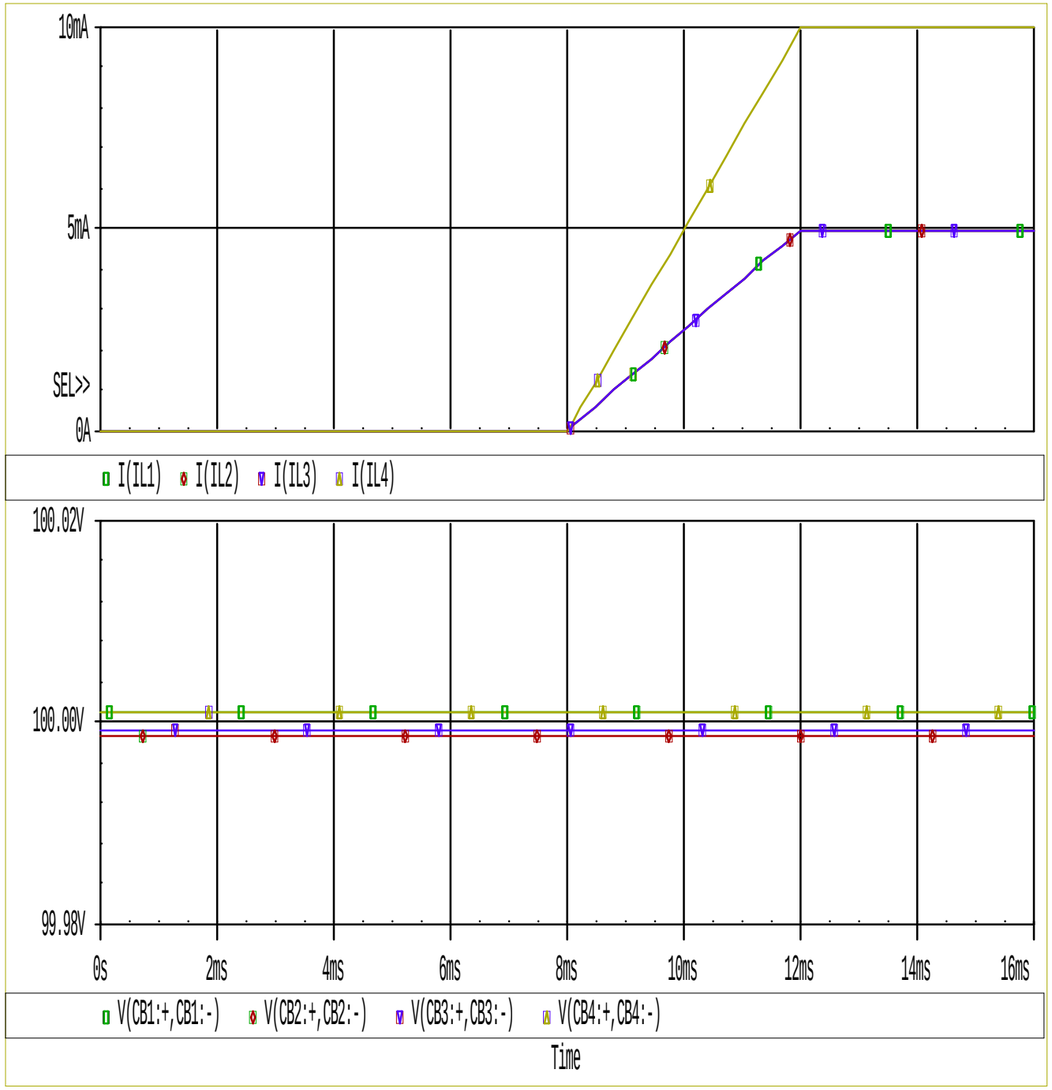


Fig 3.9: The simulation setup for the improvement for the impact of varied leakage current applied in four capacitors (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}) as shown in Fig 3.5 (a). Here Voltages are maintained at $V_{CB1} = V_{CB2} = V_{CB3} = V_{CB4} = 100$ volts across four capacitors with a negligible deviation (lower), despite leakage current dispersion (upper) i.e. $I_{L4} = 10mA$ and $I_{L1} = I_{L2} = I_{L3} = 5mA$.

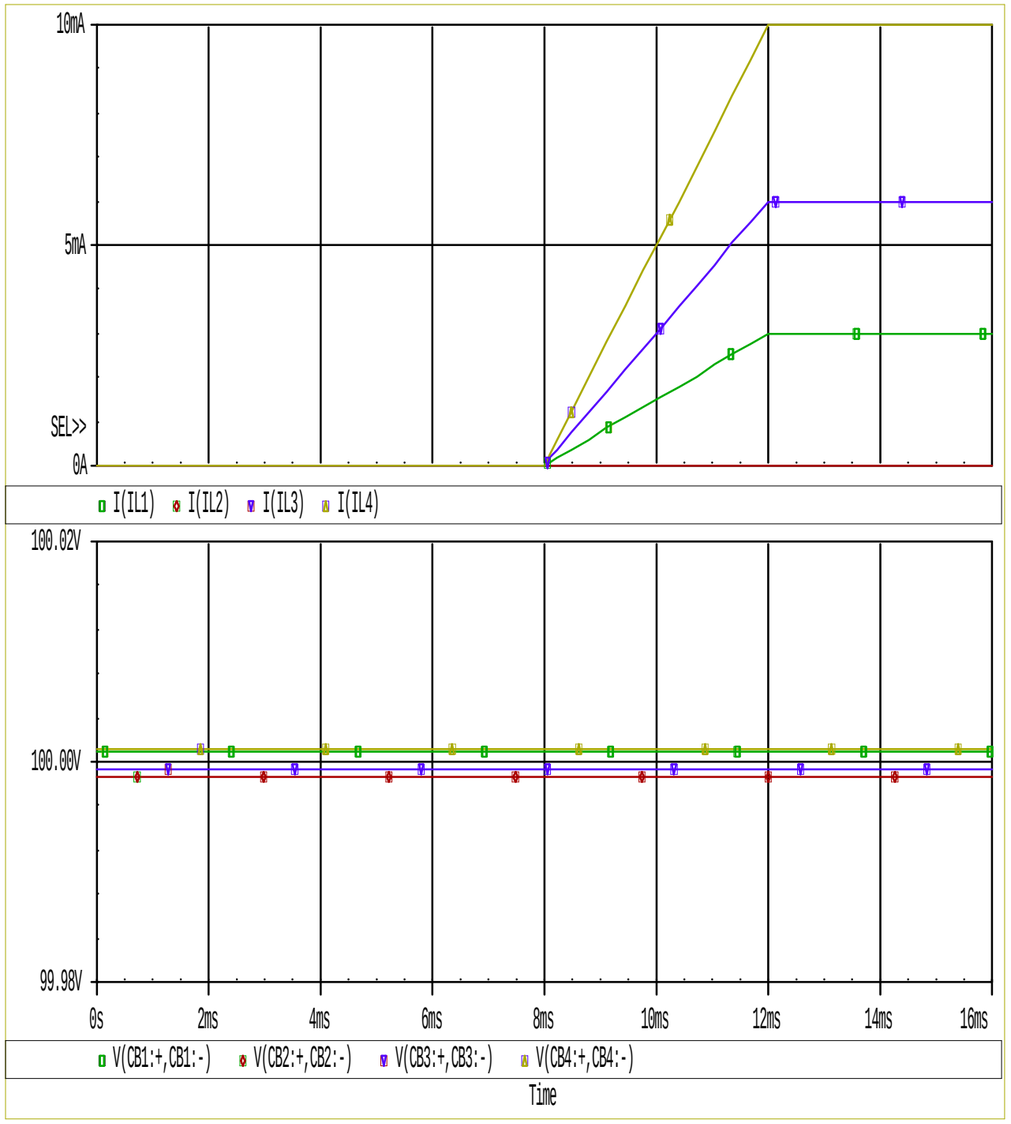
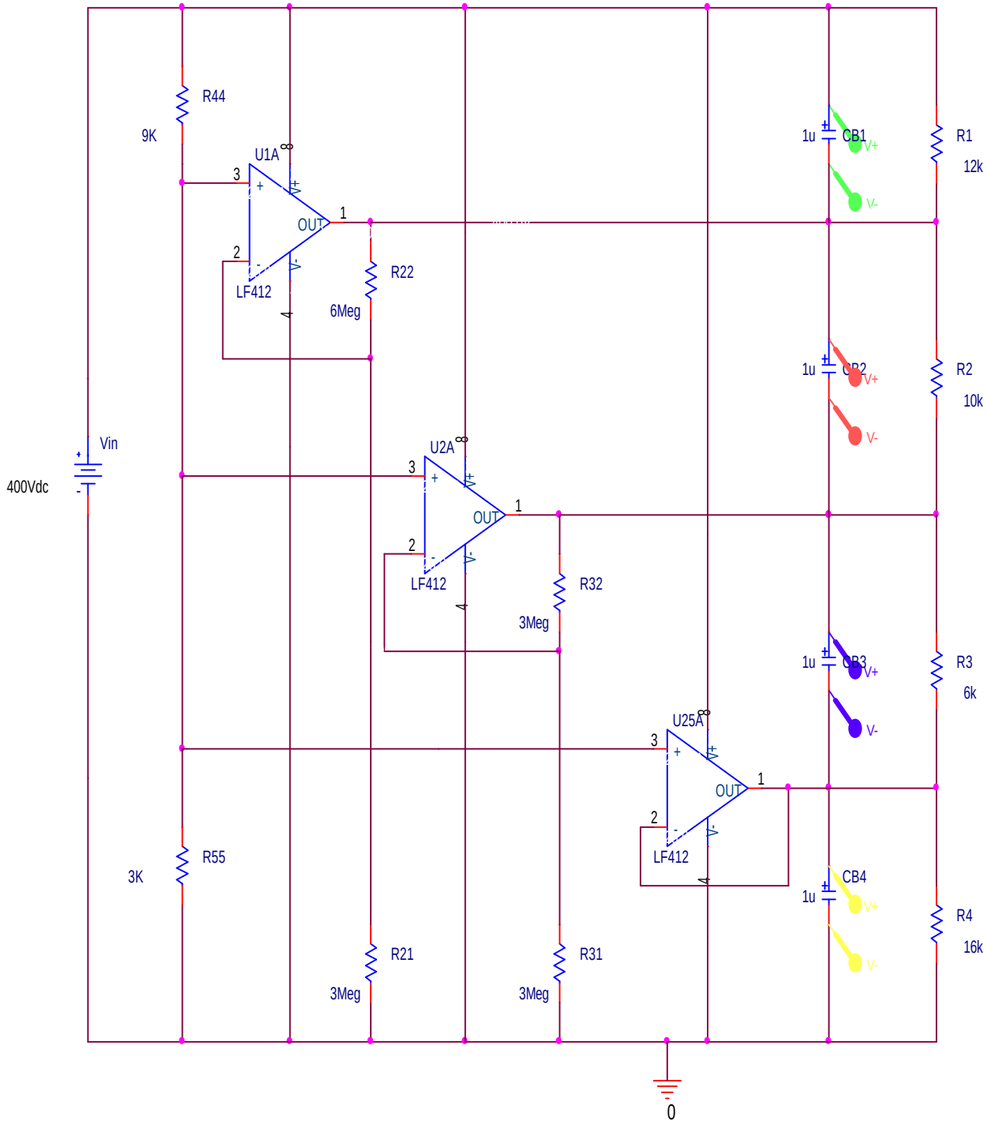
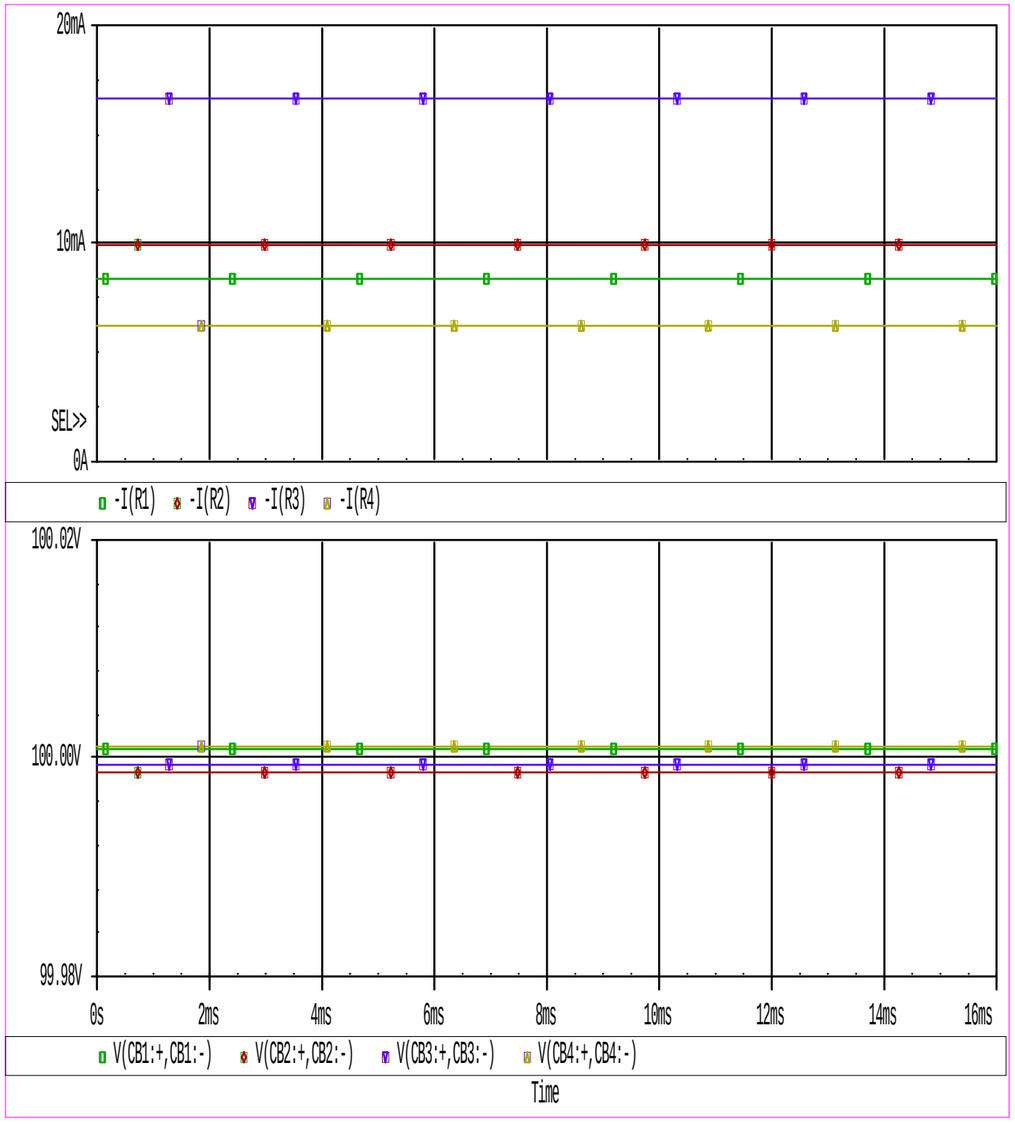


Fig 3.10: The simulation setup for the improvement for the impact of varied leakage current applied in four capacitors (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}) as shown in Fig 3.5 (a). Here Voltages are maintained at $V_{CB1} = V_{CB2} = V_{CB3} = V_{CB4} = 100$ volts across four capacitors with a negligible deviation (lower), despite leakage current dispersion (upper) i.e. $I_{L1} = 3mA$, $I_{L2} = 0mA$, $I_{L3} = 6mA$ and $I_{L4} = 10mA$.

3.5 Improving the impact of load vary



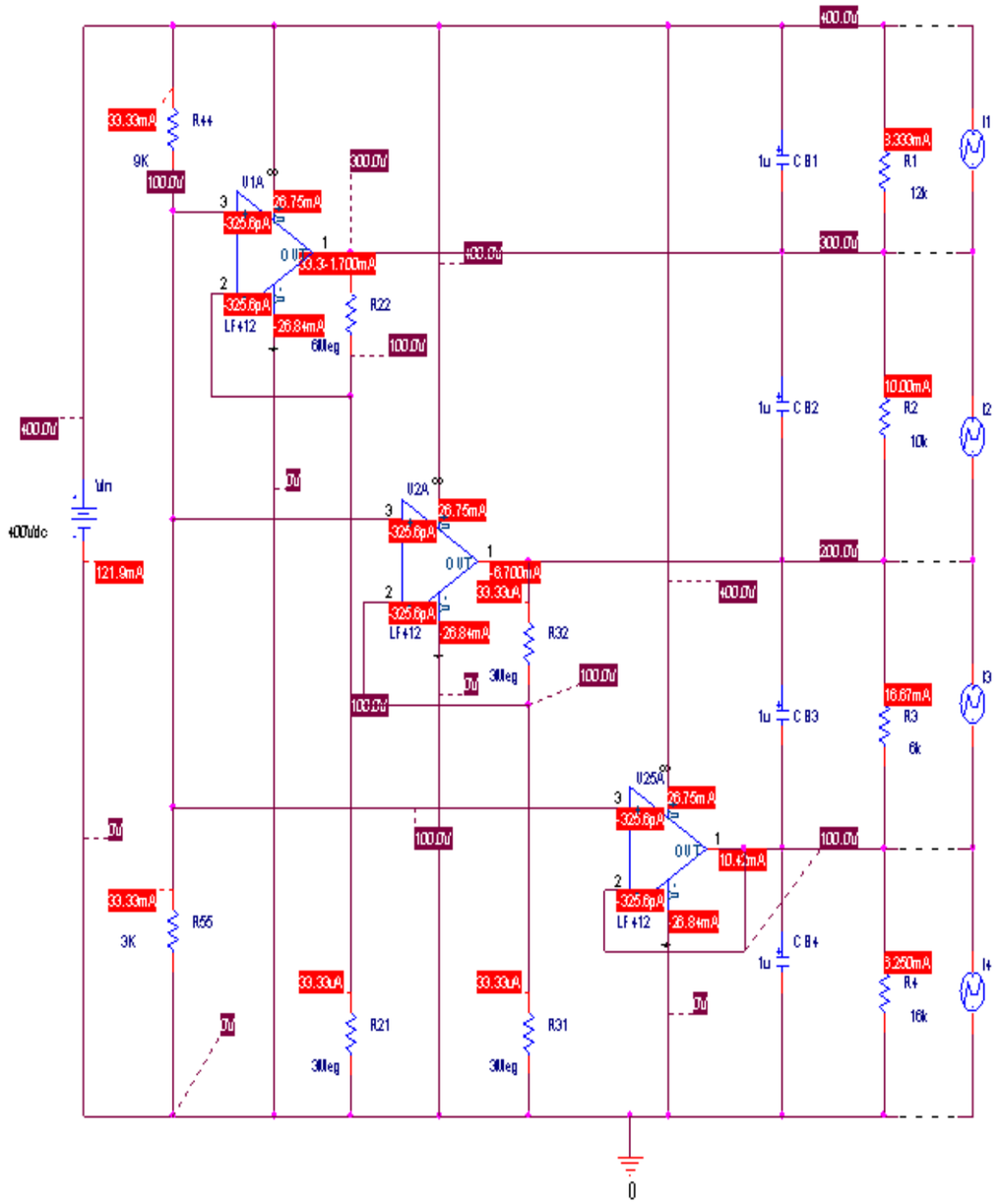
(a)



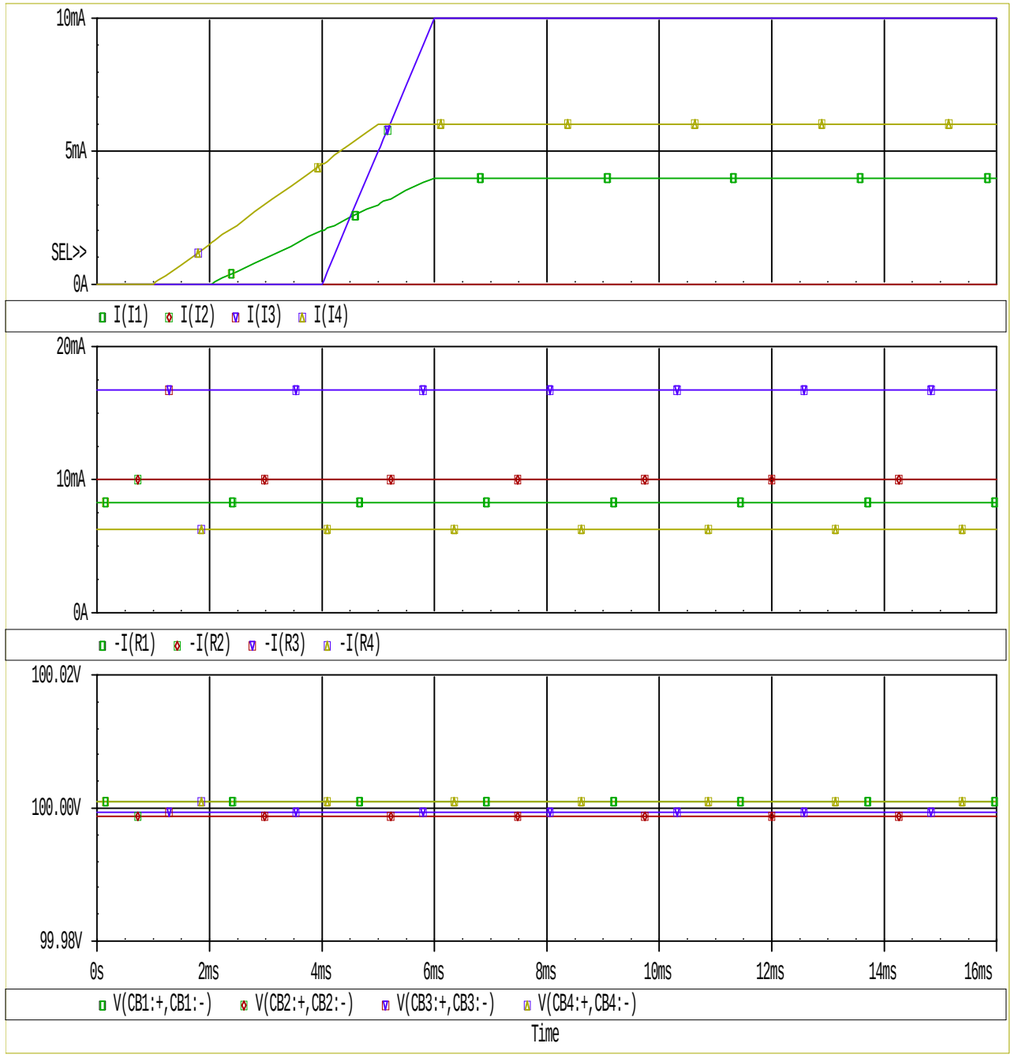
(b)

Fig 3.11: (a) The simulation setup for the improvement for the impact of varied loads (i.e. R_1, R_2, R_3 and R_4) applied across four capacitors. (b) Here, voltages are maintained at $V_{CB1} = V_{CB2} = V_{CB3} = V_{CB4} = 100$ volts across four capacitors with a negligible deviation (lower), despite varied loads as $R_4 > R_1 > R_2 > R_3$ i.e. varied load current $I_{R3} > I_{R2} > I_{R1} > I_{R4}$ (upper).

3.6 Improving despite Load Vary and leakage current dispersion



(a)



(b)

Fig 3.12: (a) The simulation setup for the improvement for the impact of varied loads (i.e. $R_4>R_1>R_2>R_3$) and different leakage currents (i.e. I_{L1}, I_{L2}, I_{L3} and I_{L4}) applied across four capacitors. (b) Here, voltages are maintained at $V_{CB1} = V_{CB2} = V_{CB3} = V_{CB4} = 100$ volts across four capacitors with a negligible deviation (lower), despite varied load currents (middle) i.e. $I_{R3}>I_{R2}>I_{R1}>I_{R4}$ and leakage current dispersion (upper) i.e. $I_{L1} = 3$mA, $I_{L2} = 0$mA, $I_{L3} = 6$mA and $I_{L4} = 10$mA.

Chapter 4

Conclusion and Suggestion for future work

4.1 Conclusions

A control technique is designed and applied to overcome the voltage instability due to leakage currents dispersion for series connected capacitors. The analysis is done using both two and four electrolytic capacitors in series to divide the bus voltage. The proposed design is successful for various leakage current dispersions as well as for varied load. The results are with negligible deviation. This is an approach with less design complexity.

From this thesis using the designed technique can be concluded as follows:

- ? All previous works were for two series capacitors only. In this thesis, four series connected capacitors are included.
- ? Replaces balancing resistances and thus reduces the resistive loss.
- ? Regulate the impact of leakage current dispersion and maintain voltage balancing among series connected capacitors.
- ? Saves the capacitors from unwanted over voltages and as a result extends the lifetime.
- ? Facilitate multiple outputs with the regulation for the impact of load variation.

4.2 Suggestion for Future Work

After reviewing the work of this thesis, it can be concluded that there are several opportunities for future work to improve the control method as well as to meet other goals.

- ? In this thesis, analysis was done for available component in simulation software. So, practical implementation with high voltage components can be verified.
- ? Regulations of equal voltages across two and four capacitors for various leakage currents were verified. Analysis can be done to regulate the predefined unequal voltages across capacitors.

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