Ultra Wideband Receiver Design for on-chip Wireless Interconnect

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by

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(Mohammad Ariful Haque)

Dedication

To my parents.

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List of Abbreviations

ILD	Inter Level Dielectric
TOF	Time of Flight
UWB	Ultra Wideband
TR	Transmitted Reference
SRD	Step Recovery Diode
PPM	Pulse Position Modulation
PAM	Pulse Amplitude Modulation
BPM	Bi-Phase Modulation
OOK	On Off Keing
BER	Bit Error Rate
AWGN	Additive White Gaussian Noise
SNR	Signal to Noise Ratio
SER	Symbol Error Probability
LNA	Low Noise Amplifier

Acknowledgement

All praises and thanks belong to Allah, the exalted for His innumerable favors and bounties that only He knows the amount of. It is He who has granted me physical and mental capabilities to complete the thesis work, without anything or anyone compelling Him to do so.

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Last but not least, I remember my parents who are always a source of my inspiration in every good action.

Abstract

The information revolution and upcoming era of silicon ultra large-scale integration (ULSI) have demanded an ever-increasing level of functional integration on single chip structure, driving a need for greater circuit density and higher performance. While traditional transistor scaling has thus far met this challenge, interconnect scaling has become the performance-limiting factor for new designs. In this thesis, we investigated the potentials of wireless on-chip interconnects system using for the future ULSI. It has been proposed, for the first time, transmitted reference (TR) Ultra Wideband (UWB) communication for intra-chip wireless interconnects system. This approach allows a straight-forward synchronization technique by giving proper delay to the reference pulse and thus avoids complicated intra-chip channel estimation for the detection unit. Therefore it results a simplified transceiver architecture. Moreover TR technique provides excellent multiple access capabilities to implement software reconfigurable wireless channel. The system performance has been investigated under a new modulation scheme termed as PAM-PPM technique, which shows superior system performance over the conventional Biphase Modulation technique.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Since the invention of the integrated circuits in the late 1950s, the development of this remarkable device has been blessed by the laws of physics and the science of materials. The initial material choices – silicon substrates, silicon dioxide gate, intermediate dielectrics, aluminum interconnection and process such as planer technology and photolithography have stood the test of 50 years. In addition, the industry has taken the advantage of the fact that decreasing transistor size not only reduced cost, but also improved performance in terms of speed, functionality and power dissipation. However, the laws of physics and the science of materials are becoming less friendly as we approach 100 nm design regime. Despite remarkable experimental results for transistors well below this dimension, there are growing challenges to our ability to effectively stay on the technology roadmap [1].

To quantify the magnitude of the problem, the delay associated with an interconnect of length, d, with negligible series resistance, is proportional to d and the square root of the relative dielectric constant, ε_r, of the inter level dielectric (ILD). The delay time is usually called the time of flight (TOF) across the signal line of the given length. For an ILD of $\varepsilon_r = 4.0$ (SiO_2), the TOF is about 6 ps/mm. For an x-direction signal of interest, it is usually surrounded by many y-direction signal lines on an adjacent wiring layer. These orthogonal signal lines will add capacitance and further degrade the TOF to as much as 8 ps/mm. These numbers can be compared to the delays of a NAND gate with a fan out of 3, which are around 70, 30 and 12 ps for the 250-, 130- and 50- nm technologies respectively [2].

A microprocessor often requires a long interconnection line between the arithmetic logic unit (ALU) and the cache storage. As a first approximation, the length of this 'global' signal line can be assumed to be equal to the edge dimension of the chip- around 15 mm, 20 mm and 30 mm for the 250-, 130- and 50-nm chip generations. The TOFs for such lines would lie in the 125 to 250 ps range, increasing as the lines got smaller and the chips larger. These numbers range from 2 to 20 times the gate delay for the equivalent design rule, and are totally unacceptable burden in the device performance [3].

VLSI designers have identified various measures that could be undertaken to solve some, if not all of the problems being faced. The shift from aluminum to copper for metallization, the use of low k dielectric layer, reverse scaling of wire geometries, the inclusion of repeaters, and standard cell modification are some that already been successfully implemented. Nevertheless, these evolutionary approaches may soon encounter fundamental material limits. Revolutionary methods and techniques must be pursued to carry on the fast progress of future ULSI technology. One of such possibilities is to use "wireless interconnect using Si integrated antenna" [4, 5].

1.2 Advantages of on-chip wireless interconnect systems

With appropriate designs, RF/microwave signals can be transmitted efficiently through either free space or guided mediums. However, the efficient transmission and receiving of the RF/microwave signals in free space require the size of antennas to be comparable with their wavelengths. As the CMOS device dimensions continue to scale down, operating speeds and cut-off frequencies (f_t and f_{max}) of CMOS devices will exceed 100 GHz in the near future. At 24 GHz, the wavelength of electromagnetic waves in free space is 12.5 mm and in silicon it is 3.7 mm. This means a quarter wave antenna needs to be only 3 and 0.9 mm in free space and silicon respectively. These in

conjunction with the increase of chip sizes to 2 cm x 2 cm have made the integration of antenna for wireless interconnection possible.

Based on these considerations, the wireless interconnect system act as a miniature wireless LAN (local-area network). Compared to global electrical wires, this wireless scheme potentially offers several advantages. First, circuits can be synchronized over much larger chip sizes because wireless approach provides three to ten times faster transmission of signals, compared to global wires. In addition, the bandwidth of the wireless interconnect system is only limited by the bandwidth of the transmitting and receiving components and not by the transmission medium as opposed to the case of global wires. Also the cross talk between channel should be much improved using FDMA and CDMA communication technique. Furthermore, wireless approach can provide new flexibility to reconfigure the interconnect system simply by changing the CDMA codes.

To realize the aforementioned advantages of wireless interconnect systems, the potentials of using Ultra Wideband (UWB) communication technology as the signal transmission technique are being investigated [6]. UWB systems are based on the transmission of very short pulses, in the order of sub-nanoseconds, and do not use a frequency carrier to convey information. This scheme is particularly attractive for wireless interconnect systems for several reasons. First, it creates lees electrical overhead on the existing circuitry of the chip because of its simplified transceiver architecture [7]. It has been shown that on chip antenna can be effectively utilized for UWB pulse generator thus avoiding expensive and power hungry analog components [8]. Moreover, to achieve a high data rate with low BER using conventional data transmission technique, one needs a substantial amount of transmitted power. Large transmitted power results in increased power consumption, which generates extra heat in the chip. Since UWB systems use ultra short pulses to transmit data, active signal occupies a small fraction of the total transmission time and hence the average power requirement is very low [9].

Thus the problem of heat generation and area penalty that originates from the circuitry of the intra-chip wireless interconnect systems is radically solved by the use of UWB signal transmission technique.

1.3 Research overview

The ultimate goal of this work is to develop an ultra wideband transmission technology to be used as wireless interconnect systems for the future ULSI. The design objectives for this UWB interconnect systems are as follows.

- To find an appropriate signal transmission technique which is suitable for intra-chip channel.
- To develop an energy efficient modulation technique in order to increase the data rate.
- To study the multiple access feasibility of the system in order to implement the reconfigurable interconnect structure.
- Theoretical study of the error rate performances of the proposed modulation scheme.
- To design the proposed receiver in circuit level using SPICE.

In fact, much work have been done on efficient design of integrated antenna but almost no work has been reported on the signal transmission technique, transceiver architecture and link budget analysis of wireless interconnect communication. Our thesis work is targeted to resolve these vital issues.

When the UWB pulse travels through a channel, it usually gets distorted. Usually, this distortion is partially compensated for or equalized at the receiver by way of channel estimation and some proper receiver design. However, for on-chip interconnect systems, effective channel estimation and the associated receiver design to

equalize the channel and to collect enough energy for data detection are not only difficult tasks but also require complicated receiver structure. That is why, it has been proposed, for the first time TR UWB technique for on-chip communication which is a scheme that devotes a portion of the transmitted energy for channel measurement. In the basic scheme of TR technique, pulses are transmitted in pairs, where the first pulse is unmodulated and the second one is modulated by the datum. Both pulses are distorted in the same way by the channel and hence TR receiver needs no channel estimation and allows for simplified synchronization. Moreover TR scheme eases the multiple access technique to implement reconfigurable interconnect architecture, simply by assigning unique delays to individual receiver. However, TR systems waste communication resources, i.e., power and time, to transmit reference signals. In most existing transmitted reference schemes, information is contained only in the amplitude or only in the delay of the two subsequent pulses. Therefore, potentials for a new modulation technique, where information is contained in the amplitude as well as in the delay between two subsequent pulses, is investigated in this thesis work so that two pulses represent at least two bit values. This reduces the required energy per bit at the transmitter on cost of the receiver complexity. Nevertheless, the proposed receiver structure has still low complexity.

The complete system was simulated in simulink of matlab. The simulink model enabled us to evaluate the system performance through bit-by-bit simulation. The receiver error probabilities were investigated with respect to signal to noise power ratio (SNR) at different data rates. A theoretical study of the bit error rate (BER) for proposed modulation scheme is also provided. The overall system performance has been evaluated over an entire chip size of 20 x 20 mm^2. Optimistic results from these simulations and theoretical studies take us a way forward to achieve the overall goal of implementing a software reconfigurable wireless interconnect systems for the future ULSI.

1.4 Thesis layout

This thesis comprises of seven chapters. **Chapter 1** first describes the limitations of present day IC technology which has initiated a tremendous research effort to stay on the technology roadmap for the future ULSI. It was shown that the main design constraint is the interconnect delay which requires innovative techniques to solve the problem. In this regard the advantages of wireless interconnect systems using integrated antenna is evaluated. The potentials of using UWB communication technology as the signal transmission technique for wireless interconnects are also discussed. Finally this chapter gives a detail outline of the objectives of this work.

Chapter 2 gives a detail literature review of the interconnect technology. The problems aroused due to the constant scaling down of the interconnects are described first. Some evolutionary techniques for interconnects such as use of copper metallization, low-k dielectric instead of aluminum and Si respectively, inserting repeaters in the long interconnect wire are then discussed. The rationale for introducing revolutionary techniques such as 3-D integration, optical interconnects and wireless interconnects is also given. The chapter also contains a comparative study of these recent techniques.

Chapter 3 provides an overview of the ultra wideband technology which includes generation of UWB pulses, advantages of UWB, modulation and demodulation techniques. This chapter also contains a brief description of the transmitted referencc UWB scheme.

Chapter 4 presents the complete transceiver architecture designed by the simulink of matlab. The system consists of five modules such as data generator, UWB modulator, AWGN channel, receiver and error calculation and display unit. The internal structure of each module is illustrated and the related waveshapes in different stages of the system are given.

Chapter 5 contains the results of the analysis conducted through out the research work. The error performance of the proposed PAM-PPM modulation scheme is

evaluated both analytically and through computer simulation. The chapter contains multiple access performance of this scheme as well as a comparative study with the conventional bi-phase modulation technique. Finally the total system performance was evaluated for an entire chip size of 20 x 20 mm^2.

Chapter 6 presents the circuit model of the transceiver system. Different blocks of the system such as low noise amplifier (LNA), delay unit, mixer was designed and simulated using ORCAD. The thesis is concluded in **chapter 7** by presenting summary of the overall research and along with some suggestions for future work.

CHAPTER 2

INTERCONNECTS: PRESENT AND FUTURE

2.1 Three tier Architectural hierarchy for VLSI Circuit design

It is useful at this point to briefly describe the architectural details of modern day chip design with a view to better understand the interconnect topologies used therein. The three tier architectural hierarchy of high-end microprocessor, shown in Fig. 2.1, exhibits three distinct levels of wiring hierarchy.

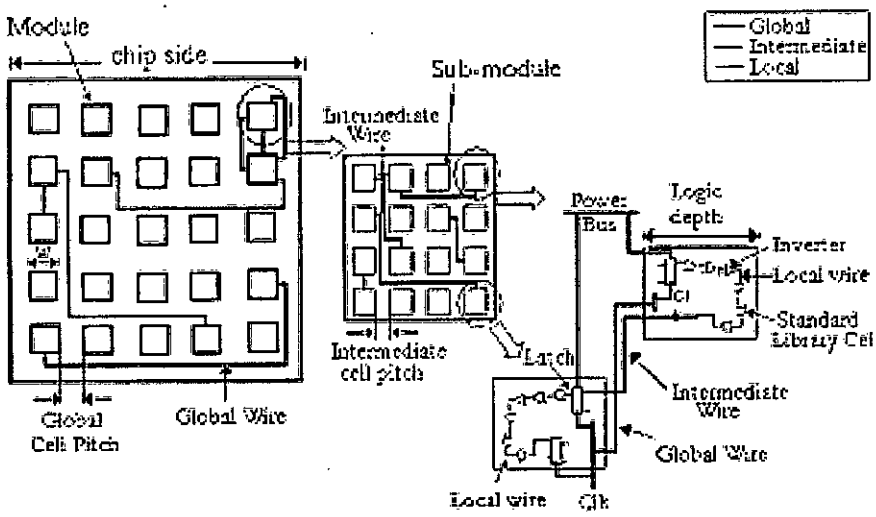


Figure 2.1: Three Tier Architectural hierarchy for VLSI circuit design

The first tier referred to as "local" comprises logic blocks built using standard cells, inverters and latches. These blocks are referred to hereafter as sub-modules. Approximately 80% of the wires on the chip begin and end within these sub-modules. The defining characteristics of these so-called "**local wires**" are that they are shorter in length and usually carry signals between various layers of logic within the sub-module. The size of a sub-module is of the order of 10 K to 50 K gates depending upon the design and layout of the microchip.

Sub-modules are used to construct modules that belong to the second tier of the architectural hierarchy. **Intermediate wires** are defined as those that interconnect multiple sub-modules laid out according to a semi-global floor plan. They are usually of lengths between that of local and global wires and are mostly used for signal communications, but may also assist in clock distribution.

Finally, modules are arranged according to a pre-defined global floor plan to construct the third and final tier entity i.e. the chip itself. **Global wires** interconnect the modules and carry signals, clock and power between them.

Typical microprocessor designs utilize a hierarchical or "reverse scaling" metallization scheme. As shown in Fig. 2.2, local interconnects are placed in the bottom layers where as global interconnects occupy the topmost layers and intermediate wires are placed in between them. The dimension of the interconnect layers increases gradually from bottom to top such that widely spaced "fat wires" are placed in uppermost layers as global interconnects.

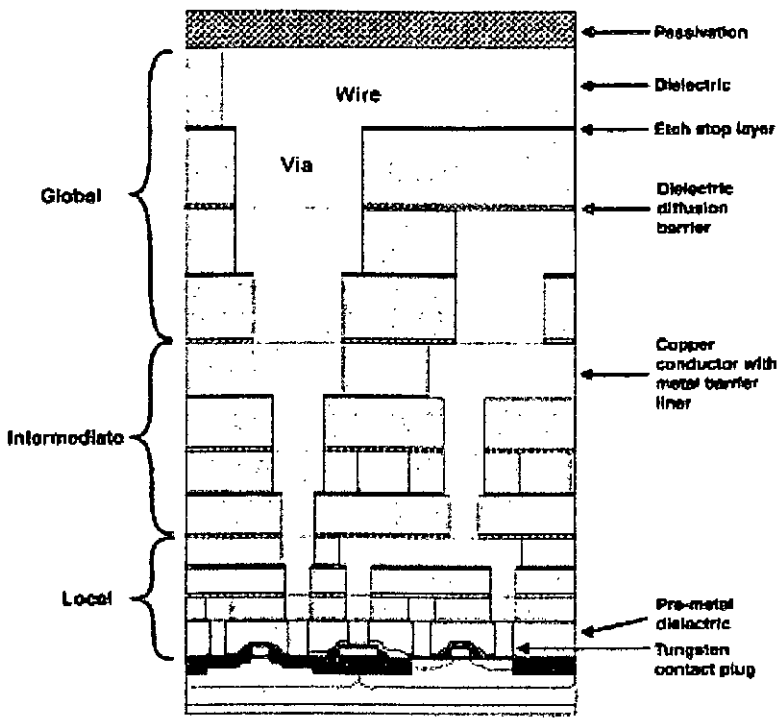


Figure 2.2: Typical cross section of a modern chip.

2.2 Evolution of Interconnect Technologies

To realize the projected integration of millions to billions of transistors on a single chip, VLSI integration is scaling down to the deep sub-micron level with an astonishing pace. Along with the transistor scaling, wire width and wire space have been scaled down together with the via size. Metal routing pitches have also been scaled down and the number of metal layers has been increased.

For classical transistor scaling, device performance improves as gate length, gate dielectric thickness, and junction depth are scaled. In contrast, scaled chip wiring (interconnect) suffers from increased resistance due to a decrease in conductor cross-sectional area and also suffer from increased capacitance for reduced spacing as well as if metal height is not reduced with conductor spacing. Thus, RC parasitics play an increasing role in overall chip performance as feature size scales down, as shown in Fig. 2.3 [10]. Therefore interconnect delay supersedes the device delay for the present day VLSI technology.

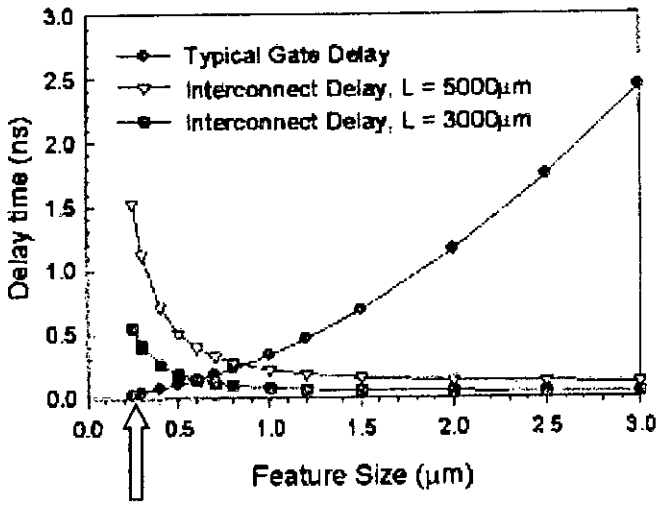


Figure2.3: Gate and interconnect delay versus feature size. Interconnect delay is shown for repeater spacing (L) of 3000 μm and 5000 μm.

A chief concern is the increasing latency or RC delay of global wiring. Since local and intermediate interconnects tend to scale in length, latency is dominated by

global interconnects connecting large functional logic blocks. Future increases in microprocessor chip size bring heightened concern, since interconnect latency is proportional to the square of length. Conventional design solutions such as the use of repeaters or reverse scaling may mitigate latency in the near term, but these approaches typically result in larger chip size and/or more levels of interconnect, leading to higher product cost. Not only that after a certain optimum repeaters, the delay tends to increase with additional repeaters.

Besides increased delay, these global wires are more prone to cross talk due to parasitic capacitance between parallel wires of increased length. Likewise, high frequency device operation introduces new bandwidth constraints on the interconnect fabric, which, due to reverse scaling laws, leads to more metal layers and increased power consumption by the metal interconnects.

Copper / Low-k materials

The semiconductor industry tried to ameliorate these delay problems by introducing copper metallization, with a resistivity about 60 percent that of aluminum, and a series of ILDs with dielectric constants down to half, or less than half, that of SiO_2.

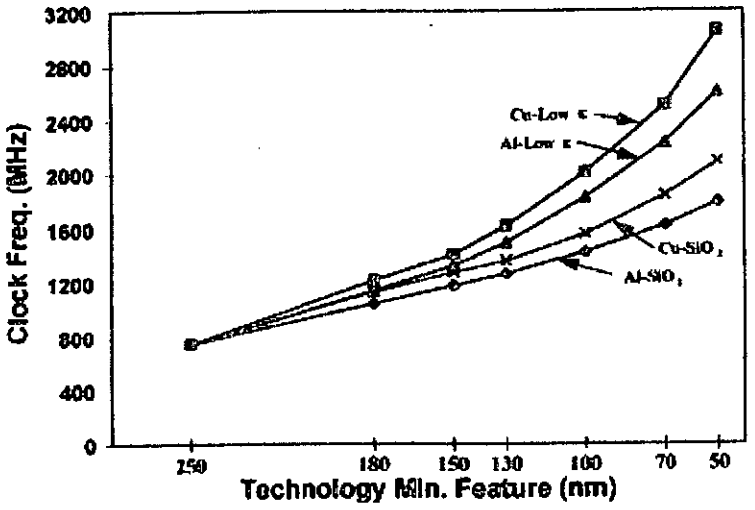


Figure 2.4: Microprocessor performance as a function of feature size and interconnect technology (Logic depth=12 gates)

Fig. 2.4 highlights the respective performance advantages of a low-k dielectric and copper metallization in a typical microprocessor implementation. Although aluminum/low-k competes well with copper/oxide, the highest performance is achieved when copper and low-k are combined.

Several companies have been working with copper metallization since the late 1980s, and the process is now quite well-defined [11]. Typically, a very thin copper seed layer is deposited by physical or chemical vapor deposition, followed by a thicker layer deposited by electroplating. Copper, however, brings some process challenges. It is difficult to plasma etch. As a group 1B element, copper has a non-negligible diffusion rate through silicon, silicon dioxide and other dielectrics. Finally, it is a potent aquatic toxin, so copper residues from integrated circuit processing must be carefully handled.

The copper etching issue has been sidestepped by the use of damascene processing. This technique involves etching trenches and vias in the underlying dielectric and blanket coating the wafer with copper, followed by a chemical mechanical polish down to the dielectric surface. This leaves only the copper that lies in the vias and trenches, effectively creating a pattern definition process.

Numerous low-organic and inorganic materials spanning a wide range of dielectric constants, from air (k=1) to fluorinated oxides (k~ 3.6) have been explored for use in interconnect systems. However, only a limited numbers have been introduced into production (predominantly with aluminum metallization) due to integration and reliability issues. Integration and reliability issues that have impeded implementation of low-dielectrics include thermally or mechanically induced cracking or adhesion loss, poor mechanical strength, moisture absorption, time-dependent behavior, chemical interactions (especially those which may occur during photolithography, etch/clean and dielectric/metal deposition), low electrical breakdown, and poor thermal conductivity.

2.3 Alternative interconnect approaches

The application of copper and low-k materials will not be sufficient to resolve all device-delay problems. Copper offers only a 40 percent improvement over aluminum in resistivity, and while this does provide a moderate improvement in microprocessor performance, its value will diminish as clock speeds increase. In addition, the TOF dependence is only as the square root of the dielectric constant, hence a reduction from the value of 4.0 (silicon dioxide) to 1.0 (theoretical limit), will only improve TOF values by 50 percent.

Therefore, in the long term, new design or technology solutions will be needed to overcome the performance limitations of conventional interconnect system. Alternative technologies for global interconnects should meet the following goals:

1) they should provide both intrachip and interchip global interconnect without any penalty in latency for going off chip(i.e., eliminate the traditional hierarchical approach)
2) They should substantially reduce the latency or delay of signal transmission, provide adequate signal bandwidth for future needs, and reduce cross coupling noise and power dissipation.

Alternative global interconnect approaches proposed thus far include:

1) Three-dimensional (3-D) integration technology
2) Optical interconnect
3) RF/Wireless interconnect

These approaches are briefly discussed and compared below.

2.3.1 3-D integration

3-D integration of active transistor layers or, as an intermediate step placement of the clock/signal and power/ground wires on opposite sides of a chip, can reduce the number and average length of two-dimensional (2-D) global wires by providing shorter "vertical" paths for connection. A 3-D approach has also been shown to reduce overall chip area when designs are interconnect-limited. Several different schemes have been proposed for implementing 3-D integration for the advanced technology nodes as shown in Fig. 2.5 [12].

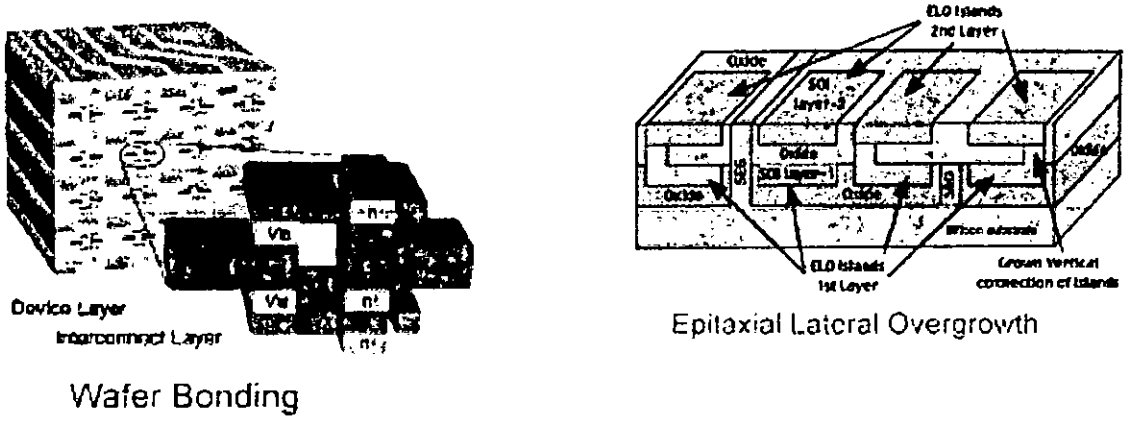


Figure 2.5: Different approaches to fabricate 3-D circuits

3-D integration also offers some attractive advantages related to system performance and enabling of new system architectures. First, it can extend the performance of high-speed transistors to technology nodes where the global wires otherwise are expected to present serious frequency limitations to advanced CMOS.

Second, for systems-on-a-chip (SOC) applications, 3-D integration may provide the means to integrate dissimilar technologies (digital, memory, analog, RF, etc.) in the same cube (offering many of the wiring delay advantages of 2-D integration) but on different active layers. For example, power hungry digital circuits could be located on the bottom layer adjacent to the heat sink and lower-power/higher-voltage

analog circuits on the top active layer. 3-D approaches could also enable integration of huge amounts of cache memory on top of a high performance microprocessor chip.

Complex and difficult challenges remain, however, including management of thermal dissipation from interior stacked active layers, the need for 3-D routing and placement tools, development of new systems architectures to exploit 3-D integration, etc. Furthermore, there are diminishing returns for adding more than three or four active layers to a 3-D chip. For this reason, including more than four active layers would provide no further savings in active chip area needed to realize a system function.

2.3.2 Optical interconnect

Optical interconnect technologies have long been considered as attractive alternatives to providing both interchip and, perhaps eventually, intrachip replacement technology for metal/dielectric global interconnects [13]. Proposed optical approaches can be grouped into **guided wave** and **free space**. Guided wave optics involves the use of waveguides to contain the optical signals within0 a board, package, or on a chip. Free-space optics utilizes diffractive optics and conventional lenses or microlens arrays to guide single or multiple parallel optical beams in free space. Fig. 2.6 shows a typical view of an optical interconnect system using optical modulator and detector units.

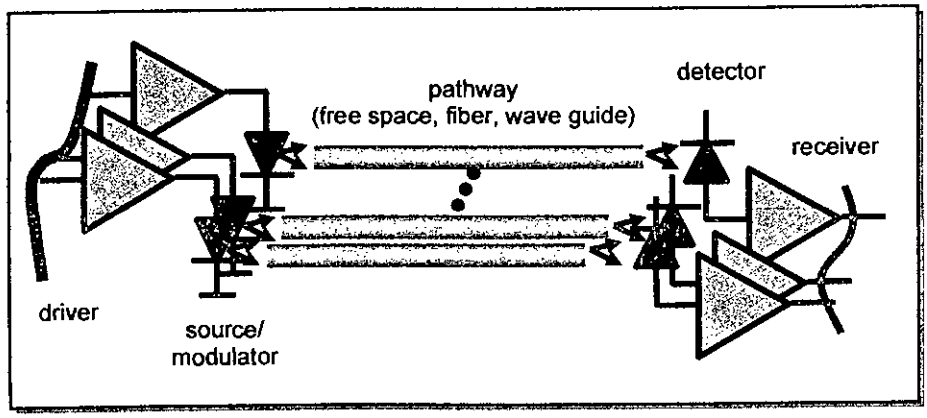


Figure 2.6: optical interconnect concept

Compared to electrical wires, optical technology offers fundamental advantages to global interconnects, given that the technology can be realized in a simple, cost effective implementation. The bandwidth of electrical interconnects is $\sim A/l^2$, where A is the cross section area of the interconnect and l is the length. Optical interconnects, however, are not bandwidth limited in this way, although they are limited by the propagation delays of optoelectronic components such as transmitters, modulators, and receivers. Further, the signal propagation velocity of electrical interconnects tends to be 10%–30% of the speed of light, c, whereas the optical propagation velocity for guided waves tends to be $\sim (1/3)c$. The signal propagation velocity for free-space optics is approximately c, with the latency again being limited only by the optoelectronic components including the transmitters or modulators and the receiver circuits.

Optical interconnects must overcome some rather difficult fundamental and technological challenges before they will find application as on-chip interconnects. The first issue, particularly for on-chip guided wave optical interconnects, is the relative size of optical components (particularly waveguides and photo-receiver circuits) required. For this reason, guided wave optical interconnects may require separate active layers in the vertical dimension with via interconnect to the functional blocks to support the required optoelectronic components. Power dissipation for receivers, and, to a lesser extent, transmitters can be prohibitively large. Other issues with optical interconnects are the technologies for fabricating III–V devices on silicon. Heteroepitaxial growth of III–V vertical-cavity surface-emitting lasers (VCSELs) on silicon CMOS circuits is a very difficult technology limited by reliability concerns.

2.3.3 RF/Wireless interconnect

Radio frequency or wireless interconnect technologies have only recently been considered as viable candidates for either on-chip or off-chip interconnects replacing metal/dielectric global wires. This new approach has become possible because of the confluence of wireless technologies for communications applications with high-frequency silicon technologies. Wireless interconnect systems can be used for both

clock and data signals. They have been demonstrated recently for clock distribution at 7.4 GHz and 15 GHz in 0.25-μm and 0.18-μm technologies respectively [5]. They have also received attention for data communication [14]. Fig. 2.7 presents the schematic diagrams of intra-chip or inter-chip wireless interconnection systems using on-chip antenna.

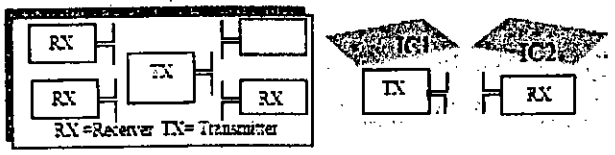


Figure 2.7: Wireless interconnect architectures for on-chip communication

A novel feature distinguishing this wireless approach is the use of code division multiple access (CDMA) and frequency division multiple access (FDMA) to obtain up to 100 channels in a 100-GHz carrier connecting multiple transmitting and receiving nodes. Using local area network (LAN) communication techniques applied to microsystems applications, this micro-LAN (M-LAN) approach will provide high-speed, low-loss intrachip clock/signal distribution among multiple block functions on a chip, or, more likely, among multiple chips in a package.

Compared to global electrical wires, RF interconnects potentially offer several advantages. First, circuits can be synchronized over much larger areas because wireless approach transmit signals three to ten compared to global wires. In addition, the bandwidth of the RF approaches, much like optical interconnects, is only limited by the bandwidths of the transmitting and receiving components, and not by the transmission medium, as is the case for global wires. Also, the crosstalk between channels should be much improved, particularly for the approach using FDMA and CDMA communication techniques. Furthermore, the signal multiplexing capability of the M-LAN approach should reduce the actual number of I/O ports going off-chip and the M-LAN communications techniques can provide new flexibility to reconfigure the interconnect system simply by changing the CDMA codes.

The approach of RF interconnects is very new for intrachip and interchip communications, although the techniques proposed are well developed for wireless communications applications. RF interconnect has to overcome some difficult challenges before becoming a viable candidate to replace global wires. First, for package applications, the RF implementation must be cost competitive with conventional interconnect systems. Further, the power dissipated by RF interconnect support circuits must be equal to or less than the power dissipated by the global interconnect wires, and the silicon area consumed by these RF circuits must only be a small fraction of the chip size.

Comparison of optical and wireless interconnects:

Though both optical and wireless interconnect schemes are simultaneously evaluated as a new technology solution for the future ULSI, the later shows a number of promising advantages.

- Optical interconnect requires conversion of electrical signal into optical signal at the transmitter side and optical signal to electrical signal at the receiver end. Optical devices are fabricated using III – V group which are not compatible with existing Si technology and hence costly to implement. On the other hand wireless interconnects provide completely CMOS compatible architecture.

- The relative size of optical components (particularly waveguides and photo-receiver circuits) compared to chip circuitry is a critical design constraint. That is why, optical interconnects may require separate active layers in the vertical dimension with via interconnect to the functional blocks to support the required optoelectronic components. To the contrary, no special guided wave mechanism is required for on-chip wireless interconnect. Hence it reduces the electronic overhead on the existing circuit components.

CHAPTER 3

ULTRA WIDEBAND COMMUNICATIONS

In our thesis, we propose a transceiver architecture to be used as wireless interconnect system by ultra wideband (UWB) technology. So, it is worthwhile at this point to describe the transmission technique of UWB communication.

3.1 Preliminaries

3.1.1 UWB Definition

UWB technology is generally defined as any wireless transmission scheme where the fractional bandwidth is greater than 0.25 or occupies 1.5 GHz or more of spectrum. (the fractional bandwidth is defined as B/f_c, where $B=f_H - f_L$ denotes the -10 dB bandwidth and center frequency $f_c = (f_H + f_L) / 2$ with f_H being the upper frequency of the -10 dB emission point, and f_L the lower frequency of the -10 dB emission point as depicted in Fig. 3.1).

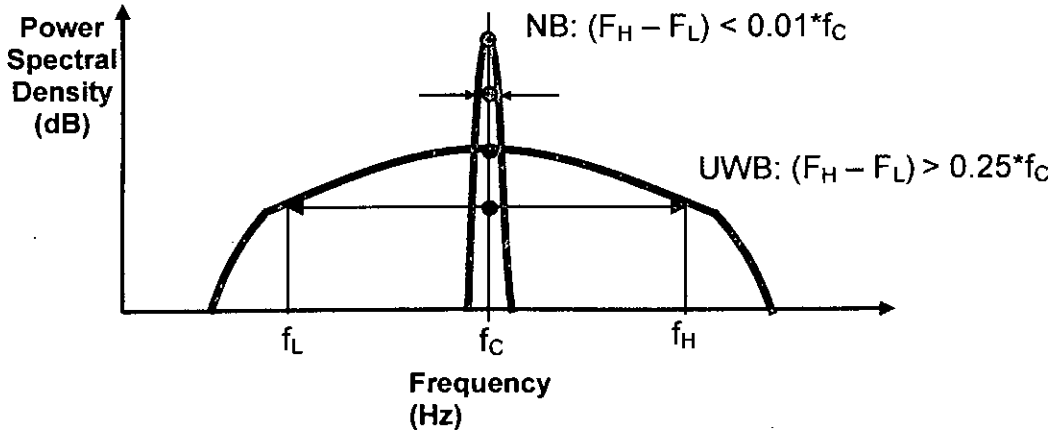


Figure 3.1 Comparison of fractional bandwidth of narrowband and wideband

UWB systems transmit and receive an extremely short duration burst of radio frequency (RF) energy – typically a few tens of picoseconds (trillionths of a second) to a few nanoseconds (billionths of a second) in duration. These bursts represent from one to only a few cycles of an RF carrier wave. The resultant waveforms are extremely broadband, so much so that it is often difficult to determine an actual RF center frequency – thus, the term "carrier-free".

3.1.2 UWB advantages

Since UWB waveforms are of such short time duration, they have some rather unique properties that have long been appreciated by the radar and communications communities.

- Enhanced capability to penetrate through the wall.
- Ultra high precision ranging at the centimeter level.
- Potential for high data rates along with a commensurate increase in user capacity.
- Potentially small size and processing power.

This ultra wideband signaling scheme is particularly attractive for wireless interconnect systems for several reasons. **First**, it creates lees electrical overhead on the existing circuitry of the chip because of its simplified transceiver architecture. UWB systems can be made nearly "all digital", with minimal RF and microwave electronics. Moreover on chip antenna can be effectively utilized to generate UWB pulse thus avoiding expensive and power hungry analog components. **Second,** to achieve a high data rate with low BER using conventional data transmission technique, one needs a substantial amount of transmitted power. Large transmitted power results in increased power consumption, which generates extra heat in the chip. Since UWB systems use ultra short pulses to transmit data, active signal occupies a small fraction of the total transmission time and hence the average power requirement is very low.

3.1.3 UWB signaling and pulse shapes

Generally adopted pulse shapes for UWB communications include the Gaussian pulse, the Gaussian monocycle (first derivative of Gaussian pulse), and the second derivative of the Gaussian pulse, as depicted in Fig. 3.2, along with their Fourier transforms.

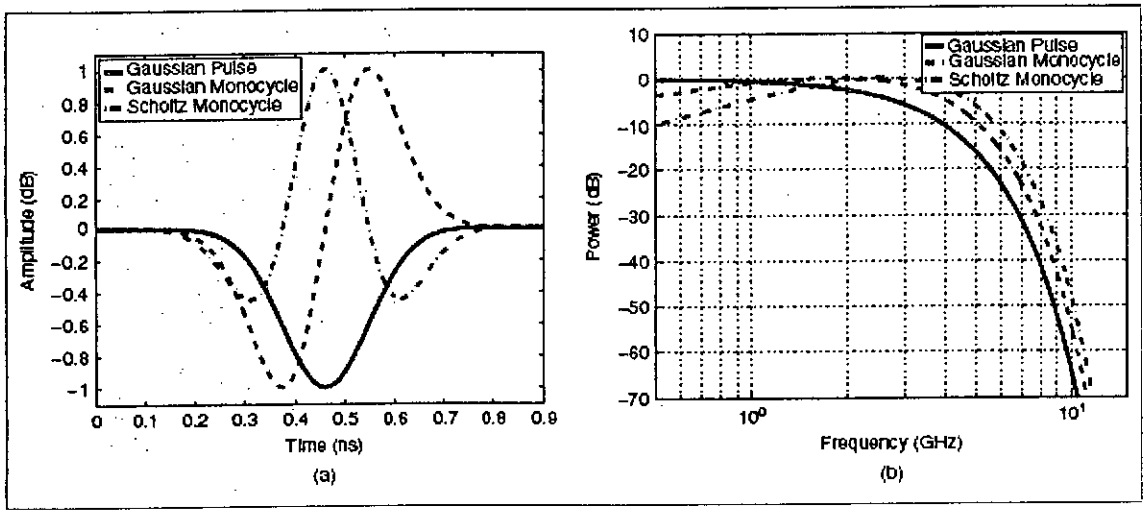


Figure3.2 (a) Generally adopted pulse shapes in UWB communication (b) Fourier transform of the pulse shapes

The reason behind the popularity of these pulses is twofold:

1) Gaussian pulses come with the smallest possible time-bandwidth product of 0.5, which maximizes range-rate resolution
2) The Gaussian pulses are readily available from the antenna pattern.

The Gaussian pulse often used to model UWB signal can be represented by

$$p(t) = Ae^{\frac{(t-\mu)^2}{2\sigma^2}} \tag{3.1}$$

where:

A is the pulse amplitude (volts)

t is time (seconds)

σ is the standard deviation of the Gaussian pulse (seconds)

μ is the mean value of the Gaussian pulse (seconds)

And the pulse width of the Gaussian pulse is typically defined as:

$$\tau = 2\pi.\sigma \text{ (sec)} \tag{3.2}$$

3.2 UWB pulse generator

Ultra-short pulse generations- usually in the range of sub-nanoseconds is one of the main issues in UWB communications systems. Several techniques are available to generate UWB pulses, among which two techniques are very promising and have got wide acceptance.

3.2.1 Step-recovery diode (SRD) approach

To date, SRD is the most common source for generating UWB pulses [15]. A typical circuit that can be employed to generate UWB pulses is shown in Fig. 3.3.

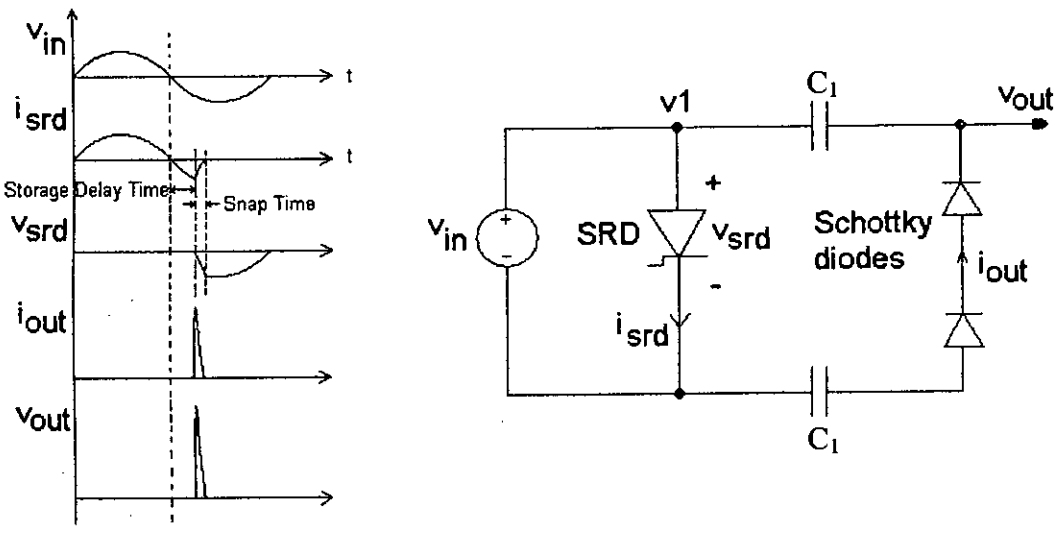


Figure 3.3: UWB pulse generator circuit using SRD

An SRD acts as a charge controlled switch using a P-I-N junction with faster switching characteristics than a typical p-n junction. A stored charge is created in the junction as a result of the minority carriers inserted during the forward bias state, where a recombination time (or carrier lifetime) must occur. The junction impedance is abruptly dependent on the stored charge, which has the capability to lead to fast rise time pulses. Explicitly, if a forward biased SRD is suddenly reversed biased, the diode appears to have a low impedance until the charge within the junction is depleted. Then, the diode snaps back into a high impedance state, essentially stopping the reverse current of the SRD. This impedance transition, along with the current within the SRD prior to cutoff, causes a voltage spike. The amount of time for this transition to occur is often referred to as "snap" time. The typical snap time ranges from 30 to 250 ps, allowing SRDs to generate pulse widths on the order of picoseconds.

The remaining circuitry is designed to shape the pulse and reduce the amount of ringing. The series Schottky diode accomplishes this task by removing any negative ringing, essentially acting as a half-wave rectifier. Any voltage below the forward voltage of approximately 0.6 volts in the input waveform causes the diode to be reversed biased, which effectively disables the output until the input reaches a positive voltage state. The series blocking capacitor (C_1) eliminates the DC offset in the ringing, which causes a small amount of positive and negative ringing to be present.

3.2.2 Pulse generation using transmitting antenna

It is the method of pulse generation in which there are no actual pulse generation circuits. This means a baseband signal is applied directly to the antenna. The baseband signal gets converted to an impulse when it's radiated [16]. Consequently, it does not need to have a pulse generator as the conventional architecture. Additionally, since the baseband signal is applied directly to an antenna, the analog amplifier (i.e. power amplifier) is not necessary. Therefore, power consumption of the transmitter is substantially reduced.

The impulse radiation principle

If a baseband signal is applied directly to a monopole antenna or a dipole antenna, an impulse will be radiated. This principle can he explained using a dipole antenna. When the frequency characteristic of the dipole antenna is high enough (a short dipole antenna), the current flow in the dipole antenna is proportional to the derivative of a baseband signal. Therefore, if the baseband signal is applied directly to the short dipole antenna, the current of Gaussian pulse will flow into the antenna. The electric field is given by

$$E_\theta = \frac{ILe^{-jkR}}{j\omega 4\pi\varepsilon}\left(\frac{1}{R^3} + \frac{jk}{R^2} - \frac{k^2}{R}\right)\sin\theta$$

where R is the distance of the antenna, L is the length of the antenna and I is the current of the antenna. When it is far from the dipole antenna, the electric field is given by

$$|E_\theta| = -\frac{ILe^{-jkR}}{j\omega 4\pi\varepsilon}\frac{k^2}{R} = \frac{j\omega\mu}{4\pi R}ILe^{-jkR}$$

Therefore the electric field that is radiated from the dipole antenna is the derivative of the current that flows in the dipole antenna. In other words, the electric field that is the second order derivatives of the baseband signal is radiated. Fig. 3.4 shows the waveform of input voltage, the transmitting antenna current and the radiated electric field from the dipole antenna.

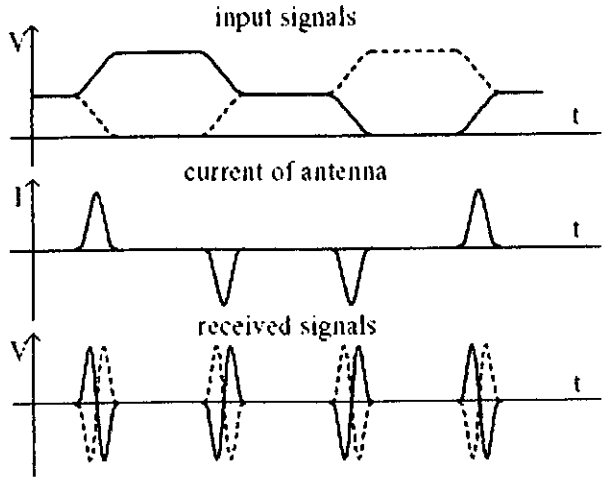
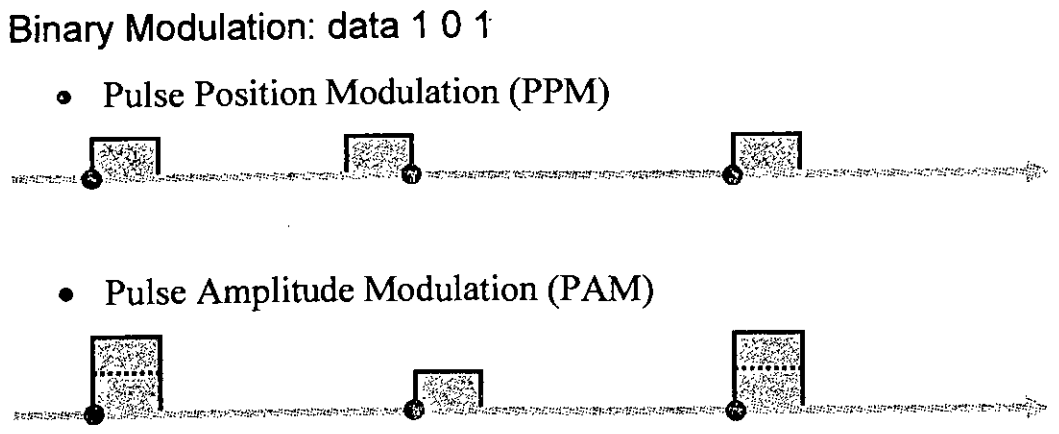


Figure 3.4: Impulse radiation from the dipole antenna

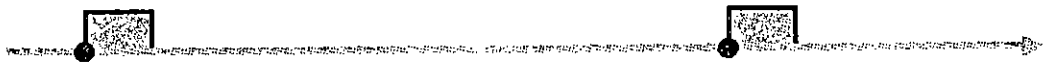
3.3 Modulation types

Although numerous modulation techniques are used with impulse-radio UWB, three common schemes are often found in research papers and journals. On-Off Keying (OOK), Bi-Phase Modulation (BPM), and Binary Pulse Position Modulation (Binary PPM) are popular UWB modulation techniques due to their simplicity and flexibility towards low duty cycle pulsed communication systems.

The basic techniques of signal transmission under different modulation schemes are outlined in Fig. 3.5



- On Off Keying (OOK)



- Bi-Phase Modulation (BPM)

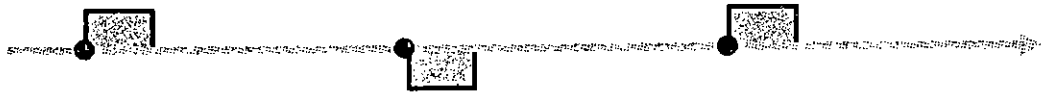


Figure 3.5: common UWB modulation techniques

3.2.1 OOK

OOK, or otherwise known as unipolar signaling in the analog baseband world, is a simple pulse modulation technique where a pulse is transmitted to represent a binary "1", while no pulse is transmitted for a binary "0", as depicted in Fig 3.5.

One obvious advantage of using OOK is the simplicity of the physical implementation, as one pulse generator is necessary, as opposed to two in biphase modulation. A single RF switch can control the transmitted pulses by switching on for a "1" data bit and off for a "0" data bit. This effortless transmitter configuration makes OOK popular for less complex UWB systems. Although OOK has a very straightforward implementation, there are numerous system drawbacks. In either a hardware or software based receiver design, synchronization can be easily lost if the data contains a steady stream of "0's." Also, the BER performance of OOK is worse than that of biphase modulation due to the smaller symbol separation for equal symbol energy.

3.3.2 BPM

In generic pulse modulation terms, pulse amplitude modulation (PAM) transmits data by varying the amplitude of each pulse based on binary data. The most common form of PAM in UWB communications is 2-PAM, or biphase modulation

(BPM), where the polarity of a pulse is modulated. In this situation, a positive pulse is transmitted for a "1" and a negative pulse is transmitted for a "0".

One advantage of biphase modulation is its improvement over OOK in BER performance. Another benefit of biphase modulation is its ability to eliminate spectral lines due to the change in pulse polarity. This aspect minimizes the amount of interference with conventional radio systems. A decrease in the overall transmitted power could also be attained, making biphase modulation a popular technique in UWB systems when energy efficiency is a priority. A disadvantage of biphase modulation is that its physical implementation is more complex. It has two pulse generators, one of them having polarity opposite to that of the other, whereas only one pulse generator is needed in OOK. This presents a problem when attempting to transmit a stream of pulses, as the time between pulses can become non-periodic if the pulse generators are not triggered in a timely fashion. Despite these issues, biphase modulation is a very efficient way to transmit UWB pulses.

3.2.3 Binary PPM

The last popular UWB modulation scheme to be discussed is PPM, which is a technique where the timing of each pulse is altered to transmit data instead of varying the amplitude. The simplest form of PPM is binary PPM, where a pulse in a uniformly spaced pulse train represents a "0" and a pulse offset in time from the pulse train represents a "1." Conceptually, the binary PPM technique is shown in Figure 3.5.

The most advantageous feature of PPM is the orthogonal signaling present in its data. Each of the pulses in time is independent of one another, meaning the time during the symbol period can be broken up to look for each pulse within a specified time slot. In the case of M-ary modulation schemes, PPM provides better error performance than PAM does and the former has also the advantage of permitting non-coherent reception. One of the disadvantages of PPM is its higher BER performance. Another apparent drawback of PPM is its susceptibility to intersymbol interference, as multiple positions are required to transmit at a higher data rate. PPM must lower the

transmitted pulse rate to account for this effect. Therefore, there is a data rate limitation when using M-ary PPM in impulse-radio UWB applications. Even when the intersymbol interference is reduced at the transmitter by decreasing the pulse rate, multipath are more likely to overlap with the next data pulse, causing bit errors at the receiver if the reflections are strong. These types of problem lead to a more complex receiver design, which hampers the use of PPM.

In addition to these basic modulation techniques, M-ary PPM, M-ary PAM and bi-orthogonal signaling by combining orthogonal PPM with BPM are also possible that results in increased data rate maintaining the same bandwidth (Fig. 3.6)

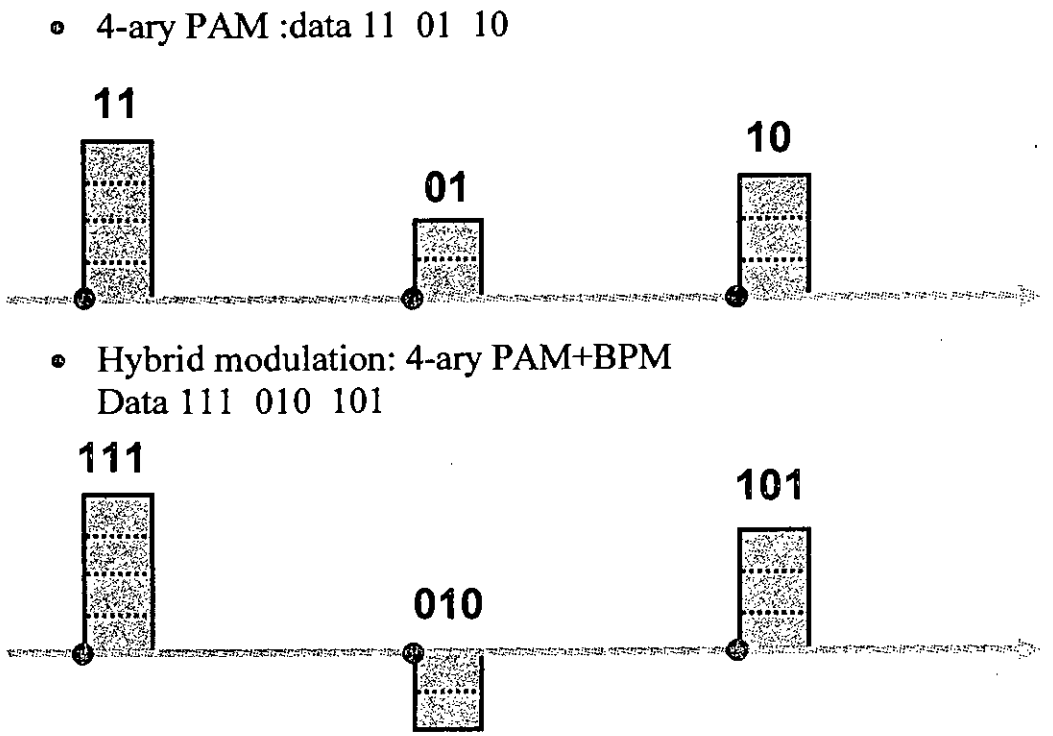


Figure 3.6: M-ary and Hybrid modulation techniques for UWB

For this thesis, hybrid modulation(PAM-PPM) technique has been used.

3.3 Demodulation technique

The way the receiver recovers its correct information from the received signal, is conventionally termed as demodulation technique. The received signal is a superposition of the transmitted signal and the additive white gaussian noise (AWGN) from the communication channel. A simplified principle of demodulation technique is illustrated in Fig. 3.7.

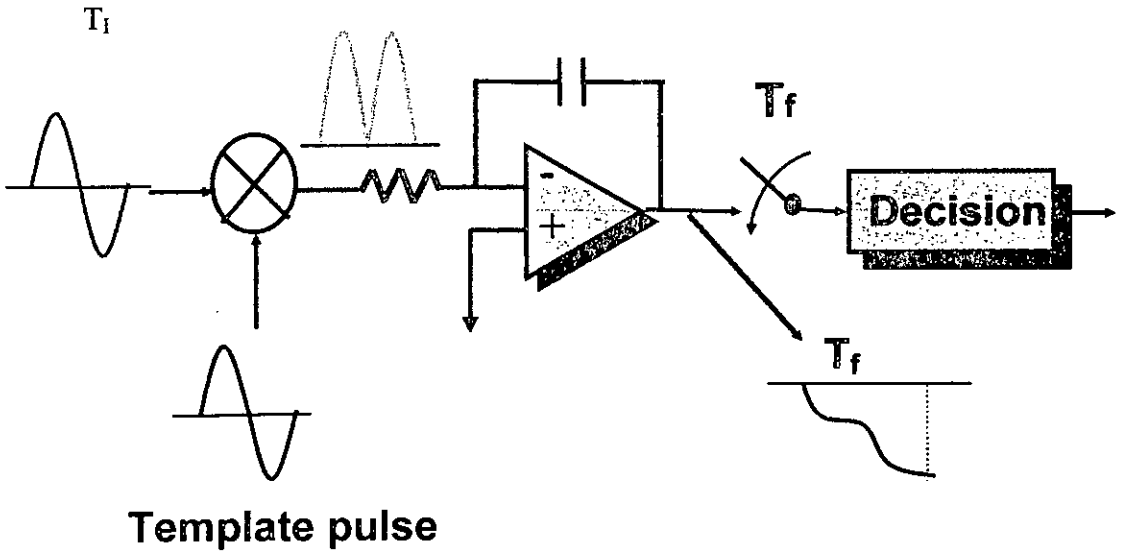


Figure 3.7: Basic correlator architecture for signal demodulation

As shown in the above figure, the receiver demodulation functionality is based on the correlation receiver which implies coherent detection of the signal. This means that a template signal is to be correlated with the received signal in order to derive the information from the incoming signal. A general correlator is simply a multiplier circuit (mixer) followed by an integration circuit. The output of the integrator is fed to a decision device that monitors the output of the integrator and performs the decision for the receiving bit.

3.4 Ultra wideband transmitted reference system

When a UWB pulse travels through the channel, it usually gets distorted, which leads to the reception of replicas of the pulse with different delays, amplitudes, phases or even different shapes. Usually, distortion is partially compensated for or equalized at the receiver by way of channel estimation and some proper receiver design. However, for highly dispersive channels such as the ones created by UWB radios, effective channel estimation and the associated receiver design to equalize the channel and to collect enough energy for data detection is difficult. Therefore, a radio design philosophy called transmitted-reference (TR) was proposed for UWB applications [17].

One of the low-complexity forms of TR system transmits a pair of pulses in each frame. The first one is unmodulated and used to provide the pulse response function of the multipath channel to the demodulator, while the second one is data-modulated. Fig. 3.8 illustrates the pulse generation scheme of TR system.

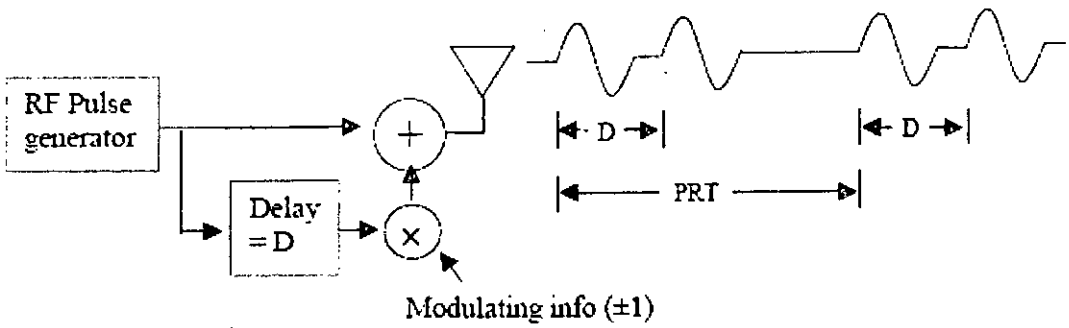


Figure 3.8: Scheme for generating TR UWB pulse

At the receiver side, a simple delay line and a cross-correlator is used to demodulate the data symbols. The advantage of a TR system is its ease of implementation because channel estimation is not required. However, the most significant drawback is the noise-cross-noise signal that appears at the correlator output, which severely degrades the performance at low pulse SNR.

Generally, TR systems waste communication resources, i.e., power and time, to transmit reference signals. In most existing transmitted reference schemes, information is contained only in the amplitude or only in the delay of the two

subsequent pulses.

Therefore, potentials for a new modulation technique, where information is contained in the amplitude as well as in the delay between two subsequent pulses, is investigated in this thesis so that two pulses represent at least two bit values. This reduces the required energy per bit at the transmitter on cost of the receiver complexity. Nevertheless, the proposed receiver structure still retains low circuit complexity.

CHAPTER 4

TRANSCEIVER ARCHITECTURE

Focusing on the intra-chip wireless interconnect systems using ultra wideband communication technology, a complete transceiver architecture has been designed using simulink of matlab. The system not only proves the validity of signal transmission scheme using computer simulation but also provides performance evaluation of the system through bit-by-bit simulation of the transceiver. Fig. 4.1 illustrates the transceiver model of the system designed with simulink.

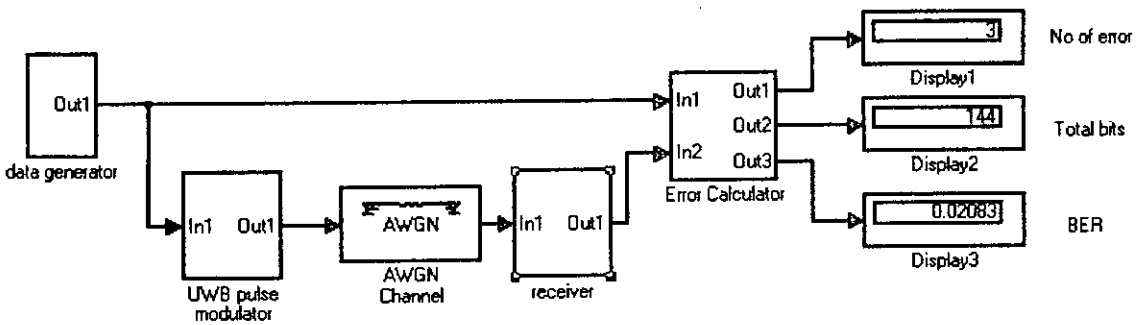


Figure 4.1: Block diagram of the transceiver model

The complete system comprises of five distinct modules such as

- Data generator
- UWB pulse modulator
- AWGN channel
- UWB receiver
- Error calculation and display unit

Before going though the details of each block, the data transmission technique of the proposed model is described first.

4.1 Data transmission technique

As mentioned in the previous chapter, in the proposed transmitted reference scheme, information is contained both in the phase and the delay of the two subsequent pulses. The transmit signal s(t) is given by,

$$s(t) = p(t) + s_1 p\left(t - T_I - \frac{|s_2 - s_1|}{2} T_D \right) \tag{4.1}$$

Where, p(t) denotes the UWB pulse form (Gaussian monocycle), s_1, $s_2 \in \{ -1; 1\}$ are the bit values, T_I and T_D are the bit-independent and bit-dependent delays of the second pulse. With this scheme 4 different transmit signals can be described as shown in fig 4.2, each representing 2 bit values.

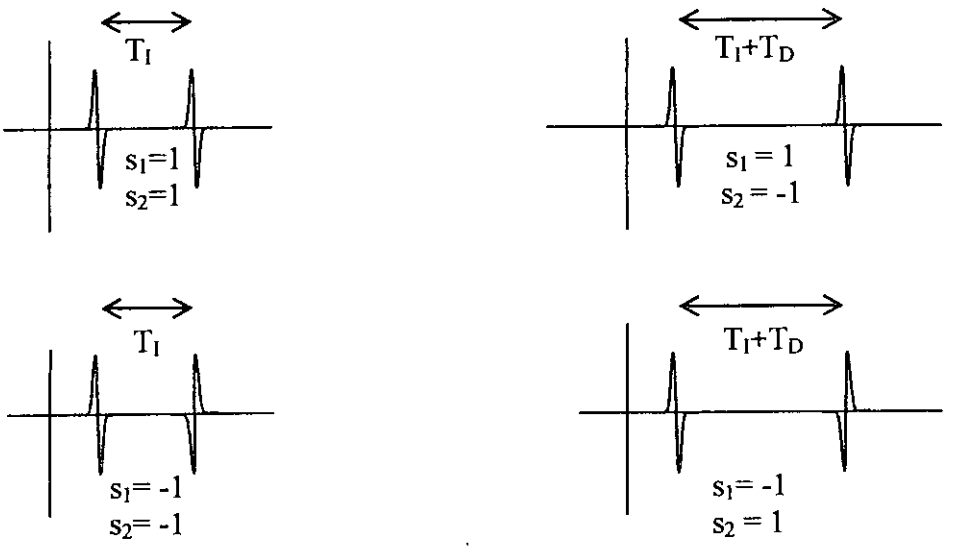


Figure 4.2: Possible pulse constellations for PAM-PPM scheme

At the receiver side a simple structure has been used which consists of two correlators with two different delays $T_1 = T_I$ and $T_2 = T_I + T_D$ as shown in Fig. 4.3. It has been assumed that the delays are larger than the pulse duration, i.e., $T_1 > T_p$ and $T_2 > T_p$. Depending on the transmit signal the output signal of one correlator is the correlation of the reference signal with the information signal while the output signal of the other correlator is the correlation of the reference signal with noise.

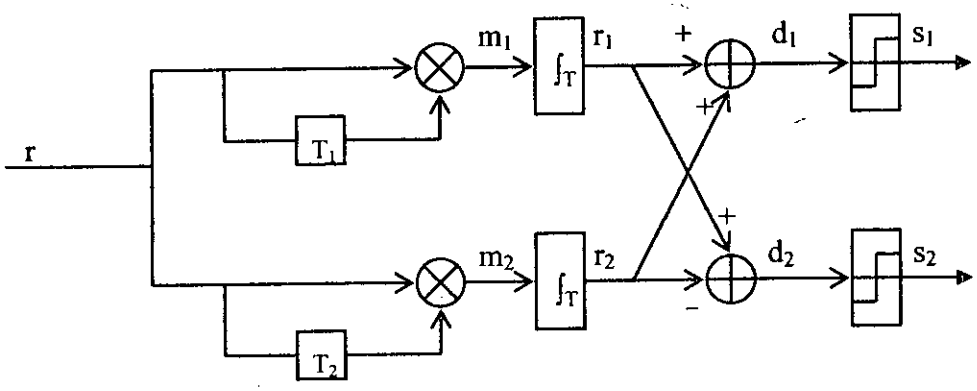


Figure 4.3: Simple receiver architecture for PAM-PPM system

The output signal r_1 and r_2 of the correlators are fed into two adders. Behind the adders the transmit signal is estimated as

$$s_1 = \begin{cases} -1 & \text{if } d_1 = r_1 + r_2 < 0 \\ 1 & \text{otherwise} \end{cases} \qquad (4.2)$$

$$s_2 = \begin{cases} -1 & \text{if } d_2 = r_1 - r_2 < 0 \\ 1 & \text{Otherwise} \end{cases}$$

4.2 Data generator

A random integer generator block has been used to generate the data sequence required for transmission and reception purpose. The block generates uniformly distributed random integers in the range [0, M-1], where M is the M-ary number defined

in the dialog box. Since the transmission scheme transmits two bits of data in each time period, the value of M has been selected as 4. The rate of data transmission can be specified by the sample time parameter of the block. A different sequence of random integers can be generated by varying the initial seed parameter. Fig. 4.4 shows the data generator module along with the generated data sequence.

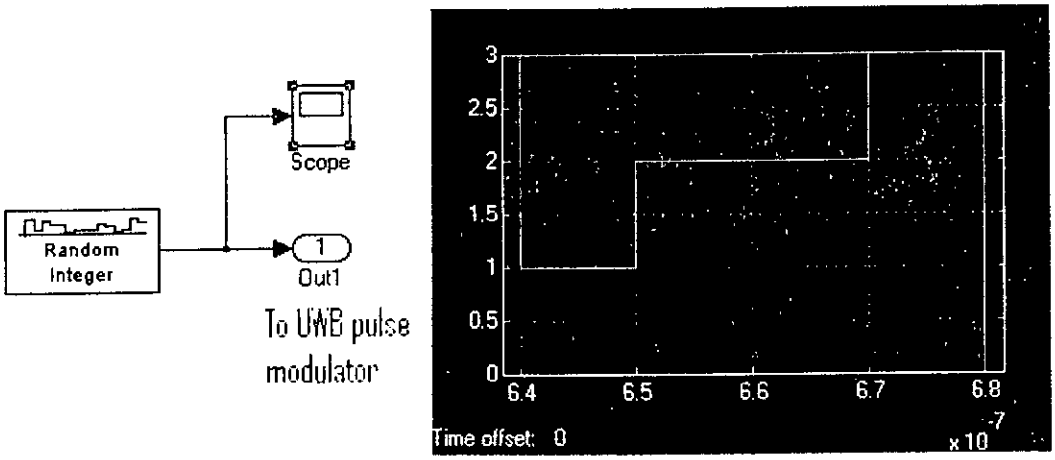


Figure 4.4: Data generator module and corresponding 4-ary random data sequence

4.3 UWB pulse modulator

The function of this module is to convert the random integers generated by the data generator to UWB pulses according to the PAM-PPM modulation scheme. Inside this module, there is a UWB pulse source which generates Gaussian monocycles continuously at a regular interval. To realize the UWB source, a structure variable called **source** was defined via matlab code which contains the data value of a Gaussian monopulse. These values were then extracted using **from workspace** block of simulink and interpolated in a periodic fashion at the interval specified by the data rate. A delayed version of the Gaussian pulse generated by **transport delay** blocks (whose phase and delay depends on the data) was added to the original pulse train.

Analyzing the pulse constellations given in figure 4.2, proper delay and associated polarity of the data pulse for each 4-ary integer number was determined and the result is summarized in table 4.1.

Table 4.1: delay and polarity for data pulse in proposed TR PAM-PPM technique

4-ary integer	bit value		delay	Polarity
	s_1	s_2		
0	-1	-1	T_1	–
1	-1	1	T_2	–
2	1	-1	T_1	+
3	1	1	T_2	+

Two **data mapper** blocks provide delay and polarity information to the multiplexer and multiplier unit respectively so that intelligence of the signal is conveyed through the pulse interval and phase of the transmitted signal. The UWB pulse modulator block along with its modulated pulses is shown in Fig. 4.5.

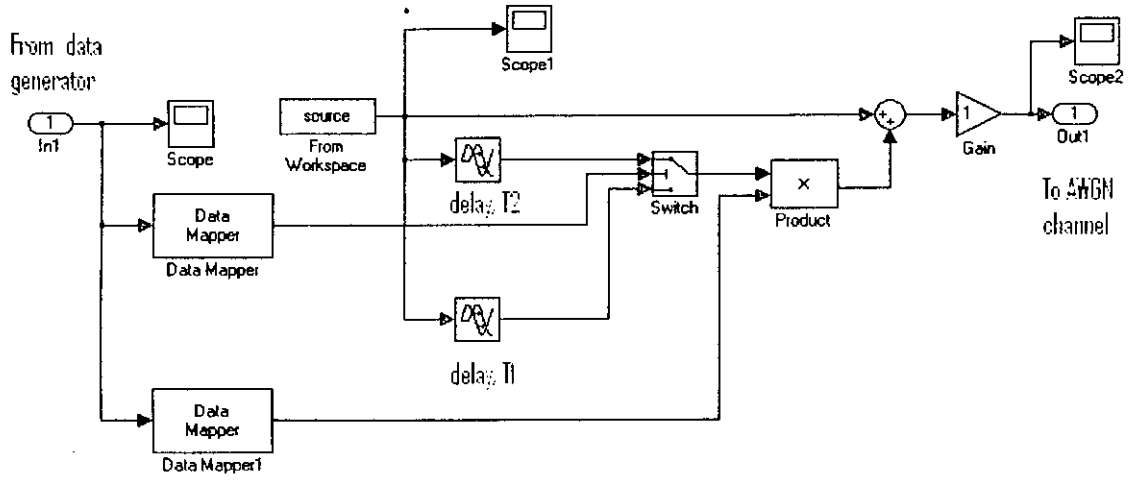


Figure 4.5(a)

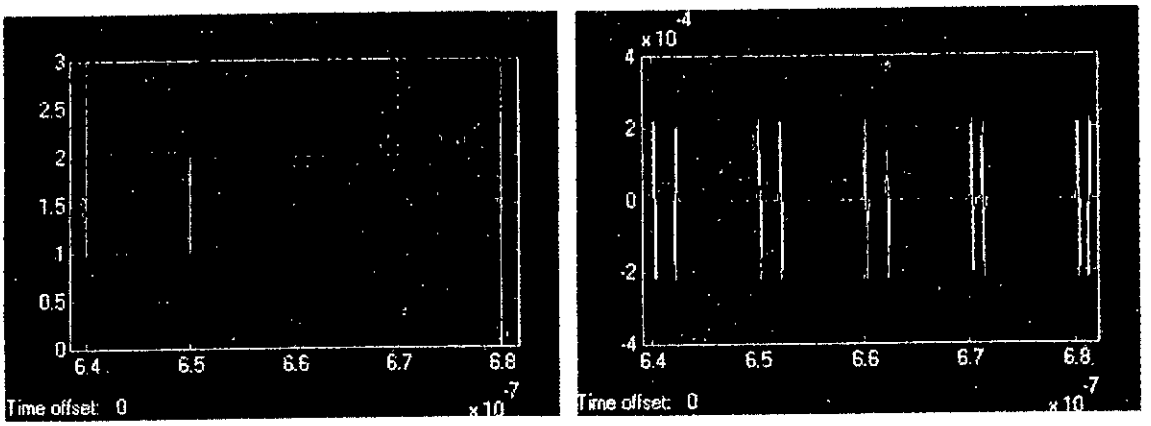


Figure 4.5(b)

Figure 4.4: (a) UWB pulse modulator (b) input data and corresponding modulated UWB signal

In the modulator block, there is an option for **gain** control of the transmitted signal. This provides the opportunity to evaluate the system performance under different SNR.

4.4 AWGN channel

The intra-chip wireless channel as shown in Fig. 4.6 can be regarded as an imperfect dielectric waveguide.

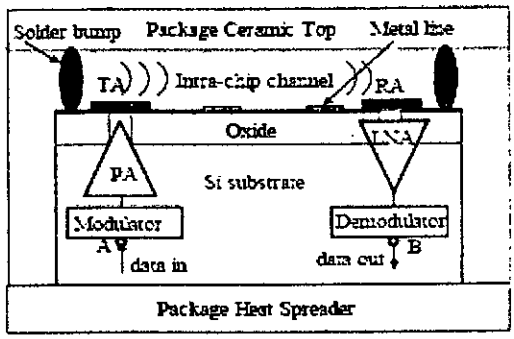


Figure 4.6: An intra-chip wireless interconnect system

The imperfectness of the dielectric waveguide is the result of the intra-chip wireless channel not being designed primarily as a wave guiding structure. In addition, the time dalay spread of the channel is negligible because of the very short distance between the transmitting and receiving antenna (on the scale of mm). Hence over such a nondispersive channel, the system performance depends on the signal to noise ratio (SNR) [18]. It is found that for intra-chip channel, the signal is corrupted by the thermal

noise and the switching noise. The thermal noise dominates the switching noise at the frequency of interest for intra-chip wireless data communication. The thermal noise power spectral density N_o is given by,

$$N_o = kT_oF = kT_o\left(\frac{T_{ant}}{T_o} + F_r\right) \tag{4.3}$$

where,

k is the Boltzman constant

T_o is the reference temperature (typically taken as 290K)

T_{ant} is the antenna temperature (taken as 330K)

F_r is the receiver noise figure (assumed as 10 dB)

In simulink, **AWGN channel block** has been used to simulate the intra-chip channel. This block adds white Gaussian noise to the input signal. Noise power was calculated using equation 4.3 and the calculated value was specified in the block using **variance from the mask** mode. The noise bandwidth B_n was determined by the relation

$$B_n = F_s = 1/T_s,$$

where,

B_n = Noise Bandwidth (Hz)

F_s = Sampling Frequency (Hz)

T_{sam} = inherited sample time of the block (s)

Fig. 4.7 illustrates the signal corruption through the AWGN channel.

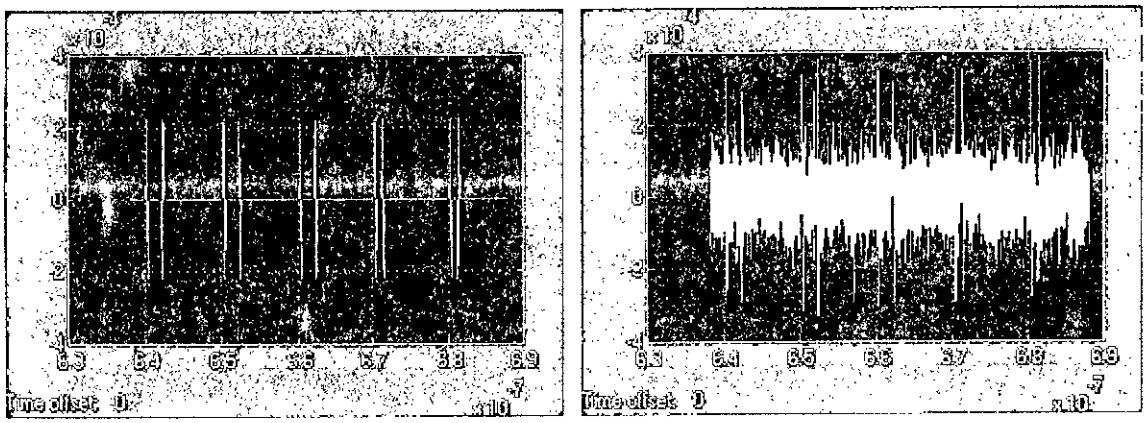


Figure 4.7: UWB pulse train before and after passing through the AWGN channel

4.5 UWB receiver

The data detection principle was explained in section 4.1. The detail diagram of the simulink receiver module is presented in Fig. 4.8.

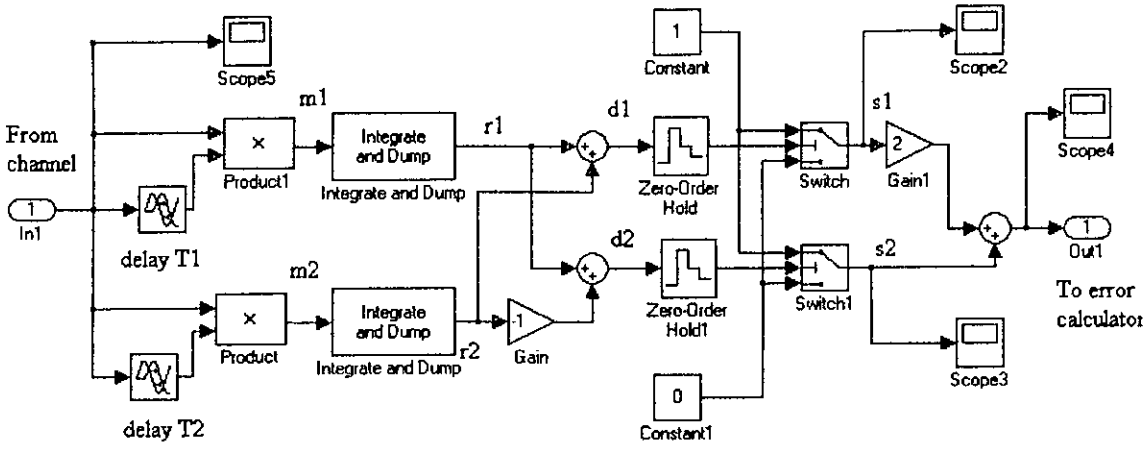


Figure 4.8: receiver module designed in simulink

Transport delay units provide the required delays of T_1 and T_2 to the received signal so that the received signal gets multiplied with its delayed versions. The output of the multiplier is integrated using an **integrate and dump block.** This block integrates the input signal in discrete time over the integration period and resets its internal state before integrating the next period. The outputs of the integrators are algebraically added, sampled, compared to the threshold values and finally combined to detect the received data. The signal states at different stages of the receiver (in compliance with Fig. 4.3) are presented in Fig. 4.9.

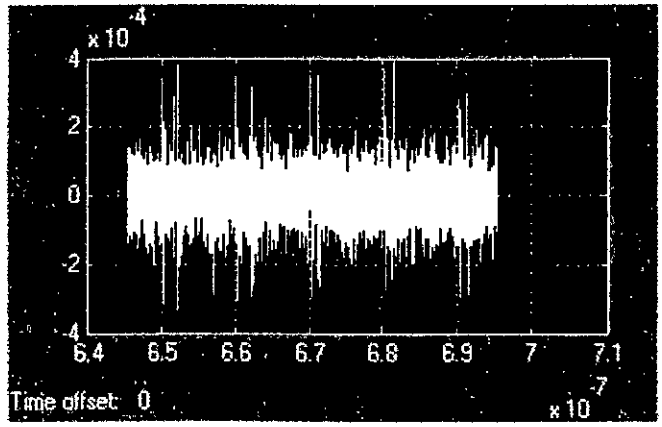
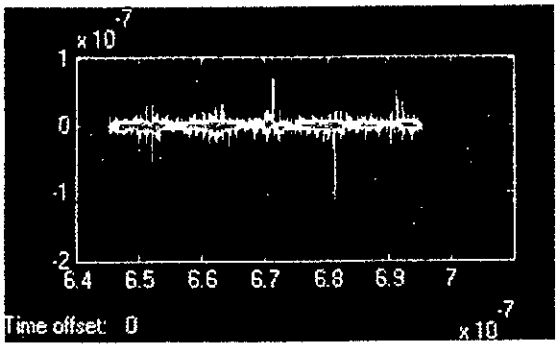
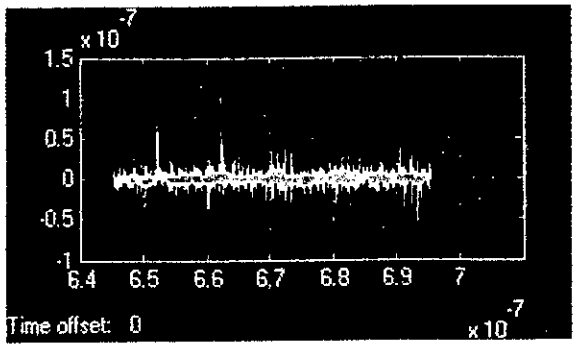
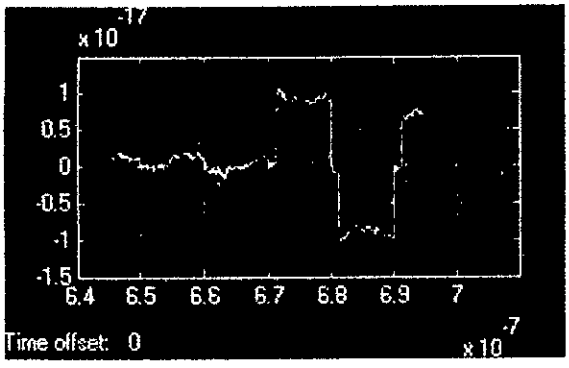


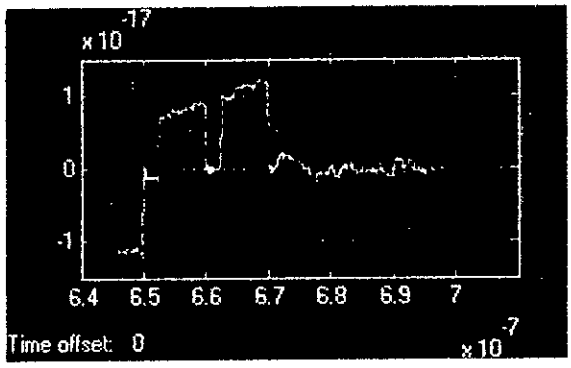
Figure 4.9(a) Received signal, r



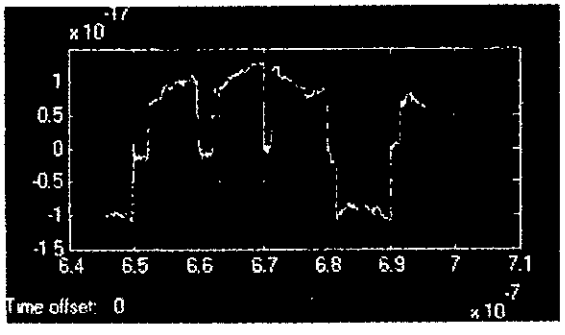


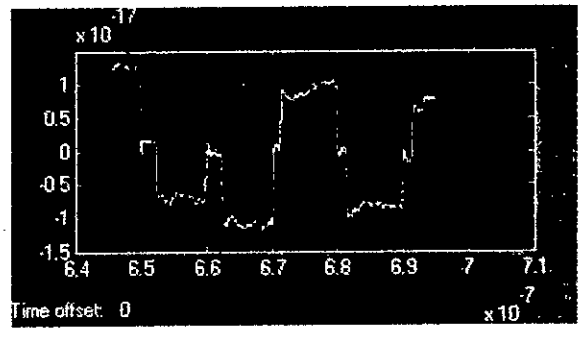
4.9(b) Outputs of the multiplier, $m1$ and m_2



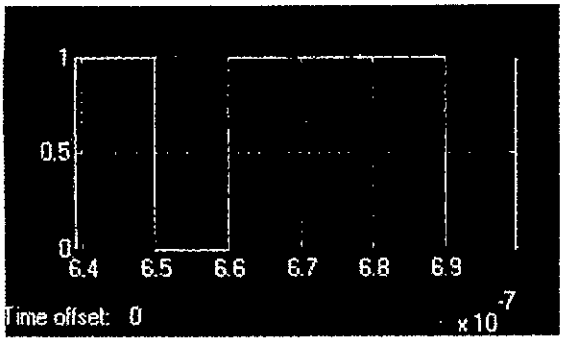


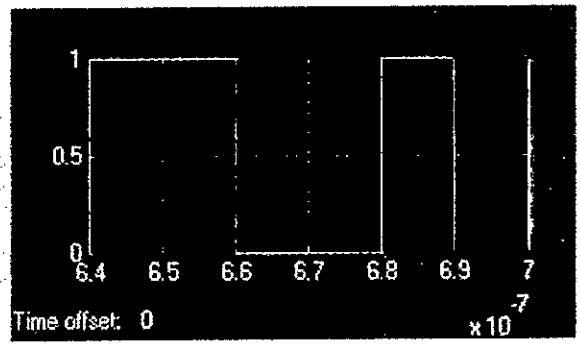
4.9(c) Outputs of the integrate and dump unit, r_1 and r_2



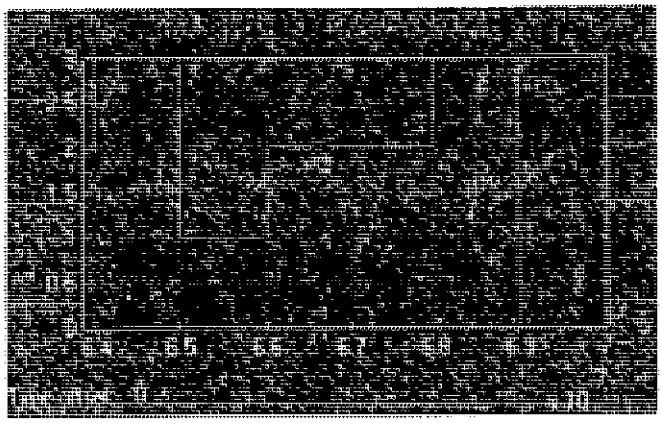


4.9(d)Outputs of the adder, d_1 and d_2





4.9(e) Outputs of the comparator, s_1 and s_2



(f) Recovered data by combining the comparator outputs

Figure 4.9: (a-f) Signal conditions at different stages of the receiver

4.6 Error calculation and display unit

The BER, or quality of the digital link, is calculated from the number of bits received in error divided by the number of bits transmitted.

BER = (Bits in Error) / (Total bits received) (4.4)

Using a test setup, this can be easily measured by means of a comparator in which the transmitted bits are matched in an XOR gate with the received bits. Fig. 4.10 shows the schematic of the setup used for such measurements.

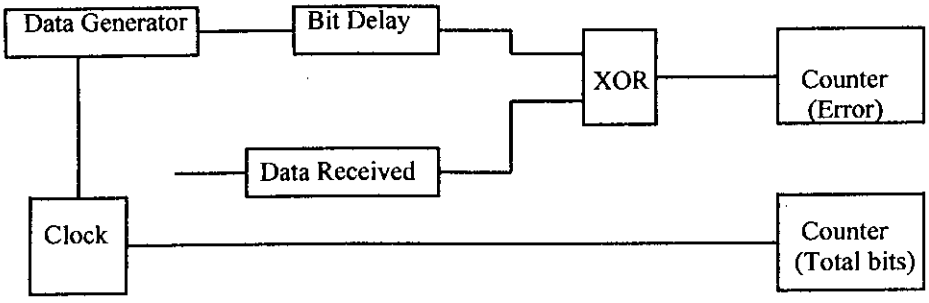


Figure4.10: Test setup for BER calculation

The transmitting and receiving circuits introduce a time delay of several bits. The transmitted bit pattern is delayed by the proper amount to match the received

pattern in time. If the bits are alike at the XOR gate input, the output is low. If they are different, the XOR output goes high, causing an event count. The event number can be set for various time periods. In general, the longer the time period, the more accurate the count. The number of bits processed should be on the order of 10/BER. This would yield an E_b/N_o uncertainty of about 0.5 dB.

The simulink module of the error calculation and display unit is shown in Fig. 4.11. The transport delay unit synchronizes the transmitted and received data by providing an appropriate lag to the transmitted data. Since we transmit and receive 4-ary data directly, the error calculator converts them to binary values for the purpose of comparison. Four **Data Mapper** blocks were used to down convert the 4-ary data to binary data where the upper two blocks gives MSB values and the lower blocks gives LSB values. The XOR operation compares the related bit values and gives high output if a mismatch appears. Two XOR outputs are combined through an OR unit and the total number of errors are recorded in a counter.

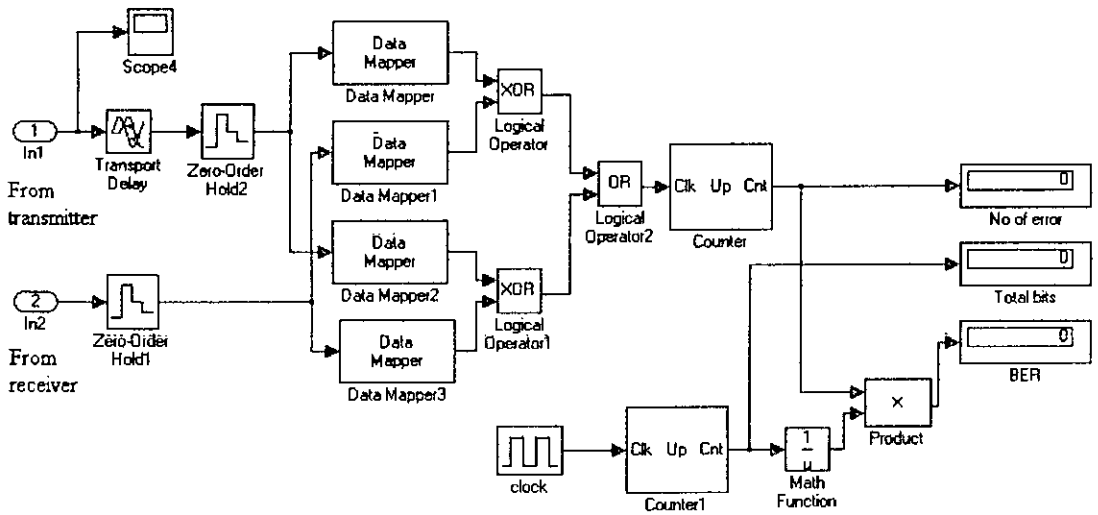


Figure 4.11: simulink module for bit-by-bit calculation of BER

For display purpose, total number of bits processed are counted by another counter. Finally, three display units showing "No. of errors", "Total bits" and "Bit Error Probability" are used to provide the error performance of the system.

4.7 Multiple access technique

Multiple access technique can be easily incorporated to our transmitted reference scheme. It is only necessary to use a different set of delays for each receiver to provide multiple access facility and this is achieved without a substantial increase in receiver complexity as opposed to conventional time hopping and DS-CDMA technique.

The multiple access scheme was designed for two transmitters and two receivers system using simulink of matlab. The architecture is shown in Fig. 4.12.

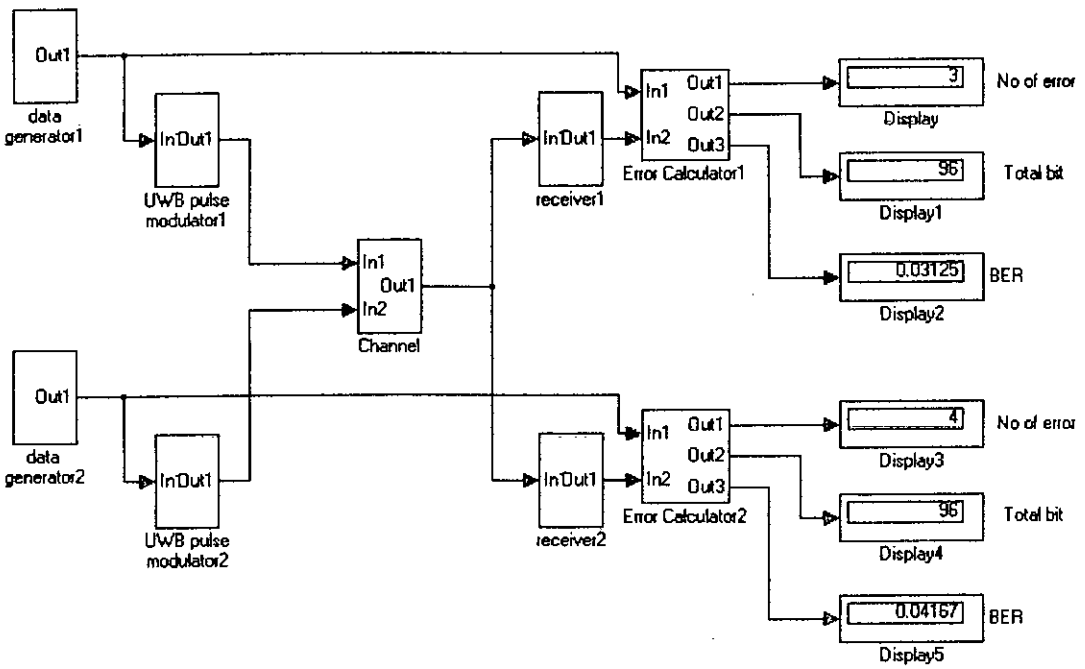
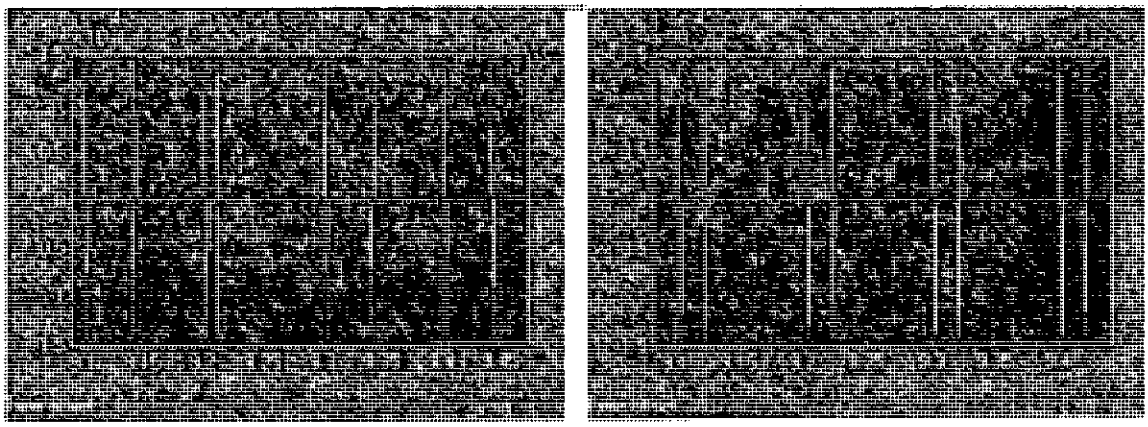


Figure 4.12: System architecture for transmitted reference multiple access scheme

In order to achieve multiple access capability, we used the delays of {1,4} and {2,3} ns in receiver 1 and receiver 2 respectively. Since each correlator has its own specific delay, the received signal is demodulated correctly to the corresponding receiver.

The pulse train of modulated data for these two receivers is shown in Fig. 4.13.



(a) *(b)*

Figure 4.13 :(a) modulated pulse train for receiver 1 where data pulses are delayed by either 1ns or 4ns (b) modulated pulse train for receiver 2 where data pulses are delayed by either 2ns or 3ns

CHAPTER 5

RECEIVER PERFORMANCE ACROSS AWGN CHANNEL

5.1 Analytical performance evaluation

In this section, the theoretical bit error rate of UWB transmitted reference PAM-PPM scheme has been investigated for the additive white Gaussian noise (AWGN) channel. The received signal r(t) can be written as,

$$r(t) = s(t) + n(t) \tag{5.1}$$

where s(t) is the signal given in (4.1) and n(t) is additive white Gaussian noise (AWGN). With $s_2' = \frac{|s_2 - s_1|}{2}$, the correlation over the time period T at the receiver with lag T_1 yields,

$$\begin{aligned} r_1 &= \int_T r(t) \cdot r(t - T_1) dt \\ &= \int_T (s(t) + n(t)) \cdot (s(t - T_1) + n(t - T_1)) dt \\ &= \int_T (p(t) + s_1 p(t - T_f - s_2' T_D) + n(t)) \cdot \\ &\quad (p(t - T_1) + s_1 p(t - T_1 - T_f - s_2' T_D) + n(t - T_1)) dt \end{aligned}$$

If the non-zero components are considered only we get,

$$\begin{aligned} r_1 = \int_T & (p(t) n(t - T_1) + s_1 p(t - T_f - s_2' T_D) p(t - T_1) \\ & + s_1 p(t - T_f - s_2' T_D) n(t - T_1) + n(t) p(t - T_1) \\ & + n(t) s_1 p(t - T_1 - T_f - s_2' T_D) + n(t) n(t - T_1)) dt \end{aligned} \tag{5.2}$$

In (5.2), $r_{1s} = \int_T s_1 p(t - T_f - s_2' T_D) p(t - T_1) dt$ represents the term which carries the actual information while the other terms are noise. If we confine on the noise terms we get,

$$r_{1n} = \int (p(t)n(t-T_1) + s_1 p(t-T_I - s_2' T_D)n(t-T_1) + n(t)p(t-T_1) + n(t)s_1 p(t-T_1-T_I-s_2' T_D) + n(t)n(t-T_1))dt \quad (5.3)$$

$$= n_1(T) + n_2(T) + n_3(T) + n_4(T) + n_5(T)$$

at the output of the first correlator.

In the same way the noise term at the output of the second correlator with lag T_2 can be written as

$$r_{2n} = \int (p(t)n(t-T_2) + s_1 p(t-T_I - s_2' T_D)n(t-T_2) + n(t)p(t-T_2) + n(t)s_1 p(t-T_2-T_I-s_2' T_D) + n(t)n(t-T_2))dt \quad (5.4)$$

$$= n_6(T) + n_7(T) + n_8(T) + n_9(T) + n_{10}(T)$$

With (5.3) and (5.4), the noise component of d_1 can be derived as

$$d_{1n} = n_1(T) + n_2(T) + n_3(T) + n_4(T) + n_5(T) + n_6(T) + n_7(T) + n_8(T) + n_9(T) + n_{10}(T) \quad (5.5)$$

In the same way the noise component of d_{2n} is given by

$$d_{2n} = n_1(T) + n_2(T) + n_3(T) + n_4(T) + n_5(T) - n_6(T) - n_7(T) - n_8(T) - n_9(T) - n_{10}(T) \quad (5.6)$$

If a signal s(t) is transmitted where the second pulse is delayed by T_1, the signal component appears only at the output of the correlator with lag T_1. As well, if the second pulse of the transmit signal is delayed by T_2, the signal component appears only at the output of the correlator with lag T_2. Therefore, the signal component of d_1 and d_2 are same for both the cases and can be expressed as $d_s = r_{1s} = d_{1s} = \int p^2(t)dt$.

The signal to noise ratio at the outputs of the adders are

$$SNR_{d1} = \frac{|d_s|^2}{\text{var}(d_{1n})} = \frac{\left|\int p^2(t)dt\right|^2}{\text{var}(d_{1n})} \quad (5.7)$$

$$SNR_{d2} = \frac{|d_s|^2}{\text{var}(d_{2n})} = \frac{\left|\int p^2(t)dt\right|^2}{\text{var}(d_{2n})} \quad (5.8)$$

5.1.1 Evaluation of SNR

The autocorrelation function of d_{1n} is

$$R_{d_{1n}}(\tau) = E\{d_{1n}(T) \times d_{1n}(T-\tau)\} - [E\{d_{1n}(T)\}]^2 \tag{5.9}$$

Since n(t) is zero mean, it can be verified that E{n(j)} = 0, j∈{1,.....,10}, and E{n(k)n(j)}= 0 except that (k ,j) = (1, 7), (2, 3), (4, 8) and (5, 10). Therefore

$$R_{d_{1n}} = \sum_{j=1}^{10} E\{n_j(T)n_j(T-\tau)\} + 2E\{n_1(T)n_7(T-\tau)\}$$
$$+ 2E\{n_2(T)n_3(T-\tau)\} + 2E\{n_4(T)n_6(T-\tau)\} + 2E\{n_5(T)n_{10}(T-\tau)\} \tag{5.10}$$

The computation of $R_{d_{1n}}$ is messy but doable. The result is listed below.

For j∈{1,...,4,6,.....9}

$$E\{n_j(T)n_j(T-\tau)\} = \int_0^T \int_{-\tau}^{T-\tau} \{r_p(u-t)r_n(u-t)\}dudt$$

The autocorrelation function of the signal pulse is equal to that of the noise, but scaled by one-half the over-all signal-to-noise power ratio, which we denote by S/N. The result is

$$E\{n_j(T)n_j(T-\tau)\} \approx \frac{1}{2}\frac{S}{N}\int_0^T \int_{-\tau}^{T-\tau} r_n^2(u-t)du\,dt \tag{5.11}$$

For j∈{5,10}

$$E\{n_j(T)n_j(T-\tau)\} \approx 2\int_0^T \int_{-\tau}^{T-\tau} r_n^2(u-t)du\,dt \tag{5.12}$$

For (k, j) = (1, 7), (4, 8)

$$E\{n_k(T)n_j(T-\tau)\} \approx s_1\frac{1}{2}\frac{S}{N}\int_0^T \int_{-\tau}^{T-\tau} r_n^2(u-t)du\,dt \text{ , if } s_2' = 0 \tag{5.13}$$

For (k, j) = (2, 3)

$$E\{n_k(T)n_j(T-\tau)\} \approx s_1\frac{1}{2}\frac{S}{N}\int_0^T \int_{-\tau}^{T-\tau} r_n^2(u-t)du\,dt \text{ , if } s_2' = 1 \tag{5.14}$$

For (k, j) = (5, 10)

$$E\{n_k(T)n_j(T-\tau)\} \approx 2\int_0^T \int_{-\tau}^{T-\tau} r_n^2(u-t)\,du\,dt \tag{5.15}$$

In the above equation, it has been assumed that, T_1 and T_2 are typically quite small when compared with T.

If a signal s(t) is transmitted where the second pulse is noninverted, i.e. $s_1 = 1$, adding the equations from (5.11) to (5.15), we get

$$R_{d_{1n}}(\tau) = 2\left(4+3\frac{S}{N}\right)\int_0^T \int_{-\tau}^{T-\tau} r_n^2(u-t)\,du\,dt$$

$$= 2(T-|\tau|)\left(4+3\frac{S}{N}\right)\int_{-\alpha}^{\alpha} r_n^2(u)\,du$$

$$= 2(T-|\tau|)\left(4+3\frac{S}{N}\right)\int_{-\alpha}^{\alpha} |S_n(f)|^2\,df \tag{5.16}$$

The notation $S_n(f)$ has been used to denote the PSD of the noise, which is equal to N_o in the band (0 – B) and in its negative frequency. Using Parseval's energy formula, we get,

$$R_{d_{1n}}(\tau) = 4(T-|\tau|)\left(4+3\frac{S}{N}\right)N_0^2 B \tag{5.17}$$

Similarly, if a signal s(t) is transmitted where the second pulse is inverted, i.e. $s_1 = -1$, we get,

$$R_{d_{1n}}(\tau) = 4(T-|\tau|)\left(4+\frac{S}{N}\right)N_0^2 B \tag{5.18}$$

Since the presented TR PAM-PPM receiver consists of two correlators with subsequent adders, it could be assumed that the error performance is the same as for TR PAM with one correlator as the receiver. Therefore, the signal-to-noise ratio SNR is given by,

$$SNR_{REC} = \frac{|d_s|^2}{\mathrm{var}(d_{1n})} + \frac{|d_s|^2}{\mathrm{var}(d_{2n})} \approx \frac{\left|\int p^2(t)dt\right|^2}{\mathrm{var}(d_{1n})} = \frac{\left(E_r/2\right)^2}{R_{d_{1n}}(0)} \tag{5.19}$$

In this expression, E_r is the total energy received over the observation interval.

5.1.2 Symbol Error Probability

Having the mean and variance of the output noise of the structure of Fig. 4.3 of chapter 4 does not necessarily allow us to compute an error probability. However, it can be argued that the noise is Gaussian [17], and so the standard results for binary antipodal signals in additive Gaussian noise can be used to develop the expression of bit error probability.

Assuming equal probability for every different transmitted bit and that proper bit synchronization has been achieved, the marginal symbol error probability is written as

$$P_e = \frac{1}{4}Q\left(\sqrt{\frac{\left(E_r/2\right)^2}{R_{d_{1n}}(0)}}\right) + \frac{1}{4}Q\left(\sqrt{\frac{\left(E_r/2\right)^2}{R_{d_{1n}}(0)}}\right) + \frac{1}{4}Q\left(\sqrt{\frac{\left(E_r/2\right)^2}{R_{d_{1n}}(0)}}\right) + \frac{1}{4}Q\left(\sqrt{\frac{\left(E_r/2\right)^2}{R_{d_{1n}}(0)}}\right) \quad (5.20)$$

where Q(x) is the Gaussian tail area above the ordinate x. Putting the values of $R_{d_{1n}}(0)$ in the above expression, we get

$$P_e = \frac{1}{2}Q\left(\sqrt{\frac{E_r^2}{16\left(4+3\frac{S}{N}\right)TBN_o^2}}\right) + \frac{1}{2}Q\left(\sqrt{\frac{E_r^2}{16\left(4+\frac{S}{N}\right)TBN_o^2}}\right)$$

$$= \frac{1}{2}Q\left(\sqrt{\frac{1}{\left(4+3\frac{S}{N}\right)TB}\frac{E_r}{4N_0}}\right) + \frac{1}{2}Q\left(\sqrt{\frac{1}{\left(4+\frac{S}{N}\right)TB}\frac{E_r}{4N_o}}\right)$$

$$= \frac{1}{2}Q\left(\sqrt{\frac{1}{\left(4+3\frac{S}{N}\right)TB}\frac{ST}{2N/B}}\right) + \frac{1}{2}Q\left(\sqrt{\frac{1}{\left(4+\frac{S}{N}\right)TB}\frac{ST}{2N/B}}\right) \quad (5.21)$$

where average power of the received signal is $S=E_r/T$ and the noise power is $N=2N_oB$. Now (5.21) can be written entirely in terms of a received signal-to-noise power ratio as

$$P_e = \frac{1}{2}Q\left(\frac{\sqrt{TB}}{2}\frac{S}{N}\left(4+3\frac{S}{N}\right)^{-1/2}\right) + \frac{1}{2}Q\left(\frac{\sqrt{TB}}{2}\frac{S}{N}\left(4+\frac{S}{N}\right)^{-1/2}\right) \quad (5.22)$$

Using the error expression given in (5.22), Fig. 5.1 plots the predicted error probabilities of TR PAM-PPM reception as a function of S/N, the received signal-to-noise power ratio. Each individual plot represents a different data rate and is characterized by a value in mega bits per second (mbps) as depicted in the legend.

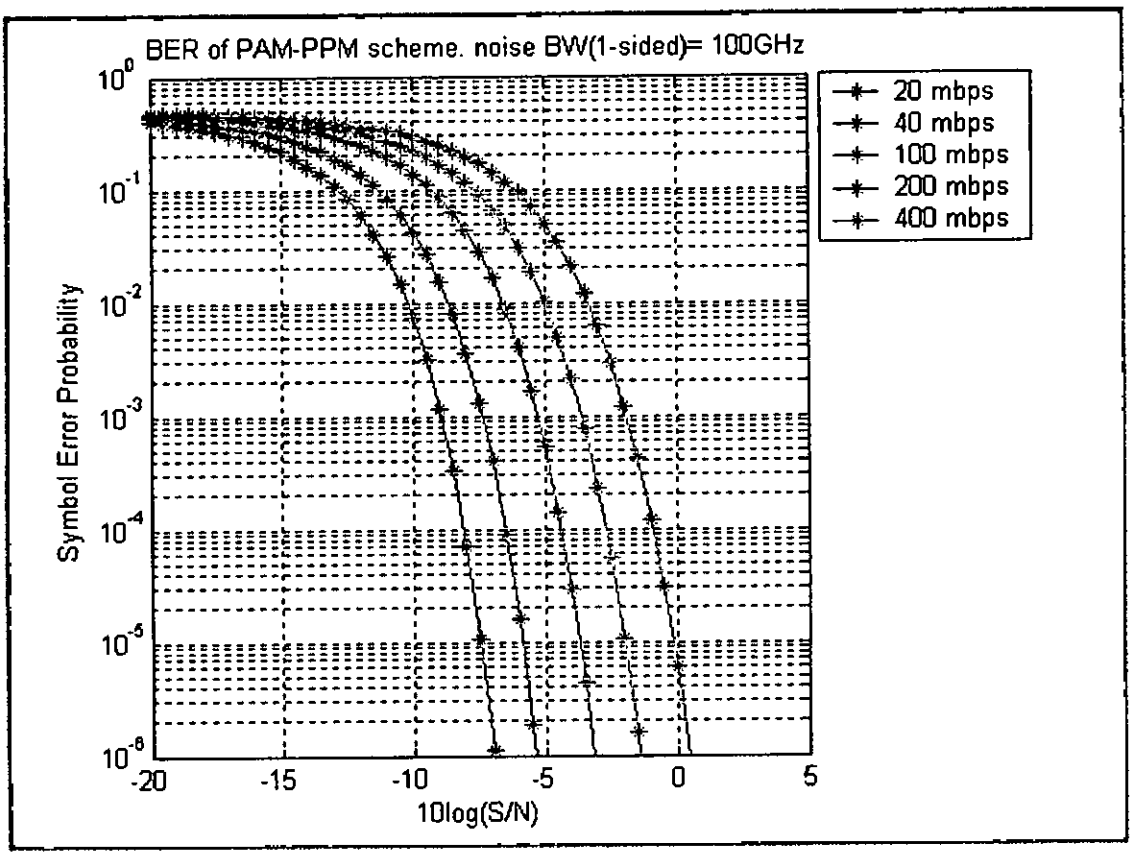


Figure 5.1: Error probabilities for PAM-PPM reception as a function of signal-to-noise power ratio

5.2 Bit-by-bit simulation result

This section presents the bit-by-bit simulation results of the ultra wideband transmitted reference PAM-PPM transceiver system which was implemented using simulink (Fig. 5.2-5.4). The system was simulated to investigate the symbol error probabilities as a function of signal-to-noise power ratio (SNR). The observations were taken for three different data rates of 100 mbps, 200 mbps and 400 mbps.

Table 5.1: simulation results for data rate of 100 mbps

SNR (dB)	Total Bits	Total Errors	Symbol Error Rate
-12.5	200	65	0.325
-10	1000	135	0.135
-7.5	1000	18	0.018
-6.5	5000	17	0.0034
-6	10000	19	0.0019
-5	66040	7	0.000106

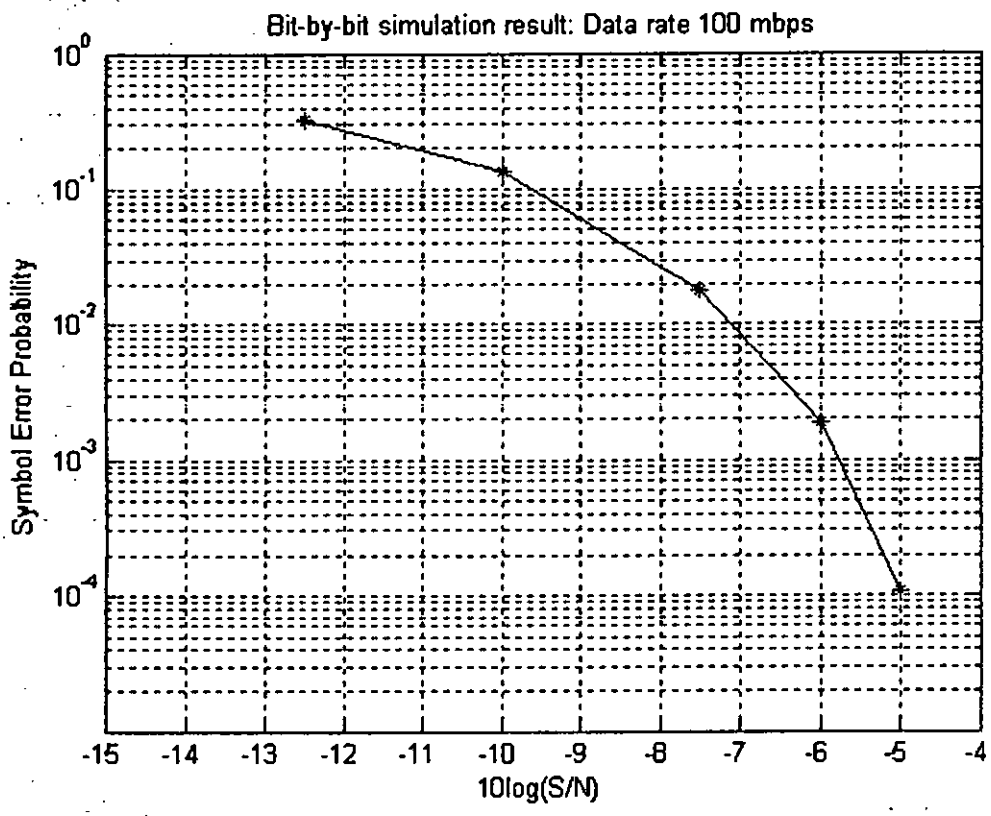


Figure5.2: Error probability for 100 mbps using bit-by-bit simulation

Table 5.2: simulation results for data rate of 200 mbps

SNR (dB)	Total Bits	Total Errors	Symbol Error Rate
-10	500	140	0.28
-7.5	500	45	0.09
-5	1170	10	0.008547
-4	10000	11	0.0011
-3.5	24430	10	0.0004093
-3	100000	11	0.00011

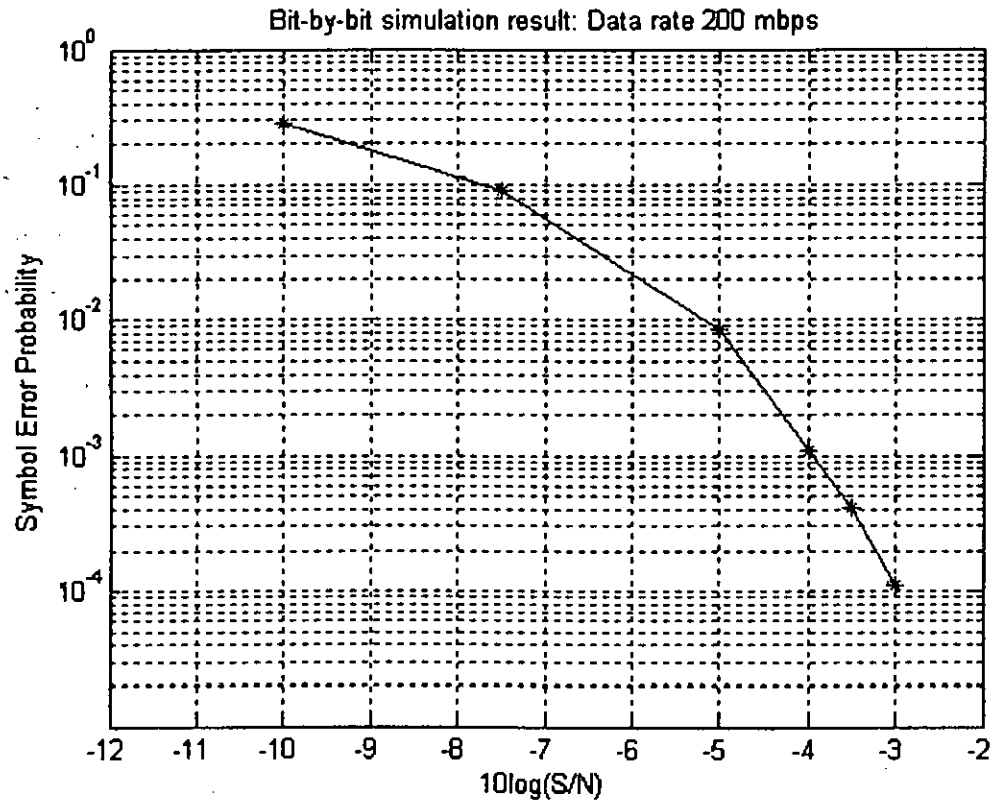


Figure5.3: Error probability for 200 mbps using bit-by-bit simulation

Table 5.3: simulation results for data rate of 400 mbps

SNR (dB)	Total Bits	Total Errors	Symbol Error Rate
-8	300	82	0.2733
-5	500	30	0.06
-3	2500	15	0.006
-2	10000	11	0.0011
-1.5	23000	11	0.0004783
-1	63820	11	0.0001724

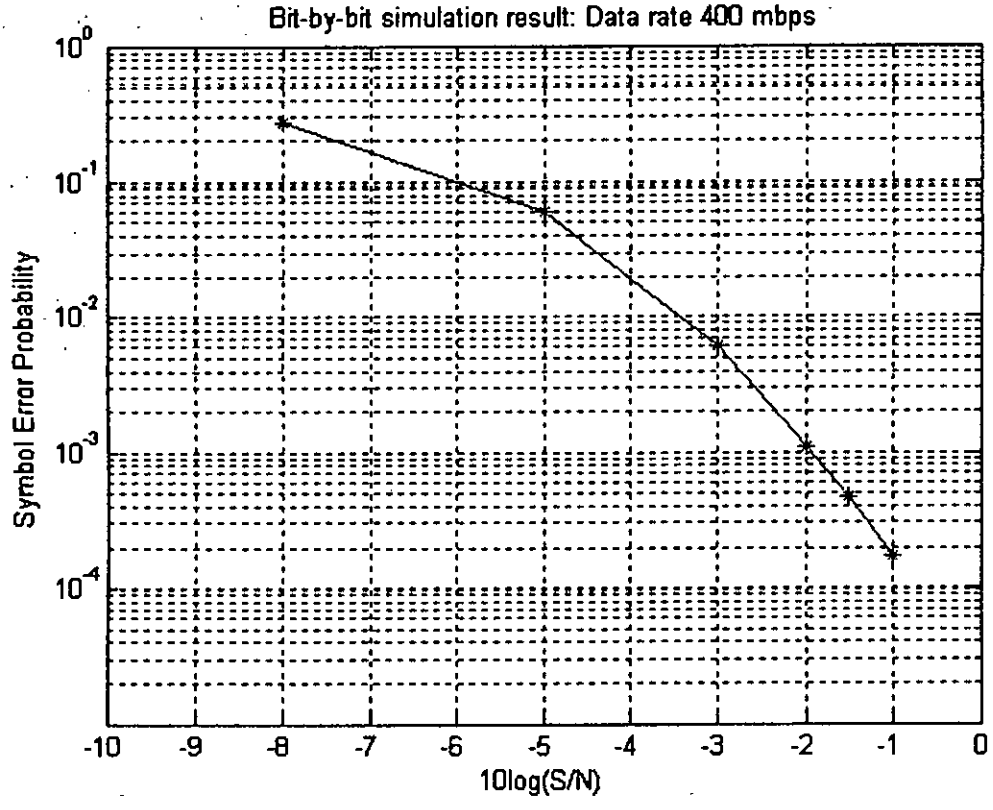


Figure5.4: Error probability for 400 mbps using bit-by-bit simulation

All the above results have been combined in a single graph in Fig. 5.5.

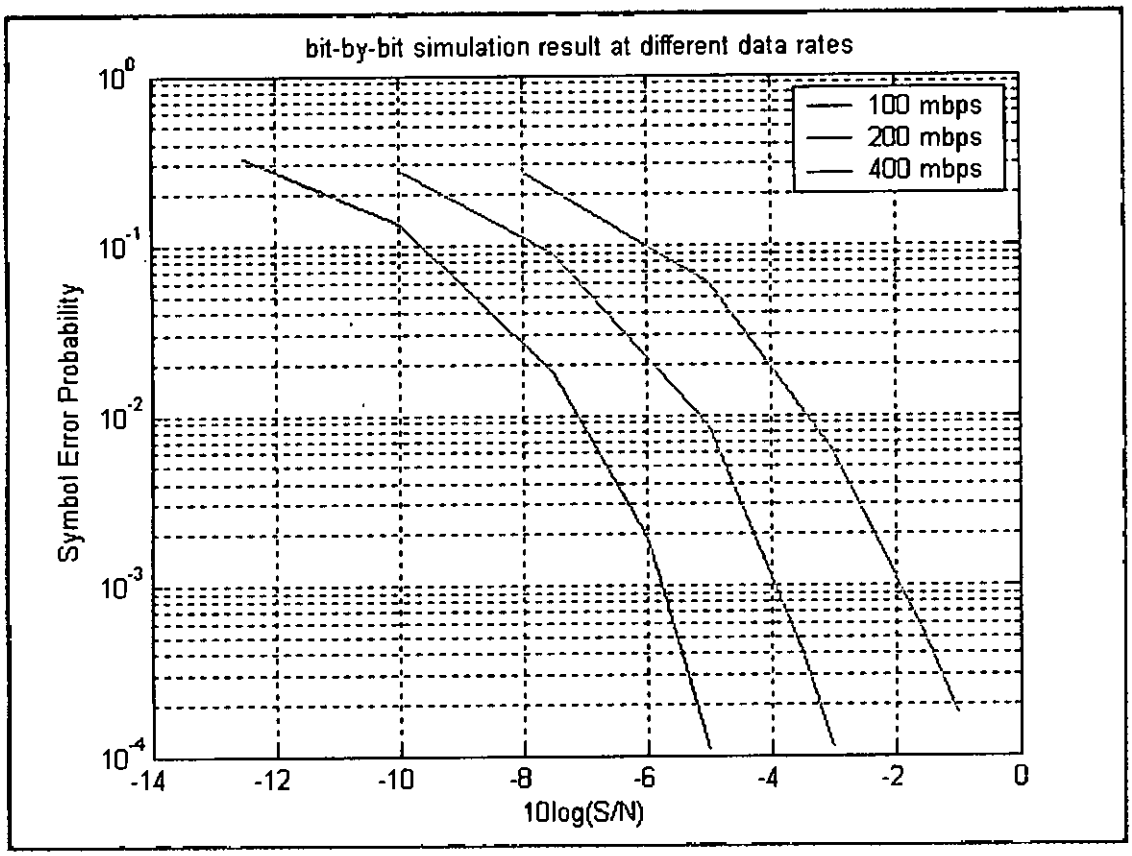


Figure 5.5: Error probabilities at different data rates.

Once the simulation results are in hand, various factors influencing the error probabilities can be analyzed as follows.

Influence of the bit rate:

In any communication link, it is expected that the lower the bit rates, the less the error probabilities for a fixed signal-to-noise power ratio. To the contrary, for transmitted reference communication, the more the integration time the more the noise contribution in the integrator output and hence there is a penalty for decreasing the data rate. Fig. 5.5 shows that the later effect is less prominent than the first one. Therefore, "the higher the data rates, the more the probability of error" remains valid for transmitted reference communication. Table 5.4 shows the comparison.

Table 5.4: Probability of error at different bit rates for an SNR of -5 dB

Data rate	100 mbps	200 mbps	400 mbps
Prob. Of error	0.0001	0.0085	0.06

Influence of SNR:

There is a sharp decrease in probability of error with the increase of signal-to-noise power ratio. As evident from the plotted result, the symbol error rate (SER) can go from 10^{-1} to 10^{-4} with a change of only 5 dB of S/N.

5.3 Comparison of analytical versus simulation result

The analytical and simulation data shows a close match between each other. It is seen that all the simulation result conforms to the analytical value with a tolerance limit of 0.5 dB. Fig. 5.5 shows the comparison for data rate of 400 mbps.

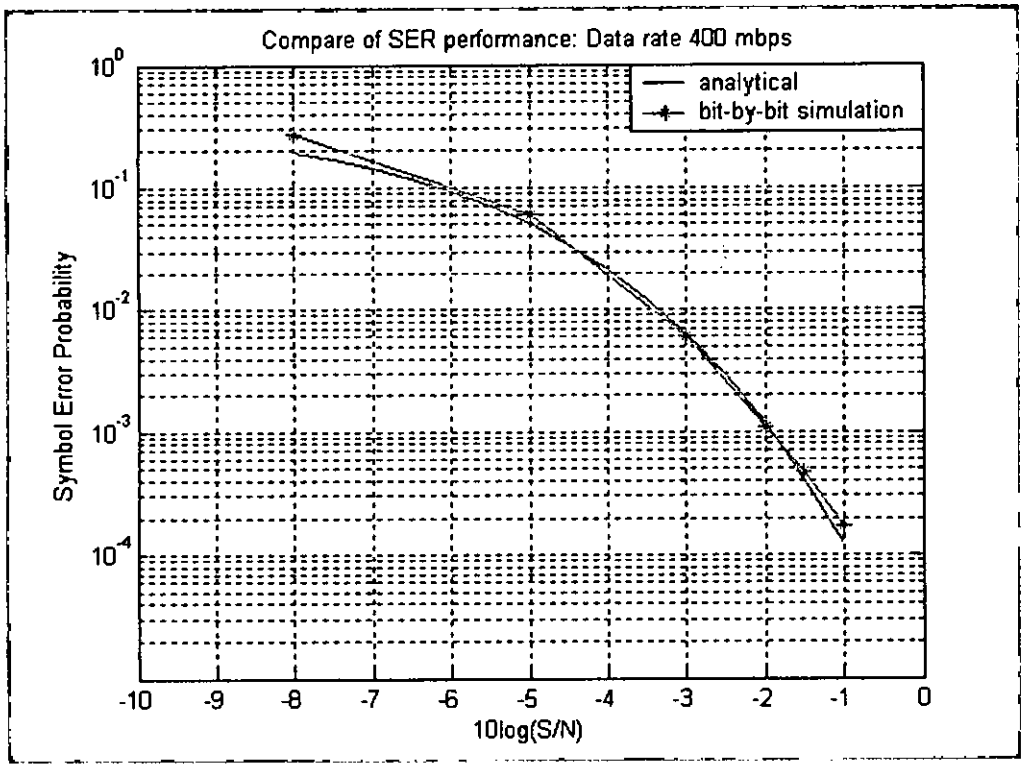


Figure 5.6: Comparison of error performance at 400 mbps

5.4 Multiple access performance

Transmitted reference scheme can be easily manipulated to achieve multiple access capability as mentioned in section 4.7. The multiple access link was simulated for two users at a data rate of 200 mbps. The bit-by-bit simulation results are presented in Table 5.5.

Table 5.5: Simulation result of multiple access performance for two user scheme

SNR (dB)	Total Bits	Receiver 1		Receiver 2	
		Total Errors	SER	Total Errors	SER
-7.5	293	15	0.052	12	0.041
-5	1123	10	0.0089	11	0.0098
-3.5	5500	11	0.002	10	0.0018
-2.5	26590	10	0.00038	10	0.00038
-2	75910	10	0.00013	13	0.00017

The salient features of the simulation results are outlined below:

- The error performance is seen to be similar for both the receivers. This can be attributed to the fact that we have used same average delays for the two receivers.

- If the data rate is same, the total amount of data to be transmitted in a two user multiple access link is double with respect to a single user link. Fig. 5.3 and Fig. 5.7 provide SER Vs SNR performance of single user link and multi user link respectively at a data rate of 200 mbps. The figures show that to achieve a SER of 10^{-4} for single user and multi user link, we need SNR of -3 dB and -2 dB

respectively. Therefore only 1 dB performance degradation occurs in the multiple access link. But if we double the total amount of transmitted data in a single user link that is at 400 mbps, we need to increase the SNR by 2 dB (Fig. 5.4). Therefore it can be concluded that transmitted reference scheme is particularly suitable for multiple access data transmission.

A graphical representation of the simulation result given in Table 5.5 is presented in Fig. 5.7.

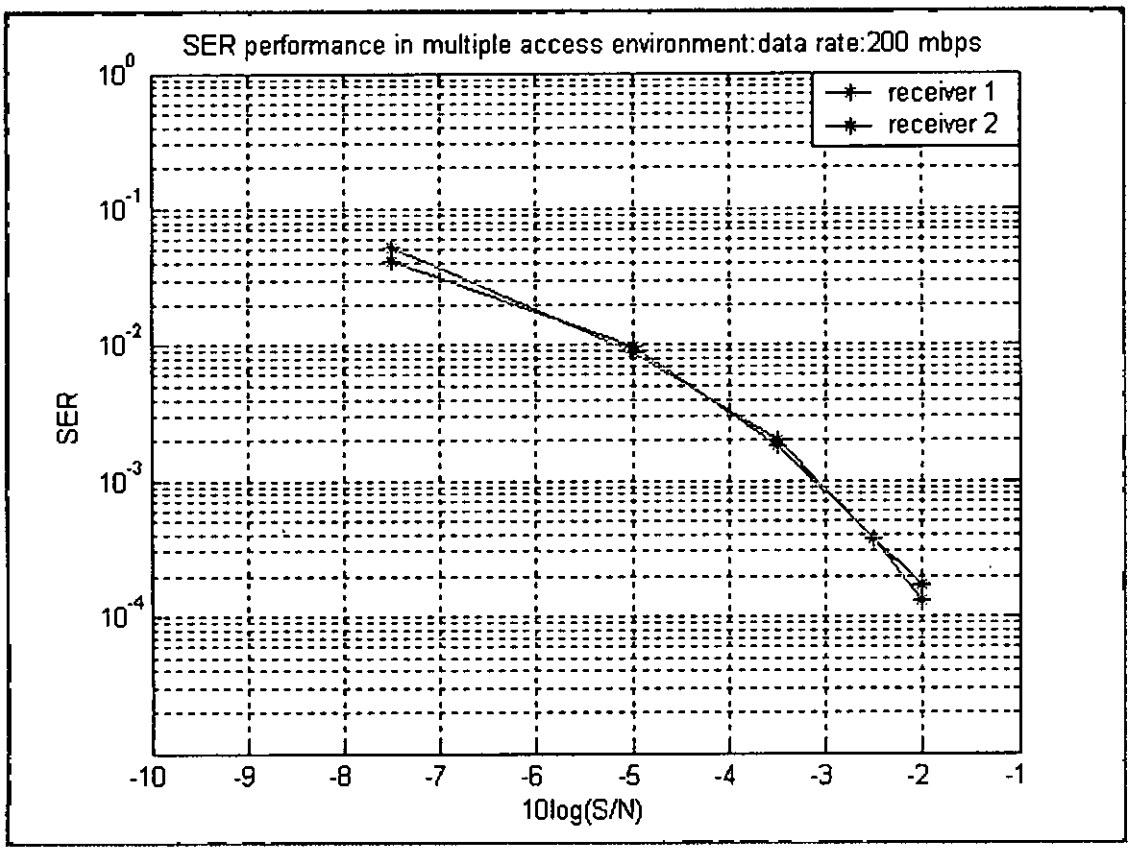


Figure 5.7: Multiple access performance of transmitted reference UWB link

5.5 System performance analysis

The overall system performance has been investigated for the entire chip size of 20 x 20 mm^2. The average received power is given by,

$$S_r = S_t + G_{tr} + G_r \tag{5.1}$$

where S_t is the transmitted energy in dBm, G_{tr} is the average value of transmission gain between the transmit and receive antenna in decibels, and G_r is the gain of the receiver in dB. The average value of the transmission gain G_{tr} can be obtained from on-chip measurement. Fig. 5.8 shows the average value of G_{tr} versus distance for dipole antennas of length 2 mm [19]. It should be mentioned that G_{tr} in the figure does not include the reduction due to the chip metal lines in between the transmit and receive antennas. This reduction can be up to 10 dB [18]. The system parameters are cited in table 5.6.

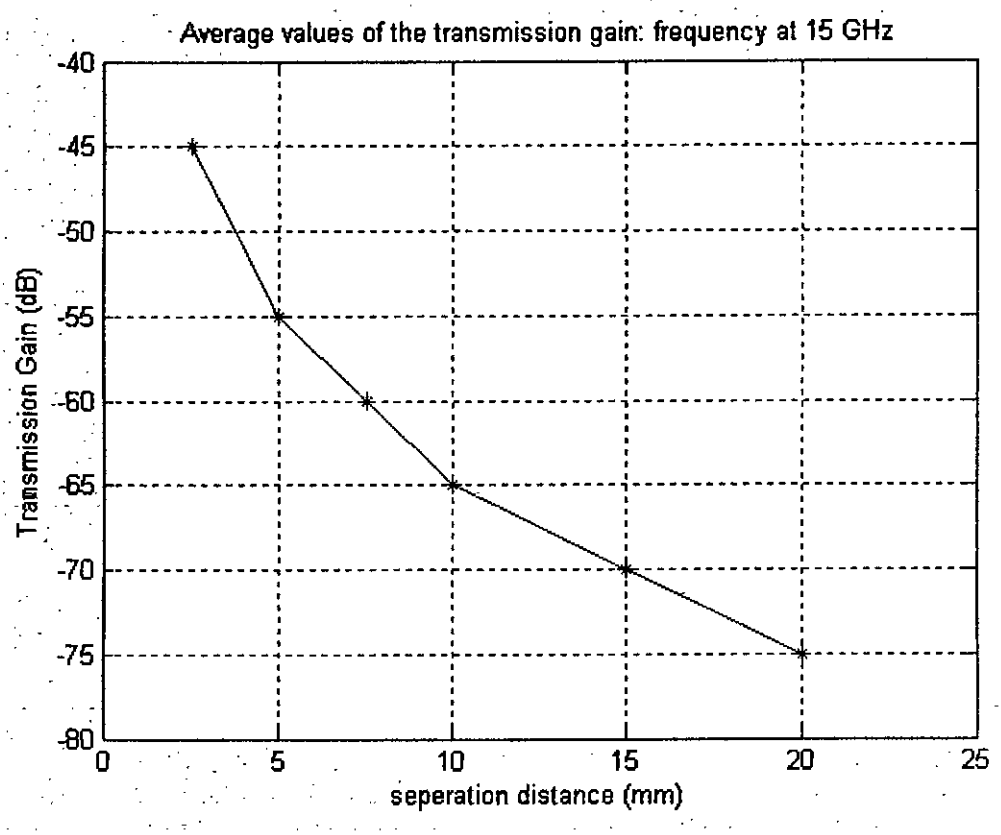


Figure 5.8: Average values of the transmission gain versus distance

Table 5.6: Specifications of the transceiver system for wireless interconnect

Parameters	Value
Data rate	400 mbps
Transmit power S_t	0 dBm
Receiver's gain G_r	20 dB
Receiver's Noise Figure F_r	10 dB

Now employing eq (5.22 the system error performance can be easily evaluated and the results are presented in Fig. 5.9.

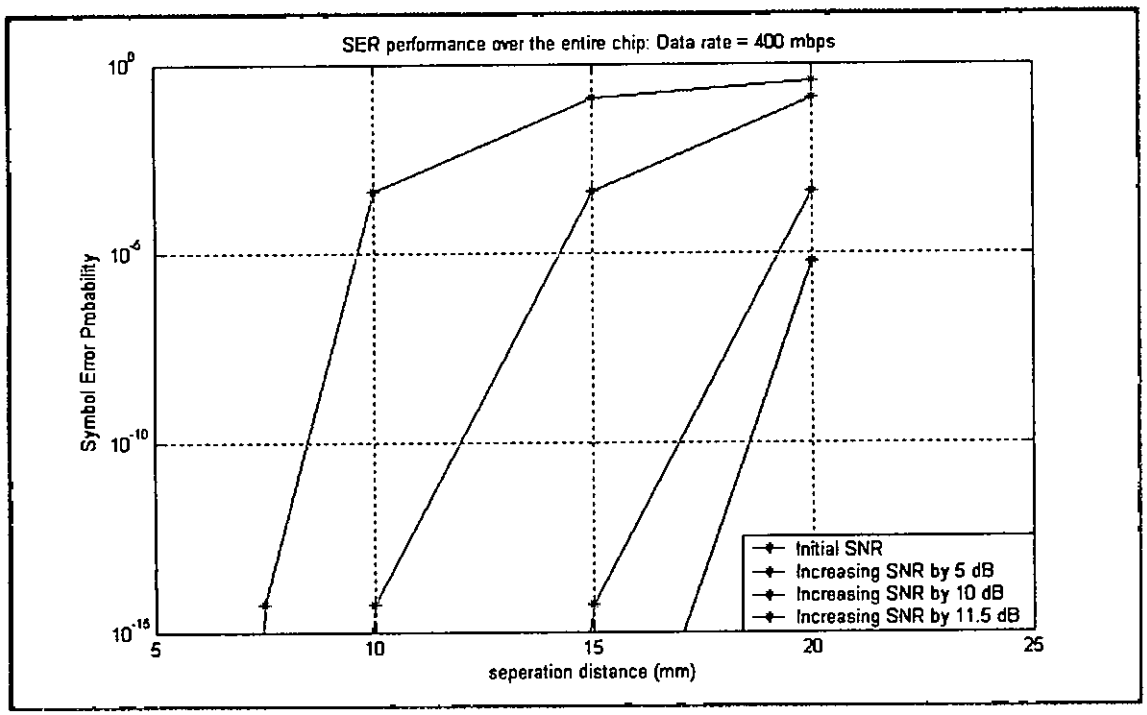


Figure 5.9: SER versus transmitter receiver separation distance

Over 10 mm distance BER is > 10^{-5} and to achieve a low BER<10^{-5} over the entire chip size of 20 x 20 mm^2, it is required to increase the SNR by 11.5 dB. This increase in SNR can be obtained either by increasing the transmitted power, receiver's gain or by decreasing the receiver's noise figure. In addition, transmission gain has the potential to be improved by 10 dB using a new process as reported in [20].

5.6 Comparison of Conventional BPM and PAM-PPM modulation

The receiver error performance was investigated with the help of simulink model for the modulation schemes of conventional BPM and proposed PAM-PPM. This study was carried out by using **windowed integrators** in the receiver correlator instead of **integrate and dump unit.** This modification allows the systems to be operated in a much low SNR value. The results are presented in Fig. 5.10. The figure shows that for same error probability, the proposed PAM-PPM modulation requires around 2 dB less SNR compared to BPM modulation.

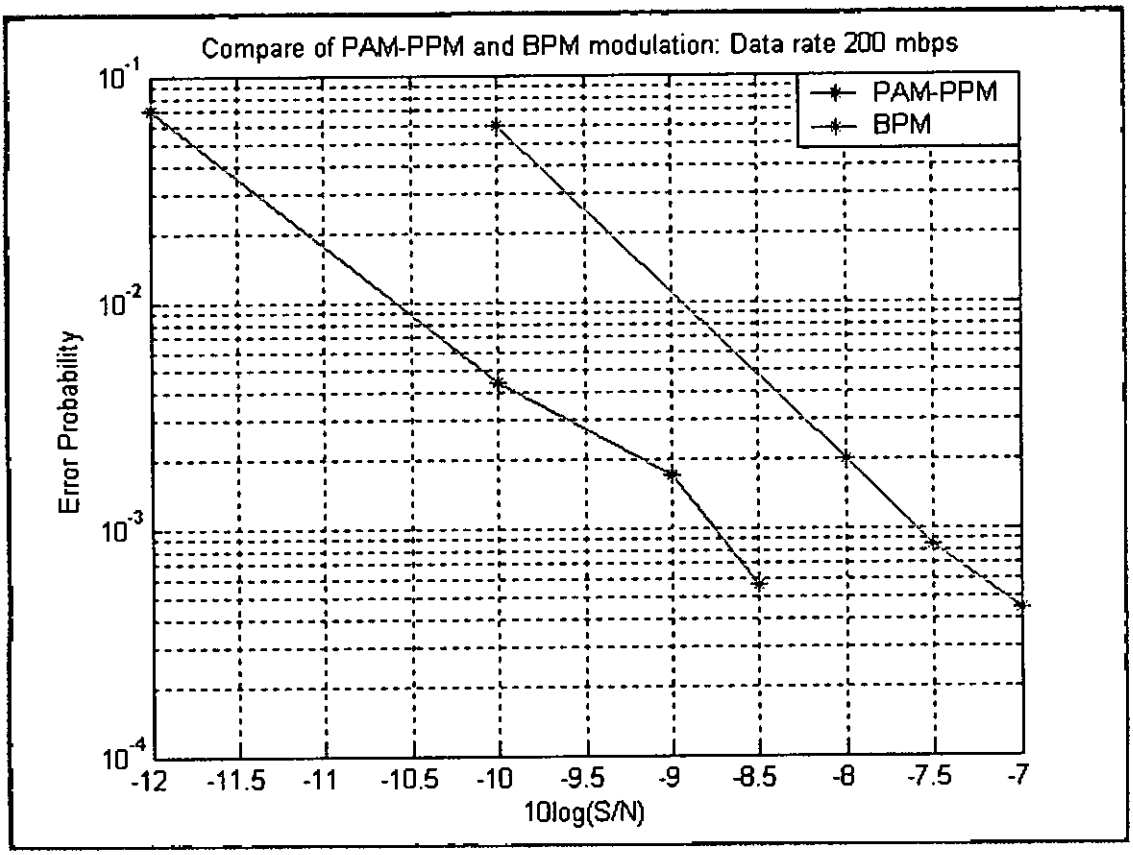


Figure 5.10: Comparison of BPM and PAM-PPM modulation schemes

CHAPTER 6

RECEIVER CIRCUIT

The proposed architecture of the ultra-wideband transmitted reference system is shown in Fig. 6.1. Details of each block are described in the following sections.

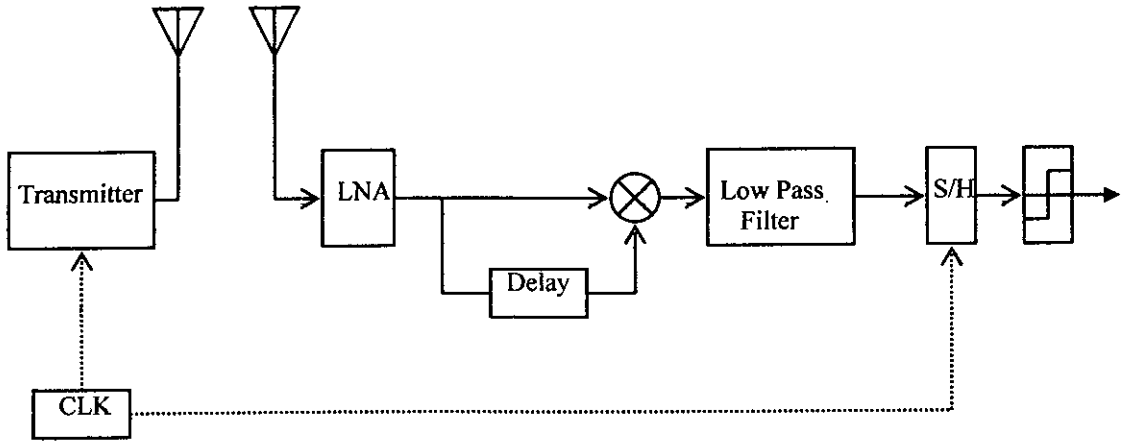
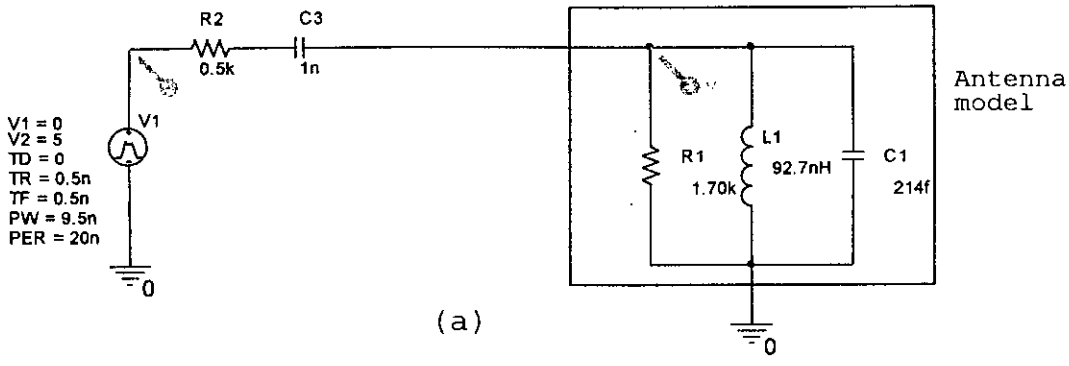


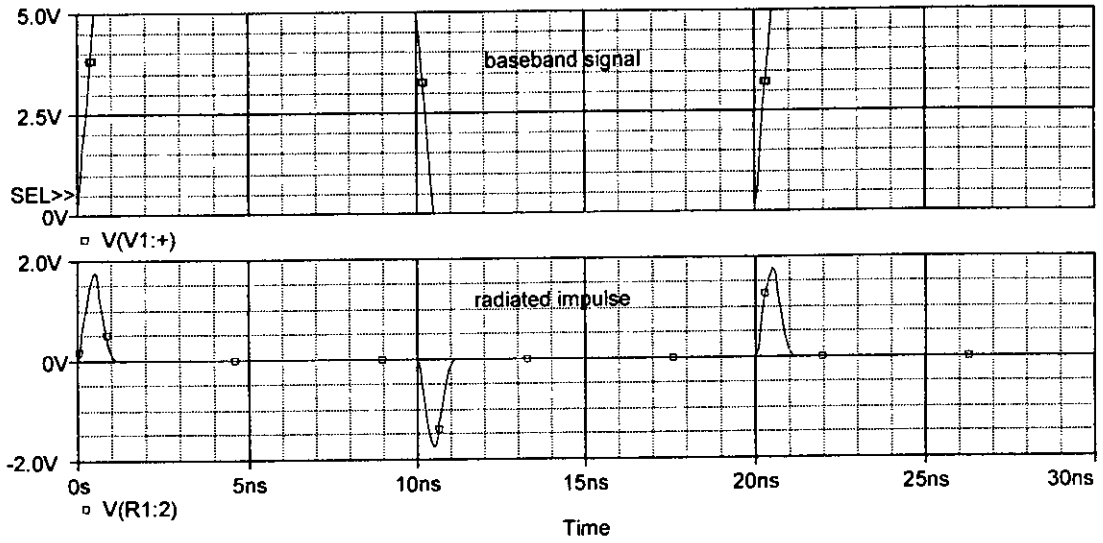
Figure 6.1: Simplified block diagram of the proposed receiver architecture

6.1 Transmitter circuits

The transmitter section consists only of digital circuits. It generates ultra wideband pulses without any conventional pulse generator. This means, the baseband signal is applied directly to the antenna and the signal is transformed into an impulse when it is radiated. Fig. 6.2 shows the circuit schematics of UWB pulse generator.



(a)



(b)

Figure 6.2: (a) circuit schematic for UWB pulse generator (b) waveform of baseband signal and radiated impulse

6.2 Receiver circuits

The receiver consists of a low noise amplifier (LNA), delay unit, mixer, low pass filter and a threshold comparator. Each block of the receiver will now be described here.

6.2.1 Low noise amplifier

The LNA is the first circuit block in the receiver chain. It first amplifies a weak signal coming from the antenna and then the amplified output is fed into the mixer. The design objective of the LNA is to amplify the received signal with as little distortion and additional noise as possible.

The LNA structure consists of three components:

- A matching network
- An amplifier
- A load

Fig. 6.3 presents our designed LNA circuit.

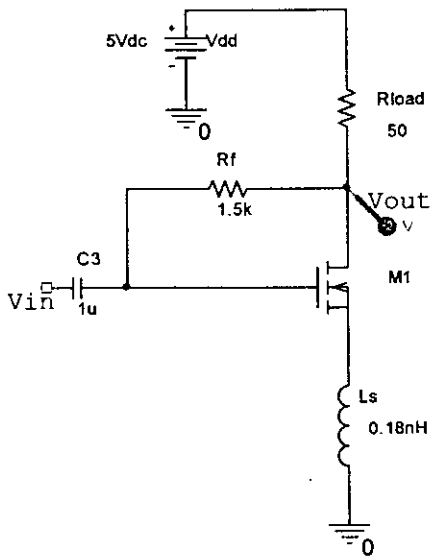


Figure 6.3: Circuit schematic of LNA

This particular LNA topology is termed as shunt-series feedback. With this architecture, the bias point of the input is fixed with the output voltage. Therefore the biasing point of this system is not set to the optimal bias point. However, this architecture gives good noise figure and wide-bandwidth characteristic for the UWB system.

As shown in Fig. 6.3, active component of the LNA is a MOS transistor in the common source configuration. The inductor L_s is added for simultaneous noise and impedance matching between the source and the input of LNA. R_f is added as a shunt feedback element to provide wideband characteristics of the amplifier.

The designed LNA is very simple in construction and requires only single stage

architecture to provide adequate gain. It has a wide bandwidth ranging from 1 GHz to 4.2 GHz with an average gain of 20 dB in the pass band. The frequency response curve of the LNA is shown in Fig. 6.4.

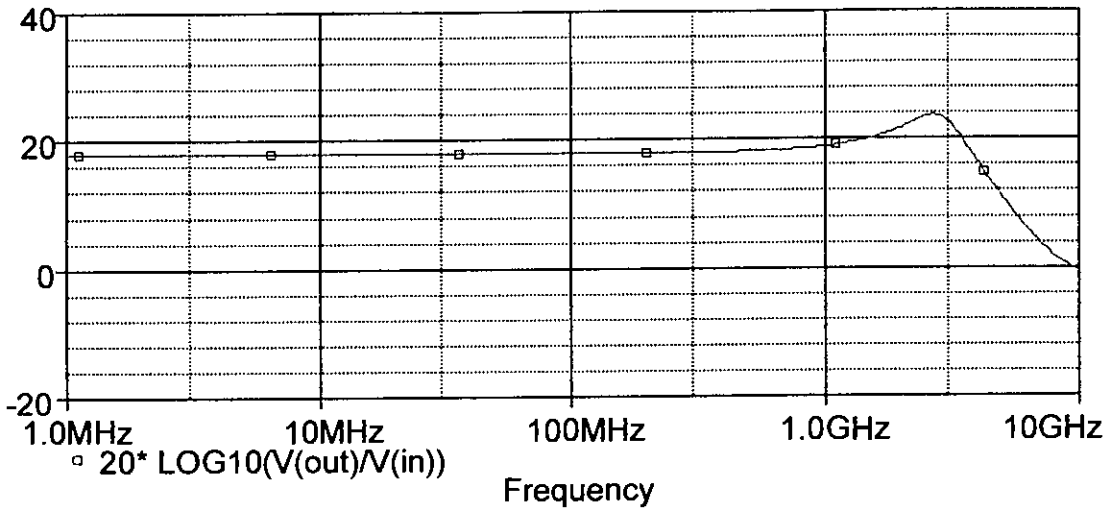


Figure 6.4: Frequency response curve of the designed LNA.

6.2.2 Delay unit

The delay unit is a crucial design block for TR radio implementation. This unit provides adequate delay to the reference pulse so that it appears simultaneously with the data pulse to the input of the correlator. There are several ways of introducing an analog delay into a signal channel.

- **Analog delay circuit:** This is the method to provide delay with the help of electrical circuit components. The theory of this technique is based on the Laplace transform of an ideal delay which can be expressed as an exponential function.

$$\frac{V_o}{V_i} = \exp(-\tau \times s) \tag{6.1}$$

Where, τ is the desired delay, which requires an infinite number of poles and zeroes to implement. Because the ideal form cannot be implemented (practically), we need to use an approximation. An accurate, simple approximation to the ideal can be achieved by using a technique known as Padé approximation. The first-order Padé approximation to an ideal delay has the following form:

$$\frac{V_o}{V_i} = \frac{1 - \tau \times s/2}{1 + \tau \times s/2} \tag{6.2}$$

where π is the desired delay.

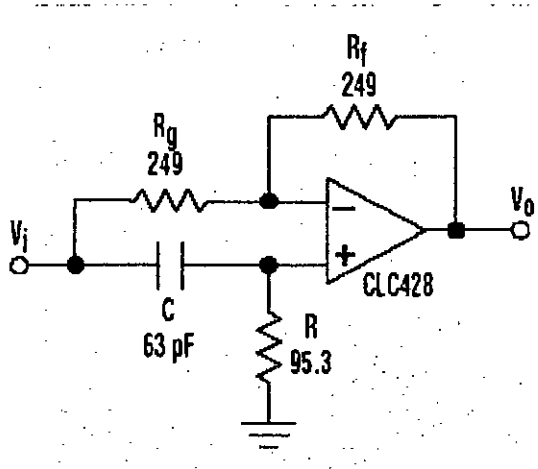


Figure 6.5: Circuit diagram of an analog delay unit

The circuit in Fig. 6.5 has the following transfer function (6.3): which has the same form as the first order Padé approximation (6.2), with the R*C time constant equaling half the desired delay time.

$$\frac{V_o}{V_i} = \frac{1 - R \times C \times s}{1 + R \times C \times s} \tag{6.3}$$

This circuit, however provides controllable delay if op-amp with a wide bandwidth is selected, is not suitable for UWB application. UWB

communication employs Gaussian monopulses to transmit data which are highly nonlinear in characteristics and hence simple first order Padé approximation is not applicable.

- **Transmission line (TL):** Another method of creating a delay is the use of wave propagation. A wave that travels at velocity V is received at a distance L a time L/V later. For nondispersive propagation, the velocity V is independent of the frequency. Phase, group and energy velocity are all the same, and things are simple. Electromagnetic waves can be created at one end of a transmission line of length L, and picked up at the other end with a delay of L/V.

The delayed version of the output of a TL is distortionless and particularly suitable for UWB application. The delay unit was simulated using a transmission line (TL) model of the SPICE program. The characteristic impedance of the TL was chosen to be 50 ohm. Fig. 6.5 shows the received signal and the corresponding delayed version at the output of the transmission line.

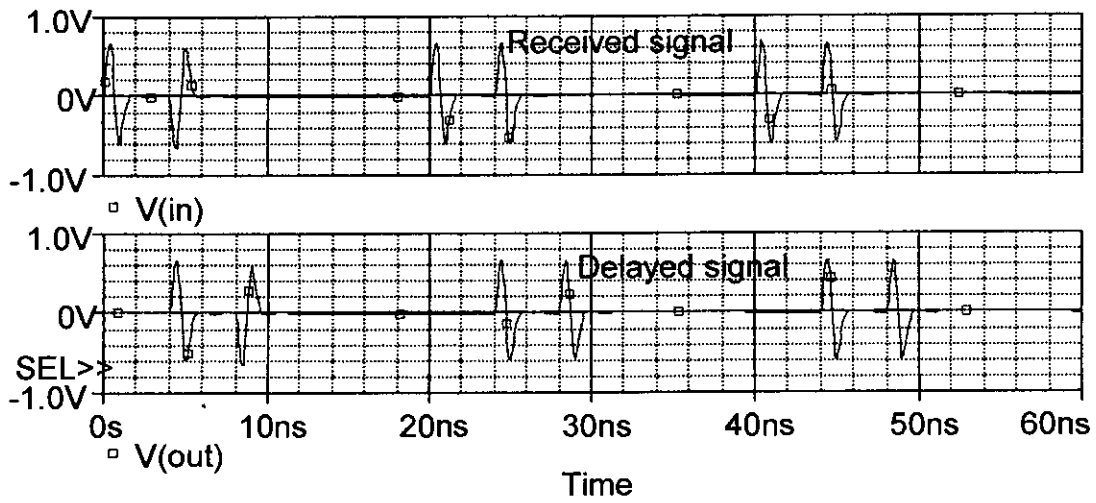


Figure6.6: Signal propagation through the delay unit

6.2.3 Mixer with low pass filter

The mixer is an essential element in the receiver architecture which correlates the incoming signal with the reference signal. Fig. 6.6 shows the proposed mixer circuit.

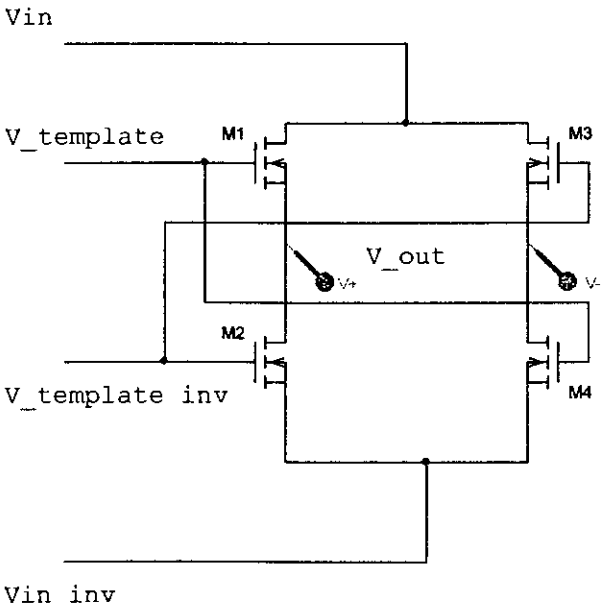


Figure 6.7(a)

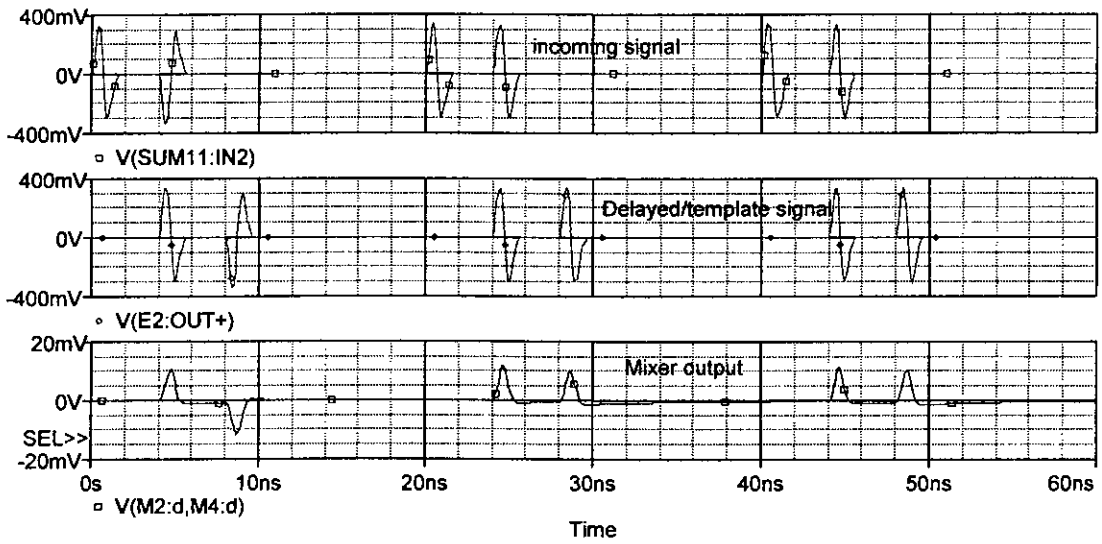


Figure 6.7(b)

Figure 6.6: (a) Voltage mixer circuit diagram and (b) simulation result

This particular type of mixer is called voltage mixer. This topology has the advantage of low power consumption, low noise figure and high linearity. Nevertheless it has conversion losses.

As shown in the simulation results of Fig. 6.6, the mixer provides zero average value when the reference and the data pulses are of opposite phase; whereas a nonzero average value is obtained when these pulses are of same phase. As a result, if the output of the mixer is passed through a low pass filter, the two different binary states of the received signal will be evaluated.

CHAPTER 7
CONCLUSION

7.1 Summary

In this thesis, the potentials of using ultra wideband transmission technology as wireless interconnects system have been investigated. At the end of the thesis, the following outcomes can be highlighted.

It has been proposed, for the first time, a TR UWB communication for on-chip wireless interconnects system. This approach allows a straight-forward synchronization technique by giving proper delay to the reference pulse and also avoids complicated intra-chip channel estimation for the detection unit. Therefore it results in a simplified transceiver architecture. Moreover, TR UWB technique is particularly suitable for implementing software reconfigurable wireless channel this scheme has excellent multiple access capabilities

The system performance has been investigated under a new modulation scheme termed as PAM-PPM technique. It is actually a hybrid modulation in which signal intelligence is encoded both in the position and amplitude of the data pulse. The error performance of this proposed modulation technique was evaluated both analytically and through computer simulation. It was found that for same error probabilities and same data rate, the system can be operated at 2 dB less SNR by applying the PAM-PPM modulation technique compared to conventional BPM modulation.

The overall system performance has been investigated over the entire chip size of 20 x 20 mm^2. With transmitted power at 0 dBm, receiver gain 20 dB and noise figure 10 dB, it was found that we need to increase the SNR by 11.5 dB to achieve a low BER<10^{-5} over the entire chip size. This increase in SNR can be obtained either by increasing the transmitted power, receiver's gain or by decreasing the receiver's noise figure. In addition, transmission gain has the potential to be improved by 10 dB using

new process as reported in [7].

The circuit diagrams of different receiver blocks was designed and simulated using SPICE. The proposed system is simple in architecture and hence creates less electronic overhead on the existing chip circuitry.

7.2 Suggestions for future work

Though TR scheme provides simplified synchronization and avoids channel estimation, it has a significant disadvantage which is yet to be solved. In TR technique the noisy delayed version of the incoming signal is used as the template signal for correlation purposes. As a result, noise content in the output of the correlator is high and the system performance is degraded. The use of **windowed integrator** instead of **integrate and dump unit** can help a lot to improve the performance.

We bypass the need for channel estimation by using TR technique; but a standard UWB channel model for intra-chip communication is necessary. This will enable us to compare TR and non TR system in terms of data rate, error probability, system complexity and power requirement.

Though the circuit model of the receiver architecture is given, their performances are yet to be evaluated in terms of noise figure, linearity and on-chip implementation.

Appendix A

Matlab code of ultra wideband pulse generation

```
clear;
fc = 2E9;  fs=100E9;            % center freq, sample freq
tc = gmonopuls ('cutoff', fc);
t1 = -2*tc : 1/fs : 2*tc;
y1 = -gmonopuls (t1, fc);
t = 0:1/fs:(1e-8);
for n=1:length(t)-1
   if n<=length(y1)
      y(n)=y1(n);
   else
      y(n)=0;
   end
end
source.time = [];
source.signals.values = y';
source.signals.dimentions = 1;
```

Appendix B

SPICE program of Low Noise Amplifier

```
Vdd 1 0 5V
Rl 1 out 50
Rf out 3 1.5k
M1 out 3 5 5 nmos1 w=3600u l=2u
Ls 5 0 0.18nH
c1 in 3 1u
vin in 0 ac 1mv

.model NMOS1 NMOS LEVEL=3 PHI=0.7 TOX=9.6E-9 XJ=0.2u
+TPG=1 VTO=0.7118 DELTA=2.3060E-1 LD=2.983E-8
+KP=1.8201E-4 Uo=506.0 THETA=1.909E-01 RSH=1.894E+1
+GAMMA=0.6051 NSUB=1.427E+17 NFS=7.15E+11 VMAX=2.496E+05
+ETA=2.5510E-02 KAPPA=1.853E-01 CGDO=9.0E-11 CGSO=9.0E-11
+CGBO=3.7295E-10 CJ=6.02E-04 MJ=0.805 CJSW=2.0E-11
+MJSW=0.761 PB=0.99

.AC DEC 101 1meg 10G
.PROBE
.END
```

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