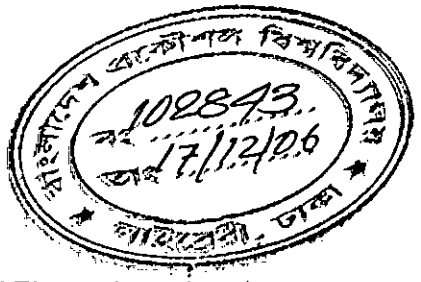
Design of a Single Phase Rectifier with Switching on the AC Side for High Power Factor and Low Total Harmonic Distortion

by

MEHJABEEN AKHTAR KHAN



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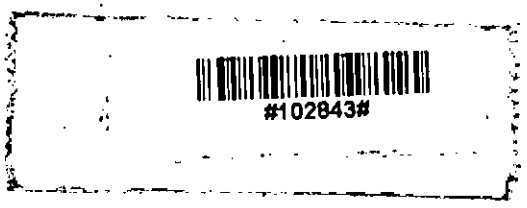

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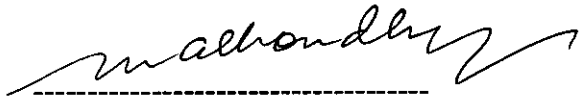

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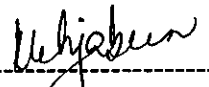

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V_m	Maximum Value of Input Voltage	V
L	Inductance	mH
C	Capatance	μF
R	Resistance	Ω
R_L	Load Resistor	Ω
T	Time Period	sec
v_o	Output Voltage	V
i_L	Load Current	Amp
i_D	Input Current	Amp
i_C	Current Through Capacitor	Amp
v_l	Voltage Across the Capacitor	V
v_s	Input Voltage	V
V_r	Peak to Peak Ripple Voltage	V
f	Frequency	Hz
ω	Angular Frequency	rad/sec
$Q_{supplied}$	Charge Supplied to the Filter Capacitor	coulomb
Q_{lost}	Charge Lost by the Capacitor	coulomb
i_{Cav}	Average Capacitor Current	Amp
i_{Dav}	Average Diode Current	Amp
i_{Dmax}	Peak Value of the Diode Current	Amp
V_c	Voltage Across Capacitor	V
ω_m	Resonating Frequency	rad/sec
τ	Time Variable Within the Switching Interval	sec
T_S	Switching Period	sec
D	Duty Cycle	-
Δi	Change in Current	Amp

ABSTRACT

A scheme for improving the input current waveshape of a single phase bridge rectifier has been proposed and analyzed. A bridge rectifier with filter capacitor connected to reduce ripples of output voltage draws discontinuous and non-sinusoidal current from the supply. In this work a switching scheme has been developed which exploits a single MOSFET switch driven by rectangular gate pulses whose duty cycle is continuously varied over the period of supply voltage. The switch provides an alternative path for the input current during the periods when due to the reverse biasing of rectifier diodes input current ceases to flow otherwise. The variation of duty cycle of the switching pulses has been intuitively varied like a rectified cosine wave. The switching scheme combined with an input LC (inductor-capacitor) filter that has a resonating frequency almost equal to that of supply voltage, has been found very effective in improving the input current waveshape. Analytical expression for the input current drawn by the rectifier with proposed switching is derived and detail simulation results are presented which shows that the rectifier with the proposed scheme draws sinusoidal current at unity power factor and has high overall efficiency. The Total Harmonic Distortion (THD) in input current is reduced below 2%. Different combinations of LC filter elements and switching frequency have been considered to obtain optimum results in terms of THD and overall circuit efficiency.

CHAPTER 1

INTRODUCTION

1.1 Background and Present State of the Problem

All electronic circuits in modern power appliances require a stable and regulated dc power supply. AC to DC conversion is therefore found as one of the most common operations in power electronics. In it's simplest form AC to DC conversion is achieved by semiconductor diodes forming a bridge rectifier. The output voltage of a bridge rectifier is pulsating DC. A filter capacitor across the load is connected to reduce the ripple in output voltage. The effect of the filter capacitor is that instead of drawing smooth sinusoidal currents, the rectifier draws currents in short pulses [1] which leads to low input power factor and injection of harmonics into the lines [2]. The presence of such low frequency current harmonics in the utility lines introduces several other problems including [2]:

a. phase displacement between current and voltage fundamentals that necessitates the use of source and distribution equipments with higher volt-ampere ratings in order to handle reactive power,
b. input ac mains voltage distortion because of associated higher peak currents, and
c. lower rectifier efficiency due to large rms values of the input current,
d. reduction of available power and heating of the ac lines, and
e. increasing the malfunction probability of associated sensitive electronic equipments.

For these reasons AC to DC converters connected to AC mains are forced to accomplish certain standards that limit injection low frequency harmonics in utility. Development of AC to DC converters/rectifiers with improved input current waveform has therefore gained importance to meet stringent power quality regulation and strict limit on the total harmonic distortion (THD) of input current placed by IEC 1000-3-2 and IEEE 519-1992 standards [3,4]. This has led to consistent research in devising various techniques for

power quality improvement and input current wave shaping by modifying classical diode bridge rectifier followed by a bulk capacitor.

For single phase rectifier applications, a converter with a non-controlled and one switch is commonly used [5-6]. The techniques exploited for improving the input current waveshape and power factor of rectifiers include both active and passive means. Passive techniques which introduce a filtering stage consisting of inductor and/or capacitors that reduce the amplitude of the low frequency harmonics are attractive for their simplicity, reduced cost and reliability. This solution, though offers a trade-off between cost and performance, is unattractive for compact uses due to their physical size and weight [2, 4,7].

Active techniques on the other hand, use a high switching frequency converter that shapes the input current to almost sinusoidal waveform with small harmonic content [4]. Since their basic compensation principles were proposed, much research has been done on active filters and their practical application [10-15]. One approach is to use three single-phase power factor corrected rectifiers in cascade [16]. The main advantage of this configuration is that a well-known single-phase power factor correction (PFC) technique can be used in three phase applications. But the technique increases component count and complicates the input synchronization logic. Harmonic injection method [17], where the injected signal modifies the duty cycle of the rectifier switch to meet IEC1000-3 requirement, is another reported method to reduce THD in input current. Nevertheless in this case the expected results are not achievable if the phase of the injected signal is not well synchronized with the fifth order harmonic of the input current. Recently a boost power factor correction (PFC) method has been reported [18] where the switch is turned on and off only twice per line period. These are called line frequency commutated rectifiers. In this case the maximum allowed switch on time is limited to keep the switch current stress at an acceptable level. As a consequence, only a limited output voltage regulation can be achieved. Another boost topology is to use six switches full bridge rectifier [13-14], which gives continuous input current, excellent power factor and low

switch current ratings but has disadvantages like considerable complexity its control circuitry, power stage and unacceptable expense for medium power application.

A family of single-switch high power factor rectifiers having continuous input current was reported that uses multiresonant scheme to operate the transistors with zero-current switching (ZCS) and diodes with zero-voltage switching (ZVS) [19]. These multiresonant rectifiers with a single transistor are capable of drawing higher quality input current at nearly unity power factor and lower stress than other quasi resonant rectifiers [20]. However, it has been shown that even though a resonant circuit is used, the transistor currents are lower than those in an equivalent high power factor PWM rectifier [21]. The active solution is satisfactory to some extent for harmonics compliance but the design complexity and cost of the additional circuitry is often found to be unacceptable in low power application.

Digital Signal Processing (DSP) based controllers have been proposed also for power factor correction in a rectifier circuit [22-23]. In this case a dual loop controller was designed to control the average input AC current as well as DC bus voltage. However, using DSPs to control power supplies has its own unique constraints imposed by limited bandwidth and sampling frequency, discretizing effects and processing delays.

Although the research efforts mentioned above have produced several power circuit configurations for power factor correction [24] that have alleviated the scenario to some extent, their greatly increased cost and complexity compared to conventional low quality rectifiers entails further study and innovation.

1.2 Objective of the Thesis

The low power factor and large harmonic line currents generated by rectifiers are long established problems which lead to voltage distortion, increased loss in distribution conductors and transformers. Hence there is a recognized need for high quality rectifiers that present high power factor load to the ac power system and draw currents of low harmonic content. The objective of this research work is to design and develop a high

performance rectifier. The thesis presents and reveals the potential of a switching scheme in achieving high quality rectification with almost sinusoidal input current with very low total harmonic distortion (THD) and unity power factor. The main reasons behind harmonic distortion of input current is the discontinuous nature of the current drawn by the rectifier due to the charging and discharging of the output filter capacitor. In this work, a switching scheme is proposed to make the input current continuous, almost sinusoidal and in phase with the supply voltage. The effect of duty cycle on shaping the input current is demonstrated analytically. Complete mathematical modeling of power factor correction and input current wave shaping scheme are carried out and simulation results are provided for performance evaluation of the proposed scheme and compared with a prototype's result.

1.3 Thesis Outline

This thesis is concerned with the design and development of a scheme to improve the input power factor and at the same time, to minimize the total harmonic distortion (THD) of the current drawn by a single phase rectifier.

In the following chapter (chapter 2), the basic principle of AC to DC conversion using diodes has been reviewed first. The reason for drawing discontinuous current by a typical rectifier has been explained. The common methods to alleviate the problem have been discussed along with their shortcomings. Finally the strategic points have been pointed out to achieve rectifiers with low harmonic distortion and high power factor.

In chapter three, the scheme for achieving single phase rectification with very high power factor (almost unity) and input current having significantly low harmonic distortion has been presented. A switching scheme with ideal switches has been introduced and described that enables the rectifier to draw almost sinusoidal current nearly in phase with the main supply. A mathematical model has been developed in order to reveal the underlying design considerations for the scheme. The input current waveform has been calculated using the derived current equation from the model to show the efficacy of the proposed scheme in achieving high quality rectification.

Chapter four presents the simulated results obtained for the proposed rectifier. Simulations have been carried out for different filter component and switching frequency. Total harmonic distortion, power factor, efficiency and other related performance parameters have been evaluated for different combinations in order to determine the optimum output.

The concluding chapter (chapter 5) provides a comprehensive summary of the whole work followed by a brief discussion on limitations of this work and some suggestions for future work.

CHAPTER 2

Input Current Drawn by a Rectifier

2.1 Introduction:

A rectifier in its simplest form consists of semiconductor diodes. Figure 2.1(a) shows the circuit diagram of a single-phase full wave diode rectifier. In both cycles (positive and negative) of input signal, unidirectional current flows through the load. This results in a pulsating DC voltage appearing across a resistive load. The ripples in the output voltage are usually suppressed by connecting a capacitor across the load. This is known as filter capacitor, which though reduces ripple factor of the output voltage, introduces harmonics into the input current drawn by the rectifier. The harmonic distortion actually results from the discontinuous nature of the input current. The discontinuous nature of the input current introduces low frequency harmonics which in turn causes problems like phase displacement between input voltage and current, input ac mains voltage distortion, lower rectifier efficiency and reduction of available power and heating of the ac lines. One problem in rectifier power supplies in that they do not use any form of power factor correction and that the filter capacitor will charge only when input voltage is close to peak or when is greater than capacitor voltage. If filter capacitor is designed using the input voltage frequency, the current will look much closer to the input waveform (load dependent); however, any little interruption on the mainline will cause the entire system to react negatively. In order to follow input voltage more closely and not have high amplitude current pulses, filter capacitor must charge over the entire cycle rather than just a small portion of it. Keeping the inrush to the capacitor constant over the entire cycle is beneficial and allows smaller filter capacitor to be used.

Without wave shape correction technique a typical rectifier supply would have a power factor of around 0.6 having considerable odd order harmonic distortion in current wave form. The third harmonic component may sometime be as large as the fundamental. Having a power factor of less than 1 along with harmonics from peak loads reduces the real power available to run the device. In order to operate a device with these

inefficiencies, the power companies must supply additional power to make up for losses. This increase in power causes the power companies to use heavier supply lines, otherwise self heating can cause burnout in the natural line conductor.

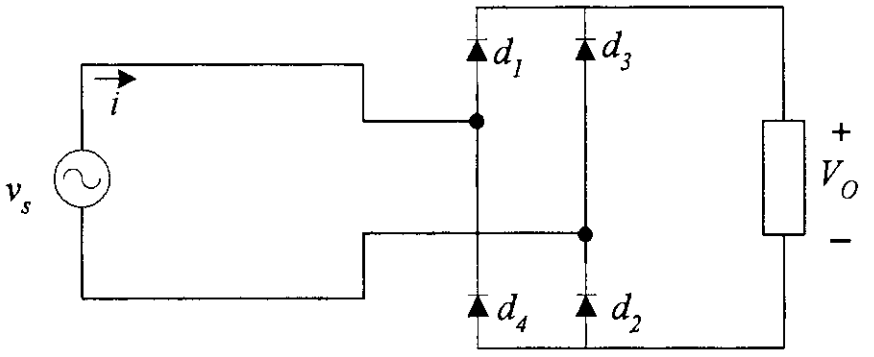


Figure 2.1 (a): A Single phase full wave bridge rectifier

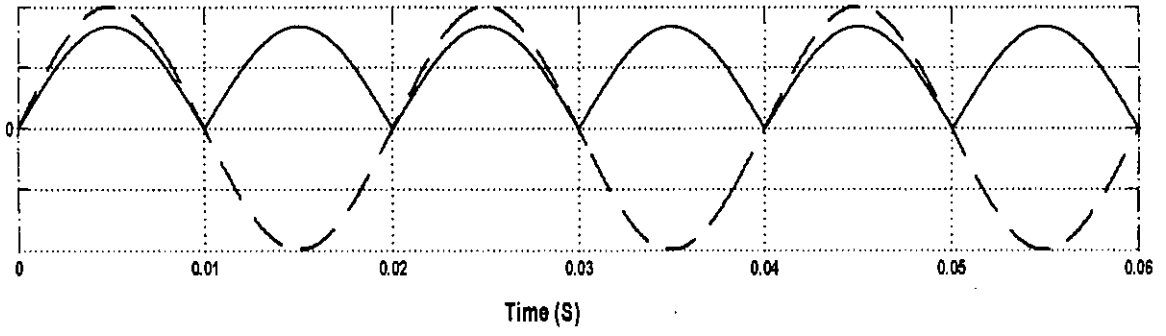


Figure 2.1 (b): Wave forms of output (firm line) and input voltage (dotted)

The harmonic distortion can cause an increase in operating temperature of generation facility, which reduces the life of equipment including rotating machines, cables, transformers, capacitors, fuses and protecting devices etc. Problems are caused by the harmonics creating additional losses and dielectric stresses in capacitors and cables, increasing currents in windings of rotating machinery and transformers and noise emissions in many products. Before going into remedial of the problem of input current shape of a rectifier, briefly the problem is discussed in next sections. In this chapter the discontinuous nature of the input current would be analyzed first. The existing methods of eliminating harmonics from the input current will then be introduced.

2.2 Input current wave distortion in bridge wave rectifier

The full-wave rectifier, unlike the half-wave rectifier utilizes both halves of the input sinusoid and it provides unipolar output by inverting the negative halves of the sine wave. One of the possible implementations of full wave rectifier circuit is a bridge rectifier circuit as shown in figure 2.1. During the positive half-cycle of input voltage, power is supplied to the load through diodes d_1 and d_2. During the negative cycle, diodes d_3 and d_4 conducts. The waveforms for the output voltage along with corresponding sinusoidal ac input voltage are shown in figure 2.1(b). The output voltage of the full wave rectifier with sinusoidal input and resistive load is a pulsating dc but with a high ripple factor which considerably reduces the average value of the output signal. However, the average value of this signal can be improved by using a filter capacitor across the load. The ripple factor of the output voltage with such filter capacitor can be minimized by proper choice of the capacitance value. Figure 2.2 shows the output signal achievable with a filter capacitor along with the circuit arrangement.

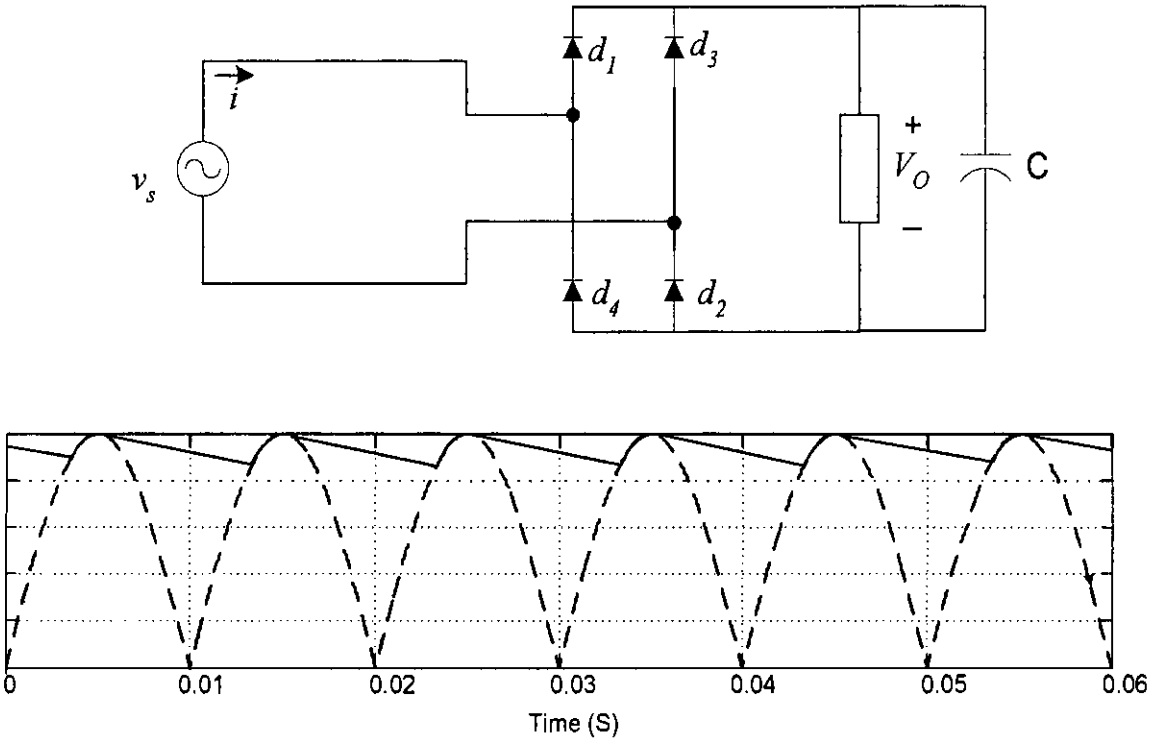


Figure 2.2: Rectifier with filter capacitor and output voltage (firm line)

Although a filter capacitor significantly reduces the ripple from the output voltage, it introduces distortion in the input current waveform. During the positive cycle of the input signal diode d_1 and d_2 conducts, supplies the load and charges the capacitor. The capacitor is charged up to the maximum value of input voltage (V_m). This causes d_1 and d_2 to be reverse biased. Since the other diodes (d_3 and d_4) are also reverse biased, the load gets disconnected from the supply voltage and the rectifier ceases to draw any input current. The charge stored in the capacitor discharges through the load. In the negative cycle diodes d_1 and d_2 are naturally reverse biased. However, unlike in the case of a rectifier without filter capacitor, diode d_3 and d_4 also remain reverse biased due to the stored charge in the capacitor until discharging of the capacitor brings the output voltage below the instantaneous amplitude of input voltage. The capacitor is then again charged to V_m and the diodes (d_3 and d_4) again are reverse biased, causing the input current to cease again. So the rectifier draws input current only for a brief period of time when the capacitor is charged either through diodes d_1, d_2 (during positive half cycle)or diodes d_3, d_4(during negative half cycle). This results in a distortion in the input current drawn by the rectifier as shown in figure 2.3.

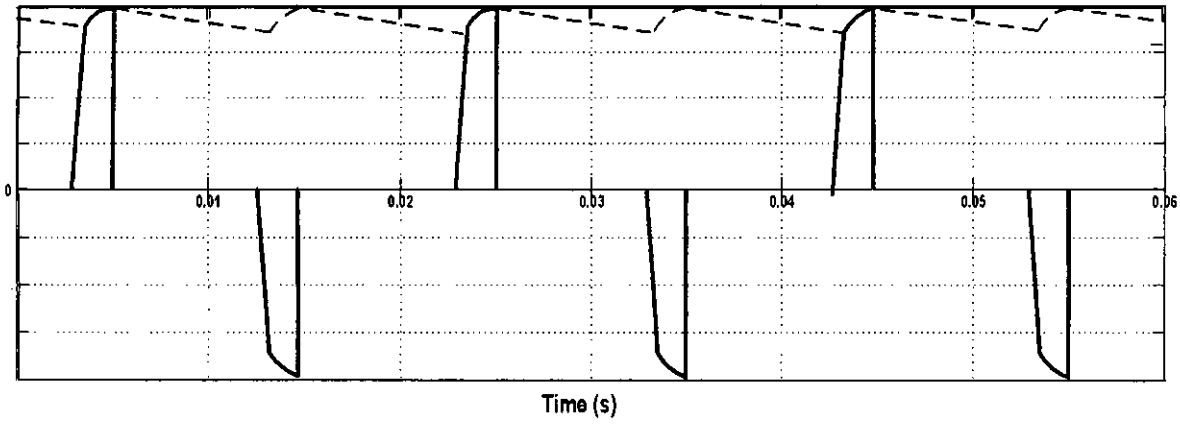


Figure 2.3: Input current drawn by a bridge rectifier with filter capacitor along with output voltage (dotted)

2.3 Analysis of Bridge Rectifier circuit with filter capacitor:

The pulsating nature of the output voltage produced by the rectifier circuits is not suitable as a dc supply for electronic circuits and therefore is suppressed by placing a capacitor

across the load resistor. Figure 3 shows the steady-state input and output voltage waveforms under the assumption that the time constant (C×R) is much greater compared to the period (T) of the input voltage signal. The waveforms of the load current is given by

$$i_L = \frac{v_0}{R} \tag{2.1}$$

The input current (i_D) drawn by the rectifier through the diodes when either of the two sets of diodes ($d_{1,2}$ or $d_{3,4}$) conduct is given by

$$\begin{aligned} i_D &= i_C + i_L \\ &= C\frac{dv_1}{dt} + i_L \end{aligned} \tag{2.2}$$

where, i_C and i_L are the currents through capacitor and load resistor respectively, v_1 is the voltage across the capacitor.

Referring to the figure, followings are observed,

1. The diodes conduct for a brief interval. At near the peak of the input sinusoid and supply the capacitor with charge equal to that lost during the much longer discharge interval. The latter is approximately equal to the period T.
2. Assuming the diodes to be ideal, conduction period of d_1 and d_2 begins at time t_1, when the input voltage v_s equals the exponentially decaying output voltage v_o. Conduction stops at t_2, shortly after the peak of v_s. The exact value of t_2 can be found by setting i_D=0 in equation (2.2).
3. When none of the diodes conduct, the capacitor C discharges through R and thus v_o decays exponentially with the time constant (C×R). The discharge interval begins almost at the peak of v_s. At the end of the discharge interval, which lasts for almost the half of the period, v_o=V_P-V_r, where, V_r is the peak to peak ripple voltage. For time constant much bigger than the period, V_r is very small.

4. When V_r is small, v_o is almost constant and equal to the peak value of v_s. Thus the dc output voltage is approximately equal to V_P. Similarly, the current i_L is almost constant and its dc component is given by

$$i_L = \frac{V_P}{R} \tag{2.3}$$

a more accurate expression for the output dc voltage can be obtained by taking average of the extreme values of v_o [25],

$$V_o = V_P - \frac{1}{2}V_r \tag{2.4}$$

With these observations in hand, expressions for V_r and the average and peak values of the input current (i.e. the diode current) can be derived. During the diode-off interval when the load is disconnected from the supply, v_o can be expressed as,

$$v_o = V_P e^{-t/CR} \tag{2.5}$$

At the end of the discharge interval,

$$V_P - V_r \cong V_P e^{-T/2/CR} \tag{2.6}$$

Since CR>>T, using the approximation $e^{-T/CR} \cong 1 - T/CR$ following expressions can be obtained,

$$V_r \cong V_P \frac{T/2}{CR} \tag{2.7}$$

It is observed that to keep V_r small a capacitance C should be selected so that CR>>T. The ripple voltage V_r in equation (7) can be expressed in terms of the frequency f = 1/T as,

$$V_r = V_P \frac{1}{2fCR} \tag{2.8}$$

An alternative interpretation of the approximation made above is that the capacitor discharges by means of a constant current $I_L = V_P/R$. However, this approximation is valid

as long as $V_r << V_P$. Assuming that diode conduction ceases almost at the peak of v_s (?), we can determine conduction interval Δt from the following condition

$$V_P \cos(\omega \Delta t) = V_P - V_r$$

where, ω is the angular frequency of input voltage. Since $(\omega \Delta t)$ is a very small angle we can employ the approximation

$$\cos(\omega \Delta t) \cong 1 - \tfrac{1}{2}(\omega \Delta t)^2$$

and obtain

$$\omega \Delta t \cong \sqrt{2 \frac{V_r}{V_P}} \qquad (2.9)$$

When $V_r << V_P$, conduction angle $\omega \Delta t$ will be small as well.

To determine the average diode current during conduction, i_{Dav}, we relate the charge that is supplied to the filter capacitor through the conducting diodes as follows,

$$Q_{supplied} = i_{Cav} \Delta t \qquad (2.10)$$

Here, i_{Cav} is the time averaged value of current flowing through the capacitor. The charge that the capacitor loses during the discharge interval is,

$$Q_{lost} = C V_r \qquad (2.11)$$

By equating charge spplied to the capacitor to the charge lost by it, the average value of input current can be obtained as,

$$i_{Dav} = I_L (1 + \pi \sqrt{\frac{V_P}{2V_r}}) \qquad (2.12)$$

When , $V_r << V_P$, the average diode current during conduction is much greater than the dc load current. This is because the diode the diode conducts for a very short interval and must replenish the charge lost by the capacitor during the much longer interval during which it is discharged by I_L.

The peak value of the diode current, i_{Dmax} can be determined by evaluating the expression in equation (2) at the onset of diode conduction, i.e. at $t = t_1 = -\Delta t$ considering $t = 0$ is at

the peak). Assuming that i_L is almost constant at the value given by equation (3), we obtain

$$i_{D\max} = I_L(1+2\pi\sqrt{\frac{V_P}{2V_r}}) \qquad (2.13)$$

From equation (12) and (13), we see that for $V_r << V_P$, $i_{Dmax} \approx 2i_{Dav}$, which reveals the fact that the waveform of i_D is almost a right-angle triangle.

From the above analysis it is quite evident that the input current drawn by a full wave bridge rectifier with filter capacitor is neither sinusoidal nor continuous (eqn 2.13). The input current flows intermittently and therefore consists of low frequency harmonics. The result is low power factor and increased loss in distribution conductors and transistors. Also the average value of input current has to be high (eqn. 2.12) as it flows for a much shorter period of time. This phenomenon necessitates the use of devices with higher current ratings which in turn increases the size and cost.

2.4 Filtering input current:

Use of filter capacitor to suppress the ripple in the output voltage wave form distorts the input current wave drawn by the rectifier. To reduce the input current harmonics an *ac filter* is used [26]. The filter is normally consisted of a LC network as shown in Figure 2.4. Normally, the filter design requires determining the magnitudes and frequency of the harmonics.

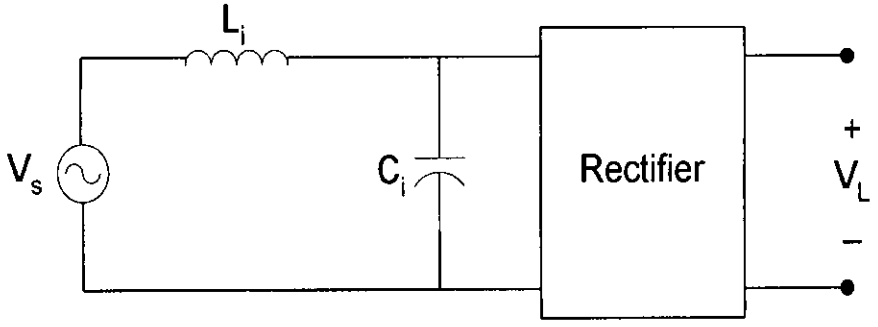


Figure 2.4: Rectifier with input AC filter

Though the LC filter on the input side reduces the harmonic content of input current to some extent, it may introduces a phase shift between input current and line voltage. Such phase displacement requires the use of source and distribution equipments (like transformers) with higher with higher volt-ampere ratings in order to handle reactive power.

CHAPTER 3

Scheme for Reducing Input Current Harmonics and Improving Power Factor

3.1 Introduction

This chapter presents the scheme developed for reducing the distortion in input current drawn by a single-phase rectifier, along with improvement of input power factor. As demonstrated in previous chapter, a rectifier with filter capacitor draws current intermittently. Such discontinuity causes generation of several low frequency harmonics that reduces the efficiency of the rectifier considerably. An electronic switching circuit has been developed in order to ensure the continuity of the input current. The switch provides a path for the input current to flow when the supply is disconnected from the load due to the reverse biasing of all four diodes of the rectifier. The switch, on the other hand, is deactivated or open circuited when the rectifier normally draws current from the supply while charging the filter capacitor. The scheme uses a series combination of inductor and capacitor in series with supply in order to improve power factor. In this chapter, the development of the switching scheme is first presented, followed by derivation for the expression of input current. It has been shown analytically that with the proposed switching scheme, rectifier draws sinusoidal input current with almost no phase difference with supply voltage.

3.2 The Proposed Scheme

The input current drawn by a single phase rectifier with filter capacitor is shown in Figure 3.1, along with the supply and output voltage. The figure shows that current is drawn by the rectifier only for two brief intervals of time in each cycle of supply voltage. A conceptual demonstration of the scheme designed for making the current continuous we propose the following scheme shown in Figure 3.2. The switch (S) being ON or closed, provides an alternative path when all the diodes (d_1 to d_4) are reverse biased and

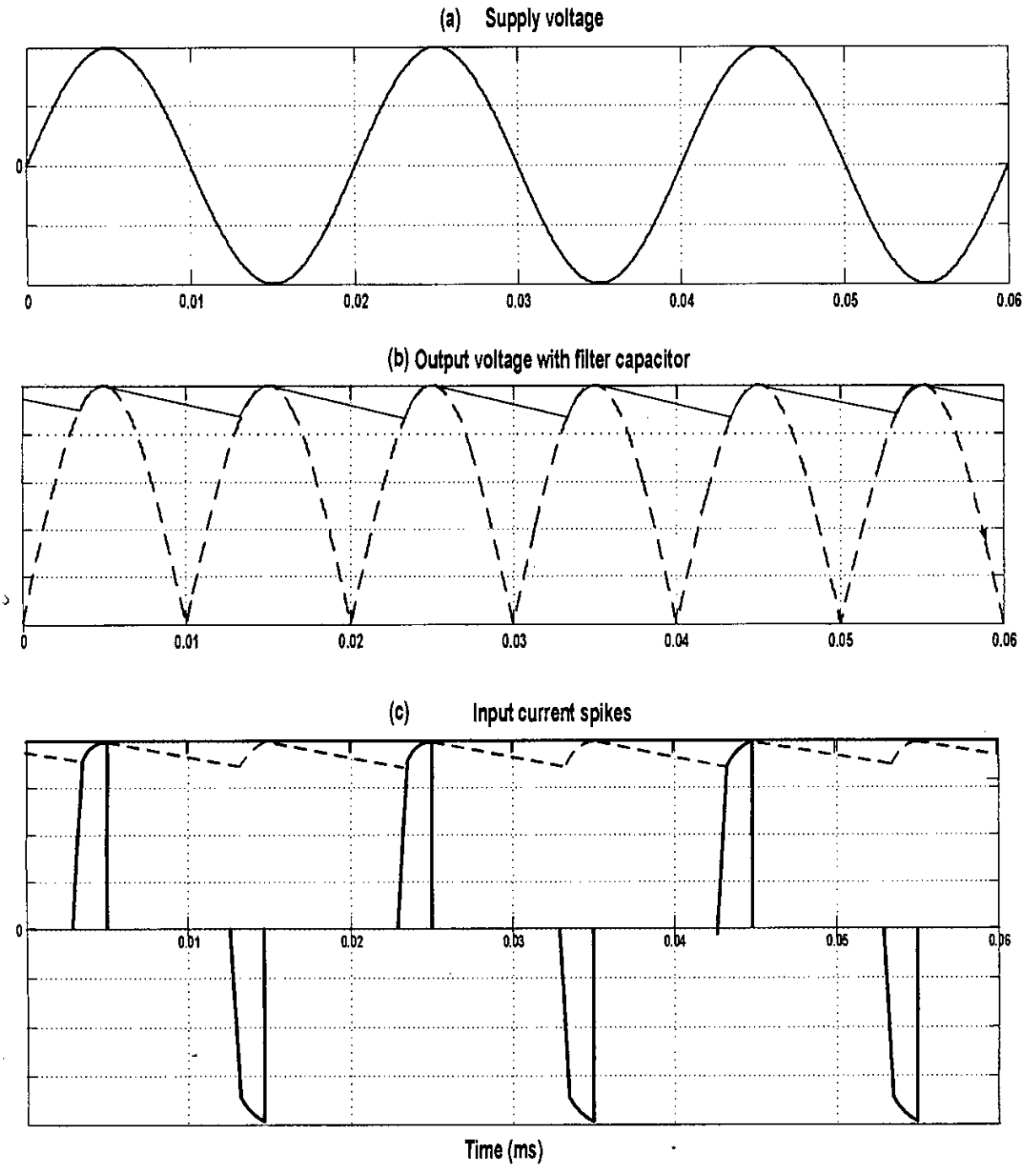


Figure 3.1: (a) supply voltage V_S, (b) output voltage with filter capacitor (firm line) and without filter (dashed lines), and (c) input current spikes (firm line) and output voltage with filter capacitor (dashed lines).

the load is disconnected from the main supply. Since input current flows when the supply voltage approaches it's maximum value (positive or negative), the switch should be triggered off during that period. For the rest of the periods, the switch should be turned ON and OFF with continuously varying duty cycle. The variation of duty cycle of switching (the ratio between ON to total period) should be smoothly varying, starting with maximum ON period and reaching to minimum ON period as the supply voltage sweeps through its zero to maximum values. The ON time initially should be high to ensure the increase of input current to a reasonable value, so that during smaller OFF period the current does not fall appreciably and thus remains smooth. As the supply voltage increases, the ON period should decrease accordingly to prevent the input current

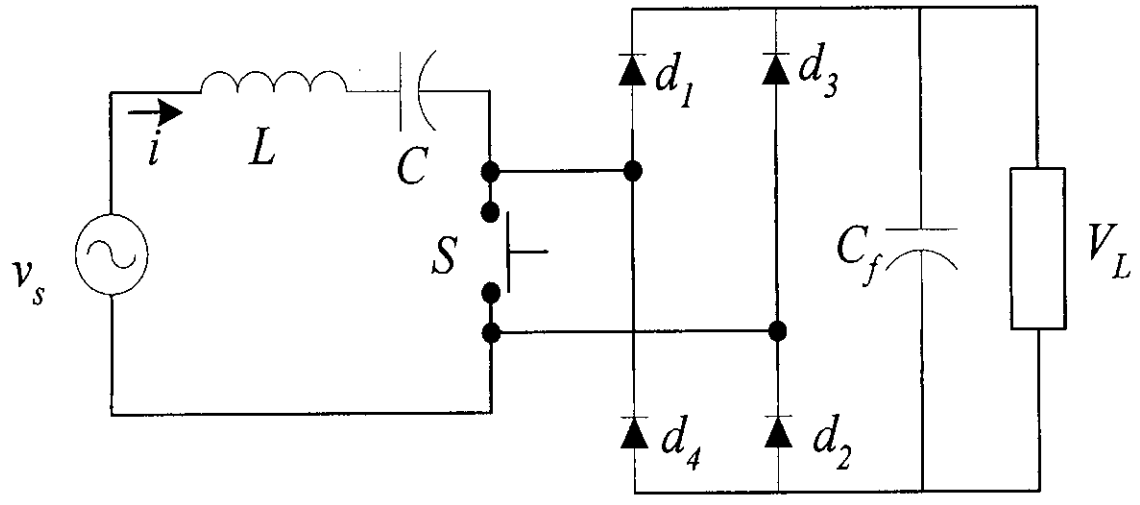


Figure 3.2: A bridge rectifier with an ac side switch

from rising indefinitely and also to allow sufficient time to fall accordingly during the OFF period. This concept reveals that the duty cycle of the switching should be varied like a rectified *cosine* function, as shown in Figure 3.3 with a frequency twice of the supply. The inductor (L) connected in series with the supply makes the current smoother by eliminating any sharp variation that may exist. However, the inductance value required for this purpose may become very large. As a result a significant portion of supply voltage would be dropped across the inductor and available output voltage would be unacceptably low.

Although with the switching scheme outlined above, the current is expected to be smoother and sinusoidal, low voltage has to be taken care of also. Moreover, the phase difference between input current and supply voltage in this case would be also unacceptable. Therefore a capacitor (C) has been connected in series with L to keep the current in phase with the supply voltage. The value of L and C are adjusted to produce a series resonance at supply frequency. This produces a selectivity due to which only the

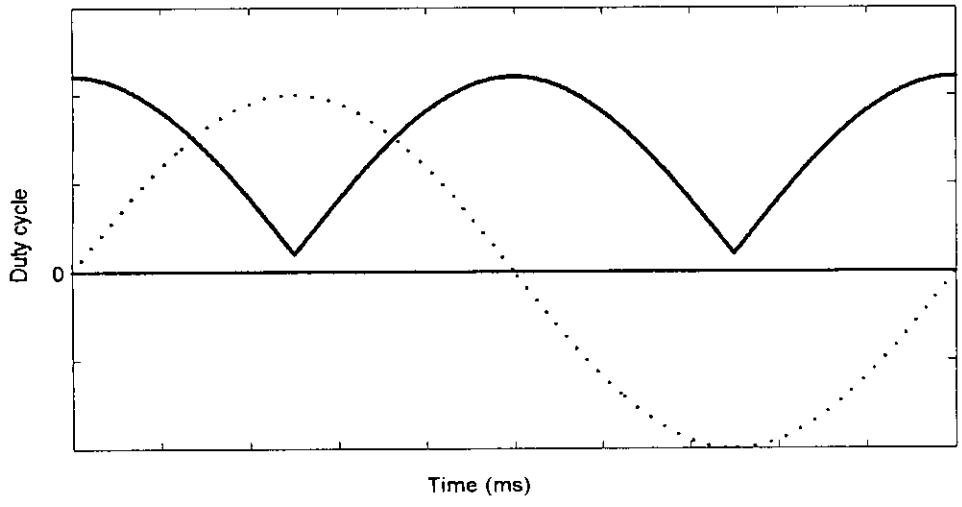


Figure 3.3: variation of duty cycle (firm line) along with supply voltage (dotted)

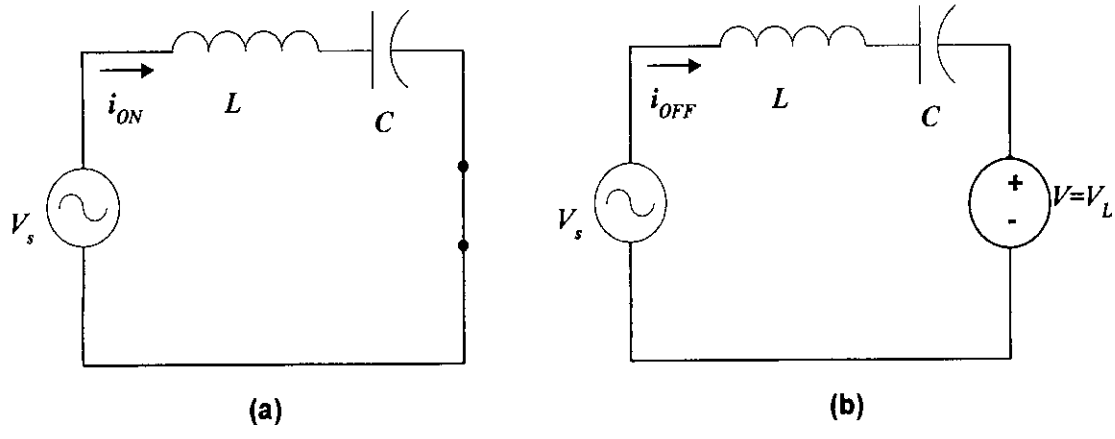


Figure 3.4: Equivalent circuits for ON state (a) and OFF state (b) of the switch S.

fundamental frequency component of the input current can flow unimpeded. The results presented in the next chapter will clearly reveal the efficacy of the switching scheme and the series combination of L and C in obtaining a sinusoidal input current with acceptably low harmonic distortion.

3.3 Analysis of the Proposed Scheme:

First the proposed scheme is analyzed with an ideal switch. The total scheme consisting of the ideal switch and the circuit arrangement for generating triggering pulses for the switch is shown in Figure 3.2. The switch is assumed to be capable of carrying current in both directions, which is essential because of desired sinusoidal nature of input current. As any ideal switch, it is assumed to be short circuited during it's ON period and open circuited during OFF period. The circuit shown in figure 3.2 can be approximated with the following circuits, as shown in Figures 3.4 with V=0 for the switch ON condition and V= V_L (load voltage) for the OFF condition. Since the switching frequency is much higher compared to that of supply, the source voltage can be considered to remain constant during any particular switching period. The supply voltage, V_S during any switching interval can be written as:

$$V_S = L\frac{di}{d\tau} + \frac{1}{C}\int_0^{\tau} i\,dt + V_C(0) + V \qquad (3.1)$$

where i is the input current, $V_c(0)$ is the initial voltage across C for the concerned switching period and τ is the time variable within the switching interval. V_S is the supply voltage at the beginning of the interval and does not change appreciably during the switching period. V_S is given by :

$$V_S = V_m \sin \omega t \qquad (3.2)$$

where V_m is the magnitude and ω is the angular frequency of the supply and t is the time at which the concerned switching interval starts. According to this the supply voltage here is actually approximated by a stair-case like sine wave as shown in Figure 3.5.
Using the Lapalce's transform equation (1) can be written as:

$$\frac{V_S}{s} = LsI(s) - LI(0) + \frac{I(s)}{Cs} + \frac{V_C(0)}{s} \tag{3.3}$$

or, $$I(s) = \frac{V_S - V_C(0) - V}{s^2LC + 1}C + \frac{LI(0)}{s^2LC + 1}sC \tag{3.4}$$

Here $I(0)$ is the initial current through the inductor L. Relating LC to their series resonating frequency by $\omega_m^2 = 1/(LC)$,

$$\begin{aligned} \mathrm{I(s)} &= \frac{V_S - V_C(0) - V}{L(s^2 + \omega_m^{\,2})} + \frac{sI(0)}{s^2 + \omega_m^{\,2}} \\ or, I(s) &= [V_S - V_C(0) - V]\sqrt{\frac{C}{L}}\frac{\omega_m}{s^2 + \omega_m^{\,2}} + I(0)\frac{s}{s^2 + \omega_m^{\,2}} \end{aligned} \tag{3.5}$$

The value of current in time domain as a function of τ can be obtained by inverse Laplace transform of equation 5:

$$i(\tau) = [V_S - V_C(0) - V]\sqrt{\frac{C}{L}}\sin\omega_m\tau + I(0)\cos\omega_m\tau \tag{3.6}$$

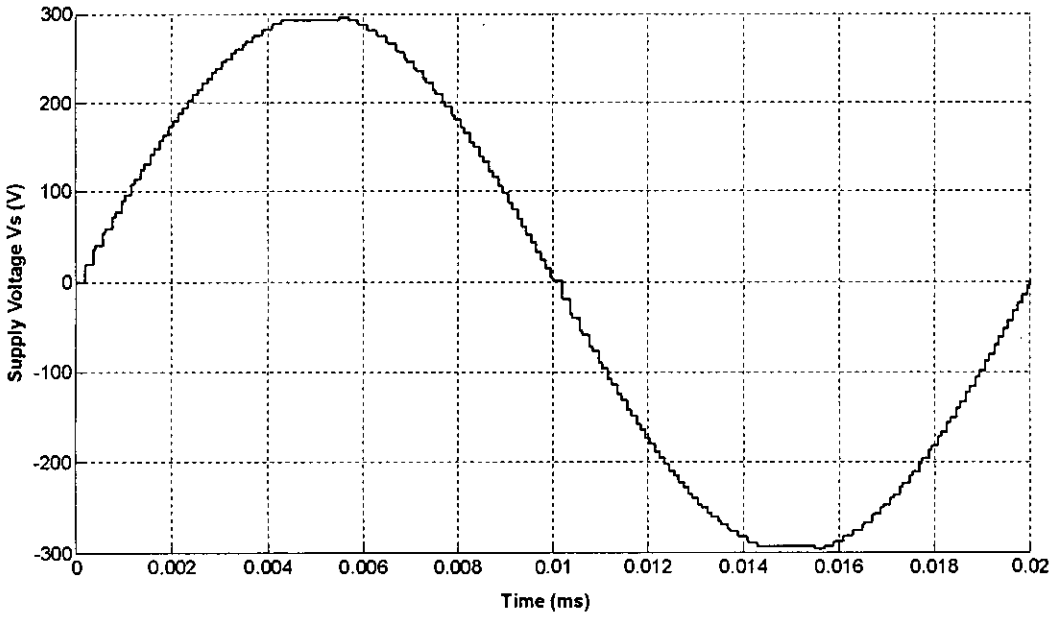


Figure 3.5: Wave Shape of V_S used for analysis. Note that the step size is varied over the time according to the variation of duty cycle variation of the switch.

Because of the fact that the usual switching frequency is very high compared to that of supply, $\omega_m\tau$ is likely to be very small and therefore $\sin(\omega_m\tau)$ and $\cos(\omega_m\tau)$ can be approximated by $\omega_m\,\tau$ and 1 respectively. So

$$i(\tau) = [V_S - V_C(0) - V]\sqrt{\frac{C}{L}}\omega_m\tau + I(0) \qquad (3.7)$$

Equation (7) gives the general expression for the input current during any switching interval. The expressions for the input current when the switch is ON and OFF respectively can be separated as follows:

$$i_{ON}(\tau) = [V_m \sin \omega t_n - V_{C,ON}(0)]\sqrt{\frac{C}{L}}\omega_m\tau + I_{ON}(0), \text{ for } 0<\tau<DT_S \qquad (3.8)$$

where t_n is the time at which the switching interval starts, $V_{C,ON}$ (0) and I_{ON}(0) are the initial voltage across C and current through L at the beginning of ON time of the switch i.e. at $t=t_n$, D is the duty cycle and T_S is the switching period. Similarly during the OFF period of switch:

$$i_{OFF}(\tau) = [V_m \sin(\omega t_n + DT_S) - V_{C,OFF}(0) - V]\sqrt{\frac{C}{L}}\omega_m\tau + I_{OFF}(0),$$

$$\text{for } 0<\tau<(1-D)T_S \qquad (3.9)$$

Here $V_{C,OFF}$ (0) and I_{OFF}(0) are the initial voltage across C and current through L at the beginning of OFF time of the switch i.e. at $t=t_n+DT_S$. It is quite evident that in order to make the input current sinusoidal, the amount of change in input current in every period should be varying like a cosine wave. The change in current (Δi) over a switching period can be found from equations (8) and (9):

$$\Delta i = i_{OFF}\big|_{\tau=(1-D)T_S} - i_{ON}\big|_{\tau=0}$$

$$= [V_m \sin(\omega t_n + DT_S) - V_{C,OFF}(0) - V]\sqrt{\frac{C}{L}}\omega_m(1-D)T_S + I_{OFF}(0) - I_{ON}(0)$$

$$(3.10)$$

From equation (10) it is quite evident that the duty cycle should vary like a cosine wave.

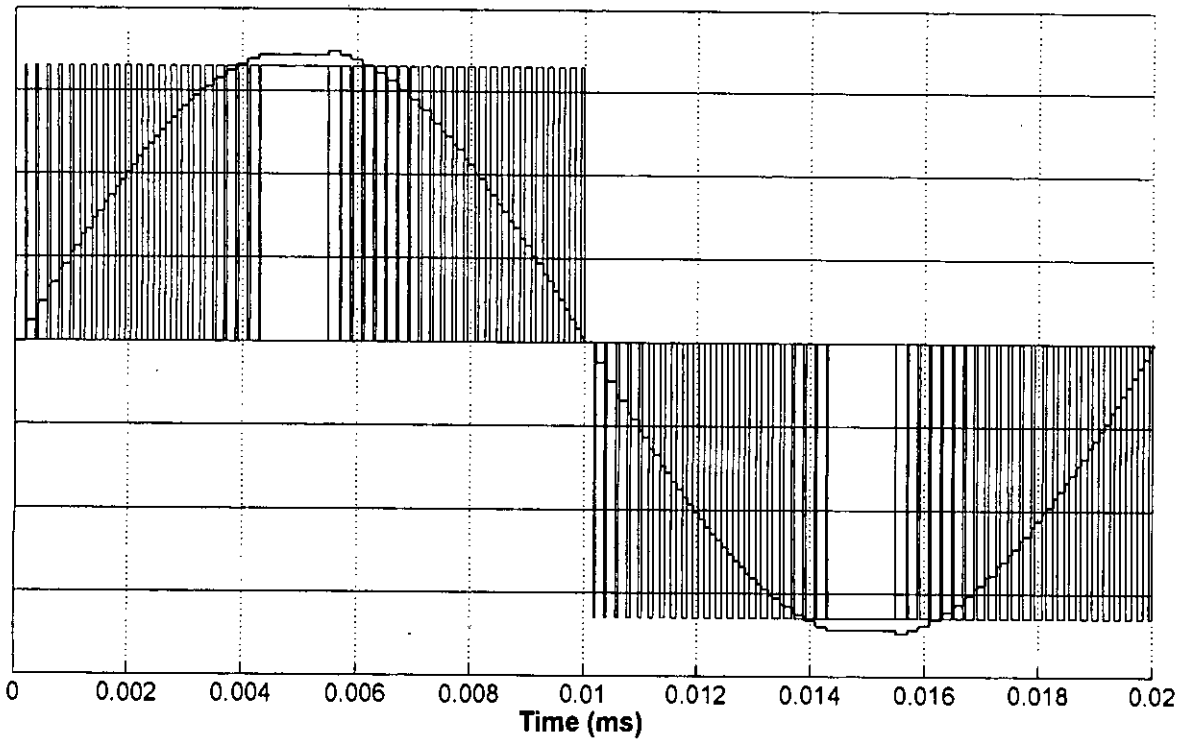


Figure 3.6: The voltage across the switch as it turns ON and OFF, along with the V_S variation. The high voltage across the switch refers to its OFF state and zero volt state refers to its ON state. Note that the ON state is initially longer and gradually decreases as V_S approaches its positive or negative maxima.

3.4 Input Current Wave shape:

Figure 3.6 shows the pulsating voltage across the switch. Duty cycles of the pulses are varying smoothly as a cosine function. The current (i) at steady state has been calculated using the concept presented in the previous section for a given value of supply and load voltage. The calculated current wave shape is shown in Figure 3.6 along with the normalized supply voltage wave. The current wave is almost sinusoidal and is the phase shift with the voltage is also negligible. This confirms the validity of the presented switching concept.

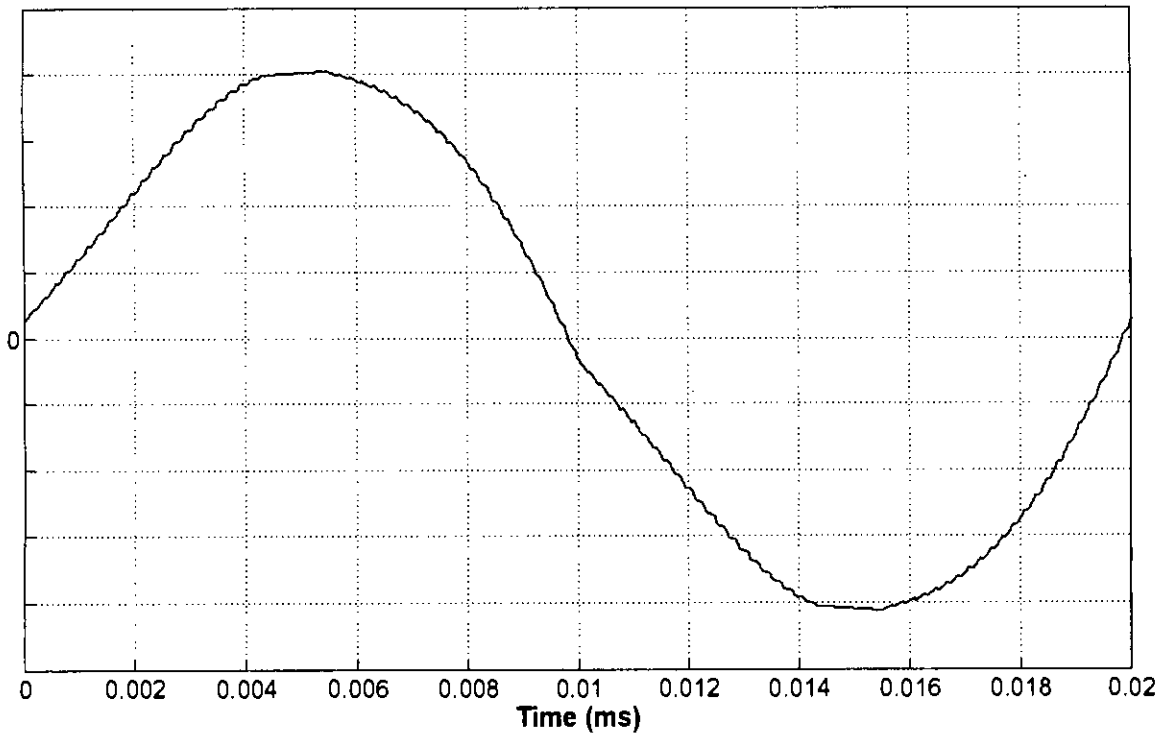


Figure 3.7: Variation of calculated input current The input current is almost sinusoidal

3.5 Conclusion

The discontinuous nature of input current drawn by a rectifier with filter capacitor has been investigated. It has been shown analytically that the discontinuity can be eliminated by employing a solid state switch along with a series inductor-capacitor resonant circuit at the input side. The switching frequency should be much higher than the supply voltage frequency. The duty cycle of the triggering pulses for the switch should be a cosine function with frequency double of the supply frequency. The calculated input current is found to be nearly sinusoidal and almost in phase with the supply voltage. In the following chapter the development of this conceptual scheme will be described along with the simulated results obtained.

CHAPTER 4

Input Side Switching Scheme of a Rectifier

4.1 Introduction:

The Performance of the scheme proposed in chapter 3 has been analyzed in this chapter through simulation. The results have been presented in order to reveal the justifications outlined in previous chapter in designing the proposed scheme. The capacitor connected in parallel to the dc load makes the current discontinuous. As already explained, such discontinuity introduces lots of problems including lower power factor. The objective of the proposed scheme has been to make the input current continuous and at the same time keep it in phase with the input voltage to make the power factor unity. For this a switching scheme has been developed which provides alternative path for the input current when the supply is disconnected from the load. The inductor connected in series with the supply voltage at the input side ensures continuity of the current through different switching intervals. To eliminate higher order harmonics and to reduce the phase shift between input voltage and current, a capacitor has been connected in series such that the resonating frequency of the LC filter equals supply frequency.

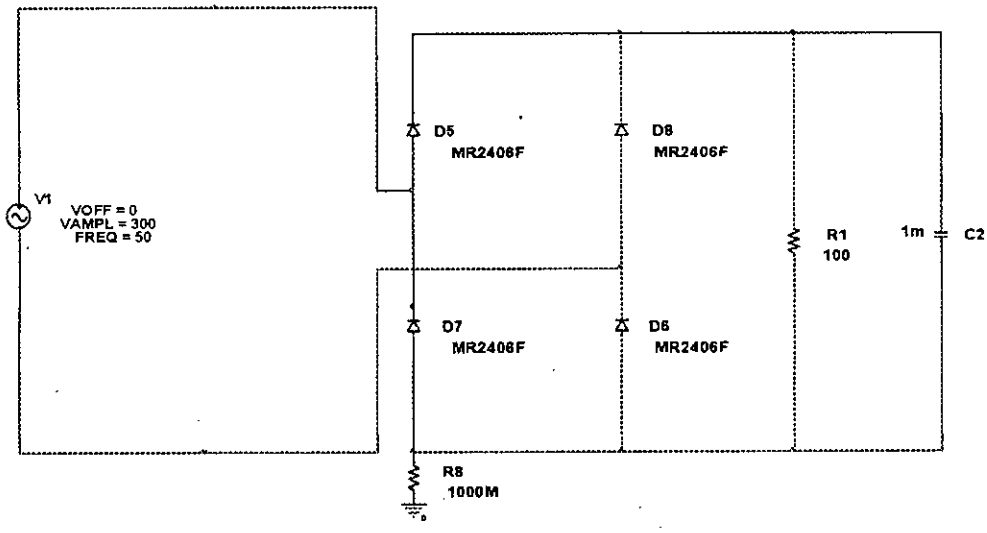


Figure 4.1: A rectifier circuit with output filter capacitor

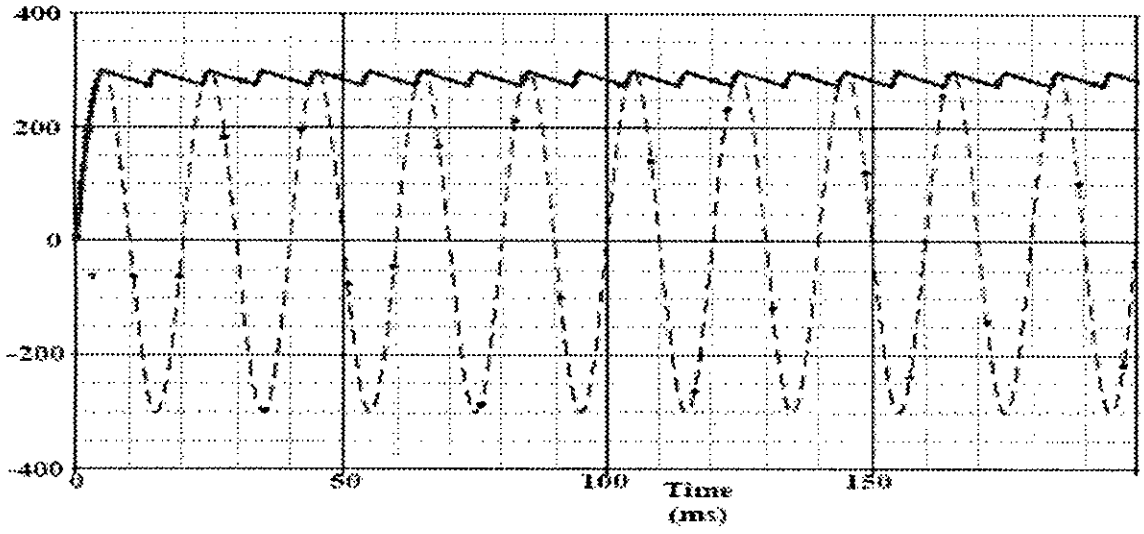


Figure 4.2: Output voltage (firm line) and supply voltage (dotted) of a typical rectifier (shown in fig4.1) with load resistor R_L =100Ω and filter capacitor C_2=1 mF.

4.2 Rectifier with output filter capacitor

Figure 4.2 shows the simulated wave shapes of input and output voltage of a typical rectifier with a 100Ω pure resistive load and 1mF filter capacitor, shown in figure 4.1. The simulated input current drawn by such a rectifier is shown in figure 4.2. As was explained in previous chapters, it is found that input current flows only for a brief period in each half cycle of a 50 Hz supply voltage.

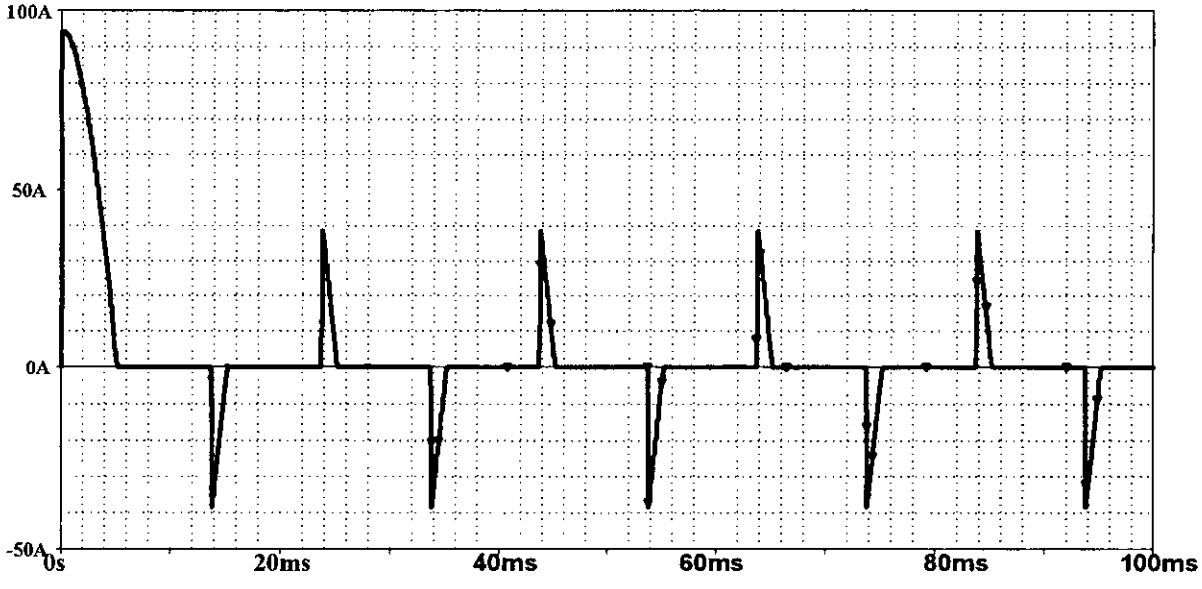


Figure 4.3: Input current drawn by the rectifier shown in fig 4.1

Harmonic contents of the input current are shown in figure 4.4 and it is clearly revealed that such discontinuous input current is totally unacceptable.

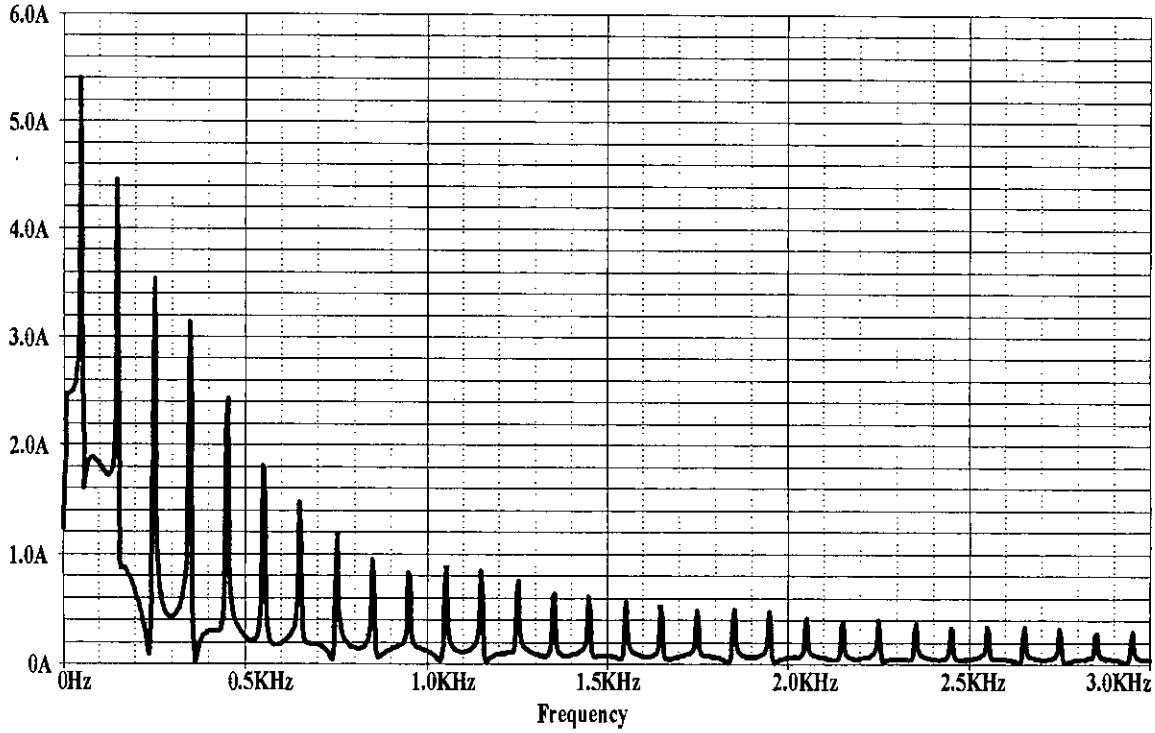


Figure 4.4: Harmonic contents of input current drawn by the rectifier shown in fig 4.1

4.3 The Switching Scheme:

The objective of the switching scheme is to enhance the continuity of the input current by providing it an alternative path through closing an electronic switch. A MOSFET (IRF 840) has been used as the switch. The gate pulse to the MOSFET has been generated by a separate module. As has been already explained in chapter 3, the duty cycle of the gate pulse has been continuously varied over the period of the supply voltage. The rectifier circuit with AC side switching arrangement is shown in figure 4.5. Figure 4.6 shows the schematic diagram of the circuit used to generate the gate pulses with varying duty cycle.

When a gate pulse is provide, the MOSFET (M1) is short circuited and input current flows through D10 and D13 (during positive half cycle) or through D12 and D9. The four diodes (D9, D10, D12, D13) ensures that current always flows in the same direction

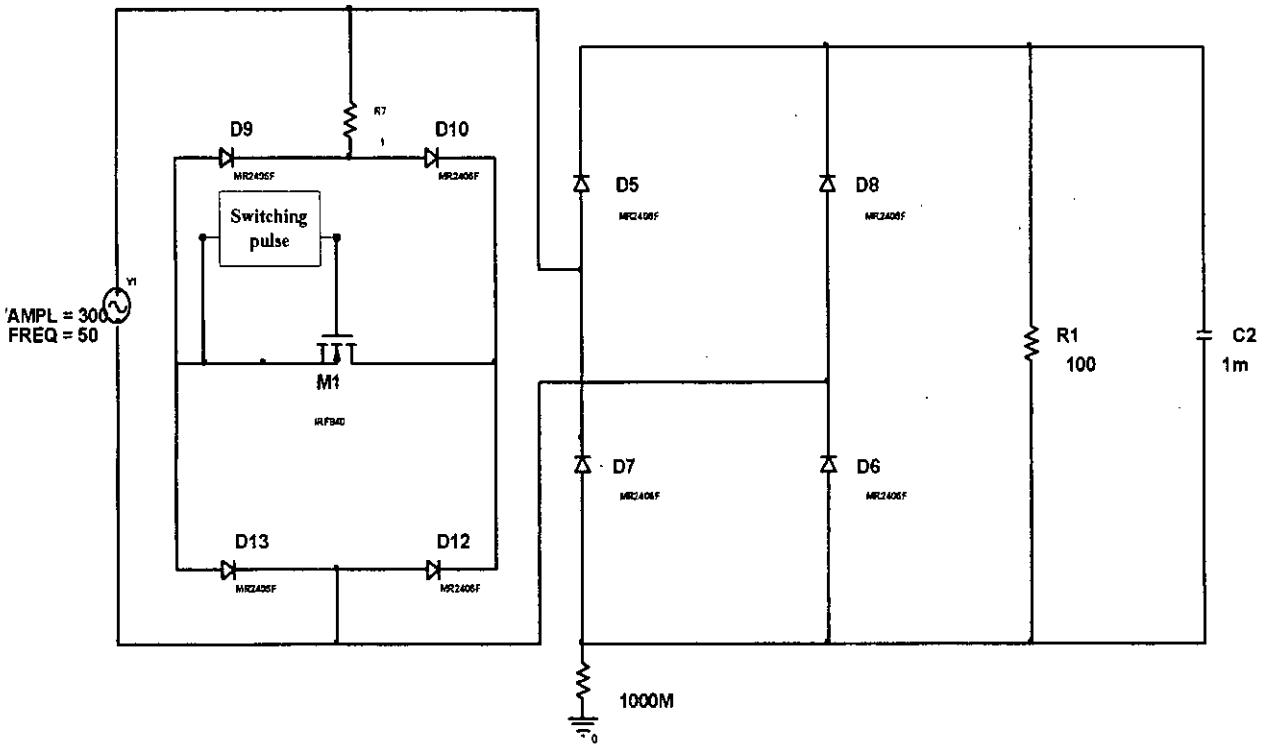


Figure 4.5: Rectifier circuit with AC side Switching

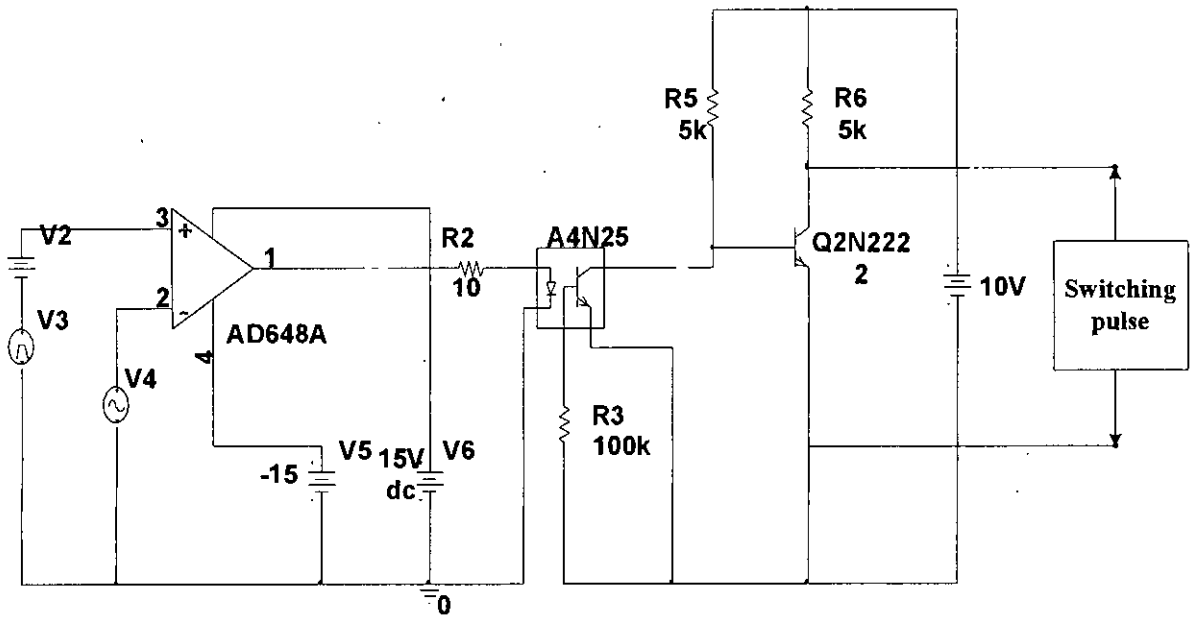


Figure 4.6: Switching module designed to generate gate pulse for M1 with continuously varying duty cycle.

through the MOSFET switch M1. The MOSFET switch is turned on when its gate to source voltage equals 10 volt.

The gate pulses have been generated by comparing a sinusoidal signal with a triangular signal, as shown in figure 4.7. The triangular wave signal and the sinusoidal signal are connected to the non-inverting and inverting terminals of an OP-AMP (AD 648A). As the input current naturally flows when the supply voltage reaches either positive or negative maxima, the duty cycle should be varied in such a way that the switch remains open during those periods. The duty cycle of the gating pulse should be maximum at the beginning of each cycle and gradually fall to minimum as the supply voltage approaches its maxima. This is required because to make it sinusoidal, the input current should increase at maximum rate at the beginning and at the minimum rate as the supply voltage approaches its minimum. This means that the duty cycle of the gate pulses should be varied like a cosine wave but with a frequency twice of the supply voltage frequency. Therefore the frequency of the triangular wave is also twice of the supply frequency, i.e. 100Hz. The frequency of the gate pulse is determined by the sinusoidal signal, which from now on will be referred as carrier signal. It has been found that a DC voltage should be added in series with the triangular one in order to produce desired gate pulse train. Since triangular wave represents a pulsating DC, it does not represent the pure DC as modulating signal (DC voltage is the desired output). Instead DC offset base rectified triangular wave has been chosen as a modulating signal so as to reduce the 100 Hz component from the high frequency modulated input current wave. Otherwise the input current will contain both the high frequency carrier and 100 Hz component. In figure 4.8, the gate pulses are generated by comparing 100Hz triangular with 1 kHz carrier (sinusoidal) signal. It is seen that, the duty cycle is smoothly varied over the supply voltage as shown in figure 3.3 of chapter 3. An opto-coupler (A4N25) has been used to provide necessary ground isolation between the switching module and the switch while producing the pulses.

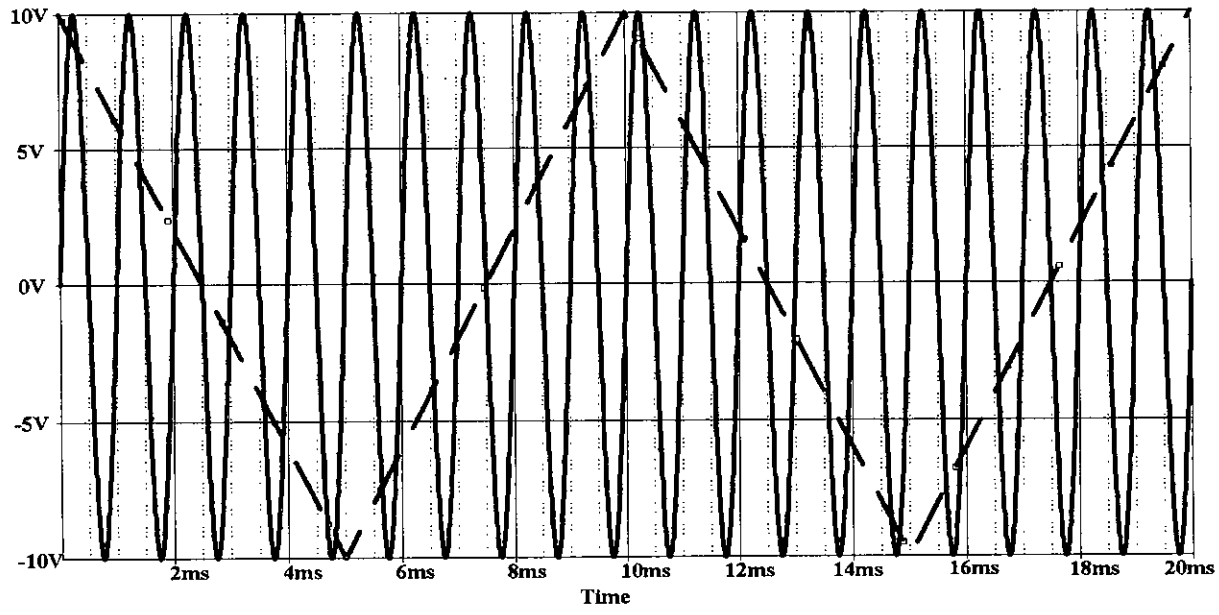


Figure 4.7: The 50 Hz triangular (dotted) and 1 kHz sinusoidal (firm) signals compared to produce gate pulses with continuously varying duty cycle.

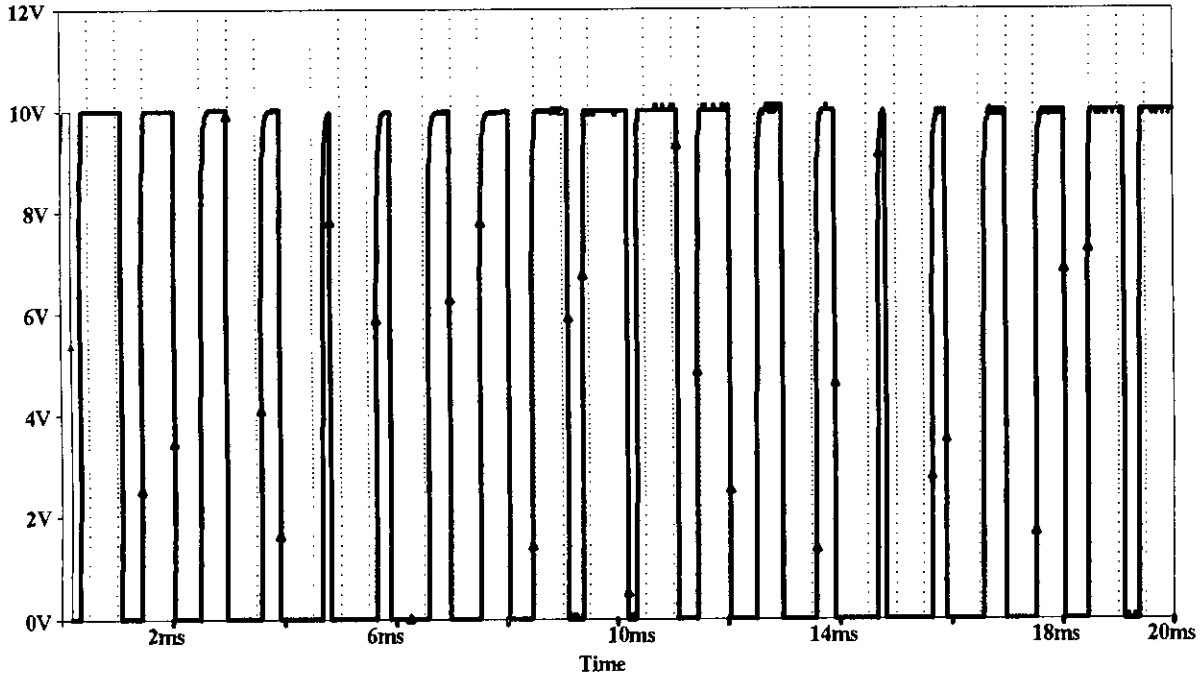


Figure 4.8: Gate pulses generated by comparing the signals shown in previous figure.

The waveshape and the Fourier Transform of simulated input current drawn by the rectifier with the gate pulses shown in fig 4.8 are documented in figures 4.9 and 4.10 respectively. In next two figures (figs 4.11 and 4.12), the simulated input current and it's Fourier Transform is shown for 5 kHz carrier or switching frequency are shown. From these figures it is evident that higher carrier frequency can reduce the low frequency harmonic contents to some extent. However it is also clear that the desired sinusoidal input current is not achievable with such switching alone even with very high frequency switching.

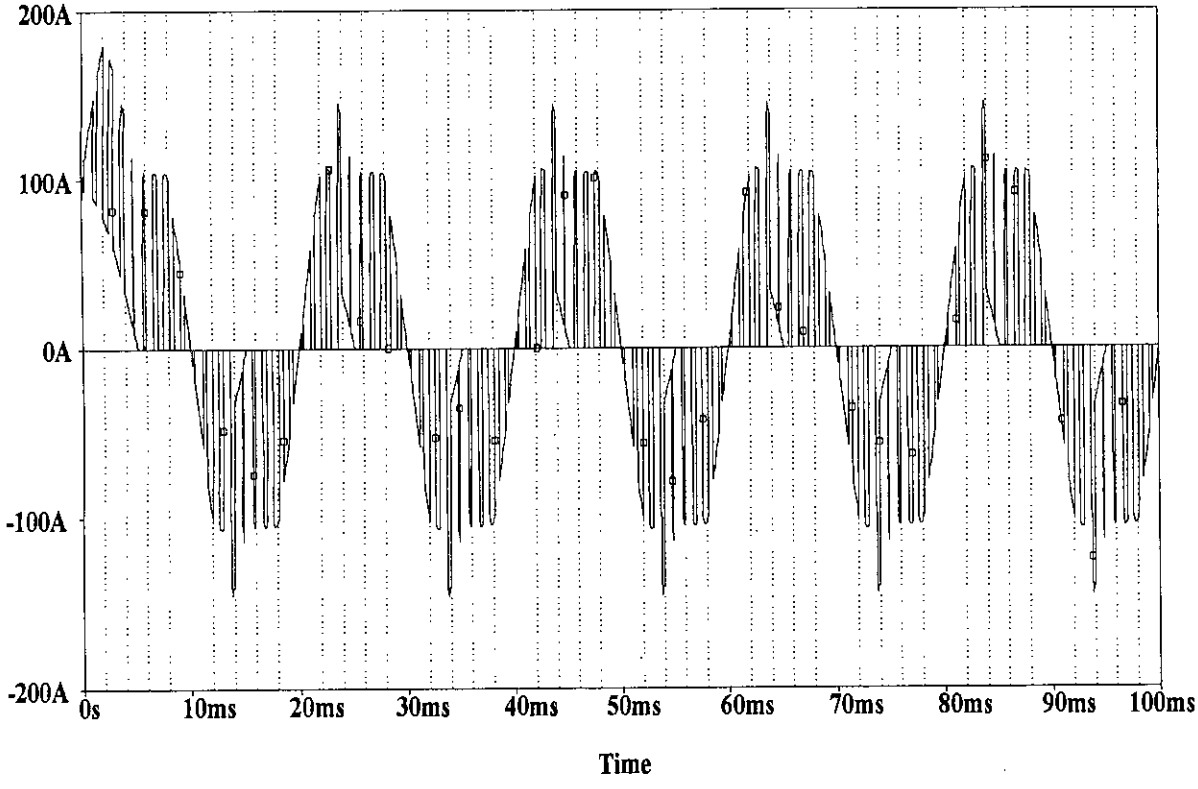


Figure 4.9: Input current obtained with 1 kHz gate pulse

4.4 Switching with input inductor

In order to make the input current observed with switching scheme described in the previous section continuous, an inductor is connected in series with the supply voltage, as shown in Figure 4.13. Since current flowing through an inductor cannot be changed instantaneously, it will prevent the current from falling to zero value when the switch is

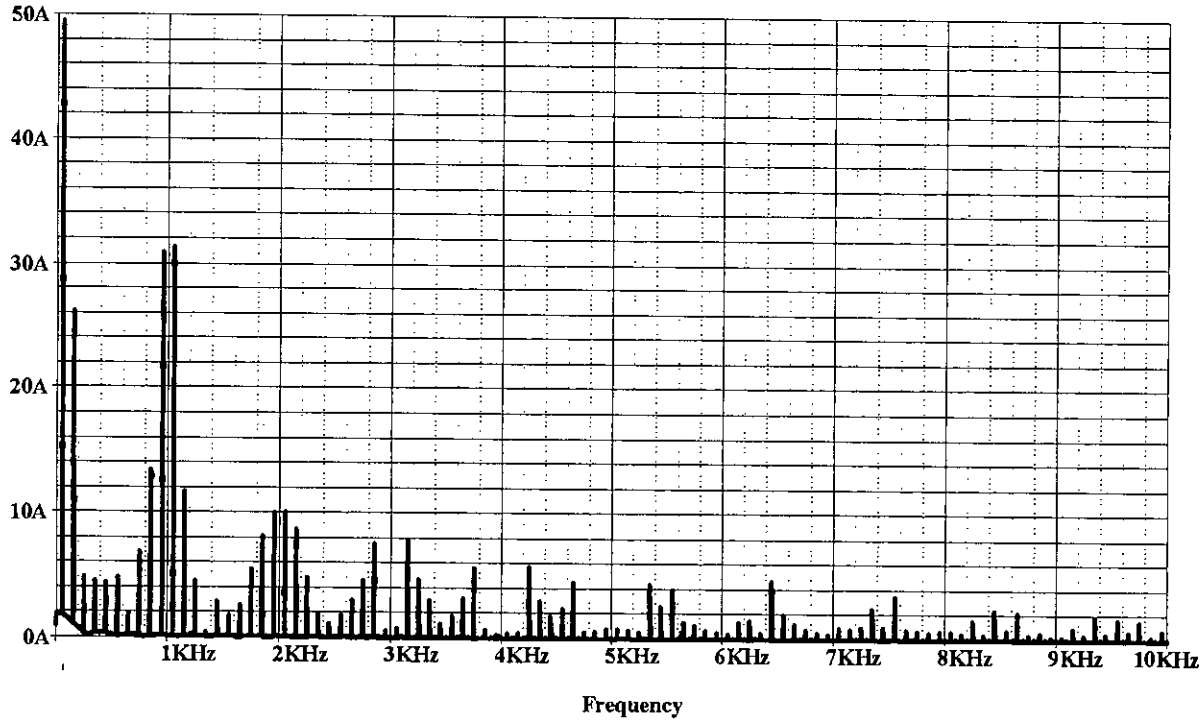


Figure 4.10: Fourier Transform of input current obtained with 1 kHz gate pulse

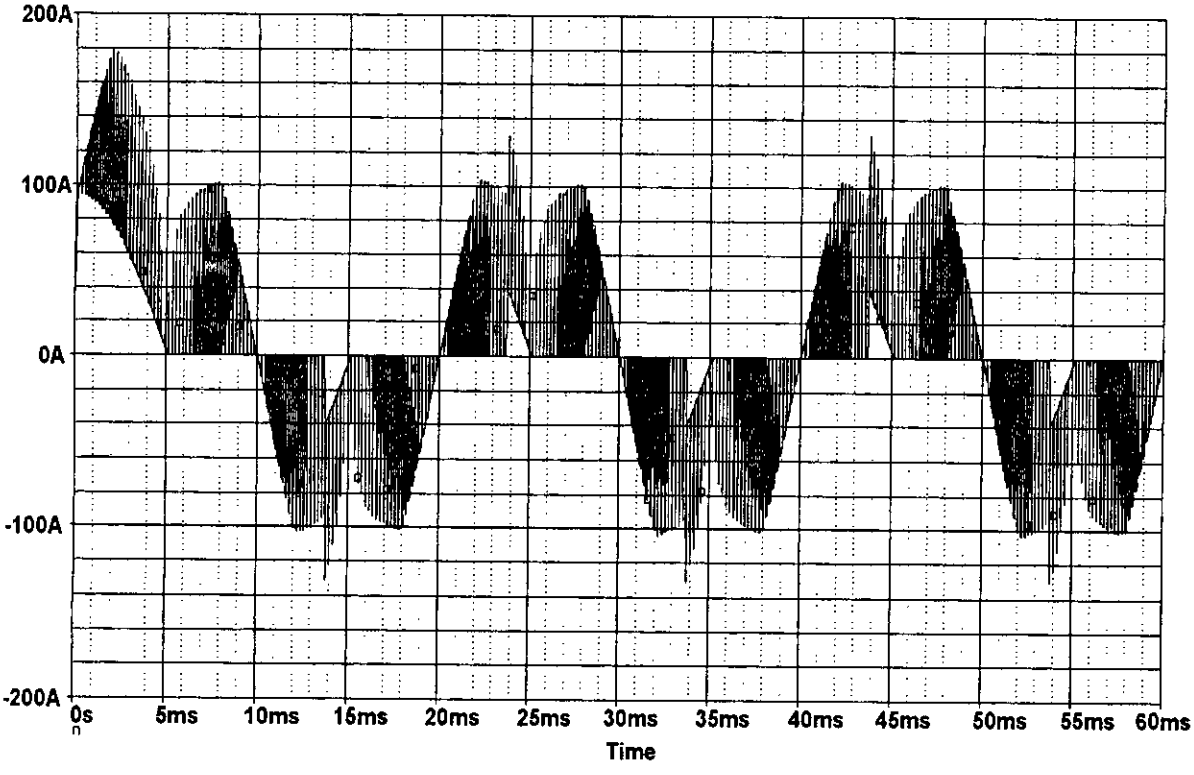


Figure 4.11: Input current obtained with 5 kHz gate pulse

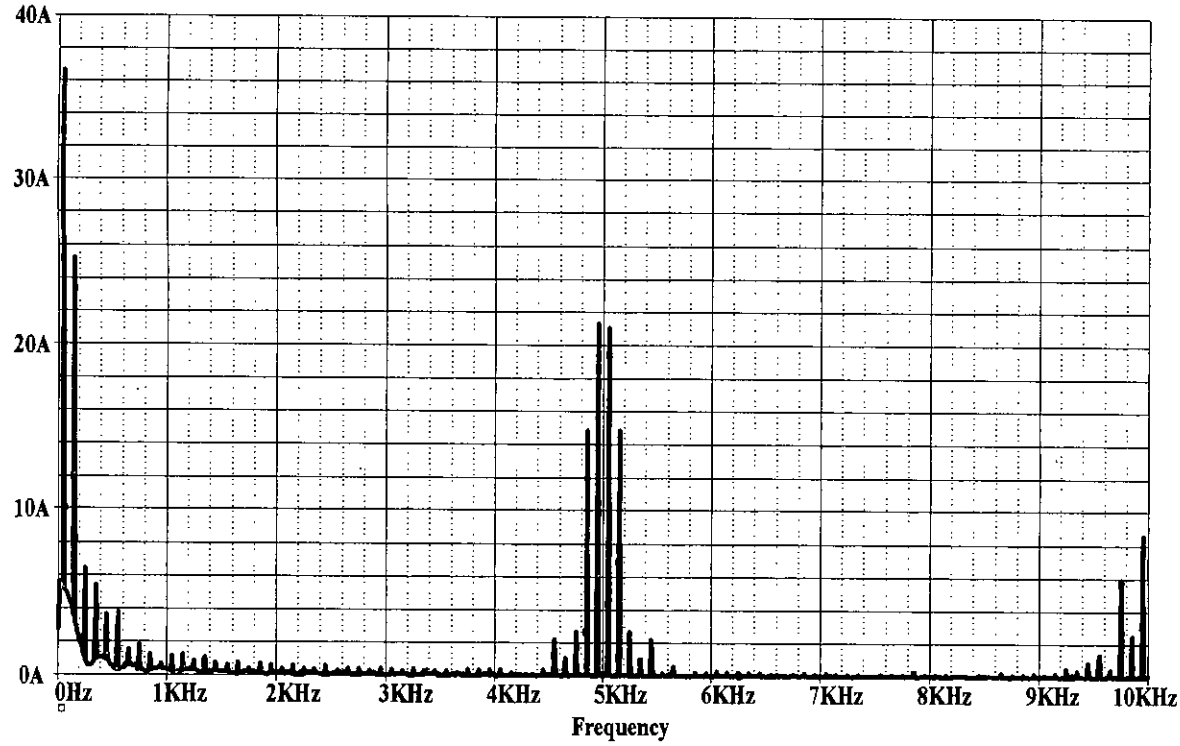


Figure 4.12: Fourier Transform of input current obtained with 5 kHz gate pulse

turned off. Instead such an input inductor is expected to keep the input current flowing during the intervals when the switch is open. The switching frequency then can be chosen in such way that the current can not fall to zero value. The variation of duty cycle over the period of supply voltage will then guide the input current to follow a sinusoidal form.

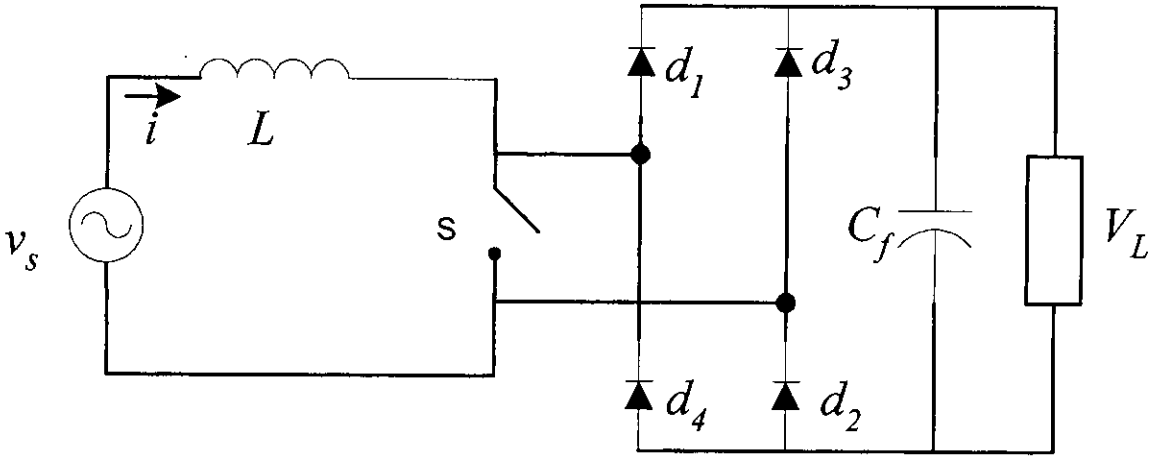


Figure 4.13: Rectifier circuit with input inductor (L) and switching (S).

To test this hypothesis, the circuit was first simulated with 10 mH and 100 mH inductors. In figure 4.14, the input currents and output voltages obtained with these two different input inductors are shown. The Fourier Transform of the input currents with 10 and 100mH are shown in figures 4.15 and 4.16. The total harmonic distortion (THD) can be calculated from these figures according to following expression:

$$THD = \frac{\sqrt{\sum_{h=2}^{h=\infty} (M_h)^2}}{M_1} \times 100\% \qquad (4.1)$$

Where M_h is the magnitude of either voltage or current harmonic component and M_1 is the magnitude of either the fundamental voltage or current. The THDs with 10 and 100mH are found to be 19% and 12% respectively.

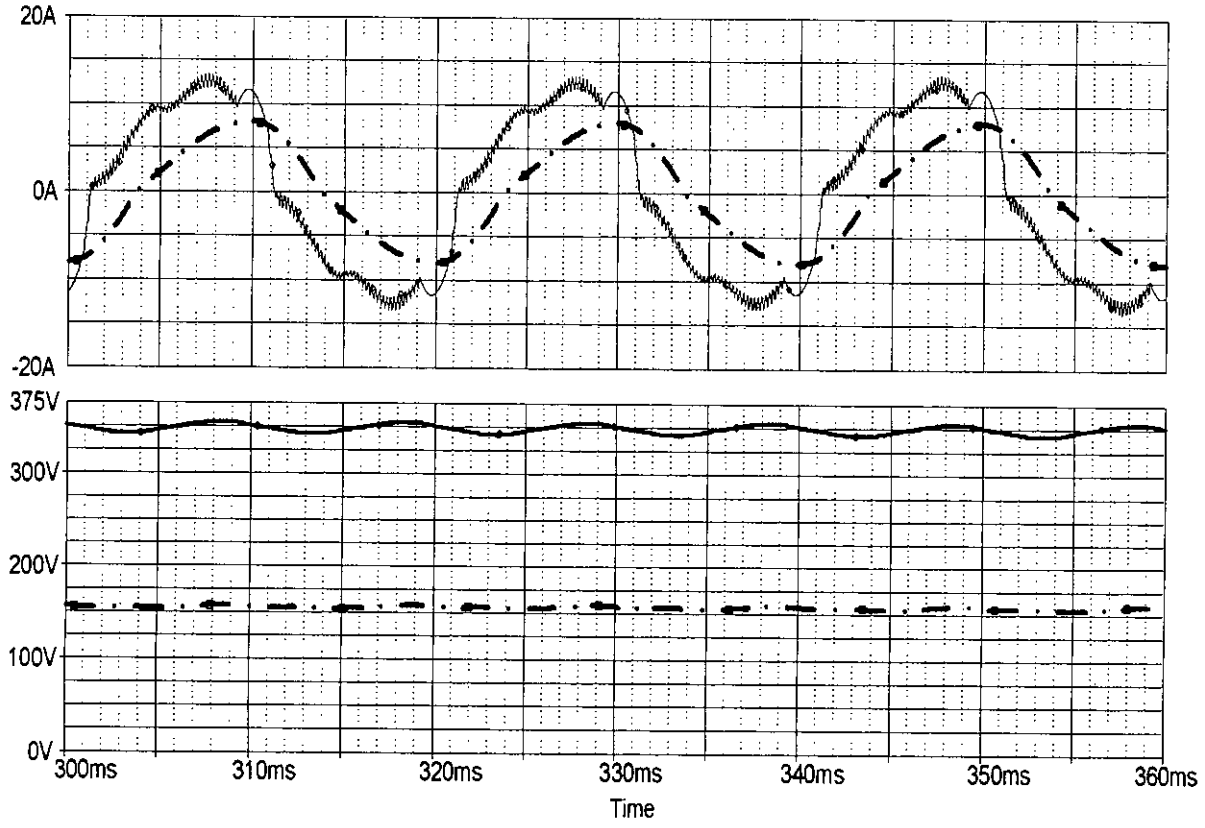


Figure 4.14: Input currents and output voltages obtained with 10mH (firm lines) and 100 mH (dotted) inductors with 5 KHz switching frequencies.

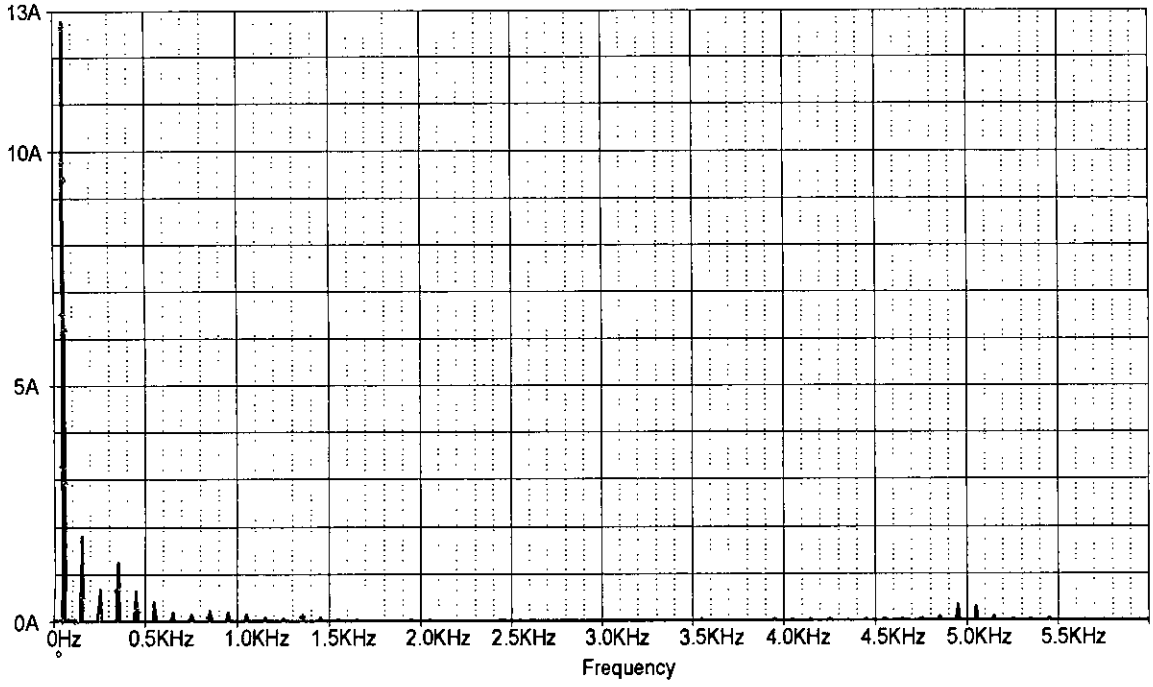


Figure 4.15: Fourier transform of input current with 10mH and 5kHz switching

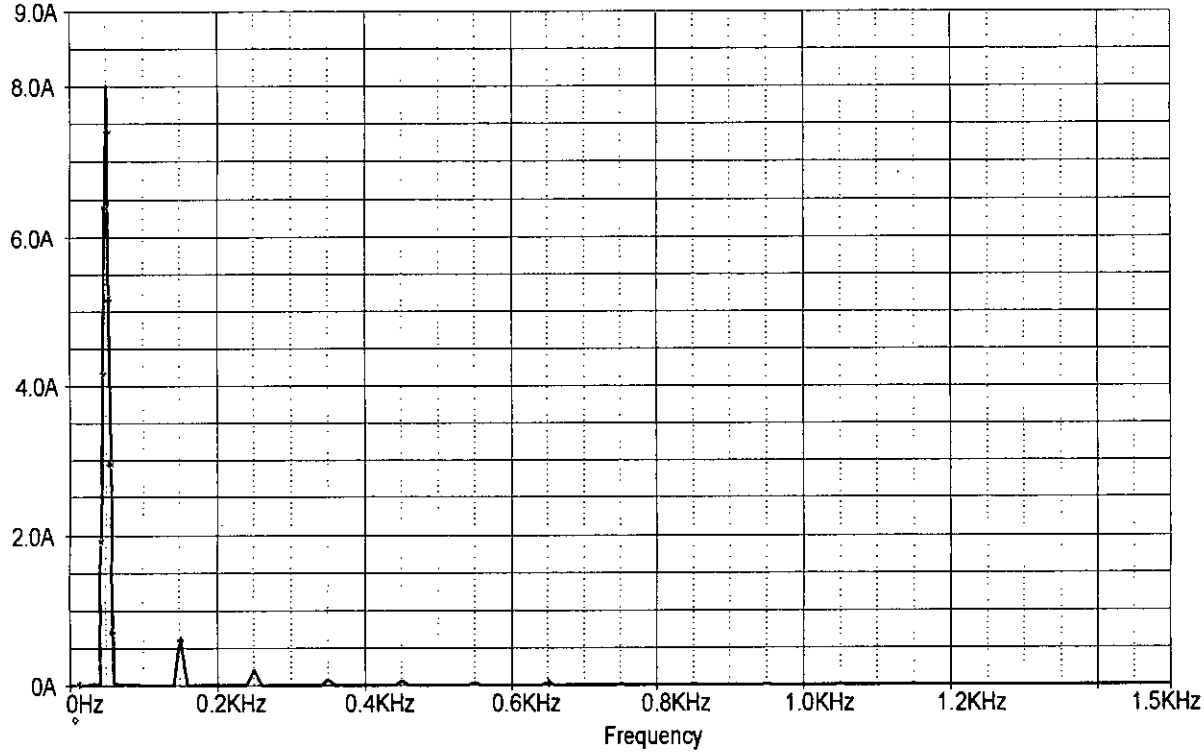


Figure 4.16: Fourier transform of input current with 10mH and 5kHz switching

Though with higher inductor (100mH) the current becomes almost sinusoidal and THD is reduced, the output voltage is also reduced to only 145V for a supply voltage having amplitude of 300V. Lowering of input current distortion by connecting a large inductor is thus overshadowed by the adverse effect of lowering of the output voltage due to large drop across the inductor. Moreover, the input current with 100mH inductor is almost 72° leading to a very low input power factor of 0.31.

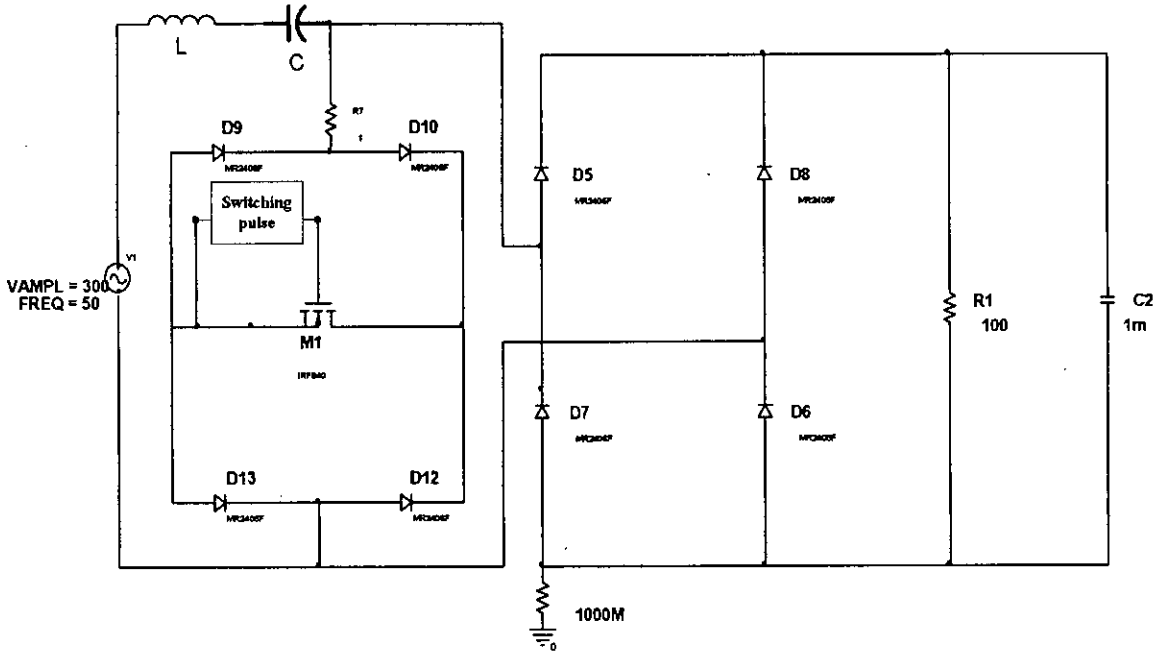


Figure 4.17: Rectifier circuit with input LC filter and switching

4.5 Switching with input LC filter:

In order to eliminate the adverse effect of voltage dropping across input inductor on output voltage, a capacitor has been also connected in series with the supply as shown in figure 4.17. The values of L and C forming the filter are chosen in such a way that its resonating frequency equals that of supply frequency which is 50 Hz. Most importantly this resonating LC combination is necessary to nullify the voltage drop across the inductor which otherwise cause drastic voltage reduction at the output. The input LC filter offers zero impedance to the fundamental frequency and at the same time blocks the higher harmonic frequencies. For a given input inductor and supply frequency, the required value of capacitance is given by

$$C = \frac{1}{4\pi^2 f^2 L} \tag{4.2}$$

where f is the supply frequency. For L=50 mH, C=202.64 μF. Figure 4.18 shows the simulated output voltage and input current with these L and C values with 5 kHz gate pulse.

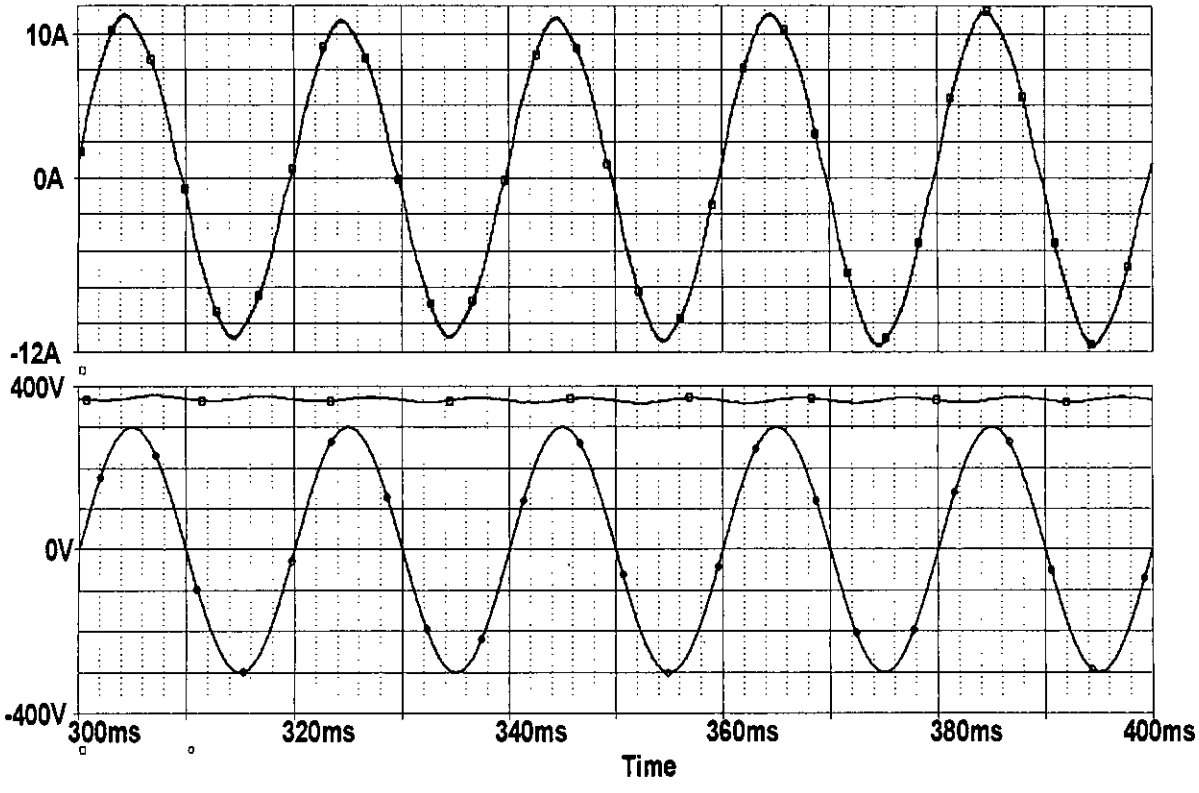


Figure 4.18: Input current (upper) and rectified output voltage along with supply voltage (lower) with L=50mH, C=202.64 μF, and 5 kHz gate pulse.

The output voltage is improved to around 365V. The dramatic improvement in current wave shape and phase relation is clearly seen from this figure. From the Fourier Transform of the input current (shown in fig 4.19), the THD is found to be 3.9% which is well bellow the IEEE standard limit for THD (5%). The phase angle between input voltage and current is found to be ~6° which implies a power factor of 0.993. With increasing the value of inductance to L=100mH and therefore C= 101.32μF, the THD is

found to be further improved to 3.3%. The phase shift in this case is also found very high, 0.994. The results with this LC combination are shown in figures 4.20 and 4.21.

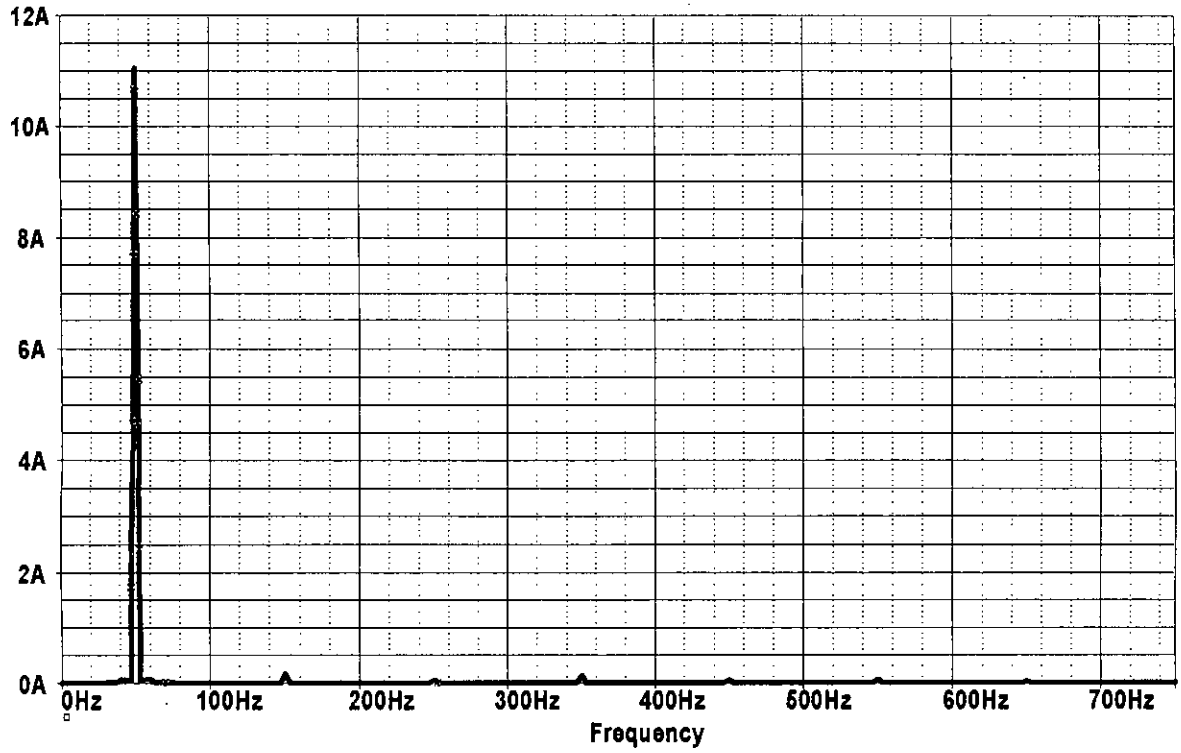


Figure 4.19: Fourier Transform of input current with L=50mH, C=202.64 μF, 5 kHz gate pulse.

The reason behind achieving sinusoidal input current at almost unity power factor can be attributed to the fact that with input LC filter output voltage becomes larger than that of supply. The output voltages for both the LC combinations discussed are found to be around 365 V. As the output voltage becomes higher than the supply voltage amplitude, the rectifier diodes (D5, D6, D7 and D8) are reversed biased and the current can flow naturally only when the switch (M1) is turned on. The duty cycle of the gate pulse of M1 is varied continuously in calculated pattern (discussed previously), such that the input follows a sinewave. When the supply voltage increases initially, the duty cycle is kept larger so that current can increase at a higher rate. As the supply voltage approaches towards its maxima, duty cycle is reduced and so increment rate of current is reduced. As the supply voltage crosses its maxima, the duty cycle again starts to increase

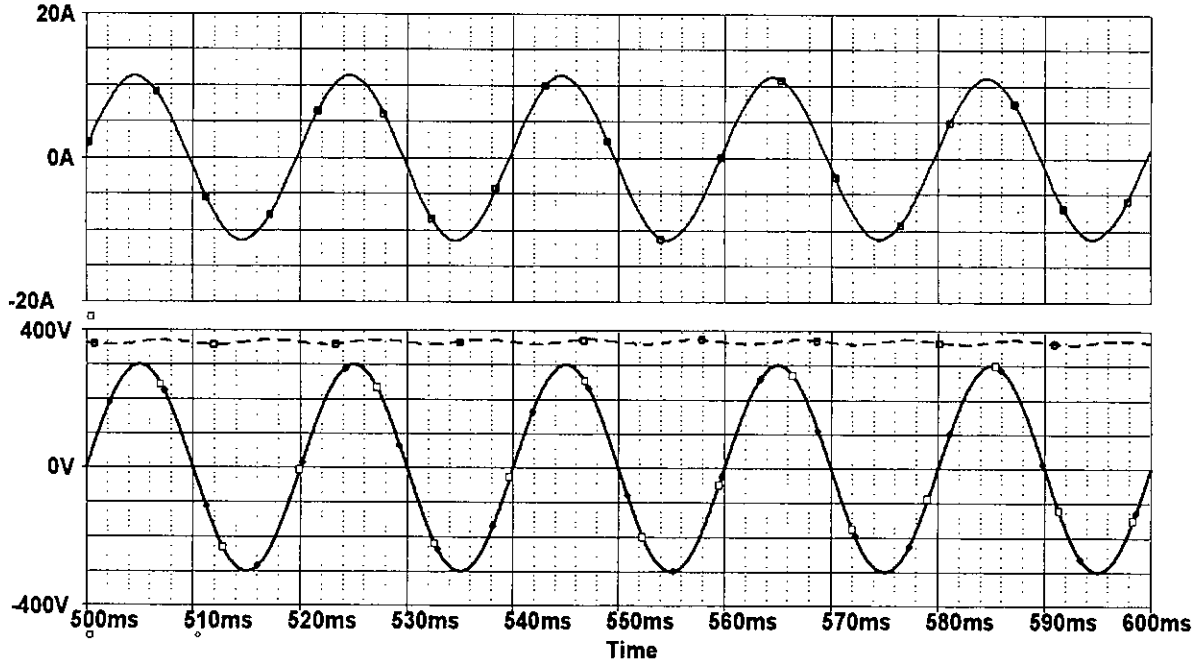


Figure 4.20: Input current (upper) and rectified output voltage along with supply voltage (lower) with L=100mH, C101.32 μF, 5 kHz gate pulse

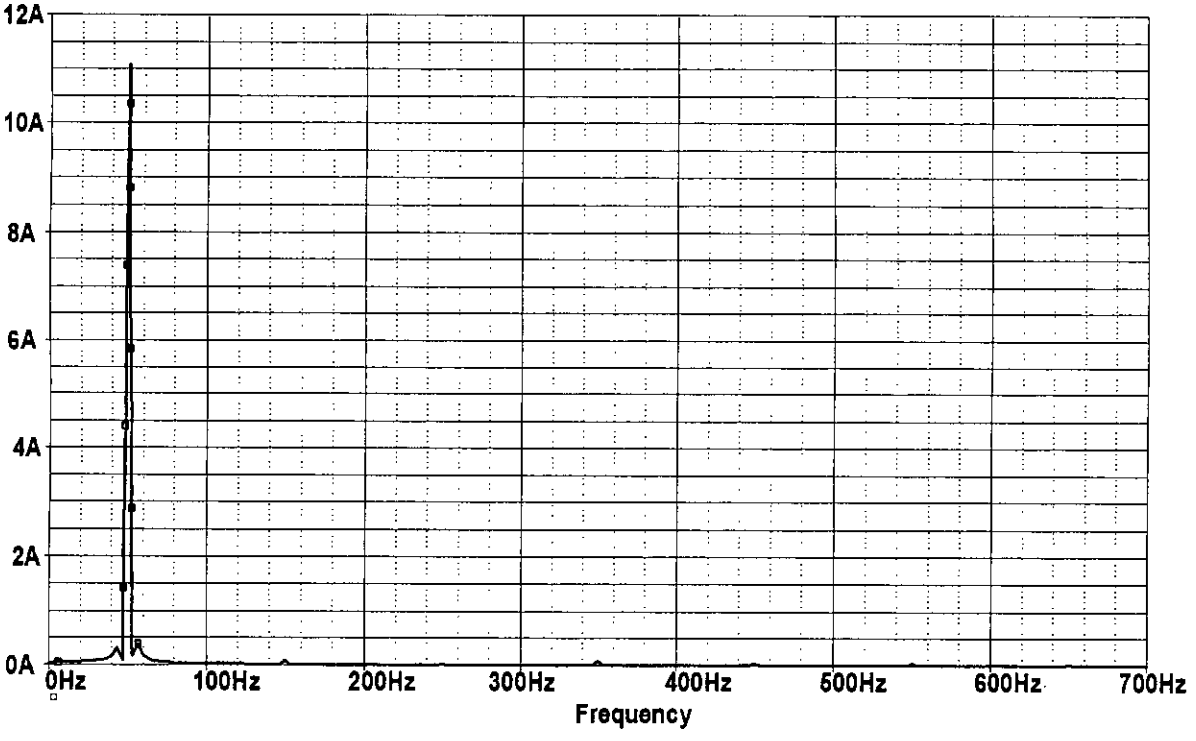


Figure 4.21: Fourier Transform of input current with L=100mH, C=101.32 μF, and 5 kHz gate pulse.

form its minima, At these points, ON time is less than OFF time and so current starts to fall. In case of inductor alone, output voltage becomes lower than the supply and therefore the above mentioned diodes remains forward biased and current flows even when the switch is turned off. This makes the switching scheme less effective and input current is distorted.

4.6 Unity power factor

With the LC combination connected in series with supply voltage and innovative switching scheme the input current has been made sinusoidal. However the phase angle between input voltage and current is not quite zero (the power factor is found to be more than 0.99 but not unity). The parallel combination of load resistor and output filter capacitor forms a capacitive load and therefore the circuit becomes slightly capacitive in nature as the equivalent impedance of input LC filter becomes zero at supply frequency. From figs 4.18 and 4.20, it is seen that input current leads the supply voltage by small

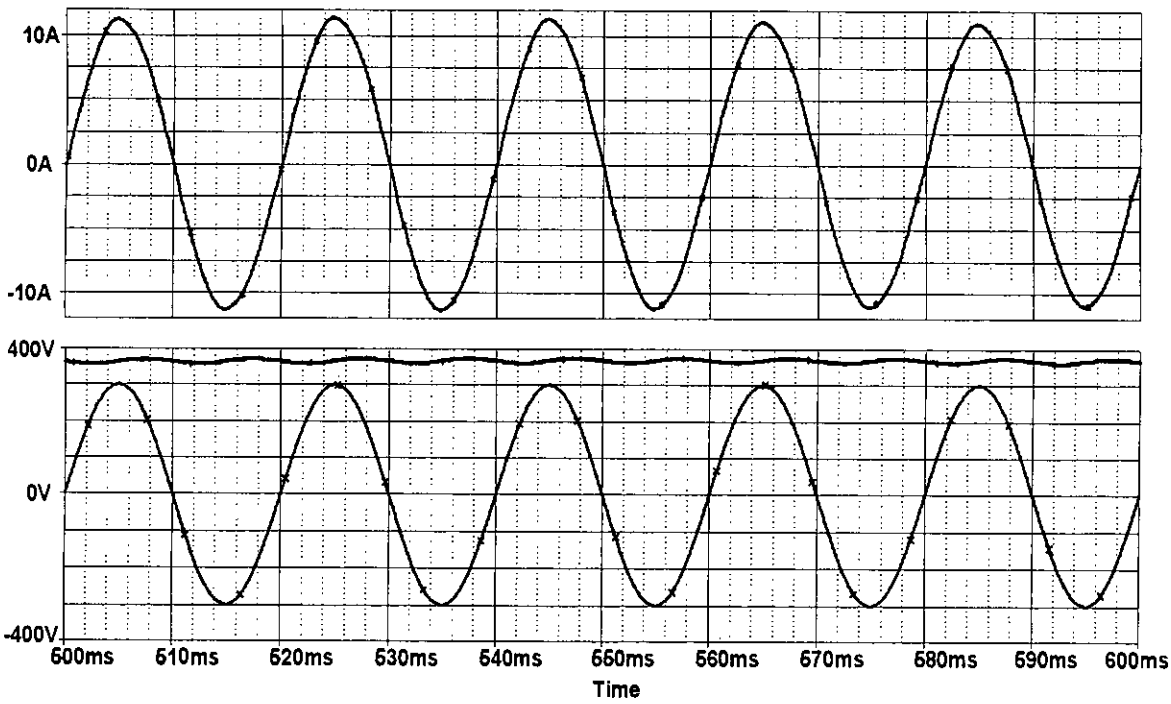


Figure 4.22: Input current (upper) and rectified output voltage along with supply voltage (lower) with L=100mH, C=103 μF, 5 kHz gate pulse.

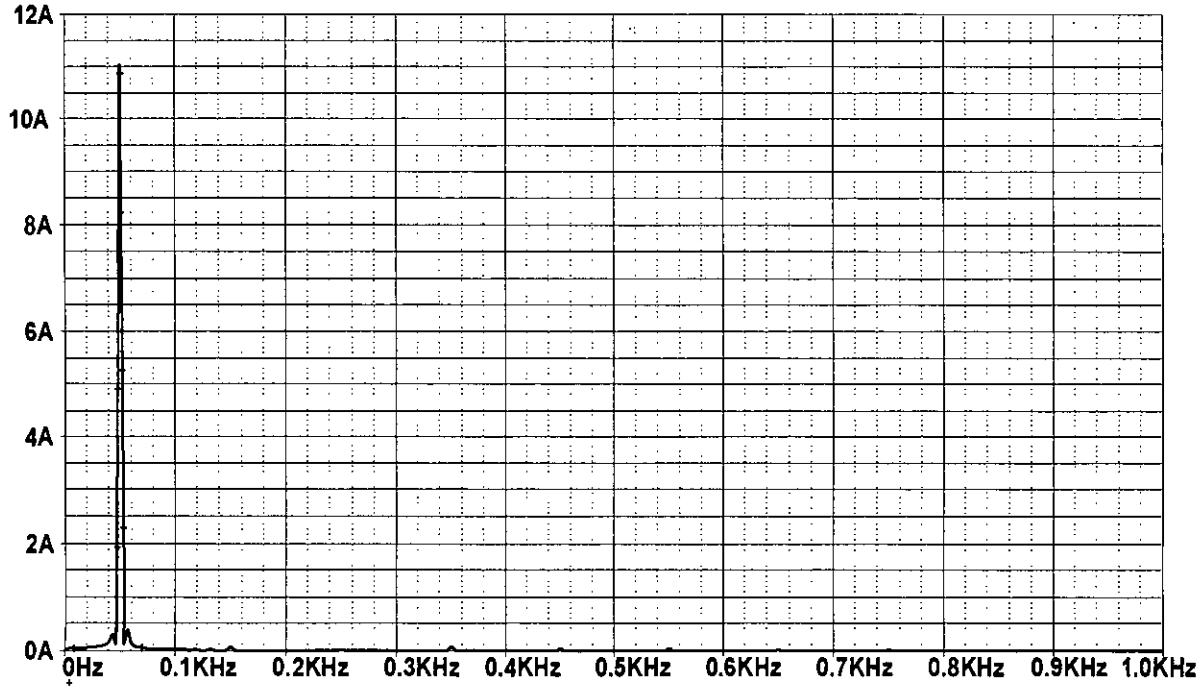


Figure 4.23: FFT of input current with L=100mH, C=103 μF, 5 kHz gate pulse.

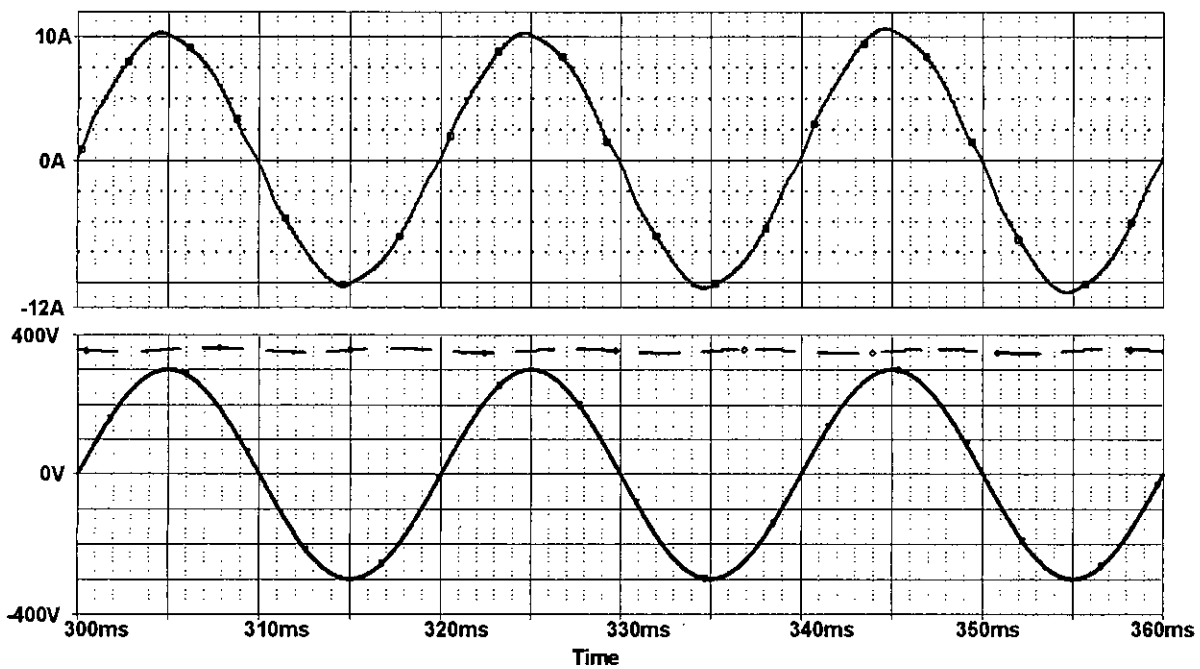


Figure 4.24: Input current (upper) and rectified output voltage along with supply voltage (lower) with L=50mH, C=207 μF, 5 kHz gate pulse and V2=3V.

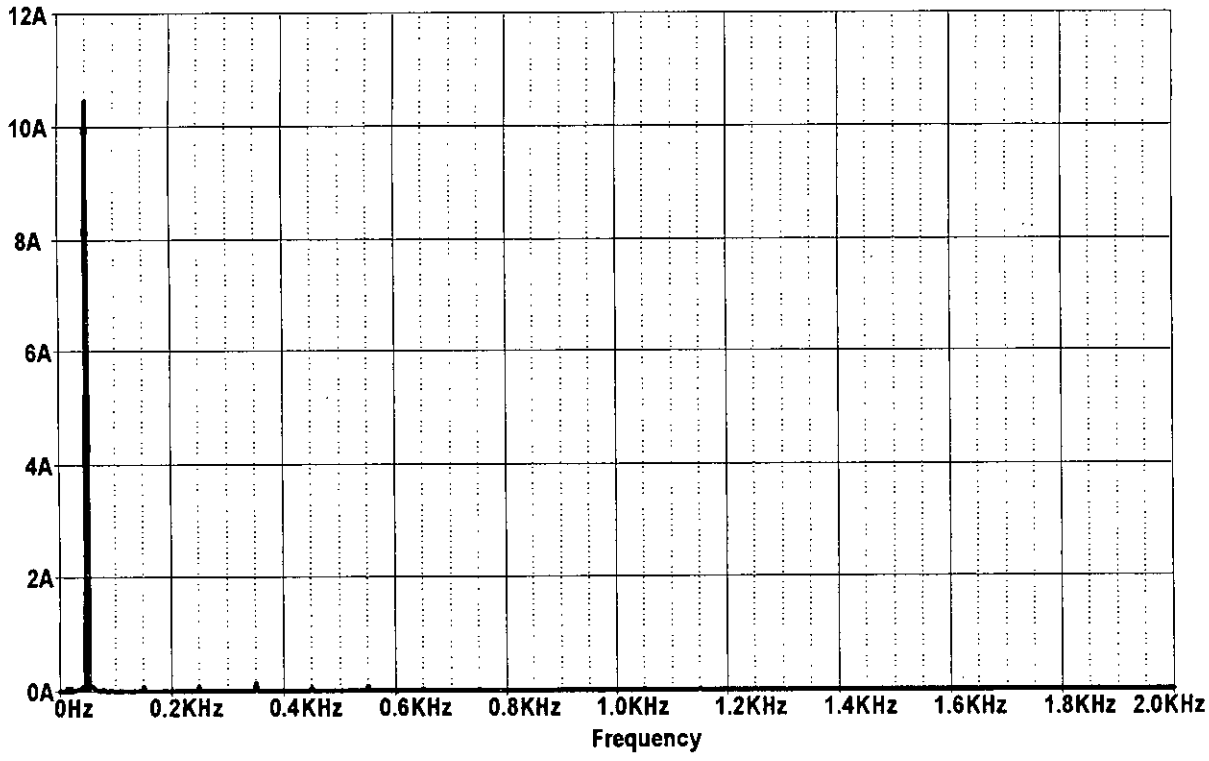


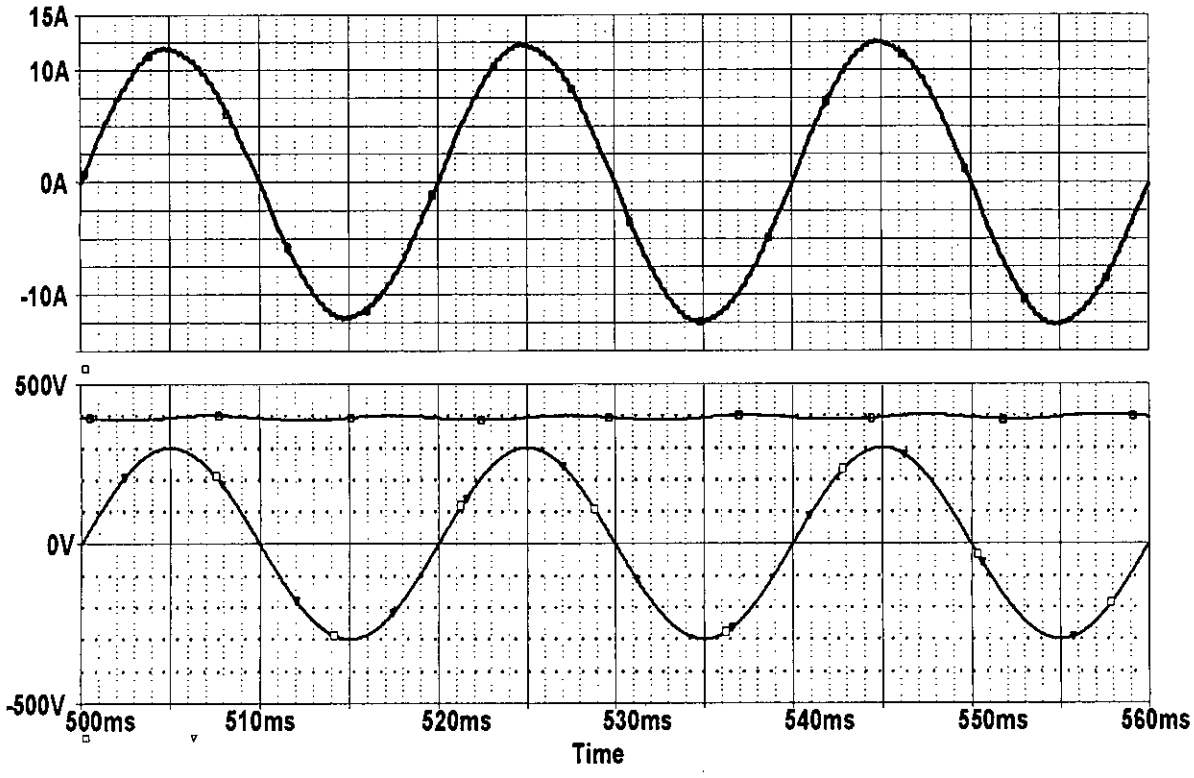
Figure 4.25: Fourier Transform of input current with L=50mH, C=207 μF, 5 kHz gate pulse.

angles. To reduce this phase angle to zero, the value of C has been increased slightly. Figures 4.22 and 4.24 shows the input current and output voltages with slightly larger capacitors that is required for resonance; with 100mH, 103 μF (instead of 101.32 μF) and with 50mH, 207.5 μF (instead of 202.64 μF) have been used. Note that in both cases the input current is in phase with the supply voltage. Figures 4.23 and 4.25 present the harmonic distribution of the input currents in these cases. With these slightly bigger capacitors the THDs with 100 and 50 mH are found to be 2.8% and 2.9% respectively.

The overall efficiency of the overall circuit with the LC filters discussed above and 5 kHz switching frequency is found to be more than 80% according to the following equation:

$$\%\eta = \frac{P_{DC}}{P_{AC}} = \frac{V_{DC} I_{DC}}{V_{rms} I_{rms}} \qquad (4.3)$$

The output voltage and hence efficiency is increased when the switching frequency is reduced to 3 kHz. Figure 4.26 represent the input current and output voltage obtained with L=100mH, C = 103μF and 3 kHz switching. The Fourier transform of the input current is shown in figure 4.27. The output voltage with these parameters is found to be around 400V with a THD of 1.6% and unity power factor. Figures 4.28 to 4.31 present the input currents, output voltages and Fourier Transforms of input currents with different LC filter combinations and different switching frequencies.



Figures 4.28: Input current (upper) and output voltage along with supply voltage (lower) with L=100m, C=103μF and 3 kHz switching frequency.

Finally Table 4.1 summarizes the results obtained with different input filter elements and switching frequencies to reveal the optimum combination. It shows that with the proposed switching scheme and input LC filter almost resonating at the supply frequency, the rectifier can draw sinusoidal input with unity power factor and high efficiency. The

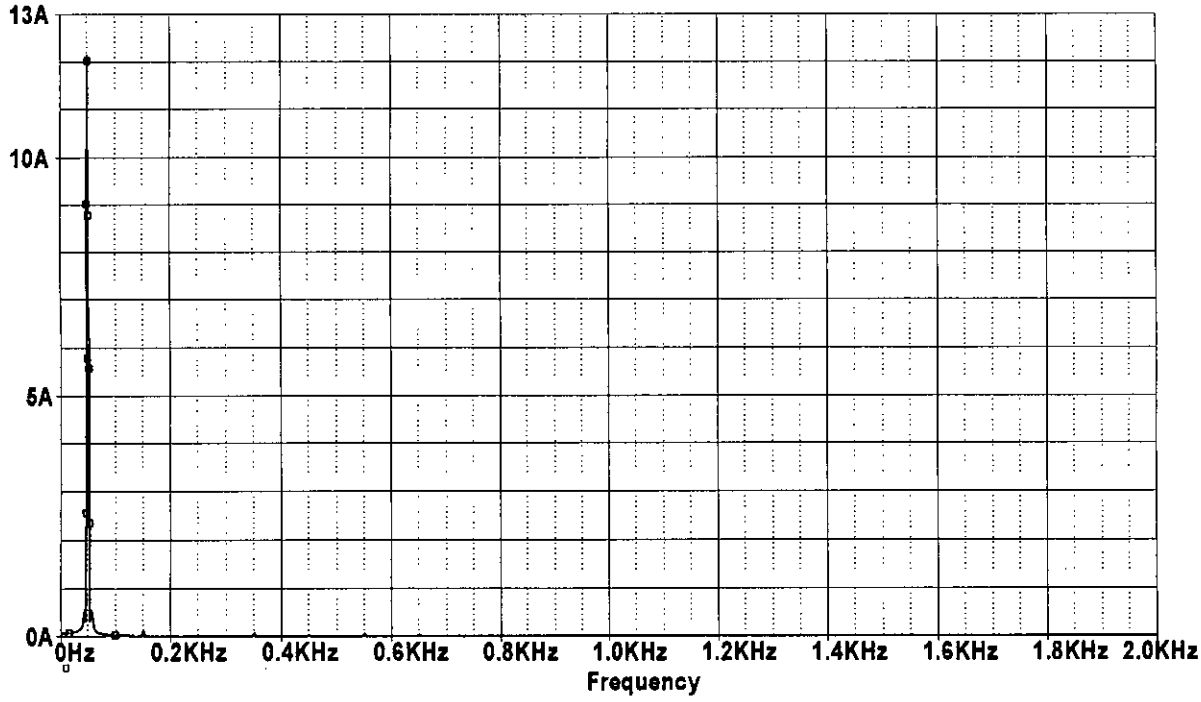


Figure 4.29: Fourier Transform of with L=100m, C=103μF and 3 kHz switching frequency.

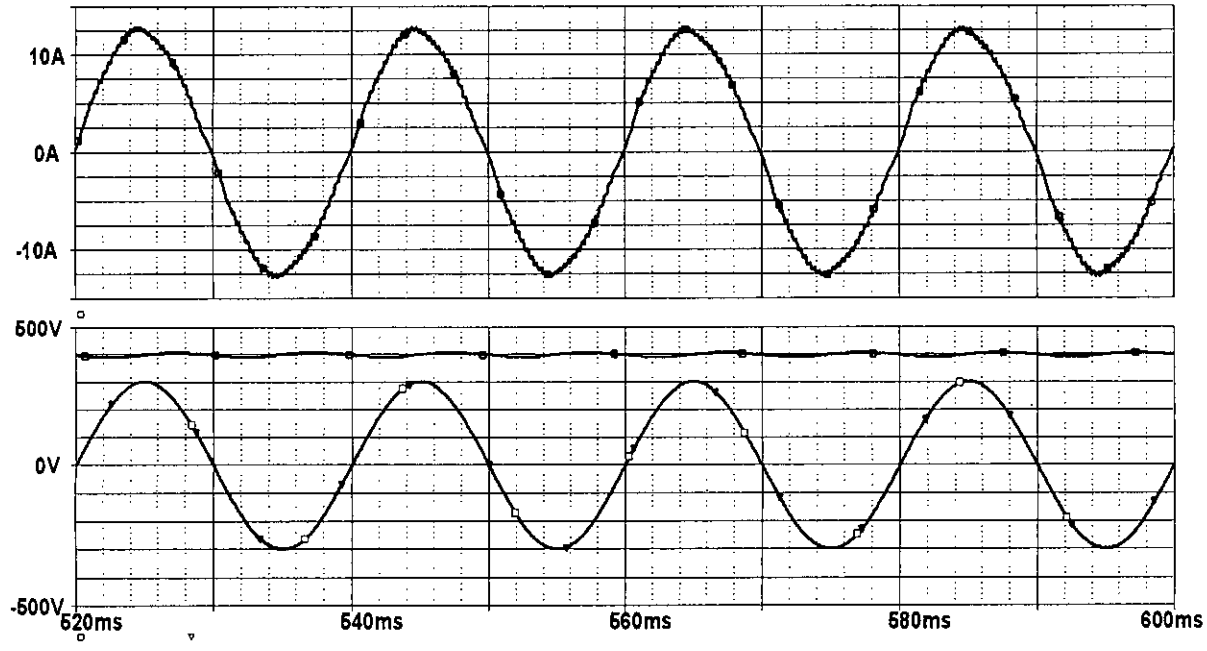


Figure 4.30: Input current (upper) and output voltage along with supply voltage (lower) with L=50m, C=206μF and 2.5 kHz switching frequency.

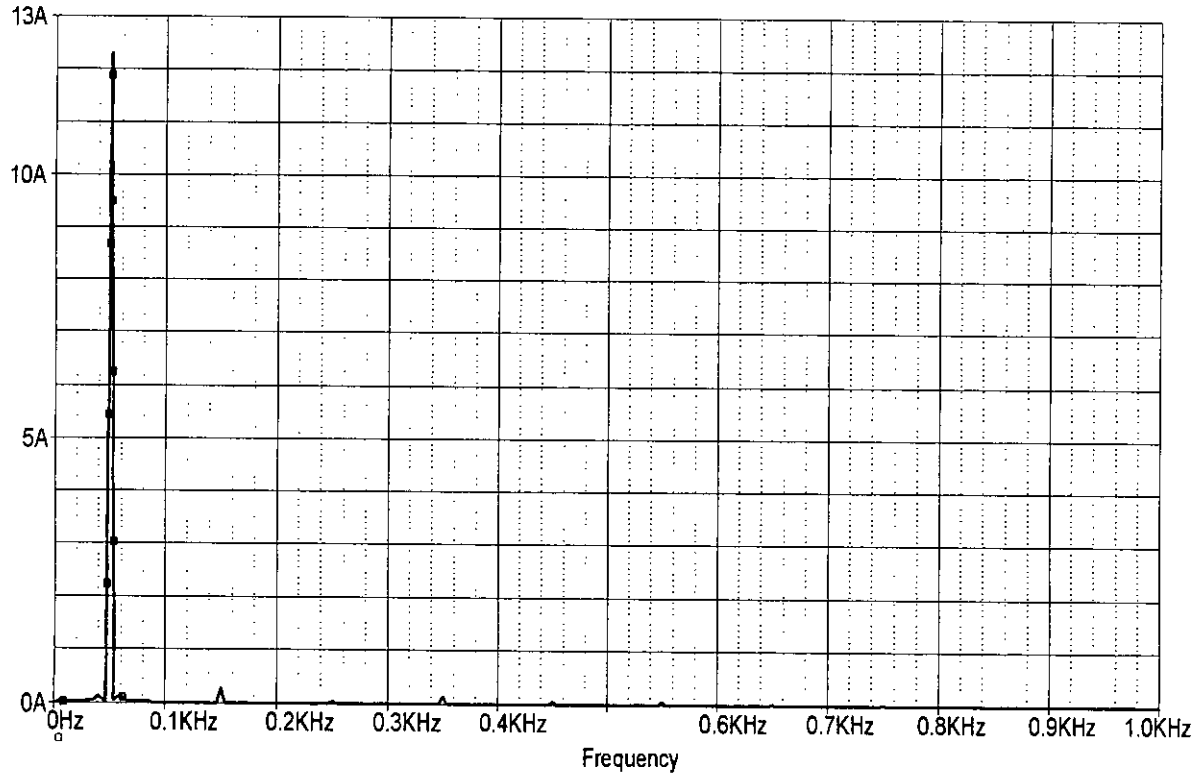


Figure 4.31: Fourier Transform of input current with L=50m, C=206μF and 2.5 kHz switching frequency.

Table 4.1: summary of the simulated results for the proposed scheme

Input Filter	Switching frequency KHz	THD %	Power Factor	V_{out} Volt	Efficiency %
L=10mH	5	18.60	-	350	-
L=100mH	5	12.4	0.31	160	-
L=50mH, C=202.64μF	5	3.9	0.993	365	79
L=100mH, C=101.32μF	5	3.3	0.994	370	81.5
L=100mH, C=103μF	5	2.8	1	365	81
L=50mH, C=207μF	5	2.9	1	370	89
L=100mH, C=103μF	3	1.6	1	400	89
L=50mH, C=206μF	2.5	2.8	1	405	91.13

best result in terms of efficiency is obtained for L=50mH, C=206μF and switching frequency of 2.5 kHz. In this case, THD of input current is 2.8%, output voltage is 405V, and efficiency is 91.13%.

4.7 Conclusion

In this chapter, the simulated results of the proposed scheme designed to improve the power factor and distortion in input current of a single phase bridge rectifier has been presented. The results have been presented in an order to reveal the design steps. Table 4.1 documents the summary of the findings through simulation and clearly shows the improvement achieved step by step. The significant improvement achieved after connecting a capacitor in series with the input inductor. The input current with the proposed switching scheme has been found to be sinusoidal with very low THD (less than 3%) and perfectly in phase with the supply voltage.

CHAPTER 5

Conclusions

5.1 Discussions

In this thesis a scheme for improving the input current wave shape and power factor of a single phase rectifier has been proposed and analyzed. The output filter capacitor connected to reduce the ripples in output voltage makes the input current drawn by the rectifier highly distorted and discontinuous. The input current flows only for brief intervals in each cycle. Such distorted, non sinusoidal input current contains harmonics which lead to heat loss, lower efficiency, input ac mains voltage distortion, lower power conversion reliability, excitation of undesirable system resonances and increased volt-ampere rating of the equipments. Making the input current sinusoidal and in phase with the supply voltage is therefore of utmost importance. In this work an input side switching scheme has been designed which along with a simple LC filter can achieve desired sinusoidal input current wave shape and unity power factor. An analytical expression of input current has been derived and from that it has been shown how the proposed scheme makes the input current sinusoidal. The simulated results are presented to confirm that the proposed switching scheme can limit the Total Harmonic Distortion (THD) in input current well within the constraints set by the present standard and improve the power factor to unity.

5.2 The Proposed Switching Scheme

In a conventional rectifier with output filter capacitor, input current is ceased to zero as the load voltage equals the supply voltage. At this point, the rectifier diodes are reverse biased. As shown in previous chapters, input current flows only for two brief periods in each cycle of supply voltage. Such spiky nature of input, due to its harmonic contents currents, is undesirable in a power system. The objective of this thesis has been to design a switching scheme which can make the input current sinusoidal and in phase with the supply voltage.

The input current flows naturally in a conventional bridge rectifier when the output voltage falls below the supply voltage. This happens as the supply voltage approaches its positive or negative maximum value. To make the current continuous, an alternative path has to be provided for the rest of the period. An electronic switch at input side provides the desired alternative path. However, keeping the switch ON for the whole naturally non-conducting period of input current would result indefinitely high and still distorted current. Therefore the switch has to be continuously turned ON and OFF. To prevent the current from falling to zero value instantaneously as the switch is turned OFF and limit the current value when switch is ON, an input inductor is used. In this work, the duty cycle of the switch has been continuously varied to make the input current sinusoidal. At the beginning of the cycle the switch is kept ON for longer period of time and gradually the ON time is reduced. Since the input current flows naturally as the supply voltage approaches peak values (positive or negative), the ON period is kept minimum during those periods. The duty cycle of switching is therefore varied like a cosine wave with a frequency twice of that of the supply. The switching pulse with a certain frequency but varying duty cycle has been generated by comparing a triangular wave (frequency twice of that of supply) with a sine wave having the required switching frequency.

At steady state the output voltage is higher than the supply voltage. As a result the input current can flow only during the ON period of the switch. This ensures that the current varies according to the duty cycle of the switch and follows a sinusoidal waveform. In order to ensure zero phase difference between input current and supply voltage a capacitor has been connected in series with the input inductor. The series LC combination resonates at supply frequency and therefore allows only the fundamental component of the input current to flow into the circuit. However this makes the equivalent circuit slightly capacitive. Therefore, the value of capacitor used is marginally higher than that required for series resonance at supply frequency.

The switching scheme designed based on the concept described above has been simulated to analyze its performance. The results are very promising which show that the proposed

scheme can produce almost pure sinusoidal input current with THD as low as 2.96% and unity power factor. The overall efficiency of the rectifier circuit with the proposed scheme is also found satisfactory, around 90%.

5.3 Limitations and suggestions for future work

In the proposed scheme presented here an input LC filter has been used to suppress the harmonic components of the input current and to improve the power factor. For this purpose, the values of L and C are so chosen that their series resonating frequency almost equals the supply frequency. This demands big inductors (in the range of mH) and capacitors (of the order of 100 μFs) which would make the circuit bulky when practically implemented.

The pattern of duty cycle variation over the period of supply voltage has been determined rather qualitatively. A more rigorous theoretical analysis should be developed in order to obtain an exact analytical expression for the duty cycle variation required to make the input current distortion less and sinusoidal. Further analysis should be carried out to establish relation between duty cycle variation and THD for given load and filter elements.

In order to have better insight regarding the performance of the rectifier with proposed scheme, Fourier analysis of the input current expression should be done and filter components should be chosen based on that. As mentioned above, the analytical expression of duty cycle variation should be incorporated in the input current equation to make it more accurate and effective in designing the switching scheme.

Switching power loss should be minimized in order to enhance the overall system efficiency. Effect of different loads on required switching frequency, duty cycle variation and efficiency should also be studied.

Finally the proposed rectifier circuit model should be implemented practically to reveal its actual potential. Such practical implementation would also give an insight regarding

the cost effectiveness of the proposed scheme compared to the existing ones for the similar purpose.

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APPENDIX A

MATLAB code to generate input current drawn by a rectifier with the proposed scheme:

```
%supply voltage and frequency
Vm=300;f=50;w=2*pi*f
fs=5e3;ws=2*pi*fs;
L=100e-3; %inductor in henry
C=1/(L*w*w);
K=((C/L)^.5)
T=1/f;Ts=1/fs;%supply signal and switching signal period
t=0:1e-6:40e-3;
Vsw=10*cos(ws*t);
int=0.5*T/(T/Ts);
delt=0;
m=0;

for n=1:length(t)
  if t(n)<4.5e-3
    Vtri(n)=(-1*(20/(0.225*T))*t(n)+10);
  elseif t(n)>=5.5e-3&t(n)<10e-3
    Vtri(n)=(10/(0.225*T)*t(n)-22.22);
  elseif t(n)>=4.5e-3&t(n)<5.5e-3
      Vtri(n)=-10.001;
  else
    m=m+1;
    Vtri(n)=Vtri(m);
  end

end
```

```
for n=1:length(t)
  if Vsw(n)>Vtri(n)
    if (Vm*sin(w*t(n)))>=0
      Vdc(n)=330;
    else
      Vdc(n)=-330;
    end
  else
    Vdc(n)=0;
  end

  Vs(n)=Vm*sin(w*t(n));
  V=-220;
  if n<2
    Vs(n)=0;
    Io(n)=0.5;
    Vo(n)=V*cos(w*t(n));
    count=1;
    %delt=count*1e-6;
  else

    if Vdc(n)==Vdc(n-1)
      Vs(n)=Vs(n-1);
      Vo(n)=Vo(n-1);
      Io(n)=Io(n-1);
      count=count+1;
      %delt=count*1e-6;
    else
      count=count+1;
      delt=count*1e-6;
```

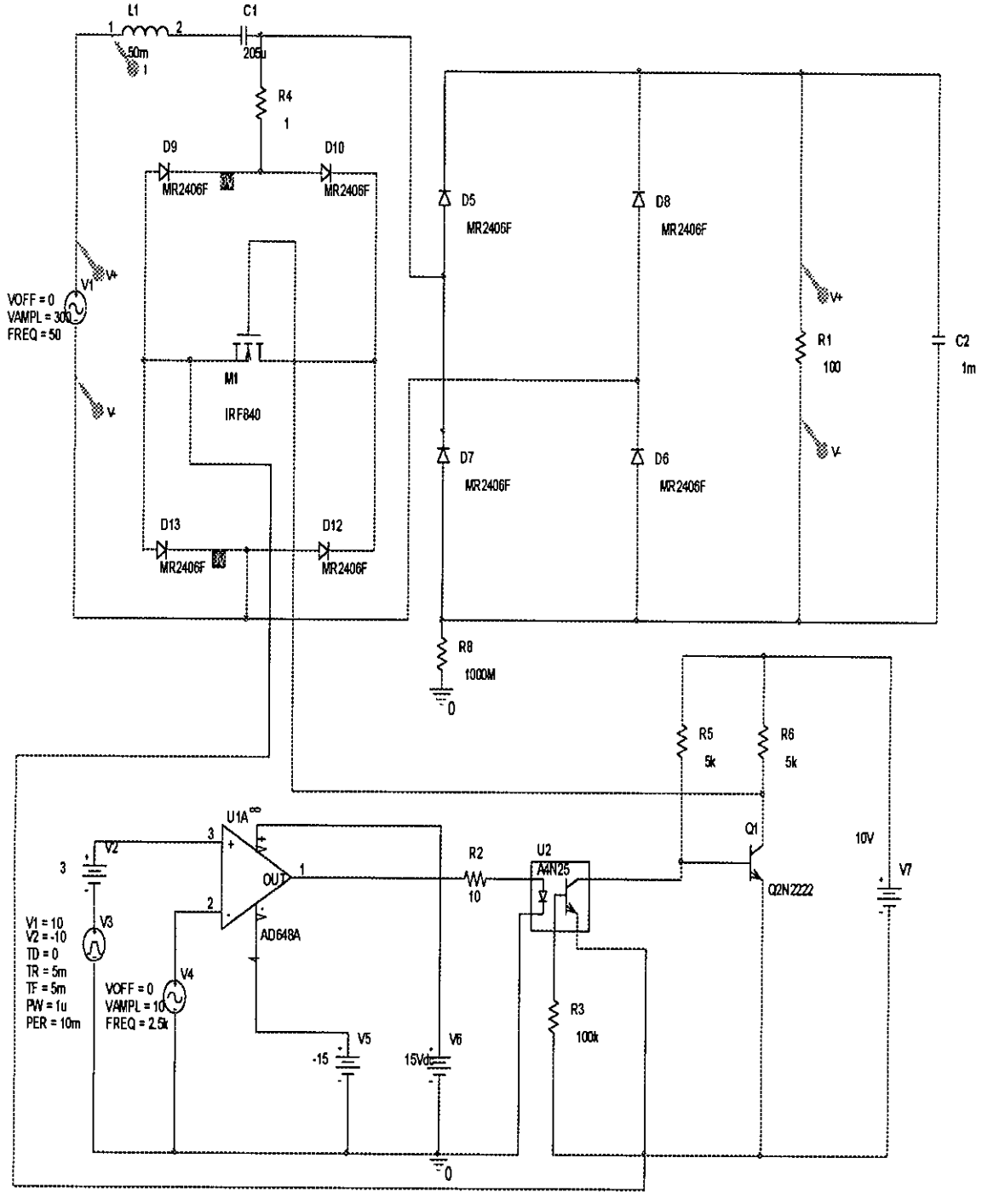
```
        Vs(n)=Vm*sin(w*t(n-1));
        Io(n)=(Vs(n-1)-Vo(n-1)-Vdc(n-1))*K*w*delt+Io(n-1);
        Vo(n)=V*cos(w*t(n));
        count=0;
      end

    end
    delt=count*1e-6;
    i(n)=(Vs(n)-Vo(n)-Vdc(n))*K*w*delt+Io(n);
end

% Printing the desired results
plot(t,i,'b')
hold on
plot(t,Io,'k')
hold on
plot(t,Vo,'g')
hold on
plot(t,Vtri,'k')
grid on
plot(t,Vs,'c')
hold on
```

APPENDIX B

A sample rectifier circuit with proposed scheme used for simulation with ORCAD 9.2



APPENDIX C

OPTO-COUPLER

An optocoupler, also called optoisolator, is an electronic component that transfers an electrical signal or voltage from one part of a circuit to another, or from one circuit to another, while electrically isolating the two circuits from each other. It consists of an infrared emitting LED chip, all enclosed in the same package. The silicon chip could be in the form of a photo diode, photo transistor, photo darlington, or photo SCR.

Functions of Opto-Coupler

- To isolate one section of a circuit from another , each section having different signal voltage levels to ensure compatibility between them.
- To prevent electrical noise or other voltage transients that may exist in a section of a circuit from interfering with another section when both sections have a common circuit reference. Noise or voltage transients can be caused by a poor printed circuit board layout.

Spectral Response of Silicon

Since silicon has a response to light (spectral response) that peaks at infrared wavelengths (between 800 and 950 nanometers), silicon devices are preferred as the photodetector section in optocouplers in conjunction with an infrared LED emitter (Figure 4.4). Matching the infrared LED to the silicon chip provides a maximum transfer of the desired electrical signal.

Different types of optocouplers have specific characteristics that determine suitability for each unique application. The simplest type is the optocoupler with a photo diode output section. The optocoupler output is often connected to an amplifier (or series of amplifiers) to change a low-level input voltage into an appropriate higher signal level.

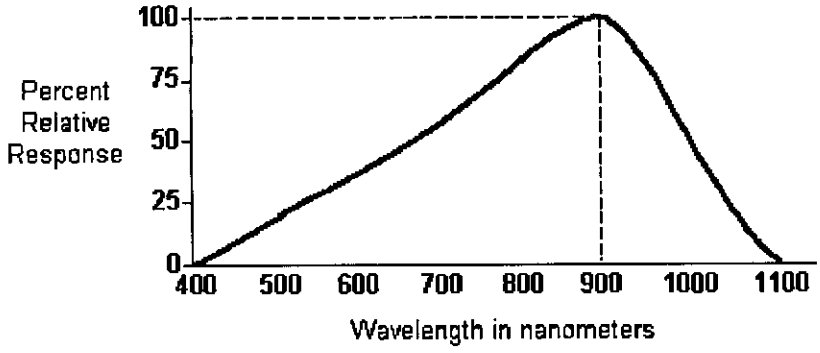


Figure: Spectral response curve of silicon

Principle of operation

When a forward bias voltage is applied to the input terminals of the LED (positive to the anode), an input current, I_{IN}, limited by the series resistor, R_S, will flow in the LED circuit. The current produces the infrared light emission at about 900 nanometers that impinges on the photosensitive silicon chip.

Photo Diode Output

- With light impinging on the silicon diode in Figure 4.5, its photovoltaic characteristic will create photo current, I_L or I_{OUT}, to flow in the silicon diode. With a load resistor, R_L, connected to the output terminals of the coupler, the photo current, I_{OUT}, will develop a voltage, V_L, across the load.

$V_L = I_{OUT} \times R_L$.

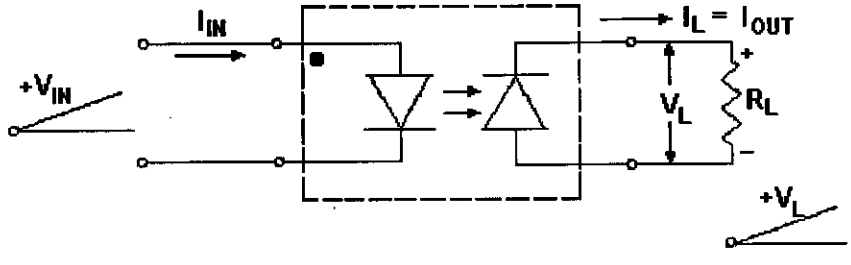


Figure : optocoupler with Photo Diode Output

• As the input signal, V_{IN}, varies; it will vary the intensity of the infrared light. The output current, I_{OUT}, will also change, causing the output voltage, V_L, to change in the same manner.

• As output current increases, output voltages will also increase, and vice-versa. A small change in input current will produce a proportionate change in output current. This characteristic of the optocoupler will act to couple low-level analog signals or small DC voltage variations with little or no distortion.

In the circuit of Figure 4.5, both signal coupling and input-to-output isolation is achieved, however, the current transfer ratio (CTR) of a diode output optocoupler is extremely low – about 10% to 15%. The term current transfer ratio (CTR) defines the relationship of output current, I_{OUT}, to input current, I_{IN}.

$$CTR = \frac{I_{OUT}}{I_{IN}}$$

The output voltage, V_L, can be coupled to the input of an amplifier to increase its amplitude to an appropriate level.

The input section of all optocouplers is an infrared LED, however, the output section can be different depending on the required application. The basic principle of operation is the same, regardless of the particular output section selected.

Photo Transistor output

Since the CTR of an optocoupler with a photo diode output is so low (10 to 15%) a preferred approach is to replace the diode chip with a silicon bipolar phototransistor (Figure 4.6).

The bipolar transistor, with its inherent current gain, β, will provide a considerably higher CTR (between 50% to 100%) depending on the beta of the phototransistor.

The base lead of the transistor can be reverse biased to reduce sensitivity, or forward biased to increase sensitivity, or left "floating" (disconnected).

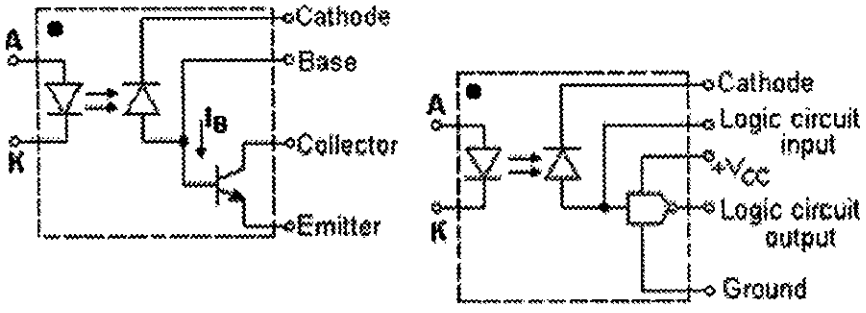


Figure: Variations of optocoupler output section