Modeling of Charge Quantization and Wave Function Penetration Effects in Ultra Thin Body Double Gate MOSFETs

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MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

By

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I hereby declare that this thesis has been done by me and it or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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Contents

List of Parameters

Parameter name	Symbol
Distance along the depth of the MOSFET	Z
Gate capacitance	C_G
Silicon film thickness	t_{si} ,Tsi
Gate voltage	V_G
Threshold voltage	V_t
Inversion charge density	$n(z)$
Fermi energy	E_F
Updating coefficient	alpha
Doping density	N_A ,Na
Dielectric thickness	t_{ox} , Tox
Center potential	V_O
Surface potential	V_S
Flatband voltage	V_{FB}
Average penetration depth	$Z_{average}$

Abstract

Modeling of charge quantization and effects of wave function penetration into gate oxide on the properties of ultra thin body double gate (DG) MOSFET in deep submicron regime are studied. Self–consistent modeling of double gate MOS inversion layer has been performed, taking into account the effects of wave function penetration on the solutions of both Schrödinger and Poisson equations. A solver, based on Finite Element Method, has been applied for the solution of both Schrödinger and Poisson equations that is much faster and efficient than conventional Schrödinger-Poisson solver. The developed numerical solver has been applied to fully depleted DG MOSFET (both n-MOS & p-MOS) for analyzing electrostatics of the device such as, inversion layer charge, average penetration depth, surface potential and gate capacitance, and hence wave function penetration effects have been revealed by comparing the results with those of without penetration. Finally, the results have been compared with established numerical solver. The solver has the capability of analyzing both symmetric and asymmetric DGMOS structures. Average penetration depth for half of the silicon film and gate capacitance has been calculated. Wave function penetration effects with the variation of substrate doping, silicon film thickness and dielectric thickness has been illustrated. It has been shown that the concept of volume inversion is not accurate for thicker semiconductor region, Average penetration depth is overestimated and capacitance is underestimated if the penetration effect is not in consideration. Also it has been shown that the penetration effect is not same for different oxide thickness, semiconductor thickness and doping density and the reasons are discussed in details.

Chapter 1

Introduction

1.1 Transistor Scaling

History of integrated circuit design reveals a general scaling methodology for MOSFET devices [1]. This scaling methodology relies heavily on the use of successively thinner gate dielectric and higher level of channel doping in order to simultaneously achieve the desired device turn-off and drive current capability as feature size decreases. According to the 2006 International Technology Road Map for Semiconductors (ITRS), the high performance logic limit of a device will correspond to a channel length of 13 nm with oxide thickness of less than 1 nm and a gate length of 13 nm [1].With ever demanding market for higher speed and lower power dissipation and higher packing density, the MOS transistor size have shrunk to a few nanometers. Transistor scaling has been made possible by the improved lithographic capability to print shorter gate lengths and the ability to grow nearly perfect insulators with ever decreasing thickness.

Even if lithographic and etching techniques can provide the necessary dimensions, bulk CMOS will run into a number of short channel effects associated with transistor scaling. The short channel effect (SCE) is characterized by threshold voltage (V_t) roll off, drain induced barrier lowering (DIBL) and sub-threshold swing. As the gate length of a MOSFET is scaled with all other device parameter held constant, sub-threshold swing increases and V_t decreases, which degrades MOSFET performance.

The ratio of on current to off current (I_{ON}/I_{OFF}) is reduced, giving designers a tradeoff between circuit speed and static power dissipation. The industry roadmap indicates that CMOS technology is approaching some physical limitations and practical technological barriers to continuous scaling.

As the downscaling of CMOS technology approaches physical limitations, the need arises for alternative device structures. Many novel structures have been proposed for the nanoscale regime. These include high-k dielectrics, incorporation of metal gates, and elevation of the source and drain regions. High-k dielectrics can be used to decrease the effective oxide thickness without increasing I_{OFF} by reducing oxide tunneling current. Metal gates solve the gate poly-Si depletion problem, which causes an increase in the oxide capacitance and lowers I_{ON}. Elevated source/drain regions allow for lower series resistance and thus, greater ON current. Also tailoring the doping profile with retrograde channel profiles, halo ion implants and ultra-shallow junction depths is often performed in order to tame the SCE. However, these improvements are not expected to push CMOS scaling down below the 65 nm [1, 2]

As the limit of bulk Si CMOS scaling approaches, new devices with slight variations to classical bulk CMOS have brought much attention to researchers and industry alike. These include partially and fully-depleted Silicon-on-Insulator (SOI), gate all-around MOSFET, Si-Ge MOSFET and Double gate (DG) MOSFETs. With the possibility of gate length scaling down to 10 nm [3, 4], DG MOSFET devices have become very much promising.

1.2 Modeling of Double-Gate (DG) MOSFET

As CMOS scaling is approaching its limit due to processing as well as fundamental considerations, double-gate (DG) MOSFET is becoming an intense subject of VLSI research. Theoretically, DG MOSFETs can be scaled to the shortest channel length possible for a given oxide thickness [5]. Among the advantages advocated for double-gate MOSFETs are: ideal 60mv/decade sub-threshold slope, volume inversion [6], setting of threshold voltage by the gate work function thus avoiding dopants and associated number fluctuation effects etc. As the gate length goes below deep submicron dimensions, the device design, as guided by scaling rules, can result in very large normal electric fields at the Si/SiO_2 interface, even near the threshold of inversion. This leads to a significant bending of the energy band at the Si/SiO_2 interface. It has long been known that with sufficient band bending, the potential well can become sufficiently narrow to quantize the motion of inversion layer carriers in the direction perpendicular to the interface [7]. This gives rise a splitting of the energy levels into subbands (2-dimensional density-of-states), such that lowest of the allowed energy levels for electrons in the well does not coincide with the bottom of the conduction band. Due to Quantization, the electron density does not reach its maximum at the oxide-semiconductor interface as in the semi-classical [8, 9], instead some distance inside the semiconductor. Fig. 1.1 shows a typical conduction band profile for a double gate n-MOSFET device and Fig. 1.2 shows the electron density in silicon near Si/SiO_2 interface as obtained from quantum mechanical (QM) calculations.

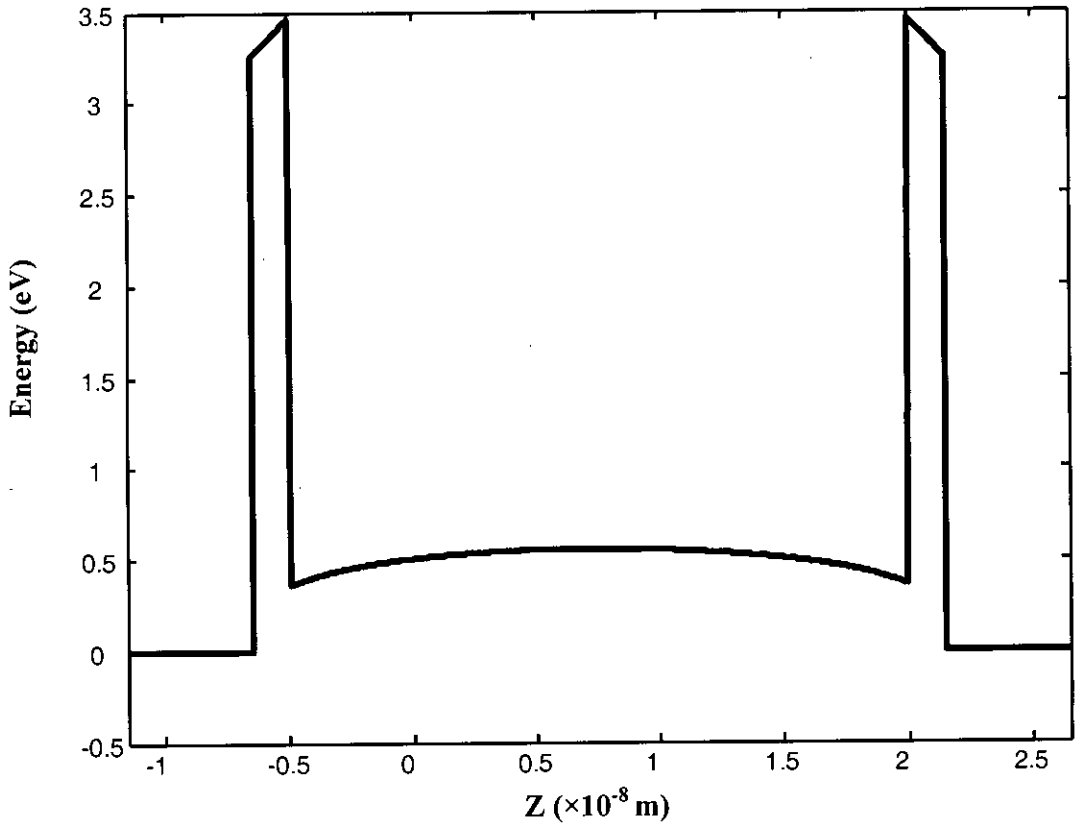

Fig. 1.1 A typical conduction band profile for a double gate n-MOSFET

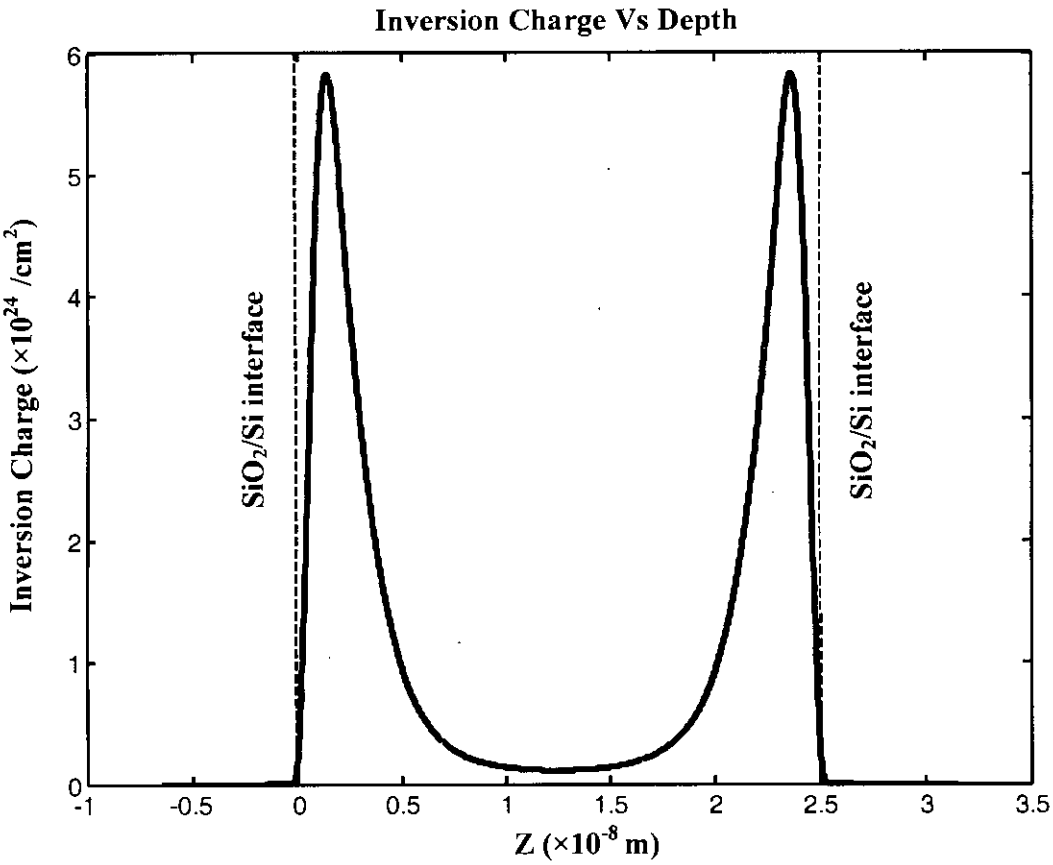

Fig. 1.2 Electron density in silicon near Si/SiO_2 interface as obtained from quantum mechanical (QM) calculation.

Due to this extension of the electron density inside semiconductor, (i) the electric potential value at the interface is greater and (ii) the capacitance and the transconductance are reduced from those predicted by the semi-classical model. At room temperature in deep submicron devices, the QM effects manifest themselves through such measurable device parameters as the inversion layer charge density, threshold voltage and the oxide thickness extracted from Capacitance vs. Voltage (C-V) or tunneling current measurement.

Thus, it is important that the above mentioned inversion layer QM effects are incorporated in deep submicron device models. The use of the traditional or semi-classical technique in device analysis and design, in which these effects are neglected, is inadequate at deep submicron dimensions and will lead to erroneous and misleading prediction of device structure and electrical behavior, such as the physical oxide thickness, threshold voltage, drive current, gate capacitance and electrostatic potential. For this reason, the two-dimensional nature of electrons in inversion layers is studied in detail by considering quantization of carrier energies.

1.3 Literature Review

QM effects in MOS inversion layers arise when high surface electric field makes the quantum well for inversion carrier's very steep and narrow, electron energies are quantized in the direction normal to the interface. In double gate structure energy quantization is always present due to presence of quantum well between two gates. A significant amount of work has been conducted to understand and model the QM effects in single gate MOS devices and double gate also in recent years. In this section, a review of these works is presented.

The first publication on a double gate SOI MOSFET dates back to 1984. The device received the acronym XMOS because of the resemblance of the structure with Greek letter Ξ [10]. This initial paper predicted the superior short-channel characteristics of such a device. The first fabricated double gate SOI MOSFET was the "Fully Depleted Lean-channel Transistor (DELTA, 1989)", where the silicon film stands vertical on its side as shown in Fig. 1.3 [11].

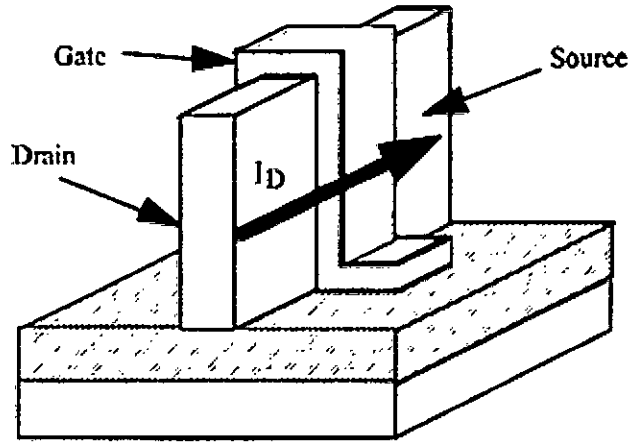

Fig. 1.3 Schematic view of a DELTA FinFET

Later vertical channel double gate SOI MOSFETs (FinFET) [12] was implemented. Volume inversion was discovered in 1987 [6], and the superior transconductance brought about by this phenomenon were first experimentally observed in 1990 in the first practical implementation of a planar double-gate MOSFET called the "Gate-All-Around" (GAA) device [13] as shown in Fig. 1.4.

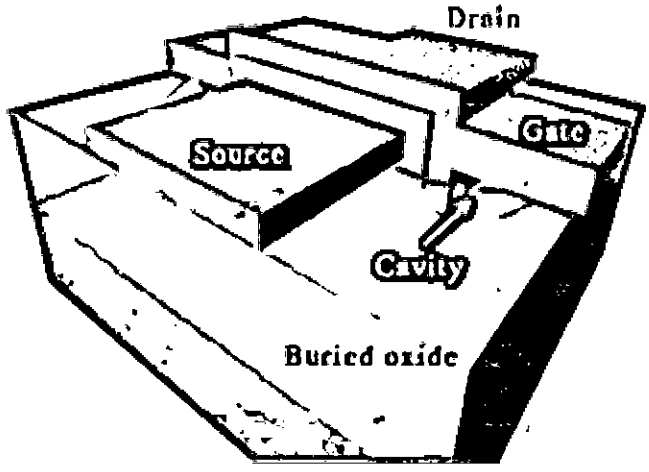

Fig. 1.4 Schematic of a Gate-all-around MOSFET

The structure that theoretically offers the best possible control of the channel region by the gate is the Surrounding-Gate MOSFET. Such a device is usually fabricated using a pillar-like silicon island with a vertical-channel which include the cylindrical thin-pillar transistor (CYNTHIA) [14] as shown in Fig. 1.5 and the pillar surrounding-gate MOSFET [15].

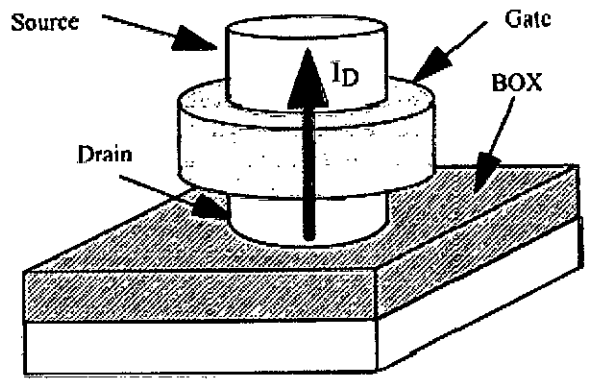

Fig. 1.5 A CYNTHIA/Surrounding-Gate MOSFET structure

The effects of volume inversion in thin-film short-channel SOI MOSFETs and the efficacy of dual-gate operation in enhancing their device performance have been analyzed by Pierret *et at.* [16] using two-dimensional device simulations and one dimensional analytical computations. Their analyses have been restricted to the strong inversion regime, which is the practically useful region of operation of SOI MOSFETs. In this region, they suggested that when compared at constant $Vg - V_t$ values, the dual channel volume inverted devices do not offer significant current-enhancement advantages, other than that expected from the second channel, over the conventional single-channel devices for silicon thickness in the 0.1 μm range.

Suzuki *et al.* [17] established a scaling theory for double-gate SOI MOSFETs, which gives guidance for the device design. They calculated dependence of sub-threshold slope S on device parameters. According to their theory, a device can be designed with a gate length of less than 0.1 μm while maintaining the ideal sub-threshold factor, which is verified numerically with a two-dimensional device simulator. In a latest publication [18], they developed models for short

channel n+ -p+ double-gate SOI MOSFETs by solving a two-dimensional (2-D) Poisson's equation in the channel region, and showed how to design a device with a decreased gate length, suppressing short channel threshold voltage shift ΔV_{th} and sub-threshold swing (S-swing) degradation.

Giorgio Baccarani *et al.* [19] presented a compact model for the Double-Gate MOSFET (DG-MOSFET), which accounts for quantum mechanical effects, including motion quantization normal to the Si-$Si0_2$ interface, band splitting into subbands and non-static effects in the transport model. The model holds both in sub-threshold and strong inversion, and ensures a smooth transition between the two regions.

Hergenrother *et al.* [20] showed that short-channel effects in fully-depleted double gate (DG) and Cylindrical, Surrounding-Gate MOSFETs are governed by the electrostatic potential as confined by the gates, and thus by the device dimensions. For equivalent silicon and gate oxide thicknesses, evanescent-mode analysis indicates that Cyl-MOSFETs can be scaled to 35% shorter channel lengths than DG-MOSFETs.

Jang *et al.* [21] have developed an analytical drain current model for symmetric double-gate SOI MOSFETs using a quasi-two-dimensional Poisson's equation. The model applicable for digital/analog circuit simulation contains the description of the sub-threshold, near threshold and above-threshold regions of operation by one single expression. They considered effects of the source/drain resistance; on important short channel effects such as- velocity saturation, drain induced barrier lowering, channel length modulation, self-heating effect due to the low thermal conductivity of the buried oxide, impact-ionization of MOS devices, parasitic bipolar junction transistor associated with drain breakdown, etc.

Majkusiak *et al.* [22] have analyzed the influence of the semiconductor film thickness in the double-gate silicon-on-insulator (SOI) MOSFET on the electron concentration distribution, electron charge density, threshold voltage, electron effective mobility, and drain current. The consideration of the semiconductor region is based on two descriptions: the "classical" model based on a solution to the Poisson's equation and the "quantum" 'model based on a self-consistent solution to the Schrodinger's and Poisson's equation system. The electron effective mobility and the drain current are calculated with the use of the local mobility model.

Taur [23] has derived a one-dimensional (1-D) analytical solution for an undoped (or lightly-doped) double-gate MOSFET by incorporating only the mobile charge term in Poisson's equation. The solution gives closed forms of band bending and volume inversion as a function of silicon thickness and gate voltage. A threshold criterion has been derived which serves to quantify the gate work function requirements for a double gate CMOS. Then in [3] the solution is applied to both symmetric and asymmetric DG MOSFETs to obtain closed forms of band bending and inversion charge as a function of gate voltage and silicon thickness. It is shown that for the symmetric DG device, "volume inversion" only occurs under sub-threshold conditions, with a slightly negative impact on performance. Comparisons under the same off-state conditions show that the on-state inversion charge density of an asymmetric DG with one channel is only slightly less than that of a symmetric DG with two channels, if the silicon film is thin. From the analytic solutions, expressions for the various components of the equivalent capacitance circuit have been derived for symmetric and asymmetric DG devices.

Fossum *et al.* [24] have developed a compact physics-based quantum-effects model for symmetrical double-gate (DG) MOSFETs of arbitrary Si-film thickness. The model, based on the quantum-mechanical variational approach, not only accounts for the thin Si film thickness dependence but also takes into account the gate-gate charge coupling and the electric field dependence; it can be used for FD SOI MOSFETs as well. The analytical solutions, verified via results obtained from self-consistent numerical solutions of the Poisson and Schrodinger equations, provide good physical insight regarding the quantization and volume inversion due to carrier confinement, which is governed by the Si-film thickness and/or the transverse electric field. A design criterion for achieving beneficial volume-inversion operation in DG devices has quantitatively defined for the first time. Further, the use of their model for aiding optimal DG device design including exploitation of the volume-inversion benefit to carrier mobility is exemplified.

Meindl *et al.* [25] have developed an analytical sub-threshold swing (S) model for symmetric DG MOSFETs using evanescent-mode analysis. Through a concept of effective conducting path, it explains a doping concentration (N_A) dependence of S, providing a unified understanding of previous models and leading to a new model for undoped DG MOSFETs. Expressions of a scale length have been derived, which expedite projections of scalability of DG MOSFETs .

Ernst *et al.* [26] have analyzed the operation of 1-3 nm thick SOI MOSFETs, in double-gate (DG) mode and single-gate (SG) mode (for either front or back channel). They found some typical effects in these ultra-thin MOSFETs such as- threshold voltage variation, large influence of substrate depletion underneath the buried oxide, absence of drain current transients, and degradation in electron mobility. By comparing SG and DG configurations they have shown the superiority of DG-MOSFETs: ideal sub-threshold swing and remarkably improved transconductance (consistently higher than twice the value in SG-MOSFETs). The experimental data and the difference between SG and DG modes have been explained by combining classical models with quantum calculations. They found that the key effect in ultimately thin DG-MOSFETs is volume inversion, which primarily leads to an improvement in mobility, whereas the total inversion charge is only marginally modified.

Wong *et al.* [27] have derived an analytical expression relating the potential and the electric field at the oxide-semiconductor interface of a symmetrical double-gate oxide intrinsic semiconductor-oxide system. The expression is applicable to all regimes of operation. The "turn-on" behavior of the system has been studied and an extrapolated threshold voltage has been defined. Opposite to the behavior of a conventional bulk metal-oxide-semiconductor capacitor realized on a doped substrate, this threshold voltage was shown to decrease with increasing oxide thickness.

Alessandrini *et al.* [28] have developed an analytical model for the electron mobility limited by surface optical phonons and applied to the simulation of ultra-thin SOI MOSFETs. The developed model reproduces the main features of experimental data recently reported in the literature and has been implemented in a conventional device simulator. An application to the analysis of technological options such as doping concentration and silicon thickness in SOI MOSFETs, have been reported.

López-Villanueva *et al.* [29] have investigated the role of the inversion-layer centroid in a DGMOSFET. The expression they have obtained for the inversion charge is similar to that found in conventional MOSFET's, with the inversion-charge centroid playing an identical role. The quantitative value of this magnitude has been analyzed in volume-inversion transistors and compared with the value obtained in conventional MOSFETs. The minority-carrier distribution

has been found to be even closer to the interfaces in volume-inversion transistors with very thin films, and therefore, some of the advantages assumed for these devices are ungrounded.

Lixin Ge *et al.* [30] have developed and demonstrated an analytical total gate capacitance (C_G) model for symmetric double-gate (DG) and fully depleted silicon-on-insulator (FD SOI) MOSFETs of arbitrary Si film have been developed and demonstrated. The model accounts for the effects of carrier energy quantization and inversion-layer screening and is verified via self-consistent numerical solutions of the Poisson and Schrödinger equations. Results provide good physical insight regarding C_G degradation due to quantization and screening governed by device structure and/or transverse electric field for nanoscale DG and FD/SOI MOSFETs. Two limits of C_G at ON-state are then derived when the silicon film thickness (t_{si}) approaches zero and infinity. The effect of inversion-layer screening on C_G, which is significant for ultrathin Si-film DG MOSFETs, is quantitatively defined. The insightful results show that the two-dimensional screening length for DG MOSFETs is independent of the doping density and much shorter than the bulk Debye length as a result of strong structural confinement.

1.4 Objective of the Work

Quantization effects in MOS inversion layer are typically studied by self-consistent solution of coupled Schrödinger and Poisson equations [7, 31].The boundary conditions commonly used for the solution of Schrödinger equation for single gate MOSFET are that the wave function goes to zero at Si-SiO_2 interface and at some point deep inside the bulk [7].The first condition is equivalent to assuming that the potential barrier height at the silicon-oxide interface seen by the inversion carriers is infinity. It is known that the actual barrier height is finite and for electron, this is approximately equal to 3.1 eV. Therefore, there should be some penetration of the wave function into the gate oxide. While this penetration is assumed to be negligible in devices with thick oxide layers, its neglect in deep submicron MOSFETs cannot be justified. Investigation has been done to understand the effects of wave function penetration [32, 33, 34] on single gate MOS device performance. From these studies, we can predict that wave function penetration effects on inversion layer charge, average penetration depth, surface potential and gate capacitance in DG MOSFETs should be more important and significant due to the presence of

two dielectrics or gates. So, some of the previously assumed advantages of volume inversion based on a greater distance to the interfaces may be impractical. Results derived with wave function penetration effects may be of help to assess the true advantages of Double-Gate MOSFETs. However, such an analysis is still missing in the literature.

The objective of this work is to develop a one dimensional (1D) self-consistent Schrödinger - Poisson solver using the appropriate boundary condition to incorporate wave function penetration effects with established accuracy and efficiency. The developed numerical solver will be applied to fully depleted DG MOSFET (both nMOS and pMOS) for analyzing electrostatics of the device such as, inversion layer charge, average penetration depth, surface potential and gate capacitance, and hence wave function penetration effects will be revealed by comparing the results with those of without penetration. Finally, the results will be compared with reported data.

1.5 Organization of the Thesis

Chapter 2 discusses the theory behind this work. At first, the self-consistent modeling of double gate fully depleted MOS structure is described. A numerically efficient and faster technique is presented based on finite element method which incorporates wave function penetration effects into the gate dielectric on both Schrödinger –Poisson equations. Chapter 3 deals with the results and discussions. In this chapter, various results obtained for n-MOSFETs and p-MOSFETs under different condition are reported and discussed. Concluding remarks of this work along with suggestions for the future work are presented in chapter 4.

Chapter 2

Self-Consistent Solution

In this chapter, a modified numerically efficient technique based on the finite element method is presented using FEMLAB. FEMLAB provides a powerful, interactive environment for modeling and solving scientific and engineering problems based on partial differential equations using finite element method. The accuracy and efficiency of FEMLAB as the self-consistent solver has been verified for single gate MOS devices on (111) and (100) Si surfaces [35]. A modified version of this solver is used in this work. The solver has the capability of analyzing high K dielectrics as well as symmetric and asymmetric double gate MOS structures.

2.1 Single-gate MOSFET

A field effect transistor (FET) operates as a conducting semiconductor channel with two ohmic contacts – the source and the drain – where the number of charge carriers in the channel is controlled by a third contact – the gate. In the vertical direction, the gate-channel- substrate structure (gate junction) can be regarded as an orthogonal two-terminal device, which is either a MOS structure or a reverse-biased rectifying device that controls the mobile charge in the channel by capacitive coupling (field effect). Examples of FETs based on these principles are metal-oxide-semiconductor FET (MOSFET), junction FET (JFET), metal-semiconductor FET (MESFET), and hetero-structure FET (HFETs). In all cases, the stationary gate-channel impedance is very large at normal operating conditions.

The basic FET structure is shown schematically in Fig. 2.1. The most important FET is the MOSFET. In silicon MOSFET, the gate contact is separated from the channel by an insulating silicon dioxide (SiO_2) layer. The charge carriers of the conducting channel constitute an inversion charge, that is, electrons in the case of a *p*-type substrate (*n*-channel device) or holes in the case of an *n*-type substrate (*p*-channel device), induced in the semiconductor at the silicon-insulator interface by the voltage applied to the gate electrode. The electrons enter and exit the

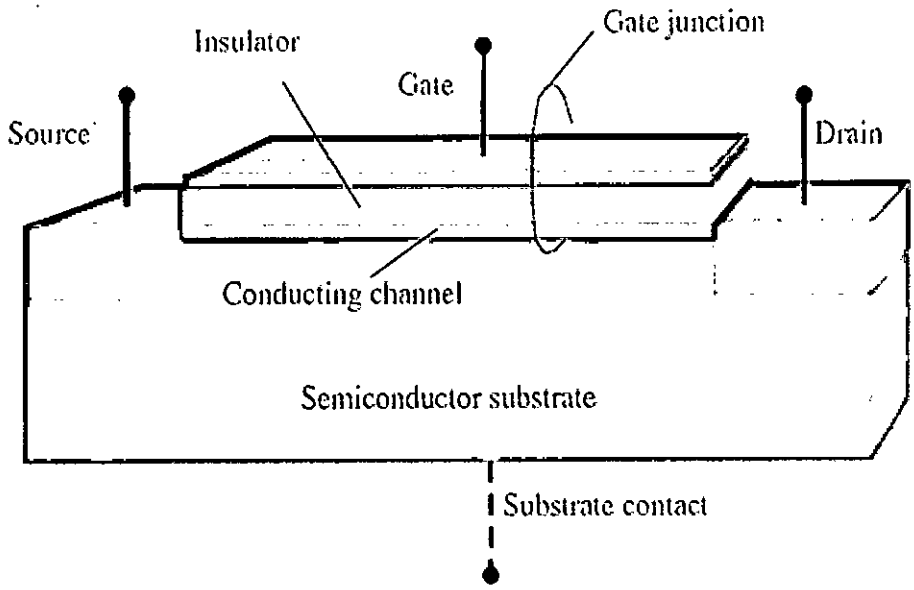

Fig. 2.1 Basic structure of SG MOSFET

channel at *n*+ source and drain contacts in the case of an *n*-channel MOSFET, and at *p*+ contacts in the case of a *p*-channel MOSFET.

2.1.1 The MOS Capacitor

To understand the MOSFET, we first have to analyze the MOS capacitor, which constitutes the important gate-channel-substrate structure of the MOSFET. The MOS capacitor is a two-terminal semiconductor device of practical interest in its own right. As indicated in Fig. 2.2, it consists of a metal contact separated from the semiconductor by a dielectric insulator. An additional ohmic contact is provided at the semiconductor substrate. Almost universally, the MOS structure utilizes doped silicon as the substrate and its native oxide, silicon dioxide, as the insulator. In the Si/SiO_2 system, the density of surface states at the oxide–semiconductor interface is very low compared to the typical channel carrier density in a MOSFET. Also, the insulating quality of the oxide is quite good.

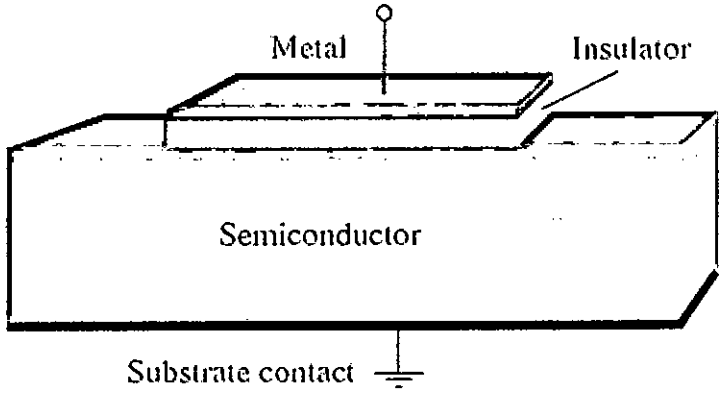

Fig. 2.2 Schematic view of a MOS capacitor

We assume that the insulator layer has infinite resistance, preventing any charge carrier transport across the dielectric layer when a bias voltage is applied between the metal and the semiconductor. Instead, the applied voltage will induce charges and counter charges in the metal and in the interface layer of the semiconductor, similar to what we expect in the metal plates of a conventional parallel plate capacitor. However, in the MOS capacitor we may use the applied voltage to control the type of interface charge we induce in the semiconductor – majority carriers, minority carriers, and depletion charge. Indeed, the ability to induce and modulate a conducting sheet of minority carriers at the semiconductor–oxide interface is the basis for the operation of the MOSFET.

2.1.2 Basic MOSFET Operation

In the MOSFET, an inversion layer at the semiconductor–oxide interface acts as a conducting channel. For example, in an *n*-channel MOSFET, the substrate is *p*-type silicon and the inversion charge consists of electrons that form a conducting channel between the *n*+ ohmic source and the drain contacts. At DC conditions, the depletion regions and the neutral substrate provide isolation between devices fabricated on the same substrate. As described above for the MOS capacitor, inversion charge can be induced in the channel by applying a suitable gate voltage relative to other terminals. The onset of strong inversion is defined in terms of a threshold voltage V_T being applied to the gate electrode relative to the other terminals. In order to assure

that the induced inversion channel extends all the way from source to drain, it is essential that the MOSFET gate structure either overlaps slightly or aligns with the edges of these contacts (the latter is achieved by a self-aligned process). Self-alignment is preferable since it minimizes the parasitic gate-source and gate-drain capacitances. When a drain-source bias V_{DS} is applied to an *n*-channel MOSFET in the above threshold conducting state, electrons move in the channel inversion layer from source to drain. A change in the gate-source voltage V_{GS} alters the electron sheet density in the channel, modulating the channel conductance and the device current.

For $V_{GS} > V_t$ in an *n*-channel device, the application of a positive V_{DS} gives a steady voltage increase from source to drain along the channel that causes a corresponding reduction in the local gate-channel bias V_{GX} (here X signifies a position x within the channel). This reduction is greatest near drain where V_{GX} equals the gate-drain bias V_{GD}. Somewhat simplistically, we may say that when $V_{GD} = V_t$, the channel reaches threshold at the drain and the density of inversion charge vanishes at this point. This is the so-called pinch-off condition, which leads to a saturation of the drain current I_{ds}. The corresponding drain-source voltage, $V_{DS} = V_{SAT}$, is called the saturation voltage. Since $V_{GD} = V_{GS} - V_{DS}$, we find that $V_{SAT} = V_{GS} - Vt$. When $V_{DS} > V_{SAT}$, the pinched-off region near drain expands only slightly in the direction of the source, leaving the remaining inversion channel intact. The drain current in saturation remains approximately constant, given by the voltage drop V_{SAT} across the part of the channel that remains in inversion. The voltage $V_{DS} - V_{SAT}$ across the pinched-off region creates a strong electric field, which efficiently transports the electrons from the strongly inverted region to the drain.

Typical current–voltage characteristics of a long-channel MOSFET, where pinch-off is the predominant saturation mechanism, are shown in Fig. 2.3. However, with shorter MOSFET gate lengths, typically in the sub-micrometer range, velocity saturation will occur in the channel near drain at lower V_{DS} than that causing pinch-off. This leads to more evenly spaced saturation characteristics than those shown in this plot.

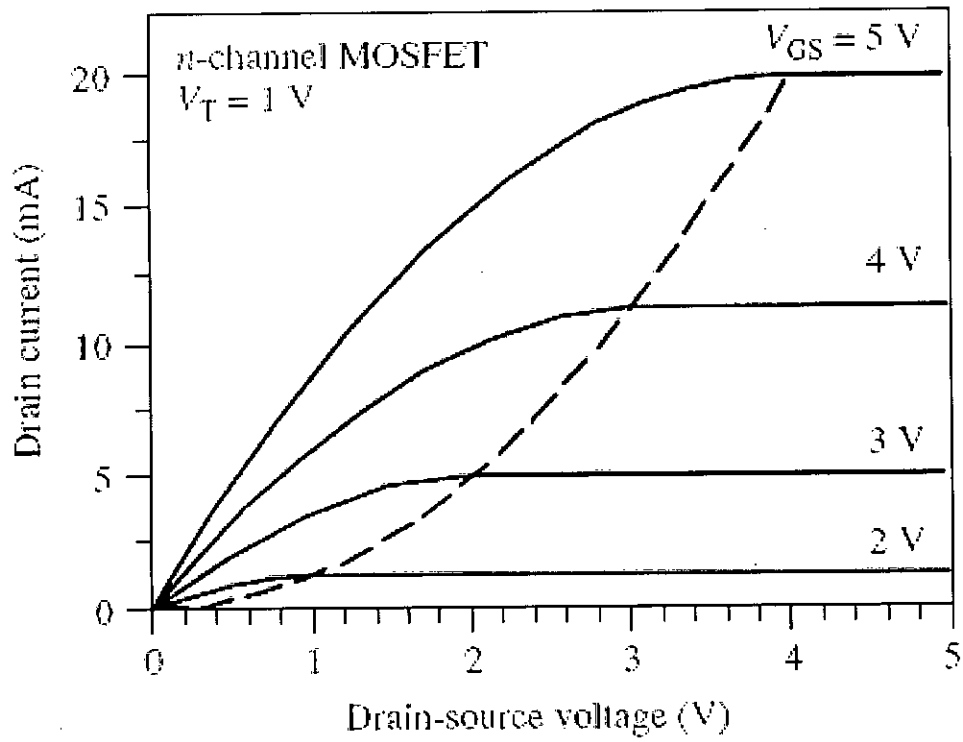

Fig. 2.3 Current–voltage characteristics of an *n*-channel MOSFET

2.1.3 Limitation of Scaled MOSFET

- **Effect of Reducing Channel Length: Drain Induced Barrier Lowering**

In devices with long channel lengths, the gate is completely responsible for depleting the semiconductor .In very short channel devices, part of the depletion is accomplished by the drain and source bias. Since less gate voltage is required to deplete the semiconductor, the barrier for electron injection from source to drain decreases. This is known as drain induced barrier lowering (DIBL).

DIBL results in an increase in drain current at a given gate voltage V_{GS}. Therefore V_t decreases as channel length decreases. Similarly, as drain voltage V_{DS} increases more semiconductor region is depleted by the drain bias, and hence I_d increases and V_t decreases.

- **Carrier Mobility: Velocity Saturation**

The mobility of the carriers reduces at higher electric fields normally encountered in small channel length devices due to velocity saturation effects. As the channel length, L, is reduced while the supply voltage is not, the tangential electric field will increase, and the carrier velocity may saturate at Ec≈10^4 V/cm for electrons. Hence for n-MOSFET with L < 1 μm, velocity saturation causes the channel current to reach saturation before $V_{DS} = V_{GS} - V_t$. Ec ≈ 5×10^4 V/cm for holes, hence velocity saturation for p-MOSFET will not become important until L < 0.25 μm.

- **Sub-threshold Conduction**

When the surface is in weak inversion ($V_{GS} < V_t$), a conducting channel starts to form and a low level of current flows between source and drain. As a result, drain leakage current and static power loss increases. Hence circuit stability decreases.

- **Hot Carrier Effects**

Hot-carrier effects are among the main concerns when shrinking FET dimensions into the deep sub-micrometer regime. Reducing the channel length while retaining high power supply levels, known as constant voltage scaling, results in increased electric field strengths in the channel, causing acceleration and heating of the charge carriers. The free carriers passing through the high-field can gain sufficient energy to cause several hot-carrier effects. This can cause many serious problems for the device operation. Some of the manifestations of hot electrons on device operation are breakdown and substrate current caused by impact ionization, creation of interface states, gate current resulting from hot-electron emission across the interface barrier, oxide charges owing to tunneling of charge carriers into oxide states, and photocurrents caused by electron–hole recombination with emission of photons. The substrate current resulting from electron–hole pair generation may overload substrate-bias generators, introduce snapback breakdown, cause CMOS latch-up, and generate a significant increase in the sub-threshold drain current.

2.2 Features of DG MOSFET

In conventional bulk MOSFETs, SCEs are caused by the lateral electric fields from the source to channel and drain to channel. As L decreases, the lateral fields terminate on more charge further into the channel, which essentially steals the charge that would normally be terminated by the gate voltage in a long-channel device. This stealing of charge by the lateral fields effectively lowers the source-to-channel barrier, which controls the conduction of electrons from source to drain. To limit this charge stealing, and thus mitigate SCEs, heavy channel doping is exploited in bulk MOSFETs. As the gate length is scaled to 50 nm and below, the required channel doping concentration is expected to be on the order of 10^{18} cm^{-3} and above. These extremely high doping levels, however, lead to

i) Severe degradation of the carrier mobility as the impurity scattering becomes dominant [36] and

ii) Severe threshold voltage variations due to random microscopic fluctuations of dopant atoms [37].

The DG MOSFET does not require channel doping for SCE control. Instead, this novel device uses a second gate and a fully depleted silicon film as the channel to enhance the electrostatic control of the gates over the channel, which effectively suppresses the impact of the source/drain. The thin silicon film is undoped or lightly doped (typical doping concentration $N_A<10^{18}$ cm^{-3} [19]) to assure the full depletion condition. For the most effective SCE control, the two gate-oxide layers are equally thin. Use of an identical material for both gates results in a symmetric DG MOSFET.

A double-gate-silicon-on-insulator DGSOI structure consists, basically, of a silicon slab sandwiched between two oxide layers as shown Fig. 2.2. A metal or a poly-silicon film contacts act as gate on each oxide which can generate an inversion region near the Si-$Si0_2$ interfaces with an appropriate bias. Thus we would have two conventional MOSFETs sharing the substrate, source, and drain.

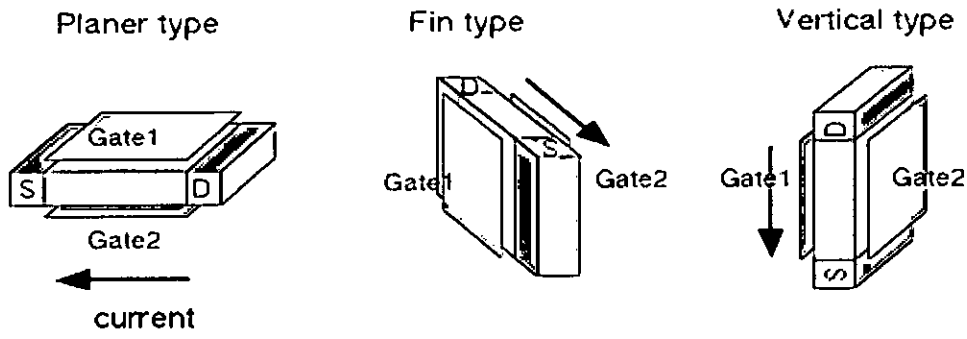

Fig. 2.4 Some feasible schematic view of DGMOS structure

The outstanding feature of these structures lies in the concept of volume inversion, introduced by Balestra *et al* [6]. If the Si film is thicker than the sum of the depletion regions induced by the two gates, no interaction is produced between the two inversion layers, and the operation of this device is similar to the operation of two conventional MOSFETs connected in parallel. However, if the Si thickness is reduced, the whole silicon film is depleted and an important interaction appears between the two potential wells. In such conditions the inversion layer is formed not only at the top and bottom of the silicon slab i.e., near the two silicon-oxide interfaces, but throughout the entire silicon film thickness. The device under this condition operates in 'volume inversion', i.e., carriers are no longer confined at interfaces, but distributed throughout the entire silicon volume. It has been reported [16, 23, 40] that volume inversion presents some significant advantages, as mentioned below:

i. Enhancement of the number of minority carriers

ii. Increase in carrier mobility and velocity due to reduced influence of scattering associated with oxide and interface charges and surface roughness and hence increase in drain current and transconductance

iii. Decrease of low frequency noise

iv. A great reduction in hot-carrier effects.

2.3 Self-consistent Solution

With the advancement of semiconductor technology, device dimensions are entering into the nanoscale regime; quantum mechanical effects are playing a growing role in device operations and performance. So semi-classical models are no longer valid and quantum mechanical modeling is inevitable. Although the quantum corrections improve the classical data, these approaches are unable to model or predict all quantum mechanical effects. In a fully quantum mechanical model the coupled Schrödinger and Poisson equations are solved self consistently [7]. The Schrödinger equation is solved under the effective mass approximation. The boundary condition of the Schrödinger and Poisson equations is also a critical issue. To calculate quantum mechanical charge distribution in MOS devices incorporating the wave function penetration effect within the oxide layer of MOS devices an open boundary condition is a must for the solution of Schrödinger equation [32]. In the absence of suitable boundary conditions, zero penetration of wave function into gate oxide is assumed in the simulation of even deep submicron MOSFETs. While an open boundary condition can be neglected in devices with thick oxide layers, its negligence in deep submicron MOSFETs cannot be justified.

In this section, the solution procedure is portrayed for a dual gate n-MOS structure shown in Fig. 2.5 in the inversion region. FEMLAB with MATLAB has been used as the Partial Differential Eqn. (PDE) solver (suitable for linear or nearly linear problems), for the self-consistent solution.

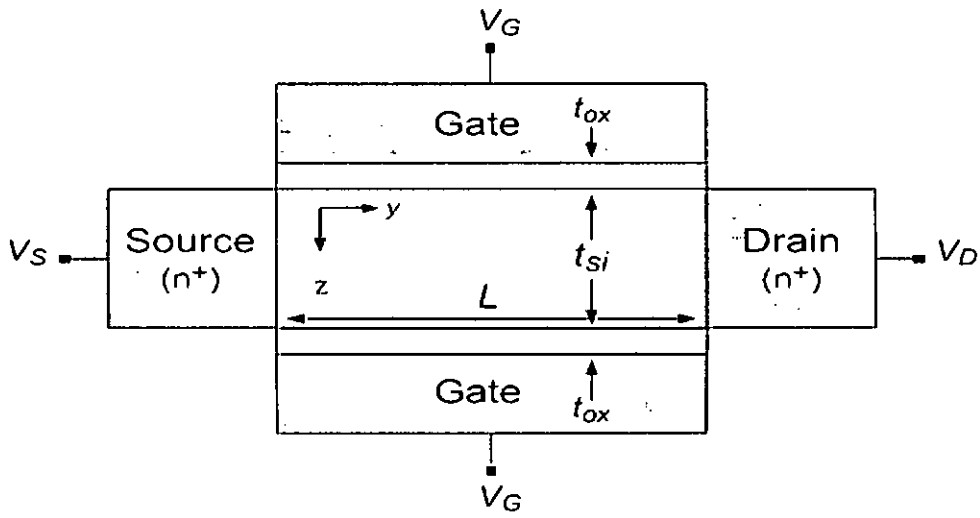

Fig. 2.5 Double-Gate MOS 2-D cross section

The classical PDEs coefficient form in multiphysics mode is used for the Poisson and Schrödinger equation. Poisson equation in coefficient form is given in FEMLAB as:

$$-\nabla.(c\nabla u) = f \tag{2.1}$$

Where c, u and f indicate permittivity of the sub domain, electrostatic potential and charge density respectively. Using relevant parameters of MOS structures (2.1) can be written as-

$$-\varepsilon_0 \varepsilon \frac{d^2 v(z)}{dz^2} = q[p(z) - n(z) + N_D - N_A] \tag{2.2}$$

Where $n(z)$, $p(z)$ are the electron, hole concentration and N_D, N_A are the ionized donor, acceptor concentration respectively. ε is the relative dielectric constant of the material and ε_0 is the permittivity of free space.

The electron concentration $n(z)$ is obtained for n-MOS structure according to the following expression:

$$n(z) = \sum_{ij} N_{ij} \, |\psi_{ij}(z)|^2 \tag{2.3}$$

Where,

$$N_{ij} = \frac{n_{vi} m_{di} kT}{\pi \hbar^2} \ln[1 + \exp(\frac{E_F - E_{ij}}{kT})] \tag{2.4}$$

$$N_{inv} = \Sigma N_{ij} \tag{2.5}$$

And

$$E_F = E_{Fbulk} + V_G \tag{2.6}$$

Where N_{ij} is the carrier concentration in the jth subband of the ith valley, n_{vi} and m_{di} are the *ith* valley degeneracy and the *i*th density-of-states effective mass in Si. N_{inv} is the total inversion carrier concentration and E_F is the Fermi energy. E_{ij} and ψ_{ij} are the eigenvalue and the eigenfunction of an electron in the *j*th energy level of the *i*th valley, which are obtained as a solution of the one-dimensional Schrödinger equation.

Schrödinger equation in coefficient form is defined in FEMLAB as:

$$-\nabla.(c\nabla u) + au = \lambda u \tag{2.7}$$

In (2.7) a, u and λ are electrostatic potential, eigen function and eigen energies respectively Using relevant parameters of effective mass Schrödinger equation for one dimensional MOS structure quantum well (2.7) can be written as-

$$[-\frac{\hbar^2}{2m^*}\frac{d^2}{dz^2} + v(z)]\psi_{ij}(z) = E_{ij}\psi_{ij}(z) \tag{2.8}$$

At first, the device geometry (the fully depleted double gate structure) is defined as shown in Fig. 2.6 in FEMLAB and the trial potential as presented in Fig. 2.7 is obtained by solving (2.1) using the full depletion approximation assuming zero mobile charge density i.e. *n(z)*=0 in (2.2) with appropriate boundary condition at each interface through FEMLAB linear PDE solver.

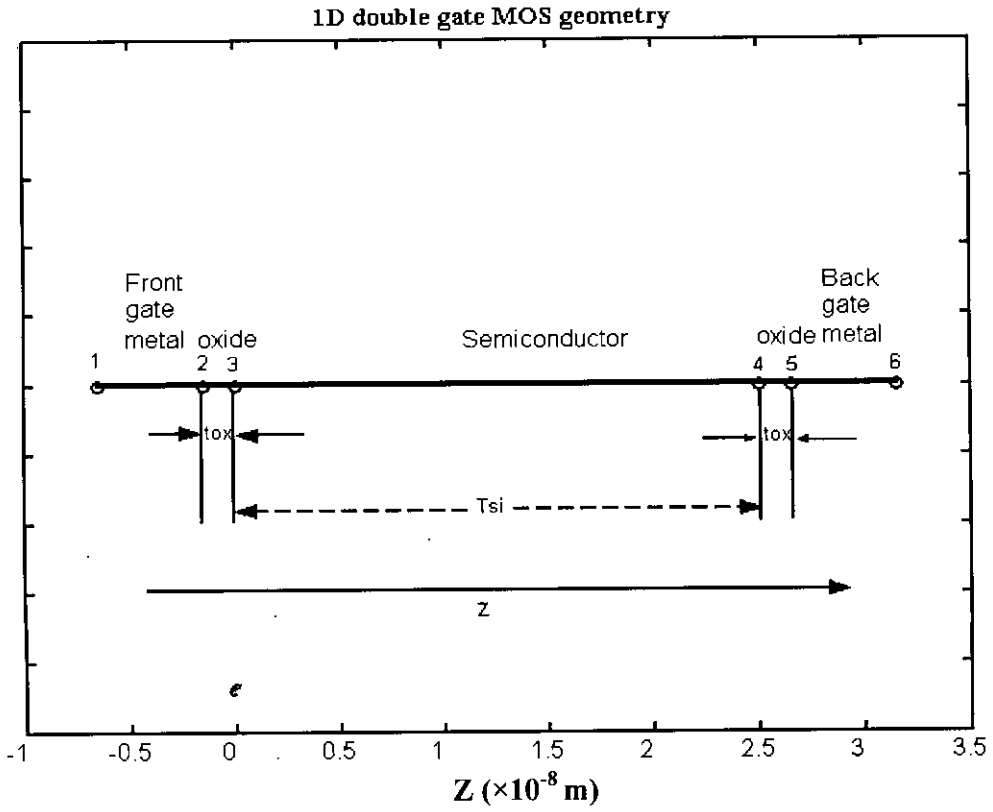

Fig. 2.6 1D geometry of Double Gate MOS structure

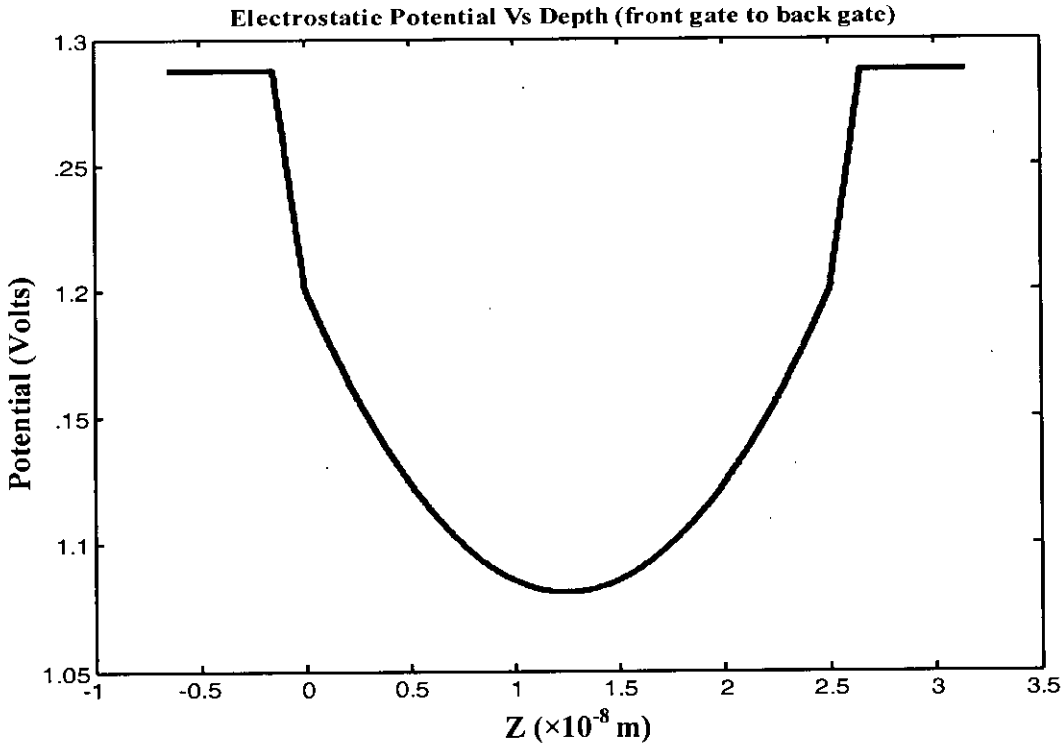

Fig. 2.7 Trial potential from full depletion approximation

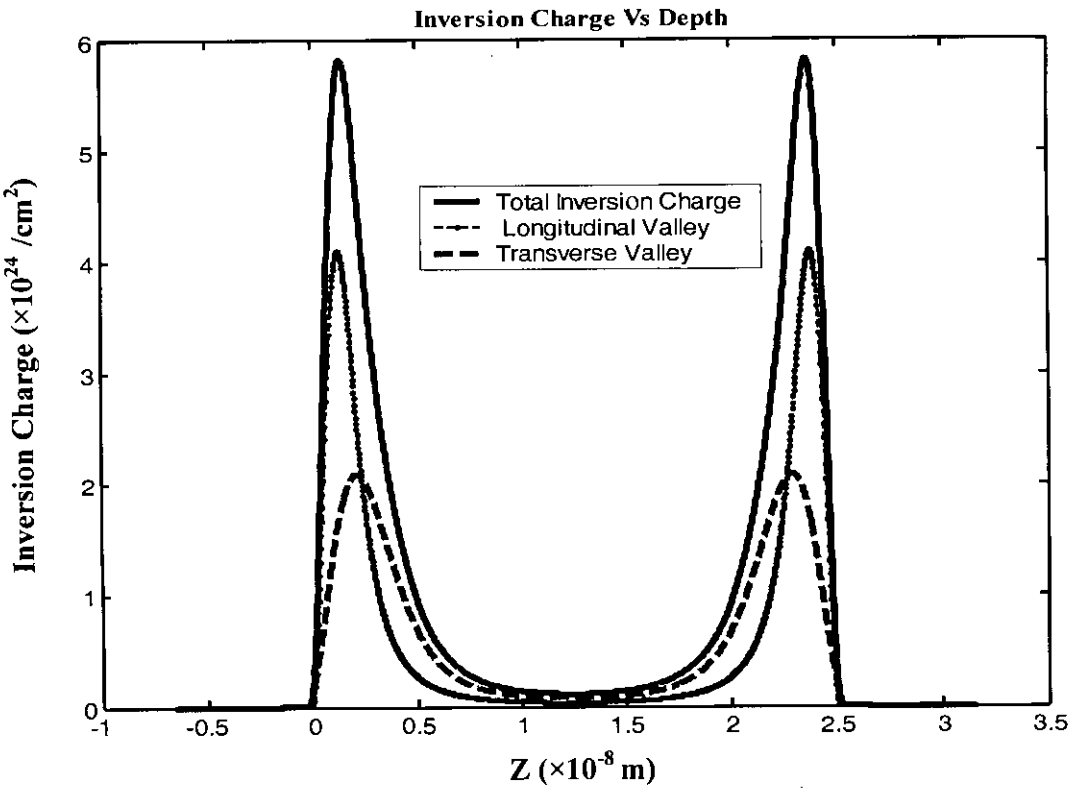

Fig. 2.8 Inversion charge density as a function of depth, z

The boundary conditions used for Poisson equation are-

Dirichlet boundary condition for boundary points 1, 2, 5, 6 and Neumann boundary condition for 3, 4 interfaces.

A discontinuous electric field boundary condition can be easily set with Neumann boundary condition in FEMLAB. Then the charge density profile *n(z)* is determined from Eq. (2.3) by solving (2.7) using FEMLAB eigen-value solver with Neumann boundary condition (needed for open boundary condition to consider penetration effect) as shown in Fig. 2.8.

This charge density profile is added to the source term of Poisson equation and then (2.1) and (2.7) are solved iteratively until the given convergence criteria [for successive iteration, change in electrostatic potential at any node point should be less than 10^{-8} volts] are fulfilled. Hence we get the actual band profile presented in Fig. 2.9 and electrostatic potential profile incorporating wave function penetration as demonstrated in Fig. 2.10. If the solution is to run without penetration effect, we just increase the barrier height in the oxide region to a very large value (e.g. 4000 eV) that practically can be considered as infinity.

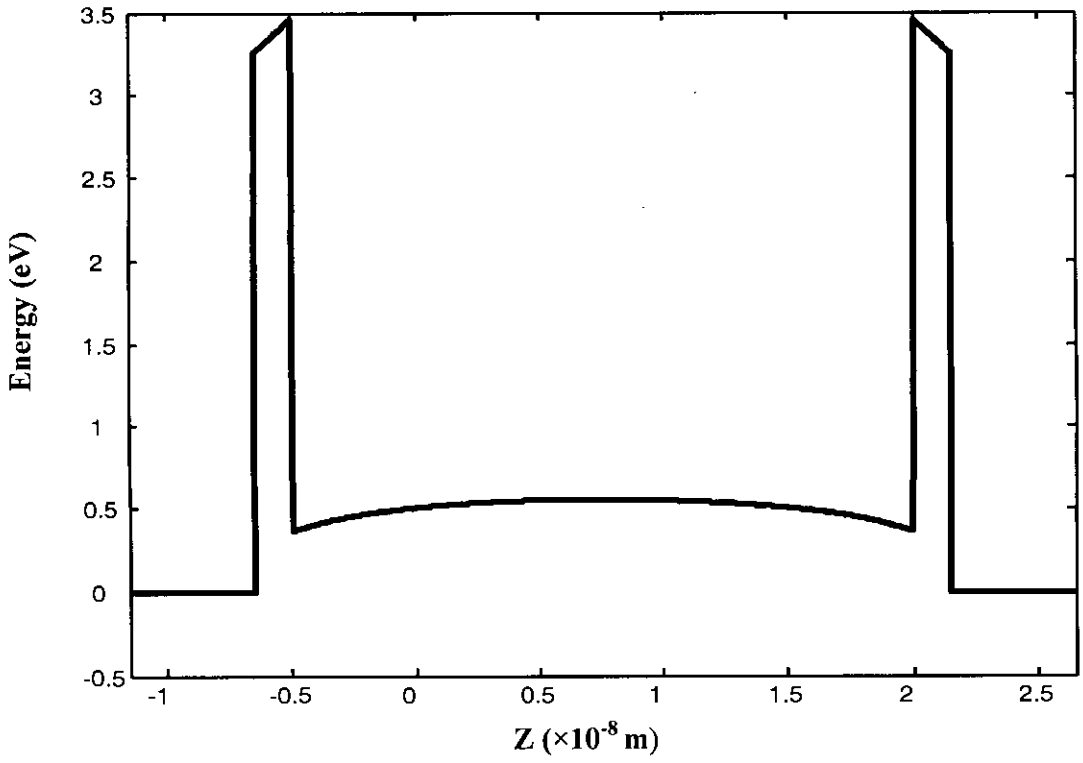

Fig. 2.9 Actual band diagram for the simulated structure

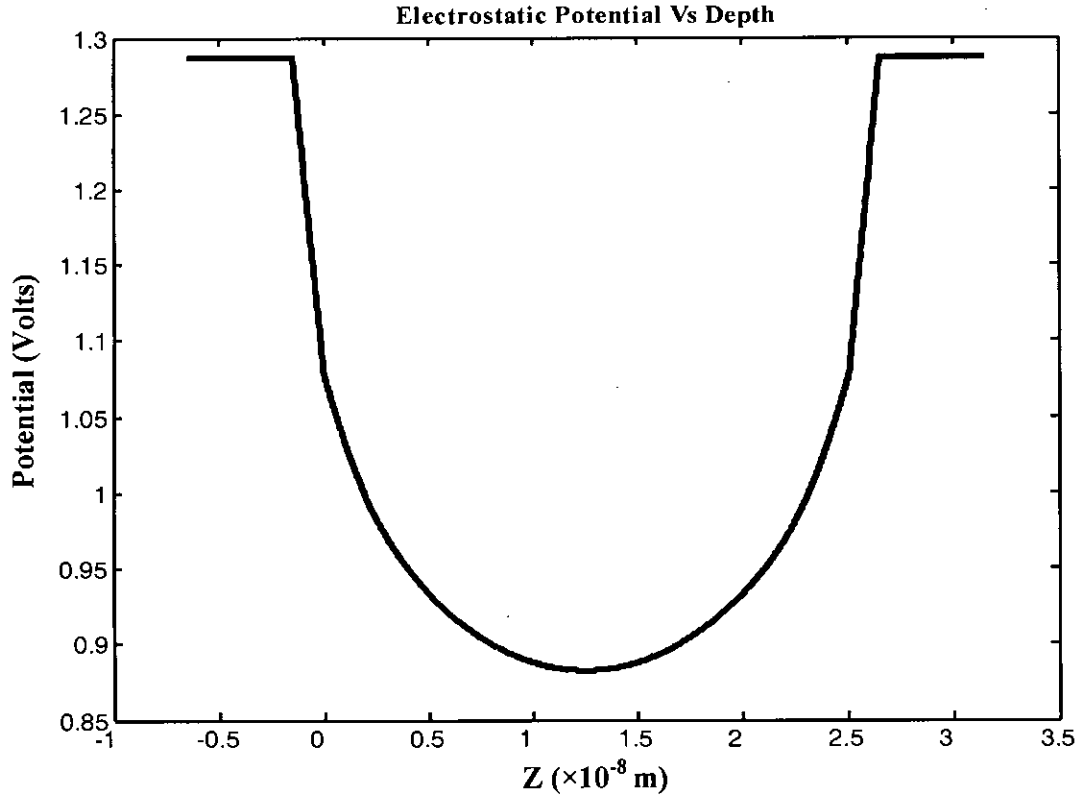

Fig. 2.10 Actual potential profile for the simulated structure

Gauss-Seidel iteration method has been used for the numerical convergence. The weighting factor should be greater than 0.9. With the increase of weighting factor the assurance of convergence increases but the simulation become slower and more iteration is needed. Throughout this thesis, 0.95 is used as the Gauss-Seidel update coefficient. e.g. if 'alpha' is the weighting factor then the updated profile is calculated as-

Vpot=Vold × alpha + Vnew × (1-alpha)

Where, Vpot is the new interpolated profile

Vold is the previous profile

Vnew is the new calculated profile

All the simulation results presented in this chapter has been generated for $N_A=10^{18}$ /cm^3, Tsi=25nm, Tox=1.5 nm and V_G=1.2875 volts.

Detail flowchart of the solution procedure is given in appendix A.

Chapter 3

Results and Discussion

The results of the self-consistent calculation for double gate MOS devices considering the effects of wave function penetration are presented in this chapter. The self-consistent calculations for both double gate n-MOSFETs and p-MOSFETs have been performed on (100) crystal plane.

In MOS devices, for the chosen interface that lies in the (100) crystal planes, the effective mass tensor becomes diagonal in the co-ordinate system which has its z-axis perpendicular to the surface pointing into the semiconductor. It is known that silicon has six ellipsoidal constant energy surfaces in the conduction band. The (111) surfaces have only one ladder of subbands with degeneracy 6 in the direction normal to the interface, since all the valleys have the same orientation with respect to the surface. For the (100) oriented surfaces, m_z for electrons can take the value of the longitudinal effective mass, m_l, for the two bulk constant energy ellipsoid perpendicular to the surface giving rise to a two-fold degenerate subband ladder and the value of the transverse effective mass, m_t, for the other four ellipsoids, giving rise to a four-fold degenerate ladder. The valleys which present the higher effective mass perpendicular to the surface have the lowest kinetic energy and lowest energy levels. Effective mass approximation has been found to be accurate in describing the quantization effects of electrons in a MOS inversion layer [38]. The values of different parameters used in the calculation are taken from Ref. [7] and are summarized in Table 3.1.

Table 3.1: Effective masses of electrons in different valleys.

Surface	(100)	
Valleys	m_l	m_t
Degeneracy, n_v	2	4
Normal mass, m_z/m_o	0.916	0.190
Density of state mass, m_d/m_O	0.190	0.417

It is known that the energy band structure for holes is non-parabolic. So, it is disputed to represent the valance band within the effective mass approximation. A first principle formalism has been used to completely describe the valance band structure including the periodic lattice potential [38]. But this technique is very complicated and is numerically inefficient. On the other hand, bulk effective mass approximation has been found to be accurate in describing the inversion layer capacitance for holes [39]. In this study, we also use the bulk effective mass approximation of Refs. [31, 39].

The constant-energy surfaces of the light hole and the heavy hole bands are represented by,

$$E_h = \left(\frac{\hbar^2 k^2}{2m_o}\right)\left[A \mp \left(B^2 + C^2\left(\frac{k_x^2 k_y^2 + k_y^2 k_z^2 + k_z^2 k_x^2}{k^4}\right)\right)^{\frac{1}{2}}\right] \tag{3.1}$$

and is reckoned positive downwards into the valance band. Here, + and - corresponds to the light hole and heavy hole bands, respectively. The parameters A, B, C are physical constants which has been determined experimentally in Ref. [31].

For the split-off band holes, the constant energy surfaces are isotropic and centered around Γ(zone center). With the three types of hole bands, we get three energy ladders. In the bulk, the light and heavy hole bands are degenerate at the Γ point (valance band edge), while the third one is separated from the other two by $\Delta E = 44$ meV due to spin-orbit coupling.

The effective mass perpendicular to Si/SiO_2 interface, m_z and density-of-states effective mass, m_d at the valance band edge on a (100) surface are reported in Refs. [31, 39]. The values of the effective masses for holes in (100) silicon used in this study are listed in Table 3.2.

Table 3.2: Effective masses for different types of holes.

Valance band	m_z/m_o	m_d/m_o
Heavy hole	0.29	0.433
Light hole	0.20	0.169
Split-off hole	0.29	0.433

3.1 n-MOS Devices on (100) silicon

Self-consistent calculations for n-MOS devices on (100) silicon are presented in this section. All the results are calculated at room temperature. Values of different parameters for silicon are taken from Ref. [7] and Table-3.1. The potential barrier height at silicon-oxide interface is considered to be 3.1 eV. Electron effective mass in oxide is assumed to be $0.5m_o$ with a parabolic dispersion relationship. Aluminum is considered as the gate electrode with a work function equal to 4.1 eV.

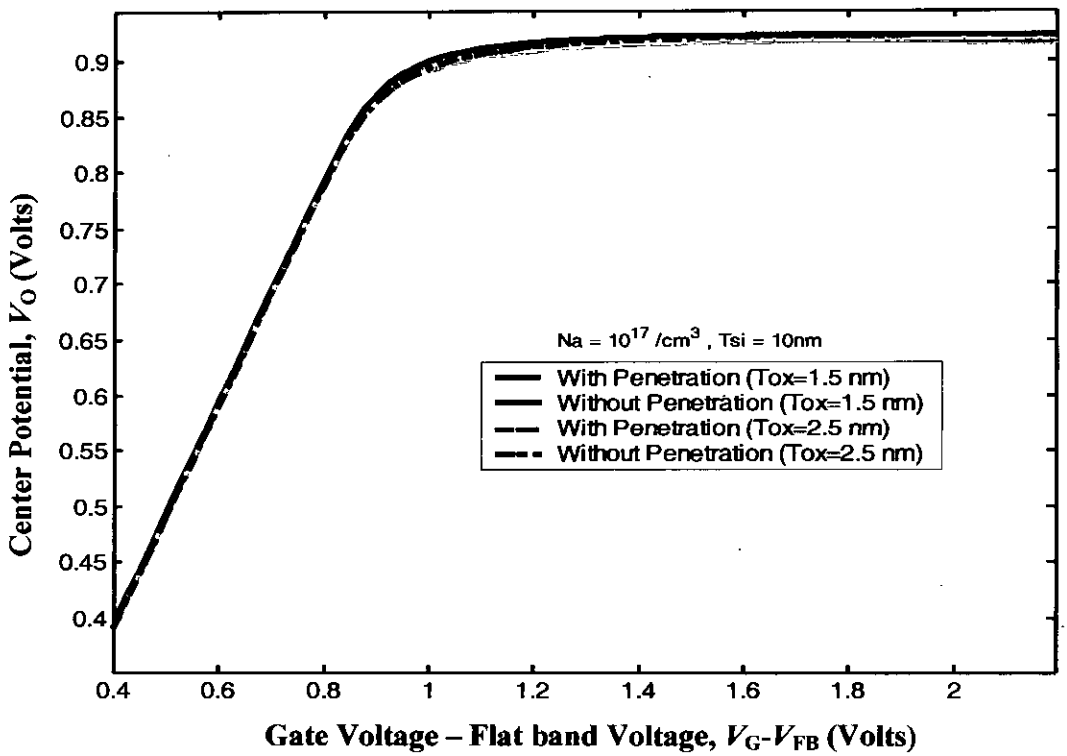

Fig. 3.1 Center Potential, V_O as function of gate voltage for different oxide thickness, Tox

Same voltage is applied to a symmetric DG MOSFET at the two gates having the same work function. At zero gate voltage, the position of the silicon bands is largely determined by the gate work function, because as long as the thin silicon is lightly doped and the depletion charge is negligible, the bands remain essentially flat throughout the thickness of the film. Since there is no contact to the silicon body, the energy levels are referenced to the electron quasi-Fermi level or the conduction band of the n+ source-drain.

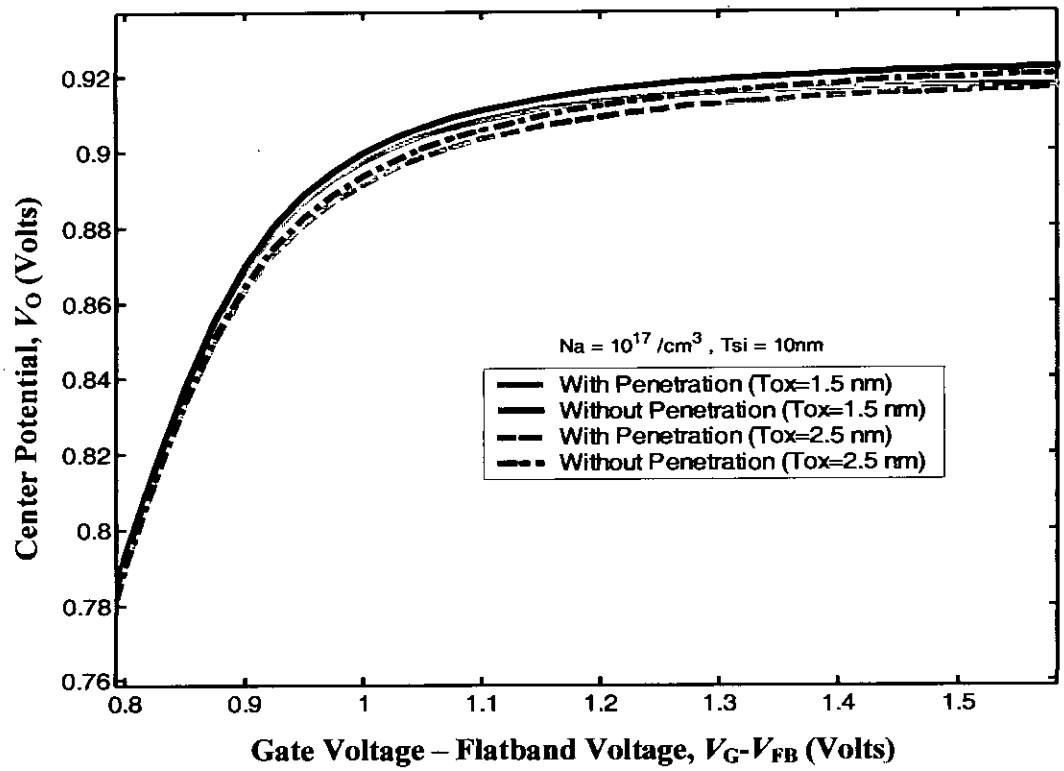

Fig. 3.2 Center Potential, V_O as function of gate voltage for different Tox

(zoomed view)

As the gate voltage increases toward the threshold voltage mobile charge or electron density becomes appreciable when the conduction band of the silicon body approaches the conduction band of the source-drain. Fig. 3.1 and 3.2 shows the variation of center potential with the variation of gate voltage for doping density (N_A) of 10^{17}/cm^3 and silicon thickness (Tsi) of 10 nm of a fully depleted symmetric double gate MOSFET. Blue lines correspond to V_O with penetration effects and black lines correspond to those without penetration obtained from self-consistent calculations. Numerical results show that the center potential is very weekly depends on oxide thickness. Initially, under weak inversion center potential increases linearly with applied voltage and in the strong inversion region it remains almost constant as predicted by analytical semi-classical results [23]. Self consistent results shows that penetration effect on V_O is negligible in weak inversion but overestimates V_O in strong inversion (in this case, up to a maximum value of 0.005V)

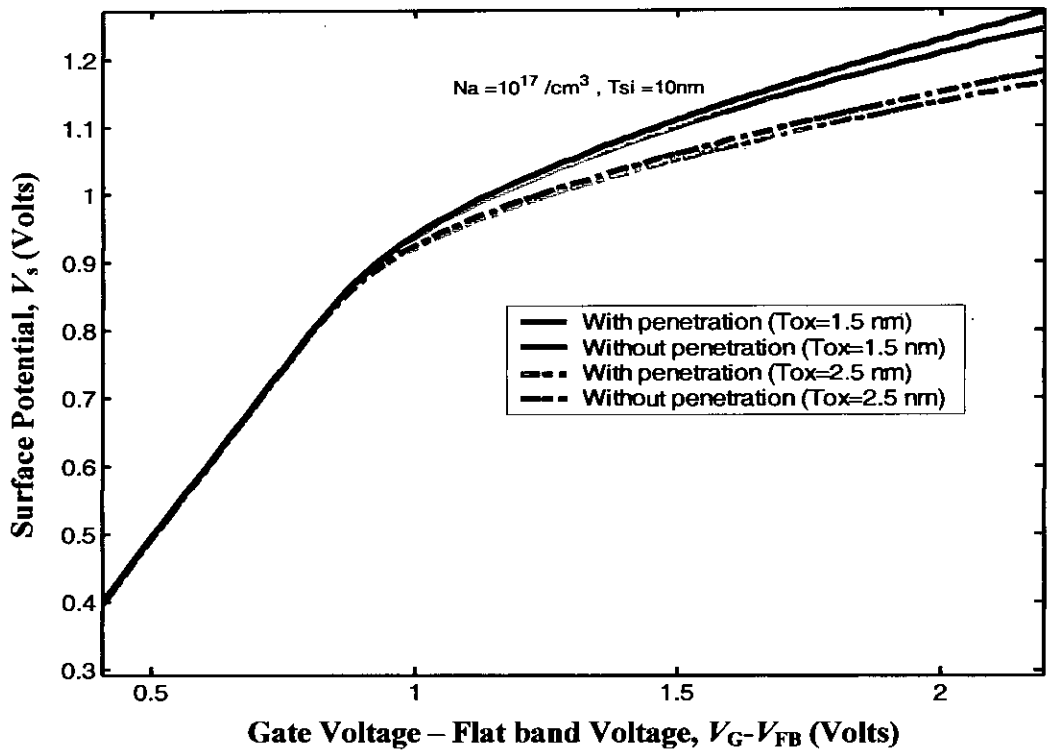

Fig. 3.3 Surface Potential, V_S as function of gate voltage for different oxide thickness, Tox

Fig. 3.3 shows the variation of surface potential (V_S) for the same structure used in Fig. 3.1.It is seen that penetration effect reduces the surface potential. In weak inversion, semi-classically it has been shown that due to volume inversion V_S and V_O coupled together and V_O is equal to V_S [23]. Quantum calculation suggests, V_S and V_O are strongly coupled but not equal in weak inversion as inversion charge (see Fig. 1.2) is not uniformly distributed in the silicon region. In strong inversion, surface potential increases almost linearly whereas center potential remains constant. With increasing oxide thickness surface potential decreases whereas reported literatures [29, 30] with no penetration effects which assume zero boundary condition for estimating eigen states at oxide-silicon surface would result no variation for oxide charge that penetrates into the oxide layers.

Fig. 3.4 and Fig. 3.5 show variations of V_O and V_S for different silicon film thickness as a function of gate voltage. Penetration effect for same thickness is similar to that of oxide variation. With the increasing Tsi, V_S and V_O decreases in weak inversion. But, V_S saturates in strong inversion and shows no variation with silicon body thickness.

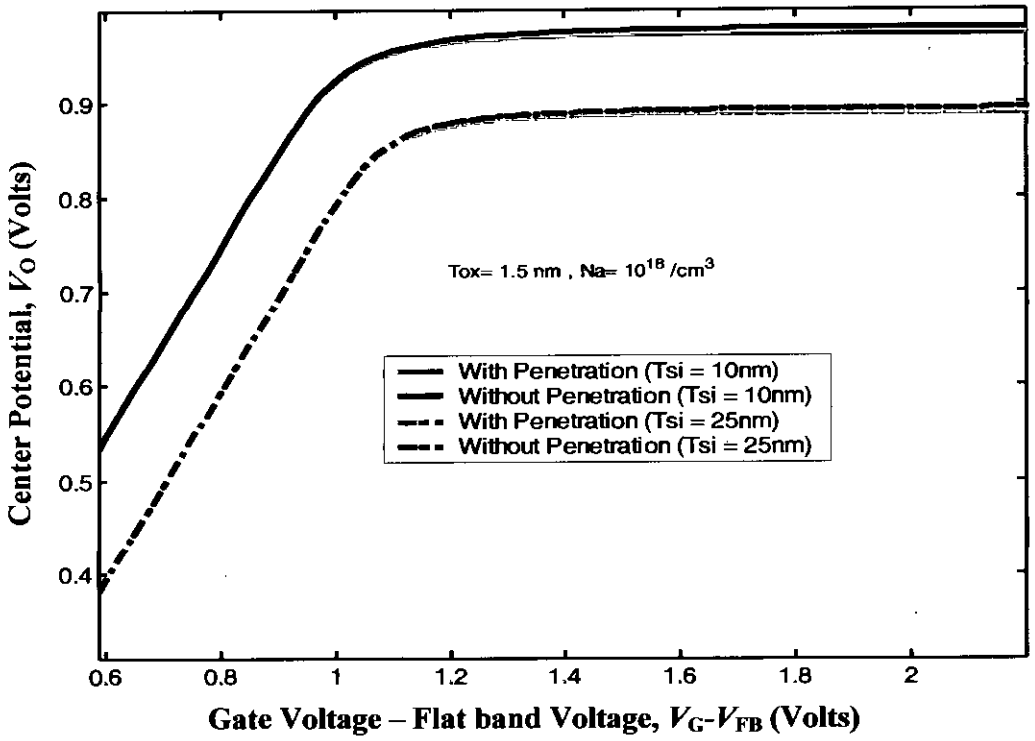

Fig. 3.4 Center Potential, V_o as function of gate voltage for different Tsi

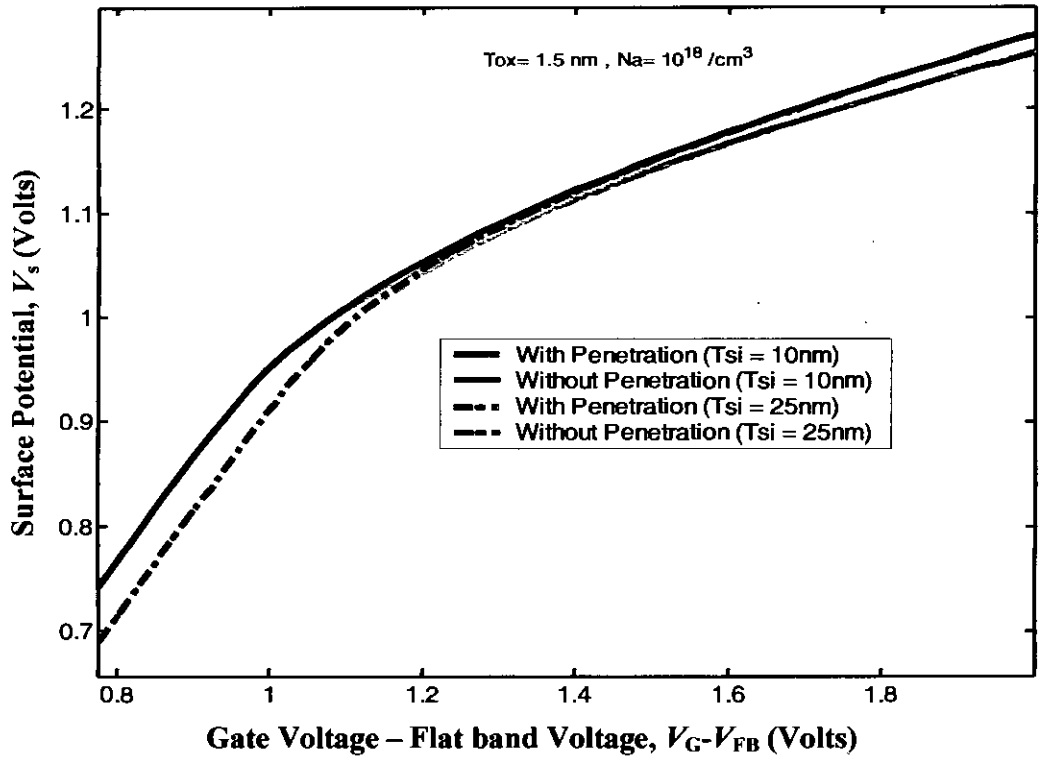

Fig. 3.5 Surface Potential, V_S as function of gate voltage for different Tsi

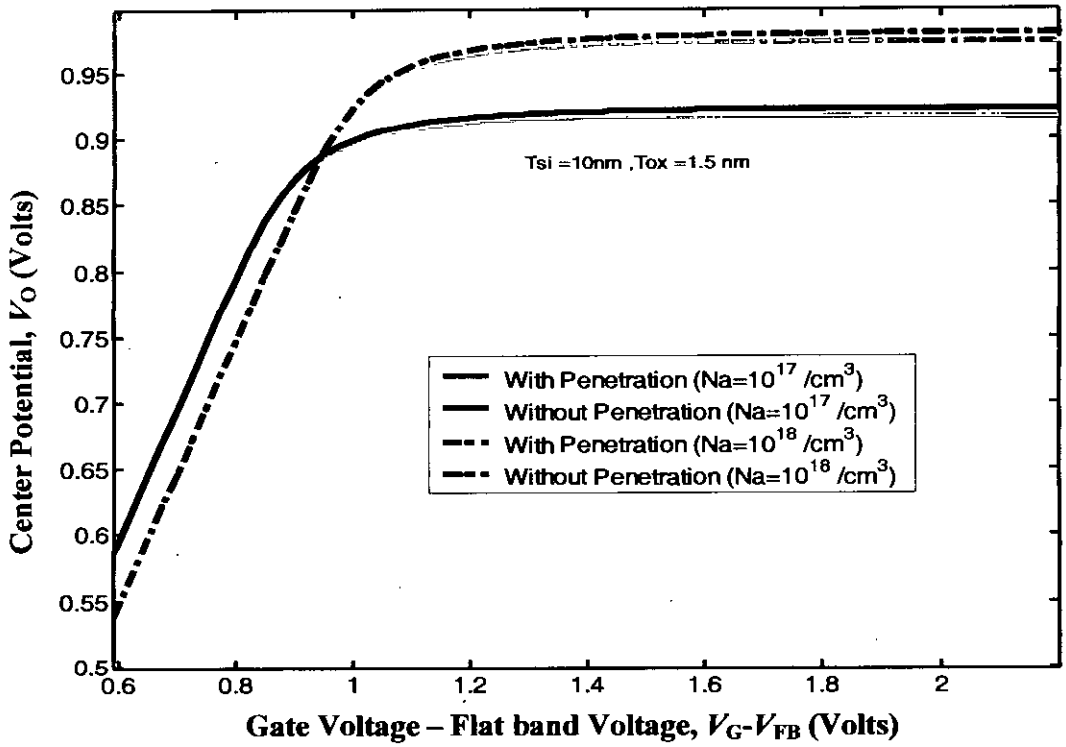

Fig. 3.6 Center Potential, V_O as function of gate voltage for different N_A

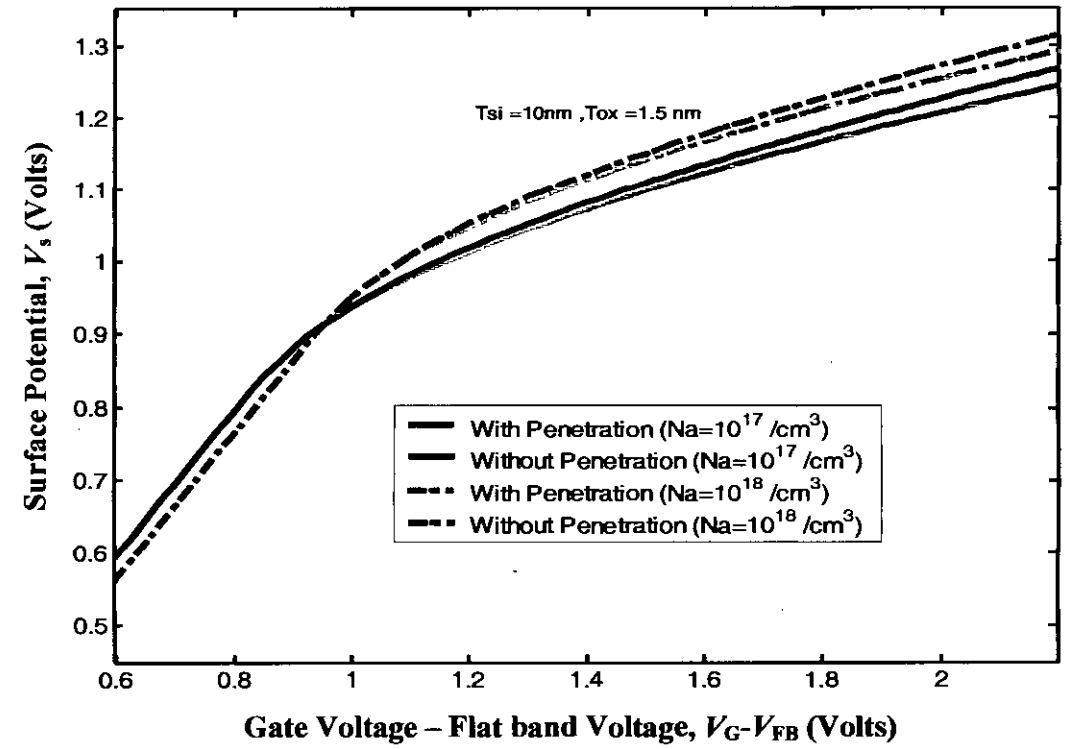

Fig. 3.7 Surface Potential, V_S as function of gate voltage for different N_A

Fig. 3.6 and Fig. 3.7 show variations of V_O and V_s for different doping density as a function of gate voltage. For low inversion when depletion charge is dominant V_O and V_s is greater for low doping density than that of high doping. But, as the inversion charge become dominant over depletion charge V_O and V_s is greater for high doping density. We can conclude that, penetration effect is similar for same oxide thickness or silicon thickness or doping density and results show that it reduces the surface potential and center potential.

There are assumed advantages of DGMOS attributed to the volume-inversion regime that have been controversial in the past, with questions raised regarding the differences and similitude between DGMOSFET's and conventional bulk MOSFET's [6, 16, 40]. When the active silicon layer is thin enough, the electron concentration in the channel peaks in the middle, and is said to be far from the interfaces, thus leading to reduced scattering due to charged centers in the oxide layers and in their interface with silicon, and less influence of surface roughness [6]. Moreover, as the entire silicon layer is able to carry current, the current capability of these devices is said to be greater than the current capability of standard bulk MOSFET's of double width. In order to assess the true advantages of DGMOSFET's for the future microelectronic technology, these features must be analyzed. Now, the effect of penetration on inversion charge centroid, $Z_{average}$ will be examined. $Z_{average}$ is calculated for half of the silicon film using the following equation [22]:

$$Z_{average} = \frac{\int_0^{Tsi/2} zn(z)dz}{\int_0^{Tsi/2} n(z)dz} \qquad \textbf{(3.1)}$$

Fig. 3.8 shows average penetration depth for half of the silicon film for two oxide thickness. It has been found that $Z_{average}$ is weakly dependent on gate voltage and oxide thickness in weak inversion, but decreases sharply with increasing inversion charge density i.e. gate voltage in strong inversion. It is also noted that $Z_{average}$ increases with oxide thickness in strong inversion regime. Due to penetration, carrier peak has been found closer to oxide-Si interface and estimates $Z_{average}$ less than that of without penetration. The shift in average distance due to penetration effect in this case about 0.1 nm and almost constant in the whole inversion regime and is independent of oxide thickness. Fig. 3.9 suggests, $Z_{average}$ is higher for higher Tsi, approaches to the same value with increasing gate voltage.

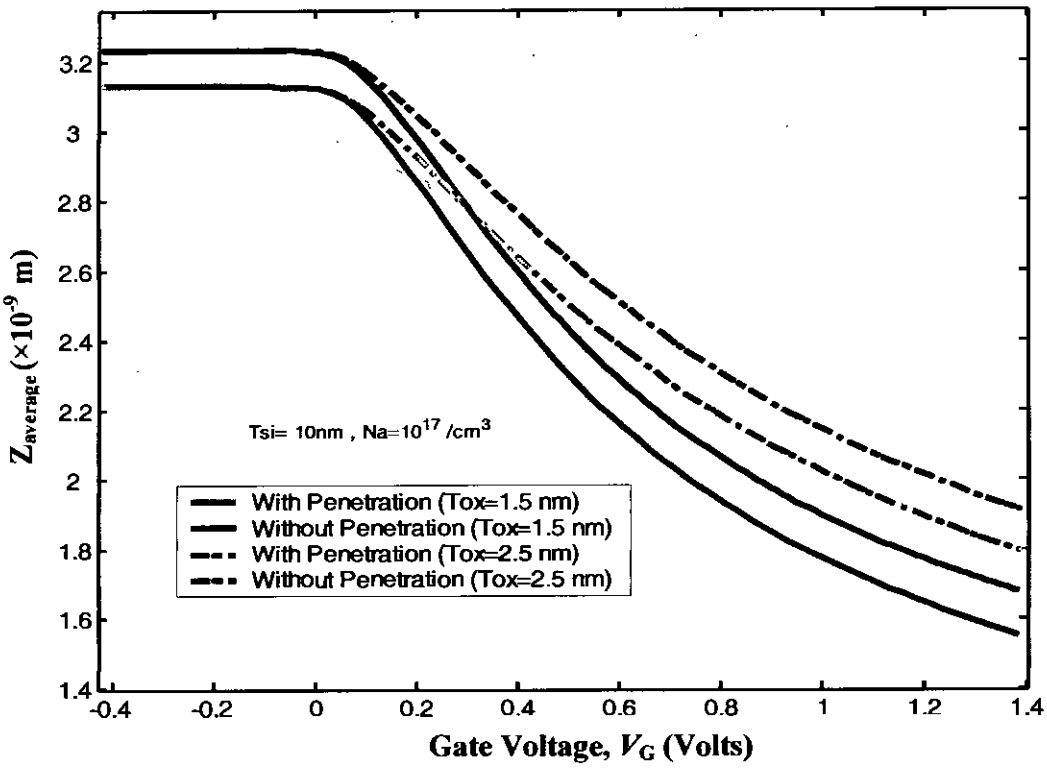

Fig. 3.8 $Z_{average}$ as a function of Gate voltage for different Tox

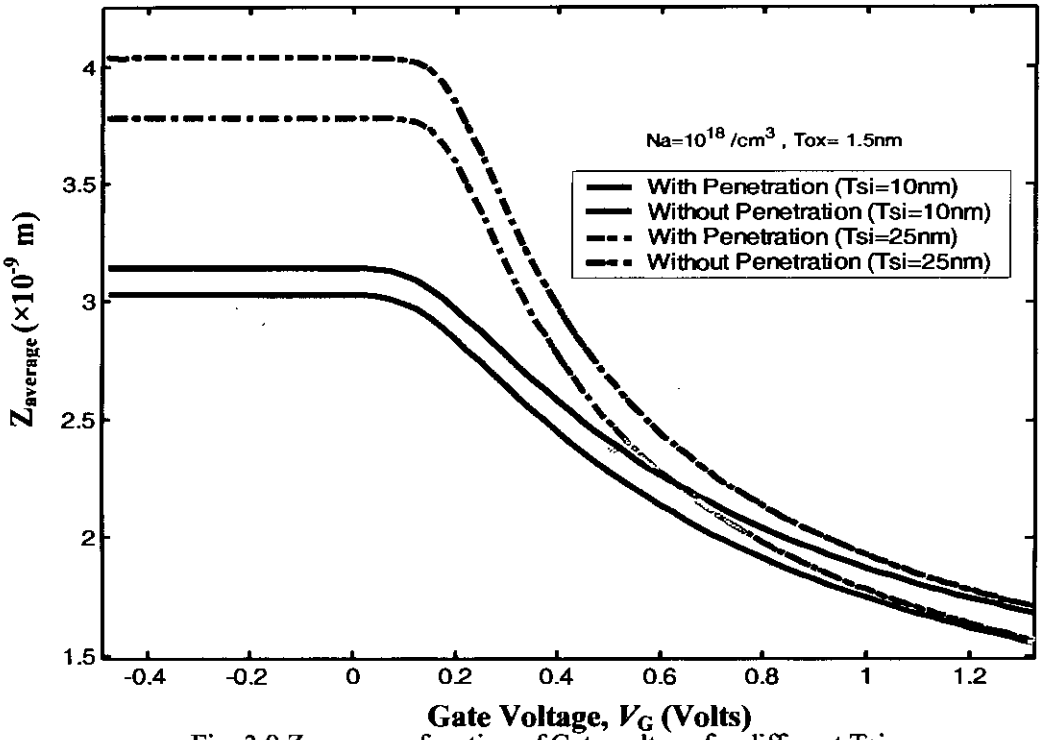

Fig. 3.9 $Z_{average}$ as a function of Gate voltage for different Tsi

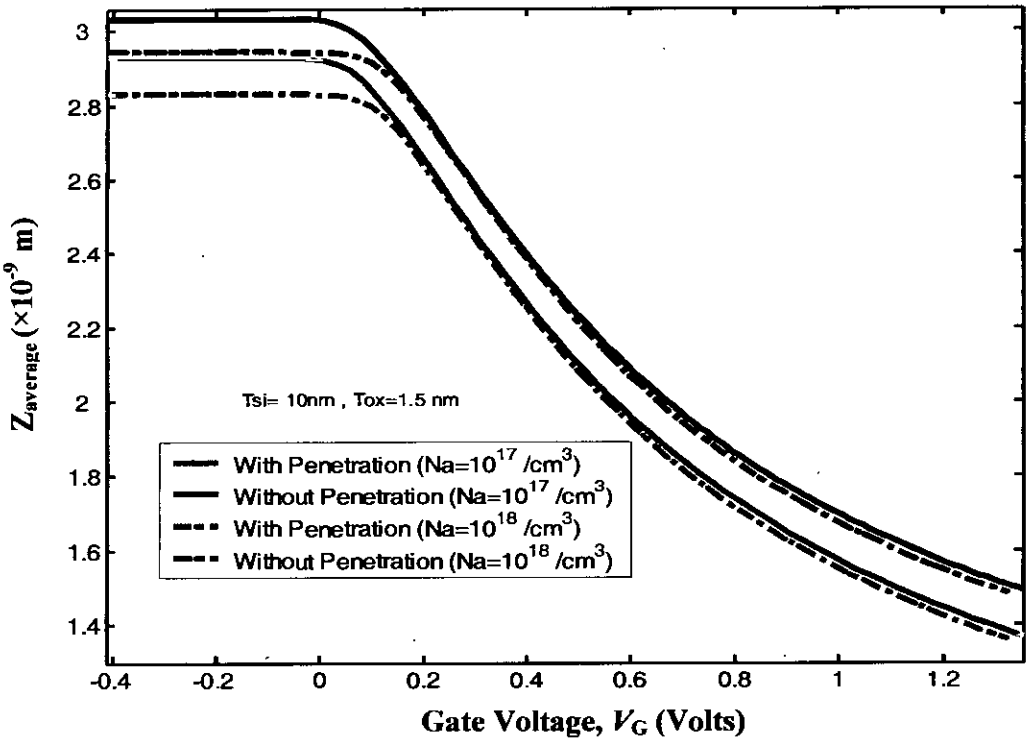

Fig. 3.10 $Z_{average}$ as a function of Gate voltage for different N_A

It is also noted that $Z_{average}$ is weakly dependent on doping density as shown in Fig. 3.10. Penetration effect on average penetration depth with the variation oxide thickness, silicon film thickness and doping can be analyzed from the % error variation curves. Fig. 3.11- 3.13 show these % errors in average penetration curves which are calculated using:

$$\%\, error = \frac{Zaverage\,(With\ Pen.) - Zaverage\,(Without\ Pen.)}{Zaverage\,(With\ Pen.)} \times 100 \qquad \textbf{(3.2)}$$

All these curves clearly indicate, due to penetration % error in average penetration depth increases with increasing gate voltage. Error is almost constant is the weak inversion region and increases in higher inversion regime. The reason is very simple, at low inversion when inversion charge is very small; the wave function penetration into oxide region is not very significant. So, very small amount of charge resides into oxide region and *n(z)* doesn't change too much. But, as the gate voltage is further increased, inversion charge increased very rapidly and hence penetration effect become very significant. We can also conclude:

- Penetration effect is more significant for thinner oxide. So, % error is higher for lower oxide as illustrated in Fig. 3.11.

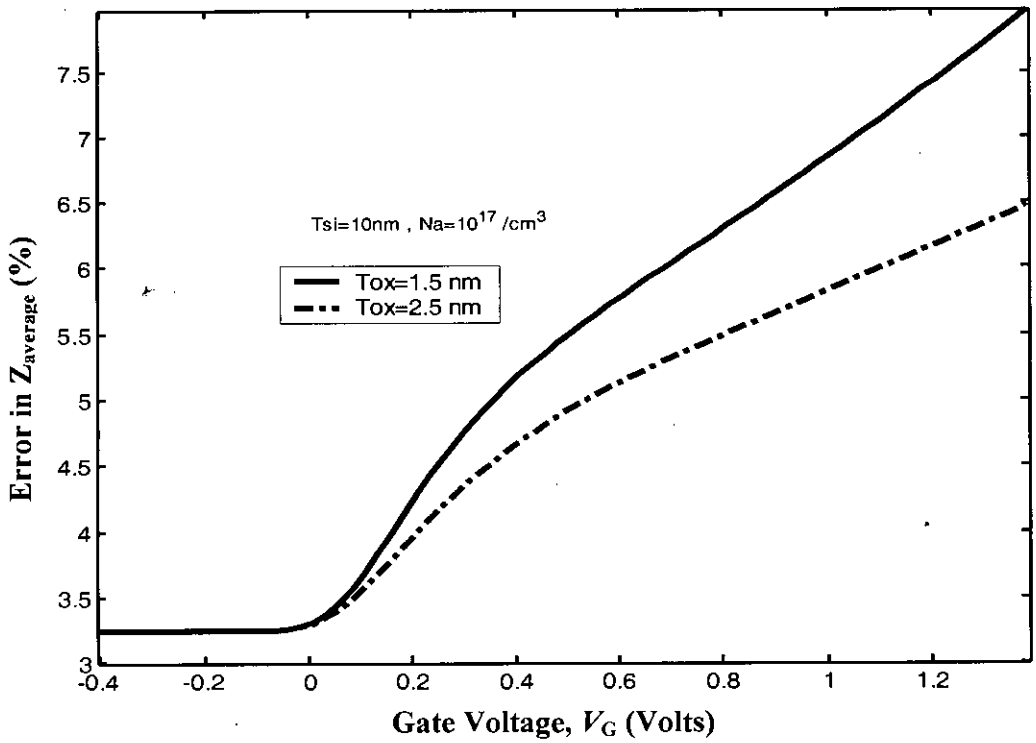

Fig. 3.11 %error in $Z_{average}$ as a function of gate voltage for different Tox

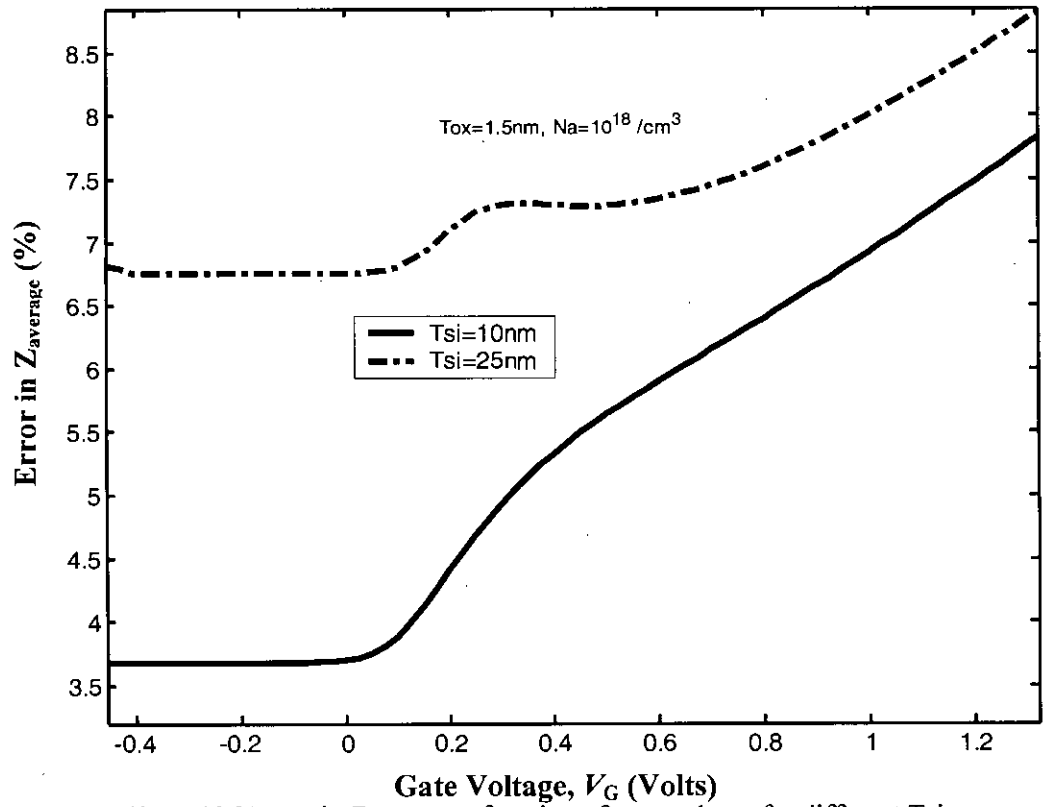

Fig. 3.12 %error in $Z_{average}$ as a function of gate voltage for different Tsi

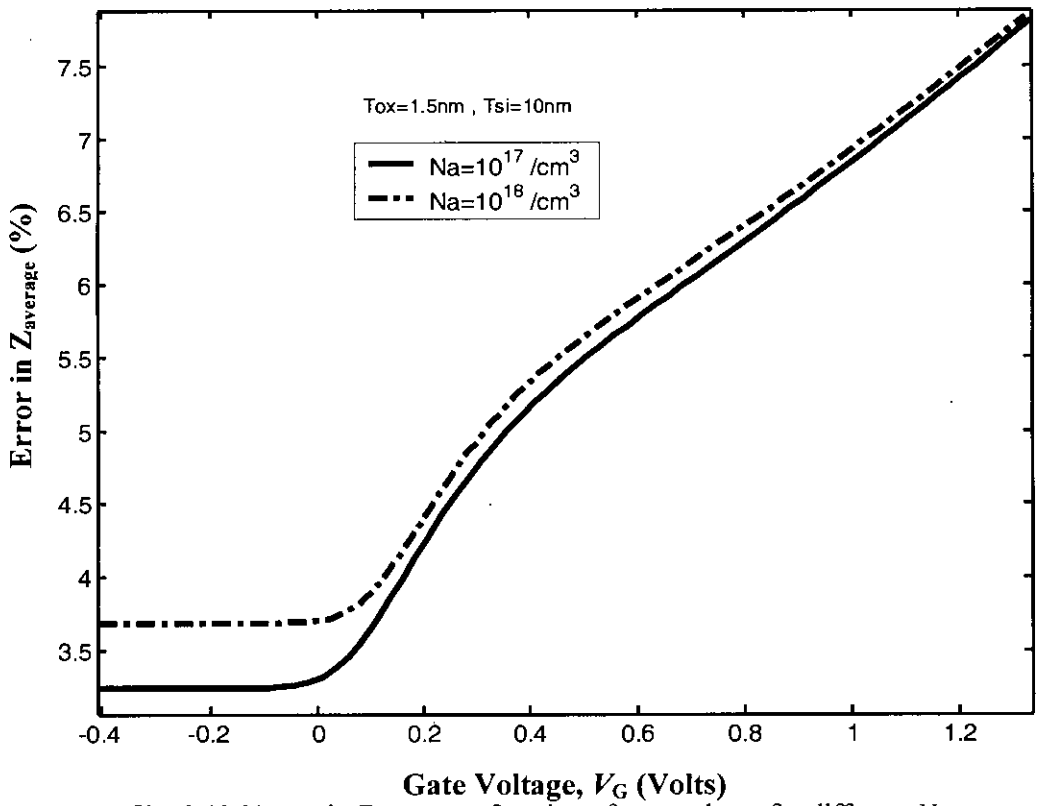

Fig. 3.13 %error in $Z_{average}$ as a function of gate voltage for different N_A

- Penetration effect is more significant for thicker Silicon region. So, %error is higher for higher silicon body thickness as shown in Fig. 3.12.
- Penetration effect is more significant higher doping density. So, %error is higher for higher doping as depicted in Fig. 3.13.

Another important quantity that has significant effects on MOS properties is the gate capacitance. C-V study so far has been done on DGMOS assuming the wave function to be zero at the dielectric-gate electrode boundary [19, 30]. The C–V calculated assuming such a boundary condition differs by an insignificant amount from the C–V calculated by letting the wave function penetrate into the gate electrode. This is understood because the probability density function is reduced by many orders of magnitude near the gate electrode and hence forcing it to zero does not introduce very significant difference in C-V characteristics.

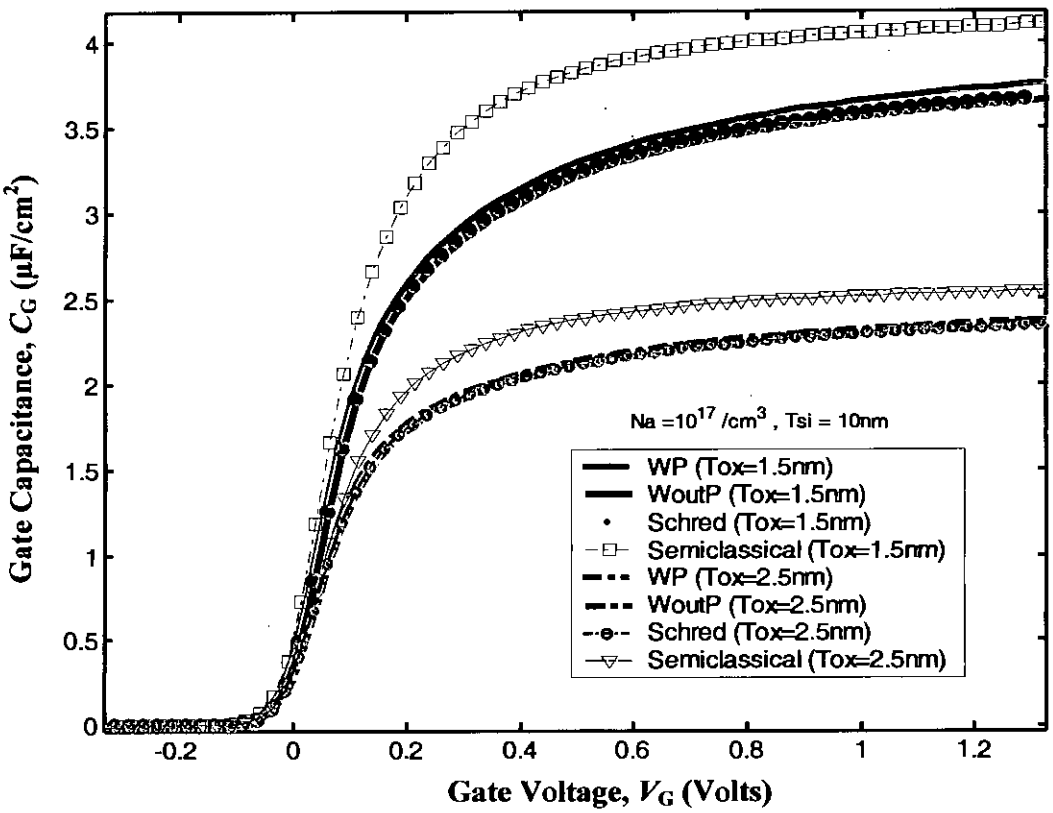

Fig. 3.14 Gate capacitance as a function of gate voltage for different oxide thickness, Tox. WP corresponds to capacitance with penetration; WoutP corresponds to capacitance without penetration.

Gate capacitance has been calculated from the basic definition of capacitance:

$$C_G = \frac{dQ_T}{dV_G} \tag{3.3}$$

Where, Q_T is the total charge when gate voltage V_G is applied on both gates. Fig. 3.14 shows the C-V characteristics of an n-channel DGMOS for two oxide thickness. To verify numerical calculation, simulated results have been compared with 'Schred'(shown in red dotted curve), a well known established numerical solver that doesn't consider penetration effect developed at Purdue University available through www.nanohub.org. Quantum simulation shows classical analysis overestimate gate capacitance to a great extent and capacitance decreases with increased oxide thickness. Our simulated results without penetration have an excellent match with 'Schred'

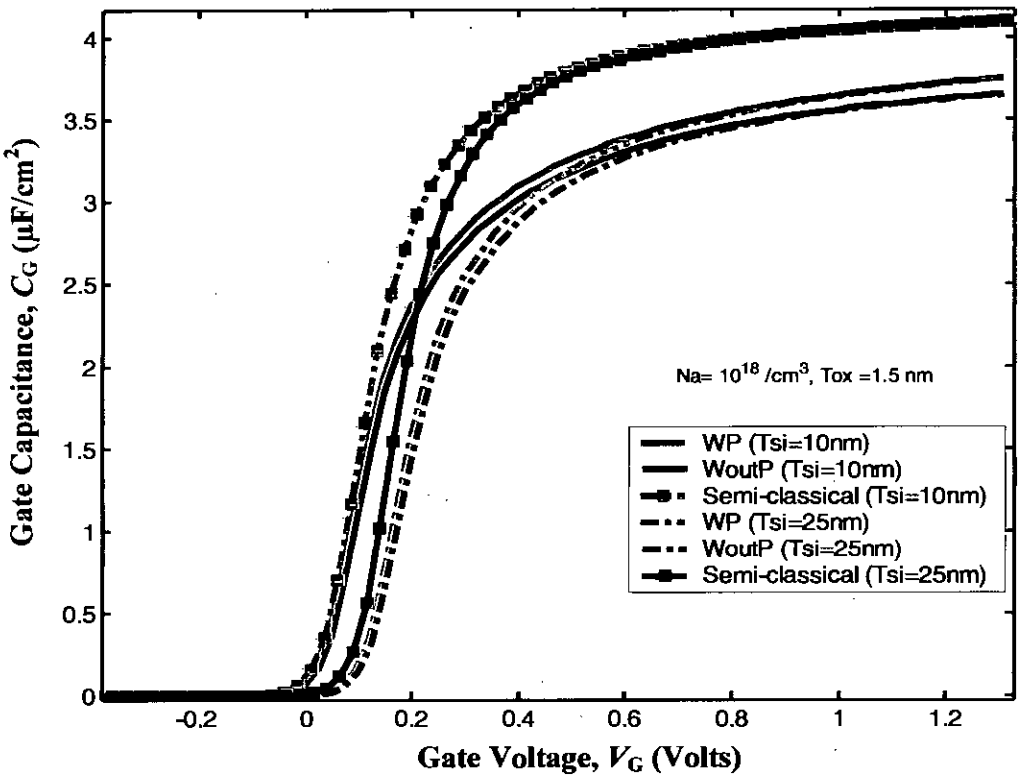

Fig. 3.15 Gate capacitance as a function of gate voltage for different Tsi

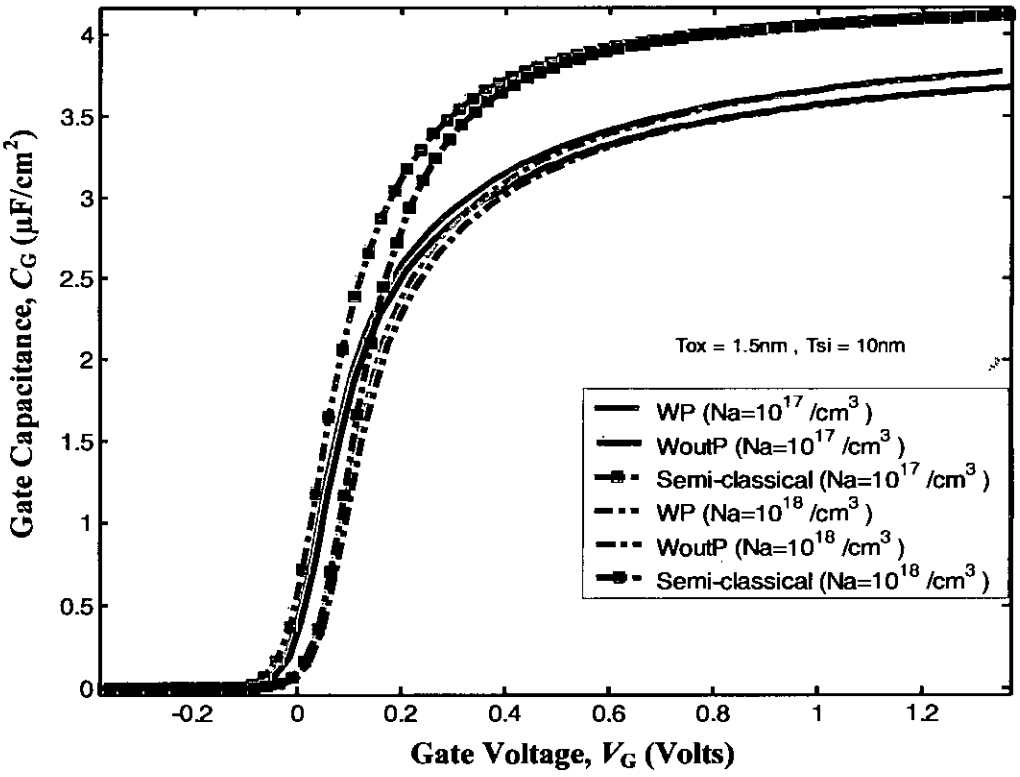

Fig. 3.16 Gate capacitance as a function of gate voltage for different doping, N_A

as the simulator doesn't include penetration effect. Due to penetration, the gate capacitance actually increases slightly from that of without penetration. Fig. 3.15 indicates, with the increase of semiconductor thickness the C-V characteristics shift rightward but the magnitude in strong inversion is same. The reason is, when the inversion is low, the band is almost flat and the charge density profile depends on semiconductor thickness actually. But as the inversion becomes stronger the band bending in interface regions determines the charge density profile and most of the charge is concentrated in the region some distance near the silicon-oxide interfaces. Fig. 3.16 shows the effect of doping on C-V curve which indicates with the increasing doping density the characteristic curves shift rightward. Effect of penetration is shown in Fig. 3.17-3.19. % error is calculated as the criteria of comparison which is calculated as:

$$\%\,error = \frac{C_G(With\ Pen.) - C_G(Without\ Pen.)}{C_G(With\ Pen.)} \times 100 \qquad \textbf{(3.4)}$$

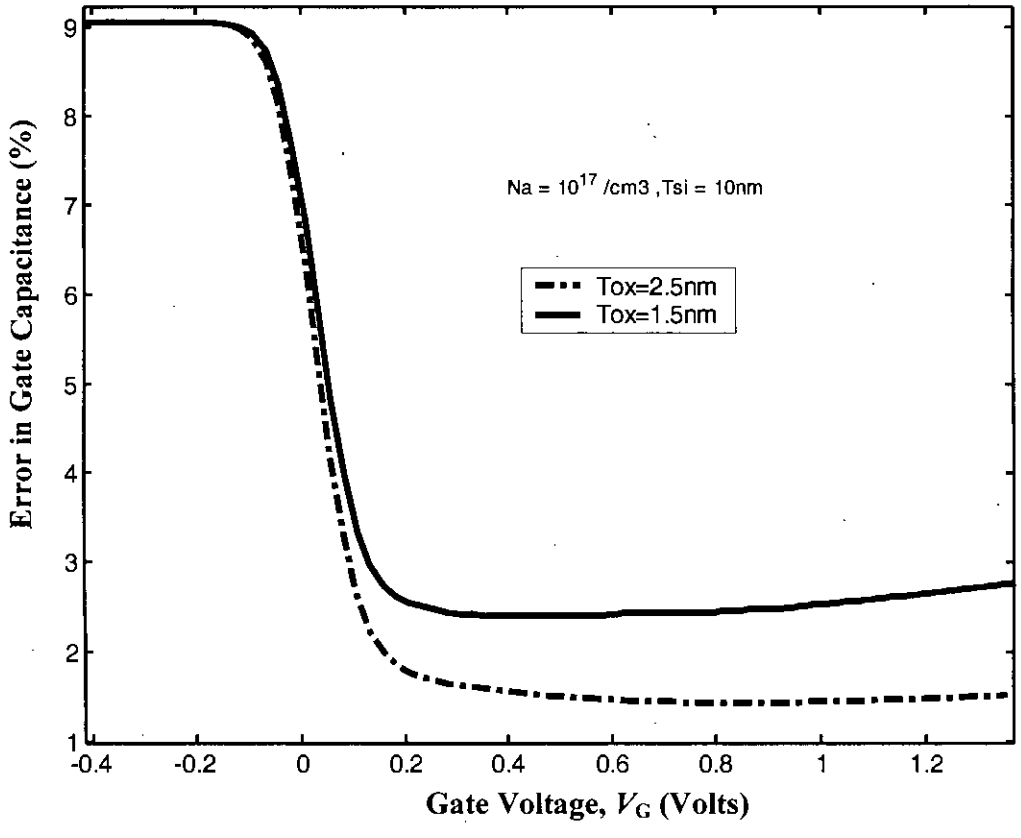

Fig. 3.17 %error in C_G as a function of gate voltage for different Tox

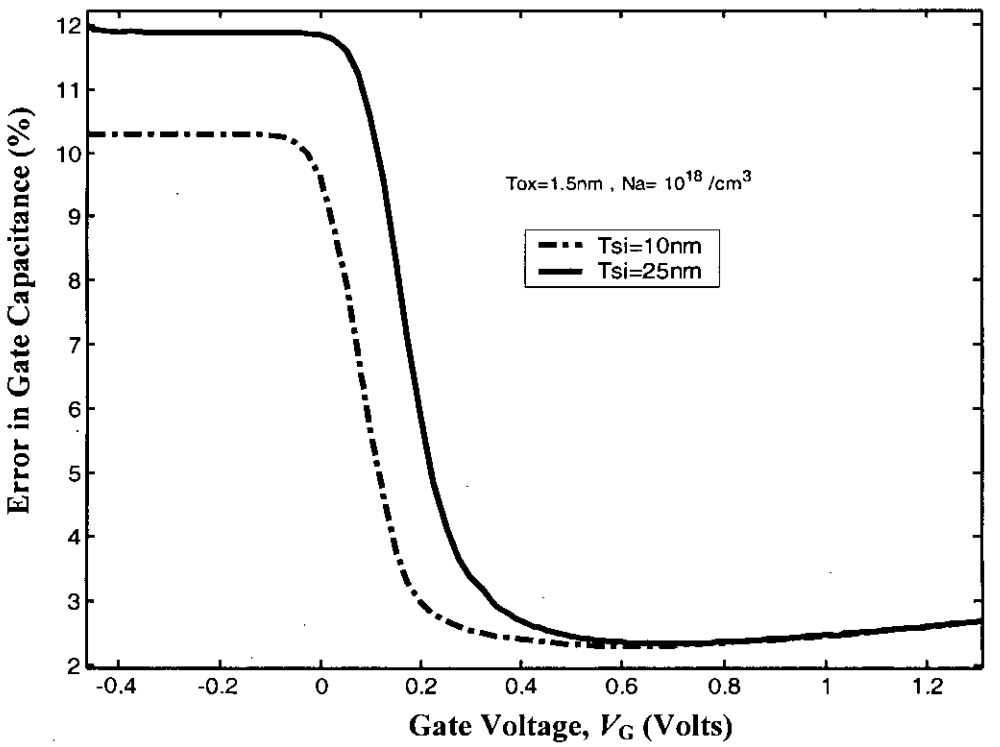

Fig. 3.18 %error in C_G as a function of gate voltage for different Tsi

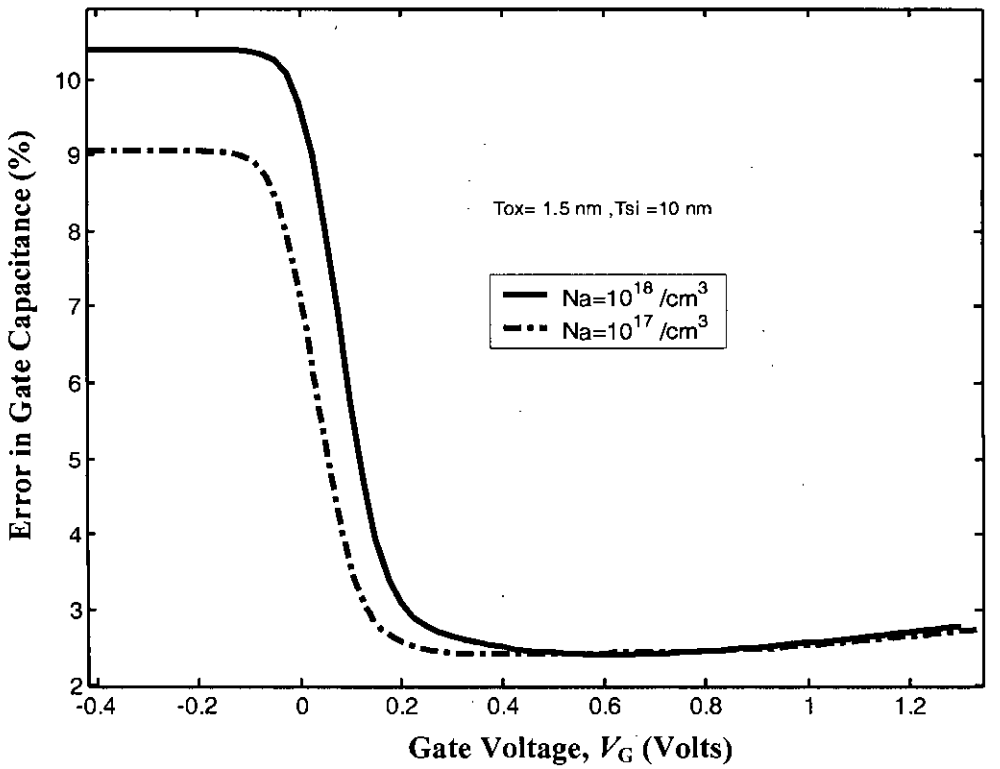

Fig. 3.19 %error in C_G as a function of gate voltage for different N_A

From These error curves of % error in gate capacitance we can conclude:

- Penetration effect is more severe for thinner oxide layer in the strong inversion regime because as the inversion becomes stronger, inversion charge centroid shift is more for thicker dielectric.
- Penetration effect i.e. % error is more severe in low inversion regime although differential error is greater in the strong inversion as justified from the Fig. 3.17-3.19.
- Penetration effect is more prominent for higher doping and thicker semiconductor region.

To show the versatality of the numerical calculation, this solver hase been applied to double gate PMOS and to an undopoed body double gate n-MOS and the results are shown in Fig. 3.20 - 3.22. These results are not discussed here in details because it has been found that they show similar behaviour as discussed earlier in this chapter.

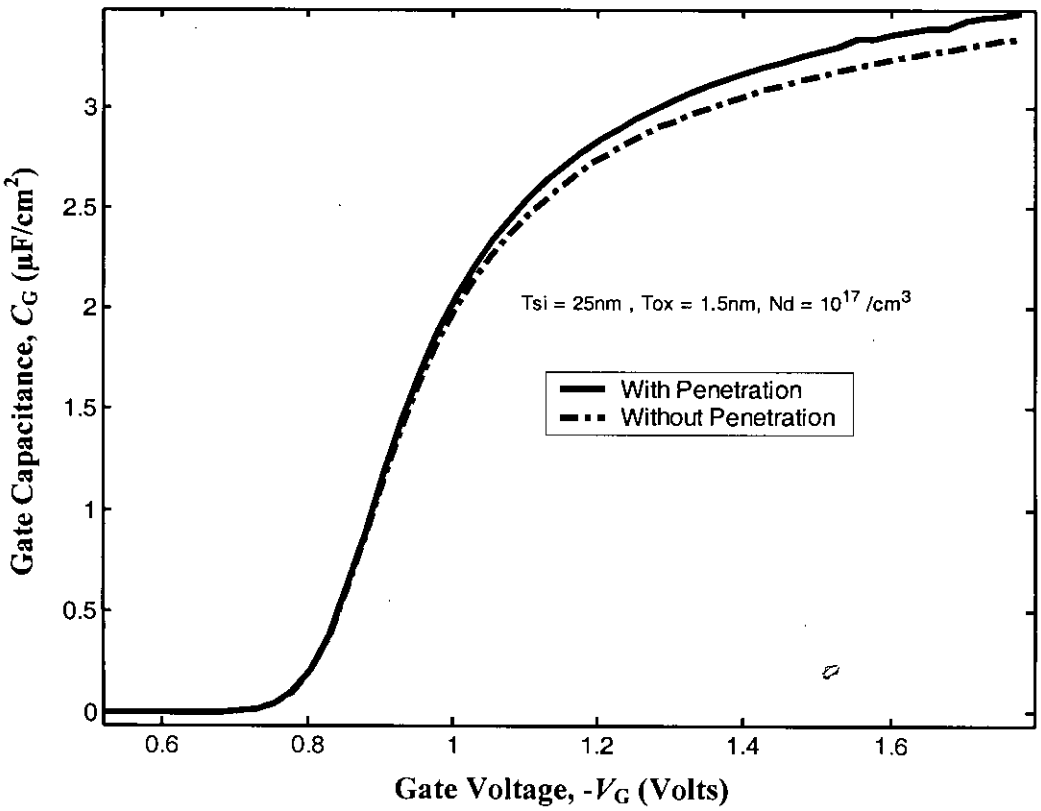

Fig. 3.20 C-V characteristic of double gate PMOS

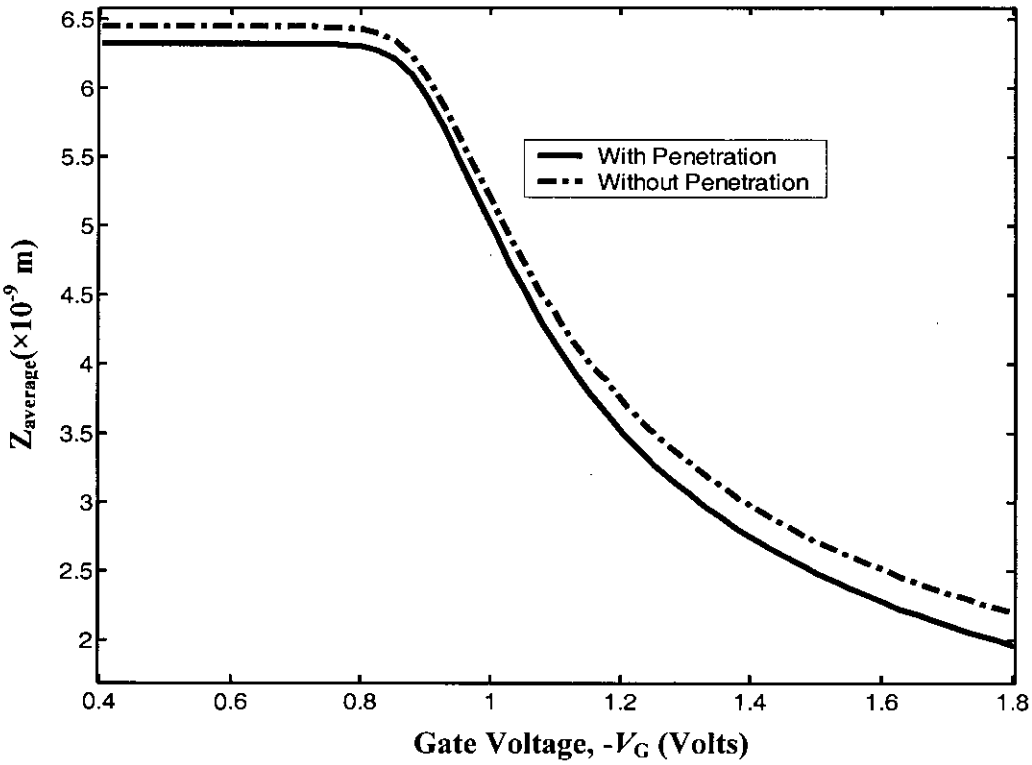

Fig. 3.21 Zaverage as a function of gate voltage for the same PMOS of Fig. 3.20

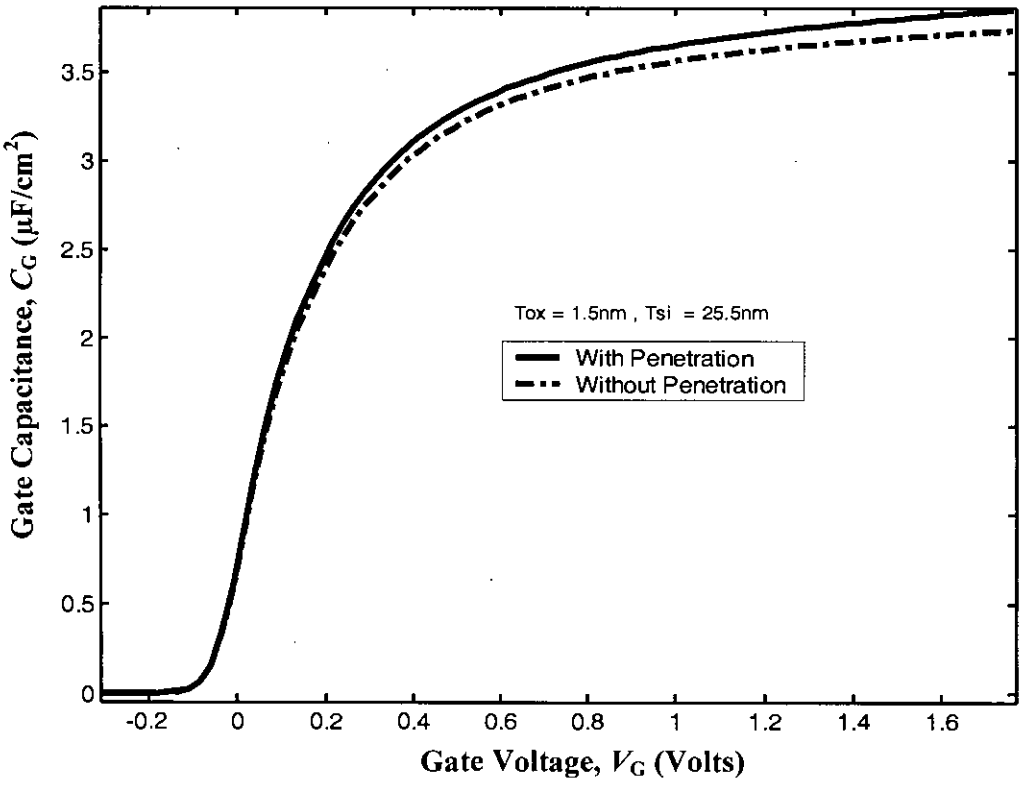

Fig. 3.22 C-V characteristics of a undoped body dual gate MOSFET

Chapter 4

Conclusion

An improved and numerically efficient self-consistent model has been developed for MOSFET simulation which incorporates the wave function penetration into the gate oxide region and can also be used for simulation without penetration effect. The proposed model is used to study the effects of wave function penetration on double gate n-MOS and p-MOS devices by comparing the numerical results with those of without penetration. Simulated results have been compared with globally recognized device simulator results.

4.1 Summary

Effects of wave function penetration into gate oxide on properties of n-MOS and p-MOS devices in deep submicron regime are studied. Penetration effects are included within the self-consistent loop by solving both Schrödinger's and Poisson's equations taking into account wave function penetration. An accurate and fast formalism has been used for the solution of Schrödinger's equation using FEMLAB. Poisson's equation is solved for the combined oxide and semiconductor regions by applying an appropriate boundary condition at the gate metal-oxide interface. Rest of the work has been done in MATLAB using the FEMLAB powerful interface with MATLAB.

Numerical results for n-MOS devices on (100) silicon show that when the effects of wave function penetration are not considered within the self consistent loop, the errors made in estimating the electrostatic potential are non-trivial. Penetration effects on properties of inversion carrier become more important as device dimensions are scaled down. Numerical results show that center potential is very weekly dependent on oxide thickness and penetration effect on V_O is negligible in weak inversion but overestimates V_O in strong inversion.

Quantum calculation suggests, V_S and V_O are strongly coupled in weak inversion as inversion charge is not uniformly distributed in the silicon region. In strong inversion, Surface potential increases almost linearly whereas center potential remains constant.

It has been found that $Z_{average}$ is weakly dependent on gate voltage and oxide thickness in weak inversion, but decreases sharply with increasing inversion charge density i.e. gate voltage in strong inversion. It is also noted that $Z_{average}$ increases with oxide thickness in strong inversion regime. Due to penetration, carrier peak has been found closer to oxide-Si interface and estimates $Z_{average}$ less than that without penetration. It is also noted that $Z_{average}$ is weakly dependent on doping density. All of the % error curves clearly indicate, due to penetration % error in average penetration depth increases with increasing gate voltage. Error is almost constant in the weak inversion region and increases in higher inversion regime. Penetration effect is more significant for thinner oxide, thicker Silicon region and higher doping density

The C–V characteristic calculated assuming close boundary condition differs by an insignificant amount from the C–V calculated by letting the wave function penetrate into the gate electrode. Due to penetration, the gate capacitance actually increases slightly from that of calculated without penetration. Penetration effect is more severe for thinner oxide layer in the strong inversion regime because as the inversion becomes stronger, inversion charge centroid shift is more for thicker dielectric. % error is more severe in low inversion regime although differential error is greater in the strong. Penetration effect increases with doping density and semiconductor thickness.

4.2 Suggestions for Future Work

Self-consistent solution is an important tool for simulation of many devices where the QM effects become significant. Our self-consistent model may be used for simulating many systems, such as single gate, double gate MOS structure, high electron mobility transistor, resonant tunneling diodes and quantum well lasers, where self-consistent calculation with open boundary condition is necessary. A few suggestions for future work are given below.

We have mainly applied our model to calculate device properties in inversion region for fully depleted double gate n-MOSFET and have shown that same analysis can be performed on the p-MOSFET. A few modifications are necessary to use it for simulating the p-MOSFET. Hence, it can be used in accumulation region also. Calculation of gate capacitance in accumulation is important from device parameter extraction point of view.

We have performed 1-D analysis of DGMOS capacitor. But when voltage is applied between the drain and the source, 2-D nature of QM effects arise in the channel. So, 2-D simulation should be performed. FEMLAB is powerful and accurate enough to do 2-D and 3-D simulation. Hence, 2-D nature of device parameter can be determined.

The direct tunneling gate current of a deep submicron MOSFET flows due to QM tunneling of inversion layer carriers from semiconductor to the gate electrode. Our model may be applied for accurate determination of direct tunneling current.

As the gate length of CMOS devices are continued to be scaled down to sub-100 nm regime, scaling rules dictate that the gate oxide thickness be scaled down to well below 1 nm. It is known, with the decreasing dielectric thickness, tunneling gate current increases rapidly. In order to decrease this leakage current, high-K materials should be used as gate dielectric. The modeling of such devices can be done easily with the proposed self-consistent model.

We have performed 1-D analysis of symmetric DGMOS structure and ignored trap charges. Same analysis can be performed on asymmetric gate structure and done incorporating trap charges.

In our calculations, we have used effective mass approximation for both electrons and holes. However, due to anisotropy and mixing of valance bands, the use of effective mass approximation for holes has been a topic of debate. The present model for p-MOS devices may be further improved by incorporating the non-parabolic valance band structure.

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Appendix A

The modified self-consistent model, which has been used in this study, has been described in section 2.2. Here, a details flow diagram of the solver is given for better understanding.

A.1 Flowcharts

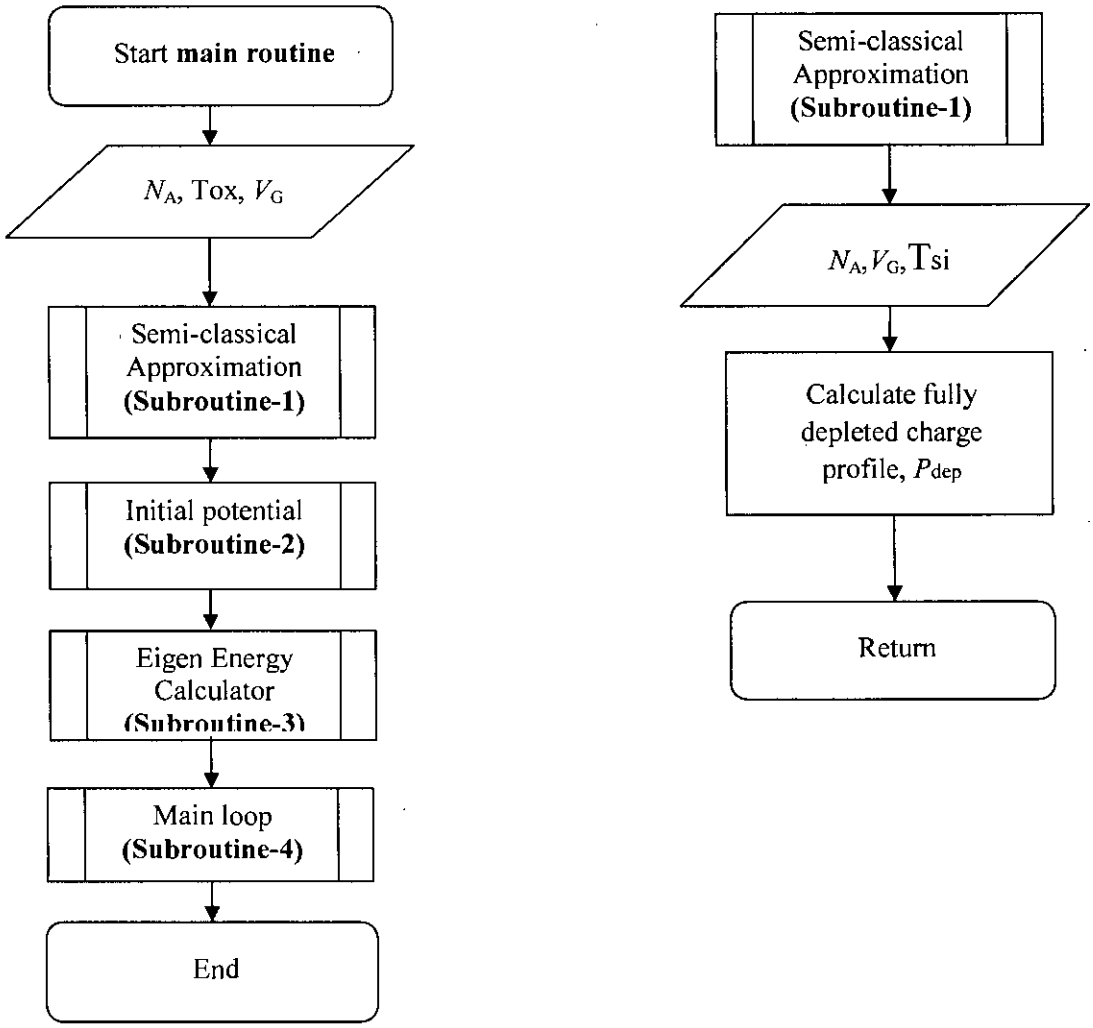

Fig. A.1 Flowchart

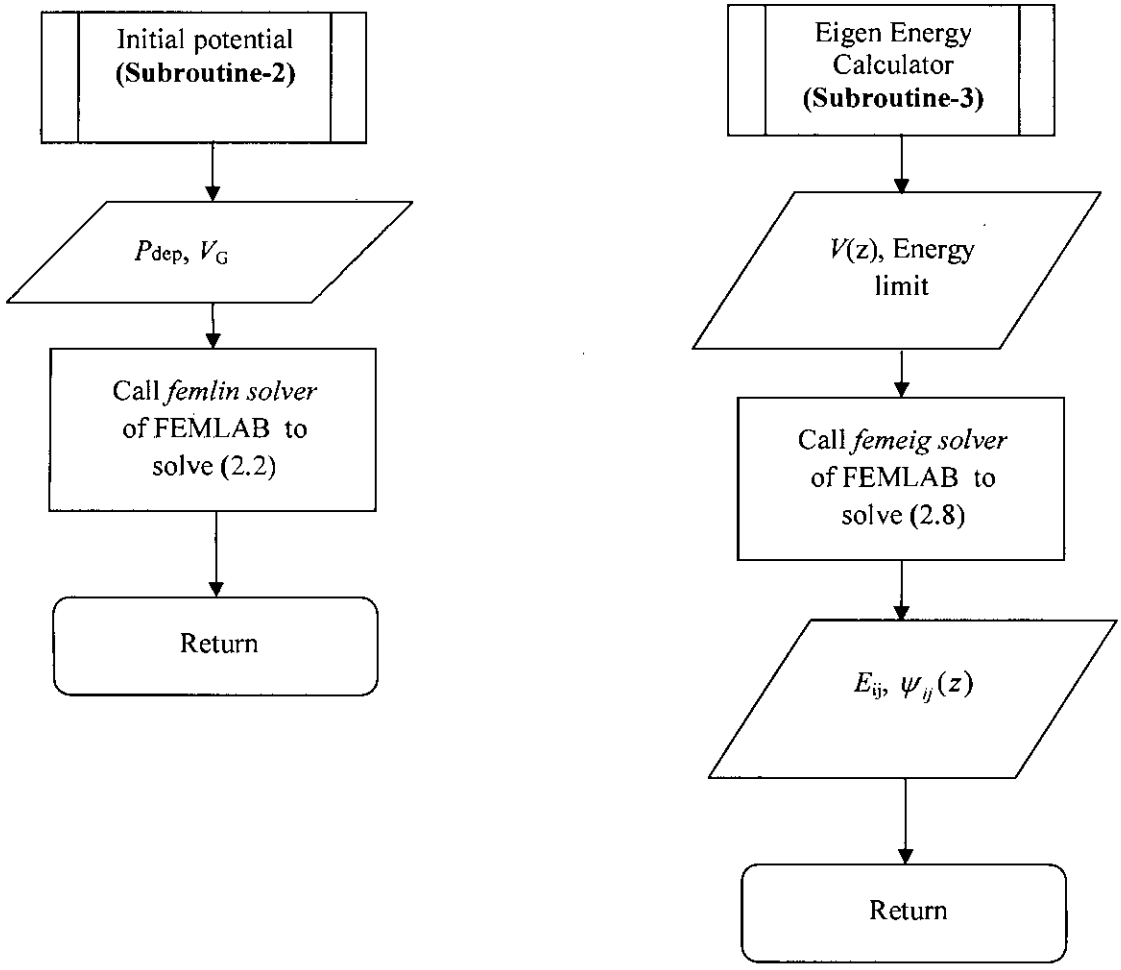

Fig. A.2 Flowchart (contd.)

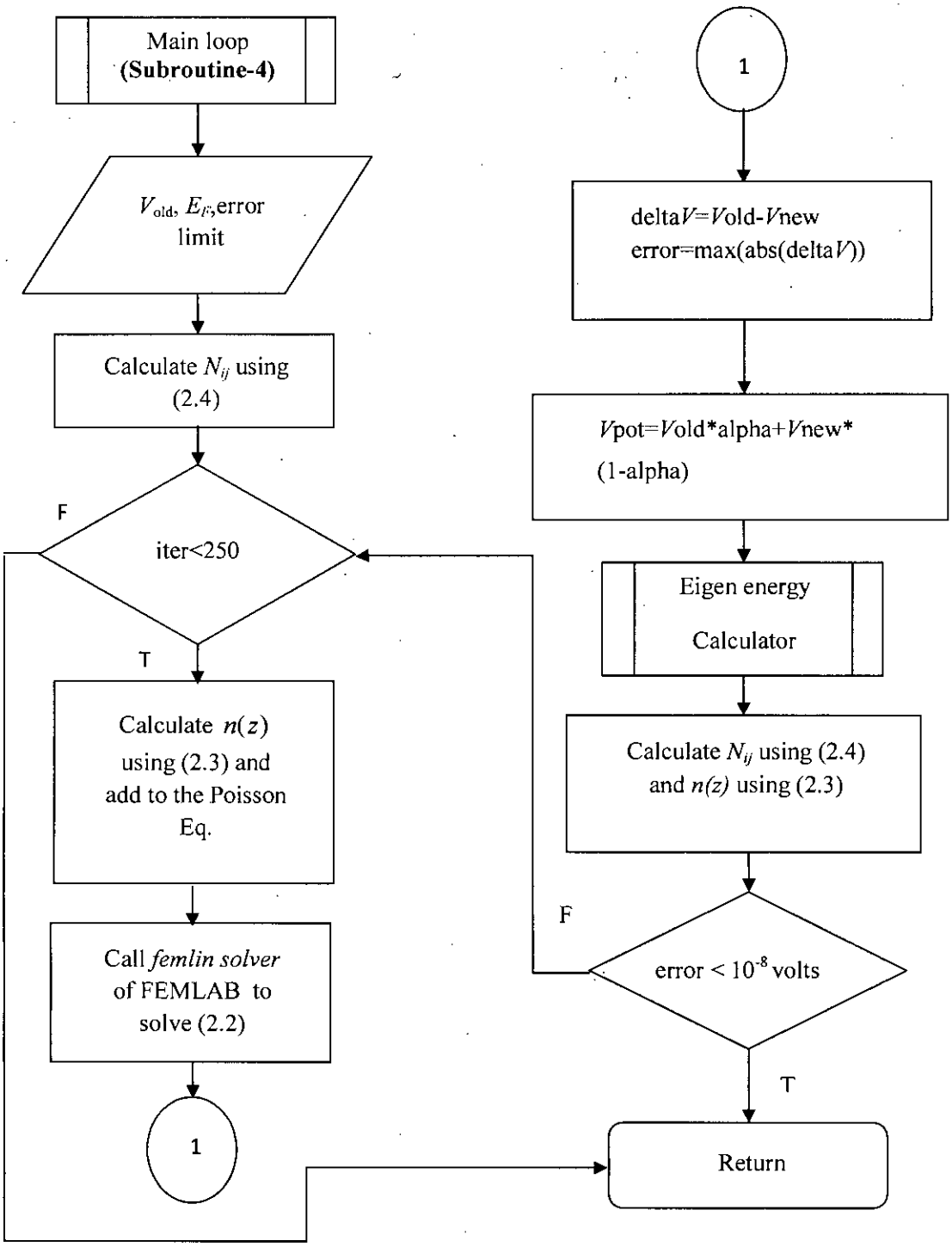

Fig. A.3 Flowchart (contd.)