# QUANTUM MECHANICAL MODELING AND CHARACTERIZATION OF SOFT BREAKDOWN PHENOMENA IN CMOS DEVICES WITH HIGH-k DIELECTRICS

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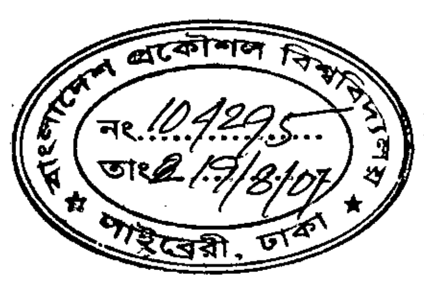

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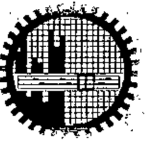
MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING



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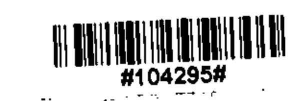

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## DEDICATION

*To my Parents*

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## ABBREVIATIONS

| | |
|---|---|
| DT | Direct Tunneling |
| FN | Fowler-Nordheim |
| HBD | Hard Break Down |
| MOSFET | Metal Oxide Field Effect Transistor |
| QBD | Quasi Break Down |
| QMTC | Quantum Mechanical Transmission Co-efficient |
| QMWI | Quantum Mechanical Wave Impedance |
| QPC | Quantum Point Contact |
| SBD | Soft Break Down |
| TAT | Trap Assisted Tunneling |
| TDDB | Time Dependent Dielectric Breakdown |
| ULSI | Ultra Large Scale Integration |
| VLSI | Very Large Scale Integration |
| VRH | Variable Range Hopping |
| WKB | Wentzel-Kramer-Brillouin |

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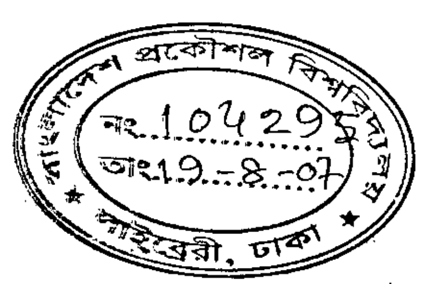
## ABSTRACT

With the emergence of the advanced ULSI technology the MOS (Metal-Oxide-Semiconductor) structure has entered the ultra thin gate oxide level. As the device size is scaled down, the reliability of the structure has become a major concern. The abrupt loss of the insulating property of the $SiO_2$ is one of the important reasons behind the failure of the MOS device performance. Much work has been devoted to the pre-breakdown degradation of the oxide when subjected to electrical stress. The insulator subjected to the electrical stress, undergoes degradation which eventually accelerates the increase in the leakage current which is termed as Stress Induced Leakage Current (SILC). In recent years, a new failure mode has been identified in ultra thin oxide of MOS devices under high field stress resulting in an abrupt increase in the conduction through gate oxide without causing hard breakdown (HBD). This new mode has been termed Soft Breakdown (SBD).

In this work, we formulated a complete quantum mechanical model for NMOS device by solving coupled Schrödinger's and Poisson's equations self-consistently to demonstrate the SBD conduction for a wide range of applied gate voltage. We simulate the gate leakage current both the fresh oxide and after the soft breakdown condition with the experimental data. The concept of lowering the barrier height at the soft breakdown spot is introduced here to calculate the soft breakdown current. In this work, a Soft Breakdown spot is characterized in terms of its barrier height, effective thickness, spot area, electron effective mass, imaginary potential etc. Variation of these parameters is considered to obtain experimental fit between the experimental and theoretical SBD current. We simulate the model for PMOS device and finally extract the SBD parameters for high-k stack. The SBD spot area in the HfAlOx is 1.4 times higher then the SBD spot area in the $SiO_2$.



# CHAPTER 1

# INTRODUCTION

## 1.1 GENERAL OVERVIEW

Aggressive scaling in microelectronics to achieve higher performance and circuit density necessitates the thinning of the $SiO_2$ gate dielectric [1]. With the advent of ULSI (Ultra Large Scale Integrated) circuit technology, MOS transistors featuring gate oxide of sub-1.5 nm have already been fabricated [2],[3]. However, the electronic structure at the atomic scale seems to limit practical oxide thicknesses to 0.7–1.2 nm [4]. This is a fundamental limit which cannot be overcome by technological advancements. In this ultrathin (<3nm) gate oxide regime, the reliability has become one of the most important concerns. The degradation and breakdown problem of $SiO_2$ have been extensively studied for more than fifty years. Much has been learnt about how to grow good quality oxide; however a definitive picture of the microscopic mechanism which finally causes oxide breakdown is still missing. With the increased degradation, the increased gate current adversely affects MOS device performance and greatly increases the standby power consumption of highly integrated chips. Moreover, gate current in small dimension MOS transistors has substantial effect on appropriate modeling of the devices.

In recent years, a new failure mechanism, called Soft Breakdown (SBD), mainly detected in ultrathin oxides (<5 nm), has received much attention for it has important consequences in the evaluation of the reliability of MOS devices [5],[6]. Since the occurrence of this failure event, it is identified as an abrupt change in the oxide conductance, which is several orders larger than that of the Hard Breakdown (HBD). Though in most of the SBD events the device remains functional [7], a large current flows through the damaged oxide. In such cases, accurate modeling of SBD current, along with the understanding of the parameters of a SBD path is extremely essential.

## 1.2 LITERATURE REVIEW

Since its use as gate insulator in 1957 [8], the degradation of thin silicon dioxide films was observed over three decades ago [9]-[12]. Several physical mechanisms have been identified as the most probable in causing defect generation in thin $SiO_2$ films. First, an empirical model for breakdown was developed by observing the electric field dependence of TDDB (Time Dependent Dielectric Breakdown) data [13]-[15]. The logarithm of the time-to-failure shows a linear relation with the applied electric field. Later a physical model known as Thermochemical model (or E model) was proposed by McPherson *et al.* [16]. According to that model, the applied electric field eventually breaks the weak bond and creates a permanent defect or trap. Chen *et al.* [17] proposed another model which shows that a positive feedback process causing current runaway, leads to breakdown. The feedback process is initiated when electron injected into the oxide transfers energy to the holes which eventually leads to additional electron injection. However, the above mentioned models were subject to debate as simply observing an empirical dependence of breakdown time on electric field is not a conclusive evidence for a particular physical model [1].

The validity of an electric field driven model becomes questionable after the observation of results from substrate hot electron injection (SHEI) experiments performed by DiMaria [18]. The important results indicate that the time to breakdown is proportional to the inverse of the injected current density, in other words tunneling electrons. In the 90s, DiMaria demonstrated the degradation of oxide due to Anode Hole Injection (AHI) [19],[20] which is initiated by high energy carriers even at low voltage. A critical hole fluence (Qp) is needed for oxide breakdown [17]. Later, Schuegraf *et al.* [21] added that this $Q_p$ decreases for decreasing oxide thickness. Contemporary works by DiMaria and Stasiak [22] showed that there is evidence for a defect generation mechanism involving the release of atomic hydrogen from the anode by energetic tunneling electrons. However, despite the existence of these models, there is still controversy concerning the physical model of breakdown in $SiO_2$. It is not known definitively whether

released species like hydrogen or injected holes causes the defect that eventually leads to breakdown.

To demonstrate the breakdown statistics, Weibull statistics is widely accepted as it fits data over a wide range of samples [23]. Weibull statistics can incorporate the oxide thickness and also the number of defects at breakdown, $N_{BD}$. Sune *et al.* [24] first formulated a statistical model and described oxide breakdown and defect generation via a Poisson process. Dumin *et al.* [ 25] incorporated the model to describe failure distributions in thin oxides. Degraeve *et al.* [26] later used percolation theory to describe the statistical process of breakdown. The parameters used to fit experimental data are the trap radius and the fraction of defects effective in initiating breakdown. Stathis [27] used a computer simulation to demonstrate the thickness dependence of using percolation theory.

In the early 80s, Maserjian *et al.* [28] observed that thin oxides that had been stressed at high voltages had increased low-level pre-tunneling leakage currents through the oxides, the current that is presently known as SILC (Stress Induced Leakage Current). From the experimental point of view, this effect was first studied in details by Olivo *et al.* [29]. At present, there is wide agreement in considering SILC as being related to a trap-assisted tunneling (TAT) mechanism occurring more or less uniformly throughout the structure area [30], [31].

In 1994, a new failure mechanism, mainly detected in ultrathin oxides (<5 nm), has been reported by Lee *et al* [32]. The new failure event is identified by an abrupt change in the oxide conductance, which is several orders of magnitude smaller than that associated with the HBD; the conduction mode has been named Quasi-Breakdown [32] (later Soft Breakdown, SBD). The main two features of this mode are a huge leakage current in the Direct Tunneling (DT) voltage range that shares some major aspects with the BD mode, and a significant increase of the noise level, sometimes in the form of large multilevel current fluctuations with respect to time. Because of the low-field leakage associated with SBD, the terminology B-mode stress-induced leakage current (SILC) has also been used in the literature [33]. To demonstrate the fluctuation of current, Depas *et al.* [5] explained it as multiple

tunneling via electron traps after critical density of traps developed to trigger breakdown. Farmer *et al.* [34] explained the fluctuations as a result of trap–trap transport of electrons.

An elaborate review of different models regarding SBD conduction has been presented by Miranda *et al.* [35]. The foremost models for the SBD conduction were based on the tunneling mechanism. Lee *et al.* [32] proposed that SBD takes place when the injected electrons travel the oxide conduction band ballistically causing a localized physical damage in the vicinity of the anode interface. The damaged region was then modeled as a resistance in series with a trapezoidal potential barrier of reduced thickness (1.8 nm for a 4 nm oxide). According to Okada *et al.* [36], Lee's model fails to reproduce the SBD for bias below 2.5 V. On the same line of thought, Yoshida *et al.* [37] also considered a trapezoidal barrier of reduced thickness (1.6 nm for a 4 nm oxide). In this latter case, the series resistance was simply eliminated. These authors concluded that the length of the conducting filament (the damaged region in the former context) never exceeds 3 nm for all the measured oxides.

Another model based on the tunneling mechanism was proposed by Goguenheim *et al.* [38], who reported that the SBD-curves can be fitted by a simple exponential law (DT related) and suggested that SBD could result from a local reduction of the oxide thickness caused by a sudden metal/insulator transition in a localized region near to the anode interface. Halimaoui *et al.* [39] simulated the SBD current by a superposition of FN and DT currents through a locally modified oxide barrier. Although they found a good agreement in the entire voltage range, the values of the physical parameters used to fit the experimental data were qualified by themselves as questionable: a trapezoidal potential barrier as high as 6 eV with a tunneling thickness of 0.9 nm for a 4.5-nm thick oxide. In summary, all these models share the idea that SBD is caused by an oxide unilateral damaging or thinning, ranging the thickness of this modified zone from 2 to 4 nm. Analyzing the SBD temperature dependence, Okada *et al.* [36] proposed variable range hopping (VRH) as the conduction mechanism for temperatures higher than 125K, however, whether such model is valid for a 3-nm thick oxide is still questionable. It is worth mentioning that VRH predicts for the current an exponential dependence on the oxide thickness.

Recently, an alternative mechanism based on the percolation theory of nonlinear conductor networks has been proposed by Houssa *et al.* [40], which gathered much interest. In this model, it is assumed that two nearest-neighbor trap sites are connected by nonlinear resistors developed through percolation. Post SBD current versus voltage curves have been successfully fitted by Sune *et al.* [41], using Quantum Point Contact (QPC), which represents a conducting filament that has developed as a result of the percolation of defects. Here two parameters are used for fitting- the barrier height of the SBD spot and $\alpha$, which is used to correlated to the shape or thickness of the contact.

A model was also developed by Alam *et al.* [42] which explains that soft breakdown is the result of limited power dissipation available at the instance of dielectric breakdown. As the oxide ages under constant voltage stress, traps are generated via a percolation process. Current begins to flow through the path and localized joule heating may result in permanent structural damage if the local power dissipation is high enough. Alam also established the connection between the statistical distribution of the theoretically predicted percolation conductance and the distribution of experimentally measured conductance after soft breakdown [43] and explained the thickness, voltage, stress, and circuit configuration dependence of soft and hard breakdown [44].

Continual device scaling requires high-k dielectric as the replacement of the conventional silicon oxide gate dielectric to suppress the gate leakage current with an allowable level. HfAlOx is considered to be one of the most promising candidates for high-k gate dielectric. It has been investigate for the same equivalent oxide thickness (EOT), the tunneling probability for a high-k dielectric becomes lower than that for $SiO_2$ due to the increased physical thickness. However, the leakage mechanism in high-k dielectric films remains unclear, although possible mechanisms have been discussed in terms of the pure tunneling, the trap assisted tunneling, Frenkel-Poole emission, etc. In addition, the actual carrier type of leakage current has not been fully investigated, though it is significantly important from the viewpoint of reliability assurance as well as the leakage current reduction. The dielectric degradation and breakdown are most important concerns in high-k CMOS

devices. In high-k dielectric stack the defect generation mainly occurs in the high-k side rather than the Interfacial layer (IL)[45]. After the Soft Breakdown (SBD), the SBD spot area in the HfAlOx is 1.4 times greater than the SBD spot area in the $SiO_2$ [45].

## 1.3 QUANTUM EFFECTS IN MOS STRUCTURES

In the semi-classical approach, the density of states above the conduction band is assumed to be continuous, and using this continuous density of states model and the Fermi function, the classical description of the electron concentration can be obtained. This approach works well if the bands are slowly varying compared to the electron's deBroglie wavelength. However, in case of an MOS the band bending near the surface can form a quantum well, which introduces energy quantization. So the semi-classical approach does not work well for these problems, and for a precise description a quantum mechanical approach has to be used.

In the classical model, the quantization of the energies above conduction band which is assumed to be continuous. The direct effect of these on MOS capacitors or on MOSFETs is an increase of threshold voltage, because the threshold voltage is approximately the gate voltage for which, the conduction band goes below the Fermi level. However, due to the energy quantization, the lowest level that electrons occupy is not the bottom of conduction band, rather it is the first energy level, which is little higher than the conduction band edge. So to bend this band below the Fermi level, a little more gate voltage is needed. This gives rise to a threshold voltage rise in MOSFETs.

The classical distribution of the inversion charge along the depth of the depth of the device ( bulk region), we know that peak of the charge arises at the oxide semiconductor interface while the quantum mechanical distribution is totally different from that and shows that the peak of the charge arises inside. The net effect is that the actual profile (quantum mechanical) has an average distance from the surface that is larger than that predicted by the classical calculations. As we know, the average carrier distance has the effect of increasing the effective oxide thickness. Thus the quantum mechanical calculation predicts a larger effective oxide thickness, which means a lower gate capacitance. Thus for a certain gate voltage, the amount

of inversion charge will be somewhat smaller than that, predicted by the classica analysis. This is more important as the oxide thickness becomes smaller with eac technology generation.

## 1.4 SCOPE OF THE WORK

Quantum mechanical approach in extracting the parameters of an SBD spot i overlooked in most of the previous works. It is reported that the SBD path is th consequence of the percolation path between different traps [40]. However, th relation between the energy levels of traps with that of an SBD spot is absent. Th various physics based parameters, such as SBD effective barrier height, electro effective mass inside the SBD spot, SBD damage area etc are discussed in this work During high gate voltage the surrounding oxide of the SBD area are degraded. T extract these various parameters the simulated current through an SBD damage oxide is related to the previously reported experimental work [46]. The gate curre was calculated using the Tsu-Esaki expression [47]. The transmission co-efficie was calculated using Quantum Mechanical Wave Impedance (QMWI) method [48].

## 1.5 THESIS LAYOUT

This thesis consists of five chapters of which chapter one gives an introduction followed by literature review and objective of this study.

Chapter 2 deals with brief description of MOSFET fundamentals and gate tunneling currents. It also contains a brief description of the origin of traps creation and an overview of Soft Breakdown phenomenon.

In Chapter 3, the quantum mechanical calculations, SBD model of both NMOS structure and PMOS with $HfAlOx/SiO_2$ stack gate oxide structure and the current expression for MOS capacitors are discussed.

The simulation results are presented in Chapter 4 based on the expressions developed in Chapter 3.

Conclusive remarks and discussions are given in chapter 5.

# CHAPTER 2

# REVIEW OF MOS STRUCTURES AND GATE OXIDE BREAKDOWN

## 2.1 INTRODUCTION

Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), briefly termed as MOS, is the building block of the complex Integrated Circuits (IC), such as microprocessors, graphics, and Digital Signal Processing (DSP) chips. Each IC packs more than 100 million MOS transistors on a single chip. Integration of one billion transistors into a single chip will become a reality before 2010.

The basic operation of a MOS is analogous to that of a capacitor. Here, one plate acts as conducting channel between two ohmic contacts (termed as the Drain and the Source) and the other (called the Gate) controls the charge inducted in the channel. An ideal insulator is placed between the gate and the channel to prevent the flow of any current flow. This research is focused on the reliability of this gate insulator. If a conducting channel is induced by the gate then this type of structure is called enhancement type MOSFET. On the other hand, if the conducting channel is diffused during fabrication the device is called depletion type MOSFET. Enhancement type MOSFET is the most popular used MOSFET. Each MOSFET has an *n* and *p* sub-type depending on the type of carriers (electrons and holes) contributing the current. In this chapter, we focus on the MOSFET structure, operation, its history and the degradation of the Gate of MOSFET.

## 2.2 A BRIEF HISTORY OF MOSFET

The operating principle of the MOSFET transistor was first described in Lilienfield's historical patent issued in 1926. It took another 34 years before Dawon Kahng and Martin Atalla successfully built a working MOSFET in 1960.

For the past 40 years, the semiconductor industry and academia have relentlessly pushed transistor scaling. Along with scaling, the MOSFET transistor evolved from the p-MOSFET in the 1960's to the n-MOSFET in the 1970's. A good understanding of gate oxide quality, such as interface traps, fixed and mobile charges, and a good control of gate oxide quality in a manufacturing environment enabled industry to make the transition from PMOS technology to a higher-performing NMOS technology in 1970's.

## 2.3 THE MOSFET STRUCTURE AND OPERATION

The structure of an n-channel enhancement type MOSFET, shown in the figure consists of a moderately doped p-type silicon substrate into which two heavily doped n+ regions, the source and the drain are diffused. Between these two regions there is a narrow region called the channel. A layer of $SiO_2$ insulator is sandwiched between the channel and the gate made of poly crystalline silicon.

When a positive voltage is applied across the gate and substrate, positive charges are accumulated on the gate. Consequently electrons drift towards the insulator in the region between the drain and source. An increasing gate voltage changes the channel to a conductive path between the drain and source. When, a voltage is applied between drain and source, electrons move from the source to the drain creating an electric current.

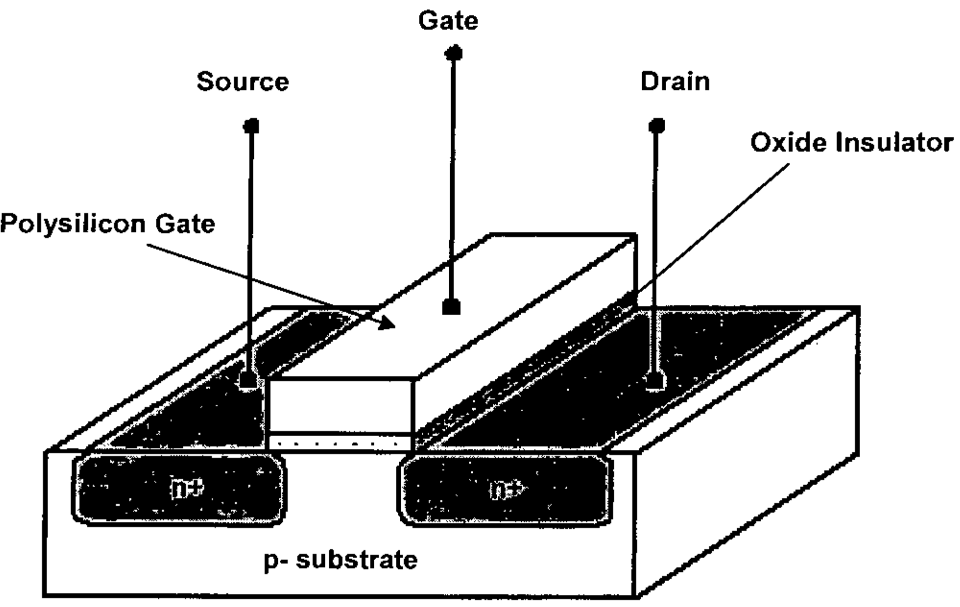



Fig. 2.1: A basic n-channel MOSFET structure.

## 2.4 MOSFET SCALING AND RECENT TRENDS

Over the past decades, the MOSFET has continually been scaled down in size to achieve lower switching time, reduces cost and lower power consumption. Typical MOSFET channel lengths were once several micrometres, but modern integrated circuits are incorporating MOSFETs with channel lengths of less than a tenth of a micrometre long. Indeed Intel will begin production of a process featuring a 65nm channel length in early 2006. Until the late 1990s, this size reduction resulted in great improvement to MOSFET operation with no deleterious consequences.

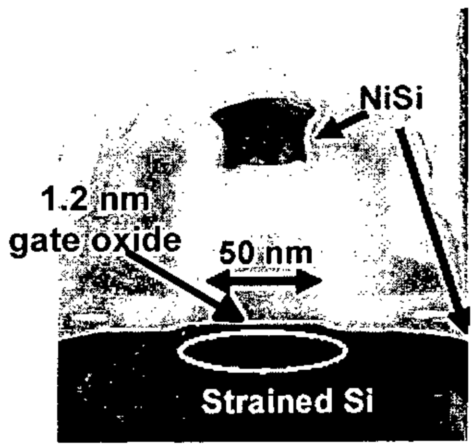



Fig. 2.2: 45-nm transistor presented in IEDM 2003 (Ref. [3]).

The most advanced MOS transistors used in volume production today are probably those of Intel's used in their 130nm logic technology with transistor gate length and gate oxide thickness are 60nm and 1.5nm, respectively. At IEDM 2003 [3], Intel presented a manufacturing-ready 90nm technology, with transistor gate length 50nm and gate oxide thickness 1.2nm. As of 2nd half of 2004, 90nm technology is at the beginning of manufacturing life cycle at a very limited number of top semiconductor manufacturers. For majority of IC manufacturers, 90nm technology is in the qualification stage or in the middle of development.

## 2.5 THE GATE AND GATE OXIDE

Early MOSFET used metal (such as aluminum) as a gate electrode, hence the name MOSFET was came. However, in fabrication processes high temperature causes metal to melt. Moreover, MOSFETs with metal gates have higher threshold voltage. Thus poly-crystalline silicon was preferable to metal as gate material as it has higher melting point. However, polysilicon is highly resistive (approximately 1000 times more resistive than metal) which reduces the signal propagation speed through the material. To lower the resistivity, dopants are added to the polysilicon. Sometimes additionally, high temperature metal such as Nickel layered onto the top of the polysilicon which decreases the resistivity. Such a blended material is called silicide. The silicide-polysilicon combination has better electrical properties than polysilicon alone and still does not melt in subsequent processing. Also the threshold voltage is not significantly higher than polysilicon alone, because the silicide material is not near the channel.

In case of the Gate Oxide, the insulator should be of high insulating property to resist leakage current from gate to the channel. As the device is scaled down, the tunneling phenomena becomes prominent leading to an increased power consumption. (The various degradation of oxide are discussed in the following sections). Insulators that have a larger dielectric constant than $SiO_2$, such as group IV(B) metal silicates e.g. Hafnium and Zirconium Silicates and Oxides, are now being researched to reduce the gate leakage. Increasing the dielectric constant of the gate oxide material allows a thicker layer while maintaining a high capacitance. The higher thickness reduces the tunneling current between the gate and the channel. An important consideration is the barrier height of the new gate oxide; the difference in conduction band energy between the semiconductor and the oxide will also affect the leakage current level. For the traditional gate oxide, silicon dioxide, the former barrier is approximately 3 eV. For many alternative dielectrics the value is significantly lower, somewhat negating the advantage of higher dielectric constant.

## 2.6 GATE OXIDE TUNNELING

According to quantum physics electrons behave both like particles and like waves and are described by the solutions of Schrödinger equation. These waves can penetrate a potential barrier that would be a forbidden area if the particle was considered in the classical way. The term tunneling phenomenon refers to this property-the particle "tunnels" through the forbidden area.

### 2.6.1 Interband Tunneling

The interband tunneling occurs because of the finiteness of the height and width of the oxide barrier. It can be either direct (DT) or Fowler-Nordheim (FN) tunneling depending upon the magnitude and polarity of the applied gate voltage. The mechanisms are governed by the shape of the tunneling barrier. If the oxide barrier is trapezoidal and the electrons do not transit through the conduction band states of the barrier, then that is called Direct Tunneling (Fig. 2.3 (a)[i]). If the tunneling barrier is triangular and the transported electrons partly transit through the conduction band states of the barrier, then FN tunneling (Fig. 2.3 (a)[ii]) occurs [49],[50].

### 2.6.2 Trap-Assisted Tunneling

With advent of modern ULSI (Ultra Large Scale Integrated) technology, the grown $SiO_2$ has reached a satisfactory purity level. However, still the $SiO_2$ is not devoid of impurities. Such impurities and oxide defects are modeled as oxide traps which in turns lead to additional leakage current. Detailed description is presented in the subsequent sections.

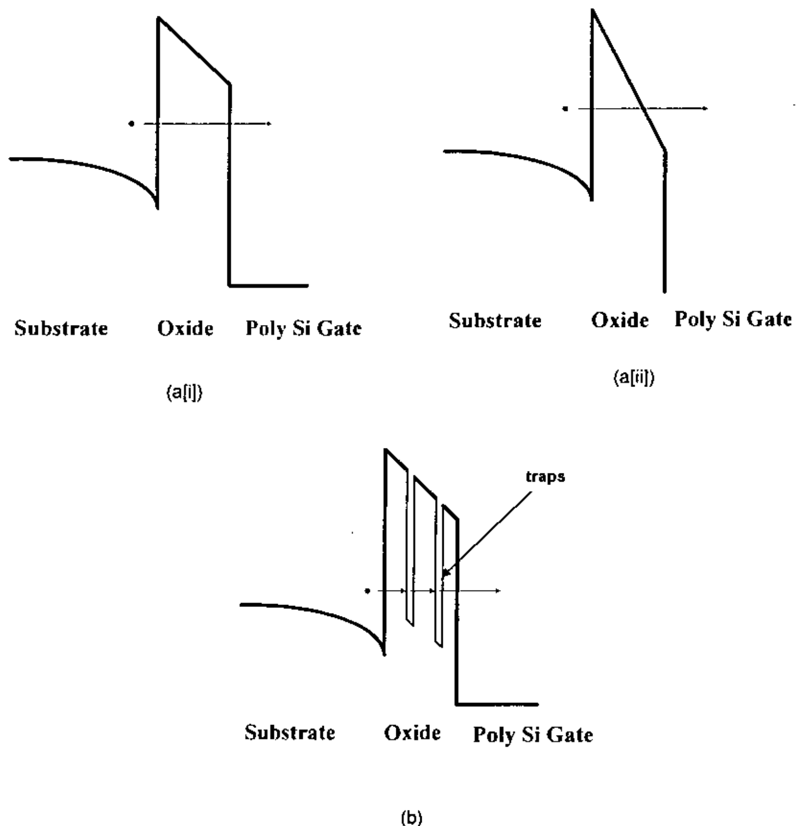



Fig. 2.3: (a) Energy band diagram of two types of Interband tunneling- [i] Direct Tunneling (DT), [ii] Fowler-Nordheim (FN) Tunneling, (b) Trap Assisted Tunneling (TAT).

## 2.7 Oxide Traps

Defects within the gate oxide are usually called traps; they are called traps because the degraded oxide can trap charges [51]. Traps are usually neutral, but quickly become positively charged near the anode, and negatively charged near the cathode [51].

## 2.8 Trap Generation

There are many different theories on how defects are generated in the gate-oxide. The two main models are the Thermochemical model ($E$ model), and the Anode Hole Injection (AHI) model ($1/E$ model), and there has been an ongoing controversy as to which model is correct, as there is data to corroborate both models [52]. Studies have showed that at high stress fields, the $1/E$ model agrees well with experimental data, and at low electric fields the $E$ model shows better agreement

with the experimental data than the $1/E$ model. Other models include the Hydrogen Release (HR) model, and the role of irradiation and channel hot-carriers. Furthermore, as a start to this section, the role of fabrication defects in the gate-oxide to breakdown will be discussed.

### 2.8.1 Fabrication Defects

Defects can be created in the oxide when the circuit is being fabricated. These defects are heavily dependent on the actual process. Defects can arise due to ion implantation during the creation of the gate, plasma damage by subsequent processing, by mechanical stress due to the isolation structure, or from process contaminants.

### 2.8.2 AHI Model

The AHI model is based on the process of electron injection into the oxide, which generates holes at the anode which then get trapped in the oxide. At high fields, this model shows better agreement to experimental data because, at such fields the electron tunneling is significant, and hole generation dominates over the Thermochemical model discussed in Section 2.8.3. The process is as follows, at high electric fields, the electrons arriving at the gate have a high kinetic energy (> $8MV/cm$) [53]. When these hot electrons reach the gate electrode they transfer their entire energy to a deep-valence band electron, and then this electron is promoted to the lowest available electron energy state, which is the conduction band edge of the anode [54]. Once the electron reaches the conduction band, it creates a hot hole, which tunnels into the oxide [54]. The holes which enter the oxide, allow for increased current density due to *hole induced trap generation* [54]. Once the trap has been created, and there is increased current density, there are more high energy electrons entering the gate which can create more hot holes, and thus there is positive feedback until breakdown occurs. An example of how a hole can create a trap in the oxide is shown in Fig. 2.4, where the holes induce two bond breakages at a single Si atom.

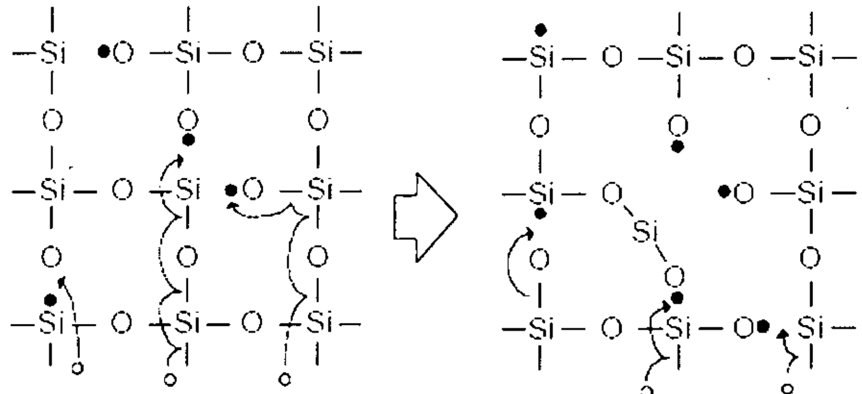


Fig. 2.4. $SiO_2$ Bond Breakage due to Hole Current [53]

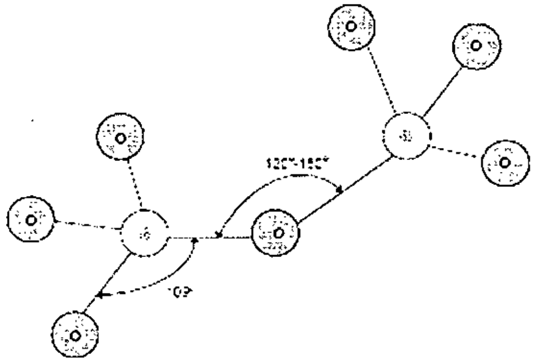


Fig. 2.5. Chemical Structure of $SiO_2$ [54]

### 2.8.3 Thermochemical Model

The *1/E* model presented above ignores important thermal processes which degrade all materials over time [55], and some recent work which covers ranges of temperature and field conditions show better agreement with the *E* (Thermochemical model) [55]. Amorphous $SiO_2$'s primary structural unit is the $SiO_4$ tetrahedron shown in Fig. 2.5. The angle between O-Si-O is always 109°, but the angle between the bond linking the tetrahedral ranges from 120° to 180° [55]. When the linking bond angle is above 150°, the bond's strength is severely weakened and an oxygen vacancy results where the Si-O-Si bond is replaced with a Si-Si bond [55].This oxygen vacancy is thought to be the defect that leads to oxide breakdown [55]. The remaining O-Si bonds within the oxide are highly polar bonds; 70% of the total energy is due to ionic contribution [55].

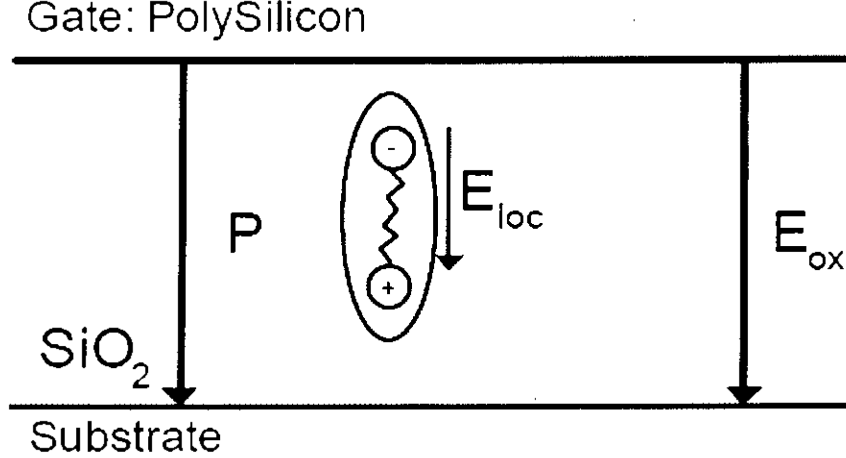



Fig. 2.6. Local Electric Field in $SiO_2$ [55]

Furthermore the Si-Si bond is a very weak bond [55]. Thus when an electric field is applied to the oxide, there is a distortion of the lattice due to the polar nature of the O-Si bond [13]. Furthermore, this distortion induces a polarization P as shown in Fig. 2.6. Thus each molecule of $SiO_2$ will not only experience the externally applied electric field, but it will also experience the dipolar field due to P [55], and thus the local electric field, $E_{loc}$, can be significantly larger than the applied field $E_{ox}$. Thus the Si-Si bonds are heavily strained due to this large local electric field, and bonds may occasionally gain enough thermal energy to cause the Si-Si bond to break, creating a hole trap. As noted above the generation of many traps will finally lead to breakdown.

## 2.9 SOFT BREAKDOWN PHENOMENA OF GATE OXIDE

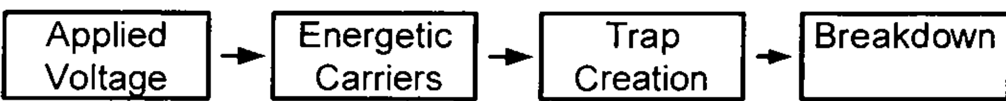



Fig. 2.7. Schematic illustration of the general framework of breakdown models.

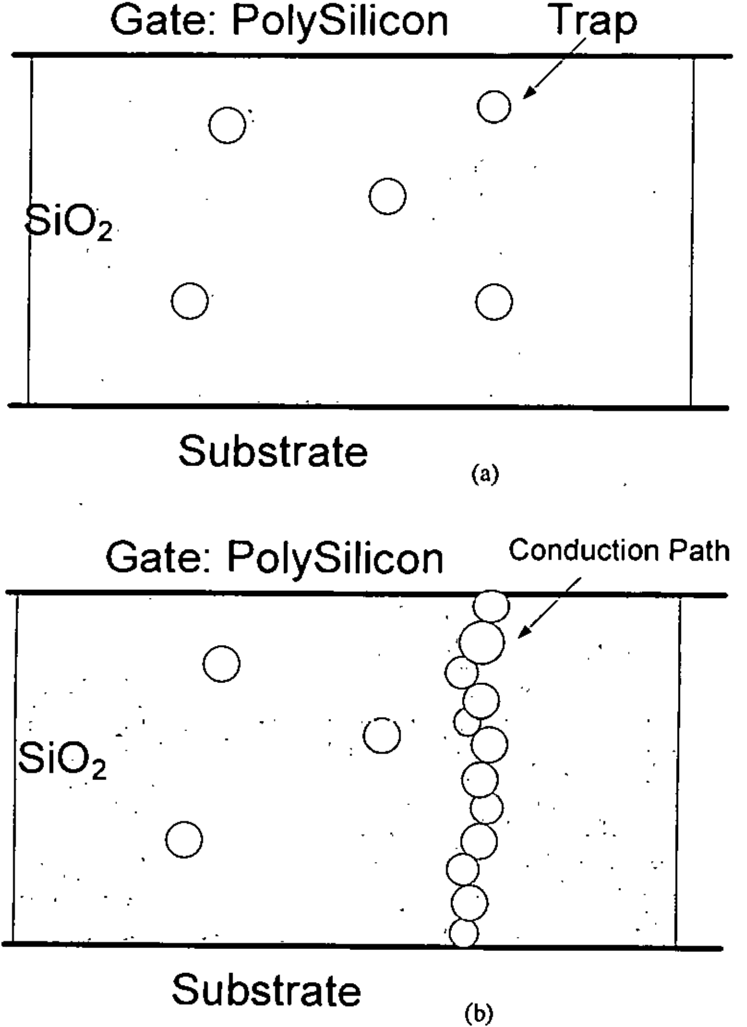



Fig. 2.8. Series of schematics illustrating the percolation of defects and ultimate breakdown in ultra-thin gate oxides. Oxide traps (circles) are generated randomly throughout the volume of the dielectric in step 1. If two neighboring traps overlap or are in contact with one of the electrodes conduction is possible. Breakdown occurs when a conducting path is created from one interface to another shown in step 2.

In 1994, a new failure mechanism was identified by Lee *et al.* [32] in ultra-thin oxide. This new phenomenon is identified as an abrupt change in the oxide conductance, which is several orders of magnitude smaller than that associated with the HBD-the conduction mode initially has been named Quasi Breakdown (QBD). This failure mode was also known as B-mode SILC [55]. (The conventional Stress Induced Leakage Current, SILC was named A-mode SILC). However, at present this mode is widely known as Soft Breakdown [5].

Two main features of this Soft Breakdown can be highlighted: i) during a high-field stress, several SBD events can occur in a single sample and this causes an apparent increase of the area involved in the conduction [56] and ii) the application of a low voltage after the occurrence of SBD events leads to the observation of large current fluctuations which have the appearance of a random telegraph signal (RTS) [56].

# CHAPTER 3

# CALCULATION OF QUANTUM MECHANICAL TUNNELING PARAMETERS IN CMOS STRUCTURES

## 3.1 INTRODUCTION

In order to calculate the current density through an oxide barrier and to understand the resonant tunneling process, an estimation of quantum mechanical transmission co-efficient (QMTC) is across the oxide potential barrier and quantum well structure is needed. The transport properties of tunnel structures may be analyzed by solving the one-electron, one-dimensional, time-independent Schrödinger equation.

The conventional method for determining the QMTC has been the Wentzel-Kramer-Brillouin (WKB) approximation [57],[58]. Although conceptually elegant, it is an approximation that does not take into account the detailed structure of a given potential below the penetrating electron energy level. Furthermore, it predicts incorrect resonant energies of a resonant system [59]. The WKB method is a quasi-classical approximation and is valid when the De-Broglie wavelengths of electrons are small compared to the distance over which the potential changes appreciably.

Chandra and Eastman [60] calculated the QMTC for a triangular barrier via the numerical method using Taylor series expansions for the wave function and its derivative. Although this method can be extended to include arbitrary structures, large number of grid-points may very often be necessary, which is computationally inefficient. There are other methods, but all of them require extensive matrix manipulation.

A simple method of calculating the QMTC of tunneling structures is presented in Sec 3.4.2; this method was formulated by Khondoker et al. [48].

## 3.2 SELF-CONSISTENT MODEL

The self consistent solution of coupled Schrodinger's and Poisson's equations as proposed by Stren [61] is presented in this section which is based on three major approximations. It is assumed 1) that the effective mass approximation is valid, so that the periodic potential can be neglected. The effective masses and the dielectric constant of the periodic potential can be used. 2) That the envelop wave function vanishes at the surface. Neither approximation is likely to be valid at high electric field. The third major approximation 3) is that surface states can be neglected and the effect of charges in the oxide or insulator adjacent to semiconductor can be replaced by an equivalent electric field.

The band bending of a semiconductor can be characterized by a potential Ø(z). In the effective mass approximation, the electron wavefunction for the ith subband is the product of the Bloch function at the bottom of the conduction band and envelope function. Envelope function $\psi_i(z)$ is the solution of

$$\frac{d^2\psi_i}{dz^2}+\frac{2m_{zi}}{\hbar^2}\left[E_i+e\phi(z)\right]\psi_i(z)=0 \qquad (3.1)$$

Here $m_{zi}$ is the effective mass in the direction perpendicular to the interface and $E_i$ is the energy f the ith bound state in the same direction. Boundary conditions commonly used for the solution of Eq. (3.1) are $\psi_i(\infty)=0$ and at the semiconductor-oxide interface, $\psi_i(0)=0$. Each solution of Eq. (3.1) gives the bottom of a continuum of levels called a subband. There can be as many as three values of $m_{zi}$ depending on the surface orientation because the conduction band of Si has six ellipsoid valleys along the (100) family direction. Solution of Eq. (3.1) gives the Eigenenergy $E_i$ and the envelop function $\psi_i(z)$.

The potential Ø(z) is found from the solution of Possion's equation, which is as follows.

$$\frac{d^2\phi(z)}{dz^2}=-\left[\rho_{depl}(z)-e\sum_i N_i\psi_i^2(z)\right]\Big/\varepsilon_{Si}\varepsilon_o \qquad (3.2)$$

Here $\varepsilon_{si}$ is the dielectric constant of the semiconductor, $N_i$ is the carrier concentration in the ith subband. $N_i$ is given by the following equation,

$$N_i = \frac{n_{vi} m_{di} kT}{\pi\hbar^2} \ln\left[1 + \exp\left(\frac{E_F - E_i}{kT}\right)\right] \qquad (3.3)$$

Where $m_{vi}$ is the valley, $m_{di}$ is the density of states effective mass per valley and $E_F$ is the Fermi energy.

$$\rho_{depl}(z) = - e(N_A - N_D), \quad 0 < z < z_d$$
$$\rho_{depl}(z) = 0, \quad z > z_d \qquad (3.4)$$

here, $z_d$ is the depletion layer thickness given by [61] as following,

$$z_d = \sqrt{\frac{2\varepsilon_{si}\varepsilon_o \phi_d}{e(N_A - N_D)}} \qquad (3.5)$$

$\O_d$ is the band bending due to depletion charge only. $\O_d$ can be calculated from [62] as following,

$$\phi_d = \phi_s - \frac{kT}{e} - \frac{eN_{inv} Z_{av}}{\varepsilon_{si}\varepsilon_o} \qquad (3.6)$$

Where $N_{inv} = \Sigma_i N_i$ is the total number of charge per unit area in the inversion charge density into Si. The two boundary conditions for solution of Eq. (3.2) are $d\O/dz=0$ for large z and at the surface, its value is $F_s$. From [61], $F_s$ is given by,

$$F_s = \frac{e(N_{inv} + N_{depl})}{\varepsilon_{si}\varepsilon_o} \qquad (3.7)$$

$N_{depl} = z_d (N_A - N_D)$ is the number of charge per unit area in the depletion layer. In a self-consistent formulation, Eqs. (3.1)- (3.6) are solved iteratively for a given $F_s$ until results converge.

In this work, we use a technique, based on Green's function formalism, to solve Schrödinger's equation with wave function penetration. This technique is described

in detail in [63], [48]. Open boundary conditions are used, which are based on the assumption that the potential profile is flat at deep inside the gate metal as well as at deep inside the bulk semiconductor. Our assumption implies that the wave function deep inside the semiconductor is exponentially decaying and deep inside the gate metal, the wave function is a plane wave.

The eigenenergies of the quasi-bound states are calculated by locating the peaks of the one-dimensional (1-D) density-of-states [64]. The corresponding wave functions including penetration can easily be obtained using the relationships described in [65]. Once the eigenenergies and the wave functions are calculated, the self-consistent formulation is applied with appropriate modifications to include penetration effects also in the solution of Poisson's equation. Since a fraction of inversion charge resides within the gate-oxide due to wave function penetration, Poisson's equation is solved for the combined oxide and semiconductor regions with the boundary conditions applied at the gate metal-oxide interface.

### 3.3. THE SOFT BREAKDOWN MODEL

In section 2.8, the literature of Soft Breakdown Phenomena is discussed in details. Soft Breakdown spot is an extremely localized damage in the oxide [66]; however its conduction level is several orders lower than that of Hard Breakdown. It is proposed that the SBD path is created when a percolation path of non-linear resistors is created between adjacent traps [46].

During the electrical stress on the gate oxide traps generate randomly in the ultrathin $SiO_2$. As more and more traps are created, they start to be overlap. For that Conduction Path is created. This is called SBD path.

The concept of barrier height lowering is introduced in our solver. According to Lee et al. we use lower barrier height at the SBD spot area [32]. In Fig 3.1 shows that in the SBD spot area we reduced the barrier height and in the undamaged area the barrier height remain unchanged. To match our simulated data with the experimental data, we varying the imaginary potential, the effective mass of the electron in the $SiO_2$, the SBD barrier height and the SBD spot area. To incorporate the scattering effect or any type of loss we use the imaginary potential.

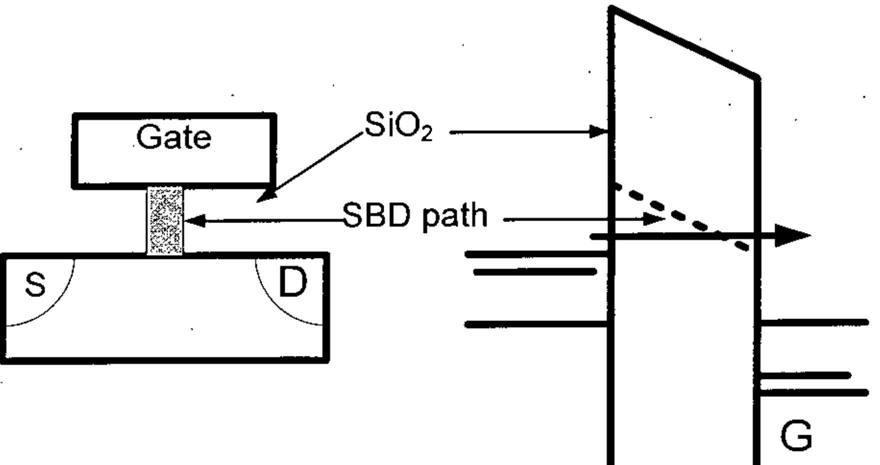



Fig. 3.1. Schematic profile of an energy band diagram of the SBD spot area and the fresh oxide area.

We also make the following assumptions:

1) The barrier of the damage oxide is lower than the barrier of the undamaged oxide.
2) The SBD spot is assumed to be cylindrical.
3) The gate oxide degradation around the SBD area is absent here.

### 3.3.1. SOFT BREAKDOWN SPOT AREA MODEL FOR NMOSFET

The reliability of gate oxide becomes of great importance as the gate oxide thickness of the next generation MOS devices is approaching to the physical limitation of direct tunneling [67, 68]. Recent reports have shown that the wear-out behavior of ultrathin gate oxide near to the physical limitation thickness has a different trend with the thickness decrement [69, 70, and 71]. Some models have been proposed to explain the soft breakdown property in the gate oxide.

The concept of lowering the barrier height at the soft breakdown spot is introduced here to calculate the soft breakdown current.

The quasi-breakdown is related to the electron traveling distance in the oxide conduction band. When the oxide is thin enough and/or the applied field is low. the

traveling distance of electrons in the oxide conduction band after F-N tunneling would be shorter than electron mean free path. In this case, the electrons travel the oxide conduction band ballistically and thereby release most of their energy at the anode region only. Continuous accumulation of the energy at the anode could lead the generation of the physically damaged region (PDR) near the $Si/SiO_2$ interface in the form of broken bonds.

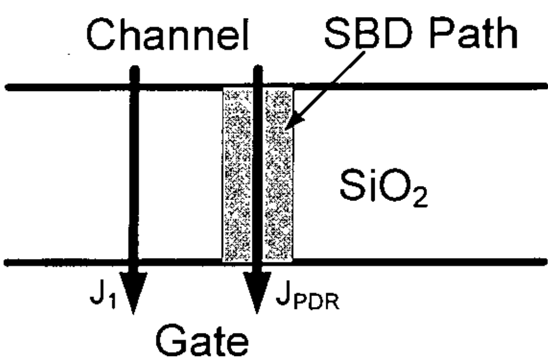



Fig. 3.2 Schematic diagram for current path in the oxide after soft breakdown

In Fig. 3.2. The total gate current ($J_T$) would be a superposition of the tunneling current through the undamaged oxide area ($J_1$) and the direct tunneling current through the physically damaged region (PDR) ($J_{PDR}$), and it can be described as

$$J_T = ( 1 - A_{ratio} ) J_1 + A_{ratio} * J_{PDR} \quad (3.8)$$

when we define Aratio as

$$A_{ratio} = A_{PDR} / A_{cap}$$

where $A_{PDR}$ is the area at which soft breakdown occurred and $A_{cap}$ is the total MOSFET area.

### 3.3.2. SOFT BREAKDOWN SPOT AREA MODEL FOR PMOS WITH HIGH-k GATE DIELECTRIC

Recently high-k materials have been proposed as alternative gate dielectrics to suppress the gate leakage current and soft breakdown phenomena [72]. The dielectric stack reliability is improved by increasing of the high k layer thickness. HfAlOx is considered to be the most promising candidate for high-k gate dielectric.

As the device size is scaled down, the physical thickness of the high-k dielectric is needed to reduce. It has been investigate that both the defect generation rate and the defect size in the $HfAlOx/SiO_2$ stack are large compared with those in $SiO_2$ [45].

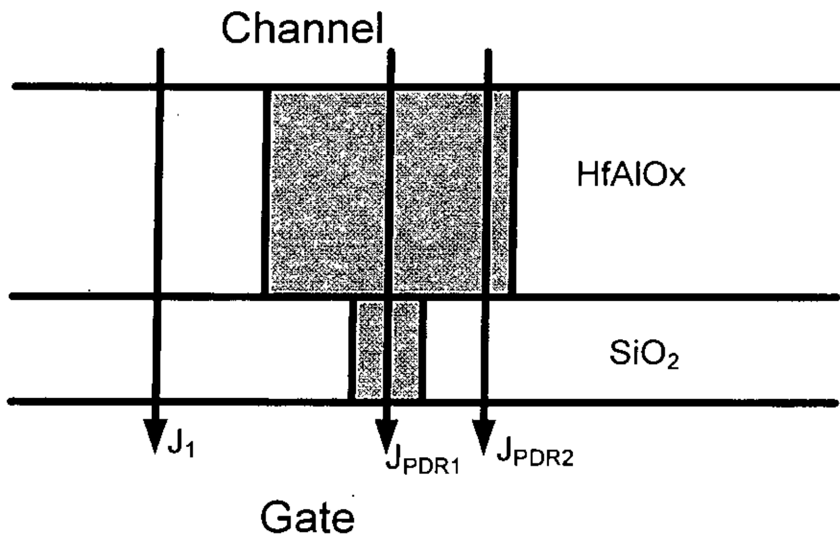



Fig. 3.3 Schematic diagram for current path in the $HfAlOx/SiO_2$ stack gate after soft breakdown

The total gate current ($J_T$) would be a superposition of the tunneling current through the undamaged oxide area ($J_1$), the tunneling current through both the damaged $SiO_2$ and HfAlOx layer ($J_{PDR1}$), and of the tunneling current through both the undamaged oxide area and the damaged HfAlOx area ($J_{PDR2}$), it can be described as

$$J_T = (1 - p^*A_{ratio})\, J_1 + A_{ratio}{}^*\, J_{PDR1} + a^*A_{ratio}{}^*\, J_{PDR2} \quad (3.9)$$

Where we define Aratio as

$A_{ratio} = A_{PDR} / A_{cap}$,

Where $A_{PDR}$ is the area at which soft breakdown occurred and $A_{cap}$ is the total MOSFET area.

a= (0.3~0.5), [45]

and p=a+1

### 3.3.3. LEAST SQUARE ERROR TECHNIQUE

To match the simulated curve with the experimental curve we use least square error technique.

$$Deviation = \sum_{n=1}^{\alpha} (error(n))^2 \tag{3.10}$$

Where error (n) = I (SBD simulated)-I (Exp.); n=1, 2, 3....n

## 3.4. CURRENT DENSITY FORMULA

The nonzero probability for tunneling of electrons through potential barrier offers the possibility of measurable currents. A typical situation is shown in Fig. 3.4 where an electron plane wave is specified by a total energy E and a transverse wave vector $k_t$. For arbitrary potential barrier, electrons incident upon the potential from both the electrodes will contribute to the total current. First, let us consider the contribution from electrons incident from the emitter. Since electrons are fermions, these electrons will contribute to the total current only if there are corresponding empty states on the side to which the electrons can tunnel. Assuming conservation of total energy and transverse momentum [47], the tunneling current density $J_{E\text{-}C}$ from a unit volume of k-space is [70].

$$J_{E-C} = \frac{q}{\hbar}\left(\frac{\partial E}{\partial k_x}\right)_E g(k) f_E(E)[1 - f_C(E + qV_a)]T(E, k_t) \tag{3.11}$$

where, $f_E$ (E) and $f_C$ (E) are the Fermi-Dirac electron distribution function at the emitter and collector electrode respectively. g(k) is the density of states per unit volume of k-space.

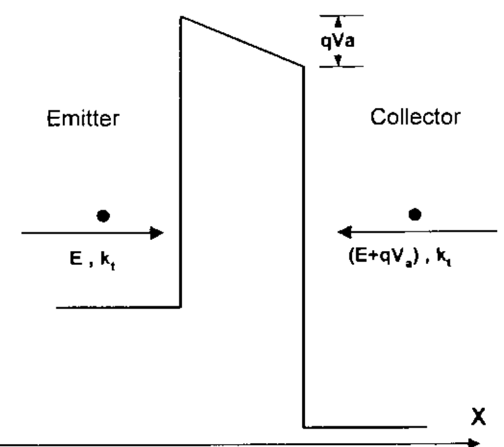



Fig. 3.4. A schematic representation of a potential energy profile employed in the derivation of the current density expression.

A similar analysis can be used to obtain the contribution from electrons of energy (E+qV$_a$) incident from the collector. Since the tunneling probability is equal for both directions, the tunneling current density $J_{C\text{-}E}$ from the collector to the empty states of the emitter is given by,

$$j_{C\text{-}E} = \frac{q}{\hbar}\left(\frac{\partial E}{\partial k_x}\right)_{(E+qV_a)} g(k) f_C(E+qV_a)\left[1-f_E(E)\right]T(E,k_t) \qquad (3.12)$$

The net tunneling current density per unit volume of k-space is,

$$J_t = J_{E\text{-}C} - J_{C\text{-}E} \qquad (3.13)$$

The density of states per unit volume of k-space is evaluated to be [64]

$$g(k) = \frac{2}{(2\pi)^3} \qquad (3.14)$$

The Fermi-Dirac electron distribution function is given by,

$$f(E) = \frac{1}{1+\exp\left(\frac{E-E_F}{k_B T}\right)} \qquad (3.15)$$

Where, $E_F$ is the Fermi energy, $k_B$ Boltzman's constant and T is the absolute temperature.

To simplify the analysis, we neglect the velocity difference between the electrons of emitter and collector and evaluate the derivative in Eqn. (3.12) at E instead of at $(E+qV_a)$. The assumption of parabolic energy momentum relationship for states describing the contacts reduces Eqn. (3.13) to,

$$J_t = \frac{2}{(2\pi)^3}\frac{q\hbar k_x}{m^*}\left[f_E(E) - f_C(E+qV_a)\right]T(E,k_t) \tag{3.16}$$

The electron effective masses for the two electrodes are assumed to be equal. Integrating $J_t$ over the entire k-space the total current density can be obtained

$$J = \frac{2}{(2\pi)^3}\frac{q\hbar}{m^*}\int_0^\infty\int_0^\infty k_x T(E,k_t)\left[f_E(E) - f_C(E+qV_a)\right]2\pi k_t\, dk_t dk_x \tag{3.17}$$

$$\therefore J = \frac{2qm^*}{(2\pi)^2\hbar^3}\int_0^\infty\int_0^\infty T(E,k_t)\left[f_E(E) - f_C(E+qV_a)\right]dE_t dE_x \tag{3.18}$$

where,

$$E = \frac{\hbar^2 k_t^2}{2m^*} + E_x \tag{3.19}$$

The effect of mass variation on the transverse motion can be neglected, as done by several authors [47], [70], [72]. This makes the transmission coefficient dependent only on the longitudinal energy $E_x$=E-$E_t$. The $E_t$ integral can now be performed giving the usual Tsu-Esaki expression [47]:

$$\therefore J = \frac{qm^* k_B T}{2\pi^2\hbar^3}\int_0^\infty T(E_x)\ln\left[\frac{1+\exp\left\{\frac{(E_{F_E} - E_x)}{k_B T}\right\}}{1+\exp\left\{\frac{(E_{F_C} - E_x - qV_a)}{k_B T}\right\}}\right]dE_x \tag{3.20}$$

The spatial dependence of effective mass is however taken into account to calculate $T(E_x)$ in Eqn. (3.20).

In the derivation of tunnel current expression the velocity of an electron of energy ($E+qV_a$) incident from the collector is assumed to be equal to that of an electron of energy E incident from the emitter. Collins *et al.* [70] found the contribution to J due to the velocity difference to be less than 10% for physically relevant tunneling systems. This is conceivable, since at low voltages the velocity difference is small, while at higher voltages the contribution from the collector is insignificant.

### 3.4.1 QUANTUM MECHANICAL CALCULATIONS FOR POTENTIAL BARRIERS

The calculation of Quantum Mechanical Transmission Co-efficient (QMTC) is necessary for analyzing the current–voltage (I-V) characteristics of resonant tunneling and quantum size devices [72]. In this work the QMTC is calculated by Quantum Mechanical Wave Impedance (QMWI) method formulated by Khondker *et al.* [48].

Using the effective mass approximation the one dimensional Schrödinger Equation is written as

$$-\frac{\hbar^2}{2}\frac{d}{dx}\left(\frac{1}{m^*(x)}\frac{d\psi}{dx}\right)+[V(x)-E]\,\psi(x)=0 \tag{3.21}$$

where, $\psi(x)$ is the envelope wave function, E is the energy of incident electron and V(x) is the potential energy. Here, $m^*(x)$ is the effective mass and ħ is the reduced Planck's constant. If we consider constant effective mass and potential constant then the Schrödinger equation reduces to,

$$\frac{d^2\psi}{dx^2}+\frac{2m^*}{\hbar^2}[E - V(x)]\psi(x)=0 \tag{3.22}$$

and the solution of the Eqn. (3.22) is,

$$\psi(x)=A^+\left(e^{\gamma x}-\rho e^{-\gamma x}\right) \tag{3.23}$$

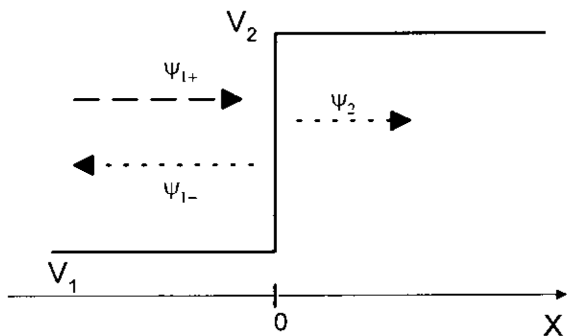



Fig. 3.5. A step potential barrier with potential height of ($V_2$-$V_1$). Where, the propagation constant, $\gamma$ is given by

$$\gamma = \alpha + j\beta = j\sqrt{\frac{2m^*[E - V(x)]}{\hbar}} \tag{3.24}$$

In Fig. 3.5, the wave function $\psi(x)$ in the region where x<0, can be defined as the superposition of two waves – one the incident wave $\psi_+$ and another is the reflected wave $\psi_-$ that is reflected from the potential discontinuity at x=0.

### 3.4.2 *Calculation of QMTC*

Now, differentiating Eqn. (3.23) w.r.t. *x* and multiplying on both sides by factor ($\hbar/jm^*$) we get,

$$\phi(x) = A^+ Z_0 \left(e^{\gamma x} + \rho e^{-\gamma x}\right) \tag{3.25}$$

Where,

$$Z_0 = \gamma\hbar / jm^* \tag{3.26}$$

According to Khondker *et al.* [48] the terms $\psi(x)$ and $\phi(x)$ are analogous to the distributed parameters I(x) and V(x) of transmission lines respectively. The term $Z_0$ is regarded as characteristic impedance of the region with potential V(x) that is analogous to the characteristic impedance of transmission line. The new parameter introduced by Khondker *et al.* [48] is Quantum Mechanical Wave Impedance, which

is defined as [48],

$$Z(x)=\frac{\phi(x)}{\psi(x)}=R(x)+jX(x) \tag{3.27}$$

Where, R(x) and X(x) are the real and imaginary parts of the QMWI at any point.

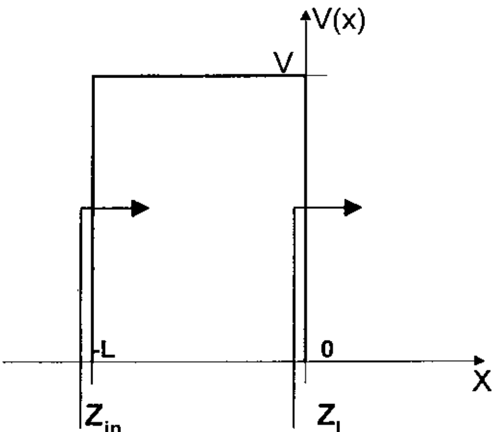



Fig. 3.6. Calculation of QMWI for a potential barrier of length L.

Fig. 3.6 illustrates the calculation of Z(x) using simple formula. If the load impedance at point x=0 is $Z_L$, then the input impedance at point x=-L will be Z(x) $=Z_{in}$ (Fig. 3.5).

Here,

$$Z_{in}=Z_0\frac{Z_L\cosh\gamma L-Z_0\sinh\gamma L}{Z_0\cosh\gamma L-Z_L\sinh\gamma L} \tag{3.28}$$

In similar way, the QMWI can be determined at the potential boundaries. Such method can also be applied for potential profiles that vary continuously with x. In such case, the potential profile is approximated as multi step functions with a sequence of N segments each having a length of L.

Here, the QMWI of the segment 1 at the boundary is considered $Z_L$ (or $Z_1$) looking to the right. By using Eqn. (3.28) we determine the input QMWI of segment 1 (or $Z_2$). This input impedance serves as the load QMWI for segment 2. In this way, the

input QMWI of N-th segment can be determined, which is the input QMWI of the whole potential profile.

Now, after determining the QMWI of the whole potential structure, the amplitude reflection co-efficient is calculated by,

$$\rho(E)=\frac{Z_L - Z_0}{Z_L + Z_0} \tag{3.29}$$

The Quantum Mechanical Transmission Co-efficient (QMTC) will be determined by,

$$T(E)=1-|\rho(E)|^2 \tag{3.30}$$

The next section will be dedicated to a detailed numeric example for calculating QMWI and QMTC.

### 3.5 CONCLUSION

By solving this self-consistent model we get the properties of carriers in inversion layer such as band bending, Eigen states, wave function distribution, carrier concentration, position of Fermi-level etc. Following Khondker et al. [48] we get Transmission Co-efficient, T (E) and then gate current after the Soft breakdown is calculated using Eqn. 3.8, Eqn. 3.9, Eqn 3.10 and Eqn 3.20.

# CHAPTER 4

# RESULTS

## 4.1 INTRODUCTION

In this chapter, the simulated results using the expressions summarized in the previous chapter are presented in details. The aim of this work is to find out the parameters of a Soft Breakdown (SBD) path from the I-V characteristics of gate oxide after a single SBD event. The focus of this work is two-fold; (i) to investigate the oxide effective mass, imaginary potential inside the oxide, oxide barrier height at the SBD area and the spot area for a given NMOS device specimen and (ii) to measure the oxide effective mass, imaginary potential, the oxide barrier height at the SBD area and the spot area both inside the oxide and HfAlOx for a PMOS device with high-k gate dielectric. And also find the ratio between the high-k SBD spot area and the $SiO_2$ oxide SBD spot area.

## 4.2 SIMULATED PARAMETERS

The simulations are performed for a MOS capacitor, with $SiO_2$ grown on p-Si substrate (100) with $N_A=5\times10^{17}$ $cm^{-3}$.The effective mass of electrons in Si is taken as $m^* = 0.916m_0$ for longitudinal valley and $m^* = 0.19m_0$ for transverse valley.

### 4.2.1 PARAMETERS FOR NMOS STRUCTURE

Oxide thickness, $T_{ox} = 4.5nm$

Oxide area = $20\mu m\times5\mu m$

$SiO_2$ barrier height, $E_{ox} = 3.25$ eV

effective mass of electrons in $SiO_2$,$m^* = 0.5m_0$ (Fresh oxide)

## 4.3 POTENTIAL PROFILE OF NMOS STRUCTURE

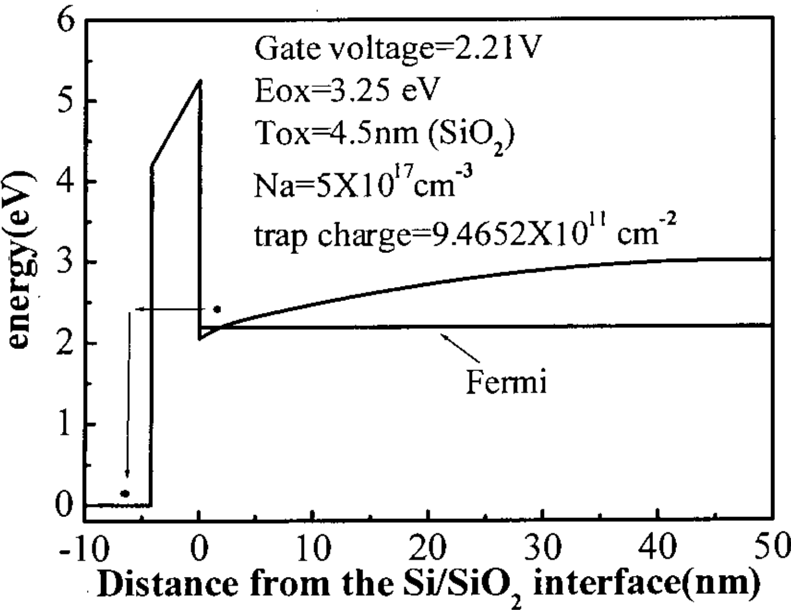



Fig.4.1. The simulated profile of an energy band diagram of a p-Si-$SiO_2$-n-poly Si structure. Here substrate doping density, $N_A=5\times10^{17}$ $cm^{-3}$ and the interface trap charge is taken $9.4652\times10^{11}$ $cm^{-2}$

The simulations are performed for a MOS capacitor, with $SiO_2$ grown on p-Si substrate (100) with $N_A = 5\times10^{17}$ $cm^{-3}$. The gate is made of poly Silicon with n-type doping. Fig. 4.1 shows the band diagram of Si-$SiO_2$-poly Si structure for none bias condition. Here, the band tilting inside $SiO_2$ is quantum mechanically calculated. The height from the conduction band edge of Si to that of $SiO_2$ is considered to be 3.25 eV [73]. In fact this barrier height differs in literature and varies between 2.3 eV and 5 eV [74].

The effective mass inside oxide, which depends upon the fabrication process, growth and condition of the amorphous oxide layer, varies between $0.25m_0$ and $1.03m_0$, as used by previous researchers [75],[76]. In this work the effective mass of electron inside $SiO_2$ is taken as $0.5m_0$.

### 4.3.1 SIMULATED FRESH OXIDE CURRENT DENSITY FOR NMOS

We know that the gate current shows different characteristics in two different regimes; the direct tunneling (DT) regime and the Fowler-Nordheim (FN) regime. In case of 4.5 nm gate oxides the direct tunneling current exhibits fluctuations (Fig. 4.2) when the applied voltage is less than 3.2V. However, the current rises sharply with the increase in the applied voltage as it enters the FN tunneling regime. In this regime the gate current shows an oscillating behavior [75] (the oscillations are absent in the results presented here as the gate voltage is limited to 5V). To incorporate the scattering effect in the oxide, complex potential, $V(x) = V_r(x) - iV_i(x)$ profile is introduced inside the oxide. The imaginary potential is related to the particle scattering lifetime, $\tau$ as $V_i = \hbar/2\tau$ [77]. For 4.5 nm thick oxide, change of $V_i$ within small range causes noticeable change in current density for low voltage range (below 3V) which is shown in Fig. 4.2. Adding $V_i$ means the electrons leaving from the desired state to the other state making it an empty state. For that the probability of tunneling current through the gate oxide increases. Imaginary potential also smoothes the wave shape of the gate current. The variation of the I-V characteristics with the electron effective mass is shown in Fig. 4.3. The figure shows using low effective mass causes noticeable change in current density at high gate voltage range (above 3V).

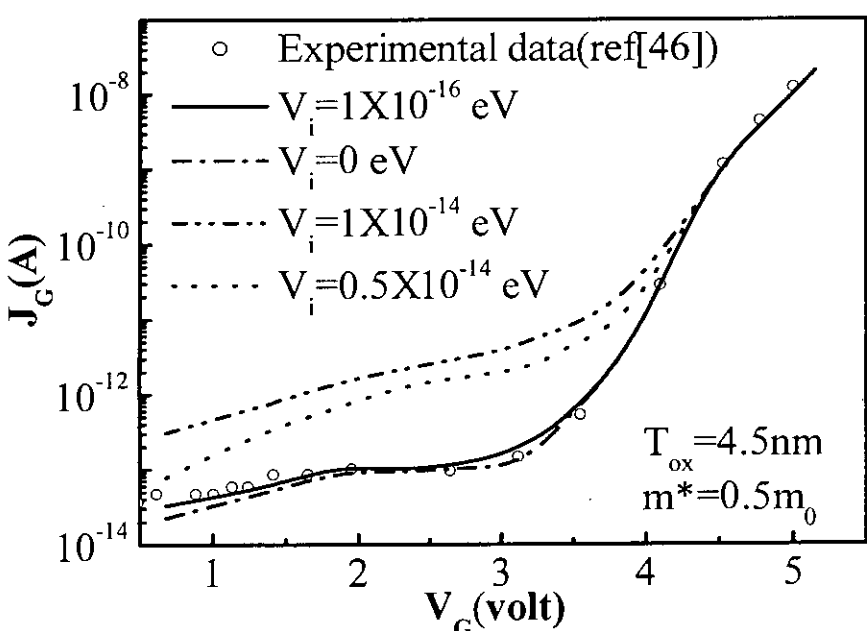



Fig. 4.2. Current density as a function of applied voltage- imaginary potential inside $SiO_2$ as a parameter.

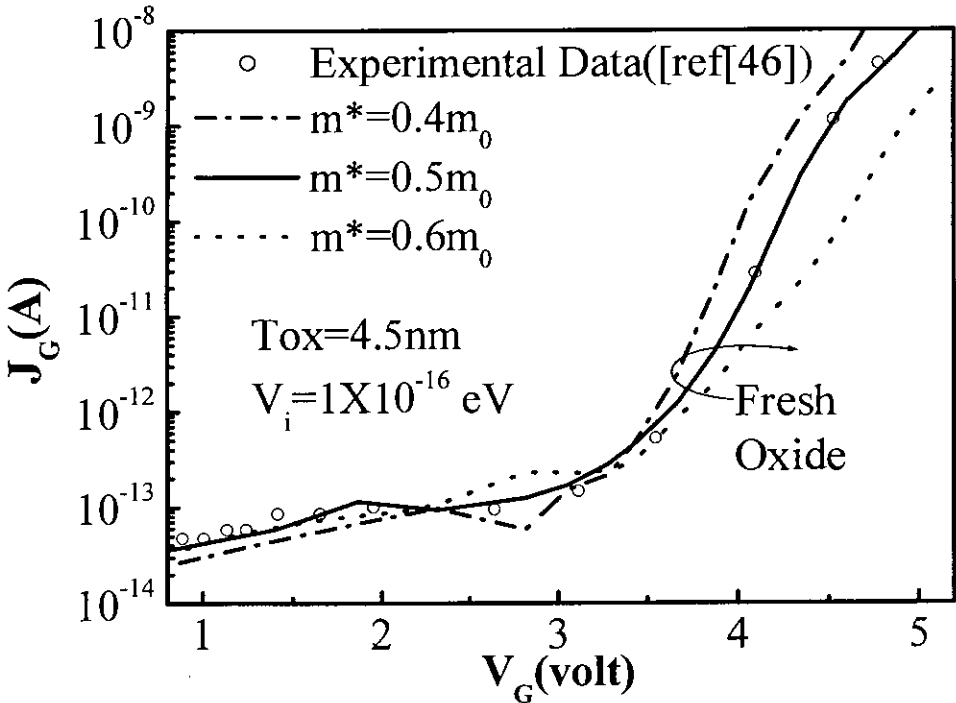



Fig.4.3. Simulated current density versus applied voltage curves for fresh oxide. Fitting the experimental data ref [46 ] by varying m* inside $SiO_2$ as a parameter.

### 4.3.2 SIMULATED SBD CURRENT DENSITY FOR NMOS

The current density has a strong dependence on the potential barrier height of the oxide. Lowering the barrier height creates significant increase in the gate current.

As the SBD is the consequence of the percolation connection of these traps we propose that the SBD path has an effective barrier height whose conduction band edge is 0-3 eV below that of the unaffected barrier. Therefore, in this work the SBD spot is characterized as the barrier lowering. The SBD spot is assumed to be cylindrical.

The total current density is obtained using superposition of the current through the SBD spot and the current through the remaining area. Here, the remaining oxide other than that of the SBD spot is assumed to be unaffected. In reality, when electrical stress is applied the degradation occurs almost in the whole oxide area [25]. However, the SBD current is several orders larger than that of a non-SBD but degraded oxide. So, such assumption can be safely incorporated.

Fig. 4.4 and 4.5 show the simulated gate oxide current using the Tsu-Esaki relation. The imaginary potential and the effective mass of electron inside the oxide were varied to achieve better agreement with the experimental data. Increasing the imaginary potential ($V_i$) the SBD current density increases which has a significant contribution at the low applied bias voltage (below 3V). For obtaining better fit the imaginary potential and the effective mass is considered $10^{-14}$ eV and $0.5m_0$ respectively. The curves exhibit slight oscillatory nature (a characteristic of FN current) for the electron effective mass less than $0.4m_0$ and greater than $0.5m_0$ (Fig. 4.5). Therefore, for the remaining simulations the effective mass of electron for the SBD spot is considered the same as that of the remaining oxide.

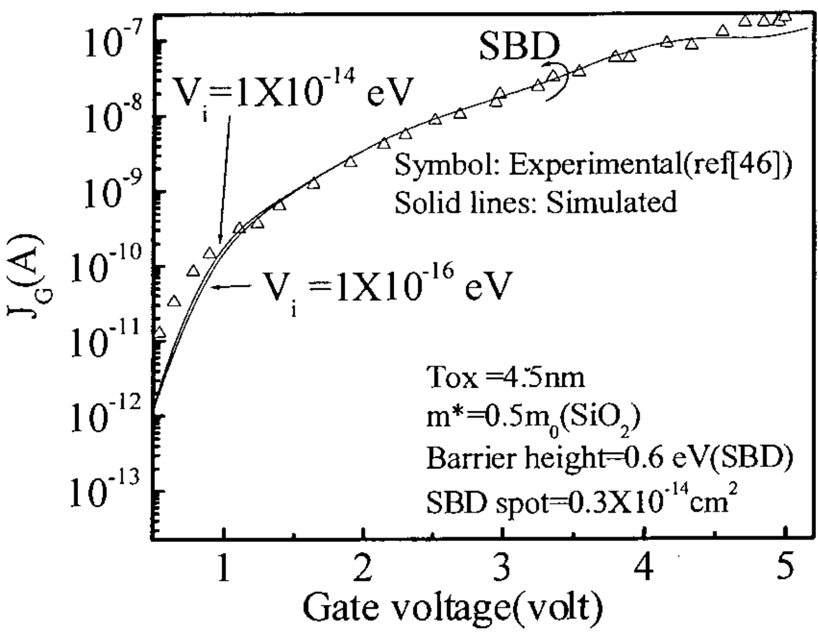



Fig.4.4. Current density as a function of applied voltage- imaginary potential inside $SiO_2$ as a parameter after soft breakdown occur.

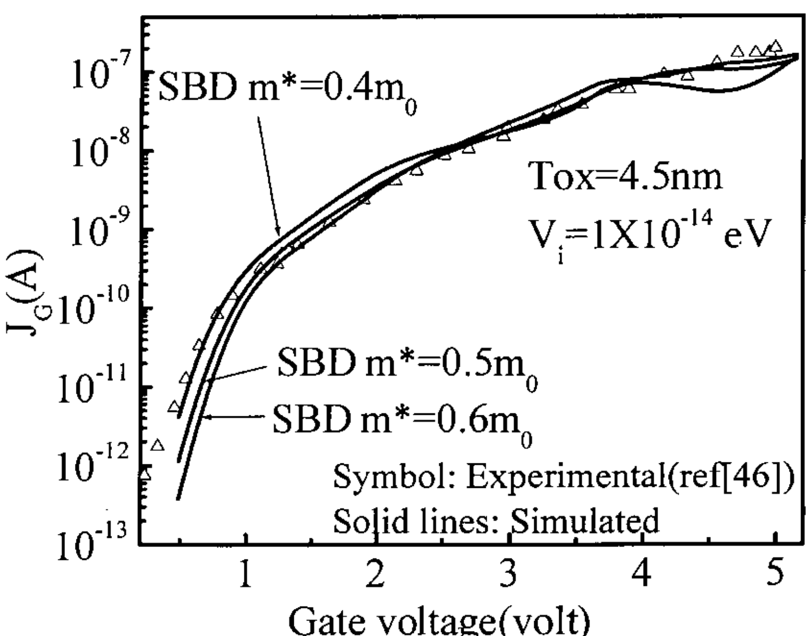



Fig. 4.5: Simulated SBD Current density- variation with the electron effective mass of the SBD spot. The oxide area is 20μm×5μm and the SBD barrier height here is 0.6 eV.

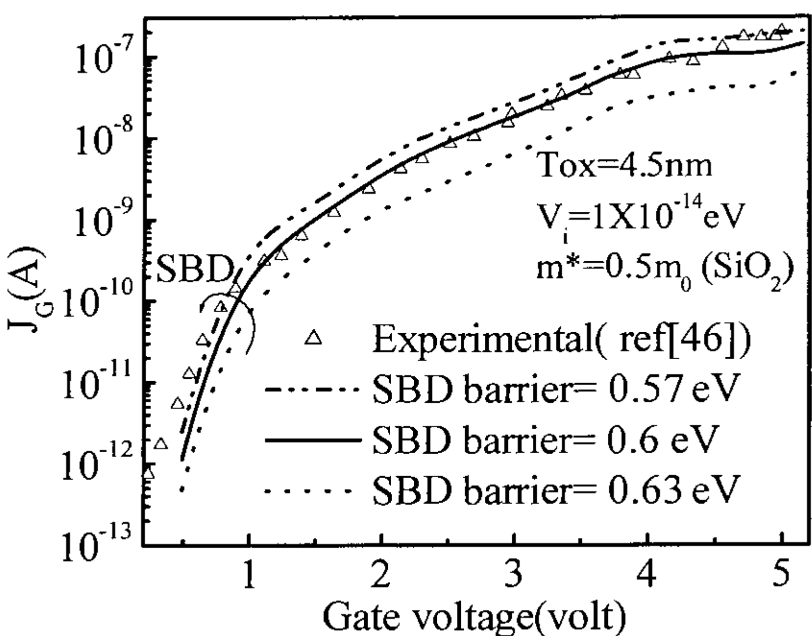



Fig. 4.6: Simulated SBD Current density- variation with the effective barrier height of the SBD spot. The oxide area is 20μm×5μm. Effective mass of the electron is same throughout the specimen. SBD area was taken to be $0.3\times10^{-14}$ $cm^2$ for simulation.

Lowering the barrier introduces a huge current in the low voltage region which closely matches the experimental data [46]. Current density with various SBD barrier heights was observed (Fig. 4.6). The SBD barrier height was measured from the conduction edge of Si at the $Si/SiO_2$ interface. Potential barriers with lower height achieve FN tunneling at lower applied voltage (Fig. 4.6). With the decrease in SBD barrier height, an increase in the current level is observable.

Moreover, these shapes exhibit oscillations that are due to the FN tunneling current. At higher voltage (>4V) the FN current of the fresh oxide suppresses the SBD current. Here, the SBD path is assumed to be $0.3\times10^{-14}$ $cm^2$ [46]. Below 0.55eV and above 0.65 eV from the conduction edge of Si at the $Si/SiO_2$ interface, the soft break current characteristic of our simulated result does not match with the experimental result [46]. However, we also simulated the SBD current density with the variation of SBD area. Increasing the SBD area the SBD current density at the given applied voltage increases considering the SBD barrier height is 0.6 eV and the effective mass of the electron is same through al the oxide area.

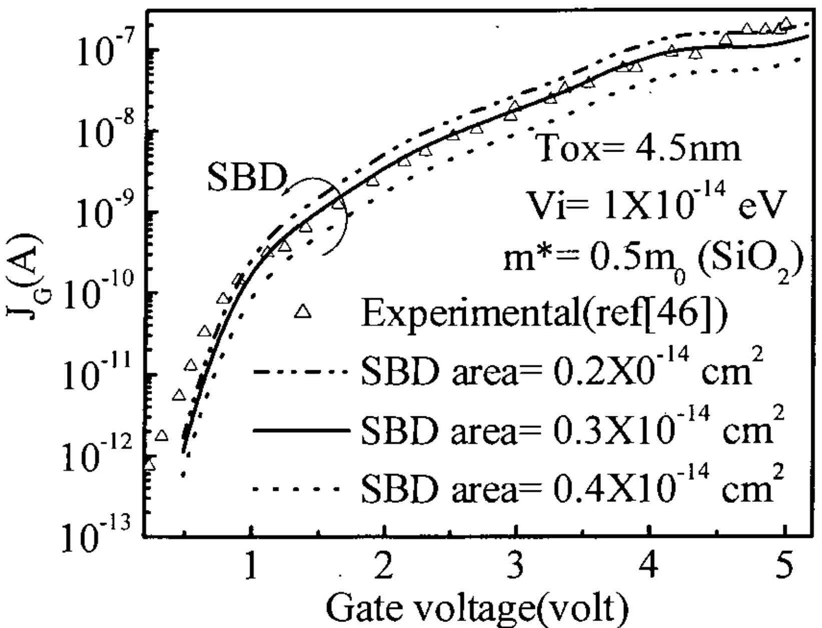



Fig. 4.7. Simulated SBD Current density- variation with area of the SBD spot. The oxide area is 20μm×5μm and the SBD barrier height here is 0.6 eV.

Fig. 4.7 shows that the current density through a Soft breakdown oxide with the variation of SBD spot area for the SBD barrier height (0.6 eV). SBD barrier height with 0.6 eV and the spot area $0.3\times10^{-14}$ cm$^2$ gives the best result so far.

Though the SBD current exhibits close match when the SBD spot barrier height is 0.6 eV and the SBD area is $0.3\times10^{-14}$ cm$^2$, there is obvious discrepancy in the lower voltage region and in the higher voltage region before the FN current suppresses the SBD current. The discrepancy in the lower voltage region may have occurred because we did not consider the charges those trap in the $SiO_2$ defect states can detrap to the gate electrode. Also surface potential charge has some effect in the low applied gate voltage range.

### 4.3.3 PARAMETER EXTRACTION USING LEAST SQUARE ERROR TECHNIQUE

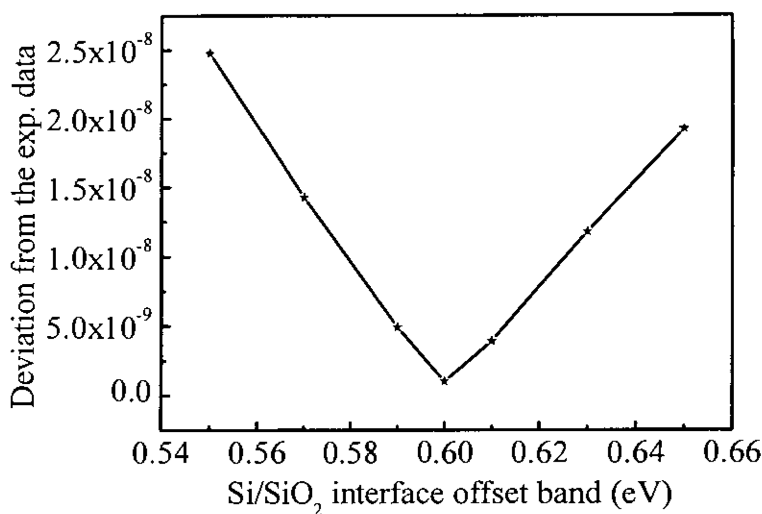



Fig. 4.8. Deviation from the experimental data to the Simulated SBD Current data versus variation with the effective barrier height of the SBD spot. The oxide area is 20μm×5μm. Effective mass of the electron is same throughout the specimen.

In Fig. 4.8 we take the simulated data of the four different SBD current for the four different gate voltage (0.67 V, 1.86V, 3.42V and 4.6V). To match the simulated data with the experimental data, we change both barrier height of the SBD spot area and the SBD spot area. Using the least square technique we find the minimum error when the SBD barrier height is 0.6eV and the spot area is $0.3\times10^{-14}$ $cm^2$. Effective mass of the electron ($m^*=0.5m_0$) is taken same throughout the specimen.

In Fig. 4.9 we again take the simulated data of the four different SBD current for the four different gate voltage (0.67 V, 1.86V, 3.42V and 4.6V). To match the simulated data with the experimental data, we change the effective mass of the electron in $SiO_2$ considering fixed barrier height of the SBD area (0.6 eV) and the spot area ($0.3\times10^{-14}$ $cm^2$). Using the least square technique of equation 3.1 we find the minimum error when the effective mass of the electron is $0.5m_0$.

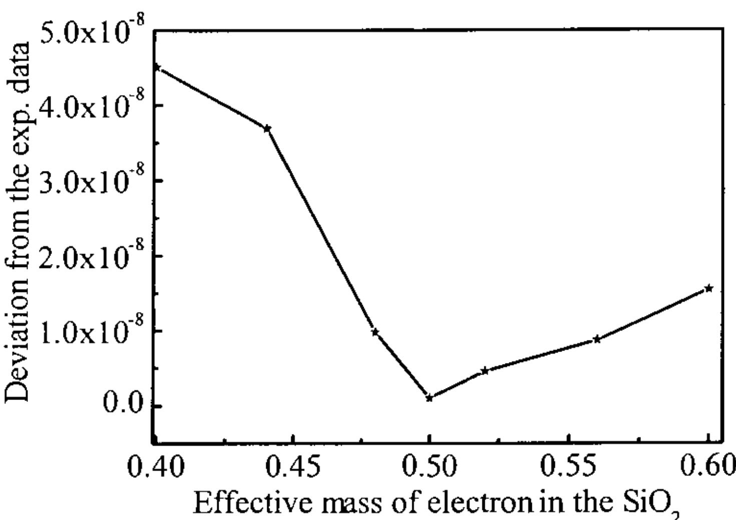



Fig. 4.9: Deviation from the experimental data to the Simulated SBD Current data versus variation with the effective mass of the electron in the SBD spot. The oxide area is 20μm×5μm. The barrier height of the SBD area is 0.6 eV and the spot area is $0.3\times10^{-14}$ $cm^2$.

In the process of simulating the SBD current we assumed that the remaining oxide other than the SBD spot is unaffected, however in reality the remaining oxide should have certain amount of degradation [25]. The degraded oxide will contribute oxide leakage current but this current is negligible compared to that of the SBD current for 4.5 nm oxides in the low voltage regime. However, in the higher voltage regime, the current is significant enough to cause an increasing I-V characteristic. This may be the reason why there is a discrepancy in the higher voltage region between 4.2V and 5V. In Fig. 4.10, SBD current density for the oxide specimen is simulated. However, the SBD current is also dependent on the current stresses applied to create SBD.

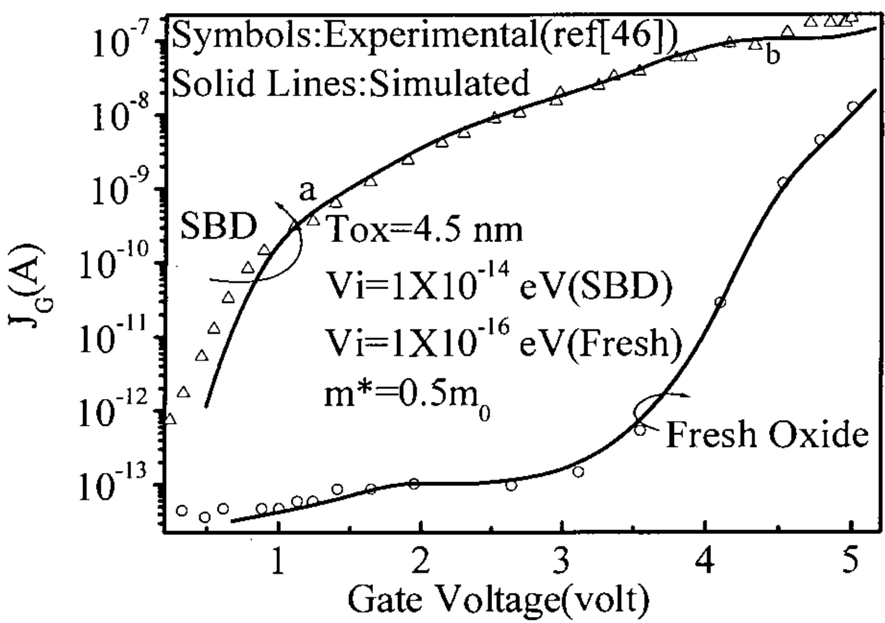



Fig. 4.10. Simulated SBD Current density for the oxide specimen. The SBD barrier height here is 0.6 eV.

In Fig. 4.10 we simulate fresh oxide current and SBD current for 20μm×5μm specimen considering the barrier height 0.6 eV, $m^*=0.5m_0$ and the surface potential, $V_i = 1\times10^{-14}$ eV. We can divide the experimental SBD current into three distinct regimes. Up to the point 'a' ($V_G$ <1.3 V) the current exhibits a sharp rise. This is because, in this regime the tunneling electrons through the SBD spot starts to intrude into the lowered conduction band on their way towards the gate. The slope of this conduction increases if the oxide area is decreases for the same electrical stress [11].Increasing the gate voltage the barrier of the $SiO_2$ becomes tilted and the electrons start FN tunneling. Upto point 'a' the triangular barrier sharpness increases rapidly. So the FN tunneling current increases fast.

The second regime can be termed as the SBD current plateau, because the SBD current has little variation but has gradually increasing characteristic. This plateau regime starts from point 'a' to point 'b' ($V_G$<4.5 V).

The third region starts from the point b. here our simulated result is little bit lower than the experimental result. At high voltage the oxide may degraded which we don't considered in our solver.

### 4.3.4 EXTRACTED PARAMETERS FOR NMOS STRUCTURE

Imaginary potential, $V_i = 1X10^{-16}$ eV (Fresh oxide)

SBD barrier in $SiO_2$, $E_{ox} = 0.6$ eV (SBD)

Effective mass of electrons in $SiO_2$,$m^* = 0.5m_0$ (SBD)

Imaginary potential in SBD $SiO_2$, $V_i = 1X10^{-14}$ eV (SBD)

SBD spot area in $SiO_2 = 0.3\times10^{-14}$ $cm^2$

## 4.4 PARAMETERS FOR PMOS WITH HIGH-k STACK GATE DIELECTRIC STRUCTURE

Oxide thickness, Tox =1.6nm $SiO_2$+3nm HfAlOx

Oxide area = $100\mu m\times100\mu m$

Dielectric constant of $SiO_2$, $\varepsilon$ =3.9

Dielectric constant of HfAlOx, $\varepsilon_{high-k}$ =14

$SiO_2$ barrier height, $E_{ox}$=4.5 eV (Hole)

HfAlOx barrier height, $E_{high-k}$=3.65 eV (Hole)

Effective mass of holes in $SiO_2$,$m^* = 0.3m_0$ (Considered for both Fresh oxide and SBD)

Effective mass of holes in HfAlOx, $m^* = 0.12m_0$ (Considered for both Fresh oxide and SBD)

## 4.5 POTENTIAL PROFILE OF PMOS HfAlOx/$SiO_2$ GATE STACK STRUCTURE

The simulations are performed for a n+ gate p-channel metal-insulator-semiconductor field-effect-transistors with HfAlOx/$SiO_2$ dielectric layers (100) with $N_D=5\times10^{17}$ $cm^{-3}$. The gate is made of poly Silicon with n-type doping. The effective mass of holes in Si is taken as $m^* = 0.433m_0$ as done by early researchers [78]. Fig. 4.11 shows the band diagram of n+ p-MISFETs for 2.21 V applied gate voltage.

The height from the valance band edge of Si to that of $SiO_2$ is considered to be 4.5 eV [59] for hole and HfAlOx is considered to be 3.65eV [59]. In this work the effective mass of hole inside $SiO_2$ is taken as $0.3m_0$ and the effective mass of hole

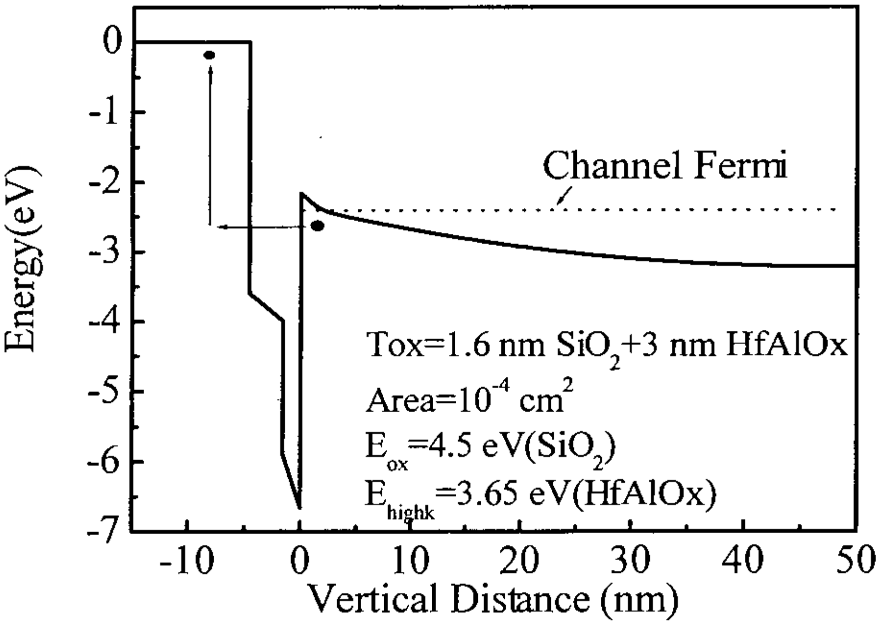



Fig.4.11. The simulated profile of an energy band diagram of a p n+ gate p-channel metal-insulator-semiconductor field-effect-transistors with HfAlOx/$SiO_2$ dielectric layers (100). Here substrate doping density, $N_D=5\times10^{17}$ $cm^{-3}$

inside HfAlOx is taken as $0.12m_0$ [78].Taking the $SiO_2$ thickness 1.6 nm and the physical thickness of the HfAlOx is 3nm as stated in ref [45].

### 4.5.1 SIMULATED FRESH OXIDE CURRENT DENSITY FOR PMOS STACK

The effective mass of the hole and the imaginary potential has significant effect on the gate tunneling current. In Fig. 4.12 we vary the imaginary potential from $10^{-16}$ eV to $10^{-13}$ eV. In the low bias region increasing the $V_i$ in the HfAlOx, the tunneling current increases considering $m^*(SiO_2) = 0.3m_0$ and $m^*(HfAOx) = 0.1m_0$. In Fig. 4.13 increasing the effective mass of hole in HfAlOx ($m^*$) from $0.08m_0$ to $0.12m_0$ considering the effective mass of hole in $SiO_2$ fixed ($m^*(SiO_2) = 0.3m_0$) and also the imaginary potential, $Vi=10^{-16}$ eV in the whole gate oxide. We observe that increasing $m^*$ the tunneling gate current with the same applied voltage decreases.

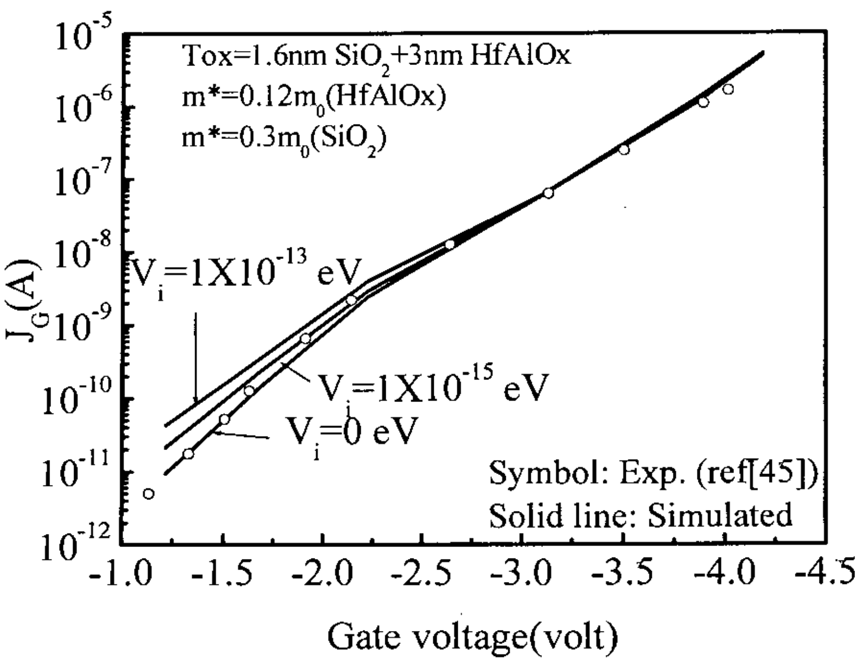



Fig. 4.12: Current density as a function of applied voltage- imaginary potential inside HfAlOx as a parameter.

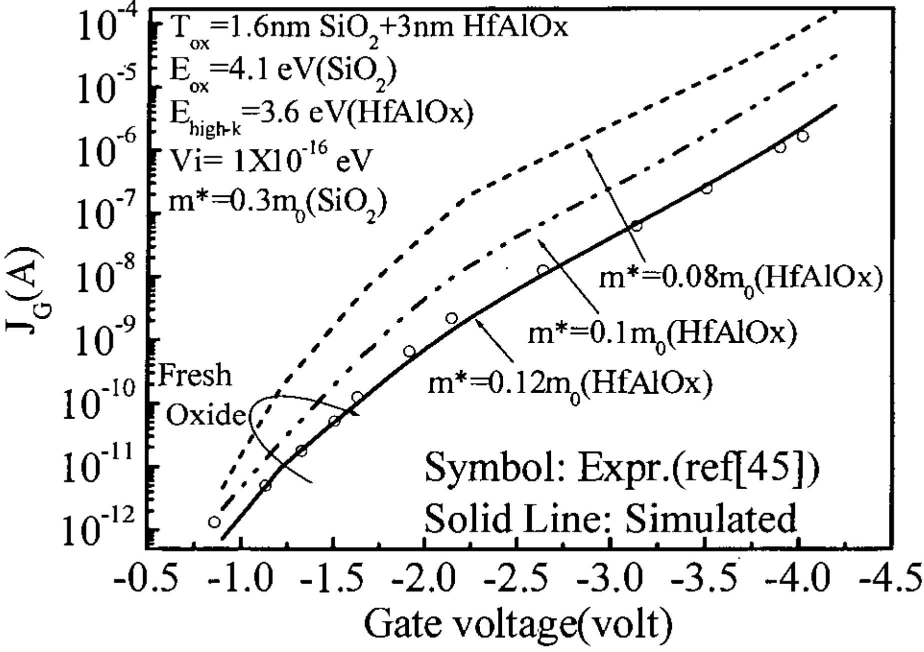



Fig.4.13 simulated current density versus applied voltage curves for fresh oxide. Fitting the experimental data ref [45 ] by varying m* inside HfAlOx as a parameter.

### 4.5.2 SIMULATED SBD CURRENT DENSITY FOR PMOS STACK

In Fig. 4.14 we match the SBD current with the experimental current. We take $V_i = 1X10^{-14}$ eV in the SBD spot area to mach the simulated curve with the experimental curve in the low bias region considering $m^*(SiO_2) = 0.3m_0$ and $m^*(HfAlOx) = 0.12m_0$ for hole. If we select above the imaginary potential we get below 1.5V the curve match very fine but above that voltage current becomes high.

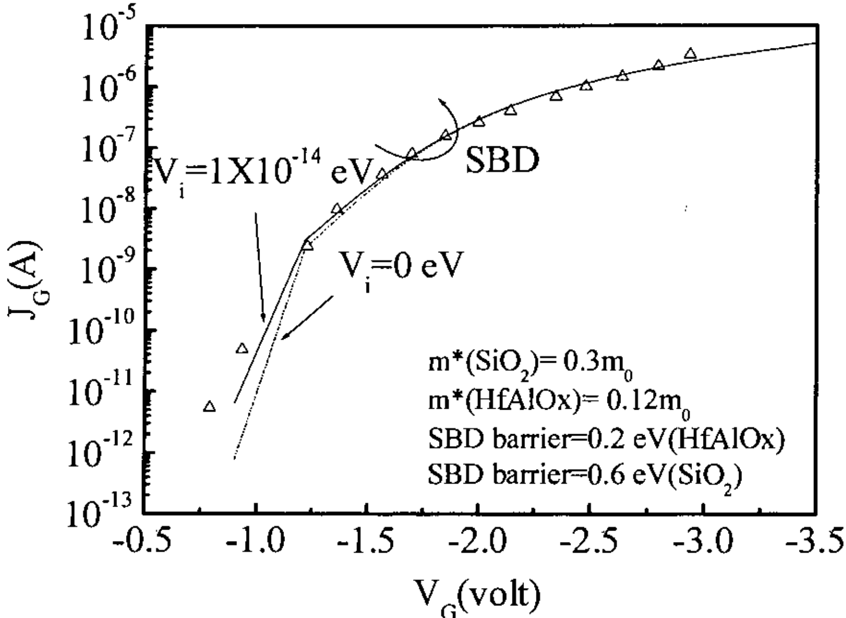



Fig. 4.14: Simulated SBD Current density- variation with the effective imaginary potential of the SBD spot. The oxide area is 100μm×100μm. Effective mass of the hole is same throughout the specimen.

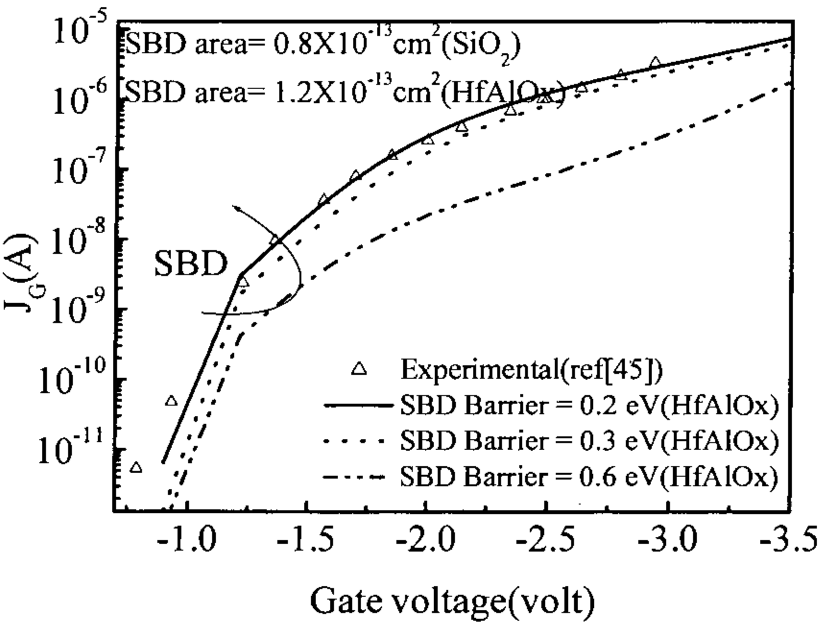



Fig. 4.15: Simulated SBD Current density- variation with the effective barrier height of the HfAlOx of the SBD spot. The oxide area is 100μm×100μm. Effective mass of the hole is same throughout the specimen. SBD area was taken to be $0.8\times10^{-13}$ cm$^2$ in the $SiO_2$ and $1.12\times10^{-13}$ cm$^2$ in the HfAlOx for simulation.

Lowering the barrier introduces a huge current in the low voltage region which closely matches the experimental data [45]. Current density with various SBD barrier heights was observed (Fig. 4.15). The SBD barrier height was measured from the conduction edge of Si at the Si/$SiO_2$ interface. Potential barriers with lower height achieve FN tunneling at lower applied voltage (Fig. 4.15). With the decrease in SBD barrier height, an increase in the current level is observable. To match the SBD current with the simulated current we vary the SBD barrier height in the HfAlOx area is varied from 0.2 eV to 0.9 eV considering the barrier height of $SiO_2$ is 0.6 eV, effective mass $m^*(SiO_2) = 0.3m_0$ and $m^*(HfAlOx)=0.1m_0$ and $V_i=1X10^{-14}$eV in the SBD area and $V_i=1X10^{-16}$ eV in the fresh oxide and SBD area was taken to be $0.8\times10^{-13}$ cm$^2$ in $SiO_2$ and $1.12\times10^{-13}$ cm$^2$ in HfAlOx.

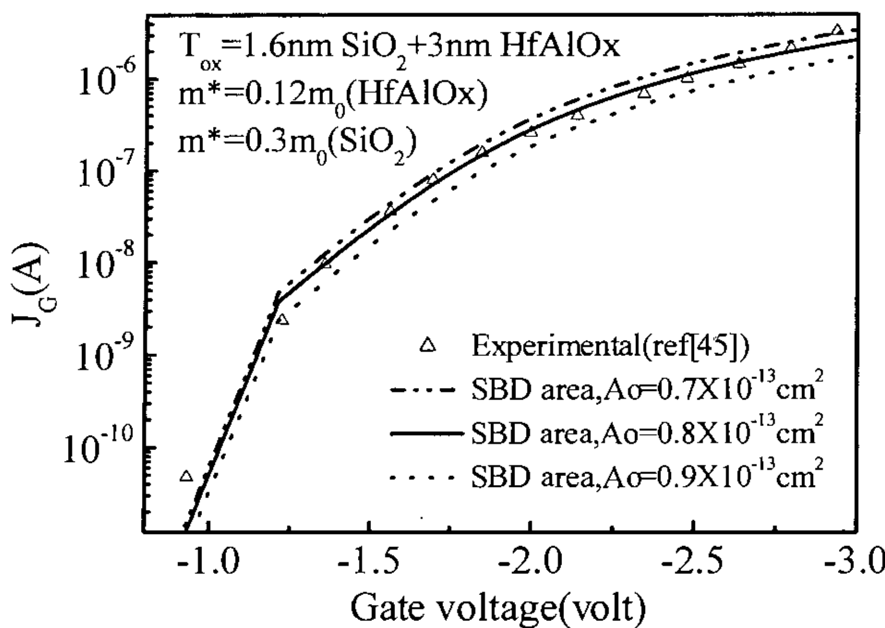



Fig. 4.16: Simulated SBD Current density- variation with area of the SBD spot. The oxide area is 100μm×100μm and the SBD barrier height here is 0.2 eV (HfAlOx) and 0.6 eV ($SiO_2$).

In Fig. 4.16 shows the current density through a Soft breakdown oxide with the variation of SBD spot area considering the SBD barrier height 0.2 eV in HfAlOx, 0.6 eV in $SiO_2$, mass $m^*(SiO_2) = 0.3m_0$, $m^*(HfAlOx)=0.12m_0$, $V_i = 1X10^{-14}$eV in the SBD area and $V_i = 1X10^{-16}$ eV in the fresh oxide. The ratio of the SBD HfAlOx spot and the $SiO_2$ spot is taken 1.5.

### 4.5.3 PARAMETER EXTRACTION USING LEAST SQUARE ERROR TECHNIQUE

To best fit the simulated SBD current curve with the experimental SBD current curve we use equation 3.6.

In Fig. 4.17 we take three different gate voltage (-1.2V, -1.67V and -2.23V) of our simulated data to match with the experimental data changing both barrier height of the SBD spot area and the SBD spot area. We find the minimum error when the SBD barrier height is 0.2eV for HfAlOx and 0.6 eV for $SiO_2$ SBD area was taken to be $0.8\times10^{-13}$ $cm^2$ in $SiO_2$ and $1.12\times10^{-13}$ $cm^2$ in HfAlOx. Effective mass of the hole ($m^*(SiO_2) = 0.3m_0$ and $m^*(HfAlOx) = 0.1m_0$) is same throughout the specimen.

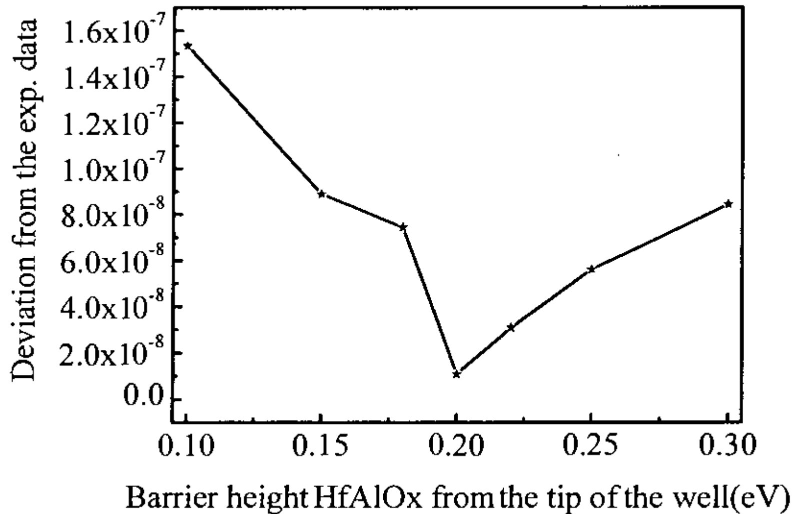



Fig. 4.17 Deviation from the experimental data to the Simulated SBD Current data versus variation with the effective barrier height of HfAlOx of the SBD spot. The oxide area is 100μm×100μm. Effective mass of the hole is same throughout the specimen.

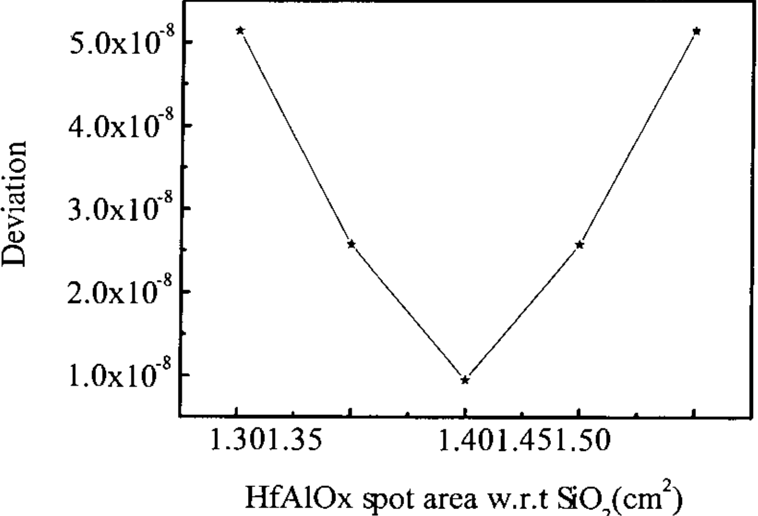



Fig. 4.18. Deviation from the experimental data to the Simulated SBD Current data versus variation with the ratio of the SBD area of HfAlOx and the SBD area of $SiO_2$ area. The oxide area is 100μm×100μm.

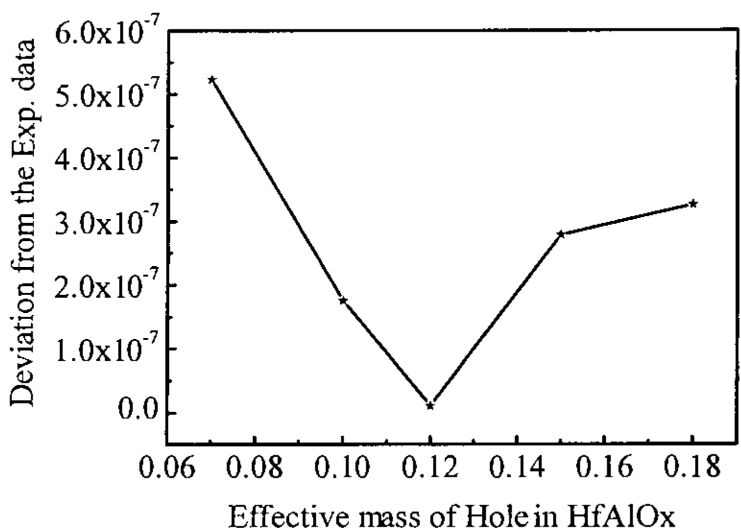



Fig. 4.19. Deviation from the experimental data to the Simulated SBD Current data versus variation with the effective mass of the hole in the SBD spot of HfAlOx.

In Fig. 4.18 again we take three different gate voltage (-1.2V, -1.67V and -2.23V) of our simulated data to match with the experimental data changing the ratio of the SBD spot of HfAlOx and the SBD spot of $SiO_2$ (1.3 ~1.5) considering fixed barrier height both the HfAlOx (0.2eV) and $SiO_2$ (0.6 eV) of the SBD area and the spot areas are $0.8\times10^{-13}$ $cm^2$ for $SiO_2$ and $1.12\times10^{-13}$ $cm^2$ for HfAlOx . Using the least square technique of equation 3.10 we find the minimum error when the ratio is 1.4. The effective mass of hole in the HfAlOx is varied to find out the best fitted curve in Fig. 4.19 considering other parameters same. In Fig. 4.20 we presented our simulated result of SBD current and fresh oxide current for stack gate PMOS device experimental result. And find out the SBD barrier height, Spot area and the imaginary potential of the specimen.

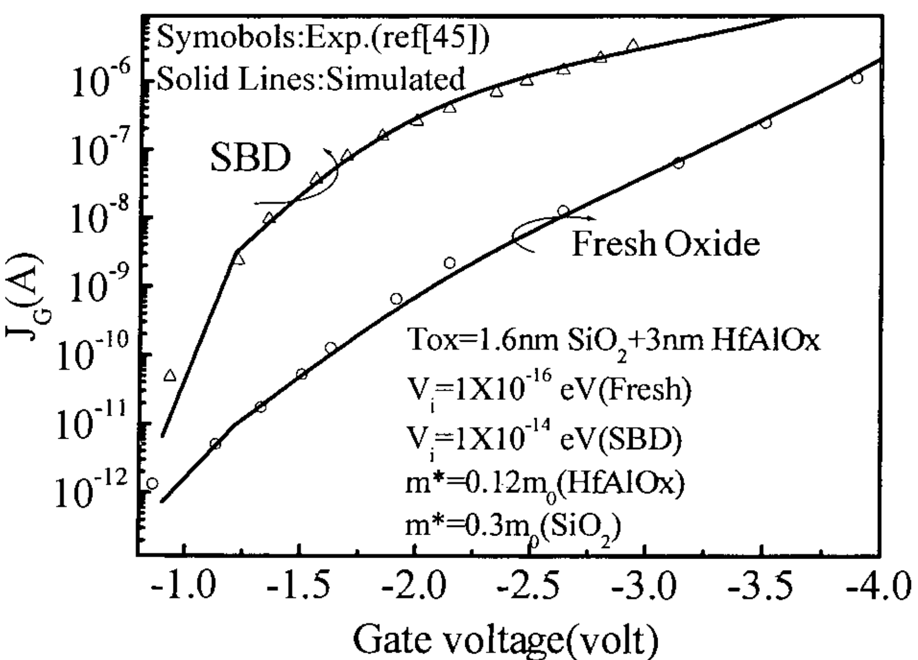



Fig. 4.20. Simulated SBD Current density for the oxide specimen. The SBD barrier height of HfAlOx (0.2eV) and $SiO_2$ (0.6 eV) of the SBD area and the spot areas are $0.8\times10^{-13}$ $cm^2$ for $SiO_2$ and $1.12\times10^{-13}$ $cm^2$ for HfAlOx .

### 4.4.3 EXTRACTED PARAMETERS FOR PMOS WITH HIGH-k STACK GATE DIELECTRIC STRUCTURE

Imaginary potential, $V_i = 1X10^{-16}$ eV (Fresh oxide)

SBD barrier in $SiO_2$, Eox= 0.6 eV (Hole) (SBD)

SBD barrier in HfAlOx, $E_{high\text{-}k}$ = 0.2 eV (Hole) (SBD)

Imaginary potential in SBD, $V_i = 1X10^{-14}$ eV

SBD spot area in $SiO_2 = 0.8\times10^{-13}$ $cm^2$ (Hole)

SBD spot area in HfAlOx = $1.12\times10^{-13}$ $cm^2$ (Hole)

## 4.6 CONCLUSION

Here we assume the barrier height lowering approach at the soft breakdown area to calculate the gate current ($J_G$) for both NMOS structure and PMOS with HfAlOx/$SiO_2$ stack gate simultaneously. Figs. 4.4 and 4.5 reveal that the influence of imaginary potential ($V_i$) is insignificant in all calculation. Hence can be neglected. For NMOS the SBD spot area is $0.3\times10^{-14}$ cm$^2$ and SBD barrier height is 0.6 eV that can be mentioned as the residual voltage at the SBD area. We also find out that the SBD area of HfAlOx is 1.4 times larger then the SBD area of the $SiO_2$ for the hole which satisfies ref [45]. The SBD spot area of the $SiO_2$ is $0.8\times10^{-13}$ cm$^2$ and the SBD spot area of the HfAlOx is $1.12\times10^{-13}$ cm$^2$. The SBD barrier of HfAlOx is smaller than the SBD barrier of $SiO_2$.

# CHAPTER 5

# CONCLUSION

## 5.1 SUMMARY

In this work, post soft breakdown gate current is modeled using a quantum mechanical approach. This gate current was developed using the Tsu-Esaki expression, whereas the transmission co-efficient of electrons through arbitrary potential barriers was determined using generalized wave impedance method.

The main objective of this study was to extract the properties of a Soft Breakdown spot of a degraded oxide specimen. It has been shown that the effective barrier height for a SBD spot becomes lowered significantly in comparison to the remaining oxide. The simulations show good agreement with reported experimental data [46]. The simulations were performed for an oxide thickness of 4.5 nm in the gate voltage range of 0-5 V.

It has been reported that the oxide traps are located 0-3 eV below the conduction band edge of the oxide [71]. As the SBD spot is created due to percolation path connection between adjacent traps, we propose that the SBD path should have a lowered barrier. In such case, as the SBD current is several orders lower than that of the Hard Breakdown, we assume that the barrier height inside the SBD spot is not totally eliminated. We proposed that the barrier height is 0.6 eV from the tip of the Si/$SiO_2$ interface (conduction band edge. The area of the SBD spot is taken to be $0.3\times10^{-14}cm^2$. A good agreement between the simulated results and reported experimental data was achieved.

We also extract the properties of a soft breakdown spot in the ultra thin high-k gate stack oxide. The defect size in the HfAlOx is 1.4 times larger than the defect size in the $SiO_2$. We proposed that the SBD barrier height is 0.2 eV for HfAlOx and 0.6eV for $SiO_2$ for hole from the tip of the Si/$SiO_2$ interface (conduction band edge). The effective mass of the SBD spot is assumed unaffected. The area of the SBD spot is taken to be $0.8\times10^{-13}cm^2$ in the $SiO_2$ and $1.12\times10^{-13}cm^2$ in the HfAlOx. A good agreement between the simulated results and reported experimental data was achieved.

## 5.2 SUGGESTION FOR FUTURE WORK

SBD spot is considered a lower barrier potential profile and the remaining oxide is considered unaffected. The degradation can be considered for the remaining oxide using the trap distribution throughout the oxide. Also the dependency of the degradation on the applied electrical stress can be considered for better results. An oxide specimen that has undergone SBD may have further degradation while going through the experiments of I-V characteristic. So, the degradation of the SBD spot also can be made dependent on the applied electrical stress.

Lateral carrier (charge) confinement in the SBD path was neglected in this work. However, incorporating lateral confinement, the physics behind the conduction mechanism can be described more accurately.

Our study is totally devoid of any time dependent property changes. The time dependent current fluctuations and the conductions are not considered here. A quantum mechanical model can also be formulated for a time dependent SBD damage.

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