Analytical Modeling of the Pocket Implanted Nano Scale n-MOSFET

by

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DOCTOR OF PHILOSOPHY

IN ELECTRICAL AND ELECTRONIC ENGINEERING

Department of Electrical and Electronic Engineering

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY

2011

CANDIDATE'S DECLARATION

It is hereby declared that this thesis titled **"Analytical Modeling of the Pocket Implanted Nano Scale n-MOSFET"** or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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Dedication

Dedicated to

My Parents, My Wife, My Daughter and the Other Family Members

who have always inspired and supported me and also sacrificed many things for me to carry on my research work smoothly

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List of Abbreviations

Abbreviated Word	Full Meaning
AFM	Atomic Force Microscopy
APCVD	Atmospheric Pressure CVD
BPSG	Borophosphorus Silicate Glass
CLM	Channel Length Modulation
CMOS	Complimentary Metal Oxide Semiconductor Field Effect Transistor
C-V	Capacitance Voltage
CVD	Chemical Vapor Deposition
DIBL	Drain Induced Barrier Lowering
FET	Field Effect Transistor
HCI	Hot Carrier Injection
HDPCVD	High Density Plasma CVD
HFET	Heterojunction Field Effect Transistor
ICP	Inductively Coupled Plasma
IGFET	Insulated-Gate Field-Effect Transistor
ILD	Inter Layer Dielectric
ITRS	International Technology Roadmap for Semiconductors
JFET	Junction Field Effect Transistor
LATI	Large-Angle-Tilt-Implanted
LDD	Lightly Doped Drain
LPCVD	Low Pressure CVD
MESFET	Metal Semiconductor Field Effect Transistor
MIS	Metal Insulator Semiconductor
MISFET	Metal Insulator Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PECVD	Plasma Enhanced CVD
PET	Potential Effect Transistor
PSG	Phosphorus Silicate Glass
QME	Quantum Mechanical Effects
RF	Radio Frequency
RIE	Reactive Ion Etching
RSCE	Reverse Short Channel Effect
RTA	Rapid Thermal Anneal
RTP	Rapid Thermal Processor
SCE	Short Channel Effect
SCM	Scanning Capacitance Microscopy

Abbreviated Word	Full Meaning
SIMS	Secondary Ion Mass Spectroscopy
SOI	Silicon On Insulator
STM	Scanning Tunneling Microscopy
TCAD	Technology Computer Aided Design
TEOS	Tetra Ethyle Ortho Silicate
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration

List of Symbols

Symbols	Name of the Symbols
D_n	Diffusion Coefficient for Electron
E_{eff}	Effective Electric Field
E_{fn}	Electron Fermi Level
$I_{D,sat}$	Drain Saturation Current
I_{DS}	Drain Current
I_{dsub}	Subthreshold drain current
I_{sub}	Subthreshold Drain Current
J_n	Electron Current Density
L	Channel Length
L_{DH}	Debye–Huckel Value
L_p	Pocket Length
L_s	Screening Length
L_{TF}	Thomas-Fermi Value
L_{th}	Thermal Length
N_C	Effective Density Of States in the Conduction Band
$N_{ch}(x)$	Lateral Non-Uniform Channel Doping
N_{eff}	Effective Doping Concentration
n_i	Intrinsic carrier concentration of Si
N_{inv}	Number of Channel Carriers per unit Area
N_{pm}	Peak Pocket Doping Concentration
N_{sd}	Source or drain doping concentration
N_{sub}	Substrate Doping Concentration
N_V	Effective Density Of States in the Valence Band
q	Electronic Charge
Q_0	Oxide Charge per unit Area
Q_{dep}	Depletion Region Charge per unit Area
Q_{inv}	Inversion Layer Charge
Q_{it}	Interface Trap Density per unit Area
r_j	Junction Depth
S_{id}/I_d^2	Normalized Noise Power Spectrum Density
T	Absolute Temperature
t_{ch}	Channel Thickness
t_{ox}	Oxide thickness
v	Carrier Velocity
V_{BS}	Substrate Voltage
$V_{D,sat}$	Drain Saturation Voltage
V_{DS}	Drain Voltage

Symbols	Name of the Symbols
v_F	Fermi Velocity
V_{FB}	Flat Band Voltage
V_{GS}	Gate Voltage
v_{th}	Thermal Velocity
V_{th}	Threshold Voltage
$V_{th,L}$	Long Channel Threshold Voltage
V_{thp}	Threshold Voltage in the Pocket Region
W_m	Maximum Width of the Surface Depletion Region
X_D	Depletion Width
Z	Channel Width
ψ	Electrostatic Potential
ψ_B	Electrostatic Potential in the Bulk
μ_n	Electron Mobility
μ_p	Hole Mobility
ρ_s	Charge Density per unit Volume
Φm	Work Function of Metal
Φs	Work Function of Semiconductor
χ	Electron Affinity of the Semiconductor
α	Dimensional Scaling Factor
β	Electric Field Scaling Factors
ε_{ox}	Dielectric Permittivity of Oxide
ε_{Si}	Dielectric Permittivity of Si
ϕ_{th}	Thermal Voltage
γ	Attenuation Coefficient of the Electron Wave Function
γ_A	Threshold sensitivity due to back bias for effective doping concentration along the channel
γ_B	Body factor corresponding to bulk doping respectively
φ_{bi}	Built-in potential at the source or drain to channel junction
φ_F	Fermi potential due to pocket implantation
φ_{MS}	Work Function between Metal and Semiconductor
μ_{bal}	Ballistic Mobility
μ_{cb}	Coulomb Scattering Mobility
μ_{eff}	Effective Mobility
μ_{ph}	Phonon Scattering Mobility
μ_{sr}	Surface Roughness Scattering Mobility
θ	Subthreshold Ideality Factor
ψ_s	Surface Potential
$\psi_{s,inv}$	Surface Potential at the onset of Strong Inversion

Acknowledgements

In the name of the Allah, the most Beneficent, the most Merciful, the most Compassionate. It is by the grace of the Almighty Allah that I was able to complete this thesis successfully. This thesis would not have been possible without the support of many people.

The author expresses his profound gratitude and a deep sense of respect to his supervisor Dr. Quazi Deen Mohd Khosru, Professor of the Department of Electrical and Electronic Engineering (EEE), Bangladesh University of Engineering and Technology (BUET), for his erudite suggestions, helpful discussions, invaluable assistance and great encouragement in the process of completing this work. His attention to detail, quest for excellence and love for perfection has inspired me to give my best efforts in this stupendous task. He has always been keen to cross his roles as a supervisor and played the role of a very helpful mentor. I am deeply indebted to him for making this research experience a memorable and successful one. Without his wholehearted supervision, it would have been impossible to finish the work in time. Not only that he always did all the official procedures and formalities very quickly.

Then the author would like to be grateful to all the examiners of the doctoral committee of EEE Department, BUET and to the external examiner Dr. Syed Kamrul Islam, Professor of the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN, USA for their invaluable suggestions and corrections made to improve this thesis.

After that the author would like to pay his thanks and humble respects to all the Heads of various tenures during the progress of his thesis works, such as, Dr. M. M. Shahidul Hassan, Dr. Mohammad Ali Choudhury, Dr. S. Shahnawaz Ahmed, Dr. Satya Prasad Majumder, Dr. Aminul Hoque and Dr. Md. Saifur Rahman, Professors of the Department of Electrical and Electronic Engineering (EEE), Bangladesh University of Engineering and Technology (BUET) for their help, support and co-operation.

The author would like to convey his thanks and gratefulness to the Committee of Advanced Studies and Research (CASR) of BUET for the financial support in this research work.

The author would also like to express his thanks and respects to all the members of the Board of Post Graduate Studies (BPGS) for their unanimous decisions for which this research has come into reality.

The author then extends his thanks to the Departmental and Central Library staffs who helped to collect various journal and conference papers as well as various undergraduate and postgraduate thesis from the Library.

Sincerest thanks are also due to my friend Dr. Mohammed Imamul Hassan Bhuiyan, Associate Professor and my M.Sc. Engg. supervisor Dr. Kazi Mujibur Rahman, Professor, Department of EEE, BUET for their encouragement, suggestions and co-operation, and also for helping me to work with LaTeX during this thesis work. Dr. Bhuiyan also supplied me numerous research articles while he was doing his PhD in Canada. My special thanks go to Dr. Md. Ziaur Rahman Khan, Associate Professor, Department of EEE, BUET for giving me his PhD thesis (degree obtained from Cambridge University, UK) to get few important articles and references. I would also like to thank Dr. Mohammad Arfiul Haque, Assistant Professor, Department of EEE, BUET (who did his PhD from Department of EEE, BUET) for supplying me the LaTeX templates and few official documents regarding PhD degree. It gives me much pleasure to express my deep feeling of gratitude to all my respected teachers who always encouraged me to complete this task. I would also like to thank all the staffs in EEE Department and other departments/sections of BUET for extending their helping hands and co-operation.

I would also like to pay attention to numerous BUETians in the e-mail group to express my gratefulness and respect for their contribution towards my research works by supplying promptly a large number of research articles of various journals and conferences upon my e-mail request and also helping me by providing the LaTeX manuals and documents.

Finally, the author expresses his heartfelt appreciation and cordial thanks to his parents, wife, daughter and other family members, friends as well as well-wishers for their inspiration, sacrifice and extension of their co-operative hands during the progress of this work.

ABSTRACT

As MOSFET device dimensions are shrinking to get optimum device performance, device structure is being modified. Additional atoms have been doped laterally by ion implantation at the source and drain sides. These additional doping atoms are known as pocket atoms that cause threshold voltage to rise when the gate length is reduced. This effect is known as reverse short channel effect or RSCE. This thesis presents the analytical models of the pocket implanted n-MOSFET. Two linear equations are used to simulate the pocket profiles along the channel at the surface from the source and drain edges towards the center of the n-MOSFET. Then the effective doping concentration is derived by integrating the pocket profiles from source to drain side and is used in the Poisson's equation in the depletion region at the surface. From this Poisson's equation, an analytical surface potential model of the pocket implanted n-MOSFET is derived using the appropriate boundary conditions. This model is used to find the threshold voltage model incorporating the bias and temperature effects. Then the inversion layer effective mobility model is also derived based on linear pocket profiles. These models are used to derive the subthreshold drain current model of the same device. Finally, low frequency drain current flicker noise model for the pocket implanted nano scale n-MOSFET has been derived using the proposed threshold voltage model.

After the model development, surface potential, threshold voltage, inversion layer effective mobility, subthreshold drain current and low frequency drain current flicker noise models are simulated by developing various MATLAB programs for different device and pocket profile parameters as well as various bias conditions. The simulated results of the proposed models are compared with the two other pocket profile models found in the literatures. The comparison shows that the models obtained using the linear pocket doping profile also produce similar results without hampering the accuracy level. Besides, the threshold voltages for various gate lengths fit well with the experimental data already published in the literatures. Not only that subthreshold drain current as well as low frequency drain current flicker noise models also fit well with the experimental data published in the literatures for the similar device and pocket profile parameters as well as bias conditions. In fact, these models possess a simple compact form that can be utilized to study and characterize the pocket implanted n-MOSFET in the nano scale regime.

Chapter 1

Introduction

1.1 Introduction

The MOS transistor, also known as the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) or Insulated-Gate Field Effect Transistor (IGFET) is by far the most common field-effect transistor in both digital and analog circuits' applications [1]. The MOSFET is the basic building block of the computer industry, digital telecommunication systems, pocket calculators and digital wristwatches [2]. The MOSFET is also used in applications like switched capacitor circuits, analog-to digital converters and filters.

This thesis is focused on investigating a pocket implanted n-MOSFET structure and developing different types of analytical models by proposing a pocket profile model. Method of pocket profile characterization is also presented. MATLAB programs and function files are developed for simulations of the models.

In this chapter, historical perspective of Complimentary Metal Oxide Semiconductor Field Effect Transistor (CMOS) technology evolution will be described. Then extensive literatures will be reviewed for these parameters. Objectives and methodology of this work will also be discussed. Finally, this chapter ends with summarizing the organization of this thesis.

1.2 Moore’s Law

In 1965, Gordon Moore, co-founder of Intel Corporation, predicted that the computer industry would double the density of components every year [3]. He speculated that this trend would continue and the chip density of 50 components per circuit in 1965

might reach 65,000 components per circuit by 1975. This speculation became known as Moore's Law and has served as the operational standard for the semiconductor industry. Other attributes of digital electronic devices like processing speed, memory capacity, even the number and size of pixels in digital cameras are linked to Moore's law as they are also improving at (roughly) exponential rates. Although originally calculated as doubling every year, Moore later refined the period to two years [4], [5]. Fig. 1.1 illustrates Moore's Law and current trends [5]. The semiconductor industry follows Moore's law by shrinking transistor dimensions. CMOS technology has been proven as one of the most important achievements in modern engineering history and has become the primary engine driving the world economy. The secret to the success is simply to keep delivering more functionality with fewer resources and device scaling, and thus to follow the Moore's Law. But transistors cannot be scaled-down infinitely. There is couple of issues that needs to be addressed when the transistor size is reduced.

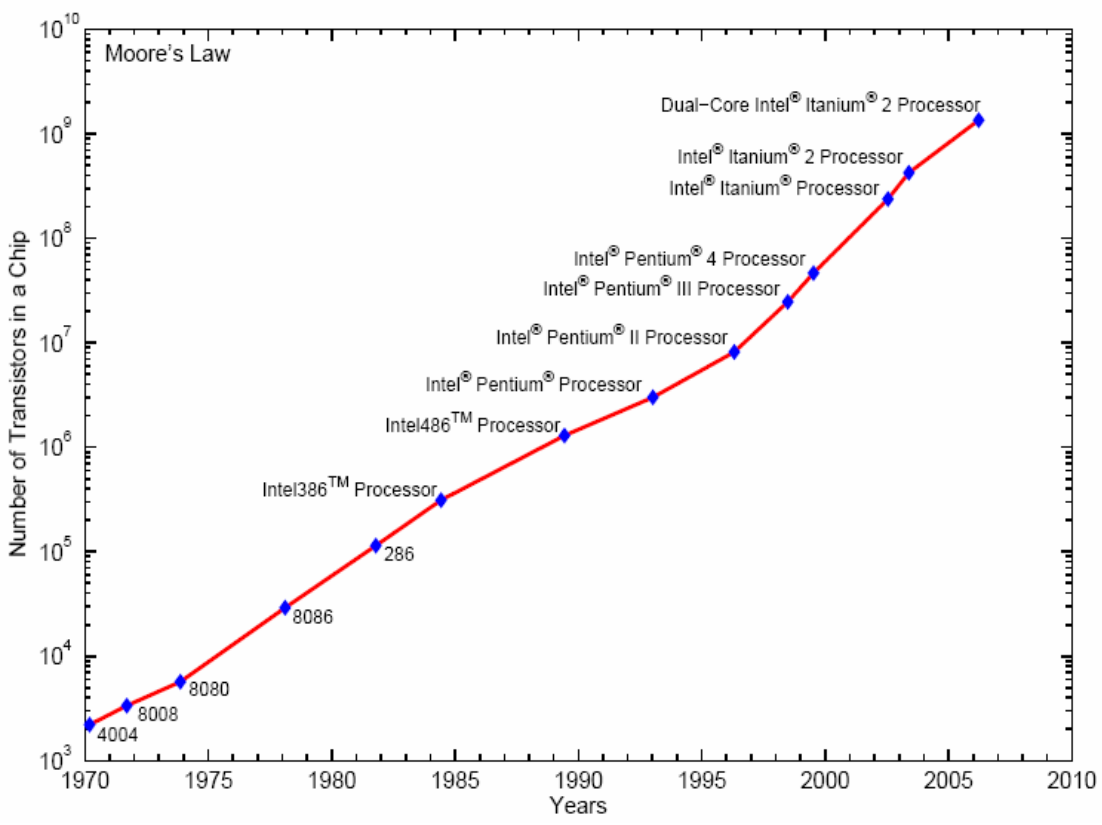

Figure 1.1: Moore's Law [5]

For digital applications, a transistor is operated as a switch. For high speed operation, it must deliver a large on-current that rapidly charges and discharges the stray capacitance of the wires connecting it to the other transistors in the circuit. In the circuit, the switching power is directly proportional to the operating frequency and to the square of the supply voltage. However, device scaling increases the number of gates on a chip and their operating frequency. Thus, in order to limit power dissipation and prevent the chip from overheating, the power supply voltage must therefore decrease when scaling the device down while maintaining the on-current. A transistor should have a very little off-current to reduce the static power loss. Because of scaling the device size, the distance between the source and drain shrinks, and it becomes increasingly difficult to turn a MOSFET off. Consequently, off-current increases exponentially with device scaling such that the off state power consumption become substantial [6].

In an interview with Techworld, Gordon Moore told that that the law cannot be sustained indefinitely. According to him "*It can't continue forever. The nature of exponentials is that you push them out and eventually disaster happens*" [7]

One of the limits to Moore's law is often believed to be in lithography and in the availability to pattern the minimum feature size. But materials are now also an important constraint. Cu has replaced Al as the interconnect material between the transistors because of current densities. In order to reduce the RC time delays of the ICs, lower dielectric constant materials, such as, SiO_2F_x or SiOCH alloys are used instead of the SiO_2 as the inter layer dielectric [8]. The excellent material and electrical properties of SiO_2 used as the gate dielectric is one of the key elements that allowed the successful scaling of silicon based MOSFETs. Amorphous SiO_2 can be thermally grown on silicon with excellent control in thickness and uniformity. It naturally forms a very stable interface with the silicon substrate with a low density of intrinsic interface defects. SiO_2 has an excellent thermal and chemical stability, which is required for the fabrication of transistors that includes annealing steps at high temperatures (up to 1000^0 C). Furthermore, the band gap of SiO_2 (9 eV) is large enough for excellent electrical isolation. It has large energy band offsets with the conduction and valence bands of Si and high breakdown fields, of the order of 13 MV/cm [9].

Table 1.1 Road map of MOSFET minimum feature size 2010 update [5]

Year	1999	2001	2002	2004	2006	2009	2010	2011	2014
L (nm)	180	130	90	65	45	38	32	22	20
t_{ox} (nm)	~4	~3	~2	~1.5	~1.5	~1.5	~1.1	~1.0	-
					with High-k/Metal gate				

All these superior properties allowed the fabrication of commercial devices with SiO_2 gate layers as thin as 2 nm [10]. Studies indicated that bulk SiO_2 electronic structure is not achieved in a thermal oxide until the thickness reaches ~0.7 nm [11]. According to the International Technology Roadmap for Semiconductors (ITRS), the next generations of Si-based MOSFETs will require oxide thicknesses below 1 nm, both for high performance logic applications (e.g. microprocessors for personal computers and workstations) and low operating power logic applications (like wireless applications) [5]. The minimum dimension size of a single device for present day technology is in the nano scale regime. Continued success in device scaling is necessary for further development of the semiconductor industry in the years to come. A group of leading companies publishes their projections for the next decade in the most recent International Technology Roadmap for Semiconductors (ITRS 2010) [5]. The roadmap projects a device gate-length down to ~20 nm around 2014 [5] as shown in Table 1.1. This forecast promises another few years of brightness. Scaling beyond 20 nm, however, can be much more difficult and different. We are quite close to the fundamental limits of semiconductor physics. How much further down can we go? It is hard to answer. Nevertheless, without doubt, we are facing numerous challenges, both practically and theoretically. Device simulation requires new theory and approaches to understand device physics and to design devices in the nano scale regime. Efforts have been put forth in recent years [12]-[16], but much more is needed. For these purposes, different types of MOSFET models are found in the literatures [17].

1.3 Device Scaling

There are two primary device structures that have being widely studied and used in CMOS technology. One is the bulk structure, where a transistor is directly fabricated on the semiconductor substrate. The other is called SOI (silicon-on-insulator), where a

transistor is built on a thin silicon layer, which is separated from the substrate by an insulator layer. The bulk structure is relatively simple from a device process point of view and still the standard structure in almost all CMOS based products until today.

For device scaling, basically it is tried to balance two things: device functionality and device reliability. Both of them have to be maintained at a smaller dimensional size. As the channel length of MOSFETs is scaled down to deep-submicrometer or nano scale regime, it is observed the reduction of threshold voltage with the reduction of channel length due to the charge sharing between the drain/source region and the channel and also due to high electric fields in the channel [1]. This effect is known as short channel effect (SCE). This effect is usually accompanied by degraded subthreshold swing (*S*), which causes difficulty in turning off a device. Primarily, there are two kinds of leakages, gate tunneling current and junction tunneling current. Both of them result from extremely scaled dimensions and high electric fields. Unwanted leakage currents can make the device fail to function properly. SCEs also include the drain induced barrier lowering (DIBL) effect. DIBL results in a drain voltage dependent on V_{th}, which complicates CMOS design at a circuit level. This effect arises as a result of two dimensional potential distribution and high electric fields in the channel region [18]. Therefore, to accomplish device scaling, it is needed to suppress any dimension related effects as much as possible. As a transistor scales, reliability concerns become more pronounced.

According to device scaling physics, increasing channel doping concentration can effectively suppress SCEs. Frank et al. recently published their work quantifying the dependence of the scale length on channel doping concentration [19].

Device scaling has come a long way. In the early days, gate length (*L*) is relatively long; a low uniform substrate concentration can be used providing satisfactory immunity of SCEs. A low substrate concentration gives a small body effect coefficient, which improves the subthreshold swing [20].

The emergence of MOS device in the sub-100 nm regime has led to the development of source/drain engineering procedures. Such procedures used to form pocket or halo regions. As the channel length decreases, a retrograde or ground plane doping profile can be introduced [21]-[22]. This doping profile has a low doping region near the Si/Oxide interface, but a high doping region underneath. The top region provides better body effect, while the bottom region suppresses SCEs. To achieve even shorter channel lengths, a ground plane profile is not enough, a more complicated doping

profile has to be added, namely the super halo [23]. In this case, high gradient halo dopings are formed next to the source/drain junction region. These heavily doped regions can effectively protect the source end of the channel region from the influence due to the electric fields from the drain diffusion region. As the channel length varies around the nominal gate length, a shorter length causes the halo regions to merge, ending up with higher substrate doping concentration, which resists V_{th} roll off. By using the ground plane and halo doping profiles, simulations show that the bulk structure can be scaled down to ~25 nm regime [23]. Also, due to the pocket implantation, V_{th} roll off is reversed with the reduction of gate length. This effect is known as Reverse Short Channel Effect (RSCE). There are many causes to originate the RSCE. Different sensitivities of pocket implant and SCE onto the channel length may constitute one of the main reasons for the threshold voltage roll-up shortly after an L longer than the shortest length of that technology. Another source of RSCE, originally in MOSFETs, is the channel concentration build-up resulting from the oxidation-enhanced-diffusion [24] or implant-damage-enhanced diffusion [25], which are very difficult to control, the electrical deactivation of arsenic [26] or boron penetration from poly-gate and oxide [27]. There are still other factors, such as, annealing [28] and salicide [29] within front end processes affecting the RSCE. By raising the doping concentration locally in the channel has been implemented via lateral channel engineering utilizing halo [30] or pocket implant [31], [32]-[36] surrounding drain/source regions is effective in suppressing SCE. The two terms are used interchangeably here although a halo may connote a pocket that is deeper than the drain. The halo or pocket implant can be either symmetrical [37] or asymmetrical [38] with respect to source or drain. Reported circuit applications include a 256 M-bit DRAM [39] and mixed-signal processor [40].

Recently, very excellent short-channel performance was demonstrated in 0.1 μm n-channel and buried p-channel MOSFET's using Large-Angle-Tilt-Implanted (LATI) pocket [37]. In fact, this pocket implant technology is found to be very promising in the effort to tailor the short-channel performances of deep-submicron as well as nano scale MOSFETs although careful tradeoffs need to be made between minimum channel length and other device electrical parameters [33]. It could be shown that with an optimized pocket implant process the saturation current is up to 10% higher

compared to a conventional optimized junction technology without increasing the leakage current of the devices minimum channel length.

1.4 Literature Review

In pocket or halo doped regions, the doping concentration is higher and gradually it decrease down to substrate region concentration in the lateral direction. Therefore, an understanding of the effects of a lateral doping profile in the channel is necessary. This thesis explores the effects of a laterally non-uniform doping distribution on the threshold voltage of a device by focusing on the Reverse Short Channel Effect (RSCE). This effect causes the threshold voltage (V_{th}) to rise as the gate length (L) shrinks because of the presence of laterally non-uniform channel doping. This thesis explores the analytical modeling areas of pocket implanted n-channel MOSFETs, such as, surface potential, threshold voltage incorporating bias and temperature effects, mobility modeling, subthreshold drain current modeling and low frequency drain current flicker noise modeling. But before start of the modeling, literatures have been reviewed extensively on different operational parameters of the pocket implanted n-MOSFET. These are provided in the next sub-sections.

1.4.1 Present RSCE Models

Various analytic models currently exist in the literature specifically for calculating the threshold voltage of devices exhibiting RSCE. Of these, two are aimed at providing models that allow a length-independent description of such devices for compact modeling. Another paper examines the effects of RSCE on the drain current and output conductance, modeling it as a potential barrier at the source and drain.

Brut et al. picture the RSCE as caused by extra doping of a Gaussian-like shape at the edge of the channel [41]. They then find an average doping of the channel ($N_{b,eff}$), integrating its doping from source to drain and dividing by the channel length. This gives an effective channel doping dependent upon the channel length. Using the definition of threshold voltage in [1], they replace the N_b with this $N_{b,eff}$ and add short channel effects (SCE) via a charge sharing description, which reduces Q_B by a multiplicative factor. Their model tracks actual V_{th} data closely for both channel length and back bias. They used five fitting parameters in the model of which three

are physically based and the other two are purely experimental parameters that allow them to fit the roll-off of the threshold voltage due to short channel effects.

Arora et al. take a similar approach but use negative fixed oxide charge as the cause of the RSCE [42], [43]. Assuming an exponentially decreasing distribution of fixed oxide charge near the source and drain, they also take an average by integrating the oxide charge from source to drain and then dividing by L. They then use this effective Q_{ox} to adjust the flat band voltage implementing the SCE differently. The final model has four fitting parameters. Similarly to Brut, the two parameters that are physically based are the magnitude (Q_{ox}) and characteristic decay length (x_o) of the extra Q_{ox}. The other two parameters allow them to fit the roll-off of the threshold voltage due to short channel effects.

Looking in general at the effect of a potential barrier at the source or drain, Hsu et al. use RSCE as an example to create their model [44]. Taking the standard equation for current over a barrier, they linearize its dependence on the voltage applied across it, giving an effective conductance modulated by the gate voltage. His equation shows that the output current is reduced by the source/drain resistance and a resistance due to the barrier. Interestingly, the feature that differentiates the barrier resistance from the source/drain resistance is that it depends upon gate voltage. Empirically coming up with an equation for the relationship between the gate voltage and barrier height, Hsu shows a nice fit to an experimental current-voltage curve with the model. They conclude that a potential barrier at the source and drain can severely degrade a MOSFET's performance. Each of these models accurately describes the Reverse Short Channel Effects in terms of threshold voltage vs. channel length characteristics.

1.4.2 Surface Potential

Solution of the Poisson's equation in the depletion region of the MOSFETs is an important step in order to determine the surface potential. Numerical device simulators like MEDICI [45] can produce most accurate solutions of the Poisson's equation. But analytical models that have been used for MOSFET device design, take less time for device simulation. It also provides device physics insight [46]. Analytical model shown in [33] does not satisfy the boundary conditions and device simulation results of MEDICI. Analytical model in [46] assume a step profile of pocket doping. Besides, Gaussian profile [47] and hyperbolic cosine function [48] were assumed for

the pocket profile to derive the threshold voltage equations. But it has been observed that linear profile of pocket doping produce better results for threshold voltage [49]. The previous works [46]-[49] are on the threshold voltage and surface potential modeling of pocket implanted MOS devices.

1.4.3 Threshold Voltage

The conventional threshold voltage model is derived for the homogeneous doping concentration [1]. An extension of the homogeneous model to the non-homogeneous impurity pileup in the vertical direction has been reported previously [18], [32], [50]. However, the reported model cannot be extended further to the pocket implantation, where inhomogeneity along the channel is the main cause for the Reverse Short Channel Effect (RSCE) [51]. Previous attempts for including the strong RSCE due to the pocket implantation in to a circuit simulation model were done by introducing model parameters without connection to the pocket profile [35]. A strong reverse short channel effect suppresses the short channel effect on threshold voltage of the MOSFET [52]. Threshold voltage model for pocket implanted MOSFETs for circuit simulation does not describe the sub-100 nm case [52].

1.4.4 Temperature Effects

It is well known that a change in the operating temperature of a device affects its characteristics and hence the circuit performance [1]. Accurate description of the temperature effects in devices is necessary to predict circuit behavior over a range of temperatures. A number of important model parameters such as mobility, threshold voltage, saturation velocity, parasitic series resistance, and source/drain junctions characteristics are temperature dependent. All of these temperature dependencies need to be modeled correctly. Since the threshold voltage of MOSFET is an important parameter its effect on temperature should be studied, especially in lower temperature operation. There are many benefits for MOSFET operating in lower temperatures, such as, improvement of subthreshold swing, increase of carrier mobility, higher saturation velocity and operation speed, lower voltage swing and reduced leakage current, improved latch up immunity, reduction of short channel effects and improved electro-migration and device power dissipation etc. Temperature dependent conventional and SOI MOS device physics and characteristics have already been

discussed in the literatures [1], [53]-[59]. Comprehensive analysis of pocket implanted MOSFETs from low-temperature operation has been described in [60]. But here model is developed using an exponential profile of pocket doping.

1.4.5 Inversion Layer Effective Mobility

The inversion layer mobility in Si MOSFET's has been a very important physical quantity as a parameter to describe the drain current and a probe to study the electric properties of a two-dimensional carrier system. Therefore, much study [61] since the 1960's has revealed dominant scattering mechanisms determining the mobility.

On the other hand, it has already been reported that the electron and hole mobilities in the inversion layer on a (100) surface follow the universal curves at room temperature independent of the substrate impurity concentration or the substrate bias when plotted as a function of effective normal fields, E_{eff} [62]. Pocket implant causes a strong non-uniform lateral doping profile. With the reduction of the channel length or with the increase of the pocket profile parameters there is a pronounced increase of the effective the channel doping concentration, the effective mobility is supposed to be degraded further due to Coulomb scattering with the ionized dopants and charged interface traps at low vertical electric fields, i.e., at low gate bias. This is called “roll-off” region. As the effective vertical field increases, the mobility becomes independent of the channel doping and all the samples approach the so-called universal curve. In this region, the main scattering processes are phonon and surface roughness scattering that do not depend on channel doping. In most circuit models [63]-[65], simple mobility models [17], [66] are used to describe the effective surface mobility neither accounting for the degradation by Coulomb scattering in heavily doped MOSFET's (only the ‘universal curve’ [67] is modeled) nor accounting for the lateral non-uniform doping profile. This neglect can cause simulation errors in the transconductance of short n-MOS pocket implanted devices of up to 50% which can not be tolerated in today's circuit simulations [68].

1.4.6 Subthreshold Drain Current

When the gate voltage is below the threshold voltage and the semiconductor surface is in weak inversion, the corresponding drain current is called the subthreshold current. The subthreshold region is particularly important for low-voltage, low-power

applications, such as, when the MOSFET is used as a switch in digital logic and memory applications, because the subthreshold region describes how the switch turns on and off. Already few papers have been published focusing on the subthreshold behavior of pocket implanted n-MOSFET [69]-[72]. In [36], models for subthreshold and above subthreshold currents in 0.1 μm pocket n-MOSFETs for low-voltage applications have been derived based on the diffusion current transport equation. But this model characterizes the localized pile-up of channel dopants as step profile. The influences of halo implant dose and tilt angle on the off-state current have been investigated by technology computer aided design (TCAD) simulation in [69]. A channel length independent subthreshold characteristic in submicron MOSFETs has been reported by Shin et al in [70] due to the presence of localized pileup of channel dopants near the source and drain ends of the channel. An analytical subthreshold current model for pocket-implanted n-MOSFETs has been presented in [71]. But this model characterizes the localized channel dopants as step profile. In [72], the authors presented an analytical model for the subthreshold current applicable for any type of FET and showed that the subthreshold current of nMOSFETs, which is mainly due to diffusion, is determined by the internal two-dimensional hole distribution across the device.

1.4.7 Low Frequency Drain Current Flicker Noise Model

In the low frequency region, flicker noise is dominant. Flicker noise affects the signal-to-noise ratio in operational amplifiers and in analog-to-digital-converters and digital-to-analog converters. Phase noise of voltage controlled oscillators originating from flicker noise is another concern for radio frequency applications. In order to reduce the low-frequency noise in MOS devices, the physical origin of flicker noise in the MOS devices should be studied and modeled properly. Already few papers have been published focusing on the degradation of drain current flicker noise due to pocket implantation in MOSFETs [73]-[79]. New pocket structures, such as, single pocket, asymmetric channel structure, [73], [75] and epitaxial channel MOSFETs [76], [77], were proposed to reduce the drain current flicker noise by elimination of pocket implantation. The low frequency noise in pocket implanted MOSFETs may result from additional oxide trap creation due to pocket implantation [77], but this was also not supported by the experiment [78]. In [78], it was shown that the non-uniform

distribution of threshold voltage along the channel resulting from the pocket implantation is responsible for the low frequency drain current flicker noise degradation, but there step doping profiles are used in the pocket implanted region to model the drain current flicker noise.

1.5 Objectives

The objectives of the thesis are to develop various analytical models of the pocket implanted nano scale n-MOSFET based on linear pocket profiles.

The specific aims of this thesis are:

1. To study the characterization of the lateral doping profiles at the source and drain edges of the pocket implanted n-MOSFET and hence to develop the doping profile models of the pocket implanted nano scale n-MOSFET.
2. To develop the surface potential model of the pocket implanted nano scale n-MOSFET assuming linear pocket doping profiles.
3. To incorporate the effective doping profiles in the threshold voltage model of the same device including substrate and drain bias effects.
4. To incorporate the temperature effects in the threshold voltage model.
5. To develop an inversion layer effective mobility model for the same device.
6. To develop a subthreshold drain current model of the pocket implanted nano scale n-MOSFET using the developed pocket doping profiles and incorporating the inversion layer effective mobility model.
7. To develop low frequency drain current flicker noise model.

The outcome of the thesis will be several models of the pocket implanted n-MOSFET, such as, doping profile, surface potential, threshold voltage incorporating bias and temperature effects, inversion layer effective mobility, subthreshold drain current and low frequency drain current flicker noise models. Fabrication and doping profile characterization technique of the pocket implanted n-MOSFET will also be discussed. Experimental verifications will also be made.

1.6 Methodology

The model derived in this work aims to be more exact in modeling the effects of a non-uniform lateral channel doping profile by taking an effective channel doping

concentration. At first, pocket implantation technology, pocket profile characterization and various types of pocket doping profiles in the literature will be studied. Then a linear pocket doping profile at the source and drain edges at the surface of the pocket implanted n-MOSFET will be established for this work. After that various operational parameters will be studied and then suitable models for these parameters of the pocket implanted n-MOSFET will be developed. One developed model will be used to develop the other models. Effects of various parameters will be incorporated in the model.

After that an analytical model that can predict the surface potential of the nano scale pocket implanted n-MOSFET will be derived incorporating the linear pocket doping profile. Here the 1-D pocket doping profile across the channel will be transformed to an effective doping concentration expression (N_{eff}), which is used in the Gauss's law to derive the model applying the appropriate boundary conditions.

Then a model capable of describing the threshold voltage of the pocket implanted nano scale n-MOSFET incorporating N_{eff} and threshold voltage shift, ΔV_{th} incorporating drain and substrate bias effects. Here a short channel threshold voltage equation is used for the case of pocket implanted n-MOSFET where exponential dependence on channel length and a linear dependence on drain and substrate biases have been observed [80]. Effects of temperature variation will be studied using threshold voltage model by incorporating various temperature dependent parameters.

Besides, an analytical inversion layer effective mobility model will be developed taking into account the pocket doping as well as temperature effects for the nano scale pocket implanted n-MOSFET. The total number of inversion layer charges will be calculated numerically using the threshold voltage and the surface potential models obtained. The pocket profile and device parameters as well as bias voltages will be varied to investigate the pocket implantation effect on effective mobility. Then a subthreshold drain current model will be developed incorporating this effective mobility model and using the conventional drift-diffusion equation. The surface potential model derived earlier will also be used. Finally, an analytical drain current flicker noise model will be developed taking into account the pocket doping effect and using the developed threshold voltage model.

After the model development, simulation results will be obtained by developing the several MATLAB programs and all the necessary function files. The simulated results

will be analyzed to evaluate the device performance and characterize the pocket implanted nao scale n-MOSFET. The simulated results will also be compared with the results obtained using the other pocket doping profiles found in the literature. Besides, experimental data already published in the different literatures will be fitted with the simulated data of the proposed analytical models.

1.7 Organization of the Thesis

This Thesis is organized as follows:

Chapter 2 reviews the threshold voltage control and the Short Channel Effects (SCE) in conventional bulk n-MOSFET. Then it describes the how the structure of the pocket implanted n-MOSFET is formed. After that, it elucidates how Reverse Short Channel Effect (RSCE) arises due to pocket implantation and the other causes of RSCE. Then it explains the lateral doping profile characterization techniques followed by the review of the existing models for the doping profiles that cause RSCE and finally, proposes the modeling of the lateral doping profile of the pocket implanted n-MOSFET.

Chapter 3 describes model derivation techniques and then presents various models of the pocket implanted nano scale n-MOSFET using the lateral doping profile model proposed in chapter 2.

Chapter 4 provides MATLAB simulation results of the developed models and explores the effects of the variation of the different device and pocket profile parameters of the pocket implanted n-MOSFET as well as of the various bias conditions. It also explains the simulated results and shows the comparisons of the proposed model with the other pocket doping profiles found in the literatures. Experimental verifications are also made for few models.

Finally, Chapter 5 concludes the thesis with a summary, limitations of the proposed models and few suggestions for the future scopes of this work.

Chapter 2

Pocket Implanted n-MOSFET

2.1 Introduction

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a very important device for very large scale and ultra large scale integrated circuits, such as, microprocessors and semiconductor memories. It is also used in power electric circuits. CMOS device dimensions are continuously being shrinking to enhance the circuit speed and density and this has become possible due to the nonstop progress of the semiconductor device process technology. But this reduction of device dimensions reduces the threshold voltage (V_{th}). This adverse V_{th} roll-off effect is perhaps the most daunting road block in future MOSFET design and modeling [33]. The minimum acceptable channel length, L_{min}, is primarily determined by the threshold voltage roll-off, which is known as Short Channel Effect (SCE). So, V_{th} is an important parameter in MOS device design and fabrication.

The pocket implant technology has been developed to combat SCE and enables gate length reduction in to the nano scale regime [23]. Using this technology V_{th} roll off can be reduced, i.e., SCE can be improved without increasing substrate concentration and/or oxide thickness [33]. This can be achieved by locally raising the channel doping next to the drain or drain/source junctions. This improvement can be observed as a delayed onset of V_{th} roll-off or an increased V_{th}, which consequently reduces the subthreshold leakage current. Furthermore, the driving capability of pocket-implanted device is enhanced due to the minimum channel length deviation. The phenomenon in which the threshold voltage of a device increases as the channel length decreases is known as the Reverse Short Channel Effect (RSCE). This behavior is the opposite of what is expected from SCE.

In the first part of this chapter, threshold voltage control and combating the SCE will be discussed. Then in the second part of this chapter, the structure and formation processes of the pocket implanted n-MOSFET will be discussed. Then the characterization and modeling of the pocket doping profile will be discussed.

2.2 Threshold Voltage Control

The threshold voltage is one of the most important parameters of the MOSFET and it is given by (2.1). Flat band voltage incorporates the effects of the fixed-oxide charge and the difference in work function. Substrate bias effect on the threshold voltage is also incorporated in to this model. Because, a reverse bias between the substrate and the source widens the depletion region and results an increase in the threshold voltage to accommodate larger inversion charge.

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2q\varepsilon_s N_{sub}\left(2\psi_B + V_{BS}\right)}}{C_{ox}} \qquad (2.1)$$

,where V_{FB} is the flat band voltage, ψ_B is the electrostatic potential in the bulk of the semiconductor, q is the electronic charge, ε_{Si} is the dielectric permittivity of Si, N_{sub} is the substrate doping concentration, V_{BS} is the reverse substrate to source bias and C_{ox} is the oxide capacitance per unit area.

Precise control of threshold voltage of a MOSFET is essential for a reliable circuit operation when the device is used in an integrated circuit. It is generally adjusted vertically through ion implantation into the channel region. The threshold voltage of an n-channel MOSFET is adjusted by boron implantation through surface oxide. V_{BS} is the reverse substrate to source bias. Precise control of threshold voltage of a MOSFET is essential for a reliable circuit operation when the device is used in an integrated circuit. It is generally adjusted through ion implantation into the channel region. The threshold voltage of an n-channel MOSFET is adjusted by a boron implantation through a surface oxide.

2.2.1 Non-uniform doping

In the last section, it is assumed that the doping concentration in the channel is uniform. In modern MOSFET technology, ion implantation is used to modify the doping profile and improve the device performance for specific applications. This

makes the doping non-uniform for practical devices. A lighter doping at deeper regions reduces drain substrate capacitance and the substrate-bias effect and, higher level at deeper region reduces punch-through between source and drain. A lighter doping level near the SiO_2-Si interface lowers the threshold voltage, reduces the field and improves mobility. Two general cases of non-uniform doping are named as high-low and low high profiles, and are depicted in Fig. 2.1, with their step-profile approximations for ease of analysis.

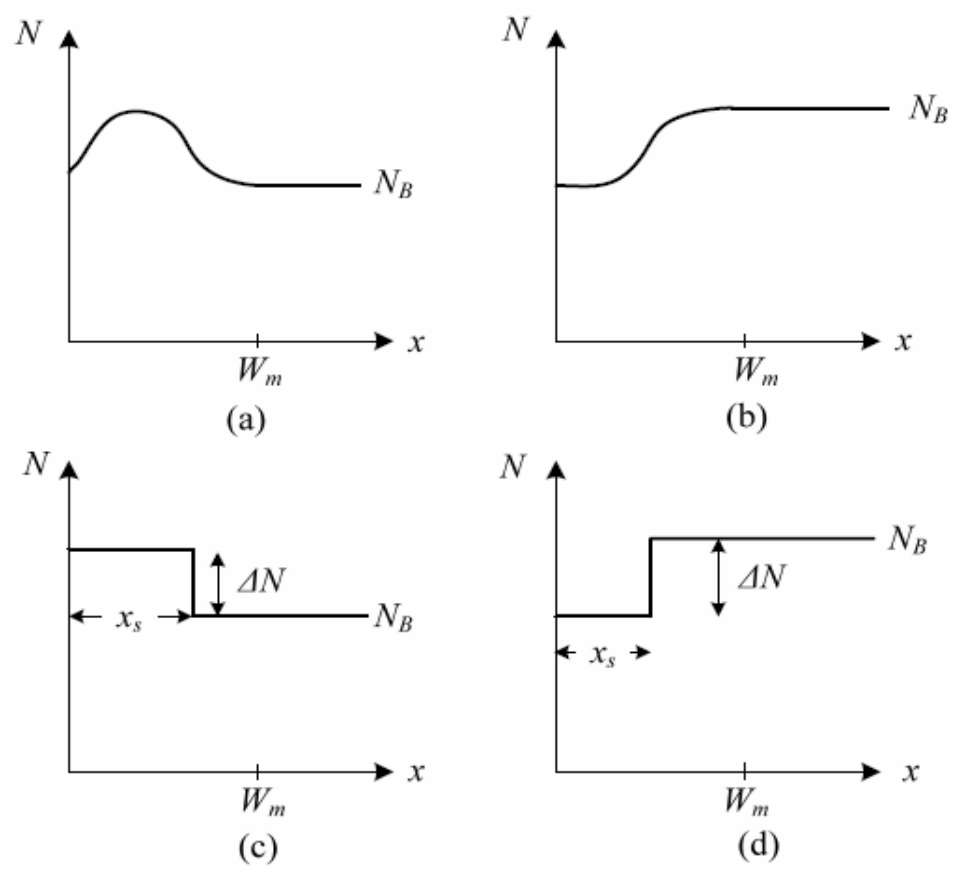

Fig. 2.1 Non-uniform channel doping profiles. (a) high-low profile. (b) low-high profile. (c) step-profile approximation of high-low profile (d) step-profile approximation of low-high profile [1]

The equation for the threshold voltage is,

$$V_T = V_{FB} + \psi_S + \frac{Q_{dep}}{C_{ox}}$$
$$= V_{FB} + 2\psi_B + \frac{q}{C_{ox}} \int_0^{W_m} N(x)dx \qquad (2.2)$$

,where Q_{dep} is the depletion layer charge and W_m is the maximum width of the depletion region which is determined by Poisson's equation with the onset of strong inversion being the boundary condition.

The surface potential is,

$$\psi_S = 2\psi_B = \frac{q}{\varepsilon_{ox}} \int_0^{W_m} xN(x)dx \qquad (2.3)$$

The definitions of ψ_B and V_{FB} become complicated for a non-uniform doping profile. However, these values can be calculated with sufficient accuracy using the background doping of N_B.

High-low profile

The threshold voltage shift due to ion implantation can be simplified by considering an idealized step profile as shown in Fig. 2.1 (c). After thermal annealing, the implant profile is approximated by the step function with step depth x_s. This depth is roughly equal to the sum of the projected range and the standard deviation of the original implant. If $x_s > W_m$, the surface region can be considered as a uniformly doped region with a higher concentration and the threshold voltage is identical to that given by equation (2.2). For $W_m > x_s$, the threshold voltage is obtained from equation (2.2).

$$\begin{aligned} V_T &= V_{FB} + 2\psi_B + \frac{q}{C_{ox}} \left\{ \int_0^{x_s} (N_B + \Delta N)dx + \int_{x_s}^{W_m} N_B dx \right\} \\ &= V_{FB} + 2\psi_B + \frac{qN_B W_m + q\Delta N x_s}{C_{ox}} \end{aligned} \qquad (2.4)$$

The value of maximum depletion width W_m can be calculated from equation (2.3).

$$2\psi_B = \frac{q}{\varepsilon_{ox}} \left\{ \int_0^{x_s} x(N_B + \Delta N)dx + \int_{x_s}^{W_m} xN_B dx \right\} \qquad (2.5)$$

$$W_m = \sqrt{\frac{2\varepsilon_{ox}}{qN_B} \left(2\psi_B - \frac{q\Delta N x_s^{\,2}}{2\varepsilon_{ox}} \right)} \qquad (2.6)$$

Substituting this value in equation (2.4),

$$V_T = V_{FB} + 2\psi_B + \frac{1}{C_{ox}} \sqrt{2q\varepsilon_{ox}N_B \left(2\psi_B - \frac{q\Delta N x_s^{\,2}}{2\varepsilon_{ox}} \right)} + \frac{q\Delta N x_s}{C_{ox}} \qquad (2.7)$$

From the above equations, it is seen that added surface doping increases V_T and decreases W_m and for the same dose, the threshold voltage is largest with the added doping closest to the surface.

The subthreshold swing has to be interpreted by comparing the gate-oxide capacitance C_{ox} to the depletion capacitance C_D. For the high-low profile, the added doping decreases W_m, increases C_D, and results in a larger subthreshold swing.

Low- high profile

Similar analysis like the high-low case, can be performed for low-high profile shown in Fig. 2.13 (b), (also called the 'retrograde profile'), with a ΔN being subtracted from the background doping. The equations for the threshold voltage and depletion width then become

$$V_T = V_{FB} + 2\psi_B + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{ox}N_B\left(2\psi_B + \frac{q\Delta N x_s^{\,2}}{2\varepsilon_{ox}}\right)} - \frac{q\Delta N x_s}{C_{ox}} \qquad (2.8)$$

$$W_m = \sqrt{\frac{2\varepsilon_{ox}}{qN_B}\left(2\psi_B + \frac{q\Delta N x_s^{\,2}}{2\varepsilon_{ox}}\right)} \qquad (2.9)$$

So, the threshold voltage decreases and the depletion layer width increases with the low-high profile.

2.3 Short Channel Effects

Since the beginning of the integrated-circuit era, the minimum feature size of the transistor has been reduced by more than two orders of magnitude. As MOSFET dimensions shrink, proper designing is necessary to preserve the long-channel behavior as much as possible. As the channel length decreases, the source and drain depletion widths become comparable to the channel length and eventually results in punch-through between the drain and the source. To prevent this higher channel doping is required. However, higher channel doping will result in an increase in the threshold voltage, so a thinner oxide is necessary to control the threshold voltage. It is clear that the device parameters are interrelated. Hence certain scaling rules are used to optimize the device performance. Even with the best scaling rules, deviations from the long-channel behavior are inevitable as the channel length becomes smaller. For a shorter channel device, the potential distribution in the channel depends on the

longitudinal field E_y (controlled by the drain bias) as well as the transverse field E_x (controlled by the gate voltage and the back-substrate bias). As that the potential distribution becomes two dimensional, the gradual channel approximation ($E_x >> E_y$) is no longer applicable for such a device. This two-dimensional potential distribution cause many undesirable electrical behaviors. With the increase in electric field, the channel mobility becomes field-dependent, and results in velocity saturation. With further increase in electric field, carrier multiplication near the drain occurs, which leads to substrate current and parasitic bipolar-transistor action. This high electric field can also results in hot-carrier injection into the oxide leading to oxide charging and subsequent threshold-voltage shift and transconductance degradation. The short-channel effects (SCE) are summarized bellow [81]:

- Threshold Voltage (V_T) is dependent on channel length (L).
- The drain current (I_D) does not saturate with drain bias (V_D), both above and below threshold.
- I_D is not proportional to $1/L$.
- Device characteristics degrade with the operation time.

The short channel effects complicate device operation and degrade device performance. So they should be eliminated or minimized so that a physical short channel device can have long channel behavior

2.3.1 Threshold voltage roll off in linear region

For a short channel device, the threshold voltage in the linear region usually becomes less positive for n-channel device with the decrease in channel length. An example of this roll off phenomenon is shown in Fig. 2.2 for two different drain source voltages [82]. The shift in threshold voltage is significant for short channel device and higher drain source voltage. The charge sharing model [83], as shown in Fig. 2.3, can explain the roll-off. It is assumed that the n-channel MOSFET is operating in the linear region. So the depletion layer width in the source and drain junction is almost equal. So, the depletion region is rectangular. For a short channel device, the channel depletion region overlaps the source and drain depletion regions. So, there will be a reduction of charges in the depletion layer from the rectangular region to trapezoidal region as shown in Fig. 2.3, and it can be assumed that all the charge induced by the

gate bias is in the trapezoidal region. The model of short channel effect (SCE) is given in many ways. This SCE is often modeled via charge sharing, where the source and drain depletion regions control some portion of the charge under the gate, effectively reducing the doping in the area [17].

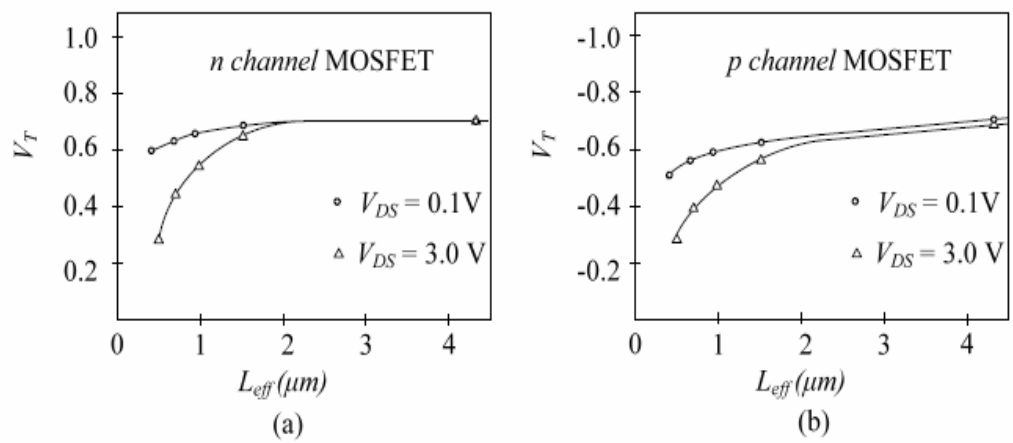

Fig. 2.2 Dependence of threshold voltage on effective channel length (L_{eff}) and drain bias [82]

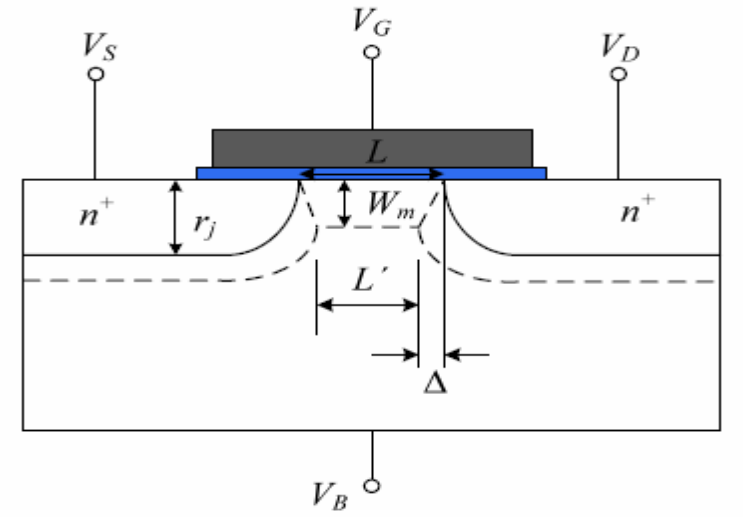

Fig. 2.3 Schematic of the charge-sharing model [1]

In terms of equation (2.1), the SCE is added by substituting Q'_B for Q_B, where Q'_B is less than Q_B and decreases with L, thus causing V_T to decrease or "roll-off". For short channel bulk n-MOSFET there will a shift in threshold voltage due to the reduction of charges in the depletion layer from the rectangular region to the trapezoidal region and this threshold voltage shift (ΔV_T) is derived as in equation (2.10) [83]. In fact, this

ΔV_T is known as short channel parameter. This parameter is then added with the long channel threshold voltage equation given in equation (2.1). The combined equation (2.60) is called threshold voltage equation for both the long and short channel n-MOSFET.

$$\Delta V_T = -\frac{qN_{sub}W_m r_j}{C_{ox}L}\left(\sqrt{1+\frac{2W_m}{r_j}}-1\right) \tag{2.10}$$

,where N_{sub} is the substrate doping concentration, W_m is the width of the depletion region, r_j the junction depth, L the channel length and C_{ox} in the oxide capacitance per unit area and the maximum width of the depletion region is given by equation (2.59) and V_{BS} being the substrate bias voltage

$$W_m = \sqrt{\frac{2\varepsilon_s\left(\psi_s + V_{BS}\right)}{qN_{sub}}} \tag{2.11}$$

This parameter (ΔV_T) should be added to the threshold voltage (V_T) derived in equation (2.1). So, the threshold voltage equation for short channel MOSFET is

$$V_{T,S} = V_{T,L} + \Delta V_T \tag{2.12}$$

It is clear form equation (2.10) that for a constant N_{sub}, W_m, r_j and C_{ox}, the change in threshold voltage is inversely proportional to the channel length, L. For a long channel device this change is negligible. But for short channel devices, the threshold voltage is reduced because the channel length becomes comparable to the width of the depletion region.

Channel Length Modulation (CLM)

Channel length modulation (CLM) is a shortening of the length of the inverted channel region of a MOSFET with the increase in drain bias in the saturation region. After pinch-off, the effective length of the channel decreases with the increase of drain voltage. As resistance is proportional to length, shortening the channel decreases its resistance, causing an increase in drain current with increasing drain bias for a MOSFET operating in saturation.

Drain Induced Barrier Lowering (DIBL)

When the source and drain depletion regions are a substantial fraction of the channel length, short-channel effects start to occur. Once the sum of these depletion widths approaches the channel length, a condition called punch-through occurs. This is due to

the lowering of the barrier near the source, referred to as drain-induced barrier lowering (DIBL). This results in a large leakage current between the source and drain. This current is a strong function of the drain bias.

For a long channel device, a drain bias can change the effective channel length, but the barrier at the source end remains unaffected as shown in Fig. 2.4 (a). But for a shorter channel device, the drain bias can influence the barrier at the source end in Fig. 2.4 (b), such that the channel carrier concentration at that location is no longer fixed. This lowering of the source barrier causes an injection of extra carriers, resulting in a substantial increase in drain current. Fig. 2.4 (b) shows that punch-through condition occurs at the semiconductor surface for a short channel device. There is a reduction in substrate concentration below the drain and source regions. This reduced substrate doping widens the depletion widths. Therefore, punch-through can also happen through the bulk. High leakage current limits the device operation for short channel MOSFETs.

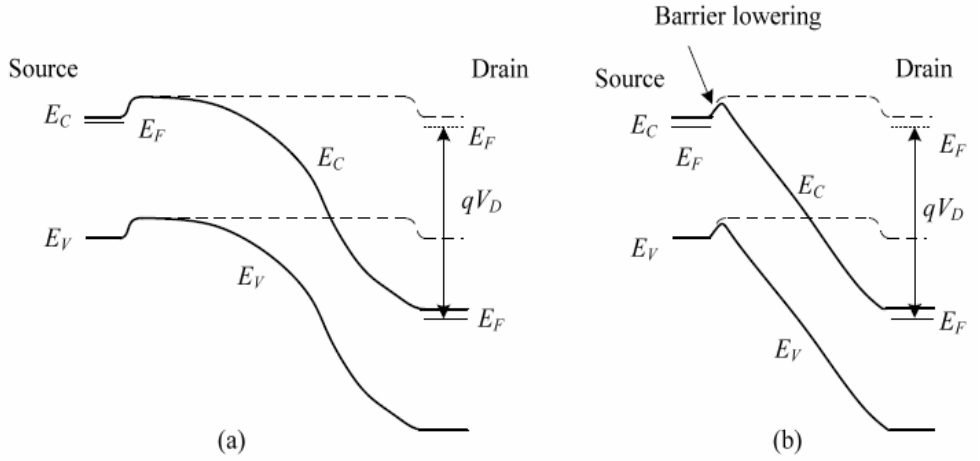

Fig. 2.4 Energy-band diagram at the semiconductor surface from source to drain, for (a) long-channel MOSFET and (b) short-channel MOSFET showing DIBL effect. Dashed line is for $V_D = 0$ and solid line is for $V_D > 0$ [81]

2.3.2 Combating Short Channel Effects

The SCE is simulated for conventional bulk n-MOSFET using equations (2.1), (2.10)-(2.12) for substrate concentration, $N_{sub} = 3.5\times10^{17}$ cm^{-3} and oxide thickness, $t_{ox} = 2.5$ nm. The result is shown in Fig. 2.5. It is observed that beyond 1 μm of MOSFET's gate length threshold voltage starts to decrease when gate length is decreased. This is

called SCE. To suppress this SCE, substrate doping concentration or oxide thickness is increased. This increases the threshold voltage, but threshold voltage roll-off becomes more steeper. When substrate concentration and/or oxide thickness are increased then threshold voltage starts to decrease at shorter gate length as shown in Fig. 2.6 i.e., V_{th} roll off region has been shifted to the left. With the reduction of gate length oxide thickness reduction is necessary. But to combat SCE oxide thickness has to be increased. On the other hand, increasing substrate concentration and oxide thickness has other deleterious effects, and thus device structure of conventional bulk n-MOSFET has to be modified.

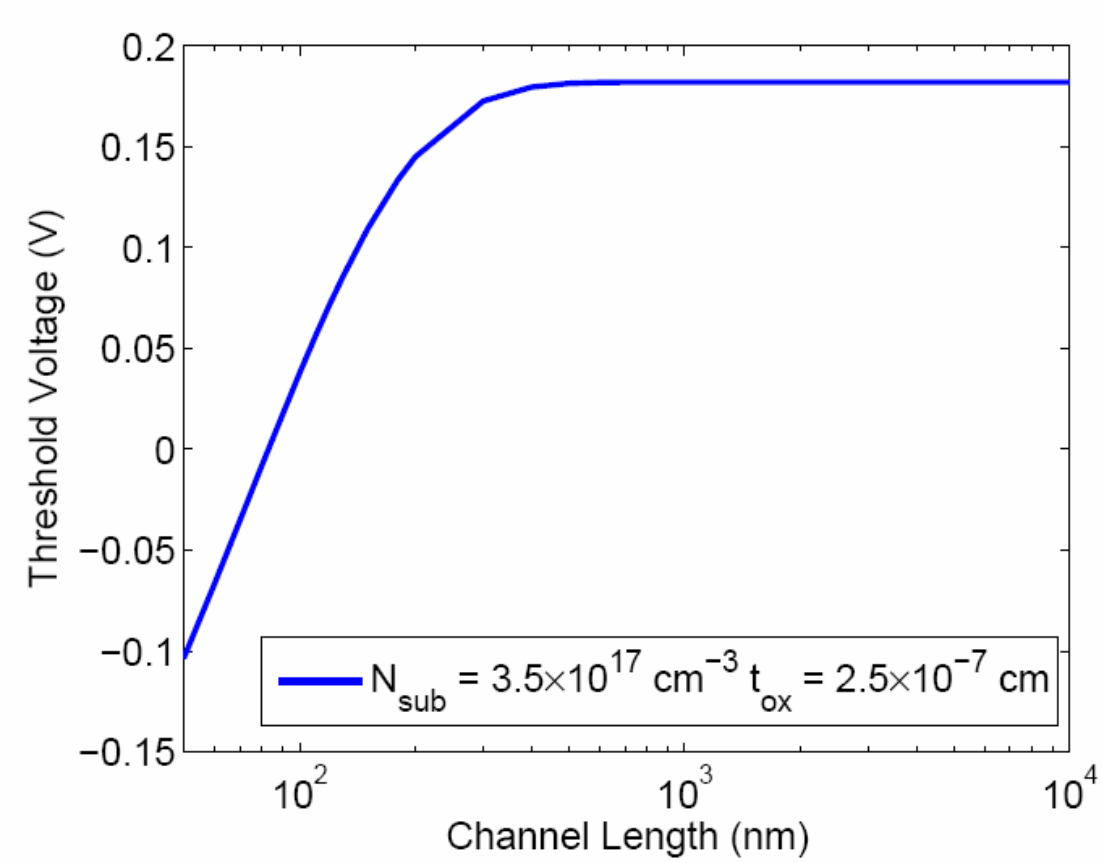

Fig. 2.5 Short Channel Effects in conventional bulk n-MOSFET

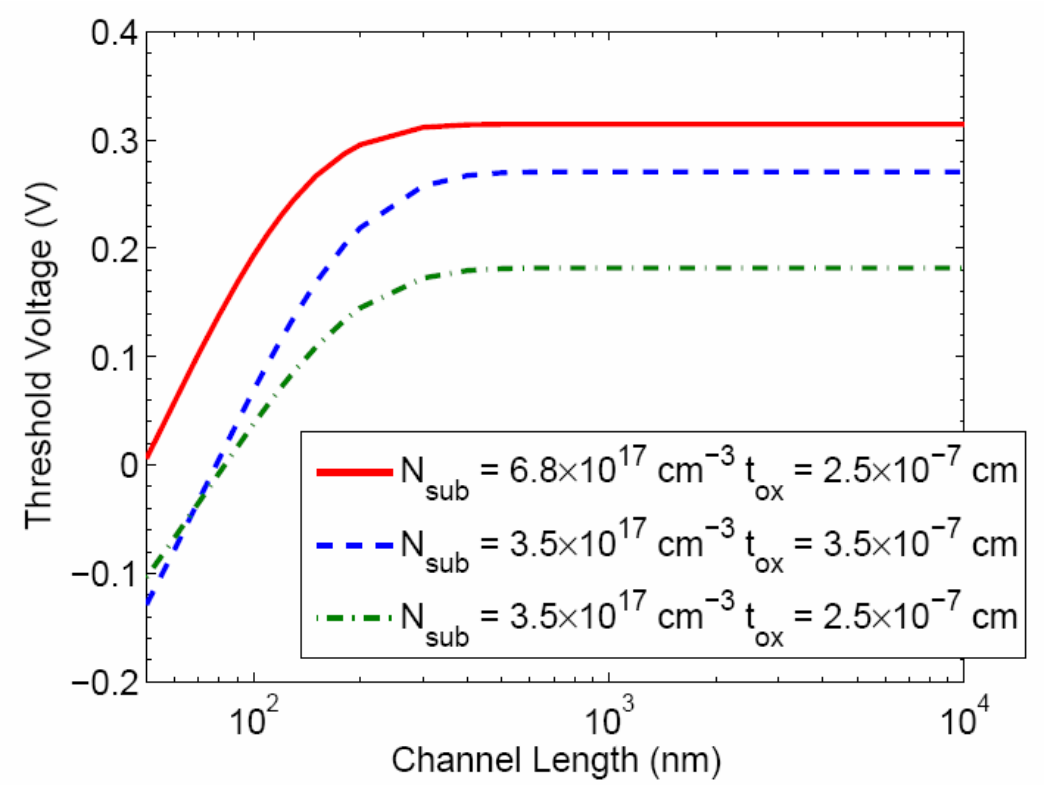

Fig. 2.6 Reduction of Short Channel Effects in conventional bulk n-MOSFET

2.4 Formation of the Pocket Implanted n-MOSFET

The emergence of MOSFET devices featuring sub-100 nm channel lengths has led to source/drain engineering procedures used to form halo or pocket region. Therefore, modeling of the pocket implanted MOSFET device is necessary. To model this device, it is also necessary to know the structure of the pocket implanted MOSFET device. The structure of the pocket implanted MOSFET device is similar to that of a bulk n-MOSFET. It differs only in the pockets formed adjacent to the heavily doped source and drain sides of the channel region. These regions comprised with the same conductivity type as the semiconductor substrate or well region, but featuring a higher dopant level than the semiconductor substrate or well region, reduce the extent of the depletion region when compared to depletion regions formed at the junctions of the non-pocket structures, thus resulting in less punch through current. However, the increased dopant concentration of the pocket region adversely influences MOSFET performance via the increased junction capacitance. Therefore, trade-offs between yield, less punch through current, increased junction capacitance arise when implementing pocket or halo regions for short channel MOSFET devices. Like conventional bulk MOS device, it is also two types- p-type and n-type. There are

various methods or processes of forming pocket implanted MOSFET structures. Since it is required to model the pocket implanted n-MOSFET in this work, therefore, the fabrication processes for the formation of the n-type pocket implanted MOS device are described in this section from reference [84].

The process for forming a pocket implanted MOS device is to place the pockets adjacent to the top portion of the sides of a heavily doped source/drain region in an area of a semiconductor substrate not covered by the gate structure or by composite insulator spacers located on the sides of the gate structure. Different region numbers of Fig. 2.7 are shown in parenthesis in the texts while describing their formation processes.

At first, a semiconductor substrate (1) comprised of single crystalline, p-type Si, featuring a <100> crystallographic orientation, is used. If desired, a p-well region as well as a threshold adjust region can be formed in a top portion of semiconductor substrate for the purposes of adjusting the dopant level of semiconductor substrate, and therefore adjusting the threshold voltage of a subsequent MOSFET device. Gate insulator layer (2), comprised of SiO_2, is next thermally grown to a thickness between about 1 to 2 nm, in an oxygen-steam or in oxygen ambient. If desired gate insulator can be comprised of Si_3N_4 or of a nitrided oxide layer formed by annealing of a base SiO_2 layer in a NO or NO_2 ambient. In addition, gate insulator can be comprised of a high-k dielectric material, such as, HfO_2.

After the formation of gate oxide layer, a conductive layer, such as, a doped polysilicon layer, or a metal silicide layer is formed at a thickness between about 100 to 250 nm, on gate insulator layer. The doped polysilicon option is accomplished via deposition of a polysilicon layer, via low pressure chemical vapor deposition (LPCVD), or plasma enhanced chemical vapor deposition (PECVD), procedures with the polysilicon layer in situ doped during deposition via the addition of arsine or phosphine to a silane or disilane ambient.

Photolithgraphic and anisotropic reactive ion etching (RIE) procedures are employed to define gate structure (3) in the conductive layer using Cl_2 or SF_6 as an etchent. Gate structure defining photoresist is removed using oxygen ashing and wet clean procedures with buffered HF acid. Then a thermal oxidation procedure is used to grow 1 to 3 nm thick SiO_2 layer (4) on the exposed surface of the gate structure.

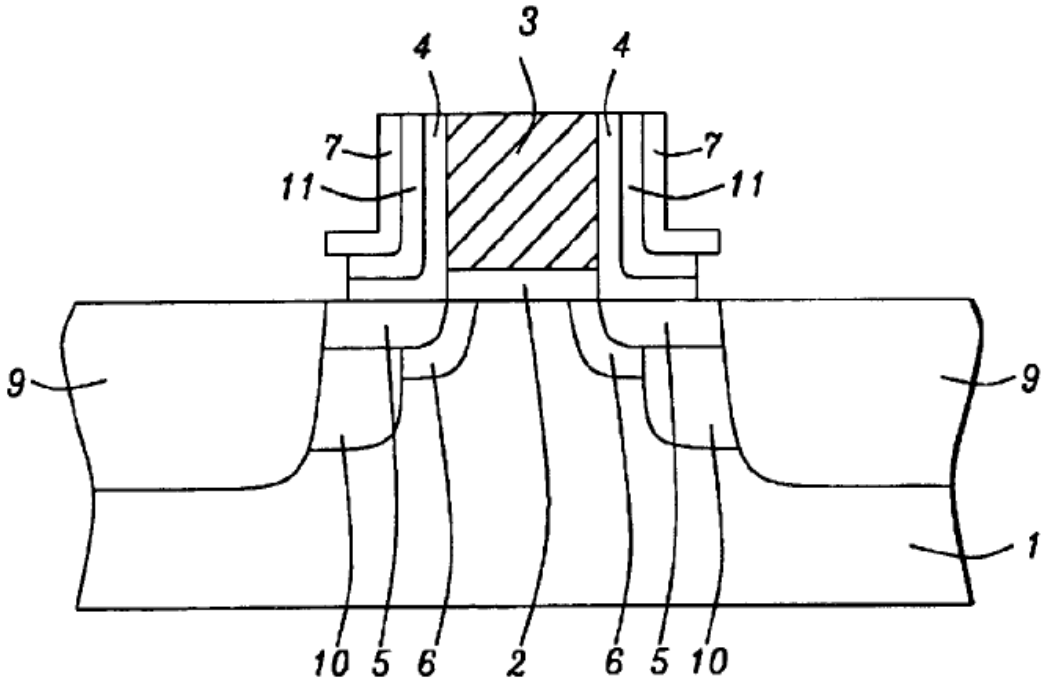

Fig. 2.7 Pocket implanted n-MOSFET with composite insulator spacers [84], various regions numbers are shown in the texts in parenthesis

In the next step, an implantation procedure is performed placing As or P ions in an area of semiconductor substrate, not covered by the gate structure, forming lightly doped drain or LDD region and is accomplished at an implant energy between about 1 to 10 KeV, for As ions and at an implant dose between about 3×10^{13} to 3×10^{15} atoms/cm^2. To prevent encroachment of the SPE depletion regions, which can alter or reduce the designed channel length, a shallow pocket implant region, featuring the same conductivity type as semiconductor substrate, but featuring a higher dopant level than substrate, is formed to completely envelope n-type LDD region (5). This is accomplished via ion implantation procedures performed in situ, either before or after implantation of n-type LDD region. The p-type pocket region (6) is obtained via implantation of boron or BF_2 ions, at energy between about 7 to 15 KeV, at a dose between about 2×10^{13} to 7×10^{13} atoms/cm^2.

A composite insulator spacer is next formed on the sides of the gate structure 3. First SiO_2 layer 11 is deposited at a thickness between 8 to 15 nm via LPCVD or PECVD procedures using tetraethylorthosilicate (TEOS) as source. Next Si_3N_4 layer (7) is deposited at a thickness between 15 to 30 nm via LPCVD or PECVD procedures. Next 40 to 70 nm SiO_2 layer (8) is deposited via LPCVD or PECVD procedures again

employing tetraethylorthosilicate (TEOS) as source and using CHF_3 as an etchant for SiO_2 and Cl_2 for Si_3N_4 employing anisotropic RIE procedure.

In the next stage, heavily doped n-type source/drain region (9) is formed in semiconductor surface areas not covered by the gate structures or by the composite insulator spacers via implantation of As or P ions at an energy between about 35 to 75 KeV at a dose between about 2×10^{15} to 7×10^{15} atoms/cm^2. This is followed by an additional ion procedure employing P ions at energy between 25 to 45 KeV at a dose between about 1×10^{13} to 4×10^{13} atoms/cm^2 to reduce the junction capacitance. A tilt angle between about 0 to 7 degrees is used for the P implantation procedure to grade the n^+/p well dopant profile.

To reduce the level of punch trough current generated by the depletion regions, a deep p-type pocket region (10) higher in p-type dopant concentration than that in the p-type substrate concentration is formed. This is accomplished via implantation of boron or BF_2 ions at an energy between about 21 to 31 KeV, at a dose between about 3×10^{13} to 8×10^{13} atoms/cm^2 and with tilt angle about 10 to 30 degrees. The implant energy chosen allows the p-type ions to penetrate the horizontal portion of the L shaped Si_3N_4 spacer component (7) as well as the portions of the underlying SiO_2 layers (11) and (4). In addition, the implant dose is great enough to form deep p-type pocket implant region (10), in exposed portion of the lighter doped shallow p-type pocket region (6), but the implant dose is not enough to completely compensate the heavily doped n-type source/drain region (9), thus resulting in p-type pocket implant region, located surrounding the only the sides of the heavily doped n-type source/drain region (9). Portions of the n-type LDD region (5), still enveloped by shallow p-type pocket implant region (6), located underlying the vertical component of the L shaped Si_3N_4 spacer component, remain uncompensated and therefore still directly influence the channel length dimension of the device.

Finally, an anneal procedure, performed via rapid thermal annealing (RTA), is applied at a temperature between about 1050 to 1090^0 C for a time between about 0 to 15 sec in an inert ambient to activate all implanted ions. The final constructed structure is shown in Fig. 2.7.

2.5 Characterization and Modeling of Pocket Doping Profile

Characterization is a follow-on activity to model development and implementation. Similarly, design verification is a follow-on activity to the design process and can be viewed as validating models developed and implemented during an earlier design phase. A number of techniques that determine one-dimensional (1-D) doping profiles have been developed and are widely used. Among these are the various capacitance-voltage (C-V) methods [1] and secondary ion mass spectroscopy (SIMS) [85]. But SIMS is destructive and time consuming. Indirect techniques include inverse modelling where a doping profile is found in such a way that its electrical behaviour obtained through numerical simulations, matches with experimental data [86-88]. The use of C-V data to extract 2-D doping profiles has been reported [86-87]. But due to the extremely small dimensions and capacitance of modern submicron devices, special test structures are needed. Noise and parasitic capacitance also become important issues. However, scanning capacitance microscopy (SCM) is a direct technique that can determine the 2-D doping profiles combined with atomic force microscopy (AFM). This is one of the most powerful methods for the characterization of semiconductor devices due to its non-destructive technique and high spatial resolution. Channel length of 0.15 micron MOSFETs were determined directly for the first time using SCM [89].

Present-day VLSI device technology demands accurate knowledge of the spatial extent in three dimensions (3-D) of active impurity dopants which have been incorporated into the discrete device elements. The active region of a MOSFET device is engineered by incorporating dopants, such as, As, B, or P, in a concentration range of 10^{15} to 10^{20} cm^{-3}. In the (2-D) junction regions of a submicron MOSFET device, it is necessary to quantify the variation (or "profile") of these impurity dopants to resolution of 100 nm or less over four orders of magnitude in concentration. Achieving such high precision in the characterization of dopant profiles is a nontrivial task in both the design and manufacturing phases. Thus, it is desirable to have a method capable of measuring dopant profiles in 2-D (or even 3-D) in a straightforward, reliable, and repeatable (nondestructive) fashion. Lateral dopant profiles have been inferred from device capacitance measurements and simulation [90], or from junction-staining [91]. A "tomographic" technique based on a matrix of SlMS measurements has been explored [92]. In this section, we have presented a

technique, using scanning capacitance microscopy (SCM) and its cousin, atomic force microscopy (AFM), which satisfies many of the desired criteria for 2-D and in some sense 3-D, dopant imaging [93, 98]. It is noted that other workers have used scanning tunnelling microscopy (STM) for potentiometry on p-n junctions [95-96].

2.5.1 Characterization of Pocket Doping Profile

Scanning capacitance microscopy (SCM) has been commonly used to image dopant gradients in silicon and other semiconductors. As a mobile, high-resolution (to 2 nm) metal-oxide-semiconductor (MOS) probe, SCM also is a non-destructive, contact less tool with which to examine local variations in dielectric thin film quality and local variations in semiconductor substrate properties. Virtually any measurement that can be made with fabricated metal electrodes can also be made with SCM. In SCM, a small metallic probe, with a radius of curvature at its tip of typically 50 nm, is scanned over a nonuniformly doped sample as depicted in Fig. 2.8. A bias voltage (dc or ac) is placed on the tip, and the local capacitance, C, or its derivative, $\partial C/\partial V$, are then measured as a function of lateral position (x). The measured capacitance or capacitive gradient, as a function of bias voltage, provides a direct measurement of the activated dopant density with high spatial resolution. The inset to Fig. 2.8 represents the simplest equivalent circuit model for the SCM-semiconductor system. This is a series capacitance stack wherein the dopant affects the detected capacitance by virtue of dictating what the local depletion capacitance, C_d, is at lateral scan position, x. C_{air} and C_{ox}, are the capacitances due to the air gap and oxide film, respectively.

Fig. 2.9 is a high level block diagram of the SCM. The central feature of the detection system is the capacitance sensor [97]. This sensor is basically a microwave inductance strip in a resonant circuit. It can measure capacitance variations between the tip and the sample of the order of 10^{-22} F/Hz$^{1/2}$. The tip scan is controlled by a feedback loop which maintains the capacitive signal constant. The piezo-scanners have a 6-mm lateral and 3-mm vertical range. To avoid low-frequency drifts caused by stray capacitances, a vertical dither is placed on the tip/sample spacing typically at 30 KHz. This also provides a means to measure the capacitive gradient.

The ac signal is filtered and rectified by the lock-in amplifier with frequency ω_l as shown in Fig. 2.9. The lock-in amplifier's output is sent to an integrating feedback

loop to maintain the constant ac signal by adjusting the average tip height above the sample. Such a system has achieved 25 nm resolution in topographic mode [98].

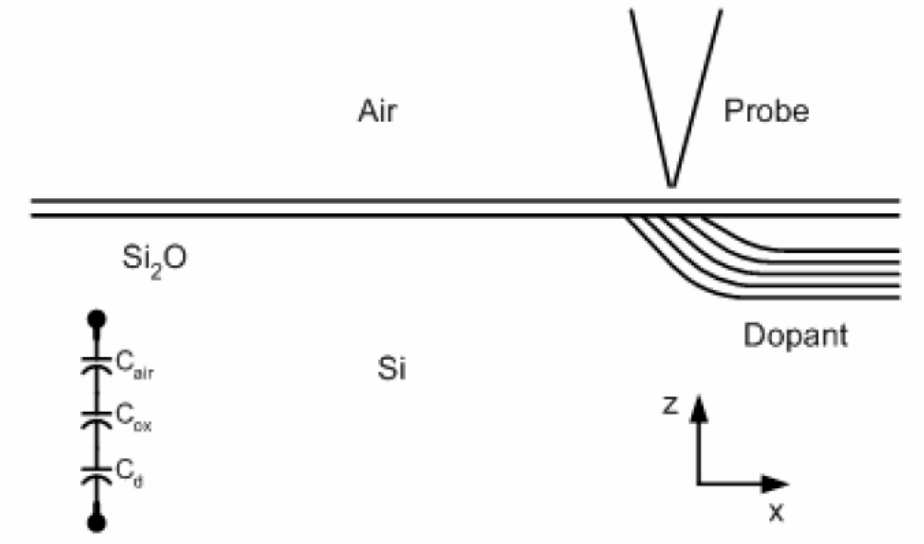

Fig. 2.8 Illustration of the basic concept of scanning capacitance microscopy

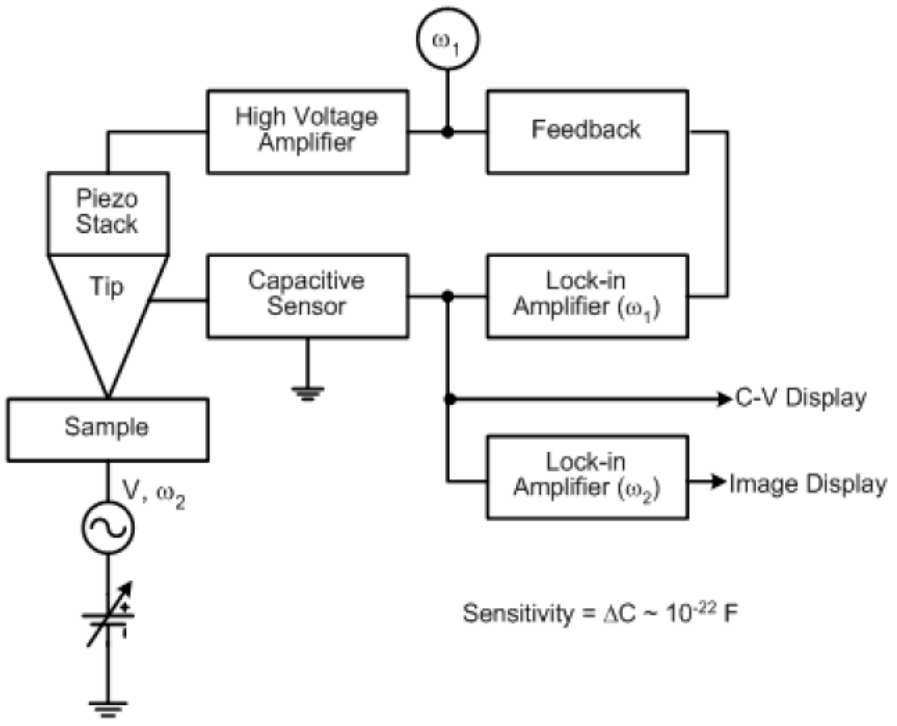

Fig. 2.9 Block diagram of the SCM apparatus with sample at bias voltage, *V*

In the AFM implementation [94], a laser heterodyne detection system is used to measure excursions of a cantilever-style tip which is mechanically oscillated near its resonance. These deviations are directly proportional to tip-to-sample forces,

including the Coulomb force due to mutual capacitance. A signal generator provides an ac and/or dc signal between tip and sample at the desired frequency (ω_2). Thus, a C-V curve can be taken at any given lateral position, or $\partial C/\partial V$ curves at constant dc bias can be acquired as the tip is scanned. Both the tip scan and data acquisition are controlled by a laboratory computer. In either SCM or AFM mode, a separate laser (633 nm) is used as an optical carrier pump to obtain transport data.

2.5.2 Modeling of Pocket Doping Profile

The pocket implanted n-MOSFET structure shown in Fig. 2.10 is considered in this work and assumed co-ordinate system is shown at the right side of the structure. Localized extra dopings are shown by circles near the source and drain side regions.

All the device dimensions are measured from the oxide-silicon interface. In the structure, the junction depth (r_j) is 25 nm. The oxide thickness (t_{ox}) is 2.5 nm, and it is SiO_2 with fixed oxide charge density of 10^{11} cm^{-2}. Uniformly doped p-type Si substrate is used with doping concentration (N_{sub}) of 4.2×10^{17} cm^{-3} with pocket implantation both at the source and drain side with peak pocket doping concentration of 1.5×10^{18} cm^{-3} and pocket lengths from 20 to 30 nm, and source or drain doping concentration of 9.0×10^{20} cm^{-3}.

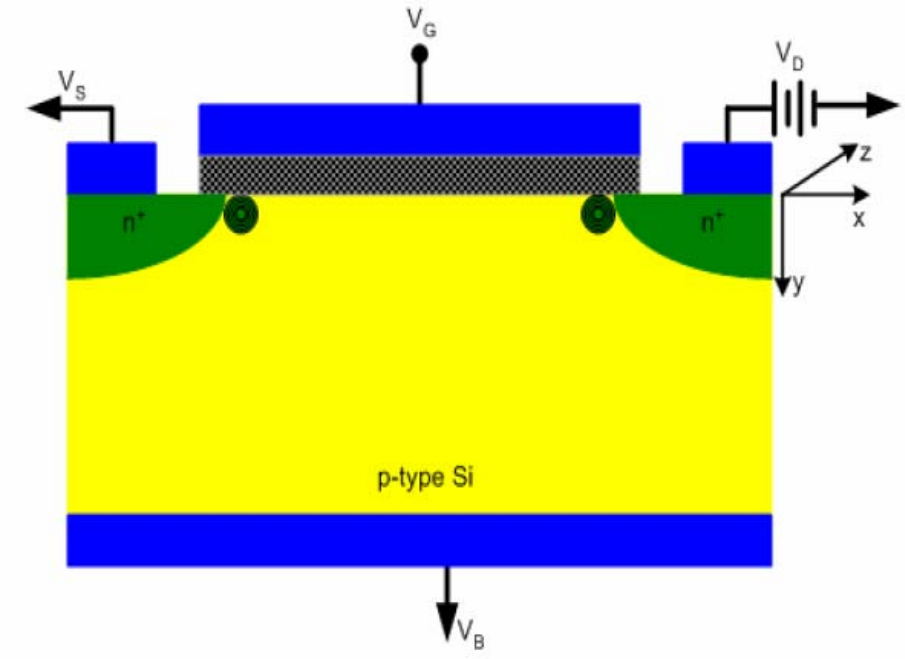

Fig. 2.10 Pocket Implanted n-MOSFET Structure

The model of the conventional bulk n-MOSFET exhibits drastic reduction of the threshold voltage (ΔV_{th}) from the long channel value beyond 100 nm as discussed earlier. This is known as short channel effect. A group of analytical models, known as "charge-sharing" models, are found in the literature to incorporate this effect. But their accuracy is limited [90]. To combat this effect pockets are implanted along the channel in the lateral direction. In [90], a model is presented that solves the two-dimensional Poisson equation analytically, and predicts threshold voltage change (ΔV_{th}) accurately as a function of drain bias (V_D), substrate bias (V_{BS}), channel length (L), oxide thickness (t_{ox}) and substrate concentration (N_{sub}). This model is then transformed to short channel n-MOSFET threshold voltage model assuming the step doping profile along the channel. Few experimental pocket doping profiles are shown in Figs. 3.8-3.10. From these figures, few researchers assume it a step doping profile, while few researchers assume it a Gaussian profile [33]; few researchers thought that it would an exponential profile or hyperbolic cosine profile [48].

This increase in threshold voltage comes from extra doping or fixed oxide charge located near the source and drain. There are various ways to achieve the RSCE. However, in this thesis our objective is to study the pocket implanted n-MOSFET device. Pocket implantation is done by adding extra impurity atoms near the source and drain. This doping profile is then caused to decrease from the source and drain sides towards the centre of the device along the channel. Therefore, accurate modeling of this pocket doping profile has to be found out. In the already published literatures, there are various types of pocket doping profiles. In [33, 46, 71], it is assumed as a step doping profile. Researchers assume it a Gaussian profile in [47]. In [41], Brut et al. picture the RSCE as caused by extra doping of a Gaussian-like shape at the edge of the channel. In [48], the pocket profile is assumed a hyperbolic cosine profile. In [60], the pocket doping profile is an exponential doping profile. In [99], few simulated lateral pocket doping profiles are provided in Fig. 2.9 for different channel lengths after thermal annealing. After examining different pocket doping profiles, in this thesis, it is assumed that the pocket profiles to be linear. This linear profile assumes that the pocket doping decreases linearly from source and drain sides towards the center of the pocket implanted n-type MOS device along the channel. This profile has two important parameters to play vital role, such as, peak of the pocket concentration (N_{pm}) and pocket length (L_p). From these two linear profiles, an effective doping

concentration will be found out and will be used to model the other operational parameters of the MOS device. The two parameters, N_{pm} and L_p, increase the effective doping concentration near the surface at the channel region of the n-MOSFET. This effect can delay threshold voltage roll-off and even threshold voltage rise with the reduction of channel length.

To preserve the long channel threshold voltage behavior for the short channel device, pocket implantation, which causes reverse short channel effect (RSCE), is done by adding acceptor atoms both from the source and drain edges. The peak pocket doping concentration (N_{pm}) gradually decreases towards the substrate level concentration (N_{sub}) with pocket length (L_p) from both the source and drain edges. The basis of the model of the pocket is to assume two laterally linear doping profiles from both the source and drain edges across the channel as shown in Figs. 2.11-2.12 for substrate concentration of 4.2×10^{17} cm^{-3} and channel length of 100 nm.

At the source side, the pocket profile is given as

$$N_s(x) = -\frac{N_{pm} - N_{sub}}{L_p}x + N_{pm}$$

$$\therefore N_s(x) = N_{sub}\frac{x}{L_p} + N_{pm}\left(1 - \frac{1}{L_p}x\right) \qquad (2.13)$$

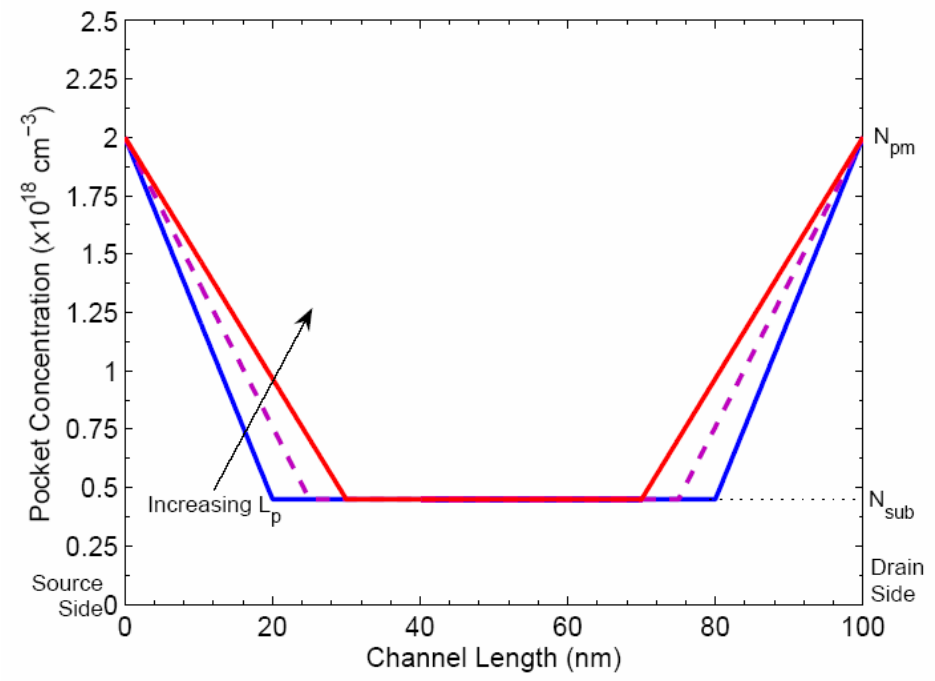

Fig. 2.11 Simulated pocket profiles at the surface for different pocket lengths, L_p = 20, 25 and 30 nm; peak pocket concentration, $N_{pm} = 1.75\times10^{18}$ cm^{-3}

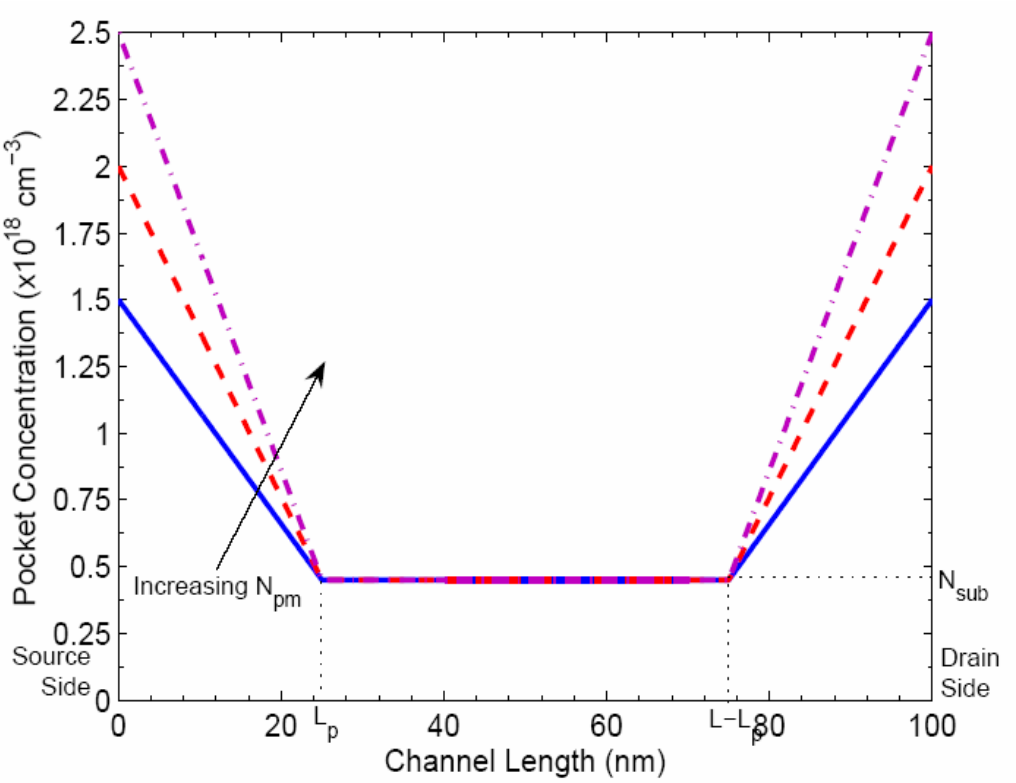

Fig. 2.12 Simulated pocket profiles at the surface for various peak pocket concentrations, N_{pm} = 1.25×10^{18}, 1.5×10^{18} and 1.75×10^{18} cm^{-3} and pocket length, L_p = 25 nm

At the drain side, the pocket profile is given as

$$N_d(x) = \frac{N_{pm} - N_{sub}}{L_p}\left[x - \left(L - L_p\right)\right] + N_{sub}$$

$$\therefore N_d(x) = N_{sub}\left(\frac{L}{L_p} - \frac{1}{L_p}x\right) + N_{pm}\left(1 - \frac{L}{L_p} + \frac{1}{L_p}x\right) \qquad (2.14)$$

,where x represents the distance across the channel.

Since these pile-up profiles are due to the direct pocket implantation at the source and drain sides, the pocket profiles are assumed symmetric at both sides. With these two conceptual pocket profiles of equations (2.13) and (2.14), the profiles are integrated mathematically along the channel length from the source side to the drain side and then the integration result is divided by the channel length (L) to derive an average effective doping concentration (N_{eff}) as shown in equation (2.15).

$$N_{eff} = \frac{1}{L}\int_0^L \left[N_s(x) + N_d(x) + N_{sub}\right]dx \qquad (2.15)$$

Putting the expressions of $N_s(x)$ and $N_d(x)$ from equations (2.13) and (2.14) in equation (2.15) the effective doping concentration is obtained in equation (2.16).

$$N_{eff} = N_{sub}\left(1-\frac{L_p}{L}\right)+\frac{N_{pm}L_p}{L} \qquad (2.16)$$

This effective doping concentration expression will be used in deriving the surface potential model by applying Gauss's law. When $L_p << L$ for long channel device then the pocket profile has very little effect on uniform substrate concentration, but when L_p is comparable with L then the pocket profile parameters affects the substrate doping concentration at the surface of the n-MOSFET. This causes the surface potential to change and hence the threshold voltage (V_T) and hence the other operational parameters of the pocket implanted MOS device due to RSCE.

2.6 Summary

In this chapter, threshold voltage control of the bulk n-MOSFET and short channel effects have been described in this chapter. Then the MATLAB simulation results of the short channel effects are shown. Also, the MATLAB simulation results of combating the short channel effects in the bulk n-MOSFET are provided. After that the formation processes of the pocket structure in the pocket implanted n-MOSFET and characterization and modeling of the pocket profiles of this device have been described. The MATLAB simulation results of the pocket profiles are also shown. In the next chapter, these mathematical pocket doping profile models will be utilized to derive the models of the various operational parameters of the pocket implanted n-MOSFET, such as, surface potential, threshold voltage incorporating bias and temperature effects, inversion layer effective mobility, subthreshold drain current and low frequency drain current flicker noise.

Chapter 3

Modeling Pocket Implanted n-MOSFET

3.1 Introduction

Creating a model for a device creates a framework which allows one to examine a device's reaction to different inputs without actually testing a real device. Additionally, such a framework will often provide greater insight into the device's operation. Any modeling usually starts from a basic theoretical description, focuses on the dominant phenomena, and often translates this into a set of mathematical equations. Given the typical tradeoffs between generality, accuracy, and speed, the types of models for the MOS transistors span a large range. Drawing upon a number of analytic models of the MOSFET, this chapter derives a model in order to examine the effect on device parameters of laterally non-uniform channel doping. This model aims to provide a level of detail in its calculation, beyond that of current models that would be useful for designers or for process engineers trying to evaluate the lateral doping distribution in an n-MOSFET exhibiting RSCE.

Computer simulation is today a standard part of integrated circuit design. During this process, the computer solves a large set of equations describing (1) the connection between the various circuit elements and (2) the models of these elements. Circuits to be simulated can contain a very large number of elements. The models for each element can contain a large number of equations. The behavior of the entire circuit may be needed at many points, e.g. 1000 times points for a transient simulation, and all equations may have to be solved repeatedly for each point, as part of numerical

iterations for solving the implicit equations. Thus some computer simulations are very time consuming. Computing time statistics show that often most of the computing time is spent in evaluating the quantities that are described by the device model equations. It follows, then, that the model equations must be as simple as possible, provided accuracy is not compromised. Over the years, many MOS transistor models for use in computer simulation have been described.

A rigorous way of describing the operation of a transistor is to write the fundamental semiconductor equations in three dimensions. These will be coupled nonlinear partial differential equations, one for each of thousands of finite volume elements in the device. Programs are available for setting up such equations and solving them numerically. Although such programs are invaluable for device (as opposed to circuit) analysis and design, the solution can take a long time even for a single transistor. Such an approach is out of the question for general circuit simulation. Much more efficient models are thus needed, which describe the electrical behavior analytically. These are called compact models, or CAD models. The word 'model' will refer to such compact models. The word technology or process will refer to a given fabrication process. In this chapter, all the analytical models that have been developed for the simulation of pocket implanted n-MOSFET will be described.

3.2 Model Derivation

From reverse engineers' and designers' perspectives, the key criteria of any model are:

1) Realistic doping shapes
2) Reasonably accurate V_{th} vs. L curves
3) Flexibility
4) Rapid calculation
5) Provides insight into connections between input and output parameters

These are the basic guidelines for the derivation of the model. The first part of any derivation is defining the intended focus and range of the model. The focus of this model is to explore the effects of changes in the shape of laterally nonuniform extra doping on MOSFET device output characteristics. As such, simplifications have been made to the device to allow this extra doping to be the focus. To create simple

potential border conditions, the source and drain have been simplified to be abrupt and very deep. This will affect the SCE, but should have limited effect on the rest of the V_{th} vs. L curve. The channel has been simplified to be uniform although because of the use of ion implantation; channels are often modeled as a step function which is higher at the surface, then abruptly lower at some depth. This seemed to add an unnecessary complication since the back bias dependency (the device characteristic that depends most heavily on doping vs. depth) was not being considered. Additionally, the model assumes that the extra doping is just added - it is not removed from somewhere else in the channel. The general form of the extra doping is assumed to be constant with changes in channel length. From a processing standpoint, this assumes that the extra doping distribution originating from the source is unaffected by the drain and vice-versa.

In terms of actual device operation, the model will focus on the subthreshold region of operation. In this region, the doping level is much greater than the inversion charge, so the potential distribution is determined by the doping only. In this region, no lateral electric fields exist in the channel, so only current flowing by diffusion needs to be considered. The gradual channel approximation (GCA), that vertical electric fields vary more quickly than horizontal electric fields, holds in this region and the solution to the vertical and horizontal potentials can be separated. Also, the potential distribution and current flow is assumed to be uniform with width so the problem is reduced to a two-dimensional one. Finally, the depletion approximation is used to give a simple boundary condition in y in the bulk of the devices.

The range of the model encompasses a variety of shapes of the extra doping at the edges. Taking the lead from the general form of diffused profiles (Gaussian or exponential), the profile is assumed to have the shape of a straight line. The equations used to describe this shape were given in chapter 2 and are used equations to derive various models in this chapter.

3.2.1 Surface Potential Model

When gate bias is applied to a pocket implanted n-MOSFET, a negatively charged depletion region is created from the surface to a particular point in the bulk region. Outside this region, the p-type substrate is neutral [1]. The surface potential (ψ_s) is

defined as the total potential drop across the region, defined from the surface to that particular point in the bulk [17].

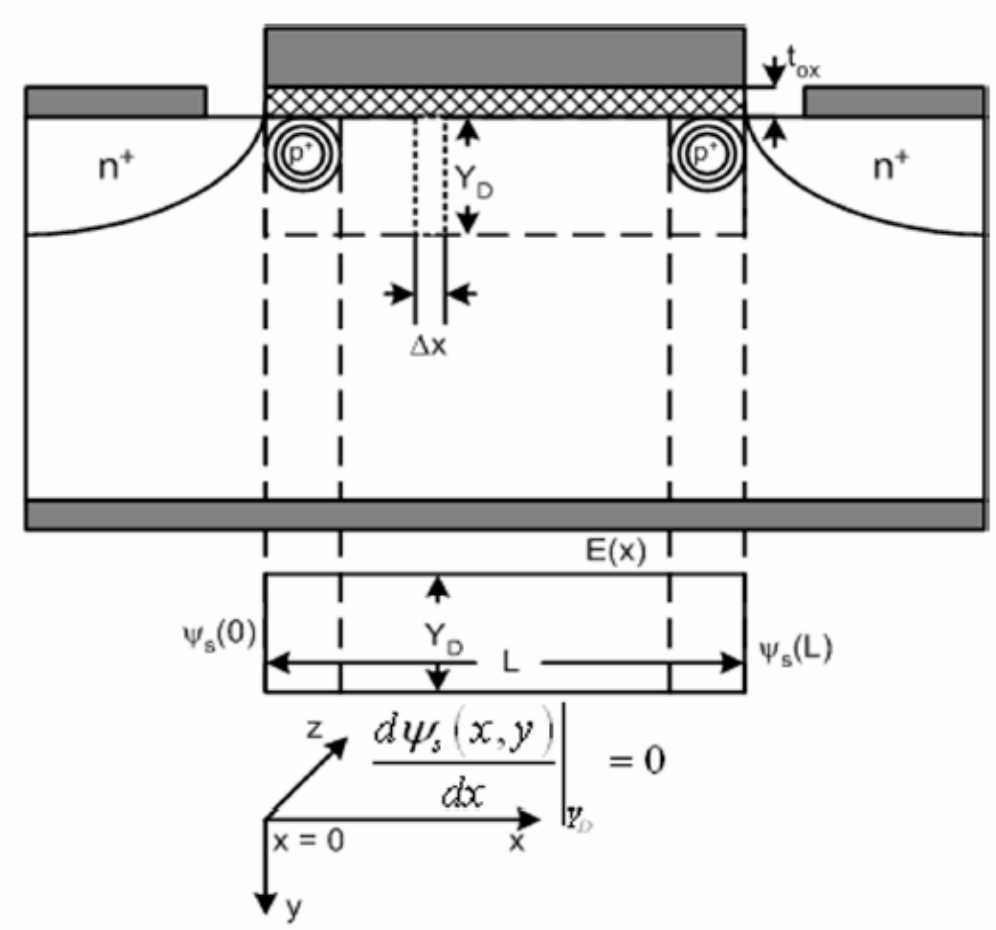

Fig. 3.1 Schematic diagram showing n-MOSFET with p+ pocket implant regions (upper figure) and Gaussian box; detailed Gaussian box with boundary conditions (lower figure) to get the surface potential model

In order to model the surface potential of the depletion region under the gate, a rectangular box is assumed, called Gaussian box, as shown in Fig. 3.1 for applying Gauss's law [100]. This box has length L, width W and height Y_D, which is actually the depletion layer width in the y-direction. Since the electric field is different from the top surface where gate voltage is applied and the lateral surface where drain voltage is applied, it is needed to calculate the electric flux flowing into the Gaussian box from these two surfaces. But the electric field is non-uniform in the lateral direction due to the potential differences between the drain and the source. So, it is assumed an infinitesimal element of the rectangular box (Gaussian box) at an arbitrary

point x of length Δx, width W and height Y_D as shown in Fig. 3.1 [33]. At first, it is required to calculate the electric flux coming from the top surface. To do this, equation (3.1) is written by applying Kirchoff's Voltage Law (KVL) for the voltage across the oxide layer at any point x along the channel by incorporating the effect of substrate bias and neglecting the charges of mobile carriers.

$$V_{ox} = V_{GS} - V_{BS} - V_{FB} - \psi_s(x) \tag{3.1}$$

,where V_{GS}, V_{BS}, V_{FB} and $\psi_s(x)$ are the gate bias voltage, substrate bias voltage, flat band voltage and surface potential at any point x respectively.

Since the flux is evaluated by multiplying the electric field and the cross-sectional area through which the electric field lines pass [100], the electric flux (Φ_{top}) coming from the top surface towards the rectangular Gaussian box of Fig. 3.1 can be written using equation (3.1) as shown in equation (3.2).

$$\Phi_{top} = \frac{V_{GS} - V_{BS} - V_{FB} - \psi_s(x)}{t_{ox}} W \Delta x \tag{3.2}$$

,where t_{ox} is the oxide thickness.

In the infinitesimal box, at point x the electric field is E and at $x+\Delta x$, the electric field is $E + \Delta E$. So, the net electric field passing through the infinitesimal box along the x-direction is ΔE. Therefore, the lateral electric flux, ($\Phi_{lateral}$) coming from the lateral surface towards the box can be written as shown in equation (3.3).

$$\Phi_{lateral} = \Delta E \frac{Y_D}{\eta} W \tag{4.3}$$

,where η is the fitting parameter. It is used here to take the non-uniformity of the lateral electric field across the channel into account. The value of η varies from 1 to 1.3 [101], and it is assumed 1 everywhere in this work. The meaning and quantification of η is discussed in [102].

The depletion layer thickness, Y_D can be obtained by solving the Poisson's equation at the depletion region at the onset of the inversion condition (i.e., when the minimum surface potential becomes equal to the inversion condition creation), $\psi_{s,min} = 2\varphi_F$ [17], as shown in equation (3.4).

$$Y_D = \sqrt{\frac{2\varepsilon_{Si}(\varphi_F - V_{BS})}{qN_{eff}}} \tag{3.4}$$

,where φ_F is called the Fermi potential due to pocket implantation as well as substrate doping concentration and is given by equation (3.5).

$$\varphi_F = \frac{kT}{q}\ln\frac{N_{eff}}{n_i} \tag{3.5}$$

,where k, T and q are the Boltzmann constant, absolute temperature and electronic charge respectively.

In this work, η is assumed constant. In fact, it is a function of the drain voltage and channel length [103], [104]. Now, if Gauss' law is applied to this infinitesimal Gaussian box then it can written as

$$\varepsilon_{Si}\Phi_{lateral} + \varepsilon_{ox}\Phi_{top} = Q_{enclosed} \tag{3.6}$$

,where ε_{Si} and ε_{ox} are the dielectric permittivity of Si and oxide respectively and $Q_{enclosed}$ is the charge enclosed by the infinitesimal Gaussian box.

Putting the expressions of equations (3.2) and (3.3) in to equation (3.6), equation (3.7) can be written as

$$\varepsilon_{Si}\Delta E\frac{Y_D}{\eta}W + \varepsilon_{ox}\frac{V_{GS}-V_{BS}-V_{FB}-\psi_s(x)}{t_{ox}}W\Delta x = qN_{ch}(x)WY_D\Delta x \tag{3.7}$$

,where $N_{ch}(x)$ is the doping concentration along the channel including pocket regions.

Dividing equation (3.7) by $W\Delta x$ and rearranging, equation (3.7) can be written as

$$\varepsilon_{Si}\frac{Y_D}{\eta}\frac{\Delta E}{\Delta x} + \varepsilon_{ox}\frac{V_{GS}-V_{BS}-V_{FB}-\psi_s(x)}{t_{ox}} = qN_{ch}(x)Y_D \tag{3.8}$$

In the limit $\Delta x \to 0$, equation (3.8) can be written as

$$\varepsilon_{Si}\frac{X_D}{\eta}\frac{dE}{dx} + \varepsilon_{ox}\frac{V_{GS}-V_{BS}-V_{FB}-\psi_s(x)}{t_{ox}} = qN_{ch}(x)X_D \tag{4.1}$$

The first term in the left hand side of the differential equation (3.9) is equal to the net electric flux entering the Gaussian box along the channel, i.e. in the x-direction. The second term represents the electric flux entering the top surface of the Gaussian box. There is no electric flux passing through the bottom of the Gaussian box. Although η is a function of the drain voltage, it is a second-order effect as explained in [105]. This quasi-two-dimensional approximation simplifies the solution of the differential equation (3.9) retaining the accuracy. Therefore, η is treated as a constant for a given technology. The depletion layer thickness, Y_D is also assumed constant. Since the effects of the variation of the lateral field in the depletion layer under the channel are incorporated through this fitting parameter η [102], [106], one may treat the term Y_D/η in equation (3.3) as an average of the depletion layer thickness along the channel. The lateral electric field is given in equation (3.10).

$$E = \frac{d\psi_s(x)}{dx} \tag{3.10}$$

From Fig. 3.1, it is obvious that the lateral channel doping, $N_{ch}(x)$ is non-uniform and the channel is divided into three regions. In the pocket implanted regions, the channel doping expressions, $N_{ch}(x)$ will be the source and drain doping concentration expressions as given in the equations (2.13) and (2.14) of chapter 2. In the central part of the channel region, $N_{ch}(x)$ will be the substrate doping concentration, N_{sub}, which is constant. But in that case the solution of the differential equation will be difficult. Therefore, in equation (3.9), the effective doping concentration, N_{eff} given in equation (2.16) of chapter 2 is used. Using equations (3.9) and (3.10), the second order differential equation (3.11) can be written as

$$\varepsilon_{Si}\frac{X_D}{\eta}\frac{d^2\psi_s(x)}{dx^2} + \varepsilon_{ox}\frac{V_{GS} - V_{BS} - V_{FB} - \psi_s(x)}{t_{ox}} = qN_{eff}X_D \tag{3.11}$$

Now the following boundary conditions are assumed

1. At $x = 0$, i.e. at the source side, the surface potential is $\psi_s(0) = \varphi_{bi} - V_{BS}$.

2. At $x = L$, i.e. at the drain end, the surface potential is $\psi_s(L) = \varphi_{bi} - V_{BS} + V_{DS}$.

,where φ_{bi} is the built-in potential given by the equation (3.12).

$$\varphi_{bi} = \frac{kT}{q}\ln\frac{N_{sd}N_{pm}}{n_i^2} \tag{3.12}$$

,where N_{sd} is the source or drain doping concentration and n_i is the intrinsic carrier concentration of Si.

After solving the 2nd order differential equation of (3.11) using the above two boundary conditions the desired complete analytical expression for the surface potential expression as given in equation (3.13) is obtained by finding the transient solution and the particular integral using the conventional differential equation solution techniques and then adding the two solutions together.

$$\psi_s(x) = \frac{c_1}{\sinh\sqrt{\frac{a_0}{a_2}}L}\sinh\sqrt{\frac{a_0}{a_2}}(L-x) + \frac{c_1 + V_{DS}}{\sinh\sqrt{\frac{a_0}{a_2}}L}\sinh\sqrt{\frac{a_0}{a_2}}x - \frac{b_1}{a_0} \tag{3.13}$$

,where the parameters a_0, a_2, b_1 and c_1 are given by the equations (3.14)-(3.17).

$$a_0 = \frac{\varepsilon_{ox}}{t_{ox}} \tag{3.14}$$

$$a_2 = \frac{\varepsilon_s}{\eta} X_D \tag{3.15}$$

$$b_1 = qN_{eff} X_D - \frac{\varepsilon_{ox}}{t_{ox}}\left(V_{GS} - V_{BS} - V_{FB}\right) \tag{3.16}$$

$$c_1 = \varphi_{bi} - V_{BS} + \frac{b_1}{a_0} \tag{3.17}$$

3.2.2 Threshold Voltage Model

Threshold voltage (V_{th}) is one of those mostly used parameters in analog and digital circuit design and simulations, thus a computation effective expression of V_{th} is desirable. Otherwise, proper functioning of the circuits is not possible. The term threshold voltage has different meanings in the literatures [17]. In this work, threshold voltage is defined as the gate voltage required to just start the moderate inversion. Since the doping concentration is non-uniform along the channel due to pocket implantation, for accurate determination of the threshold voltage requires numerical simulations. But this is computation intensive and time consuming. Therefore, in this work, an analytical threshold voltage model of the pocket implanted n-MOSFET is proposed. It has two parts. One part incorporates the gate, drain and substrate bias effects and the other part incorporates the temperature effects. These two parts are described in the following two subsections.

Bias effects

In [49], the threshold voltage model was obtained by solving the 1-D Poisson equation and then applying Gauss's law, but that model did not incorporate the effect of substrate and drain biases. The threshold voltage model derived in [80] incorporated the effects of substrate and drain biases on threshold voltage for vertically non-uniform doping profile. Based on that concept, we derived a threshold voltage model for our proposed pocket doping profile along the channel. This model incorporates the effective doping concentration of our linear pocket profiles given in equation (2.16) to derive the threshold voltage equations and hence we obtain the V_{th} expression as given in equation (3.18).

$$V_{th} = V_{th,L} + \gamma_B \left[\frac{N_{sub}}{N_{eff}} (2\varphi_F) - V_{BS} \right]^{\frac{1}{2}} - \gamma_A \frac{N_{sub}}{N_{eff}} (2\varphi_F)^{\frac{1}{2}} - \frac{6t_{ox}}{d_1} \left[2(\varphi_{bi} - V_{BS}) + V_{DS} \right] \exp\left(-\frac{\pi L}{4d_1} \right) \quad (3.18)$$

,where $V_{th,L}$ is the long channel threshold voltage for the pocket implanted n-MOSFET and φ_{bi} is the built-in potential and are given by the equations (3.19) and (3.12) respectively. The second and the third parts include the threshold voltage due to the effects of both substrate bias and effective doping concentration. The fourth part incorporates the drain and substrate bias effects and the short channel effects.

$$V_{th,L} = V_{FB} + 2\varphi_F + \gamma_A (2\varphi_F)^{\frac{1}{2}} \quad (3.19)$$

,where V_{FB} is the flat band voltage. From simulation it is found as -0.9316V. φ_F, γ_A and γ_B are Fermi potential due to pocket implantation, threshold sensitivity due to back bias for effective doping concentration along the channel and body factor corresponding to bulk doping respectively. γ_A and γ_B are given in equations (3.20)-(3.21), while φ_F is given in equation (3.5).

$$\gamma_A = \frac{(2q\varepsilon_{Si} N_{eff})^{\frac{1}{2}}}{C_{ox}} \quad (3.20)$$

$$\gamma_B = \frac{(2q\varepsilon_{Si} N_{sub})^{\frac{1}{2}}}{C_{ox}} \quad (3.21)$$

The depth (where band bending of $2\varphi_F$ occurs) of the pocket doping vertical to the channel and the built-in potential at the source or drain to channel junction are given by the equations (4.14) and (4.15) respectively.

$$d_1 = \left(\frac{2\varepsilon_{Si}}{qN_{eff}} \right)^{\frac{1}{2}} (2\varphi_F)^{\frac{1}{2}} \quad (3.22)$$

Temperature effects

It is well known that a change in the operating temperature of a device affects its characteristics and hence the circuit performance. Accurate description of the temperature effects in devices is necessary to predict circuit behavior over a range of temperatures. Threshold voltage is the most significant parameter in the study of temperature dependence of any MOS device characteristics. Because MOS device *I-V*

characteristics are proportional to the square of the difference of gate voltage and threshold voltage. Thus a small change in threshold voltage causes a large change in the output current. Therefore, it is necessary to calculate the threshold voltage accurately with temperature changes. There are many material parameters that are related to the calculation of the threshold voltage, and a number of empirical relationships have been obtained from the experimental data [107].

To incorporate the effects of temperature on reverse short channel effects in the pocket implanted n-MOSFET, all the parameters that depend on the temperature are modeled. These parameters are the intrinsic carrier concentration of Si (n_i), effective density of states in the conduction band (E_c) and valence band (E_v) (N_C and N_V respectively), the energy band gap of Si (E_g), the metal-semiconductor work function difference (φ_{MS}), flat-band voltage (V_{FB}) and the fixed oxide charge density (Q_f) and are given in equations (3.23-3.28).

$$n_i = \sqrt{N_C N_V}\, e^{\frac{-qE_g}{2kT}} \tag{3.23}$$

$$N_C = 1.73\times10^{16} T^{\frac{3}{2}} \tag{3.24}$$

$$N_V = 4.8\times10^{15} T^{\frac{3}{2}} \tag{3.25}$$

$$E_g = E_{g0} - \frac{\alpha T^2}{T+\beta} \tag{3.26}$$

$$\varphi_{MS} = -\frac{E_g}{2} - \varphi_F \tag{3.27}$$

$$V_{FB} = \varphi_{MS} - \frac{Q_f}{C_{ox}} \tag{3.28}$$

A simple band diagram of a MOS structure is considered to understand these temperature dependent parameters as shown in Fig. 3.2. These parameters are then used in the threshold voltage model of equation (3.18) to study the temperature effects on RSCE. The intrinsic carrier concentration of Si (n_i), given in equation (3.23), depends on temperature (T) as well as effective density of states N_C and N_V in the conduction band (E_c) and valence band (E_v) respectively. N_C and N_C given by equations (3.24) and (3.25) respectively are also dependent on temperature. The energy band gap of Si, E_g is a function of the absolute temperature (T) as in equation (3.26), where E_{g0} is the band gap energy at room temperature, α and β are the empirical constants. The metal-semiconductor work function difference (φ_{MS}), given

in equation (3.27) depends on the energy band gap and the Fermi potential. This, in turn, causes the φ_{MS} to vary with temperature. Flat-band voltage, V_{FB} given in equation (3.28) is also temperature dependent as it is a function of (φ_{MS}),. The threshold voltage model presented in equation (3.18) are function of all these temperature dependent parameters and thus this model will be used to study the behavior of temperature sensitivity of the threshold voltage for the pocket implanted n-MOSFET.

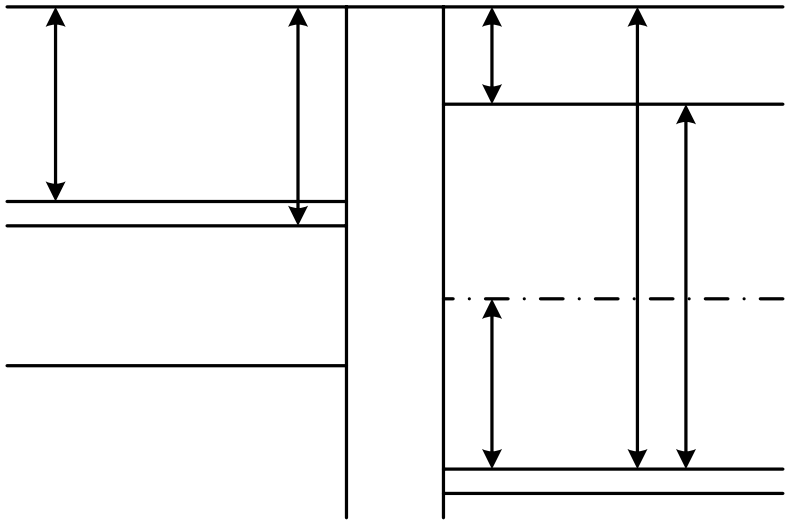

Fig. 3.2 Band diagram of metal oxide semiconductor structure [108]

3.2.3 Inversion Layer Effective Mobility Model

The inversion layer mobility in Si MOSFET's has been a very important physical quantity as a parameter to describe the drain current and a probe to study the electric properties of a two-dimensional carrier system. It has been shown that the effective mobility strongly depends on the effective surface electric field. With the increase of surface electric field the effective mobility degrades. This is generally attributed to the increased impurity scattering of the electrons. If this condition is full-filled then one can observe the influence of the changes in the doping concentration on the mobility. The potential well at the surface depends upon the electric field normal to the surface. The surface electric field is given by the Gauss's law as in equation (3.29) [66].

$$E_s = \frac{1}{\varepsilon_{Si}}\left(Q_{dep} + Q_{inv}\right) \tag{3.29}$$

,where ε_{Si} is the permittivity of Si, Q_{dep} is the surface depletion charge per unit area, Q_{inv} is the surface inversion carrier charge per unit area.

At the onset of strong inversion, assuming Q_{inv} = 0, the surface field is determined mainly by the Q_{dep} term in equation (3.29). Therefore, if two devices with different surface doping concentrations were biased appropriately to have the same Q_{dep}, it would imply that the E_s in both the devices would be the same. This further implies that the surface potential well in both would be identical. But the inversion layer mobility depends only on the shape of the surface potential well and not on the surface doping concentration. The mobility decreases with increasing magnitude of Q_{dep}. Additionally, it can be implied that, for a given device, the magnitude of Q_{dep}, increases with the increase in the magnitude of V_{BS}, and therefore the inversion layer electron mobility should decrease with V_{BS}. Therefore, to incorporate this effect, the electron potential energy diagram shown in Fig. 3.3 [66] is considered.

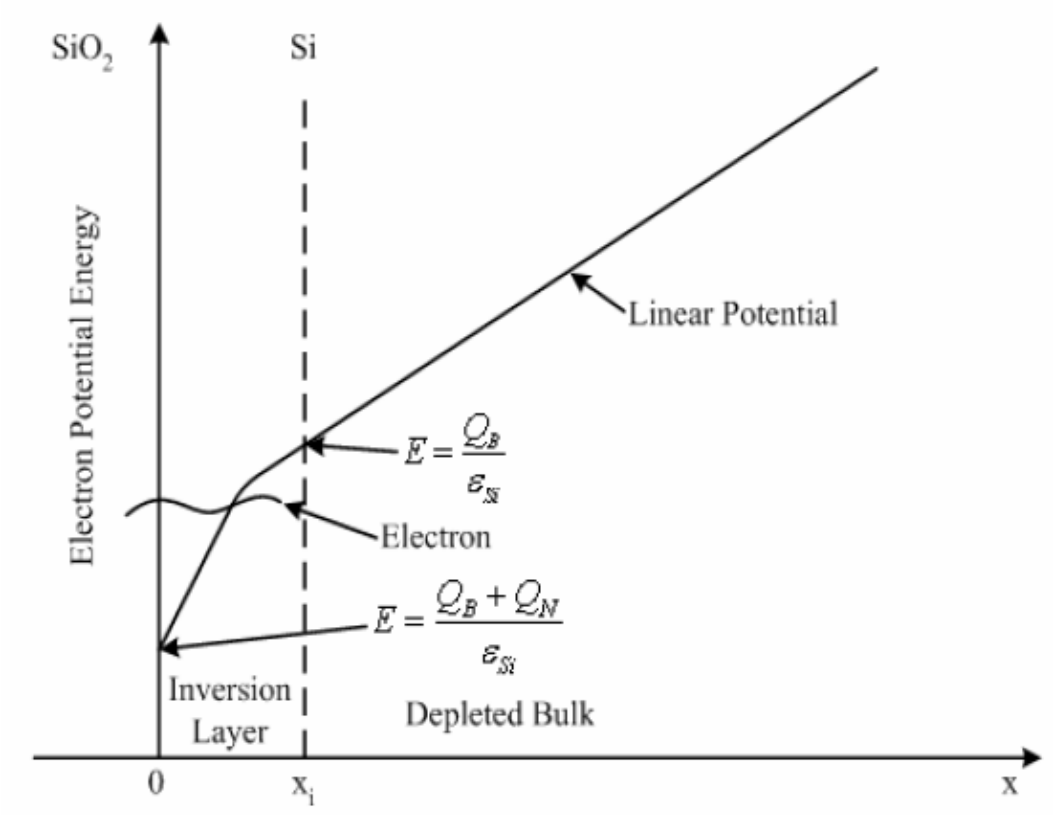

Fig. 3.3 Electron potential energy diagram [66]

The inversion layer thickness is generally much smaller than that in the depletion region. The electric field experienced by an electron at the surface is due to the depletion layer and inversion layer charge, whereas the electric field experienced by an electron at $x = x_i$ is only due to Q_{dep}. In general, the electric field at any point y, ($0 < y < y_i$) can be expressed as in equation (3.30).

$$E(x) = \frac{Q_{dep}}{\varepsilon_{Si}} + \frac{q}{\varepsilon_{Si}} \int_{y}^{y_i} n(x) dx \qquad (3.30)$$

,where q is the charge of an electron, x is a dummy variable, $n(x)$ is the density of the inversion layer electrons along an axis normal to the surface and y_i, the edge of the inversion layer, can be taken as the value of y at which the intrinsic and the extrinsic Fermi levels intersect.

When the electric field of equation (3.30) is averaged over the electron distribution in the inversion layer, an effective electric field expression is obtained and is known as the universal mobility model [66], where the effective normal electric field, E_{eff} is defined by equation (3.31).

$$E_{eff} = \frac{1}{\varepsilon_{Si}} \left(Q_{dep} + \eta Q_{inv} \right) \qquad (3.31)$$

In order to provide the universal relationship (i.e. the substrate bias and substrate concentration independence of effective mobility vs. effective normal electric field curve), the value of η should taken to be 1/2 for the electron mobility [66] and 1/3 for the hole mobility [109]. This relationship has been often utilized as a precise mobility model in device simulators [110, 111]. The depletion charge in equation (3.31) can be determined by the threshold voltage equation and the inversion layer change can be determined from $Q_{inv} = C_{ox} \left(V_{gs} - V_{th} \right)$. Thus equation (3.31) can be transformed in to equation (3.32).

$$E_{eff} = \frac{C_{ox}}{\varepsilon_{Si}} \left(\eta \left(V_{GS} - V_{th} \right) + V_{th} - V_{FB} - 2\psi_{s.inv} \right) \qquad (3.32)$$

,where V_{GS} is the gate voltage and V_{th} is the threshold voltage of the pocket implanted n-MOSFET obtained from equation (3.18), V_{FB} is the flat band voltage obtained from equation (3.28) and C_{ox} is the oxide capacitance per unit area.

There has been much study on effective mobility [61] since the 1960's. This has revealed that the dominant scattering mechanisms determine the mobility. The three most relevant scattering processes in MOSFET devices are the (screened) Coulomb

scattering, the phonon scattering and the surface roughness scattering through which the electrons exchange momentum and kinetic energy with their environment. Phonon scattering mechanisms is due to the energy quanta called 'phonons' of lattice vibrations. In a MOS transistor, electrons in the inversion layer flow near the semiconductor-oxide interface (i.e. the surface of the semiconductor). The electric field component perpendicular to the direction current flow, referred to as normal component tends to accelerate the inversion layer electrons toward the surface and subjects them to additional scattering. Now there is Coulomb scattering not only due to ionized impurity atoms, but also due to interface trapped charges and the fixed oxide charges. The inversion layer charge itself, if it is significant, tends to partly screen itself from the effects of the Coulomb scattering. Additional scattering occurs due to surface roughness. All these tend to lower the mobility of electrons in the inversion layer to values smaller than the bulk mobility. Based on these scattering processes three mobility models are derived for the pocket implanted MOSFET. Each of these three terms has been modeled analytically as functions of the variables N_{eff} (effective channel dopant density for the pocket implantation case), N_{inv} (inversion layer electron density), and T (temperature).

A. *Coulomb scattering mobility model*

The Coulomb term has been extensively studied based on the Boltzmann transport equation [112]. However, in order to get an analytical solution, an excessively large number of approximations are required and therefore these works cannot help in building up a closed form formula for modeling purposes. Generally speaking, we are looking for a formula that should highlight the main functional dependencies, while minor details should be accounted for by tailoring a few fitting parameters.

It is well known that the mobility due to the unscreened Coulomb potential linearly increases with the average carrier energy. Denoting with μ_0 the unscreened mobility per each scattering center per unit area, we may write $\mu_0 = AkT$, where the factor A will be considered as a fitting parameter. Theoretical analyses, such as the one reported in [113], point out that the electrons in a quantized state scatter mostly with the charged centers located within a thermal length, $L_{th} = \hbar / \sqrt{(2kTm_{n,eff})}$ (with $m_{n,eff}$ being the effective mass for electron) from the Si/SiO_2 interface. Therefore, by calling N_{eff} the channel dopant density per unit volume and N_{int} the interface charged states per unit area, equation (3.33) may be written.

$$\mu_C = \frac{\mu_0}{N_{\text{int}}\alpha + N_{eff} L_{th}} \tag{3.33}$$

The denominator of equation (3.33) can be regarded as the effective number of Coulomb scatterers per unit area. The coefficient α is proportional to the square of the electron wave function at the interface [113]. Numerical calculations show that α typically assumes values of the order of some 10^{-2}, while $N_{eff}L_{th}$ is higher than 10^{11} cm^{-2}. Therefore oxide charge scattering can be safely neglected provided that the density of interface charges is well below 10^{12} states cm^{-2}. In the following, we will assume $N_{int} = 0$.

In most of the operating bias range the electron density ranges from 10^{12} cm^{-2} to 10^{13} cm^{-2}, and the scattering potentials are significantly screened by free carriers. This effect makes the Coulomb mobility increase with the electron density and it is responsible for the mobility rise just above threshold. Three theoretical aspects must be remembered at this stage.

1) Screening is usually accounted for by replacing the semiconductor dielectric constant, ε_{Si}, with a dielectric function dependent on the momentum exchanged by the carrier in the scattering event.

2) To the first order the mobility is dependent on the scattering rate of the electrons at the average thermal energy kT. At room temperature, these carriers have a "thermal length" (i.e., the inverse of the electron wave vector), $L_{th} \simeq 2.5$ nm . It follows that the average dielectric constant entering the Coulomb scattering potential is given by equation (3.34).

$$\varepsilon = \varepsilon_{Si}\left(1 + \frac{L_{th}}{L_s}\right) \tag{3.34}$$

,where L_s is the so called screening length.

Since mobility is inversely proportional to the square of the scattering potential, that is proportional to the square of the average dielectric constant, we expect that (3.33) may account for screening when modified as in equation (3.35).

$$\mu_C = \frac{\mu_0}{N_{eff} L_{th}}\left(1 + \frac{L_{th}}{L_s}\right)^2 \tag{3.35}$$

3) When the electron density, N_{inv} gets higher than 10^{12} cm^{-2}, some electron states become fully occupied. The degeneracy of the electron gas affects both the value of

the screening length and the value of the average electron energy. In a nondegenerate electron gas the screening length L_s is the Debye–Huckel value $L_{DH} = (2\varepsilon kT)/(qQ_{inv})$, while in the fully degenerate case L_s is equal to the Thomas–Fermi value $L_{TF} = (\pi\hbar^2\varepsilon_{Si})/(q^2 m_{n,eff})$. Between these two extremes, the screening length may be derived from a detailed calculation based on the Random Phase Approximation (RPA). The analytical expression of the effective screening length that has the dependence on the carrier density is given by $L_s = \sqrt{L_{TF}^{\ 2} + L_{DH}^{\ 2}}$.

Since the accuracy of the above formula is very good, it has been used in the model to account for the dependence of on carrier density.

Degeneracy also increases the average electron momentum and the corresponding kinetic energy. This effect has impact on both and the carrier wavelength at the average energy. It may be accounted for by introducing a suitable degeneracy factor in order to write the average electron energy as F^2kT, thus replacing $\mu_0 = AkT$ with a value of $\mu_0 F^2$. Correspondingly, the thermal length, L_{th} in the screening term is replaced by a shorter effective length L_{th}/F. From a comparison with the numerical calculation of the Coulomb mobility we have found that a good analytical approximation for the factor F is the ratio between the Debye-Huckel and the effective screening length, i.e. $F = L_s/L_{DH}$. By inserting these corrections, equation (3.35) can be transformed in to a formula for the Coulomb limited mobility model modified for the pocket implanted n-MOSFET incorporating effective pocket doping concentration from equation (2.16) and is given in equation (3.36).

$$\mu_{cb} = \mu_0 \frac{L_s}{N_{eff} L_{th} L_{DH}} \left(1 + \frac{L_{th}}{L_s}\right)^2 \qquad (3.36)$$

The approximation made in this equation is correct at both low electron densities where $F \simeq 1$ and at high electron densities where $F \gg 1$ but at the same time $\frac{L_{th}}{L_s} \gg 1$ so that the screening factor in parentheses scales as F^{-1}.

B. *Phonon scattering mobility model*

The most commonly used expression of the phonon scattering mobility term, μ_{ph} is the one derived by Schwarz and Russek [114] as given in equation (3.37).

$$\mu_{ph} = \left(\frac{AT}{E_{eff}} + \frac{B}{E_{eff}^{1/3}}\right)\frac{1}{T} \qquad (3.37)$$

By tailoring the fitting parameters A and B, the expression holds for all quantization regimes [115]. In the so-called electrical quantum limit [116], when all channel electrons lie in the lowest quantized subband, the coefficient A vanishes and the formula correctly reduces to the one reported in [117].

Equation (3.37) accounts only for scattering from intravalley acoustic phonons resulting in a T^{1} temperature dependence. On the other hand, experiments suggest a $T^{1.8}$ power law [62]. This discrepancy is due to the nonnegligible role of phonon scattering from intervalley modes, which have stronger temperature dependence. On the other hand, some physically based expressions, such as the one of Masaki et al., are cumbersome and with many fitting parameters (i.e., the deformation potential and the energy of each phonon mode).

Gamiz et al. [118] have shown that the phonon limited mobility may be approximated by equation (3.38) taking the temperature influence into account.

$$\mu_{ph} = \mu_{phB}\left[\left(\frac{T}{T_0}\right)^{n} + \left(\frac{T}{T_0}\right)^{r}\left(\frac{E_{eff}}{E_0}\right)^{\alpha(T)}\right]^{-1} \qquad (3.38)$$

,where μ_{phB}(300K) = 1470 cm^2/V-sec is the phonon limited bulk mobility, n = 2.109, r = 1.7, $E_0 = 7\times10^4$ V/cm and $\alpha(T) = 0.2\left(T/T_0\right)^{-0.1}$ with T_0 is another fitting parameter or base temperature taken as 300K.

Equation (3.38) was derived from a detailed Monte Carlo analysis of phonon scattering in quantized inversion layers and thus it may be regarded as the one reproducing the most recent theoretical results. In this work, equation (3.38) is just modified with the effective field expressions derived in equation (3.32) for the pocket implanted n-MOSFET.

C. *Surface roughness scattering mobility model*

The Si-SiO_2 interface is not ideally flat, but shows irregularities with a typical amplitude of one or two atomic layers. Scattering by this potential fluctuations degrades the carrier mobility at high effective fields. A detailed TEM analysis of the interface between Si and a thermally grown oxide was performed by Goodnick and coworkers [119] and their results have been taken as a reference in many following theoretical and numerical works. In their study, the roughness of the Si-SiO_2 interface appeared to be characterized by an r.m.s. displacement of about 0.2 nm and a

correlation length of about 1.3 nm, that is, about half the electron thermal length at room temperature. This means that on the spatial scale of the carrier wavelength, the surface potential appears almost uncorrelated, thus featuring an almost constant power spectrum. As long as this condition holds, the surface roughness mobility is inversely proportional to the square of the effective electric field as given in equation (3.39) [115], [120]..

$$\mu_{sr} = \delta E_{eff}^{-2} \tag{3.39}$$

But this formula neglects the effects of carrier scattering, which is responsible for a weak temperature dependence of this term. In fact, as the temperature increases, the screening of the scattering potential weakens and the mobility decreases. We have accounted for the effect by modifying the term, δ according to the equation (3.40).

$$\mu_{sr} = \delta e^{-\left(\frac{T}{T_0}\right)^2} E_{eff}^{-\gamma} \tag{3.40}$$

,where δ and γ are fitting parameters depending on the quality of the Si-SiO_2 interface. However, in this work, $\delta = 8.8\times10^{14}$ V/sec and $\gamma = 2$ are used.

The equivalent mobility (μ_{eqv}) is the overall mobility of the channel incorporating all scattering mechanisms combined by the Matthiessen's rule [1] as in equation (3.41).

$$\frac{1}{\mu_{eqv}} = \frac{1}{\mu_{cb}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \tag{3.41}$$

The curve of equivalent mobility versus effective normal electric field follows the universal relationship [62, 121].

D. *Ballistic mobility model*

The effective electron mobility in short channel (nano scaled) MOSFETs must be much smaller than the electron mobility in long channel devices. This reduction was predicted for ballistic devices in [122]–[124]. Equivalent mobility (μ_{eqv}) determined in this way is not applicable for nano scale MOSFET. If the nano scale device physics is not considered in the mobility curve, the mobility is termed as the ballistic or apparent mobility [125]. The physical reasons for a drastic mobility reduction are related to the ballistic motion first predicted in 1979 [126], [127]. In ballistic field effect transistors, electrons travel from the source to the drain ideally without any collisions with impurities or phonons. Electrons propagate in the device channel with a randomly oriented thermal velocity, v_{th}, (or with a Fermi velocity, v_F, for a degenerate electron gas) and, hence, have only a limited time to accelerate in the electric field and acquire

a drift velocity. Their transit time is determined by L/v_{th}, where L is the device length, (or by L/v_F in a degenerate case). As a result, in low electric fields, the current is proportional to the electric field and to the electron concentration, just like in the collision-dominated case. Therefore, for MOSFETs with nano scale channel lengths, the mobility thus obtained has to be modified. It has been observed that the mobility extracted from electrical characteristics decreases with the shrinking of the channel length (L). The equivalent mobility determined by equation (3.41) is said to be apparent mobility. The electron mobility has to be substituted by a parameter that we call ballistic mobility [122, 123, 128], which (for a non-degenerate electron gas) is given by equation (3.42) [123].

$$\mu_{bal} = \frac{2qL}{\pi m_{n,eff} v_{th}} \tag{3.42}$$

,where v_{th} is the average thermal velocity of the electron in the channel and is given by equation (3.43) [125].

$$v_{th} = \sqrt{\frac{8kT}{\pi m_{n,eff}}} \tag{3.43}$$

The equivalent mobility may be linked to the ballistic mobility using Matthiessen's rule and thus equivalent electron mobility can be determined by equation (3.44).

$$\frac{1}{\mu_{n,eff}} = \frac{1}{\mu_{eqv}} + \frac{1}{\mu_{bal}} \tag{3.44}$$

It should be noted that Matthiessen's rule tacitly assumes the momentum relaxation time due to the different scattering mechanisms have the same energy dependence. In order to correctly account for the various scattering sources a weighted statistical averaging of the relaxation times should be performed. Nevertheless Matthiessen's rule should give a good first-order approximation, especially when valley reproduction is taken in to account [129].

3.2.4 Subthreshold Drain Current Model

In the subthreshold regime, the n-MOSFET is in weak inversion or diffusion mode, in which the electrons have to cross a potential barrier in the silicon channel region. For a pocket implanted MOSFET, there can, in fact, be two barriers especially in a long channel, as shown in Fig. 3.4. Hence, conventional formulas for drain current in uniformly doped MOSFETs [42, 130, 131] are not applicable here. The subthreshold

current has deleterious effects on the performance of digital circuits in terms of increased power dissipation and a possible shift in logic levels. An accurate estimation of the subthreshold behavior by means of physical modeling is therefore important for the device and circuit design.

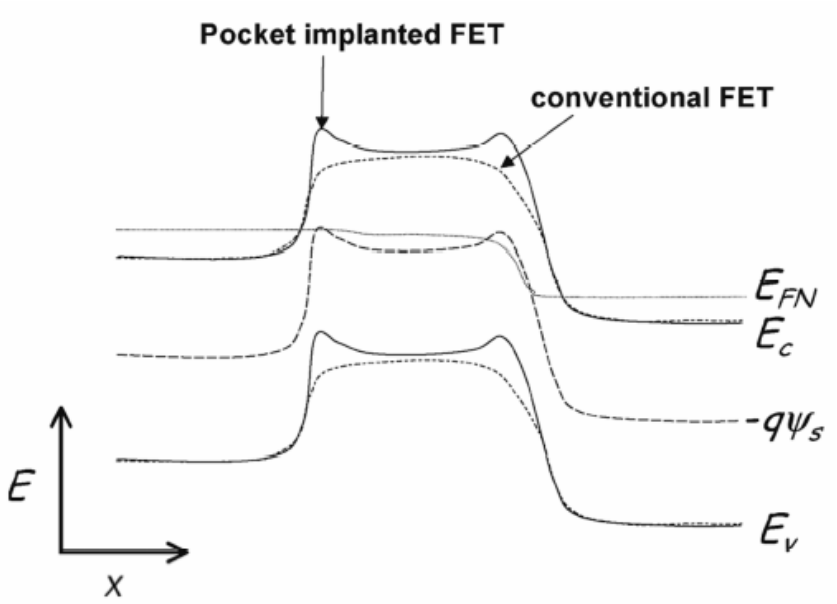

Fig. 3.4 Schematic energy band diagram in the channel region of the pocket implanted n-MOSFET. It is to be noted that the potential barriers caused by the pocket implants that also affect the surface potential ψ_s [72]

The objective in this part of the thesis is to develop a compact and physics based subthreshold current model for pocket implanted MOS devices. The p^+-type pocket implanted doping profile in the channel has been characterized in chapter 2 where an effective doping concentration was found in equation (2.16). The derived channel potential in equation (3.13) will now be used. Based on the drift-diffusion equation, the electron current density J_n in an n-MOSFET can be written as in equation (3.45).

$$J_n = q\left(-n\mu_n \frac{d\psi_s}{dx} + D_n \frac{dn}{dx}\right)$$

$$J_n = qD_n\left(\frac{-n}{\phi_{th}} \frac{d\psi_s}{dx} + \frac{dn}{dx}\right) \qquad (3.45)$$

,where $\psi_s(x)$, n, D_n and q are surface potential, electron density, diffusion co-efficient and electronic charge. ϕ_{th} is the thermal voltage and is given by equation (3.46).

$$\phi_{th} = \frac{kT}{q} = \frac{D_n}{\mu_{n,eff}} \tag{3.46}$$

Multiplying equation (3.45) by an integrating factor of $e^{-\psi_s/\phi_{th}}$, the right hand side of equation (3.45) can be transformed into an exact derivative. Then using the assumed boundary conditions for the surface potential modeling in sub-section 3.2.1, the electron current density equation (3.47) is found.

$$J_n = -qD_n N_{eff} \exp\left(-\frac{\varphi_{bi} - V_{BS}}{\phi_{th}}\right) \frac{\left(1 - \exp\left(\frac{V_{DS}}{\phi_{th}}\right)\right)}{\int_0^L \exp\left(-\frac{\psi_s}{\phi_{th}}\right) dx} \tag{3.47}$$

The complete analytical expression for the surface potential in equation (3.13) has already been obtained. The integral in the denominator of the right hand side of equation (3.47) is evaluated using the numerical integration technique of multiple segments Simpson's 1/3 rule and the surface potential model given in equation (3.13). The diffusion co-efficient for electron (D_n) in equation (3.47) has been evaluated by using the Einstein relation given in equation (3.46) and the effective electron mobility ($\mu_{n,eff}$) is obtained from equation (3.44). Finally, the drain current, I_{ds} in the channel is obtained by multiplying J_n and the channel cross-sectional area (which is the multiplication of effective channel thickness, t_{ch} and channel width, W) as given in equation (3.48).

$$I_{ds} = J_n W t_{ch} \tag{3.48}$$

The effective channel thickness, t_{ch} can be obtained as the distance from the surface to the position along the y-direction where the electrostatic potential has changed by V_{th} [132]. When the gate voltage V_{GS} is in the close vicinity of the threshold voltage, the drain current I_{ds} becomes the subthreshold current, I_{sub}. By using Gauss' law, the vertical component of the electric field at the surface, V_{th}/t_{ch}, is equal to Q_{dep}/ε_{Si} in the subthreshold region. Thus the effective channel thickness is found in equation (3.49).

$$t_{ch} = V_{th} \sqrt{\frac{\varepsilon_{Si}}{2qN_{eff}\left(2\varphi_F - V_{BS} + V_{GT}/\theta\right)}} \tag{3.49}$$

,where $V_{GT} = V_{GS} - V_{th}$, θ is the subthreshold ideality factor reflecting the gate voltage division between the insulator capacitance and the depletion layer capacitance and φ_F is the Fermi potential due to pocket implantation and is given as in equation (3.5).

Threshold voltage, V_{th} for this calculation is taken from equation (3.18). The effective channel thickness given in equation (3.49) is only valid when $-\psi(s) + V_{BS} < V_{GT}/\theta$, i.e., in the weak inversion and depletion regions.

3.2.5 Low Frequency Drain Current Flicker Noise Model

A careful examination of the drain current of a MOS transistor reveals that it varies with time if one or more of the terminal voltages vary with time. This minute fluctuations of drain current are referred to as noise. It may occur whether externally applied signals are present or not and can occur due to several mechanisms. It is characterized by the mean square or the root mean square value. The amount of noise depends on the bandwidth of the measuring instrument. A common measurement involves a very narrow bandwidth, centered on a frequency f. The current noise (i_n) spectral components within this bandwidth have a certain mean square value. The ratio of this value to the bandwidth, as the latter is allowed to approach zero, is called the power spectral of the current noise, denoted by $S_i(f)$ having unit of A^2/Hz. Often the square root of the power spectral density is used instead, given in unit of $A/Hz^{1/2}$. For a noise voltage, one can similarly define a power spectral density $S_v(f)$ in V^2/Hz or its square root in $V/Hz^{1/2}$. The total mean square noise current within an arbitrary bandwidth extending from $f = f_1$ to $f = f_2$ can be found by summing the mean square values of the individual components within each sub-bandwidth Δf. More precisely, using power spectral density concept, it is

$$\overline{i_n^2} = \int_{f_1}^{f_2} S_i(f)\, df \qquad (3.50)$$

A similar result can be obtained for voltage noise.

A well-known example of device noise is the thermal noise in a resistor also called Johnson noise or Nyquist noise. It is due to the random thermal motion of the carriers in it [133]. Thermal noise is said to be white noise, because its power spectral density is flat up to extremely high frequencies (over 10^{12} Hz). A typical plot of power spectral density for the drain current noise of a MOS device is shown in Fig. 3.5. Two distinct regions, with different noise behavior in each, can be identified. These regions can be thought of as separated by a corner frequency f_c. Values from several hertz to several megahertz are common for this quantity depending on device construction, geometry and bias. The type of noise dominating at high frequencies in Fig. 3.5 is termed as white noise denoted by i_w. The noise dominating at low frequencies in Fig.

4.5 is called flicker noise or 1/*f* noise (since the power spectral density is nearly proportional to the inverse of the frequency) denoted by i_f. These two components are independent. In calculating the total noise mean square value due to both, one can consider the effect of each separately and then add the individual mean square values and thus

$$\overline{i_n^2}=\overline{i_w^2}+\overline{i_f^2} \qquad (3.51)$$

These mean square values of the corresponding noise spectral components within a very small bandwidth in equation (3.51) are divided by that bandwidth and allowing it to approach zero, the total power spectral density, $S_i(f)$ can be written as

$$S_i(f)=S_{iw}(f)+S_{if}(f) \qquad (3.52)$$

,where $S_{iw}(f)$ and $S_{if}(f)$ are the power spectral densities of the white and flicker noise components, respectively as indicated in Fig. 3.5.

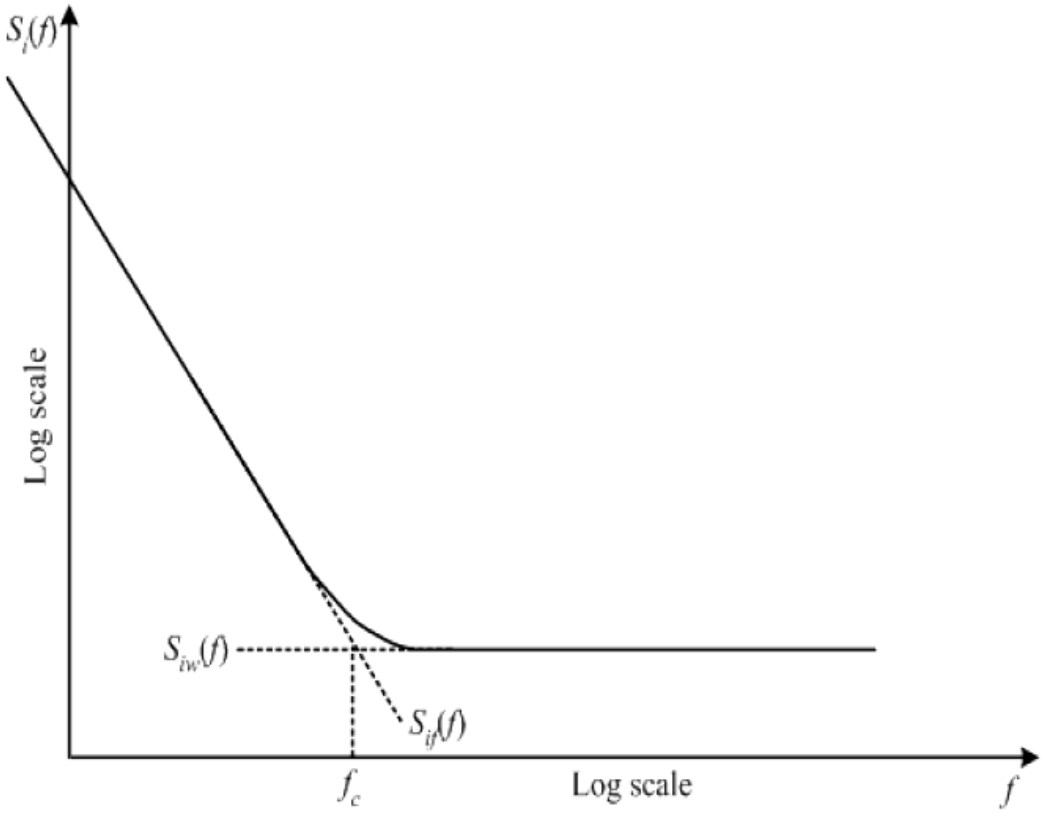

Fig. 3.5 A typical plot of the drain-noise current power spectral density vs. frequency in log-log axes

Flicker noise in MOS transistor has been the subject of intensive studies for several decades. There are theories for the origin of this noise, with involved physics and

sometimes conflicting conclusions and several unresolved issues. There are two dominant theories for the flicker noise.

The first theory attributes the origin of flicker noise to the random fluctuation of the number of carriers in the channel, due to fluctuations in the surface potential; the fluctuations are in turn caused by trapping and releasing of carriers by traps located near the Si-SiO_2 interface [17]. The characteristic times involved in this process cover a very wide range, and when very large numbers of such events are considered, it can be shown that a power spectral density nearly proportional to the inverse of the frequency results [133].

The second theory attributes flicker noise to mobility fluctuations, due to carrier interactions with lattice fluctuations. Results based on this theory suggest that the power spectral density is inversely proportional to the gate oxide capacitance per unit area. But this inverse proportionality is not universally accepted [17].

Due to the statistical nature of the flicker noise, devices with too small an area may exhibit a large fluctuation range in noise [134]. The availability of smaller dimension MOSFETs have provided an opportunity to study the noise generated by individual oxide traps [135-137]. For MOSFETs with very small channel area ($< 1\ \mu m^2$), it is possible to have only a single active oxide trap in the vicinity of the quasi-Fermi level over the entire channel. Capture and emission of a channel carrier by the trap result in discrete modulation of the channel current resemble a random telegraph signal (RTS). A single RTS can be regarded as a single Lorentzian component of the flicker noise in conventional devices. In [138], it was confirmed that the oxide traps generate noise by modulating the carrier number as well as the carrier mobility through Coulombic scattering. Physical parameters for modeling the scattering effect have been extracted from the RTS data. Based on the new information obtained from the study of random telegraph noise, a new flicker noise model was proposed which incorporates both the number of fluctuation and surface mobility fluctuation mechanisms [139]. The latter is attributed to the scattering effect of the fluctuating oxide charge. As these fluctuations have the same cause, they are correlated with each other and it was found that this model could consistently explain most of the noise data reported in the literatures. Therefore, this unified drain current flicker noise model for the conventional bulk n-MOSFET has been extended to the pocket implanted n-MOSFET. According to this unified drain current flicker noise model [139], the

normalized noise power spectrum density (S_{id}/I_d^2) for the conventional MOS device has the simple analytic form at very low drain voltages as given in equation (3.53).

$$\frac{S_{id}}{I_d^2} = \frac{kT}{\gamma f W L^2} \int_0^L N_t\left(E_{fn}, x\right)\left[\frac{1}{N_{inv}(x)} + \alpha\mu\right]^2 dx \qquad (3.53)$$

,where $\gamma = 10^8$ cm^{-1} is the attenuation coefficient of the electron wave function in the oxide, α is the scattering coefficient [78], $N_{inv}(x)$ is the number of channel carriers per unit area, and $N_t(E_{fn}, x)$ is the oxide trap density at the electron Fermi level, E_{fn}.

At a very low gate overdrive bias, the mobility fluctuation term $\alpha\mu$ in equation (3.53) is smaller than $1/N_{inv}(x)$ term. Therefore, $\alpha\mu$ term can be neglected. Then the carrier density is uniform along the channel and is given by equation (3.54).

$$qN_{inv} = C_{ox}\left(V_{GS} - V_{th}\right) \qquad (3.54)$$

,where V_{GS} is the gate voltage and V_{th} is the threshold voltage for the pocket implanted n-MOSFET given in equation (3.18) and C_{ox} is the oxide capacitance per unit area.

Since the oxide (interface) trap density is not affected by the pocket implantation process, it is assumed that the oxide trap density along the channel is uniform. From Fig. 3.1, it is evident that the channel region is divided into three distinct regions. The first and the third regions are the pocket implanted regions and the centre region is the uniformly doped substrate region. Hence, the noise model is also divided in three parts as given in equation (3.55).

$$\frac{S_{id}}{I_d^2} = \frac{kT}{\gamma f W L^2} N_t\left[\int_0^{L_p} \frac{1}{N_s^{\,2}(x)} dx + \int_{L_p}^{L-L_p} \frac{1}{N_{sub}^{\,2}} dx + \int_{L-L_p}^{L} \frac{1}{N_d^{\,2}(x)} dx\right] \qquad (3.55)$$

Using equations (2.13), (2.14), (3.53) and (3.54), equation (3.55) can be written as in equation (3.56), which is the desired model.

$$\frac{S_{id}}{I_d^2} = \frac{kTq^2}{\gamma f W L^2 C_{ox}^2} N_t\left[\frac{2L_p}{\left(V_{GS} - V_{th}\right)\left(V_{GS} - V_{thp}\right)} + \frac{L - 2L_p}{\left(V_{GS} - V_{th}\right)^2}\right] \qquad (3.56)$$

,where V_{thp} is the threshold voltage in the pocket region found using equation (3.18), but for this case effective doping concentration (N_{eff}) along the channel is replaced by the effective doping concentration near the pocket regions only.

3.3 Summary

In this chapter, different models are developed for the pocket implanted n-MOSFET. At first, the surface potential model is developed by applying Gauss's law, then the threshold voltage model of the pocket implanted n-MOSFET is proposed incorporating the bias and temperature effects. After that the inversion layer effective mobility model is presented and using this model subthreshold drain current model is developed from the drift-diffusion equation. Finally, the low frequency drain current flicker noise model is proposed using the proposed threshold voltage model. In the next chapter, all of these models will be simulated in the MATLAB environment and simulation results will be presented and discussed. Besides, verifications of few proposed models will be done by using the experimental data already published in the literatures.

Chapter 4

Simulation Results and Discussions

4.1 Introduction

This chapter explores the connection between the different models of the pocket implanted n-MOSFET developed in chapter 4 through different simulation results for the various device and pocket profile parameters as well as different temperature and bias conditions. For simulation purpose, MATLAB software package is used. Codes are developed in MATLAB environment for all the models developed. Pocket profiles are also simulated using MATLAB codes.

MATLAB simulation of all the codes have been performed in an

IBM machine with
240 GB hard disk drive,
2 GB RAM
and an Intel Core2 Duo CPU with 2.8 GHz clock frequency
using Microsoft Windows XP operating system.

Built-in timers of MATLAB have been used to calculate the execution time of each program for the different parameters of the pocket implanted n-MOSFET.

4.2 Surface Potential Model

In order to verify the proposed analytical surface potential model for the pocket implanted n-MOSFET, different types of simulations were performed in MATLAB. At first, the bias conditions are changed to observe the effects on surface potential. Then the device parameters and pocket profile parameters are changed to verify the proposed model. Then a comparison of the proposed surface potential model using linear pocket profile model is made with the other pocket profile models found in the literatures.

Fig. 4.1 shows the variation of surface potential along the channel for different drain biases. It has been observed that as the drain bias increases surface potential increases at the drain side whereas it remains constant at the source side. It proves the validity of the assumed boundary conditions while deriving the model.

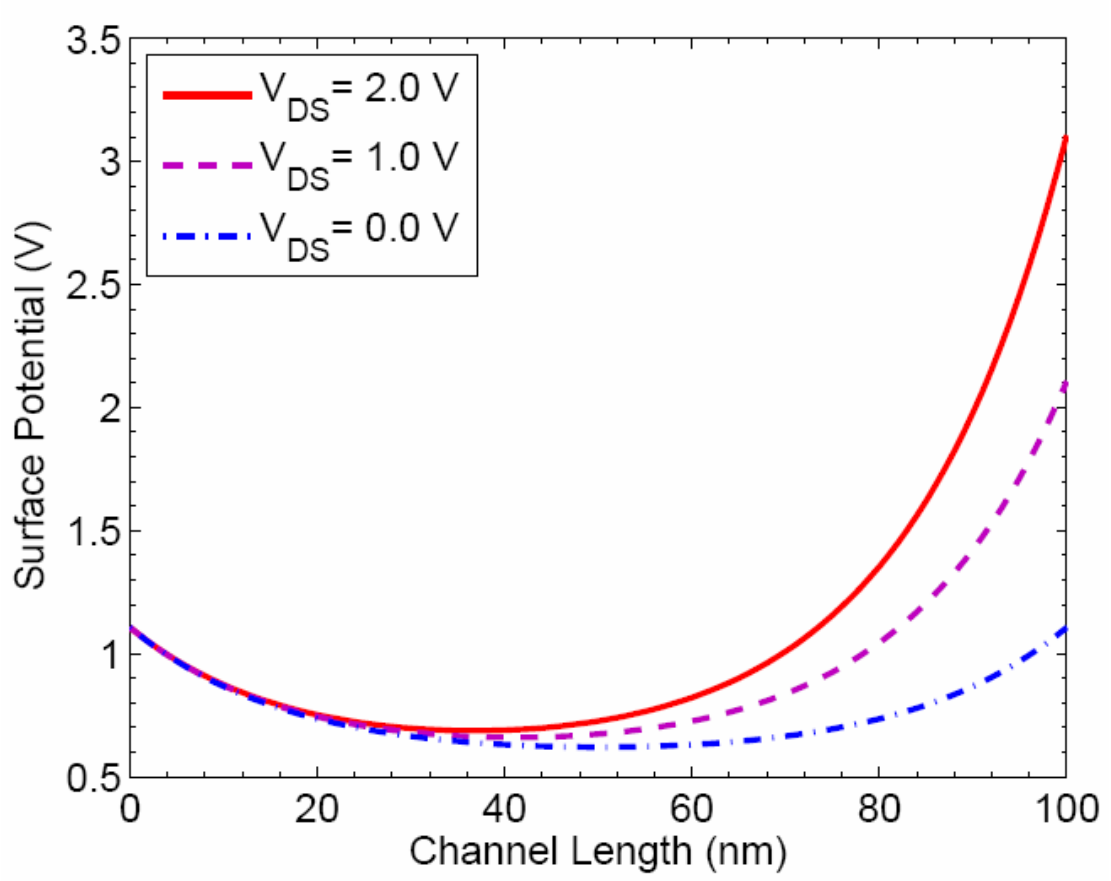

Fig. 4.1 Surface potential vs. channel length curves for various drain biases with channel length, L = 100 nm and substrate bias, V_{BS} = 0.0 V

From Fig. 4.2, it is observed that as substrate bias increases in the negative direction keeping drain bias constant at 0 V, both sides of the curve shifts upward. Since when

substrate bias increases in the negative direction, more holes are attracted towards the substrate terminal and hence depletion region charge increases, thereby increasing the surface potential.

Fig. 4.3 shows the variation of surface potential along the channel for different gate voltages below the threshold voltage with channel length of 0.1 μm. It is observed from this figure that as the gate voltage is increased, the peak of the potential minimum shifts upward without changing the boundary values. Since the boundary values of the surface potential are not dependent on gate bias. The reason for the increase of the surface potential minimum can be attributed to the increase of the depletion layer charge with the increasing gate bias.

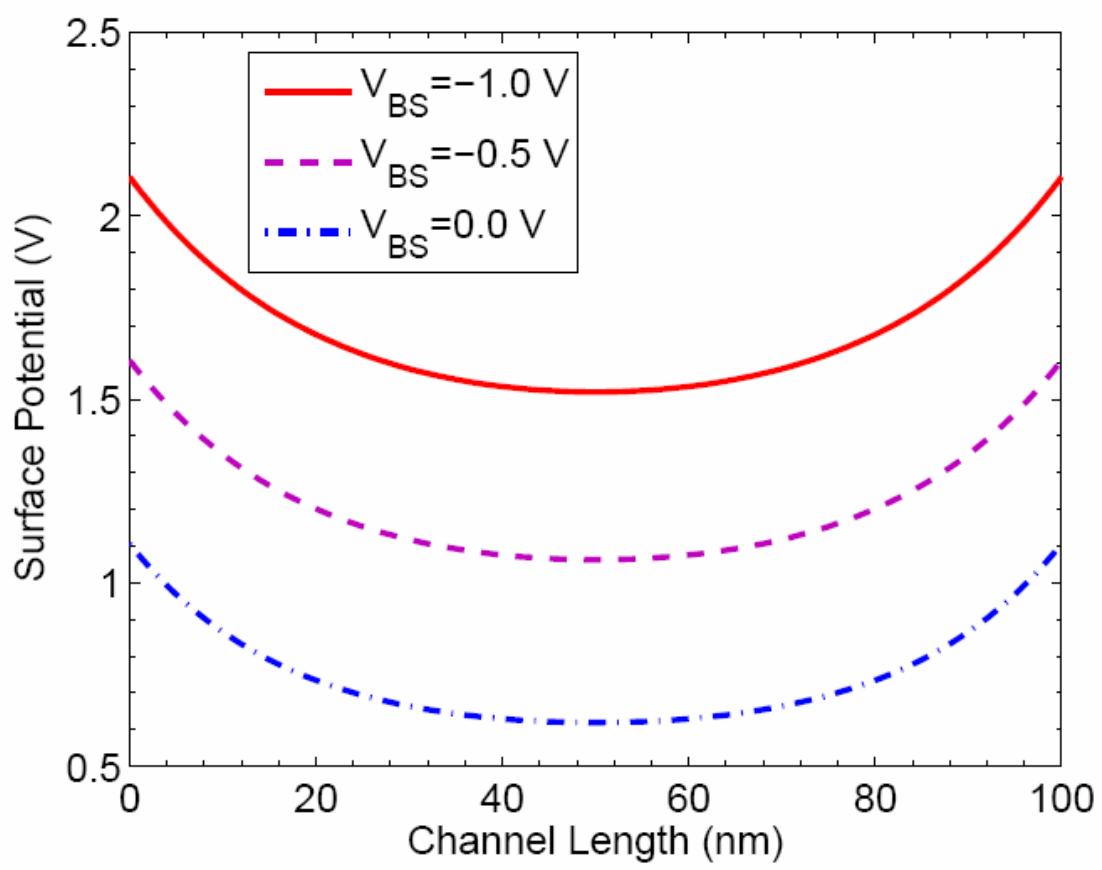

Fig. 4.2 Surface potential vs. channel length curves for various substrate biases with channel length, L = 100 nm and drain bias, V_{DS} = 0.0 V

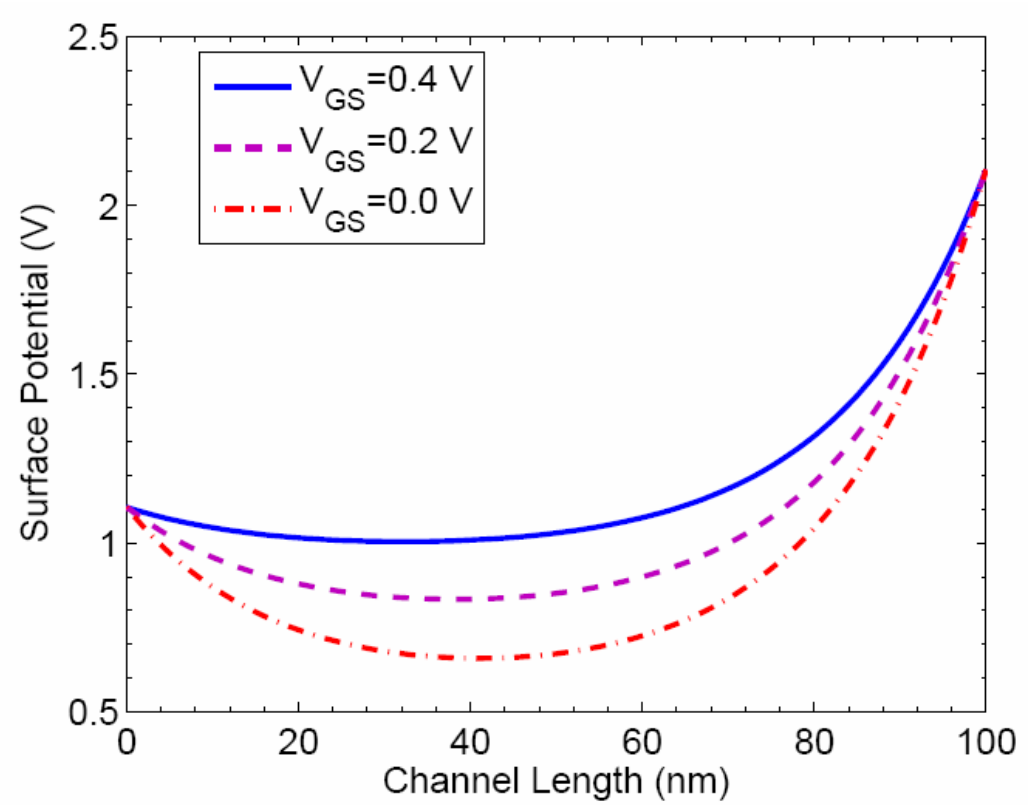

Fig. 4.3 Surface potential curves along the channel for various gate biases below the threshold voltage with channel length, L = 100 nm, substrate bias, V_{BS} = 0.0 V and drain bias, V_{DS} = 1.0 V

From Fig. 4.4, it is found that as the channel lengths are decreased from 100 nm to 50 nm, surface potential is same as in Fig. 4.1 for V_{DS} = 1.0 V at source/drain sides of the device. But the potential minimum shifts upward direction and are pushed towards the source side as the channel lengths are decreased. This occurs due to the incorporation of the depletion region charges of the source and drain sides in to the depletion region charge under the gate at the surface. The values of the minimum surface potential and its position along the channel from the source side are shown in Table 4.1 for different channel lengths.

Table 4.1 Minimum surface potential and its position along the channel from the source side for different channel lengths

L (nm)	$\psi_{s,min}$ (V)	x_{min} (nm)
50	0.866	17
100	0.659	41
250	0.622	115

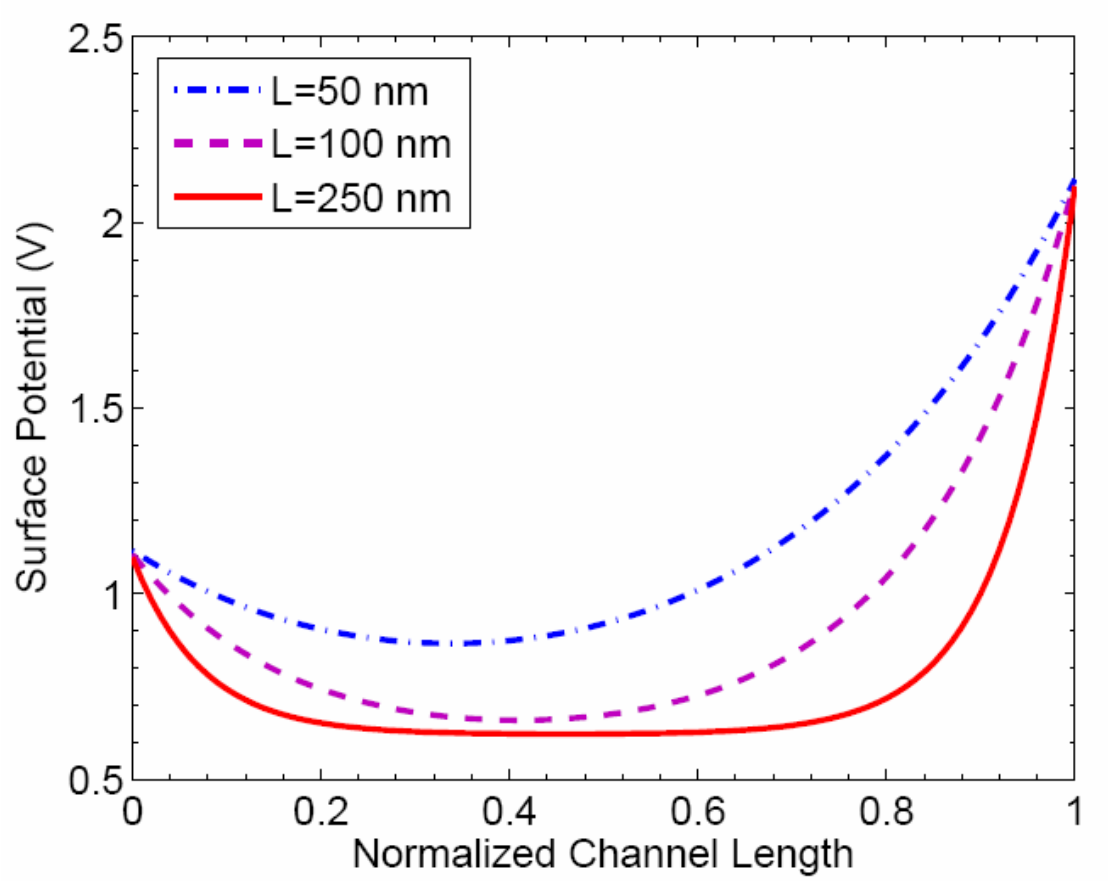

Fig. 4.4 Surface potential curves along the channel for various channel lengths with substrate bias, V_{BS} = 0.0 V and drain bias, V_{DS} = 1.0 V

Fig. 4.5 shows the variation of surface potential along the channel for different oxide thicknesses with zero substrate bias and drain bias, V_{DS} = 1.0 V. It is observed that as the oxide thickness decreases the potential minimum increases near the source side. But near the drain, opposite phenomenon is observed. When oxide thickness decreases oxide capacitance increases. This increases the surface charge and hence surface potential for a fixed bias condition. Since at the drain side with the reduction of the oxide thickness, the oxide capacitance increases as well as the off-state current increases thus the potential at the drain side decreases. Hence DIBL effect will be more pronounced as the oxide thickness is decreased at the drain side.

Fig. 4.6 shows that the surface potential increases with the decreasing pocket lengths. Since when the pocket length decreases the effective doping concentration also decreases. But the boundary value remains the same as expected.

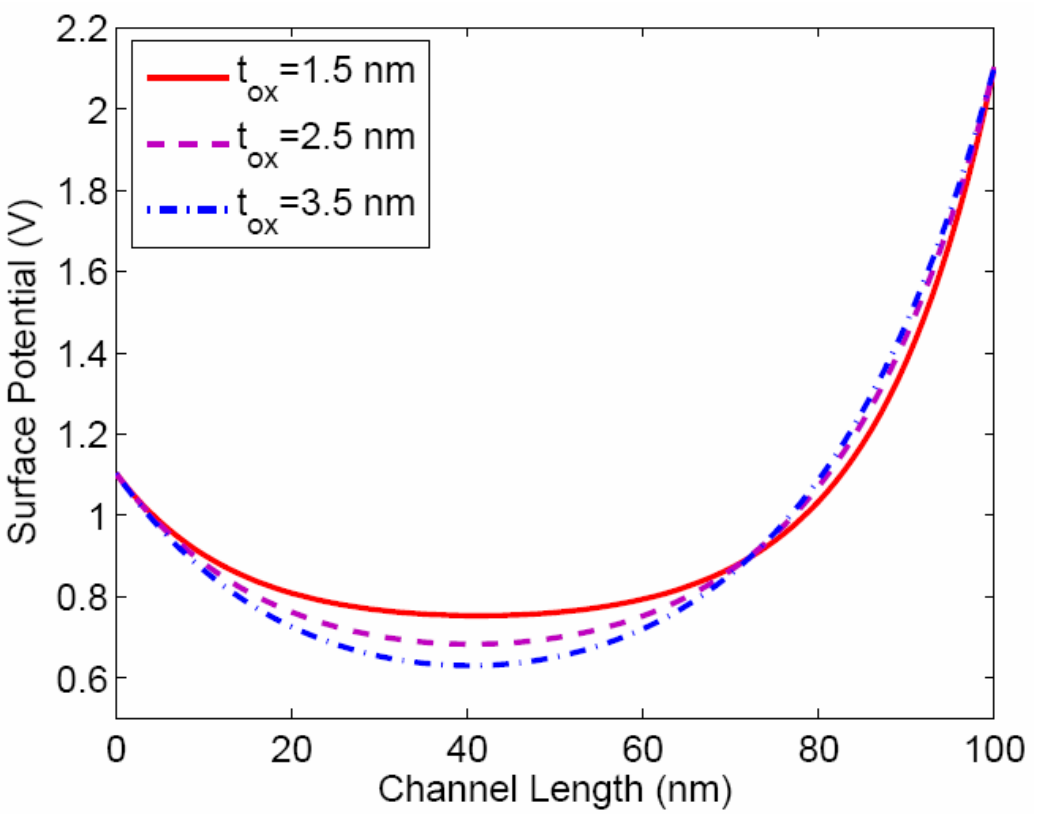

Fig. 4.5 Surface potential curves along the channel for various oxide thicknesses with channel length, L = 100 nm, substrate bias, V_{BS} = 0.0 V and drain bias, V_{DS} = 1.0 V

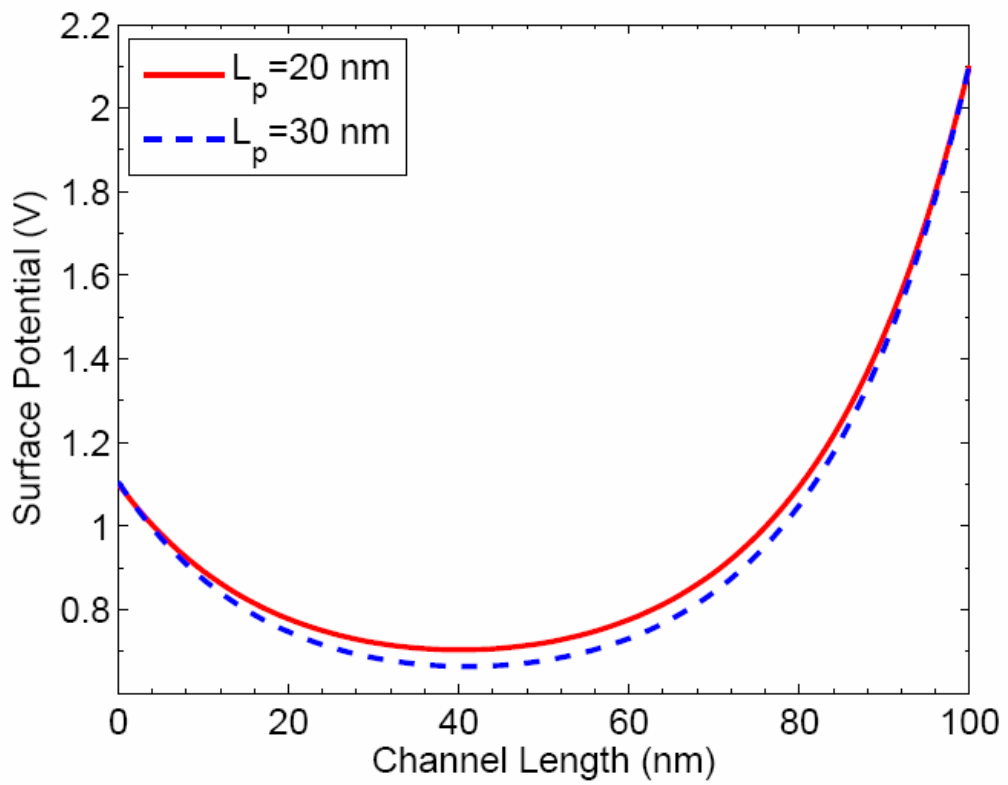

Fig. 4.6 Surface potential curves along the channel for various pocket lengths with channel length, L = 100 nm, substrate bias, V_{BS} = 0.0 V and drain bias, V_{DS} = 1.0 V

Fig. 4.7 shows the surface potential variation with the position of the channel for different peak pocket doping concentration. It is observed that the surface potential increases as the peak pocket doping concentration decreases. This is due to the decrease of effective carrier concentration along the channel. The results are shown for zero substrate bias and drain bias of 1 V.

Fig. 4.8 shows the surface potential curves along the channel for the proposed linear profile with two other pocket doping profile models found in the literature, such as, Gaussian function [47] and hyperbolic cosine function [48] models. These two pocket doping models are used in the proposed analytical surface potential model and then simulated for various bias conditions and pocket profiles and device parameters. It is found that the proposed model using linear profiles works well and satisfies all the conditions of the surface potential model and shows similar behavior like the other models.

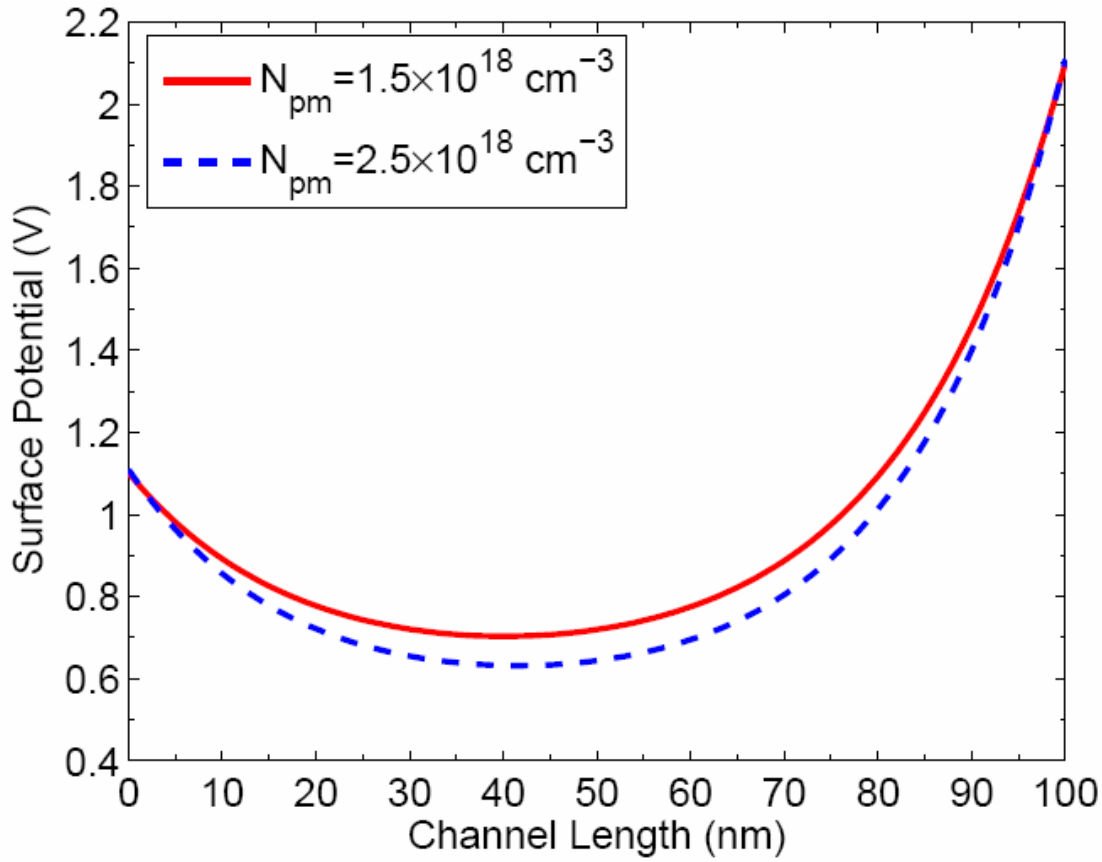

Fig. 4.7 Surface potential curves along the channel for various peak pocket doping concentration with channel length, L = 100 nm, substrate bias, V_{BS} = 0.0 V and drain bias, V_{DS} = 1.0 V

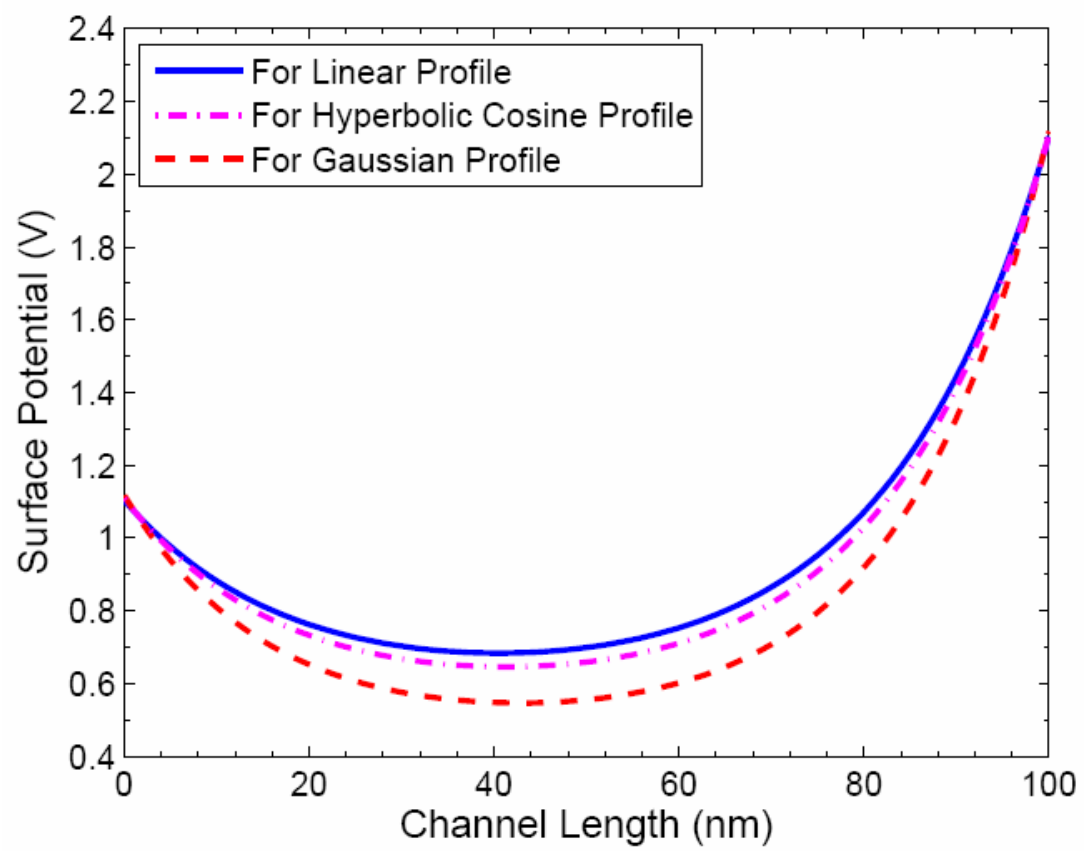

Fig. 4.8 Surface potential curves along the channel for various pocket profiles found in the literatures with channel length, L = 100 nm, substrate bias, V_{BS} = 0.0 V, drain bias and V_{DS} = 1.0 V

4.3 Threshold Voltage Model

Since there are two parts of the threshold voltage model as described in two subsections of chapter 3, in this chapter simulation results and discussions are also presented in the following two subsections.

4.3.1 Bias Effects

The simulated V_{th} vs. L curve has been drawn for this new model is shown in Figs. 4.9-4.10 for zero drain and substrate biases. It is shown that with the increasing pocket lengths and peak pocket concentrations the peak of these curves increase and the onset of threshold voltage (V_{th}) roll-up happens at a longer channel length and also the onset of V_{th} roll-off happens at a shorter channel length. This result exhibits strong reverse short channel effect (RSCE) with the increased L_p and N_{pm}. If these are increased further by keeping the other parameters constant then V_{th} roll-off starts to vanish exhibiting only reverse short channel effect.

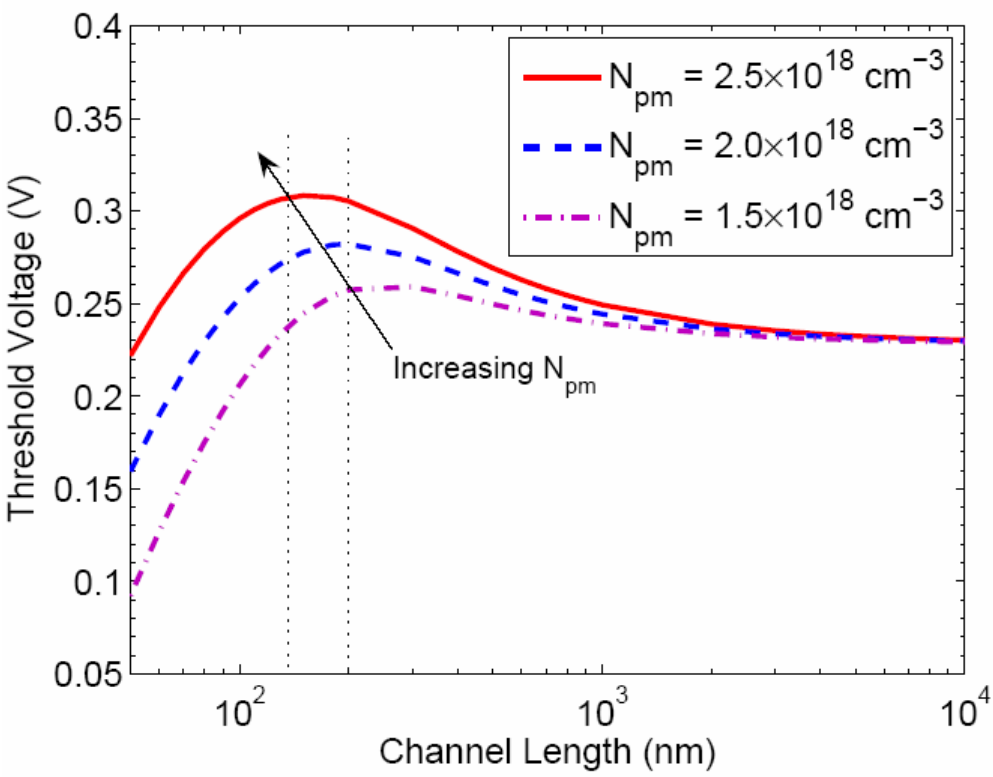

Fig. 4.9 Threshold voltage vs. channel length curves along the channel for various peak pocket doping concentration with V_{BS} = 0.0 V, V_{DS} = 0.0 V and L_p = 25 nm

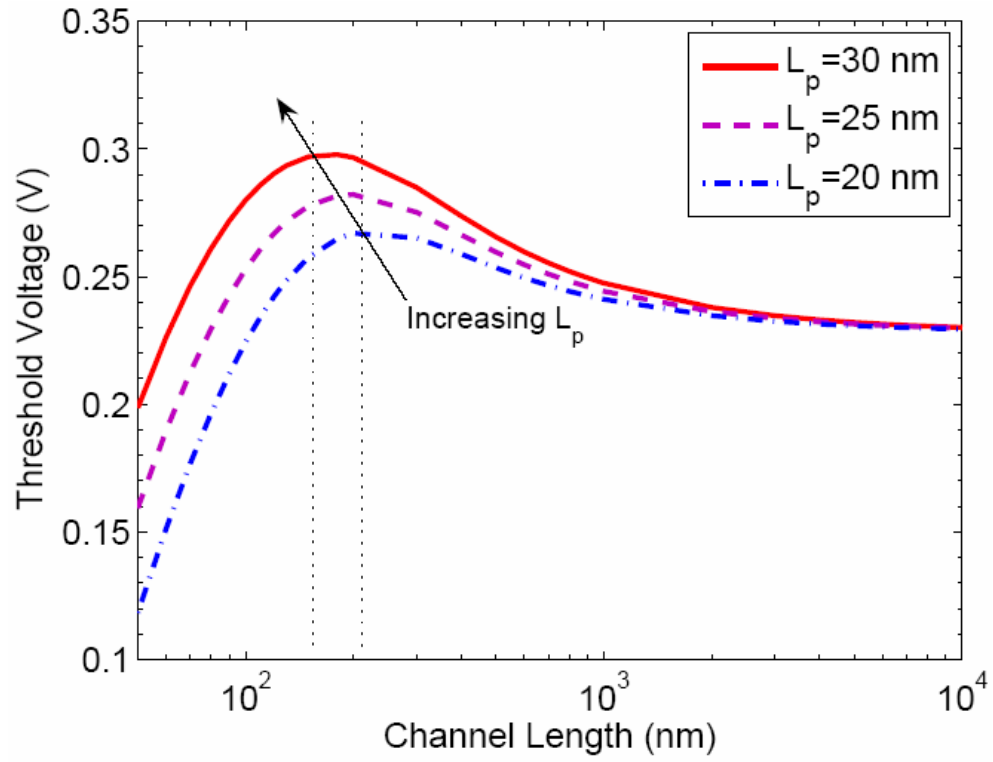

Fig. 4.10 Threshold voltage vs. channel length curves along the channel for various pocket lengths with V_{BS} = 0.0 V, V_{DS} = 0.0 V and N_{pm} = 1.75×10^{18} cm^{-3}

From Fig. 4.11, it is observed that as the drain bias increases, both RSCE and SCE occur both at longer channel length due to the drain induced barrier lowering (DIBL). As channel length becomes shorter DIBL effect is more pronounced. Higher drain bias makes the threshold voltage negative. Since at shorter channel length, electric field is very high and it lowers the potential barrier that separates it from the adjacent diffused junction. Therefore, due to the presence of high channel doping even at negative gate voltage drain current starts to flow.

From Fig. 4.12, it is found that as the substrate bias increases in the negative direction the threshold voltage increases. This is due to the increment of depletion charge under the gate. Also, with increasing magnitude of V_{BS}, RSCE occurs at longer channel length (L), threshold voltage (V_{th}) roll-off becomes steeper and V_{th}-L curve crosses the zero-substrate bias curve at shorter channel length. This is because of the linear dependence of V_{DS} and V_{BS} on V_{th} and exponential dependence of L on V_{th}. As V_{BS} becomes more negative RSCE starts to diminish.

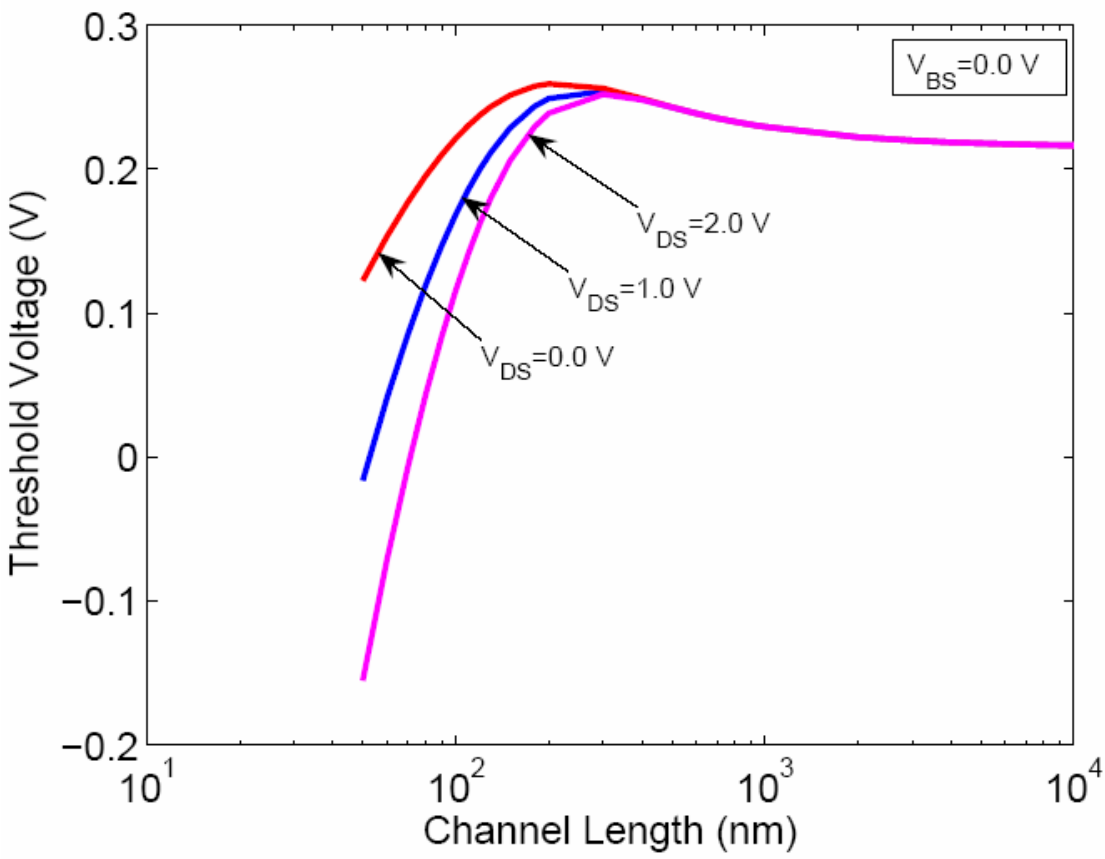

Fig. 4.11 Threshold voltage vs. gate length curves for various drain biases at zero substrate bias

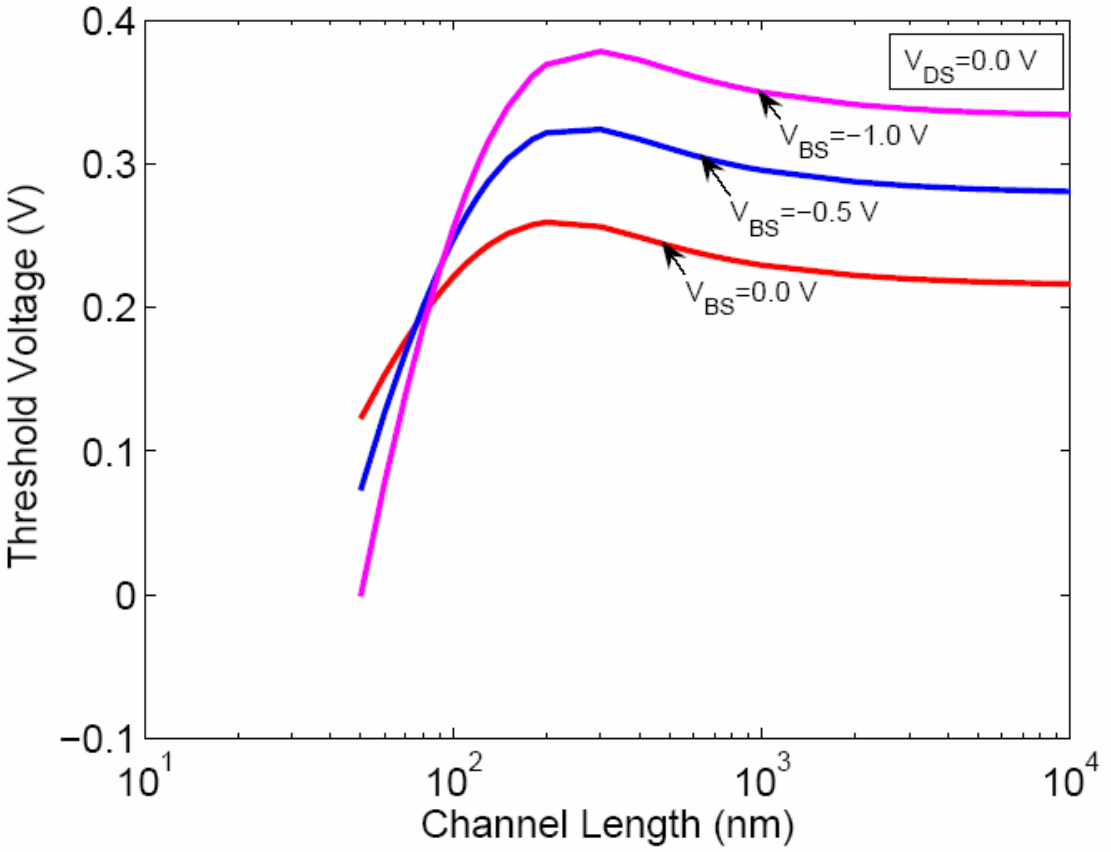

Fig. 4.12 Threshold voltage vs. gate length curves for various substrate biases at zero drain bias

Figs. 4.13-4.14 show the variation of threshold voltage with the drain bias for different substrate biases of V_{BS} = 0.0 V and -1.0 V respectively with channel length as a parameter. It is observed that as the drain bias increases threshold voltage decreases. As the channel length shrinks, this effect becomes more prominent. For longer channel device, lateral electric field is less than the transverse electric field. Thus for low drain bias diffusion current dominates over drift current. Hence threshold voltage does not deviate too much from low drain bias to high drain bias. But for shorter channel device, lateral electric field becomes stronger at low drain bias too. Hence drift current increases at low drain bias thereby larger threshold voltage deviation is observed from low to high drain bias.

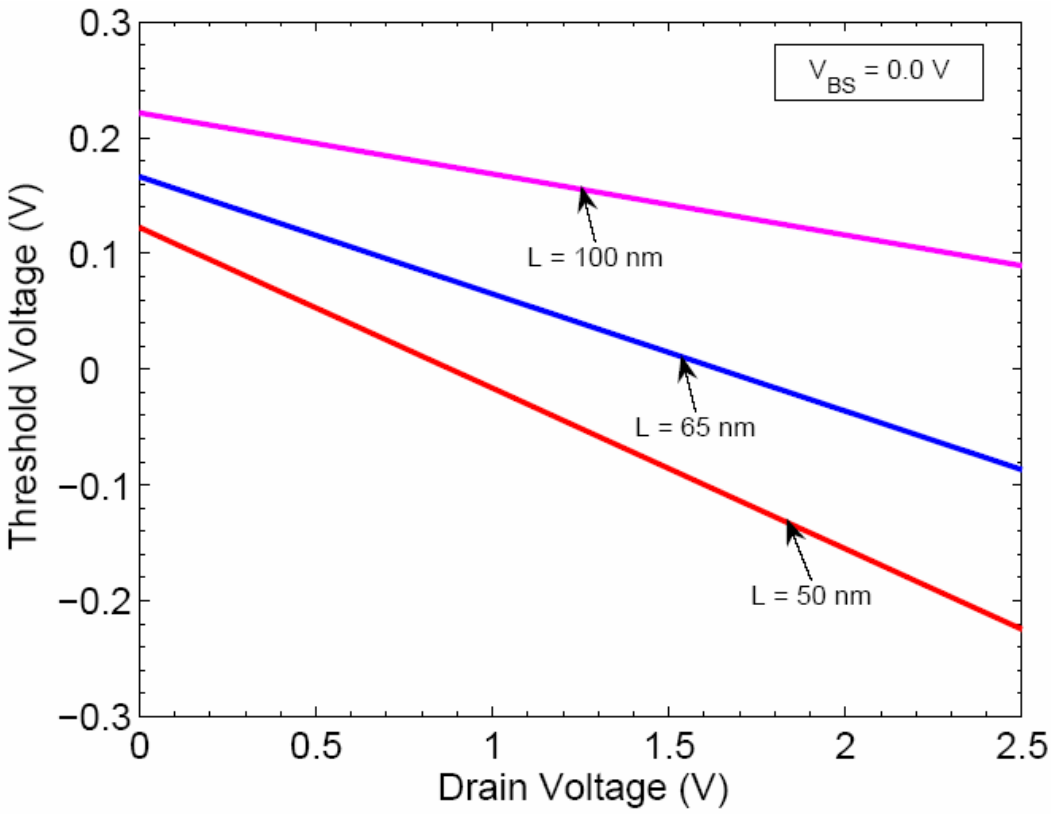

Fig. 4.13 Threshold voltage vs. drain voltage curves for various gate lengths with substrate bias, V_{BS} = 0.0 V

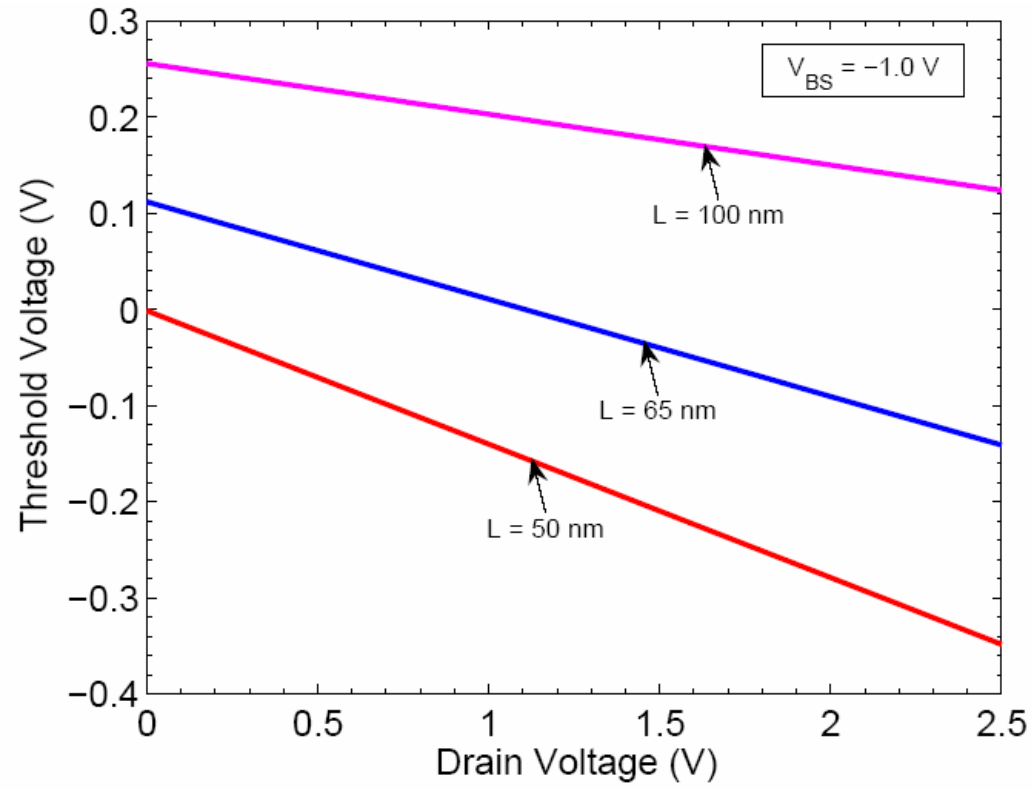

Fig. 4.14 Threshold voltage vs. drain voltage curves for various gate lengths with substrate bias, V_{BS} = -1.0 V

Fig. 4.15 shows the variation of threshold voltage with the substrate bias for different channel lengths at zero drain bias. It is seen that as VBS increases in the negative direction threshold voltage increases for long channel lengths and decreases for short channel lengths, i.e. in the nano scale regime, and near 100 nm channel lengths threshold voltage is insensitive to substrate bias. This phenomenon happens due to the pocket implantation. When substrate bias increases in the negative direction in the long channel device, depletion layer charge increases due to the increase of depletion layer width that causes the threshold voltage to increase. But in the short channel device, source/drain junction's depletion regions become an important part of the depletion region under the gate and hence threshold voltage decreases. Thus when the substrate bias increases in the negative direction threshold voltage starts to rise in the long channel but in the short channel device it starts to fall. For 100 nm device, threshold voltage is almost insensitive to substrate bias due to the effects of pocket implantation.

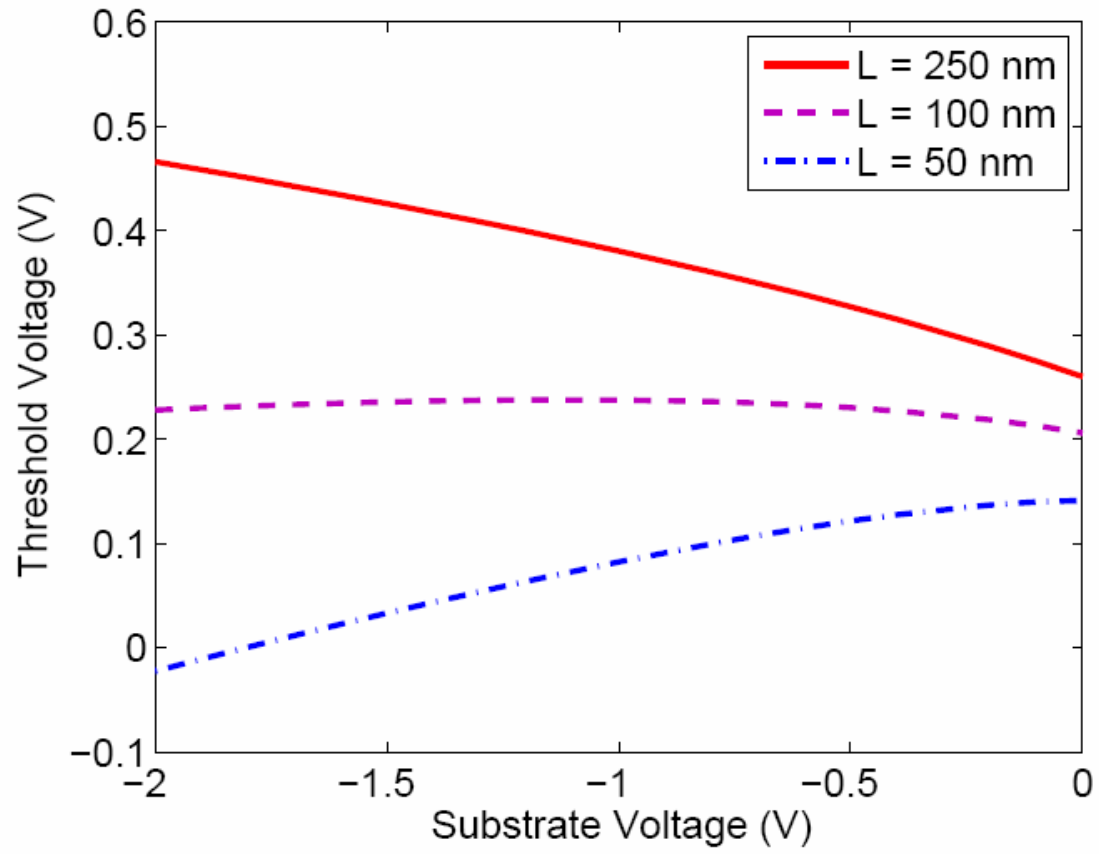

Fig. 4.15 Threshold voltage vs. substrate voltage curves for various gate lengths with V_{DS} = 0.0 V

Fig. 4.16 shows that the proposed model based on linear pocket profile exhibits similar results of suppressing short channel effects in comparison with the other models for the pocket profiles based on Gaussian [47] and hyperbolic cosine functions [48]. This can be explained using the Fig. 4.17 where the effective carrier concentration variation with the channel lengths are shown. Here, it is seen that the effective carrier concentration increases very smoothly for the linear pocket profile as the channel length shrinks. But in case of hyperbolic cosine function, it does not start to increase until 200 nm. But the SCE starts before 0.1 μm [49]. Therefore, for hyperbolic cosine model, at first SCE starts and then again RSCE becomes stronger below 100 nm.

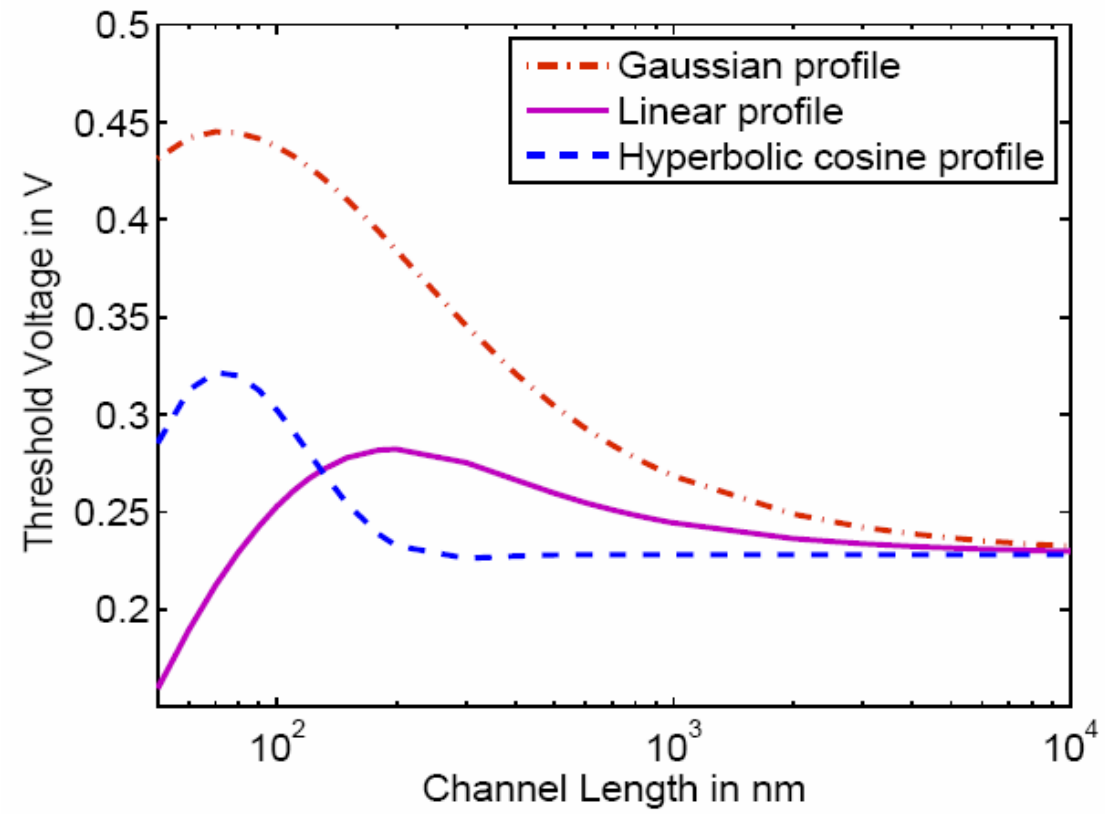

Fig. 4.16 Threshold voltage vs. gate length curves for three different pocket profiles based on linear, Gaussian and hyperbolic cosine functions for $N_{pm} = 1.75\times10^{18}$ cm^{-3}, $L_p = 25$ nm and $N_{sub} = 4.2\times10^{17}$ cm^{-3}

On the other hand, in case of Gaussian function, the effective carrier concentration increases more rapidly than that in the linear model. Therefore, in Fig. 4.16, it is observed that RSCE is stronger. Thus in this case, threshold voltage increases until 70 nm. But in sub-100 nm regime the purpose is to suppress the SCE only by the RSCE

by implanting the pockets. Besides, simulation time taken to calculate threshold voltage by using the proposed model is less than that by using Gaussian function and hyperbolic cosine function models. Also, the accuracy level of the proposed model does not hamper to a large extent.

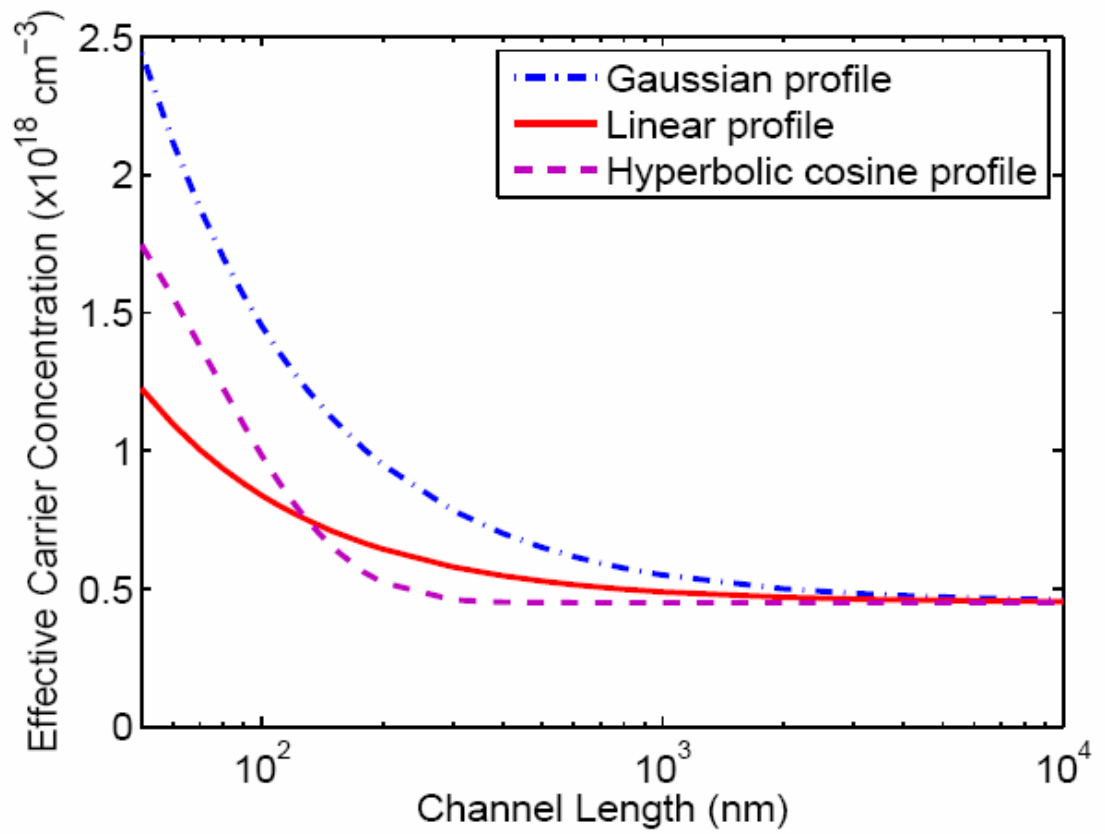

Fig. 4.17 Effective carrier concentration with channel lengths for three different pocket profiles based on linear, Gaussian and hyperbolic cosine functions for N_{pm} = 1.75×10^{18} cm^{-3}, L_p = 25 nm and N_{sub} = 4.2×10^{17} cm^{-3}

In Fig. 4.18, it is tried to fit experimental data of reference [33] to the simulated data of the proposed linear pocket profile based threshold voltage model for the same device parameters given in [33]. The parameter values are- substrate concentration, N_{sub} = 1.0×10^{17} cm^{-3}, peak pocket concentration, N_{pm} = 5.5×10^{17} cm^{-3}, pocket length along the channel, L_p = 60 nm either from source or drain side, oxide thickness, t_{ox} = 6 nm, junction depth, r_j = 80 nm, substrate bias, V_{BS} = 0.0 V and drain bias, V_{DS} = 0.05 V and 1.5 V. Flat band voltage obtained by simulation is V_{FB} = -0.9 V.

From Fig. 4.18, it is clear that the simulated data almost agrees well with the experimental data in [33]. In the short channel regime also the experimental data

published in [33] almost follows the proposed threshold voltage model using linear profile. By changing the process conditions, it is possible to adjust the experimental results with the simulated data. Because, only flat band voltage is adjusted to fit the experimental data.

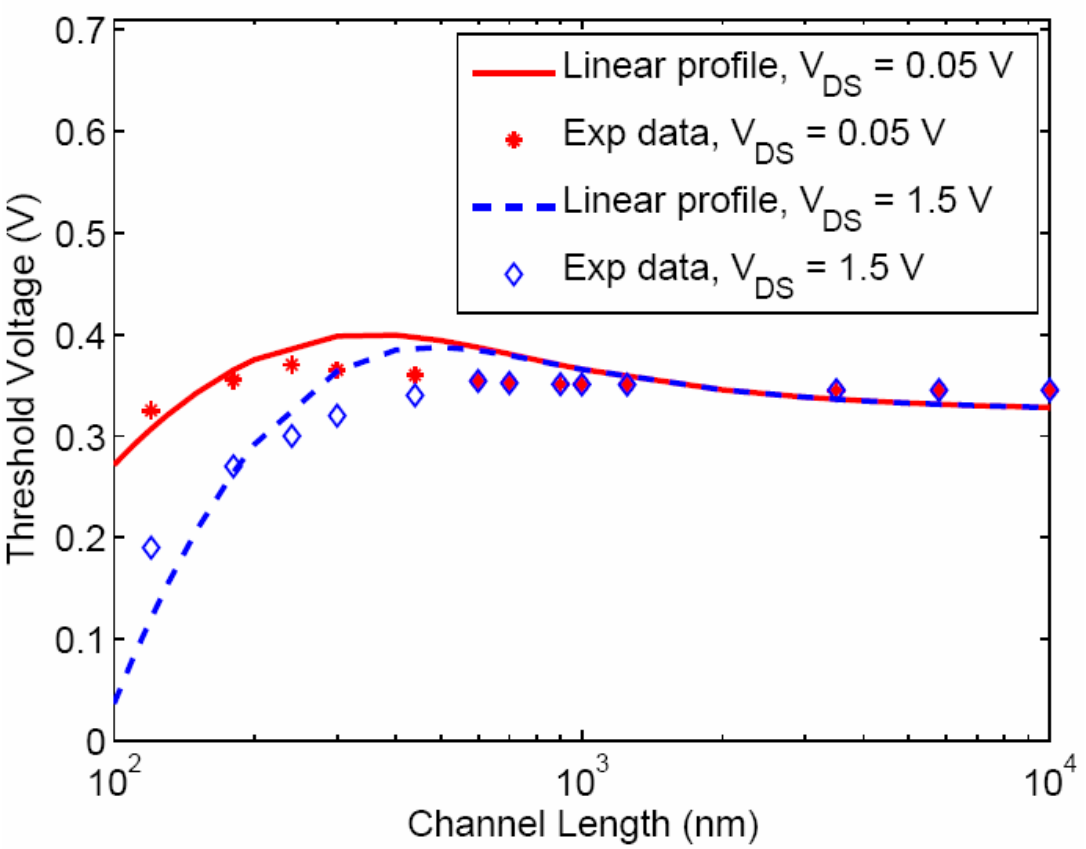

Fig. 4.18 Fitting experimental data of reference [33] to the simulated results of the proposed linear pocket profile based threshold voltage model

4.3.2 Temperature Effects

At first, to observe the effects of temperature on all the parameters that depend on the threshold voltage, various simulations were performed. Then the threshold voltage was simulated for various pocket profile parameters and temperature conditions including the effects of these temperature dependent parameters. The metal-semiconductor work function difference comes from the band gap and the Fermi potential. Its magnitude decreases with the increase of temperature as shown in Fig. 4.19.

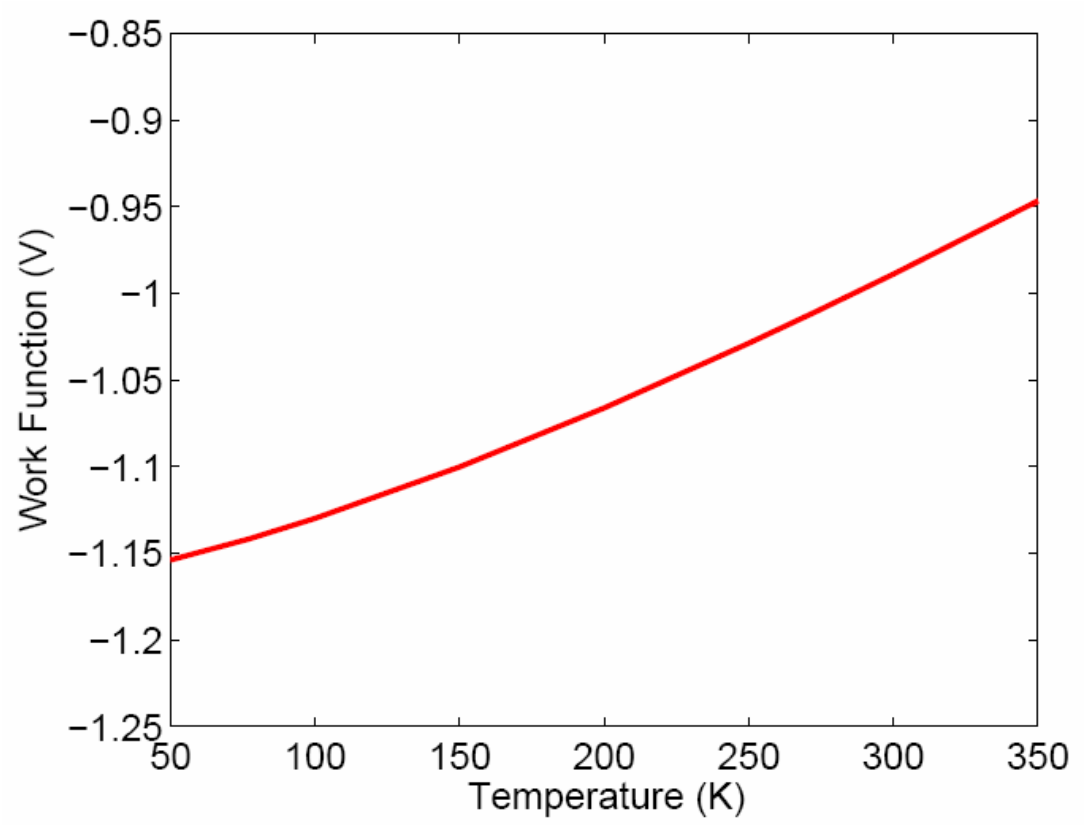

Fig. 4.19 Metal-Semiconductor work function difference variation with temperature

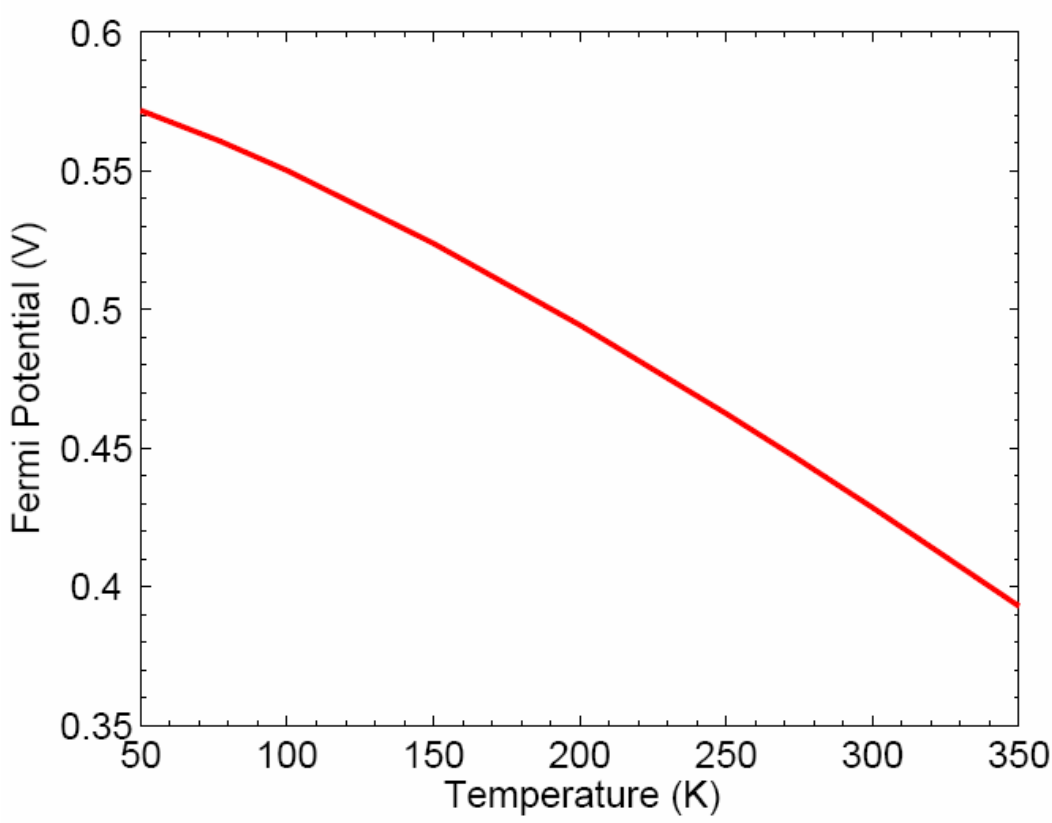

Fig. 4.20 Fermi potential variation with temperature

Energy band gap decreases with increasing temperature as obtained from equation (3.26). Fermi potential, (φ_F) depends on effective doping concentration, temperature and intrinsic concentration as shown in equation (3.5). The intrinsic carrier concentration (n_i) varies with temperature as observed from equations (3.23)-(3.25). It also varies with the energy band gap which is a temperature dependent parameter as observed equation (3.26). It is observed that the intrinsic carrier concentration (n_i) increases with the temperature. This can be attributed to the fact that as the temperature increases covalent bonds break in the Si crystal lattice and hence increases the number of electron-hole pair. Therefore, with the increase in the temperature, the Fermi potential decreases as shown in Fig. 4.20.

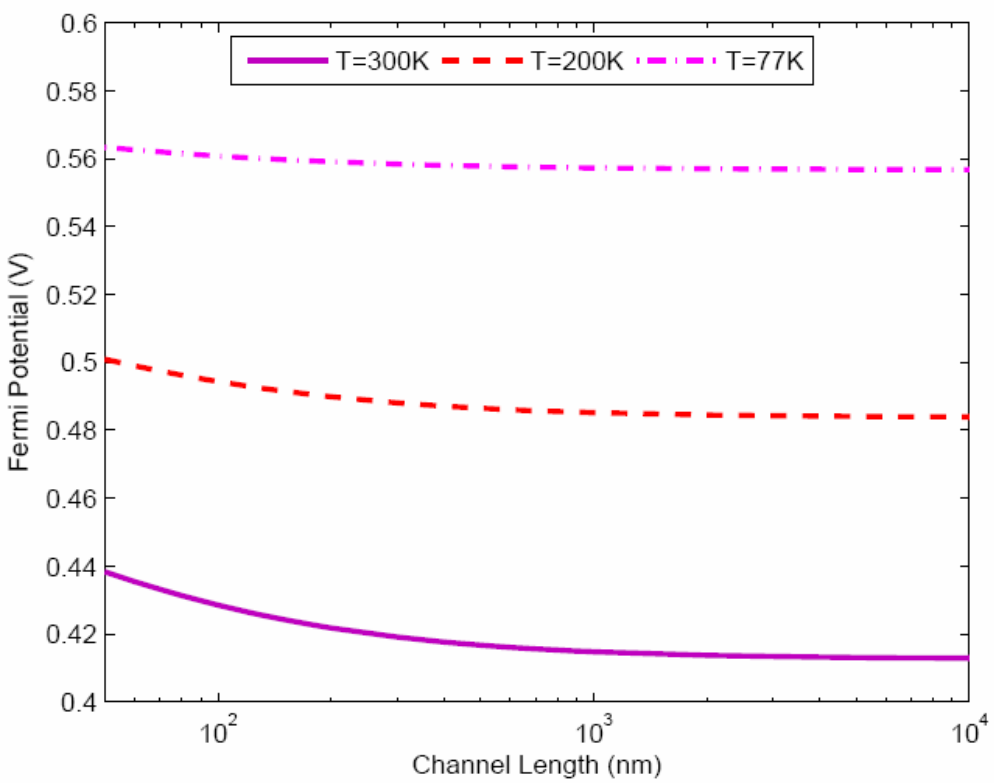

Fig. 4.21 Fermi potential variation with gate length for various temperatures with drain bias, V_{DS} = 0.1 V and substrate bias, V_{BS} = 0.0 V

From Fig. 4.21, it has been observed that at higher temperature the Fermi potential variation is appreciable at the lower value of the channel length but at lower temperature this variation is lower. This is because of the less lattice vibrations.

Threshold voltage was simulated for various pocket profile parameters and temperature conditions. From simulations in Figs. 4.19-4.20, it is observed that metal-

semiconductor work function difference increases, energy band gap decreases, intrinsic carrier concentration increases and Fermi potential increases with temperature. The combined effect of these parameters is that the threshold voltage increases with decreasing temperature as shown in Fig. 4.22. The result is consistent with the already published results in the literature [54].

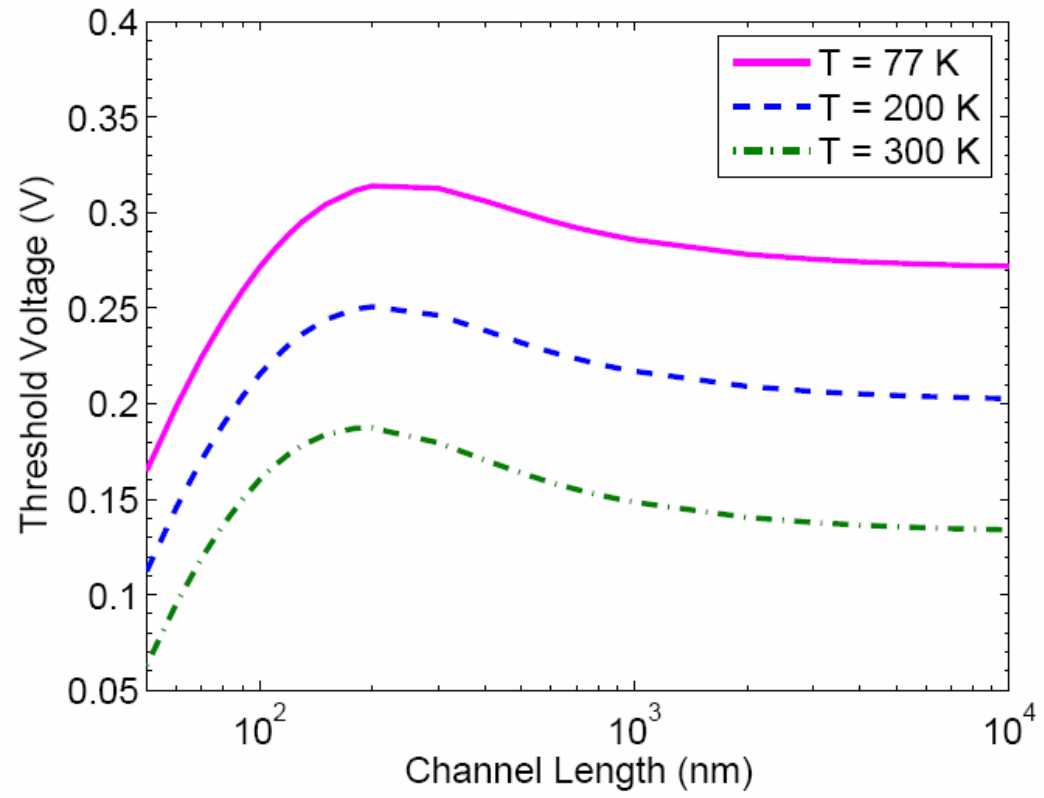

Fig. 4.22 Threshold voltage variation with gate length for various temperatures with drain bias, V_{DS} = 0.05 V and substrate bias, V_{BS} = 0.0 V

Fig. 4.23 shows that at shorter channel lengths threshold voltage variation is negligible when substrate concentration is changed, whereas in longer channel length threshold voltage is more sensitive to substrate bias concentration at low temperature of 77 K. This is further verified in Figs. 4.24-4.25.

Finally, the result is compared with the other pocket doping profiles given in [47]-[48]. The comparison given in Fig. 4.26 shows that the proposed model gives similar results and smooth variation of threshold voltage with gate length at different temperatures without hampering the accuracy to a large extent. This smooth variation is obtained due to the smooth variation of effective doping concentration with the channel length as observed in Fig. 4.17.

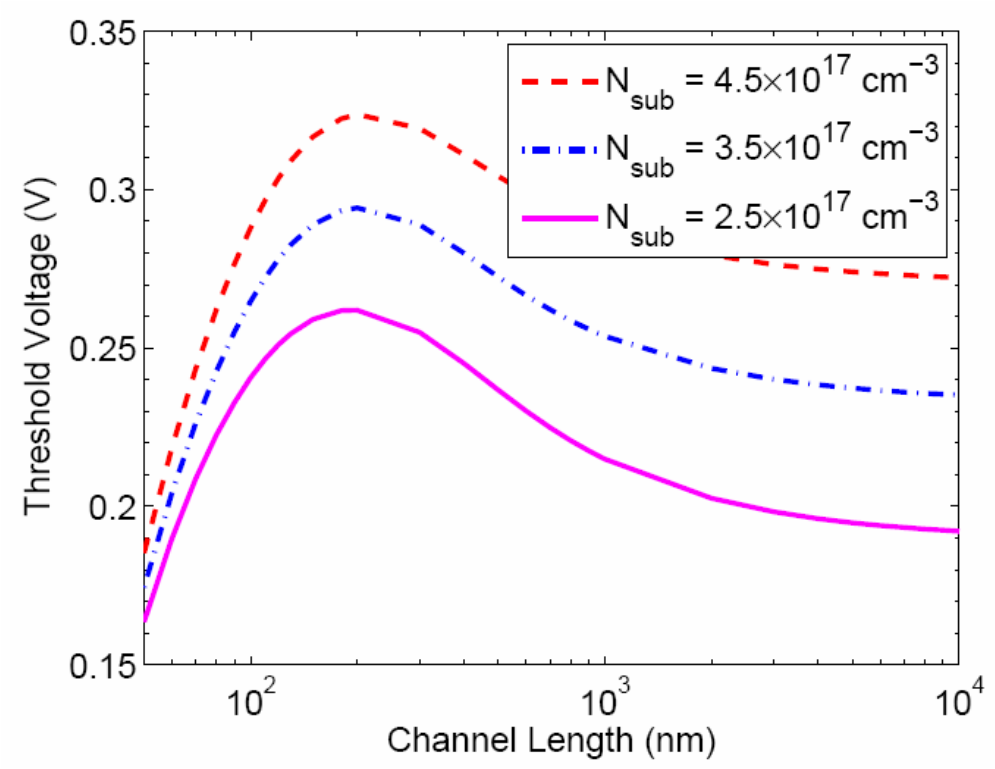

Fig. 4.23 Comparison of threshold voltage variation vs. gate length for various substrate concentrations at temperature of T = 77 K

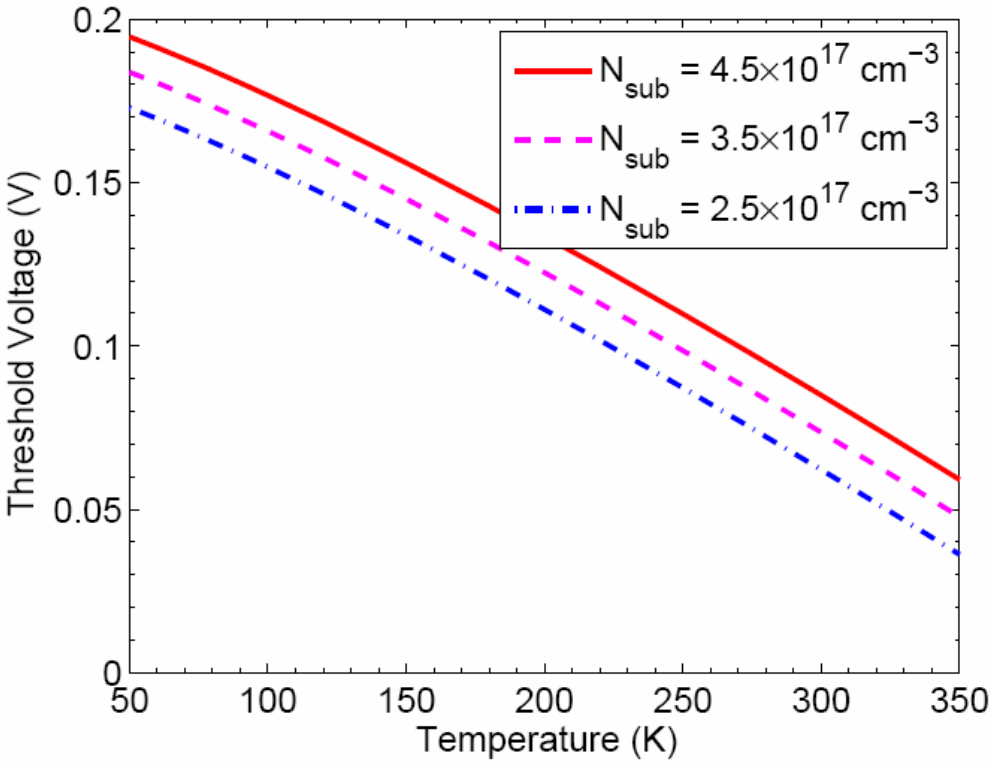

Fig. 4.24 Comparison of threshold voltage variation vs. temperature for various substrate concentrations at gate length, L = 50 nm

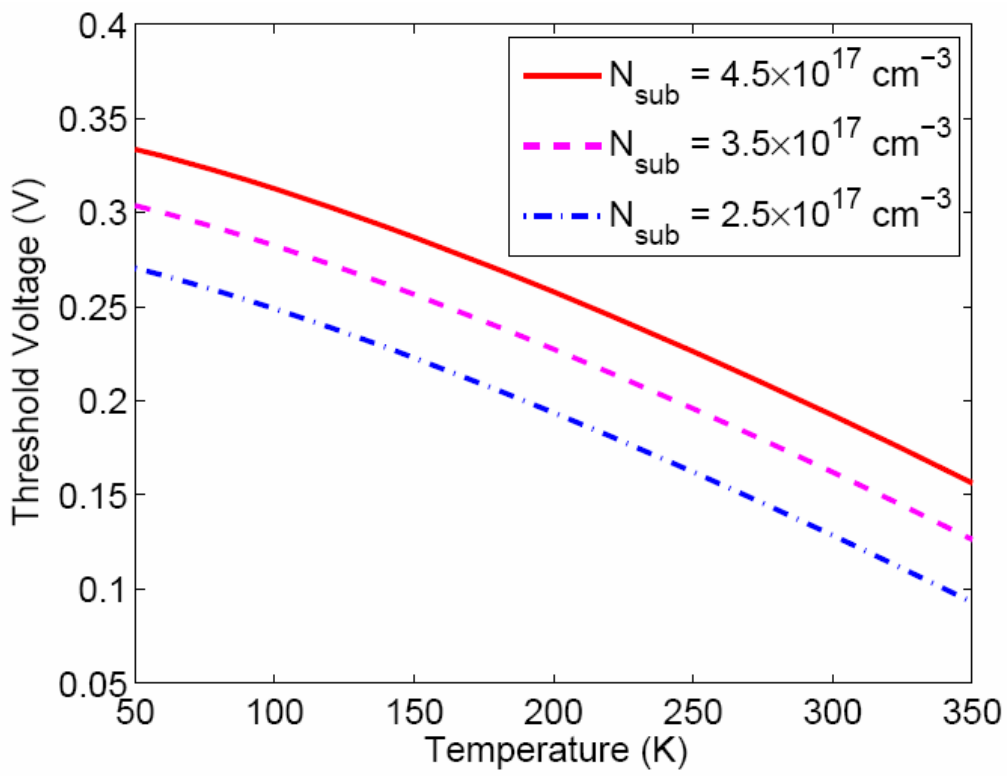

Fig. 4.25 Comparison of threshold voltage variation vs. temperature for various substrate concentrations at gate length, L = 0.25 μm

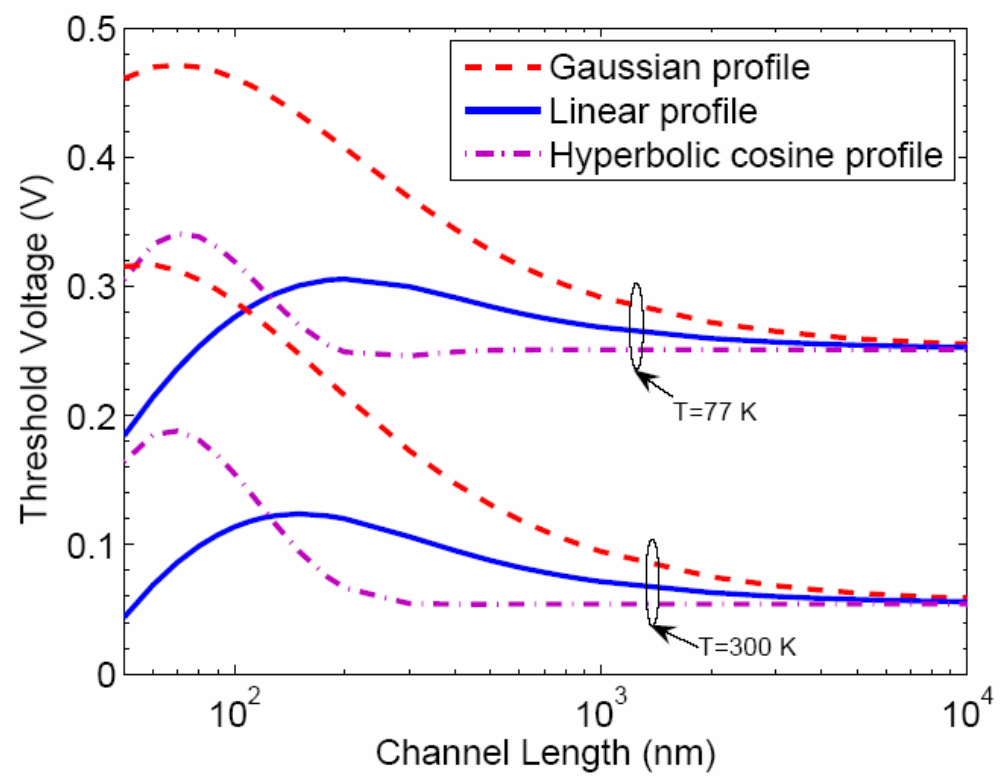

Fig. 4.26 Comparison of threshold voltage variation with gate length for various temperatures

4.4 Inversion Layer Effective Mobility Model

Figs. 4.9-4.10 show threshold voltage variation with gate lengths for different pocket doses and pocket lengths respectively. It has been observed that as the pocket dose or the pocket length is increased the reverse short channel effect increases and thus delays the threshold voltage roll off. Since mobility is affected by the threshold voltage, therefore, variation of pocket dose or pocket length will cause the variation of the effective mobility.

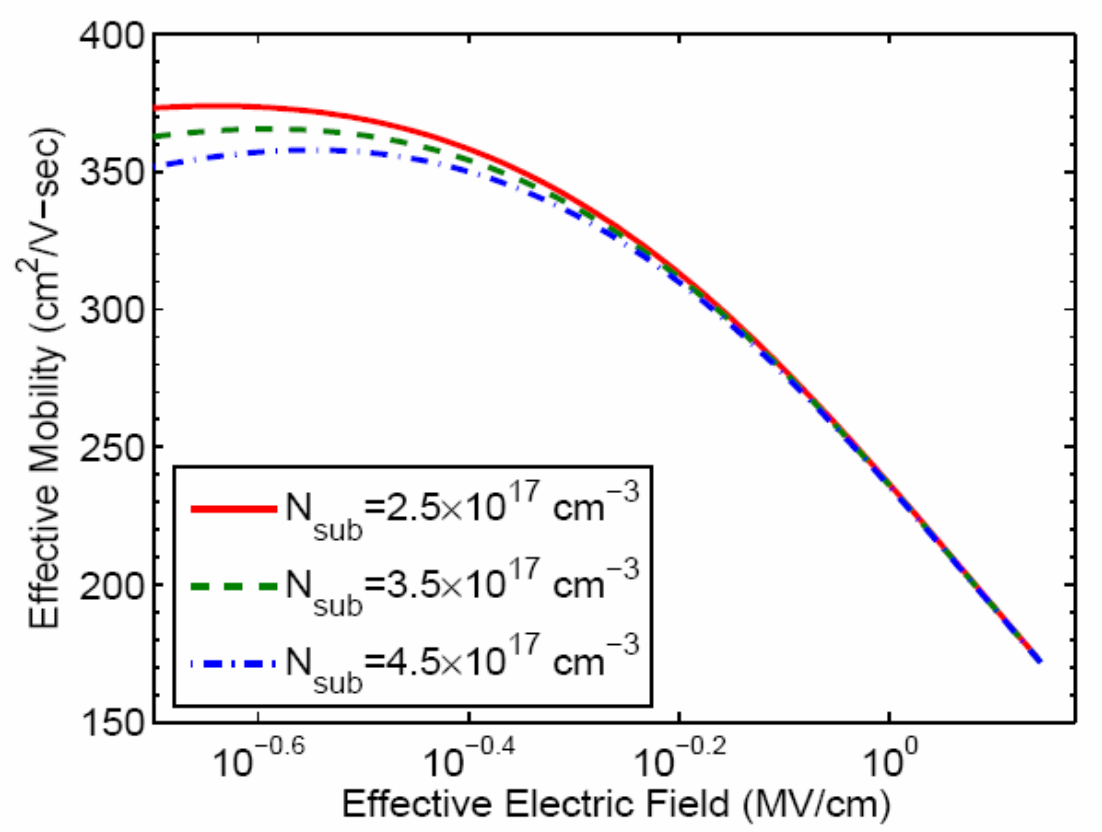

Fig. 4.27 Effective mobility vs. effective electric field for different substrate concentrations (N_{sub}) with L = 0.1 μm, L_p = 25 nm, N_{pm} = 1.75×10^{18} cm^{-3}, V_{DS} = 0.05 V and T = 300K

From the E_{eff} dependence curves of the different types of mobility models as shown in Fig. 3 of [62], it is observed that the phonon scattering and surface roughness scattering mechanisms dominate at the higher value of electric field since the carrier concentration is higher and the mobility due to Coulomb scattering dominates at low value of effective normal electric field due to the low value of inversion charge.

Fig. 4.27 shows that the effective mobility is not changed much with the variation of the substrate doping concentration. But at very low electric fields the effective mobility degrades with the increase of the substrate doping concentration, because then the Coulomb scattering rate dominates over the surface roughness and phonon scattering rate as observed in Fig. 3 of [62]. Because at higher substrate doping more ionized ions are available at the surface.

Fig. 4.28 shows the variation of the effective mobility with the variation of effective electric field for the different channel lengths. It is observed that as the channel length decreases the effective mobility decreases because scattering increases in the device with lower channel length. But at lower values of the electric fields mobility tends to degrade. This can be ascribed to coulomb scattering term at the lower values of effective normal electric fields.

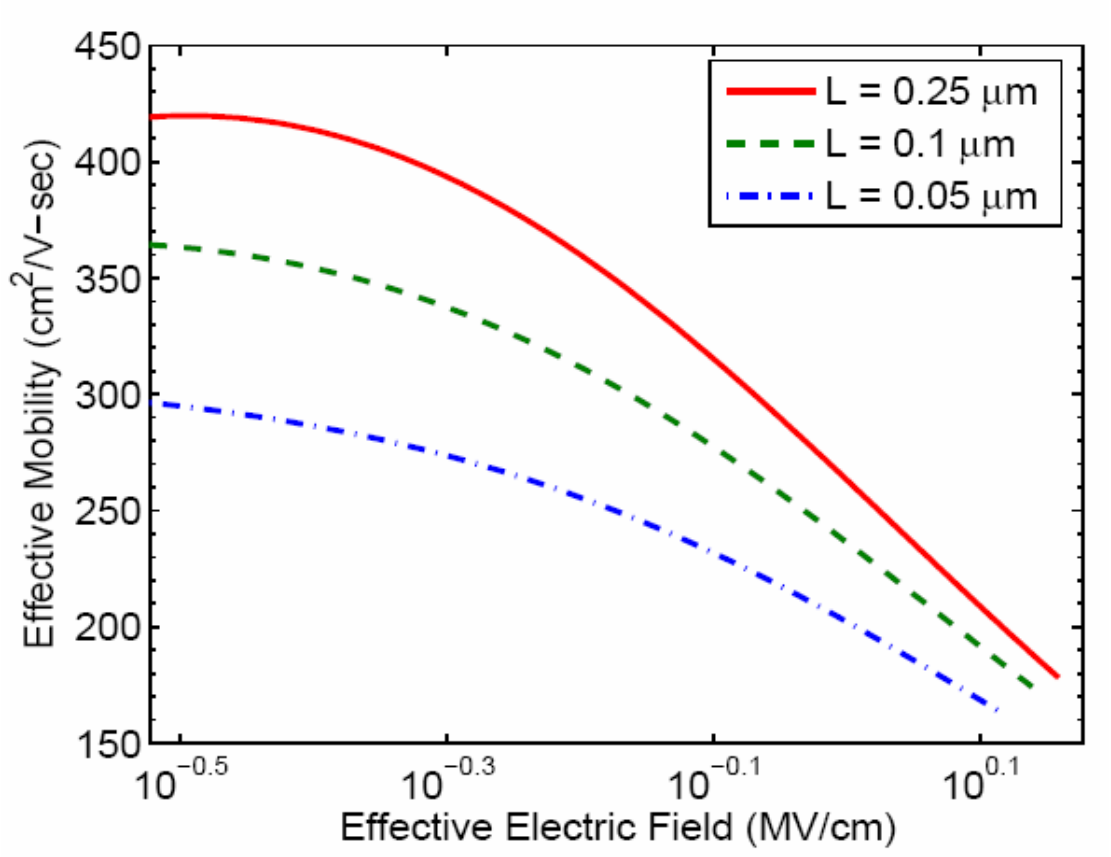

Fig. 4.28 Effective mobility vs. effective electric field for different channel lengths (L) with $N_{sub} = 3.5\times10^{17}$ cm^{-3}, $L_p = 25$ nm, $N_{pm} = 1.75\times10^{18}$ cm^{-3}, $V_{DS} = 0.05$ V and $T = 300$K

Fig. 4.29 shows the variation of the effective mobility with the variation of effective electric field for the different oxide thicknesses. It is observed that as the oxide thickness decreases the effective mobility increases at lower electric fields because now the gate has more control over the channel. This can be ascribed to coulomb scattering term at the lower values of effective normal electric fields. But mobility does not change appreciably when the electric field is very high.

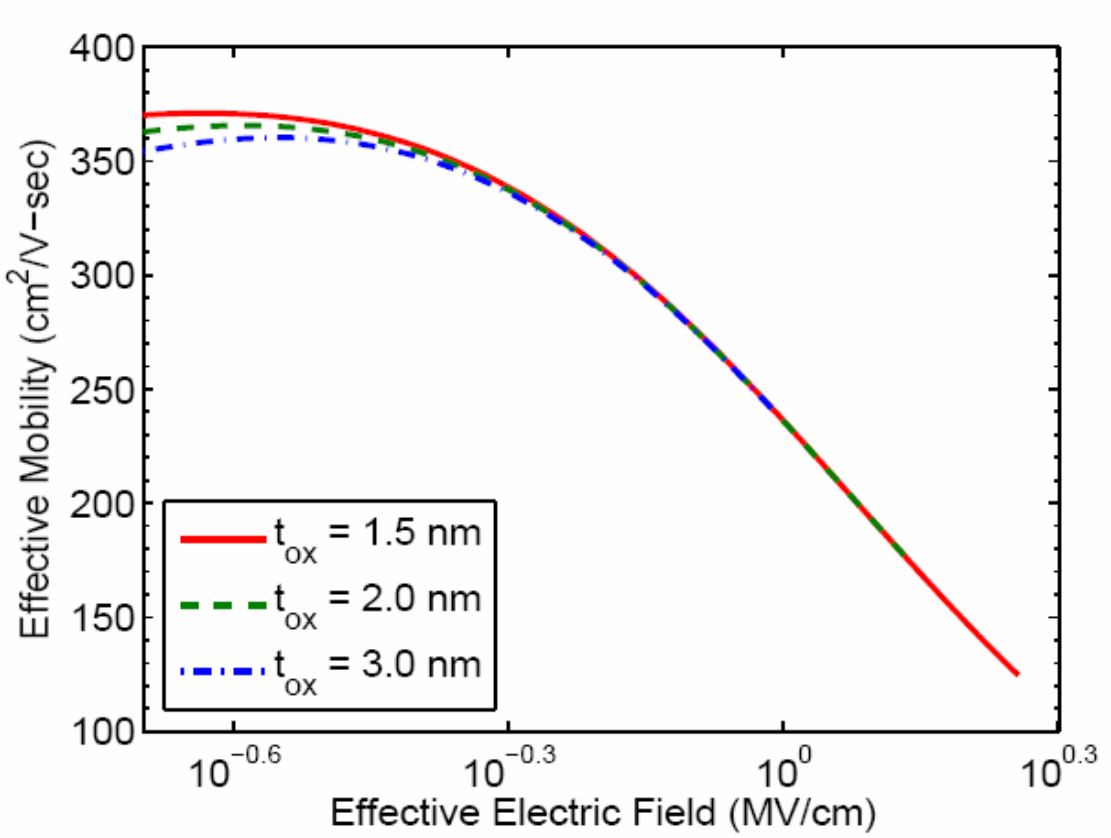

Fig. 4.29 Effective mobility vs. effective electric field for different oxide thicknesses (t_{ox}) with L_p = 25 nm, L = 0.1 μm, N_{sub} = 3.5×10^{17} cm^{-3}, N_{pm} = 1.75×10^{18} cm^{-3}, V_{DS} = 0.05 V and T = 300K

For Figs. 4.30-4.31, the same explanation may be given. That is, increased pocket dose and pocked length cause the effective mobility to degrade at low values of normal electric fields because of the increased Coulomb scattering rate due to the incorporation of the more ions in the channel by the pocket implantation. But at the higher value of the effective normal electric field, there is no deviation in the effective mobility curve due to the change of pocket profile parameters. This holds the universality of the effective mobility curve.

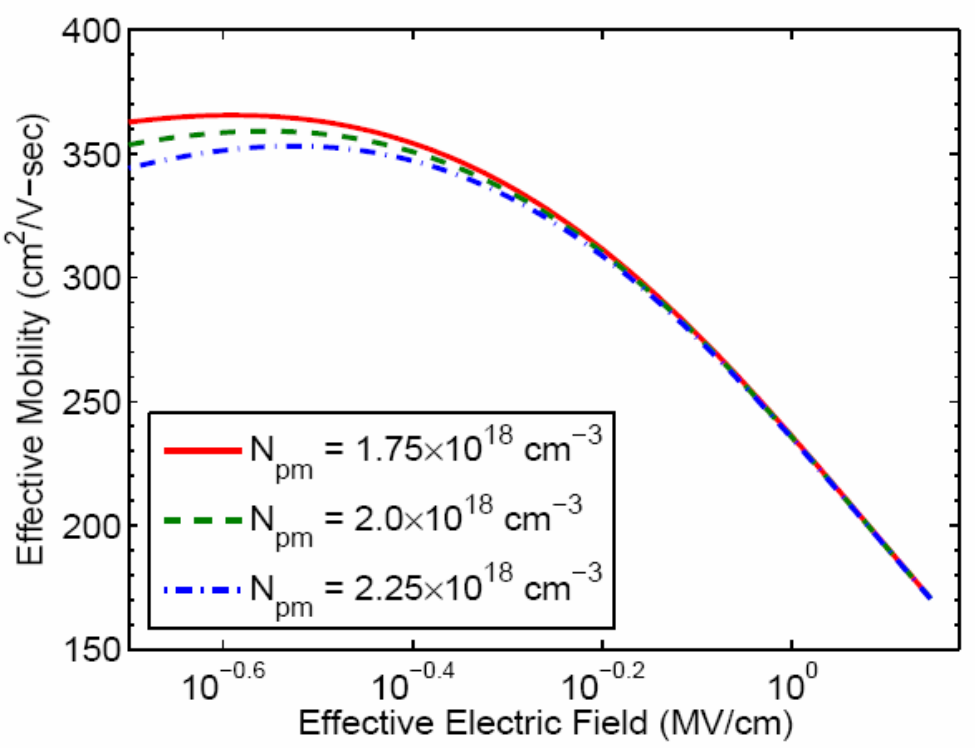

Fig. 4.30 Effective mobility vs. effective electric field for different peak pocket doping concentrations (N_{pm}) with L = 0.1 μm, L_p = 25 nm, N_{sub} = 3.5×10^{17} cm^{-3}, V_{DS} = 0.05 V and T = 300K

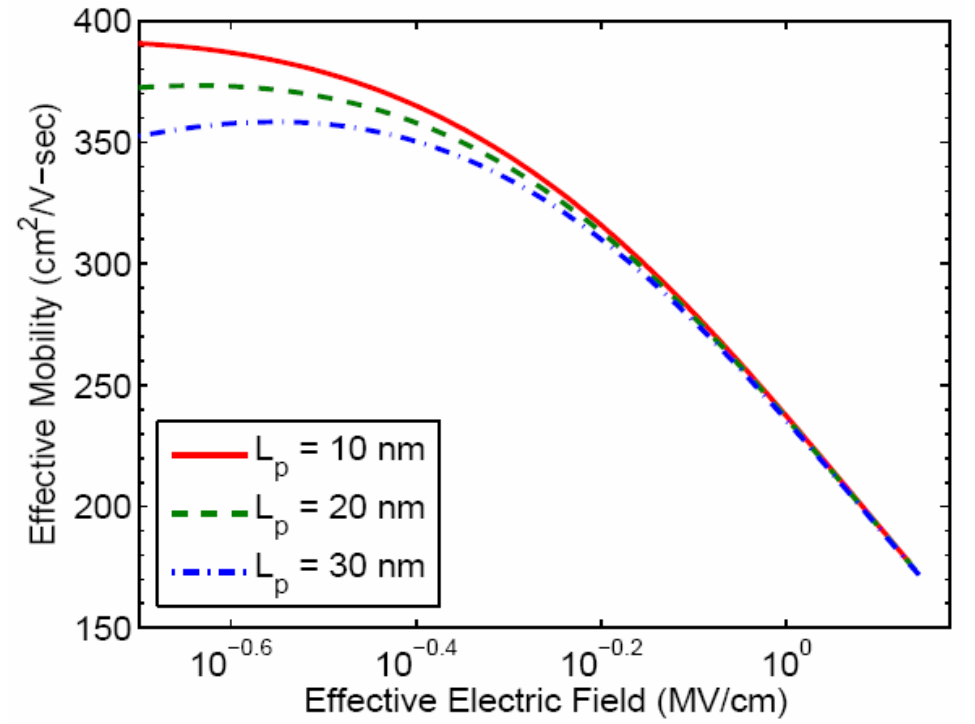

Fig. 4.31 Effective mobility vs. effective electric field for different pocket lengths (L_p) with L = 0.1 μm, N_{sub} = 3.5×10^{17} cm^{-3}, N_{pm} = 1.75×10^{18} cm^{-3}, V_{DS} = 0.05 V, T = 300K

Figs. 4.32-4.33 show the variation of effective mobility with the effective electric field for different temperatures and two different channel lengths of 100 nm and 50 nm. It is observed that as the temperature goes down the effective mobility increases because with the decrease of temperature, carriers scattering is less at the surface. But when the electric field is low then the mobility goes down for a particular temperature because of the increase of the coulomb scattering. Due to pocket implantation, threshold voltage has not decreased until 100 nm, but at 50 nm channel length threshold voltage has already decreased due to SCE as shown in Figs. 4.9-4.10. Hence at the very low values of the effective normal electric field, the mobility curve becomes flat at lower temperature for the shorter channel length device.

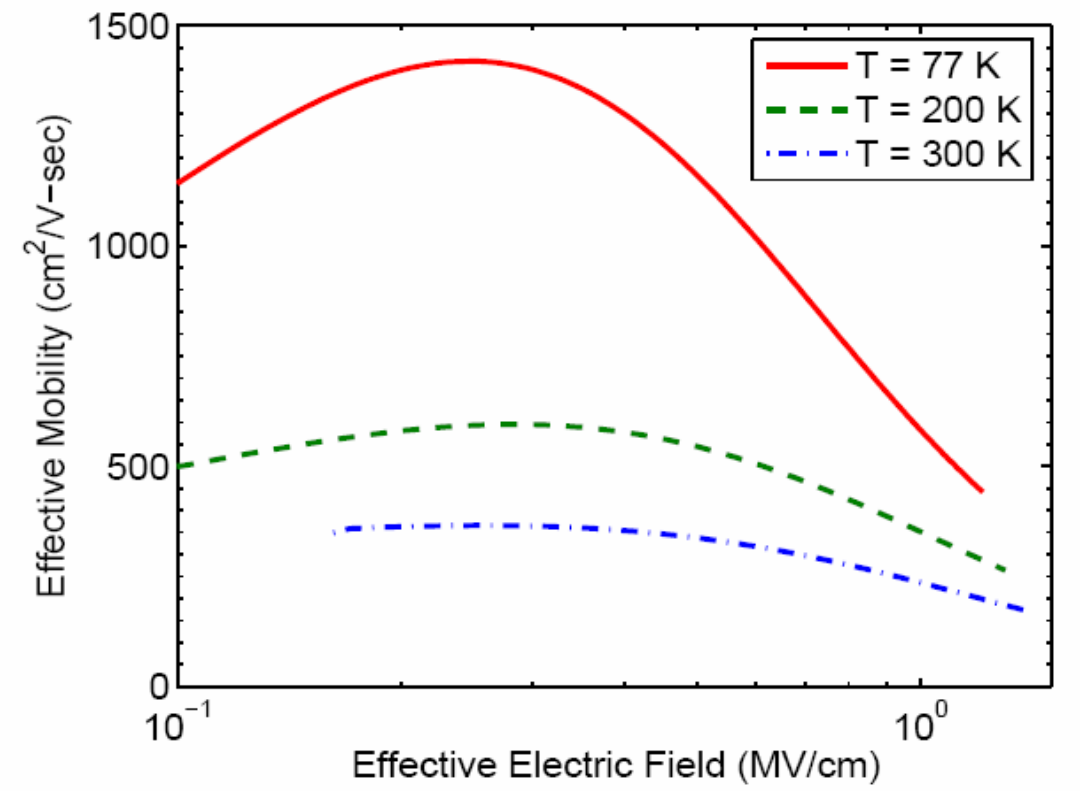

Fig. 4.32 Effective mobility vs. effective electric field for different temperatures (T) with L = 0.1 μm, N_{sub} = 4.5×10^{17} cm^{-3}, L_p = 25 nm, N_{pm} = 1.75×10^{18} cm^{-3} and V_{DS} = 0.05 V

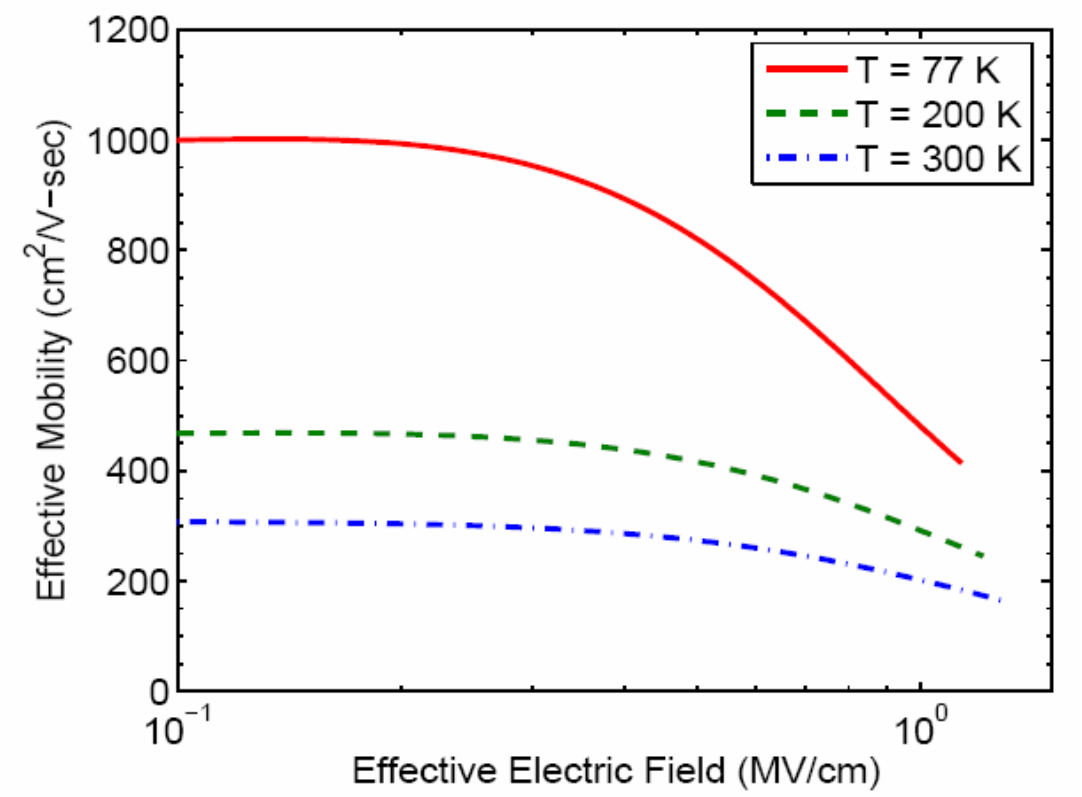

Fig. 4.33 Effective mobility vs. effective electric field for different temperatures (T) with L = 50 nm, L_p = 25 nm, N_{sub} = 4.5×10^{17} cm^{-3}, N_{pm} = 1.75×10^{18} cm^{-3} and V_{DS} = 0.05 V

4.5 Subthreshold Drain Current Model

In order to verify the analytical subthreshold current model for the pocket implanted n-MOSFET, different types of simulations were performed. The proposed surface potential, threshold voltage with bias and temperature effects and mobility models are incorporated in the subthreshold drain current model.

In Figs. 4.34-4.36 subthreshold current variation for different gate voltages are shown for two different drain biases of 0.0.05 V and 2.5 V with different channel lengths of 0.25 μm, 100 nm and 50 nm. It is observed that for longer channel length device, subthreshold current does not change appreciably as the drain bias increases, but for shorter channel length device, subthreshold current changes appreciably as the drain bias increases. This also occurs due to significant DIBL effect.

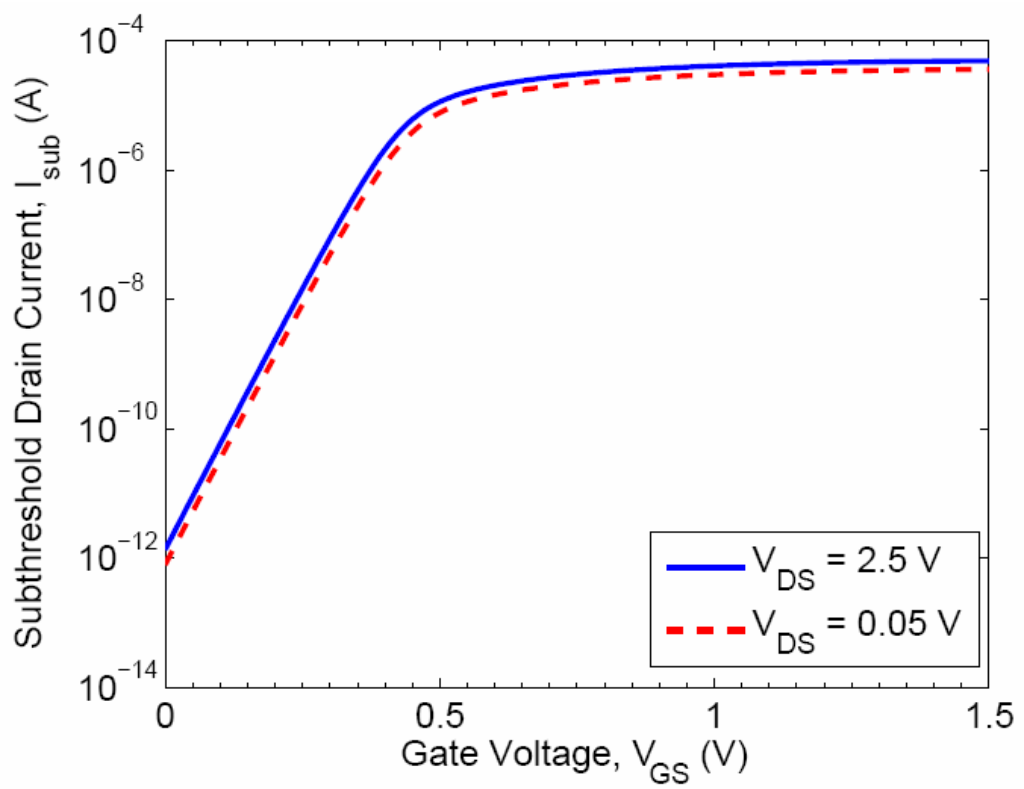

Fig. 4.34 Subthreshold drain current versus gate voltage for two drain biases, V_{DS} = 0.05 V and V_{DS} = 2.5 V with channel length, L = 0.25 μm

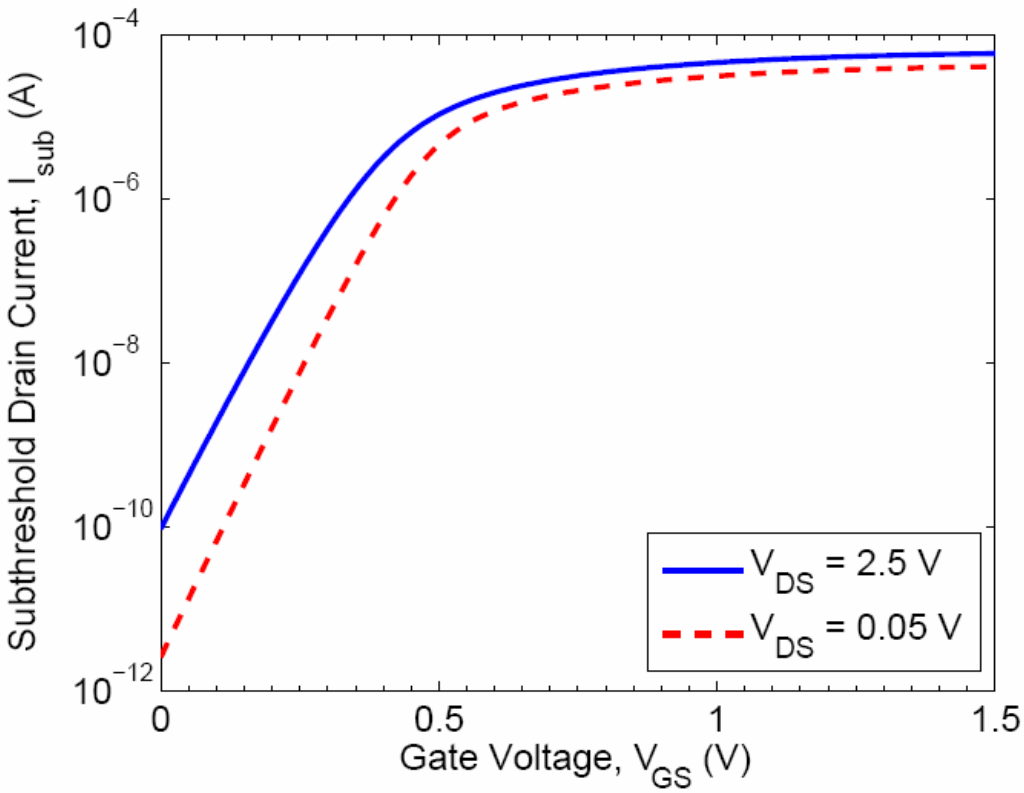

Fig. 4.35 Subthreshold drain current versus gate voltage for two drain biases, V_{DS} = 0.05 V and V_{DS} = 2.5 V with channel length, L = 100 nm

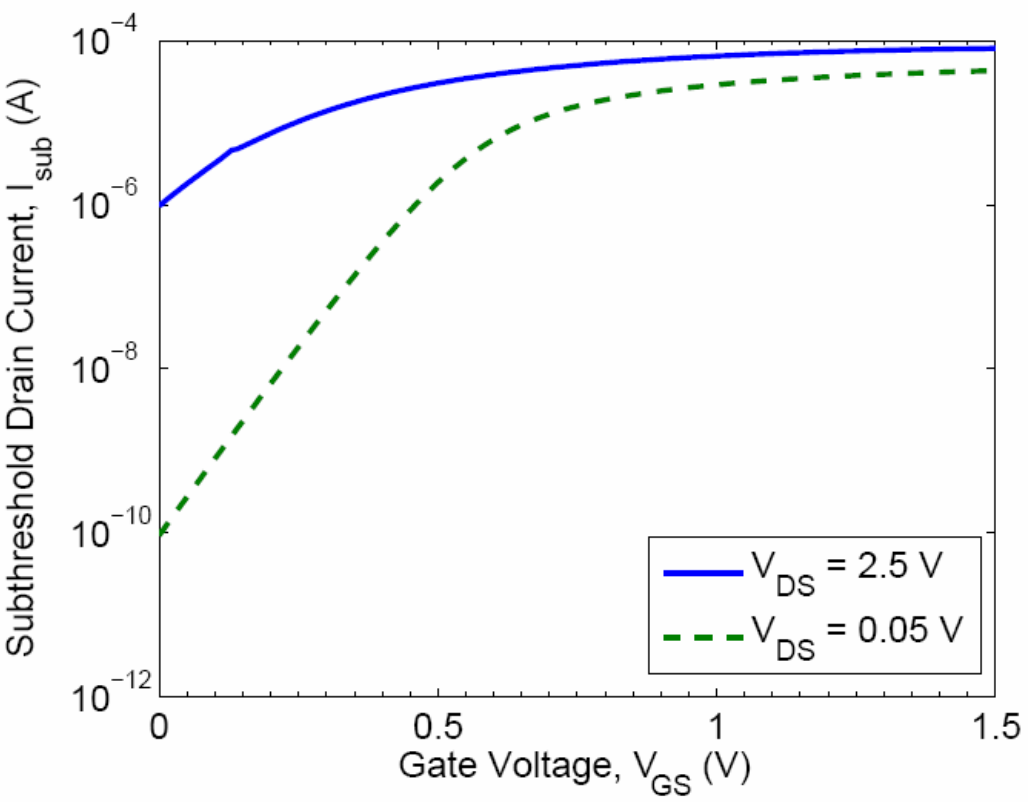

Fig. 4.36 Subthreshold drain current versus gate voltage for two drain biases, V_{DS} = 0.05 V and V_{DS} = 2.5 V with channel length, L = 50 nm

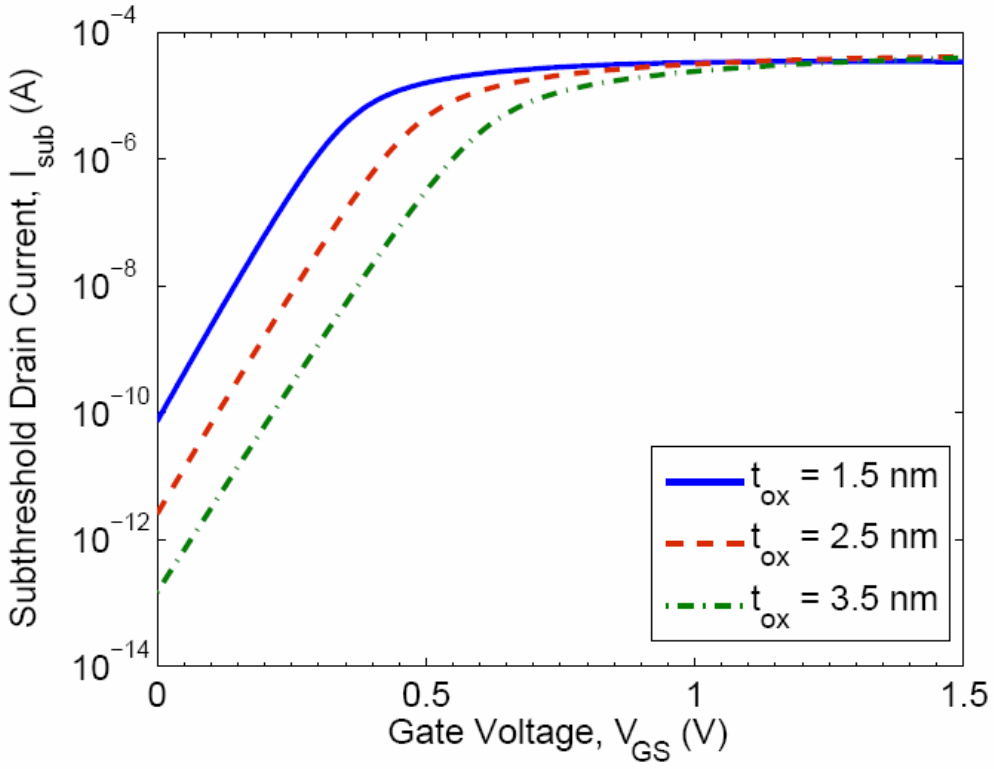

Fig. 4.37 Subthreshold drain current versus gate voltage for different oxide thicknesses with drain bias, V_{DS} = 0.05 V and channel length, L = 100 nm

Fig. 4.37 shows the variation of subthreshold drain current with the gate voltage for three different oxide thicknesses of 1.5, 2.5 and 3.5 nm with peak pocket implant concentration, N_{pm} = 2.5×10^{18} cm^{-3}, pocket length, L_p = 25 nm, channel length, L = 100 nm, substrate bias, V_{BS} = 0.0 V and drain bias, V_{DS} = 0.05 V. It is observed that as the oxide thickness increases, the subthreshold current decreases for the same applied gate bias and drain bias. This happens due to the less control on the inversion layer charge when oxide thickness increases.

Fig. 4.38 shows the variation of subthreshold drain current with the gate voltage for three different peak pocket implant concentration of N_{pm} = 2.5×10^{18} cm^{-3}, 1.5×10^{18} cm^{-3} and 1.0×10^{18} cm^{-3} and drain bias of V_{DS} = 0.05 V with channel length, L = 100 nm and pocket length, L_p = 25 nm. It is observed that as the peak of the pocket implant concentration increases, the subthreshold current decreases for the same applied gate bias and drain bias. This happens due to the additional doping atoms of pocket implantations present near the source and drain edges. It is also observed that as the peak pocket implant concentration decreases further then the subthreshold slope decreases. Because then the RSCE diminishes. This is expected from the pocket implanted n-MOSFET for short channel devices.

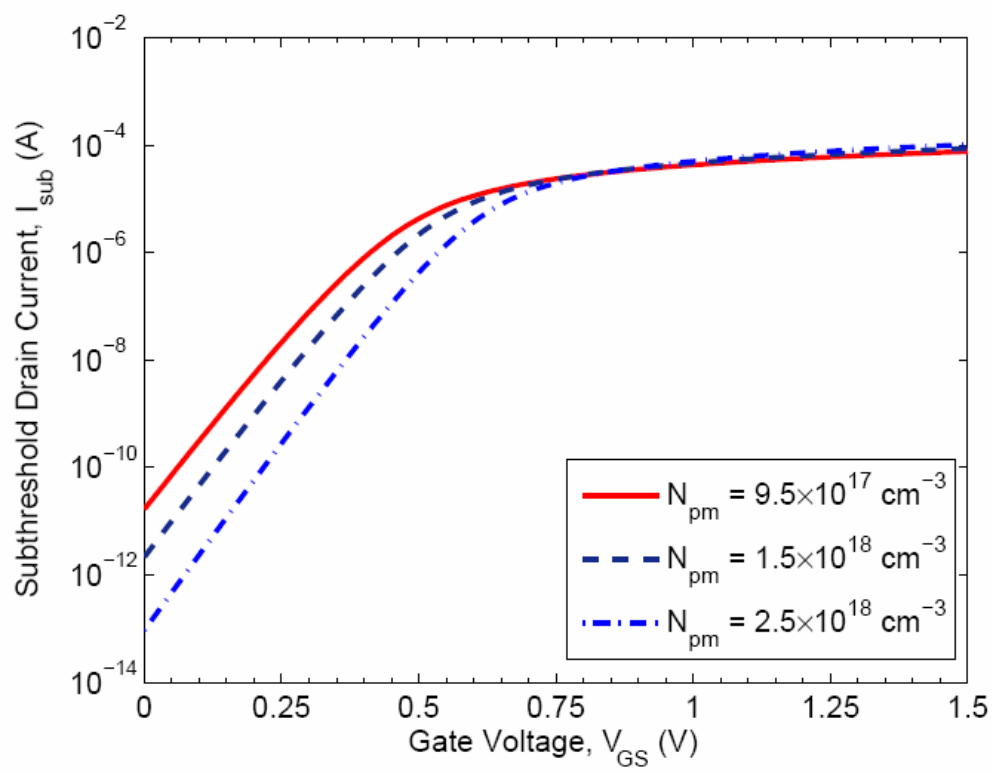

Fig. 4.38 Subthreshold drain current versus gate voltage for three different peak pocket implant concentrations, drain bias, V_{DS} = 0.05 V with L = 100 nm

Fig. 4.39 shows the variation of subthreshold drain current with the gate voltage for three different pocket lengths of L_p = 30 nm, 25 nm and 20 nm and drain bias of V_{DS} = 2.5 V with channel length, L = 100 nm and peak pocket implant concentration of N_{pm} = 2.5×10^{18} cm^{-3}. It is observed that as the pocket length increases, the subthreshold drain current decreases for the same applied gate bias. This also happens due to the additional doping atoms of pocket implantation present near the source and drain edges. But subthreshold slope does not change significantly with the variation of pocket length. That is, variation of peak pocket concentration has greater effect than variation of pocket length on subthreshold current.

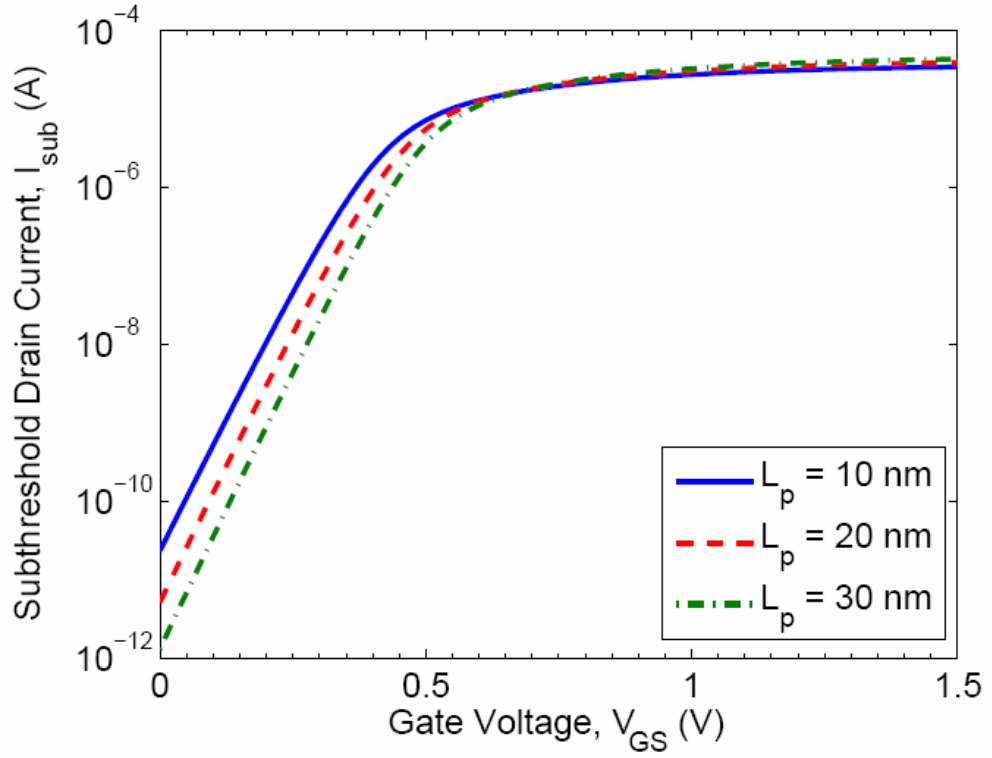

Fig. 4.39 Subthreshold drain current versus gate voltage for three different pocket lengths and drain bias, V_{DS} = 0.05 V with channel length, L = 100 nm

Figs. 4.40-4.42 show the variation of subthreshold current for a set of substrate biases (V_{BS}) of 0 V, -0.5 V and -1 V with different channel lengths (L) of 0.25 μm, 100 nm and 50 nm respectively and drain bias (V_{DS}) of 0.05 V. It is observed that the subthreshold current decreases with increasing substrate bias in the negative direction for the same applied gate and drain voltage. The results are in consistent with the substrate bias effect on subthreshold current found in the literature. But it has also been observed that the amount of current increment with increasing gate voltage is

less, and the subthreshold slope decreases more rapidly as the gate voltage increases in the shorter channel length device.

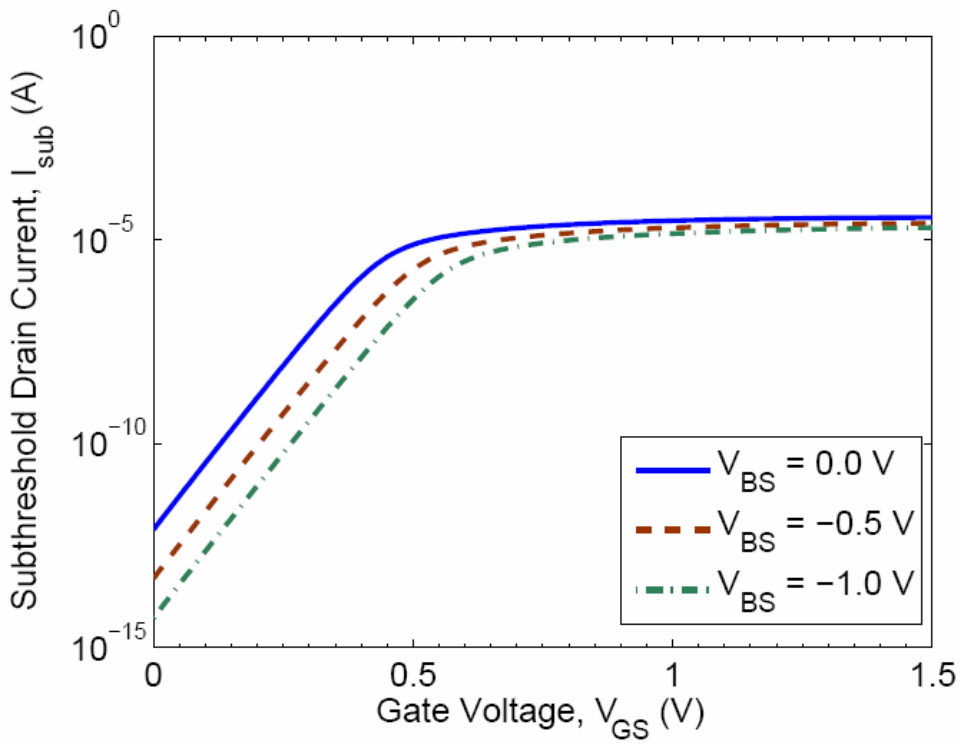

Fig. 4.40 Subthreshold drain current versus gate voltage for different substrate biases with V_{DS} = 0.05 V and L = 0.25 μm

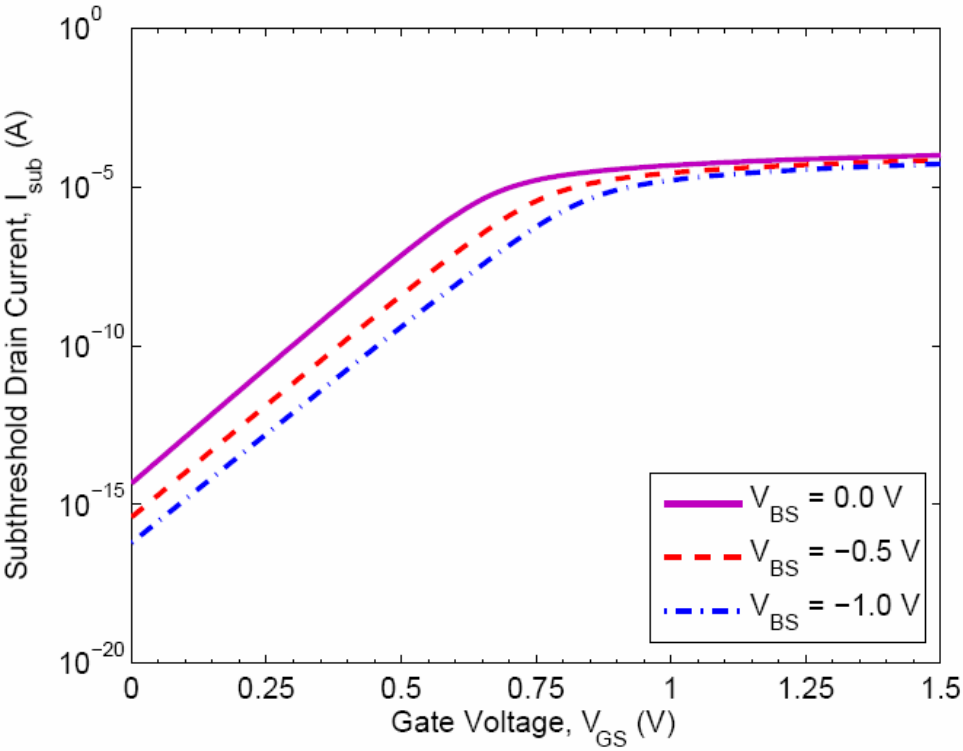

Fig. 4.41 Subthreshold drain current versus gate voltage for different substrate biases with V_{DS} = 0.05 V and L = 100 nm

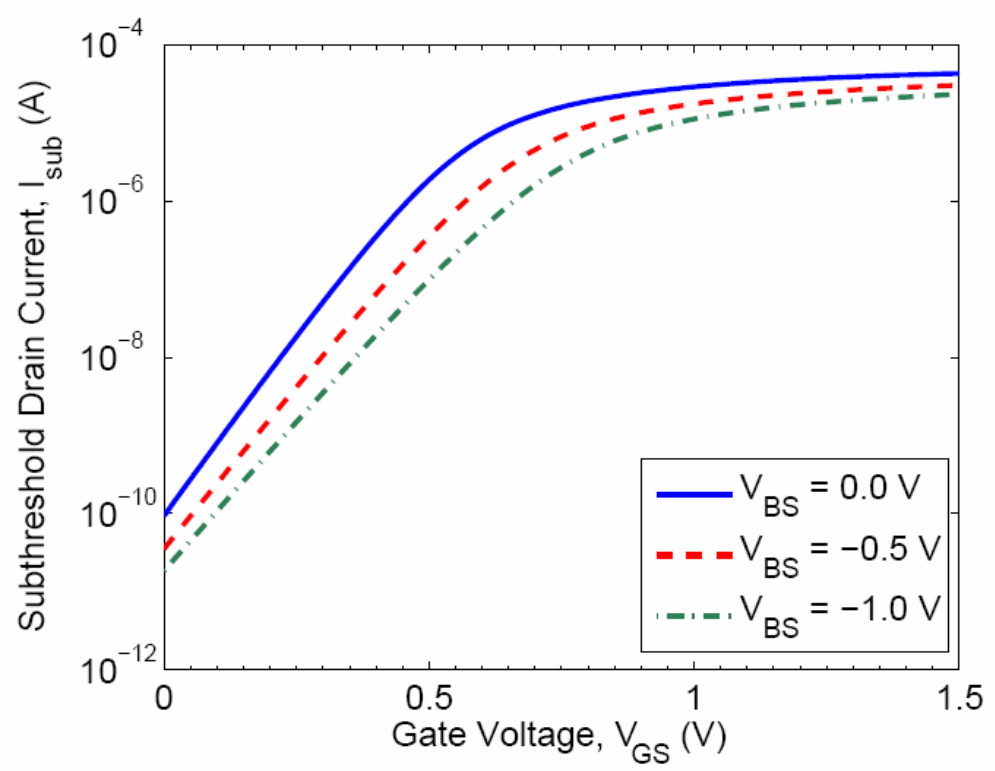

Fig. 4.42 Subthreshold drain current versus gate voltage for different substrate biases, V_{BS} = 0.0 V, -0.5 V and -1.0 V with drain bias, V_{DS} = 0.1 V and L = 50 nm

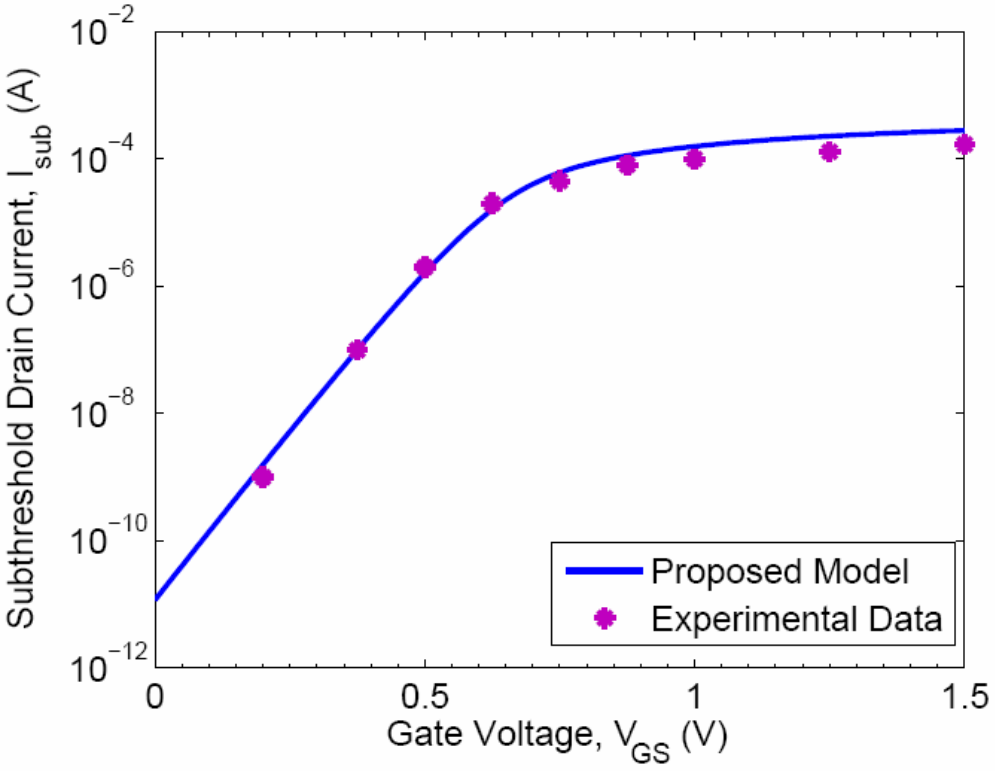

Fig. 4.43 Fitting experimental data already published in the literature [70] with the simulated results of the proposed subthreshold drain current model

In Fig. 4.43, experimental data from [70] is fitted to the simulated data for the device parameters given in [70]. The parameter values are- substrate concentration, N_{sub} = 5.5×1017 cm^{-3}, peak pocket concentration, N_{pm} = 8.0×1017 cm^{-3}, pocket length along the channel, L_p = 40 nm either from source or drain side, oxide thickness, t_{ox} = 4 nm, junction depth, r_j = 50 nm, substrate bias, V_{BS} = 0.0 V and drain bias, V_{DS} = 0.05 V. From Fig. 4.43, it is clear that the simulated data agrees well with the experimental data in [70] of the subthreshold region. By changing the process conditions, it is possible to adjust the experimental results with the simulated data.

4.6 Low Frequency Drain Current Flicker Noise Model

Fig. 4.9 shows threshold voltage variation with gate lengths for two different pocket doses. It has been observed that as the peak pocket concentration and hence the pocket dose is increased the reverse short channel effect increases. It also delays the threshold voltage roll off, but the threshold voltage roll-up happens at longer channel length. If the peak pocket concentration is increased further then the SCE starts to vanish. That is, the higher the pocket dose the higher the RSCE and thereby eliminating the effect of SCE.

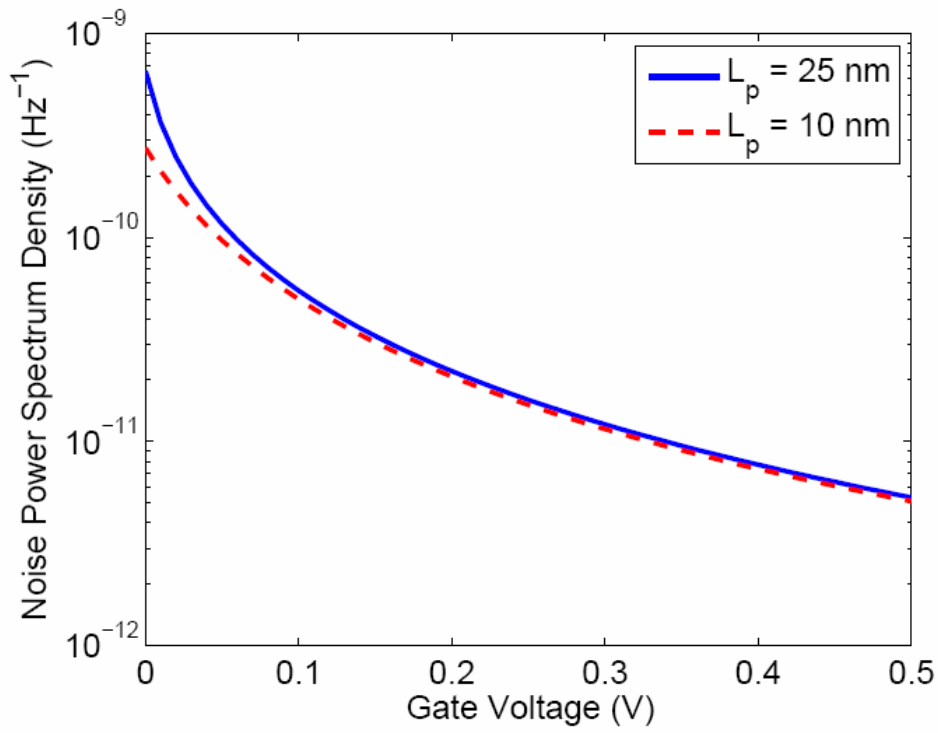

Fig. 4.44 Noise power spectrum density vs. gate voltage for different pocket lengths with L = 50 nm, N_{pm} = 1.25×10^{18} cm^{-3}, V_{DS} = 0.2 V and f = 100 Hz

Fig. 4.44 shows the noise behavior for two different pocket lengths. Pocket lengths have little effect on noise behavior. Only for the lower gate bias, the noise increases when the pocket length is increased. But as shown in Fig. 4.45, the noise behavior is affected seriously by the peak pocket concentrations. The model is simulated for a very low frequency of 100 Hz and at a low drain bias of 0.2 V. As the gate bias is increased the noise is decreased. Also for the higher gate bias, the noise does not increased much for the increment of the pocket dose. It is also observed that for a particular gate bias noise behavior is worse for the higher pocket dose.

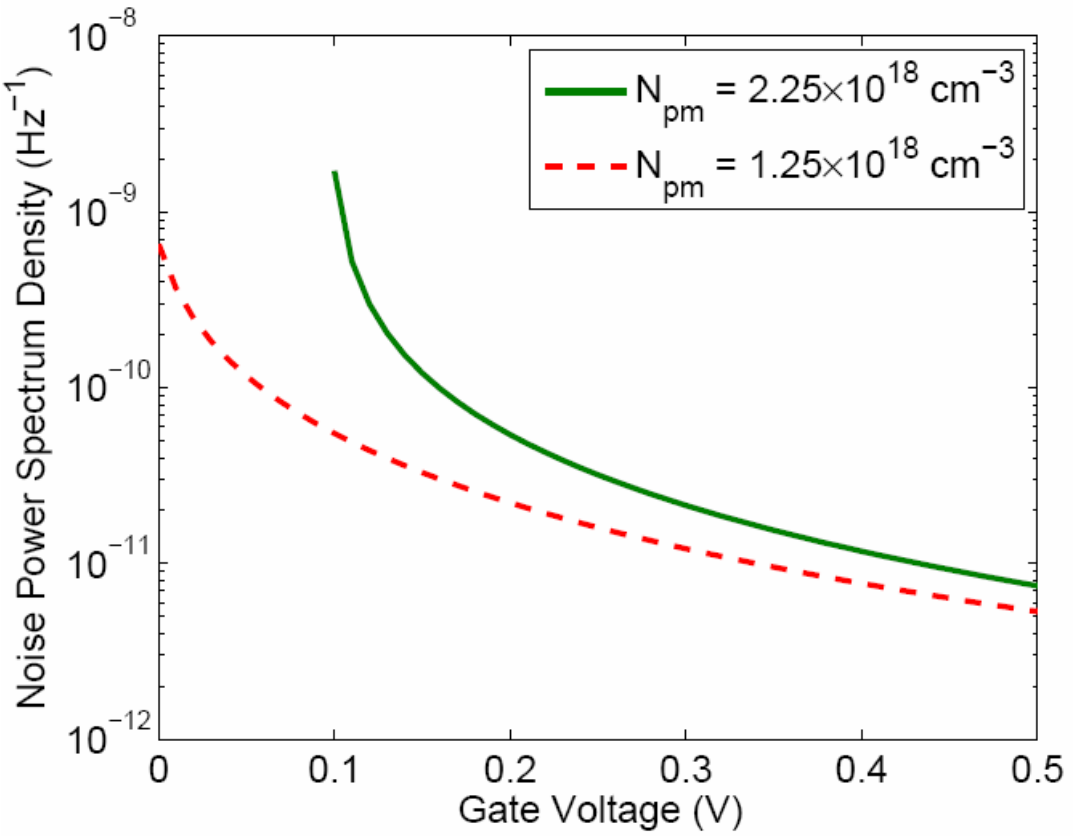

Fig. 4.45 Noise power spectrum density vs. gate voltage for two pocket doses with L = 50 nm, L_p = 25 nm, V_{DS} = 0.2 V and f = 100 Hz

Fig. 4.46 shows that as the drain bias is increased the noise is improved. At higher gate bias, the decrement of noise is smaller for the higher drain bias than that at the lower gate bias, but at lower gate bias as the drain bias is increased the noise is improved at higher rate. As drain bias increases, threshold voltage decreases at 50 nm channel length and hence gate over drive voltage increases and finally, the noise power spectrum density decreases. This is can be attributed to the increase of the

lateral electric field with the increase of the drain bias thereby increasing the drift velocity of the electrons in the inversion channel and thus electrons get less time for thermal agitation in the channel.

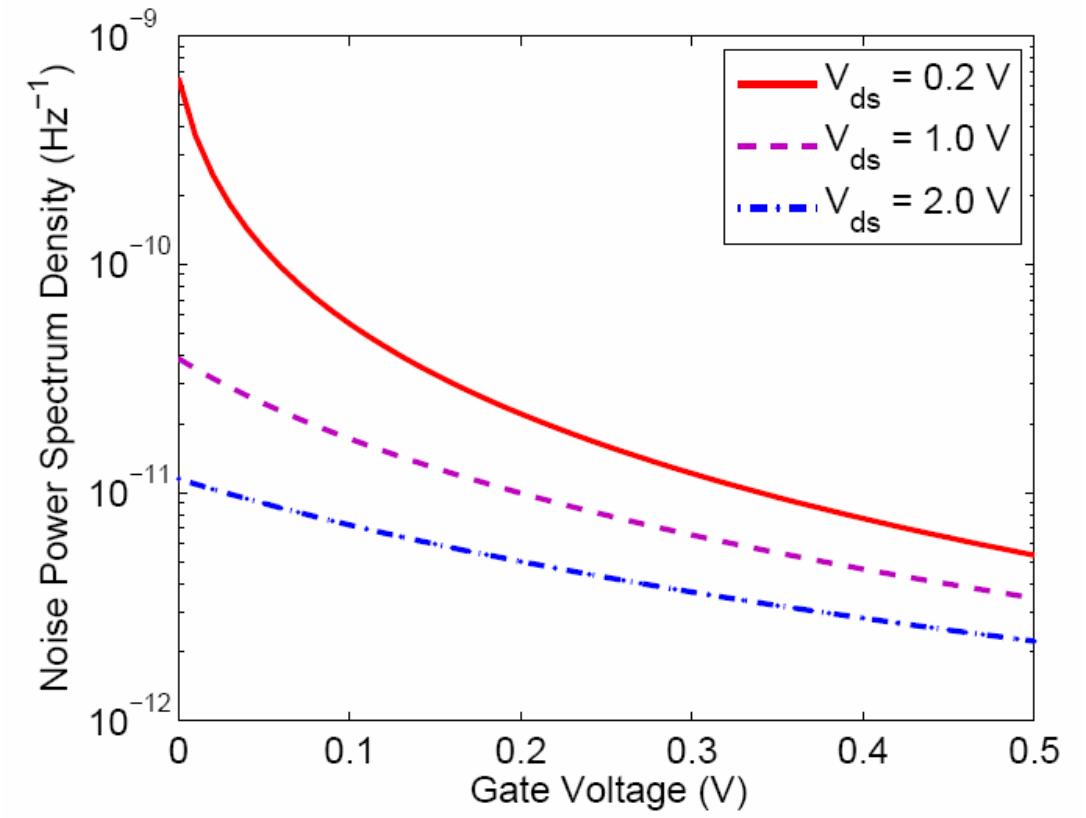

Fig. 4.46 Noise power spectrum density vs. gate voltage for different drain biases with L = 50 nm, N_{pm} = 1.25×10^{18} cm^{-3}, L_p = 25 nm and f = 100 Hz

Fig. 4.47 shows the noise power spectrum density variations with the gate length for two different pocket doses at gate and drain bias of 0.5 V and 0.2 V respectively. It is noted that the noise degradation is more significant in shorter channel length device as pocket implant region is comparable with the channel length of the device. For longer channel length, the noise is not changed with the increment of the peak pocket implantation dose.

Fig. 4.48 shows the noise power spectrum density variations with the gate length for two different oxide thicknesses at gate and drain biases of 0.5 V and 0.2 V respectively. It is noted that the noise degradation is more significant when the oxide thickness is higher. Because when oxide thickness increases there are more chances for the interface trap charges to reside in the oxide layer.

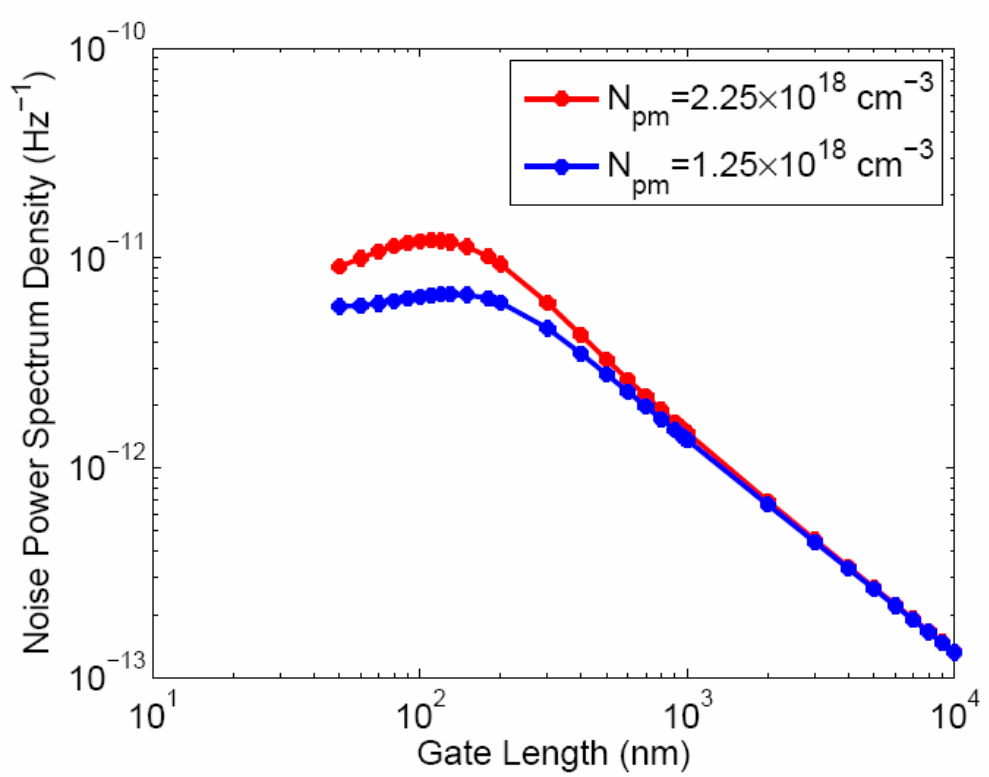

Fig. 4.47 Noise power spectrum density vs. gate length for two pocket doses with L_p = 25 nm, V_{GS} = 0.5 V, V_{DS} = 0.2 V and f = 100 Hz

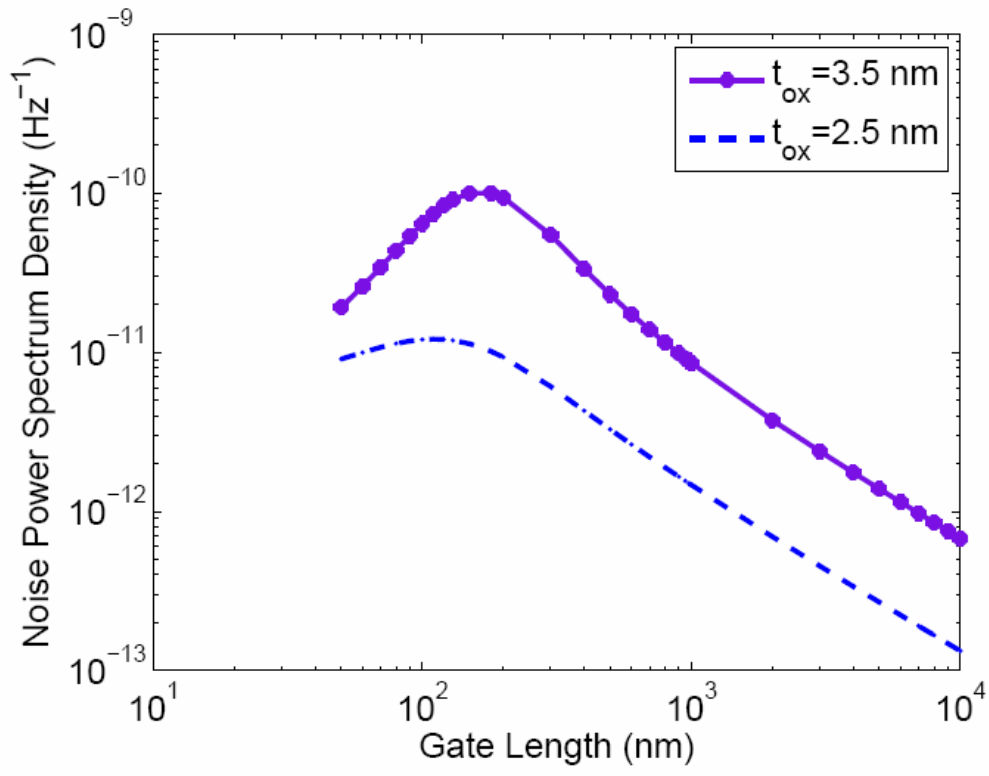

Fig. 4.48 Noise power spectrum density vs. gate length for different oxide thicknesses with N_{pm} = 2.25×10^{18} cm^{-3}, L_p = 25 nm, V_{GS} = 0.5 V, V_{DS} = 0.2 V and f = 100 Hz

In Fig. 4.49, the noise behavior is shown with the gate biases for different oxide thicknesses. As the oxide thickness is increased for a particular gate voltage the noise behavior is worse. At lower gate bias the noise increases rapidly. When oxide thickness increases, noise increases.

In Fig. 4.50, experimental data from [78] is fitted with the simulated data for the device parameters given in [78]. The parameter values are- substrate concentration, $N_{sub} = 5.5\times10^{17}$ cm^{-3}, peak pocket concentration, $N_{pm} = 2.25\times10^{17}$ cm^{-3}, pocket length along the channel, $L_p = 71$ nm either from source or drain side, oxide thickness, $t_{ox} = 5.8$ nm, substrate bias, $V_{BS} = 0.0$ V and drain bias, $V_{DS} = 0.2$ V, frequency, $f = 100$ Hz, channel length, $L = 0.32$ µm, channel width, $W = 10.0$ µm, threshold voltage for the center region of the channel, $V_T = 0.43$ V and threshold voltage for the pocket region of the channel, $V_{Tp} = 0.61$ V. From Fig. 4.50, it is clear that the simulated data almost agrees with the experimental data in [78]. It is possible to adjust the experimental results with the simulated data by changing the process conditions.

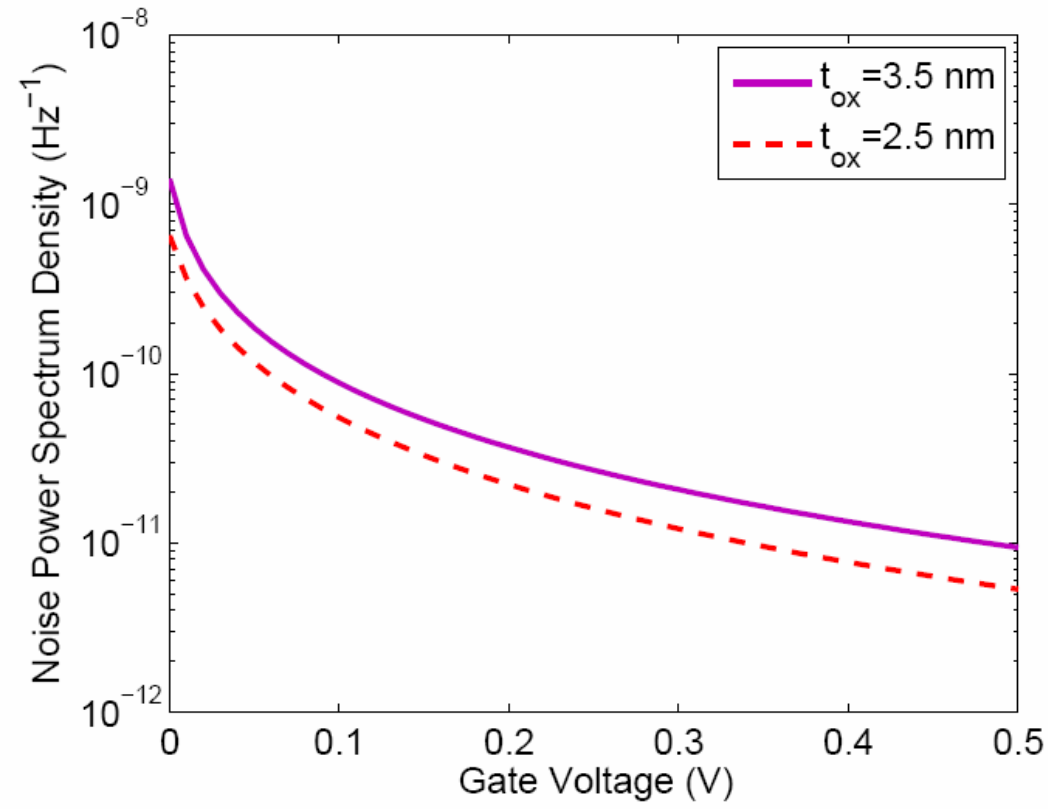

Fig. 4.49 Noise power spectrum density vs. gate bias for different oxide thicknesses with $N_{pm} = 1.25\times10^{18}$ cm^{-3}, $L_p = 25$ nm, $V_{GS} = 0.5$ V, $V_{DS} = 0.2$ V and $f = 100$ Hz

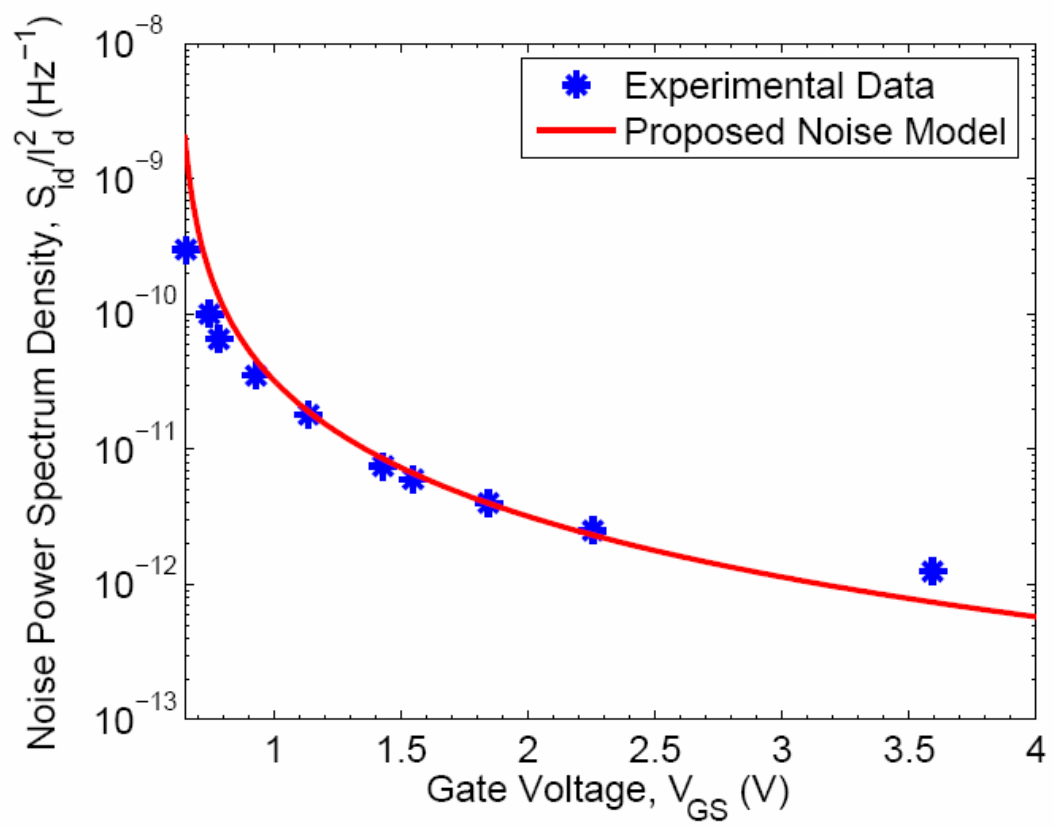

Fig. 4.50 Fitting experimental data already published in the literature [78] with the simulated results of the proposed low frequency drain current flicker noise model

4.7 Summary

In this chapter, all the simulation results for different analytical models of the pocket implanted n-MOSFET have been presented for different device and pocket profile parameters as well as various bias conditions. Explanations of each figure have also been provided. Comparisons of the linear pocket profile model have been made with the other pocket doping profile models found in the literatures. Using the other pocket profile models, the proposed analytical models have been simulated and compared also. Besides, threshold voltage, subthreshold drain current and low frequency drain current flicker noise models are also verified with the experimental data published in the literatures. In the next chapter, conclusions will be presented and few suggestions on further works on the modeling of the pocket implanted n-MOSFET or future extensions of these models will be provided.

Chapter 5

Conclusions

5.1 Conclusions

Different analytical models for ultra thin oxide and nano scale pocket implanted n-MOSFET have been developed. The device structure and the fabrication processes of the pocket implanted n-MOSFET are discussed. Then an efficient pocket doping profile characterization technique using scanning capacitance microscope (SCM) has also been suggested with associated diagrams found in the literatures. The models for the pocket doping are developed assuming two linear pocket doping profiles along the channel at the surface of the pocket implanted n-MOSFET from the source and drain edges towards the center of the channel region. Using these linear pocket doping models, different analytical models for surface potential, threshold voltage, inversion layer effective mobility, subthreshold drain current and low frequency drain current flicker noise have been developed.

The surface potential model satisfies all the boundary conditions and predicts the surface potential at all conditions very well. Then the model is simulated incorporating the other pocket doping profiles found in the literatures. It is observed that the linear pocket doping profile model predicts the surface potential very well. The well-known Reverse Short Channel Effect (RSCE) has been observed through the proposed threshold voltage model incorporating drain and substrate bias effects. The low temperature operation has also been studied by including different temperature dependent parameters in the proposed threshold voltage model. The comparison of the proposed threshold voltage model assuming linear pocket profiles with the other two pocket profile models found in the literature show that the proposed model produces similar results without hampering the accuracy level to a large extent but reduces the simulation time. Experimental results of the threshold voltage for the pocket implanted n-MOSFET already published in the literature fit well with the proposed model. Inversion layer effective mobility model is developed by incorporating all the

scattering mechanisms and ballistic phenomena. The model is also simulated for different device and pocket profile parameters. The simulation predicts the similar results found in the literature. Then using the proposed surface potential, threshold voltage and inversion layer effective mobility models, a subthreshold drain current model is developed based on drift-diffusion equation. This model is also simulated for various bias conditions as well as different device and pocket profile parameters. The simulation results fit very well with the experimental results of the subthreshold drain current for the pocket implanted n-MOSFET published in the literature. Finally, using the proposed threshold voltage model, a low frequency drain current flicker noise model has been developed for the same device. This model is simulated by changing the pocket profile and device parameters as well as bias conditions. Experimental data of the flicker noise published in the literature fits well with the proposed model. It is found that the proposed models efficiently determine different operational parameters of the pocket implanted ultra thin oxide nano scale n-MOSFET. Therefore, these models are very useful for circuit simulation of the pocket implanted n-MOSFET having channel length in the nano scale regime and can also be utilized to study and characterize the pocket implanted advanced ULSI devices.

5.2 Limitations of the Work

The proposed surface potential model can not predict the change of surface potential due to the effect of 2-D potential distribution. The threshold voltage model can not predict the 2-D effect and the effect of energy quantization due to the channel lengths in the nano scale regime. The inversion layer effective mobility model does not include the quantum mechanical effects. More parameters of the pocket implanted n-MOSFET still needs to be modeled.

5.3 Future Scopes

Research work is a continuous process. So, it is important to think about the scopes of the further extension of the current research work. In this work, few models for the ultra thin oxide nano scale pocket implanted n-MOSFET have been analyzed . This work also has several possible extensions that could be attempted as ongoing research work. Some specific recommendations based on the present work are given in the following paragraphs.

As the MOSFET channel length scaled in to the nano scale regime, the SiO$_2$ (insulator) becomes ultra-thin (i.e., thickness below 4 nm). This causes a significant increase in quantum effects near the Si-SiO$_2$ interface by shifting the average inversion charge density away from the interface to the bulk, reducing the charge density to be zero at the interface, increasing the effective oxide thickness over the physical thickness, and increasing the semiconductor energy band gap due to the quantization effect. Therefore, quantum mechanical effects can be incorporated in the proposed models of the surface potential, threshold voltage, inversion layer effective mobility, subthreshold drain current and low frequency drain current flicker noise. Since the oxide thickness is very low, wave function penetration effect can also be incorporated into these models.

Besides, temperature and voltage dependent effective doping concentration model can be developed for the pocket implanted n-MOSFET. The pocket doping profile model is developed in one-dimension. But this model can be extended into two- or three-dimensions as well.

This work is done for the symmetric double pockets at the source and drain sides. But pockets can be included in drain side only (i.e., single pocket) or asymmetric double pockets at the source and drain sides. Effects of temperature variation in the subthreshold drain current model can be incorporated. The subthreshold drain current model can be extended into the complete drain current model (i.e. above the threshold voltage level) including the Drain Induced Barrier Lowering (DIBL), Channel Length Modulation (CLM) and velocity saturation effects. Besides, the models for switching time and RF-operation can be developed for this device. Not only that reliability issues can also be studied due to the incorporation of the pocket doping.

List of Publications

Journal Papers

[1] **Muhibul H. Bhuyan** and Quazi D. M. Khosru, “Inversion Layer Effective Mobility Model for Pocket Implanted nano scale n-MOSFET,” International Journal of Electrical and Electronics Engineering, ISSN 2010-3972, vol. 5, no. 1, pp. 50-57, January 2011.

[2] **Muhibul H. Bhuyan** and Quazi D. M. Khosru, “An Analytical Subthreshold Drain Current Model for Pocket Implanted Sub-100 nm n-MOSFET,” Journal of Electron Devices, France, ISSN 1682-3427, vol. 8, pp. 263-267, October 2010.

[3] **Muhibul H. Bhuyan** and Quazi D. M. Khosru, “Linear Pocket Profile Based Threshold Voltage Model for Sub-100 nm n-MOSFET,” International Journal of Electrical and Computer Engineering, ISSN 2010-3956, vol. 5, no. 5, pp. 310-315, September 2010.

[4] **Muhibul H. Bhuyan** and Quazi D. M. Khosru, “Effects of Temperature on Reverse Short Channel Effect in Pocket Implanted Sub-100 nm n-MOSFET,” Journal of Materials Science and Engineering, USA, ISSN 1934-8959, vol. 4, no. 7, pp. 18-23, July 2010.

[5] **Muhibul H. Bhuyan** and Quazi D. M. Khosru, “Linear Profile Based Analytical Surface Potential Model for Pocket Implanted Sub-100 nm n-MOSFET,” Journal of Electron Devices, France, ISSN 1682-3427, vol. 7, pp. 235-240, April 2010.

International Conference Papers

[1] **Muhibul H. Bhuyan** and Quazi D. M. Khosru, “Low Frequency Drain Current Flicker Noise Model for Pocket Implanted Nano Scale n-MOSFET,” Proceedings of the 15th International Conference on Nano Materials and Device Conference (NMDC 2010), October 12-15, 2010, CA, USA, pp. 295-299.

[2] **Muhibul H. Bhuyan** and Quazi D. M. Khosru, “Linear Pocket Profile Based Threshold Voltage Model For Sub-100 nm n-MOSFET Incorporating Substrate and Drain Bias Effects,” Proceedings of the 5th International Conference on Electrical and Computer Engineering (ICECE 2008), December 20-22, 2008, Dhaka, Bangladesh, pp. 447-451.

[3] **Muhibul H. Bhuyan** and Quazi D. M. Khosru, “An Analytical Surface Potential Model for Pocket Implanted Sub-100 nm n-MOSFET,” Proceedings of the 5th International Conference on Electrical and Computer Engineering (ICECE 2008), December 20-22, 2008, Dhaka, Bangladesh, pp. 442-446.

[4] **Muhibul H. Bhuyan**, Fouzia Ferdous and Quazi D. M. Khosru, “A Threshold Voltage Model for sub-100 nm Pocket Implanted MOSFET,” Proceedings of the 4th International Conference on Electrical and Computer Engineering (ICECE 2006), December 19-21, 2006, Dhaka, Bangladesh, pp. 418-421.

Abstract

[1] **Muhibul H. Bhuyan** and Quazi D. M. Khosru, “Linear Pocket Profile Based Threshold Voltage Model for NMOSFET down to 50 nm,” Proceedings of the 1st National Conference on Electronics, Information and Telecommunication (NCEIT 2007), June 29-30, 2007, Rajshahi, Bangladesh, p. 192.

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Appendix A: Gauss Law

The electric field of a given charge distribution can in principle be calculated using Coulomb's law. An alternative method to calculate the electric field of a given charge distribution relies on a theorem called Gauss' law. Gauss' law states that *"If the volume within an arbitrary closed mathematical surface holds a net electric charge Q, then the electric ux (Φ) though its surface is equal to Q/ε_0."*

Gauss's law can be written in the following form:

$$\Phi = \frac{Q}{\varepsilon_0} \tag{1}$$

The electric flux (Φ) through a surface is defined as the product of the area A and the magnitude of the normal component of the electric field E:

$$\Phi = E\cos\theta \tag{2}$$

,where θ is the angle between the electric field and the normal of the surface.

To apply Gauss' law one has to obtain the flux through a closed surface. This flux can be obtained by integrating equation (2) over all the area of the surface. The convention used to define the flux as positive and negative is that the angle θ is measured with respect to the perpendicular erected on the outside of the closed surface: field lines leaving the volume make a positive contribution and field lines entering the volume make a negative contribution.

Appendix B: Properties of Silicon

Property	Value
Structure (All Cubic)	Diamond
Lattice Parameter a_0 at 300K	0.54311 nm
Density at 300K	2.3290 g.cm^{-3}
Atomic Concentration at 300K	5.00×10^{22} cm^{-3}
Dielectric Constant at 300 K	11.9
Nature of Energy Gap E_g	Indirect
Energy Gap E_g at 300 K	1.1242 eV
Energy Gap E_g at 0 K	1.1700 eV
Effective Concentration N_C of CB states:	
at 4.2 K	4:55×1016 cm^{-3}
at 300 K	2:86×1019 cm^{-3}
Effective Concentration N_V of VB states:	
at 4.2 K	1:87×1016 cm^{-3}
at 300 K	3:1×1019 cm^{-3}
Intrinsic Carrier Concentration n_i at 300 K	1:07×1010 cm^{-3}

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Appendix C: Fundamental Physical Constants

Name	Symbol	Value	Unit
Atomic Mass Unit	m_u	$1.66053873(13)\times10^{-27}$	kg
Avogadro's Number	N_A	$6:02214199(47)\times10^{23}$	mol^{-1}
Boltzmann's Constant	k	$1:3806503(24)\times10^{-23}$	JK^{-1}
Electric Constant	ε_0	$8:854187817\times10^{-12}$	Fm^{-1}
Electron Mass	m_e	$9:10938188(72)\times10^{-31}$	kg
Electron-Volt	eV	$1:602176462(63)\times10^{-19}$	J
Elementary Charge	q	$1:602176462(63)\times10^{-19}$	C
Faraday Constant	F	$9:64853415(39)\times10^{14}$	$Cmol^{-1}$
Hydrogen Ground State		13.6057	eV
Magnetic Constant	μ_0	$4\pi\times10^{-7}$	H/m
Molar Gas Constant	R	8:314472(15)	$JK^{-1}mol^{-1}$
Natural Unit of Action	$\hbar$	$1:054571596(82)\times10^{-34}$	Js
Newtonian Constant of Gravitation	G	$6:673(10)\times10^{-11}$	$m^3kg^{-1}s^{-2}$
Neutron Mass	m_n	$1:67492716(13)\times10^{-27}$	kg
Planck Constant	h	$6:62606876(52)\times10^{-34}$	Js
		$h = 2\pi\hbar$	
Planck Length	l_p	$1:6160(12)\times10^{-35}$	m
Planck Mass	m_p	$2:1767(16)\times10^{-8}$	kg
Planck Time	t_p	$5:3906(40)\times10^{-44}$	s
Proton Mass	m_P	$1:67262158(13)\times10^{-27}$	kg
Speed of Light in Vacuum	c	$2:99792458\times10^{8}$	ms^{-1}