IMPACT OF UNIAXIAL STRAIN ON THE CAPACITANCE-VOLTAGE CHARACTERISTICS OF HIGH-k DOUBLE GATE MOSFET

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By

Khadija Abul Khair

Department of Electrical and Electronic Engineering

Bangladesh University of Engineering and Technology

Dhaka-1000

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Declaration

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

Khadija Abul Khair

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December, 2011

Dedication

To My Mother

Abstract

Suppression of short-channel effects (SCE) will be key challenges for transistor scaling. High-k Double-Gate MOSFET may eventually be needed to meet performance requirements in the sub-20nm gate length regime because SCE can be effectively suppressed without the need for high channel doping concentrations, resulting in enhanced carrier mobilities. Strained-Si has also been considered as a key technology for enhancing carrier mobilities via modification of the electronic band structure of the channel material and effective masses of the electron. In this work, to accurately simulate the DG MOSFET self-consistent fully-coupled1D Schrodinger and Poisson's equation model has been used. Quantum mechanical effects have been considered by incorporating wave function penetration effect and open boundary conditions at the Si/HfO_2 interfaces. It has been found that, the uniaxial strain increases the gate capacitance as it reduces eigen energy levels of longitudinal valleys of Si, thereby increasing the total charge. Moreover, the uniaxial strain reduces the threshold voltage, shifts the inversion channel towards the Si/HfO_2 interfaces and reduces the gate leakage current.

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Chapter 1

Introduction

1.1 Mobility Scaling

In 1947 the bipolar transistor had been invented and the semiconductor industry grew rapidly. In 1958 the concept of an integrated circuit (IC) was invented by J. Kilby and the geometric scaling had been introduced to reduce the cost-per-function with enhanced performance. Aggressive geometric scaling has been accomplished as guided by the ITRS (International Technology Roadmap for Semiconductors) [1].

Geometric scaling is done by reducing the gate length L_g which introduces several Short Channel Effects (SCE) such as increased off-state leakage current, threshold voltage roll-off and Drain Induced Barrier Lowering (DIBL). To suppress SCE, gate oxide thickness (t_{ox}), channel depletion width (x_d) and source/drain junction depth (x_j) should be scaled down with L_g. But thin gate oxide increases band-to-band tunneling and thus increases gate leakage current.

To scale down the depletion width, increased channel doping concentration is necessary which reduces the off-state leakage current. But the high channel dopingconcentration degrades carrier mobility, increases band-to-band tunneling across the reverse-biased drain junction and gate-induced drain leakage (GIDL). Shallow source/drain junctions decrease the capacitive coupling of the source/drain to the channel and degrade on-state drive current by increasing parasitic series resistance.

Therefore, the geometric scaling should be replaced with a new scaling vector and this is the mobility scaling [2-4]. Strained-Si technology has been widely used to improve mobility and thus increasing the on-state current without increasing the off-state current [5-11]. Many works incorporated biaxial strain [12-13] but uniaxial strain results in highest drive current enhancement and smaller stress-induced n-channel MOSFET threshold voltage shift. The process induced uniaxial stress offers largeperformance improvement at low cost and minimally

increased manufacturing complexity and is scalable to future technology nodes [14]. Process induced strain can be incorporated by using silicon nitride cap, silicide, and SiGe source/drain. Strain enhances the mobility by splitting the conduction band edge (lowering the longitudinal valleys and increasing the transverse valleys of Si).

1.2 Multiple Gate Devices

To fulfill the ITRS requirements, multiple gate devices are promising architectures for their improved electrostatic control of the channel. The dominant leakage path for off-state leakage current is located far from the gate, which is least effectively controlled by the gate. Therefore, advanced SOI MOSFETs and Double-Gate MOSFET can suppress the leakage current by eliminating the part of the channel that is not effectively modulated by the gate. SOI MOSFET requires thinner body than DG MOSFET because its body is controlled by one gate, on the other hand the DG MOSFET controls the body with two gates therefore it can use thicker body.

In addition, the DG device does not require high channel doping which eliminates mobility degradation and statistical dopant fluctuation. DG MOSFET has higher transconductance and hence high current driving ability [15]. The drain-induced barrier lowering is also minimized by the shielding effect of the double gate [16]. The lightly doped DG MOS reduces gate leakage current. It can be reduced further if high-k dielectric material is used which will also helpful for scaling down the oxide thickness. Among the high-k dielectrics being studied, HfO_2 appears promising due to its relatively high dielectric constant (25) as compared to Si_3N_4 (7.5) and Al_2O_3(9.1) [17] and its relatively large band gap (5.8 eV) as compared to TiO_2 (3.03 eV) and Ta_2O_5 (4 eV) [18].

1.3 Literature review

In 1984 the concept of double-gate SOI MOSFET known as XMOS was invented [19] depicting good short channel characteristics. Since then to model Double-Gate MOSFET, various types of approaches have been used. R. F. Pierret et al. uses two-dimensional device simulations and one dimensional analytical computation to analyze the dual-gate operation in the strong inversion region [20]. K. Suzuki et al. developed a model for short channel n^+-p^+ double gate SOI MOSFET by solving a 2D Poisson's equation [21]. Y. Taur has derived a 1D analytical solution for an undoped or lightly doped DG MOSFET by incorporating only the mobile charge [22].

The complete carrier based non charge sheet analytical model is based on the Poisson's equation to solve for the carrier concentration directly rather than relying on the surface potential alone [23]. This model covers all three regions of CV characteristics and it does not depend on any fitting parameter, auxiliary functions or variables. The mobile carrier concentration is calculated from Boltzmann statistics for the Poisson's equation. The electric field in the center of the Si film has been assumed to be zero and then an exact closed-form expression for the carrier concentration-electron concentration at the center of the channel Si has been derived as a function of gate voltage, channel voltage and Si film. SCE are incorporated in 2D Poisson's equation and to calculate the capacitance, the spatial distribution of the carrier charge across the MOSFET channel is found considering the drain current continuity characteristics.

In explicit continuous model, implicit equations for intermediate parameters by numerical iteration or the table lookup method are solved to avoid computational inefficiency and sporadic exceptions [24]. This model is continuous through the all operation regions, i.e., linear, saturation and subthreshold without using charge sheet approximation and ad hoc fitting parameters. Here, at first the Poisson's equation is solved under the gradual channel approximation. The solution is an implicit equation which is solved using the following general method:

(1) Compose a continuous starting function as the initial approximation.
(2) Modify the starting function with high-order correction.
(3) Make another correction to improve accuracy.

In this way an accurate explicit model DG MOSFET has been derived.

In [25] an analytical solution of gate capacitance for DG and FD/SOI MOSFETs has been derived. To incorporate the symmetric nature, the front and back gates are tied together. The expression of the surface potential referenced to the hypothetical neutral body is obtained by integrating the Poisson's equation. This expression is used in Gauss's law, where it is related to inversion charge and gate voltage. Then this equation is differentiated to obtain the gate capacitance.

Self-consistent numerical model using fully-coupled 1D Schrodinger's and Poisson's equation is very popular for modeling DG MOSFET [26]. A complete model of DG MOSFET which accurately incorporates the QM effects is very important for future circuit simulators.

1.4 Objective of the thesis

In this thesis, a 1D coupled Schrodinger–Poisson self-consistent simulator has been developed for symmetric double gate MOSFET with silicon as substrate and silicon dioxide or halfnium oxide as insulator material. Poisson's equation has been solved using Finite Difference Method

and Schrodinger's equation has been solved using the Hamiltonian Matrix Formalism. As wavefunction penetration into the gate dielectric plays an importantrole in the state-of-the-art nanoscale devices, effect of wave function penetration into the front gate and back gate has been incorporated in the simulator.The accurate value of Quasi Fermi level has been calculated. The effect of uniaxial strain has been incorporated in the simulator by changing the value of effective masses. Due to uniaxial strain the conduction band goes up for transverse valleys and goes down for longitudinal valleys of silicon. These changes have been included. Once the electrostatics of the devices is calculated at different gate voltages, gate capacitance – gate voltage characteristics can be modeled. Transmission coefficients of electrons will be calculated which depends on height and barrier of the potential barrier. Then tunneling lifetime obtained from eigen energies and transmission probability of electrons is multiplied with charge density to calculate the gate tunneling current. Summation of the current components over each carrier subband and valley yields the total gate current.

1.5 Organization of the thesis

In chapter two the structure and device physics of Double-Gate MOSFET will be discussed. Then the advantages of high-k DG MOS will be presented. Also the necessary theories to include strain effect on band structure and effective mass will be explained from literature.

In chapter three, the method to solve gate capacitance and gate leakage current by the coupled Poisson's equation and the Schrodinger's equation will be discussed. Then the fully coupled 1D Schrodinger and Poisson's equation will be presented for the purpose of simulation.

In chapter four, results obtained from the simulation will be given and the comparisons between different level of applied stress, between HfO_2 and SiO_2 and between the DG MOS and SG MOS will be presented.

Chapter 2

Double Gate MOSFET

The double-gate MOSFET can be scaled promisinglydue to itsinherent robustness to short-channel effects, high current driving capability and the 60 mV/decade slope of the turn-on characteristic at room temperature [16]. Although the manufacturability of DG MOSFET is still challenging, this extremely interesting device concept is very advantageous for semiconductor device industry.

2.1 Device Structure and physics

As a result of different fabrication processes, DG MOSFETs can be grouped into

i. Planer DG MOSFET
ii. FinFET
iii. Vertical DG MOSFET.

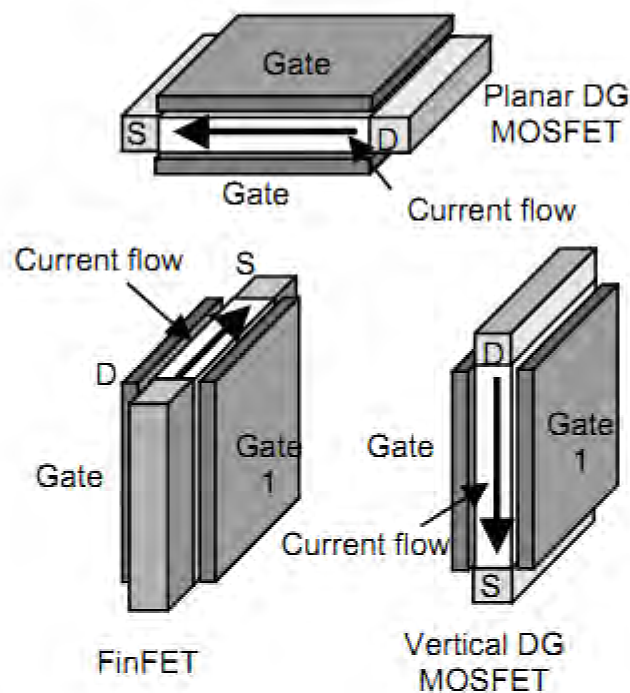


Figure 2.1: Different structure of DG MOSFET [28]

The first type of structure is close to the planar MOSFET in geometry except that it has a bottom gate. An advantage of this topology is the good control of the silicon channel thickness but the fabrication of the self-aligned bottom gate in this structure has been very challenging and the another problem is that the gate length must be controlled by lithography.

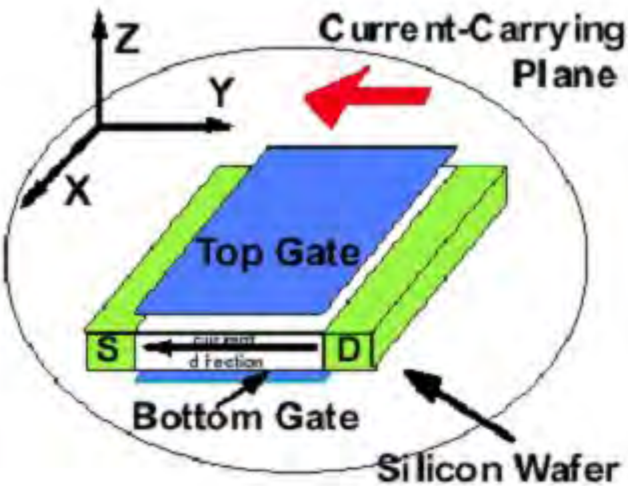


Figure 2.2: Planar Device Structure

The current flows parallel to the wafer in the second type of structure. However, the Si/SiO2 interface is formed on the sidewalls of an etched silicon fin. Both the gate length and the channel thickness are defined by the lithography in this structure. Also, the width of the transistor is fixed by the fin height, and thus multiple fins have to be used to obtain higher drive current.

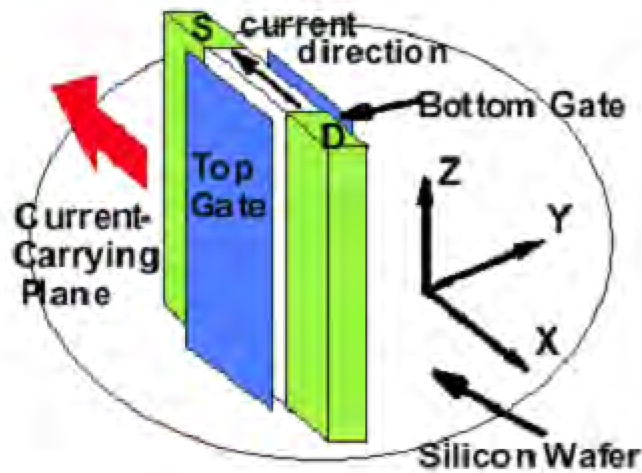


Figure 2.3: FinFET Structure

In the third type of device structure, the current flow is perpendicular to the wafer and the gate lengthis defined by non-lithographic methods such as a timed etch or a thin filmdeposition. Gate length is decoupled from the packing density but the fullydepletedoperation is challenging since the silicon channel thicknesshas to be defined by lithography.

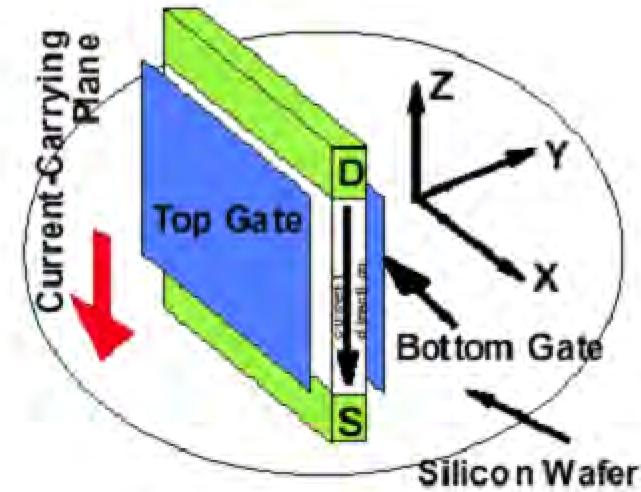


Figure 2.4: Vertical Device Structure

The operation modes of DG MOSFET can be classified into symmetric DG (SDG) MOSFET and Asymmetric DG (ADG) MOSFET. The both gates of symmetric type has identical work functions so that the two surface channels turn on at the same gate voltage and the asymmetric type has different work functions for the gates and only one channel turns on at the threshold voltage.

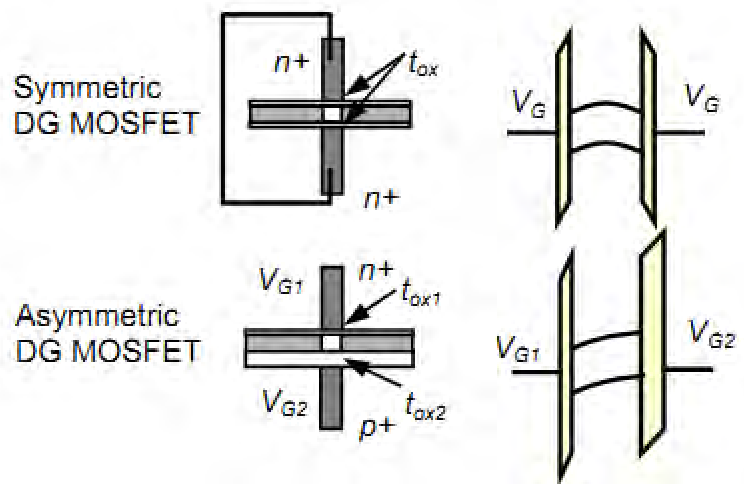


Figure 2.5: The two operation modes for DG MOSFETs [28]

TheSDG device shows higher carrier mobility due to its lower transverseelectric field as compared to the ADG device. Figure 2.6 shows the energy band diagram along the vertical direction (across the front and back gates) of the SDG structure. It describes how conductive channels are formed for the lightly doped n-channel SDG MOSFETs.

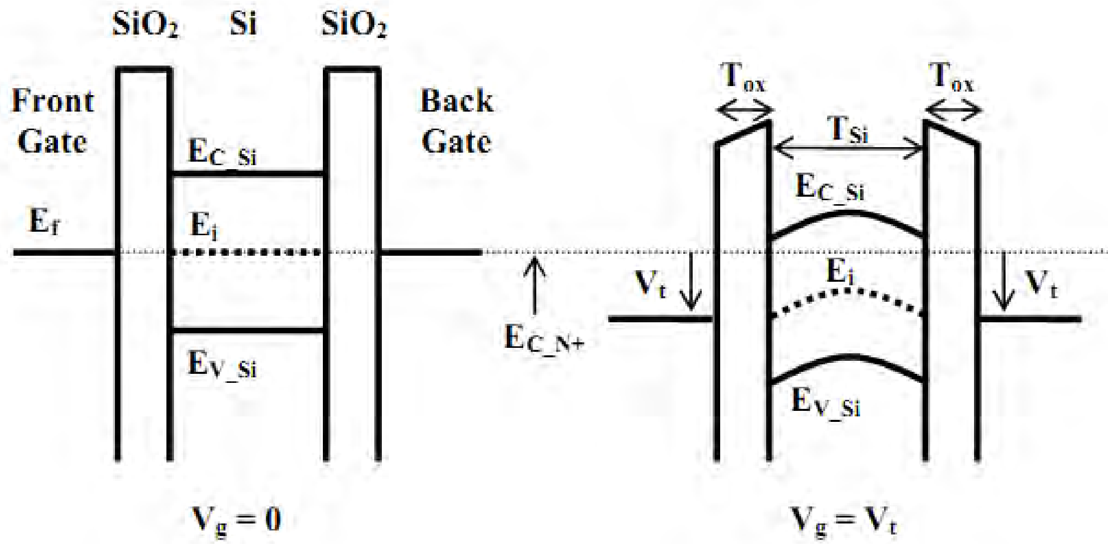


Figure 2.6: Symmetric DG MOSFET [4]

Here, E_f is the fermi level, E_i is the intrinsic Fermi level, E_{C_Si} is the conduction band of the silicon body and E_{C_N+} is the conduction band edge of the N+source/drain. The same voltage is applied to the two gates having the same work function. At zero gate voltage, the position of the silicon bands is largely determined by the gate work function, because as long as the thin silicon is lightly doped and the depletion charge is negligible, the bands remain essentially flat throughout the thickness of the film. Since there is no contact to the silicon body, the energy levels are referenced to the electron quasi-Fermi level or the conduction band of the n^+ source-drain (not shown), represented by the long dotted line in Fig. 2.6. As the gate voltage increases toward the threshold voltage, mobile charge or electron density becomes appreciable when the conduction band of the silicon body moves to near the conduction band of the source-drain.Since the work functions of two gates are identical, the conduction bands in bothsurfaces (under the front and back gates) are bent by the exactly same amount. As a result,at on-state, two conductive channels are formed for the SDG device, unless the siliconbody thickness is not very

thin (e.g., <5nm). In that case, as the gate voltage approaches V_t, the bands of the whole silicon body including the center follow Vg, thus volumeinversion takes place [27].

To account for process varieties, a DG MOSFET can be decomposed into an intrinsic core part together with a number of parasitic components as shown in Figure 2.7. The core part of the DG MOSFET remains more or less the same for different processes and can be accurately described by the device physics. The parasitic part, however, is strongly structural dependent and more empirical approach has to be used to include their effects. This allows the initial modeling work to focus on the core structure. A modular approach allows the empirical part to be replaced by a physical formulation once the more definite device structure becomes available [28].

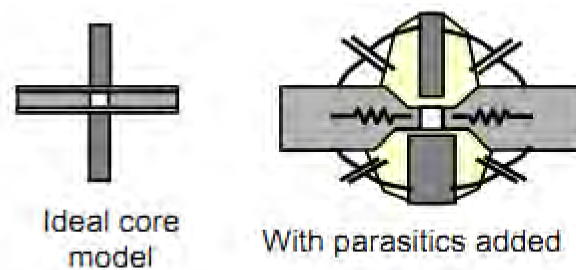


Figure 2.7: Decomposition of a DG MOSFET into the ideal core and the parasitic components [28]

2.2 Short Channel Effects (SCE)

The short-channel effects are attributed to two physical phenomena:

1. Thelimitation imposed on electron drift characteristics in the channel,
2. The modification of the threshold voltage due to the shortening channel length.

In particular five different short-channel effects can be distinguished:

1. Drain-induced barrier lowering
2. Surface scattering
3. Velocity saturation
4. Increased off-state leakage current
5. Threshold voltage roll-off

Subthreshold swing degradation and other short-channel effects are caused by the encroachment of electric field line from the drain on the channel region, thereby competing for the available depletion charge, and reducing the threshold voltage.In small-geometry MOSFETs, the potential barrier is controlled by both thegate-to-source voltage and the drain-to-source voltage. If the drain voltage is increased, thepotential barrier in the channel decreases, leading to drain-induced barrier lowering (DIBL). The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage. The channel current that flows under these conditionsis called the sub-threshold current. Figure2.8 shows how the gates and the drain compete for the depletion charge. Gate control is exerted in the yand z directions and competes with the variation of electric field in the xdirection due to the drain voltage.

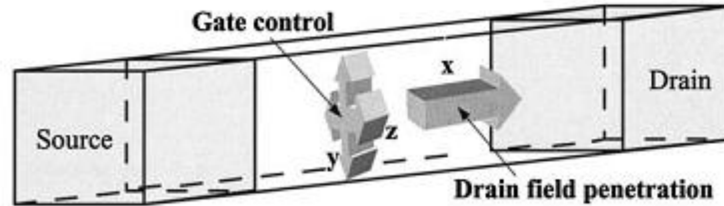


Figure 2.8: Definition of coordinate system in a multiple-gate device. Gate-induced fields are in the x and z directions. Drain penetration field is in the y direction.

As the channel length becomes smaller due to the lateral extension of the depletion layer into thechannel region, the electric field component e_x increases, and the surface mobilitybecomes field-dependent. Since the carrier transport in a MOSFET is confined within the narrowinversion layer, and the surface scattering (that is the collisions suffered by the electrons that areaccelerated toward the interface by e_y) causes reduction of the mobility, the electrons move withgreat difficulty parallel to the interface, so that the average surface mobility, even for small valuesof e_x, is about half as much as that of the bulk mobility.

In order to suppress the SCE in bulk MOSFETs, other parameters have beenscaled down together with gate length (L_g), such as the gate oxide thickness (T_{ox}), the channel depletion width (X_d), and the source/drain junction depth (X_j).To scale down the depletion width, increased channel doping concentration isnecessary which reduces the off-state leakage current byincreasing the channelpotentialand eliminating leakagecurrent paths far from the gate dielectric interface. However, the high channel potential makes V_T high and the high channel dopingconcentration degrades carrier mobility due to increased vertical electric field and more

impurity scattering and also increases band-to-band tunneling across the reverse-biaseddrain junction and gate-induced drain leakage (GIDL). In addition, statistical fluctuation of channel dopants causes more V_T variations, especially in the nanoscale regime. Shallow source/drain junctions decrease the capacitive coupling of the source/drain to the channel and increase parasitic series resistance, resulting in degraded on-state drive current.

The dominant path of off-state leakage current is located far from the gate, which is least effectively controlled by the gate. Therefore, to eliminate the part of the channel that is not effectively controlled, thin body thickness can be used. An ultra-thin body (thinner than 50% of L_g) is necessary to effectively suppress the leakage current for Silicon-on-Insulator MOSFET, on the other hand, the body thickness requirement for the double-gate(DG) MOSFET can be relaxed (to be 50% to 70% of Lg) due to enhanced channel controlby the two gates [29].The use of ultra-thin films poses the problem of severe mobility reduction, high source and drains resistance and tight etch selectivity budget in ultra-thin SOI devices. Quite clearly, the use of double-gate relaxes the requirements on film thickness.

A backside conducting layer is more suitable to reduce short channel effects in FETs, because it can screen the drain field away from the channel. This feature of double-gated FETs is enabled it to be scaled to shorter dimensions than fullly-depleted SOI MOSFETs, for the same channel thickness [15]. The undoped or lightly doped Si film of DG MOSFET overcomes the band-to-band tunneling problem. Moreover, to allow 0.1 V for threshold variation due to tolerances and gate length variation leaves 0.1 V necessitates low temperature operation. Since band-to-band tunneling turns out to be quite small in double-gate FETs, these limitations can be overcome.

When the depletion region surrounding the drain extends to the source, so that the two depletion layers merge, punchtrough occurs. The shield effect of the double gate prevents punch-through to occur even at zero doping concentration within the channel, which is important to prevent degradation of the output characteristics and excess leakage currents at zero gate voltage [16].

For the thinnest silicon films, an unambiguous mobility increase in DG with respect to SG mode is observed even at the same effective field strength [30]. The threshold voltage of the three-terminal DG-MOSFET is not influenced by the body effect,as opposed to the bulk MOSFET which is a four-terminal device. Moreover, the current drive of a double-gate device is double that of a single-gate transistor with same gate length and width [31]. Therefore, the DG-MOSFET is very promising for miniaturization.

2.3 Volume inversion

If the film is thicker than the maximum depletion regions induced by the two gates, the inversion channels grow independently, while the middle of the film remains undepleted and dominated by majority carriers. In this case the device operation is simply given by the parallel combination of two MOS transistors, i.e., in the linear region. A different behavior, caused by the interaction of the two interfaces, occurs in film with a thickness smaller than the summation of depletion widths induced by the two gates. In this case, an electrostatic potential increase at the interfaces and in the film volume and the channel is no more confined at an interface. This volume inversion represents tremendous advantages:

1. Greatly increased number of minority carriers.
2. Reduced influence of surface-induced scattering events and interface defects.
3. Use of volume which is much thicker than a surface inversion layer and offers high current mobility.
4. Enhanced effective mobility and transconductance.

These special features led to a great improvement in performance, visibly in current value, subthreshold slope, transconductance and speed [32].

2.4 High-k Dielectric

In order to properly suppress short channel effects, the ratio between the physical gate-length and the oxide thickness should not drop below approximately 50:1 that results in an oxide thickness below 1 nm for physical channel lengths around 40 nm [30]. The thickness of SiO2-based gate dielectrics is approaching physical limits, for which quantum mechanical tunneling induces severe gate leakage current through the gate dielectric. Moreover, as the dielectric thickness is decreased, charge leakage through the dielectric becomes larger, resulting in difficulty in retaining the stored charge between refresh cycles [17]. This leakage due to quantum mechanical tunneling cannot be mitigated ultimately by improvement in the quality of a given dielectric. Therefore, to suppress gate leakage current alternative gate dielectric materials with higher permittivity (high-k gate dielectrics) can be used to further reduce the equivalent oxide thickness (EOT) with a physically thick dielectric.

To select high-k materials, there are six-fold requirements [43]:

1. High dielectric constant
2. Thermodynamically stable
3. Kinetically stable
4. A band offset with Si of over 1 eV
5. Good electrical interface with Si
6. A few bulk electrically active devices.

Figure 2.9 shows band gap vs. dielectric constant plot. From the figure it is clear that there is a tradeoff between dielectric constant and band gap energy. Considering that high-k materials are introduced mainly because of excess leakage problem, too narrow band gap materials such as TiO_2 or BaO_2 are not suitable for gate oxide. As shown in figure 2.9, HfO_2 (6 eV; k=25), ZrO_2 (6 eV; k=25) and La_2O_3 (5.5 eV; k=30) are mid-gap materials and have relatively high dielectric constant.

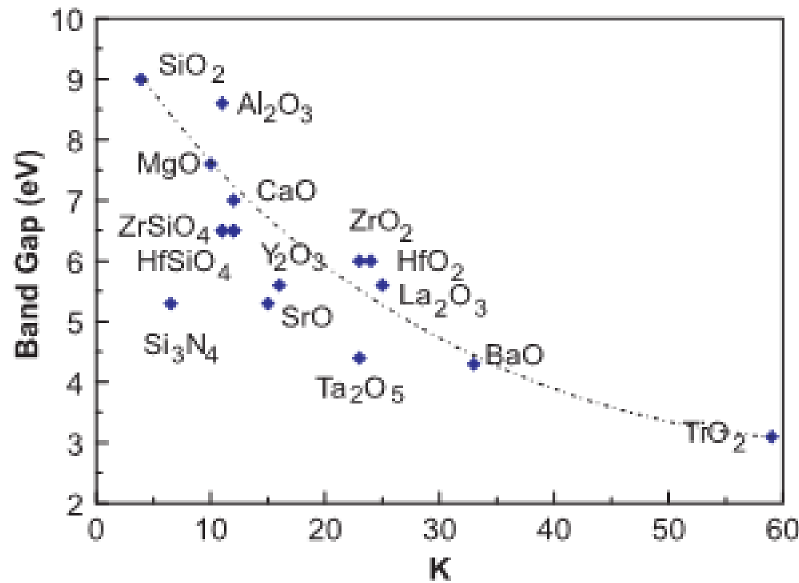


Figure 2.9: Band gap vs. dielectric constant plot of various high-k materials studied forgateinsulator. [43]

Using tabulated thermodynamic data, a comprehensive investigation of the thermo-dynamic stability of binary oxides in contact with silicon at 1000 K was conducted in [33]. The oxide must not react with Si to form SiO_2 as it increases EOT. ZrO_2 is found to be slightly unstable with Si as it is formed $ZrSi_2$. On the other hand La_2O_3 is hygroscopic in nature. Therefore HfO_2 is the preferred dielectric over ZrO_2 and La_2O_3.

If we choose an amorphous dielectric, then it should remain amorphous when annealed to up to 1000º C for 5 seconds. Although HfO_2 crystallizes below 1000º C, it does not differ the insulation property as the leakages are same both for amorphous and crystalline HfO_2.

Crystalline oxide epitaxially grown on Si also maintains the high interface quality. A few bulk electrically active defects can be achieved by processing control and annealing. The density of hafnia is greater than silica, which makes it a more effective barrier to migrating impurities [18]. Moreover, it has a relatively high free energy of reaction with Si. All these features make HfO_2 as a promising dielectric.

2.5 Gate Capacitance

An incremental or small-signal capacitance per unit area can be defined as

$$C_g \equiv \frac{dQ_g}{dV_g}$$

Where

$$C_g = \frac{1}{C_{ox}} + \frac{1}{C_b + C_i}$$

Here,

C_{ox} = oxide capacitance

C_d = depletion region capacitance

C_i = inversion region capacitance

For gate voltage V_g in the weak inversion region, as the inversion layer capacitance is negligible the gate capacitance C_g is basically the series combination of C_{ox} and C_b. As V_g is increased, C_b becomes smaller. Therefore the series combination of C_{ox} and C_b also decreases. Above weak inversion, C_i becomes significant and drastically, and C_g approaches C_{ox}. Physically an abundance of electrons exists at high V_g immediately below the oxide and provides the bottom plate of the oxide capacitor [34].

Gate capacitance is one of the most important parameters for the MOS devices as the transconductance is dependent on the gate capacitance.Moreover, an accurate simulation of CV curves is very important for MOS system parameter extraction such as oxide thickness,substrate and poly-Si doping etc. Moreover, the capacitance-voltage (CV) measurement can be used to determine the interface quality. If an accurate model is developed, then a good agreementbetween measured C-V curve and simulated C-V curve confirms the correct estimation ofthe parameters.

2.6 Gate Current

The gate current due totunneling through the thin-gate oxide or the gate leakage current is one of the major problems in nanoscale MOSFETs. The gate current transport across the oxide-substrate interface under a positive gate bias can be divided into the following five mechanisms, as shown in Figure 2.10.

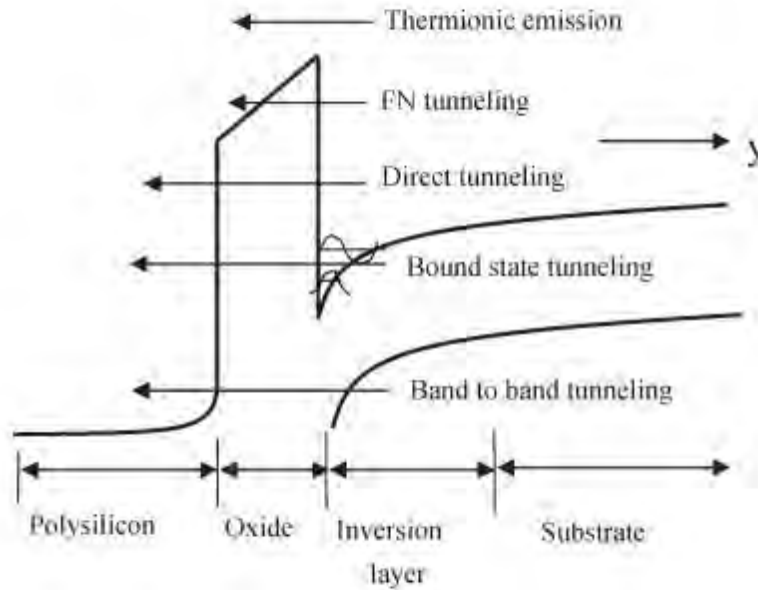


Figure 2.10: Schematic gate-current components between the polysilicon gate and semiconductor substrate in nanoscale MOSFETs [35].

1) Thermionic emission of hot electrons.
2) Fowler–Nodheim (FN) tunneling through a triangularpotential barrier at the top of the oxideconduction band.
3) Direct tunneling due to electrons tunneling through anapproximate trapezoidal potential barrier.
4) Tunneling of electrons residing in the subbands of strongly inverted surface, also known as bound state tunneling.
5) Band-to-band tunneling of electrons from the valenceband of substrate to conduction band of polysilicon gate at high gate voltages.

In nanoscale MOSFETs, the oxide thickness is limited by direct tunneling rather than by hot-carrier injection. When oxide thickness is decreased, the gate voltage is scaled down. Therefore, hot-carrier effects become insignificant by decreasing in an exponential fashion incomparison to

direct-tunneling components [35]. On the other hand, Fowler-Nordheim (FN) tunneling is dominant for thicker oxide and higher electric field [36] and band-to-band tunneling is significant at high gate voltage. Therefore direct tunneling and bound state tunneling is the main transport mechanism for the gate leakage current for the thinner oxide and lower electric field.

The gate leakage current density can be expressed as

$$J = q\sum_{i,j}\frac{N_{ij} * T_{ij}}{\tau_{ij}}$$

Here,

N_{ij}=carrier concentration in the jth energy subband of the ith valley

T_{ij}=transmission probability of electron in the jth energy subband of the ith valley

τ_{ij}= lifetime of carrier in the jth energy subband of the ith valley which can be related to the eigen energy as following [37]:

$$\tau_{ij} = \frac{j\,\pi\hbar}{E_{ij}}$$

Transmission probability is calculated using the transmission line analogy, matching of the impedances seen by a carrier in the potential well [38]. Here the quantum mechanical transmission probability, D(E) is given by

$$D(E) = 1 - |\rho(E)|^2$$

Where $|\rho|^2$is the quantum mechanical reflection coefficient.

$$\rho = \left[\frac{\gamma_2}{m_2^*} - \frac{\gamma_1}{m_1^*}\right] \Big/ \left[\frac{\gamma_2}{m_2^*} + \frac{\gamma_1}{m_1^*}\right]$$

Here γ_1 and γ_2 are the propagation constant of region 1 and 2 respectively.

$$\gamma_i = j\sqrt{\frac{2m_i^*}{\hbar^2}(E - V_i)}$$

In [39] the relative probability that the electron will tunnel from region 1 to 2 is defined as the transmission coefficient T, and this depends on potential barrier height (V_i-E) and the width of the barrier, a.

$$T = \frac{1}{1 + Dsinh^2(\gamma a)}$$

Where

$$D = \frac{V_i^2}{4E(V_i - E)}$$

Indouble-gate MOSFETs, gate current canbe suppressed due to the reduced vertical electric field. The inherent symmetry of the two gate electrodes decreases the effective vertical electric field. If the substrate thickness is sufficient, i.e. larger than the summation of the two depletion width, then no electric field exists in the center. This reduces the depth of the potential well, which lowers the bound state energy and broadens the inversion charge distribution, thus resulting in a lower tunneling probability and the impingement frequency at which electrons are directed toward the silicon–dielectric interface.

The gate leakage current can be reduced using a high k dielectric such as HfO_2. Therefore, the advantage of the DG structures is not only maintained, but also enhanced as device technology migrates to high k gate-dielectric materials and the thickness of dielectric can be more aggressively scaled with double-gate devices at a given technology node than would be possible with a bulk design.

2.7 Strained-Si Technology

Geometrical scaling has approached to its limit due to SCE and increased gate leakage current. Therefore, the industry is looking for a new scaling vector and mobility scaling looks promising to improve on-state current without degrading off-state leakage current. The on-state current of a MOS device can be expressed as

$$I_{on} \approx \mu C_{ox} \frac{W}{L_g} \left(V_{gs} - V_t\right)^2$$

From the equation it can be said that I_{on} can be increased by decreasing t_{ox} ($C_{ox}=\varepsilon/t_{ox}$) and L_g. But decreasing L_g causes SCE and decreasing t_{ox} increases gate current through tunneling. Increasing doping density can decrease the off-state leakage current but at the same time it degrades the carrier mobility. Therefore, increasing mobility is getting attention to improve the on-state current.

The mobility of the MOSFET device can be enhanced by inducing the strain into the channel. The substrate straining process is obtained by forming Si layer over a relaxed SiGe and provides biaxial tensile strain. The process strain can be producedby the process such as silicon nitride cap, silicide, and SiGe source/drain which generates uniaxial strain [4]. Intel introduced strained

Si to its 90-nm process via locally straining nMOS and pMOS devices using two separate techniques. A tensile Si_3N_4 cap layer bonds compressivelyto the source and drain. It stretches the nMOS channel, improving electron mobility relative to relaxed devices. A tensile Si nitride-capping layerused to create a stretched nMOS channel is shown in Figure 2.11 [2].

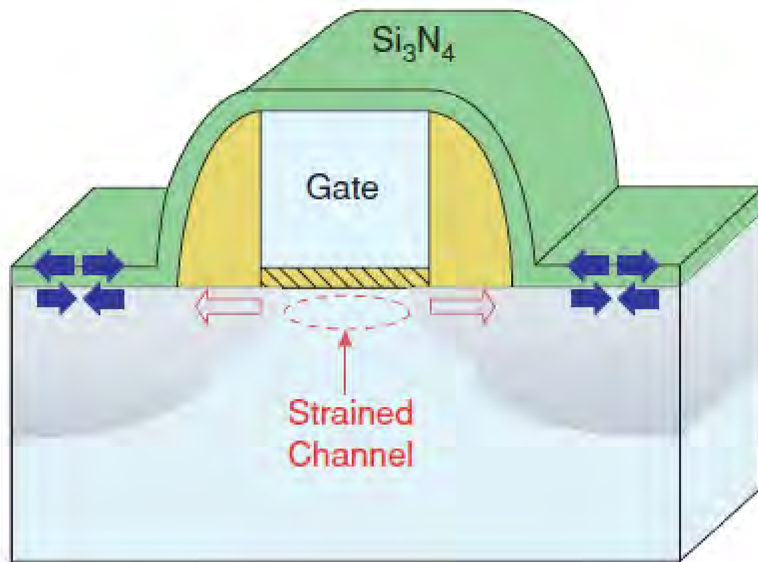


Figure 2.11: silicon nitride capping layer to create tensile strain in nMOS [2]

The capping films are introduced in two ways,

1. A permanent layer post silicide
2. A sacrificial layer before source and drain anneal

The process flow of permanent layer consists of a uniform deposition of a highly tensile Si_3N_4 liner post silicidation over the entire wafer, followed by patterning and etching the film off *p*-channel transistors. Next, a highly compressive SiN layer is deposited, and this film is patterned and etched from *n*-channel regions. In this way a SiN layers with more than 2 GPa of tensile stress and more than 2.5 GPa of compressive stress can be developed [3].

The sacrificial layer introduces strain into the Si channel via a stress memorization of the poly-Si gate. The flow consists of the following steps:

1) poly-Si gate amorphization

2) deposition of a high-stress SiN layer on top of the poly-Si gate
3) recrystallization of the poly-Si gate during source/drain anneal
4) removal of the SiN layer.

After removal of the poly-Si capping layer, some stress remains in the poly-Si gate and Si channel and thus highly tensile nitride capping layer acts as a temporary stressor.

A local epitaxial film grown in the source and drain regions can also introduce uniaxial stress into the Si channel. The process flow consists of the following steps:

1. the Si source and drain are etched, creating an Si recess
2. SiGe (for *p*-channel) or SiC (for *n*-channel) is epitaxially grown in the source and drain.

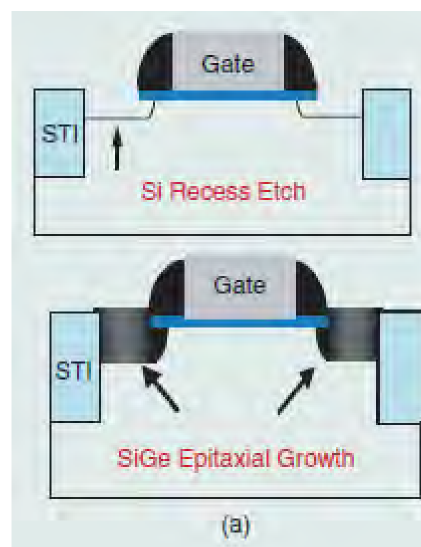


Figure 2.12: Strained-Si p-channel MOSFET process flow [3]

First generation embedded SiGe using 17% Ge to create 500 MPa of channel stress. Next generations bring the SiGe closer to the channel and will likely increase the Ge concentration to introduce 900 MPa of channel stress [5].

Uniaxial strain can also be incorporated through mechanical process. In [4], to provide package strain, the die of the test circuit is tightly glued on a Si wafer/strip as the package substrate. The uniform mechanical displacement at the centerline is applied on the Si strip and the chip die is stressed via the glue between the chip and the package substrate.

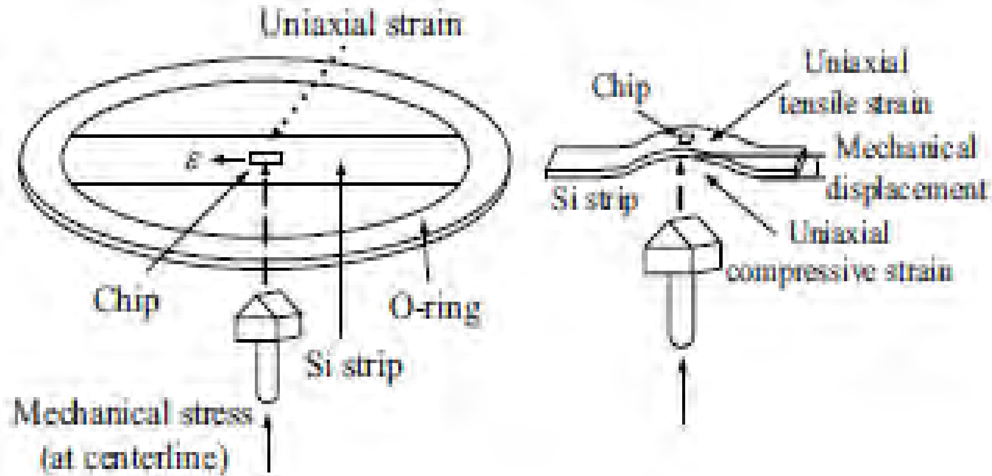


Figure 2.13: The schematc diagram of externally applied uniaxial package strain [4]

Figure 2.14 illustrates another way to introduce uniaxial strain mechanically. Two plates having two parallel ridges are used for four-point bending to apply compressive and tensile uniaxial stress parallel to the direction of carrier transport. The wafer bending curvature induced by external mechanical stress is measured by Tencor FLX-2320.

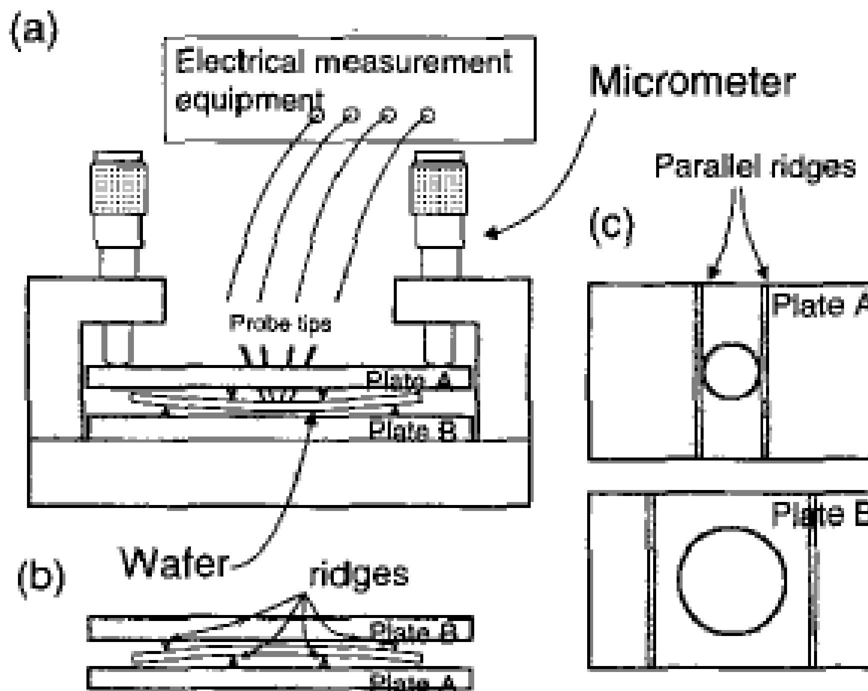


Figure 2.14: The schematic diagram of bending apparatus to introduce uniaxial strain [10]

2.7.1 Physics of strained Si

For electron transport in bulk Si which has a cubic symmetry, the conduction band is comprised of six degenerate valleys of equal energy (Δ_6), as shown in Figure 2.15. The effective mass for any direction is the reciprocal of the curvature of the electron energy function in that direction. For unstressed bulk Si, the total electron conductivity mass, $m*$, is obtained by adding the contributions of the six degenerate valleys and is given by

$$m^* = \left[\frac{1}{6}\left(\frac{2}{m_l}\right) + \left(\frac{4}{m_t}\right)\right]^{-1}$$

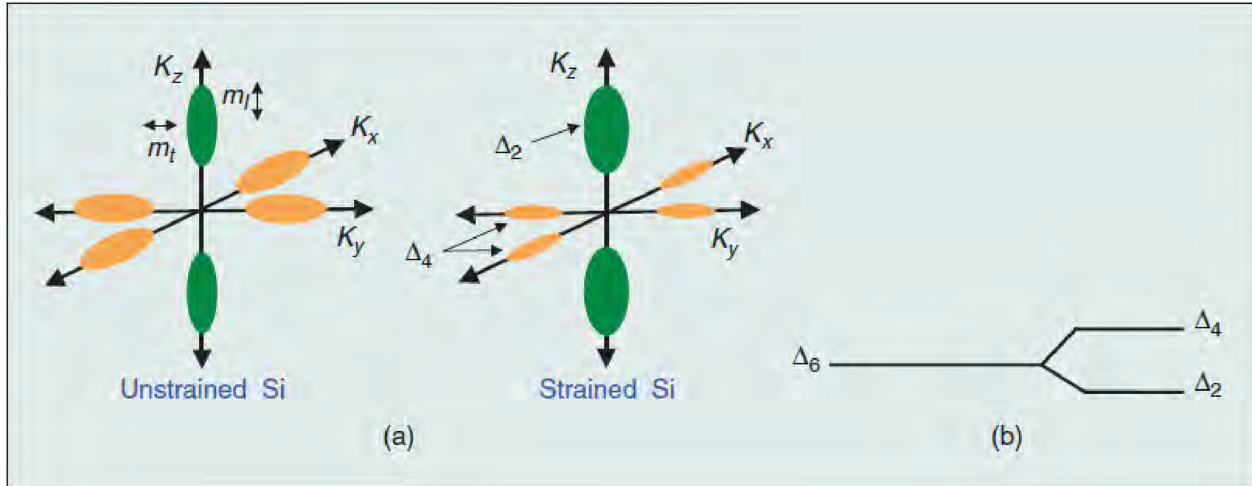


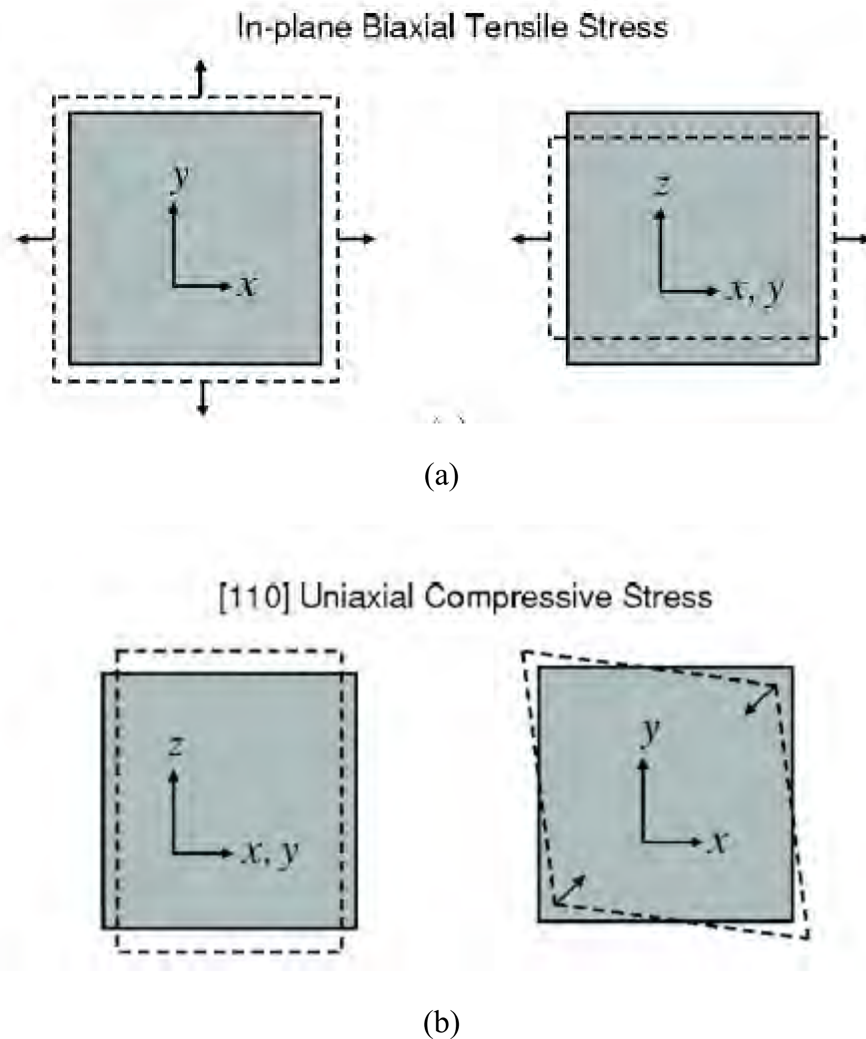
Figure 2.15: *(a)* Ellipsoids of constant electron energy in reciprocal (“k”) space, each corresponding to one of the degenerate conduction band valleys. For this case, the four orange-colored valleys are in the plane of the Si and the two green colored valleys are out of the plane. (b) Energy level at the bottom of the six conduction band valleys. Application of advantageous strain splits the energy level as shown, removing the degeneracy (i.e., the equivalence in energy) between the $\Delta_2$and $\Delta_4$valleys [3].

Strain removes the degeneracy between the four in-plane valleys (Δ_4) and the two out-of-plane valleys (Δ_2) by splitting them in energy, as shown in Figure 2.15. The lower energy of the Δ_2 valleys means that they are preferentially occupied by electrons. This causes reduction in conductivity effective mass which improves the electron mobility as is given by

$$\mu = \frac{q\tau}{m^*}$$

where $1/\tau$ is the inter-valley phonon scattering rate. Electron scattering rate must also be reduced due to the conduction valleys splitting into two sets of energy levels, which lowers the rate of intervalley phonon scattering between the Δ_2 and Δ_4 valleys [3].

Advantageous strain reduces crystal symmetry, thus symmetry is an intuitive means to study the strain effects in semiconductors. For cubic crystal shear strain is more important, because it reduces crystal symmetry. By applying biaxial stress, the shapes of xz and yz planes are changed from square to rectangular, whereas xy planes remain square. On the other hand, <110> uniaxial compressive stress converts the xy plane into rhombus shape and the xz and yz planes into rectangular shapes [14].



(a)

(b)

Figure 2.16: (a) Cubic crystals under in-plane biaxial tensile stress. Under this type of stress, the *x*-*y* plane is still a square, but the *x*, *y*-*z* plane becomes a rectangle. (b) Cubic crystals under uniaxial <110> compressive stress. Under this type of stress, the *x*-*y* plane becomes a rhombus, and the *x*,*y*-*z* plane becomes a rectangle [14].

Relationship between stress and strain can be shown by a matrix multiplication.

$$\begin{bmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \\ \epsilon_{yz} \\ \epsilon_{zx} \\ \epsilon_{xy} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{S_{44}}{2} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{S_{44}}{2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{S_{44}}{2} \end{bmatrix} \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{bmatrix}$$

Here, $\in$ is the applied stress, σ is the resulted strain. In case of Si, the compliance coefficients S_{11}, S_{12} and S_{44} have the following values:

$S_{11}= 8.63\times10^{-12}\ N^{-1}m^2$

$S_{12}= -2.13\times10^{-12}\ N^{-1}m^2$

$S_{44}= 12.49\times10^{-12}\ N^{-1}m^2$

For <110> uniaxial straining process, stress is applied in three different directions ($\sigma_{xx} = \sigma_{yy} = \sigma_{xy} = \sigma/2$).

The expression of band splitting due to strain is presented by Baslev[23] as following:

Band splitting in Δ_2 conduction valleys with respect to the mean position of the conduction band shift,

$$\Delta E_c^2 - \Delta E_c^0 = -\frac{1}{3}(S_{11} - S_{12})\Xi_u P$$

Band splitting in Δ_4 conduction valleys with respect to the mean position of the conduction band shift,

$$\Delta E_c^4 - \Delta E_c^0 = -\frac{1}{6}(S_{11} - S_{12})\Xi_u P$$

Hydrostatic shift of the mean position of the conduction band,

$$\Delta E_c^0 = \Delta E_{g0} - |E_{\varepsilon\varepsilon}| - \frac{1}{3}(S_{11} - S_{12})\Xi_u P$$

The change in band gap energy,

$$\Delta E_g^0 = \left(\Xi_d + \frac{1}{3}\Xi_u - a\right)(S_{11} + 2S_{12})\Xi_u P$$

The valence band splitting due to strain,

$$|E_{\varepsilon\varepsilon}| = \frac{1}{2}\left[b^2(S_{11}-S_{12})^2 + 3\left(\frac{d}{2\sqrt{3}}S_{44}\right)^2\right]^{\frac{1}{2}}|P|$$

Here

ΔE_c^0 =hydrostatic band shifting of the conduction band

ΔE_c^i =band splitting of the ith valley

ΔE_{g0}=change in the energy band gap

P=applied stress

Ξ_u=8.6 eV

$\Xi_d + \frac{1}{3}\Xi_u - a$=3.8 eV

$|b|$=2.4 ± 0.2 eV

$|d|$=5.3 ± 0.4 eV

Figure 2.17 and figure 2.18 show the changes of conduction band and energy band gap with the applied stress. The conduction bands of longitudinal and transverse valleys go down and up respectively. Moreover, the shift of longitudinal valley is greater than the shift of transverse valley. On the other hand, the energy band gap is increased with applied stress.

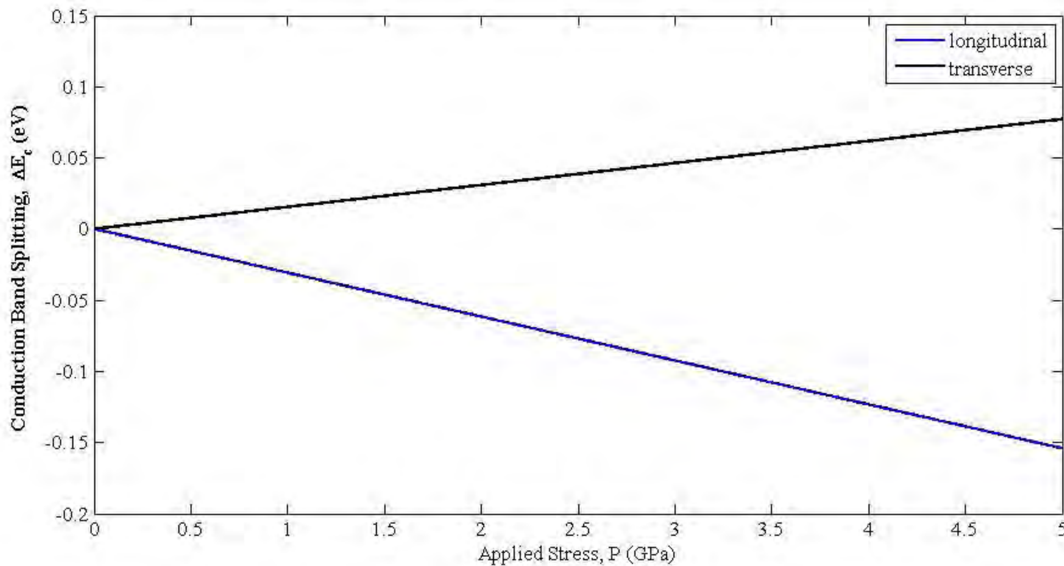


Figure 2.17: Band splitting in conduction valleys

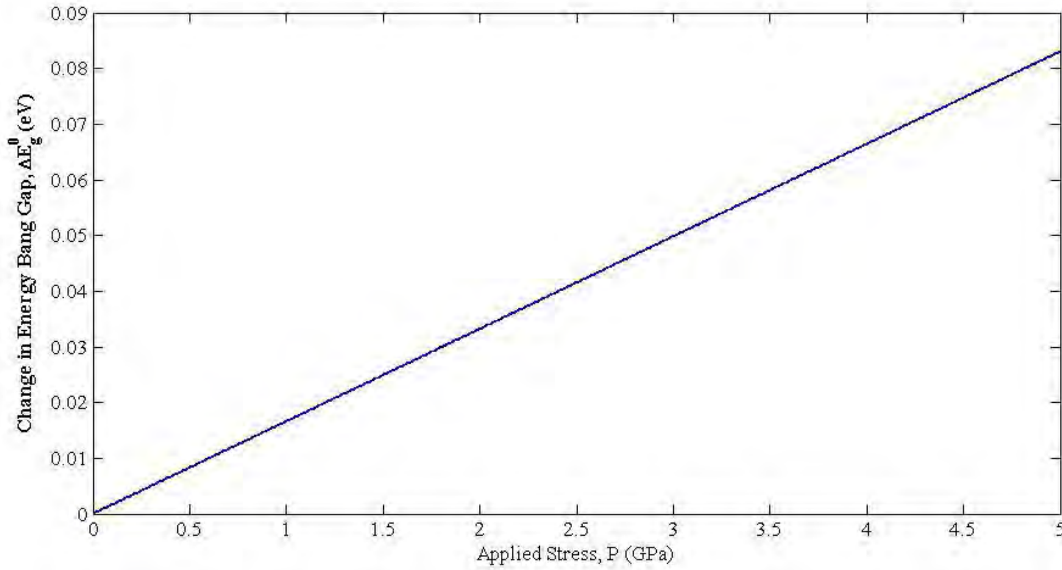


Figure 2.18: Change in Energy band gap

The changes in effective masses are presented by Dhar et al. [41]. The effective masses in three crystal directions <100>, <010> and <001> are represented by m_x, m_y and m_z respectively. They can be expressed as

$$m_x = 0.918 + 0.0236P^2$$

$$m_y = 0.196 - 0.016P$$

$$m_z = 0.196 + 0.029P$$

Quantization effective masses and density of state effective masses are related to m_x, m_y and m_z as following:

$$m_{dl} = \sqrt{m_y m_z}$$

$$m_{dt} = \sqrt{m_x m_y}$$

$$m_{zl} = m_x$$

$$m_z = m_z$$

Figure 2.19 and figure 2.20 show the changes of quantization effective masses and density of state effective masses with applied stress.

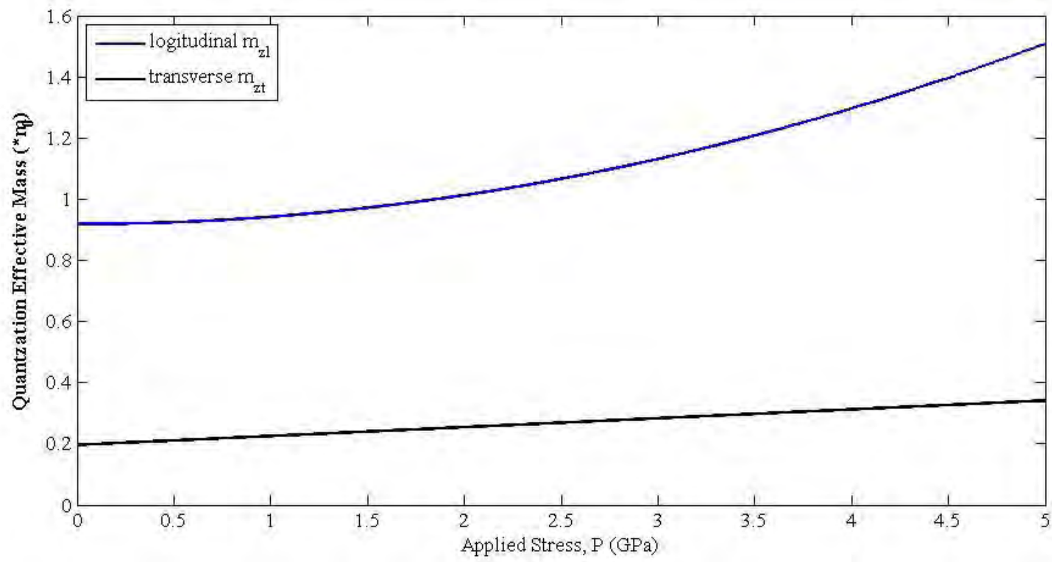


Figure 2.19: Changes in quantization effective masses

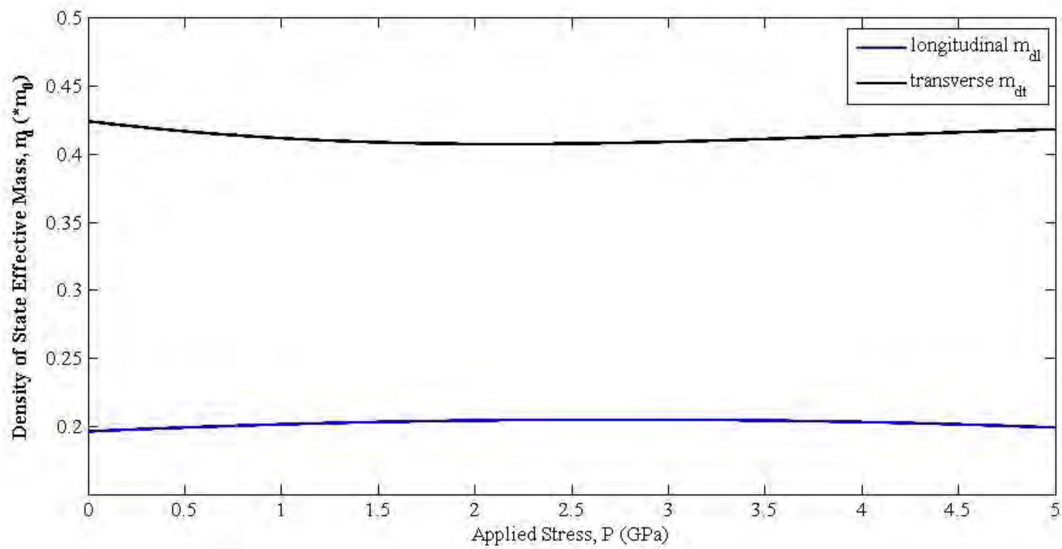


Figure 2.20: Changes in density of state effective masses

The change in band gap energy also changes the intrinsic carrier concentration as follows:

$$n_i = 1.5 \times 10^{10} \times \exp(\Delta E_g)$$

Chapter Three

Simulation Technique

In this thesis, a 1D coupled Schrodinger–Poisson self-consistent simulator has been developed for symmetric double gate MOSFET with silicon as substrate and silicon dioxide or halfnium oxide as insulator material.Self-consistent numerical model using fully-coupled 1D Schrodinger's and Poisson's equation is very popular for modeling DG MOSFET [25-26]. This model fully accounts for quantum mechanical effects, such as wave-function penetration effect, motion quantization normal to the Si-SiO_2 interface and band splitting into subbands. Due to the confinement of electron motion normal to the Si–SiO_2 interface, the conduction band within the transistor channel is split in several subbands, each of which is associated with the corresponding energy eigenvalue. For a silicon crystal with <100> orientation, two energy eigenvalues with degeneracy factor 2 and 4 are created by the sixminima in the conduction band. In this model open boundary condition is used to consider wave function penetration into the dielectric region.

Self-consistent Schrodinger-Poisson solver is widely used for simulation of MOS device. The Poisson's equation is solved by finite difference method considering uniform grid spacing. Next step is to solve Schrodinger equation by Hamiltonian matrix formalism. Then Poisson's equation and Schrodinger's equation are coupled together to obtain the electrostatics of MOS device. Neglectingthe coupling between Schrodinger and Poisson's equations,thesolutions are expected to become less and lessaccurate for large values of the electron density andfor increasing values of the silicon thickness [16].

3.1 Poisson's equation solver

Poisson solver is needed to obtain the potential profile V(z). Generalized Poisson's equation can be written as,

$$\frac{\partial^2 V}{\partial z^2} = \frac{\rho}{\epsilon}$$

Here, ρ is the total charge distribution along the z. In this method the derivatives in the partial difference equation are approximated by linearcombinationsoffunction values at the grid points.

$$\frac{\partial^2 V}{\partial z^2} \approx \frac{V_{i-1} - 2V_i + V_{i+1}}{\Delta z^2}$$

Therefore,

$$\frac{\partial^2 V}{\partial z^2} = \frac{\rho}{\epsilon}$$

$$\Rightarrow \ \epsilon \, \partial^2 V = \rho \partial z^2$$

$$\Rightarrow \ \epsilon_{i-1} V_{i-1} - 2\epsilon_i V_i + \epsilon_{i+1} V_{i+1} = \rho_i \Delta z^2$$

This equation is solved in the matrix form as following:

$$[\epsilon] * [V] = [\rho] * \Delta z^2$$

$$\Rightarrow [V] = \frac{[\rho] * \Delta z^2}{[\epsilon]}$$

3.2 Poisson's equation solver for DG MOS

The generalized Poisson's equation is

$$\frac{\partial^2 V(z)}{\partial z^2} = \frac{\rho}{\epsilon}$$

Where

$$\frac{\rho}{\epsilon} = \begin{cases} -\dfrac{\rho_{inv}(z)}{\epsilon_0 \epsilon_{ox}}; \ 0 \le z \le t_{ox} \\ -\dfrac{\rho_{inv}(z) + \rho_{dep}(z)}{\epsilon_0 \epsilon_{Si}}; \ t_{ox} < z \le t_{ox} + t_{Si} \\ -\dfrac{\rho_{inv}(z)}{\epsilon_0 \epsilon_{ox}}; \ t_{ox} + t_{Si} < z \le 2t_{ox} + t_{Si} \end{cases}$$

Halfnium oxide (HfO_2) of 1 nm EOT is used here as a high-k dielectric and Si of 30 nm thickness is used as substrate. Symmetric double-gate MOSFET is considered, therefore

$$V_1 = V_{end} = V_g$$

To incorporate open boundary condition, the oxide electric field is to relate with Si electric field as follows

$$\epsilon_{ox}\varepsilon_{ox} = \epsilon_{Si}\varepsilon_{Si}$$

Hence, the set of linear equations becomes as follows:

In the first dielectric region,

$$V_1 = V_g$$

$$\frac{V_1 - 2V_2 + V_3}{(\Delta z^2)} = \frac{\rho}{\epsilon}$$

$$\frac{V_2 - 2V_3 + V_4}{(\Delta z^2)} = \frac{\rho}{\epsilon}$$

$$\ldots\ldots\ldots\ldots\ldots\ldots$$

$$\ldots\ldots\ldots\ldots\ldots\ldots$$

At the first interface,

$$-\epsilon_{ox}V_{i-1} + (\epsilon_{ox} + \epsilon_{Si})V_i - \epsilon_{Si}V_{i+1} = 0$$

In the Si,

$$\frac{V_{i-1} - 2V_i + V_{i+1}}{(\Delta z^2)} = \frac{\rho}{\epsilon}$$

At the second interface,

$$-\epsilon_{ox}V_{i-1} + (\epsilon_{ox} + \epsilon_{Si})V_i - \epsilon_{Si}V_{i+1} = 0$$

At the second dielectric region,

$$\frac{V_{i-1} - 2V_i + V_{i+1}}{(\Delta z^2)} = \frac{\rho}{\epsilon}$$

$$\ldots\ldots\ldots\ldots\ldots\ldots$$

$$\ldots\ldots\ldots\ldots\ldots\ldots$$

$$V_{end} = V_g$$

Initially, $\rho_{inv}(z) = 0$ for all z and the 30 nm Si substrate is fully depleted at the doping density of 1×10^{17} cm^{-3}. Therefore,$\rho_{dep}(z) = -qN_A$for $t_{ox} < z \leq t_{ox}+t_{Si}$.

3.3 Schrodinger's equation Solver

Schrodinger's equation is solved by Hamiltonian Matrix formalism.The energy band levels around the conduction band minimum can be described by [42]:

$$h(\vec{k}) = E_c + \frac{\hbar^2 k^2}{2m^*}$$

where E_c is the conduction band minimum energy and m^* is the effective mass. A differentialequation can beformed that will yield energy eigenvalues replacing $\vec{k}$ with $-i\vec{\nabla}$.

$$\left[E_c - \frac{\hbar^2}{2m^*}\nabla^2\right]\psi(\vec{r}) = E\psi(\vec{r})$$

For one dimension,

$$\left[E_c - \frac{\hbar^2}{2m^*}\frac{d^2}{dz^2}\right]\psi(\vec{z}) = E\psi(\vec{z})$$

Finite difference method is used to convert it into a Hamiltonian matrix. This conversionis done by choosing a discrete lattice. We can represent the wave function $\psi(z)$ by a columnvector,

$$\psi(z) = \{\psi(z_1)\psi(z_2) \dots \psi(z_{i-1})\psi(z_i)\psi(z_{i+1}) \dots\}^T$$

Then the matrix representing the Hamiltonian operator (H_{op}) is obtained as

$$H_{op} \equiv E_c - \frac{\hbar^2}{2m^*}\frac{d^2}{dx^2}$$

Using finite difference method it can be written as,

$$\left(\frac{d^2}{dz^2}\psi\right)_{z=z_i} = 2\frac{(z_i - z_{i-1})\psi_{i+1} - (z_{i+1} - z_{i-1})\psi_i + (z_{i+1} - z_i)\psi_{i-1}}{(z_{i+1} - z_{i-1})(z_{i+1} - z_i)(z_i - z_{i-1})}$$

For uniform mesh size of $\triangle z=a$ which reduces to

$$\left(\frac{d^2}{dz^2}\psi\right)_{z=z_i} = \frac{\psi_{i+1} - 2\psi_i + \psi_{i-1}}{a^2}$$

And

$$(E_c\psi)_{z=z_i} \rightarrow E_c(z_i)\psi_i$$

If we assume

$$t_i = \frac{\hbar^2}{2m_i^* a^2}$$

Then

$$[H_{op}\psi]_{z=z_i} = -t_{i-1}\psi_{i-1} + (E_c(z_i) + t_{i-1} + t_i)\psi_i - t_i\psi_{i+1}$$

3.4 Schrodinger's equation solver for DG MOS

To incorporate uniaxial strain on the channel, effective masses of Si and band offset have been changed. These changed effective masses and band profile are used to solve Schrodinger's equation by Hamiltonian matrix. The normalized wave functions both for longitudinal valleys and transverse valleys are shown in the following figures.

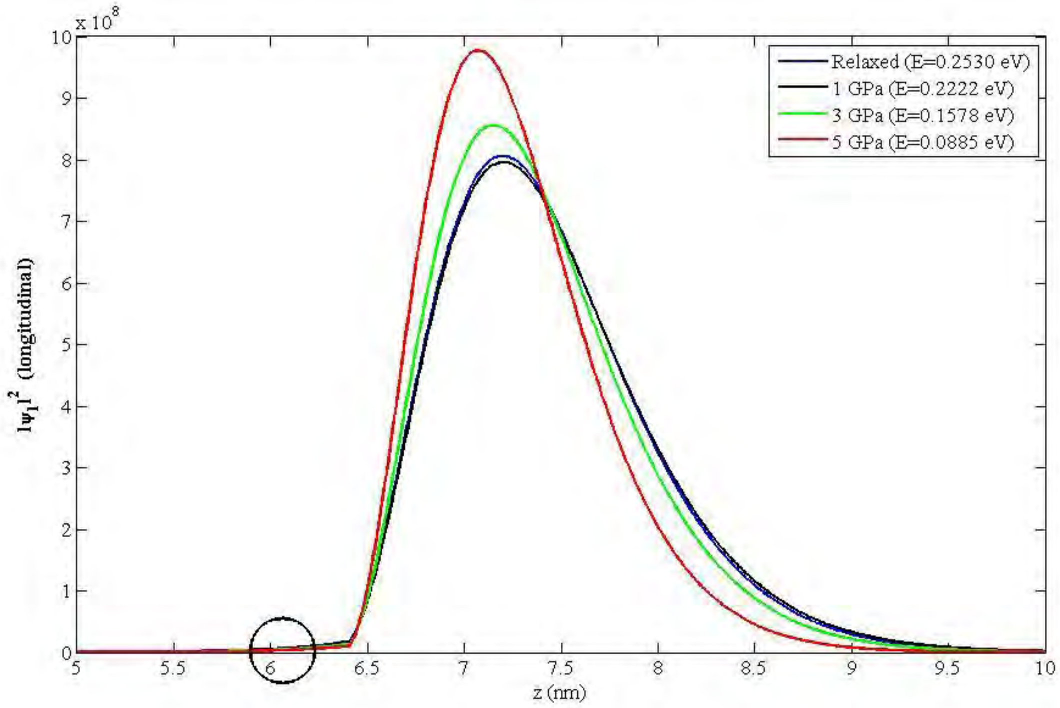


Figure 3.1: Normalized Wave function for 1st eigen energy of longitudinal valleys (HfO_2)

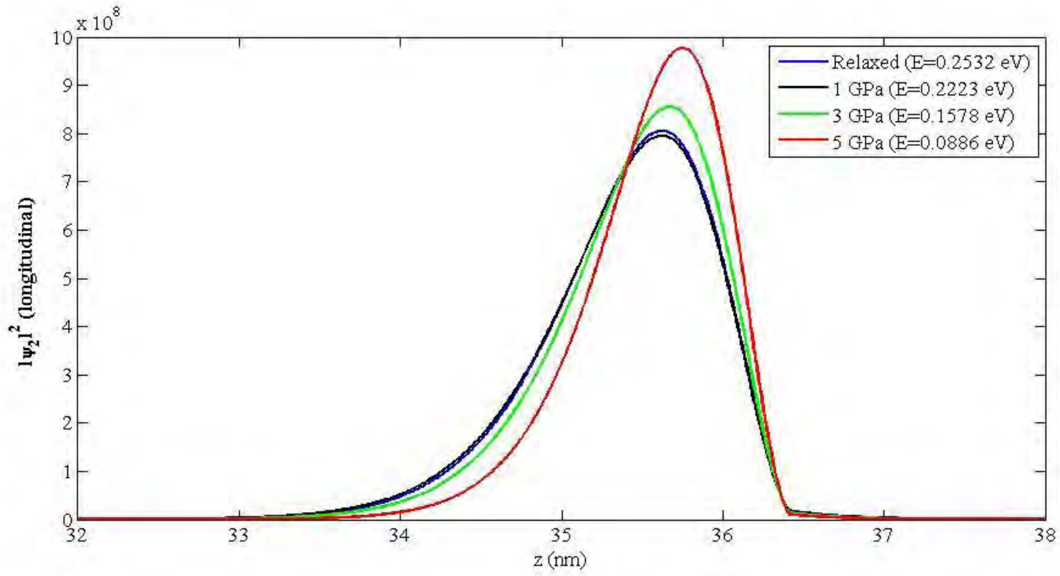


Figure 3.2: Normalized wave function for 2nd eigen energy of longitudinal valley (HfO_2)

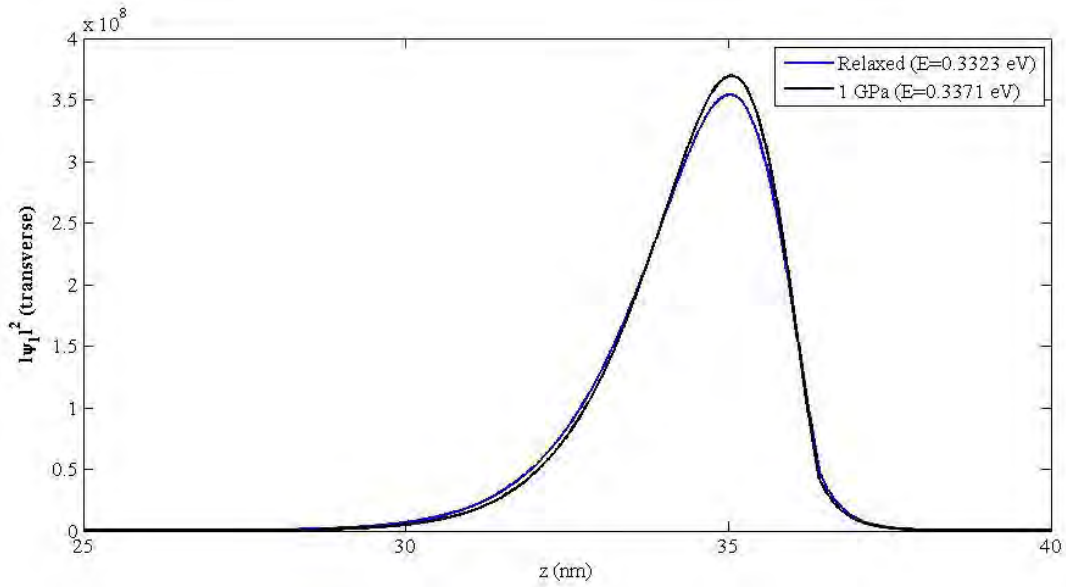


Figure 3.3: Normalized wave function for 1st eigen energy of transverse valley (HfO_2)

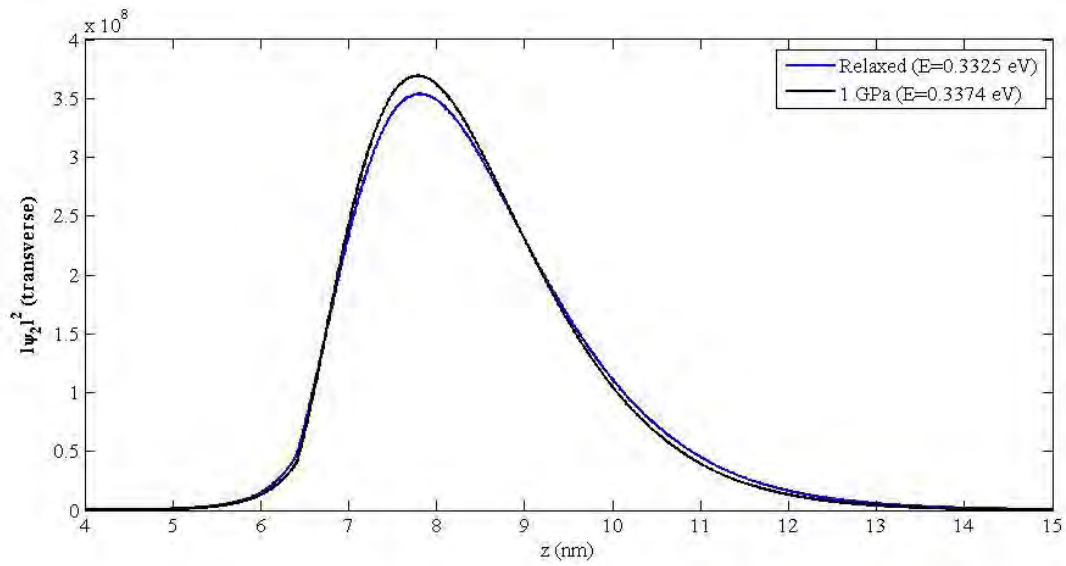


Figure 3.4: Normalized wave function for 2ndeigen energy of transverse valley (HfO_2)

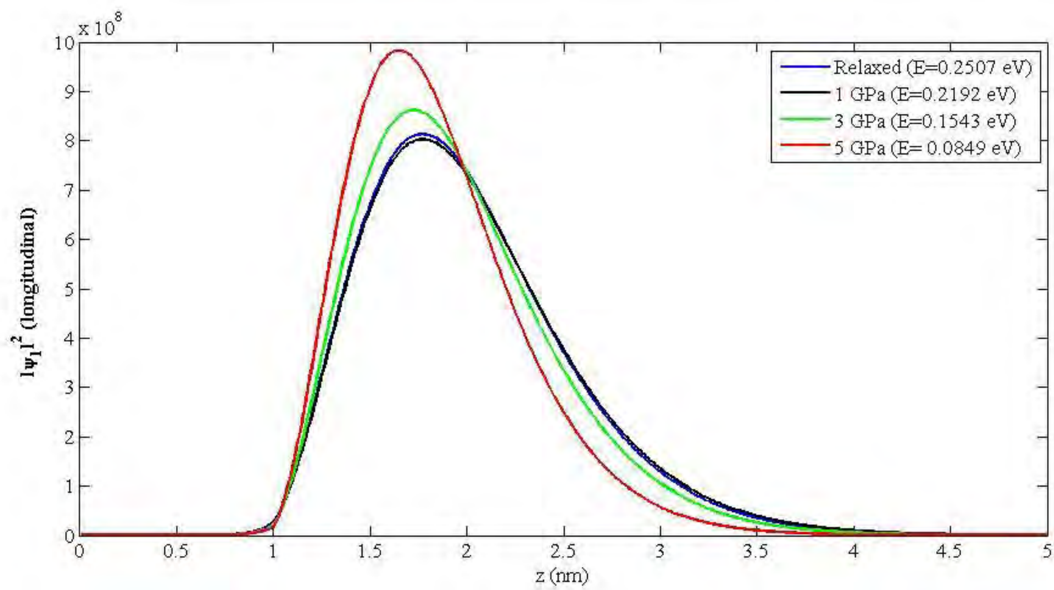


Figure 3.5: Normalized Wave function for 1steigen energy of longitudinal valleys (SiO_2)

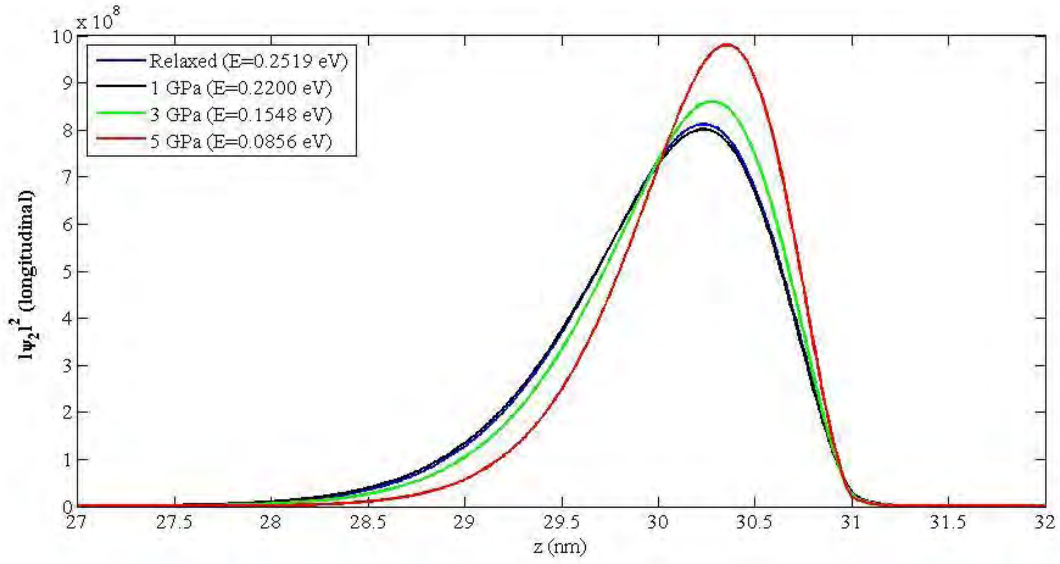


Figure 3.6: Normalized wave function for 2nd eigen energy of longitudinal valley (SiO_2)

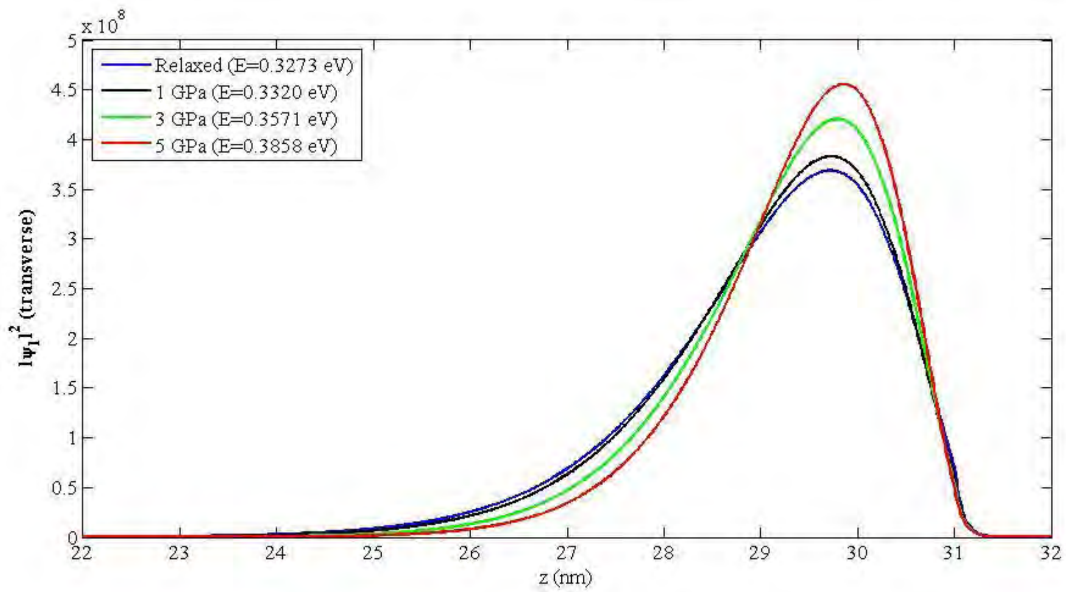


Figure 3.7: Normalized wave function for 1st eigen energy of transverse valley (SiO_2)

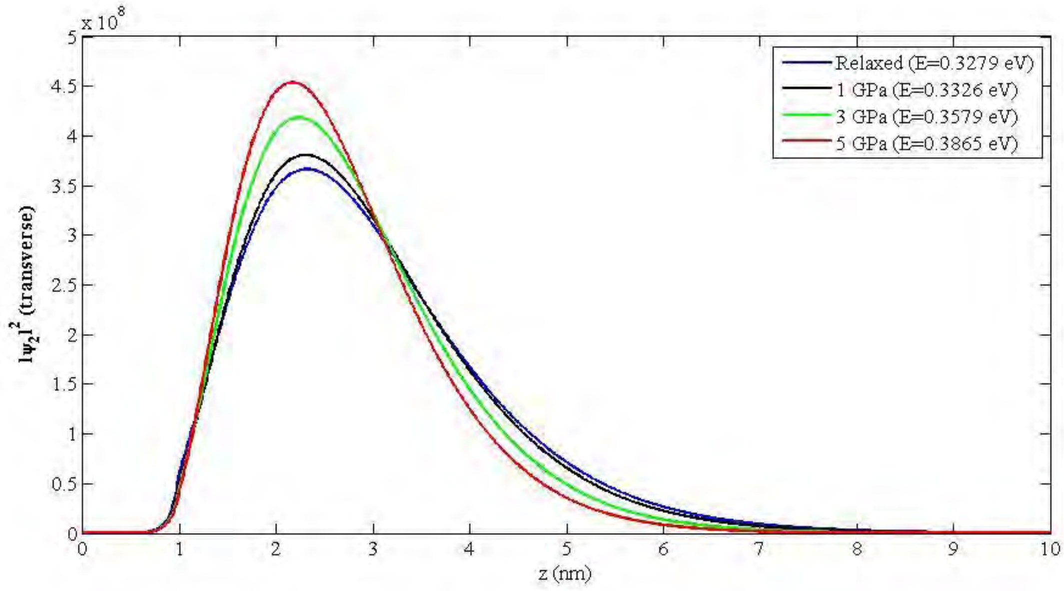


Figure 3.8: Normalized wave function for 2nd eigen energy of transverse valley (SiO_2)

Normalized wave functions both for HfO_2 and SiO_2 are shown here for various strain. In Figure 3.1, the wave function penetration into the dielectric region has been notified. For 1 nm EOT, the physical thickness of HfO_2 is 6.41 nm and the wave functions spread their tails into this region.

From the solution of Schrodinger's equation, also the corresponding eigen energies have been found. Due to uniaxial strain the conduction band of longitudinal valley goes down and the conduction band of transverse valley goes up. Therefore, the eigen energies of the longitudinal valleys are smaller than that of the transverse valleys.

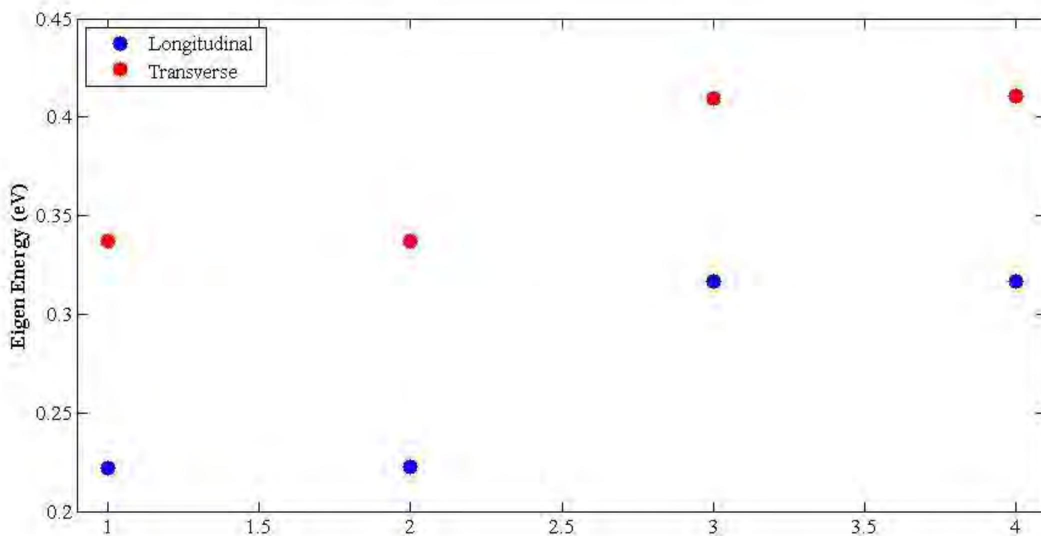


Figure 3.9: 1st four eigen energies of longitudinal and transverse valleys (HfO_2, 1 GPa)

In figure 3.9, 1 GPa stress is applied and the differences of eigen energies between longitudinal and transverse valleys have been observed. For higher stress these differences are increased and electrons prefer to be occupied in the longitudinal valleys.

The behavior of the eigen energies with increasing strain has been observed in figure 3.10 and 3.11 both for HfO_2 and SiO_2 and it has been seen that strain lowers the eigen energies.

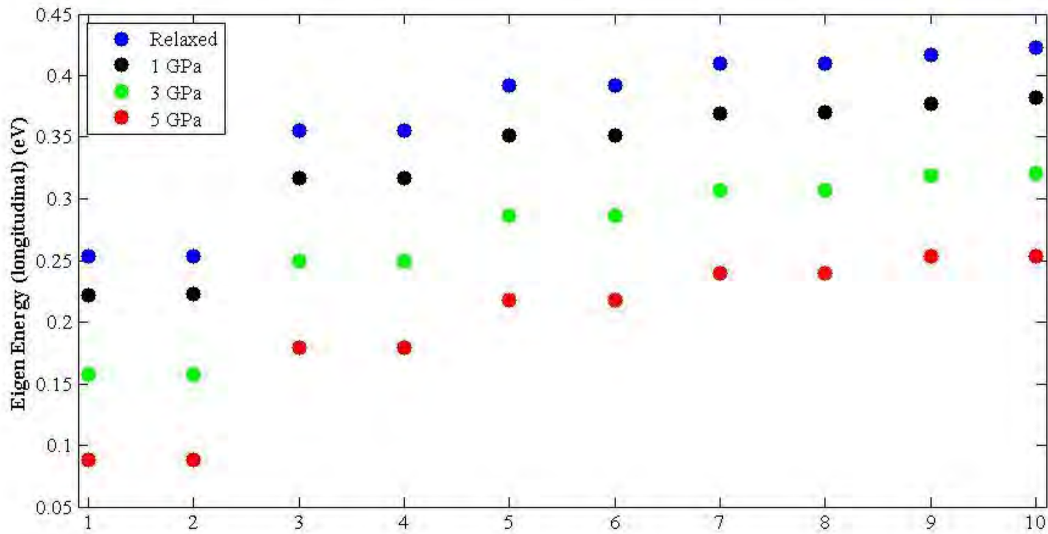


Figure 3.10: 1st ten eigen energies for various strain (HfO_2)

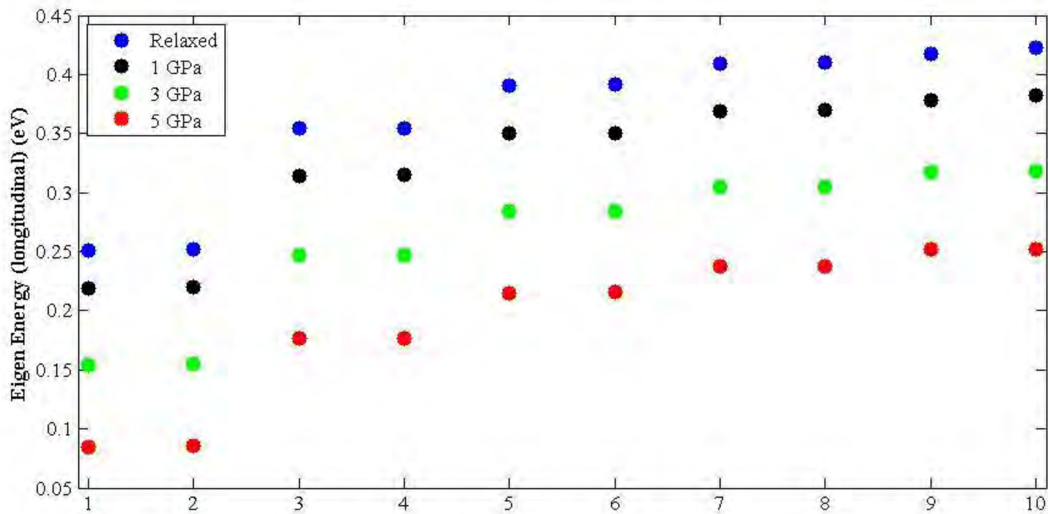


Figure 3.11: 1st ten eigen energies for various strain (SiO_2)

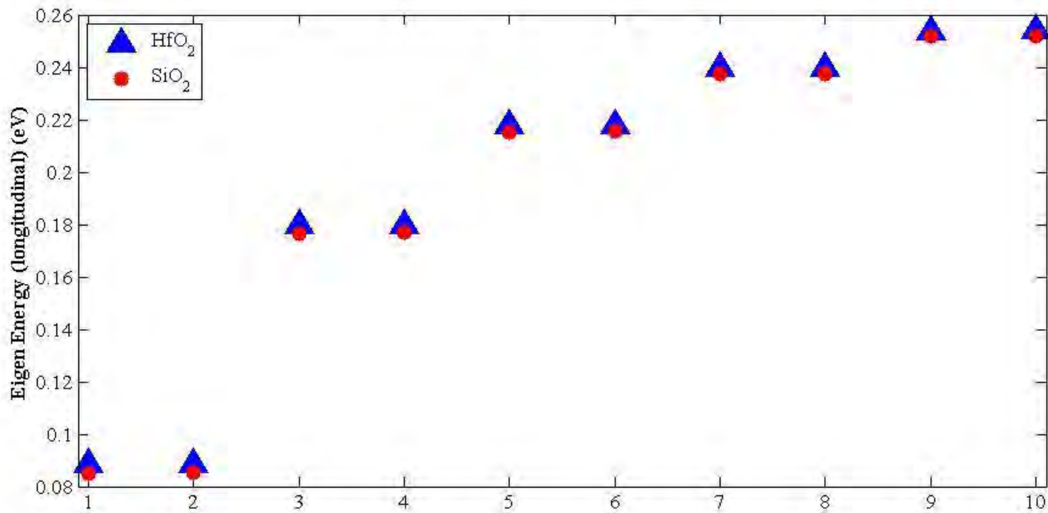


Figure 3.12: 1st ten eigen energies both for HfO_2 and SiO_2 as dielectrics (P= 5GPa)

The values of eigen energies of HfO_2 and SiO_2 are nearly same, although the eigen energies of HfO_2 is slightly higher as shownin figure 3.12.

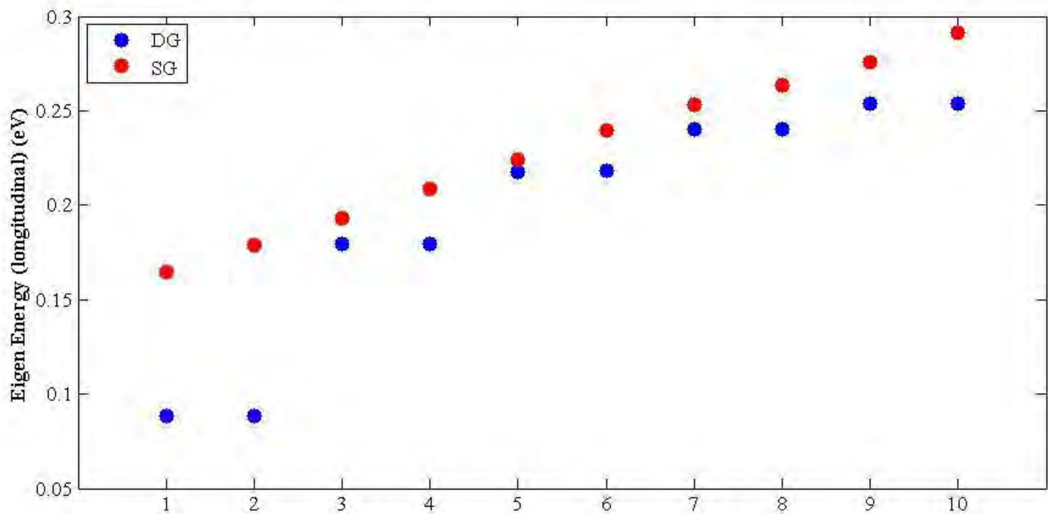


Figure 3.13: The eigen energies for SG and DG MOSFET with HfO_2 as dielectric (P= 5GPa)

For single-gate MOSFET, the eigen energies are larger than the double-gate MOSFET and for DG MOSFET, the eigen energies are in pairs due to their symmetric structure.

The Schrodinger's equation and the Poisson's equation are fully coupled to obtain the final electrostatic of the device and to calculate capacitance and gate leakage current density.

Chapter Four

Results and Discussions

4.1 Charge Calculation

The carrier concentration in the jth subband of the ith valley is given by

$$N_{ij} = \frac{n_{vi} m_{di} kT}{\pi \hbar^2} ln\left[1 + \exp(\frac{E_F - E_{ij}}{kT})\right]$$

Here, n_{vi} is the valley degeneracy, m_{di} is the density of state mass in the ith valley and E_{ij} is the eigen energy in the jth subbandof the ith valley. In DG structure, the substrate is not connected with ground; therefore the quasi-fermi level E_F has been calculated.

The Inversion charge distribution can be found from

$$\rho_{inv}(z) = -q \sum_{i,j} N_{ij} \left|\psi_{ij}(z)\right|^2$$

Therefore, the inversion charge per unit area,

$$Q_{inv} = \int \rho(z) dz$$

and the total charge

$$Q_t = Q_{inv} + t_{Si} * \rho_{dep}$$

The depletion charge per unit area is unchanged as the device is fully depleted; therefore the effects of uniaxial strain are same for both Q_t and Q_{inv}.

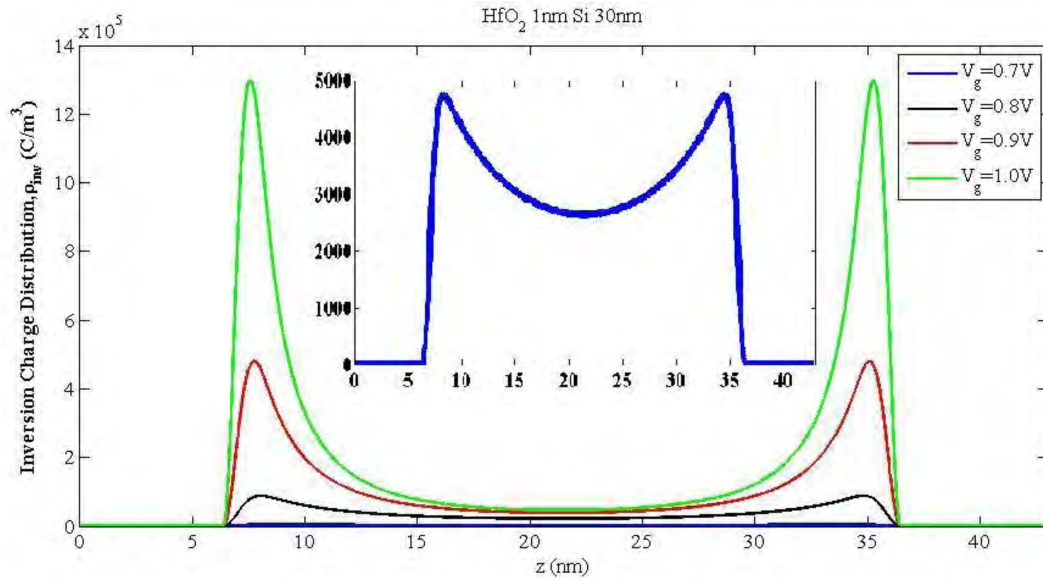


Figure 4.1: Inversion charge distribution for various gate voltages (HfO_2)

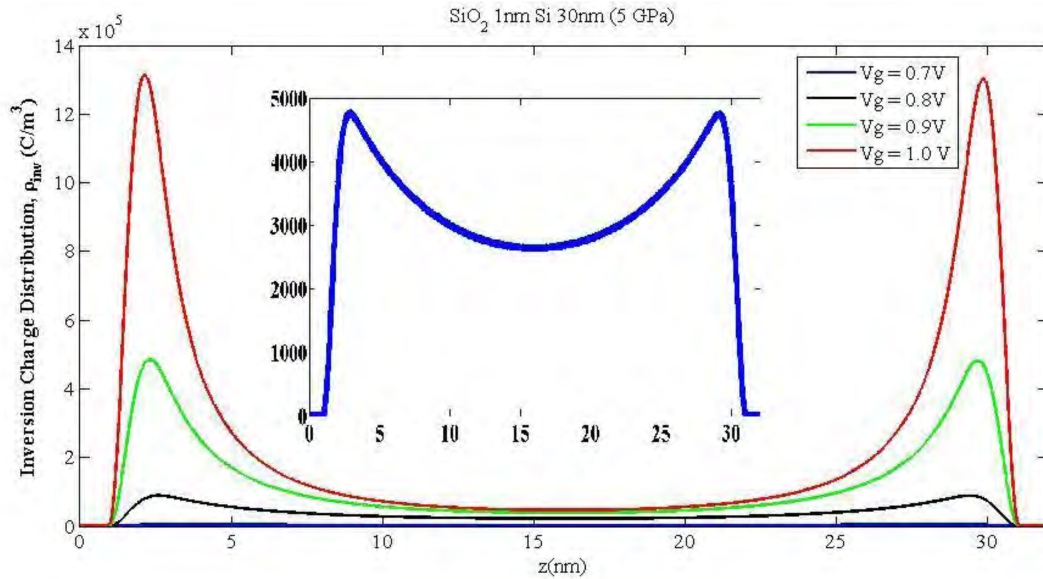


Figure 4.2: Inversion charge distribution for various gate voltages (SiO_2)

As the gate voltage increases the device goes from depletion to inversion region and the inversion charge decreases in the middle of the Si substrate making the two inversion channel decoupled (Figure 4.1 and 4.2)

The uniaxial strain causes the inversion charge to increase and also shifts the inversion channel towards the interface which improves the control of the gate on the channel. These have been observed in Figure 4.3 and 4.4.

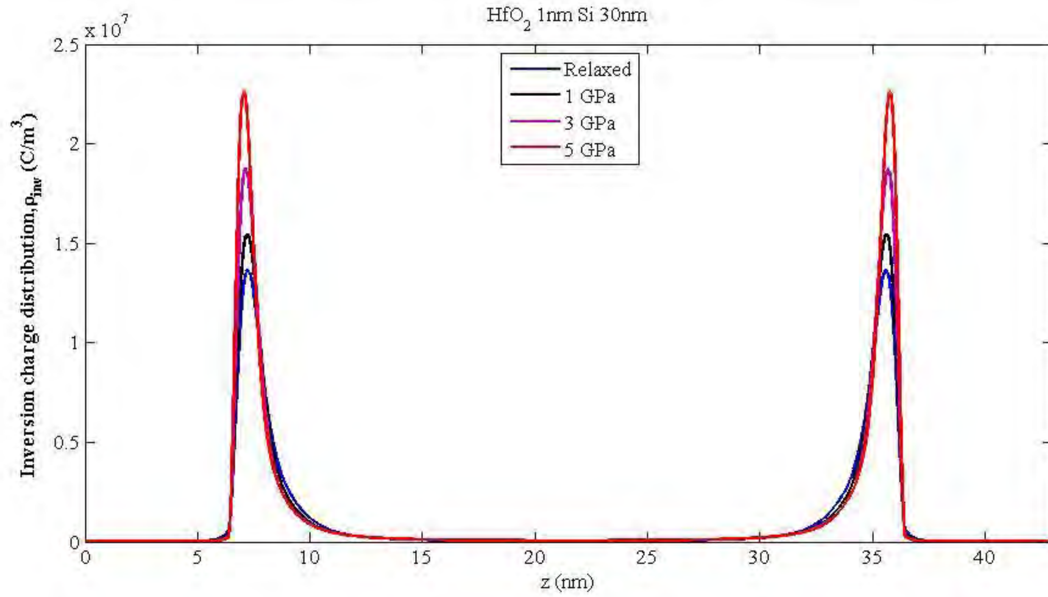


Figure 4.3: The effects of strain on inversion charge distribution (HfO_2)

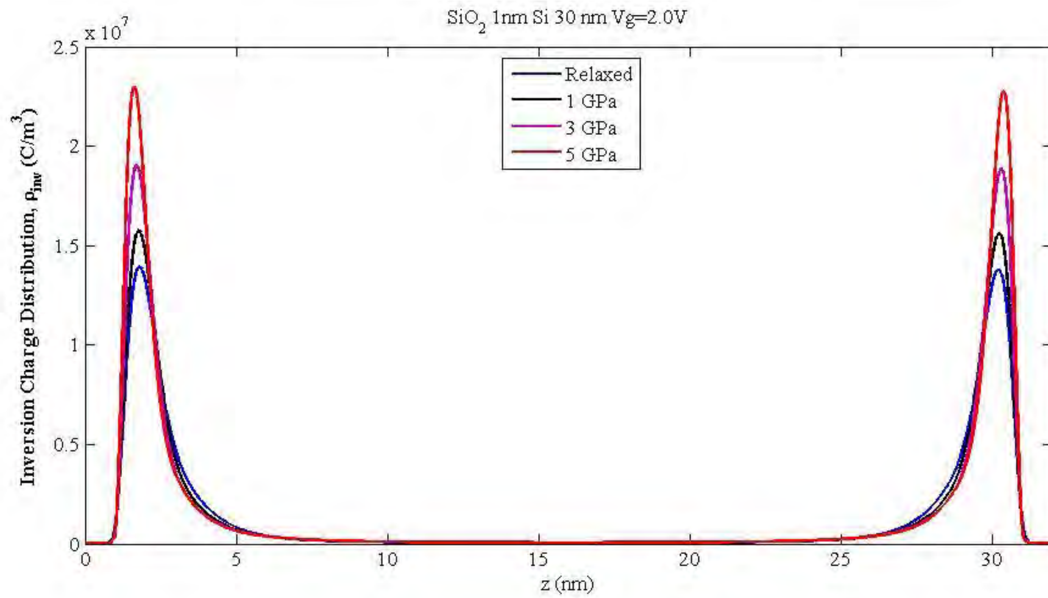


Figure 4.4: The effects of strain on inversion charge distribution (SiO_2)

The shift of inversion channel is clarified from the following figures (Figure 4.5 and 4.6). In Figure 4.5, the distance from the interface of the peak position of inversion charge distribution is calculated. The distances become smaller with increasing strain. The shifting of the channel by uniaxial strain is more effective when HfO_2 is used as dielectrics, as shown in figure 4.6. Here the percentage change in distances with respect to the relaxed condition has been calculated.

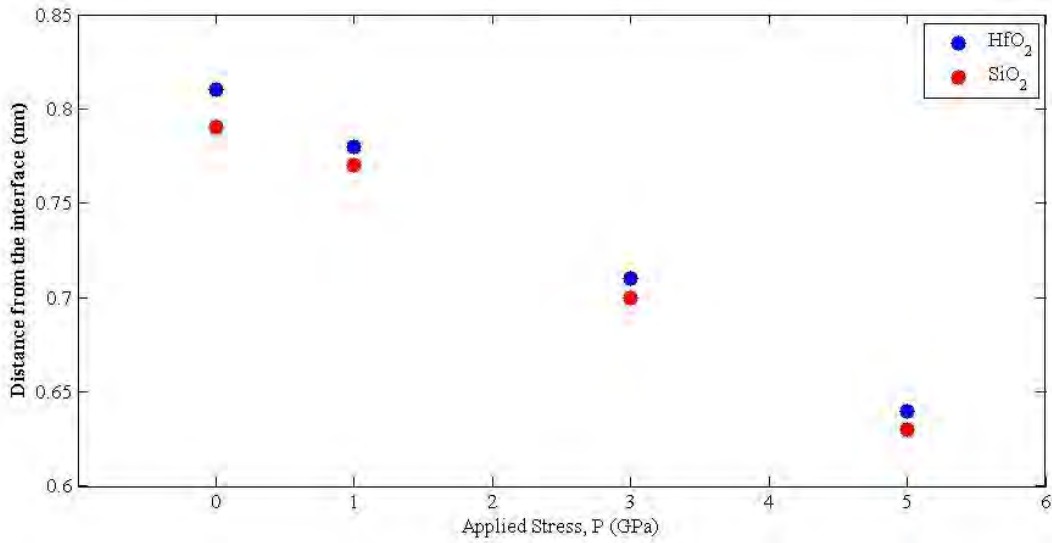


Figure 4.5: The distance from the interface of the peak position of inversion charge distribution

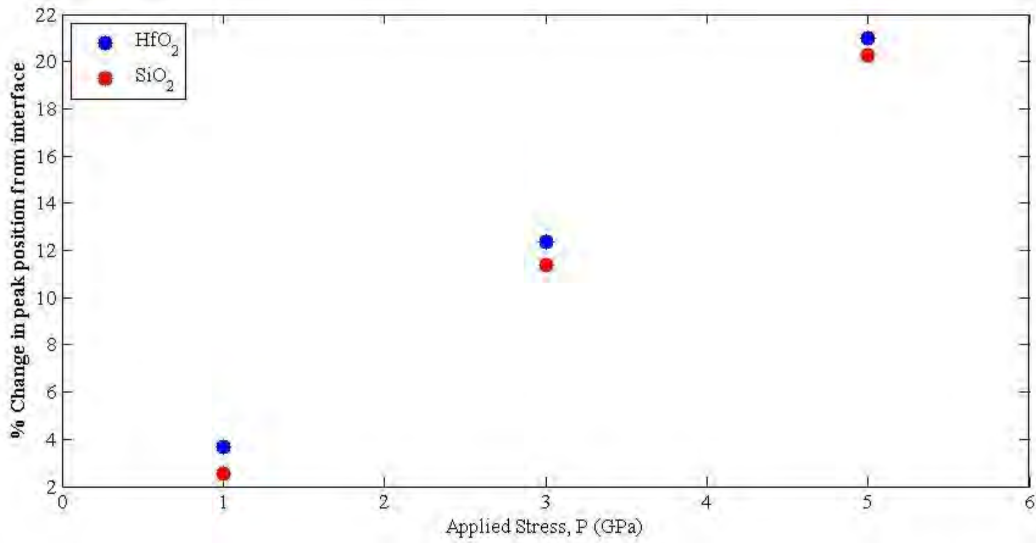


Figure 4.6: Percentage change of the distances with respect to the relaxed condition

Electrons by nature first fill the lower energy state. Moreover, if the number of lower energy states is increased in the conduction band more electrons are able to transit from the valence band to the conduction band. Uniaxial stress lowers the energy state and thus increases the total charge as shown in figure 4.7 and figure 4.8.

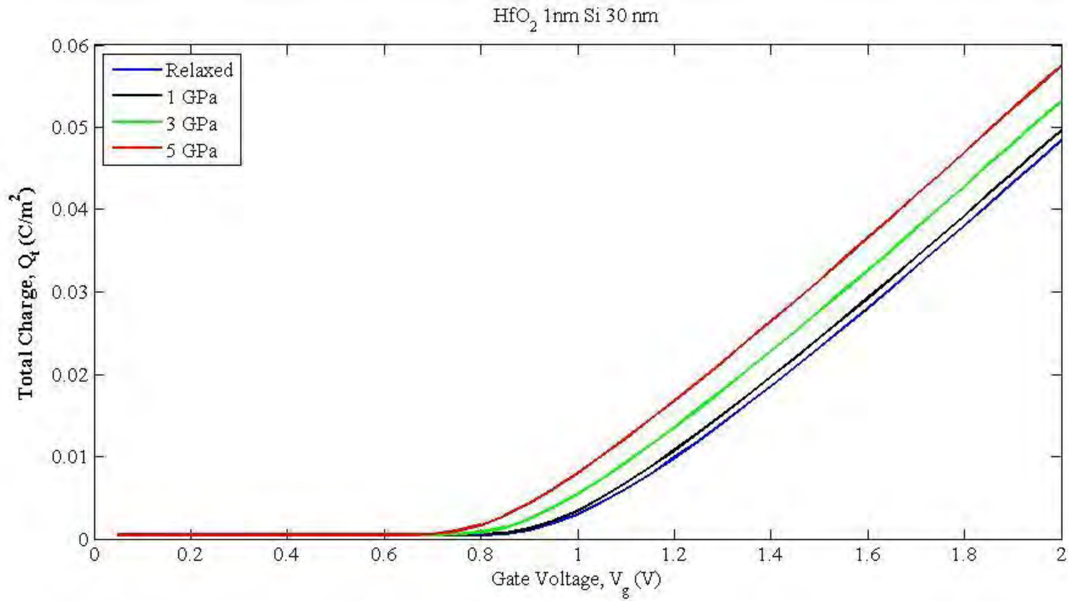


Figure 4.7: Increase of total charge with applied stress (HfO_2)

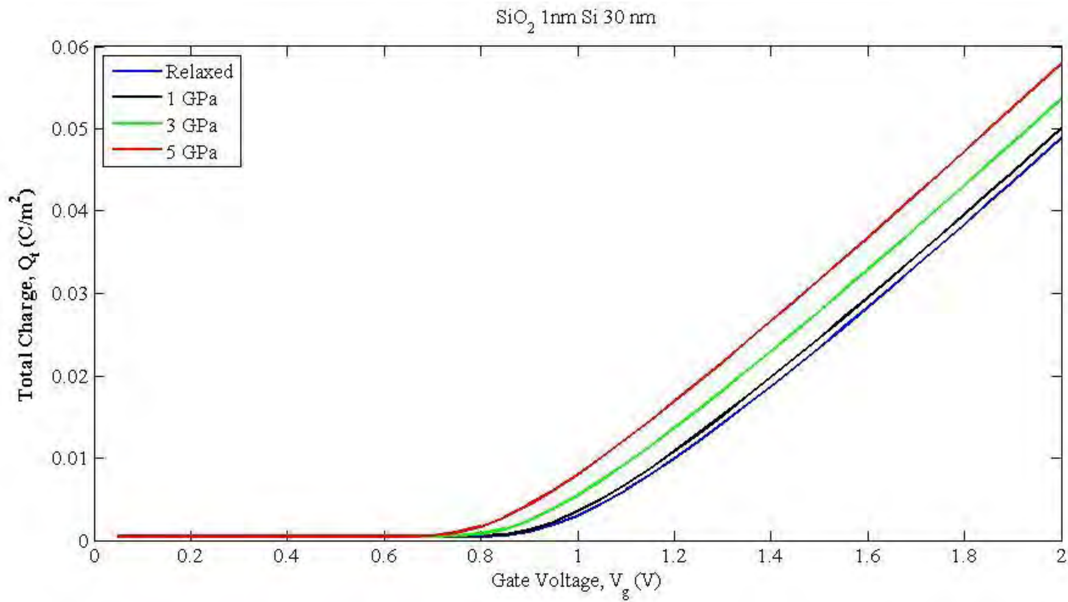


Figure 4.8: Increase of total charge with applied stress (SiO_2)

As EOT is kept same for both dielectrics, the total charges are almost same and the difference between them is on the 10^{-4} C/m^2 order (Figure 4.8). The percentage change between HfO_2 and SiO_2 are also calculated and it has been observed that the change is below 1% after applying stress.

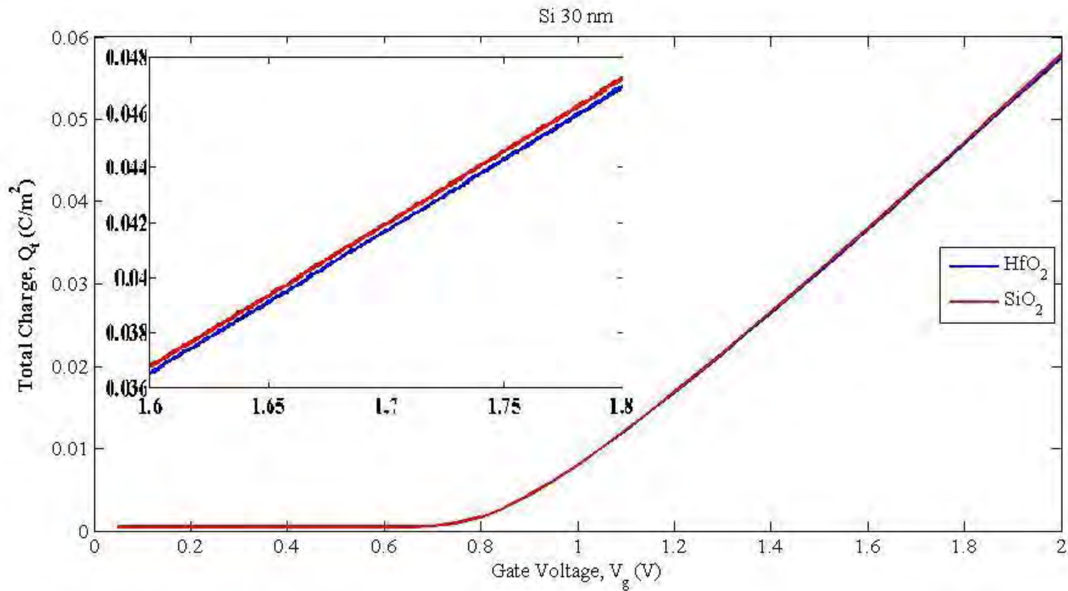


Figure 4.9: Comparison of total charges of HfO_2 and SiO_2 at 5 GPa

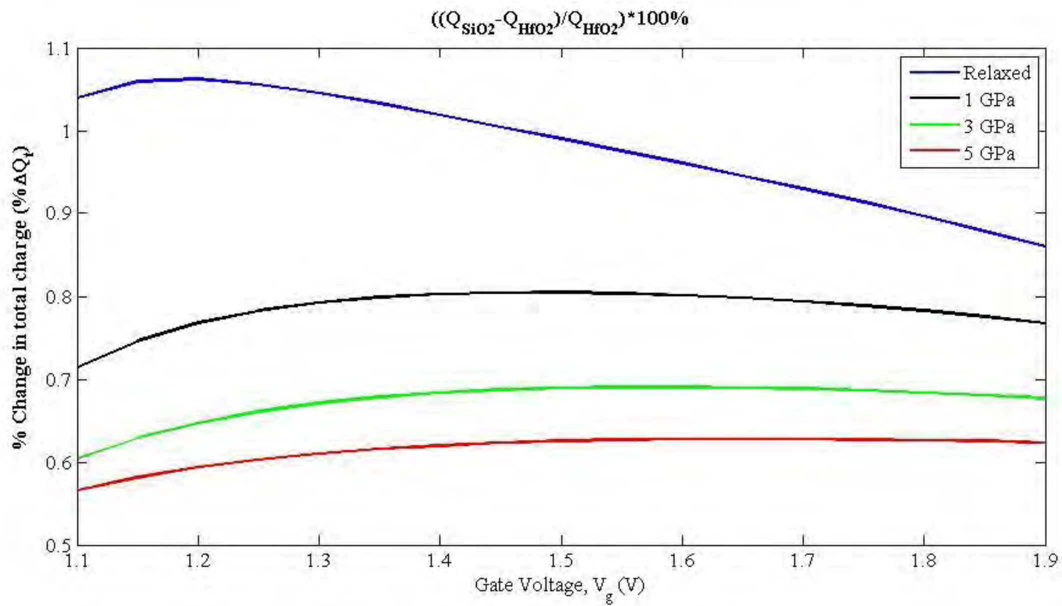


Figure 4.10: Percentage change in total charge for various stresses

The total charge of double-gate MOS is compared with that of the single-gate and the total charge of DG MOS is double of that of SG MOS as anticipated (Figure 4.11). In figure 4.12, the calculation of percentage change depicts that it is almost 50% in the inversion region.

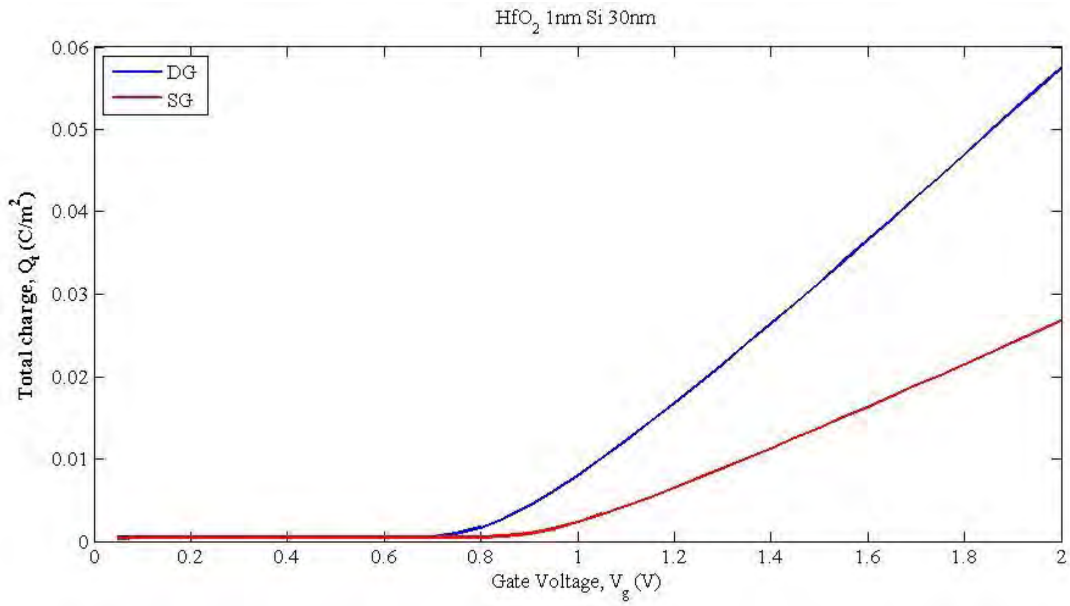


Figure 4.11: Total charge of DG and SG MOS at 5 GPa

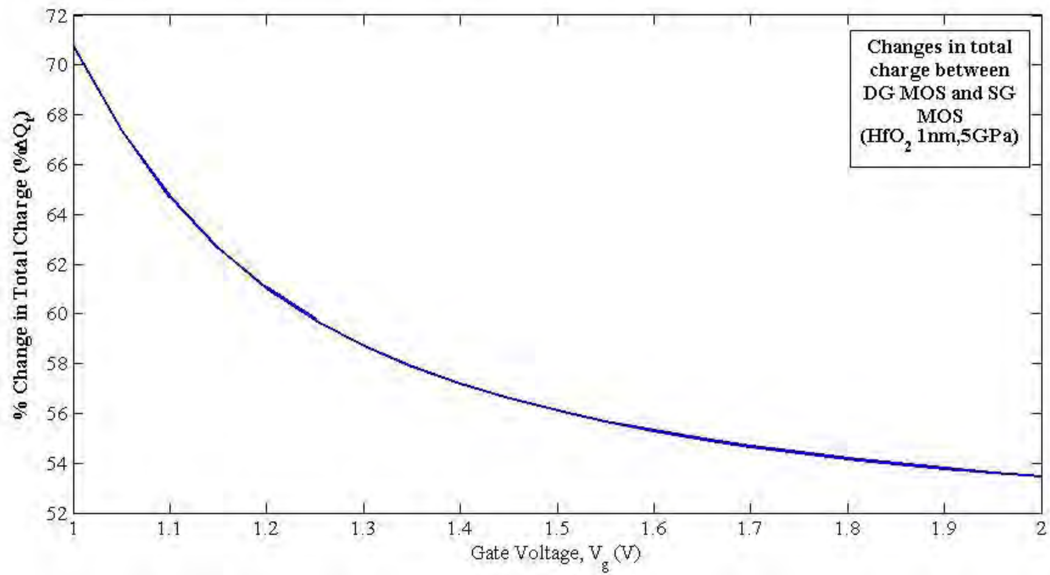


Figure 4.12: The percentage change between the DG and SG MOS with respect to the DG MOS.

4.2The effects on Gate Capacitance

As the total charge has been increased with strain, the gate capacitance is also increased by 2.5% in the strong inversion as depicted in figure 4.14 and 4.16. Threshold voltage shifts from 0.75 V at relaxed condition to 0.6 after applying 5 GPa stress (figure 4.15 and 4.17).

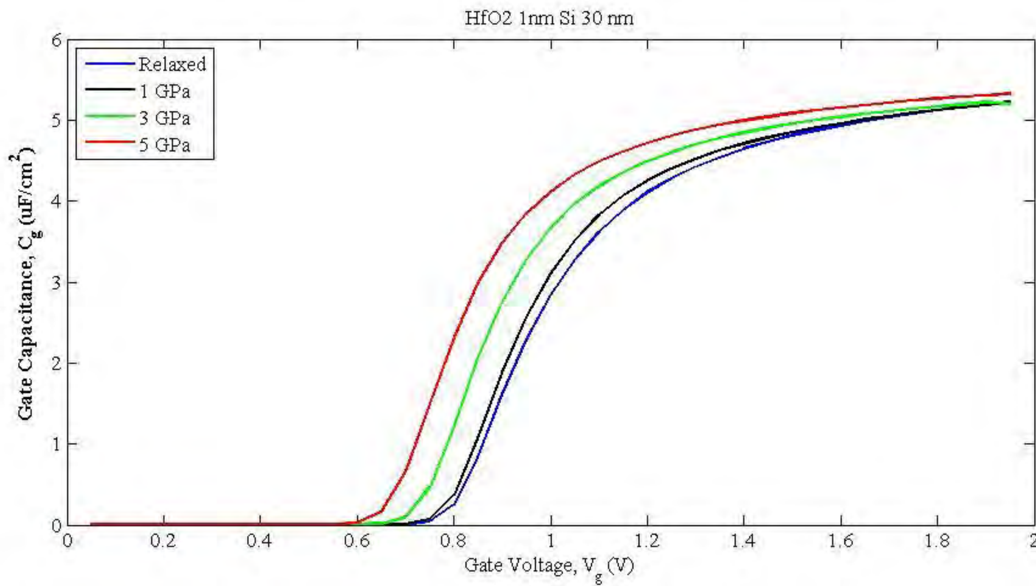


Figure 4.13: The variation of gate capacitances with applied stress (HfO_2)

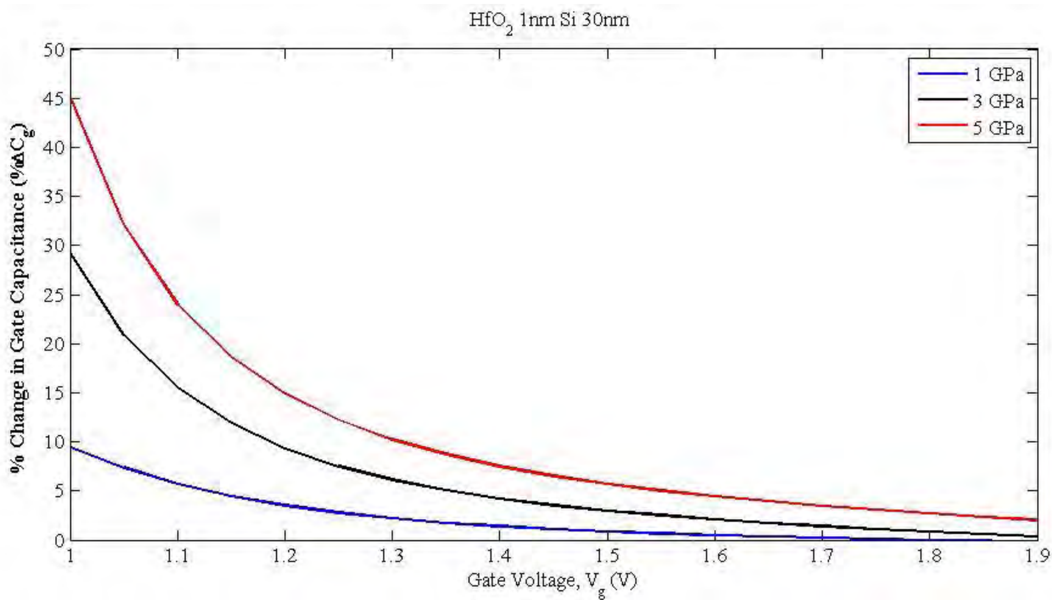


Figure 4.14: The percentage change in Gate Capacitances (HfO_2)

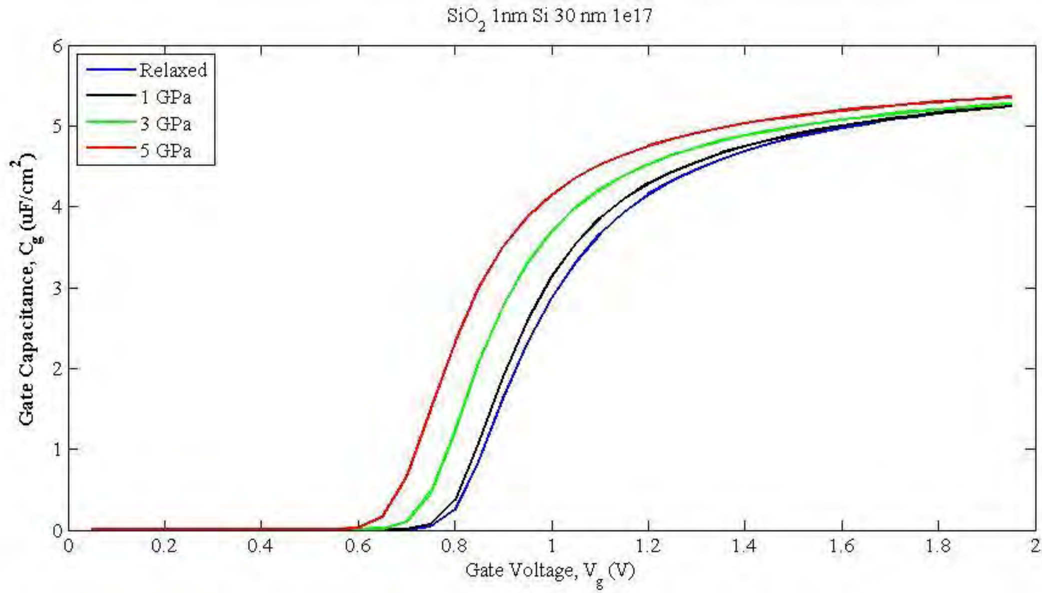


Figure 4.15: The variation of gate capacitances with applied stress (SiO_2)

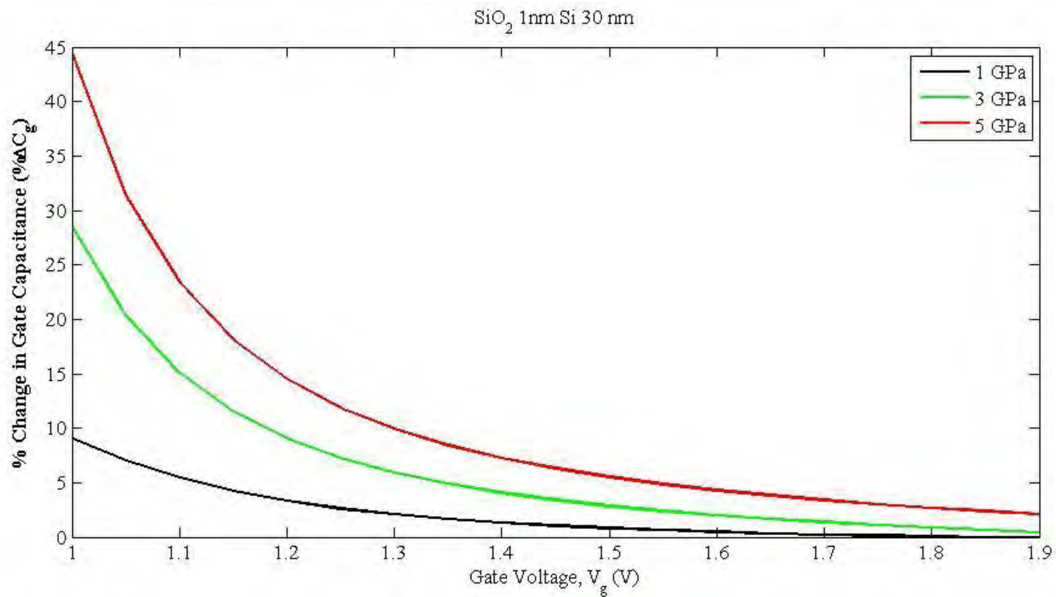


Figure 4.16: The percentage change in Gate Capacitances (SiO_2)

The comparison between the HfO_2 and SiO_2 follows the comparison of total charge and the difference of gate capacitances between them is on the order of 1 nm/F (figure 4.17). The percentage change is also below 1% for gate capacitance (figure 4.18).

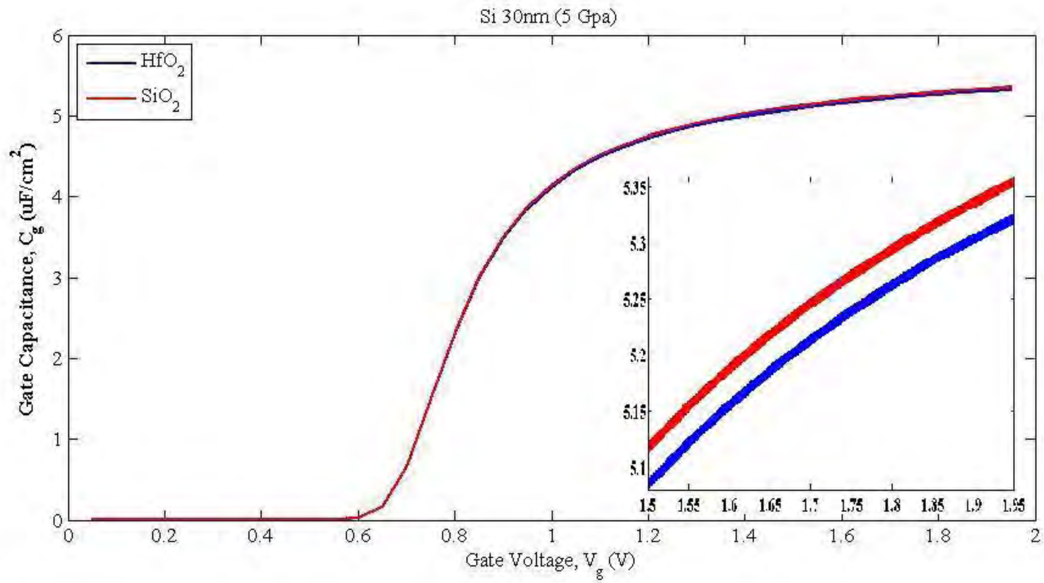


Figure 4.17: The comparison of gate capacitances between HfO_2 and SiO_2 at 5GPa

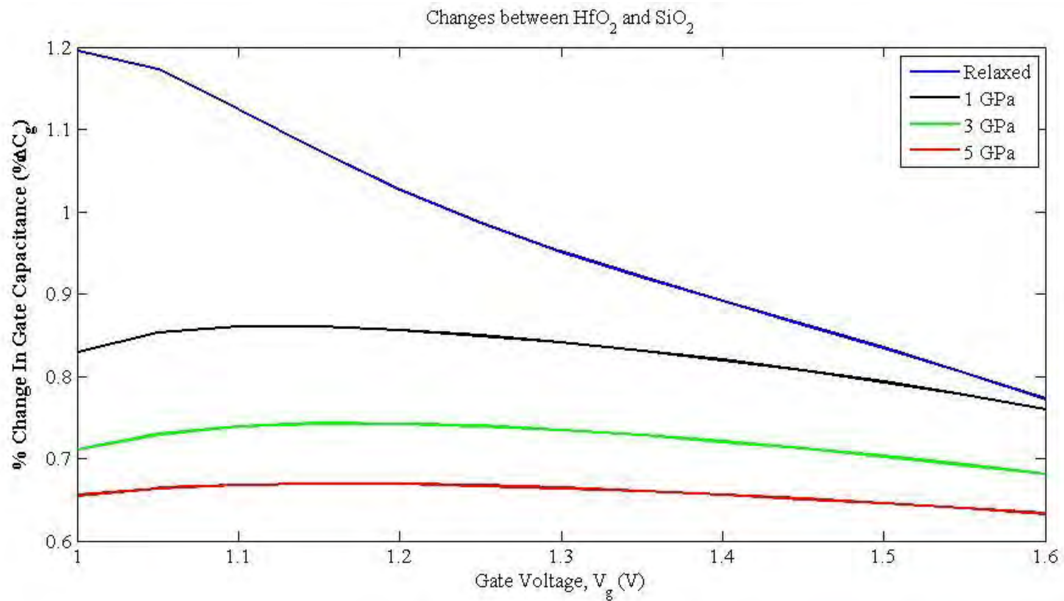


Figure 4.18: The percentage change in gate capacitances at various gate voltages

The percentage change in gate capacitances with strain increases and is almost 6% at 5GPa as observed in figure 4.19. Another thing is that the change for HfO_2 is greater than that of the SiO_2.

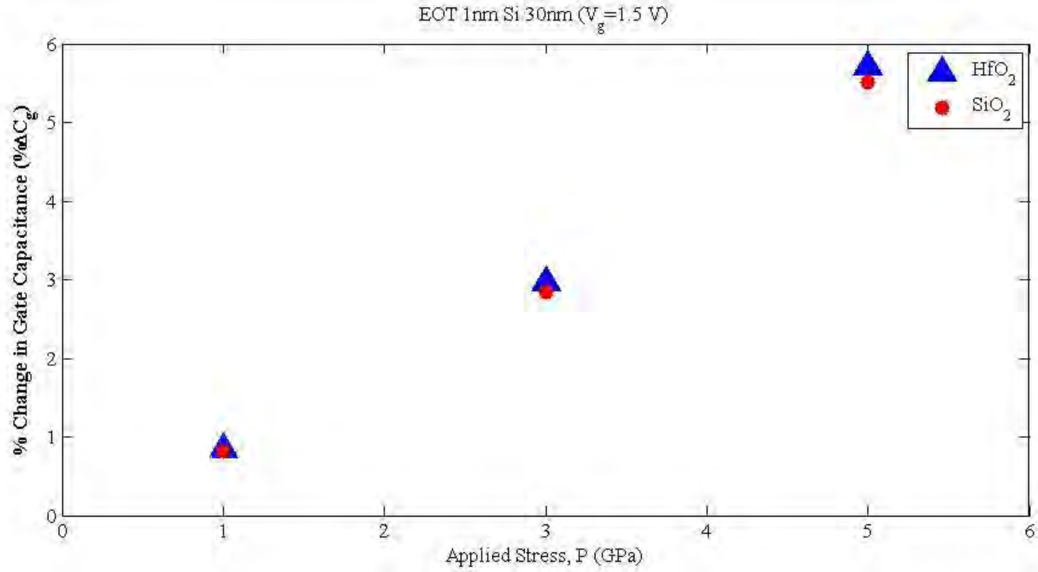


Figure 4.19: The percentage change in gate capacitances at various stresses

The gate capacitance is doubled for DG MOSFET as compared with SG MOSFET and the percentage change is around 50% showing in figure 4.20 and 4.21 respectively.

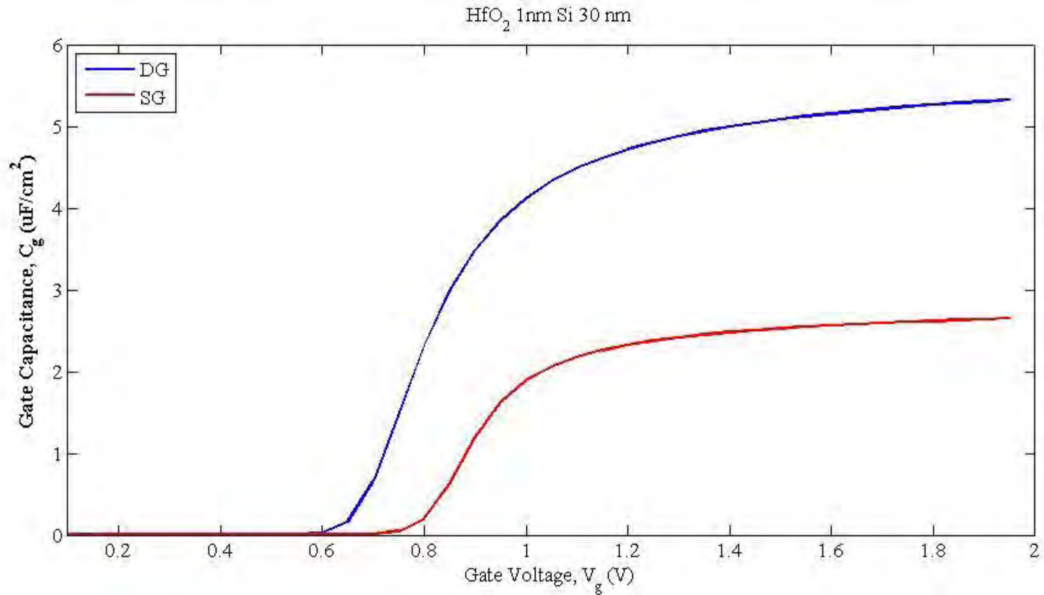


Figure 4.20: The comparison of gate voltages between DG and SG MOSFET at 5 GPa

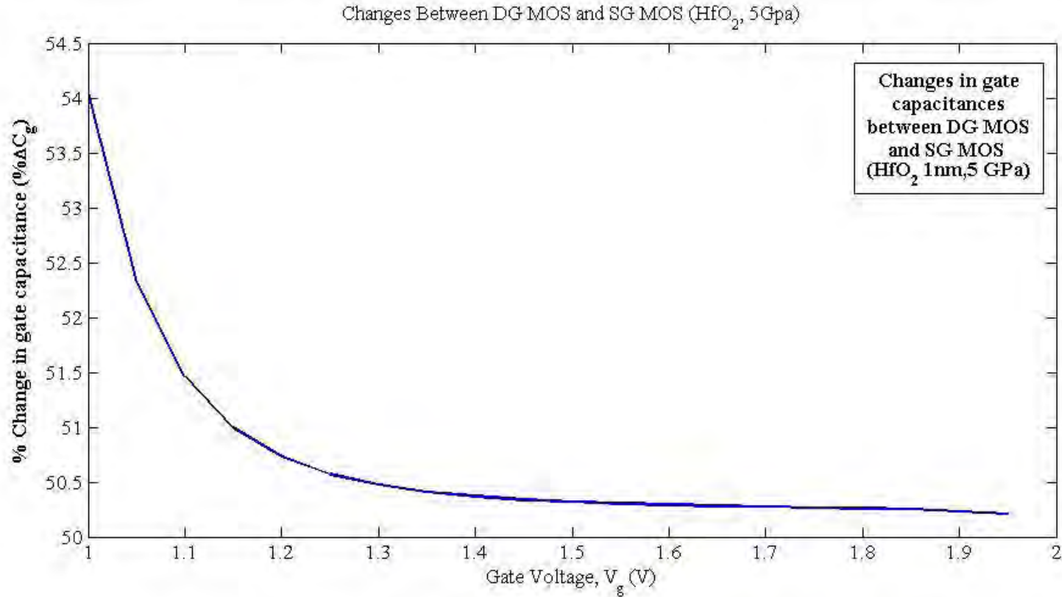


Figure 4.21: The percentage change of gate capacitance in SG MOS with respect to DG MOS

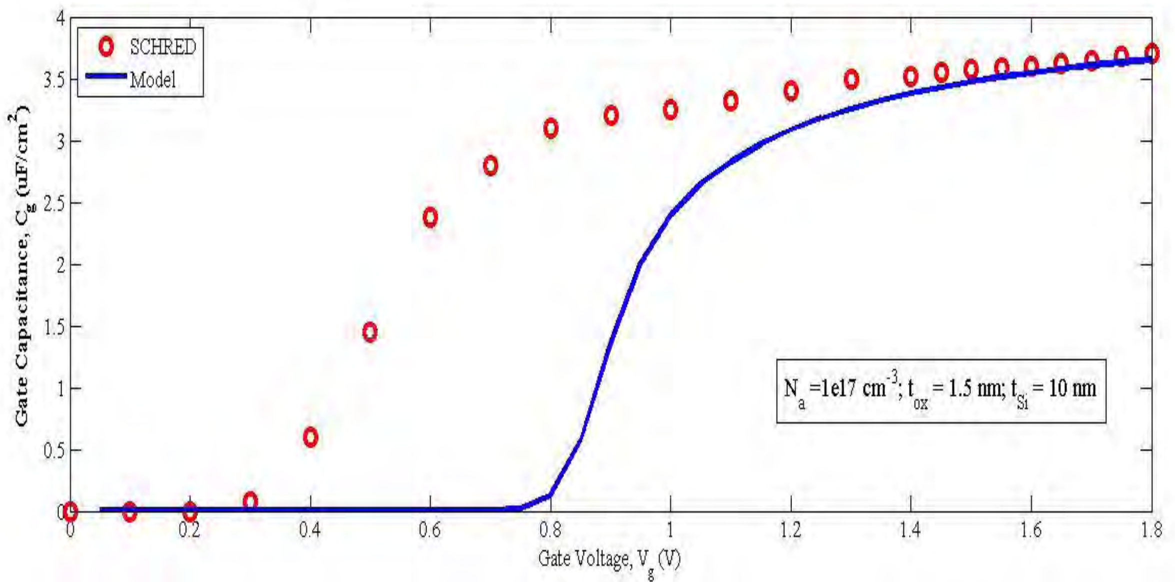


Figure 4.22: The comparison with SCHRED-predicted total Gate Capacitance

To verify the numerical calculation, I consider an n-channel symmetric DG device with 1.5 nm thick SiO_2 and 10 nm thick Si substrate. I compare my numerical calculation with result obtained from SCHRED (a well-known established numerical solver developed at Pardue University available through www.nanohub.org). The result in SCHRED agrees well with corresponding strong inversion region as shown in figure 4.22. The SCHRED does not consider wave function

penetration effects. Therefore, their data overestimates the inversion charge in the weak inversion region and does not match with my data. If the charges in the dielectric region are considered to be in the channel region, then it is expected that the simulated data will follow the data from SCHRED.

4.3The effects on Gate leakage current

The strain lowers the eigen energy thus increases the carrier lifetime τ_{ij} of electron and electrons now occupy lower energy state; therefore the tunneling of electrons are decreased after applying stress as shown in figure 4.23 and 4.24.

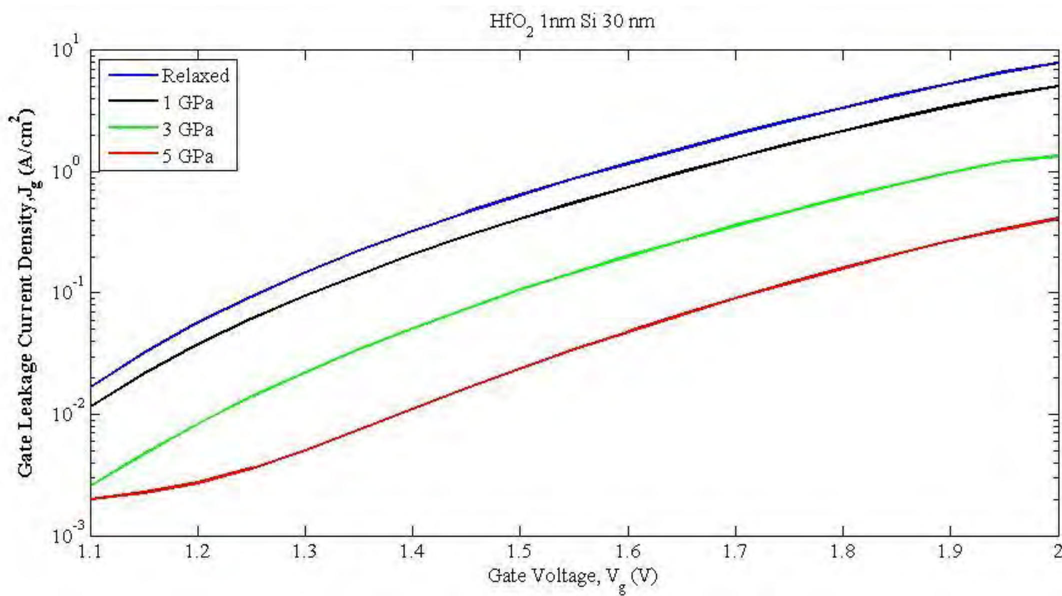


Figure 4.23: Gate leakage current density at various stresses (HfO_2)

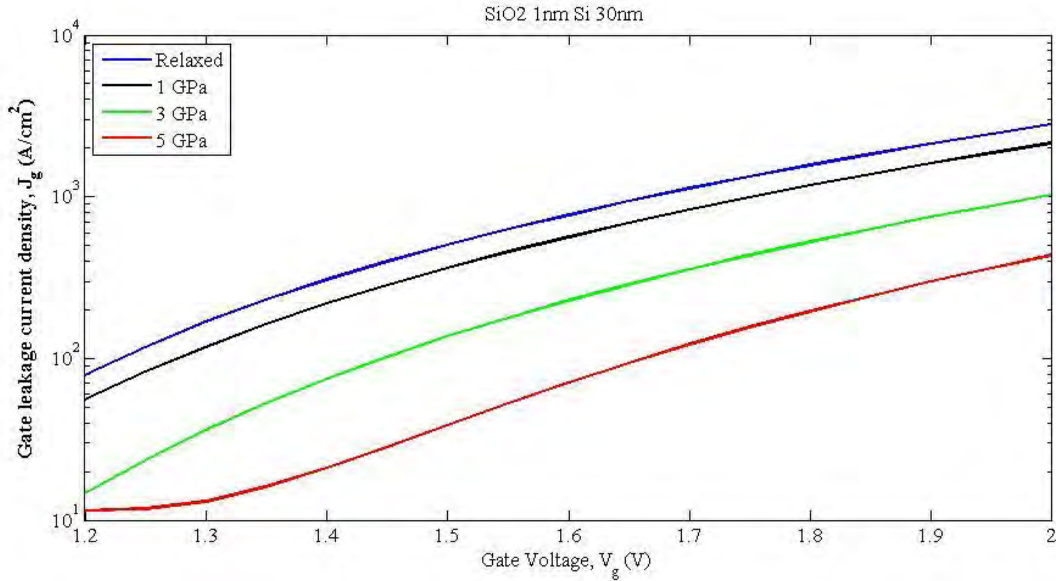


Figure 4.24: Gate leakage current density at various stresses (SiO_2)

The physical thickness of high-k dielectric can be increased without degrading the gate capacitance as EOT remains same. This is the major motivation of using high-k dielectric like HfO_2. In figure 4.25, it has been observed that the gate leakage current can be decreased by four decade at 5 GPa.

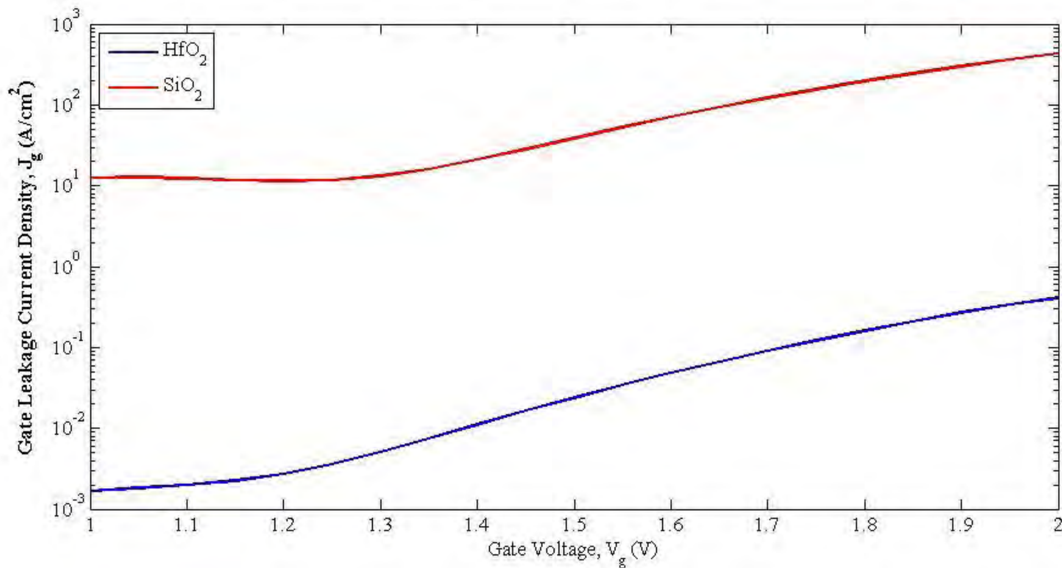


Figure 4.25: Comparison of Gate leakage Current density between HfO_2 and SiO_2

The gate leakage current of DG MOS decreases as compared with SG MOS due to its reduced vertical field. The vertical electric field caused by one gate voltage is lowered by the opposite

gate voltage. The gate leakage current of DG MOS is about 10^4 A/cm^2 smaller than the SG MOS as depicted in figure 4.26.

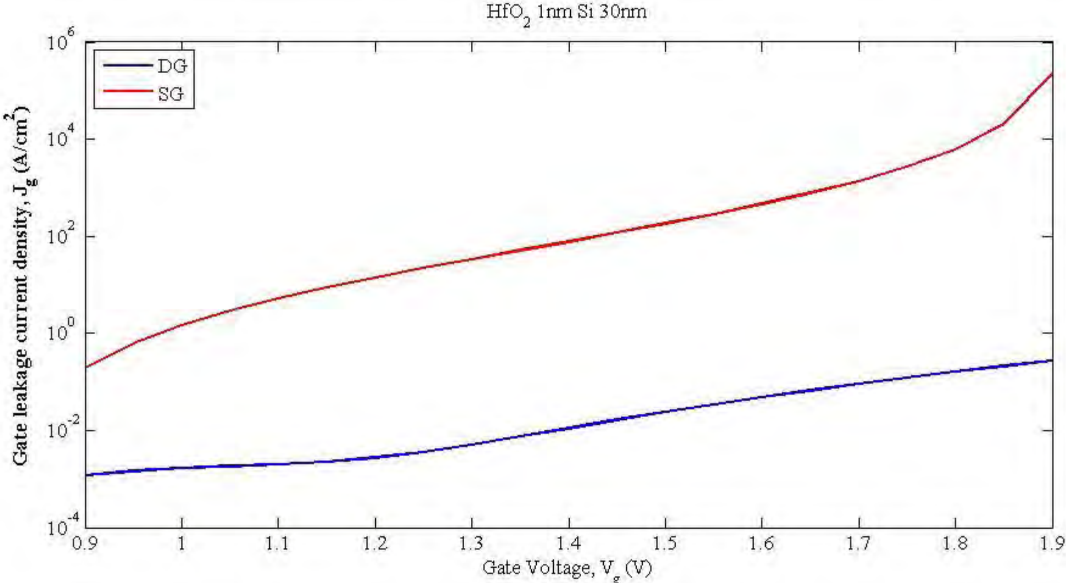


Figure 4.26: Comparison of gate leakage current between DG MOS and SG MOS

Chapter 5
Conclusion

5.1 Conclusion

It is highly expected that uniaxial strain can give better performance and enhance the advantageous features of high-k double gate MOSFET. Uniaxial strain decreases the value of eigen energies and hence increasing the total charge. This increases the gate capacitances. It is also observed that the value of threshold voltages decreases and the inversion channel shifts towards the Si/HfO_2 interfaces. The gate leakage current density can be reduced for both using high-k dielectric and applying uniaxial stress. If the two gates alignment problem and other fabrication challenges of strained technology can be overcome, then high-k DG MOSFET incorporating uniaxial strain will be a promising device for future circuit simulation.

5.2 Future Works

Self-consistent solution can also be used to simulate Asymmetric Double-Gate MOSFET and other multiple gate devices. My work considers n-channel substrate, the p-channel substrate can also be considered by taking some modifications into account. In this thesis, 1D analysis of DG MOSFET is performed. But when voltage is applied into the drain, a 2D analysis is necessary to calculate the mobility and I-V characteristics. The effects of Si film thickness can also be observed on gate capacitance and gate leakage current. We have fixed the EOT at 1nm, the impact of uniaxial strain on a device having EOT < 1 nm will also be presented. There are five types of mechanisms for gate leakage current, the direct tunneling current and bound state tunneling current are considered here. Including tunneling due to thermionic emission of hot electron, Fowler-Nodheim (FN) tunneling and band-to-band tunneling, more accurate values of gate leakage current will be obtained. To incorporate the thermionic emission and the FN tunneling, higher eigen energy state should be included. Interface trap charge is also necessary to compute for exact values of total charge.

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