Effect Of Strain On Electrostatic And Ballistic Transport Performance Limit For High Mobility Substrate MOSFETs And MOS HEMTs

A thesis submitted for the partial fulfillment of the requirement of the degree

of

Master of Science in Electrical and Electronic Engineering

by

Raisul Islam

Department of Electrical and Electronic Engineering,

Bangladesh University of Engineering and Technology,

Dhaka-1000

August, 2011

Effect of Strain on Electrostatic and Ballistic Transport Performance Limit for High Mobility Substrate MOSFETs and MOS HEMTs

by

Raisul Islam

Master of Science in Electrical and Electronic Engineering

Department of Electrical and Electronic Engineering

Bangladesh University of Engineering and Technology

August, 2011

Contents

List of Figures

List of Tables

Certification

The thesis titled **"Effect of Strain on Electrostatic and Ballistic Transport Performance Limit for High Mobility Substrate MOSFETS and MOS HEMTS"** submitted by Raisul Islam, Roll no. 1009062032P, session: October, 2009, has been accepted satisfactory in partial fulfillment of the requirement for the degree of *Master of Science in Electrical and Electronics Engineering* on August 20, 2011.

Board of Examiners

Chairman

Dr. Quazi Deen Mohd. Khosru
Professor,
Department of Electrical and Electronics Engineering,
Bangladesh University of Engineering and Technology,
Dhaka - 1000, Bangladesh.

Member (Ex-Officio)

Dr. Md. Saifur Rahman
Professor & Head,
Department of Electrical and Electronics Engineering,
Bangladesh University of Engineering and Technology,
Dhaka - 1000, Bangladesh.

Member

Dr. A. B. M. Harun-Ur-Rashid
Professor,
Department of Electrical and Electronics Engineering,
Bangladesh University of Engineering and Technology,
Dhaka - 1000, Bangladesh.

Member (External)

Dr. Zahid Hasan Mahmood
Professor,
Department of Applied Physics, Electronics & Communication Engineering,
University of Dhaka,
Dhaka - 1000, Bangladesh.

Declaration

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree of diploma.

Signature of the candidate

_____

Raisul Islam

Acknowledgment

The author would like to convey his gratitude to Dr. Quazi D. M. Khosru, Professor of the Department of Electrical and Electronic Engineering, BUET, for showing him the path and lineaments of solid state device and benign support during this research.

The author would also like to express his gratitude to Prof. Dr. Md. Saifur Rahman, Head of the Department of Electrical and Electronic Engineering, BUET, for rendering his support.

The author is grateful to all the members of the Board of Examiners for their valuable and fruitful suggestions.

The author is also thankful to all teachers, colleagues, and friends for providing encouragement to complete this research work.

Last but not the least, the author is indebted to all of his family members, specially his wife, for constant encouragement and mental support to complete this work.

Dhaka, Raisul Islam

Bangladesh

August 2011

Abstract

Recently reported technique to deposit a suitable gate oxide on InGaAs channel material has led the researchers to fabricate surface channel $In_xGa_{1-x}As$ MOSFETs with a thin channel layer on a metamorphically grown buffer layer. In this type of device, biaxial strain appears due to the mismatch in lattice parameter between channel layer and buffer layer. Also, $In_xGa_{1-x}As/InAs$ MOS HEMT has been successfully fabricated recently. No systematic study has been found regarding the effect of strain on device performance of these devices. In this thesis, using self-consistent simulation technique, a detailed study has been performed to observe the effect of strain on device performance in these types of devices. Both electrostatic and transport performance have been taken into consideration. Ballistic transport limit has been calculated using a 1-D model. This work has revealed some significant performance issues pertaining to strain in these devices. Also a new technique to extract threshold voltage in surface channel MOSFET has been proposed. In this technique, the peak of the ratio of first subband occupancy to the total inversion carrier concentration is identified. The gate voltage corresponding to the peak is extracted as the threshold voltage. It has been observed that the threshold voltage is significantly affected due to the change in strain. Also, the occupancy of the first subband does not remain constant throughout the gate bias. This suggests that for compact or analytical modeling of the device, contribution of the higher subbands should be taken into account. For MOS HEMT, it has been observed that delta doped barrier layer provides better device performance. The results presented in this thesis reveals some important issues pertaining to the future generation channel engineering in order to achieve high speed, low power device with alternate substrate material.

Chapter 1

Introduction

1.1 Preface

Due to aggressive scaling in traditional Si CMOS device, it will reach to its fundamental limit within the next decade [1]. Improving the "Short channel effects" and increasing the drive currents are the two notable impediments towards miniaturization in Si CMOS device. Search for alternative substrate material and/or innovative device structure as a viable replacement is the key challenge for the researchers over the past few years [2]. Among different innovative device structures, Si based multi-gate devices like double gate [3], tri-gate [4], gate-all-around (GAA) [5] transistors are fabricated and systematically studied. These novel transistors can effectively improve short channel effects but improvement in drive current is not possible with Si based material system due to its low mobility. For this reason, research in alternative semiconductor material has emerged with the potential of improving drive current by finding a suitable high mobility material system.

To this end, III-V material can be an attractive material which has 50-100$\times$ higher electron mobility than Si [6]. So devices fabricated with III-V material can provide higher drive current. Unfortunately, there are also some challenges in implementing III-V MOS device, of which finding a suitable high-k dielectric material as gate oxide is the

most challenging one. Enormous efforts have been made by the researchers in the past four decades to find suitable high-k gate dielectrics for III-V MOSFETs [7, 8]. Recently, InGaAs MOSFETs with Al_2O_3 as the high-k gate dielectric has been found to be a viable solution and high performance of this device has been reported [9]. These types of devices have thin surface channel layer over a buffer layer which is grown metamorphically on different substrate (InP, GaAs etc.). Indium content variation between channel layer and buffer layer results in lattice mismatch between these two layers. In this way strain is developed in the channel layer which affects the band offsets in the heterostructure and the effective mass of both electrons and holes [10]. Therefore, strain introduction in the channel layer of surface channel III-V MOSFETs brings variation in device performance (both electrostatic and ballistic transport). If the In percentage of the channel layer is higher than that of buffer layer, compressive strain is developed and this type of device has been successfully demonstrated in the previous report [11]. However, the channel can be tensile strained by varying the In percentage of the channel with respect to the buffer layer.

Although strained channel in these type of devices bring significant variation in device performance no systematic study has been done on the effect of channel strain in the electrostatic and transport properties of $In_xGa_{1-x}As$ channel device. Moreover, no report has been made regarding tensile strained device where the Indium mole fraction in channel layer is lower than that in the buffer layer. That is why a comparative study of device performance in order to find the effect of incorporating strain is significant. Also the systematic study of device performance variation with the variation in the amount and type of strain in the channel layer is of great importance to the research community. This study will reveal significant technological issue on future generation III-V MOSFETs and it will shed some light on future channel engineering for high speed, low power device design.

Beside the surface channel III-V MOSFETs, buried channel high electron mobility transistors (HEMT) have also got the focus of the research community over the last few decades [12]. This type of transistors have the advantage of avoiding carrier scattering due to the use of intrinsic material as the channel device. Both Schottky barrier gate

and oxide barrier gate has been reported for these devices [13, 14] fabricated with nitride materials. Since the growth of nitride material is difficult, recently some HEMTs are reported to be fabricated using InAs and/or GaAs material [15]. Among this, InAs MOS HEMT (known also as quantum-well-FET) is notable due to the fact that it has oxide gate which will reduce the gate leakage current [16]. Self-consistent analysis has yet to be done for this device to investigate the effect of material composition variation on device performance.

In this work, the effect of strain on surface channel InGaAs MOSFET has been studied using self-consistent numerical simulation technique. Both the electrostatic and transport properties have been taken into consideration while performance comparison is done. Ballistic transport performance has been considered which essentially represents the performance limit for a particular device. Also self-consistent analysis for InGaAs/InAs MOS HEMT has been done and the effect of Indium mole fraction variation in the barrier layer has been studied. Both delta doped and uniformly doped barrier layer has been taken into account for comparison.

From this work, one significant result has been found regarding the threshold voltage of surface channel MOSFET. It has been found that the ratio of the first subband charge concentration to the total charge concentration varies with gate voltage unlike the Si MOSFET which has this ratio constant throughout the gate bias. From this, a new extraction technique of threshold voltage has been proposed for this device. It has also been found that the impact of higher subband charge concentration on the total charge concentration is not constant throughout the gate bias which leads to the variation in threshold voltage, C-V and I-V characteristics with the variation in strain.

1.2 Literature Review

The advantage of III-V materials over Si has long been known to the researchers because it has electron mobility many times higher than its Si counterpart. Initially the device research with III-V material was centered around GaAs. The first GaAs MOS-

FET work was reported by Becke and White in 1965 [17]. This device was fabricated with deposited SiO_2 as the gate dielectric. Though it had large amount of interface traps, it operated successfully within a few hundred megahertz frequency range. But soon it is realized that SiO_2 is not a suitable gate dielectric for GaAs MOSFETs which started a long series of enormous research efforts in the last four decades.

Motivated by the success of thermally grown native SiO_2 on Si, using native oxide on GaAs was intensely studies at the very beginning. Among these research efforts thermal oxidation [18], dc and rf plasma oxidation [19] and vacuum ultraviolet photo-chemical oxidation [20] are noteworthy. Unfortunately none was proved to be viable for commercial GaAs MOSFET technology. One general observation is that the native oxide is not stable, mostly leaky with low dielectric breakdown strength, and cannot be forward biased beyond a few volts.

In 1980, Spicer *et al.* performed extensive experimentation on III-V metal-semiconductor (MS) and metal-oxide-semiconductor (MOS) structure and concluded that the Schottky-barrier formation on III-V semiconductors is due to defects formed near the interface by deposition of the metal or any chemisorption of oxygen [21]. This model also applies to the formation of states at III-V oxide interface. It is concluded that Fermi level position in GaAs is pinned at the midgap whether or not it is an MS or MOS interface.

Fermi-level pinning in III-V semiconductors discouraged the researchers to compete with Si in large-scale integrated circuits. However, the development of molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) in the late '70s made the heterojunctions, quantum wells and superlattices practical. Stromer *et al.* reported enhance mobility using a single AlGaAs/GaAs heterojunction, which led to the discovery of the fractional quantum hall effect in 1981 [22].

Mimura *et al.* reported high-electron-mobility-transistor (HEMT) in 1980 [23], which eventually made its way toward commercial application finding broad application in communication, military and aerospace industry today.

Passlack *et al.* reported that *in situ* deposition of $Ga_2O_3(Gd_2O_3)$ dielectric film on a GaAs surface produced MOS structures on GaAs with a low interface trap density

(D_{it}) [24, 25]. He again reported a series of work where the previous dielectric process has been modified using a Ga_2O_3 template in $Gd_xGa_{0.4-x}O_{0.6}/Ga_2O_3$ dielectric stacks on GaAs [26].

Rajagopalan *et al.* introduced an implant-free enhancement-mode device concept and demonstrated good device performance to eliminate the difficulty in realizing the inversion operation due to the relative low thermal budget of III-V and gate dielectric stacks [27]. Hale *et al.* reported that unpinning of Fermi level in GaAs MOSFET is due to Ga_2O restoring the surface As and Ga atoms to near bulk charge [28].

Ye *et al.* started working on atomic layer deposition (ALD) technique to deposit high-k dielectric Al_2O_3 and HfO_2 on GaAs and other III-V materials and reported depletion mode MOSFETs on GaAs, InGaAs and GaN using ALD Al_2O_3 as gate dielectric [29].

In 2008, Xuan *et al.* demonstrated inversion mode high performance InGaAs MOSFET with ALD Al_2O_3. A high drain current of 1 A/mm and a transconductance of 0.35 S/mm has been reported [9]. It has also been reported by Xuan *et al.* that In rich InGaAs is a potential channel material for this type of device due to its higher effective mobility and manageable band gap for low drain voltage [11]. Currently, many research groups are working on ALD IIIV MOSFETs [30].

Among these works, Shahrjerdi *et al.* studied the impact of two different chemical surface treatment methods on the C-V characteristics of GaAs MOS capacitors using NH_4OH and $(NH_4)_2S$ prior to atomic layer deposition (ALD) of Al_2O_3 [31]. They concluded that in both the cases high quality of ALD-Al_2O_3 is formed resulting it MOS capacitors exhibit a steep transition from accumulation to depletion as well as very low leakage current density. Formation of true inversion layer was confirmed using both chemical treatment protocols. However, it was found that sulfur-passivated GaAs demonstrates better frequency dispersion behavior and slightly smaller capacitance equivalent thickness than hydroxylated GaAs.

Besides InGaAs and GaAs based materials, numerous reports have been published on the experimental work using nitride materials. Hu *et al.* worked on AlGaN/GaN

HEMT with schottky barrier gate. In this work, reliability evaluation of Schottky contact was done. Upon applying two different frequency to similar HEMT structure, the schottky barrier height (SBH) and the ideality factor are investigated through I-V characteristics. It was found that both SBH and the ideality factor decreases after the same time [13].

However, Schottky barrier HEMT suffers serious problem of high leakage current due to the absence of any oxide layer between semiconductor and metal gate. Kim *et al.* fabricated 30 nm $In_{0.7}Ga_{0.3}As$ HEMT with excellent logic performance, scalability and high frequency performance. The most significant results of this work is that the removal of dopants from the barrier suppresses forward gate leakage current by few orders of magnitude when compared with equivalent normal HEMTs [15].

Pozzovivo *et al.* showed that in InAlN/GaN MOS HEMT the gate leakage current is reduced by six to ten orders of magnitude compared to schottky barrier HEMT of similar design. With analytical modeling, the higher mobility of the electrons in the channel of MOS HEMT was also reported [14].

Huang *et al.* successfully fabricated AlGaN/GaN MOS HEMT with a direct growth of oxide layer on AlGaN surface using photochemical oxidation method [32]. Radosavljevic *et al.* fabricated quantum well FET (QWFET) or InGaAs MOS HEMT using the advanced composite high-k gate stack on Si substrate [33]. It has been reported that composite high-k gate stack enables both low gate leakage and high effective carrier velocity in the QW channel.

Muligate structure with III-V materials has also been reported recently. Wu *et al.* has successfully demonstrated the first well-behaved inversion-mode InGaAs FinFET with gate length down to 100 nm with ALD Al_2O_3 as gate dielectric [34]. It has been showed that the short channel effect has been improved for III-V device with three dimensional device design.

Besides experimental works, some simulation based study was also done on III-V MOSFETs and HEMTs. Kalna *et al.* investigated the performance potential of n-type implant free $In_{0.25}Ga_{0.75}As$ MOSFETs with high-k dielectrics using Monte Carlo simu-

lation technique. In this work, excellent scaling potential of the implant free MOSFET concept was demonstrated [35].

Steighner *et al.* showed a new approach of laterally-diffused-metal oxide semiconductor (LDMOS) with $In_{0.53}Ga_{0.47}As$. Using 2-D device simulation, comparisons between $In_{0.53}Ga_{0.47}As$ and Si LDMOS are made, demonstrating the advantages of $In_{0.53}Ga_{0.47}As$ LDMOS [36].

Kharche *et al.* studied the scaling behavior of ultra-scaled InAs HEMTs using a 2-dimensional real-space effective mass ballistic quantum transport simulator [37]. After being benchmarked with experimental results, this simulator was used to optimize the logic performance of the not-yet-fabricated 20 nm InAs HEMT. It has been demonstrated that the best performance is achieved in thin InAs channel devices by reducing the insulator thickness to improve the gate control while increasing the gate work function to suppress the gate leakage.

Kao *et al.* has demonstrated the effects of interface trap states on the sub-threshold characteristics of InGaAs based MOSFETs, MOS HEMTs and tunnel FETs [16]. It has been reported that based on the Fermi-level position and the density of interface trap states (D_{it}), the sub-threshold response for these three devices may vary, with tunnel FETs having the least sub-threshold degradation due to (D_{it}).

Since the interface trap states is an important issue in the design and performance of III-V MOSFETs, efficient algorithm has also been reported. Satter *et al.* reported an accurate algorithm to extract D_{it} from the experimental C-V characteristics using self-consistent simulation technique [38].

However, the effect of strain on InGaAs MOSFETs and MOS HEMTs has yet to be reported in the literature.

1.3 Objective of This Work

The objective of this work is,

- To provide a comparative analysis of electrostatic and ballistic transport properties of InGaAs surface channel MOSFETs with respect to the strain variation (both tensile and compressive) in the channel.
- To study the electrostatic and ballistic transport properties of InAs MOS HEMT with high-k gate dielectric.

In this thesis, the performance comparison will be done using 1-D self-consistent simulation technique taking energy quantization and wave function penetration into gate dielectric into account. The Poisson's equation will be solved using Finite Difference Method and the Schrödinger's equation will be solved using the Hamiltonian Matrix formalism [39]. From the electrostatic solution capacitance-voltage (C-V) characteristics and charge carrier profile will be studied. However, to study the ballistic transport properties, electrostatic solution will be utilized to determine the ballistic current of the device using 'top-of-the-barrier' model [40, 41]. In this model, self-consistently obtained eigen states and charge concentrations are used to calculate Fermi level under drain and source bias, which is used in calculating drain to source current. For different device structure the modification of the equations will be done using appropriate boundary conditions. Strained channel will have different material parameters than that of the unstrained one. This strain effect will be incorporated in the simulation by proper calculation of the material parameters having strain under consideration.

1.4 Organization of the Thesis

Required numerical model and formulation for strain effect incorporation is discussed in chapter 2. In chapter 3, the detailed results of InGaAs MOSFETs are discussed. In chapter 4, the detailed results of InGaAs/InAs MOS HEMT are discussed. Finally, the conclusions were made in chapter 5 and suggestions for future work have been provided.

Chapter 2

Model and Formulation

This chapter describes the structure of the device considered in this work. The basic self-consistent solver model and formulation is presented. Detailed description of how the strain effect considered is also discussed in this chapter. Finally, which of the material parameters are affected by incorporating strain has been presented.

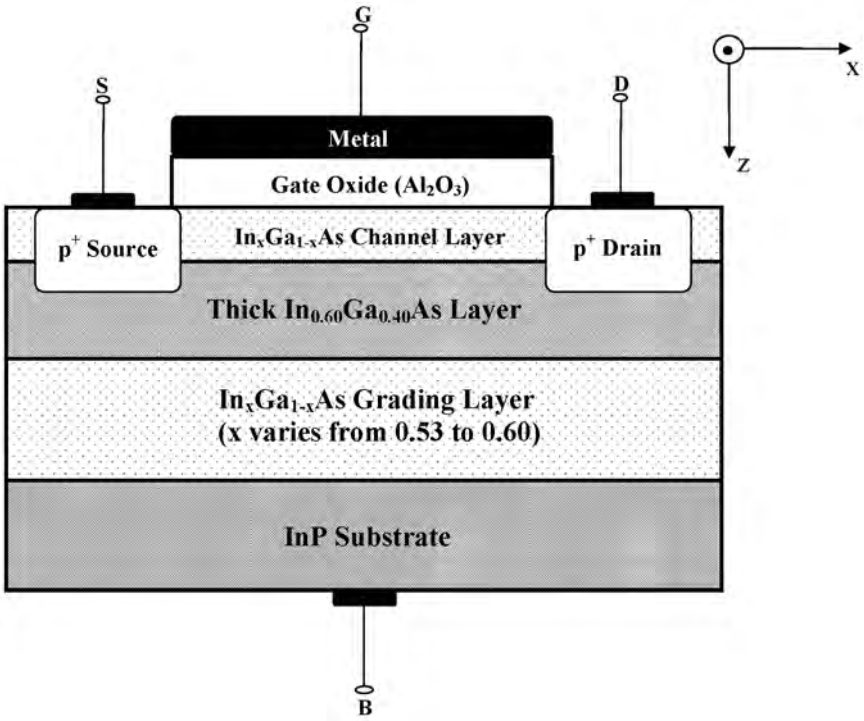

Figure 2.1: The basic MOSFET structure considered in this work.

2.1 The Basic Device Structure

Fig. 2.1 shows an n-channel enhancement-type MOSFET with $In_xGa_{1-x}As$ as the channel material. This device is fabricated on p^+ InP substrate. $In_{0.53}Ga_{0.47}As$ is lattice matched with the InP substrate. That is why a metamorphic layer is grown on the substrate where the In fraction is varied gradually from 0.53 to 0.60. This layer is 500 nm and thick enough to accommodate all the traps and defects from lattice mismatch. Metamorphically grown layers are epitaxial layers with graded mole fraction of constituting materials reported previously in [42] which allows to grow a layer lattice mismatched with commonly used substrate. After the metamorphically grown grading layer, a thick buffer layer of $In_{0.60}Ga_{0.40}As$ is epitaxially grown which is now lattice-matched with the interface of the metamorphic layer. Finally, the channel layer of 20 nm thickness is grown on the $In_{0.60}Ga_{0.40}As$ buffer layer. If the Indium mole fraction in the channel layer is not matched with that of the buffer layer below, strain will be developed. Depending on whether the lattice constant of the channel layer is higher or lower than that of the buffer layer tensile or compressive strain will be developed. If the Indium mole fraction is the same as the buffer layer, no strain will be developed and the MOSFET will act as a generic III-V MOSFET. Above the channel layer, gate oxide is deposited. For $In_xGa_{1-x}As$, Al_2O_3 is found to be a suitable gate oxide material in recent studies and high performance MOS devices are reported having Atomic Layer Deposited (ALD) Al_2O_3 as gate oxide [9]. Finally, Ni/Au metal is considered as the gate metal.

In this work, five different Indium mole fractions are being considered, i.e. 0.30, 0.53, 0.60, 0.65, and 0.75. Among these five different channels materials, two represent compressively strained channel, two represent tensile strained channel and one represents no strain. The doping density of the channel is also varied and three doping densities are considered, i.e. 1×10^{17}, 5×10^{17}, and 1×10^{18} cm^{-3}. The other device parameters are kept constant. All the device parameters considered in the work are summarized in the table 2.1.

In this work,the self-consistent simulation technique is used to obtain electrostatic prop-

Table 2.1: Parameters' list considered in this work

Parameter Name	**Values Considered**
Channel thickness	20 nm
Oxide thickness	10 nm
Channel doping density	1×10^{17}, 5×10^{17}, and 1×10^{18} cm^{-3}
Buffer doping density	Same as channel
Channel layer In mole fraction	0.30, 0.53, 0.60, 0.65, 0.75
Buffer layer In mole fraction	0.60

erties of III-V MOSFET. Using the coupled solution of 1-D Schrödinger and Poisson equation in the gate to substrate direction, C-V characterization is obtained. From the results obtained by the self-consistent simulation, using the "top of the barrier approach" proposed by Assad *et al.*, transport characterization is done where the ballistic current limit is calculated [41]. In Fig. 2.1, the gate to substrate direction is denoted by the z-direction, and the source to drain direction is denoted by the x-direction. In the self consistent simulation strain effect in the channel layer is incorporated by properly calculating the material parameters affected by strain using the equations described in [10].

2.2 Self-consistent Simulation

The self-consistent simulation is the technique of device simulation where the Schrödinger and Poisson equation is solved using the appropriate device structure and boundary conditions. In this work, a self-consistent Schrödinger-Poisson solver is developed to compare the effect of different types and amount of strain on the channel material. So the formulation of the solver consists of two parts, one is to develop the basic solver and the other is to incorporate strain effect into it.

2.2.1 Basic Model

Schrödinger solver

Stern [43] and Moglestue [44] described a self-consistent solution approach for the first time. Stern, however made a basic assumption that effective mass approximation is valid and that is why periodic potential need not be taken into account. By the effective mass approximation, 1-D Schrödinger's equation can be formulated as,

$$\left[-\frac{1}{2}\hbar^2\nabla m^{*-1}\nabla + eV(z) + \Delta E_{c,v}(z)\right]\psi_{0_{ij}} = E_{ij}^{'}\psi_{0_{ij}} \tag{2.1}$$

Here m^* is the effective mass tensor, $V(z)$ is the electrostatic potential, e is the electronic charge, and $E_{ij}^{'}$ is the energy. $\Delta E_{c,v}(z)$ is the energy band offset (c denotes conduction band and v denotes valence band) which is also a function of z because it is different in different layers of the device. Stern showed that the electronic wavefunction $\psi_{0_{ij}}$ for the jth subband in the ith valley can be expressed in terms of Bloch function travelling parallel to the interface, constrained by an envelope function normal to it. This can be represented as,

$$\psi_{0_{ij}}(x, y, z) = \psi_{ij}(z)e^{i\theta z}e^{ik_x x + ik_y y} \tag{2.2}$$

Where, $k_x$and k_y representsthe component of the wave vector k in x and y direction. $\psi_{ij}(z)$can be calculated by the solving the equation as,

$$\left[-\frac{\hbar^2}{2m_{zi}}\frac{d^2}{dz^2} + eV(z) + \Delta E_{c,v}(z)\right]\psi_{ij}(z) = E_{ij}\psi_{ij}(z) \tag{2.3}$$

Where, $m_{zi}$is the quantization effective mass and E_{ij} is the eigenenergy of the jth subband in the ith valley in the z direction.

Eq. (2.3) is solved using two boundary conditions as,

1. $\psi_{ij}(\infty) = 0$ deep inside the semiconductor

2. $\psi_{ij}(-t_{ox}) = 0$ at the metal oxide interface (taking t_{ox} as the oxide layer thickness and oxide-semiconductor interface as the origin)

Each eigenvalue E_{ij} found from the solution of Eq. (2.3) is the bottom of a subband, with energy levels given by,

$$E_{ij}^{'} = E_{ij} + \frac{\hbar^2 k_x^2}{2m_x} + \frac{\hbar^2 k_y^2}{2m_y} \tag{2.4}$$

Here, m_x and m_y are the effective masses in the transport plane. The conduction band of $In_xGa_{1-x}As$ has one spherical valley along any direction, since it is a direct bandgap material. As a result there is only one m_z. So Eq. (2.3) is solved numerically in order to find the eigenenergy and the envelop function. In this work, Hamiltonian Matrix formalism [39] is used to solve the Schrödinger's equation numerically.

Poisson Solver

Poisson solver is needed to obtain the potential profile$V(z)$. This is the starting phase of the self-consistent solver. In this work, Poisson equation is solved in finite difference method. The 1-D Poisson equation applicable for the MOSFET is formulated as,

$$\frac{d^2V}{dz^2} = -\frac{[\rho_{depl}(z) + \rho_{inv}(z)]}{\varepsilon_{semi}\varepsilon_0}, \quad for \quad z > 0 \tag{2.5}$$

$$\frac{d^2V}{dz^2} = -\frac{[\rho_{inv}(z)]}{\varepsilon_{ox}\varepsilon_0}, \quad for \quad z \leq 0 \tag{2.6}$$

Here, ε_{semi} is the dielectric constant of semiconductor, ε_{ox} is the dielectric constant of the oxide, $\rho_{depl}(z)$ is the depletion charge and $\rho_{inv}(z)$ is the inversion charge distribution along z direction. Inversion charge is calculated with taking wave function penetration effect in account. Once proper charge distributions are known accurate determination of the potential profile is done. $\rho_{inv}(z)$ is calculated from eigenenergies

and wavefunction values obtained by solving Schrödinger's equation. $\rho_{inv}(z)$ is given by,

$$\rho_{inv}(z) = \sum_{ij} N_{ij} \left|\psi_{ij}(z)\right|^2 \tag{2.7}$$

Here N_{ij} is the sheet carrier concentration in the semiconductor channel which is given by,

$$N_{ij} = \frac{n_{vi} m_{di} kT}{\pi\hbar^2} \ln\left[1 + e^{\frac{E_F - E_{ij}}{kT}}\right] \tag{2.8}$$

Here, n_{vi} is the valley degeneracy which for $In_xGa_{1-x}As$ is 1 and m_{di} is the density of states effective mass of the ith valley as shown in the previous section in this chapter. E_F is the Fermi level.

Depletion charge density $\rho_{depl}(z)$ is given by,

$$\rho_{depl}(z) = \begin{cases} -e(N_A - N_D), & 0 < z < z_d \\ 0, & z > z_d \end{cases} \tag{2.9}$$

Here, z_d is the depletion layer thickness which is determined by an adaptive algorithm. In this algorithm, z_d is estimated first from very small value to a gradual increase and in each case *V(z)* is calculated from Poisson's equation. Each time it is checked, whether after the estimated z_d, *V(z)* is horizontal or not. If it is horizontal then the corresponding z_d is considered to be the appropriate z_d for that specific gate bias.

In order to solve the Poisson's Equation, appropriate boundary conditions are used. These are,

1. $V(z_d) = 0$

2. $V(-t_{ox}) = V_g$, at the metal-oxide interface. Here, V_g acts as the applied gate voltage.

3. At the oxide-semiconductor interface, $F_s = F_{ox}$, where,

$$F_s = \frac{e(N_{inv} + N_{depl})}{\varepsilon_{semi}\varepsilon_0},\ F_{ox} = \frac{e(N_{inv} + N_{depl})}{\varepsilon_{ox}\varepsilon_0} \tag{2.10}$$

are the surface electric fields and,

$$N_{depl} = z_d(N_A - N_D) \tag{2.11}$$

is the number of charge per unit area in the depletion layer.

If accumulation region of operation is considered, depletion layer thickness need not be calculated and inversion charge distribution $\rho_{inv}(z)$ is to be replaced by bound accumulation charge distribution$\rho_{acc}(z)$. However $\rho_{acc}(z)$ is calculated using the previously mentioned Eq. (2.7) and (2.8). In place of depletion charge distribution $\rho_{depl}(z)$extended state charge distribution $\rho_{ext}(z)$ is to be used which is calculated in semi-classical approach [45].

2.2.2 Coupling Schrödinger and Poisson's Equation

Self-consistent simulation is done for each gate bias for a MOS device. Here gate bias acts as the input. First for a particular gate bias Poisson's equation is solved by finite difference method. According to finite difference method,

$$\frac{d^2V}{dz^2} = \frac{V_{n+2} - 2V_{n+1} + V_n}{\Delta z^2} = -\frac{\rho_n}{\varepsilon} \tag{2.12}$$

Here, *n+2*, *n+1* and *n* are different grid space points. ρ_n is the value of total charge in space point *n* and ε is the dielectric constant for the corresponding point- oxide or semiconductor. Δz is the grid spacing. Solving the Poisson's equation, voltage profile for a particular gate bias is gained. This voltage profile given input to the Schrödinger's

equation facilitates the solution resulting in eigen states and wavefunctions. From these, charge profile ρ_{inv} is estimated. Taking the full charge profile, (ρ_{inv},ρ_{depl}) Poisson's equation is solved again. A new potential profile is generated by taking 96% of the older profile and 4% of the newer profile. The whole calculation described above is done repetitively. This procedure is repeated until error between two successive profile is less than 0.01%. For higher gate voltages starting potential profile for the calculation is taken as the last converged profile of previous gate voltage.

2.2.3 The Incorporation of the Strain Effect

Basic Model

Strain deforms the crystal lattice. It arises when two layers of semiconductor material have different lattice constant. The relative change of lattice constant is measured as the amount of strain,

$$\varepsilon_{ij} = \frac{\Delta a_i}{a_j} \tag{2.13}$$

Which may be different in each direction (*a*, lattice constant; *i, j = x, y* or *z axis*). The fractional change in volume due to strain is given by

$$\frac{\Delta V}{V} = \varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz} \tag{2.14}$$

In our work we consider the common case of biaxial strain due to lattice mismatch in superlattices grown in the z direction with ε_{xx}=ε_{yy}≠ε_{zz} and ε_{ij}= 0 for $i \neq j$. The two strain components are related by the elastic stiffness constant C_{11} and C_{12} as [10],

$$\varepsilon_{zz} = -2\frac{C_{12}}{C_{11}}\varepsilon_{xx} \quad with \quad \varepsilon_{xx} = \varepsilon_{yy} = \frac{a_{st} - a_0}{a_0} \tag{2.15}$$

where a_{st} and a_0 are the lattice constant of the strained and unstrained crystal, respectively. Whether $\varepsilon_{xx}$and ε_{yy} are positive or negative determines whether the crystal will be compressive or tensile strained as follows,

1. **For compressive strain,** $a_{st} < a_0,\ \varepsilon_{xx} = \varepsilon_{yy} < 0,\ and\ \varepsilon_{zz} > 0$

2. **For tensile strain ,** $a_{st} > a_0,\ \varepsilon_{xx} = \varepsilon_{yy} > 0,\ and\ \varepsilon_{zz} < 0$

3. **For no strain,** $a_{st} = a_0,\ \varepsilon_{xx} = \varepsilon_{yy} = 0,\ and\ \varepsilon_{zz} = 0$

The strain primarily affects band structure and effective mass [10]. From the two-band k.p model calculation done in [10], the conduction band edge and the heavy hole and the light hole valence band edge at the Γ point with the strain effect taking into account is given by,

$$E_c(0) = E_c^0 = E_v^0 + E_g + a_c(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \tag{2.16}$$

$$E_{hh}(0) = E_{hh}^0 = E_v^0 - P_\varepsilon - Q_\varepsilon \tag{2.17}$$

$$E_{lh}(0) = E_{lh}^0 = E_v^0 - P_\varepsilon + Q_\varepsilon \tag{2.18}$$

where,

$$P_\varepsilon = -a_v(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \tag{2.19}$$

$$Q_\varepsilon = -\frac{b}{2}(\varepsilon_{xx} + \varepsilon_{yy} - 2\varepsilon_{zz}) \tag{2.20}$$

and the factors $a_c$and $a_v$are called hydrostatic deformation potentials; b is the shear deformation potential. The interesting thing to be noted here is that strain does not allow degeneracy in the band structure in heavy hole and light hole band at the Γ point.

However, in the previous discussion, the results for heavy hole and light hole band neglects their interaction with the spin orbit band. This interaction results into the formation of split-off (SO) hole band having a split-off energy Δ_0 which is the energy difference between the heavy/light- hole band with the split-off hole band at Γ point. Using the three band k.p model, including the spin-orbit interaction, the band edges at the Γ point for heavy hole, light hole and split-off (SO) hole band is given by,

$$E_{hh}^0 = E_v^0 - P_\varepsilon - Q_\varepsilon \tag{2.21}$$

$$E_{lh}^{0} = E_{v}^{0} - P_{\varepsilon} + \frac{1}{2}\left[Q_{\varepsilon} - \Delta_0 + \sqrt{\Delta_0^2 + 9Q_{\varepsilon}^2 + 2Q_{\varepsilon}\Delta_0}\right] \tag{2.22}$$

$$E_{so}^{0} = E_{v}^{0} - P_{\varepsilon} + \frac{1}{2}\left[Q_{\varepsilon} - \Delta_0 - \sqrt{\Delta_0^2 + 9Q_{\varepsilon}^2 + 2Q_{\varepsilon}\Delta_0}\right] \tag{2.23}$$

From these equations, it is observed that the expression for the light hole band is somewhat different from the previous result in Eq. (2.18) due to the interaction with the SO band. The conduction band edge is still given by the Eq. (2.16). Analytical formulas for the detailed band structure $E\left(\overrightarrow{k}\right)$ are discussed in detail in [46].

Effective mass of heavy hole, light hole and split off hole is also affected by the strain. From the detailed band structure (E-k diagram) the effective masses are calculated. Since there are three components of the wave vector in three directions (k_x,$k_y$and k_z), we consider the quantization effective mass in the k_z direction (denoted by superscript z) and the in-plane effective mass within the k_x– k_y plane (denoted by superscript t). From the series expansion of E up to the second order of k near the Γpoint, the effective masses for $\overrightarrow{k} = 0$ can be extracted as,

$$m_{hh}^{z} = \frac{m_0}{\gamma_1 - 2\gamma_2} \tag{2.24}$$

$$m_{hh}^{t} = \frac{m_0}{\gamma_1 + \gamma_2} \tag{2.25}$$

$$m_{lh}^{z} = \frac{m_0}{\gamma_1 + 2\gamma_2 f_{+}} \tag{2.26}$$

$$m_{lh}^{t} = \frac{m_0}{\gamma_1 - \gamma_2 f_{+}} \tag{2.27}$$

$$m_{so}^{z} = \frac{m_0}{\gamma_1 + 2\gamma_2 f_{-}} \tag{2.28}$$

$$m_{so}^{t} = \frac{m_0}{\gamma_1 - \gamma_2 f_{-}} \tag{2.29}$$

employing the strain factor,

$$f_{\pm}(s) = \frac{2s\left[1 + 1.5\left(s - 1 \pm \sqrt{1 + 2s + 9s^2}\right)\right] + 6s^2}{0.75\left(s - 1 \pm \sqrt{1 + 2s + 9s^2}\right)^2 + s - 1 \pm \sqrt{1 + 2s + 9s^2} - 3s^2} \tag{2.30}$$

with the strain parameter $s = Q_{\varepsilon}/\Delta_0$. Without strain, $s = 0$ and $f_{\pm}(0) = 1$. Here, γ_1 and γ_2 are the Luttinger parameters.

Table 2.2: Percentage strain for different In mole fraction

Channel Material	Buffer Material	Channel Lattice Constant, a_0(nm)	Buffer Lattice Constant, a_{st}(nm)	% Strain*
$In_{0.30}Ga_{0.70}As$	$In_{0.60}Ga_{0.40}As$	5.7750	5.8964	2.10 (T)
$In_{0.53}Ga_{0.47}As$		5.8681		0.48 (T)
$In_{0.60}Ga_{0.40}As$		5.8964		0.00 (N)
$In_{0.65}Ga_{0.35}As$		5.9166		0.34 (C)
$In_{0.75}Ga_{0.25}As$		5.9571		1.02 (C)

*Here, T = Tensile Strain, C = Compressive Strain, N = No Strain

In this work, conduction band and valence bands are treated separately, so the interaction of the conduction band with valence band is neglected and effective mass for electron is not affected by strain.

Change in Parameters due to Strain

In this work, five different Indium mole fractions (0.30, 0.53, 0.60, 0.65, and 0.75) for the channel material are considered and $In_{0.60}Ga_{0.40}As$ is used as the buffer layer.

In the table 2.2, the percentage strain along with the lattice parameters are given for each Indium mole fraction. This strain has an effect on the hole effective mass, the conduction band and the valence band offset.

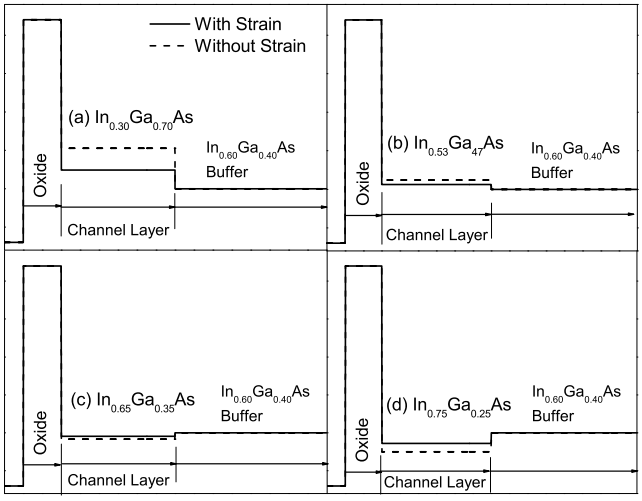

Figure 2.2: Comparison of conduction band edges for different channel considering strain and without strain.

Table 2.3: Comparison of hole effective mass (quantization) with respect to strain

Hole Type	Channel Material	% Strain†	m_{eff} strained* (a)	m_{eff} no strain* (b)	% Change $\frac{(b)-(a)}{(b)} \times 100$
m^z_{hh}	$In_{0.30}Ga_{0.70}As$	2.10 (T)	0.3446	0.3446	0
m^z_{lh}			0.0419	0.0530	20.9434
m^z_{so}			0.1702	0.0530	-221.132
m^z_{hh}	$In_{0.53}Ga_{0.47}As$	0.48 (T)	0.3408	0.3408	0
m^z_{lh}			0.0370	0.0403	8.1886
m^z_{so}			0.0857	0.0403	-112.655
m^z_{hh}	$In_{0.60}Ga_{0.40}As$	0.00 (N)	0.3397	0.3397	0
m^z_{lh}			0.0375	0.0375	0
m^z_{so}			0.0375	0.0375	0
m^z_{hh}	$In_{0.65}Ga_{0.35}As$	0.34 (C)	0.3389	0.3389	0
m^z_{lh}			0.0386	0.0358	-7.8212
m^z_{so}			0.0573	0.0358	-60.0559
m^z_{hh}	$In_{0.75}Ga_{0.25}As$	1.02 (C)	0.3373	0.3373	0
m^z_{lh}			0.0421	0.0328	-28.3537
m^z_{so}			0.0425	0.0328	-29.5732

†Here, T = Tensile Strain, C = Compressive Strain, N = No Strain

*The values are normalized by free electron mass

Table 2.4: Comparison of hole effective mass (in-plane) with respect to strain

Hole Type	Channel Material	% Strain†	m_{eff} strained* (a)	m_{eff} no strain* (b)	% Change $\frac{(b)-(a)}{(b)} \times 100$
m^t_{hh}	$In_{0.30}Ga_{0.70}As$	2.10 (T)	0.0672	0.0672	0
m^t_{lh}			0.2278	0.1451	-56.9952
m^t_{so}			0.0747	0.1451	48.5183
m^t_{hh}	$In_{0.53}Ga_{0.47}As$	0.48 (T)	0.0517	0.0517	0
m^t_{lh}			0.1370	0.1189	-15.2229
m^t_{so}			0.0667	0.1189	43.9024
m^t_{hh}	$In_{0.60}Ga_{0.40}As$	0.00 (N)	0.0483	0.0483	0
m^t_{lh}			0.1128	0.1128	0
m^t_{so}			0.1128	0.1128	0
m^t_{hh}	$In_{0.65}Ga_{0.35}As$	0.34 (C)	0.0461	0.0461	0
m^t_{lh}			0.0980	0.1087	9.8436
m^t_{so}			0.0692	0.1087	36.3386
m^t_{hh}	$In_{0.75}Ga_{0.25}As$	1.02 (C)	0.0423	0.0423	0
m^t_{lh}			0.0754	0.1015	25.7143
m^t_{so}			0.0749	0.1015	26.2069

†Here, T = Tensile Strain, C = Compressive Strain, N = No Strain

*The values are normalized by free electron mass

In the table 2.3, the comparative picture of the quantization effective mass in three types of holes due to strain is given and in the table 2.4 the comparative picture of the in-plane effective mass in three types of holes due to strain is given. From both of the table, it can be observed that heavy hole mass is not affected by strain. However, the light hole and split-off hole effective masses change significantly due to strain and the change in effective mass increases with the increase of the amount of strain either-compressive or tensile. The interesting point to note here is that for same strain value split-off hole effective mass is changed more than that of light hole band. All this change can affect the eigen state of the bound charge and the occupation in these subbands. Hence, the C-V and the I-V characteristics should have significant effect of strain.

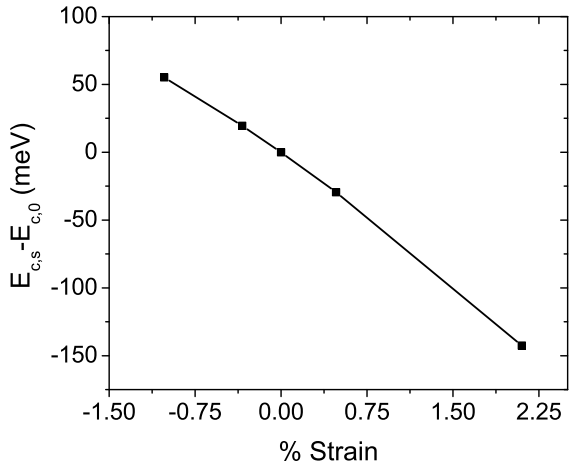

Figure 2.3: The difference in conduction band edge of the channel layer with and without strain.

Besides the effective mass point of view, the effect of strain on device performance can also be investigated in the perspective of band offset. In the Fig. 2.2, the conduction band edges are illustrated for four different channel materials. In this figure, both band edges taking strain effect into consideration and without strain effect is presented. From this figure, it is observed that in both the cases of tensile and compressive strain, it reduces the band offset between channel and the buffer layer. However, for the tensile strained channel material, the band edge of the channel is higher than that of the buffer. In this case strain reduces this offset. In case of compressive strained channel material, the band edge of the channel is lower than that of the buffer. In this case also

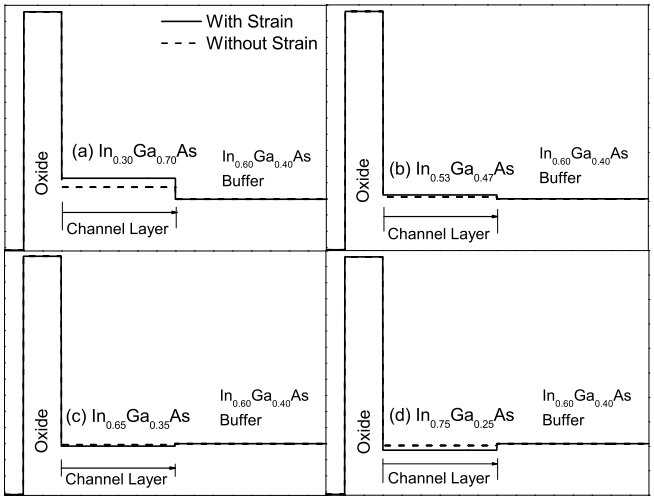

Figure 2.4: Comparison of heavy hole band edges for different channel considering strain and without strain.

the strain reduces this offset, but for compressive strained material, the reduction in the band offset minimizes the depth of the quantum well formed by the inherent band offset in the superlattice structure.

If we denote the conduction band edge in the channel material with strain effect incorporated as $E_{c,s}$ and that without strain as $E_{c,0}$, then $E_{c,s}$ - $E_{c,0}$ denotes the change is conduction band edge due to strain. Fig. 2.3 illustrates this quantity as a function of strain. From this figure, it is observed that the change in conduction band edge changes almost linearly with the amount of strain. In this figure, negative strain means compressive and positive strain means tensile strain. For around 1% of compressive strain, the conduction band edge increases up to 50 meV and for around 2% of tensile strain the conduction band edge decreases up to 150 meV. From this result, it can be inferred that tensile strain has more influence on the conduction band edge compared to the compressive strain.

In case of valence band edge, there are three bands all of which are influenced by the strain. Fig. 2.4, 2.5 and 2.4 represents the heavy hole (HH), light hole (LH) and split-off (SO) hole band respectively for different channel materials. From these figures, it is understood that strain affects these three bands differently. This difference is more clearly observed in the Fig. 2.7. In this figure, the difference in valence band edge

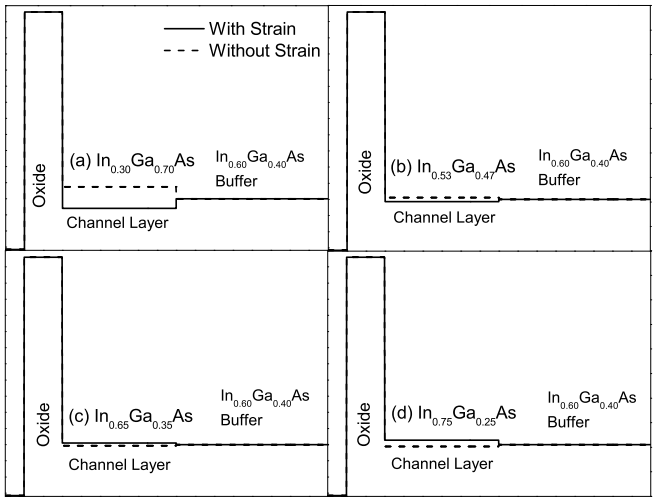

Figure 2.5: Comparison of light hole band edges for different channel considering strain and without strain.

is plotted against the amount of strain for three types of valence bands. From this figure it is observed that HH band edge difference changes linearly with strain, LH band edge difference is slightly linear and SO band edge difference is parabolic. The interesting thing to note here is that with increasing amount of strain (both compressive and tensile) the difference of band edge varies widely among HH, LH and SO band. Also, the trend in the band edge difference is opposite for HH and LH band. However, SO band edge difference is quite small compared to the other two types of holes.

2.3 Model Validation

In order to validate the proposed model, we have benchmarked it with experimental results. In [47], experimental measurement of C-V characteristics is presented for the same device structure discussed here. However, $In_{0.65}Ga_{0.35}As$ is used as the channel material and $In_{0.53}Ga_{0.47}As$ is used as the buffer layer which is lattice matched with InP substrate. In the reported device density of interface trap states (D_{it}) affects the device performance but in our work we have assumed ideal oxide-semiconductor interface with no D_{it}. So, in order to benchmark our model with the reported experimental result, the effect of D_{it} needs to be incorporated. From the algorithm shown

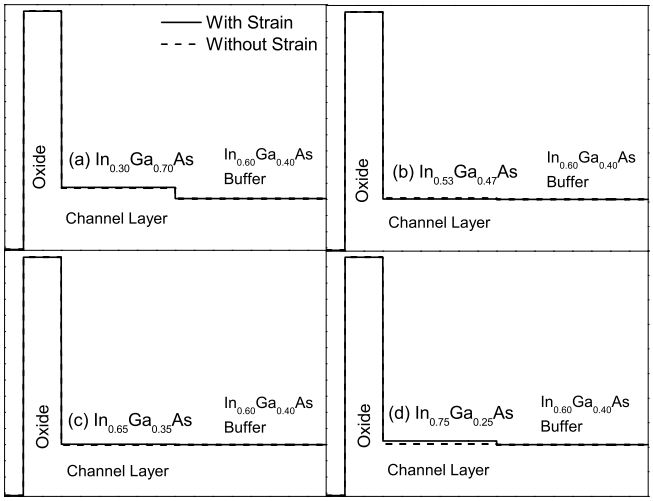

Figure 2.6: Comparison of split-off hole band edges for different channel considering strain and without strain.

in [48], using the D_{it} profile reported in [38], we have simulated the C-V characteristics of the reported device using our model described earlier in this chapter taking the strain effect into account. The simulated result along with the experimental result is presented in Fig. 2.8. From this figure, it is observed that the simulated result is in acceptable agreement with the experimental result. This result essentially justifies our proposed self-consistent simulation model along with the model to incorporate the strain effect.

In the next chapter, the effect of these changes in band edge and effective mass due to strain will be discussed in terms of the electrostatic and transport behavior of the device.

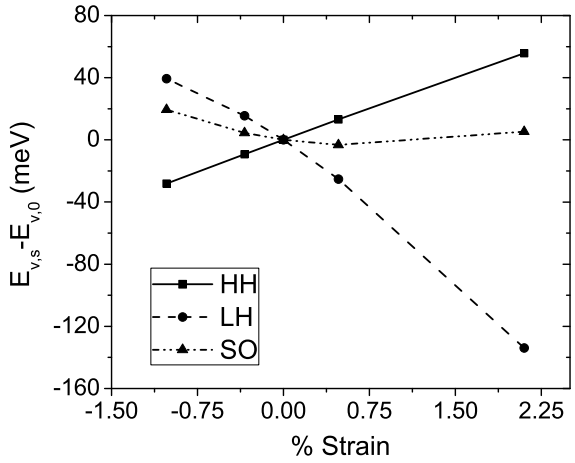

Figure 2.7: The difference in valence band edge of the channel layer with and without strain.

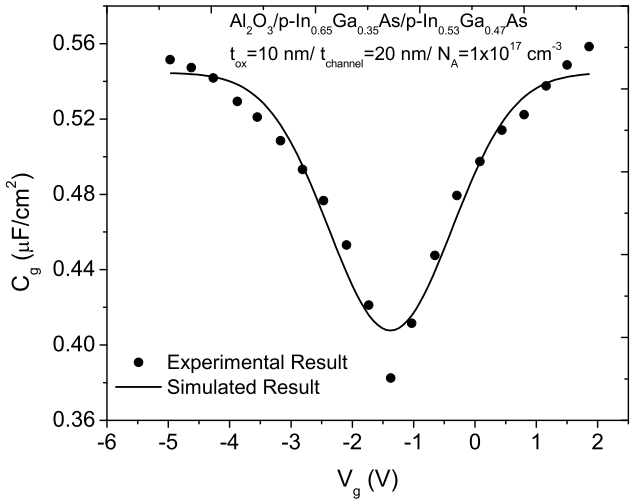

Figure 2.8: The gate capacitance as a function of gate voltage comparing the simulated and the experimental result.

Chapter 3

Results and Discussions - MOSFET

In this chapter, the effect of strain on device performance will be presented. Also, the comparison of device performance with and without strain will be done. Both electrostatic and ballistic transport properties will be included in the discussion.

3.1 Electrostatic Performance

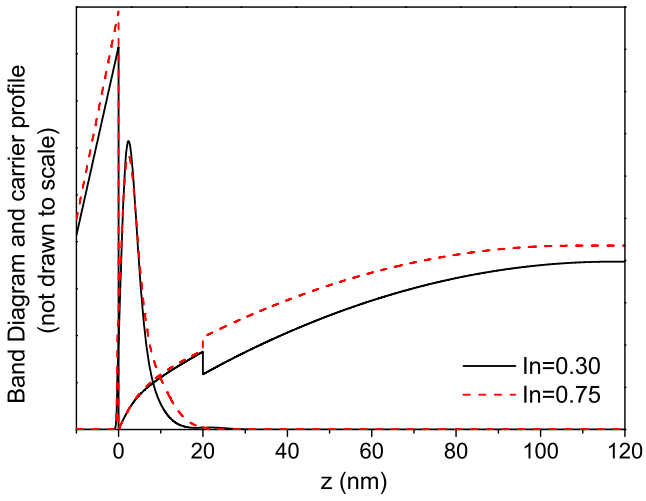

Figure 3.1: Energy band diagram along with carrier profile for both tensile strained (In=0.30) and compressive strained device (In=0.75).

Before going into the details of the electrostatic properties of the device the generic energy band diagram and carrier profile should be understood. In Fig. 3.1, the energy band diagram along with the inversion carrier profile is given. It has been observed that the band offset is different for tensile and compressive strained device. Also, the carrier profile remains inside the channel layer. From this figure the position and shape of the quantum well and the associated inversion carrier profile upon gate bias is clearly understood. Also the difference in band diagram due to strain can be perceived.

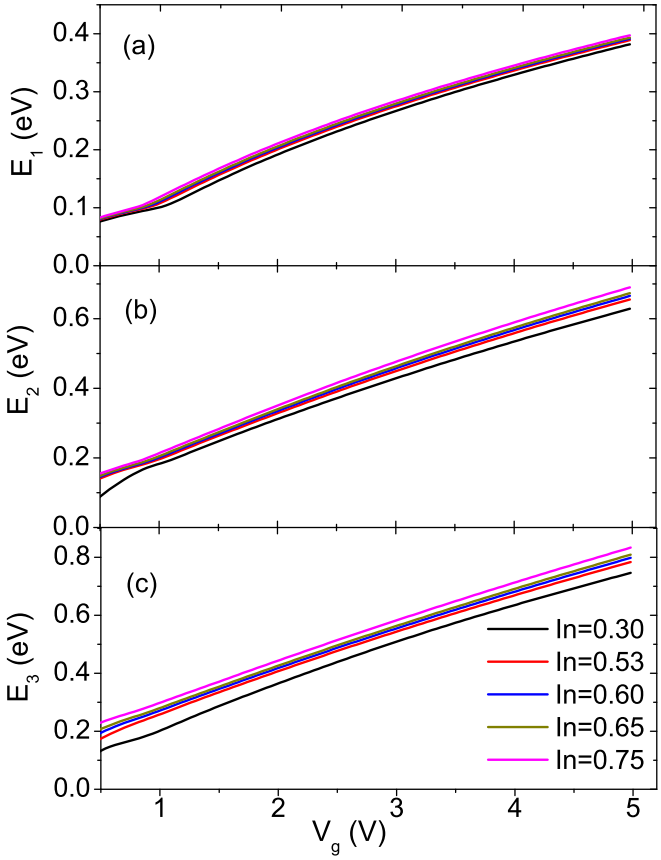

Figure 3.2: (a) First Eigen state (b) Second Eigen state (c) Third Eigen state as a function of gate voltage for different channel materials with $N_A = 1\times10^{17}$ cm^{-3}.

3.1.1 Eigen Energy

Eigen state denotes the subband minima for different subbands in the quantum well of the device formed due to the applied gate voltage. Bound state charge depends

on the eigen state of the device. Fig. 3.2, 3.3 and 3.4 presents the first three electron eigen states of the device as a function of gate voltage for different channel materials for three different doping density. From these figures it is observed that first eigen state does not vary significantly with the amount and type of strain. However, from tensile (In = 0.30) to compressive strain (In = 0.75) the eigen energy increases with strain for all the applied gate voltages. Due to the increase in eigen states, the subbands are less populated than the one with lower eigen states. Also notable from this figure is that the upper eigen states are more sensitive to the amount of strain (Fig. 3.5). This can attributed to the change in conduction band offset between channel and the buffer layer. The lowest eigen states lie close to the bottom of the quantum well formed and any change in the quantum well due to the change in band offset affects the upper eigen states.

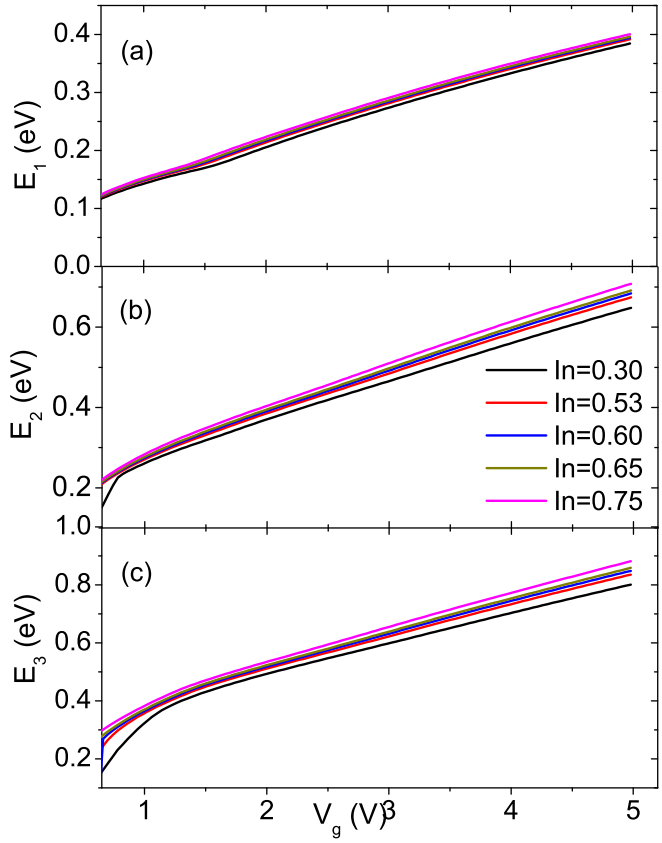

Figure 3.3: (a) First Eigen state (b) Second Eigen state (c) Third Eigen state as a function of gate voltage for different channel materials with $N_A = 5\times10^{17}$ cm^{-3}

Fig. 3.5 illustrates the effect of doping density on eigen states along with percentage

of strain. From this figure, it is observed that with the increase in doping density the eigen states is increasing. This is due to the fact that with increasing doping density the well becomes narrow as the depletion width decreases. However, it is noteworthy that the difference in eigen state due to doping density increases for higher subbands. Also, the third subband in lower doping is comparable with the second subband for higher doping. The change in eigen states due to strain is observed to be smaller in higher doping density. It can be observed more clearly in upper eigen states.

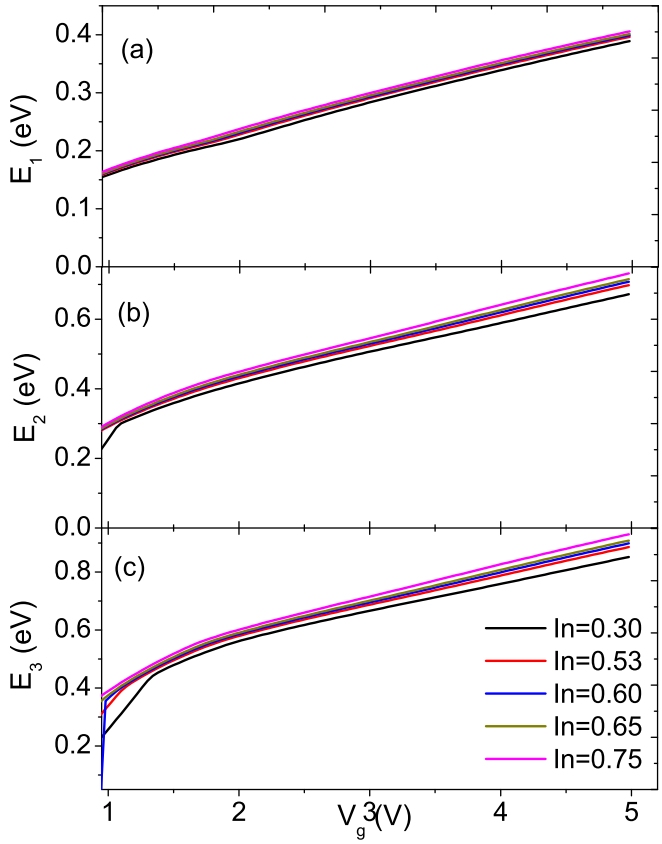

Figure 3.4: (a) First Eigen state (b) Second Eigen state (c) Third Eigen state as a function of gate voltage for different channel materials with $N_A = 1\times10^{18}$ cm^{-3}.

The important conclusion that can be drawn from this discussion is that due to lower eigen states, tensile strained device can have higher occupancy in the first subband and first subband becomes more populated.

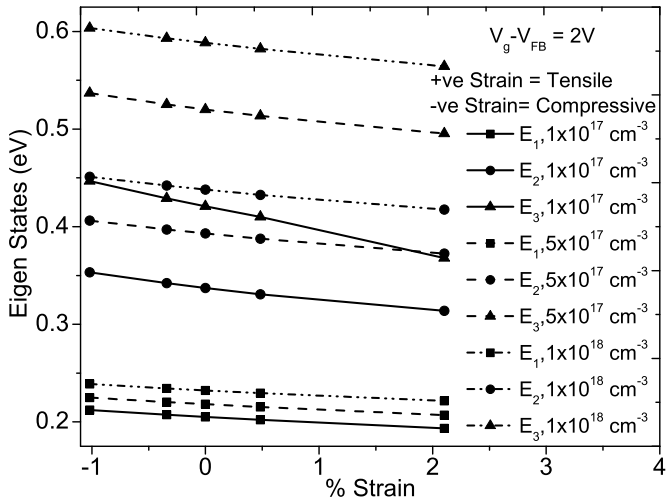

Figure 3.5: Three eigen states as a function of percentage strain for different doping density at a gate voltage of 2 V.

3.1.2 Sheet Carrier Density

The sheet carrier density is an important parameter which controls the C-V characteristics and also channel-formation. This quantity is affected by both effective mass and band diagram according to Eq. (2.8). Fig. 3.6, 3.7 and 3.8 represent the inversion sheet carrier density as a function of gate voltage for different channel materials for three doping densities. The figures reveal that in deep inversion region, the charge is not affected very much. The reason for this can be realized if we observe Fig. 3.9 where the energy band diagram is plotted for one tensile and one compressively strained device. In order to compare, two gate voltages are considered. For low gate voltage the discontinuity between the channel layer and buffer layer is closer to the bottom of the device whereas it lies much higher in case of high gate voltage.

When the band offset is closer to the bottom of the band it can affect the charge occupation of the lowest eigen state more easily than when it lies far from the bottom of the band. That is why in higher gate voltages the sheet carrier density is almost same for the devices having any channel material. For low gate voltage, the change in band offset affects the first eigen state and hence the inversion carrier density is affected by strain. For tensile strained material (In = 0.30) the carrier density is lower than the compressive strained device in lower gate voltage. That is why the carrier is

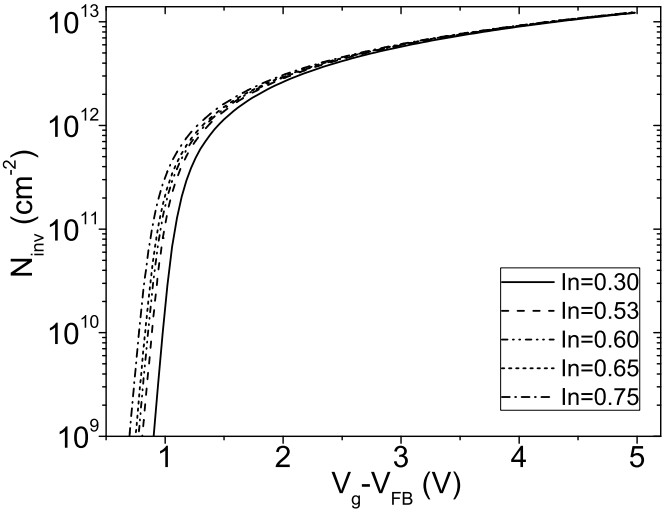

Figure 3.6: Inversion sheet carrier density as a function of gate voltage for different channel materials at a doping density of 1×10^{17} cm^{-3}.

changed in much higher rate in tensile strained device to make it equal to the carrier of compressively strained device in higher gate voltage. This can result in the higher inversion gate capacitance and higher threshold voltage. In order for our previous discussion to be valid, the first subband charge occupation needs to be dominant in these types of devices. This is evident in Fig. 3.10, 3.11 and 3.12 where the ratio of the 1^{st} subband carrier density to the total inversion carrier density is plotted for different channel materials against the gate voltage. From this figure it is evident that the first subband occupation is higher in compressive strained devices before the threshold voltage. This is because before the threshold, the depletion charge is dominant and the amount of total inversion charge is not significant. However, at the onset of threshold, the occupation of the first subband increases rapidly due to accommodate the higher rate of inversion charge generation.

After the threshold, the device tends to go towards deep inversion. Then the well becomes very much deeper and the upper subbands have non-negligible charge occupation and the ratio falls down gradually. From the figures it is also observed that in the deep inversion the first subband charge occupation is higher in tensile strained device than that of the compressive strained device. This opposite trend can cause the inversion gate capacitance to be higher in tensile strained device. From the first subband occupancy curve, we can give a new definition of threshold voltage. In the

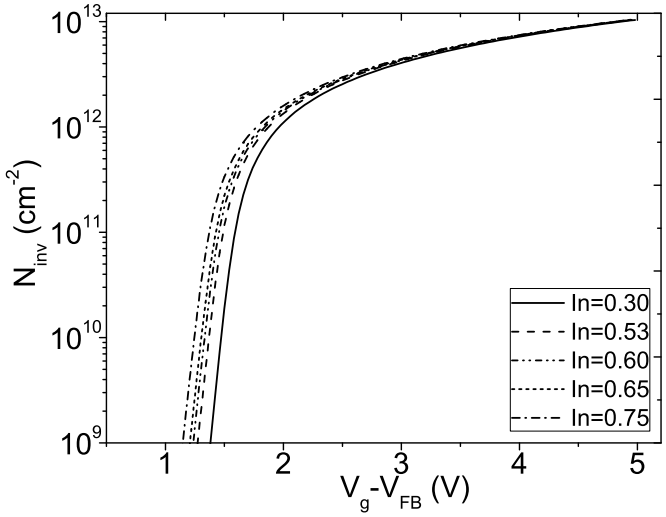

Figure 3.7: Inversion sheet carrier density as a function of gate voltage for different channel materials at a doping density of 5×10^{17} cm^{-3}.

Fig. 3.10, 3.11 and 3.12, we can easily determine the peak value of each curve and the gate voltage associated with the peak. This gate voltage can be defined as threshold voltage. As a matter of fact, threshold voltage is an important device parameter for which numerous definitions are present in the literature [49]. Our proposed method for extracting threshold voltage can be a novel technique to extract threshold voltage using self consistent simulation. In order to benchmark this method with an existing method, we have extracted threshold voltage for these set of devices using the 'extrapolation technique' described in [50]. Then we have compared the threshold voltage obtained by our proposed method with that of the reported method.

Fig. 3.13 shows the comparison of threshold voltages obtained using two methods as a function of Indium percentage in the channel. From this figure, it is evident that our method slightly underestimates the threshold voltage. However, it is in reasonable agreement with the reported method. The trend of the function closely matches for all doping densities. From this figure, the effect of strain of device threshold voltage is revealed. Tensile strained devices have higher threshold voltage than compressive strained device. This result suggest that strain engineering can be an effective way to channel engineering resulting in the ability to tune channel threshold voltage by changing the Indium mole fraction in channel.

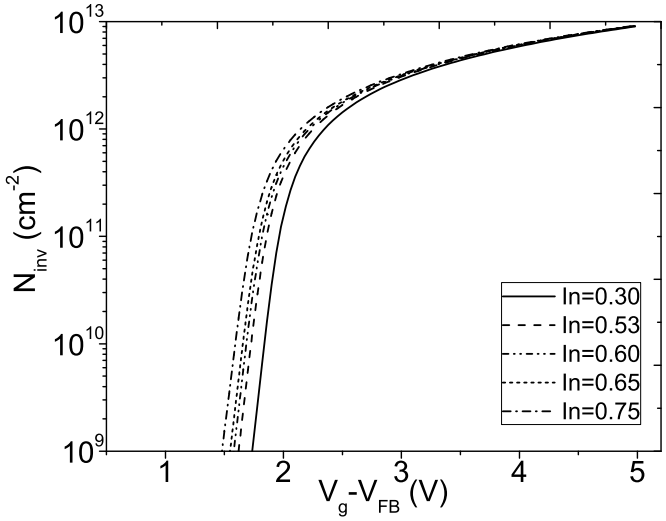

Figure 3.8: Inversion sheet carrier density as a function of gate voltage for different channel materials at a doping density of 1×10^{18} cm^{-3}.

3.1.3 Capacitance Voltage Characteristics

The capacitance voltage characteristics (C-V) is an important device performance which gives us the idea of device's dynamic behavior. Also, this characteristics facilitates numerous device parameter extraction [38]. The gate capacitance (C_g) of a MOSFET consists of two capacitance in series – a) Oxide capacitance (C_{ox}) and b) Semiconductor capacitance (C_s). Semiconductor capacitance is calculated by the differentiation of semiconductor sheet charier density with respect to semiconductor potential (surface potential). The gate capacitance is obtained by differentiating the total charge with respect to the gate voltage.

The relation between these quantities can be expressed as,

$$\frac{1}{C_g} = \frac{1}{C_s} + \frac{1}{C_{ox}} \tag{3.1}$$

In the Fig. 3.14, 3.15 and 3.16, the semiconductor capacitance as a function of surface potential is presented. In these figures, it is observed that semiconductor capacitance vary widely with the change in strain. Tensile strained device has higher semiconductor capacitance in inversion than that of the compressively strained device. Due to the higher threshold voltage, tensile strained device goes to inversion at a higher gate

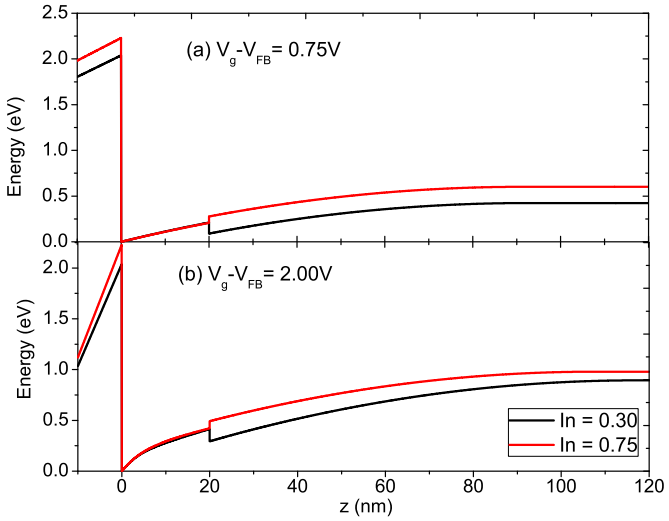

Figure 3.9: Comparison of energy band diagram of two differently strained device for different gate voltages having N_A=1×10^{17}cm^{-3}.

voltage and in the C_s-ϕ_s curve this is revealed by the late rise in the capacitance with increasing gate voltage. For this reason, there is a cross-over in gate capacitance. This cross-over can be explained in terms of the Fig. 3.10, 3.11 and 3.12 where this type of cross over is seen.

Due to this cross over, 1^{st} subband carrier concentration also demonstrate similar type of cross-over at the same point where this cross-over in C-V curve is observed.

Since the rate of change of charge concentration with respect to gate voltage gives us the capacitance, the tensile strained device show higher capacitance that that of the compressive strained device. Fig. 3.17, 3.18 and 3.19 gives the first subband carrier concentration for different channel materials as a function of gate voltage. From these figures, it can be observed that there is a cross-over after the threshold voltage where after the cross-over point tensile strained charge concentration becomes higher than that of compressively strained device. Hence, the rate of change of charge concentration is higher for tensile strained device. Thus the semiconductor capacitance is the highest in In = 0.30 device and lowest in In = 0.75 in deep inversion.

Indeed, this cross-over can be attributed to the knee region of the Fig. 3.10, 3.11 and 3.12. In these figures, the first subband occupancy is increased up to threshold voltage and then it decreases gradually. After threshold the inversion charge increases

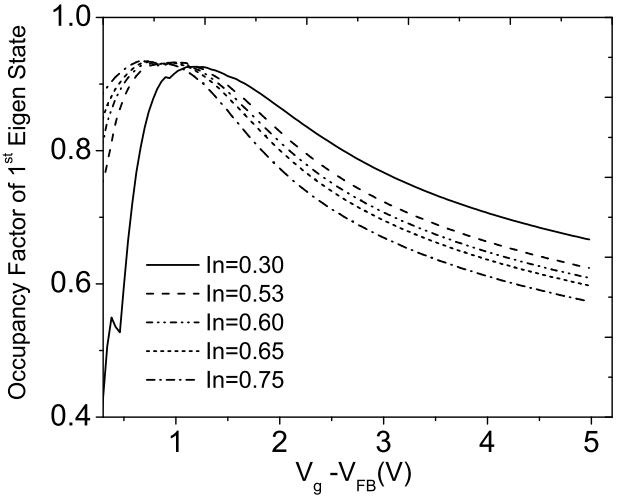

Figure 3.10: Ratio of the first subband carrier density to total inversion sheet carrier density as a function of gate voltage for different channel material at N_A = 1×10^{17} cm^{-3}.

rapidly and populates the higher subband and so the occupancy of the first subband decreases. However, the slope of the occupancy curve changes at deep inversion resulting in a knee region of the curve. The gate voltage corresponding to this knee region closely matches with the voltage in $C_s - \phi_s$ curve where the cross-over is seen. Hence the main reason for this cross over in semiconductor capacitance curve is the change in contribution of different subband to the total inversion charge. This result is quite different than that reported in [51] where the first subband occupancy is found to be constant at deep inversion for Si MOSFET. That is why, by multiplying a constant empirical parameter to the first subband carrier concentration, the total inversion carrier concentration can be determined in Si device. This is not possible in III-V MOSFETs because of its lower electron effective mass. Due to lower electron effective mass, the upper subbands become more populated compared to Si and its contribution in total charge can not be neglected. Furthermore, charge contribution of the upper subband is not constant throughout the entire bias region. For this reason, the $C_s - \phi_s$ shows a slope change and cross-over among different strained channels is observed.

Fig. 3.20, 3.21 and 3.22 illustrates the gate capacitance as a function of gate voltage for three different doping density. In these figures, the depletion and inversion region shows slight dependence on strain and it is consistent with the result shown previously.

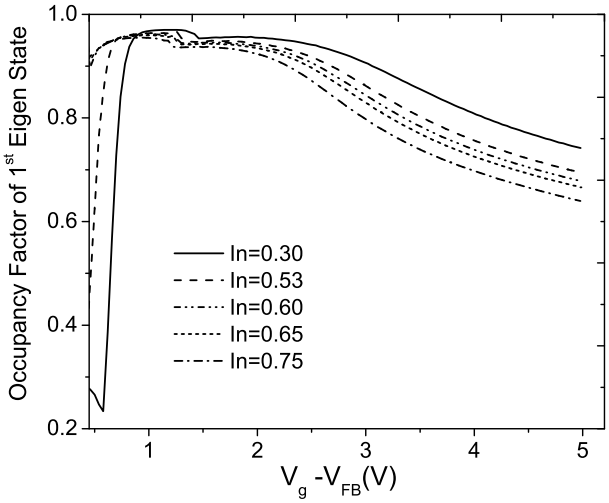

Figure 3.11: Ratio of the first subband carrier density to total inversion sheet carrier density as a function of gate voltage for different channel material at $N_A = 5\times10^{17}$ cm^{-3}.

Interestingly the dependence of C-V on strain in accumulation region is significantly different that what it is in inversion region. In the accumulation region, the gate capacitance for unstrained device is the lowest and the more strained the channel is the more gate capacitance is observed. For p-type channel material, the carrier in accumulation is hole. The sensitivity of hole parameters with respect to strain variation is higher than that of electron. In case of holes, both band offset and effective mass changes due to strain and for this reason the rate of change of charge concentration with respect to applied gate voltage varies significantly. The reason for unstrained channel to show the lowest gate capacitance is that in absence of strain, there is no band offset between channel and buffer layer. So the quantum well formed is not much prominent. In this case, the extended state charge dominates the overall charge concentration. This extended charge does not vary significantly for high gate bias. The bound state charge and extended state charge becomes comparable in high bias. That is why the rate of change of overall charge concentration is not higher than the strained device. So the gate capacitance is small compared to the strained device.

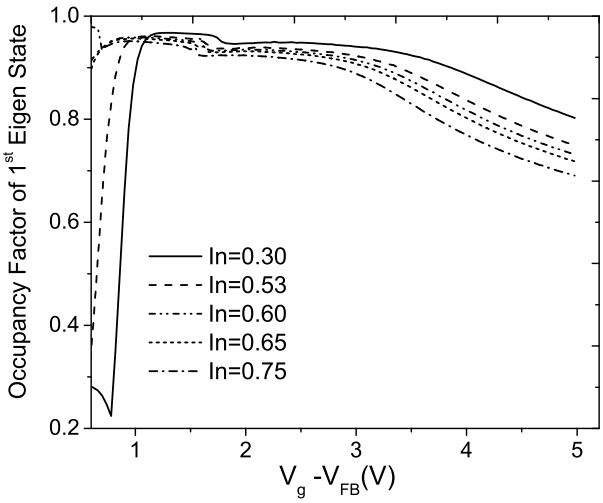

Figure 3.12: Ratio of the first subband carrier density to total inversion sheet carrier density as a function of gate voltage for different channel material at N_A = 1×10^{18} cm^{-3}.

3.2 Ballistic Transport Performance

When the gate length of the device is in the nanoscale regime, the drain current becomes ballistic. In the ballistic transport, scattering is not considered. So the ballistic transport calculation gives the limiting value of the transport performance of a specific device. It is an important performance parameter of the device. In this work, we have calculated the ballistic current of the $In_xGa_{1-x}As$ MOSFETs with the model shown in [41]. This model is based on the theory developed by Natori [40]. According to this model the total ballistic current is composed of the individual contribution of different subbands. For each subband, the carrier injection velocity is determined and the back-injection from drain is also taken into account. From this, the ballistic current is calculated.

Fig. 3.23, 3.24 and 3.25 presents the drain current as a function of drain voltage for a gate voltage of 2V. From this figure it is found that the tensile strained device gives less current compared to the compressively strained device. This fact can be more clearly observed in Fig. 3.26 where the drive current is plotted with respect to percentage strain. In this figure it is also noteworthy that for lower doping density the current varies more due to strain compared to the device with higher doping density. The rea-

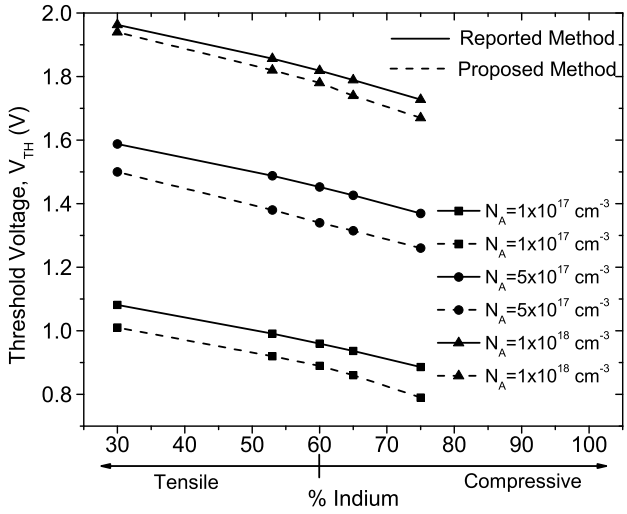

Figure 3.13: Threshold voltage as a function of Indium percentage in two different methods for different doping densities.

son for tensile strained device to have lower drain current is that in tensile strained device we have observed less inversion carrier concentration. Also, in tensile strained device the lowest subband occupancy is higher. So the contribution from upper subband makes the current is compressively strained device higher than that of the tensile strained device.

3.3 Comparison of Device Performance with and without Strain Effect

In order to understand the effect of strain on device performance we also need to look into the device performance without taking strain effect into account. This comparison will enable us to understand the importance of taking strain effect into account and the possible source of errors due to neglecting strain. Fig. 3.27 presents the comparison of C-V characteristics between the results obtained from strain effect taken into account and not taken into account. In this figure we can observe that strain has not much effect on capacitance at deep inversion but it has significant impact on capacitance at moderate inversion. This can be attributed to the similarity of inversion carrier density at deep inversion for all type of devices-strained and unstrained. However, if strain is

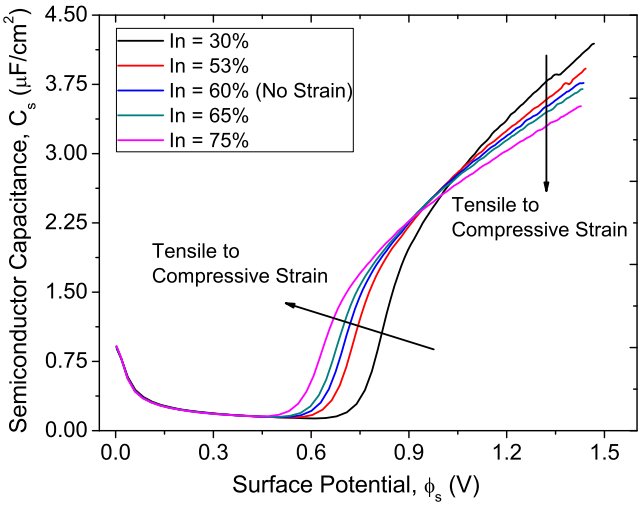

Figure 3.14: Semiconductor capacitance as a function of surface potential for $N_A = 1\times10^{17}$ cm^{-3}.

neglected, the threshold voltage estimation will not be correct. Fig. 3.28 presents the comparison of the threshold voltage with and without taking strain effect into account. From this figure we can understand that if the effect of strain is neglected in device simulation, threshold voltage is overestimated for tensile strained device and underestimated in compressive strained device. This will result into incorrect calculation of inversion carrier density and hence ballistic performance limit. In the Fig. 3.29, the opposite trend of threshold voltage (Fig. 3.28) is seen. From this curve, it is understood that due to incorrect estimation of threshold voltage, device current is overestimated in compressive strained device and underestimated in tensile strained devices. Also the change in device current from compressive to tensile strained device is smaller in strain effect is incorporated properly.

Thus neglecting strain effect can lead us to incorrect decision regarding device performance for $In_xGa_{1-x}As$ channel MOSFET, whose performance depend critically on the amount and type of strain evolved in the channel material.

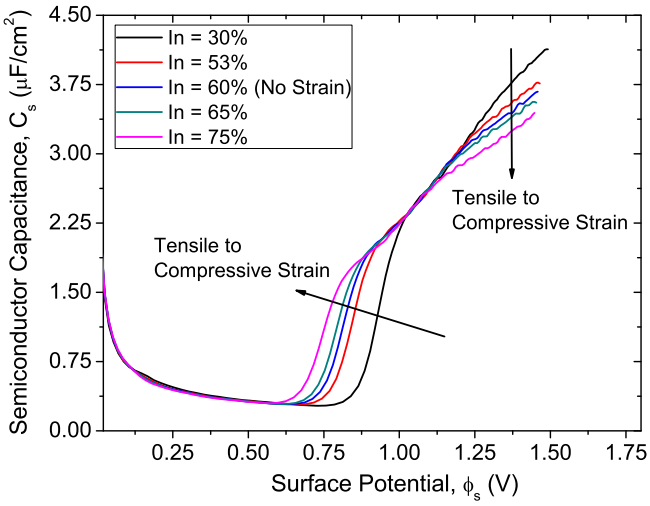

Figure 3.15: Semiconductor capacitance as a function of surface potential for $N_A = 5\times10^{17}$ cm^{-3}.

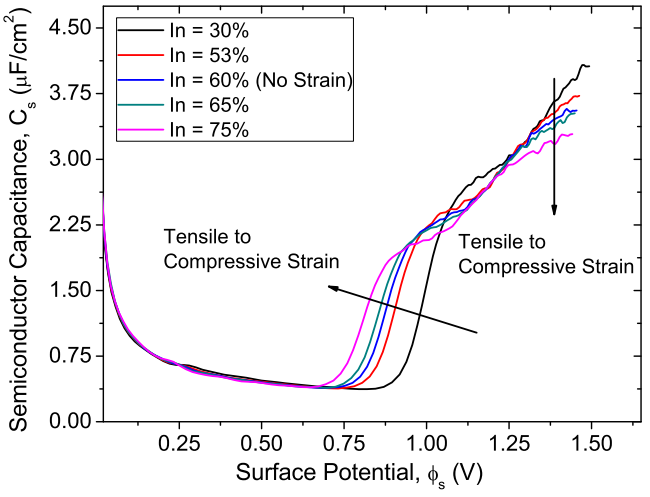

Figure 3.16: Semiconductor capacitance as a function of surface potential for $N_A = 1\times10^{18}$ cm^{-3}.

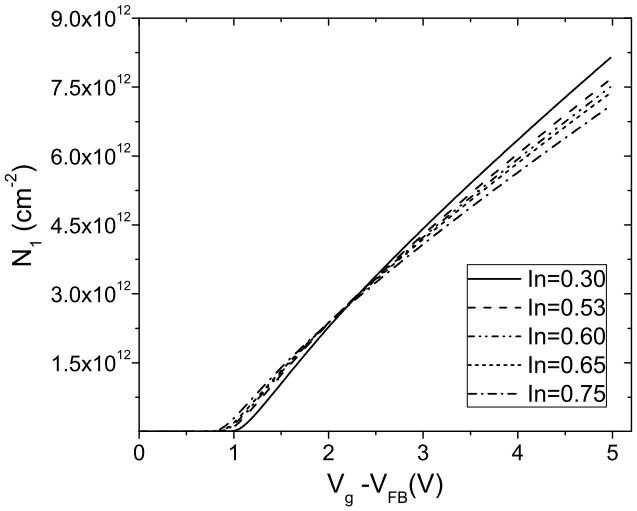

Figure 3.17: First subband carrier concentration as a function of gate voltage for N_A=1$\times 10^{17}$ cm^{-3}.

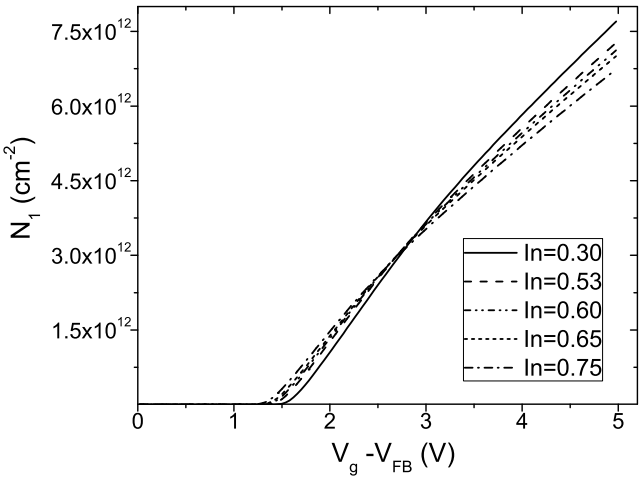

Figure 3.18: First subband carrier concentration as a function of gate voltage for N_A=5$\times 10^{17}$ cm^{-3}.

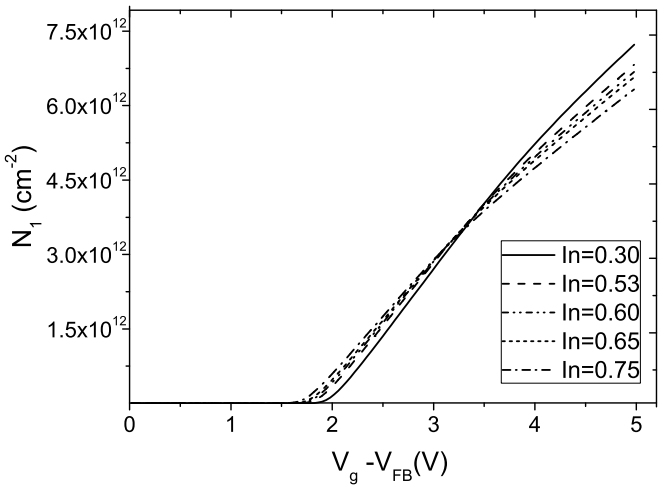

Figure 3.19: First subband carrier concentration as a function of gate voltage for N_A=1×10^{18} cm^{-3}.

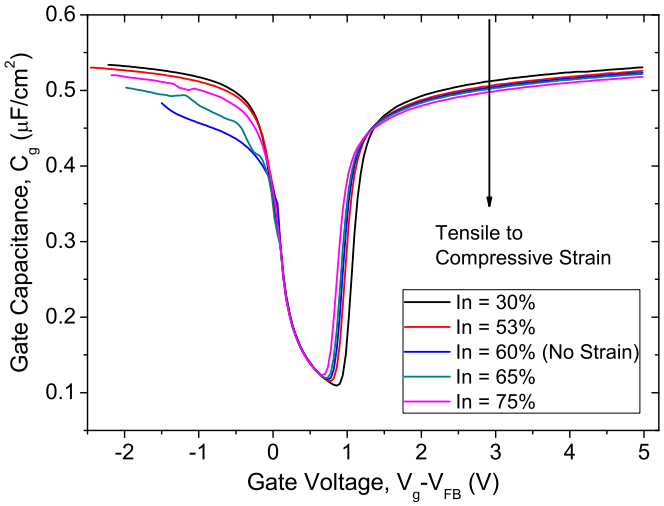

Figure 3.20: Gate capacitance as a function of gate voltage for different channel materials for N_A=1×10^{17} cm^{-3}.

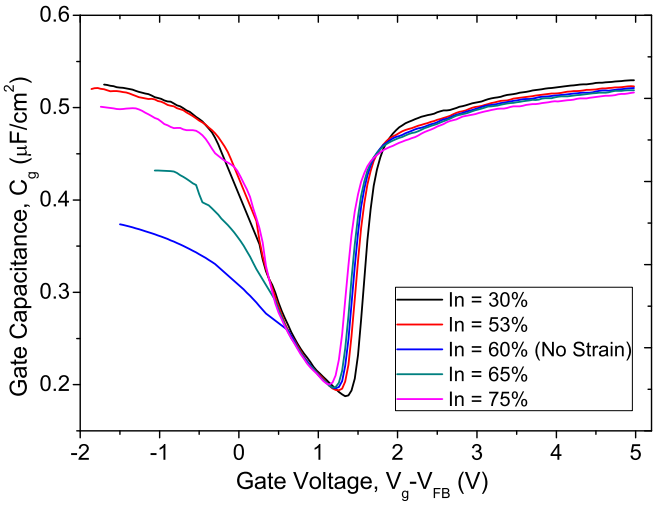

Figure 3.21: Gate capacitance as a function of gate voltage for different channel materials for N_A=5×10^{17} cm^{-3}.

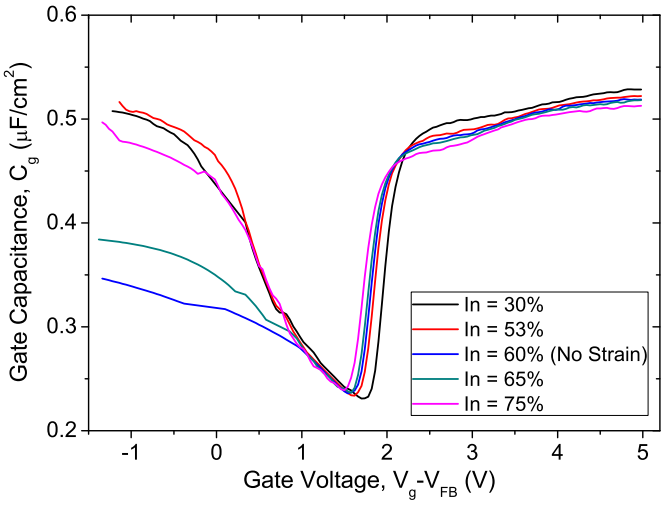

Figure 3.22: Gate capacitance as a function of gate voltage for different channel materials for N_A=1×10^{18} cm^{-3}.

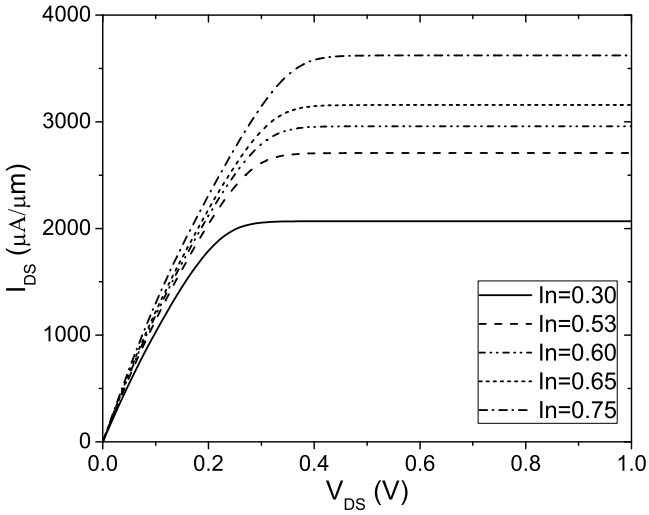

Figure 3.23: Drain current as a function of drain voltage for different channel materials for N_A=1×10^{17} cm^{-3} at the gate voltage of 2V.

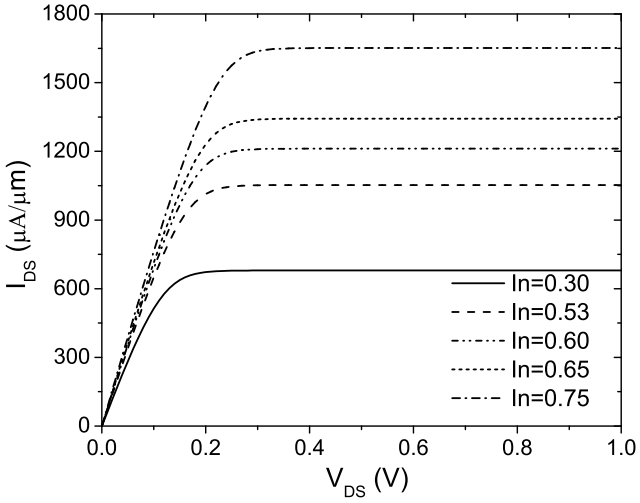

Figure 3.24: Drain current as a function of drain voltage for different channel materials for N_A=5×10^{17} cm^{-3} at the gate voltage of 2V.

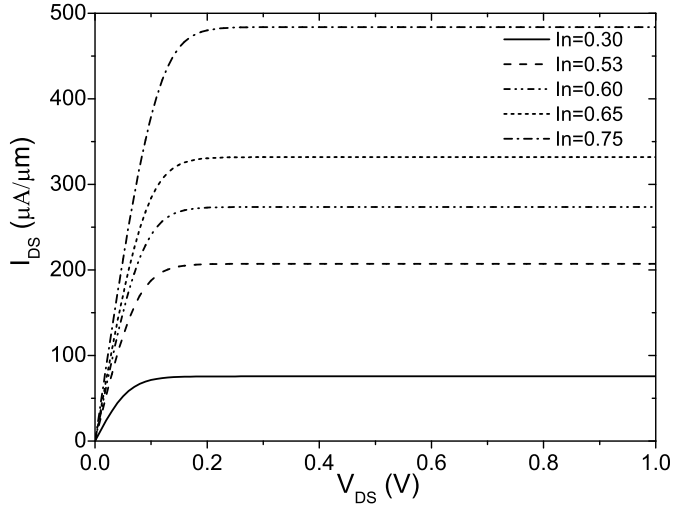

Figure 3.25: Drain current as a function of drain voltage for different channel materials for N_A=1×10^{18} cm^{-3} at the gate voltage of 2V.

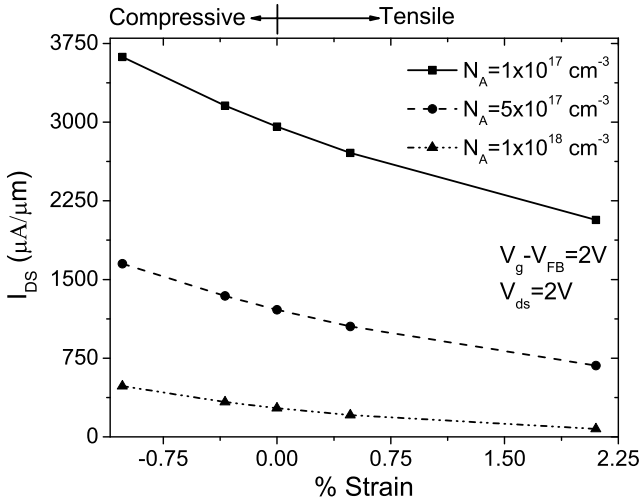

Figure 3.26: Drain current as a function of percent strain for different doping densities.

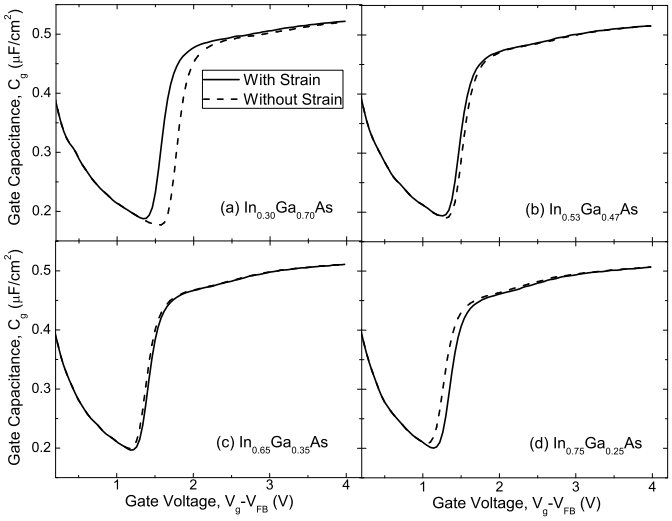

Figure 3.27: Comparison of gate capacitance as a function of gate voltage with and without strain effect into consideration.

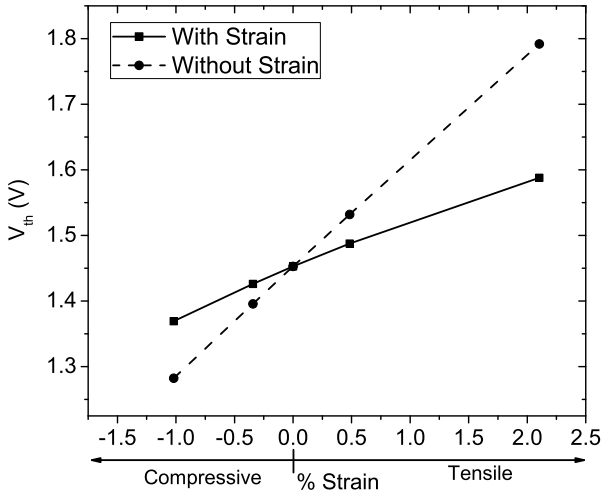

Figure 3.28: Comparison of threshold voltage as a function of strain with and without strain effect into consideration.

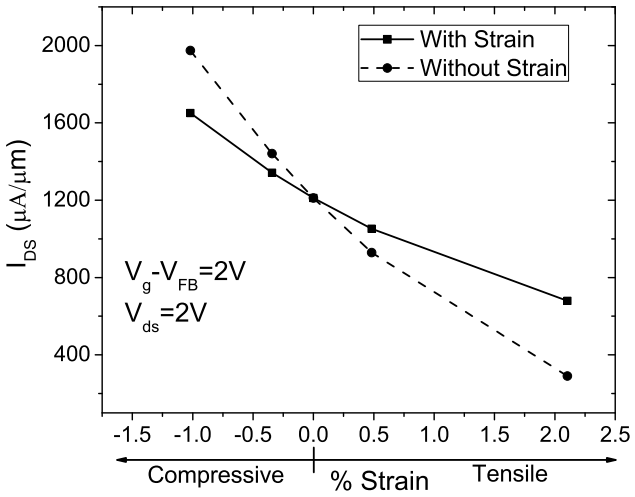

Figure 3.29: Comparison of drain current as a function of strain with and without strain effect into consideration.

Chapter 4

Analysis of MOS HEMT

In this chapter the basic device structure of MOS HEMT is discussed along with the simulation results.

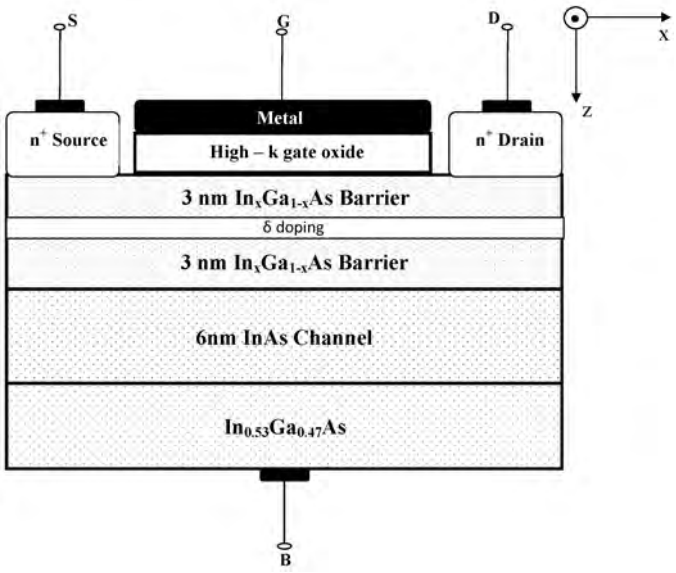

Figure 4.1: Basic device structure of the MOS HEMT considered in this work.

4.1 Basic Device Structure

Fig. 4.1 illustrates the basic device structure of the MOS HEMT considered in this work. The channel layer is InAs and it is kept fixed. The back barrier is always $In_{0.53}Ga_{0.47}As$

and it is lattice matched with InP substrate. The barrier layer has a delta doping region at the middle. The delta doped region is taken to be 1 nm. The total barrier layer is 7 nm. The doping that is considered in the delta doped region is $5 \times 10^{19}\ cm^{-3}$. Besides delta doping, uniformly doped barrier layer is also considered. However, in order to keep the total number of dopant atoms same, in case of uniformly doped barrier layer, the doping density is considered to be $5/7 \times 10^{19}\ cm^{-3}$. All the doping are of n-type. The channel layer is kept undoped in all the cases.

The Indium mole fraction is varied in the barrier layer. Three Indium mole fractions are considered i.e. 0.30, 0.53 and 0.75. For this MOS HEMT structure 1-D self-consistent simulation technique is applied. The basic model and formulation discussed in chapter 2 is applicable for this device. However, proper boundary conditions are used. This device is a depletion type device. So negative voltage is considered for device performance. Both electrostatic and transport properties of InGaAs/InAs MOS HEMT were

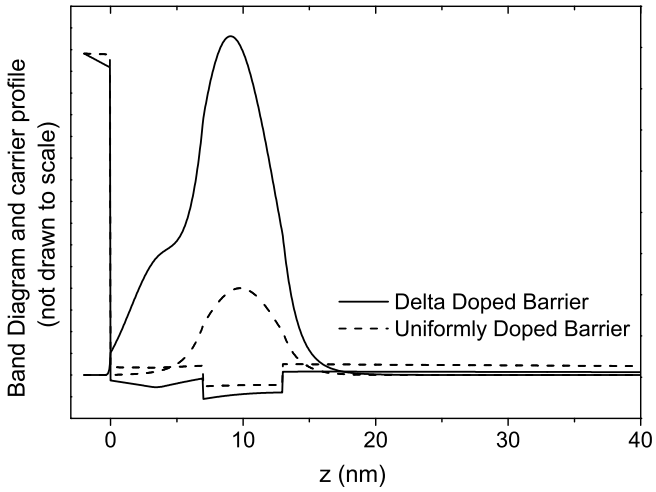

Figure 4.2: Energy band diagram along with carrier profile both for MOS HEMT having delta doped barrier and uniform doped barrier.

analyzed. For the purpose of comparison, both delta doped barrier and uniformly doped barrier were considered. The results are compared for three different Indium mole fractions in barrier layer. The channel is kept fixed all the time.

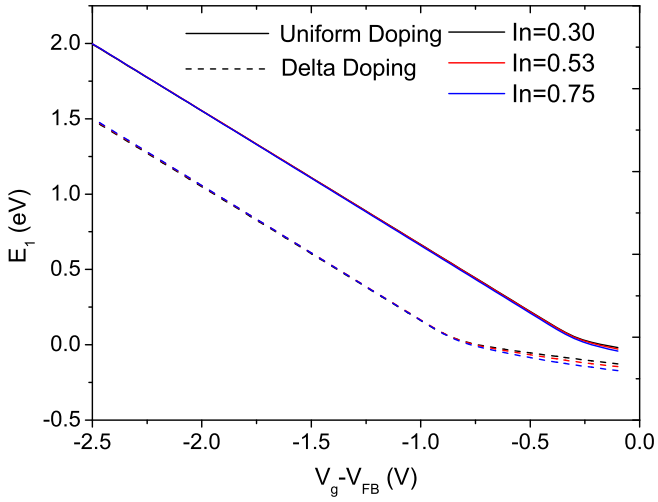

Figure 4.3: First eigen state as a function of gate voltage for both uniformly doped and delta doped barrier.

4.2 Electrostatic Properties

Fig 4.2 gives the general view of the energy band diagram of the device concerned for an applied gate bias along with the inversion carrier profile for both delta doped and uniformly doped barrier layer. The notable change in band diagram is observed and the difference in carrier profile is seen. However, the peak of the carrier profile remains inside the channel layer for both of these devices

Fig. 4.3 presents the first subband eigen energy as a function of gate voltage. Since the device works in the depletion mode, the gate voltages are negative. However, it is observed that with higher gate voltage in negative direction the device is turning off and the eigen state is increasing. The important thing to note here is that the difference in eigenenergy between uniformly doped and delta doped barrier layer. It has been observed that delta doped device turn off at a higher gate voltage. So it has a higher threshold voltage. Fig. 4.4 presents the 2-DEG (2-D Electron Gas) sheet carrier density as a function of gate voltage for both delta doped and uniformly doped device. In this figure, the effect of changing Indium mole fraction in the barrier layer is seen. However, it is more prominent in delta doped device than in uniformly doped device. The delta doped device show greater carrier concentration than uniformly doped device. This can improve device transport characteristics in the delta doped device. Fig. 4.5

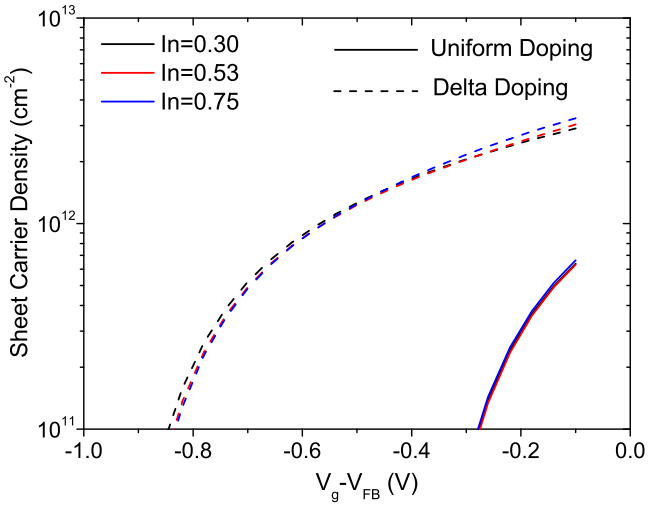

Figure 4.4: Sheet carrier density as a function of gate voltage for both uniformly doped and delta doped barrier.

illustrates the gate capacitance characteristics of the device for both uniform and delta doped barrier. Since this HEMT has an oxide gate, C-V characteristics can be an important performance metric. It is observed that the delta doped device show higher gate capacitance as compared to the uniformly doped device. However, the change in slope in C-V is seen in the delta doped device in the on region. This change in slope is maximum for In=0.53. However, with the changing Indium mole fraction the gate capacitance increases greatly. This can be attributed to the change in band offset that changes the quantum well configuration where the 2-DEG forms.

4.3 Transport Properties

The ballistic current is calculated for MOS HEMT in the same way as described in chapter 2. Fig, 4.6 presents the typical $I_d - V_d$ characteristics of the MOS HEMT. From this result, it is observed that the delta doping improves the current. However, when there is delta doping in the device the drive current is more sensitive to the Indium mole fraction in the barrier layer than when the doping in barrier layer is uniform.

In the conclusion, it can be said that Indium mole fraction does not have significant contribution in the performance of MOS HEMT specially for uniformly doped device.

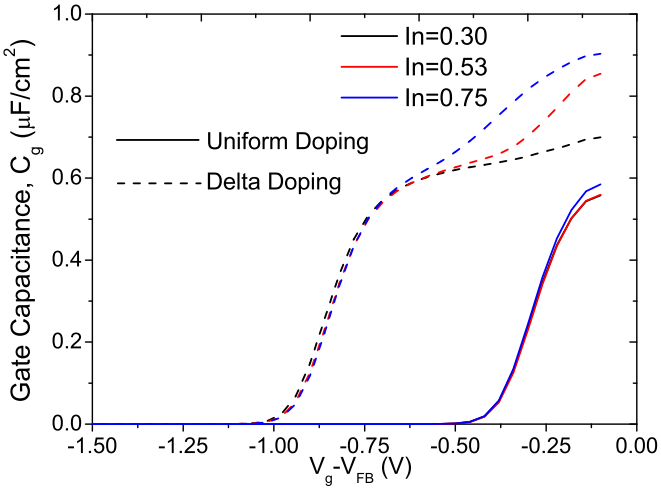

Figure 4.5: Gate capacitance as a function of gate voltage for both uniformly doped and delta doped barrier.

However, the delta doped barrier enhance the device performance in many perspective.

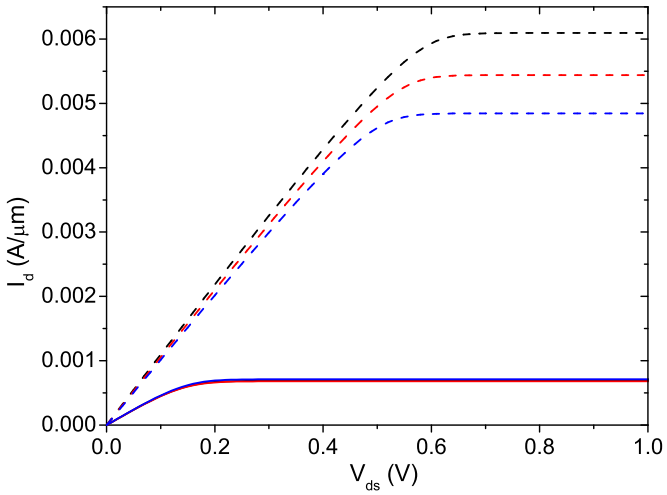

Figure 4.6: Drain current as a function of drain voltage for both uniformly doped and delta doped barrier at a gate voltage of 0.1V.

Chapter 5

Conclusion

5.1 Summary

In this thesis, a systematic and comprehensive study was done to investigate the effect of strain on the device performance of InGaAs surface channel MOSFETs. Also a comparative study is presented for InGaAs/InAs MOS HEMTs. In both the study, self-consistent simulation technique is used to determine the device performance under specific biasing condition.

Some important and interesting results are observed. Also a new method to determine the threshold voltage of InGaAs MOSFET is presented from the first subband occupancy curve. It has been observed that if the effect of strain is neglected, the inversion capacitance is not changed, but the threshold voltage is affected significantly. Also, it has been found that both tensile and compressive strain has significant effect on device performance. The inherent mechanism of strain to affect device performance has also been investigated. It has been observed that band offset has a significant effect on device performance and due to strain this band offset changes noticeably. In case of holes it is found that due to strain both the effective mass change and band offset change affect device performance. Hence the hole performance is critically dependent on the amount and the type of strain. Since the hole mobility is very small in III-V device, this

strain can be an effective way to channel engineering so that p-MOS device by III-V material can be made viable.

Also, from the analysis of MOS HEMT, it is found that the change in Indium mole fraction in the barrier layer does not affect device performance significantly. However, there is a significant improvement of device performance if delta doped barrier is used instead of uniformly doped barrier.

5.2 Suggestion of Future Works

This work can facilitate further study with this device structure. The suggestions for future work is as follows,

- The effect of variation of other device parameters like channel layer thickness can also be studied. Also, the change in Indium mole fraction in the barrier layer of InGaAs MOSFET can be a topic of study.
- Comparison of this device's performance with that of devices having nitride materials can be done.
- In this work, no effect of interface trap density is considered. However, interface trap density is an important issue pertaining to III-V materials and this can be taken into account while doing comparative study with III-V device.
- One method to extract threshold voltage is proposed in this study. Further studies can be done regarding the feasibility of this extraction technique and its effectiveness can be investigated.
- Only ballistic transport performance is considered in this work. Further study can be done with more complicated but accurate current calculation model.
- The effect of strain can be modeled analytically.

Bibliography

[1] "International technology roadmap for semiconductors," 2009. [Online]. Available: http://www.itrs.net/links/2009ITRS/Home2009.htm

[2] K. C. Saraswat, C. O. Chui, D. Kim, T. Krishnamohan, and A. Pethe, "High mobility materials and novel device structures for high performance nanoscale MOSFETs," 2002, pp. 659–662.

[3] R. Chau, B. Doyle, L. Kavalieros, D. Barlage, A. Murthy, M. Doczy, R. Arghavani, and S. Datta, "Advanced depleted-substrate transistors: Single-gate, Double-gate and Tri-gate," in *Extended Abstracts Int. Solid-State Devices Materials Conf.*, 2002, pp. 67–69.

[4] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, "High performance fully-depleted tri-gate CMOS transistors," *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 263–265, Apr. 2003.

[5] B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo, and D. L. Kwong, "Vertical Silicon-Nanowire formation and Gate-All-Around MOSFET," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 791–794, Jul. 2008.

[6] R. Chau, S. Datta, and A. Majumdar, "Opportunities and challenges of III-V nanoelectronics for future high-speed, low-power logic applications," in *Proc. Compound Semiconductor Integrated Circuit Symposium*, 2005, pp. 17–20.

[7] F. Ren, J. Kuo, M. Hong, W. Hobson, J. Lothian, J. Lin, H. Tsai, J. Mannaerts, J. Kwo, S. Chu, Y. Chen, and A. Cho, "$\mathrm{Ga_2O_3(Gd_2O_3)}$/InGaAs enhancement-mode n-

channel MOSFETs," *IEEE Electron Device Lett.*, vol. 19, no. 8, pp. 309 –311, Aug. 1998.

[8] Y. Xuan, Y. Wu, T. Shen, T. Yang, and P. Ye, "High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al_2O_3, HfO_2 and HfAlO as gate dielectrics," in *IEDM Tech. Dig.*, Dec. 2007, pp. 637 –640.

[9] Y. Xuan, Y. Wu, and P. Ye, "High-performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1 A/mm," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 294–296, Apr. 2008.

[10] Joachim Pipreck, *Semiconductor Optoelectronic Devices: Introduction to Physics and Simulation*. Academic Press: San Diego, California, 2003, pp. 27–32.

[11] Y. Xuan, T. Shen, M. Xu, Y. Wu, and P. Ye, "High-performance surface channel in-rich $In_{0.75}Ga_{0.25}As$ MOSFETs with ALD high-k as gate dielectric," in *IEDM Tech. Dig.*, Dec. 2008.

[12] Peide D. Ye, "Main determinants for IIIV metal-oxide-semiconductor field-effect transistors (invited)," *J. Vac. Sci. Technol. A*, vol. 26, no. 4, pp. 697–704, 2008.

[13] P. Hu, S. Feng, C. Guo, G. Zhang, and Y. Qiao, "Reliability evaluation of schottky contact of AlGaN/GaN HEMT, based on two AC voltages with different frequencies," in 10^{th} *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Nov. 2010, pp. 1710 –1712.

[14] G. Pozzovivo, J. Kuzmik, S. Golka, W. Schrenk, G. Strasser, D. Pogany, K. Cico, M. Tapajna, K. Frohlich, J.-F. Carlin, M. Gonschorek, E. Feltin, and N. Grandjean, "Gate insulation and drain current saturation mechanism in InAlN/GaN metal-oxide-semiconductor high-electron-mobility transistors," *Applied Phys. Lett.*, vol. 91, no. 4, Jul. 2007.

[15] T.-W. Kim, D.-H. Kim, and J. del Alamo, "30 nm $In_{0.7}Ga0.3As$ inverted-type HEMTs with reduced gate leakage current for logic applications," in *IEDM Tech. Dig.*, Dec. 2009.

[16] W. Kao, A. Ali, E. Hwang, S. Mookerjea, and S. Datta, "Effect of interface states on sub-threshold response of III-V MOSFETs, MOS HEMTs and tunnel FETs," *Solid-State Electronics*, vol. 54, no. 12, pp. 1665 – 1668, 2010.

[17] H. Becke, R. Hall, and J. White, "Gallium arsenide MOS transistors," *Solid-State Electron.*, vol. 8, no. 10, pp. 813 – 818, 1965.

[18] D. N. Butcher and B. J. Sealy, "The thermal oxidation of GaAs," *J. Phys. D: Appl. Phys.*, vol. 11, no. 10, 1978.

[19] O. A. Weinreich, "Oxide films grown on GaAs in an oxygen plasma," *J. Appl. Phys.*, vol. 37, no. 7, 1966.

[20] C. F. Yu, M. T. Schmidt, D. V. Podlesnik, E. S. Yang, and R. M. Osgood, "Ultraviolet-light-enhanced reaction of oxygen with gallium arsenide surfaces," *J. Vac. Sci. Technol. A*, vol. 6, no. 3, pp. 754–756, 1988.

[21] W. E. Spicer, I. Lindau, P. Skeath, C. Y. Su, and P. Chye, "Unified mechanism for schottky-barrier formation and III-V oxide interface states," *Phys. Rev. Lett.*, vol. 44, no. 6, pp. 420–423, Feb. 1980.

[22] H. L. Störmer, R. Dingle, A. C. Gossard, W. Wiegmann, and M. D. Sturge, "Two-dimensional electron gas at a semiconductor-semiconductor interface," *Solid State Communications*, vol. 29, no. 10, pp. 705 – 709, 1979.

[23] T. Mimura, S. Hiyamizu, T. Fujii and K. Nanbu, "A new field-effect transistor with selectively doped $\mathrm{GaAs/n-Al_xGa_{1-x}As}$ heterojunctions," *Jpn. J. Appl. Phys.*, vol. 19, pp. 225–227, 1980.

[24] M. Passlack, M. Hong, and J. P. Mannaerts, "Quasistatic and high frequency capacitancevoltage characterization of $\mathrm{Ga_2O_3-GaAs}$ structures fabricated by in situ molecular beam epitaxy," *Applied Phys. Lett.*, vol. 68, no. 8, 1996.

[25] M. Passlack, M. Hong, J. Mannaerts, R. Opila, S. Chu, N. Moriya, F. Ren, and J. Kwo, "Low $\mathrm{D_{it}}$, thermodynamically stable $\mathrm{Ga_2O_3-GaAs}$ interfaces: fabrication, characterization, and modeling," *IEEE Trans. Electron Devices*, vol. 44, no. 2, pp. 214 –225, Feb. 1997.

[26] M. Passlack, N. Medendorp, R. Gregory, and D. Braddock, "Role of Ga_2O_3 template thickness and gadolinium mole fraction in $Gd_xGa_{0.4-x}O_0.6/Ga_2O_3$ gate dielectric stacks on GaAs," *Applied Phys. Lett.*, vol. 83, no. 25, pp. 5262 –5264, 2003.

[27] K. Rajagopalan, J. Abrokwah, R. Droopad, and M. Passlack, "Enhancement-mode GaAs n-channel MOSFET," *IEEE Electron Device Lett.*, vol. 27, no. 12, pp. 959 –962, Dec. 2006.

[28] M. J. Hale, S. I. Yi, J. Z. Sexton, A. C. Kummel, and M. Passlack, "Scanning tunneling microscopy and spectroscopy of gallium oxide deposition and oxidation on $GaAs(001) - c(2 \times 8)/(2 \times 4)$," *J. Chem. Phys.*, vol. 119, no. 13, pp. 6719 –6728, 2003.

[29] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, H.-J. L. Gossmann, M. Hong, K. K. Ng, and J. Bude, "Depletion-mode $InGaAs$ metal-oxide-semiconductor field-effect transistor with oxide gate dielectric grown by atomic-layer deposition," *Appl. Phys. Lett.*, vol. 84, no. 3, pp. 434 –436, 2004.

[30] G. Dalapati, Y. Tong, W.-Y. Loh, H. K. Mun, and B. J. Cho, "Electrical and interfacial characterization of atomic layer deposited high-k gate dielectrics on GaAs for advanced CMOS devices," *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 1831 –1837, Aug. 2007.

[31] D. Shahrjerdi, E. Tutuc, and S. K. Banerjee, "Impact of surface chemical treatment on capacitance-voltage characteristics of GaAs metal-oxide-semiconductor capacitors with Al_2O_3 gate dielectric," *Appl. Phys. Lett.*, vol. 91, no. 6, 2007.

[32] L.-H. Huang, S.-H. Yeh, C.-T. Lee, H. Tang, J. Bardwell, and J. Webb, "AlGaN/GaN Metal-Oxide-Semiconductor High-Electron Mobility Transistors using oxide insulator grown by photoelectrochemical oxidation method," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 284 –286, Apr. 2008.

[33] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. Hudait, J. Fastenau, J. Kavalieros, W. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee,

W. Rachmady, U. Shah, and R. Chau, "Advanced high-K gate dielectric for high-performance short-channel $In_{0.7}Ga_{0.3}As$ quantum well field effect transistors on silicon substrate for low power logic applications," in *IEDM Tech. Dig.*, Dec. 2009.

[34] Y. Wu, R. Wang, T. Shen, J. Gu, and P. Ye, "First experimental demonstration of 100 nm inversion-mode InGaAs FinFET through damage-free sidewall etching," in *IEDM Tech. Dig.*, Dec. 2009.

[35] K. Kalna, A. Asenov, and M. Passlack, "Monte carlo simulation of implant free InGaAs MOSFET," in *Seventh International Conference on New Phenomena in Mesoscopic Structures and the Fifth International Conference on Surfaces and Interfaces of Mesoscopic Devices*, ser. Journal of Physics: Conference Series, vol. 38. Institute of Physics, 2006, pp. 200–203.

[36] J. Steighner, J.-S. Yuan, and Y. Liu, "Simulation and analysis of InGaAs power MOSFET performances and reliability," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 180 –189, Jan. 2011.

[37] N. Kharche, G. Klimeck, D.-H. Kim, J. del Alamo, and M. Luisier, "Performance analysis of ultra-scaled InAs HEMTs," in *IEDM Tech. Dig.*, Dec. 2009.

[38] M. M. Satter, A. E. Islam, D. Varghese, M. A. Alam, and A. Haque, "A self-consistent algorithm to extract interface trap states of MOS devices on alternative high-mobility substrates," *Solid-State Electronics*, vol. 56, no. 1, pp. 141 – 147, 2011.

[39] S. Datta, *Quantum Transport: Atom to Transistor*. Cambridge University Press, 2005.

[40] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *Journal of Applied Physics*, vol. 76, pp. 4879–4890, Oct. 1994.

[41] F. Assad, Z. Ren, D. Vasileska, S. Datta, and M. Lundstrom, "On the performance limits for Si MOSFETs: a theoretical study," *IEEE Trans. Electron Devices*, vol. 47, no. 1, pp. 232 –240, Jan. 2000.

[42] W.-C. Hsu, D.-H. Huang, Y.-S. Lin, Y.-J. Chen, J.-C. Huang, and C.-L. Wu, "Performance improvement in tensile-strained $In_{0.5}Al_{0.5}As/In_xGa_{1-x}As/In_{0.5}Al_{0.5}As$

metamorphic HEMT," *IEEE Trans. Electron Devices*, vol. 53, no. 3, pp. 406 –412, 2006.

[43] F. Stern, "Self-consistent results for n-type si inversion layers," *Phys. Rev. B*, vol. 5, pp. 4891 –4899, 1972.

[44] C. Moglestue, "Self-consistent calculation of electron and hole inversion charges at silicon-silicon dioxide interface," *J. Appl. Phys.*, vol. 59, no. 5, pp. 3175 –3183, 1986.

[45] D. A. Neaman, *Semiconductor Physics and Devices Basic Principles*, 3rd ed. McGraw-Hill International, Inc., New York, USA, 2003.

[46] C. Y. P. Chao and S. L. Chuang, "Spin-orbit-coupling effects on the valence band structure of strained semiconductor quantum wells," *Phys. Rev. B*, vol. 46, pp. 4110 –4122, 1992.

[47] D. Varghese, Y. Xuan, Y. Wu, T. Shen, P. Ye, and M. Alam, "Multi-probe interface characterization of $In_{0.65}Ga_{0.35}As/Al_2O_3$ MOSFET," in *IEDM Tech. Dig.*, Dec. 2008.

[48] M. M. Satter and A. Haque, "Modeling effects of interface traps on the gate C-V characteristics of MOS devices on alternative high-mobility substrates," *Solid State Electronics*, vol. 54, pp. 621–627, 2010.

[49] A. Ortizconde, F. Garciasanchez, J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectronics Reliability*, vol. 42, no. 4-5, pp. 583–596, 2002.

[50] Y. Tsividis, *Operation and Modeling of the MOS Transistor*. WCB McGraw Hill, Singapore, 1999, p. 98.

[51] F. Li, S. Mudanai, L. Register, and S. Banerjee, "A physically based compact gate C-V model for ultrathin (EOT $\sim$1 nm and below) gate dielectric MOS devices," *IEEE Trans. Electron Devices*, vol. 52, no. 6, pp. 1148 – 1158, Jun. 2005.