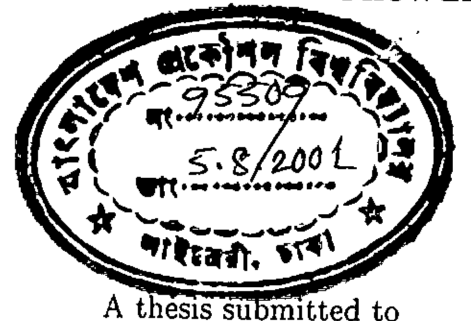
Study of tunneling gate current in a MOS structure incorporating inelastic scattering processes

by

Murshed Mahmud Chowdhury



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It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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Murshed Mahmud Chowdhury

Dedication

To my parents

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Abstract

The continuous down sizing of MOSFETs is decreasing the gate oxide thickness towards the deep sub-micron regime resulting significant increase in the gate current. Accurate modeling of this gate current is necessary from both power consumption and device modeling points of view. For the last three decades many models have been used to explain and estimate the gate leakage current. Most of the models are computationally extensive, overlooks the penetration of the wave function inside the oxide, ignores inelastic scattering effects and there remains a gap between modeled and experimental data. Despite the importance of scattering effects, extensive studies on trap distribution inside the direct tunneling gate oxide does not exist.

In this work, a simple tunneling current model is developed based on quantum mechanical wave impedance method. The model handles scattering effects by including an imaginary potential term in Schrödinger's equation. Different spatial distributions of traps inside the oxide layer have been considered by different researchers to explain the voltage-current characteristics of the gate current. However no theoretical investigation exists to estimate the trap distribution from the direct tunneling gate current. In this work different possible spatial distributions of traps inside the oxide layer have been considered to obtain a best fit between simulated and experimental gate currents. Formation of traps during fabrication and traps generated during operation are both taken into account to obtain the final expression for the trap distribution. It has been found that a Gaussian distribution of traps with peak at gate edge of the oxide gives the best fit with the experiment. The study also observes that carrier induced trap generation takes place during tunneling and is directly proportional to the probability density function inside the oxide. An excellent match between the experimental and simulated current values are obtained for the above mentioned trap distribution.

Chapter 1

Introduction

Transistor scaling theories require that the gate oxide thickness be reduced as the minimum channel length is scaled down to retain good control of the channel by the gate. Metal oxide semiconductor field effect transistor (MOSFET) with oxide thickness as thin as $15A^o$ has been fabricated and is expected to have good potentials in the future very large scale integrated circuits(VLSIs) [1]. With the decrease in oxide thickness gate tunneling current increases exponentially and has become a major design consideration. The increased gate current adversely affects MOS device performance and greatly increases the standby power consumption of highly integrated chips. Moreover, gate current in small dimension MOS transistors have substantial effect on appropriate modeling of the devices. Characterization of scaled devices requires accurate determination of the material and device parameters such as oxide thickness, oxide charges, substrate and polysilicon doping densities, etc. Both high and low frequency capacitance-voltage (C-V) characteristics are used in determining the device parameters. But anomalous dependence of C-V characteristics on test structure geometry for ultra-thin oxides were reported and is accounted for the tunneling of electrons [2]. Thus efficient modeling of gate current is important for the development of the advanced MOS devices.

1.1 Literature Review

Since its use as gate insulator in 1957 [3] many research works have been devoted to the conduction through silicon dioxide. In the last three decades two approaches are taken in explaining the experimental gate current with the physical origin in the literature. One explains with band to band tunneling [4-12] and the other is with trap assisted tunneling [13-21]. In 1969 Lezlinger and Snow [4] showed that the current through thermally grown silicon dioxide is 'electrode limited'. For rather thick oxides ($> 640A^o$) they showed that the gate current follows the Fowler-Nordheim (FN) emission theory. Like other similar works done at that time they overlooked quantum mechanical effects in the silicon inversion layer and their model underestimated the measured current. After Frank Stern's publication of self consistent results of quantum mechanical effects in the silicon inversion layer [22], quantum-effects were given serious thoughts in the modeling of gate current. Weinberg [5, 23] derived a different pre-exponential factor for the FN expression considering the fact that the FN expression derived by Fowler and Nordheim (1928) is based on the three-dimensional Fermi gas of free electrons where as in the inversion layer electrons form two dimensional Fermi gas due to quantum effects [22]. For more than $1000A^o$ thick oxides Weinberg showed that the modified FN model of gate current is consistent with the experimental results considering oxide effective mass is $0.5m_o$ (m_o =mass of free electron) and taking the carrier contribution from the lowest sub-band only. Rana *et al.* [7] modeled gate current including the accumulation regime self-consistently and showed good agreements with measured tunneling current. In their work they also explained why classical calculations were successful in predicting the tunneling currents. Self consistent solutions give a greater substrate potential drop and classical calculations give larger electric field in the oxide. The tunneling rate is dependent exponentially on both oxide electric field and the energy of incident electron. With increased gate voltage the difference in oxide electric fields predicted by the

classical and self consistent models increases but, at the same time the energies of electrons increase in self consistent models making the predicted tunneling currents similar in both models. Lo *et al.* [8, 24] modeled gate tunneling current calculating the lifetimes of quasi-bound states and achieved a quite good match with the measured gate current data. They also claimed that employing Wentzel-Kramers-Brillouin (WKB)approximation [5, 6] in calculating the tunneling current from thin oxides, is inappropriate. They argued that for electrons exhibiting quasi two-dimensional behavior, the transmission probability applicable to an incident Fermi gas is not a meaningful concept, however no quantitative proof have been provided. Shih and others [9] showed the viability of WKB approximation at low biases comparing the gate current models employing WKB approximation with their gate current model which employs first-order perturbation theory within the one-band effective mass approximation to calculate the lifetime of an inversion layer quasi-bound state. Register *et al.* [10] calculated the direct tunneling current in the accumulation regime considering the 'electron impact frequency' and employing a modified WKB approximation in calculating the tunneling probability. The correction in WKB approximation takes care of the reflection from the potential discontinuities. Yang and co-workers [11] developed gate current model for ultra-thin gate oxides employing modified WKB approximation [10] for the transmission probability and 'tunneling lifetime', and achieved good agreements with measured data except at very low biases. Recently Ghetti and others [12] have investigated different components of gate current using self consistent potential profile to calculate transmission probability through an exact solution of Schrödinger equation in the framework of effective mass approximation in terms of Airy's function following the transfer matrix method. In all the models described so far the tunneling current is assumed to be the result of band to band tunneling only. The potential barrier at Si/SiO_2 interface is assumed infinite in most of the models [7-12] i.e. wave functions penetration in the oxide

is ignored.

Different studies have shown that the prediction of band to band tunneling models differ appreciably with measured gate current specially at very low biases [8, 11, 24]. Although this is considered to be due to the effects of traps [11], detail and complete studies of the distribution of the traps and their effects on gate current in the direct tunneling regime are virtually nonexistent. Most of the authors [13-19] studied the effect of traps in the Fowler-Nordheim (FN) tunneling regime employing stresses on the insulator. Dummin and Maddux [13] found an increase in leakage current after the oxide is subjected to high voltage stress. They correlated this increase with the trap creation inside the oxide due to high voltage stress. They found that the leakage current increases linearly with the increase in trap densities. There study also found stress induced traps are generated near the injecting electrode and the conduction process after stress follows localized Schottky emission at the traps. Kuei and others [17] studied the effect of hot carrier induced interface traps on the gate current. They used a substrate injection model and verified the increase of gate current at high drain bias. Jang *et al.* [20] developed a gate current model using modified 'Lucky electron model' to include effect of oxide trapping especially by hot carriers for lightly doped drain and single-drain nMOSFETs. Takagi and co-workers [25] reported the presence of inelastic scattering in the stress induced leakage current and proposed a model for gate current [18] with energy relaxation based on two step tunneling model using WKB approximation. Duan and Yuan [19] studied the conduction band deformation effect on stress induced leakage current including the inelastic trap assisted tunneling.

In addition, to unveil the effects of traps on gate current, research works on the distribution of traps inside the oxide have been in progress for more than three decades and still there is no consensus on the distribution of traps inside the oxide. Khosru [26] studied the hole trap distribution inside the oxide using

charge pumping method and found that most of the traps are located within a few nano meter of Si/SiO_2 interface and the spatial distribution of traps is found to be an exponentially decreasing distribution function with respect to the distance from the Si/SiO_2 interface. Wei *et al.* [21] developed a technique to separate and characterize interface and oxide traps generated in an ultra-thin direct tunneling gate oxide. They found that direct tunneling shifts the trap centroid towards the anode and increase the oxide trap density in contrast to the trap generated in the FN regime. Yamabe *et al.* [27] have studied the trapped charges distribution by a combination of wet etching in silicon dioxide film and oxide surface topography by atomic force microscopy. From their study they found that traps are not only distributed near Si/SiO_2 interface but also in the wider range of SiO_2 and the distribution is not uniform.

1.2 Scope of the work

The effects of traps in direct tunneling gate current in thin oxides is overlooked in most of the works. But traps produced during fabrication or due to applied voltage has significant role in tunneling mechanism. Carrier tunneling through the silicon dioxide with the assistance of traps are discussed in this work. The traps are modeled by imaginary potential [28] and thus considered to introduce incoherent component in the gate current. Effect of different distribution of traps inside the oxide on gate current is examined. A non-uniform distribution of traps is proposed based on the matching of simulated gate current with the measured one. The gate current is found by exact solution of Schrödinger's equation in the effective mass framework employing quantum mechanical wave impedance method [29] and calculating the probability distribution function by Green's function formalism [30].

1.3 Thesis Layout

This thesis consists of five chapters of which chapter one gives an introduction followed by literature review and objective of this study.

Chapter 2 deals with brief description of MOSFET fundamentals and gate tunneling currents. It also contains a brief description of the origin of traps and their classifications.

In Chapter 3, the mathematical model used to calculate the scattering assisted tunneling currents in MOSFET is developed. It also presents the quantum mechanical calculations in the Si substrate inversion layer.

The simulation results are presented in Chapter 4 based on the model developed in Chapter 3. The calculations are done for thin oxide ($< 32A^o$) MOSFETs in the inversion regime. Different traps distribution are studied to obtain the best possible match with the experimental results.

Conclusive remarks and discussions are given in chapter 5 with a recommendation for further works.

Chapter 2

Review of MOS Theory

The concept of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) was first proposed by Lilienfeld (1930). The basic idea of the device is analogous to that of a capacitor, where one plate of the capacitor serves as a conducting channel between two ohmic contacts. The other plate controls the charges induced in the channel. When an ideal zero conductance insulator is placed between the plates then no dc current passes through the plates. If the conducting channel is induced by other plate then the device is called enhancement type MOSFET. On the other hand if the conducting channel is diffused during fabrication the device is called depletion type MOSFET. Each type has an n and p sub-type depending on the type of carrier (electrons or holes) contributing the current. In this chapter a brief overview of n type enhancement MOSFET physics and a description of the gate leakage current is presented.

2.1 The nMOSFET

The structure of an n-channel enhancement-type MOSFET, shown in Fig. 2.1, consists of a moderately doped p-type silicon substrate into which two heavily doped n^+ regions, the source and the drain are diffused. Between these two regions there is a narrow region of p-type substrate, called channel. A layer of SiO_2 insulator is sandwiched in between the substrate and a poly crystalline silicon

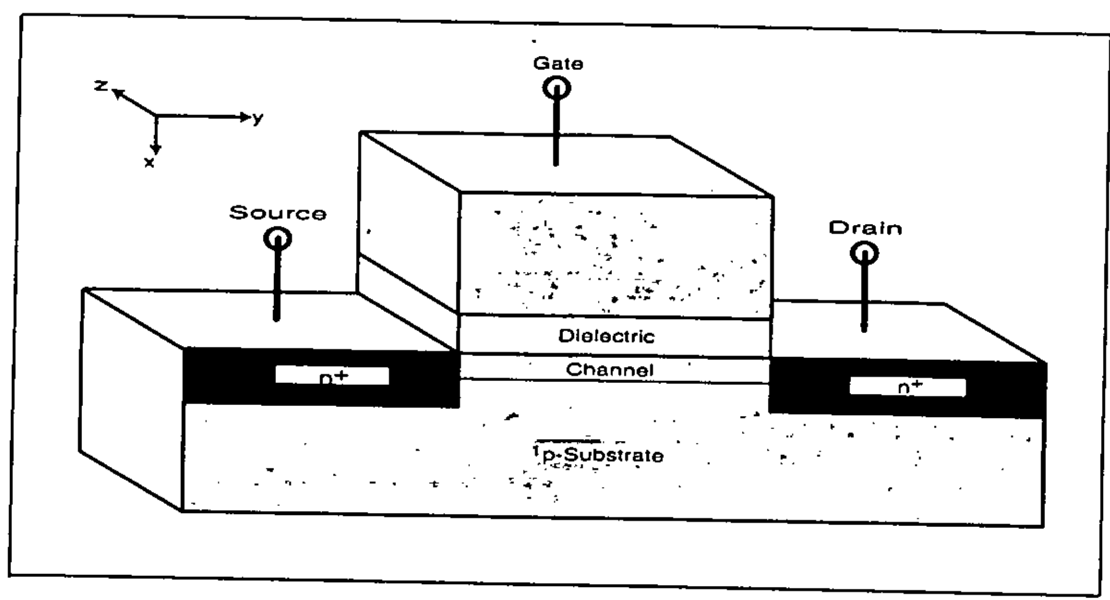


Figure 2.1: Basic n-channel MOSFET structure. Current flow is along the y−direction, the confinement potential varies along x−direction and the width of the device is along z−direction.

(or metal such as aluminum) referred to as the gate. When a positive voltage is applied to the gate, relative to the substrate and source, positive charges are accumulated on the gate metal and negative charges are induced in the underlying Si, forming a depletion region and a thin sheet of mobile electrons. The variation of the gate voltage changes the electron concentration in the channel and, hence, the channel conductance and the device current. When the drain to source bias is applied, charge carriers move from the source to the drain across the channel.

2.2 The Band Diagram

The $E - x$ diagrams of an ideal MOS transistor is shown in the Fig. 2.2 at zero bias [31]. At zero bias voltage the band bending in the semiconductor layer is determined by the difference of the work functions of the metal and the semiconductor. The band bending may be compensated by applying a voltage, V_{FB}

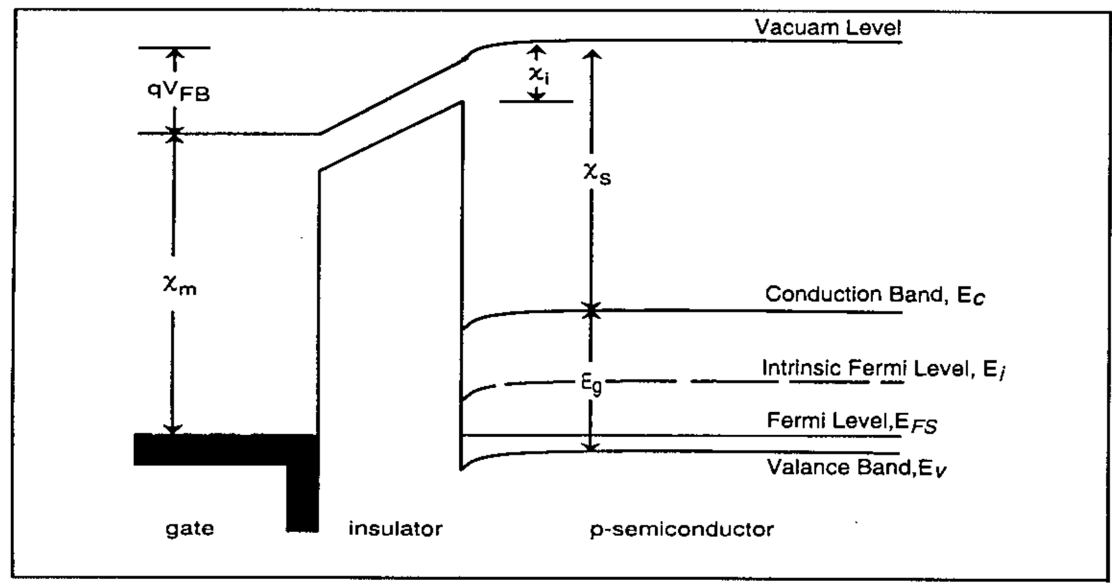


Figure 2.2: Band Diagram for the ideal MOS structure at zero bias for $\chi_M < \chi_s$.

across gate and substrate equal to this difference:

$$V_{FB} = \chi_m - \chi_s - E_c + E_F \quad (2.1)$$

where χ_m is the metal work function, χ_s is the electron affinity of the semiconductor, E_c is the conduction band edge, E_F is the Fermi level. V_{FB} is called the *Flat band voltage* and typically has a value around $-1V$. In practical cases Eq. 2.1 has to incorporate the effect of surface states at the interface layer and the presence of fixed charges in the insulator. As seen from the Fig. 2.2 at zero bias and when $\chi_m < \chi_s$ the concentration of holes near surface is less than that in the bulk. When the flat band voltage, V_{FB} is applied to the gate, the bands become flat (Fig. 2.3) and the concentration of holes at the insulator-semiconductor interface becomes equal to the equilibrium concentration of holes in this p-type semiconductor. When larger positive bias is applied to the gate, the region close to the insulator-semiconductor interface becomes depleted of holes. This situation is named as the *depletion*. At even larger positive gate voltages the band bending becomes so large that the Fermi level at the insulator-semiconductor interface be-

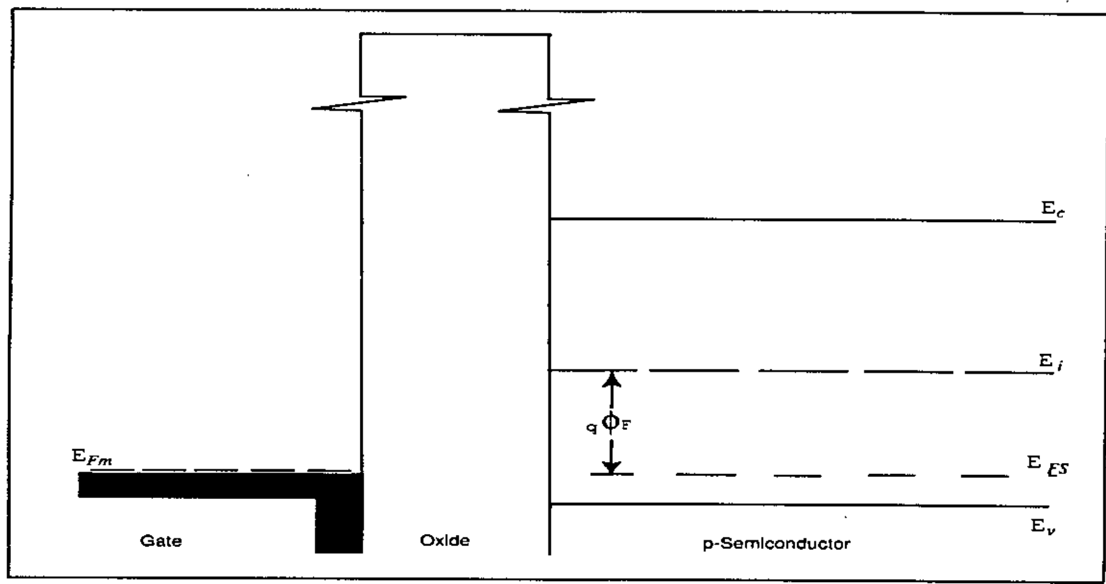


Figure 2.3: Band Diagram for the ideal MOS structure under flat band condition

come closer to the bottom of the conduction band than to the top of the valence band (Fig. 2.4). In this case the concentration of carriers near interface actually corresponds to that of an n-type semiconductor. This is called *inversion.* The concentration of electron increases exponentially with the increase of band bending. The inversion is defined as strong inversion when the difference of the Fermi level and the intrinsic Fermi level at the interface becomes equal and opposite in sign to this difference in the bulk of the semiconductor. That is, the total band bending at interface, ϕ_s at the onset of strong inversion is [32]:

$$\phi_s = 2\phi_F = 2\frac{kT}{q}\ln\frac{Na}{n_i} \tag{2.2}$$

where N_a is the acceptor concentration, n_i is the intrinsic carrier concentration, k is the Boltzmann's constant, q is the electronic charge and T is the temperature in Kelvin. The minimum gate voltage required to induce strong inversion is termed as *threshold voltage*, V_T. Taking zero substrate potential, negligible interface charges and poly-silicon depletion effects and assuming the inversion layer charge small compared to that in the depletion layer at the onset of strong inversion V_T

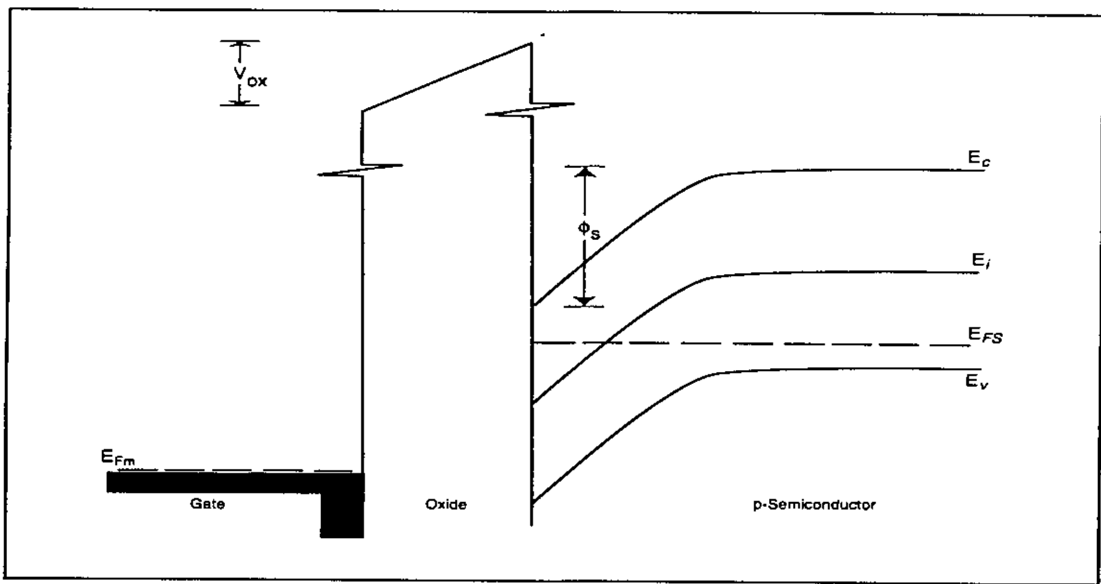


Figure 2.4: Band Diagram for the ideal MOS structure at inversion condition

can be written as:

$$V_T = V_{FB} + 2\phi_F + (4qN_a\phi_F\epsilon_s)^{1/2}/C_{ox} \tag{2.3}$$

where ϵ_s is the dielectric permittivity of substrate and C_{ox} is the oxide capacitance given by ϵ_{OX}/t_{OX}; ϵ_{OX} is the dielectric permittivity of oxide and t_{OX} is the oxide thickness.

In the inversion regime, if a voltage is applied across drain to source current starts flowing laterally. But the presence of a dielectric (large band gap) in the transverse direction impedes current flow in the transverse direction, from the substrate to the gate.

2.3 The Gate leakage Current

Due to the presence of a barrier in the Si/SiO_2 boundary (Fig. 2.4) classical mechanics predict negligible gate current flow in MOSFET. But quantum mechanics predicts flow of current in the transverse direction by a process called quantum tunneling. Both electron and holes are capable of tunneling through the barrier

even if the energy of the carrier is much less than the potential barrier of the gate oxide layer. As the device is scaled down the gate oxide thickness is also reduced and the gate tunneling current increases exponentially. In today's thin oxide MOS transistors, gate leakage current is due to mainly two types of electron tunneling, namely interband tunneling and trap assisted tunneling, in contrast to the old generation MOSFETs where the thermionic emission is the dominant gate current mechanism.

2.3.1 Interband Tunneling

The interband tunneling occurs because of the finiteness of the height and width of the oxide barrier. It can be either direct (DT) or Fowler-Nordheim (FN) tunneling depending upon the magnitude and polarity of the applied gate voltage [33]. The mechanisms are governed by the shape of the tunneling barrier. If the oxide barrier is trapezoidal and the electrons do not transit through the conduction band states, then the tunneling is said to be direct tunneling (Fig. 2.5(a)). If the tunneling barrier is triangular and the transported electrons partly transit through the conduction band states, then FN tunneling (Fig. 2.5(b)) is said to occur. In devices with ultra-thin oxides DT is the dominant interband tunneling mechanism and exists even under near equilibrium condition.

2.3.2 Traps and trap-assisted Tunneling

Other than the finite thickness of the oxide barrier there is another mechanism of current conduction through the oxide layer. Any breakdown of regular periodicity of the oxide layer may act as trap for electron or hole and can cause additional leakage current. The traps in the metal-semiconductor-insulator structure can be classified according to their physical location, type and atomic origin [34]. In a MOS structure, traps are distributed mainly in three areas, (i) The gate-oxide interface (ii) The oxide layer and (iii) the Oxide-Substrate layer. It is expected

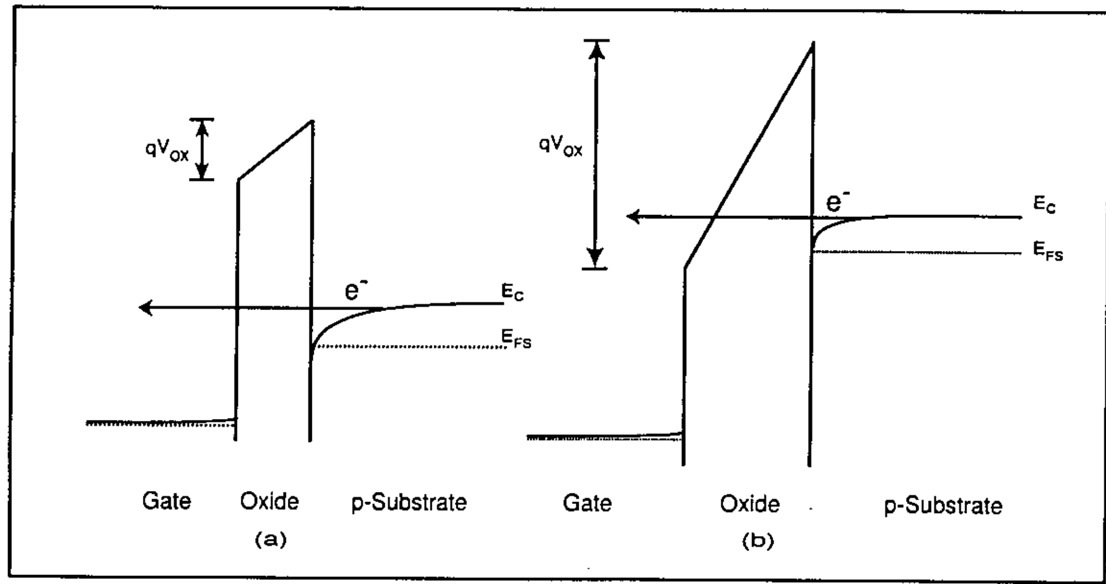


Figure 2.5: Interband tunneling in MOS: (a) Direct Tunneling (b) Fowler-Nordheim tunneling

that there are traps in the Si substrate and gate conductor layers, their impact is yet to be proved from leakage current point of view .

The traps can be either electronic or protonic. The electronic traps cover both electron traps and hole traps. These are imperfection centers having three dimensional quantum mechanical electron bound state solution for electron traps or hole bound state solutions for hole traps. The term 'imperfections' refers to the dangling bonds from host atoms and the impurities, both of whom have sufficiently large localize potential to trap an electron or a hole. The electron trap can also trap a hole and vice-versa. For example an electron trap after capturing an electron can capture a hole. The protonic traps [34] are centers which can capture one or more protons or hydrogen atoms.

The electron traps can be of two types depending upon their origin - (i) traps formed during fabrication (ii) traps generated due to applied gate voltage. Traps formed during the fabrication steps are intrinsic oxide traps, intrinsic interface traps and impurities. Intrinsic oxide traps includes the trivalent silicon or silicon

dangling bonds, the oxygen vacancy or double silicon dangling bonds, the broken strained $Si - O$ bonds, etc. [34]. These traps are of rather complex configuration originated from the crystalline silicon and amorphous oxide's bond mismatch. During the fabrication steps impurities may substitute the silicon atoms in the SiO_2 matrix and act as traps. For example poly-Si gate is doped by boron implantaion to obtain resonable conductance. During this implantation it is necessary to activate the dopant with a high-temperature anneal, typically in $950 - 1050^oC$. At this high-temperature boron has very high diffusion coefficient in silicon dioxide and as such penetrates into the gate dielectric [3]. Other than boron, phosphorus, germanium, aluminum, hydrogen, chlorine, etc. may also get implanted in the SiO_2 layers. These impurities are substitutional and may get bonded to oxygens and/or dangling oxygen bonds inside SiO_2.

During operation, defects may be generated by the tunneling of carriers (electrons or holes) through SiO_2. The energy of the carrier has direct effect on the generation of such defects and on the rates they are produced. There are four regions for which the relation between generation of the defects and electron (or hole) energy is clarified [3, 35, 36]. The first regime is where the electron energy is greater than $9eV$, the band gap of SiO_2. Electron-hole pairs are created by impact ionization and the subsequent trapping of holes and electrons, and the recombination of electrons on trapped hole sites, generates defects in the form of electron traps and interface states. This regime is generally limited to thick films and extremely high electric field. When carrier energy is less than the SiO_2 band gap, traps are created by anode hole injection. At these energies holes can be created at anode and may be injected back in the oxide film, where they can be trapped and create defects. Anode hole injection occurs in either relatively thick films ($> 100A^o$) and when the electric field across the oxide is greater than $\sim 5MV/cm$, or in thin films with applied bias greater than $\sim 7 - 8V$. The third regime includes only electrons. When the electrons have energy at least

$2eV$ above the SiO_2 conduction band they can create defects by a mechanism termed as 'trap creation' [3]. The threshold voltage, $2eV$ [35] is approximately the energy required to liberate a hydrogen bond from SiO_2 matrix. This regime requires a bias voltage between 5 to 7 volts (for poly-Si gate MOS devices) [3]. The fourth regime is where defect is created below a bias voltage $< 5V$. The actual mechanism of the creation of the defects in this regime is not yet very clear and assumed to be resulted from the transport of electrons through the oxide and is statistical in nature.

In trap-assisted tunneling electron tunnels from silicon conduction band to trap level in the forbidden gap of oxide. The traps can be considered as localized scattering centers and the trap assisted tunneling can be through elastic as well as inelastic channels. The inelastic scattering is a specific case of scattering where the total kinetic energy changes and in which a specific energy level is excited or deexcited, while in the elastic collisions energy and phase coherence is conserved [37]. However, when there is sufficiently large number of randomly distributed impurities and defects, elastic scattering also has phase randomizing effects due to averaging over many paths corresponding to different actions [38]. Also inelastic scattering is presumably more effective in phase randomizing than in relaxing energy [38]. Thus in scaled MOS transistors the effects of traps can be assumed to be limited in phase randomizing of carriers only.

From the above discussions the gate current can be decomposed into two components: one is the coherent part arising from the fact that the barrier thickness is finite and the second is the incoherent part due to the effects of defects and impurities in the oxide.

Chapter 3

Quantum Model of MOS devices

Scaling of the MOS devices result in the reduction of device dimensions and substrates tend to have a high impurity concentration facing a strong electric field. As a result, energy states quantize into subbands and make the classical models unreliable [39] in describing MOSFET behavior. Even at near flat band, when confinement of majority carrier is weak, classical models are not satisfactory [40]. That is why quantum mechanical (QM) models are necessary to describe the charge distribution in the inversion layer formed at the insulator semiconductor interface due to the transverse field caused by the gate bias. Calculation of quantum mechanical effects in the substrate inversion layer and QM formulation of gate leakage currents from the MOS inversion layer is presented in this chapter.

3.1 QM Calculation of the Silicon Inversion Layer

The transverse electric field required to create inversion in the channel causes band bending in the substrate. Hence, a potential well is formed at Si/SiO_2 interface. In modern MOS devices, even near threshold, the transverse field is so high that it induces significant band bending. In such cases, the well becomes narrow to quantize the motion of the carriers in the direction perpendicular to the interface and splits energy levels into subbands (Fig.3.1). The lowest of the energy bands in the well does not coincide with the bottom of the conduction

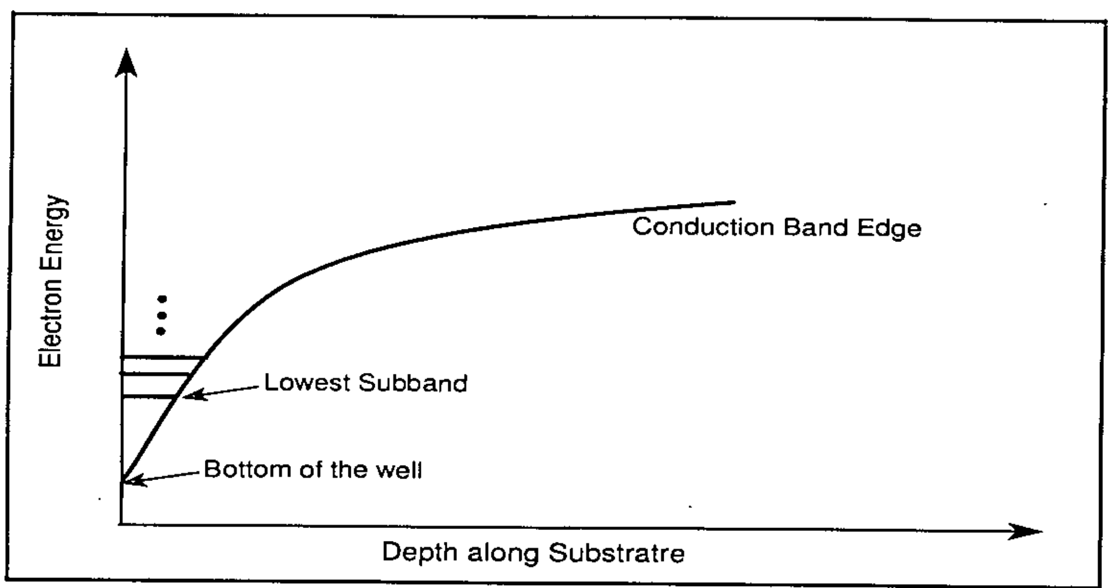


Figure 3.1: Splitting of electron energy state into subbands in the substrate. The energy states are displaced upward from the bottom of the conduction band.

band. Classical mechanics does not give this picture of discrete energy bands and leads to an overestimation of carrier concentration at inversion. So a proper quantum mechanical treatment of charge carriers is necessary.

In this work the Schrödinger's equation is solved using effective mass approximation by Quantum Mechanical Wave Impedance (QMWI) [29] method assuming the substrate potential distribution to be exponential.

Using the effective mass approximation the one electron Schrödinger Equation is written as

$$\frac{-\hbar^2}{2}\frac{d}{dx}\left(\frac{1}{m^*(x)}\frac{d\psi}{dx}\right) + [V(x) - E]\psi = 0 \tag{3.1}$$

where $m^*(x)$ is the electron effective mass, $\hbar$ is the reduced Planks constant, $\psi(x)$ is the envelop wave function, E is the energy of incident electron and $V(x)$ is the potential energy. Considering effective mass and potential is constant the solution of the Eq. 3.1 can be written in the following form:

$$\psi(x) = A^+[\exp(\gamma x) - \rho \exp(-\gamma x)] \tag{3.2}$$

where

$$\gamma = \alpha + j\beta = j\sqrt{\frac{2m^*(E - V(x))}{\hbar^2}} \tag{3.3}$$

is the propagation constant, ρ is the amplitude reflection coefficient. Here, the time variation is implicitly assumed to be as $\exp(-\frac{jEt}{\hbar})$. Differentiating Eq. 3.2 with respect to x and multiplying on both sides by a factor $\frac{\hbar}{jm^*}$:

$$\phi(x) = \frac{2\hbar}{jm^*}\frac{d\psi}{dx} = A^+ Z_o[\exp(\gamma x) + \rho\exp(-\gamma x)] \tag{3.4}$$

where

$$Z_o = \frac{2\gamma\hbar}{jm^*} \tag{3.5}$$

Khondker *et al.* [29] showed that $\psi(x)$ in Eq. 3.2 and $\phi(x)$ in Eq. 3.4 is analogous to the voltage $I(x)$ and current $V(x)$, respectively in a transmission line with distributed parameters. Z_o is regarded as characteristic impedance of a region and analogous to the characteristic impedance for the transmission line. The Quantum Mechanical Wave Impedance (QMWI), $Z(x)$ is defined [29] as

$$Z(x) = \frac{\phi(x)}{\psi(x)} = R(x) + jX(x) \tag{3.6}$$

where $R(x)$ and $X(x)$ are the real and imaginary parts of the impedance at any point. In order to evaluate $Z(x)$ as a function of distance x the potential energy profile is approximated as multistep functions with a sequence of N segments. Fig. 3.2 shows an arbitary potential profile. If the boundaries of rth segment are designated as x_r and x_{r+1}, the QMWI looking into positive x direction (right) at x_r, $Z_R(x_r)$ can be calculated as [29]

$$Z_R(x_r) = Z_o(r)\frac{Z_R(x_{r+1})cosh(\gamma_r l_r) - Z_o(r)sinh(\gamma_r l_r)}{Z_o(r)cosh(\gamma_r l_r) - Z_R(x_{r+1})sinh(\gamma_r l_r)} \tag{3.7}$$

where the propagation constant $\gamma_r = \alpha_r + j\beta_r = j\sqrt{(\frac{2m_r}{\hbar^2})(E - V_r)}$, $l_r = x_{r+1} - x_r$ and the characteristic impedance $Z_o(r) = \frac{2\hbar\gamma_r}{jm_r}$. Similarly, the QMWI looking in the negative x direction (left) at x_r, $Z_L(x_r)$ can be calculated by

$$Z_L(x_r) = Z_o(r-1)\frac{Z_L(x_{r-1})cosh(\gamma_{r-1}l_{r-1}) + Z_o(r-1)sinh(\gamma_{r-1}l_{r-1})}{Z_o(r-1)cosh(\gamma_{r-1}l_{r-1}) + Z_L(x_{r-1})sinh(\gamma_{r-1}l_{r-1})} \tag{3.8}$$

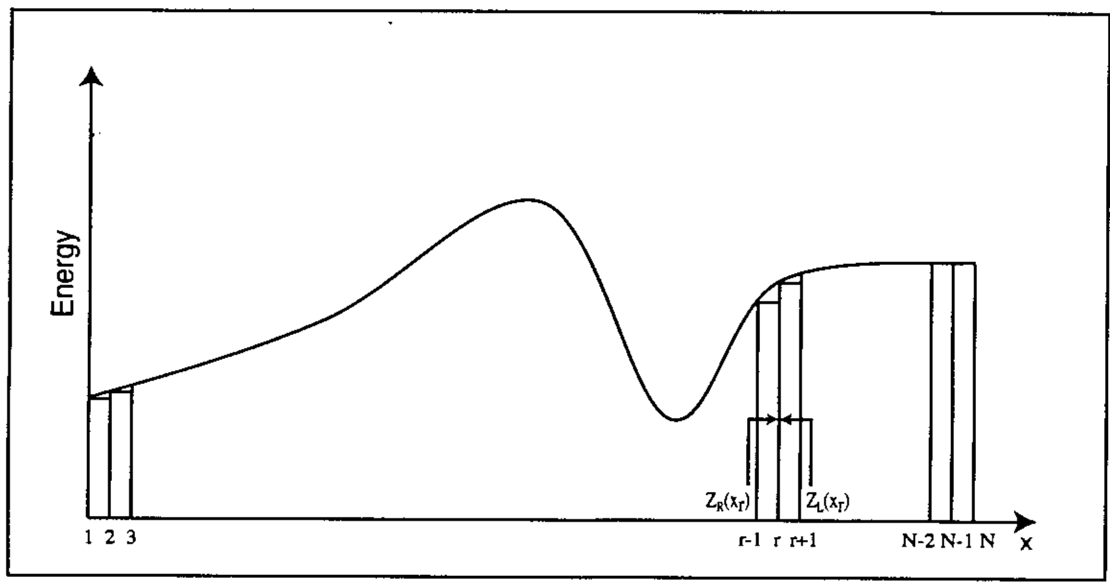


Figure 3.2: Potential profile illustrating the calculation of QMWI. The profile is approximated by N number of step functions.

The eigen energy state of the ith valley and jth sub-band (j=1,2,...) E_{ij} can be found by imposing the resonance condition for a non-leaky system

$$Z_r(E_{ij}) = Z_l(E_{ij}) \tag{3.9}$$

That is at eigen energy the QMWI looking through positive x (right) is equal to the QMWI looking through negative x (left) at any point x. When particles leak out from the system, the density-of-state (DOS) rather than being a delta function broadens in energy. Eigen energies for such leaky systems can be found by observing the peaks of the DOS. At any x and energy E the density-of-state $N(x;E)$ can be expressed as [30]

$$N(x;E) = \frac{4}{\pi\hbar}\Im m\left(\frac{i}{Z^+(x;E) - Z^-(x;E)}\right) \tag{3.10}$$

Once the eigen energy is found the sheet carrier density, N_{ij} is found by using the 2-D electron density of states and Fermi-Dirac Statistics [22]:

$$N_{ij} = \left(\frac{kT}{\pi\hbar^2}\right)n_{vi}m_{di}\ln\left(1 + \exp\left(\frac{E_F - E_{ij}}{kT}\right)\right) \tag{3.11}$$

where i=1,2, j=1,2,3,..., and n_{vi} is the degeneracy of the ith valley, m_{di} is the density of state effective mass per valley, and E_F is the Fermi energy.

The transmission line analogy can be extended to calculate normalized probability density function by employing Green's Function Formalism [30]. To find the probability density function a small amount of perturbation is introduced in the system by replacing the real potential $V(x)$ in Eq. 3.3 with a complex potential $V_{re} - j\epsilon$, ϵ being an small positive energy and V_{re} is the potential energy. Then the normalized probability density functions, $\mid \psi_{ij}(x) \mid^2$ at any eigen energy E_{ij} is expressed as:

$$\mid \psi_{ij}(x) \mid^2 = \frac{4\epsilon}{\hbar}\Im m(\frac{i}{Z^+(x; E_{ij}) - Z^-(x; E_{ij})}) \tag{3.12}$$

3.2 Current Density

The probability current density S is written as [41]

$$S = Re(\psi^* \frac{\hbar}{jm}\nabla\psi) = \frac{\hbar}{2jm^*}[\psi^*\nabla\psi - (\nabla\psi^*)\psi] \tag{3.13}$$

In one dimension

$$S = \frac{\hbar}{2jm^*}(\psi^*\frac{d\psi}{dx} - \frac{d\psi^*}{dx}\psi) \tag{3.14}$$

Using Eq. 3.4 S can be rewritten as

$$S = \frac{1}{2}Re[\phi\psi^*] \tag{3.15}$$

Then the current density J for a single electron:

$$J = qS = \frac{q}{2}Re[\phi\psi^*] \tag{3.16}$$

If a velocity, v_g is defined such that the current density is :

$$J = qv_g\mid \psi \mid^2 \tag{3.17}$$

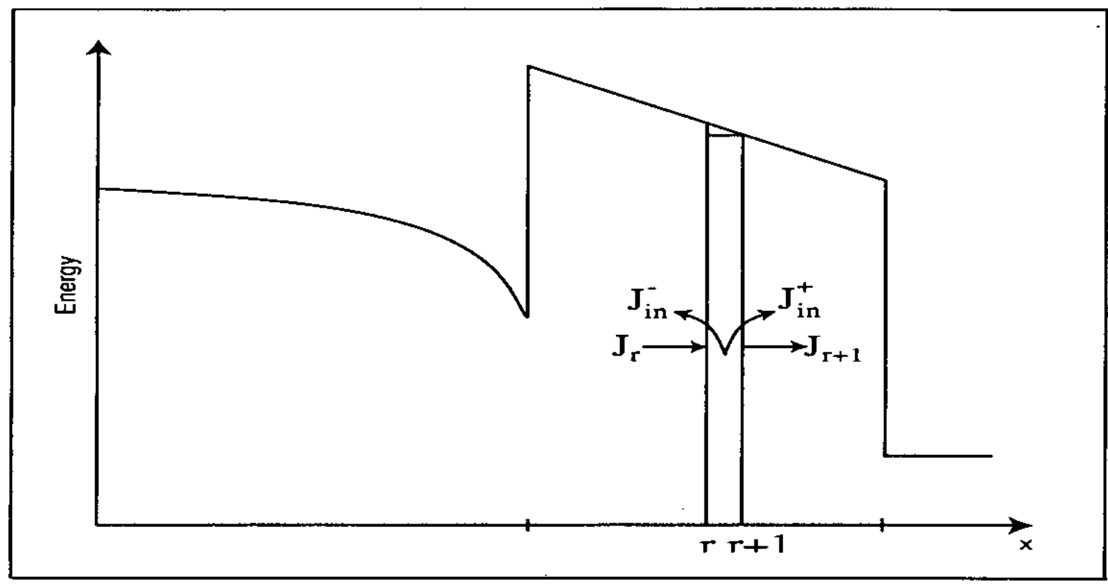


Figure 3.3: Illustrations for the calculation of current density

then it becomes similar to the group velocity given by Anwar *et al.* in Ref. [42] and expressed in terms of QMWI as

$$v_g = \frac{1}{2}Re[Z(x)] \tag{3.18}$$

and the current density J can be expressed using Eq. 3.17 and Eq. 3.31 as

$$J = \frac{q}{2}Re[Z(x)] \mid \psi \mid^2 \tag{3.19}$$

Let's consider the Fig. 3.3 where the potential energy profile is approximated by a multi step function. To get the spatial distribution of current along this potential let us differentiate Eq. 3.16 and use Eq. 3.4 within any segment r having boundaries x_r and x_{r+1}, assuming that within this rth segment the potential energy and effective mass are constant. Then

$$\frac{\delta J}{\delta x} = \frac{q}{2}Re[\frac{\delta \phi}{\delta x}\psi^* + \phi\frac{\delta \psi^*}{\delta x}] \tag{3.20}$$

Replacing $\delta\phi/\delta x$ and $\delta\psi^*/\delta x$ using the expression of $'\phi'$ from Eq. 3.4 the $\delta J/\delta x$ can be written as

$$\frac{\delta J}{\delta x} = \frac{q}{2}(Re[\frac{2\hbar\gamma^2}{jm^*}\psi\psi^*] + Re[\frac{-jm^*}{2\hbar}\phi^*\phi]) \tag{3.21}$$

$\phi^*\phi$ is a real quantity so the second term is imaginary and can be excluded from the above expression. Putting the expression of $'\gamma'$ from Eq. 3.3

$$\begin{aligned}\frac{\delta J}{\delta x} &= \frac{q}{2}Re[\frac{2\hbar(\alpha+j\beta)^2}{jm^*} \mid \psi \mid^2] \\ &= \frac{q}{2}Re[\frac{2\hbar(\alpha^2-\beta^2+j2\alpha\beta)}{jm^*} \mid \psi \mid^2] \\ &= \frac{2q\alpha\beta\hbar \mid \psi \mid^2}{m^*}\end{aligned}$$

using the value of $\mid \psi \mid^2$ from Eq. 3.19 $\frac{\delta J}{\delta x}$ can be written as

$$\frac{\delta J}{\delta x} = \frac{4\alpha\beta\hbar}{m^* Re[Z(x)]}J \tag{3.22}$$

When potential energy V is real the propagation constant γ can be only real or imaginary depending in the electron energy as seen from Eq. 3.3. That is either β or α is zero. In such cases as seen from the Eq. 3.22 the rate of change of current density with respect to distance is zero.

If the current density at x_r boundary is J_r, current density at x_{r+1} boundary is J_{r+1} and $Re[Z(x)]$ is a slowly varying function of x, and assuming Δx to be small then solving Eq. 3.22 the current density, J_{r+1} is found as

$$J_{r+1} = J_r \exp(\frac{4\alpha_r\beta_r\hbar}{m_r^* Re[Z_r^+]}\Delta x_r) \tag{3.23}$$

where the subscripts indicate the corresponding edges, $\Delta x_r = x_{r+1} - x_r$ and Z_r^+ refers to the QMWI looking towards positive x direction at rth edge. This equation allows us to get the current density iteratively at any x if the current density at a point $x = x_o$ is known.

3.3 Calculation of Incoherent Current

When scattering is present in a system it interrupts the ballistic motion of electrons. In most cases the scattering can be visualized as disappearing from any given state and instantaneous reappearing of electrons in different phase space.

Scattering causes the incident wave to decay and introduces a phase shift to the incident wave. To incorporate such effects of scattering the scattering processes are included in a single channel formalism by viewing this processes as "absorbing" particle from incident beam, with the absorption being described by a complex potential $V(x) = V_r(x) - iV_i(x)$ instead of the real potential in the Schrödinger's equation (Eq. 3.1). The imaginary potential V_i is related to the particle scattering lifetime, τ as $iV_i = i\hbar/2\tau$ [28]. The incorporation of an imaginary potential V_i breaks the phase coherence as seen from the Eq. 3.3 and the product $\alpha\beta$ will be negative in Eq. 3.23. The consequence of this is that the current at rth boundary (Fig. 3.3) will be less than that at the $(r+1)$th boundary. Thus scattering essentially results in dissipation of coherent current and Eq. 3.23 alone cannot satisfy the current continuity anymore. To satisfy the current continuity the contribution of the incoherent current has to be found, in addition to the contribution of coherent current described by Eq. 3.23.

To find the incoherent part the loss of coherent current has to be found first, that is ΔJ_r (subscript indicating the corresponding segment), which is

$$\Delta J_r = J_r - J_{r+1} \tag{3.24}$$

This loss of coherent current ΔJ_r corresponds to the generation of incoherent current at rth segment. The incoherent current has probability of being scattered to both left or right as shown in Fig. 3.3. ΔJ_r can be written as the sum of the incoherent current scattered to left or right.

$$\Delta J_r = J_{in}^+ + J_{in}^- \tag{3.25}$$

where J_{in}^+ represents incoherent current in the positive x direction (right) and J_{in}^- is the incoherent current in the negative x direction (left). Khondker and Alam [43] showed that the ratio of electrons being scattered in to left or right is determined by the respective local group velocities. That is

$$\frac{J_{in}^+}{J_{in}^-} = \frac{v_g^+}{v_g^-} = \frac{Re[Z^+]}{Re[Z^-]} \tag{3.26}$$

v_g^+ and v_g^- being the group velocities towards positive x or negative x direction respectively. Combination of Eq. 3.25 and Eq. 3.26 gives

$$J_{in}^+ = \frac{Re[Z^+]}{Re[Z^+] + Re[Z^-]} \Delta J_r \tag{3.27}$$

$$J_{in}^- = \frac{Re[Z^-]}{Re[Z^+] + Re[Z^-]} \Delta J_r \tag{3.28}$$

The current continuity is now satisfied for the rth segment as the current density at rth interface is equal to that at $(r+1)$th interface (Fig. 3.3) i.e.

$$J_r - J_{in}^- = J_{r+1} + J_{in}^+ \tag{3.29}$$

3.4 Calculation of the Gate tunneling Current

Above formalism is applied in calculating the tunneling current in MOSFET as follows. First the current density at oxide-semiconductor interface, J_1 is found by using Eq. 3.19. Then assuming constant effective mass in the oxide and approximating the oxide conduction band profile by $'n'$ segment multistep function the coherent current at metal-oxide interface, J_n can be obtained using Eq. 3.23 iteratively. The total current density is equal to the sum of coherent current at metal-oxide interface(J_n) and the contribution from incoherent current towards left from all the oxide segments assuming that one electron encounters scattering only once in its journey towards gate. This assumption, i.e. neglecting secondary scattering is reasonable for thin devices where device dimensions are approaching near mean free scattering path of electrons. Then for the sheet concentration of jth subband N_{ij} (Eq. 3.11) the current density arising from that subband is:

$$J_j = \{J_n + \sum_{r=1}^{n} J_{in}^+\} N_{ij} \tag{3.30}$$

where J_j is the gate current contributed by the electron of jth subband. The total gate current, J_T is found by summing up the contribution from all subbands ($\sum J_j$) as a function of gate voltage that follows the voltage balance equation:

$$V_g = V_{FB} + V_{ox} + \phi_s \tag{3.31}$$

where V_{FB} is the flat band voltage (Eq. 2.1), $V_{ox} = F_{ox}t_{ox}$ is the voltage drop across the oxide and ϕ_s is the substrate band bending. The electric field F_{ox} is related to substrate electric field via Gauss Law. If polysilicon is used rather than metal as gate electrode polysilicon depletion effect is included by adding V_{poly}, voltage drop due to polysilicon in the right side of the above equation.

Chapter 4

Results

In this chapter the results of the simulation based on the formalism discussed in previous chapter is presented. After describing simulated MOS structure the quantum mechanical calculation in the inversion layer is presented here. Then gate current with and without scattering is presented. A comparison of the simulated and measured [8, 11] gate current is made to check the validity of the model. The simulations are done using MATLAB.

4.1 Simulated potential profile

In this section a description of the simulated one-dimensional (1-D) Si-SiO_2 MOS system and the assumptions and approximations used are described. All simulation are performed for $\langle 111 \rangle$ Si substrate. SiO_2 with dielectric constant of 3.9 and a uniformly doped silicon substrate with a dielectric constant of 11.8 are assumed. The electron effective masses used for Si are that given by Stern [22] for $\{111\}$ surface i.e. normal effective mass, $m^* = 0.258m_o$ and density of state effective mass, $m_{di} = 0.358m_o$ where m_o is the free-electron mass. All calculations are done for room temperature (T=300K).

The MOS potential profile in the substrate at inversion is taken as an exponential function of the form:

$$\phi(x) = A[1 - \exp(-Bx)] \tag{4.1}$$

where $\phi(x)$ is substrate band bending along depth x,A and B are constants. The boundary conditions that Eq. 4.1 has to satisfy are

$$at \quad x = 0, \quad \phi(x) = \phi_s \tag{4.2}$$

$$at \quad x = 0, \quad \frac{d}{dx}\phi(x) = F_s \tag{4.3}$$

where ϕ_s is the band bending at the interface as appeared in Eq. 3.31 and F_s is the substrate electric field. Due to quantum mechanical effects the relation between substrate band bending and substrate electric field differs significantly from the classical relation, in the inversion regime [11]. Here an empirical equation [44] is used to relate ϕ_s and F_s that matches the result of Ref. [11].

$$F_s = C\phi_s^5 \tag{4.4}$$

the constant C is found from employing the conditions at the onset of strong inversion. At the onset of strong inversion the total substrate band bending is twice the difference between Fermi level and intrinsic Fermi level, (Eq. 2.2). The substrate electric field is given by [22]

$$F_s = q(N_{inv} + N_{depl})/\varepsilon_{Si}\varepsilon_o \tag{4.5}$$

where N_{depl} is the total number of charges per unit area in the depletion region and is given as $N_{depl} = \sqrt{2\varepsilon_{Si}\varepsilon_o\phi_s N_A/q}$ where ε_{Si} is the relative permittivity of silicon and ε_o permittivity of free space. $N_{inv} = \sum N_j$ is the total inversion layer charge and is negligible at the onset of strong inversion. As 111-Si has six identical valleys the subscript i is excluded from the symbol N_{ij} (Eq. 3.11) from here on.

Fig. 4.1 shows the MOS potential for two different gate voltages (V_G) obtained using above relations for the oxide thickness, $t_{OX} = 20A^o$. The band bending at the interface is obviously dependent on substrate doping concentration, which is implicit in the constant 'C' in the Eq. 4.4. Fig. 4.2 shows the dependency

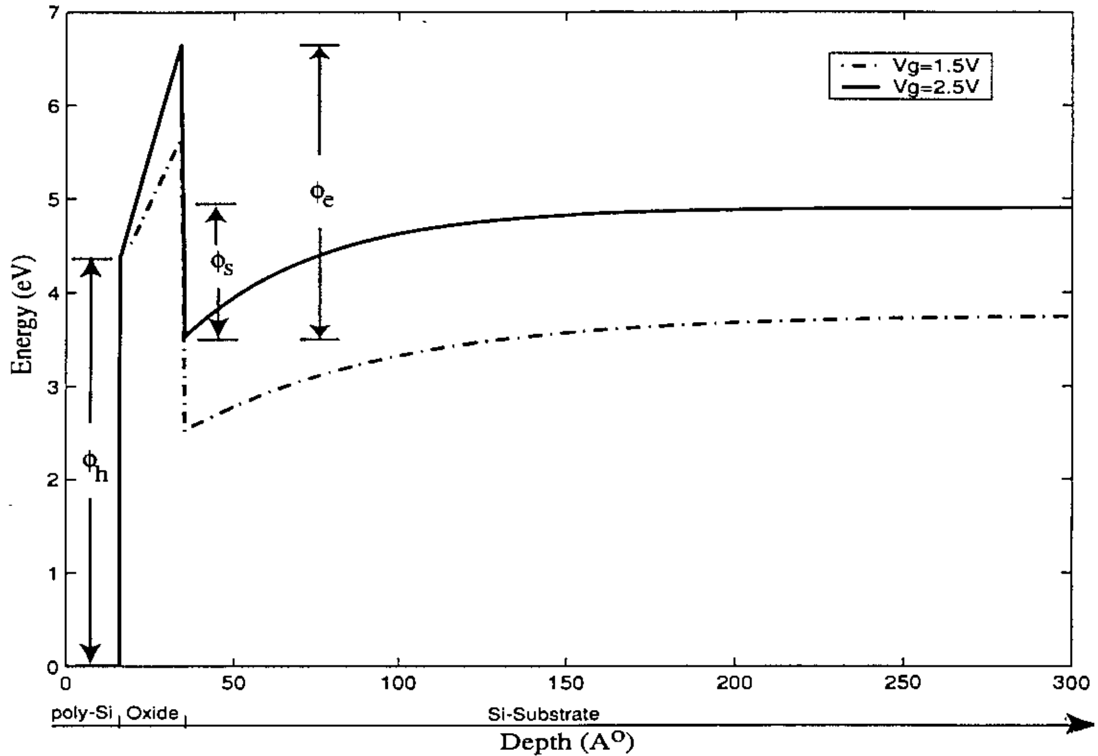


Figure 4.1: MOS profile at different gate bias. Oxide thickness is $20A^o$and substrate doping is 5x10[17] cm^{-3}

of ϕ_s on acceptor doping concentration, N_A. With the increase in the acceptor concentration the band bending decreases for the same gate bias.

The value of barrier height due to conduction band discontinuity differs in literature. The oxide barrier from the substrate (ϕ_e in Fig. 4.1) ranges between $2.3eV$ and $5eV$ [45]. Value of this parameter taken here is $3.15eV$ [11, 24]. Due to amorphous nature the band gap of SiO_2 and polysilicon is not precise. Band gap of SiO_2 varies between $9eV$ and $10eV$ and band gap of polysilicon varies between $1.5eV$ and $1.8eV$. This causes the oxide barrier height at gate-edge, ϕ_h to vary between $4eV$ and $6eV$. For the present calculation it is assumed to be equal to $4.15eV$. The effect of classical image force is neglected as the image potential rounds the top of the barrier only and hardly alters the tunneling distance [23].

The use of doped polysilicon as gate electrode introduces thin space charge

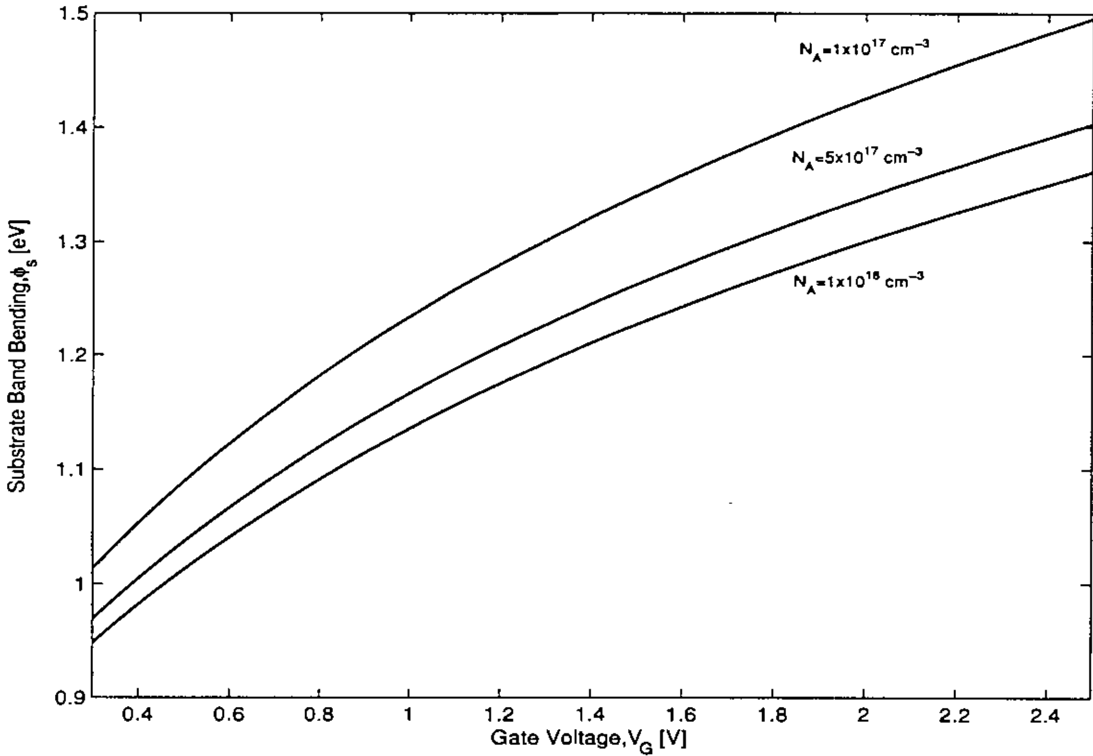


Figure 4.2: Variation of total band bending at Si/SiO_2 interface with substrate doping. Oxide thickness is $20A^o$.

layer near the gate oxide interface which acts to retard the applied field. Effect of this layer is termed as polysilicon depletion effect. The depletion effects is treated generally as thickening of the effective oxide thickness by a constant amount [46]. But the width of poly-depletion layer depends on the applied electric field and so it's effect is greatly overestimated when treated as an equivalent oxide layer [47]. Also the small signal MOS capacitance measurements give overestimated picture of the severeness of the poly-depletion effects [47]. Considering these facts the polysilicon depletion effect is considered negligible in this work.

Despite the importance of $E - k$ relation in the oxide for modeling the electron tunneling through the oxide, experiments or calculations of band dispersion is virtually nonexistent. Over the years two types of dispersion relations are used [23] : the parabolic dispersion [23, 9] and Franz-type [8, 11] dispersion. In

this work a parabolic $E-k$ relation in the oxide is assumed. The effective mass of electron in oxide depends on the growth and material condition of the amorphous oxide layer. The values adopted by various researchers lie between $0.25m_o$ and $1.03m_o$ [23, 48]. It is taken to be $0.65m_o$ here.

4.2 Quantum mechanical calculations for the Si substrate

Eigenstates

In Fig. 4.3 the variation of eigen energies or subbands with applied bias is shown. The figure shows first three eigen states. As the gate bias is increased the substrate potential profile becomes steeper (Fig. 4.1) so carriers are confined to a

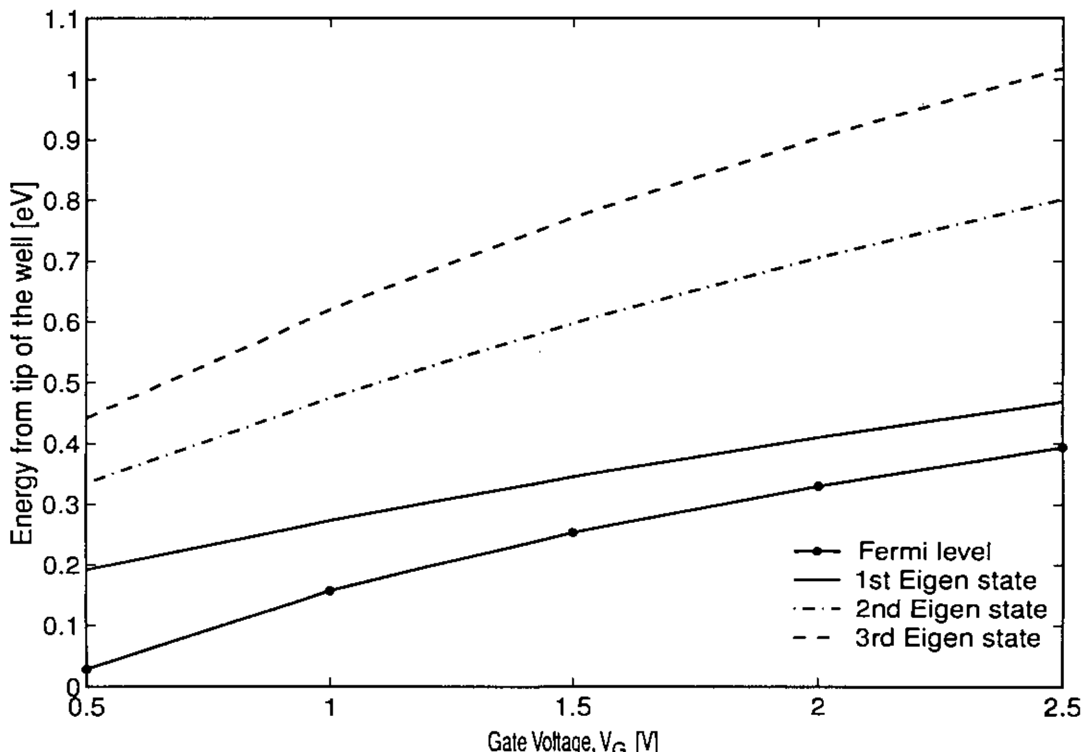


Figure 4.3: Variation of Fermi level and the three lowest subband energy levels for electrons in the inversion layer with gate bias. Oxide thickness is $20A^o$and substrate doping is 5x10[17] cm^{-3}

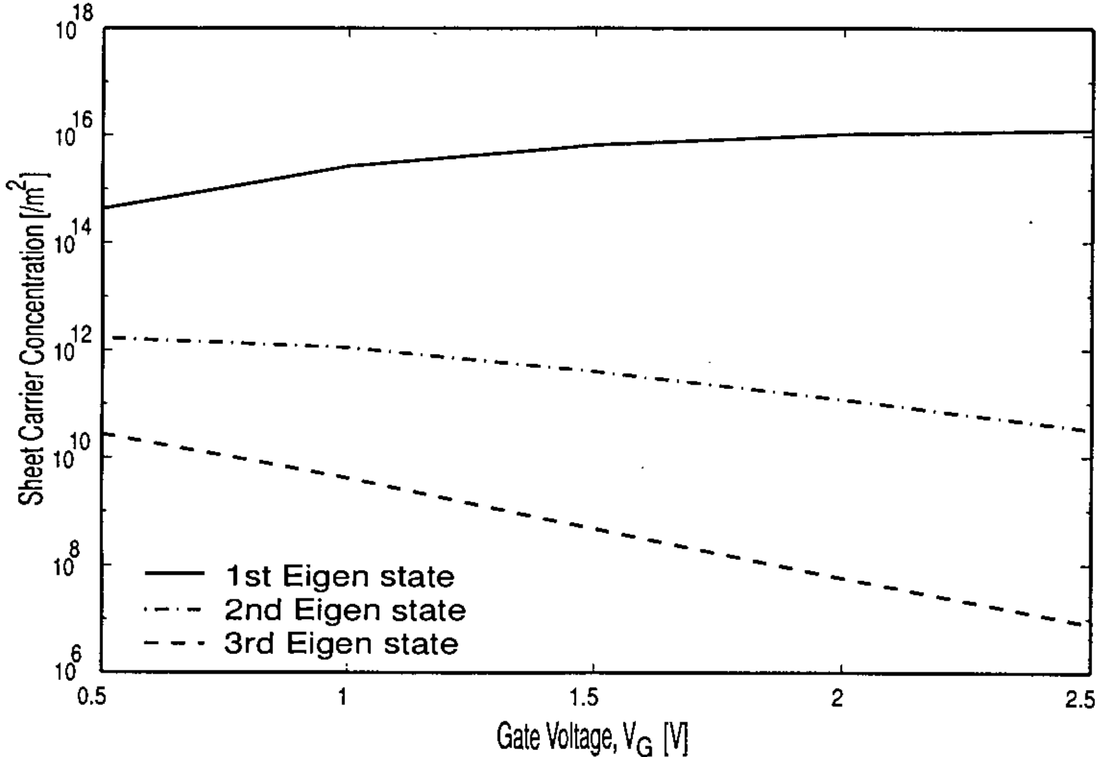


Figure 4.4: Sheet carrier density for the three lowest subbands and their variation with gate bias. Oxide thickness is $20A^o$.

narrower well. So, the eigen energies measured from the tip of the potential well increases with the increased bias (Fig. 4.3). As the bias is increased the difference between successive eigen states also increases.

Carrier Concentration

The inversion sheet carrier density calculated using Eq. 3.11 for the first three eigen states is shown in Fig 4.4. With the increase of applied bias the concentration increases for the first eigen state and decreases for the two upper eigen states. This is evident, that the difference between the upper two eigen states and Fermi energy increases with gate bias whereas the difference between first eigen state and Fermi energy decreases (Fig. 4.3). The large difference between the concentrations at first subband and that at the second or third subband reveals that as far as carrier concentration is concerned only the lowest subband can be used

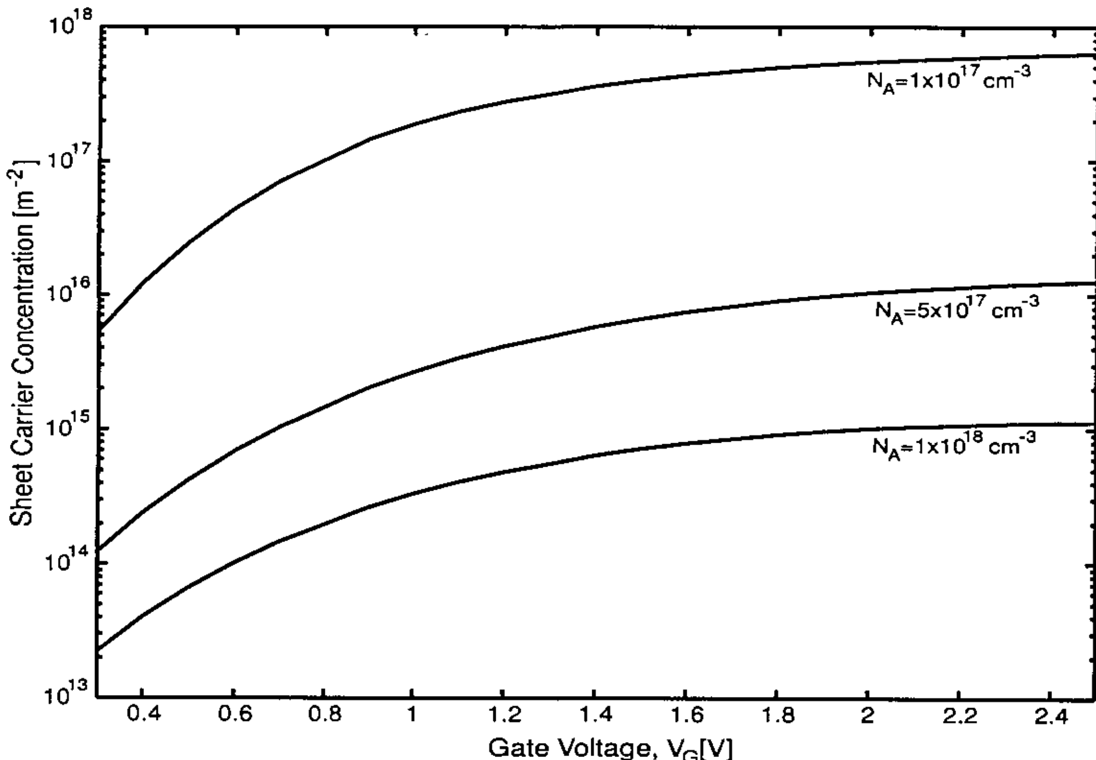


Figure 4.5: Sheet carrier density at different substrate doping concentration. Oxide thickness is $20A^o$.

with reasonable accuracy, and is done so in this work. Fig. 4.5 shows sheet carrier density at different acceptor doping concentration. With the increase in acceptor doping concentration the electron density decreases nonlinearly in the inversion regime when bias is constant. This is because, increased doping increases threshold voltage and decreases band bending for the same gate voltage(Fig. 4.2). So more voltage is required to induce same amount of inversion layer charge.

Probability Density function

Fig. 4.6 shows normalized probability density functions at the lowest three subbands. The probability density functions are calculated employing equation 3.12. The advantage of using this equation is that it is derived using asymptotic boundary conditions [30] rather than the conventional boundary condition [49]. In conventional boundary conditions it is assumed that wave function does not penetrate

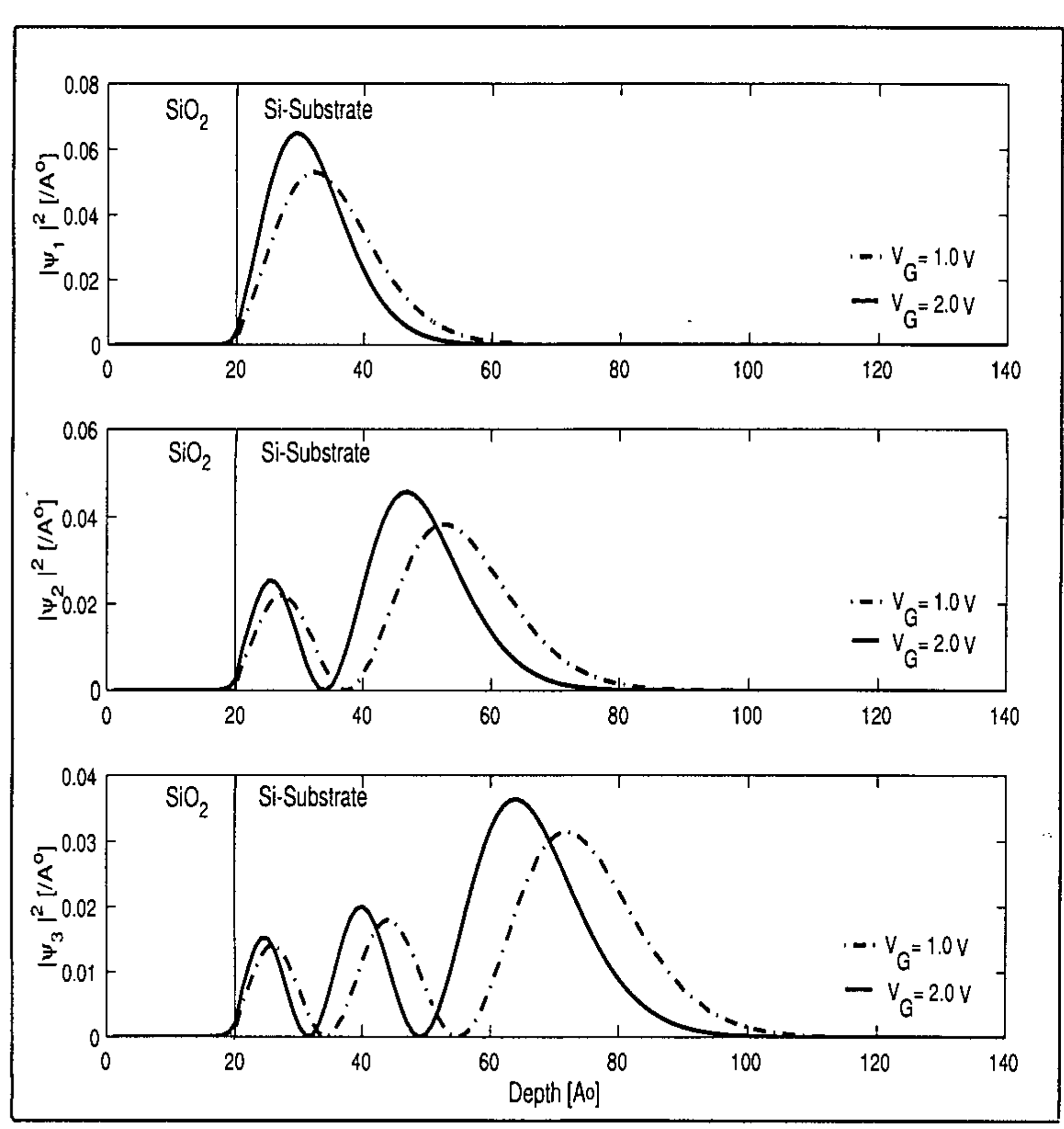


Figure 4.6: Normalized probability density function , $|\psi_j|^2$ at jth subband. Oxide thickness is $20A^o$ and substrate doping density is 5x10^{17} cm^{-3}.

the oxide whereas asymptotic boundary conditions do not impose such conditions and thus allow us to get the exponentially decaying probability density function in the oxide. In all three subbands the peak of the probability density function shifted towards the Si/SiO_2 boundary with increased applied bias.

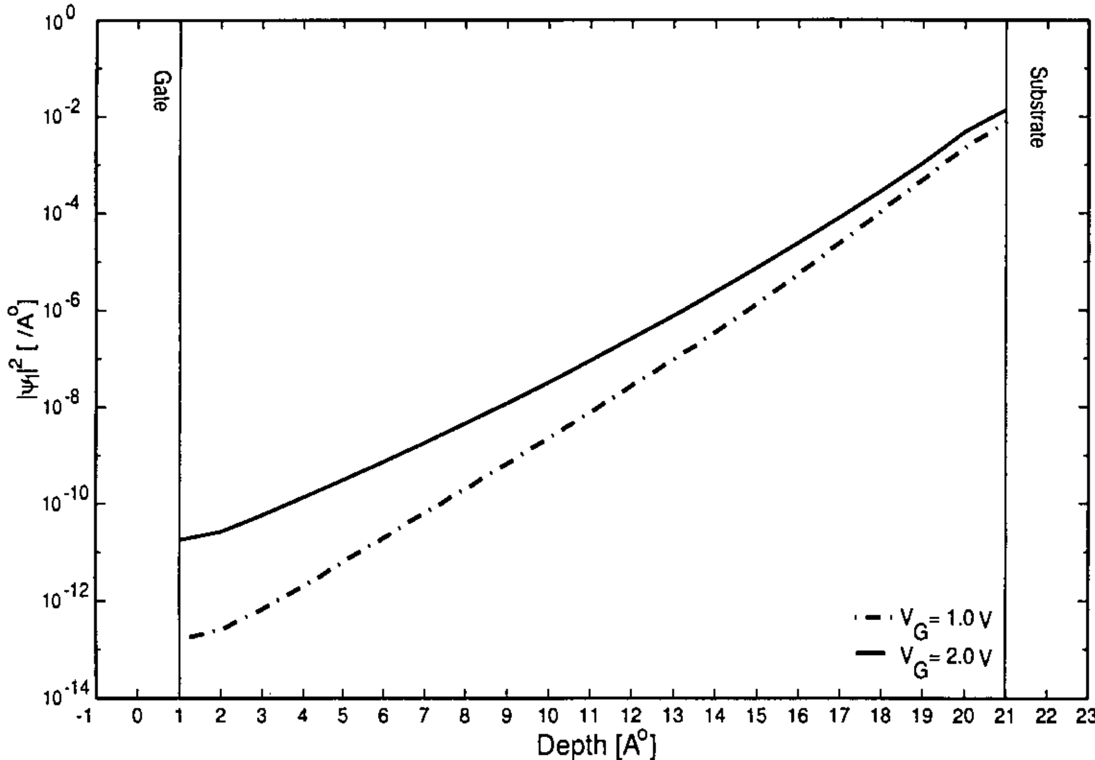


Figure 4.7: Normalized probability density function inside the oxide. Oxide thickness is $20A^o$ and substrate acceptor doping density is 5x10^{17} cm^{-3}.

As the bias is increased the substrate potential profile gets steeper and motion of electron is more restricted. So the probability density function gets confined to a smaller width and its peak increases as the bias is increased. In side the oxide the probability density function is calculated using an iterative approach and is shown in Fig. 4.7. First, the wave function at Si/SiO_2 interface is calculated employing Eq. 3.12 then current density distribution is iteratively calculated using Eq. 3.23 throughout the oxide and from this current density wave function distribution inside the oxide is obtain by Eq. 3.19. The probability density function

decays exponentially inside the oxide and has significant values within the first few angstroms from the oxide/substrate interface.

4.3 The gate current without scattering

When scattering effect is not considered the gate current is mainly the result of substrate conduction band to gate conduction band electron tunneling. The current is coherent in nature and does not vary spatially within the oxide. Also within the oxide thickness range considered in this work, the gate current is in the direct tunneling regime. In this section the sensitivity of the gate leakage current, without any scattering effect (the coherent current), on the device parameters such as substrate doping concentration and oxide thickness is examined.

Variation with substrate doping density

With increased doping the threshold voltage increases (Eq. 2.3) decreasing the band bending (Fig. 4.2). This means that the difference between Fermi level and the lowest subband ($E_F - E_1$) increases and the difference between the tip of the well and the lowest subband decreases. These results in lower sheet carrier concentration (Fig. 4.5) and lower carrier energy (with respect to barrier) reducing tunneling probability.

Fig. 4.8 shows the variation of coherent gate current with gate voltage at different substrate doping. Five times increase in the gate voltage increases the current around five orders of magnitude.

Variation with oxide thickness

Fig. 4.9 shows the variation of coherent gate current at different oxide thickness. Increase in the oxide thickness decreases the gate current in an exponential manner. With the decrease in oxide thickness the threshold voltage (Eq. 2.3) decreases linearly increasing substrate band bending. As the substrate band bending in-

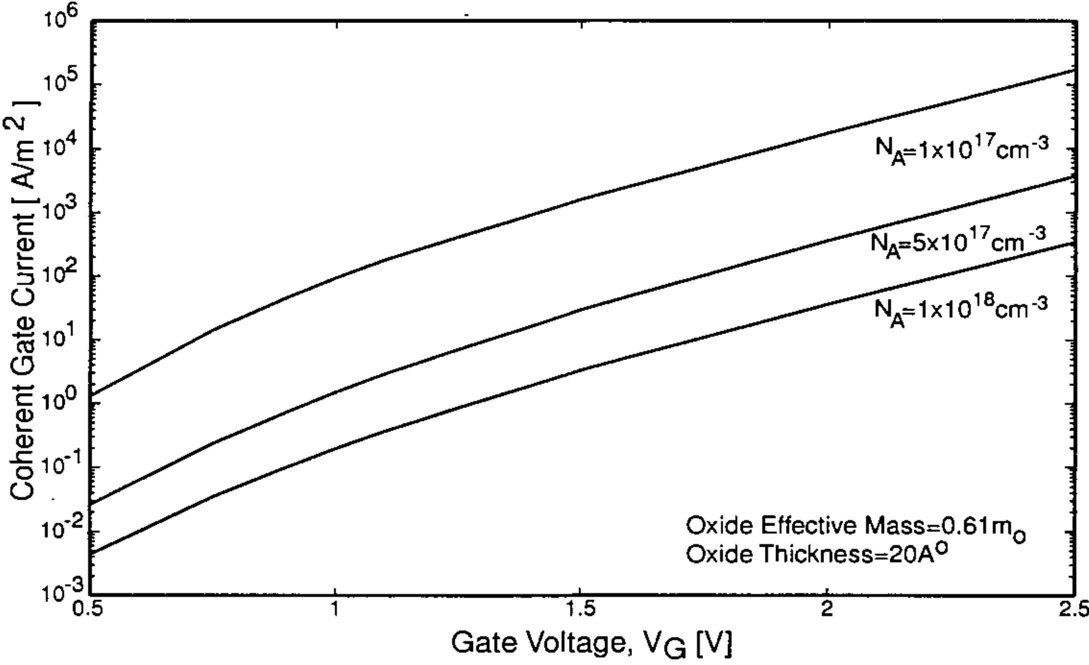


Figure 4.8: Variation of coherent gate current with applied gate voltage at different substrate doping concentration

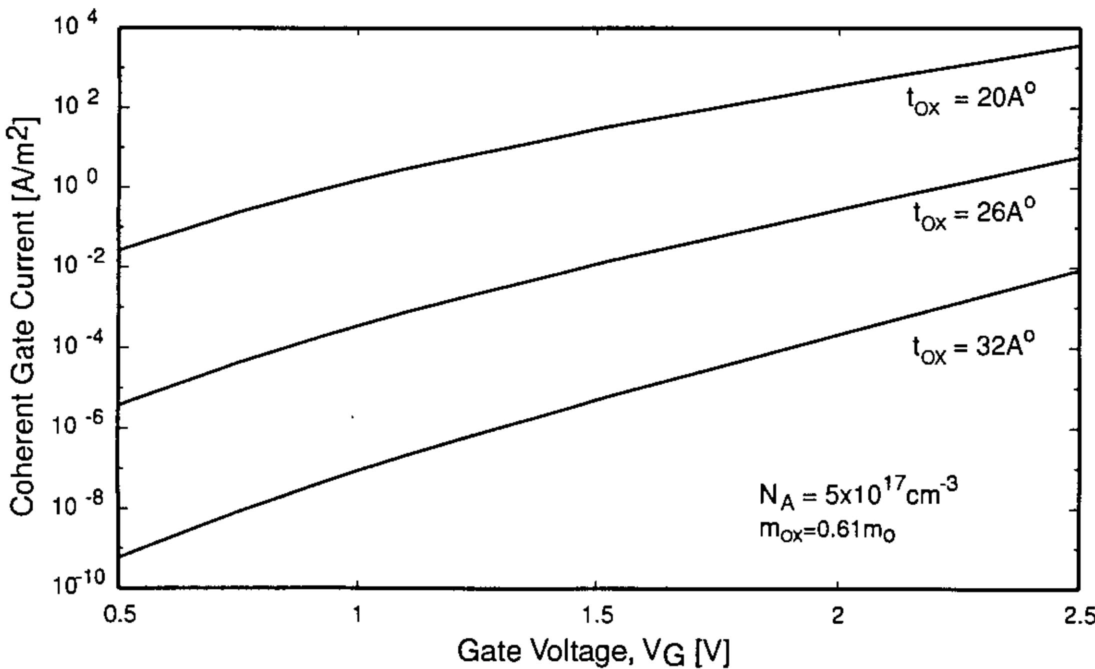


Figure 4.9: Variation of coherent gate current with applied gate voltage at different oxide thickness

creases, the energy difference between Fermi level and subbands decreases which increases the inversion layer charge concentration. So, with the thin oxides, there are more carriers available for tunneling. With reduced thickness the probability of tunneling through the the oxide is also increased.

The curves for thicker oxides are steeper than that for thinner oxides. This indicates that the coherent current becomes less sensitive to applied bias as the oxide thickness decreases.

4.4 The gate current with scattering

The effect of scattering is, as discussed earlier, included in this work by introducing an imaginary potential term in the Schrödinger's equation. In this section the effect of scattering on gate current at different oxide thickness and the effect of different scattering profile on gate current is examined.

Constant imaginary potential term represents uniformly distributed scattering centers throughout the oxide. Fig. 4.10 shows gate current in presence of uniform scatterers throughout the oxide. The curves show gate currents for no scattering ($V_i = 0eV$), medium scattering ($V_i = 6\text{x}10^{-9}$ or $\tau = 54.85ns$) and strong scattering ($V_i = 6\text{x}10^{-7}$ or $\tau = 0.5485ns$). The variation of coherent currents in presence of scattering is also shown. When scattering is present the barrier becomes more transparent resulting in an increase in tunneling current in the Si/SiO_2 edge (Fig. 4.11) and so there is an increase in total current at gate edge at all gate voltages in presence of scattering. But coherent current encounters scattering through out its journey towards metal edge and some part of its lose coherency. This reduced coherent component of gate current may be greater or smaller than the gate current without scattering depending on the scattering strength, oxide thickness and applied voltage. This is seen from the Fig. 4.11 also. In this figure the distribution of coherent current inside the oxide is shown. When there is no scattering the coherent current does not face attenuation and

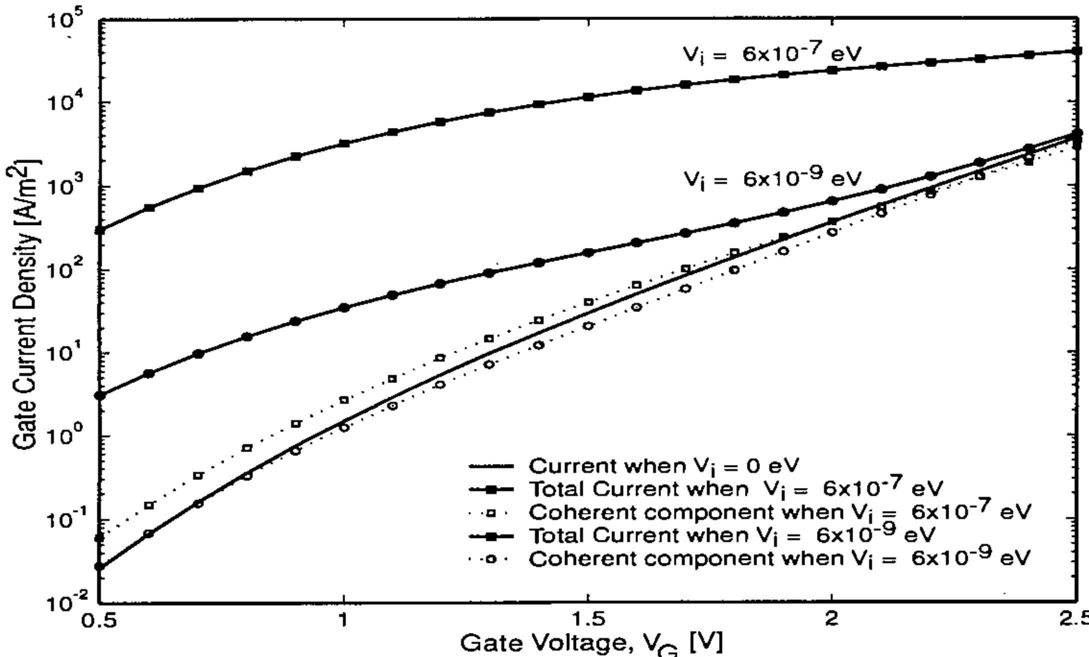


Figure 4.10: Variation of gate current with gate voltage for different scattering strength. The coherent component of the current in the presence of scattering is also shown. Oxide thickness is $20A^{o}$ and substrate acceptor doping is $5x10^{17}$ cm^{-3}.

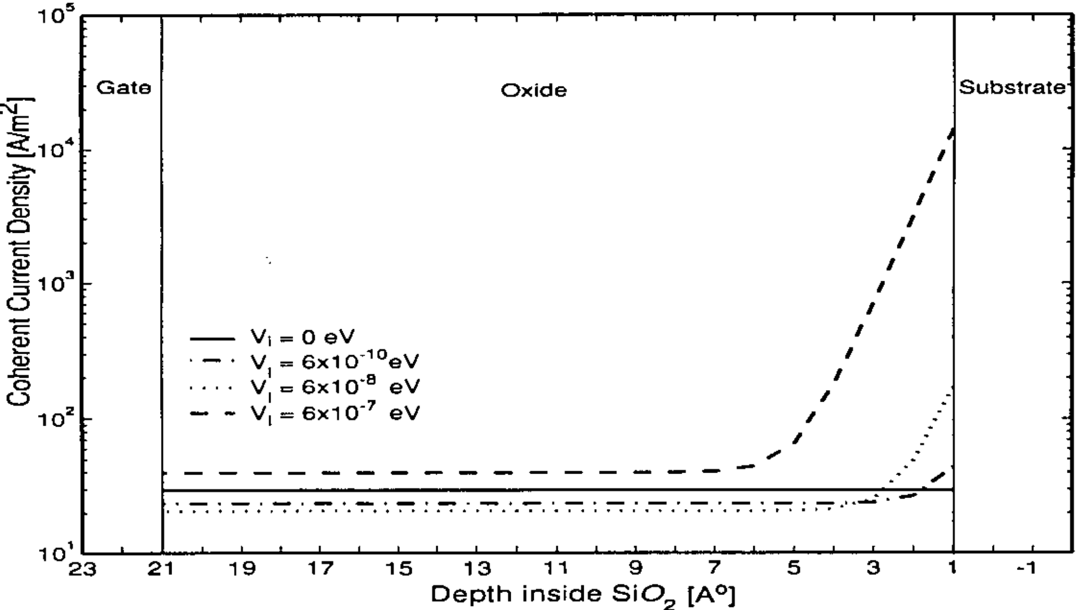


Figure 4.11: Dependency of coherent current profile inside the oxide on scattering strength. Applied gate bias is $2V$ and substrate acceptor doping is $5x10^{17}$ cm^{-3}.

remains constant throughout the oxide. But with scattering, the coherent current decreases exponentially and the rate of decrease is proportional to the scattering strength. Another feature of this figure (Fig. 4.11) is that there is almost no effect of scattering on coherent current near 10 to 15 A^o of the gate edge . This is because, near gate edge the group velocity of electron is high enough to avoid scattering and electron transport becomes ballistic.

When the scattering is strong, the total current profile becomes less sensitive with increasing voltage (Fig. 4.10). When there is no scattering increase in gate voltage decreases the tunneling barrier height (the difference between the Si/SiO_2 barrier and the first subband) so there is an exponential increase in tunneling probability. But with strong scattering the barrier is so leaky that contribution in tunneling from increased gate voltage i.e. reduced tunneling barrier height is little. That is why the current profile with scattering looks flattened. With medium scattering, slope of the gate current profile increases at high gate voltage. At such strength the coherent current dominates under high gate voltages and the profile of total current takes the shape of the profile of coherent current.

Fig. 4.12 shows gate current at different oxide thickness with $V_i = 1.5\text{x}10^{-8}eV$. Though at $20A^o$ oxide thickness, the curves for simulated and measured data are in close proximity, the difference between the simulated and the measured gate current becomes large as the oxide become thicker ($32A^o$). So a constant imaginary potential representing uniform scattering distribution through out the oxide is no longer acceptable. Fig. 4.13 shows gate current for $20A^o$ and $32A^o$ thick oxides assuming a non-uniform potential distribution. The distribution is assumed to be decreasing exponentially from the Si/SiO_2 interface, a scattering distribution reported by hot hole injection measurements [26]. Best possible match is obtained when $V_i = 1.5\text{x}10^{-8}\exp(-vx)$, x being the distance inside the oxide in meter measured from Si/SiO_2 interface and constant, v=1x10^{11}. Though the difference between measured and simulated gate current for $32.2A^o$ thick oxide

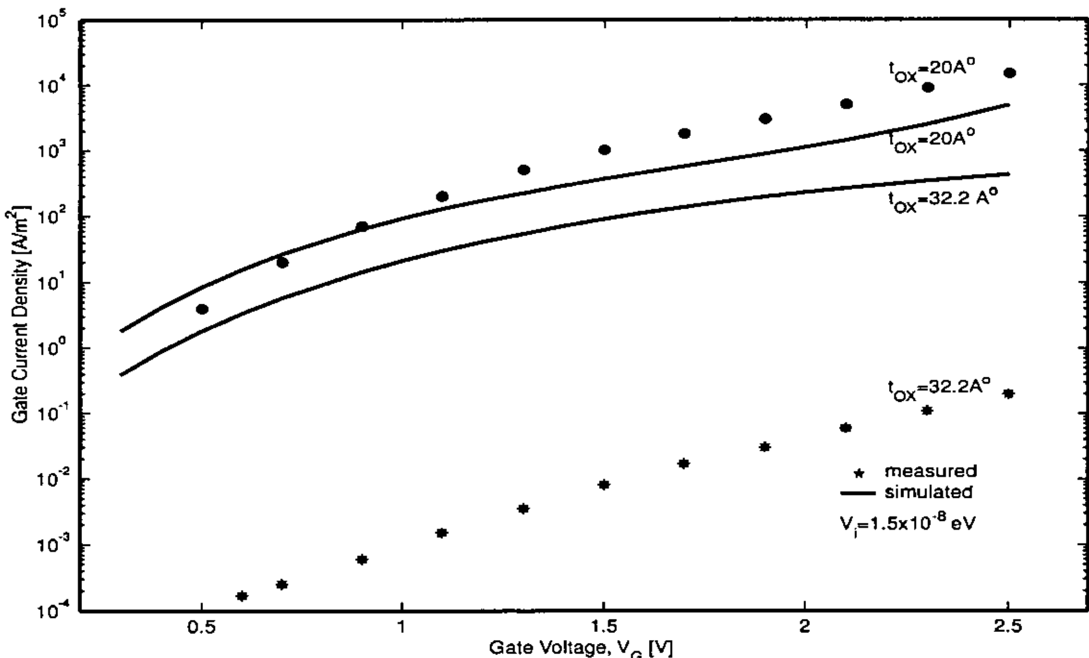


Figure 4.12: Variation of gate current with gate voltage at two different oxide thickness with the same scattering strength. N_A=5x10^{17} cm^{-3}.

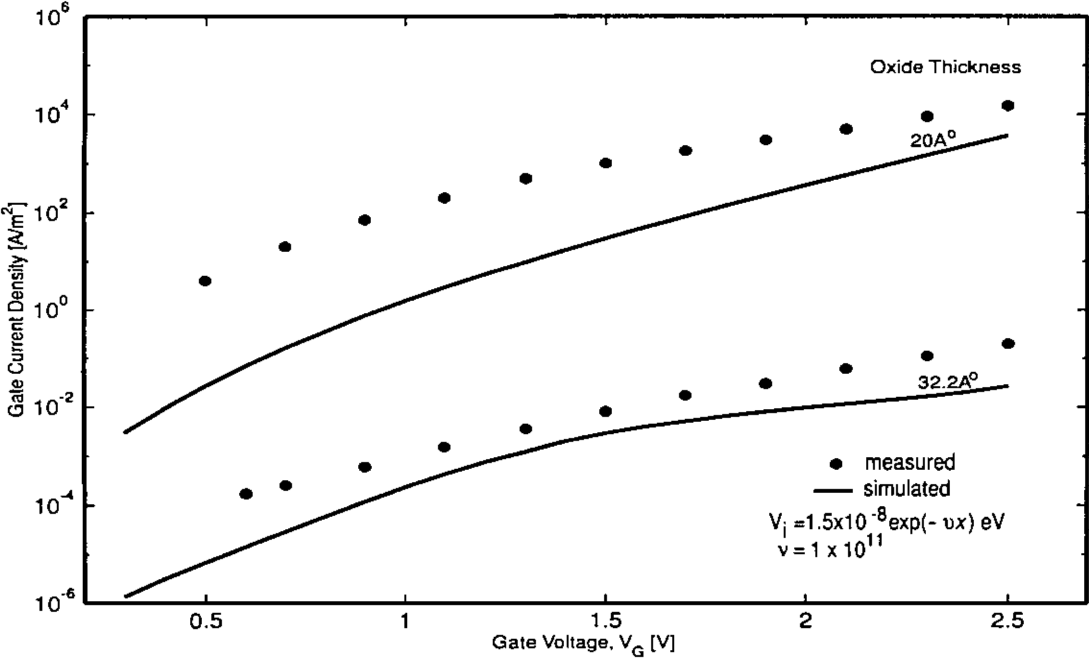


Figure 4.13: Variation of gate current with gate voltage at different oxide thickness assuming trap distribution with a peak at Si/SiO_2 interface. N_A=5x10^{17} cm^{-3}.

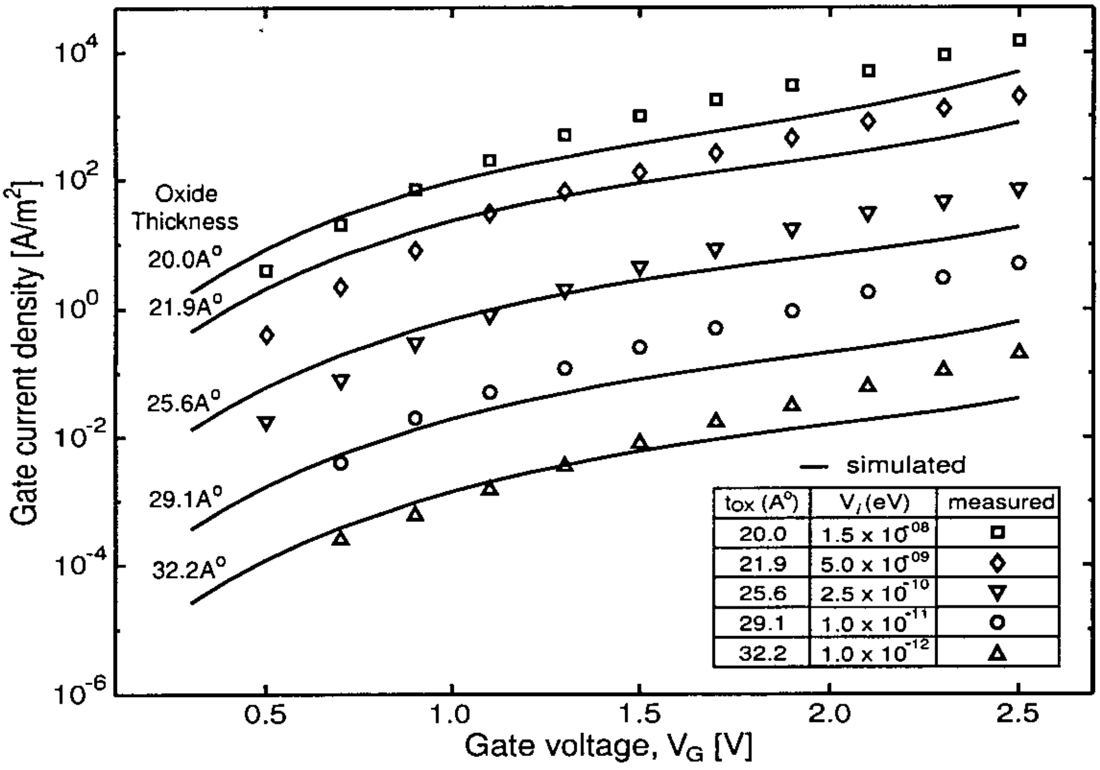


Figure 4.14: Variation of gate current with gate voltage at different oxide thickness with uniform scattering strength. The scattering strength is dependent on oxide thickness. Substrate acceptor doping is 5x10^{17} cm^{-3}.

is decreased, the slope of the simulated curves never follows the experimental curves.

Fig. 4.14 shows simulated and measured gate current for five different oxide thickness. Here the scattering strength is taken uniform for a particular device but dependent on oxide thickness. The outcome is a better match between simulated and measured data over a small gate voltage range. For all the oxide thickness at lower voltages the simulated current is greater than the measured one and at higher voltages the simulated current is smaller than the measured current. This indicates an applied voltage dependent distribution of scatterers inside the oxide.

Fig. 4.15 the simulated current and the scattering distribution is considered to be applied voltage dependent parameter. For any given gate voltage, the distribution is assumed to be uniform throughout the oxide layer. Here $V_i = \nu V_G$,

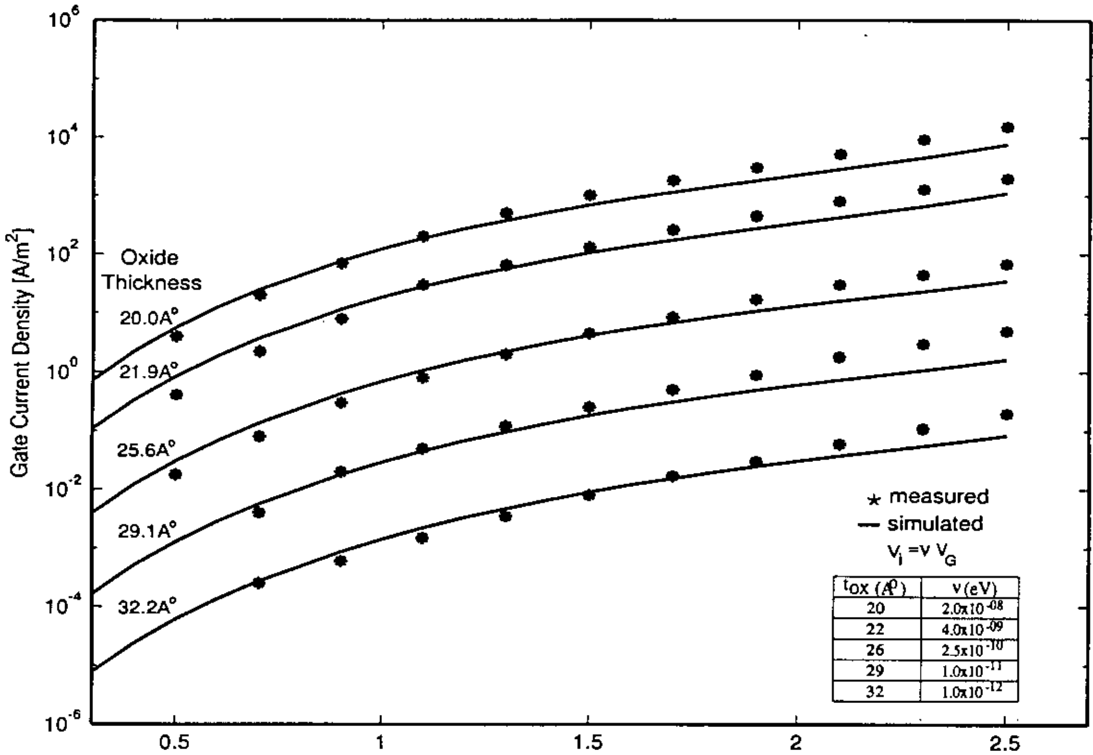
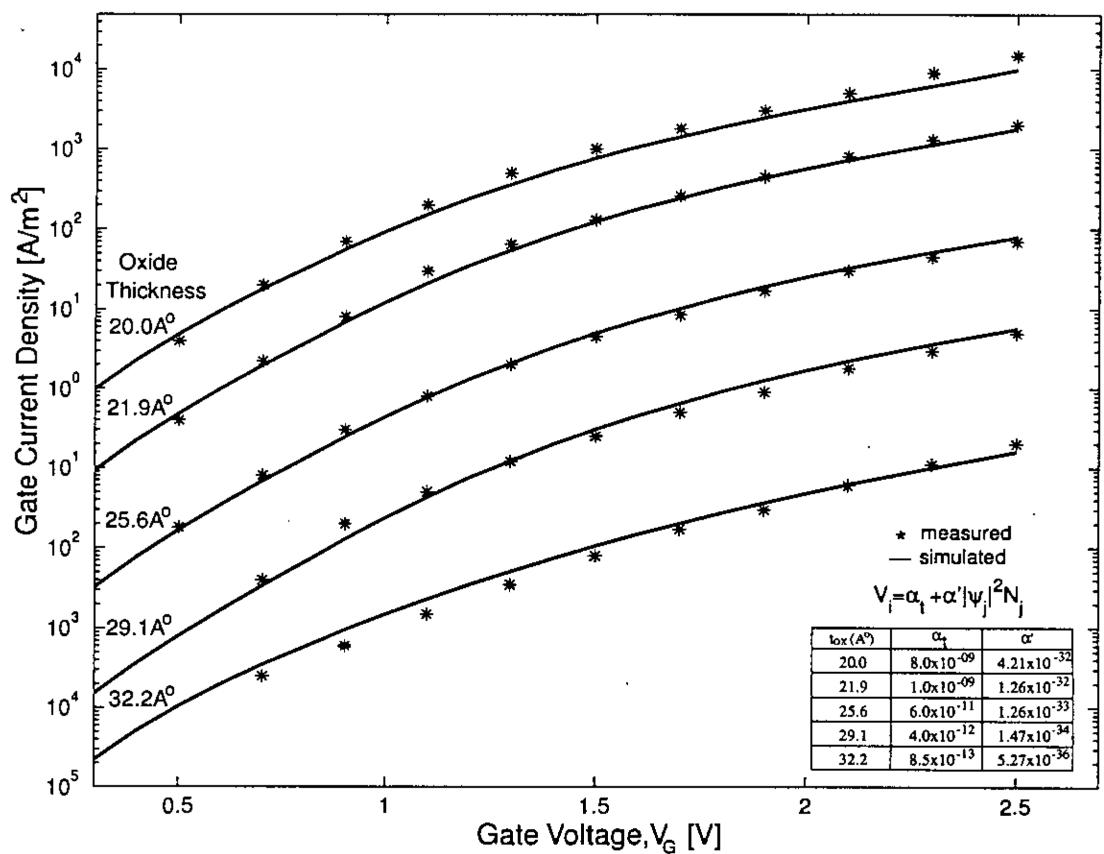


Figure 4.15: Variation of gate current with gate voltage at different oxide thickness. Substrate acceptor doping is 5x10^{17} cm^{-3}.

ν being oxide thickness dependent uniform scattering strength. The resultant curves now show a better match with the measured data but at higher gate voltages the simulated current is consistently smaller than the experimental data. It can be concluded that the distribution of scatterers is not a simple linear function of applied gate voltage.

So far, two conclusions can be drawn : (i) the scattering is obviously has a applied voltage dependent component but not simple function of applied gate voltage and (ii) there is a oxide thickness dependent component. Both of these observations are well supported by various experiments [3, 35] where it is reported that traps can be either implanted during fabrication (oxide thickness dependent part) or generated during operation (gate voltage dependent).

The voltage dependency may arise from the following phenomena. With in-



tox (A^o)	α_t	α'
20.0	8.0×10^{-09}	4.21×10^{-32}
21.9	1.0×10^{-09}	1.26×10^{-32}
25.6	6.0×10^{-11}	1.26×10^{-33}
29.1	4.0×10^{-12}	1.47×10^{-34}
32.2	8.5×10^{-13}	5.27×10^{-36}

Figure 4.16: Variation of gate current with gate voltage at different oxide thickness. Effective electron mass in oxide is $0.61m_o$ and substrate acceptor doping is $5\text{x}10^{17}\ cm^{-3}$.

creased applied voltage the penetration of wave function inside the oxide increases the overall carrier concentration inside the oxide layer. So there is an increased probability of interaction of electrons with already existing traps implanted at fabrication. Hence, the voltage dependency can be included in imaginary potential (V_i) by including a term proportional to the product $|\psi_j|^2N_j$. The fabrication dependence can be addressed by adding a constant in V_i's expression. Fig. 4.16 shows the simulated and measured gate current for five different oxide thickness. The imaginary potential V_i has the form:

$$V_i = \alpha_t + \alpha'|\psi_j|^2N_j \qquad (4.6)$$

both α_t and α' have different values for different oxide thickness. For the par-

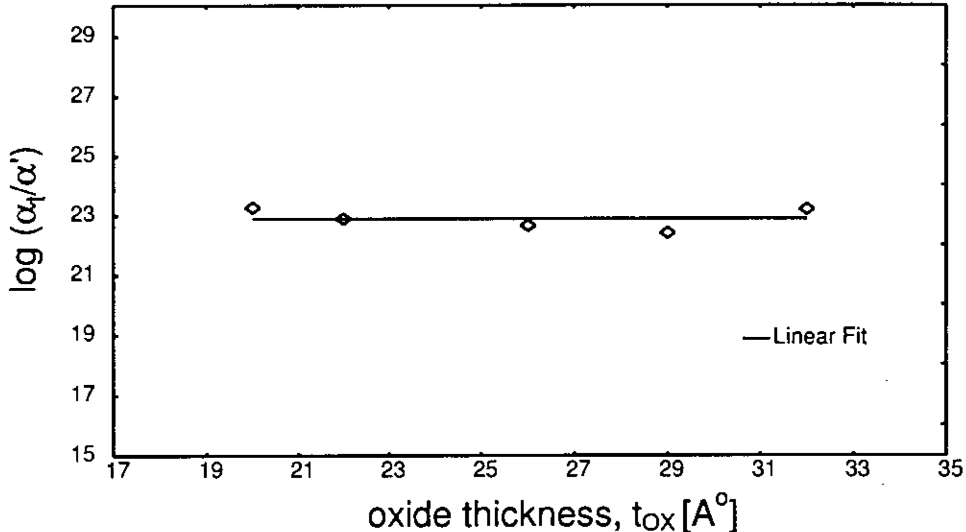


Figure 4.17: Variation of $\log(\alpha_t/\alpha')$ with gate oxide thickness

ticular values of α_t and α' (given in the Fig. 4.16)the simulated current is in better agreement with the measured data for a wider range of applied gate voltage. Fig. 4.17 shows the variation of $\log(\alpha_t/\alpha')$ with gate oxide thickness. It is apparent from the figure that the ratio is almost constant throughout. So, α' can be considered as α_t multiplied by a constant i.e.$\alpha' = \alpha_t\alpha_v$.

The imaginary potential profile (Eq. 4.6) now can be rewritten as

$$V_i = \alpha_t(1 + \alpha_v|\psi_j|^2 N_j) \tag{4.7}$$

where α_t is the term taking care of oxide thickness dependence of trap distributions and α_v is the proportionality constant for operation dependence. One aspect of this equation is that if there is no fabrication induced traps ($\alpha_t = 0$) then there is no operation induced traps either. Fig. 4.18 shows the comparison of measured and simulated gate current density for V_i calculated from Eq. 4.7. The values of the constants are chosen to achieve best fit.

The values of α_t for different oxide thickness, as shown in Fig. 4.19, has an exponential nature with oxide thickness. That is, as the oxide thickness is reduced the fabrication dependent trap density increases. If the variation of $\log(\alpha_t)$ is

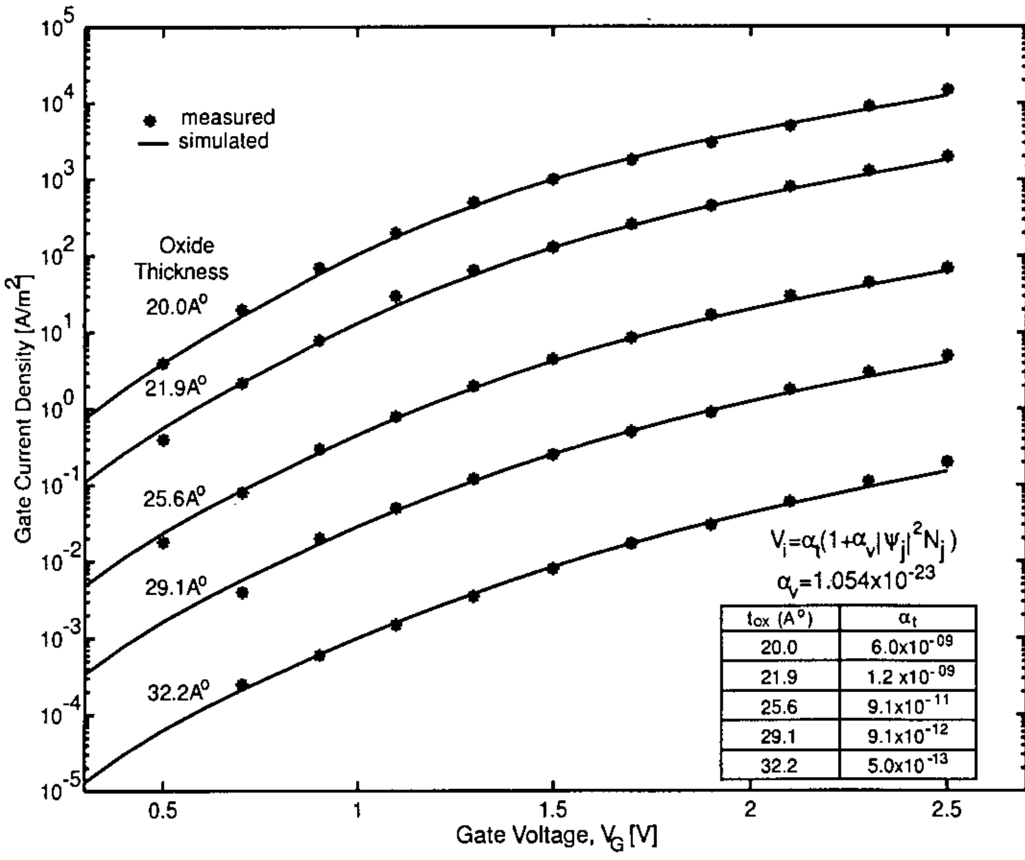


Figure 4.18: Comparison of simulated and measured gate current. Effective electron mass in oxide is $0.61m_o$ and substrate acceptor doping is 5x10^{17} cm^{-3}.

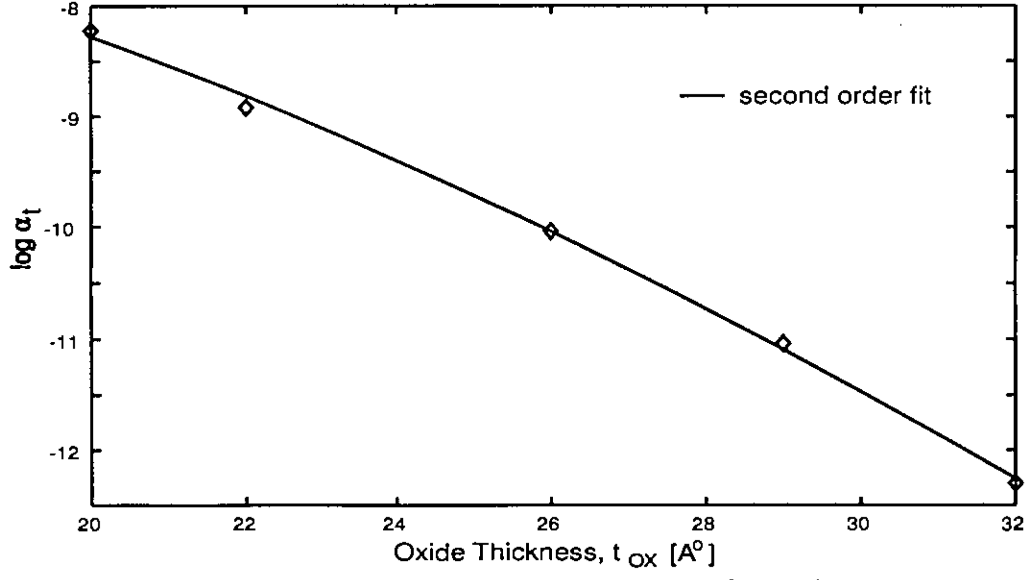


Figure 4.19: Variation of α_t with gate oxide thickness

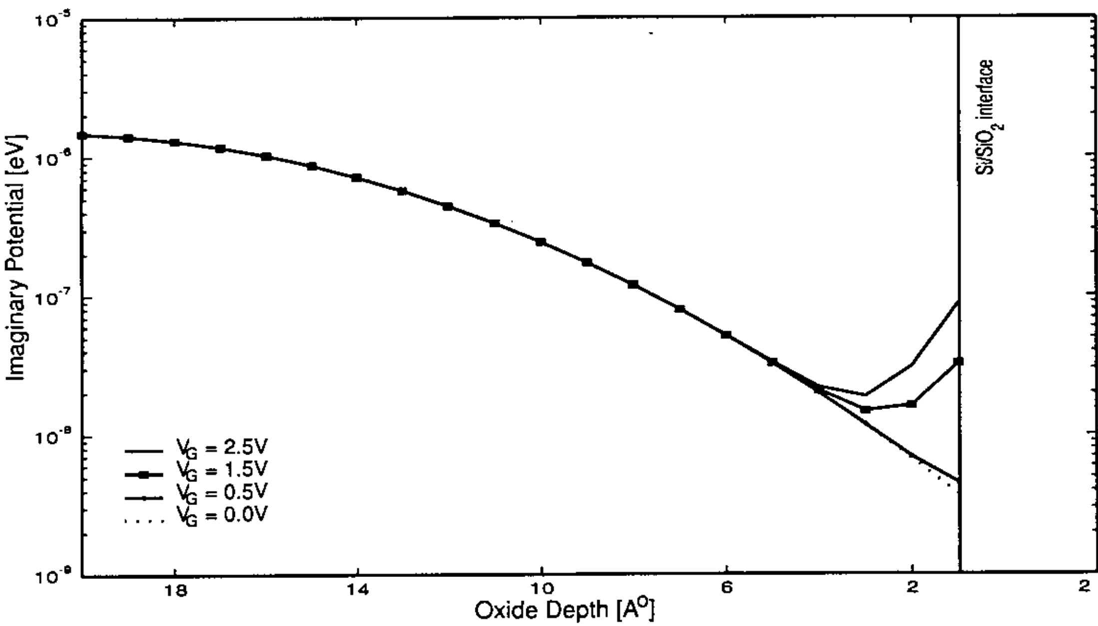


Figure 4.20: Distribution of imaginary potential inside the oxide.

fitted with a second order polynomial (Fig. 4.19), $\log \alpha_t$ can be expressed as

$$\log \alpha_t = -5.67 - 0.0044t_{OX} - 0.006296t_{OX}^2 \tag{4.8}$$

where t_{OX} is the oxide thickness in angstorm. The coefficient of x^2 is the dominant term here indicating a dominantly Gaussian distribution.It may be mentioned that the polysilicon doping is dominated by ion-implantation techniques and distribution of implanted ion follows a Gaussian distribution. So it is reasonable to represent the fabrication dependent scattering profile (α_t) by a Gaussian distribution. Applying a Gaussian fit on the discrete values of α_t from Fig. 4.18, the expression of imaginary potential (Eq. 4.7) can be re-written as

$$V_i = \alpha_{tm} \exp(-\varsigma x_m^2)(1 + \alpha_v |\psi_j|^2 N_j) \tag{4.9}$$

The peak value of α_t, α_{tm} and the constant ς is chosen to achieve a better match between simulated current and the experiments. The chosen value of α_{tm} is 1.5x10^{-6}, which is quite reasonable with equivalent scattering life time being τ=0.219ns. Fig. 4.20 shows the distribution of imaginary potential given by

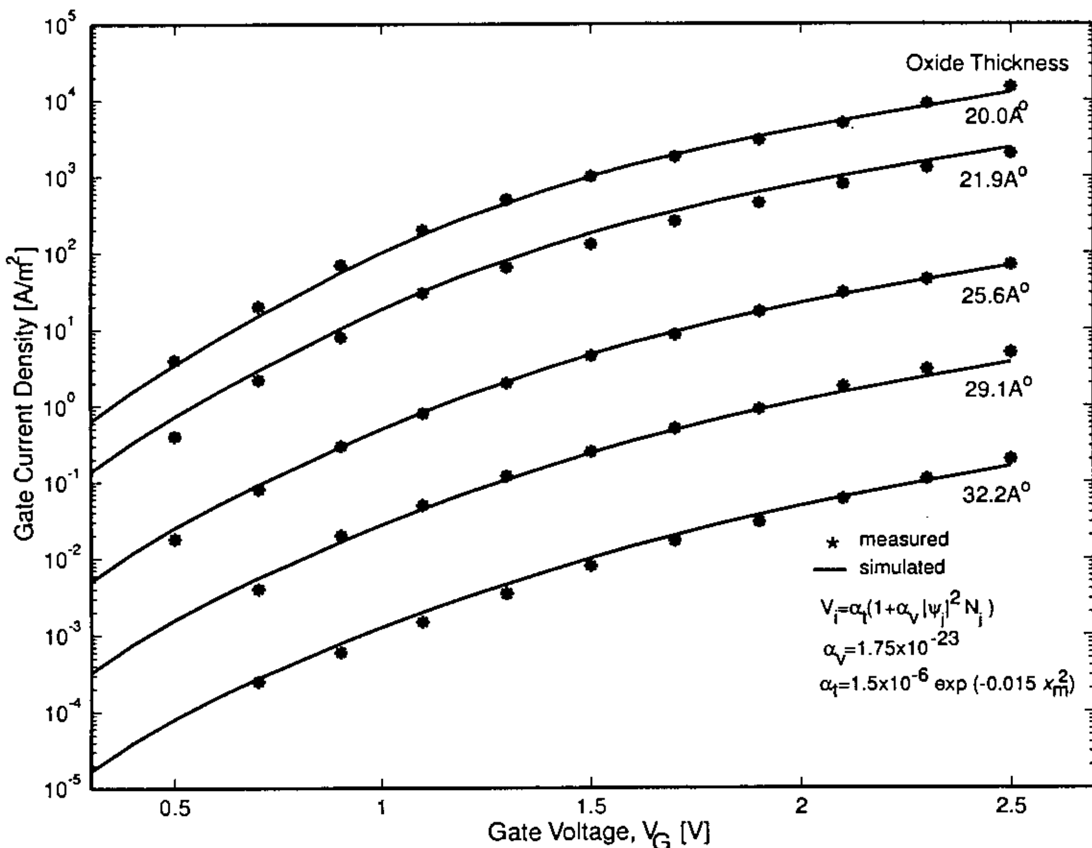


Figure 4.21: Comparison of simulated and measured gate current considering the distribution of traps implanted during fabrication is Gaussian. Effective electron mass in oxide is $0.61m_o$ and substrate acceptor doping is 5x10^{17} cm^{-3}.

Eq. 4.9 inside $20A^0$ oxide layer. The comparison of simulated and measured gate current with the above distribution of traps (Eq. 4.9) is shown in Fig. 4.21. The outcome is an excellent match of simulated gate current with the experiments.

Chapter 5

Conclusion

5.1 Summary

In this study, a quantum mechanical gate current model is developed incorporating the effects of scattering within the insulator. It employs the concept of generalized quantum mechanical impedance along with Green's function formalism to calculate carrier concentrations and wave functions. The model is free from calculation of complex eigen energies, tedious matrix manipulation and overlooking of the penetration of wave functions inside the oxide. It is generalized in the sense that the model is developed assuming arbitrary potential profile.

The main objective of this research is to estimate the trap distribution inside the oxide layer from the gate current. It has been shown that the traps implanted during fabrication and the traps generated during the operation of the MOSFET dominate the overall scattering mechanism inside the oxide. The simulation results for MOSFET's gate current using the developed model shows good match with experimental data taken from two groups [8, 11] for oxide thickness ranging $20A^o$ to $32A^o$ within a wide gate voltage range. The good agreement of the simulated gate current with experiment at the low gate voltages($\sim 0.5V$) as well as at high voltages ($\sim 2.5V$) is credited to the incorporation of scattering of carriers due to traps inside the oxide.

The simulations in chapter 4 show that gate current is predominantly effected

by the traps near the Si/SiO_2 and the effect of traps near gate edge is negligible when tunneling from substrate inversion layer is considered. It is observed that a uniform scattering distribution reduces the gaps of simulated and measured results but scattering strength has to be reduced with increased oxide thickness. Another feature of uniform scattering distribution is that it seems to overestimate the gate currents at low voltages and under-estimates the gate current at higher voltages and this trend is consistent with oxide thickness variation. These two features focus on the two distinct origin of traps: (i) traps are produced during the fabrication and are dependent on the oxide thickness and (ii) the traps are generated during operation and are dependent on the applied voltage.

Concentration of the implanted traps during fabrication decreases with the increase of oxide thickness. This can be explained if the traps are thought to be the result of impurity penetration in the oxide during the fabrication of gate. Penetration from gate implies that the peak of impurity distribution inside the oxide is at gate edge and decreases exponentially with the increasing distance from the gate. If the traps are the result of the penetration of impurities during the ion implantation of dopant in the poly-silicon gate, then the distribution will be a Gaussian distribution with a peak at gate edge. With the increase of the gate oxide thickness such trap concentration at Si/SiO_2 edge decreases.

The traps generated during operation are believed to be the result of the electron transport through the oxide. The traps generated are proportional to the number of carriers penetrated in the oxide and so the operation generated traps are modeled with an imaginary potential proportional to $|\psi_j|^2 N_j$. As the gate voltage is increased both $|\psi_j|^2$ and N_j increase leading to an increase in generated traps. This increased scattering now correctly estimates the gate current at high voltages.

Thus it is found that the trap distribution is composed of two components. One is the distribution of traps implanted during fabrication and the other is the

distribution of traps generated during operation. The implanted trap distribution has its peak at gate edge and follows a Gaussian distribution. The operation induced traps distribution has its peak at Si/SiO_2 interface. It is proportional to the sheet electron density and probability distribution function. At very low voltages the penetration of wave functions inside the oxide is less severe and thus the operation induced traps have less significant effects on gate current than the effect of bulk-dependent or fabrication induced traps. But at higher voltages the oxide penetration of wave functions become significant and also the carrier concentration increases, so the effect of operation induced traps on gate current becomes dominant.

5.2 Suggestion for future works

The model described here calculates gate current at inversion. For gate current at sub-threshold region another component of gate current, the contribution of carriers from gate electrode may become significant and has to be considered.

For computational simplicity self-consistent calculations of inversion layer parameters is not considered. Computational accuracy can be achieved with self-consistent calculation and also the values of trap distribution parameters may become more realistic.

The method can also be applied to stacked dielectrics (for example combination of silicon nitride and silicon dioxide) by modifying the potential profile appropriately. In such cases, consideration of different distribution of traps may be needed as impurity diffusion coefficient differs with materials.

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