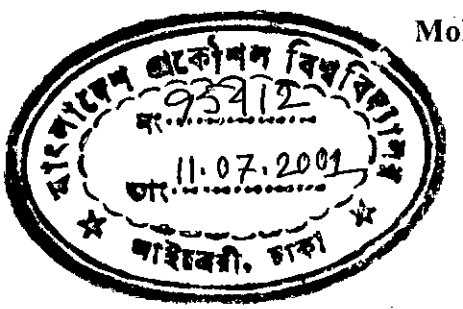
Testability Analysis of Complementary Pass Transistor Logic Circuits

by

Mohammad Muzahidul Karim



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DEDICATION

This work is dedicated to my parents for their constant support and my wife for her sincere love.

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ABSTRACT

Since the first time a new family of advanced differential CMOS logic called complementary pass transistor logic (CPL) was proposed, a lot of work on it in circuit and system level have been followed. It has been shown that CPL has much higher speed, lower power dissipation and consumes less silicon area for the same functionality compared to conventional CMOS circuits. Though CPL circuits have emerged as a promising candidate for VLSI design, testability issue of CPL circuits have not been examined yet. This thesis analyze the testability of CPL circuits and propose design for testability of CPL VLSI chip.

Testability analysis of Complementary Pass Transistor Logic (CPL) gates under various single stuck faults are presented first. It is shown that all stuck-on faults in the basic CPL gates (AND/NAND, OR/NOR, XOR/XNOR) can be detected by current monitoring which is popularly known as I_{DDQ} testing but no logic monitoring is possible. Similarly all stuck-at faults between gate and source of all the MOS devices of basic CPL gates can be detected only by current monitoring. However, for stuck-at fault between gate and drain of basic CPL gates, it is shown that all faults can be detected by current monitoring, except for the MOS M_3 in AND/NAND gate and MOS M_2 in OR/NOR gates. It is also shown that all stuck-open fault in the basic CPL gates are detectable by logic monitoring using appropriate two-pattern test. Finally, testability analysis of CPL full adder under various single stuck fault is performed. It is found that stuck-on fault on all the MOS transistor of the SUM logic and the CARRY logic circuit can be detected by steady state current monitoring with appropriate test vectors. For some of these test vectors the fault can also be detected by logic monitoring, but in all cases this is also accompanied by a large flow of signal source current. Similarly all bridging fault can be detected by current monitoring, but no logic monitoring is possible. Stuck open fault on all the MOS transistors on the SUM and the CARRY logic circuit can be detected by appropriate two pattern test. Finally it is concluded that signal source current monitoring (I_{DDQ} testing) is the best method for fault detection in CPL circuits and gives a very wide range of fault coverage.

Finally, current testing for on line fault detection in CPL VLSI chip have been proposed. Both fault detection by off the chip current monitoring and on-chip current monitoring is shown. For off-chip current monitoring a separate power supply rail for each of the approximately 15,000 gates is proposed. A small polysilicon resistor is inserted in the VDD rail. A tiny voltage drop occurs in the circuit under faulted condition which is then connected to a signal processing circuit and gives signal under faulted condition. For on-chip current monitoring the use of Built-In-Current-Sensor (BICS) is proposed and shown that it has negligible hardware overhead. It is expected these finding will enhance the acceptability of CPL circuits for VLSI design.

CHAPTER 1

INTRODUCTION

1.1. Aims

In the past decades, rapid advances in silicon VLSI technology, the maturing of digital IC design, and increased market demands have created the need for more and more integration on a single chip. The ultimate goal is to realize a full system on a single chip. Engineers are trying to reach this goal of massive integration by attacking the problem from two aspects - one is by improving the technology, i.e., by realizing lower feature size process and hence decreasing the device (transistor) size. The other is the use of innovative circuit techniques so that the same functionality and improved speed can be achieved with a less number of devices in the circuit. Complementary Pass-transistor Logic (CPL) is an advanced differential CMOS logic family that has much higher speed and lower power dissipation compared to conventional static CMOS logic [1]. It also consumes less silicon area for the same functionality compared to conventional CMOS circuits.

Today's high performance integrated circuits contain millions of transistor on a single chip [2]. As a result testing has become a difficult and time-consuming job. It is also becoming an increasing part of the time it takes from conception to marketing of a chip. The frequently quoted advantages of VLSI such as reduced system cost, improved performance and greater reliability will be lost unless VLSI chips can be economically tested. As a result it is essential to adopt design for testability approach in designing such complex integrated circuits in order to facilitate testing and save cost [3].

Though CPL circuits have emerged as a promising candidate for realizing VLSI circuits, testability issues of CPL circuits have not been examined yet. For successful application of any circuit technique in today's VLSI/ULSI chip, testability of the system and design-for-testability is a very important issue that needs to be adequately addressed. This requires a good understanding of the behavior of the circuits under fault.

The objective of this thesis is to make a rigorous analysis of testability of CPL circuits using all the models commonly employed in VLSI fault modeling and to propose a smart strategy for fault detection in CPL circuits [4-6]. These findings will be utilized to propose

methodology, which when included in the CPL VLSI chip will give the capability of on-line fault detection. It is expected that this design for testability approach will greatly reduce testing time and complexity and will enhance the acceptability of CPL circuits as an alternative of CMOS circuits for VLSI design.

1.2 Literature Review

Several differential CMOS logic families such as cascade voltage switch logic (CVSL) [7] and differential split-level logic (DSL) [8] have been proposed for CMOS circuit speed improvement. These have the common features of complementary data inputs/outputs, an nMOS logic tree, and a pMOS cross-coupled load, which together can reduce input capacitance, increase logic functionality, and sometimes eliminate inverter circuits. Therefore, these logic families can increase speed. However, the actual advantage of CVSL circuits is less than that anticipated in the original papers, as clarified in [9]. This is because the pMOS cross-coupled latch cannot easily be inverted due to the regenerative property of the latch. High-speed inversion of the pMOS latch is possible only when the gate width of the pMOS is sufficiently small. However, a small gate width severely degrades the pull-up transit time. DSL is faster than conventional CMOS, however at the expense of static power consumption [9].

Complementary Pass-transistor Logic (CPL) is an advanced differential CMOS logic family that has much higher speed and lower power dissipation compared to conventional static CMOS logic. It was first reported in the pioneering paper of Kazuo et. al. [1]. The main concept behind CPL is the use of an nMOS pass-transistor network for logic organization, and elimination of the pMOS latch. CPL consists of complementary inputs/outputs, an nMOS pass transistor logic network and CMOS output inverters. Arbitrary Boolean functions can be constructed from the pass transistor network by combining the basic circuit modules, an AND/NAND module, an OR/NOR module and an XOR/XNOR module. Kazuto et al [1] have fabricated a 3.8 ns 257 mW CMOS 16x16-bit multiplier and showed that CPL is twice as fast as conventional CMOS due to lower input capacitance and higher logic functionality. A lot of other works in circuit and system level have been published since the first time

complementary pass transistor logic (CPL) was proposed [1]. For example Abu-Khater et al [10] have shown that CPL implementation of full adder provides a power saving of 50% while Booth encoder for multiplier provided 30% of power saving compared to the conventional CMOS circuits. The later also provides 15% speed improvement. Many other researchers have fabricated CPL circuits and compared to CMOS, CPL have shown improvement in both speed and power [11-13]. Besides CPL circuits consume less silicon area compared to conventional CMOS circuits for the same functionality.

The frequently quoted advantage of VLSI are reduced system cost, improved performance and greater reliability. These advantages, however, will be lost unless VLSI chips can be economically tested. The dramatic increases in the ratio of the number of internal devices to input-output terminal pins of VLSI chips drastically reduces the controllability and observability of the circuit. Controllability refers to the ease of producing a specific internal signal value by applying signal to the circuit input terminals. Observability refers to the ease with which the state of internal signals can be deduced from the signals at the circuit output terminals. With chips containing millions or more transistors, testing are becoming costly or even computationally infeasible to implement [14]. Testing is becoming an increasing part of the time it takes from conception to marketing of a chip.

An approach, which is advocated to ease the burden of testing, is to use design for testability techniques. Many such techniques have been proposed. All of them have the common aim of trying to reduce the amount of time it takes to generate test vectors and apply them to the chip. Design for testability should become the rule rather than the exception in the future.

If we try to derive test vectors for every possible physical failure in a VLSI chip, the problem would soon become unmanageable. In order to successfully tackle the problem, the physical failure in a chip is represented at a higher level with the help of a fault model. The classical method of testing integrated circuits uses the stuck-at fault model [15,16]. Further work shows that this model alone may be inadequate for defects in CMOS circuits [17]. To replace or complement the stuck-at model, researchers have proposed other models more closely related to the physical mechanism causing faults. These models cover defects such as bridges

and opens in the physical layout [17-19]. A testing strategy to detect bridging fault in CMOS circuits using I_{DDQ} testing have been proposed in [20]. Their strategy provides compact test vector sets with very high coverage of Bridging faults and is applicable to circuit implemented with several kinds of logic modules. For Bi-CMOS circuits testability, most of the work reported in literature to-date have concentrated on fault characterization of the conventional family [21-23]. Different testing methods are also presented on the conventional BiCMOS gates [21-24]. A design for testability (DFT) technique for detecting short and bridging faults in CMOS/BiCMOS logic circuits has been presented in [25]. The DFT technique in [25] applies for detecting the defects that causes an excessive increase in power supply current (I_{DDQ} current). It has been claimed that about 67% of all possible shorts and bridging faults are detectable with this technique.

Though CPL circuits have emerged as a promising candidate for VLSI design, fault characterization and testability issues of CPL circuits have not been examined yet.

1.3 Organization of the thesis

Chapter two introduces the concept of CPL logic. Size, speed and performance of CPL logic circuits are compared with that of conventional CMOS circuits. A concise introduction to different fault models to idealize the physical failures in integrated circuits is also presented in this chapter. Chapter three discusses the fault characterization of basic CPL modules and presents both qualitative analysis and simulation results. In chapter four and five an examination into the behavior of CPL full adder sum and carry logic circuit under different single stuck faults are carried out. This includes both qualitative analysis and simulation-based characteristics of single faults in all the MOS transistors in the sum and the carry logic circuit of CPL full adder. In Chapter six design for testability concept for CPL circuit have been investigated and I_{DDQ} testing for CPL have been proposed. Chapter seven concludes the thesis with some suggestions for future work.

CHAPTER 2

CPL CIRCUITS AND FAULT MODELS

2.1 Introduction:

The topology and operation of CPL logic circuits are presented in this chapter. A comparison of CPL circuits with Conventional CMOS circuits is also presented. This chapter also focuses on the various faults that occur in integrated circuits and the fault models used to analyze the behavior of the faulty circuits.

2.2 CPL Logic Circuits : Concept and Examples

CPL circuit uses an nMOS pass-transistor network for logic organization and eliminates the pMOS latch. It consists of complementary inputs/outputs and an nMOS pass transistor logic network. The pass transistor function as pull-down and pull-up devices. Thus the pMOS latch can be eliminated, allowing the advantage of the differential circuits to be fully utilized. Because the high level of the pass transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistor, the signal is amplified by a CMOS inverter before connecting to the next stage. At the same time the CMOS output inverters shift the logic threshold voltage and drive the capacitive load.

Arbitrary Boolean function can be constructed from the pass transistor network by combining the three basic circuit modules: an AND/NAND module, an OR/NOR module and an EXOR/EXNOR module. One attractive feature of CPL is that the CPL complementary outputs are produced by the simple four transistor circuits. The various functions are produced by an identical circuit configuration with only a change of the input configuration.

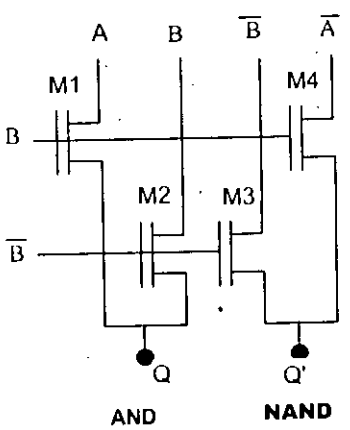


Fig.2.1 CPL AND/NAND Logic Circuit

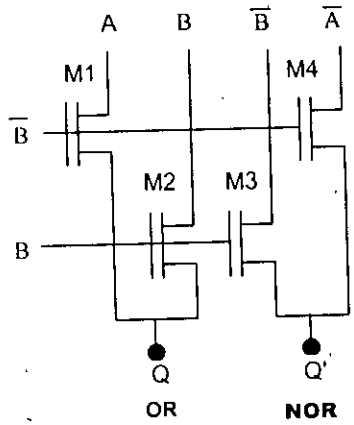


Fig.2.2 CPL OR/NOR Logic Circuit

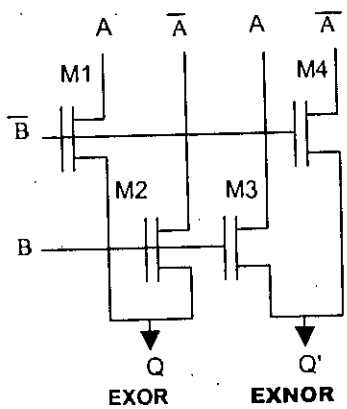


Fig.2.3 CPL EXOR/EXNOR Logic Circuit

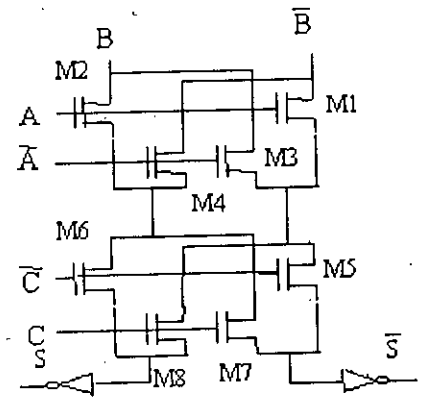


Fig. 2.4 CPL Full Adder SUM Circuit.

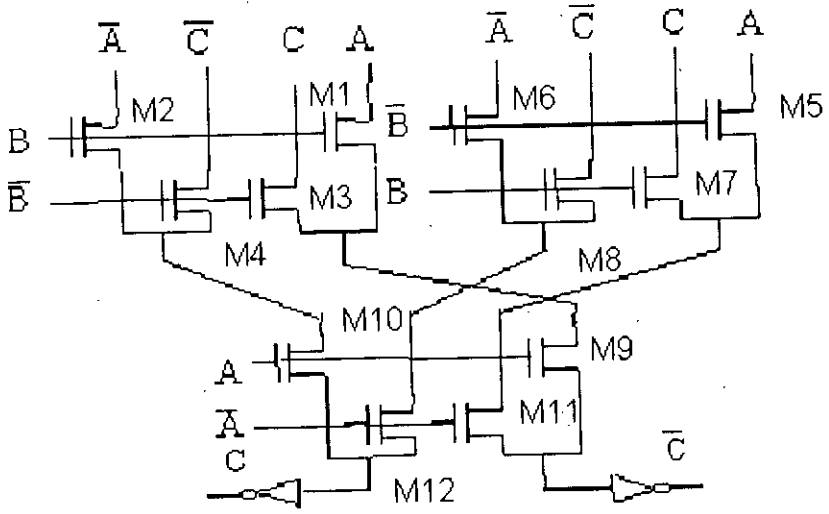


Fig. 2.5 CPL Full Adder CARRY Circuit

2.3 Comparison between CMOS and CPL Circuits

CPL technology can be utilized to achieve higher speeds compared to conventional CMOS [1]. As pMOS devices are eliminated from the logic construction of the CPL, the input capacitance is about half that of the conventional CMOS configuration, thus achieving higher speed and lower power consumption. CPL circuits are simpler than CMOS circuits and fewer devices are required by CPL structures [1]. Consequently, CPL structures occupy less area than equivalent CMOS structures. A comparison between a CMOS full adder with a CPL full adder designed with same process technology is shown below [1].

Table 2.1

Comparison between a CMOS full adder with a CPL full adder

Properties	CMOS full adder	CPL full adder
Transistor Count	40	28
Area	4730 mm^2	4218 mm^2
Delay (4v)	0.63 ns	0.28 ns
Power (100 Mhz)	1.2 mW	0.86 mW

However, despite the clear advantage of CPL circuit over CMOS circuit testability of CPL circuit not been examined yet. For successful application of any circuit technique in today's VLSI chip, testability of the system and design for testability are very important issues that needs to be address adequately.

2.4 Physical Failure in Integrated Circuits

Various physical defects can occur in an Integrated Circuit during the fabrication or during its use [21, 22]. A defect that causes a change of the logical function of the circuit can be represented by a logical abstraction known as logical fault. Similarly a defect that causes a change in a continuous parameter of the circuit can be represented by an abstraction called a parametric fault (such as current drawn by the circuits). Since the process technology of CPL circuit is same as CMOS technology, CPL devices are prone to the defects, which occur in CMOS circuits.

The most common defects are

1. Shorts (e.g., gate oxide shorts or channel may be shorted etc.)
2. Opens (e.g., intra gate breaks)
3. Circuit degradation (e.g., threshold voltage variation).

2.5 Faults and Errors

A fault is an actual defect that occurs in the device. If a vector applied to a faulty device produces an incorrect response, an error is said to have occurred. When this fault is exposed at the circuit outputs by the same input vector, an error results. In this case the error is manifested as an incorrect logic value at one or more of the circuit outputs.

2.6 Fault Models

If we try to device test vectors for every possible physical failure in a VLSI chip, the problem would soon become unmanageable, In order to tackle the problem successfully, physical failures in a chip are represented with the help of a fault model [15-19, 26]. Any one fault from the fault model may represent many physical failures. The most commonly used fault models for CMOS circuits are

a. Stuck-on
b. Stuck-at
c. Stuck-open
d. Bridging

In this work the behaviors of CPL circuits under various faults are investigated using the above models.

2.6.1 Stuck-on Fault Model

If a transistor is permanently ON irrespective of the input signal applied at the gate then it is referred to as stuck-on [27]. The fault may occur when the source and drain transistor are short circuited. This type of fault can be modeled by replacing a resistor R_{fault} in Parallel with the transistor between the respective terminals.

2.6.2 Stuck-at Fault Model

The fault model, which has found widespread use in the industry, is the stuck at fault model [28]. In this model it is assumed that the fault causes a line in the circuit to behave as if it is permanently at logic 0 or logic 1. If the line is permanently at logic 0 it is said to be stuck at 0, otherwise if the line is permanently at logic 1 it is said to be stuck at 1.

2.6.3 Stuck-open Fault Model

When a transistor is rendered non-conducting by a fault it is said to be stuck open. A stuck open fault may force a combination CPL circuit to behave in a sequential fashion. Thus in order to detect a stuck open fault, a sequence of vectors is required. A sequence of two vectors referred to as the two pattern test is usually applied to detect the fault. The first vector is called initialization vector and the second vector is called test vector. The two pattern test should be applied at a rate more rapid than that associated with the leakage current time constant [27]. Otherwise a correct transition may be observed at the output even in the presence of fault. To model an open fault of a device terminal, a large resistance is inserted between the device terminal and the circuit node to which the terminal would otherwise be connected.

2.6.4 Bridging Fault Model

A bridging fault is generally defined to be a short among two or more signal lines in the circuit. Such a short could occur, for example, due to defective masking or etching, aluminum migration, breakdown of insulator, etc. [29]

CHAPTER 3

FAULT CHARACTERIZATION OF BASIC CPL CIRCUITS

3.1 Introduction

This chapter presents the results of investigation into basic CPL circuits under various single stuck faults. To avoid the complexity of dealing with multiple defect case, it is assumed in the work that not more than one defect can occur at a time. Single stuck-on, Bridging and single stuck-open faults in MOS transistors are considered. Multiple faults are clearly possible but it seems reasonable to suppose that a circuit with two faults will still fail test programs. Of course there may be fault masking but very few engineers believe that this is a significant problem in practice [18]. The behavior of all the three basic circuit modules in CPL, namely a AND/NAND module, an OR/NOR module and a EXOR/EXNOR under various single stuck fault are investigated. First qualitative analysis is performed which is then followed by extensive SPICE simulations. In all simulations SPICE level3 MOS model parameters of a 1.2μm process were used. It is expected that the use of sub-micron process parameters with better SPICE model such as BSIM will increase the normal operating current by some extent, however, the large difference between normal operating current and current under faulted condition will remain unchanged.

3.2 Fault Modeling

Physical defects in VLSI circuits can be modeled as open or shorts in switch level representation [7, 18]. For a more realistic modeling the possibility of a short between two terminals (drain-source for MOS) of a transistor as well as an open in one transistor node (source or drain of MOS) are considered. Shorts are modeled as a small resistor between two nodes. Open circuits are modeled as a large resistor inserted between the effected nodes and the node to which it would be normally has been connected. The values of the resistors, modeling shorts and opens, are varied in a wide range to take into account faults of various strengths.

In this thesis all input high logic level will be referred as V_{IH}, fault of MOS 1 will be referred as M_1.

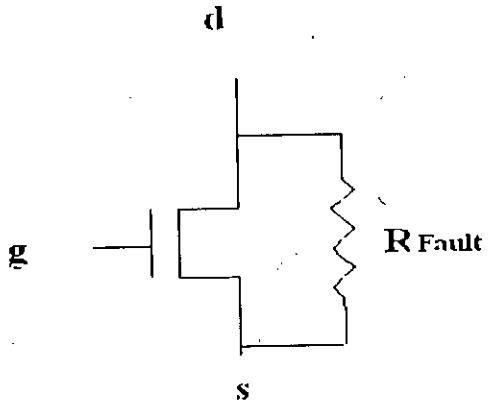


Fig. 3.1 Stuck on fault model

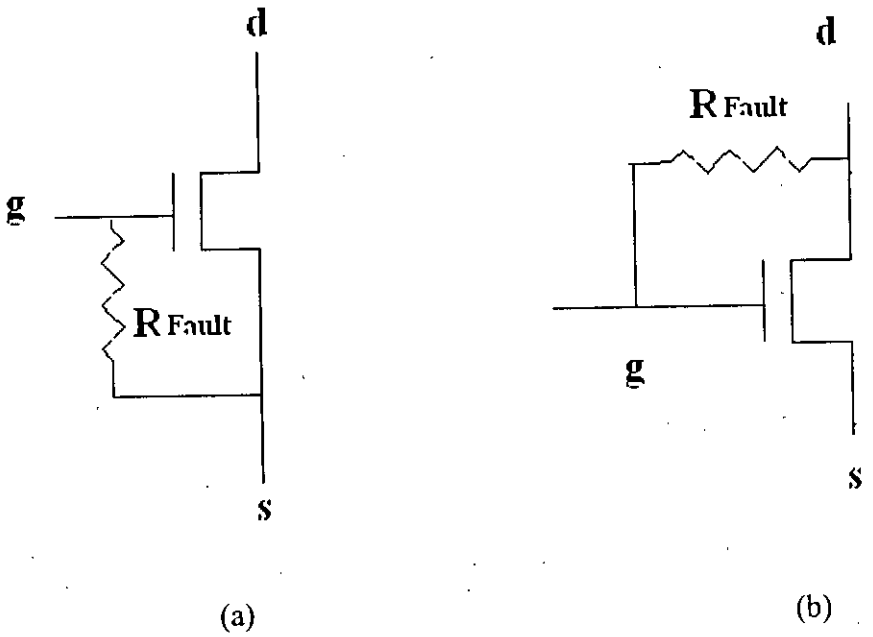


Fig. 3.2 Bridging fault model

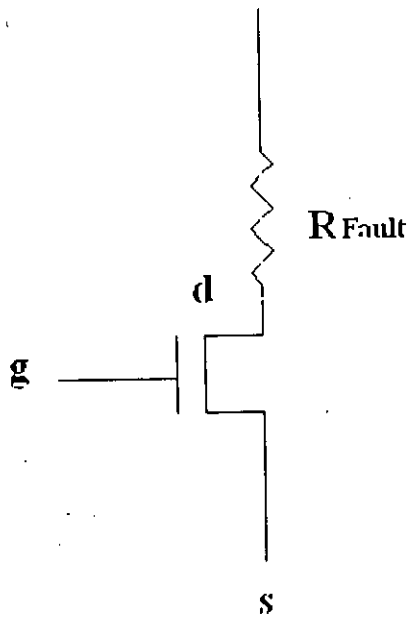


Fig. 3.3 Stuck open fault model

Figure 3.1, 3.2 and 3.3 show how these three types of faults are modeled. In these figures, R_{Fault} determines the fault strength. These fault models have been used to simulate faults of various strengths by simply changing the value of R_{Fault} or R_f.

3.3 Behavior Under Single Stuck-on Faults:

The behavior of basic CPL circuits under single stuck on fault in MOS are analyzed in this section. All the basic CPL circuit models, i.e., NAND/AND, NOR/OR and EXNOR/EXOR gates are considered. The two input NAND/AND gate shown in figure 2.1, the two input NOR/OR gate shown in figure 2.2 and the two input EXNOR/EXOR gate shown in figure 2.3 are used for analysis.

3.3.1 Qualitative Analysis for CPL AND/NAND Circuit:

M_1 : (stuck-on fault in M_1 of the CPL AND/NAND gate of figure 2.1)

An AND/NAND gate with a single MOS stuck on fault in MOS M_1 is shown in figure 3.4 The fault is modeled by placing a resistor R_f between the gate source and drain terminal of the faulted MOS. The tests vectors (0,0), (0,1) and (1,1) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, when the vector (1,0) is applied, MOS M_2 turns ON and a large

current I_{DDQ} flows through R_f and M_2. In a fault free circuit, the (1,0) vector would have pulled the output node down to the ground level. In the faulty circuit, the voltage becomes,

$$V_{out} = \{R_{on}/(R_f+R_{on})\} V_{IH}$$

where R_{on} is the on resistance of MOS M_2 and V_{IH} is the input high logic level at A. When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to V_{IH} depending on the fault strength (R_f), hence the stuck on fault at M_1 cannot be detected by logic monitoring. However, the steady state current, is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring, i.e., I_{DDQ} Testing.

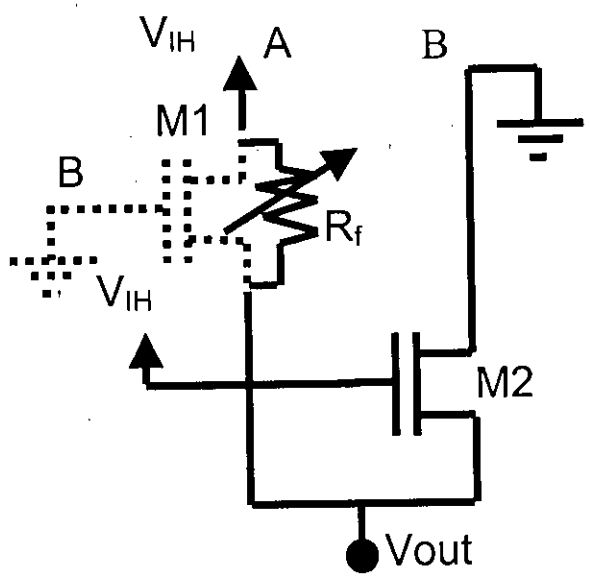


Fig. 3.4 Stuck-on fault in MOS M_1 of CPL AND gate for test vector [A=1, B=0]

M_2 : (stuck on fault in M_2 of the CPL AND/NAND gate of figure 2.1)

In figure 3.5 the fault is modeled by placing a resistor R_f between the gate source and drain terminal of the faulted MOS. The tests vectors (0,0), (1,0) and (1,1) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, when the vector (0,1) is applied, M_1 turns ON and a large current flows through R_f and M_1. The output voltage becomes,

$$V_{out} = \{R_{on}/(R_f+R_{on})\} V_{IH}$$

where V_{IH} is the input high voltage level shown in the figures as 5V. When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to V_{IH}, hence the stuck on fault at M_2 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring, i.e., I_{DDQ} Testing.

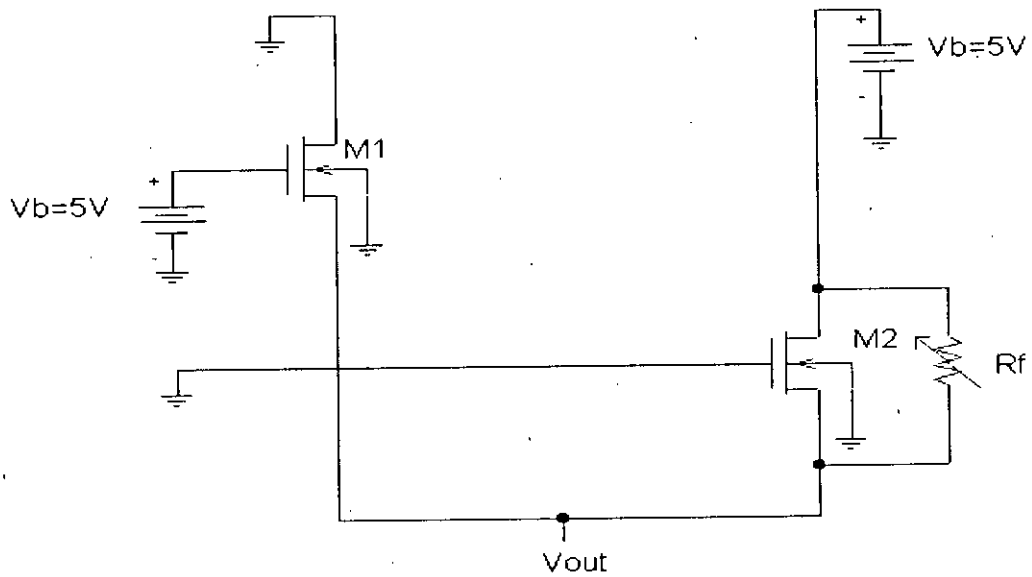


Fig. 3.5. Simulation circuit for stuck-on fault on MOS M_2 of CPL AND circuit for test vector [A=0, B=1]

M_3 : (stuck on fault in M_3 of the CPL AND/NAND gate of figure 2.1)

In figure 3.6 the fault is modeled by placing a resistor R_f between the gate source and drain terminal of the faulted MOS. The tests vectors (0,0), (1,0) and (1,1) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, when the vector (0,1) is applied, M_4 turns ON and a large current flows through R_f and M_4.

$$V_{out} = \{R_f/(R_f+R_{on})\}V_{IH}$$
$$= V_{IH}/(1+ R_{on}/ R_f)$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the stuck on fault at M_3 cannot be detected by logic

monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring, i.e., I_{DDQ} Testing.

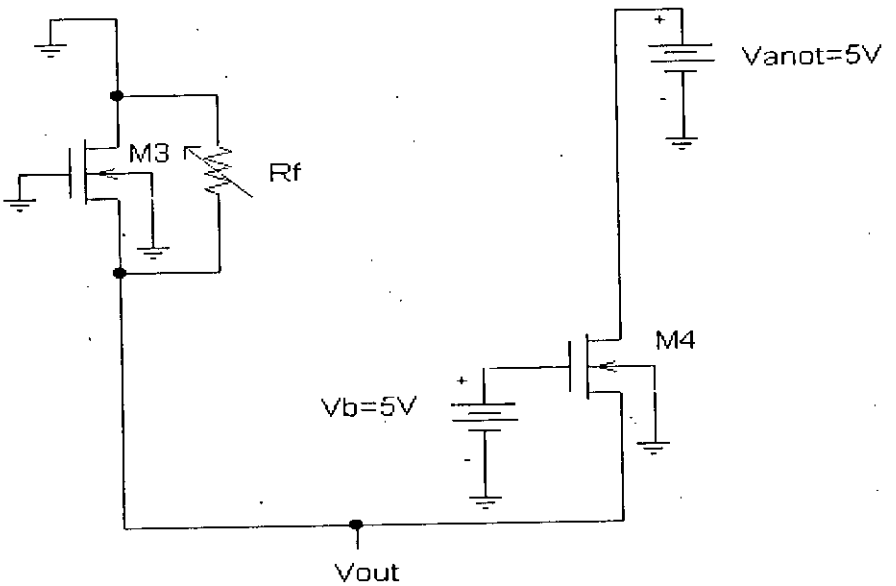


Fig. 3.6 Simulation circuit for stuck-on fault on MOS M_3 of CPL NAND circuit for test vector [A=0, B=1].

M_4 : (stuck on fault in M_4 of the CPL AND/NAND gate of figure 2.1)

In figure 3.7 the fault is modeled by placing a resistor R_f between the gate source and drain terminal of the faulted MOS. The tests vectors (0,0), (0,1) and (1,1) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, when the vector (1,0) is applied, M_3 turns ON and a large current flows through the circuit.

$$V_{out} = \{R_f/(R_f+R_{on})\} V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the stuck on fault at M_4 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring, i.e., I_{DDQ} Testing.

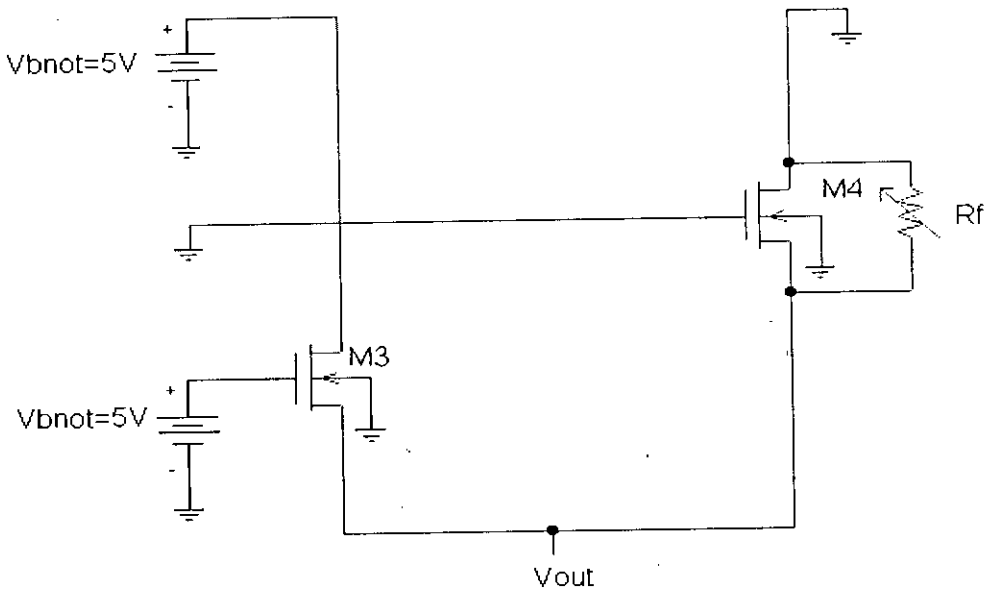


Fig. 3.7 Simulation circuit for stuck-on fault on MOS M_4 of CPL NAND circuit for test vector [A=1, B=0].

3.3.2 SPICE Simulation Results for Stuck-on Fault in CPL AND/NAND Circuit

This section summarizes the SPICE simulation results for a single stuck on fault in the MOS devices of the CPL AND/NAND logic gates.

Table 3.1

SPICE Simulation results for stuck on faults in CPL AND/NAND gate.

Effect of Fault Strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
		V_a	V_b		
M_1	1	5	0	4.997	2.34E-03
	10	5	0	4.976	2.34E-03
	100	5	0	4.767	2.32E-03
	1K	5	0	2.824	2.17E-03
	10K	5	0	0.266	4.73E-04
	100K	5	0	0.026	4.97E-05
M_2	1	0	5	4.997	2.34E-03
	10	0	5	4.976	2.32E-03
	100	0	5	4.767	2.09E-03
	1K	0	5	2.824	1.11E-03
	10K	0	5	0.266	2.33E-04
	100K	0	5	0.026	2.94E-05
M_3	1	0	5	0.002	2.34E-03
	10	0	5	0.023	2.31E-03
	100	0	5	0.209	2.09E-03
	1K	0	5	1.111	1.11E-03
	10k	0	5	2.329	2.32E-04
	100k	0	5	2.943	2.94E-05
M_4	1	5	0	0.002	2.34E-03
	10	5	0	0.023	2.34E-03
	100	5	0	0.209	2.32E-03
	1k	5	0	1.111	2.17E-03
	10k	5	0	2.329	4.73E-04
	100k	5	0	2.943	4.97E-05

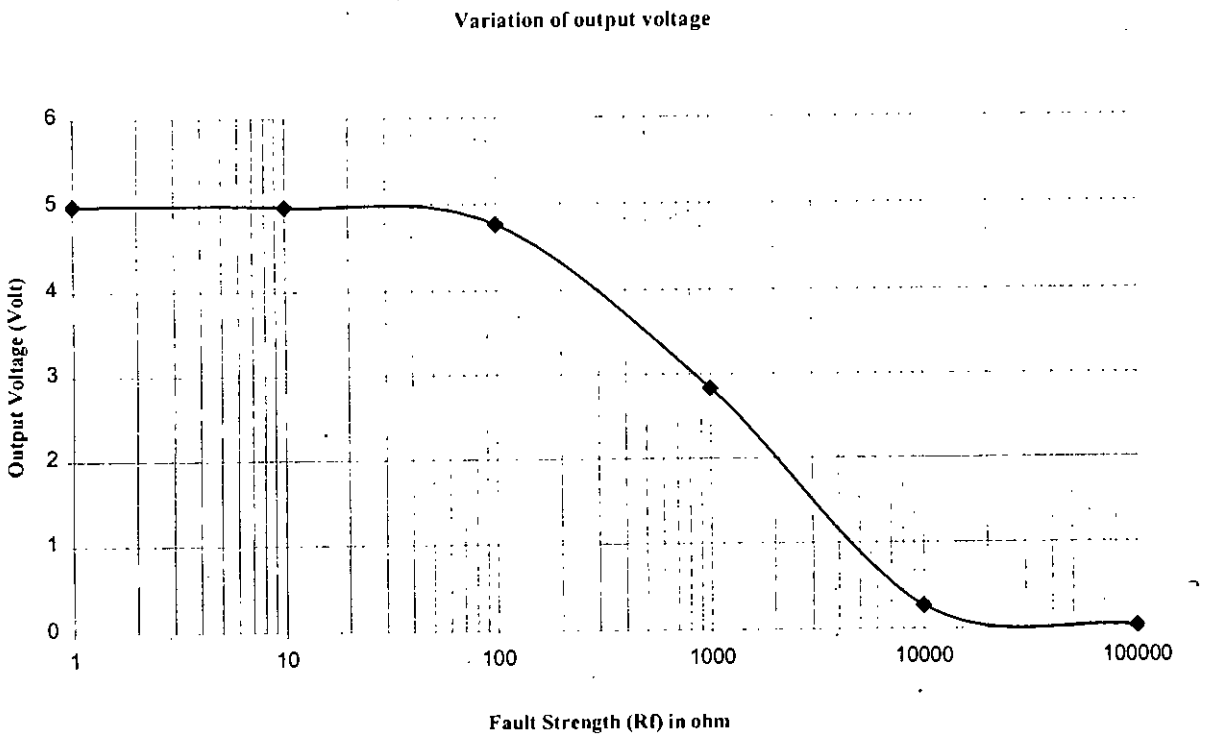


Fig 3.8 Output voltage vs. Fault Strength.

(Stuck on fault for M_1 Test Vector 10 and M_2 Test Vector 01)

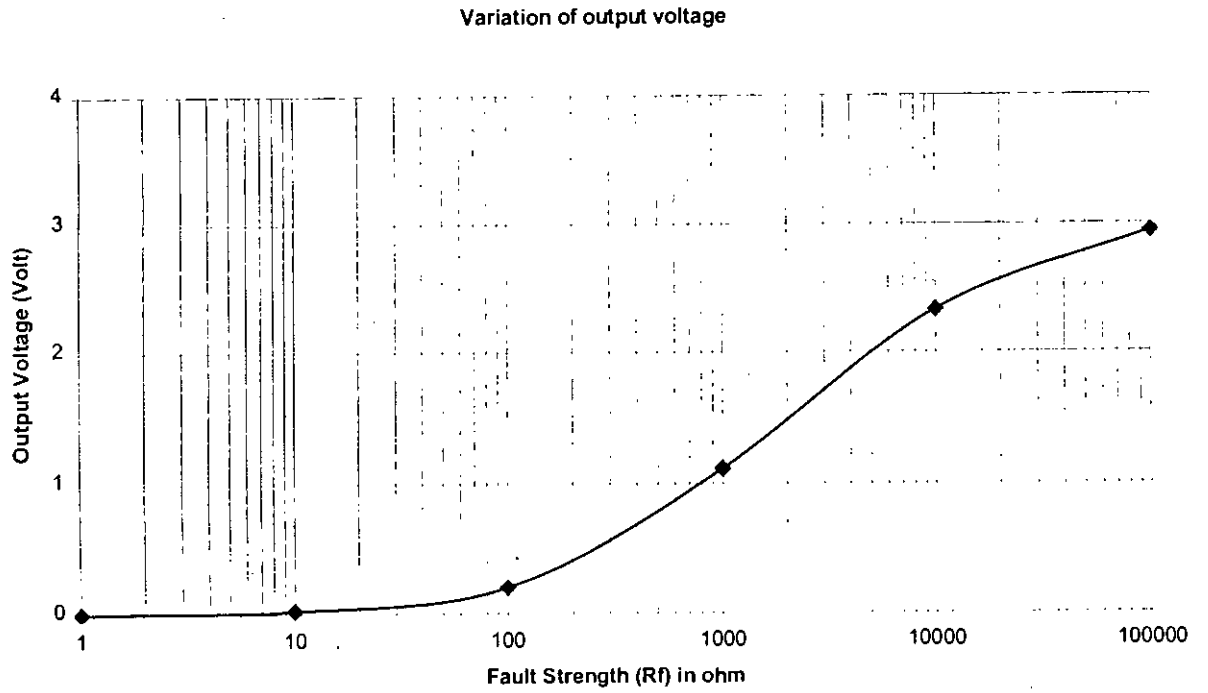


Fig 3.9 Output voltage vs. Fault strength

(Stuck on fault for M_3 Test Vector 01 and M_4 Test Vector 10)

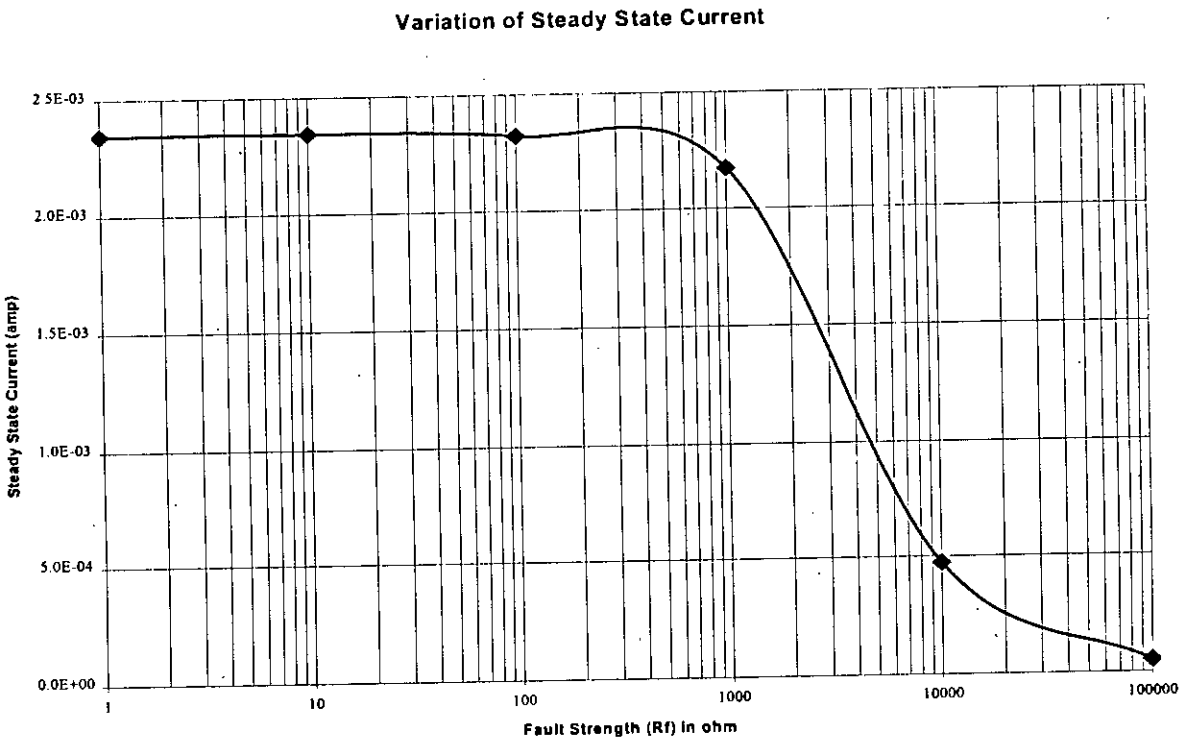


Fig 3.10 Steady state current vs. Fault strength

(Stuck on fault for M_1 and M_4 Test Vector 10)

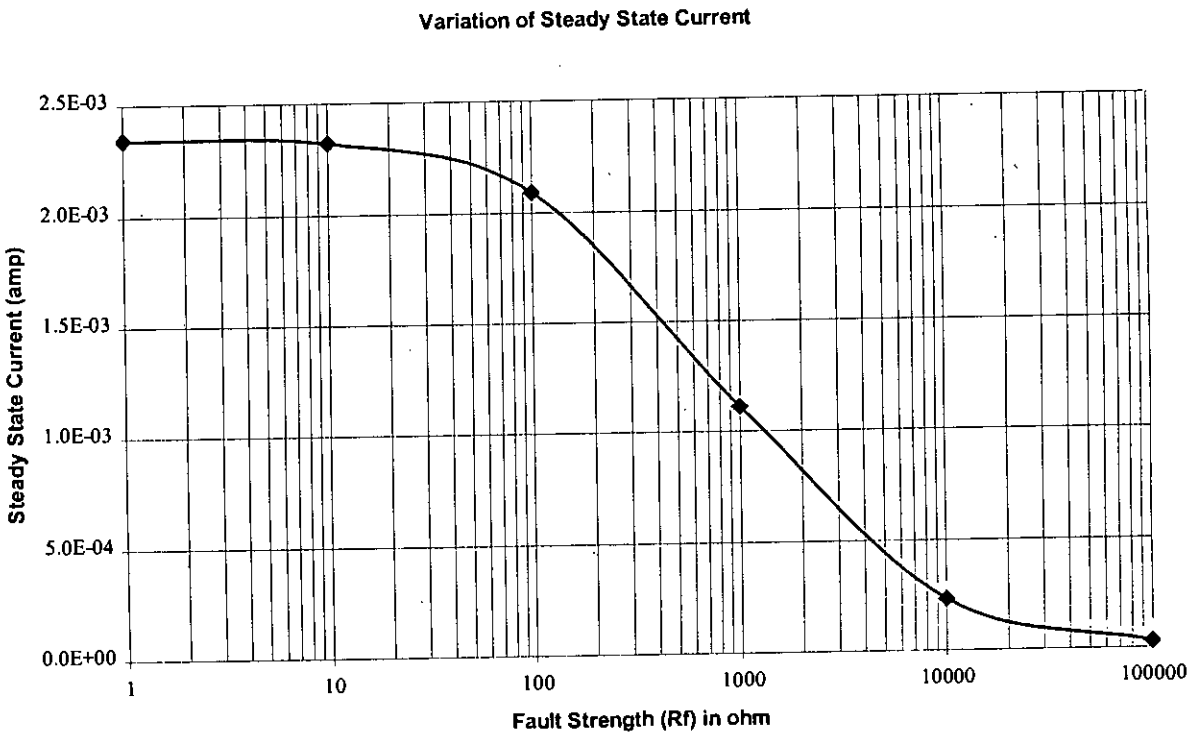


Fig 3.11 Steady state current vs. Fault strength

(Stuck on fault for M_2 and M_3 Test Vector 01)

Effects of Fault Resistance:

As seen from table 3.1, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 1 Ω to 100 kΩ, the output voltage varies from 0 to 4.9766 Volt. This appreciable variation in output voltage clearly shows that the output logic level is indeterminable. This agrees with our prediction that the fault cannot be detected by logic monitoring. As seen from the table, steady state current is in the range of mili-ampere compared to normal operating current of 5 pA. Therefore, the fault can be detected by current monitoring. For clarification of these points the variation of output voltage and steady state current with fault strength for stuck-on fault on MOS M_1 of CPL AND gate is shown below. When the fault strength is as

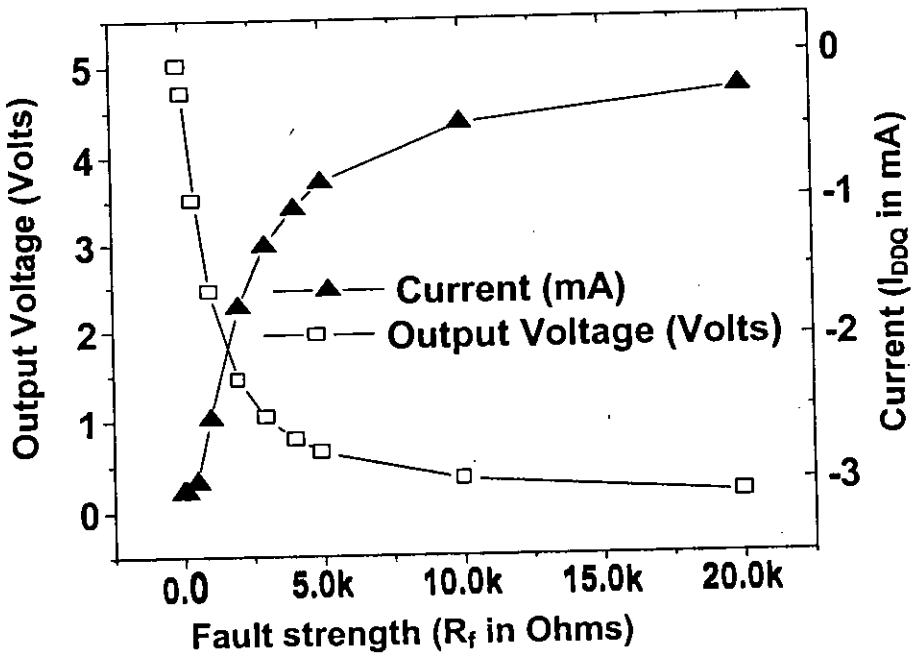


Fig. 3.12. Variation of output voltage and steady-state current with fault strength for stuck-on fault on MOS M_1 of CPL AND circuit. Test vector [A=0,B=1].

high as 10-20 K Ohms the output voltage is approximately 0 hence gives a correct logic. However, even at 20 K ohms the steady state current 0.35mA compared to 5 pA for a fault free circuit. Therefore the ratio of steady state current for faulty condition and fault free condition is very high and it can be effectively used as a parameter for fault detection.

Table 3.2

The following table shows the summary for stuck on faults in CPL AND/NAND circuit.

Summary for Stuck-on faults in CPL AND/NAND Circuit

Fault	Test Vector	V_{out}	I_{DDQ}	Logic Monitoring possible?	Current Monitoring possible?
M_1	(00)	0	5 pA	No	No
	(01)	0	3.66E-11	No	No
	(10)	***0.026 to 4.97***	***4.97E-5 to 2.34E-3***	***No***	***Yes***
	(11)	5	5 pA	No	No
M_2	(00)	0	6 pA	No	No
	(01)	***0.026 to 4.97***	***4.97E-5 to 2.94E-5***	***No***	***Yes***
	(10)	0	3.66E-11	No	No
	(11)	5	0	No	No
M_3	(00)	5	0	No	No
	(01)	***0.026 to 2.94***	***2.34E-3 to 2.94E-5***	***No***	***Yes***
	(10)	0	3.66E-11	No	No
	(11)	0	0	No	No
M_4	(00)	5	0	No	No
	(01)	5	0	No	No
	(10)	***0.026 to 2.94***	***2.34E-3 to 4.97E-5***	***No***	***Yes***
	(11)	0	0	No	No

3.3.3 Qualitative Analysis for CPL OR/NOR Circuit

M_1 : (stuck on fault in M_1 of the CPL OR/NOR gate of figure 2.2)

In fig 3.13 the fault is modeled by placing a resistance R_f between the gate and source terminal of the faulted MOS. The tests vectors (0,0), (1,0) and (1,1) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, when the vector (0,1) is applied, M_2 turns ON and a large current flows through the circuit. The output voltage

$$V_{out} = \{R_f/(R_f+R_{on})\}\ V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any valuc from 0 to V_{IH} depending on R_f, hence the stuck on fault at M_1 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring i.e. I_{DDQ} Testing.

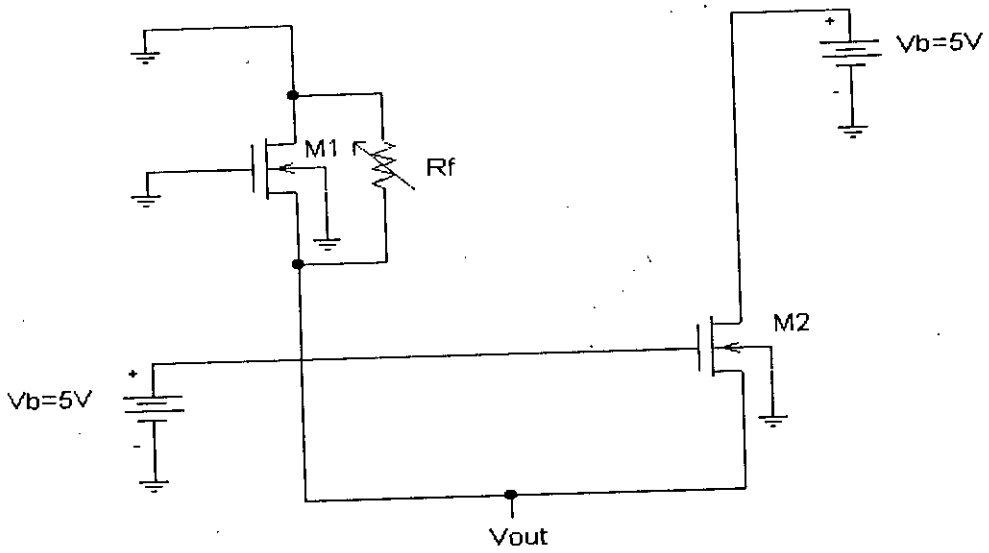


Fig. 3.13: Simulation circuit for stuck-on fault on MOS M_1 of CPL OR gate for test vector [A=0, B=1].

M_2 : (stuck on fault in M_2 of the CPL OR/NOR gate of figure 2.2)

The fault is modeled by placing a resistor between gate and source of M_2. The tests vectors (0,0), (0,1) and (1,1) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, the vector (1,0) can successfully detect the fault because of a flow of large current through the circuit. The is expression for current and voltage is similar to the previous case. The result of SPICE simulations are presented in the tables at the end of this article.

M_3 : (stuck on fault in M_3 of the CPL OR/NOR gate of figure 2.2)

In fig 3.14 the fault is modeled. The tests vectors (0,0), (0,1) and (1,1) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, when the vector (1,0) is applied, M_4 turns ON and a large current flows through the circuit.

$$V_{out} = \{R_{on}/(R_f+R_{on})\} V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the stuck on fault at M_3 cannot be detected by logic

monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring i.e. I_{DDQ} Testing.

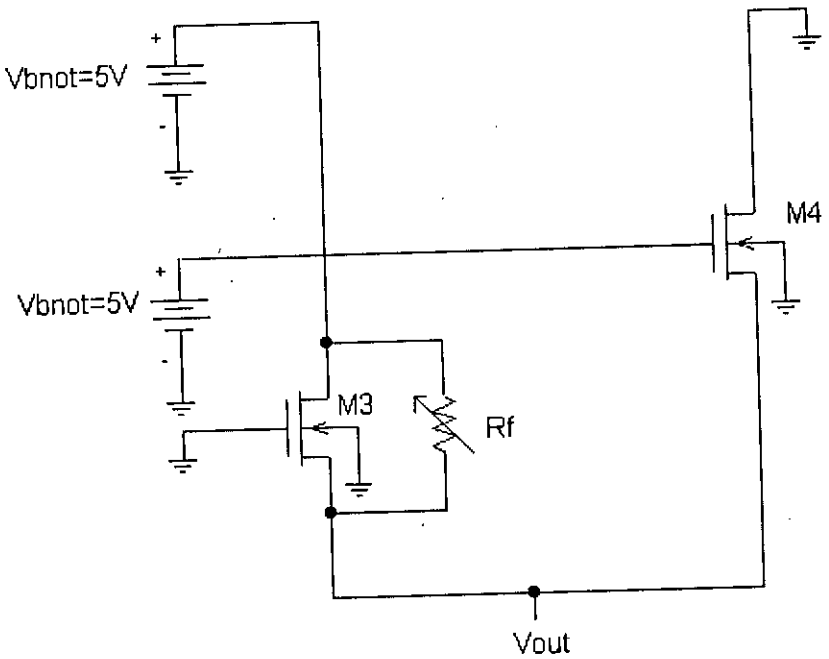


Fig. 3.14 Simulation circuit for stuck-on fault on MOS M_3 of CPL NOR gate for test vector [A=1, B=0]

M_4 : (stuck on fault in M_4 of the CPL NOR/OR gate of figure 2.2)

The fault is modeled by placing a resistor between gate and source of M_4. The tests vectors (0,0), (1,0) and (1,1) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, the vector (0,1) can successfully detect the fault because of a flow of large current through the circuit. The expression for current and voltage is similar to the previous case. The result of SPICE simulations are presented in the tables at the end of this article.

3.3.4 SPICE Simulation Results for Stuck on Fault in CPL OR/NOR Circuit

This section summarizes the SPICE simulation results for a single stuck on fault in the MOS devices of the CPL OR/NOR logic gates.

Table 3.3. SPICE Simulation results for stuck on faults in CPL OR/NOR gate.

Effect of fault strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
		V_a	V_b		
M_1	1	0	5	0.003	2.34E-03
	10	0	5	0.033	2.34E-03
	100	0	5	0.269	2.32E-03
	1K	0	5	1.365	2.17E-03
	10K	0	5	2.865	4.73E-04
	100K	0	5	3.267	4.97E-05
M_2	1	5	0	0.002	2.34E-03
	10	5	0	0.023	2.32E-03
	100	5	0	0.209	2.09E-03
	1K	5	0	1.111	1.11E-03
	10K	5	0	2.329	2.33E-04
	100K	5	0	2.943	2.94E-05
M_3	1	5	0	4.997	2.34E-03
	10	5	0	4.996	2.31E-03
	100	5	0	4.692	2.09E-03
	1K	5	0	2.446	1.11E-03
	10k	5	0	0.327	2.32E-04
	100k	5	0	0.032	2.94E-05
M_4	1	0	5	4.997	2.34E-03
	10	0	5	4.996	2.34E-03
	100	0	5	4.692	2.32E-03
	1k	0	5	2.446	2.17E-03
	10k	0	5	0.327	4.73E-04
	100k	0	5	0.032	4.97E-05

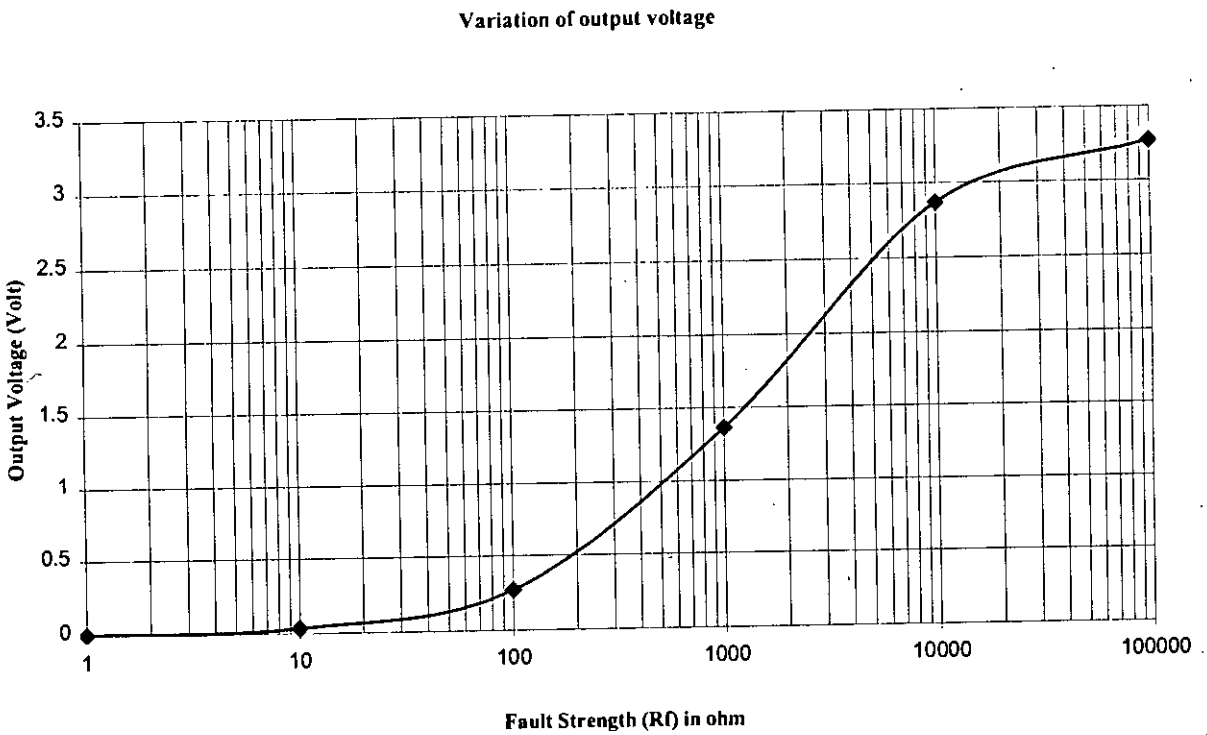


Fig 3.15 Output voltage vs. Fault Strength

(Stuck on fault for M_1 Test Vector 10 and M_2 Test Vector 01)

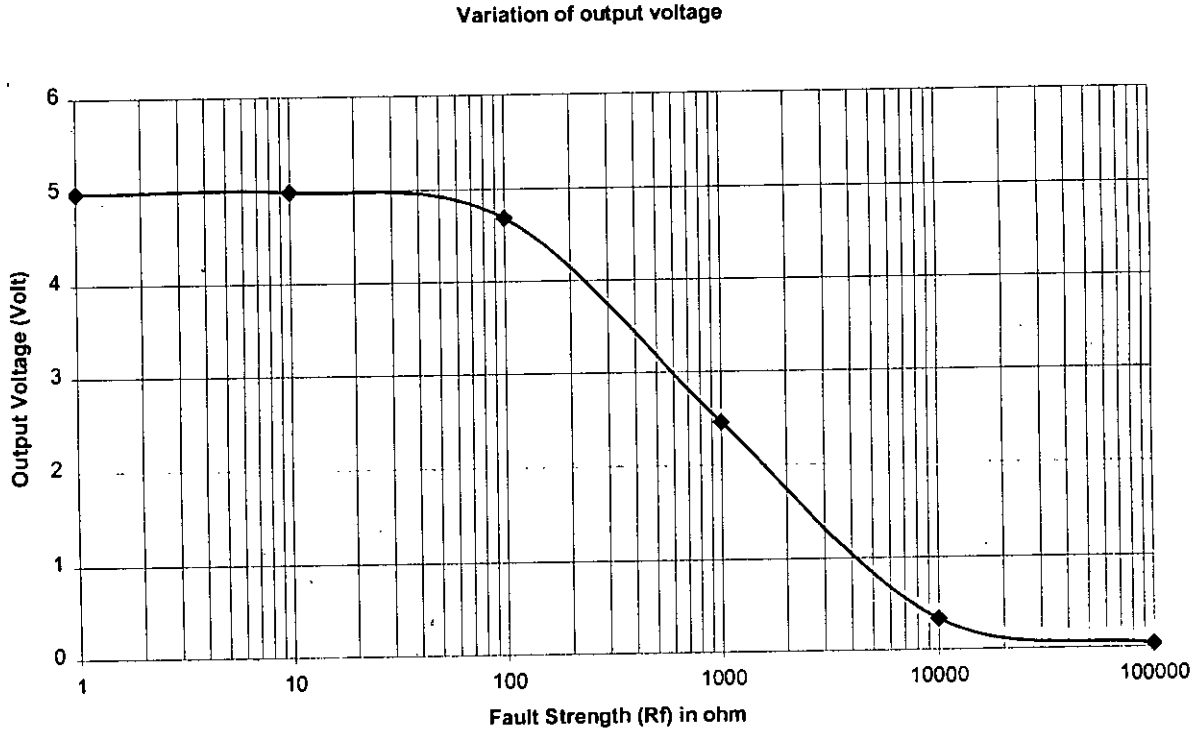


Fig 3.16 Output voltage vs. Fault Strength

(Stuck on fault for M_3 Test Vector 01 and M_4 Test Vector 10)

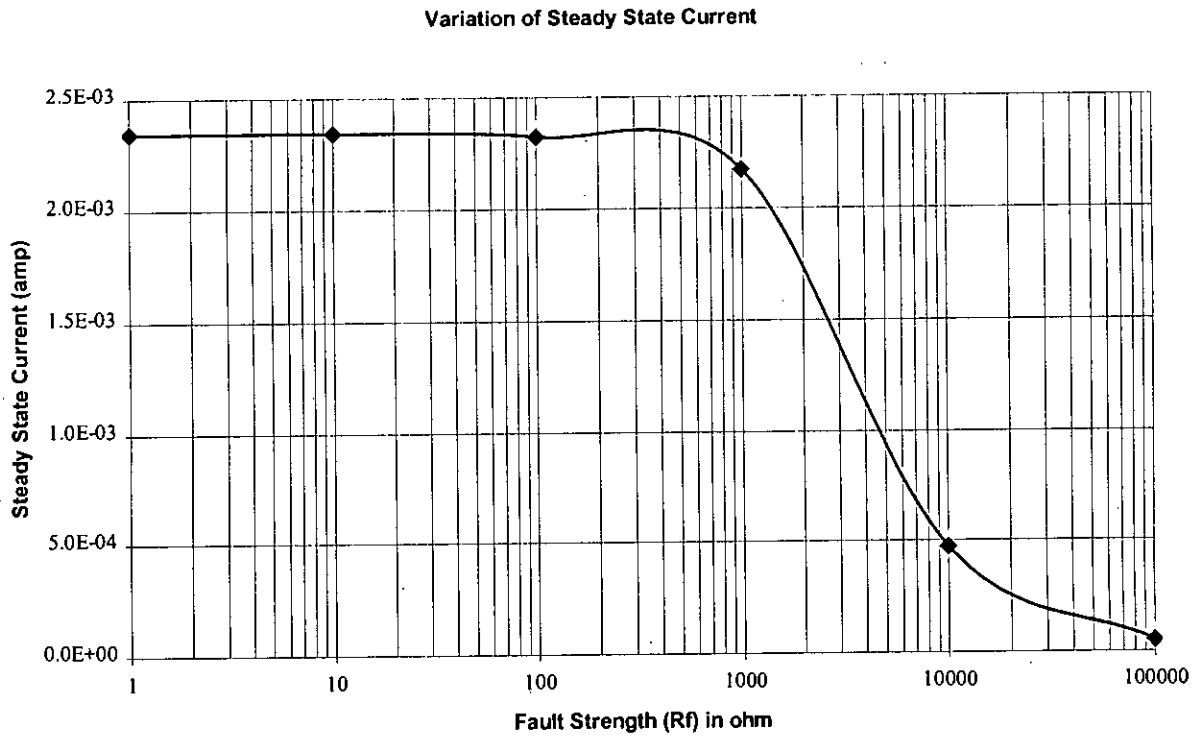


Fig 3.17 Steady State Current vs. Fault Strength

(Stuck on fault for M_1 and M_4 Test Vector 10)

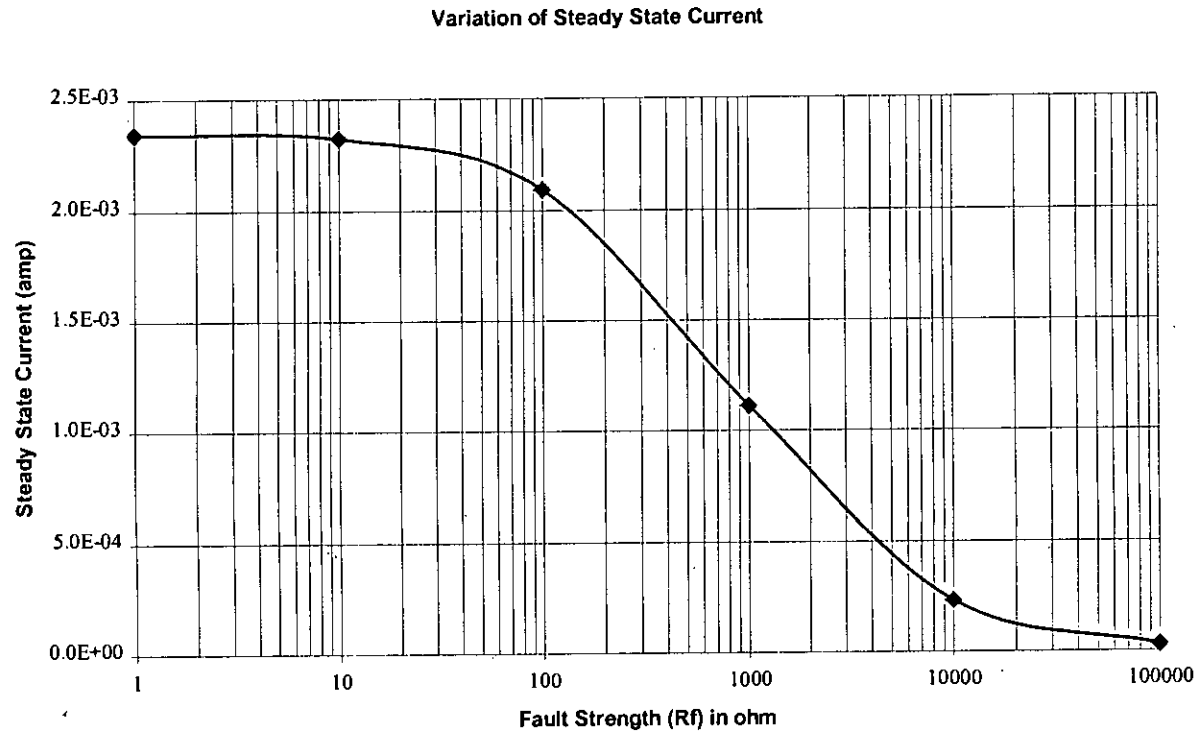


Fig 3.18 Steady State Current vs. Fault Strength

(Stuck on fault for M_2 and M_3 Test Vector 01)

Effects of Fault Resistance:

As seen from table 3.3, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 1 ohm to 100 kohm, the output voltage varies from o to 4.997 Volt. This appreciable variation in output voltage clearly shows that the output logic level is indeterminable. This agrees with our prediction that the fault cannot be detected by logic monitoring. As seen from the table, signal current is in the range of miliampere compared to normal operating current of 5pA. Therefore, the fault can be detected by current monitoring.

Table 3.4

The following table shows the summary for stuck on faults in CPL OR/NOR circuit.

Summary for Stuck-on faults in CPL OR/NOR Circuit

Fault	Test Vector	V_{out} (Volt)	I_{DDQ} (amp)	Logic Monitoring possible?	Current Monitoring possible?
M_1	(00)	0	0	No	No
	(01)	***0.003 to 3.267***	***2.346E-03 to 4.974E-05***	***No***	***Yes***
	(10)	5	5 pA	No	No
	(11)	5	0	No	No
M_2	(00)	0	0	No	No
	(01)	4.11	5 pA	No	No
	(10)	***002 to 2.943***	***2.34E-03 to 2.94E-05***	***No***	***Yes***
	(11)	5	0	No	No
M_3	(00)	5	0	No	No
	(01)	5	0	No	No
	(10)	***4.997 to 0.032***	***2.34E-03to 2.94E-05***	***No***	***Yes***
	(11)	0	0	No	No
M_4	(00)	5	0	No	No
	(01)	***4.997 to 0.032***	***2.34E-03 to 4.97E-05***	***No***	***Yes***
	(10)	0	5 pA	No	No
	(11)	0	0	No	No

3.3.5 Qualitative Analysis for CPL EXOR/EXNOR Circuit

M_1 : (stuck on fault in M_1 of the CPL EXOR/EXNOR gate of figure 2.3)

The fault is modeled by placing a variable resistance R_f between source and drain terminal of the faulted MOS. The tests vectors (0,0), and (1,0) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, when the vector (0,1) & (1,1) is applied a large current flows in the circuit.

Test Vector 01:

For the vector of (0,1) (figure 3.19), M_2 turns ON and a large current flows through the circuit. The output voltage

$$V_{out} = \{R_f/(R_f+R_{on})\}V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the stuck on fault at M_1 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring i.e. I_{DDQ} Testing.

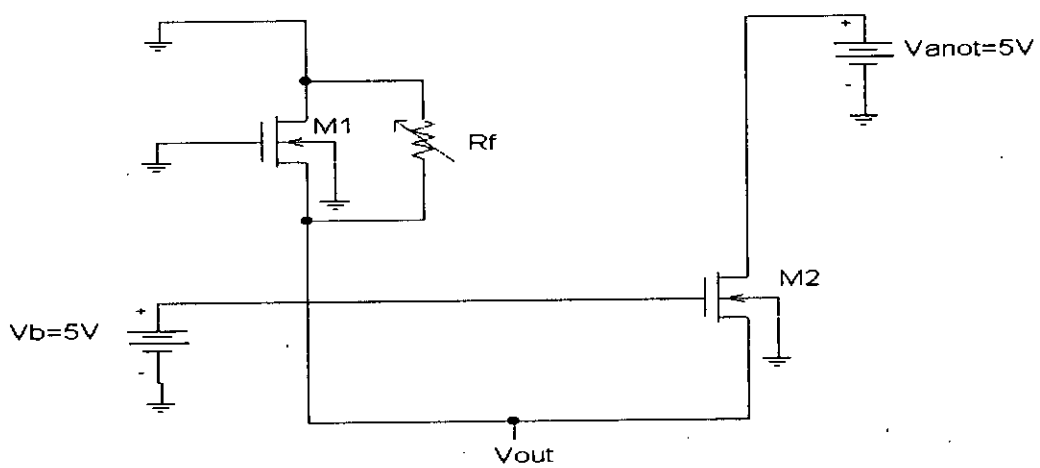


Fig. 3.19: Simulation circuit for stuck on fault in M_1 of the CPL EXOR/EXNOR gate for test vector [A=0, B=1]

Test Vector 11:

For the vector of (1,1) in figure 3.20, M_2 turns ON and a large current flows through the circuit. The output voltage

$$V_{out} = \{R_{on}/(R_f+R_{on})\}V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the stuck on fault at M_1 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring i.e. I_{DDQ} Testing.

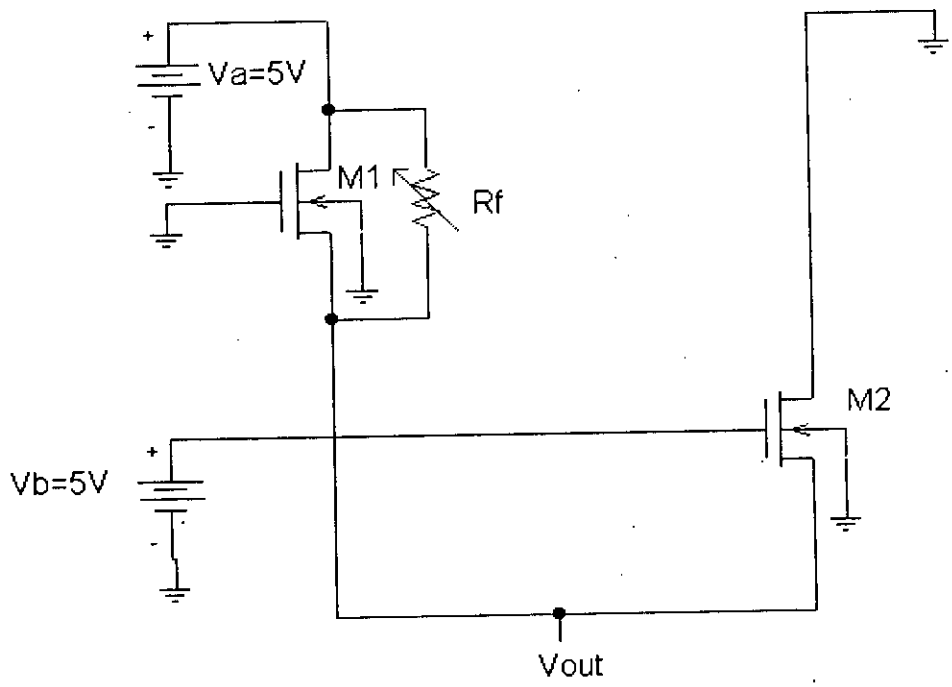


Fig. 3.20 Simulation circuit for stuck on fault in M_1 of the CPL EXOR /EXNOR gate for test vector [A=0, B=1]

M_2 : (stuck on fault in M_2 of the CPL EXNOR/EXOR gate of figure 2.3)

The tests vectors (0,1) and (1,1) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, when the vector (0,0) and (1,0) is applied large steady state current flows in the circuit. The expression for voltage and current are similar to previous case. The SPICE simulation result is presented in the table at the end of this article.

M_3 : (stuck on fault in M_3 of the CPL EXOR/EXNOR gate of figure 2.3)

The tests vectors (0,1) and (1,1) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, when the vector (0,0) and (1,0) is applied large steady state current flows in the circuit. The expression for voltage and current are similar to previous case. The SPICE simulation result is presented in the table at the end of this article.

M_4 : (stuck-on fault in M_4 of the CPL EXOR/EXNOR gate of figure 2.3)

The tests vectors (0,0), and (1,0) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, when the vector (0,1) and (1,1) are applied large steady state current flows in the circuit. The expression for voltage and current are similar to previous case. The SPICE simulation result is presented in the table at the end of this article.

3.3.6 SPICE Simulation Results for Stuck on Fault for CPL EXOR/EXNOR Circuit

This section summarizes the SPICE simulation results for a single stuck on fault in the MOS devices of the CPL EXOR/EXNOR logic gates.

Table 3.5

SPICE Simulation results for stuck on faults in CPL EXOR/EXNOR gate.

Effect of fault strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
		V_a	V_b		
M_1	1	0	5	0.026	3.048E-03
	10	0	5	0.028	3.004E-03
	100	0	5	0.266	2.666E-03
	1K	0	5	1.365	1.363E-03
	10K	0	5	2.824	2.855E-04
	100K	0	5	3.941	2.955E-05
	1	5	5	4.997	3.053E-03
	10	5	5	4.976	3.053E-03
	100	5	5	4.692	3.053E-03
	1K	5	5	2.446	2.551E-03
	10K	5	5	0.004	4.672E-04
	100K	5	5	0	4.974E-05
M_2	1	0	0	4.997	3.053E-03
	10	0	0	4.976	3.053E-03
	100	0	0	4.692	3.053E-03
	1K	0	0	2.446	2.551E-03
	10K	0	0	0.004	4.672E-04
	100K	0	0	0	4.974E-05
	1	5	0	0.026	3.048E-03
	10	5	0	0.028	3.004E-03
	100	5	0	0.266	2.666E-03
	1K	5	0	1.365	1.363E-03
	10K	5	0	2.824	2.855E-04
	100K	5	0	3.941	2.955E-05

Table 3.5 (Cond)

SPICE Simulation results for stuck on faults in CPL EXOR/EXNOR gate.

Effect of fault strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
		V_a	V_b		
M_3	1	0	0	0.026	3.048E-03
	10	0	0	0.028	3.004E-03
	100	0	0	0.266	2.666E-03
	1K	0	0	1.365	1.363E-03
	10k	0	0	2.824	2.855E-04
	100k	0	0	3.941	2.955E-05
	1	5	0	4.997	3.053E-03
	10	5	0	4.976	3.053E-03
	100	5	0	4.692	3.053E-03
	1K	5	0	2.446	2.551E-03
	10k	5	0	0.004	4.672E-04
	100k	5	0	0	4.974E-05
M_4	1	0	5	4.997	3.053E-03
	10	0	5	4.976	3.053E-03
	100	0	5	4.692	3.053E-03
	1K	0	5	2.446	2.551E-03
	10k	0	5	0.004	4.672E-04
	100k	0	5	0	4.974E-05
	1	5	5	0.026	3.048E-03
	10	5	5	0.028	3.004E-03
	100	5	5	0.266	2.666E-03
	1k	5	5	1.365	1.363E-03
	10k	5	5	2.824	2.855E-04
	100k	5	5	3.941	2.955E-05

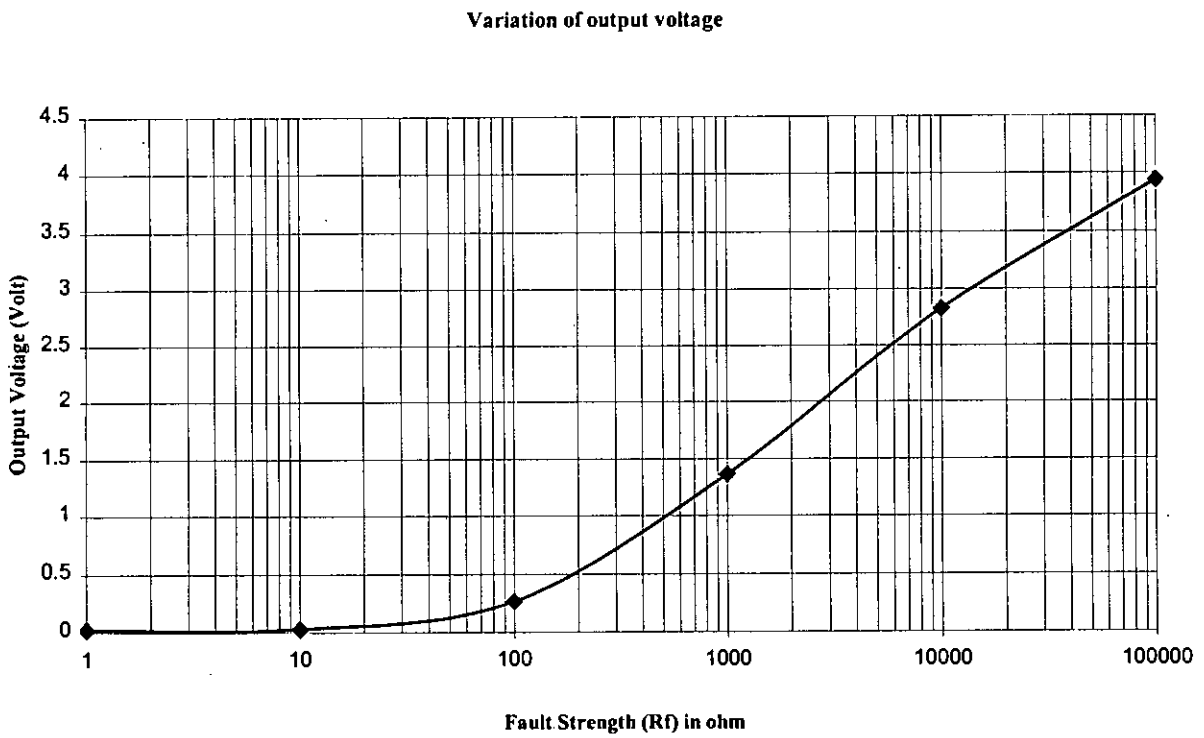


Fig 3.21 Output Voltage vs. Fault Strength

(Stuck on fault for M_1 (01), M_2 (10), M_3 (00) and M_4 (11))

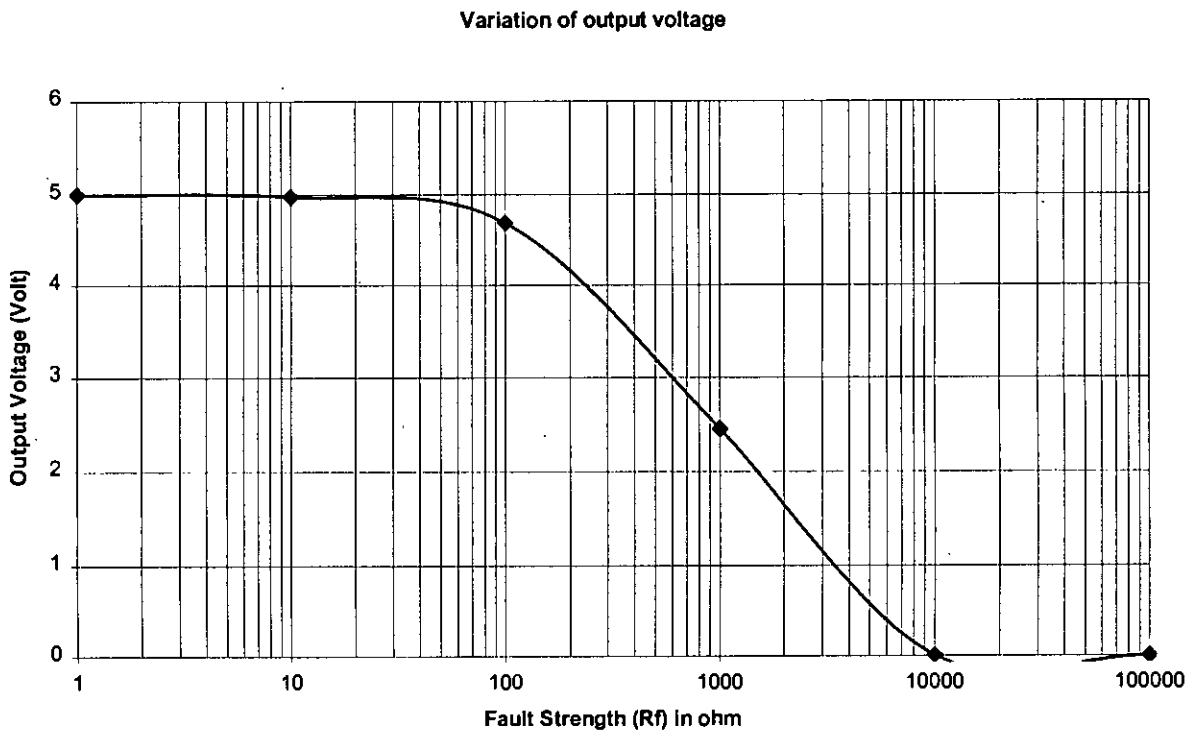


Fig 3.22 Output Voltage vs. Fault Strength

(Stuck on fault for M_1 (11), M_2 (00), M_3 (10) and M_4 (01))

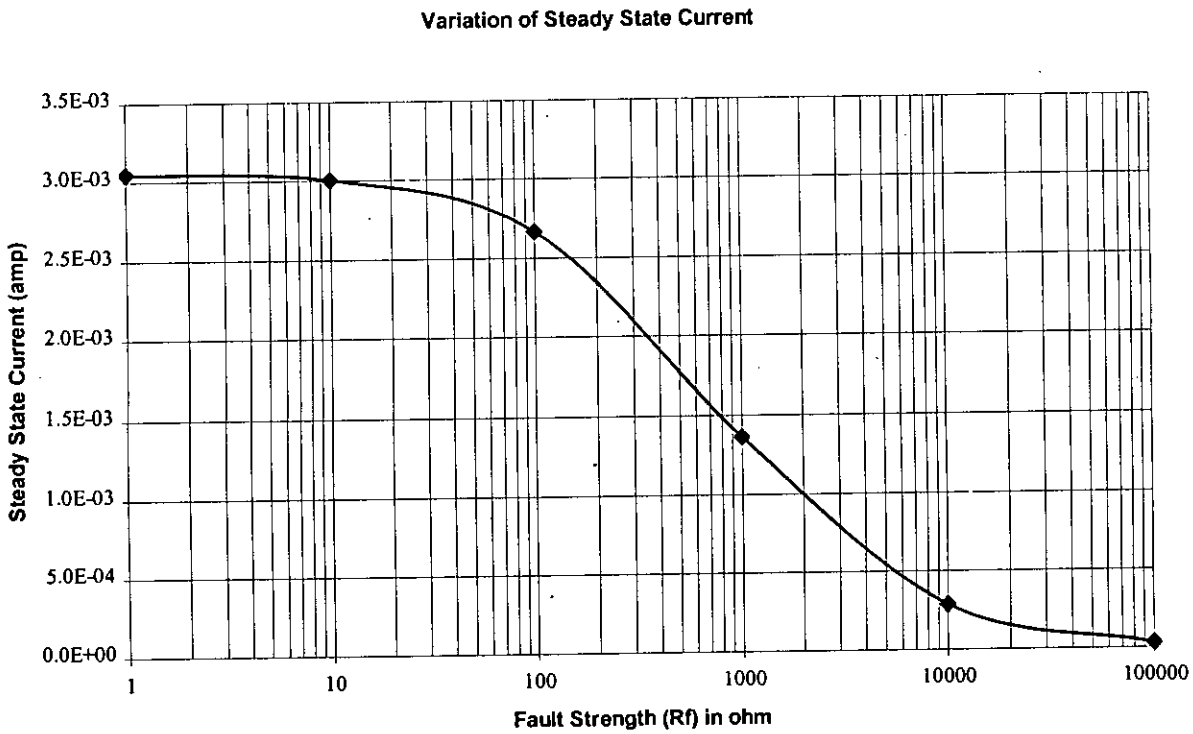


Fig 3.23 Steady State Current vs. Fault Strength
(Stuck on fault for M_1 (01), M_2 (10), M_3 (00) and M_4 (11))

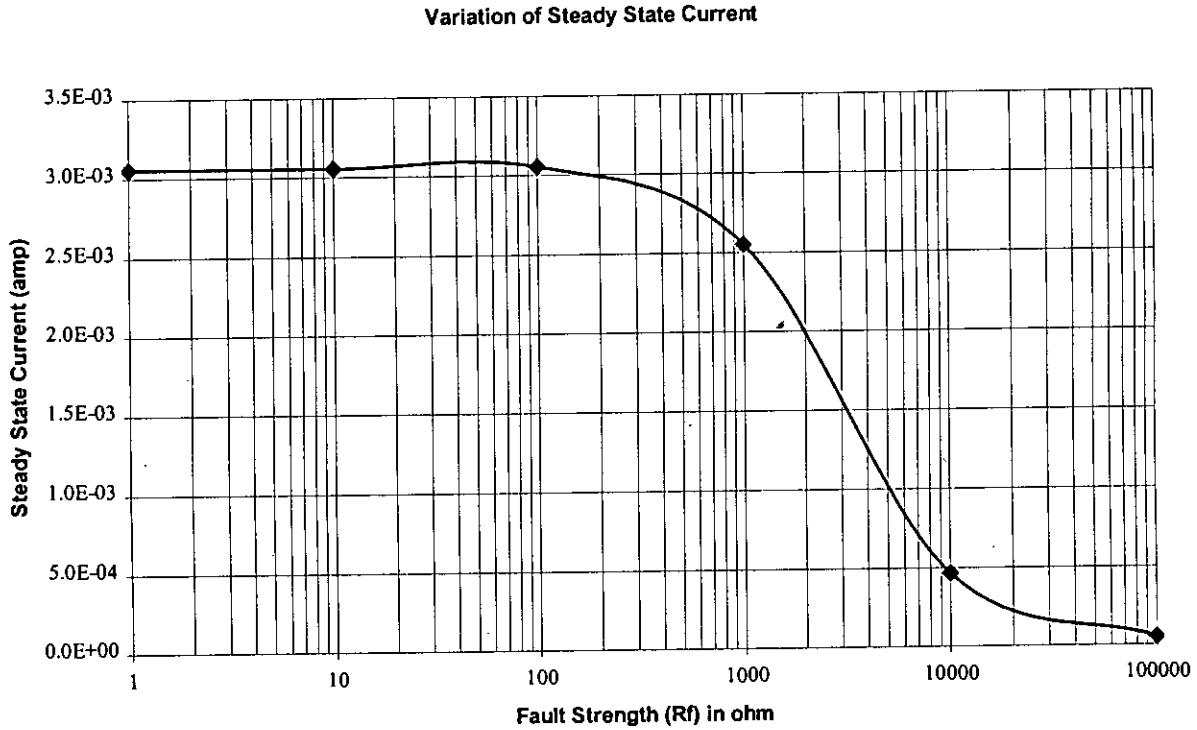


Fig 3.24 Steady State Current vs. Fault Strength
(Stuck on fault for M_1 (11), M_2 (00), M_3 (10) and M_4 (01))

Effects of Fault Resistance:

As seen from table 3.5, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 1 Ω to 100 kΩ, the output voltage varies from 0 to 4.9766 Volt. This appreciable variation in output voltage clearly shows that the output logic level is indeterminable. This agrees with our prediction that the fault cannot be detected by logic monitoring. As seen from the table, signal current is in the range of miliampere compared to normal operating current of 5pA. Therefore, the fault can be detected by current monitoring.

Table 3.6

The following table shows the summary for stuck on faults in CPL EXOR/EXNOR circuit.

Summary for Stuck on faults in CPL EXOR/EXNOR Ckt:

Fault	Test Vector	V_{out} (Volt)	I_{DDQ} (amp)	Logic Monitoring possible?	Current Monitoring possible?
M_1	(00)	0	0	No	No
	(01)	***0.026 to 3.49***	***3.04E-3 to 2.955E-5***	***No***	***Yes***
	(10)	5	0	No	No
	(11)	***4.997 to 0***	***3.053E-3 to 4.97E-5***	***No***	***Yes***
M_2	***(00)***	***4.997 to 0***	***3.053E-3 to 4.97E-5***	***No***	***Yes***
	(01)	5	0	No	No
	(10)	***0.026 to 3.49***	***3.04E-3 to 2.955E-5***	***No***	***Yes***
	(11)	0	0	No	No
M_3	***(00)***	***0.026 to 3.49***	***3.04E-3 to 2.955E-5***	***No***	***Yes***
	(01)	0	0	No	No
	(10)	***4.997 to 0***	***3.05E-3 to 4.974E-5***	***No***	***Yes***
	(11)	5	0	No	No
M_4	(00)	5	0	No	No
	(01)	***4.997 to 0***	***3.05E-3 to 4.974E-5***	***No***	***Yes***
	(10)	0	0	No	No
	(11)	***0.026 to 3.49***	***3.04E-3 to 2.955E-5***	***No***	***Yes***

3.4 Behavior Under Single Bridging Faults:

A bridging fault is defined as a fault which connects two or more signal lines in the circuit. In CPL circuit this fault may occur due to thin oxide short causing a short circuit between the gate and the source / drain region of the MOS transistor. Since gate and source / drain are connected to different signal this will cause a bridging fault. Here we have considered two types of bridging faults; (i) bridging fault between gate and source and (ii) bridging fault between gate and drain. Now in a MOS transistor the source and the drain terminal are relative and work interchangeably depending on relative polarity of their voltage. On the other hand in CPL circuits, there are two set of input :One horizontal input set connected to the gate. This is referred to as complementary gate input. The other is the vertical input set coming from the top and connected to the MOS source or drain terminal. But it is customary to refer this input set as drain input. We therefore consider the top vertical terminal of the MOS symbol in CPL circuits of Fig. 2.1 to 2.5 as drain and the bottom vertical terminal as source.

3.4.1 Qualitative Analysis for CPL AND/NAND Circuit

M_1 : (bridging fault in M_1 of the CPL AND/NAND gate of figure 2.1)

The fault is modeled in figure 3.25 by placing a resistor between the gate and source terminal of the faulted MOS M_2. The tests vectors (0,0), (1,0) and (1,1) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, when the vector (0,1) is applied, M_1 turns ON and a large current flows through R_f and M_1 of the circuit. The output voltage is

$$V_{out} = \{R_{on}/(R_f+R_{on})\}V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the bridging fault at M_1 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring i.e. I_{DDQ} Testing.

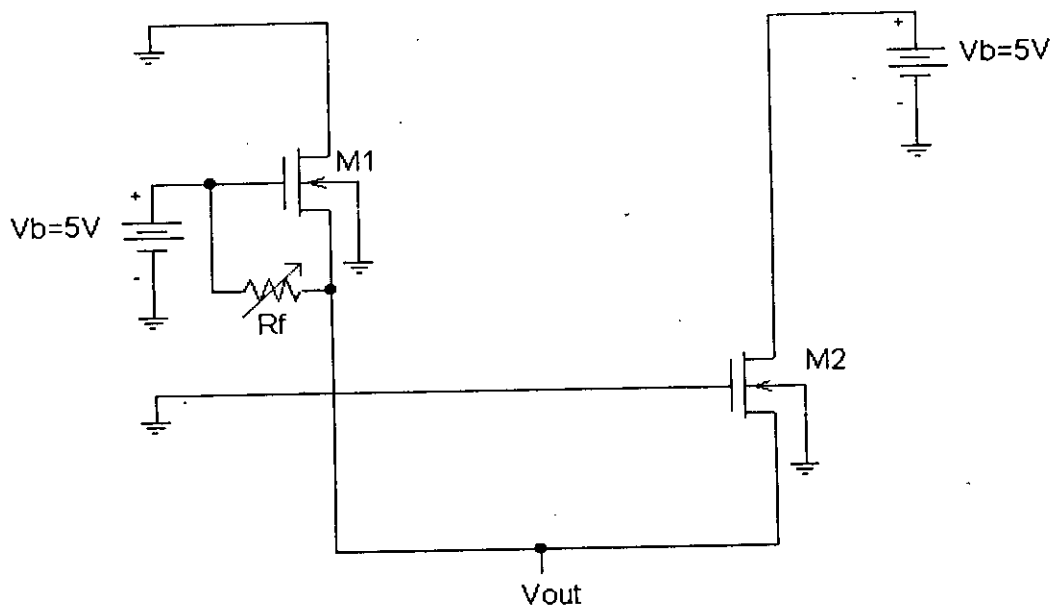


Fig. 3.25 Simulation circuit for gate to source bridging fault on MOS M_1 of basic CPL AND circuit for test vector [A=0, B=1]

M_2 : (bridging fault in M_2 of the CPL AND/NAND gate of figure 2.1)

Similar analysis have been done for gate to source bridging fault on MOS M_2 of CPL AND/NAND circuit. The tests vectors (0,1) produce correct logic and no significant current flows in the circuit when this test vector is applied. Hence these vectors are incapable of detecting the fault. However, when the vector (0,0), (1,0) and (1,1) are applied, large steady state current flows and the fault can be detected by current monitoring. However, the output voltage varies from 0 to V_{IH} depending on the fault strength and hence the fault can not be detected by logic monitoring. The expression for output voltage and steady state current are similar to the previous case. The SPICE simulation results are summarized in the tables.

M_3 : (bridging fault in M_3 of the CPL AND/NAND gate of figure 2.1)

The fault is modeled in figure 3.26. The tests vectors (0,0), (1,0) and (1,1) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. However, when the vector (0,1) is applied, M_4 turns ON and a large current flows through the circuit. The output voltage is

$$V_{out} = \{R_f/(R_f+R_{on})\} V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from

0 to V_{IH} depending on R_f, hence the bridging fault at M_3 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is

$$I = V_{IH}/(R_f+R_{on})$$

Hence, the fault can be detected by current monitoring i.e. I_{DDQ} Testing.

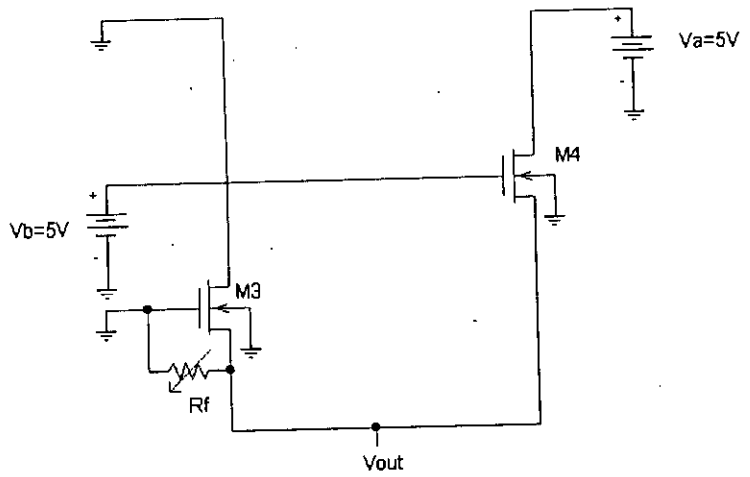


Fig. 3.26. Simulation circuit for gate to source bridging fault on MOS M_3 of basic CPL AND circuit for test vector [A=0, B=1].

M_4 : (bridging fault in M_4 of the CPL AND/NAND gate of figure 2.1)

The tests vectors (0,1) produce correct logic and no significant current flows in the circuit when this test vector is applied. Hence these vectors are incapable of detecting the fault. However, when the vector (0,0), (1,0) and (1,1) are applied, the fault can be detected by current monitoring but no logic monitoring is possible. The expression for output voltage and steady state current are similar to the previous case. The SPICE simulation results are summarized in the tables.

3.4.2 SPICE Simulation Bridging Fault Results for CPL AND/NAND Circuit

This section summarizes the SPICE simulation results for a single bridging fault in the MOS devices of the CPL AND/NAND logic gates.

Table 3.7

SPICE Simulation results for bridging faults in CPL AND/NAND Ckt.

Effect of fault strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
		V_a	V_b		
M_1	1	0	5	4.997	3.053E-03
	10	0	5	4.996	3.053E-03
	100	0	5	4.692	3.053E-03
	1K	0	5	2.446	2.551E-03
	10K	0	5	0.327	4.672E-04
	100K	0	5	0.030	4.015E-05
M_2	1	0	0	4.997	3.053E-03
	10	0	0	4.996	3.053E-03
	100	0	0	4.692	3.053E-03
	1K	0	0	2.446	2.551E-03
	10K	0	0	0.327	4.672E-04
	100K	0	0	0.030	4.015E-05
	1	5	0	4.997	3.053E-03
	10	5	0	4.996	3.053E-03
	100	5	0	4.692	3.053E-03
	1K	5	0	2.446	2.551E-03
	10K	5	0	0.327	4.672E-04
	100K	5	0	0.030	4.015E-05
	1	5	5	0.003	3.048E-03
	10	5	5	0.033	3.000E-03
	100	5	5	0.269	2.666E-03
	1K	5	5	1.365	1.363E-03
	10K	5	5	2.865	2.855E-04
	100K	5	5	4.325	3.048E-05

Table 3.7

SPICE Simulation results for bridging faults in CPL AND/NAND Ckt.

Effect of fault strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
		V_a	V_b		
M_3	1	0	5	0.003	3.048E-03
	10	0	5	0.030	3.000E-03
	100	0	5	0.269	2.666E-03
	1K	0	5	1.365	1.363E-03
	10K	0	5	2.865	2.855E-04
	100K	0	5	4.325	3.048E-05
M_4	1	0	0	0.003	3.048E-03
	10	0	0	0.030	3.000E-03
	100	0	0	0.269	2.666E-03
	1K	0	0	1.365	1.363E-03
	10K	0	0	2.865	2.855E-04
	100K	0	0	4.325	3.048E-05
	1	5	0	0.003	3.048E-03
	10	5	0	0.030	3.000E-03
	100	5	0	0.269	2.666E-03
	1K	5	0	1.365	1.363E-03
	10K	5	0	2.865	2.855E-04
	100K	5	0	4.325	3.048E-05
	1	5	5	4.997	3.053E-03
	10	5	5	4.996	3.053E-03
	100	5	5	4.692	3.053E-03
	1K	5	5	2.446	2.551E-03
	10K	5	5	0.327	4.672E-04
	100K	5	5	0.030	4.015E-05

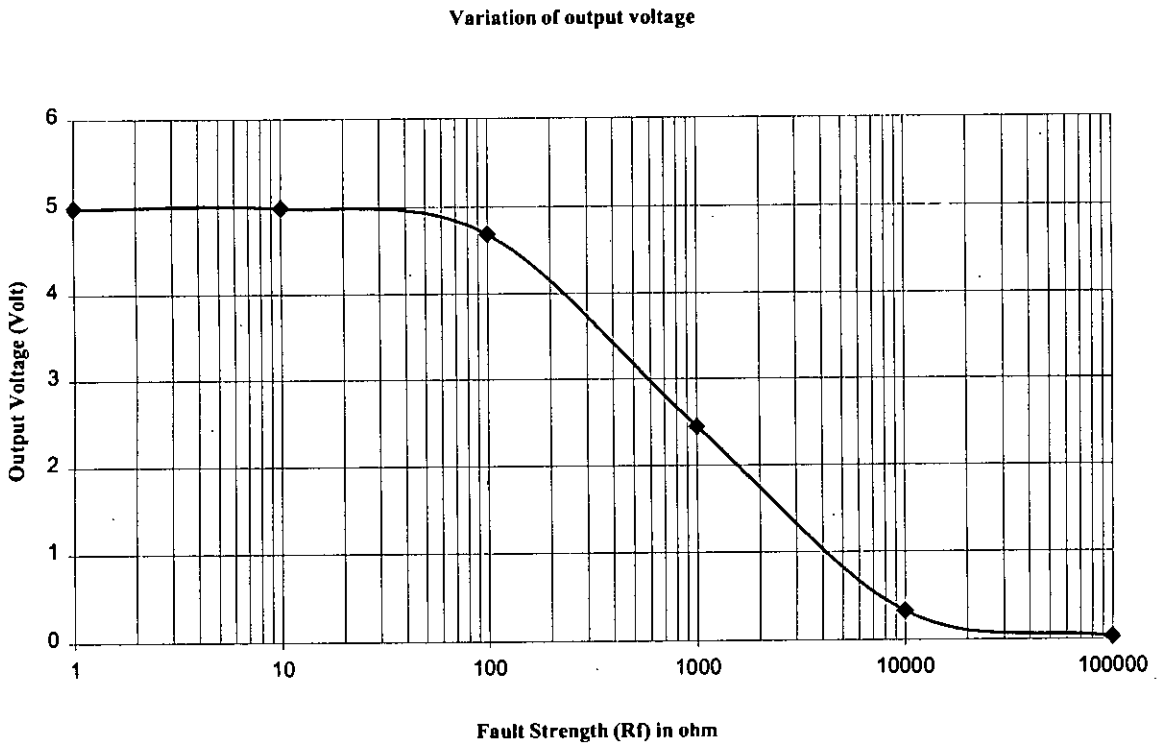


Fig 3.27 Output voltage vs. Fault strength

(Bridging fault for M_1 (01), M_2 (00)(10) and M_4 (11))

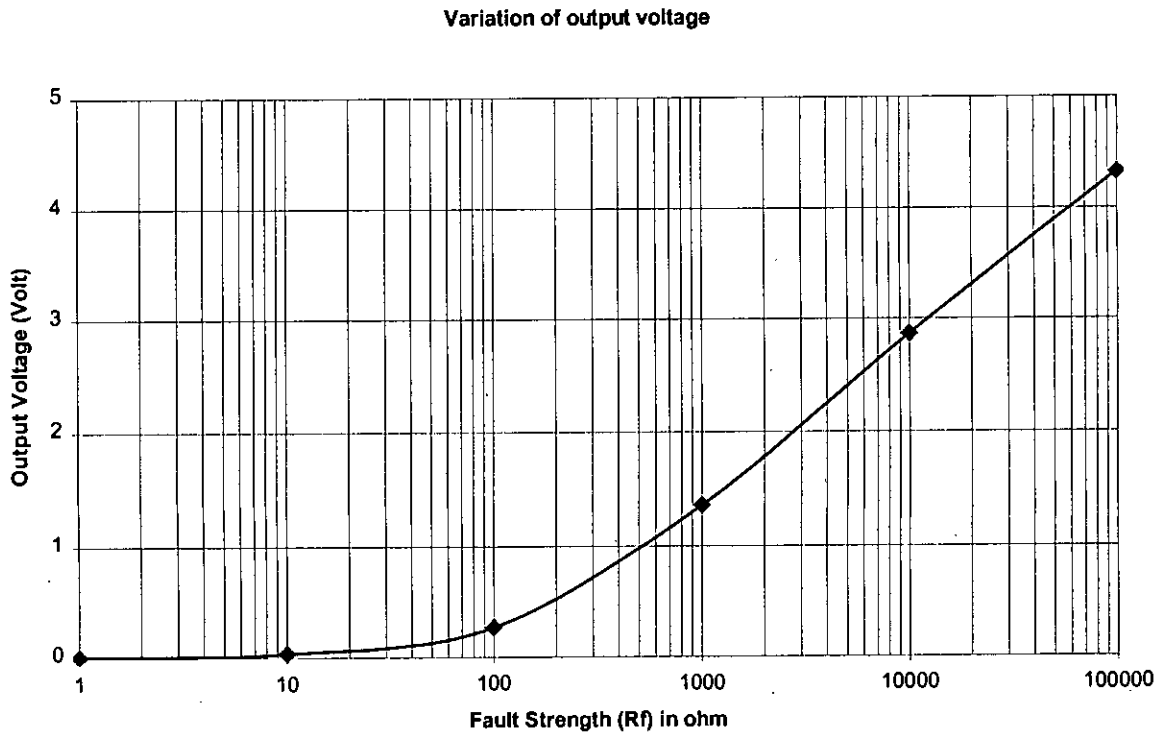


Fig 3.28 Output voltage vs. Fault strength

(Stuck on fault for M_2 (11), M_3 (01) and M_4 (00)(10))

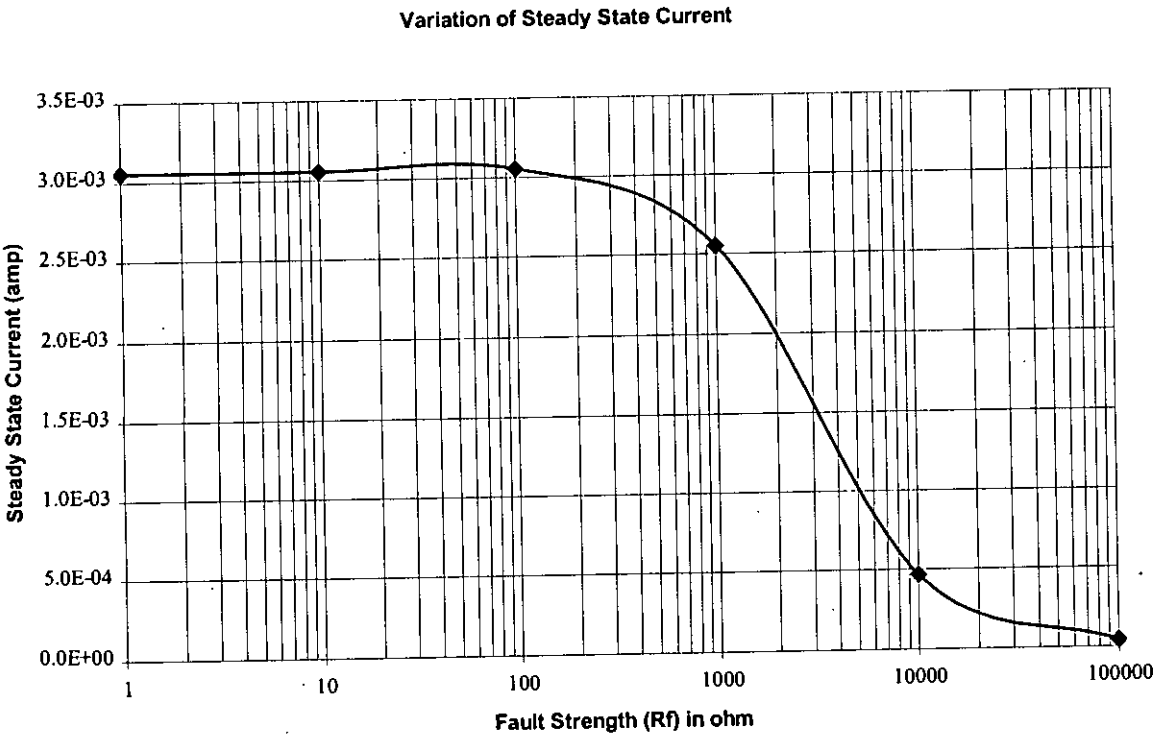


Fig 3.29 Steady State Current vs. Fault strength
(Bridging fault for M_1 (01), M_2 (00)(10) and M_4 (11))

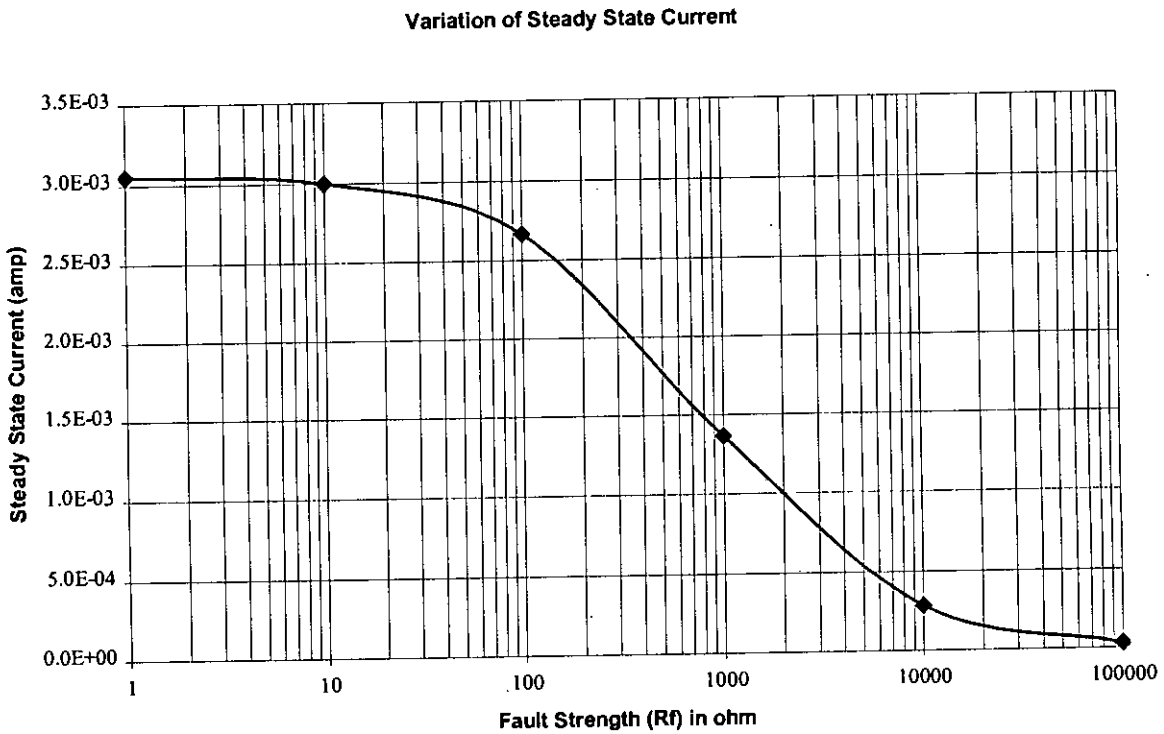


Fig 3.30 Steady State Current vs. Fault strength
(Stuck on fault for M_2 (11), M_3 (01) and M_4 (00)(10))

Effects of Fault Resistance:

As seen from table 3.7, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 1 Ω to 100 kΩ, the output voltage varies from 0.03 to 4.997 Volt. This appreciable variation in output voltage clearly shows that the output logic level is indeterminable. This agrees with our prediction that the fault cannot be detected by logic monitoring. As seen from the table, signal current is in the range of miliampere compared to normal operating current of 5 pA. Therefore, the fault can be detected by current monitoring.

Table 3.8

The following table shows the summary for bridging faults in CPL AND/NAND circuit.

Summary for bridging faults in CPL NAND/AND Circuit

Fault	Test Vector	V_{out} (Volt)	I_{DDQ} (amp)	Logic Monitoring possible?	Current Monitoring possible?
M_1	(00)	0	0	NO	NO
	(01)	*4.997 to 0.03*	*3.053E-03 to 4.015E-05*	*NO*	*YES*
	(10)	4.9	5pa	NO	NO
	(11)	5	0	NO	NO
M_2	*(00)*	*4.997 to 0.03*	*3.053E-03 to 4.015E-05*	*NO*	*YES*
	(01)	4.9	5pa	NO	NO
	(10)	*4.997 to 0.03*	*3.053E-03 to 4.015E-05*	*NO*	*YES*
	(11)	*0.03 to 4.325*	*3.048E-03 to 3.048E-05*	*NO*	*YES*
M_3	(00)	5	0	NO	NO
	(01)	*0.03 to 4.325*	*3.048E-03 to 3.048E-05*	*NO*	*YES*
	(10)	5	5pa	NO	NO
	(11)	0	0	NO	NO
M_4	*(00)*	*0.03 to 4.325*	*3.048E-03 to 3.048E-05*	*NO*	*YES*
	(01)	5	5pa	NO	NO
	(10)	*0.03 to 4.325*	*3.048E-03 to 3.048E-05*	*NO*	*YES*
	(11)	*4.997 to 0.03*	*3.053E-03 to 4.015E-05*	*NO*	*YES*

3.4.3 Qualitative Analysis for CPL OR/NOR Circuit:

M_1 : (bridging fault in M_1 of the CPL OR/NOR gate of figure 2.2)

The fault is modeled in figure 3.31, 3.32 and 3.33 where the faulted MOS is replaced by a variable resistance R_f. The test vector (1,0) produces correct logic and no significant current flows in the circuit when this test vectors are applied. Hence this vector is incapable of detecting the fault. However, when the vector (0,0), (0,1) and (1,1) are applied, a large current flows through the circuit.

Test Vector 00:

The output voltage is

$$V_{out} = \{R_{on}/(R_f+R_{on})\}V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the bridging fault at M_1 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f+R_{on})$$

Hence, the fault can be detected by current monitoring i.e. I_{DDQ} Testing.

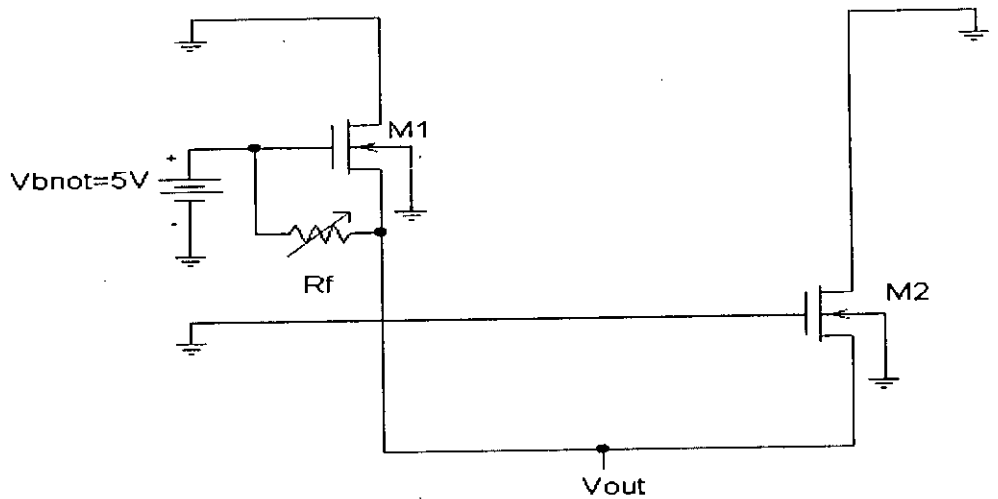


Fig. 3.31 Simulation circuit for gate to source bridging fault on MOS M_1 of basic CPL OR/NOR circuit for test vector [A=0, B=0].

Test Vector 01:

The output voltage is

$$V_{out} = \{R_f/(R_f+R_{on})\} V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the bridging fault at M_1 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring i.e. I_{DDQ} Testing.

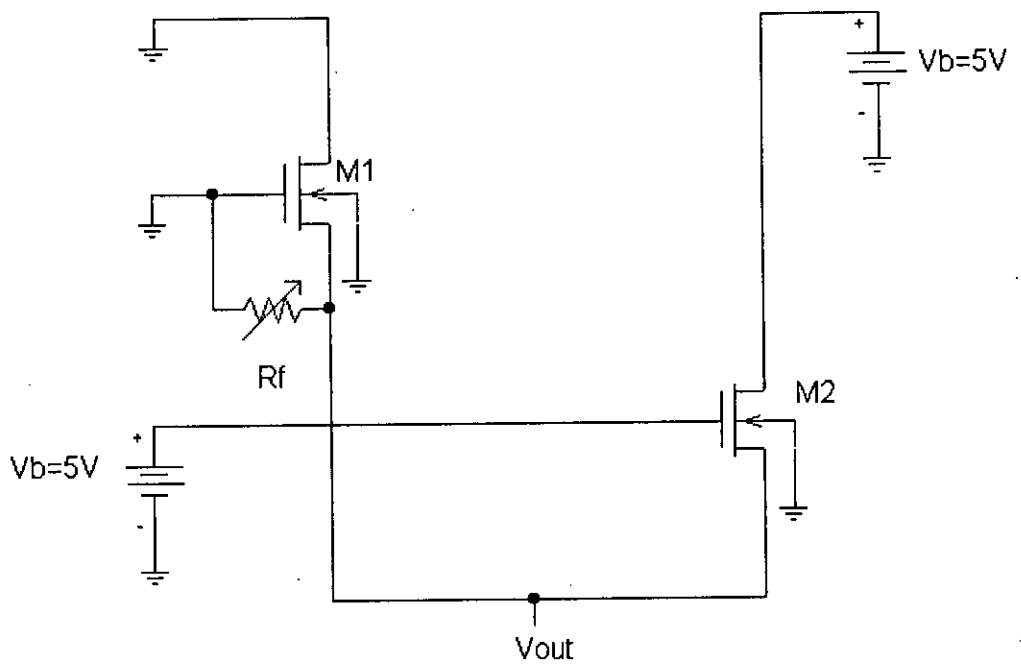


Fig. 3.32 Simulation circuit for gate to source bridging fault on MOS M_1 of basic CPL OR/NOR circuit for test vector [A=0, B=1].

Test Vector 11:

The output voltage is

$$V_{out} = \{R_f/(R_f+R_{on})\} V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the bridging fault at M_1 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring i.e. I_{DDQ} Testing.

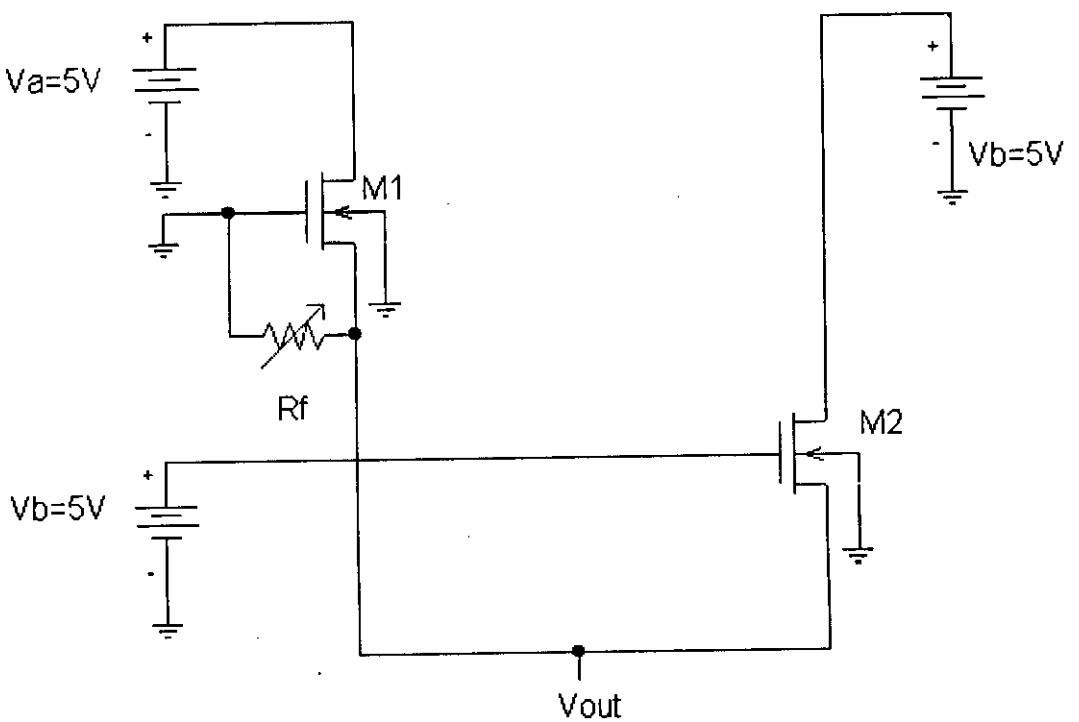


Fig. 3.33 Simulation circuit for gate to source bridging fault on MOS M_1 of basic CPL OR/NOR circuit for test vector [A=1, B=1].

M_2 : (bridging fault in M_2 of the CPL OR/NOR gate of figure 2.2)

Similar qualitative analysis have been done for bridging fault on MOS M_2 of CPL OR/NOR gate The test vector (0,0), (0,1) and (1,1) produces correct logic and no significant current flows in the circuit when this test vectors are applied. Hence this vector is incapable of detecting the fault. However, when the vector (1,0) is applied, a large current flows through the circuit. The current and voltage expression are similar to previous case. SPICE simulation results are summarized in the tables at the end of this article.

M_3 : (bridging fault in M_3 of the CPL OR/NOR gate of figure 2.2)

Similar qualitative analysis have been done for bridging fault on MOS M_3 of CPL OR/NOR gate The fault is modeled by placing a variable resistance R_f. The test vector (1,0) produces correct logic and no significant current flows in the circuit when this test vectors are applied. Hence this vector is incapable of detecting the fault. However, when the vector (0,0), (0,1) and (1,1) are applied, a large current I_{DDQ} flows through the circuit. The current and voltage expression are similar to previous case. SPICE simulation results are summarized in the tables at the end of this article.

M_4 : (bridging fault in M_4 of the CPL NOR/OR gate of figure 2.2)

Similar qualitative analysis is also done for bridging fault on MOS M_4 of CPL OR/NOR gate The test vectors (0,0), (0,1) and (1,1) produces correct logic and no significant current flows in the circuit when this test vectors are applied. Hence this vector is incapable of detecting the fault. However, when the vector (1,0) is applied, a large current flows through the circuit. The current and voltage expression are similar to previous case. SPICE simulation results are summarized in the tables at the end of this article.

3.4.4 SPICE Simulation Bridging Fault Results for CPL OR/NOR Gate

This section summarizes the SPICE simulation results for a single bridging fault in the MOS devices of the CPL OR/NOR logic gates.

Table 3.9

SPICE Simulation results for bridging faults in CPL OR/NOR Ckt.

Effect of fault strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
		V_a	V_b		
M_1	1	0	0	4.997	3.053E-03
	10	0	0	4.996	3.053E-03
	100	0	0	4.692	3.053E-03
	1K	0	0	2.446	2.551E-03
	10K	0	0	0.327	4.672E-04
	100K	0	0	0.031	4.462E-05
	1	0	5	0.003	3.048E-03
	10	0	5	0.033	3.004E-03
	100	0	5	0.269	2.666E-03
	1K	0	5	1.365	1.366E-03
	10K	0	5	2.865	2.855E-04
	100K	0	5	3.892	3.140E-05
	1	5	5	0.003	3.048E-03
	10	5	5	0.033	3.004E-03
	100	5	5	0.269	2.666E-03
	1K	5	5	1.365	1.366E-03
	10K	5	5	2.865	2.855E-04
	100K	5	5	3.892	3.140E-05
M_2	1	5	0	0.003	3.048E-03
	10	5	0	0.033	3.004E-03
	100	5	0	0.269	2.666E-03
	1K	5	0	1.365	1.366E-03
	10K	5	0	2.865	2.855E-04
	100K	5	0	3.892	3.140E-05

Table 3.9

SPICE Simulation results for bridging faults in CPL OR/NOR Ckt.

Effect of fault strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
		V_a	V_b		
M_3	1	0	0	0.003	3.048E-03
	10	0	0	0.033	3.004E-03
	100	0	0	0.269	2.666E-03
	1K	0	0	1.365	1.366E-03
	10K	0	0	2.865	2.855E-04
	100K	0	0	3.892	3.140E-05
	1	0	5	4.997	3.053E-03
	10	0	5	4.996	3.053E-03
	100	0	5	4.692	3.053E-03
	1K	0	5	2.446	2.551E-03
	10K	0	5	0.327	4.672E-04
	100K	0	5	0.031	4.462E-05
	1	5	5	4.997	3.053E-03
	10	5	5	4.996	3.053E-03
	100	5	5	4.692	3.053E-03
	1K	5	5	2.446	2.551E-03
	10K	5	5	0.327	4.672E-04
	100K	5	5	0.031	4.462E-05
M_4	1	5	0	4.997	3.053E-03
	10	5	0	4.996	3.053E-03
	100	5	0	4.692	3.053E-03
	1K	5	0	2.446	2.551E-03
	10K	5	0	0.327	4.672E-04
	100K	5	0	0.031	4.462E-05

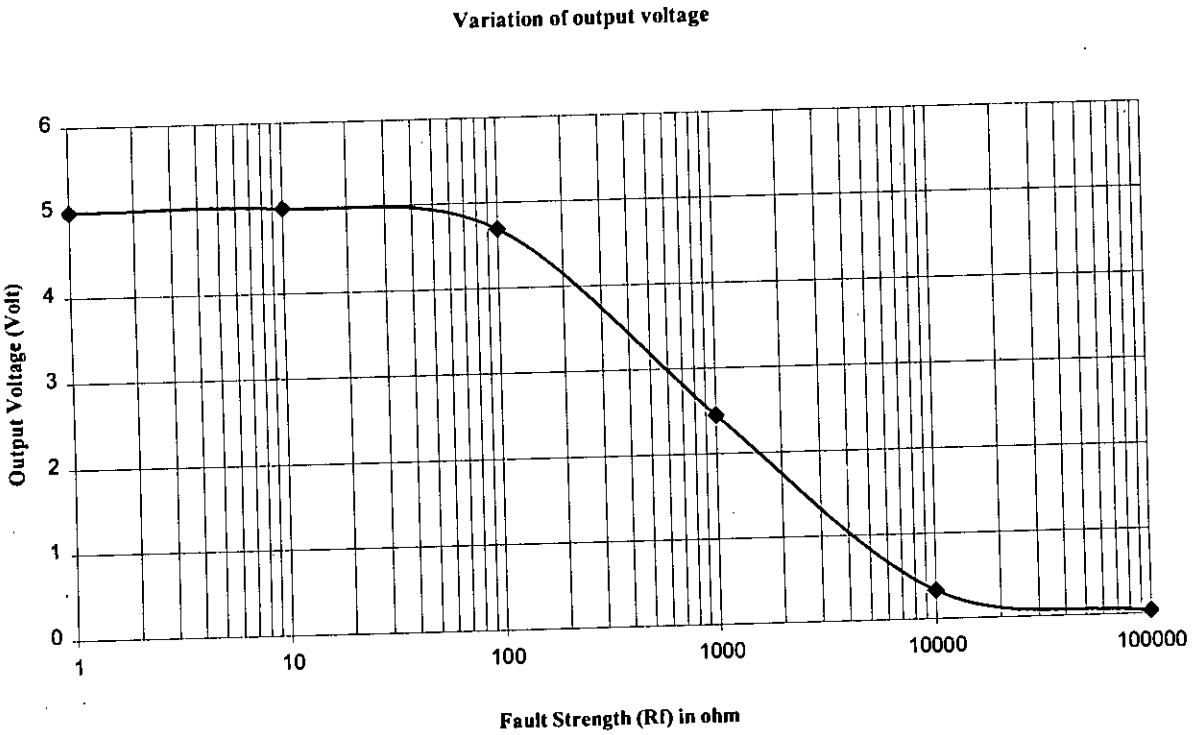


Fig 3.34 Output Voltage vs. Fault strength
(Bridging fault for M_1 (00), M_3 (01)(11) and M_4 (10))

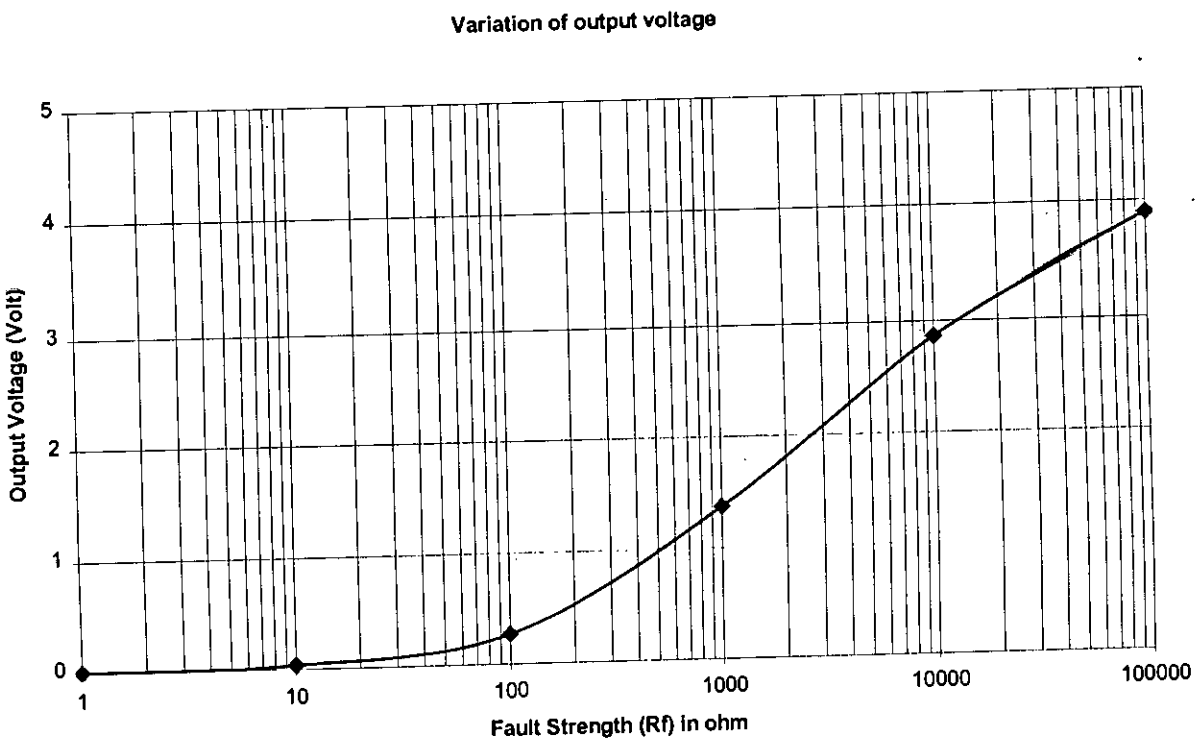


Fig 3.35 Output Voltage vs. Fault strength
(Bridging fault for M_1 (01)(11), M_2 (10) and M_3 (00))

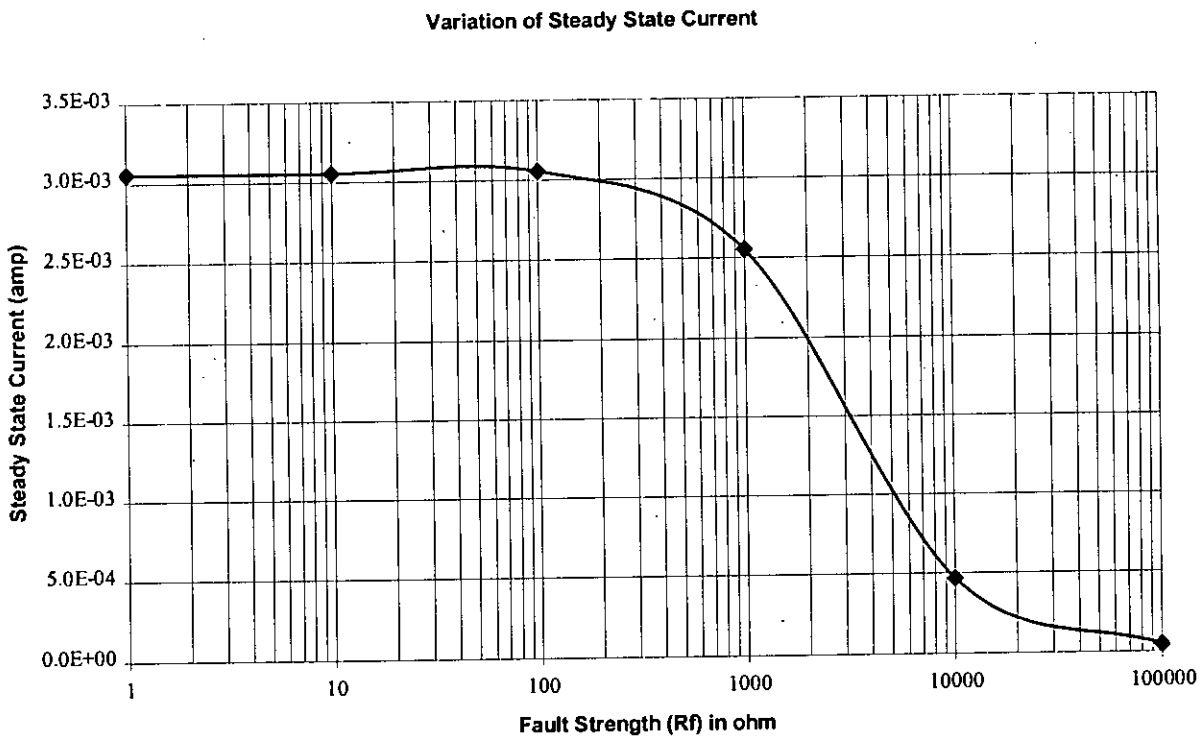


Fig 3.36 Steady State Current vs. Fault strength
(Bridging fault for M_1 (00), M_3 (01)(11) and M_4 (10))

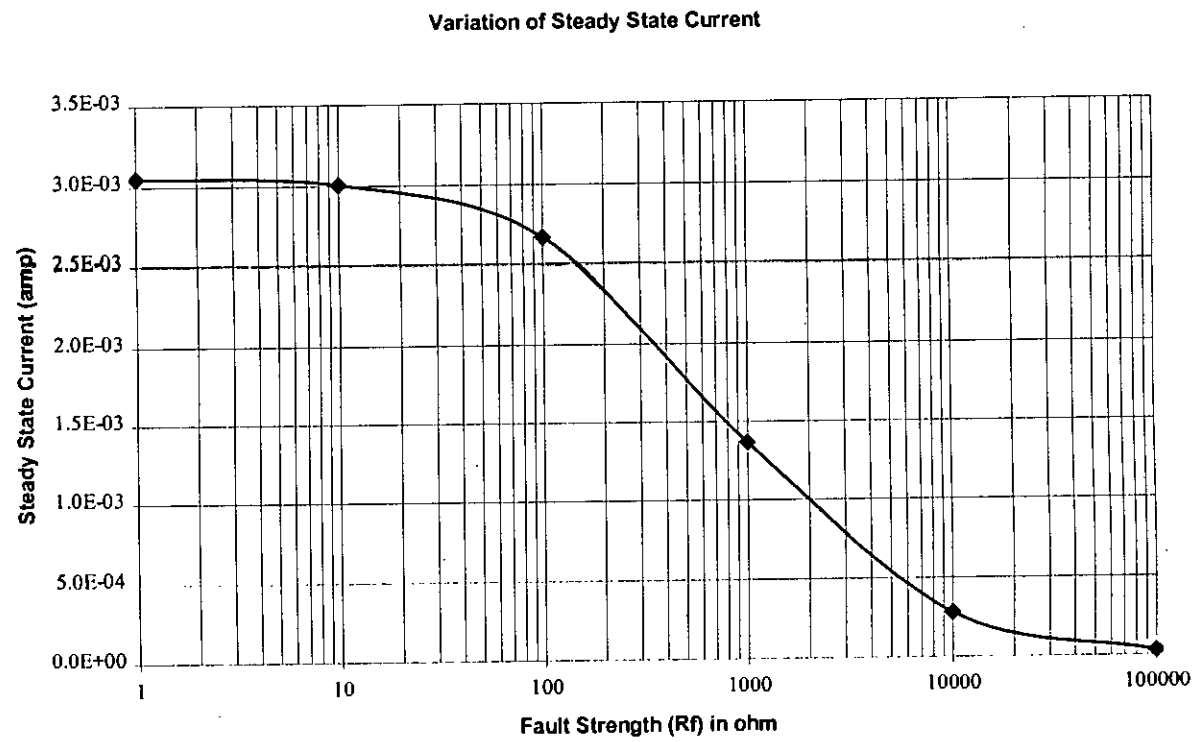


Fig 3.37 Steady State Current vs. Fault strength
(Bridging fault for M_1 (01)(11), M_2 (10) and M_3 (00))

Effects of Fault Resistance:

As seen from table 3.9, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 1 Ω to 100 kΩ, the output voltage varies from 0.03 to 4.997 Volt. This appreciable variation in output voltage clearly shows that the output logic level is indeterminable. This agrees with our prediction that the fault cannot be detected by logic monitoring. As seen from the table signal current is in the range of mili ampere compared to normal operating current of 0A. Therefore, the fault can be detected by current monitoring.

Table 3.10

The following table shows the summary for bridging faults in CPL OR/NOR circuit.

Summary for Bridging faults in CPL OR/NOR Circuit:

Fault	Test Vector	V_{out} (Volt)	I_{DDQ} (amp)	Logic Monitoring possible?	Current Monitoring possible?
M_1	***(00)***	***4.997 to 0.031***	***3.053E-03 to 4.462E-05***	***NO***	***YES***
	(01)	***0.031 to 3.892***	***3.048E-03 to 3.140E-05***	***NO***	***YES***
	(10)	4.113	5E-15	NO	NO
	(11)	***0.031 to 3.892***	***3.048E-03 to 3.140E-05***	***NO***	***YES***
M_2	(00)	0	0	NO	NO
	(01)	4.113	5E-15	NO	NO
	(10)	***0.031 to 3.892***	***3.048E-03 to 3.140E-05***	***NO***	***YES***
	(11)	5	0	NO	NO
M_3	***(00)***	***0.031 to 3.892***	***3.048E-03 to 3.140E-05***	***NO***	***YES***
	(01)	***4.997 to 0.031***	***3.053E-03 to 4.462E-05***	***NO***	***YES***
	(10)	4.9	5E-15	NO	NO
	(11)	***4.997 to 0.031***	***3.053E-03 to 4.462E-05***	***NO***	***YES***
M_4	(00)	5	0	NO	NO
	(01)	0	0	NO	NO
	(10)	***4.997 to 0.031***	***3.053E-03 to 4.462E-05***	***NO***	***YES***
	(11)	0	0	NO	NO

3.4.5 Qualitative Analysis for CPL EXOR/EXNOR Circuit:

M_1 : (bridging fault in M_1 of the CPL EXNOR/EXOR gate of figure 2.3)

The fault is modeled in figure 3.38 and 3.39 where the faulted MOS is replaced by a variable resistance R_f. The test vectors (1,0) and (1,1) produce correct logic and no significant current flows in the circuit when this test vectors are applied. Hence this vector is incapable of detecting the fault. However, when the vector (0,0) and (0,1) are applied, a large current flows through the circuit.

Test Vector 00:

The output voltage is

$$V_{out} = \{R_{on}/(R_f+R_{on})\}V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the bridging fault at M_1 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f+R_{on})$$

Hence, the fault can be detected by current monitoring i.e. I_{DDQ} Testing.

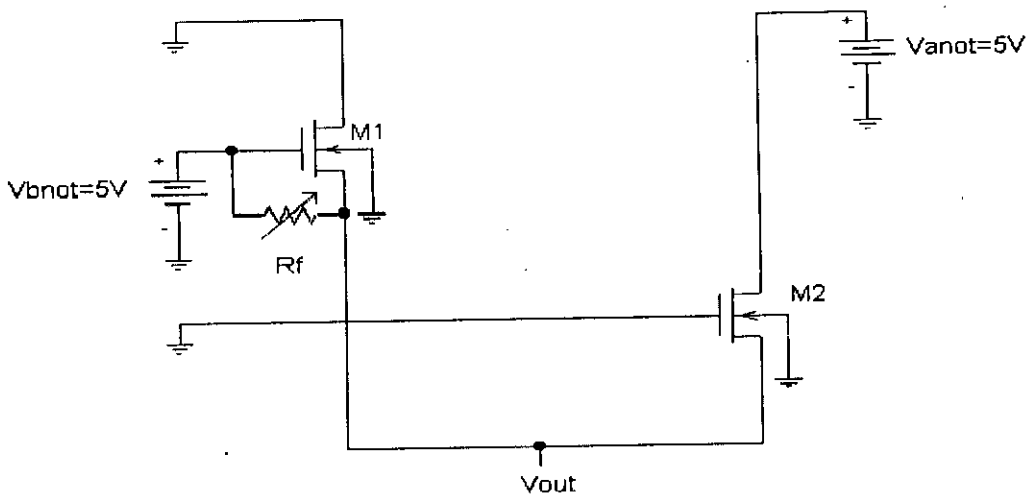


Fig. 3.38 Simulation circuit for bridging fault on MOS M_1 of CPL EXOR/EXNOR gate for test vector [A=0, B=0].

Test Vector 01:

The output voltage is

$$V_{out} = \{R_f/(R_f+R_{on})\} V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the bridging fault at M_1 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring i.e. I_{DDQ} Testing.

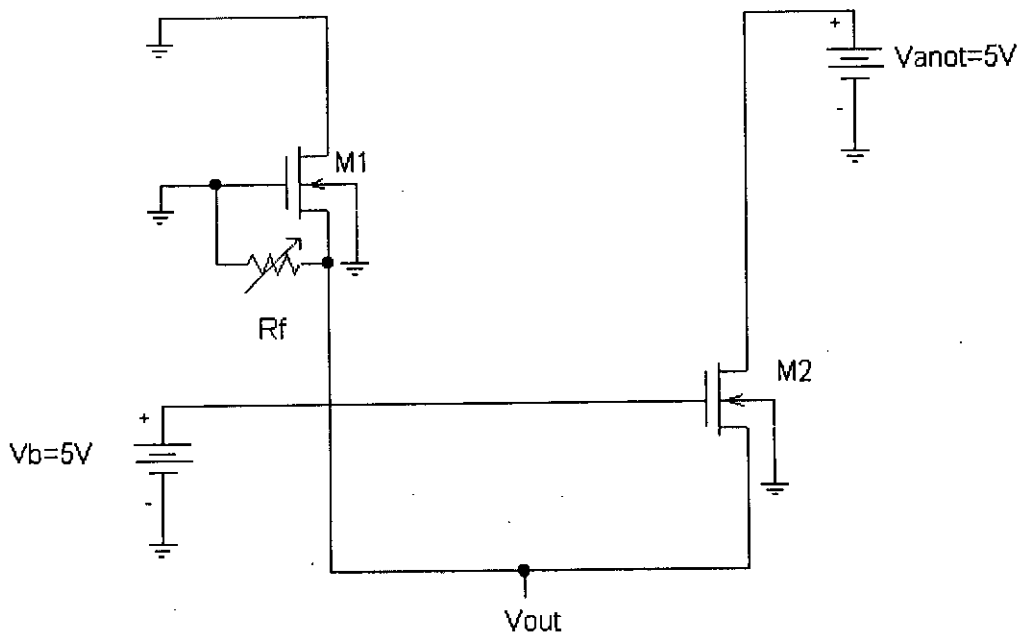


Fig. 3.39 Simulation circuit for bridging fault on MOS M_1 of CPL EXOR/EXNOR gate for test vector [A=0, B=1]

M_2 : (bridging fault in M_2 of the CPL EXOR/EXNOR gate of figure 2.3)

Similar qualitative analysis have been done for bridging fault on MOS M_2 of CPL EXOR/EXNOR gate. The test vectors (0,0) and (0,1) produce correct logic and no significant current flows in the circuit when this test vectors are applicd. Hence this vector is incapable of detecting the fault. However, when the vector (1,0) and (1,1) are applied, a large current flows through the circuit. The current and voltage expression

are similar to previous case. SPICE simulation results are summarized in the tables at the end of this article.

M_3 : (bridging fault in M_3 of the CPL EXNOR/EXOR gate of figure 2.3)

Qualitative analysis have been done for bridging fault on MOS M_3 of CPL EXOR/EXNOR gate. The test vectors (1,0) and (1,1) produce correct logic and no significant current flows in the circuit when this test vectors are applied. Hence this vector is incapable of detecting the fault. However, when the vector (0,0) and (0,1) are applied, a large current flows through the circuit. The current and voltage expression are similar to previous case. SPICE simulation results are summarized in the tables at the end of this article.

M_4: (bridging fault in M_4 of the CPL EXNOR/EXOR gate of figure 2.3)

The fault is modeled in figure 3.40 and 3.41 where the faulted MOS is replaced by a variable resistance R_f. The test vectors (0,0) and (0,1) produce correct logic and no significant current flows in the circuit when this test vectors are applied. Hence this vector is incapable of detecting the fault. However, when the vector (1,0) and (1,1) are applied, a large current flows through the circuit.

Test Vector 10:

The output voltage is

$$V_{out} = \{R_{on}/(R_f+R_{on})\}V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the bridging fault at M_4 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f+R_{on})$$

Hence, the fault can be detected by current monitoring i.e. I_{DDQ} Testing.

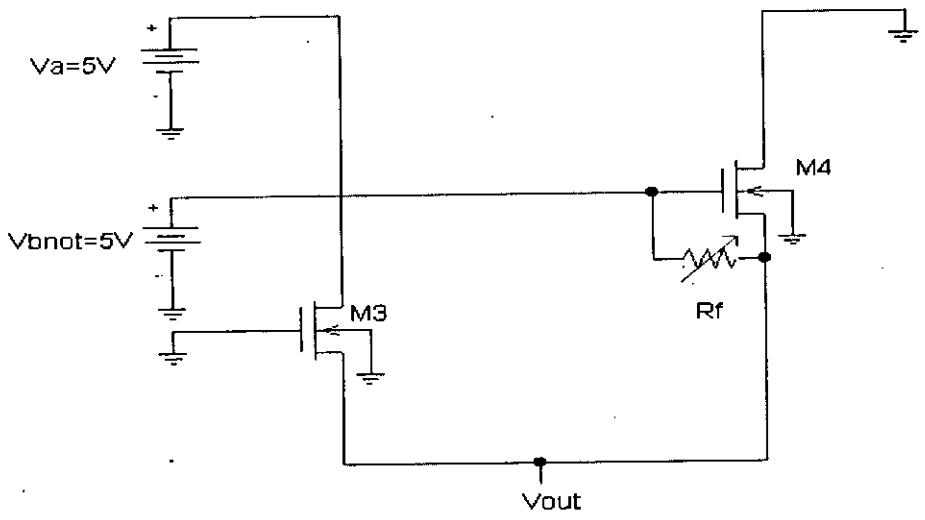


Fig. 3.40 Equivalent Circuit for gate to source bridging fault on MOS M_4 of CPL EXOR/EXNOR gate for test vector [A=1, B=0].

Test Vector 11:

The output voltage is

$$V_{out} = \{R_f/(R_f+R_{on})\} V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the bridging fault at M_4 cannot be detected by logic monitoring. However, Steady state current is significantly large due to the low resistance path between V_{IH} and ground. Steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be dctected by current monitoring (I_{DDQ} Testing).

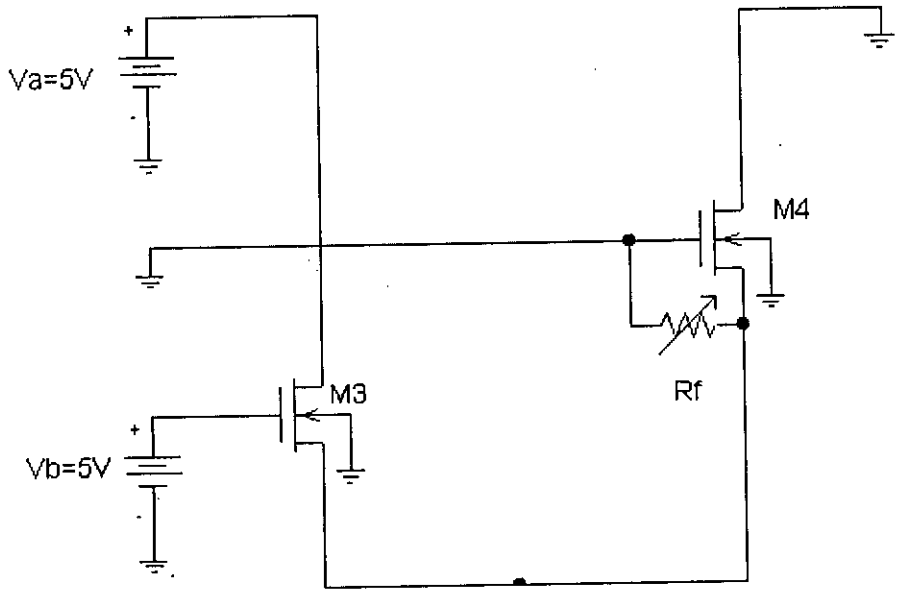


Fig. 3.41 Equivalent Circuit for gate to source bridging fault on MOS M_4 of CPL EXOR/EXNOR gate for test vector [A=1, B=1].

3.4.6 SPICE Simulation Bridging Fault Results for CPL EXNOR/EXOR Circuit

This section summarizes the SPICE simulation results for a single bridging fault in the MOS devices of the CPL EXNOR/EXOR logic gates.

Table 3.11

SPICE Simulation results for bridging faults in CPL EXNOR/EXOR Ckt.

Effect of fault strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
		V_a	V_b		
M_1	1	0	0	4.997	3.053E-03
	10	0	0	4.996	3.053E-03
	100	0	0	4.692	3.053E-03
	1K	0	0	2.446	2.551E-03
	10K	0	0	0.327	4.672E-04
	100K	0	0	0.030	4.526E-05
	1	0	5	0.003	3.048E-03
	10	0	5	0.033	3.004E-03
	100	0	5	0.269	2.666E-03
	1K	0	5	1.365	1.363E-03
	10K	0	5	2.865	2.855E-04
	100K	0	5	3.892	2.769E-05
M_2	1	5	0	0.003	3.048E-03
	10	5	0	0.033	3.004E-03
	100	5	0	0.269	2.666E-03
	1K	5	0	1.365	1.363E-03
	10K	5	0	2.865	2.855E-04
	100K	5	0	3.892	2.769E-05
	1	5	5	4.997	3.053E-03
	10	5	5	4.996	3.053E-03
	100	5	5	4.692	3.053E-03
	1K	5	5	2.446	2.551E-03
	10K	5	5	0.327	4.672E-04
	100K	5	5	0.030	4.526E-05

Table 3.11

SPICE Simulation results for bridging faults in CPL EXNOR/EXOR Ckt.

Effect of fault strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
		V_a	V_b		
M_3	1	0	0	0.003	3.048E-03
	10	0	0	0.033	3.004E-03
	100	0	0	0.269	2.666E-03
	1K	0	0	1.365	1.363E-03
	10K	0	0	2.865	2.855E-04
	100K	0	0	3.892	2.769E-05
	1	0	5	4.997	3.053E-03
	10	0	5	4.996	3.053E-03
	100	0	5	4.692	3.053E-03
	1K	0	5	2.446	2.551E-03
	10K	0	5	0.327	4.672E-04
	100K	0	5	0.030	4.526E-05
M_4	1	5	0	4.997	3.053E-03
	10	5	0	4.996	3.053E-03
	100	5	0	4.692	3.053E-03
	1K	5	0	2.446	2.551E-03
	10K	5	0	0.327	4.672E-04
	100K	5	0	0.030	4.526E-05
	1	5	5	0.003	3.048E-03
	10	5	5	0.033	3.004E-03
	100	5	5	0.269	2.666E-03
	1K	5	5	1.365	1.363E-03
	10K	5	5	2.865	2.855E-04
	100K	5	5	3.892	2.769E-05

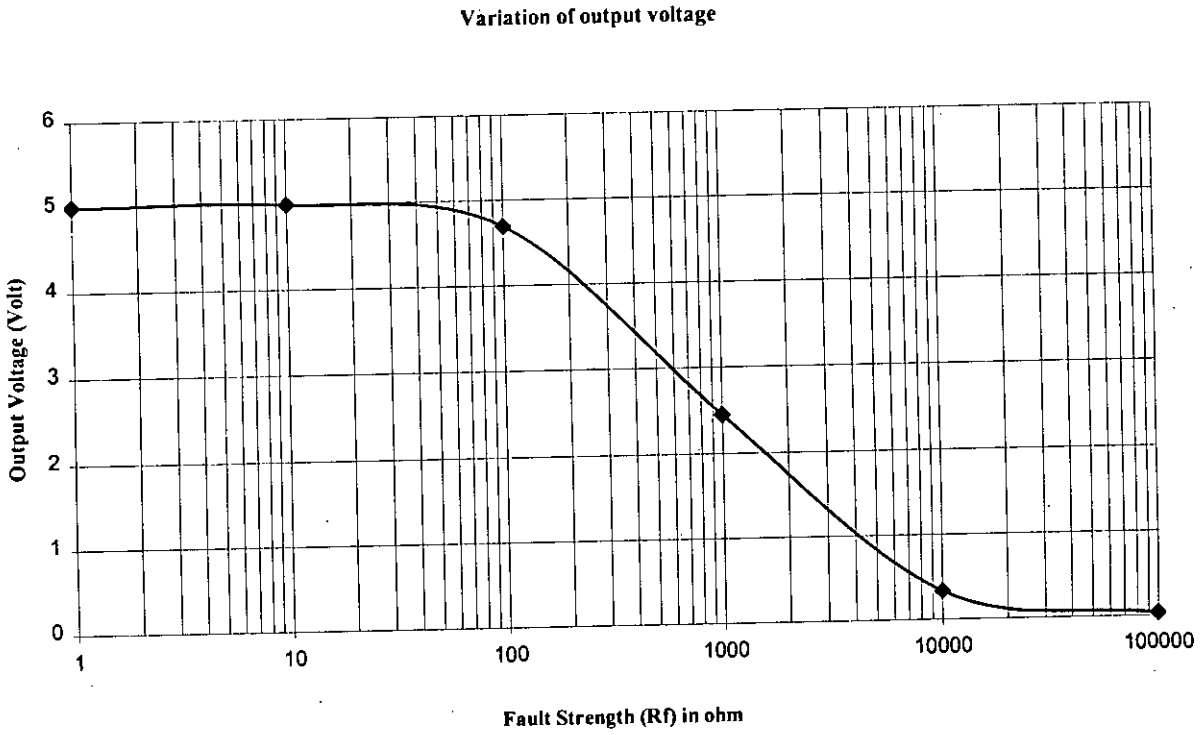


Fig 3.42 Output Voltage vs. Fault strength
(Bridging fault for M_1 (00), M_2 (11),M_3 (01) and M_4 (10))

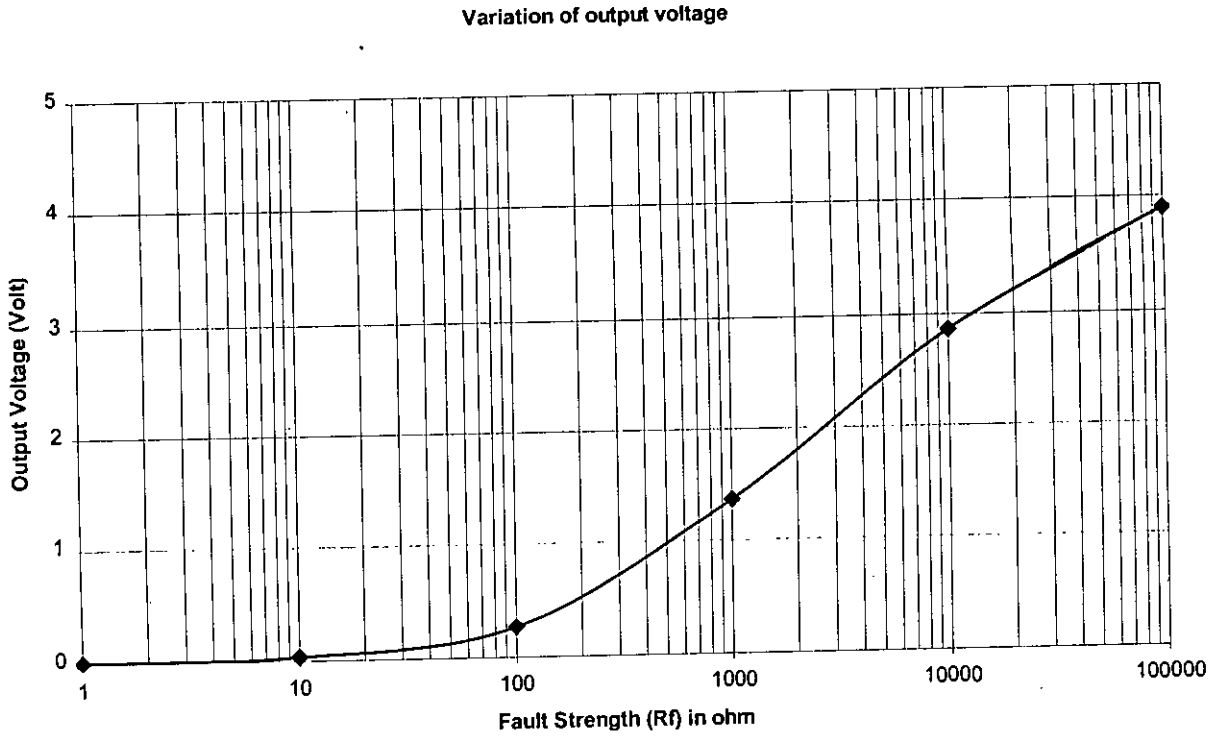


Fig 3.43 Output Voltage vs. Fault strength
(Bridging fault for M_1 (01), M_2 (10), M_3 (00) and M_4 (11))

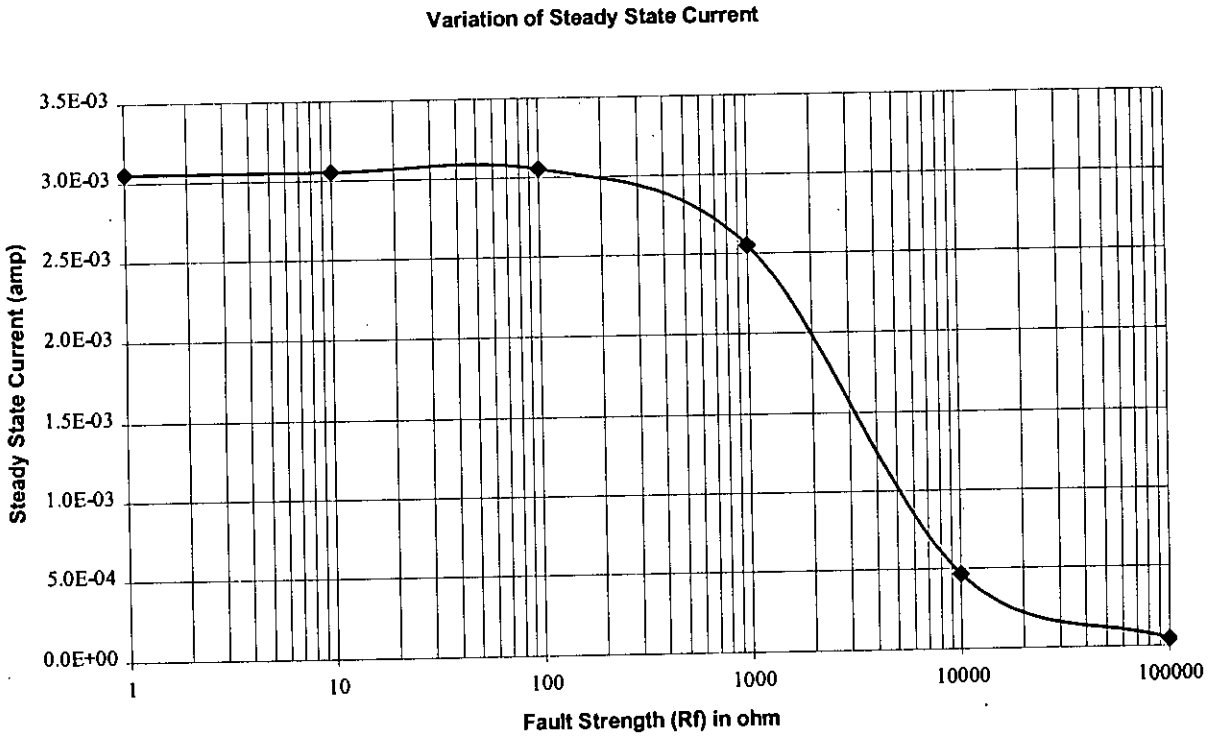


Fig 3.44 Steady State Current vs. Fault strength
(Bridging fault for M_1 (00), M_2 (11),M_3 (01) and M_4 (10))

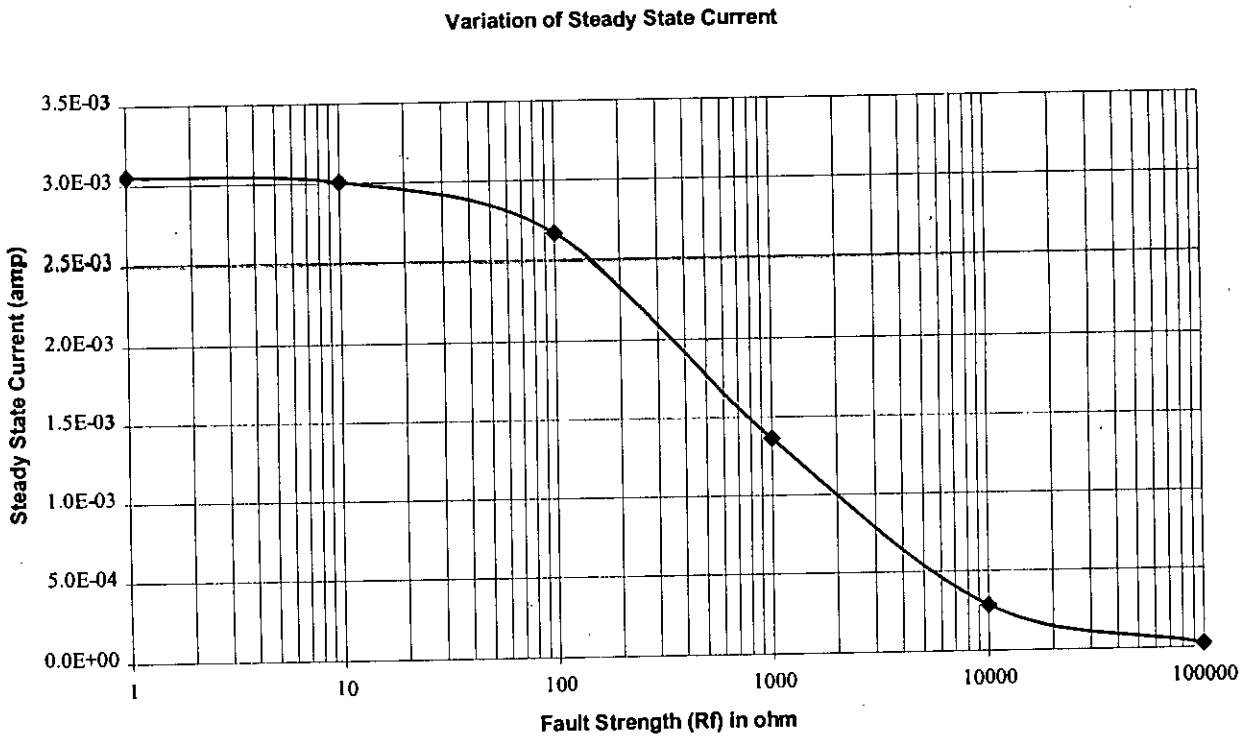


Fig 3.45 Steady State Current vs. Fault strength
(Bridging fault for M_1 (01), M_2 (10), M_3 (00) and M_4 (11))

Effects of Fault Resistance:

As seen from table 3.11, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 1 Ω to 100 kΩ, the output voltage varies from 4.997 to 0.003 Volt. This appreciable variation in output voltage clearly shows that the output logic level is indeterminable. This agrees with our prediction that the fault cannot be detected by logic monitoring. As seen from the table signal current is in the range of miliampere compared to normal operating current of 5 pA. Therefore, the fault can be detected by current monitoring.

Table 3.12

The following table shows the summary for bridging faults in CPL EXOR/EXNOR circuit.

Summary for Bridging faults in CPL EXOR/EXNOR Circuit:

Fault	Test Vector	V_{out} (Volt)	I_{DDQ} (amp)	Logic Monitoring possible?	Current Monitoring possible?
M_1	*(00)*	*0.0 to 4.997*	*3.053E-03 to 4.526E-05*	*NO*	*YES*
	(01)	*0.003 to 3.892*	*3.048E-03 to 2.769E-05*	*NO*	*YES*
	(10)	5	0	NO	NO
	(11)	0	0	NO	NO
M_2	(00)	0	0	NO	NO
	(01)	5	0	NO	NO
	(10)	*0.003 to 3.892*	*3.048E-03 to 2.769E-05*	*NO*	*YES*
	(11)	*0.03 to 4.997*	*3.053E-03 to 4.526E-05*	*NO*	*YES*
M_3	*(00)*	*0.003 to 3.892*	*3.048E-03 to 2.769E-05*	*NO*	*YES*
	(01)	*0.03 to 4.997*	*3.053E-03 to 4.526E-05*	*NO*	*YES*
	(10)	0	0	NO	NO
	(11)	5	0	NO	NO
M_4	(00)	5	0	NO	NO
	(01)	0	0	NO	NO
	(10)	*0.003 to 3.892*	*3.048E-03 to 2.769E-05*	*NO*	*YES*
	(11)	*0.03 to 4.997*	*3.053E-03 to 4.526E-05*	*NO*	*YES*

3.5 Behavior Under Single Stuck open Faults

The behavior of CPL circuits under single stuck open fault in MOS are analyzed in this section. Both the CPL NAND/AND, NOR/OR and EXNOR/EXOR gates are considered. The two input NAND gate shown in figure 2.1, the two input NOR/OR gate shown in figure 2.2 and the two input EXNOR/EXOR gate shown in figure 2.3 for the CPL case are used for analysis.

Physical defects may cause a MOS to become permanently open and insensitive to its input signal. The MOS is then said stuck open. To model a stuck open fault, a large resistance is inserted between the MOS terminal and the circuit node to which the terminal would otherwise be connected. Detection of the stuck-open fault can be achieved by utilizing the two pattern test. In this test, two vectors are applied to the faulted circuit sequentially. The two vectors must be chosen so that under fault free conditions, the outputs corresponding to these vectors are complements of each other. Moreover one of the vectors must be chosen so that application of this vector to the CPL gate under faulted conditions cause both MOS in the CPL gate to be OFF at the same time. As a result, the O/P node becomes isolated from the drain inputs of the MOS. The CPL gate is then said to be in 'non conducting state'. The Input vector responsible for the non conducting state of the CPL gate is called a 'Test Vector'. The other vector, called the 'Initialization Vector', is chosen so that application of this vector produces correct output logic even under faulted conditions. Once the above two vectors are chosen, the two pattern test is applied as follows:

1) A capacitor is connected to the output node.
2) The output node is initialized by applying the Initialization Vector.
3) The Test Vector is applied next, thus causing the capacitor at the output node of the faulted circuit to be isolated from the rest of the circuit. Consequently, the capacitor cannot change state and is forced to retain its original state.

The fault free circuit would have produced complemented outputs due to the application of these two vectors sequentially. The faulted circuit, however, produces an almost unchanged output & this leads to detection of the fault. Two pattern test should be applied at a rate more rapid than that associated with leakage current time constant of the circuit. In all cases below, test vector is applied to the faulty circuit 10

ns after the application of the initialization vector and the output is monitored after a time delay of 100ns.

3.5.1 Qualitative Analysis for CPL AND/NAND Circuit:

M_1 : (stuck open fault in M_1 of the CPL AND/NAND gate of figure 2.1)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_1, a high resistance is inserted at the lower end of M_1 to isolate it from the rest of circuit. It is observed that when the vector (11) is applied - M_2 turns off and M_1 remains off since it is stuck-open. Since both MOS are off when (11) is applied thus producing a non-conducting stage in the gate. Hence, the (11) vector can be taken as a Test Vector for M_1 stuck-on fault. In the fault free circuit, the (11) vector would produce a high output. Consequently, the vectors that produced a low output under faulted and fault free conditions are the Initialization Vectors for the two pattern test. Vectors (00), (10) produce low outputs under both the above conditions and therefore can be considered as Initialization Vectors. Applying any one of the Initialization Vectors first and then the Test Vector can detect the fault. Each of these cases is analyzed below.

i. **Initialization Vector (00), Test Vector (11):**

When a capacitor is connected to the output terminal of the faulted gate of fig 3.46 and the vector (00) is applied, the output voltage is at 0 Volt. The Test Vector (11) is applied next, thus causing the output capacitance to be isolated from the circuit. Ideally the output capacitance retains its original state of 0 V. But practically, a current flows from the 5V power source Va through M_1 and the resistance R_f to charge the output capacitance to 5V. Also M_2 supplies a leakage current that charges Cout. These charging currents are very small since the large resistance R_f limits one and the other is only a leakage current. As a result, the time to charge the capacitance to 5V is longer than the time that would be required in a fault free gate. This delay in charging the output capacitance to 5 V is the fundamental criterion for faulted detection.

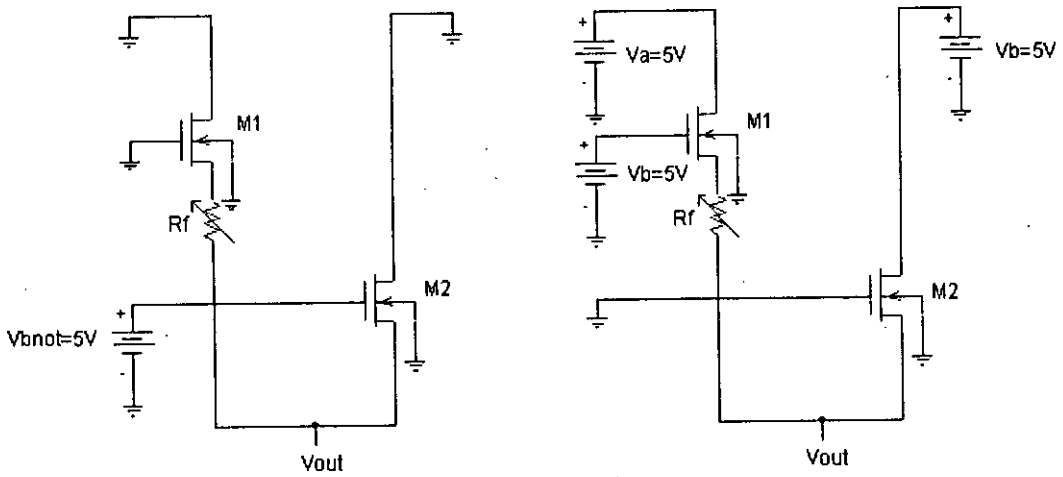


Fig. 3.46 Equivalent circuit for qualitative analysis of stuck-open fault on MOS M_1 of CPL AND/NAND circuit. (i) Initialization vector [A=0, B=0] (ii) Test Vector [A=1, B=1].

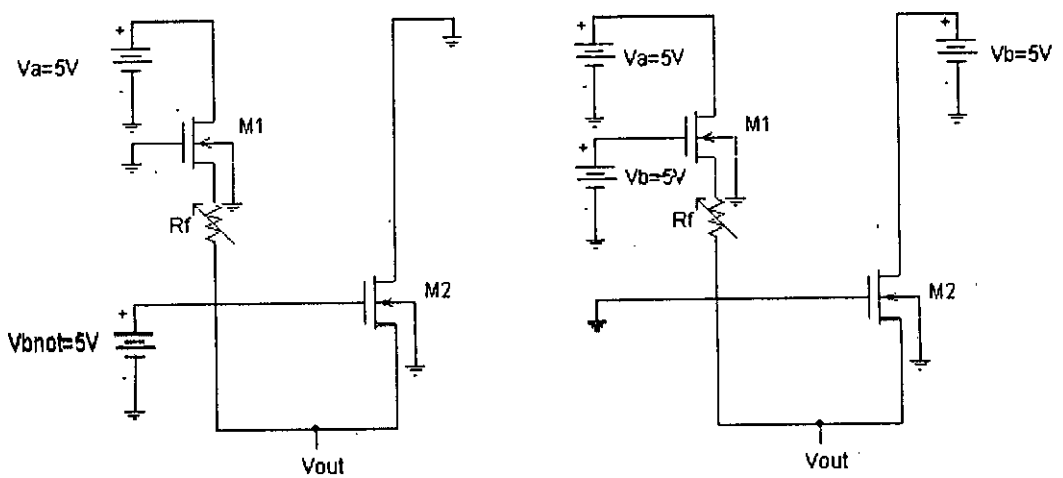


Fig. 3.47 Equivalent circuit for qualitative analysis of stuck-open fault on MOS M_1 of CPL AND/NAND circuit. (i) Initialization vector [A=1, B=0] (ii) Test Vector [A=1, B=1].

ii. Initialization Vector (10), Test Vector (11):

When a capacitor is connected to the output terminal of the faulted gate of fig 3.47 and the vector (10) is applied, the output voltage is at 0 Volt. The Test Vector (11) is applied next, thus causing the output capacitance to be isolated

from the circuit. Ideally the output capacitance retains its original state of 0 V. But practically, a current flows from the 5V power source Va through M_1 and the resistance R_f to charge the output capacitance to 5V. Also M_2 supplies a leakage current that charges Cout. These charging currents are very small since the large resistance R_f limits one and the other is only a leakage current. As a result, the time to charge the capacitance to 5V is longer than the time that would be required in a fault free gate. This delay in charging the output capacitance to 5 V is the fundamental criterion for faulted detection.

M_2 : (stuck open fault in M_2 of the CPL AND/NAND gate of figure 2.1)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_2, a high resistance is inserted at the lower end of M_2 to isolate it from the rest of circuit. It is observed that when the vector (00) and (10) are applied - M_1 turns off and M_2 remains off since it is stuck-open. Since both MOS are off when (00) and (10) are applied thus producing a non-conducting stage in the gate. Hence, the (00) and (10) vectors can be taken as a Test Vector for M_2 fault. In the fault free circuit, the (00) and (11) vectors will produce a low output. Consequently, the vectors that produced a high output under faulted and fault free conditions are the Initialization Vectors for the two pattern test. Vectors (11) produce high output under both the above conditions and therefore can be considered as Initialization Vector. Applying the Initialization Vector first and then any one of the Test Vectors can detect the fault. The qualitative analysis is similar to the previous case. SPICE simulation results are summarized in the tables.

M_3 : (stuck open fault in M_3 of the CPL AND/NAND gate of figure 2.1)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_3, a high resistance is inserted at the lower end of M_3 to isolate it from the rest of circuit. It is observed that when the vector (00) and (10) are applied - M_4 turns off and M_3 remains off since it is stuck-open. Since both MOS are off when (00) and (10) are applied thus producing a non-conducting stage in the gate. Hence, the (00) and (10) vectors can be taken as a Test Vector for M_3 fault. In the fault free circuit, the (00) and (10) vectors will produce a high output. Consequently, the vectors that produced a low output under faulted and fault free conditions are the Initialization Vectors for the two pattern test. Vectors (11) produce low output under both the above conditions and therefore can be considered as Initialization Vector. Applying the Initialization Vector first and then any one of the Test Vectors can detect the fault. Each of these cases is

analyzed below. The qualitative analysis is similar to the previous case. SPICE simulation results are summarized in the tables.

M_4 : (stuck open fault in M_4 of the CPL AND/NAND gate of figure 2.1)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_4, a high resistance is inserted at the lower end of M_4 to isolate it from the rest of circuit. It is observed that when the vector (11) is applied - M_3 turns off and M_4 remains off since it is stuck-open. Since both MOS are off when (11) is applied thus producing a non-conducting stage in the gate. Hence, the (11) vector can be taken as a Test Vector for M_4 fault. In the fault free circuit, the (11) vector will produce a low output. Consequently, the vectors that produced a high output under faulted and fault free conditions are the Initialization Vectors for the two pattern test. Vectors (00) and (10) produce high output under both the above conditions and therefore can be considered as Initialization Vector. Applying any one of the Initialization Vectors first and then the Test Vector can detect the fault. The qualitative analysis is similar to the previous case. SPICE simulation results are summarized in the tables.

3.5.2 SPICE Simulation Results for Stuck open fault in CPL AND/NAND Circuit

This section summarizes the SPICE simulation results for a single stuck open fault in the MOS devices of the CPL AND/NAND ckt.

Table 3.13

SPICE Simulation result for stuck open fault in CPL AND/NAND.

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_1	10 M	1	00	11	0	0
		10	00	11	0	0
		100	00	11	77.6E-03	3.991E-11
	100 M	1	00	11	0	0
		10	00	11	0	8.354E-15
		100	00	11	7.07E-04	1.89E-17
	10 M	1	10	11	0	5E-12
		10	10	11	0	5E-12
		100	10	11	8.04E-04	3.986E-11
	100 M	1	10	11	0	4.9E-12
		10	10	11	0	4.9E-12
		100	10	11	7.35E-04	1.89E-17
M_2	10 M	1	11	00	5	0
		10	11	00	4.97	2.645E-03
		100	11	00	4.96	1.328E-07
	100 M	1	11	00	5	0
		10	11	00	4.97	2.645E-03
		100	11	00	4.97	1.329E-07
	10 M	1	11	10	5	0
		10	11	10	4.97	2.645E-03
		100	11	10	4.96	1.328E-07
	100 M	1	11	10	5	0
		10	11	10	4.97	2.645E-03
		100	11	10	4.97	1.329E-07

Table 3.13

SPICE Simulation result for stuck-open fault in CPL AND/NAND.

Effect of fault strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_3	10 M	1	11	00	0	0
		10	11	00	0	0
		100	11	00	77.6E-03	3.991E-11
	100 M	1	11	00	0	0
		10	11	00	0	8.354E-15
		100	11	00	7.07E-04	1.89E-17
	10 M	1	11	10	0	0
		10	11	10	0	0
		100	11	10	77.6E-03	3.991E-11
	100 M	1	11	10	0	0
		10	11	10	0	8.354E-15
		100	11	10	7.07E-04	1.89E-17
M_4	10 M	1	10	11	4.11	0
		10	10	11	4.11	1.22E-12
		100	10	11	4.10	13.31E-06
	100 M	1	10	11	4.11	0
		10	10	11	4.11	1.22E-12
		100	10	11	4.10	13.28E-12
	10 M	1	00	11	5	0
		10	00	11	4.97	2.645E-03
		100	00	11	4.96	1.328E-07
	100 M	1	00	11	5	0
		10	00	11	4.97	2.645E-03
		100	00	11	4.97	1.329E-07

Effects of Fault Resistance and Time Interval:

As fault resistance varies from 10 MΩ to 100 MΩ, the output voltage and Steady state current has a little effect. The time interval has a great effect on the output voltage. Suppose the initialization vector causes the output capacitance to charge to high level. The application of the test vector causes the faulty node to be isolated from the circuit. Now if we wait too long to take measurement after the application of the test vector the output voltage will level will gradually decrease due to device leakage current. It is found that application of the test vector 10 ns after application of the initialization vector and taking the measurement after 100 ns is a good choice.

Table 3.14

The following table shows the summary for stuck open faults in CPL AND/NAND circuit.

Summary for Stuck open faults in CPL AND/NAND Circuit:

Fault	Successful Two Pattern Vectors	O/P Logic Level Un-faulted	O/P Logic Level Faulted	I_{DDQ} (amp)	Logic monitoring possible?	Current monitoring possible?
M_1	(00) (11)	01	00	1.890E-17	Yes	No
	(10),(11)	01	00	1.890E-17	Yes	No
M_2	(11),(00)	10	11	1.329E-07	Yes	No
	(11),(10)	10	11	1.329E-07	Yes	No
M_3	(11),(00)	01	00	3.991E-11	Yes	No
	(11),(10)	01	00	3.991E-11	Yes	No
M_4	(10),(11)	10	11	13.28E-12	Yes	No
	(00),(11)	10	11	1.328E-07	Yes	No

3.5.3 Qualitative Analysis for CPL OR/NOR Circuit:

M_1 : (stuck open fault in M_1 of the CPL OR/NOR gate of figure 2.2)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_1, a high resistance is inserted at the lower end of M_1 to isolate it from the rest of circuit. It is observed that when the vector (00) is applied - M_2 turns off and M_1 remains off since it is stuck-open. Since both MOS are off when (00) is applied thus producing a non-conducting stage in the gate. Hence, the (00) vector can be taken as a Test Vector for M_1 fault. In the fault free circuit, the (00) vector would produce a low output. Consequently, the vectors that produced a high output under faulted and fault free conditions are the Initialization Vectors for the two pattern test. Vectors (01) and (11) produce high outputs under both the above conditions and therefore can be considered as Initialization Vectors. Applying any one of the Initialization Vectors first and then the Test Vector can detect the fault. Each of these cases is analyzed below.

i. **Initialization Vector (01), Test Vector (00):**

When a capacitor is connected to the output terminal of the faulted gate of fig 3.48 and the vector (01) is applied, the output voltage is at 5 Volt. The Test Vector (00) is applied next, thus causing the output capacitance to be isolated from the circuit. Ideally the output capacitance retains its original state of 5 V. But practically, a discharge path exists for the output capacitance through the resistance R_f and M_1. The discharging time is very large due to the large resistance R_f. As a result, the time to discharge the capacitance to 0 V is longer than the time that would be required in a fault free circuit. This delay in discharging the output capacitance to 0 V is the fundamental criterion for faulted detection.

ii. **Initialization Vector (11), Test Vector (00):**

When a capacitor is connected to the output terminal of the faulted gate of fig 3.49 and the vector (11) is applied, the output voltage is at 5 Volt. The Test Vector (00) is applied next, thus causing the output capacitance to be isolated from the circuit. Ideally the output capacitance retains its original state of 5 V. But practically, a discharge path exists for the output capacitance through the resistance R_f and M_1. The discharging time is very large due to the large resistance R_f. As a result, the time to discharge the capacitance to 0 V is longer than the time that would be required in a fault free circuit. This delay in

discharging the output capacitance to 0 V is the fundamental criterion for faulted detection.

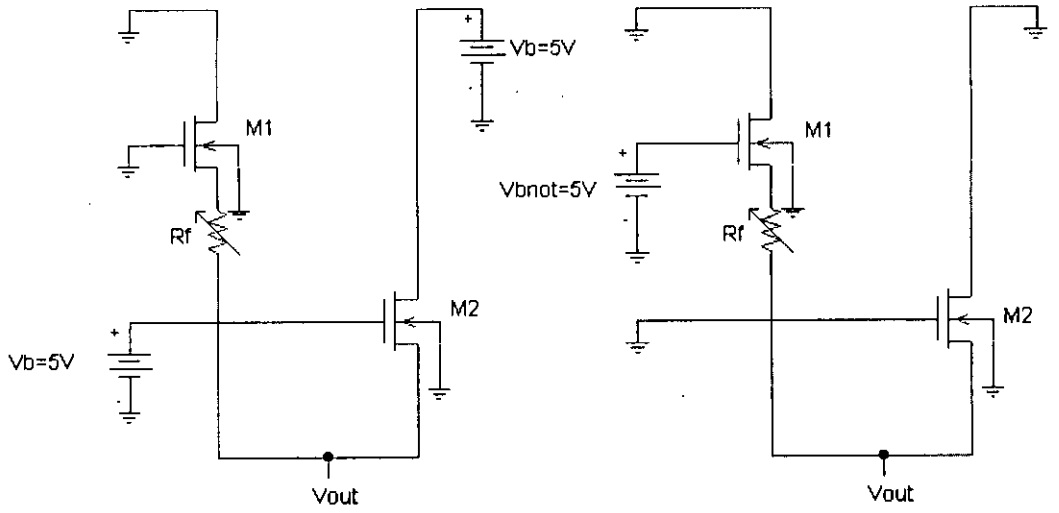


Fig 3.48 Equivalent circuit for stuck-open fault on MOS M_1 of CPL OR/NOR circuits. I.V. [A=0, B=1], T.V. [A=0, B=0]

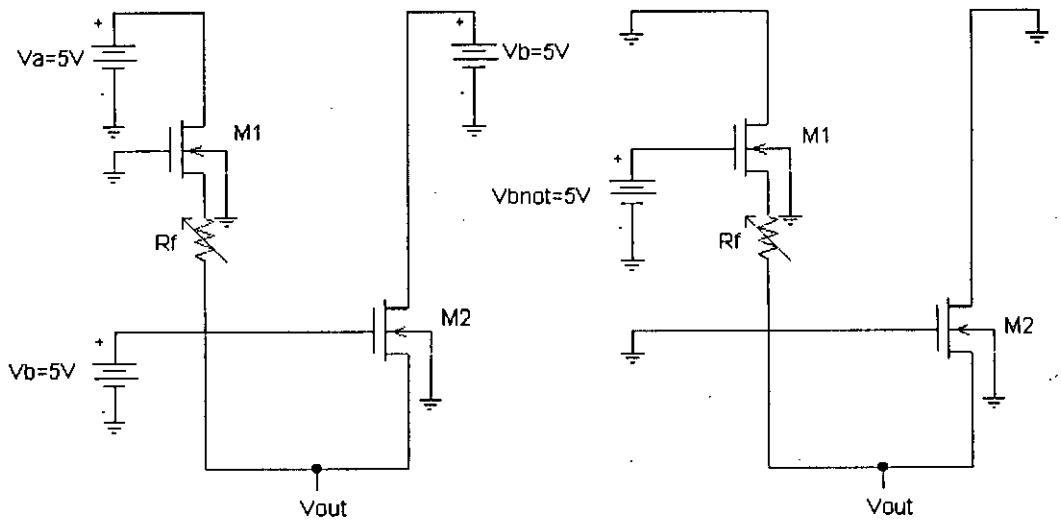


Fig. 3.49 Equivalent circuit for stuck-open fault on MOS M_1 of CPL OR/NOR circuits. I.V. [A=1, B=1], T.V. [A=0, B=0]

M_2 : (stuck open fault in M_2 of the CPL OR/NOR gate of figure 2.2)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_2, a high resistance is inserted at the lower end of M_2 to isolate it from the rest of circuit. It is observed that when the vector (01) and (11) are applied - M_1 turns off and M_2 remains off since it is stuck-open. Since both MOS are off when (01) and (11) are applied thus producing a non-conducting stage in the gate. Hence, the (01) and (11) vectors can be taken as a Test Vector for M_2 fault. The initialization vector is (00) for both of the case. The qualitative analysis is similar to the previous case. SPICE simulation result is summarized in the tables.

M_3 : (stuck open fault in M_3 of the CPL OR/NOR gate of figure 2.2)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_3, a high resistance is inserted at the lower end of M_3 to isolate it from the rest of circuit. It is observed that when the vector (01) and (11) are applied - M_4 turns off and M_3 remains off since it is stuck-open. Since both MOS are off when (01) and (11) are applied thus producing a non-conducting stage in the gate. Hence, the (01) and (11) vectors can be taken as a Test Vector for M_3 fault. The initialization vector is (00) for both of the case. The qualitative analysis is similar to the previous case. SPICE simulation result is summarized in the tables.

M_4 : (stuck open fault in M_4 of the CPL OR/NOR gate of figure 2.2)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_4, a high resistance is inserted at the lower end of M_4 to isolate it from the rest of circuit. It is observed that when the vector (00) and (11) are applied - M_3 turns off and M_4 remains off since it is stuck-open. Since both MOS are off when (00) and (11) are applied thus producing a non-conducting stage in the gate. Hence, the (00) and (11) vectors can be taken as a Test Vector for M_4 fault. For test vector (00) initialization vector is (01) and for test vector (11), initialization vector is (00). The qualitative analysis is similar to the previous case. SPICE simulation result is summarized in the tables.

3.5.4 SPICE Simulation Results for Stuck open Fault in CPL OR/NOR Circuit

This section summarizes the SPICE simulation results for a single stuck open fault in the MOS devices of the CPL NOR/OR ckt.

Table 3.15

SPICE Simulation result for stuck open fault in CPL OR/NOR.

Effect of fault strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_1	10 M	1	01	00	4.113	0
		10	01	00	4.113	1.22E-12
		100	01	00	2.5	13.31E-06
	100 M	1	01	00	4.113	0
		10	01	00	4.113	1.22E-12
		100	01	00	3.055	13.28E-12
	10 M	1	11	00	4.113	0
		10	11	00	4.113	1.22E-12
		100	11	00	2.5	13.31E-06
	100 M	1	11	00	4.113	0
		10	11	00	4.113	1.22E-12
		100	11	00	3.055	13.28E-12
M_2	10 M	1	00	01	0	0
		10	00	01	0.4	0
		100	00	01	3.02	3.991E-11
	100 M	1	00	01	0	0
		10	00	01	0.5	8.354E-15
		100	00	01	2.492	1.89E-17
	10 M	1	00	11	0	0
		10	00	11	0.4	0
		100	00	11	3.02	3.991E-11
	100 M	1	00	11	0	0
		10	00	11	0.5	8.354E-15
		100	00	11	2.492	1.89E-17

Table 3.15

SPICE Simulation result for stuck open fault in CPL OR/NOR.

Effect of fault strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_3	10 M	1	00	01	4.113	0
		10	00	01	4.113	1.22E-12
		100	00	01	2.5	13.31E-06
	100 M	1	00	01	4.113	0
		10	00	01	4.113	1.22E-12
		100	00	01	3.055	13.28E-12
	10 M	1	00	11	4.113	0
		10	00	11	4.113	1.22E-12
		100	00	11	2.5	13.31E-06
	100 M	1	00	11	4.113	0
		10	00	11	4.113	1.22E-12
		100	00	11	3.055	13.28E-12
M_4	10 M	1	01	00	0	0
		10	01	00	0.4	0
		100	01	00	3.02	3.991E-11
	100 M	1	01	00	0	0
		10	01	00	0.5	8.354E-15
		100	01	00	2.492	1.89E-17
	10 M	1	00	11	0	0
		10	00	11	0.4	0
		100	00	11	3.02	3.991E-11
	100 M	1	00	11	0	0
		10	00	11	0.5	8.354E-15
		100	00	11	2.492	1.89E-17

Effects of Fault Resistance and Time Interval:

As seen from table 3.15, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 10 MΩ to 100 MΩ, the output voltage and Steady state current has a little effect. The time interval has a great effect on the output voltage. Since Steady state current do not increase very high the current monitoring is not possible to determine the stuck open fault. But if we take lower time interval the output voltage variation gives us the fault detection.

Table 3.16

The following table shows the summary for stuck open faults in CPL OR/NOR circuit.

Summary for Stuck open faults in CPL OR/NOR Circuit:

Fault	Successful Two Pattern Vectors	O/P Logic Level Un-faulted	O/P Logic Level Faulted	I_{DDQ} (amp)	Logic monitoring possible?	Current monitoring possible?
M_1	(01,00)	01	00	1.22E-12	Yes	No
	(11,00)	01	00	1.22E-12	Yes	No
M_2	(00,01)	00	01	1.89E-17	Yes	No
	(00,11)	00	01	1.89E-17	Yes	No
M_3	(00,01)	01	00	1.22E-12	Yes	No
	(00,11)	01	00	1.22E-12	Yes	No
M_4	(01,00)	00	01	1.89E-17	Yes	No
	(00,11)	00	01	1.89E-17	Yes	No

3.5.5 Qualitative Analysis for CPL EXOR/EXNOR Circuit:

M_1 : (stuck open fault in M_1 of the CPL EXOR/EXNOR gate of figure 2.3)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_1, a high resistance is inserted at the lower end of M_1 to isolate it from the rest of circuit. It is observed that when the vectors (00) and (10) are applied - M_2 turns off and M_1 remains off since it is stuck-open. Since both MOS are off when (00) and (10) are applied thus producing a non-conducting stage in the gate. Hence, the (00) and (10) vectors can be taken as a Test Vector for M_1 fault.

Test Vector 00:

In the fault free circuit, the (00) vector would produce a low output. Consequently, the vectors that produced a high output under faulted and fault free conditions are the Initialization Vectors for the two pattern test. Vectors (01) and (10) produce high outputs under both the above conditions and therefore can be considered as Initialization Vectors. Applying any one of the Initialization Vectors first and then the Test Vector can detect the fault. Each of these cases is analyzed below.

i. **Initialization Vector (01), Test Vector (00):**

When a capacitor is connected to the output terminal of the faulted gate of fig 3.50 and the vector (01) is applied, the output voltage is at 5 Volt. The Test Vector (00) is applied next, thus causing the output capacitance to be isolated from the circuit. Ideally the output capacitance retains its original state of 5 V. But practically, a discharge path exists for the output capacitance through the resistance R_f and M_1. The discharging time is very large due to the large resistance R_f. As a result, the time to discharge the capacitance to 0 V is longer than the time that would be required in a fault free circuit. This delay in discharging the output capacitance to 0 V is the fundamental criterion for faulted detection.

ii. **Initialization Vector (10), Test Vector (00):**

The operation of this two pattern testis similar to i.

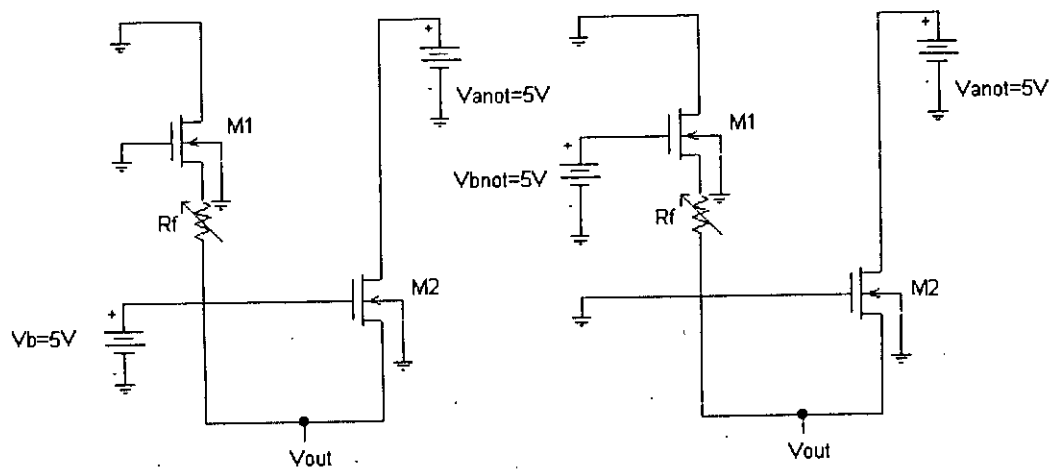


Fig.3.50 Equivalent circuit for suck on fault on MOS M_1 of CPL EXOR/EXNOR circuit. I.V. [A=0, B=1] T.V. [A=0, B=0]

Test Vector 10:

In the fault free circuit, the (10) vector would produce a high output. Consequently, the vectors that produced a low output under faulted and fault free conditions are the Initialization Vectors for the two pattern test. Vectors (00) and (11) produce low outputs under both the above conditions and therefore can be considered as Initialization Vectors. Applying any one of the Initialization Vectors first and then the Test Vector can detect the fault. Each of these cases is analyzed below.

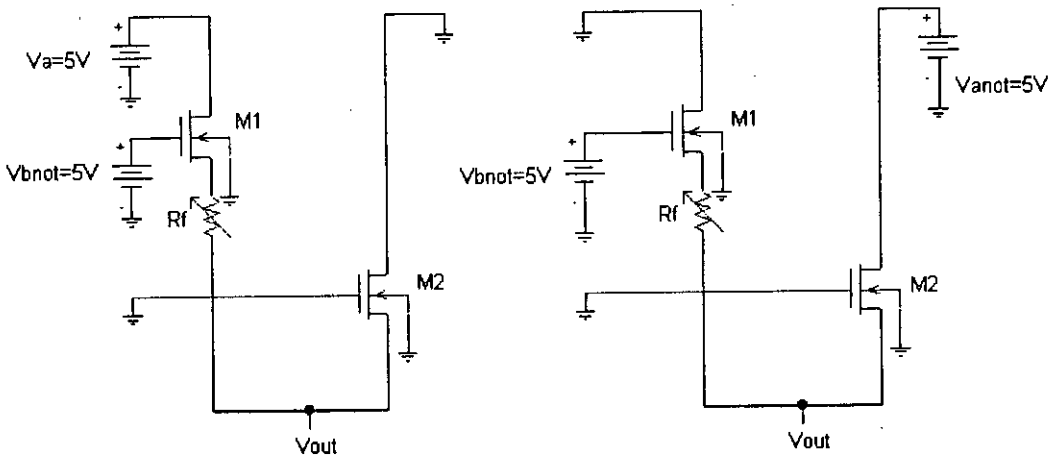


Fig. 3.51 Equivalent circuit for suck on fault on MOS M_1 of CPL EXOR/EXNOR circuit. I.V. [A=1, B=0] T.V. [A=0, B=0]

i. **Initialization Vector (00), Test Vector (10):**

When a capacitor is connected to the output terminal of the faulted gate of fig 3.51 and the vector (00) is applied, the output voltage is at 0 Volt. The Test Vector (10) is applied next, thus causing the output capacitance to be isolated from the circuit. Ideally the output capacitance retains its original state of 0 V. But practically, a charging path exists for the output capacitance through the resistance R_f and M_1. The discharging time is very large due to the large resistance R_f. As a result, the time to discharge the capacitance to 5 V is longer than the time that would be required in a fault free circuit. This delay in charging the output capacitance to 5 V is the fundamental criterion for faulted detection.

ii. **Initialization Vector (11), Test Vector (10):**

The operation of this two pattern testis similar to i.

M_2 : (stuck open fault in M_2 of the CPL EXNOR/EXOR gate of figure 2.3)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_2, a high resistance is inserted at the lower end of M_2 to isolate it from the rest of circuit. It is observed that when the vector (01) and (11) are applied - M_1 turns off and M_2 remains off since it is stuck-open. Since both MOS are off when (01) and (11) are applied thus producing a non-conducting stage in the gate. Hence, the (01) and (11) vectors can be taken as a Test Vector for M_2 fault. For test vector (01) initialization vectors are (00) and (11). Again for test vector (11) initialization vectors are (01) and (10). The qualitative analysis is similar to the previous case. SPICE simulation result is summarized in the tables.

M_3 : (stuck open fault in M_3 of the CPL EXNOR/EXOR gate of figure 2.3)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_3, a high resistance is inserted at the lower end of M_3 to isolate it from the rest of circuit. It is observed that when the vector (01) and (11) are applied - M_4 turns off and M_3 remains off since it is stuck-open. Since both MOS are off when (01) and (11) are applied thus producing a non-conducting stage in the gate. Hence, the (01) and (11) vectors can be taken as a Test Vector for M_3 fault. For test vector (01) initialization vectors are (00) and (11). Again for test vector (11) initialization vectors are (10) and (01). The qualitative analysis is similar to the previous case. SPICE simulation result is summarized in the tables.

M_4 : (stuck open fault in M_4 of the CPL EXNOR/EXOR gate of figure 2.3)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_4, a high resistance is inserted at the lower end of M_4 to isolate it from the rest of circuit. It is observed that when the vectors (10) and (00) are applied - M_3 turns off and M_4 remains off since it is stuck-open. Since both MOS are off when (10) and (00) are applied thus producing a non-conducting stage in the gate. Hence, the (10) and (00) vector can be taken as a Test Vector for M_4 fault. For test vector (10) initialization vectors are (00) and (11). Again for test vector (00) initialization vectors are (10) and (01). The qualitative analysis is similar to the previous case. SPICE simulation result is summarized in the tables.

3.5.6 SPICE Simulation Results for Stuck open Fault in CPL EXOR/EXNOR Circuit

This section summarizes the SPICE simulation results for a single stuck open fault in the MOS devices of the CPL EXOR/EXNOR ckt.

Table 3.17

SPICE Simulation result for stuck open fault in CPL EXOR/EXNOR.

Effect of fault strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_1	10 M	1	01	00	4.113	0
		10	01	00	4.113	1.22E-12
		100	01	00	2.506	13.31E-06
	100 M	1	01	00	4.113	0
		10	01	00	4.113	1.22E-12
		100	01	00	3.514	13.28E-12
	10 M	1	10	00	4.113	0
		10	10	00	4.113	1.22E-12
		100	10	00	2.506	13.31E-06
	100 M	1	10	00	4.113	0
		10	10	00	4.113	1.22E-12
		100	10	00	3.514	13.28E-12
	10 M	1	00	10	0	0
		10	00	10	0	0
		100	00	10	3.017	3.991E-11
	100 M	1	00	10	0	0
		10	00	10	0	8.354E-15
		100	00	10	1.058	1.89E-17
	10 M	1	11	10	0	0
		10	11	10	0	0
		100	11	10	3.017	3.991E-11
	100 M	1	11	10	0	0
		10	11	10	0	8.354E-15
		100	11	10	1.058	1.89E-17

Table 3.17

SPICE Simulation result for stuck open fault in CPL EXOR/EXNOR.

Effect of fault strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_2	10 M	1	00	01	0	0
		10	00	01	0	0
		100	00	01	3.017	3.991E-11
	100 M	1	00	01	0	0
		10	00	01	0	8.354E-15
		100	00	01	1.058	1.89E-17
	10 M	1	11	01	0	0
		10	11	01	0	0
		100	11	01	3.017	3.991E-11
	100 M	1	11	01	0	0
		10	11	01	0	8.354E-15
		100	11	01	1.058	1.89E-17
	10 M	1	10	11	4.113	0
		10	10	11	4.113	1.22E-12
		100	10	11	2.506	13.31E-06
	100 M	1	10	11	4.113	0
		10	10	11	4.113	1.22E-12
		100	10	11	3.514	13.28E-12
	10 M	1	01	11	4.113	0
		10	01	11	4.113	1.22E-12
		100	01	11	2.506	13.31E-06
	100 M	1	01	11	4.113	0
		10	01	11	4.113	1.22E-12
		100	01	11	3.514	13.28E-12

Table 3.17

SPICE Simulation result for stuck open fault in CPL EXOR/EXNOR.

Effect of fault strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_3	10 M	1	00	01	4.113	0
		10	00	01	4.113	1.22E-12
		100	00	01	2.506	13.31E-06
	100 M	1	00	01	4.113	0
		10	00	01	4.113	1.22E-12
		100	00	01	3.514	13.28E-12
	10 M	1	11	01	4.113	0
		10	11	01	4.113	1.22E-12
		100	11	01	2.506	13.31E-06
	100 M	1	11	01	4.113	0
		10	11	01	4.113	1.22E-12
		100	10	11	3.514	13.28E-12
	10 M	1	10	11	0	0
		10	10	11	0	0
		100	10	11	3.017	3.991E-11
	100 M	1	10	11	0	0
		10	10	11	0	8.354E-15
		100	10	11	1.058	1.89E-17
	10 M	1	01	11	0	0
		10	01	11	0	0
		100	01	11	3.017	3.991E-11
	100 M	1	01	11	0	0
		10	01	11	0	8.354E-15
		100	01	11	1.058	1.89E-17

Table 3.17

SPICE Simulation result for stuck open fault in CPL EXOR/EXNOR.

Effect of fault strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_4	10 M	1	00	10	4.113	0
		10	00	10	4.113	1.22E-12
		100	00	10	2.506	13.31E-06
	100 M	1	00	10	4.113	0
		10	00	10	4.113	1.22E-12
		100	00	10	3.514	13.28E-12
	10 M	1	11	10	4.113	0
		10	11	10	4.113	1.22E-12
		100	11	10	2.506	13.31E-06
	100 M	1	11	10	4.113	0
		10	11	10	4.113	1.22E-12
		100	11	10	3.514	13.28E-12
	10 M	1	10	00	0	0
		10	10	00	0	0
		100	10	00	3.017	3.991E-11
	100 M	1	10	00	0	0
		10	10	00	0	8.354E-15
		100	10	00	1.058	1.89E-17
	10 M	1	01	00	0	0
		10	01	00	0	0
		100	01	00	3.017	3.991E-11
	100 M	1	01	00	0	0
		10	01	00	0	8.354E-15
		100	01	00	1.058	1.89E-17

Effects of Fault Resistance and Time Interval:

As seen from table 3.17, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 10 MΩ to 100 MΩ, the output voltage and Steady state current has a little effect. The time interval has a great effect on the output voltage. Since Steady state current do not increase very high the current monitoring is not possible to determine the stuck open fault. But if we take lower time interval the output voltage variation gives us the fault detection.

Table 3.18

The following table shows the summary for stuck open faults in CPL EXOR/EXNOR circuit.

Summary for Stuck open faults in CPL EXOR/EXNOR Circuit:

Fault	Successful Two Pattern Vectors	O/P Logic Level Un-faulted	O/P Logic Level Faulted	I_{DDQ} (amp)	Logic monitoring possible?	Current monitoring possible?
M_1	(01,00)	10	11	1.22E-12	Yes	No
	(10,00)	10	11	1.22E-12	Yes	No
	(00,10)	01	00	1.89E-17	Yes	No
	(11,10)	01	00	1.89E-17	Yes	No
M_2	(00,01)	01	00	1.89E-17	Yes	No
	(11,01)	01	00	1.89E-17	Yes	No
	(10,11)	10	11	1.22E-12	Yes	No
	(01,11)	10	11	1.22E-12	Yes	No
M_3	(00,01)	10	11	1.22E-12	Yes	No
	(11,01)	10	11	1.22E-12	Yes	No
	(10,11)	01	00	1.89E-17	Yes	No
	(01,11)	01	00	1.89E-17	Yes	No
M_4	(01,00)	01	00	1.89E-17	Yes	No
	(10,00)	01	00	1.89E-17	Yes	No
	(00,10)	10	11	1.22E-12	Yes	No
	(11,10)	10	11	1.22E-12	Yes	No

3.6 Discussion

Testability analysis of Complementary Pass Transistor Logic (CPL) gates under various single stuck faults are presented in this chapter. It is shown that all stuck-on faults in the basic CPL gates (AND/NAND, OR/NOR, XOR/XNOR) can be detected by current monitoring which is popularly known as I_{DDQ} testing but no logic monitoring is possible. Similarly all bridging faults between gate and source of all the MOS devices of basic CPL gates can be detected only by current monitoring. However, for bridging fault between gate and drain of basic CPL gates, it is shown that all faults can be detected by current monitoring, except for the MOS M_3 in AND/NAND gate and MOS M_2 in OR/NOR gates, i.e., for the MOS transistor in which the gate and the drain terminals are connected to the same signal. It is also shown that all stuck-open fault in the basic CPL gates are detectable by logic monitoring using appropriate two-pattern test.

Table 3.19

The following table shows the summary for various faults in CPL basic logic gate circuits.

Summary of fault detection in CPL basic circuits

CPL Basic Gate	Transistor	Stuck-on Fault	Bridging Fault		Stuck-open Fault
			Gate-Source	Gate-Drain	
		Detected by	Detected by	Detected by	Detected by
AND/ NAND	M_1	I_{DDQ} testing	I_{DDQ} testing	I_{DDQ} testing	Two patter test
	M_2	"	"	"	"
	M_3	"	"	*Not detectable*	"
	M_4	"	"	I_{DDQ} testing	"
OR/ NOR	M_1	I_{DDQ} testing	I_{DDQ} testing	I_{DDQ} testing	Two patter test
	M_2	"	"	*Not detectable*	"
	M_3	"	"	I_{DDQ} testing	"
	M_4	"	"	"	"
EXOR/ EXNOR	M_1	I_{DDQ} testing	I_{DDQ} testing	I_{DDQ} testing	Two patter test
	M_2	"	"	"	"
	M_3	"	"	"	"
	M_4	"	"	"	"
Fault coverage		**100%**	**100%**	**83%**	**100%**

CHAPTER 4

FAULT CHARACTERIZATION OF CPL FULL ADDER SUM CIRCUIT

4.1 Introduction

A CPL full adder circuit consists of two circuits. They are full adder sum circuit and full adder carry circuit. The behaviors of CPL full adder sum circuits under single faults in various devices are investigated in this chapter. As stated in Chapter 3 to avoid the complexity of dealing with multiple defects, it is assumed that not more than one defect can occur at a time. Single stuck on, bridging and stuck open faults in CPL MOS are examined. The results of qualitative analysis and extensive SPICE simulation using various fault models are presented in this chapter.

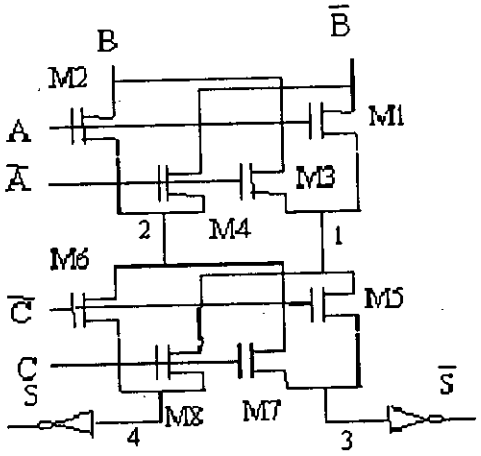


Fig. 4.1 CPL SUM logic circuit

4.2 Behavior Under Single Stuck on faults

The behavior of CPL full adder sum circuits under single stuck on fault on each of the MOS transistors are analyzed in this section.

4.2.1 Qualitative Analysis

M_1 : (stuck on fault in M_1 of the CPL Full Adder Sum gate of figure 4.1)

Referred to figure 4.1 physical defects may cause M_1 to be permanent ON, thus causing a stuck on fault. The fault is modeled in figure 4.2, 4.3, 4.4 and 4.5 where a variable resistance R_f is placed between source and drain terminal of the faulted MOS. The tests vectors (100), (101), (110) and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault.

Test Vector 000

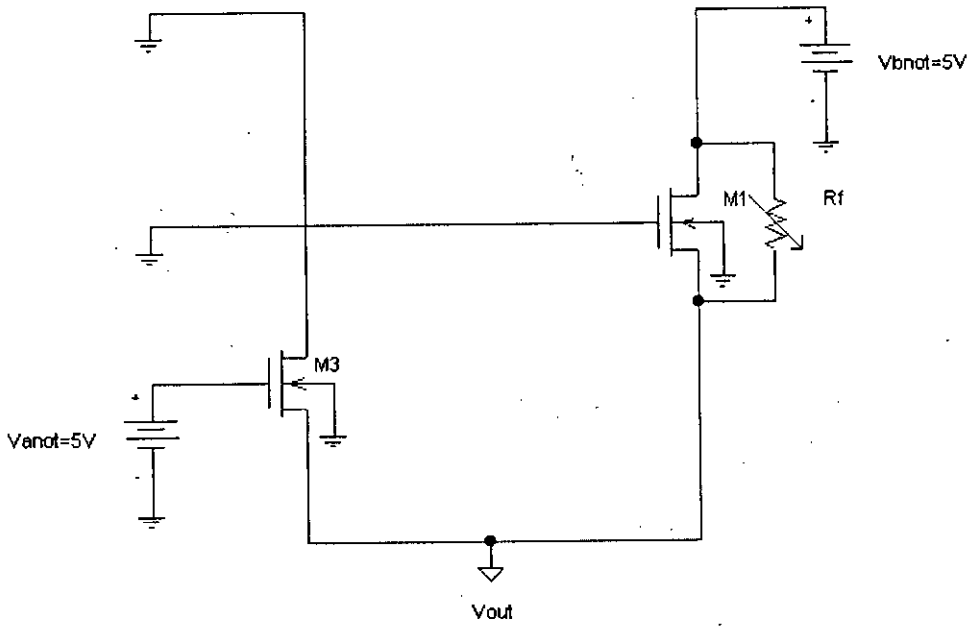


Fig. 4.2 Equivalent circuit for stuck-on fault on MOS M_1 for test vector [A=0, B=0 and C=0].

In Figure 4.2, the vector (000) is applied, M_3, M_4, M_5 and M_6 turn ON and a steady state current I_{DDQ} flows through R_f and M_3. In the faulted circuit, the output at node 1

$$V_{out}=\{R_{on}/(R_f+R_{on})\}V_{IH}$$

Where R_{on} is the on resistance of MOS M_3 and V_{IH} is the input high logic level. When fault strength is maximum , i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, Hence, the stuck on fault at M_1 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I= V_{IH} /(R_f +R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 001:

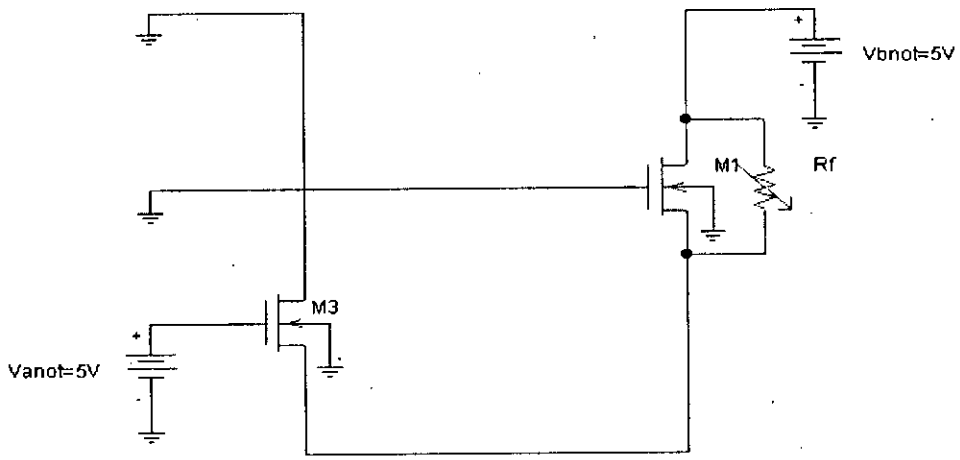


Fig. 4.3 Equivalent circuit for stuck-on fault on MOS M_1 for test vector [A=0, B=0 and C=1].

In Figure 4.3, the vector (001) is applied, M_3, M_4, M_7 and M_8 turn ON and a steady state current I_{DDQ} flows through R_f and M_3. In the faulted circuit, the output voltage varies from low to high depending on the fault strength (R_f). Hence, the stuck on fault at M_1 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH} /(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 010:

In Figure 4.4, the vector (010) is applied, M_3, M_4, M_5 and M_6 turn ON and a steady state current I_{DDQ} flows R_f and M_3 through the circuit. In the faulted circuit, the output is

$$V_{out}=\{R_f/(R_f+R_{on})\}V_{IH}$$

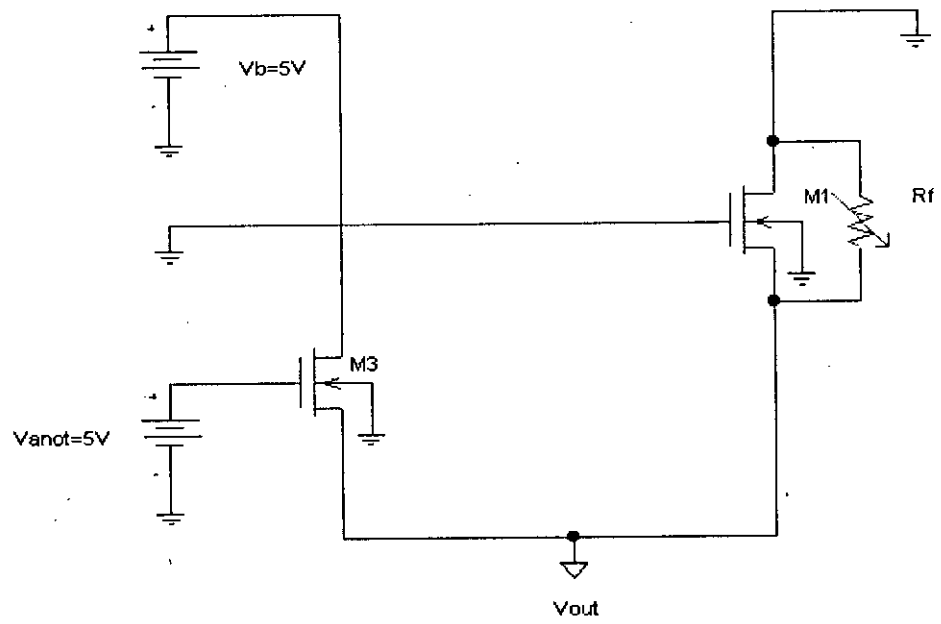


Fig. 4.4 Equivalent circuit for stuck-on fault on MOS M_1 for test vector [A=0, B=1 and C=0].

Above equation shows that when fault strength is maximum , i.e., R_f approaches zero, V_{out} approaches 0 and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, Hence, the stuck on fault at M_1 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH} /(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 011:

In Figure 4.5, the vector (011) is applied, M_3, M_4, M_7 and M_8 turn ON and a steady state current I_{DDQ} flows through R_f and M_3. In the faulted circuit, the output is independent of the fault strength (R_f). Hence, the stuck on fault at M_1 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

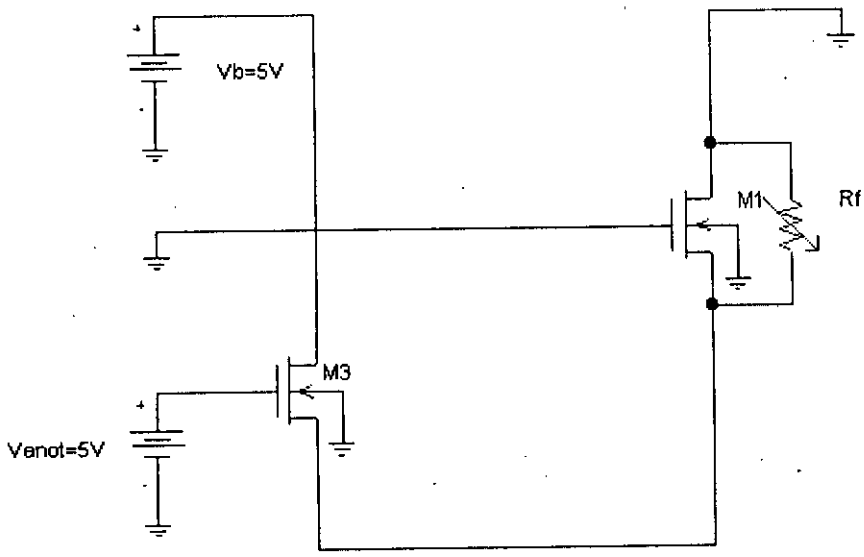


Fig. 4.5 Equivalent circuit for stuck-on fault on MOS M_1 for test vector [A=0, B=1and C=1]

Stuck-on fault on MOS M_2 of the CPL Full Adder Sum circuit.

Similar qualitative analysis has been performed for stuck-on fault on MOS M_2. The fault is modeled with a variable resistance R_f placed between the source and drain terminal of the faulted MOS. The tests vectors (100), (101) (110) and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. When test vectors (000), (001), (010), (011) are applied a large steady state current flows through the circuit. The expression for output voltage and current are similar to the previous case and are not shown here for the sake of conciseness of the thesis. The SPICE simulation results are summarized in the tables at the end of this article.

Stuck-on fault on MOS M_3 of the CPL Full Adder Sum circuit.

Similar qualitative analysis has been performed for stuck-on fault on MOS M_3. The fault is modeled with a variable resistance R_f placed between the source and drain terminal of the faulted MOS. The tests vectors (000), (001), (010) and (011) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. However when test

vector (100), (101), (110), and (111) are applied a large steady state current flows through the circuit. The expression for output voltage and current are similar to the previous case and are not shown here for the sake of conciseness of the thesis. The SPICE simulation results are summarized in the tables at the end of this article.

M_4 : (stuck on fault in M_4 of the CPL Full Adder Sum gate of figure 4.1)

Qualitative analysis has been done for stuck-on fault on MOS M_4 in a similar way. The tests vectors (000), (001), (010) and (011) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. When test vector (100), (101), (110), (111) are applied the output voltage varies from low to high depending on the fault strength, Hence, logic monitoring is not possible. However when these vector are applied a large steady state current flows through the circuit. Hence,, the stuck-on fault on MOS_4 can be detected by current monitoring using the above test vector.

M_5 : (stuck on fault in M_5 of the CPL Full Adder Sum gate of figure 4.1)

The fault is modeled in figure 4.6, 4.7, 4.8 and 4.9 where a variable resistance R_f is placed between the drain and source of the faulted MOS, M_5. The tests vectors (000), (010), (100) and (110) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault.

Test Vector 001:

In Figure 4.6, the vector (001) is applied, M_3, M_4, M_7 and M_8 turn ON and a steady state current I_{DDQ} flows through M_4, M_7, R_f and M_3 of the circuit. In the faulted circuit, the output voltage is

$$V_{out}=\{(R_f+R_{on})/(R_f+3R_{on})\}V_{IH}$$

Above equation shows that when fault strength is maximum , i.e., R_f approaches zero, V_{out} approaches $V_{IH}/3$ and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from $V_{IH}/3$ to V_{IH} depending on R_f. Hence, the stuck on fault at M_5 cannot be detected by logic monitoring. However, the steady state current, I is

significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f + 3R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

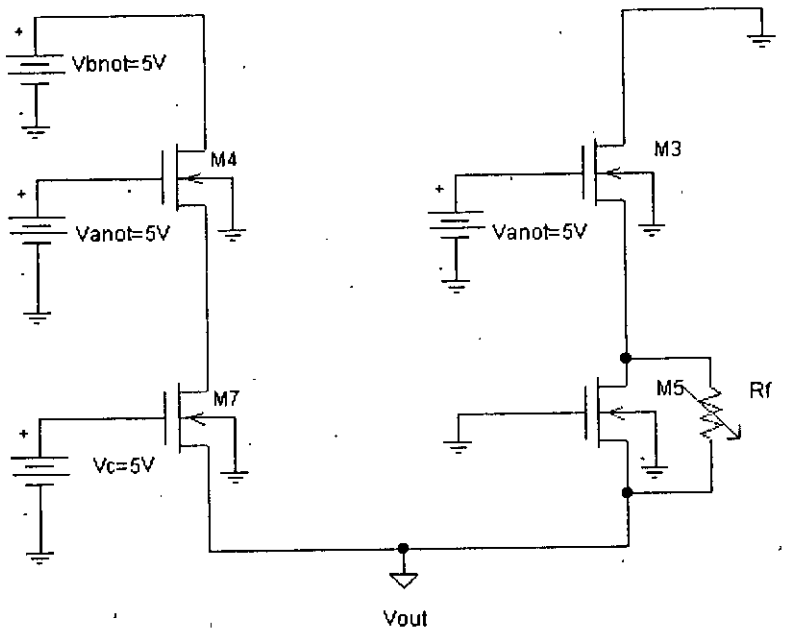


Fig. 4.6. Equivalent circuit of stuck-on fault on MOS M_5 of the CPL Full Adder Sum circuit for test vector [A=0, B=0, C=1].

Test Vector 011:

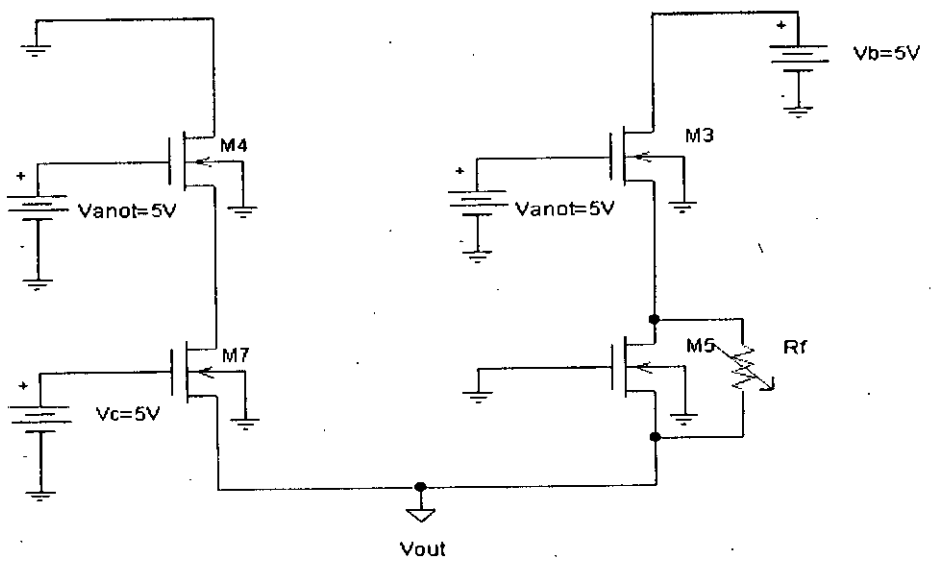


Fig. 4.7. Equivalent circuit of stuck-on fault on MOS M_5 of the CPL Full Adder Sum circuit for test vector [A=0, B=1, C=1].

In Figure 4.7, the vector (011) is applied, M_3, M_4, M_7 and M_8 turn ON and a steady state current I_{DDQ} flows through M_3, R_f, M_7 and M_4 of the circuit. In the faulted circuit, the output voltage is

$$V_{out}=\{2R_{on}/(R_f+3R_{on})\}V_{IH}$$

Above equation shows that when fault strength is maximum , i.e., R_f approaches zero, V_{out} approaches $2V_{IH}/3$ and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from $2V_{IH}/3$ to 0 V depending on R_f. Hence, the stuck on fault at M_5 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f +3R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 101:

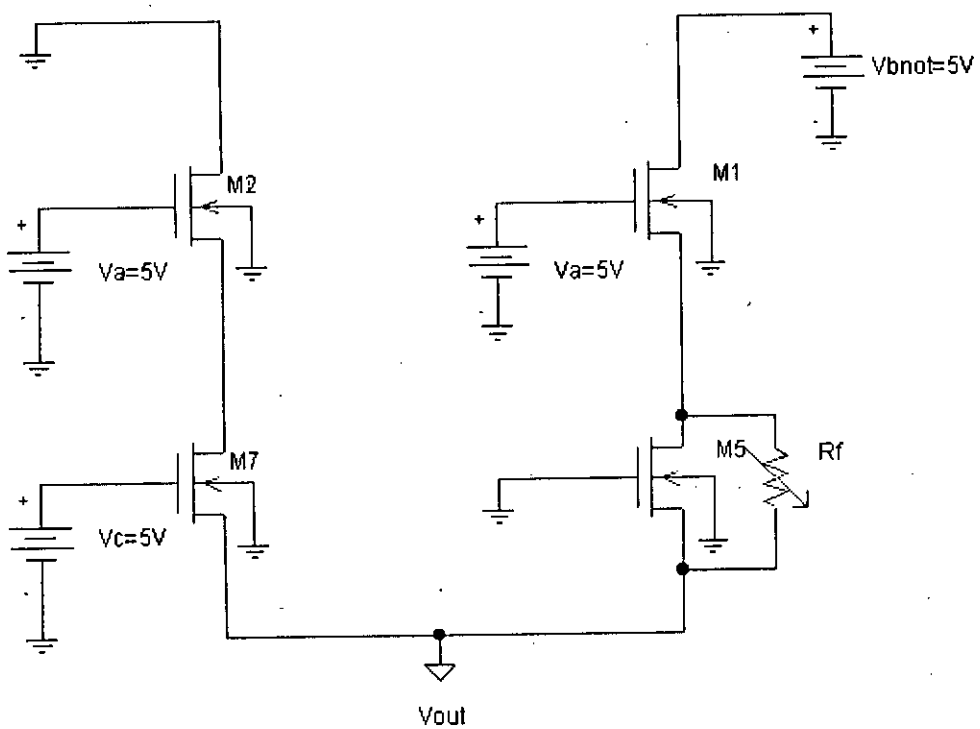


Fig. 4.8. Equivalent circuit of stuck-on fault on MOS M_5 of the CPL Full Adder Sum circuit for test vector [A=1, B=0, C=1].

In Figure 4.8, the vector (101) is applied, M_1, M_2, M_7 and M_8 turn ON and a steady state current I_{DDQ} flows through M_1, R_f, M_7 and M_2 of the circuit. In the faulted circuit, the output voltage is

$$V_{out}=\{2R_{on}/(R_f+3R_{on})\}V_{IH}$$

Above equation shows that when fault strength is maximum , i.e., R_f approaches zero, V_{out} approaches $2V_{IH}/3$ and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from $2V_{IH}/3$ to 0 V depending on R_f. Hence, the stuck on fault at M_5 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f +3R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 111:

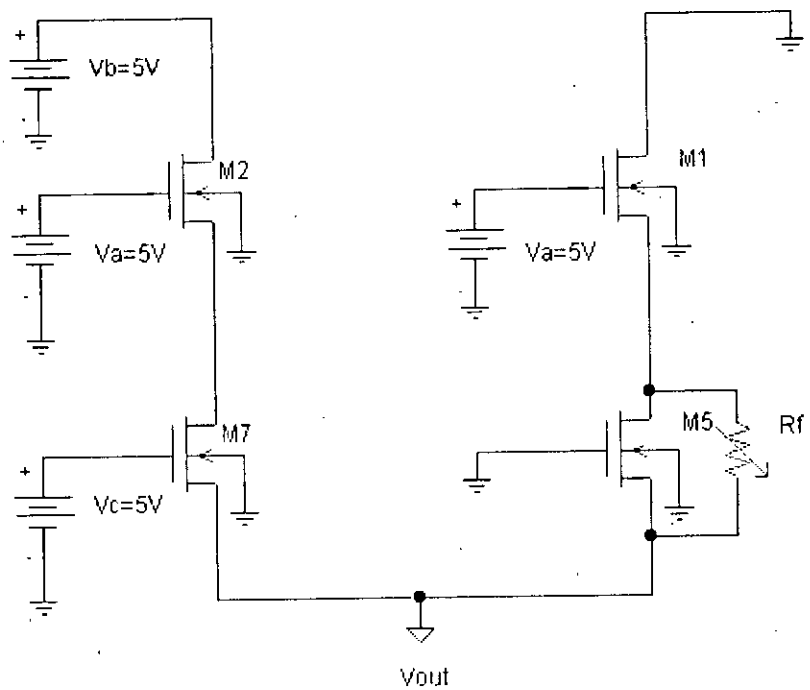


Fig. 4.9. Equivalent circuit of stuck-on fault on MOS M_5 of the CPL Full Adder Sum circuit for test vector [A=1, B=1, C=1].

In Figure 4.9, the vector (111) is applied, M_1, M_2, M_7 and M_8 turn ON and a steady state current I_{DDQ} flows through M_2, M_7, R_f and M_1 of the circuit. In the faulted circuit, the output voltage

$$V_{out}=\{(R_f+R_{on})/(R_f+3R_{on})\}V_{IH}$$

Above equation shows that when fault strength is maximum , i.e., R_f approaches zero, V_{out} approaches $V_{IH}/3$ and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from $V_{IH}/3$ to V_{IH} depending on R_f. Now since V_{out} can attain any value from $V_{IH}/3$ to V_{IH} depending on R_f. Hence, the stuck on fault at M_5 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f +3R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

M_6 : (stuck on fault in M_6 of the CPL Full Adder Sum gate of figure 4.1)

Qualitative analysis have been done for stuck-on fault on MOS M_6 in a similar way. The tests vectors (000), (001), (010) and (011) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. When test vectors (001), (011), (101) and (111) are applied a large steady state current flows through the circuit. The expression for output voltage and current are similar to the previous case and are not shown here for the sake of conciseness of the thesis. The SPICE simulation results are summarized in the tables at the end of this article.

M_7 : (stuck on fault in M_7 of the CPL Full Adder Sum gate of figure 4.1)

Qualitative analysis have been done for stuck-on fault on MOS M_7 in a similar way. The tests vectors (001), (011), (101) and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. When test vectors (000), (010), (100) and (110) are applied a large steady state current flows through the circuit. The expression for output voltage and current are similar to the previous case and are not shown here for the sake of conciseness of the thesis. The SPICE simulation results are summarized in the tables at the end of this article.

M_8 : (stuck on fault in M_8 of the CPL Full Adder Sum gate of figure 4.1)

Qualitative analysis have been done for stuck-on fault on MOS M_8 in a similar way. The tests vectors (001), (011), (101) and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. When test vectors (000), (010), (100) and (110) are applied a large steady state current flows through the circuit. The expression for output voltage and current are similar to the previous case and are not shown here for the sake of conciseness of the thesis. The SPICE simulation results are summarized in the tables at the end of this article.

4.2.2 SPICE Simulation Results

This section summarizes the SPICE simulation results for a single stuck on fault in the MOS devices of the CPL full adder sum circuit.

Table: 4.1

SPICE Simulation result for stuck on fault in CPL Full Adder Sum Ckt.

Effect of fault Strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_1	1	0	0	0	3.267	2.350E-03
	10	0	0	0	3.267	2.350E-03
	100	0	0	0	3.267	2.330E-03
	1K	0	0	0	2.824	2.180E-03
	10K	0	0	0	0.266	4.730E-04
	100K	0	0	0	0.026	4.970E-05
M_1	1	0	0	5	3.267	2.346E-03
	10	0	0	5	3.267	2.345E-03
	100	0	0	5	3.267	2.329E-03
	1K	0	0	5	3.248	2.176E-03
	10K	0	0	5	3.243	4.735E-04
	100K	0	0	5	3.240	4.989E-05
M_1	1	0	5	0	0.002	2.340E-03
	10	0	5	0	0.023	2.320E-03
	100	0	5	0	0.209	2.090E-03
	1K	0	5	0	1.111	1.111E-03
	10K	0	5	0	2.329	2.330E-04
	100K	0	5	0	2.943	2.940E-05
M_1	1	0	5	5	0	2.344E-03
	10	0	5	5	0	2.318E-03
	100	0	5	5	0	2.093E-03
	1K	0	5	5	0	1.111E-03
	10K	0	5	5	0	2.329E-04
	100K	0	5	5	0	2.944E-05

Table: 4.1 (Cont'd)

SPICE Simulation result for stuck on fault in CPL Full Adder Sum Ckt.

Effect of fault Strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_2	1	0	0	0	0	2.340E-03
	10	0	0	0	0	2.310E-03
	100	0	0	0	0	2.090E-03
	1K	0	0	0	0	1.110E-03
	10k	0	0	0	0	2.320E-04
	100k	0	0	0	0	2.940E-05
M_2	1	0	0	5	0	2.344E-03
	10	0	0	5	0.002	2.318E-03
	100	0	0	5	0.209	2.093E-03
	1k	0	0	5	1.111	1.111E-03
	10k	0	0	5	2.329	2.329E-04
	100k	0	0	5	2.943	2.943E-05
M_2	1	0	5	0	3.266	2.340E-03
	10	0	5	0	3.266	2.340E-03
	100	0	5	0	3.266	2.320E-03
	1K	0	5	0	3.266	2.170E-03
	10k	0	5	0	3.266	4.730E-04
	100k	0	5	0	3.266	4.970E-05
M_2	1	0	5	5	3.263	2.346E-03
	10	0	5	5	3.263	2.345E-03
	100	0	5	5	3.263	2.329E-03
	1k	0	5	5	2.824	2.176E-03
	10k	0	5	5	0.266	4.735E-04
	100k	0	5	5	0.002	4.990E-05

Table: 4.1 (Cont'd)

SPICE Simulation result for stuck on fault in CPL Full Adder Sum Ckt.

Effect of fault Strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_3	1	5	0	0	0.023	2.340E-03
	10	5	0	0	0.023	2.320E-03
	100	5	0	0	0.209	2.090E-03
	1K	5	0	0	1.120	1.110E-03
	10K	5	0	0	2.329	2.330E-04
	100K	5	0	0	2.943	2.940E-05
M_3	1	5	0	5	0	2.344E-03
	10	5	0	5	0	2.318E-03
	100	5	0	5	0	2.093E-03
	1K	5	0	5	0	1.111E-03
	10K	5	0	5	0	2.329E-04
	100K	5	0	5	0	2.943E-05
M_3	1	5	5	0	3.267	2.340E-03
	10	5	5	0	3.267	2.350E-03
	100	5	5	0	3.267	2.330E-03
	1K	5	5	0	3.267	2.180E-03
	10K	5	5	0	0.266	4.730E-04
	100K	5	5	0	0.026	4.970E-05
M_3	1	5	5	5	3.262	2.346E-03
	10	5	5	5	3.262	2.345E-03
	100	5	5	5	3.242	2.329E-03
	1K	5	5	5	3.247	2.176E-03
	10K	5	5	5	3.245	4.734E-04
	100K	5	5	5	3.239	4.991E-05

Table: 4.1 (Cont'd)

SPICE Simulation result for stuck on fault in CPL Full Adder Sum Ckt.

Effect of fault Strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_4	1	5	0	0	3.266	2.340E-03
	10	5	0	0	3.266	2.340E-03
	100	5	0	0	3.266	2.390E-03
	1k	5	0	0	3.266	2.170E-03
	10k	5	0	0	3.266	4.730E-04
	100k	5	0	0	3.266	4.970E-05
M_4	1	5	0	5	3.264	2.346E-03
	10	5	0	5	3.264	2.345E-03
	100	5	0	5	3.264	2.329E-03
	1k	5	0	5	2.824	2.176E-03
	10k	5	0	5	0.266	4.735E-04
	100k	5	0	5	0.026	4.970E-05
M_4	1	5	5	0	0	2.390E-03
	10	5	5	0	0	2.320E-03
	100	5	5	0	0	2.090E-03
	1k	5	5	0	0	1.110E-03
	10k	5	5	0	0	2.330E-04
	100k	5	5	0	0	2.940E-05
M_4	1	5	5	5	0.002	2.344E-03
	10	5	5	5	0.021	2.318E-03
	100	5	5	5	0.209	2.093E-03
	1k	5	5	5	1.111	1.111E-03
	10k	5	5	5	2.329	2.329E-04
	100k	5	5	5	2.943	2.940E-05

Table: 4.1 (Cont'd)

SPICE Simulation result for stuck on fault in CPL Full Adder Sum Ckt.

Effect of fault Strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_5	1	0	0	5	0.566	9.16E-04
	10	0	0	5	0.570	9.12E-04
	100	0	0	5	0.625	8.78E-04
	1k	0	0	5	1.020	6.45E-04
	10k	0	0	5	2.057	1.94E-04
	100k	0	0	5	2.817	2.80E-05
M_5	1	0	5	5	1.320	9.16E-04
	10	0	5	5	1.320	9.13E-04
	100	0	5	5	1.260	8.89E-04
	1k	0	5	5	0.900	6.99E-04
	10k	0	5	5	0.240	2.14E-04
	100k	0	5	5	0.030	2.92E-05
M_5	1	5	0	5	1.320	9.12E-03
	10	5	0	5	1.319	9.13E-04
	100	5	0	5	1.260	8.89E-04
	1k	5	0	5	0.900	6.94E-04
	10k	5	0	5	0.234	2.14E-03
	100k	5	0	5	0.030	2.92E-05
M_5	1	5	5	5	0.566	9.16E-04
	10	5	5	5	0.571	9.12E-04
	100	5	5	5	0.625	8.70E-04
	1k	5	5	5	1.019	6.45E-04
	10k	5	5	5	2.060	1.95E-04
	100k	5	5	5	2.817	2.80E-05

Table: 4.1 (Cont'd)

SPICE Simulation result for stuck on fault in CPL Full Adder Sum Ckt.

Effect of fault Strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_6	1	0	0	5	1.320	9.16E-04
	10	0	0	5	1.320	9.13E-04
	100	0	0	5	1.260	8.89E-04
	1k	0	0	5	0.900	6.99E-04
	10k	0	0	5	0.240	2.14E-04
	100k	0	0	5	0.030	2.92E-05
M_6	1	0	5	5	0.566	9.16E-04
	10	0	5	5	0.570	9.12E-04
	100	0	5	5	0.625	8.78E-04
	1k	0	5	5	1.020	6.45E-04
	10k	0	5	5	2.057	1.94E-04
	100k	0	5	5	2.817	2.80E-05
M_6	1	5	0	5	0.566	9.16E-04
	10	5	0	5	0.570	9.12E-04
	100	5	0	5	0.625	8.78E-04
	1k	5	0	5	1.020	6.45E-04
	10k	5	0	5	2.057	1.94E-04
	100k	5	0	5	2.817	2.80E-05
M_6	1	5	5	5	1.320	9.16E-04
	10	5	5	5	1.320	9.13E-04
	100	5	5	5	1.260	8.89E-04
	1k	5	5	5	0.900	6.99E-04
	10k	5	5	5	0.240	2.14E-04
	100k	5	5	5	0.030	2.92E-05

Table: 4.1 (Cont'd)

SPICE Simulation result for stuck on fault in CPL Full Adder Sum Ckt.

Effect of fault Strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp).
M_7	1	0	0	0	1.324	9.16E-04
	10	0	0	0	1.319	9.13E-04
	100	0	0	0	1.267	8.89E-04
	1k	0	0	0	0.900	6.94E-04
	10k	0	0	0	0.234	2.14E-04
	100k	0	0	0	0.030	2.92E-05
M_7	1	0	5	0	0.566	9.16E-04
	10	0	5	0	0.571	9.12E-04
	100	0	5	0	0.625	8.78E-04
	1k	0	5	0	1.019	6.45E-04
	10k	0	5	0	2.057	1.95E-04
	100k	0	5	0	2.817	2.80E-05
M_7	1	5	0	0	0.566	9.16E-04
	10	5	0	0	0.571	9.12E-04
	100	5	0	0	0.625	8.78E-04
	1k	5	0	0	1.019	6.45E-04
	10k	5	0	0	2.057	1.95E-04
	100k	5	0	0	2.817	2.80E-05
M_7	1	5	5	0	1.324	9.16E-04
	10	5	5	0	1.319	9.13E-04
	100	5	5	0	1.270	8.89E-04
	1k	5	5	0	0.900	6.94E-04
	10k	5	5	0	0.235	2.14E-04
	100k	5	5	0	0.030	2.92E-05

Table: 4.1 (Cont'd)

SP1CE Simulation result for stuck on fault in CPL Full Adder Sum Ckt.

Effect of fault Strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_8	1	0	0	0	0.566	9.16E-04
	10	0	0	0	0.570	9.12E-04
	100	0	0	0	0.625	8.78E-04
	1k	0	0	0	1.020	6.45E-04
	10k	0	0	0	2.057	1.94E-04
	100k	0	0	0	2.817	2.80E-05
M_8	1	0	5	0	1.320	9.16E-04
	10	0	5	0	1.320	9.13E-04
	100	0	5	0	1.260	8.89E-04
	1k	0	5	0	0.900	6.99E-04
	10k	0	5	0	0.240	2.14E-04
	100k	0	5	0	0.030	2.92E-05
M_8	1	5	0	0	1.320	9.16E-04
	10	5	0	0	1.320	9.13E-04
	100	5	0	0	1.260	8.89E-04
	1k	5	0	0	0.900	6.99E-04
	10k	5	0	0	0.240	2.14E-04
	100k	5	0	0	0.030	2.92E-05
M_8	1	5	5	0	0.566	9.16E-04
	10	5	5	0	0.570	9.12E-04
	100	5	5	0	0.625	8.78E-04
	1k	5	5	0	1.020	6.45E-04
	10k	5	5	0	2.057	1.94E-04
	100k	5	5	0	2.817	2.80E-05

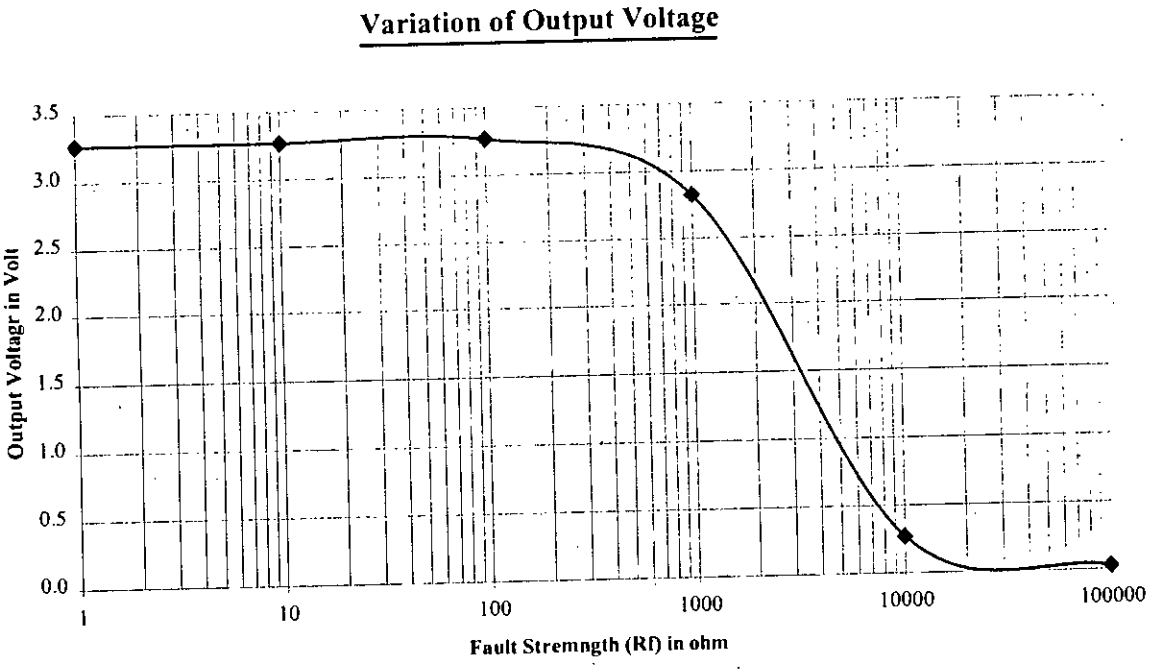


Fig 4.10: Output voltage vs. Fault strength

(Stuck on fault for M_1(000), M_2(011), M_3(110) and M_4(101))

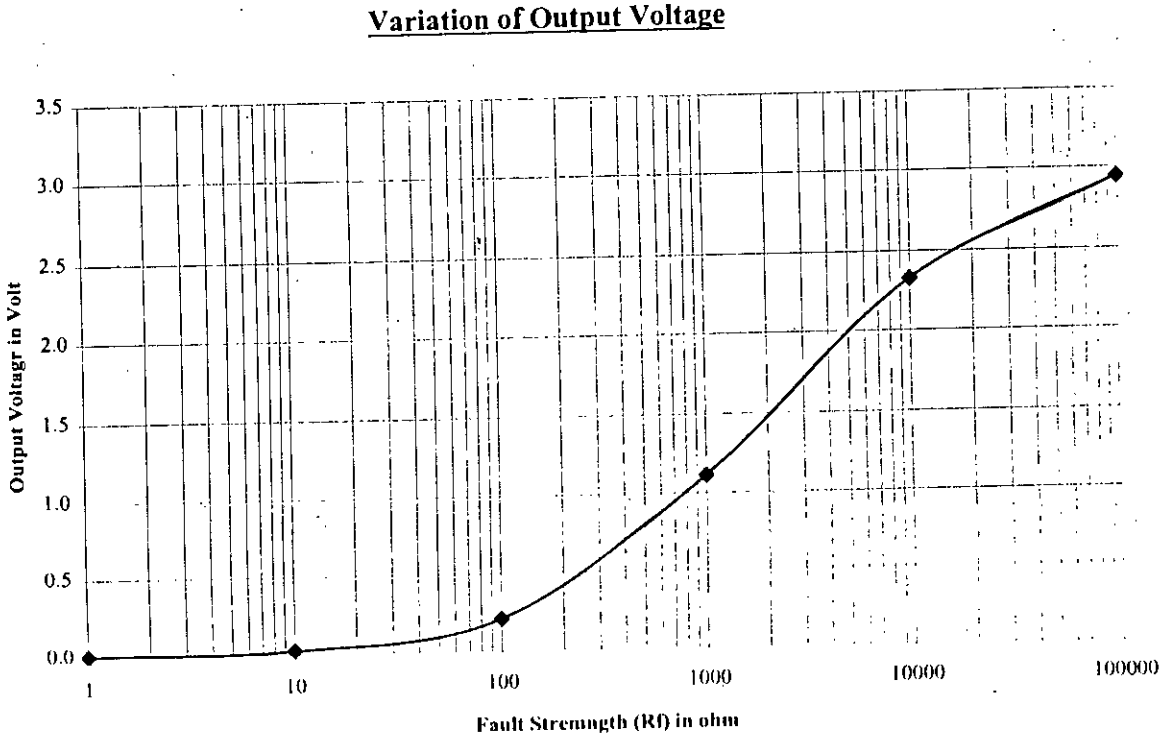


Fig 4.11: Output voltage vs. Fault strength

(Stuck on fault for M_1 (010), M_2 (001), M_3 (100) and M_4 (111))

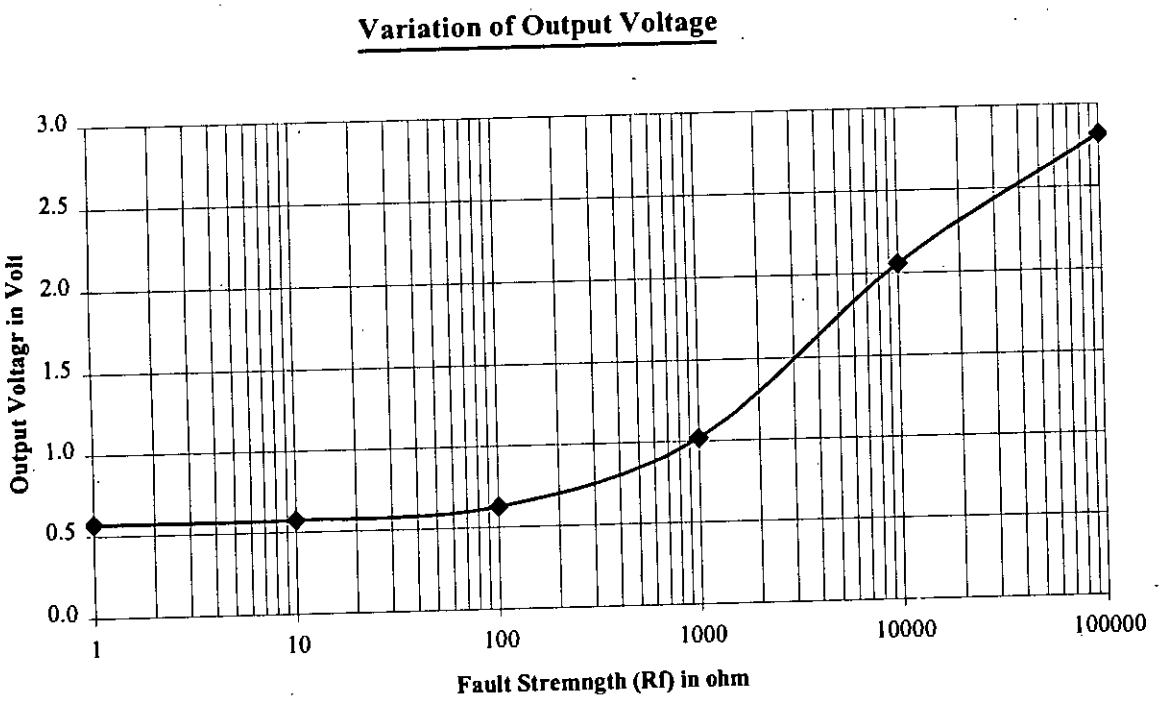


Fig 4.12: Output voltage vs. Fault strength

(Stuck on fault for M_5(001)(111), M_6(011)(101), M_7(010)(100), M_8(000)(110))

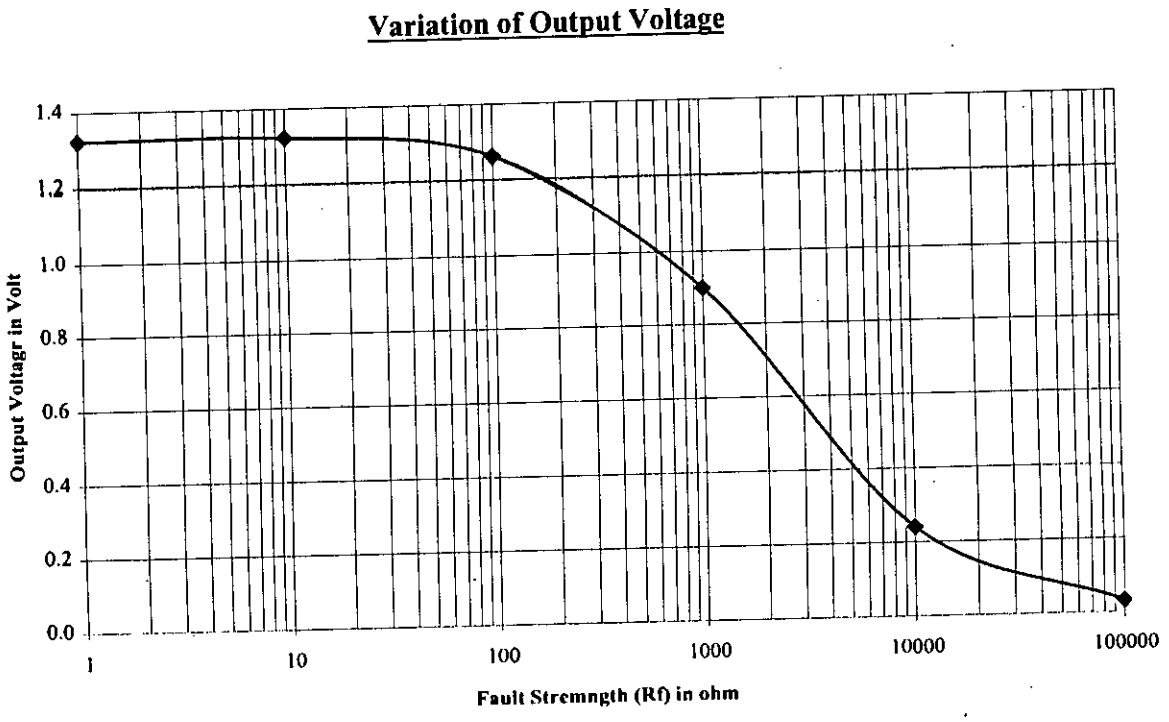


Fig 4.13: Output voltage vs. Fault strength

(Stuck on fault for M_5(011)(101), M_6(001)(111), M_7(000)(110), M_8(010)(100))

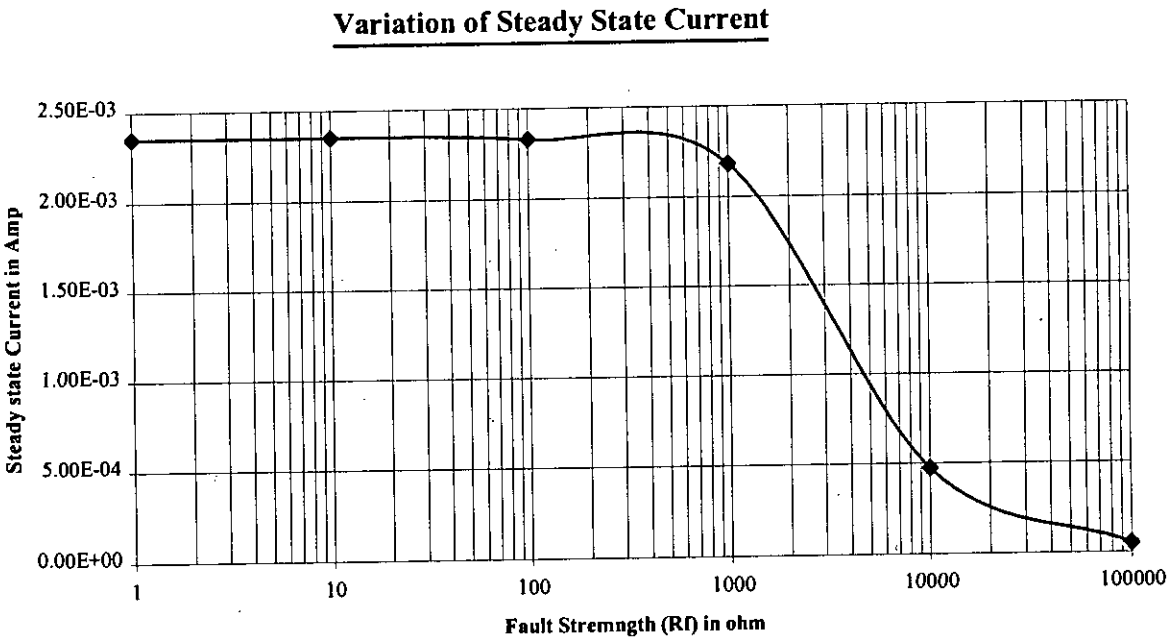


Fig 4.14: Steady State Current vs. Fault strength

(Stuck on fault for M_1(000), M_2(011), M_3(110) and M_4(101))

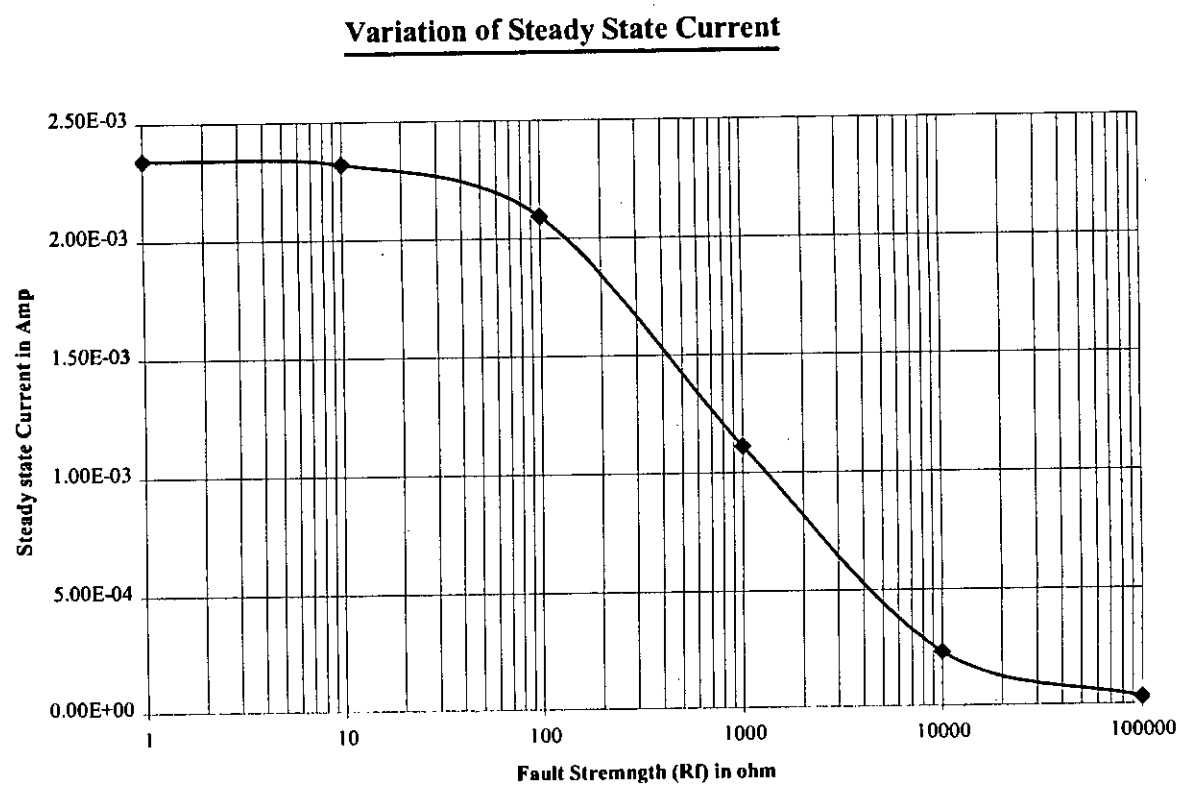


Fig 4.15: Steady State Current vs. Fault strength

(Stuck on fault for M_1 (010), M_2 (001), M_3 (100) and M_4 (111))

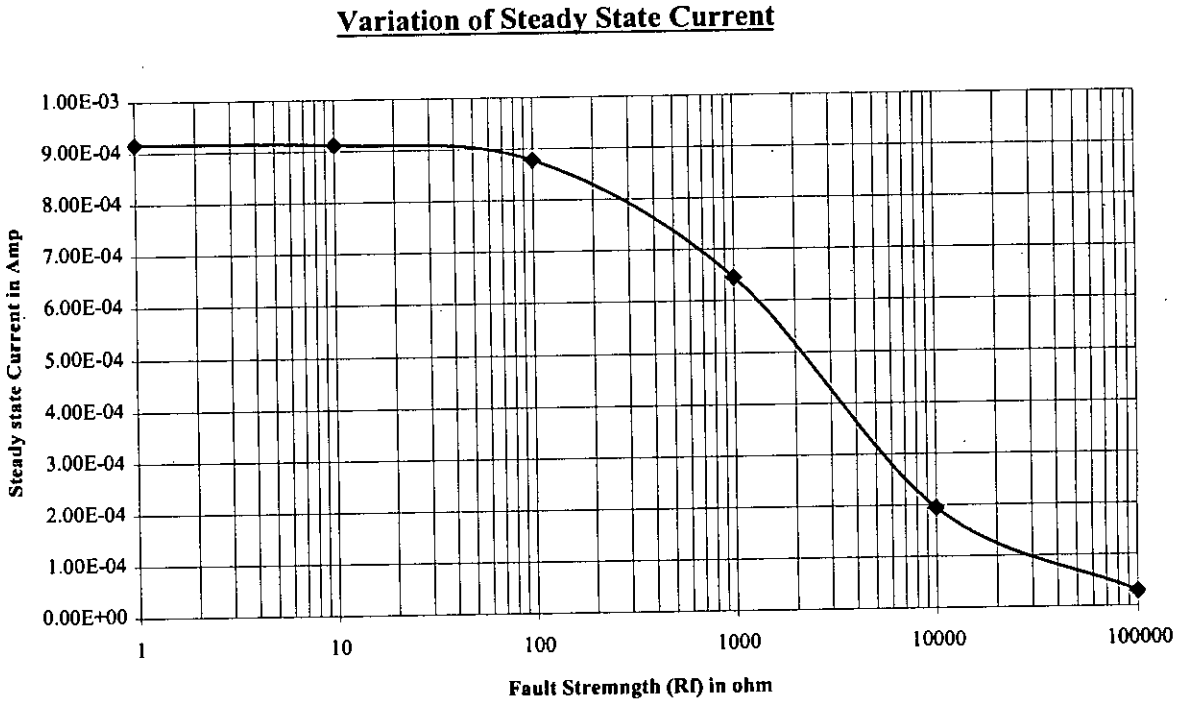


Fig 4.16: Steady State Current vs. Fault strength

(Stuck on fault for M_5(001)(111), M_6(011)(101), M_7(010)(100), M_8(000)(110))

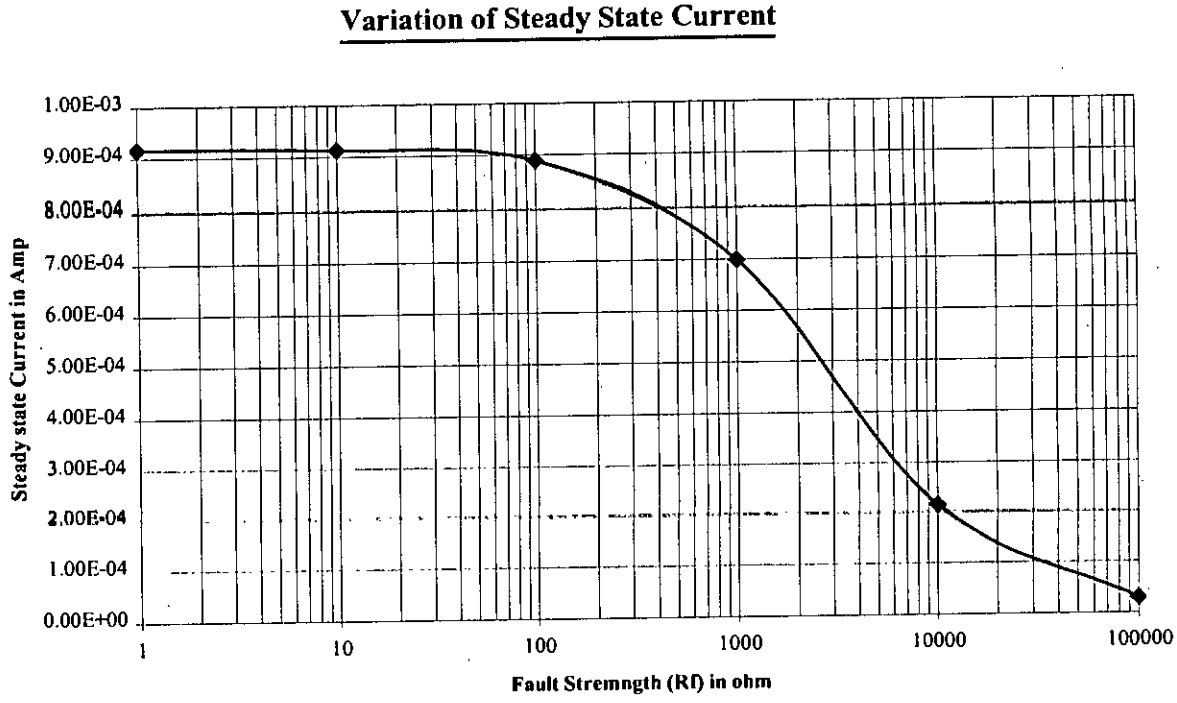


Fig 4.17: Steady State Current vs. Fault strength

(Stuck on fault for M_5(011)(101), M_6(001)(111), M_7(000)(110), M_8(010)(100))

Effects of Fault Resistance

From the results of Table 4.1 and Fig 4.10 to 4.13 show, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 1 Ω to 100 kΩ, the output voltage varies from 0 to 3.267 Volt. This appreciable variation in output voltage clearly shows that the output logic level is indeterminable. This agrees with our prediction that the fault cannot be detected by logic monitoring. As seen from the table and fig 4.14 to 4.17, steady state current is in the range of miliampere compared to normal operating current of 2.968E-11 A. Therefore, the fault can be detected by current monitoring.

Table 4.2

The following table shows the summary for stuck on faults in CPL Full Adder Sum circuit.

Summary for Stuck on faults in CPL Full Adder Sum Circuit

Fault	Successful Test Vector	Output Logic Level (Volt)	I_{DDQ} (amp)	Logic monitoring possible?	Current monitoring possible?
M_1	(000),(001), (010), (011)	0 to 3.267	2.350E-03 to 2.940E-05	No	Yes
M_2	(000),(001), (010), (011)	0 to 3.266	2.346E-03 to 2.940E-05	No	Yes
M_3	(100),(101), (110), (111)	0 to 3.267	2.346E-03 to 2.940E-05	No	Yes
M_4	(100),(101) (110), (111)	0 to 3.266	2.346E-03 to 2.940E-05	No	Yes
M_5	(001),(011), (101), (111)	0 to 2.817	9.16E-04 to 2.80E-05	No	Yes
M_6	(001),(011), (101), (111)	0 to 2.817	9.16E-04 to 2.80E-05	No	Yes
M_7	(000),(010), (100), (110)	0 to 2.817	9.16E-04 to 2.80E-05	No	Yes
M_8	(000),(010), (100), (110)	0 to 2.817	9.16E-04 to 2.80E-05	No	Yes

4.3 Behavior Under Single Bridging faults

The behavior of CPL full adder sum circuits under single bridging faults in MOS transistors are analyzed in this section.

4.3.1 Qualitative Analysis

M_1 : (Bridging fault in M_1 of the CPL Full Adder Sum gate of figure 4.1)

Referred to figure 4.1 physical defects may cause a short circuit to exist between gate and source of M_1, thus causing a bridging fault. The fault is modeled by placing a resistance R_f between the gate and the source terminal of the faulty device M_1 as shown in figure 4.18, 4.19, 4.20 and 4.21. The tests vectors (000), (001), (100) and (101) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault.

Test Vector 010

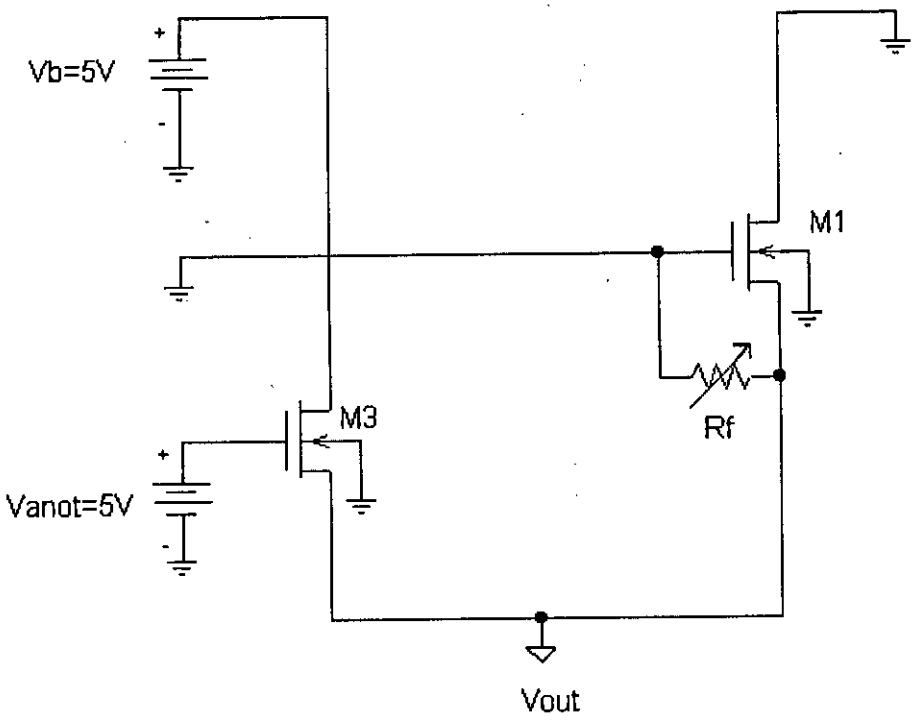


Fig. 4.18 Equivalent circuit of gate to source bridging fault in MOS M_1 of CPL Full adder SUM circuit. Test Vector [A=0, B=1, C=0].

In Figure 4.18, the vector (010) is applied, M_3, M_4, M_5 and M_6 turn ON and a steady state current I_{DDQ} flows through M_3 and R_f of the circuit. In the faulted circuit, the output voltage at node 1 is

$$V_{out} = \{R_f/(R_f+R_{on})\}V_{IH}$$

Above equation shows that when fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, Hence, the bridging fault at M_1 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 011

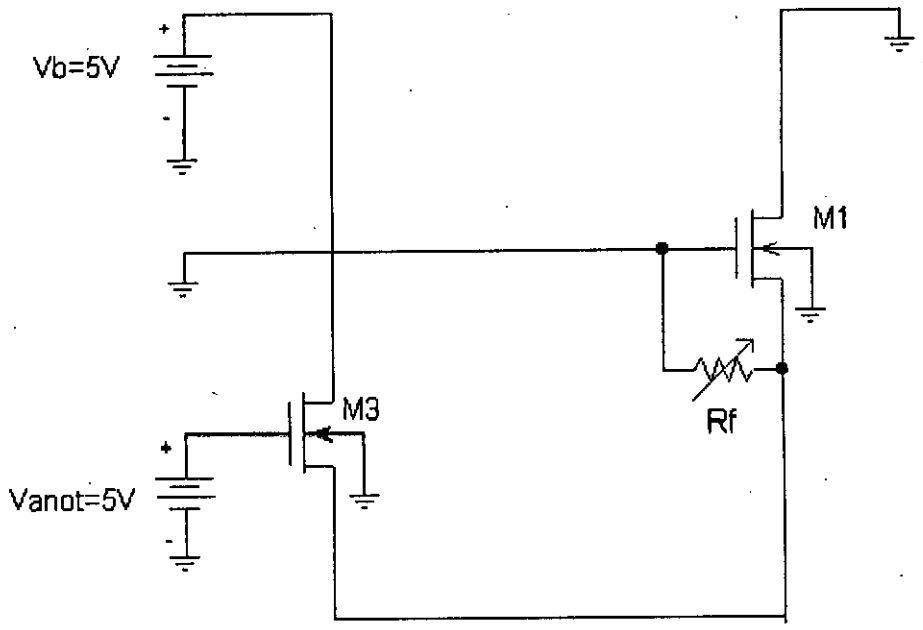


Fig. 4.19 Equivalent circuit of gate to source bridging fault in MOS M_1 of CPL Full adder SUM circuit. Test vector [A=0, B=1, B=1].

In Figure 4.19, the vector (011) is applied, M_3, M_4, M_7 and M_8 turn ON and a steady state current I_{DDQ} flows through M_3 and R_f of the circuit. In the faulted circuit, the output in independent of fault strength R_f. Hence, the bridging fault at M_1 cannot be detected by logic monitoring. However, the steady state current, I is significantly

large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 110

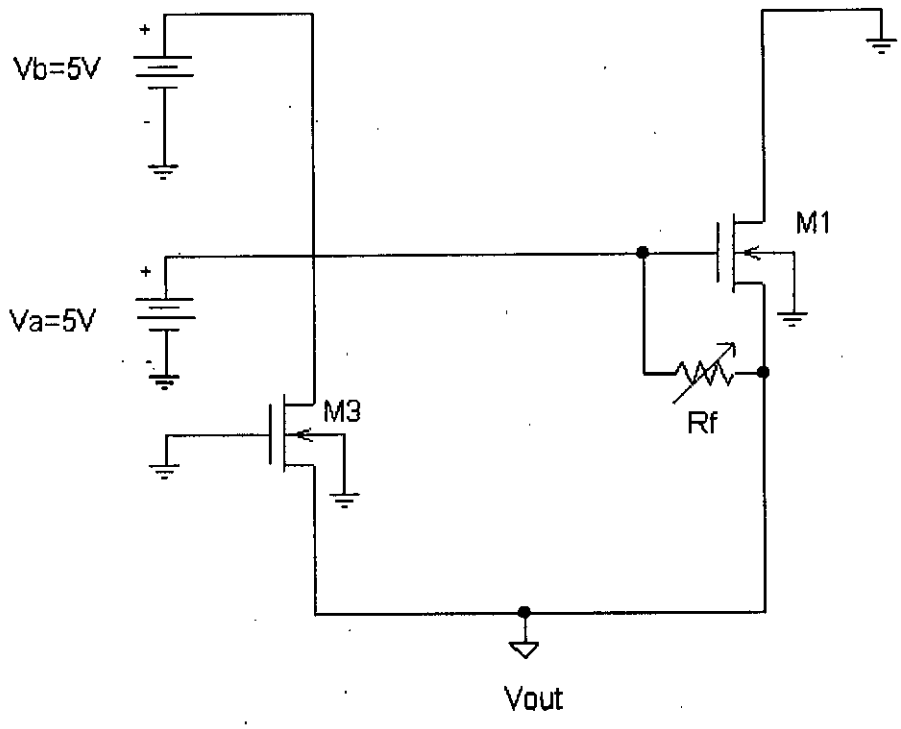


Fig. 4.20 Equivalent circuit of gate to source bridging fault in MOS M_1 of CPL Full adder SUM circuit. Test Vector [A=1, B=1, C=0].

In Figure 4.20, the vector (110) is applied, M_1, M_2, M_5 and M_6 turn ON and a steady state current I_{DDQ} flows through M_1 and R_f of the circuit. In the faulted circuit, the output voltage is

$$V_{out}=\{R_{on}/(R_f+R_{on})\}V_{IH}$$

Above equation shows that when fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, Hence, the bridging fault at M_1 cannot be detected by logic monitoring. However, the steady state current, I is

significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 111

In Figure 4.21, the vector (111) is applied, M_1, M_2, M_7 and M_8 turn ON and a steady state current I_{DDQ} flows through M_1 and R_f of the circuit. In the faulted circuit, the output in independent of fault strength R_f. Hence, the bridging fault at M_1 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

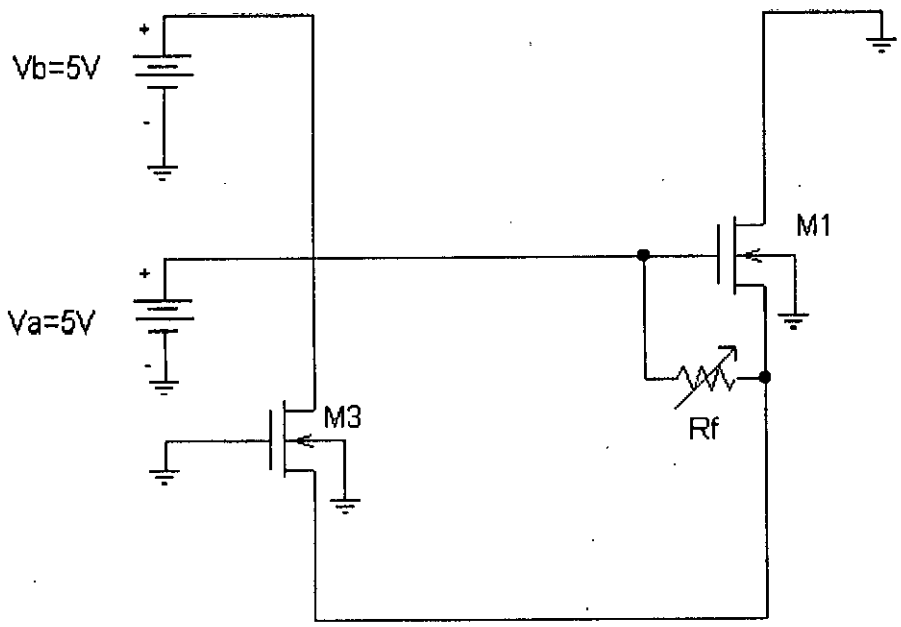


Fig. 4.21 Equivalent circuit of gate to source bridging fault in MOS M_1 of CPL Full adder SUM circuit. Test Vector [A=1, B=1, C=1]

M_2 : (Bridging fault in M_2 of the CPL Full Adder Sum gate of figure 4.1)

Qualitative analysis have been performed for gate to source bridging fault on MOS M_2. The fault is modeled with a variable resistance R_f placed between the gate and source terminal of the faulted MOS. The tests vectors (010), (011) (110) and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. When test vectors (000), (001), (100), (101) are applied a large steady state current flows through the circuit. The expression for output voltage and current are similar to the previous case and are not shown here for the sake of conciseness of the thesis. The SPICE simulation results are summarized in the tables at the end of this article.

M_3 : (Bridging fault in M_3 of the CPL Full Adder Sum gate of figure 4.1)

Qualitative analysis have been performed for gate to source bridging fault on MOS M_3. The fault is modeled with a variable resistance R_f placed between the gate and source terminal of the faulted MOS. The tests vectors (010), (011) (110) and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. When test vectors (000), (001), (100), (101) are applied a large steady state current flows through the circuit. The expression for output voltage and current are similar to the previous case and are not shown here for the sake of conciseness of the thesis. The SPICE simulation results are summarized in the tables at the end of this article.

M_4 : (Bridging fault in M_4 of the CPL Full Adder Sum gate of figure 4.1)

Qualitative analysis have been performed for gate to source bridging fault on MOS M_4. The fault is modeled with a variable resistance R_f placed between the gate and source terminal of the faulted MOS. The tests vectors (000), (010) (100) and (101) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. When test vectors (010), (011), (110), (111) are applied a large steady state current flows through the circuit. The expression for output voltage and current are similar to the previous case and are not shown here for the sake of conciseness of the thesis. The SPICE simulation results are summarized in the tables at the end of this article.

M_5 : (Bridging fault in M_5 of the CPL Full Adder Sum gate of figure 4.1)

The fault is modeled in figure 4.22, 4.23, 4.24 and 4.25 where a variable resistance R_f is placed between the gate and source terminal of the faulted MOS M_5. The tests vectors (010), (011), (100), and (101) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault.

Test Vector 000

In Figure 4.22, the vector (000) is applied, M_3, M_4, M_5 and M_6 turn ON and a steady state current I_{DDQ} flows through M_3, M_5 and R_f the circuit. In the faulted circuit, the output voltage is

$$V_{out} = \{2R_{on}/(R_f+2R_{on})\}V_{IH}$$

Above equation shows that when fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, Hence, the bridging fault at M_5 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f+2R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

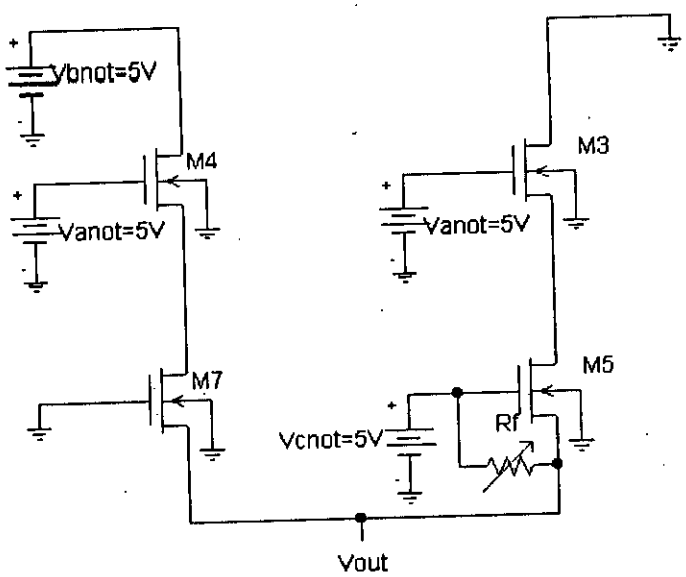


Fig. 4.22 Equivalent circuit of gate to source bridging fault on MOS M_5 of the CPL Full Adder Sum Circuit. Test Vector [A=0, B=0, C=0]

Test Vector 001

In Figure 4.23, the vector (001) is applied, M_3, M_4, M_7 and M_8 turn ON and a steady state current I_{DDQ} flows through M_4, M_7 and R_f the circuit. In the faulted circuit, the output voltage is

$$V_{out} = \{R_f/(R_f+2R_{on})\}V_{IH}$$

Above equation shows that when fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, Hence, the bridging fault at M_5 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f+2R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

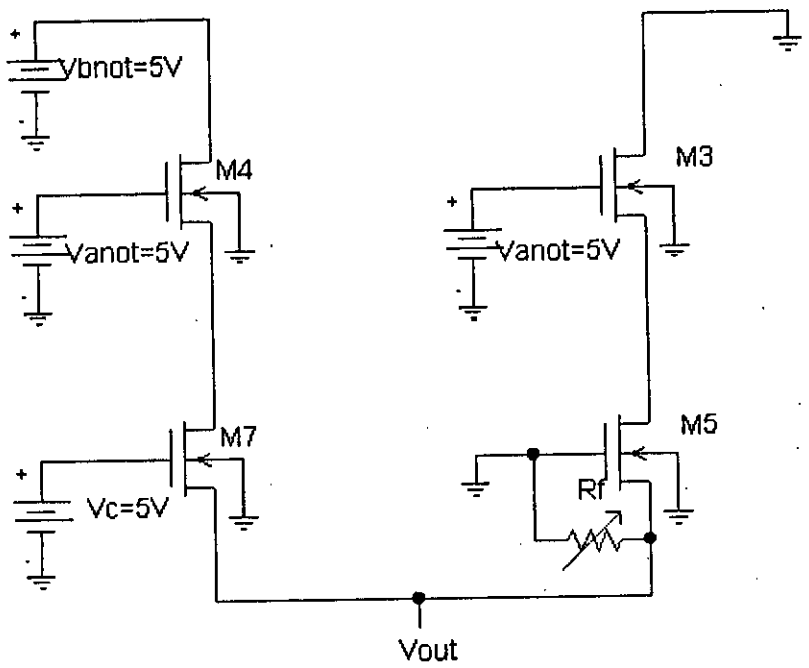


Fig. 4.23 Equivalent circuit of gate to source bridging fault on MOS M_5 of the CPL Full Adder Sum Circuit. Test Vector [A=0, B=0, C=1].

Test Vector 110

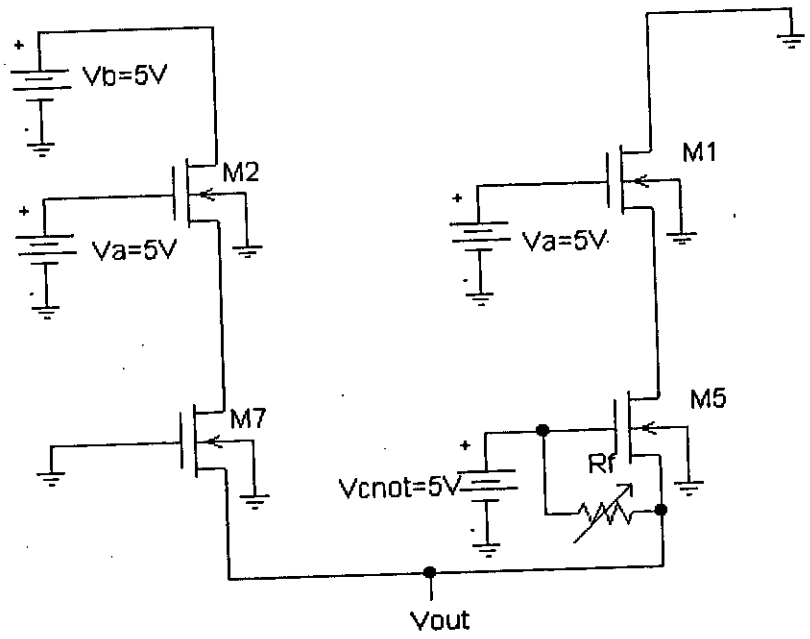


Fig. 4.24 Equivalent circuit of gate to source bridging fault on MOS M_5 of the CPL Full Adder Sum Circuit. Test Vector [A=1, B=1, C=0].

In Figure 4.24, the vector (110) is applied, M_1, M_2, M_5 and M_6 turn ON and a steady state current I_{DDQ} flows through M_1, M_5 and R_f the circuit. In the faulted circuit, the output voltage is

$$V_{out}=\{2R_{on}/(R_f+2R_{on})\}V_{IH}$$

Above equation shows that when fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, Hence, the bridging fault at M_5 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f+2R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 111

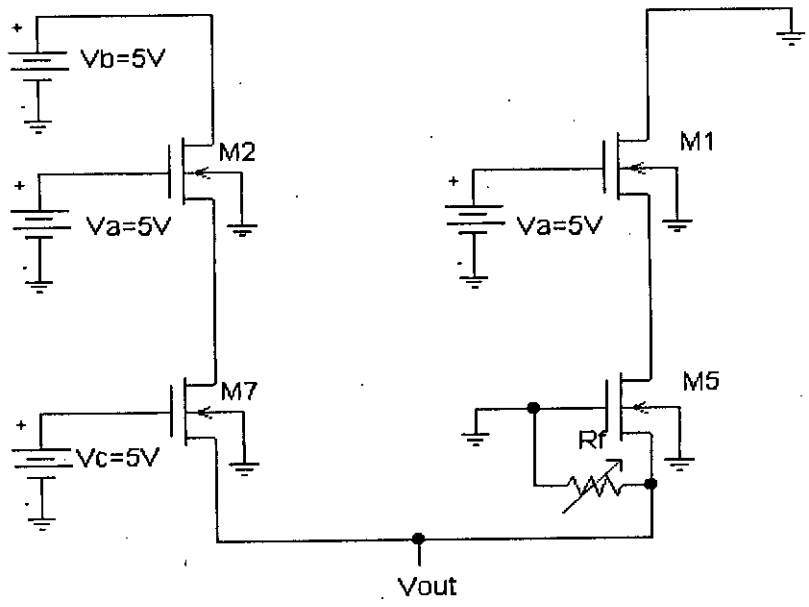


Fig. 4.25 Equivalent circuit of gate to source bridging fault on MOS M_5 of the CPL Full Adder Sum Circuit. Test Vector [A=1, B=1, C=1].

In Figure 4.25, the vector (111) is applied, M_1, M_2, M_7 and M_8 turn ON and a steady state current I_{DDQ} flows through M_2, M_7 and R_f of the circuit. In the faulted circuit, the output voltage is

$$V_{out} = \{R_f/(R_f+2R_{on})\}V_{IH}$$

Above equation shows that when fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, Hence, the bridging fault at M_5 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f + 2R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

M_6 : (Bridging fault in M_6 of the CPL Full Adder Sum gate of figure 4.1)

Qualitative analysis have been performed for gate to source bridging fault on MOS M_6. The fault is modeled with a variable resistance R_f placed between the gate and source terminal of the faulted MOS. The tests vectors (000), (001) (110) and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. When test vectors (010), (011), (100), (101) are applied a large steady state current flows through the circuit. The expression for output voltage and current are similar to the previous case and are not shown here for the sake of conciseness of the thesis. The SPICE simulation results are summarized in the tables at the end of this article.

M_7 : (Bridging fault in M_7 of the CPL Full Adder Sum gate of figure 4.1)

Qualitative analysis have been performed for gate to source bridging fault on MOS M_7. The fault is modeled with a variable resistance R_f placed between the gate and source terminal of the faulted MOS. The tests vectors (000), (001) (110) and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. When test vectors (010), (011), (100), (101) are applied a large steady state current flows through the circuit. The expression for output voltage and current are similar to the previous case. Hence, the analysis for only one test vector is shown below. The SPICE simulation results are summarized in the tables at the end of this article.

Test Vector 010

In Figure 4.26, the vector (010) is applied, M_3, M_4, M_5 and M_6 turn ON and a steady state current I_{DDQ} flows through M_3, M_5 and R_f of the circuit. In the faulted circuit, the output voltage is

$$V_{out}=\{R_f/(R_f+2R_{on})\}V_{IH}$$

Above equation shows that when fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, Hence, the bridging fault at M_7 cannot be detected by logic monitoring. However, the steady state current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$I = V_{IH}/(R_f + 2R_{on})$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

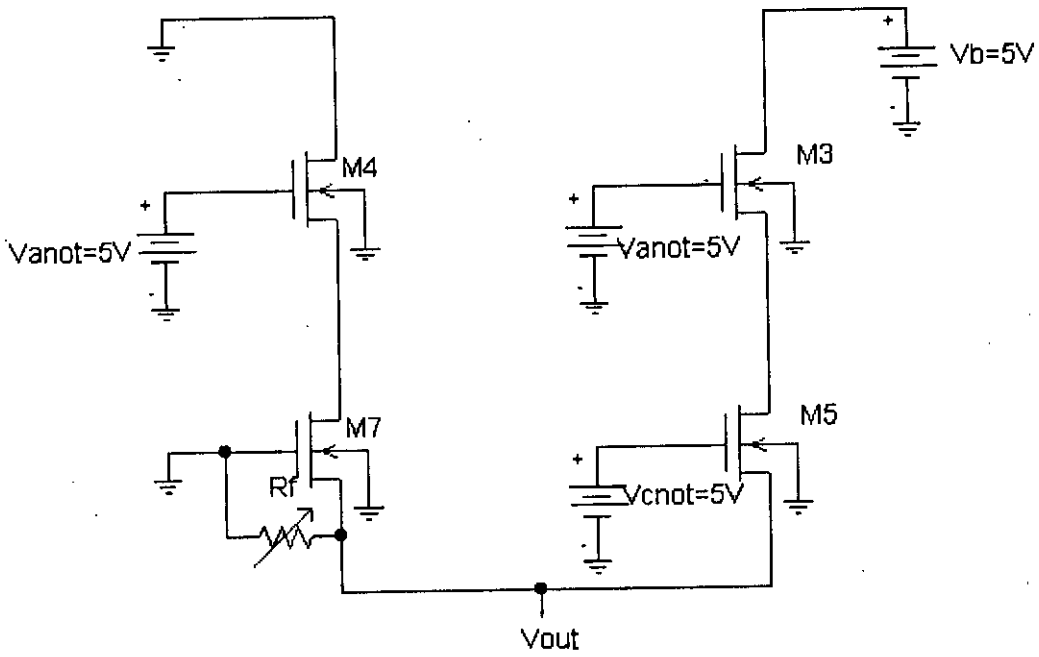


Fig. 4.26 Equivalent circuit of gate to source bridging fault on MOS M_7 of the CPL Full Adder Sum Circuit. Test Vector [A=0, B=1, C=0].

M_8 : (Bridging fault in M_8 of the CPL Full Adder Sum gate of figure 4.1)

Qualitative analysis have been performed for gate to source bridging fault on MOS M_8. The fault is modeled with a variable resistance R_f placed between the gate and source terminal of the faulted MOS. The tests vectors (010), (011) (100) and (101) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. When test vectors (000), (001), (110) and (111) are applied a large steady state current flows through the circuit. The expression for output voltage and current are similar to the previous case and are not shown here for the sake of conciseness of the thesis. The SPICE simulation results are summarized in the tables at the end of this article.

4.3.2 SPICE Simulation Results

This section summarizes the SPICE simulation results for a single bridging fault in the MOS devices of the CPL full adder sum circuit.

Table: 4.3

SPICE Simulation result for bridging fault in CPL Full Adder Sum Ckt.

Effect of fault Strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_1	1	0	5	0	0.002	2.344E-03
	10	0	5	0	0.023	2.318E-03
	100	0	5	0	0.209	2.093E-03
	1K	0	5	0	1.111	1.111E-03
	10K	0	5	0	2.329	2.329E-04
	100K	0	5	0	2.943	2.943E-05
M_1	1	0	5	5	0	2.344E-03
	10	0	5	5	0	2.318E-03
	100	0	5	5	0	2.093E-03
	1K	0	5	5	0	1.111E-03
	10K	0	5	5	0	2.329E-04
	100K	0	5	5	0	2.944E-05
M_1	1	5	5	0	3.262	2.346E-03
	10	5	5	0	3.263	2.345E-03
	100	5	5	0	3.263	2.329E-03
	1K	5	5	0	2.824	2.176E-03
	10K	5	5	0	0.266	4.733E-04
	100K	5	5	0	0.026	4.974E-05
M_1	1	5	5	5	3.262	2.346E-03
	10	5	5	5	3.262	2.345E-03
	100	5	5	5	3.262	2.329E-03
	1K	5	5	5	3.248	2.176E-03
	10K	5	5	5	3.241	4.733E-04
	100K	5	5	5	3.240	4.970E-05
M_2	1	0	0	0	0	2.344E-03
	10	0	0	0	0	2.318E-03
	100	0	0	0	0	2.093E-03
	1K	0	0	0	0	1.111E-03
	10K	0	0	0	0	2.329E-04
	100K	0	0	0	0	2.943E-05

Table: 4.3 (Cont'd)

SPICE Simulation result for bridging fault in CPL Full Adder Sun Ckt.

Effect of fault Strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_2	1	0	0	5	0.002	2.344E-03
	10	0	0	5	0.023	2.318E-03
	100	0	0	5	0.209	2.093E-03
	1K	0	0	5	1.111	1.111E-03
	10K	0	0	5	2.329	2.329E-04
	100K	0	0	5	2.943	2.943E-05
M_2	1	5	0	0	3.257	2.346E-03
	10	5	0	0	3.257	2.345E-03
	100	5	0	0	3.257	2.329E-03
	1K	5	0	0	3.257	2.176E-03
	10K	5	0	0	3.257	4.733E-04
	100K	5	0	0	3.256	4.974E-05
M_2	1	5	0	5	3.264	2.346E-03
	10	5	0	5	3.264	2.345E-03
	100	5	0	5	3.264	2.329E-03
	1K	5	0	5	2.824	2.176E-03
	10K	5	0	5	0.266	4.733E-04
	100K	5	0	5	0.026	4.970E-05
M_3	1	0	0	0	3.267	2.346E-03
	10	0	0	0	3.267	2.345E-03
	100	0	0	0	3.267	2.329E-03
	1K	0	0	0	2.824	2.176E-03
	10K	0	0	0	0.266	4.733E-04
	100K	0	0	0	0.026	4.974E-05
M_3	1	0	0	5	3.267	2.346E-03
	10	0	0	5	3.267	2.345E-03
	100	0	0	5	3.267	2.329E-03
	1K	0	0	5	3.248	2.176E-03
	10K	0	0	5	3.243	4.733E-04
	100K	0	0	5	3.241	4.970E-05

Table: 4.3 (Cont'd)

SPICE Simulation result for bridging fault in CPL Full Adder Sun Ckt.

Effect of fault Strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_3	1	5	0	0	0.002	2.344E-03
	10	5	0	0	0.023	2.318E-03
	100	5	0	0	0.209	2.093E-03
	1K	5	0	0	1.111	1.111E-03
	10K	5	0	0	2.329	2.329E-04
	100K	5	0	0	2.943	2.943E-05
M_3	1	5	0	5	0	2.344E-03
	10	5	0	5	0	2.318E-03
	100	5	0	5	0	2.093E-03
	1K	5	0	5	0	1.111E-03
	10K	5	0	5	0	2.329E-04
	100K	5	0	5	0	2.943E-05
M_4	1	0	5	0	3.255	2.346E-03
	10	0	5	0	3.255	2.345E-03
	100	0	5	0	3.255	2.329E-03
	1K	0	5	0	3.255	2.176E-03
	10K	0	5	0	3.255	4.733E-04
	100K	0	5	0	3.255	4.974E-05
M_4	1	0	5	5	3.263	2.346E-03
	10	0	5	5	3.263	2.345E-03
	100	0	5	5	3.264	2.329E-03
	1K	0	5	5	2.824	2.176E-03
	10K	0	5	5	0.266	4.733E-04
	100K	0	5	5	0.002	4.970E-05
M_4	1	5	5	0	0	2.344E-03
	10	5	5	0	0	2.318E-03
	100	5	5	0	0	2.093E-03
	1K	5	5	0	0	1.111E-03
	10K	5	5	0	0	2.329E-04
	100K	5	5	0	0	2.943E-05

Table: 4.3 (Cont'd)

SPICE Simulation result for bridging fault in CPL Full Adder Sun Ckt.

Effect of fault Strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_4	1	5	5	5	0.002	2.344E-03
	10	5	5	5	0.023	2.318E-03
	100	5	5	5	0.209	2.093E-03
	1K	5	5	5	1.111	1.111E-03
	10K	5	5	5	2.329	2.329E-04
	100K	5	5	5	2.943	2.943E-05
M_5	1	0	0	0	4.999	1.317E-03
	10	0	0	0	4.987	1.317E-03
	100	0	0	0	4.869	1.314E-03
	1K	0	0	0	3.710	1.290E-03
	10K	0	0	0	0.528	4.472E-04
	100K	0	0	0	0.005	4.948E-05
M_5	1	0	0	5	0	1.316E-03
	10	0	0	5	0.001	1.307E-03
	100	0	0	5	0.122	1.224E-03
	1K	0	0	5	0.781	7.814E-04
	10K	0	0	5	2.032	2.032E-04
	100K	0	0	5	2.816	2.816E-05
M_5	1	5	5	0	4.999	1.317E-03
	10	5	5	0	4.987	1.317E-03
	100	5	5	0	4.869	1.314E-03
	1K	5	5	0	3.710	1.290E-03
	10K	5	5	0	0.528	4.472E-04
	100K	5	5	0	0.005	4.948E-05
M_5	1	5	5	5	0.001	1.316E-03
	10	5	5	5	0.001	1.307E-03
	100	5	5	5	0.122	1.224E-03
	1K	5	5	5	0.781	7.814E-04
	10K	5	5	5	2.032	2.032E-04
	100K	5	5	5	2.816	2.816E-05

Table: 4.3 (Cont'd)
SPICE Simulation result for bridging fault in CPL Full Adder Sum Ckt.
Effect of fault Strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_6	1	0	5	0	4.999	1.317E-03
	10	0	5	0	4.987	1.317E-03
	100	0	5	0	4.869	1.314E-03
	1K	0	5	0	3.710	1.290E-03
	10K	0	5	0	0.528	4.472E-04
	100K	0	5	0	0.005	4.948E-05
M_6	1	0	5	5	0.001	1.316E-03
	10	0	5	5	0.001	1.307E-03
	100	0	5	5	0.122	1.224E-03
	1K	0	5	5	0.781	7.814E-04
	10K	0	5	5	2.032	2.032E-04
	100K	0	5	5	2.816	2.816E-05
M_6	1	5	0	0	4.999	1.317E-03
	10	5	0	0	4.987	1.317E-03
	100	5	0	0	4.869	1.314E-03
	1K	5	0	0	3.710	1.290E-03
	10K	5	0	0	0.528	4.472E-04
	100K	5	0	0	0.005	4.948E-05
M_6	1	5	0	5	0.001	1.316E-03
	10	5	0	5	0.001	1.307E-03
	100	5	0	5	0.122	1.224E-03
	1K	5	0	5	0.781	7.814E-04
	10K	5	0	5	2.032	2.032E-04
	100K	5	0	5	2.816	2.816E-05
M_7	1	0	5	0	0	1.316E-03
	10	0	5	0	0.001	1.307E-03
	100	0	5	0	0.122	1.224E-03
	1K	0	5	0	0.781	7.814E-04
	10K	0	5	0	2.032	2.032E-04
	100K	0	5	0	2.798	3.042E-05
M_7	1	0	5	5	4.999	1.317E-03
	10	0	5	5	4.987	1.316E-03
	100	0	5	5	4.869	1.314E-03
	1K	0	5	5	3.710	1.290E-03
	10K	0	5	5	0.528	4.471E-04
	100K	0	5	5	0.005	5.366E-05

Table: 4.3 (Cont'd)
SPICE Simulation result for bridging fault in CPL Full Adder Sum Ckt.
Effect of fault Strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_7	1	5	0	0	0.001	1.316E-03
	10	5	0	0	0.001	1.307E-03
	100	5	0	0	0.122	1.224E-03
	1K	5	0	0	0.781	7.814E-04
	10K	5	0	0	2.032	2.032E-04
	100K	5	0	0	2.798	3.042E-05
M_7	1	5	0	5	4.999	1.317E-03
	10	5	0	5	4.987	1.317E-03
	100	5	0	5	4.869	1.314E-03
	1K	5	0	5	3.710	1.290E-03
	10K	5	0	5	0.528	4.471E-04
	100K	5	0	5	0.005	5.366E-05
M_8	1	0	0	0	0.005	1.316E-03
	10	0	0	0	0.001	1.307E-03
	100	0	0	0	0.001	1.224E-03
	1K	0	0	0	0.122	7.814E-04
	10K	0	0	0	0.781	2.032E-04
	100K	0	0	0	2.032	2.816E-05
M_8	1	0	0	5	2.816	1.317E-03
	10	0	0	5	4.999	1.314E-03
	100	0	0	5	4.987	1.290E-03
	1K	0	0	5	4.869	4.472E-04
	10K	0	0	5	3.710	4.948E-05
	100K	0	0	5	0.528	4.948E-05
M_8	1	5	5	0	0.005	1.316E-03
	10	5	5	0	0.005	1.307E-03
	100	5	5	0	0.001	1.224E-03
	1K	5	5	0	0.001	7.814E-04
	10K	5	5	0	0.122	2.032E-04
	100K	5	5	0	0.781	2.816E-05
M_8	1	5	5	5	2.816	1.317E-03
	10	5	5	5	4.999	1.314E-03
	100	5	5	5	4.987	1.290E-03
	1K	5	5	5	4.869	4.472E-04
	10K	5	5	5	3.710	4.948E-05
	100K	5	5	5	0.528	4.948E-05

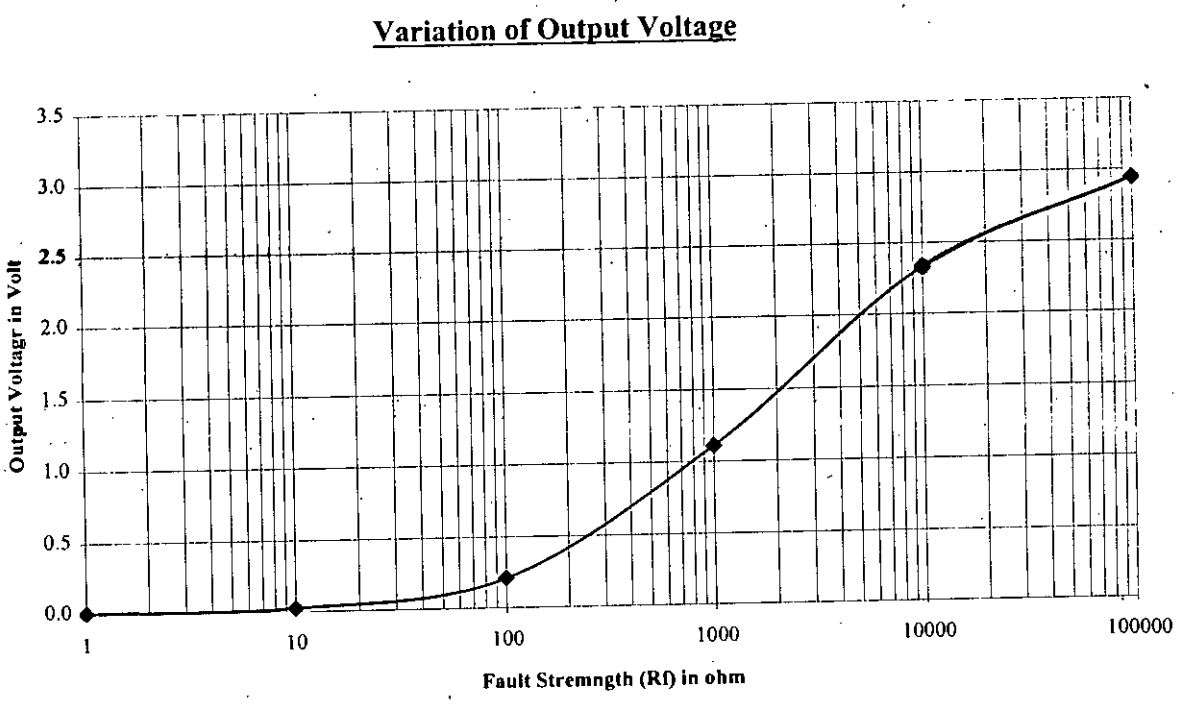


Fig 4.27: Output voltage vs Fault Strength
(Bridging fault of M_1 (010), M_2 (001), M_3 (100) and M_4 (111))

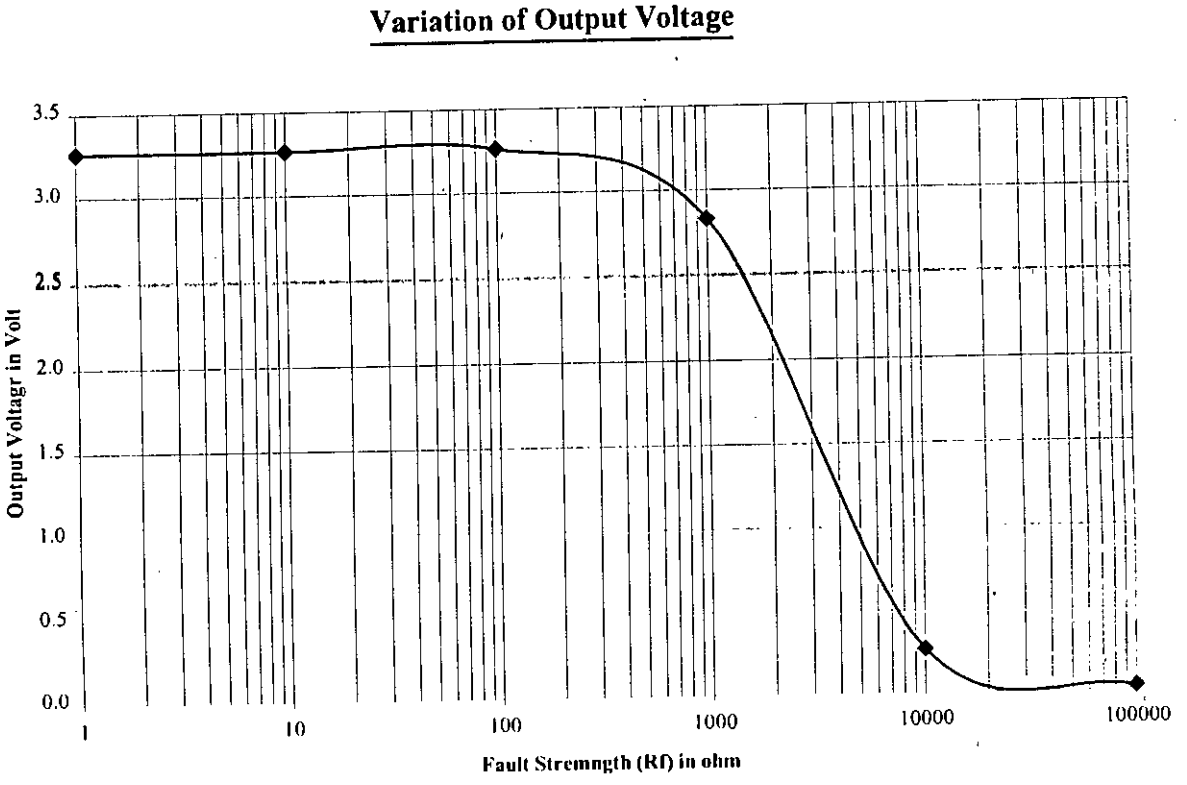


Fig 4.28:Output Voltage vs Fault Strength
(Bridging fault of M_1 (110), M_2 (101), M_3 (000) and M_4 (011))

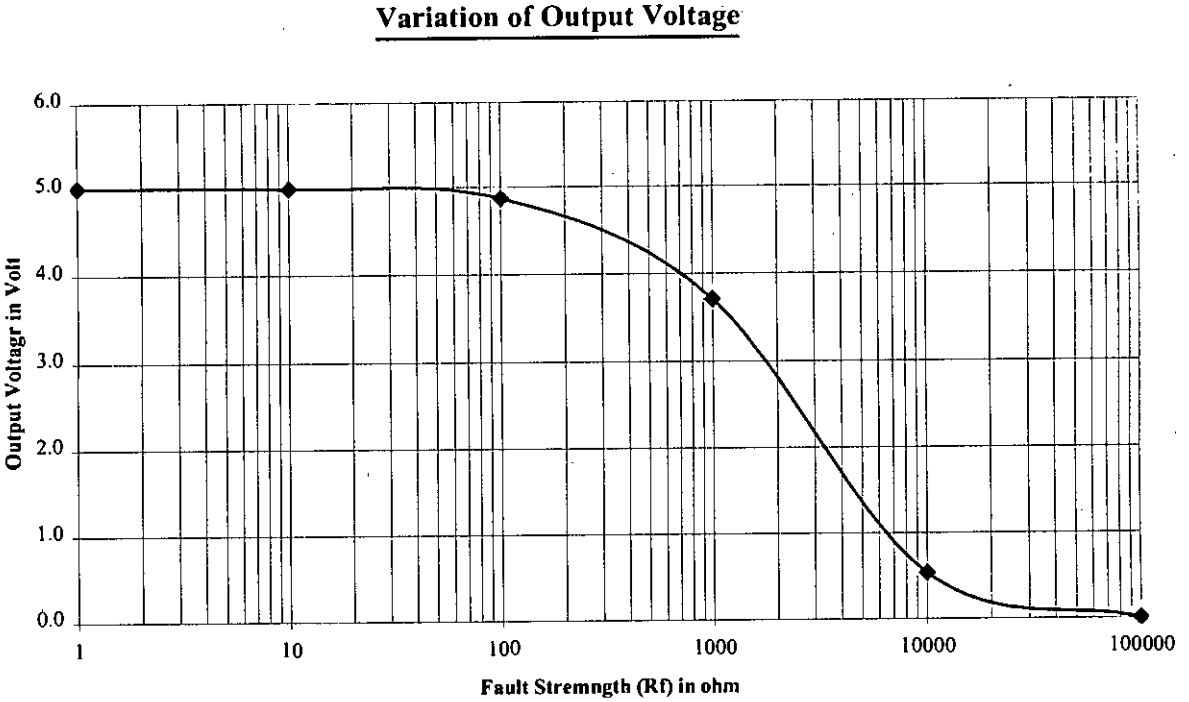


Fig 4.29: Output Voltage vs Fault Strength
Bridging fault of M_5 (000)(110), M_6 (010)(100), M_7 (011)(101) and M_8 (001)(111)

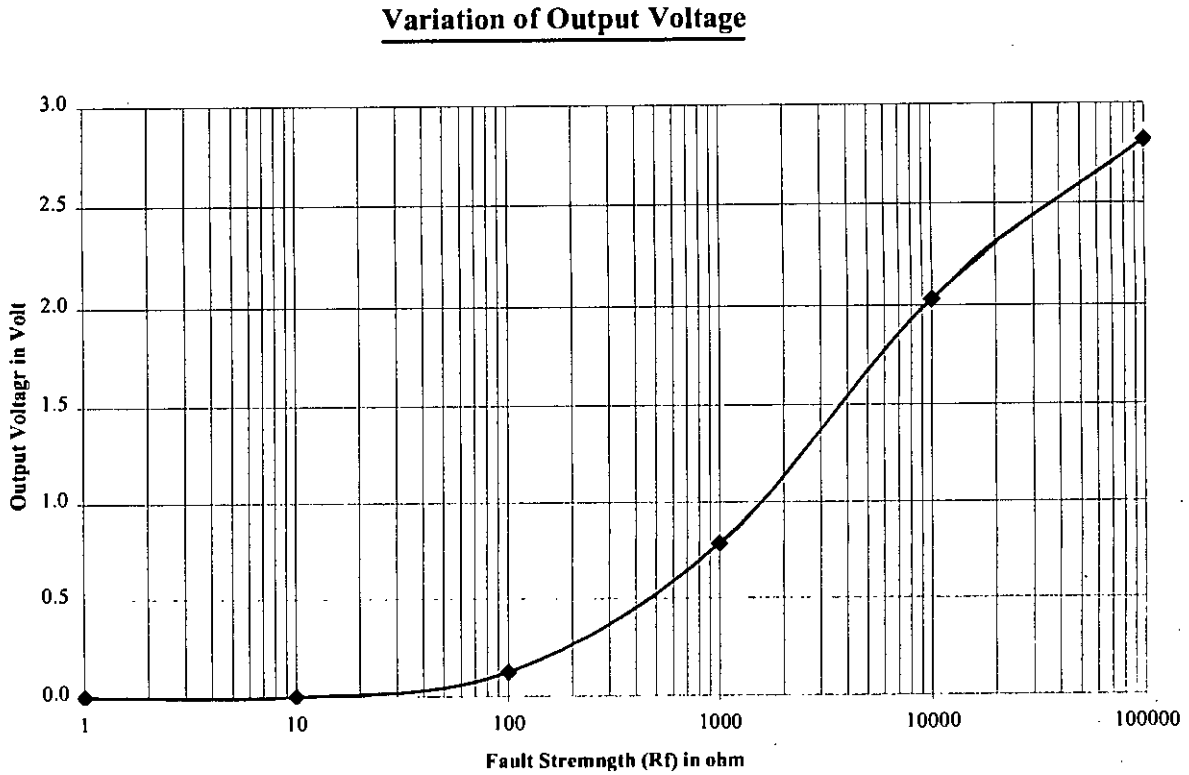


Fig 4.30: Output Voltage vs Fault Strength
Bridging fault of M_5 (001)(111), M_6 (011)(101), M_7 (010)(100) and M_8 (000)(110)

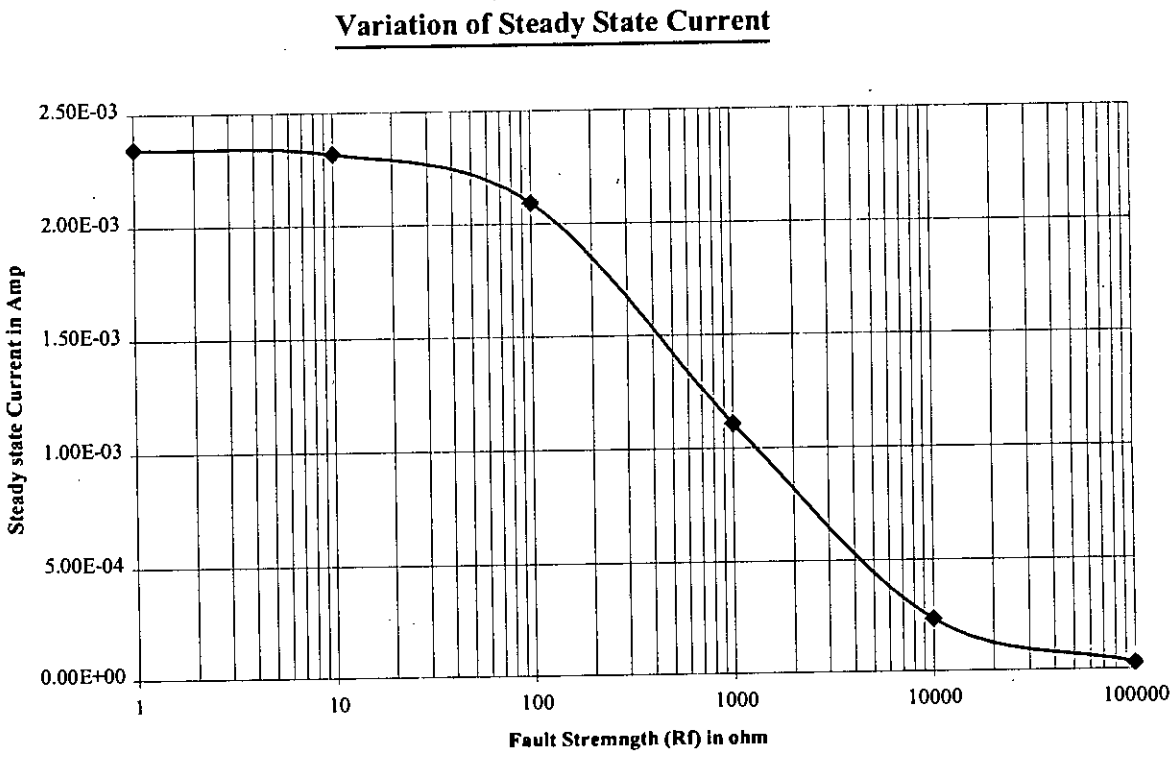


Fig 4.31: Steady State Current vs Fault Strength (Bridging fault of M_1 (010), M_2 (001), M_3 (100) and M_4 (111))

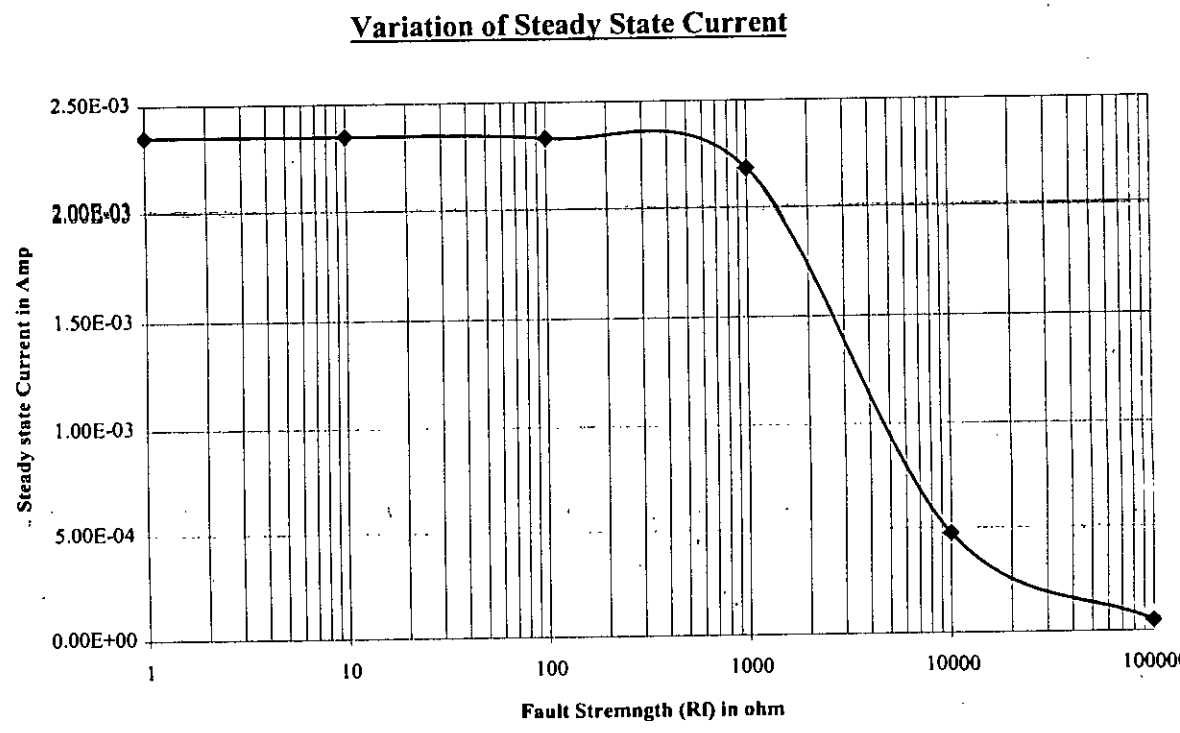


Fig 4.32: Steady State Current vs Fault Strength (Bridging fault of M_1 (110), M_2 (101), M_3 (000) and M_4 (011))

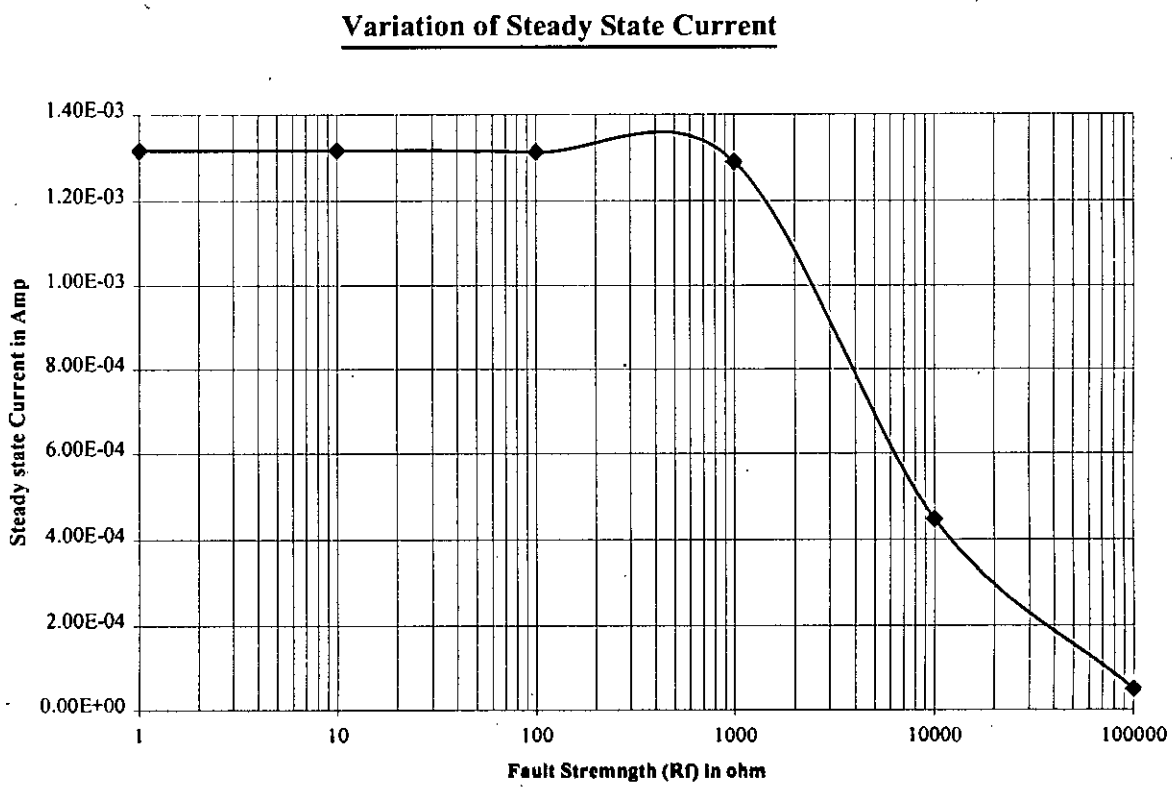


Fig 4.33: Steady State Current vs Fault Strength
Bridging fault of M_5 (000)(110), M_6 (010)(100), M_7 (011)(101) and M_8(001)(111)

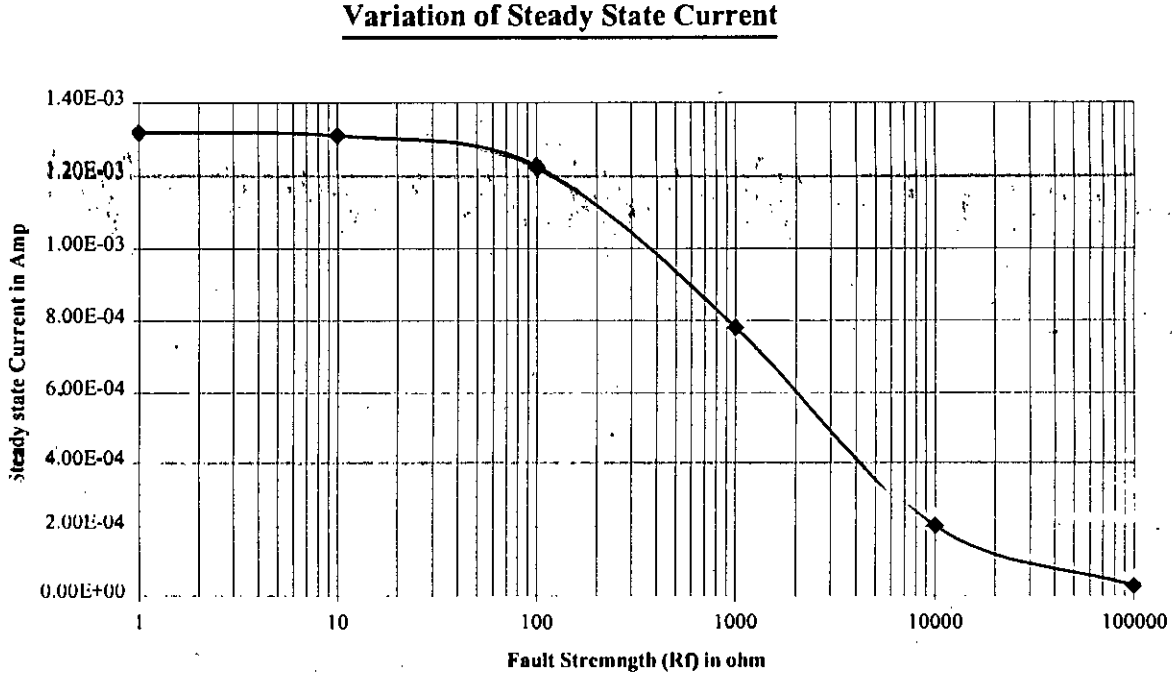


Fig 4.34: Steady State Current vs Fault Strength
Bridging fault of M_5 (001)(111), M_6 (010)(100), M_7 (010)(100) and M_8 (000)(110)

Effects of Fault Resistance

From the results of Table 4.3, Fig 4.27 to 4.30 show, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 1 Ω to 100 kΩ, the output voltage varies from 0 to 4.999 Volt. This appreciable variation in output voltage clearly shows that the output logic level is indeterminable. This agrees with our prediction that the fault cannot be detected by logic monitoring. As seen from the table and fig 4.31 to 4.34, steady state current is in the range of miliampere compared to normal operating current of 2.968E-11 A. Therefore, the fault can be detected by current monitoring.

Table: 4.4

The following table shows the summary of bridging fault in CPL Full Adder Sum circuit.

Summary for bridging faults in CPL Full Adder Sum Ckt.

Fault	Successful Test Vector	Output Logic Level (Volt)	I_{DDQ} (amp)	Logic monitoring possible?	Current monitoring possible?
M_1	(010),(011), (110), (111)	0 to 3.262	2.346E-03 to 2.943E-05	No	Yes
M_2	(000),(001), (100), (101)	0 to 3.264	2.346E-03 to 2.943E-05	No	Yes
M_3	(000),(001), (100), (101)	0 to 3.267	2.346E-03 to 2.943E-05	No	Yes
M_4	(010),(011), (110), (111)	0 to 3.264	2.346E-03 to 2.943E-05	No	Yes
M_5	(000),(001), (110), (111)	0 to 4.999	1.317E-03 to 2.816E-05	No	Yes
M_6	(010),(011), (100), (101)	0 to 4.999	1.317E-03 to 2.816E-05	No	Yes
M_7	(010),(011), (100), (101)	0 to 4.999	1.317E-03 to 3.042E-05	No	Yes
M_8	(000),(001), (110), (111)	0 to 4.999	1.317E-03 to 3.042E-05	No	Yes

4.4 Behavior Under Single Stuck open faults

Physical defect may cause a MOS to become permanently open insensitive to its input signal. The behavior of CPL full adder sum circuits under single stuck open faults in MOS transistors are analyzed in this section.

4.4.1 Qualitative Analysis

M_1 : (stuck open fault in M_1 of the CPL Full Adder Sum gate of fig 4.1)

To model a stuck open fault a large resistor is inserted between the MOS terminal and the circuit node to which the terminal would otherwise be connected. Detection of the stuck open fault can be achieved by utilizing two pattern test, the first vector to be applied is called initilization vector and the second vector is called test vector. It is observed that when the vector (100) and (110) are applied - M_3, M_4, M_7, M_8 turns off and M_1 remains off since it is stuck-open. Since M_3, M_4, M_7, M_8 and M_1 MOS are off when (100) and (110) are applied thus a non-conducting stage is produced in the full adder SUM circuit. Hence, the (100) and (110) vectors can be taken as a Test Vector for M_1 fault.

Test Vector (100):

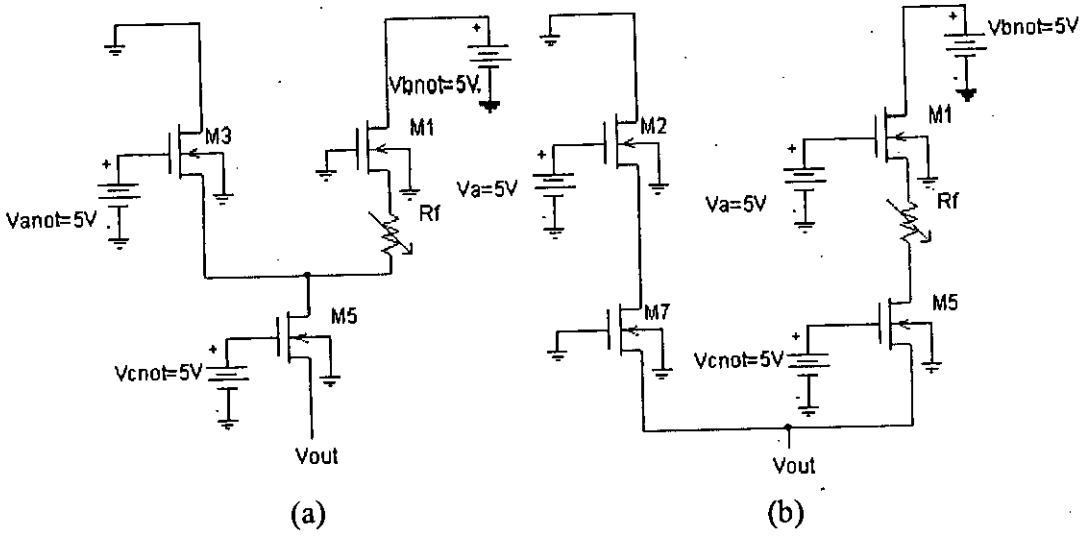


Fig. 4.35 Equivalent circuit for stuck-open fault in MOS M_1 of CPL Full Adder Sum Circuit with (a) Initialization Vector [000] and (b) Test vector [100].

In the unfaulted circuit, the (100) vector would produce a high output. Consequently, the vectors that produced a low output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vectors (000), (011), (101) and (110) produce low outputs under both the above conditions and therefore can be considered as Initialization Vectors. Applying any one of the Initialization Vectors first and then the Test Vector can detect the fault. Each of these cases is analyzed below.

i. **Initialization Vector (000), Test Vector (100):**

When a capacitor is connected to the output terminal of the faulted gate of fig 4.35 and the vector (000) is applied, the output voltage is at 0 Volt. The Test Vector (100) is applied next, thus causing the output capacitance to be isolated from the faulty circuit. Ideally the output capacitance retains its original state of 0 V at the faulty circuit. But practically, a current flows from the 5V power source V_{IH} through M_1 and the resistance R_f to charge the output capacitance to 5V. Also M_7 supplies a leakage current that charges Cout. These charging currents are very small since the large resistance R_f limits one and the other is only a leakage current. As a result, the time to charge the capacitance to 5V is longer than the time that would be required in an unfaulted gate. This delay in charging the output capacitance to 5 V is the fundamental criterion for fault detection. In all the cases in our analysis test vector is applied to the faulted circuit 10 ns after the application of the initialization vector and output is monitored after a time delay of 100 ns. In this case the fault free circuit shows high and the faulty circuit shows low. Hence, the error can be detected by logic monitoring.

ii. **Initialization Vector (011), Test Vector (100):**

The operation of this two pattern testis similar to i.

iii. **Initialization Vector (101), Test Vector (100):**

The operation of this two pattern testis similar to i.

iv. **Initialization Vector (110), Test Vector (100):**

The operation of this two pattern testis similar to i.

Test Vector (110):

In the unfaulted circuit, the (110) vector would produce a low output. Consequently, the vectors that produced a high output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vector (001) produce high outputs under both the above conditions and herefore can be considered as Initialization Vectors. Applying the Initialization Vectors first and then the Test Vector can detect the fault. This case is analyzed below.

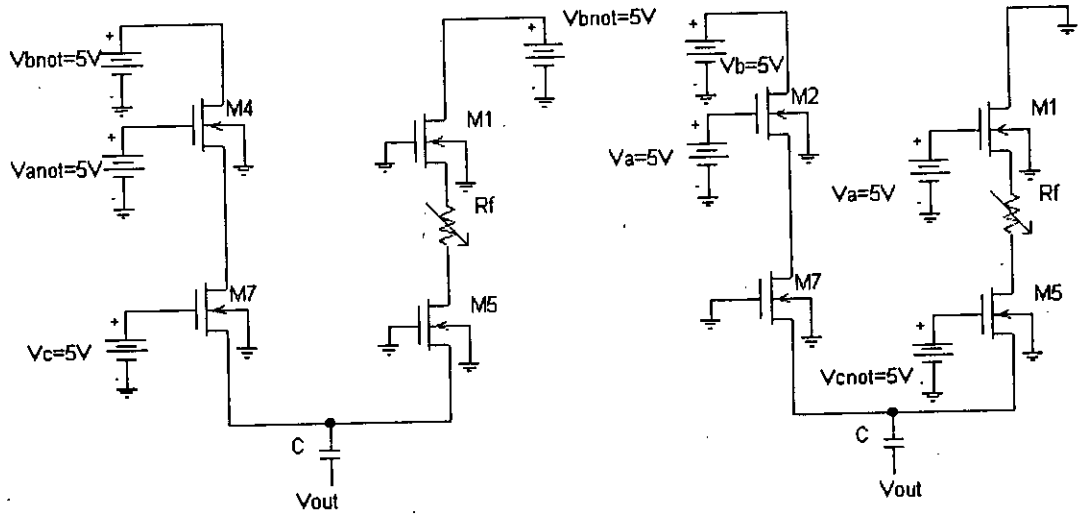


Fig. 4. 36 Equivalent circuit for stuck-open fault in MOS M_1 of CPL Full Adder Sum Circuit with (a) Initialization Vector [001] and (b) Test vector [110].

i. Initialization Vector (001), Test Vector (110):

When a capacitor is connected to the output terminal of the faulted gate of fig 4.36 and the vector (001) is applied, the output voltage is at 5 Volt. The Test Vector (110) is applied next, thus causing the output capacitance to be isolated from the circuit. Ideally the output capacitance retains its original state of 5 V. But practically, a discharge path exists for the output capacitance through the resistance R_f and M_1. The discharging time is very large due to the large resistance R_f. As a result, the time to discharge the capacitance to 0 V is longer than the time that would be required in an unfaulted circuit. This delay in discharging the output capacitance to 0 V is the fundamental criterion for faulted detection.

uck open fault in M_2 to M_8 of the CPL Full Adder Sum gate of figure 4.1

In a similar way stuck-open fault on MOS transistor M_2 to M_8 of the basic CPL adder SUM circuit have been qualitatively analyzed and simulated by SPICE. The successful two pattern test vectors which can detect the faults are summarized in the table.

4.4.2 SPICE Simulation Results

This section summarizes the SPICE simulation results for a single stuck open fault in the MOS devices of the CPL full adder Sum circuit.

Table: 4.5

SPICE Simulation result for stuck open fault in CPL Full Adder Sum Ckt.

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_1	50 M	1	000	100	0	2.971E-11
		10	000	100	4.811E-12	2.971E-11
		100	000	100	0.0889	6.336E-08
	100 M	1	000	100	0	2.968E-11
		10	000	100	4.811E-12	2.968E-11
		100	000	100	0.0454	3.306E-08
	200 M	1	000	100	0	2.968E-11
		10	000	100	4.811E-12	2.968E-11
		100	000	100	0.1212	1.691E-08
M_1	50 M	1	001	110	6.237	2.971E-11
		10	001	110	3.267	2.971E-11
		100	001	110	2.621	5.242E-08
	100 M	1	001	110	3.267	2.968E-11
		10	001	110	3.267	2.968E-11
		100	001	110	2.764	2.764E-08
	200 M	1	001	110	3.267	2.968E-11
		10	001	110	3.267	2.968E-11
		100	001	110	2.856	1.428E-08
M_1	50 M	1	011	100	4.987E-07	2.183E-11
		10	011	100	1.558	2.966E-13
		100	011	100	1.409	2.818E-08
	100 M	1	011	100	4.987E-07	2.183E-11
		10	011	100	1.558	2.966E-13
		100	011	100	1.482	1.482E-08
	200 M	1	011	100	4.987E-07	2.183E-11
		10	011	100	1.558	2.966E-13
		100	011	100	1.554	7.770E-09

Table: 4.5
SPICE Simulation result for stuck open fault in CPL Full Adder Sum Ckt.

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_1	50 M	1	101	100	0	2.971E-11
		10	101	100	1.450E-11	2.971E-11
		100	101	100	0.6935	5.135E-08
	100 M	1	101	100	0	2.967E-11
		10	101	100	1.450E-11	2.967E-11
		100	101	100	0.5707	2.688E-08
	200 M	1	101	100	0	2.966E-11
		10	101	100	4.427E-12	2.966E-11
		100	101	100	0.5075	1.383-08
M_1	50 M	1	110	100	7.983E-11	1.072E-11
		10	110	100	2.277E-10	3.227E-15
		100	110	100	1.225E-11	9.479E-15
	100 M	1	110	100	3.992E-11	2.139E-15
		10	110	100	1.139E-10	2.139E-15
		100	110	100	6.124e-12	4.367E-15
	200 M	1	110	100	1.996E-11	1.071E-11
		10	110	100	5.695E-11	4.613E-15
		100	110	100	3.063E-12	2.214E-15
M_2	50 M	1	111	101	3.266	0
		10	111	101	3.266	6.150E-14
		100	111	101	2.938	3.828E-10
	100 M	1	111	101	3.265	0
		10	111	101	3.265	6.150E-14
		100	111	101	3.097	3.828E-10
	200 M	1	111	101	3.263	0
		10	111	101	3.263	6.150E-14
		100	111	101	3.178	3.828E-10
M_2	50 M	1	110	111	0	0
		10	110	111	1.450E-11	1.857E-14
		100	110	111	0.6937	4.194E-15
	100 M	1	110	111	0	0
		10	110	111	1.450E-11	1.857E-14
		100	110	111	0.5707	4.767E-15
	200 M	1	110	111	0	0
		10	110	111	1.450E-11	1.857E-14
		100	110	111	0.5075	2.613E-15

Table: 4.5
SPICE Simulation result for stuck open fault in CPL Full Adder Sum Ckt.

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_2	50 M	1	010	101	3.267	0
		10	010	101	3.267	9.900E-14
		100	010	101	2.621	3.742E-10
	100 M	1	010	101	3.267	0
		10	010	101	3.267	9.900E-14
		100	010	101	2.764	3.741E-10
	200 M	1	010	101	3.267	0
		10	010	101	3.267	9.900E-14
		100	010	101	2.856	3.679E-10
M_2	50 M	1	101	111	0	2.971E-11
		10	101	111	6.284E-13	2.971E-11
		100	101	111	0.2707	2.438E-14
	100 M	1	101	111	0	2.968E-11
		10	101	111	3.143E-13	2.968E-11
		100	101	111	0.1363	2.482E-15
	200 M	1	101	111	0	2.968E-11
		10	101	111	1.572E-13	2.968E-11
		100	101	111	0.0683	4.090E-14
M_2	50 M	1	001	101	3.267	2.971E-11
		10	001	101	3.267	2.971E-11
		100	001	101	2.937	3.832E-10
	100 M	1	001	101	3.267	2.968E-11
		10	001	101	3.267	2.968E-11
		100	001	101	3.097	3.849E-10
	200 M	1	001	101	3.267	2.968E-11
		10	001	101	3.267	2.968E-11
		100	001	101	3.181	3.852E-10
M_3	50 M	1	110	000	0	0
		10	110	000	4.811E-12	1.893E-14
		100	110	000	8.893E-02	9.618E-15
	100 M	1	110	000	0	0
		10	110	000	4.811E-12	1.893E-14
		100	110	000	4.549E-02	3.228E-14
	200 M	1	110	000	0	0
		10	110	000	4.811E-12	1.893E-14
		100	110	000	1.212E-01	3.395E-14

Table: 4.5
SPICE Simulation result for stuck open fault in CPL Full Adder Sum Ckt.

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_3	50 M	1	111	000	3.267	0
		10	111	000	3.267	9.900E-14
		100	111	000	2.621	3.742E-10
	100 M	1	111	000	3.267	0
		10	111	000	3.267	9.900E-14
		100	111	000	2.764	3.741E-10
	200 M	1	111	000	3.267	0
		10	111	000	3.267	9.900E-14
		100	111	000	2.856	3.679E-10
M_3	50 M	1	000	010	0	2.971E-11
		10	000	010	6.284E-13	2.971E-11
		100	000	010	0.2706	2.438E-14
	100 M	1	000	010	0	2.968E-11
		10	000	010	3.143E-13	2.968E-11
		100	000	010	0.1636	2.438E-14
	200 M	1	000	010	0	2.968E-11
		10	000	010	1.572E-13	2.968E-11
		100	000	010	0.06833	4.090E-14
M_3	50 M	1	001	000	3.267	2.971E-11
		10	001	000	3.267	2.971E-11
		100	001	000	2.210	3.739E-10
	100 M	1	001	000	3.267	2.968E-11
		10	001	000	3.267	2.968E-11
		100	001	000	2.329	3.673E-10
	200 M	1	001	000	3.267	2.968E-11
		10	001	000	3.267	2.968E-11
		100	001	000	2.410	3.533E-10
M_3	50 M	1	010	000	3.267	0
		10	010	000	3.267	6.150E-14
		100	010	000	2.938	3.828E-10
	100 M	1	010	000	3.265	0
		10	010	000	3.265	6.150E-14
		100	010	000	3.097	3.828E-10
	200 M	1	010	000	3.263	0
		10	010	000	3.263	6.150E-14
		100	010	000	3.178	3.828E-10

Table: 4.5
SPICE Simulation result for stuck open fault in CPL Full Adder Sum Ckt.

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_3	50 M	1	011	000	0	0
		10	011	000	1.450E-11	1.857E-14
		100	011	000	0.6935	2.612E-15
	100 M	1	011	000	0	0
		10	011	000	1.450E-11	1.857E-14
		100	011	000	0.5707	4.767E-15
	200 M	1	011	000	0	0
		10	011	000	1.450E-11	1.857E-14
		100	011	000	0.5075	1.625E-14
M_3	50 M	1	100	000	3.267	2.971E-11
		10	100	000	3.267	2.971E-11
		100	100	000	2.937	3.832E-10
	100 M	1	100	000	3.267	2.968E-11
		10	100	000	3.267	2.968E-11
		100	100	000	3.097	3.849E-10
	200 M	1	100	000	3.267	2.968E-11
		10	100	000	3.267	2.968E-11
		100	100	000	3.181	3.852E-10
M_4	50 M	1	111	011	3.267	0
		10	111	011	3.267	1.893E-14
		100	111	011	2.937	5.874E-08
	100 M	1	111	011	3.267	0
		10	111	011	3.267	1.893E-14
		100	111	011	3.097	3.097E-08
	200 M	1	111	011	3.267	0
		10	111	011	3.267	1.893E-14
		100	111	011	3.181	1.590E-08
M_4	50 M	1	000	001	0	2.971E-11
		10	000	001	0	2.971E-11
		100	000	001	6.935E-01	5.135E-08
	100 M	1	000	001	0	2.967E-11
		10	000	001	1.450E-11	2.967E-11
		100	000	001	0.5707	2.688E-08
	200 M	1	000	001	0	2.966E-11
		10	000	001	1.450E-11	2.966E-11
		100	000	001	0.5075	1.383E-08

Table: 4.5
SPICE Simulation result for stuck open fault in CPL Full Adder Sum Ckt.

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_4	50 M	1	101	001	0	2.971E-11
		10	101	001	4.811E-12	2.971E-11
		100	101	001	0.08893	6.340E-08
	100 M	1	101	001	0	2.968E-11
		10	101	001	4.811E-12	2.968E-11
		100	101	001	0.04630	3.306E-08
	200 M	1	101	001	0	2.968E-11
		10	101	001	4.811E-12	2.968E-11
		100	101	001	0.1212	1.691E-08
M_4	50 M	1	001	011	3.266	2.971E-11
		10	001	011	3.266	2.971E-11
		100	001	011	2.938	5.876E-08
	100 M	1	001	011	3.265	2.967E-11
		10	001	011	3.265	2.967E-11
		100	001	011	3.097	3.096E-08
	200 M	1	001	011	3.263	2.966E-11
		10	001	011	3.263	2.966E-11
		100	001	011	3.178	1.589E-08
M_4	50 M	1	011	001	0	0
		10	011	001	6.284E-13	3.132E-14
		100	011	001	0.2706	5.976E-08
	100 M	1	011	001	0	0
		10	011	001	3.143E-13	3.131E-14
		100	011	001	0.1363	3.122E-08
	200 M	1	011	001	0	0
		10	011	001	1.572E-13	3.130E-14
		100	011	001	6.833E-02	1.595E-08
M_4	50 M	1	100	011	3.267	2.971E-11
		10	100	011	3.267	2.971E-11
		100	100	011	2.621	5.242E-08
	100 M	1	100	011	3.267	2.968E-11
		10	100	011	3.267	2.968E-11
		100	100	011	2.764	2.764E-08
	200 M	1	100	011	3.267	2.968E-11
		10	100	011	3.267	2.968E-11
		100	100	011	2.856	1.428E-08

Table: 4.5
SPICE Simulation result for stuck open fault in CPL Full Adder Sum Ckt.

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_5	50 M	1	110	010	0	2.971E-11
		10	110	010	4.811E-12	2.971E-11
		100	110	010	0.08893	6.340E-08
	100 M	1	110	010	0	2.968E-11
		10	110	010	4.811E-12	2.968E-11
		100	110	010	0.04630	3.306E-08
	200 M	1	110	010	0	2.968E-11
		10	110	010	4.811E-12	2.968E-11
		100	110	010	0.1212	1.691E-08
M_5	50 M	1	001	000	3.267	2.971E-11
		10	001	000	3.267	2.971E-11
		100	001	000	2.621	5.242E-08
	100 M	1	001	000	3.267	2.968E-11
		10	001	000	3.267	2.968E-11
		100	001	000	2.764	2.764E-08
	200 M	1	001	000	3.267	2.968E-11
		10	001	000	3.267	2.968E-11
		100	001	000	2.856	1.428E-08
M_5	50 M	1	111	000	3.267	2.971E-11
		10	111	000	3.267	2.971E-11
		100	111	000	2.621	5.242E-08
	100 M	1	111	000	3.267	2.968E-11
		10	111	000	3.267	2.968E-11
		100	111	000	2.764	2.764E-08
	200 M	1	111	000	3.267	2.968E-11
		10	111	000	3.267	2.968E-11
		100	111	000	2.856	1.428E-08
M_5	50 M	1	000	010	0	2.971E-11
		10	000	010	4.811E-12	2.971E-11
		100	000	010	0.08893	6.340E-08
	100 M	1	000	010	0	2.968E-11
		10	000	010	4.811E-12	2.968E-11
		100	000	010	0.04630	3.306E-08
	200 M	1	000	010	0	2.968E-11
		10	000	010	4.811E-12	2.968E-11
		100	000	010	0.1212	1.691E-08

Table: 4.5
SPICE Simulation result for stuck open fault in CPL Full Adder Sum Ckt.

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_6	50 M	1	111	110	0	2.971E-11
		10	111	110	4.811E-12	2.971E-11
		100	111	110	0.08893	6.340E-08
	100 M	1	111	110	0	2.968E-11
		10	111	110	4.811E-12	2.968E-11
		100	111	110	0.04630	3.306E-08
	200 M	1	111	110	0	2.968E-11
		10	111	110	4.811E-12	2.968E-11
		100	111	110	0.1212	2.971E-11
M_6	50 M	1	011	100	3.267	2.971E-11
		10	011	100	3.267	2.971E-11
		100	011	100	2.621	5.242E-08
	100 M	1	011	100	3.267	2.968E-11
		10	011	100	3.267	2.968E-11
		100	011	100	2.764	2.764E-08
	200 M	1	011	100	3.267	2.968E-11
		10	011	100	3.267	2.968E-11
		100	011	100	2.856	1.428E-08
M_6	50 M	1	101	100	3.267	2.971E-11
		10	101	100	3.267	2.971E-11
		100	101	100	2.621	5.242E-08
	100 M	1	101	100	3.267	2.968E-11
		10	101	100	3.267	2.968E-11
		100	101	100	2.764	2.764E-08
	200 M	1	101	100	3.267	2.968E-11
		10	101	100	3.267	2.968E-11
		100	101	100	2.856	1.428E-08
M_6	50 M	1	001	110	0	2.971E-11
		10	001	110	4.811E-12	2.971E-11
		100	001	110	0.08893	6.340E-08
	100 M	1	001	110	0	2.968E-11
		10	001	110	4.811E-12	2.968E-11
		100	001	110	0.04630	3.306E-08
	200 M	1	001	110	0	2.968E-11
		10	001	110	4.811E-12	2.968E-11
		100	001	110	0.1212	1.691E-08

Table: 4.5

SPICE Simulation result for stuck open fault in CPL Full Adder Sum Ckt.

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_7	50 M	1	100	011	3.267	2.971E-11
		10	100	011	3.267	2.971E-11
		100	100	011	2.621	5.242E-08
	100 M	1	100	011	3.267	2.968E-11
		10	100	011	3.267	2.968E-11
		100	100	011	2.764	2.764E-08
	200 M	1	100	011	3.267	2.968E-11
		10	100	011	3.267	2.968E-11
		100	100	011	2.856	1.428E-08
M_7	50 M	1	000	001	0	2.971E-11
		10	000	001	0	2.971E-11
		100	000	001	0.08893	6.340E-08
	100 M	1	000	001	0	2.968E-11
		10	000	001	0	2.968E-11
		100	000	001	0.04630	3.306E-08
	200 M	1	000	001	0	2.968E-11
		10	000	001	0	2.968E-11
		100	000	001	0.1212	2.971E-11
M_7	50 M	1	110	001	0	2.971E-11
		10	110	001	0	2.971E-11
		100	110	001	0.08893	6.340E-08
	100 M	1	110	001	0	2.968E-11
		10	110	001	0	2.968E-11
		100	110	001	0.04630	3.306E-08
	200 M	1	110	001	0	2.968E-11
		10	110	001	0	2.968E-11
		100	110	001	0.1212	2.971E-11
M_7	50 M	1	010	011	3.267	2.971E-11
		10	010	011	3.267	2.971E-11
		100	010	011	2.621	5.242E-08
	100 M	1	010	011	3.267	2.968E-11
		10	010	011	3.267	2.968E-11
		100	010	011	2.764	2.764E-08
	200 M	1	010	011	3.267	2.968E-11
		10	010	011	3.267	2.968E-11
		100	010	011	2.856	1.428E-08

Table: 4.5
SPICE Simulation result for stuck open fault in CPL Full Adder Sum Ckt.

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval (ns)	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_8	50 M	1	110	111	3.267	2.971E-11
		10	110	111	3.267	2.971E-11
		100	110	111	2.621	5.242E-08
	100 M	1	110	111	3.267	2.968E-11
		10	110	111	3.267	2.968E-11
		100	110	111	2.764	2.764E-08
	200 M	1	110	111	3.267	2.968E-11
		10	110	111	3.267	2.968E-11
		100	110	111	2.856	1.428E-08
M_8	50 M	1	010	101	0	2.971E-11
		10	010	101	0	2.971E-11
		100	010	101	0.08893	6.340E-08
	100 M	1	010	101	0	2.968E-11
		10	010	101	0	2.968E-11
		100	010	101	0.04630	3.306E-08
	200 M	1	010	101	0	2.968E-11
		10	010	101	0	2.968E-11
		100	010	101	0.1212	2.971E-11
M_8	50 M	1	100	101	0	2.971E-11
		10	100	101	0	2.971E-11
		100	100	101	0.08893	6.340E-08
	100 M	1	100	101	0	2.968E-11
		10	100	101	0	2.968E-11
		100	100	101	0.04630	3.306E-08
	200 M	1	100	101	0	2.968E-11
		10	100	101	0	2.968E-11
		100	100	101	0.1212	2.971E-11
M_8	50 M	1	000	111	3.267	2.971E-11
		10	000	111	3.267	2.971E-11
		100	000	111	2.621	5.242E-08
	100 M	1	000	111	3.267	2.968E-11
		10	000	111	3.267	2.968E-11
		100	000	111	2.764	2.764E-08
	200 M	1	000	111	3.267	2.968E-11
		10	000	111	3.267	2.968E-11
		100	000	111	2.856	1.428E-08

Effects of Fault Resistance and Time Interval:

As seen from table 4.5, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 50 MΩ to 200 MΩ, the output voltage and power supply current has a little effect. Since Steady state current do not increase very high the current monitoring is not possible to determine the stuck open fault. But in all cases two pattern test can detect fault. However time has great effect on the output voltage variation. As seen from the data application of the test vector 10 ns after the application of the initialization vector and observing the output after 50 ns will give result for two pattern test.

Table: 4.6

The following table shows the summary of stuck open faults in CPL Full Adder Sum circuit.

Summary for Stuck Open fault in CPL Full Adder Sum Ckt.

Fault	Successful Two Pattern Vectors	O/P Logic Level Un-faulted	O/P Logic Level Faulted	I_{DDQ} (amp)	Logic monitoring possible?	Current monitoring possible?
M_1	(000,100)	01	00	1.691E-08	Yes	No
	(011,100)	01	00	1.482E-08	Yes	No
	(101,100)	01	00	1.383E-08	Yes	No
	(110,100)	01	00	2.214E-15	Yes	No
	(001,110)	10	11	1.428E-08	Yes	No
M_2	(001,101)	10	11	3.852E-10	Yes	No
	(010,101)	10	11	9.900E-14	Yes	No
	(111,101)	10	11	3.828E-10	Yes	No
	(101,111)	01	00	3.679E-10	Yes	No
	(110,111)	01	00	2.613E-15	Yes	No
M_3	(001,000)	10	11	3.533E-10	Yes	No
	(010,000)	10	11	3.828E-10	Yes	No
	(011,000)	10	11	1.625E-10	Yes	No
	(100,000)	10	11	3.852E-10	Yes	No
	(111,000)	10	11	3.679E-10	Yes	No
	(000,010)	01	00	4.090E-14	Yes	No
	(111,101)	10	11	3.828E-10	Yes	No
M_4	(000,001)	01	00	3.533E-10	Yes	No
	(011,001)	01	00	3.828E-10	Yes	No
	(101,001)	01	00	1.625E-10	Yes	No
	(001,011)	10	11	3.852E-10	Yes	No
	(100,011)	10	11	3.679E-10	Yes	No
	(111,011)	10	11	4.090E-14	Yes	No
M_5	(001,000)	10	11	2.971E-11	Yes	No
	(111,000)	10	11	2.971E-11	Yes	No
	(000,110)	01	00	1.691E-08	Yes	No
	(110,010)	01	00	1.691E-08	Yes	No
M_6	(001,100)	10	11	2.971E-11	Yes	No
	(101,100)	10	11	2.971E-11	Yes	No
	(001,110)	01	00	1.691E-08	Yes	No
	(111,110)	01	00	1.691E-08	Yes	No
M_7	(000,001)	01	00	1.691E-08	Yes	No
	(110,001)	01	00	1.691E-08	Yes	No
	(010,011)	10	11	2.971E-11	Yes	No
	(100,011)	10	11	2.971E-11	Yes	No
M_8	(000,111)	10	11	2.971E-11	Yes	No
	(110,111)	10	11	2.971E-11	Yes	No
	(010,101)	01	00	1.691E-08	Yes	No
	(100,101)	01	00	1.691E-08	Yes	No

4.5 Discussion

It is found that stuck-on fault on all the MOS transistor of the SUM logic circuit can be detected by steady state current monitoring with appropriate test vectors. For some of these test vectors the fault can also be detected by logic monitoring, but in all cases this is also accompanied by a large flow of signal source current. Similarly all bridging fault can be detected by current monitoring, but no logic monitoring is possible. Stuck open fault on all the MOS transistors on the SUM logic circuit can be detected by appropriate two pattern test. Finally it is concluded that signal source current monitoring (I_{DDQ} testing) is the best method for fault detection in CPL circuits and gives a very wide range of fault coverage.

Table: 4.7

The following table shows the summary of various faults in CPL Full Adder Sum circuit.

Summay of Fault Detection of CPL Full Adder Sum Circuit

Transistor	Stuck-on Fault	Bridging Fault (G-S)	Stuck-open Fault
	Detected by	Detected by	Detected by
M_1	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
M_2	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
M_3	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
M_4	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
M_5	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
M_6	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
M_7	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
M_8	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
Fault coverage	**100% by I_{DDQ} testing**	**100% by I_{DDQ} testing**	**100% by Two pattern test**

CHAPTER 5

FAULT CHARACTERIZATION OF CPL FULL ADDER CARRY CIRCUIT

5.1 Introduction

The behaviors of CPL full adder carry circuits under single faults in various devices are investigated in this chapter. As stated in Chapter 3 to avoid the complexity of dealing with multiple defects, it is assumed that not more than one defect can occur at a time. Single stuck-on, bridging and stuck-open faults in all the MOS transistors are examined. The results of extensive SPICE simulation using various fault models are presented in this chapter.

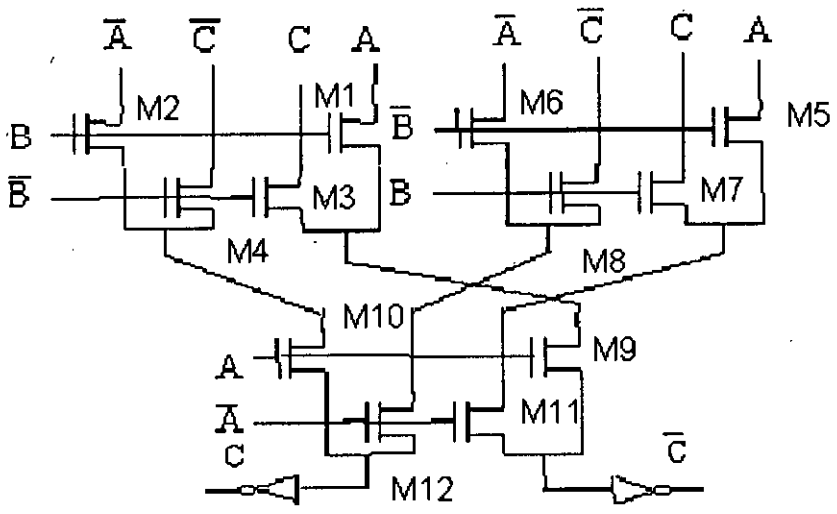


Figure 5.1: CPL Full Adder Carry Circuit.

5.2 Behavior Under Single Stuck on faults

The behaviors of CPL full adder carry circuits under single stuck on faults in MOS are analyzed in this section.

5.2.1 Qualitative Analysis

M_1 : (stuck on fault in M_1 of the CPL Full Adder Carry gate of figure 5.1)

Referred to figure 5.1 physical defects may cause M_1 to be permanent ON, thus causing a stuck on fault. The fault is modeled in figure 5.2 and 5.3 where the faulted MOS is replaced by a variable resistance R_f. The tests vectors (000), (010), (011), (101), (110) and (111) produce correct logic and no significant current flows in the

circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault.

Test Vector 001:

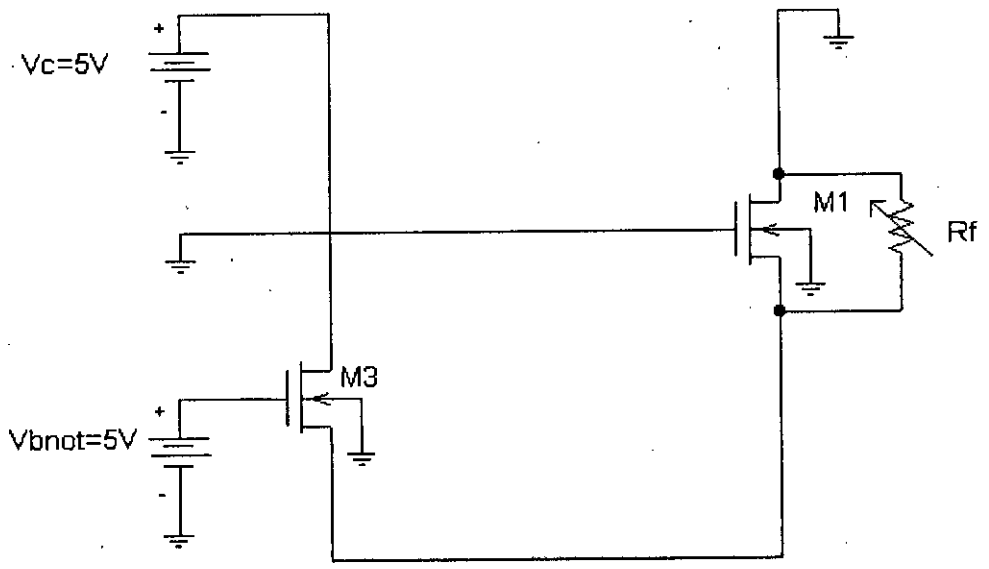


Fig. 5.2 Equivalent circuit for stuck on fault in MOS M_1 of CPL CARRY circuit. Test Vector [A=0, B=0, C=1].

In Figure 5.2, the vector (001) is applied, M_3, M_5 and M_{11} turn ON and a steady state current I_{DDQ} flows through M_3 and R_f of the circuit. In the faulted circuit, the output V_{out} is independent of the fault strength (R_f). Hence, the stuck on fault at M_1 cannot be detected by logic monitoring. However, the signal current, I is significantly large due to the low resistance path between V_{IH} and ground. The signal current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 100:

In Figure 5.3, the vector (100) is applied, M_3, M_5 and M_9 turn ON and a steady state current I_{DDQ} flows M_3 and R_f of through the circuit. In the faulted circuit, the output

$$V_{out} = \{R_{on}/(R_f+R_{on})\} V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0

to V_{IH} depending on R_f, Hence, the stuck on fault at M_1 cannot be detected by logic

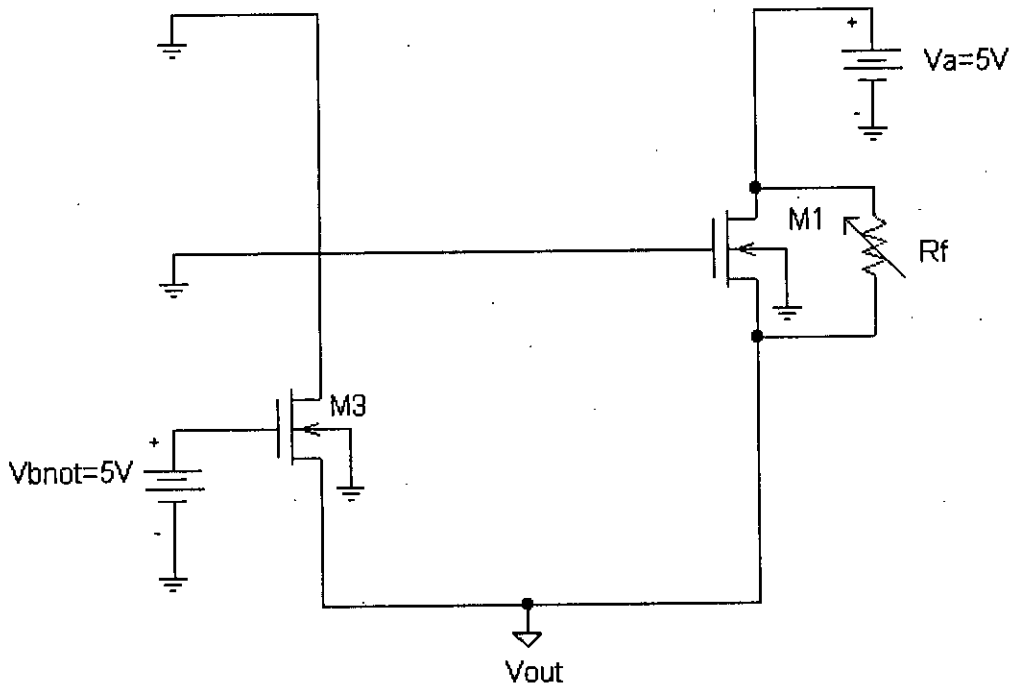


Fig. 5.3 Equivalent circuit for stuck on fault in MOS M_1 of CPL CARRY circuit. Test Vector [A=1, B=0, C=0].

monitoring. However, the signal current, I is significantly large due to the low resistance path between V_{IH} and ground. The steady state current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

M_3 : (stuck on fault in M_3 of the CPL Full Adder Carry circuit of figure 5.1)

Similar qualitative analysis have been done for stuck-on fault in MOS M_3 of the CPL full adder carry circuit. The tests vectors (000), (001), (010) (100), (101), and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. However when test vector [011] and [110] are applied a large steady state current flows through the circuit. Hence, the fault can be detected by current monitoring using the above two test vector. However, the output voltage varies from low to high depending on the fault strength. Hence, logic monitoring is not possible.

M_5 : (stuck on fault in M_5 of the CPL Full Adder Carry gate of figure 5.1)

Similar qualitative analysis have been done for stuck-on fault in MOS M_5 of the CPL full adder carry circuit. The tests vectors (000), (001), (010) (100), (101), and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. However when test vector [011] and [110] are applied a large steady state current flows through the circuit. Hence, the fault can be detected by current monitoring using the above two test vector. However, the output voltage varies from low to high depending on the fault strength. Hence, logic monitoring is not possible.

M_7 : (stuck on fault in M_7 of the CPL Full Adder Carry gate of figure 5.1)

Similar qualitative analysis have been done for stuck-on fault in MOS M_7 of the CPL full adder carry circuit. The tests vectors (000), (010), (011), (101), (110), and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. However when test vector [001] and [100] are applied a large steady state current flows through the circuit. Hence, the fault can be detected by current monitoring using the above two test vector. However, the output voltage varies from low to high depending on the fault strength. Hence, logic monitoring is not possible.

M_9 : (stuck on fault in M_9 of the CPL Full Adder Carry gate of figure 5.1)

The fault is modeled in figure 5.4 and 5.5 where the faulted MOS is replaced by a variable resistance R_f. The tests vectors (000), (010), (100), (101), (110), and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault.

Test Vector 001:

In Figure 5.4, the vector (001) is applied, M_3, M_5 and M_{11} turn ON and a steady state current I_{DDQ} flows through M_3, M_{11}, R_f and M_5 of the circuit. In the faulted circuit, the output voltage

$$V_{out} = \{2R_{on}/(R_f+3R_{on})\}V_{IH}$$

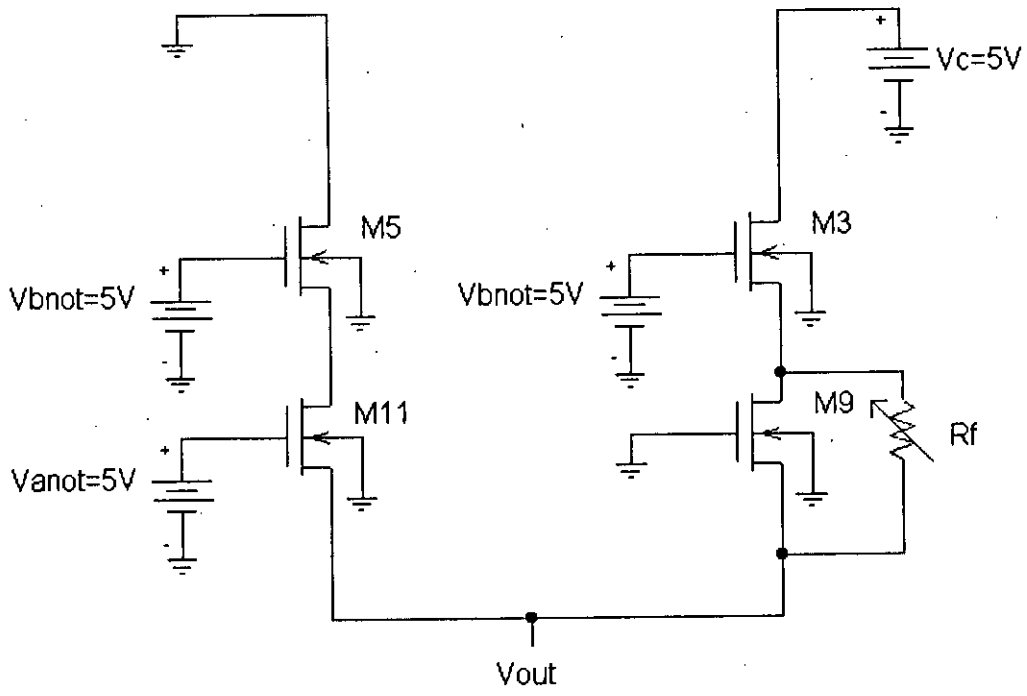


Fig. 5.4 Equivalent circuit for stuck on fault in MOS M_9 of CPL CARRY circuit. Test Vector [A=0, B=0, C=1].

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches $2V_{IH}/3$ and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to $2V_{IH}/3$ depending on R_f, Hence, the stuck on fault at M_9 cannot be detected by logic monitoring. However, the signal current, I is significantly large due to the low resistance path between V_{IH} and ground. The signal current is given by

$$I = V_{IH}/(R_f + 3R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 011:

In Figure 5.5, the vector (011) is applied, M_1, M_7 and M_{11} turn ON and a steady state current I_{DDQ} flows M_7, M_{11}, R_f and M_1 of through the circuit. In the faulted circuit, the output voltage

$$V_{out} = \{(R_f+R_{on})/(R_f+3R_{on})\} V_{IH}$$

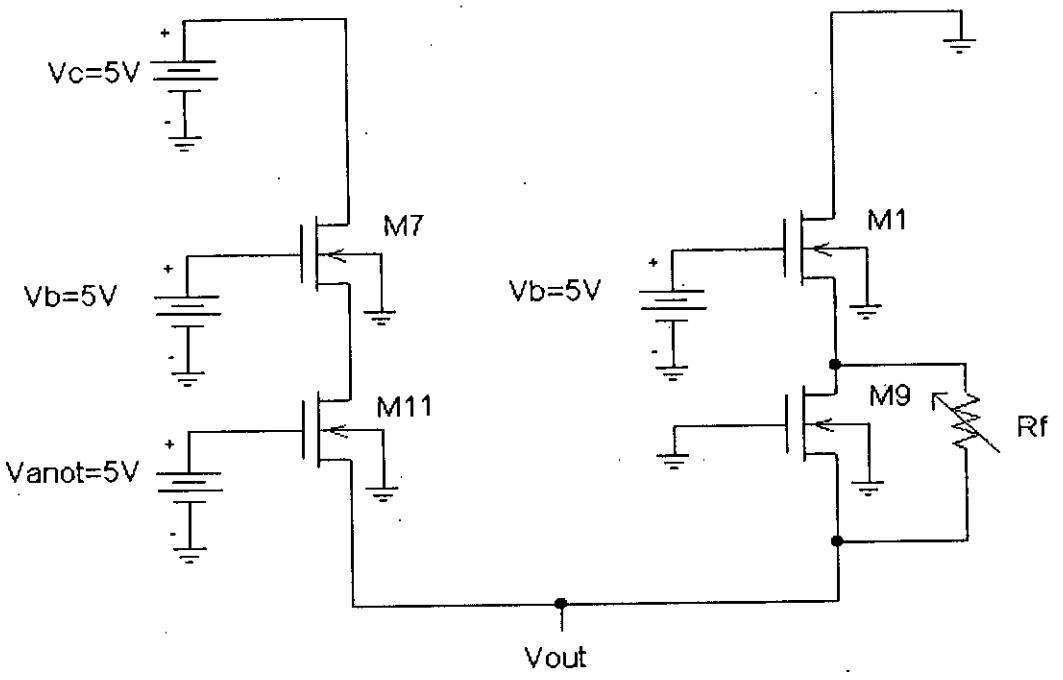


Fig. 5.5 Equivalent circuit for stuck on fault in MOS M_9 of CPL CARRY circuit. Test Vector [A=0, B=1, C=1].

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches $V_{IH}/3$ and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from V_{IH} to $V_{IH}/3$ depending on R_f, Hence, the stuck on fault at M_9 cannot be detected by logic monitoring. However, the signal current, I is significantly large due to the low resistance path between V_{IH} and ground. The signal current is given by

$$I = V_{IH}/(R_f + 3R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

M_{11} : (stuck on fault in M_{11} of the CPL Full Adder Carry gate - figure 5.1)

Similar qualitative analysis have been done for stuck-on fault in MOS M5 of the CPL full adder carry circuit. The tests vectors (000), (001), (010), (011), (101), and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault. However when test vector [100] and [110] are applied a large steady state current flows through the circuit. Hence, the fault can be detected by current monitoring using the above two test vector. However, the output voltage varies from low to high depending on the fault strength. Hence, logic monitoring is not possible.

5.2.2 SPICE Simulation Results

This section summarizes the SPICE simulation results for a single stuck on fault in the MOS devices of the CPL full adder sum circuit.

Table: 5.1

SPICE Simulation result for stuck on fault in CPL Full Adder Carry gate. Effect of Fault Strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_1	1	0	0	5	0	2.34E-03
	10	0	0	5	0	2.32E-03
	100	0	0	5	0	2.09E-03
	1K	0	0	5	0	1.11E-03
	10K	0	0	5	0	2.33E-04
	100K	0	0	5	0	2.94E-05
M_1	1	5	0	0	3.2267	2.35E-03
	10	5	0	0	3.2267	2.35E-03
	100	5	0	0	3.2267	2.33E-03
	1K	5	0	0	2.8243	2.18E-03
	10K	5	0	0	0.2666	4.73E-04
	100K	5	0	0	0.0260	4.97E-05
M_3	1	0	5	5	3.2666	2.35E-03
	10	0	5	5	3.2666	2.35E-03
	100	0	5	5	3.2666	2.33E-03
	1K	0	5	5	3.2666	2.18E-03
	10K	0	5	5	3.2666	4.77E-04
	100K	0	5	5	3.2666	4.97E-05
M_3	1	5	5	0	0.0023	2.34E-03
	10	5	5	0	0.0232	2.32E-03
	100	5	5	0	0.2093	2.09E-03
	1K	5	5	0	1.1112	1.11E-03
	10K	5	5	0	2.3290	2.33E-04
	100K	5	5	0	2.9434	2.94E-05
M_5	1	0	5	5	0.0023	2.34E-03
	10	0	5	5	0.0232	2.32E-03
	100	0	5	5	0.2093	2.09E-03
	1K	0	5	5	1.1112	1.11E-03
	10K	0	5	5	2.3290	2.33E-04
	100K	0	5	5	2.9434	2.94E-05
M_5	1	5	5	0	3.2666	2.35E-03
	10	5	5	0	3.2666	2.35E-03
	100	5	5	0	3.2666	2.33E-03
	1K	5	5	0	3.2666	2.18E-03
	10K	5	5	0	3.2666	4.73E-04
	100K	5	5	0	3.2666	4.97E-05

Table: 5.1 (Cont'd)
SPICE Simulation result for stuck on fault in CPL Full Adder Carry gate.
Effect of Fault Strength

Stuck on MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out} (Volt)	Steady state current I_{DDQ} (amp)
		V_a	V_b	V_c		
M_7	1	0	0	5	3.2667	2.35E-03
	10	0	0	5	3.2667	2.35E-03
	100	0	0	5	3.2667	2.33E-03
	1K	0	0	5	2.8243	2.18E-03
	10K	0	0	5	0.2666	4.73E-04
	100K	0	0	5	0.0260	4.97E-05
M_7	1	5	0	0	0	2.34E-03
	10	5	0	0	0	2.32E-03
	100	5	0	0	0	2.09E-03
	1K	5	0	0	0	1.11E-03
	10K	5	0	0	0	2.33E-04
	100K	5	0	0	0	2.94E-05
M_9	1	0	0	5	1.3247	9.16E-04
	10	0	0	5	1.3193	9.13E-04
	100	0	0	5	1.2672	8.89E-04
	1K	0	0	5	0.9003	6.94E-04
	10K	0	0	5	0.2348	2.14E-04
	100K	0	0	5	0.0305	2.92E-05
M_9	1	0	5	5	0.5660	9.16E-04
	10	0	5	5	0.5716	9.12E-04
	100	0	5	5	0.6250	8.78E-04
	1K	0	5	5	1.0197	6.45E-04
	10K	0	5	5	2.0600	1.95E-04
	100K	0	5	5	2.8172	2.80E-05
M_{11}	1	5	0	0	1.3247	9.16E-04
	10	5	0	0	1.3193	9.13E-04
	100	5	0	0	1.2672	8.89E-04
	1K	5	0	0	0.9003	6.94E-04
	10K	5	0	0	0.2348	2.14E-04
	100K	5	0	0	0.0305	2.92E-05
M_{11}	1	5	5	0	0.5660	9.16E-04
	10	5	5	0	0.5716	9.12E-04
	100	5	5	0	0.6250	8.78E-04
	1K	5	5	0	1.0197	6.45E-04
	10K	5	5	0	2.0572	1.95E-04
	100K	5	5	0	2.8172	2.80E-05

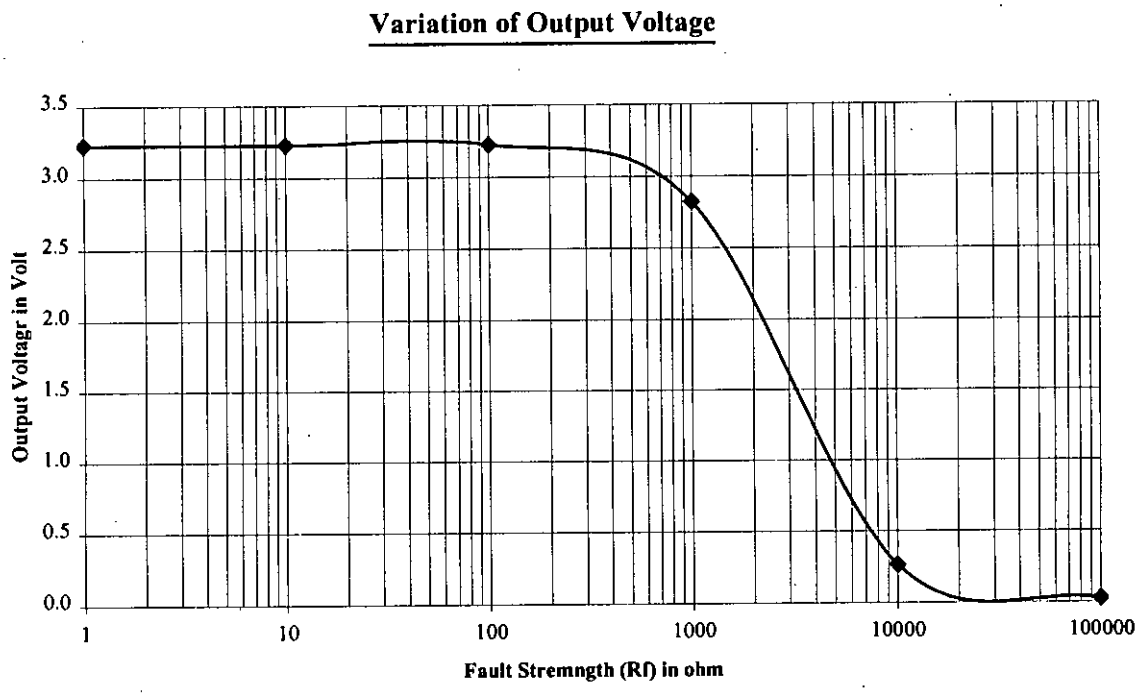


Fig 5.6: Output Voltage vs Fault Strength
(Stuck on fault for M_1 Test Vector 100 and M_7 Test Vector 001)

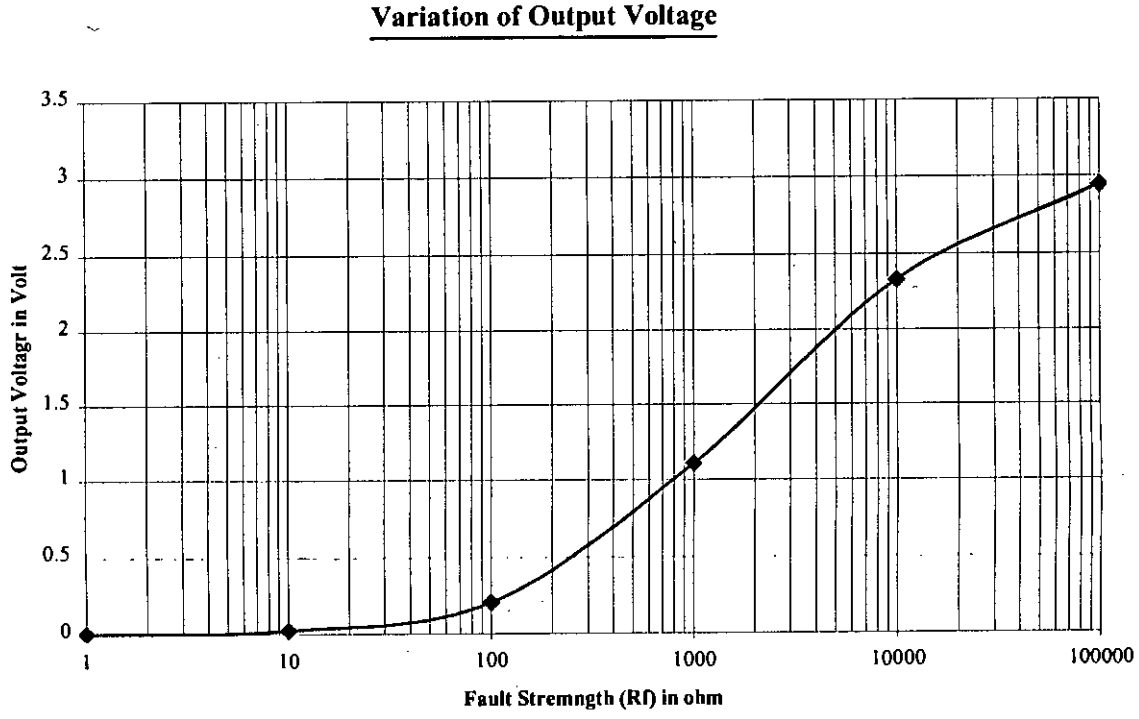


Fig 5.7: Output Voltage vs Fault Strength
(Stuck on fault for M_3 Test Vector 110 and M_5 Test Vector 011)

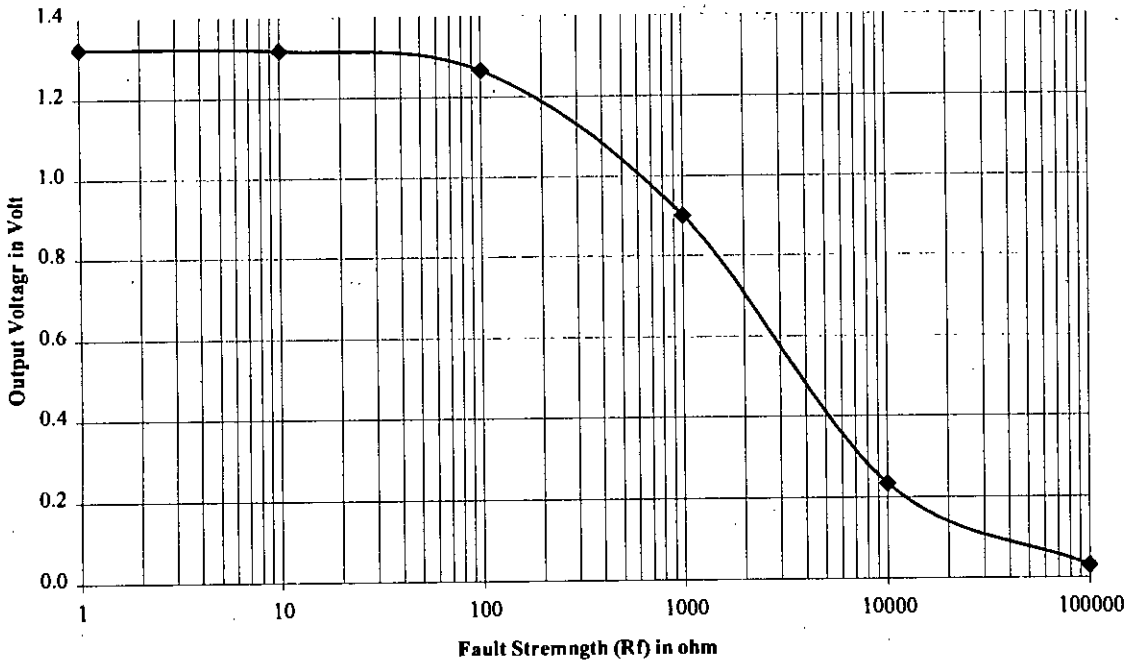


Fig 5.8: Output Voltage vs Fault Strength
(Stuck on fault for M_9 Test Vector 001 and M_{11} Test Vector 100)

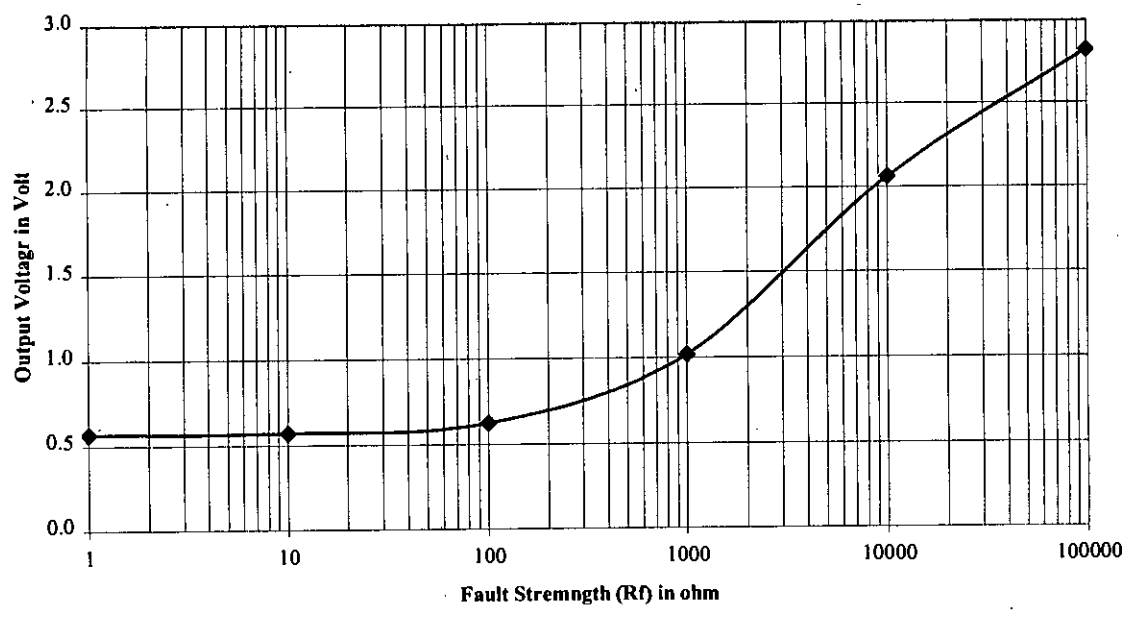


Fig 5.9: Output Voltage vs Fault Strength
(Stuck on fault for M_9 Test Vector 011 and M_{11} Test Vector 110)

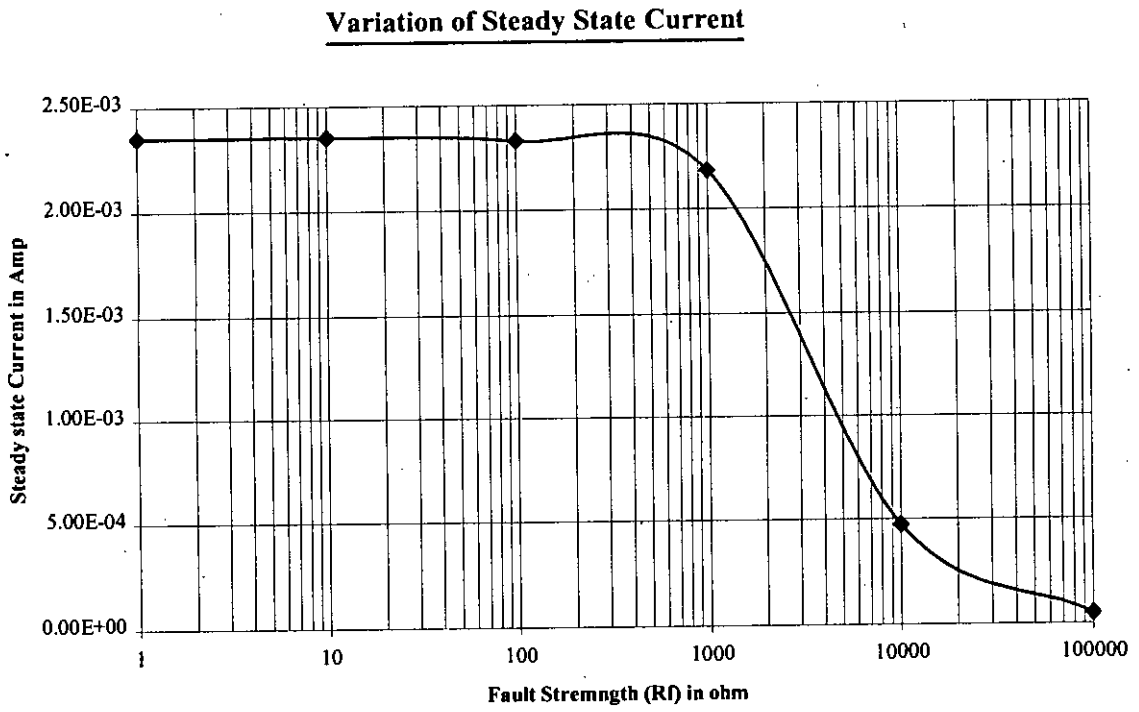


Fig 5.10: Steady State Current vs Fault Strength (Stuck on fault for M_1 Test Vector 100 and M_7 Test Vector 001)

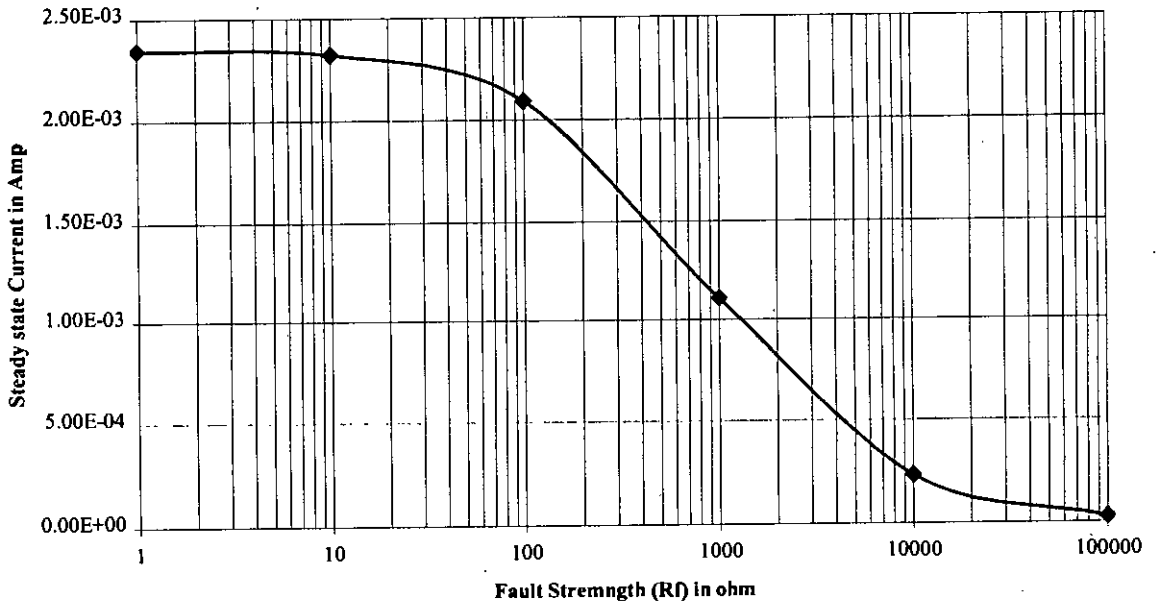


Fig 5.11: Steady State Current vs Fault Strength (Stuck on fault for M_3 Test Vector 110 and M_5 Test Vector 011)

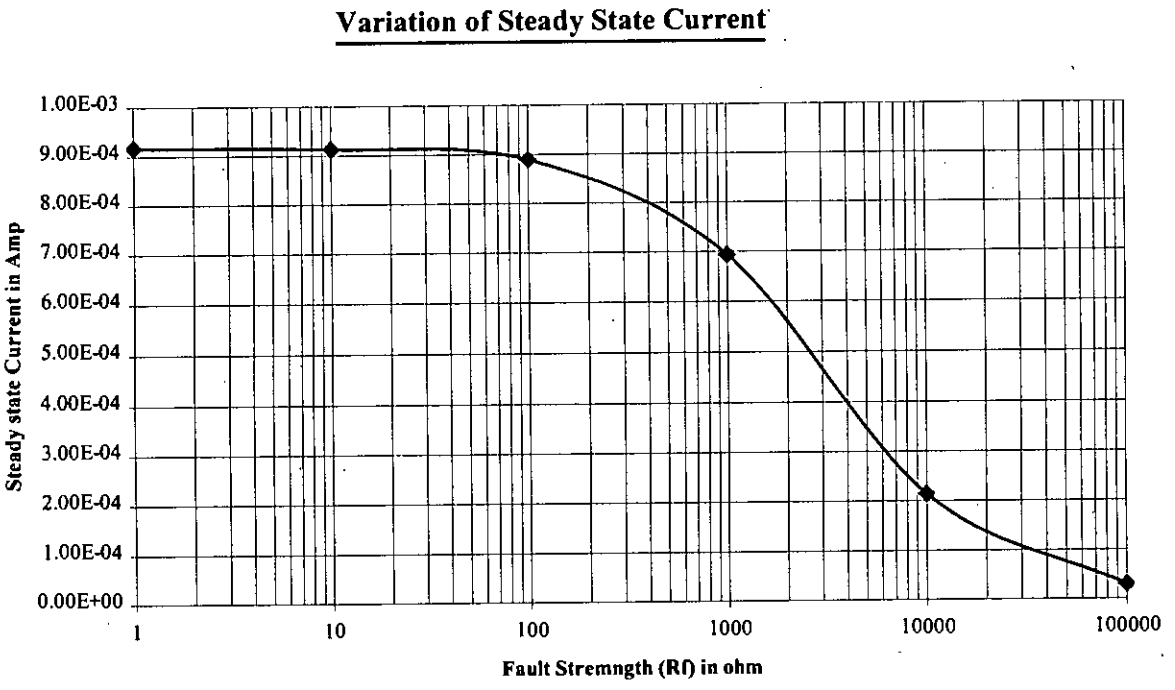


Fig 5.12: Steady State Current vs Fault Strength
(Stuck on fault for M_9 Test Vector 001 and M_{11} Test Vector 100)

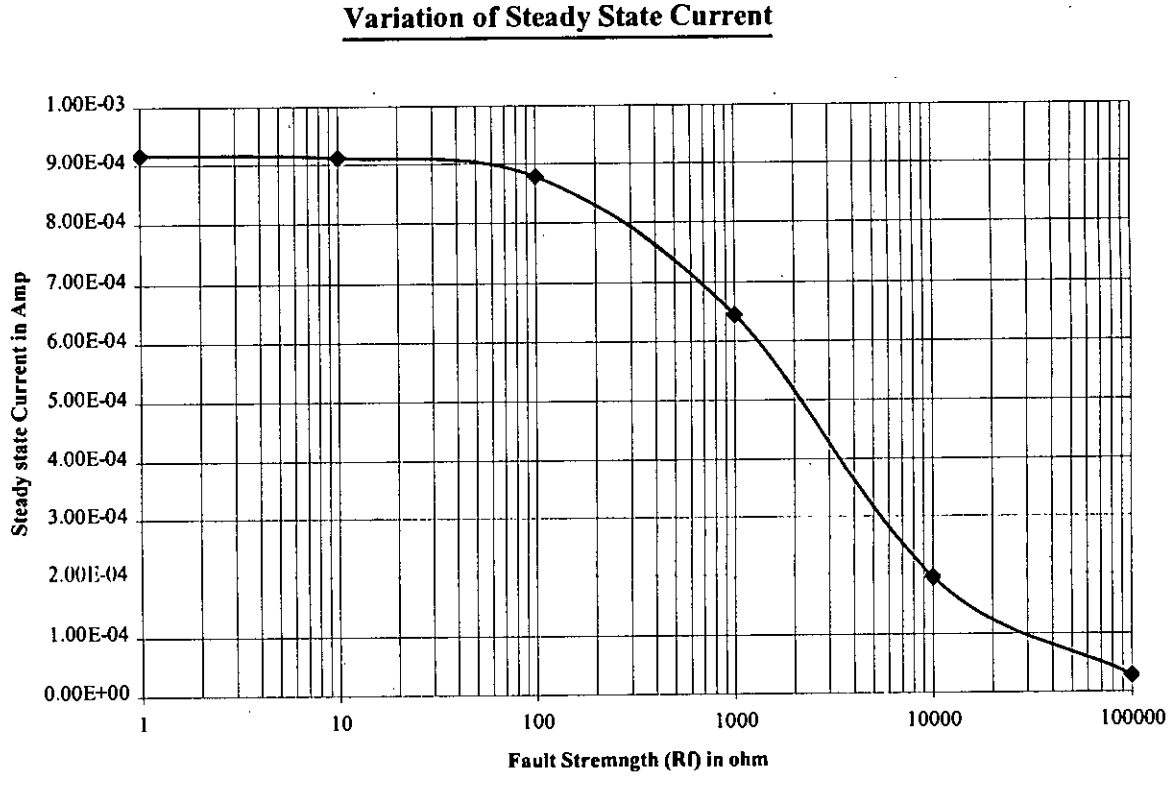


Fig 5.13: Steady State Current vs Fault Strength
(Stuck on fault for M_9 Test Vector 011 and M_{11} Test Vector 110)

Effects of Fault Resistance

From the results of Table 5.1 shows, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 1 Ω to 100 kΩ, the output voltage varies from 0 to 3.2667 Volt. This appreciable variation in output voltage clearly shows that the output logic level is indeterminable. This agrees with our prediction that the fault cannot be detected by logic monitoring. As seen from the table, signal current is in the range of miliampere compared to normal operating current of 0A. Therefore, the fault can be detected by current monitoring.

Table 5.2

The following table shows the summary of stuck on faults in CPL Full Adder Carry circuit.

Summery for Stuck on faults in CPL Full Adder Carry gate

Fault	Successful Test Vector	Output Logic Level (Volt)	I_{DDQ} (amp)	Logic monitoring possible?	Current monitoring possible?
M_1	(001),(100)	0 to 3.2667	2.34E-03 to 2.94E-05	No	Yes
M_3	(011),(110)	0 to 3.2667	2.34E-03 to 2.94E-05	No	Yes
M_5	(011),(110)	0 to 3.2667	2.34E-03 to 2.94E-05	No	Yes
M_7	(001),(100)	0 to 3.2667	2.34E-03 to 2.94E-05	No	Yes
M_9	(001),(011)	0 to 2.8172	2.34E-03 to 2.94E-05	No	Yes
M_{11}	(100),(110)	0.03 to 3.26	2.34E-03 to 2.94E-05	No	Yes

5.3 Behavior Under Single Bridging faults

The behavior of CPL full adder CARRY circuit under single bridging faults in all the MOS transistor of the circuit are analyzed in this section.

5.3.1 Qualitative Analysis

M_1 : (bridging fault in M_1 of the CPL Full Adder Carry gate of figure 5.1)

Referred to figure 5.1 physical defects may cause a short circuit to exist between gate and source of M_1, thus causing a bridging fault. The fault is modeled in figure 5.14, 5.15, 5.16 and 5.17 where the faulted MOS is replaced by a variable resistance R_f. The tests vectors (000), (100), (110) and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault.

Test Vector 001:

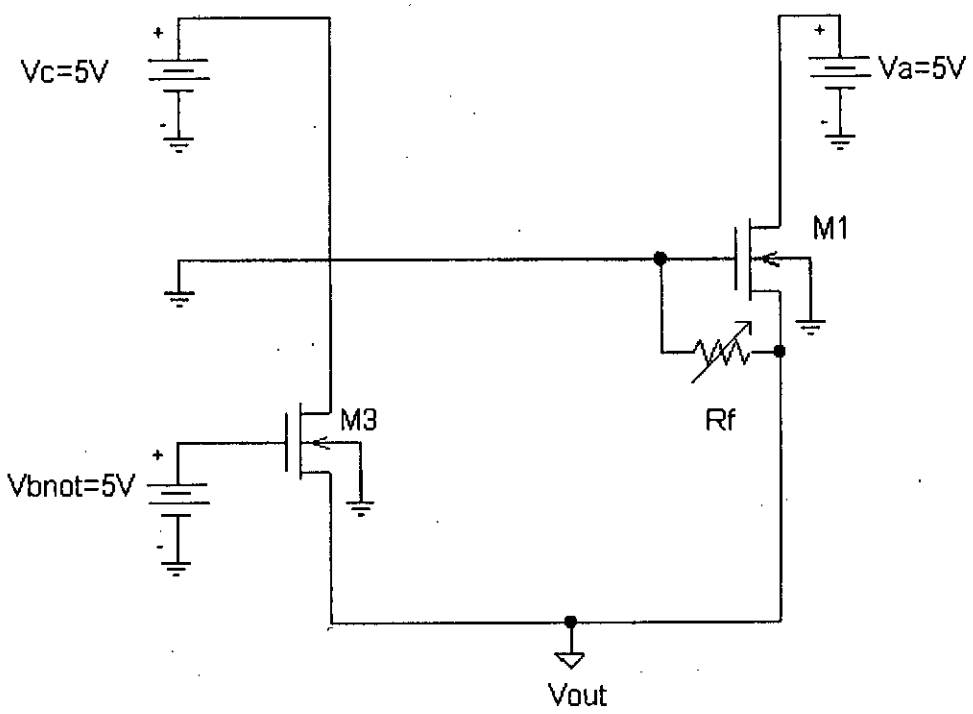


Fig. 5.14 Equivalent circuit of gate to source bridging fault on MOS M_1 of CPL Full Adder CARRY circuit. Test Vector [A=0, B=0, C=1]

In Figure 5.14, the vector (001) is applied, M_3, M_5 and M_{11} turn ON and a steady state current I_{DDQ} flows through M_3 and R_f of the circuit. In the faulted circuit, the output V_{out} is independent of the fault strength (R_f). Hence the bridging fault at M_1 cannot be detected by logic monitoring. However, the signal current, I is significantly large due to the low resistance path between V_{IH} and ground. The signal current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 010:

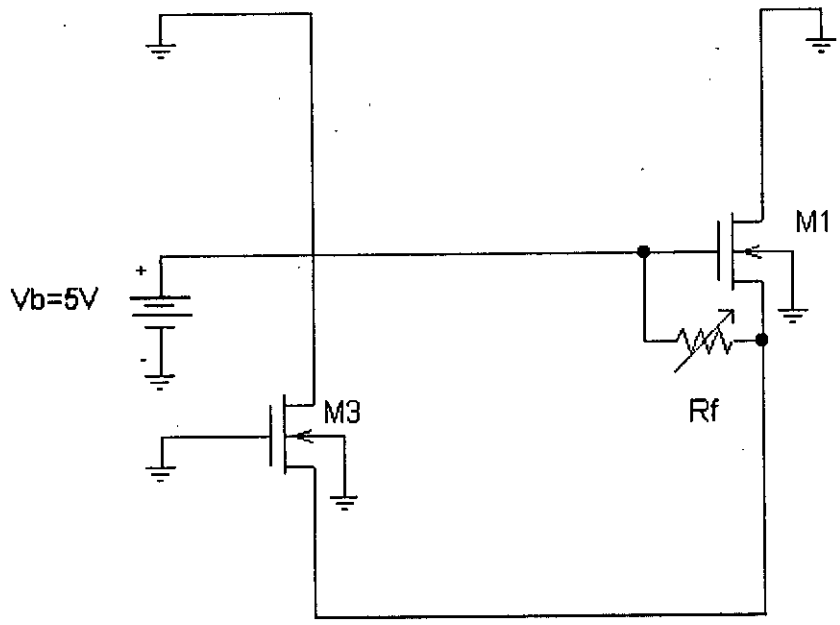


Fig. 5.15 Equivalent circuit of gate to source bridging fault on MOS M_1 of CPL Full Adder CARRY circuit. Test Vector [A=0, B=1, C=0]

In Figure 5.15, the vector (010) is applied, M_1, M_7 and M_{11} turn ON and a steady state current I_{DDQ} flows through M_1 and R_f of the circuit. In the faulted circuit, the output V_{out} is independent of the fault strength (R_f). Hence the bridging fault at M_1 cannot be detected by logic monitoring. However, the signal current, I is significantly large due to the low resistance path between V_{IH} and ground. The signal current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 011:

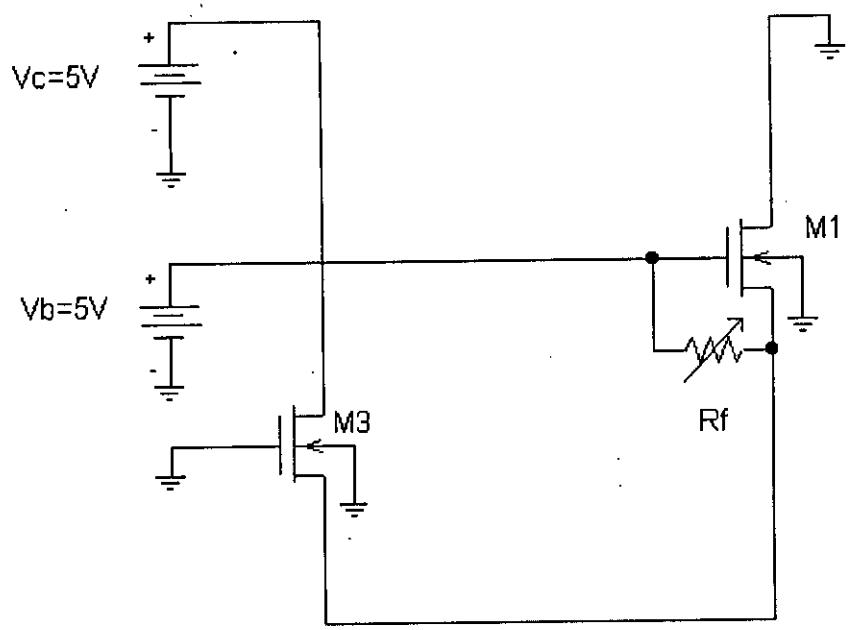


Fig. 5.16 Equivalent circuit of gate to source bridging fault on MOS M_1 of CPL Full Adder CARRY circuit. Test Vector [A=0, B=1, C=1]

In Figure 5.16, the vector (011) is applied, M_1, M_7 and M_{11} turn ON and a steady state current I_{DDQ} flows through M_1 and R_f of the circuit. In the faulted circuit, the output V_{out} is independent of the fault strength (R_f). Hence the bridging fault at M_1 cannot be detected by logic monitoring. However, the signal current, I is significantly large due to the low resistance path between V_{IH} and ground. The signal current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

Test Vector 101:

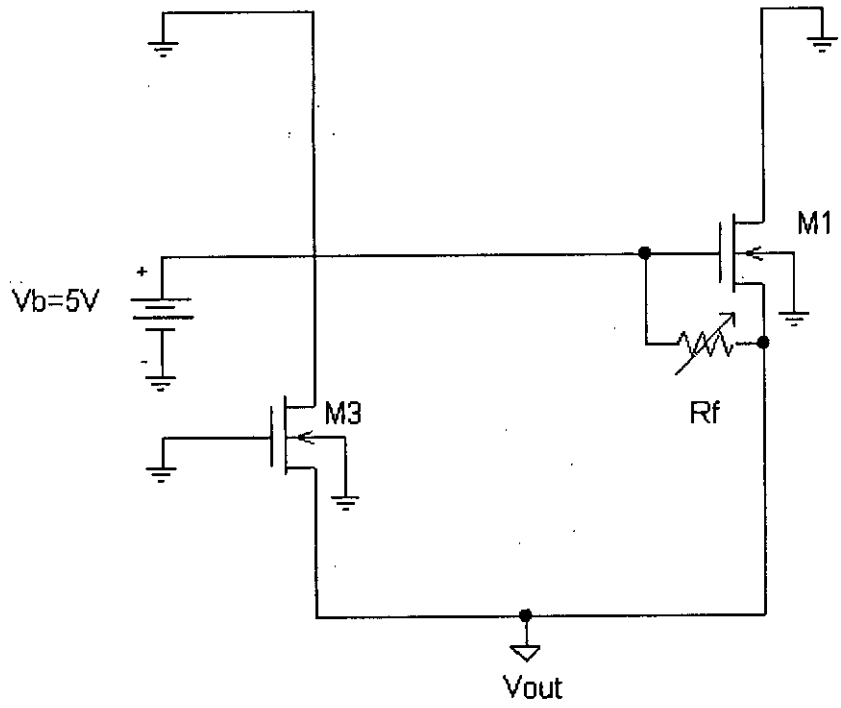


Fig. 5.17 Equivalent circuit of gate to source bridging fault on MOS M_1 of CPL Full Adder CARRY circuit. Test Vector [A=1, B=0, C=1]

In Figure 5.17, the vector (101) is applied, M_3, M_5 and M_9 turn ON and a steady state current I_{DDQ} flows through M_1 and R_f of the circuit. In the faulted circuit, the output voltage

$$V_{out} = \{R_f/(R_f+R_{on})\} V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the bridging fault at M_1 cannot be detected by logic monitoring. However, the signal current, I is significantly large due to the low resistance path between V_{IH} and ground. The signal current is given by

$$I = V_{IH}/(R_f + R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

M_3 : (bridging fault in M_3 of the CPL Full Adder Carry gate of figure 5.1)

Similar qualitative analysis have been done for gate to source bridging fault on MOS M_3 of the CARRY circuit. The tests vectors (001), (010), (011) and (101) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. When test vector [000], [100], [110], [111] are applied, the output voltage varies from low to high depending on the fault strength. Hence logic monitoring can not be used. However, when these vectors are applied a large current flows through the circuit. Hence, the fault can be detected by current monitoring.

M_5 : (bridging fault in M_5 of the CPL Full Adder Carry gate of figure 5.1)

Similar qualitative analysis have been done for gate to source bridging fault on MOS M_5 of the CARRY circuit. The tests vectors (010), (100), (101) and (110) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. When test vector [000], [001], [011], [111] are applied, the output voltage varies from low to high depending on the fault strength. Hence logic monitoring can not be used. However, when these vectors are applied a large current flows through the circuit. Hence, the fault can be detected by current monitoring.

M_7 : (bridging fault in M_7 of the CPL Full Adder Carry gate of figure 5.1)

Similar qualitative analysis have been done for gate to source bridging fault on MOS M_7 of the CARRY circuit. The tests vectors (000), (001), (011) and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. When test vector [010], [100], [101], [110] are applied, the output voltage varies from low to high depending on the fault strength. Hence logic monitoring can not be used. However, when these vectors are applied a large current flows through the circuit. Hence the fault can be detected by current monitoring.

M_9 : (bridging fault in M_9 of the CPL Full Adder Carry gate of figure 5.1)

The fault is modeled in figure 5.18 and 5.19 where a variable resistance R_f is connected between gate and source of the faulted MOS. The tests vectors (000),

(001), (010), (101), (110) and (111) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence, these vectors are incapable of detecting the fault.

i. Test Vector 011:

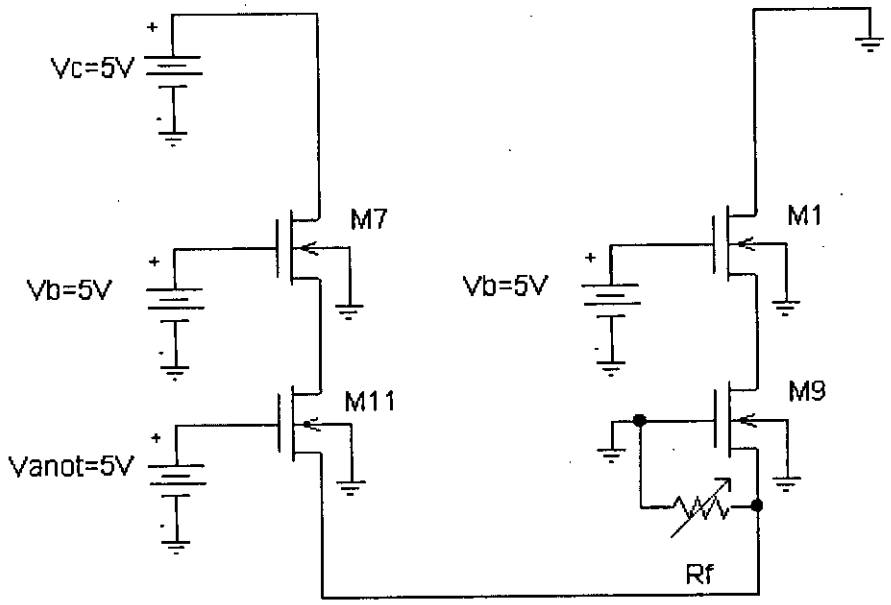


Fig. 5.18 Equivalent circuit of gate to source bridging fault on MOS M_9 of CPL Full Adder CARRY circuit. Test Vector [A=0, B=1, C=1]

In Figure 5.18, the vector (011) is applied, M_1, M_7 and M_{11} turn ON and a steady state current I_{DDQ} flows through M_7, M_{11} and R_f of the circuit. In the faulted circuit, the output

$$V_{out} = \{R_f/(R_f+2R_{on})\}V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches 0 V and when R_f is very large V_{out} approaches V_{IH}. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the bridging fault at M_9 cannot be detected by logic monitoring. However, the signal current, I is significantly large due to the low resistance path between V_{IH} and ground. The signal current is given by

$$I = V_{IH}/(R_f+2R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

ii. Test Vector 100:

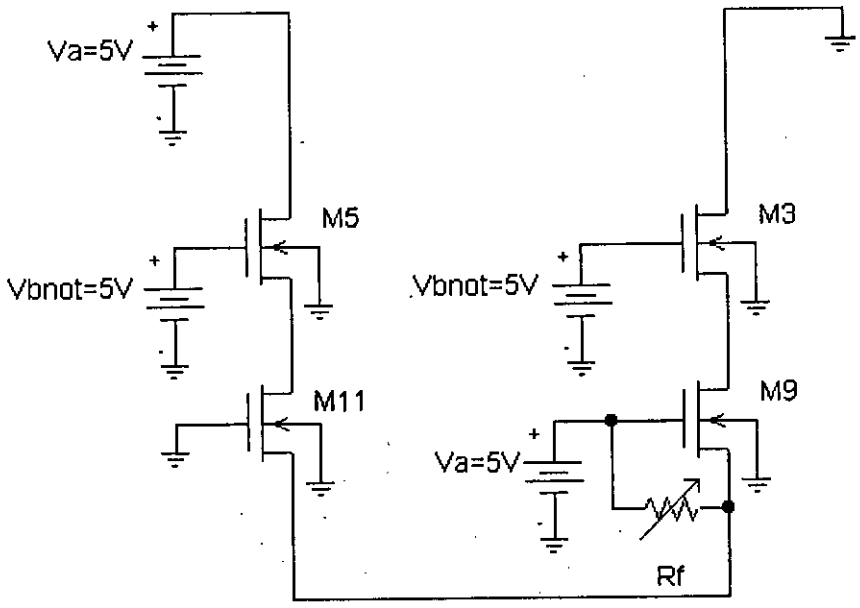


Fig. 5.19 Equivalent circuit of gate to source bridging fault on MOS M_9 of CPL Full Adder CARRY circuit. Test Vector [A=1, B=0, C=0]

In Figure 5.19, the vector (100) is applied, M_3, M_5 and M_9 turn ON and a steady state current I_{DDQ} flows through M_3, M_9 and R_f of the circuit. In the faulted circuit, the output

$$V_{out} = \{2R_{on}/(R_f+2R_{on})\}V_{IH}$$

When fault strength is maximum, i.e., R_f approaches zero, V_{out} approaches V_{IH} and when R_f is very large V_{out} approaches 0 V. Now since V_{out} can attain any value from 0 to V_{IH} depending on R_f, hence the bridging fault at M_9 cannot be detected by logic monitoring. However, the signal current, I is significantly large due to the low resistance path between V_{IH} and ground. The signal current is given by

$$I = V_{IH}/(R_f+R_{on})$$

Hence, the fault can be detected by current monitoring (I_{DDQ} Testing).

M_{11}: (bridging fault in M_{11} of the CPL Full Adder Carry gate of figure 5.1)

Similar qualitative analysis have been done for gate to source bridging fault on MOS M_{11} of the CARRY circuit. The tests vectors (011) and (100) produce correct logic and no significant current flows in the circuit when these test vectors are applied. Hence these vectors are incapable of detecting the fault. . When test vector [000], [001], [010], [101], [110], and [111] are applied, the output voltage varies from low to high depending on the fault strength. Hence logic monitoring can not be used. However, when these vectors are applied a large current flows through the circuit. Hence, the fault can be detected by current monitoring.

5.3.2 SPICE Simulation Results

This section summarizes the SPICE simulation results for a single bridging fault in the MOS devices of the CPL full adder carry circuit.

Table: 5.3

SPICE Simulation result for bridging fault in CPL Full Adder Carry gate. Effect of Fault Strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out} (Volt)	Steady state current I_{DDQ} (amp)
		V_a	V_b	V_c		
M_1	1	0	0	5	0	2.344E-03
	10	0	0	5	0	2.318E-03
	100	0	0	5	0	2.093E-03
	1K	0	0	5	0	1.111E-03
	10K	0	0	5	0	2.329E-04
	100K	0	0	5	0	2.943E-05
M_1	1	0	5	0	0	2.346E-03
	10	0	5	0	0	2.345E-03
	100	0	5	0	0	2.329E-03
	1K	0	5	0	0	2.176E-03
	10K	0	5	0	0	4.733E-04
	100K	0	5	0	0	4.974E-04
M_1	1	0	5	5	3.2666	2.346E-03
	10	0	5	5	3.2666	2.345E-03
	100	0	5	5	3.2666	2.329E-03
	1K	0	5	5	3.2666	2.176E-03
	10K	0	5	5	3.2666	4.733E-04
	100K	0	5	5	3.2666	4.974E-05
M_1	1	5	0	5	0.0023	2.344E-03
	10	5	0	5	0.0232	2.318E-03
	100	5	0	5	0.2093	2.093E-03
	1K	5	0	5	1.1112	1.111E-03
	10K	5	0	5	2.3290	2.329E-04
	100K	5	0	5	2.9434	2.943E-05
M_3	1	0	0	0	0.1309	-2.346E-03
	10	0	0	0	0.1309	2.345E-03
	100	0	0	0	0	2.329E-03
	1K	0	0	0	0	2.176E-03
	10K	0	0	0	0	4.733E-04
	100K	0	0	0	0	1.201E-04
M_3	1	5	0	0	3.262	2.346E-03
	10	5	0	0	3.264	2.345E-03
	100	5	0	0	3.265	2.329E-03
	1K	5	0	0	2.824	2.176E-03
	10K	5	0	0	0.2666	4.733E-04
	100K	5	0	0	0.0260	4.974E-05

Table: 5.3 (Cont'd)

SPICE Simulation result for bridging fault in CPL Full Adder Carry gate.

Effect of Fault Strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_3	1	5	5	0	0.0024	2.344E-03
	10	5	5	0	0.0232	2.318E-03
	100	5	5	0	0.2093	2.093E-03
	1K	5	5	0	1.111	1.111E-03
	10K	5	5	0	2.328	2.328E-04
	100K	5	5	0	2.941	2.942E-05
M_3	1	5	5	5	0.0023	2.344E-03
	10	5	5	5	0.0231	2.318E-03
	100	5	5	5	0.2093	2.093E-03
	1K	5	5	5	1.111	1.111E-03
	10K	5	5	5	2.329	2.329E-04
	100K	5	5	5	2.943	2.943E-05
M_5	1	0	0	0	3.267	2.346E-03
	10	0	0	0	3.267	2.345E-03
	100	0	0	0	3.267	2.329E-03
	1K	0	0	0	2.823	2.202E-03
	10K	0	0	0	0.266	5.386E-04
	100K	0	0	0	0.0206	4.974E-05
M_5	1	0	0	5	3.267	2.346E-03
	10	0	0	5	3.267	2.345E-03
	100	0	0	5	3.267	2.329E-03
	1K	0	0	5	2.824	2.176E-03
	10K	0	0	5	0.266	4.733E-04
	100K	0	0	5	0.02603	4.973E-05
M_5	1	0	5	5	0.002	2.344E-03
	10	0	5	5	0.022	2.318E-03
	100	0	5	5	0.293	2.093E-03
	1K	0	5	5	1.111	1.111E-03
	10K	0	5	5	2.329	2.329E-04
	100K	0	5	5	2.943	2.943E-05
M_5	1	5	5	5	3.264	2.344E-03
	10	5	5	5	3.264	2.318E-03
	100	5	5	5	3.264	2.093E-03
	1K	5	5	5	3.264	1.111E-03
	10K	5	5	5	3.264	2.329E-04
	100K	5	5	5	3.264	2.943E-05

Table: 5.3 (Cont'd)

SPICE Simulation result for bridging fault in CPL Full Adder Carry gate.

Effect of Fault Strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_7	1	0	5	0	3.257	2.346E-03
	10	0	5	0	3.257	2.630E-03
	100	0	5	0	3.263	2.329E-03
	1K	0	5	0	2.823	2.176E-03
	10K	0	5	0	0.266	4.733E-04
	100K	0	5	0	0.026	4.974E-05
M_7	1	5	0	0	0	2.344E-03
	10	5	0	0	0	2.318E-03
	100	5	0	0	0	2.093E-03
	1K	5	0	0	0	1.111E-03
	10K	5	0	0	0	2.329E-04
	100K	5	0	0	0	2.943E-05
M_7	1	5	0	5	3.252	2.344E-03
	10	5	0	5	3.252	2.318E-03
	100	5	0	5	3.254	2.093E-03
	1K	5	0	5	3.257	1.111E-03
	10K	5	0	5	3.249	2.329E-04
	100K	5	0	5	3.249	2.943E-05
M_7	1	5	5	0	3.262	2.364E-03
	10	5	5	0	3.260	2.345E-03
	100	5	5	0	3.262	2.329E-03
	1K	5	5	0	3.260	2.176E-03
	10K	5	5	0	3.260	4.734E-04
	100K	5	5	0	3.260	4.974E-05
M_9	1	0	5	5	0.001	1.316E-03
	10	0	5	5	0.013	1.307E-03
	100	0	5	5	0.122	1.224E-03
	1K	0	5	5	0.781	7.814E-04
	10K	0	5	5	2.032	2.032E-04
	100K	0	5	5	2.816	2.816E-05
M_9	1	5	0	0	4.999	1.317E-03
	10	5	0	0	4.987	1.317E-03
	100	5	0	0	4.869	1.314E-03
	1K	5	0	0	3.710	1.290E-03
	10K	5	0	0	0.528	4.472E-04
	100K	5	0	0	0.005	4.948E-05

Table: 5.3 (Cont'd)
SPICE Simulation result for bridging fault in CPL Full Adder Carry gate.
Effect of Fault Strength

Bridging MOS transistor	Fault Resistance R_f (Ω)	Sensitizing vector (Volt)			V_{out}	Steady state current I_{DDQ}
		V_a	V_b	V_c	(Volt)	(amp)
M_{11}	1	0	0	0	4.999	1.317E-03
	10	0	0	0	4.987	1.317E-03
	100	0	0	0	4.869	1.314E-03
	1K	0	0	0	3.710	1.290E-03
	10K	0	0	0	0.528	4.472E-04
	100K	0	0	0	0.005	4.948E-05
M_{11}	1	0	0	5	4.999	1.317E-03
	10	0	0	5	4.987	1.317E-03
	100	0	0	5	4.869	1.314E-03
	1K	0	0	5	3.710	1.290E-03
	10K	0	0	5	0.528	4.472E-04
	100K	0	0	5	0.052	4.948E-05
M_{11}	1	0	5	0	4.999	1.317E-03
	10	0	5	0	4.987	1.317E-03
	100	0	5	0	4.869	1.314E-03
	1K	0	5	0	3.710	1.290E-03
	10K	0	5	0	0.528	4.472E-04
	100K	0	5	0	0.052	4.947E-05
M_{11}	1	5	0	5	0.001	1.316E-03
	10	5	0	5	0.013	1.307E-03
	100	5	0	5	0.122	1.224E-03
	1K	5	0	5	0.781	7.814E-04
	10K	5	0	5	2.032	2.032E-04
	100K	5	0	5	2.816	2.816E-05
M_{11}	1	5	5	0	0.001	1.316E-03
	10	5	5	0	0.013	1.307E-03
	100	5	5	0	0.122	1.224E-03
	1K	5	5	0	0.781	7.814E-04
	10K	5	5	0	2.032	2.032E-04
	100K	5	5	0	2.816	2.816E-05
M_{11}	1	5	5	5	0.001	1.316E-03
	10	5	5	5	0.013	1.307E-03
	100	5	5	5	0.122	1.224E-03
	1K	5	5	5	0.781	7.814E-04
	10K	5	5	5	2.032	2.032E-04
	100K	5	5	5	2.816	2.816E-05

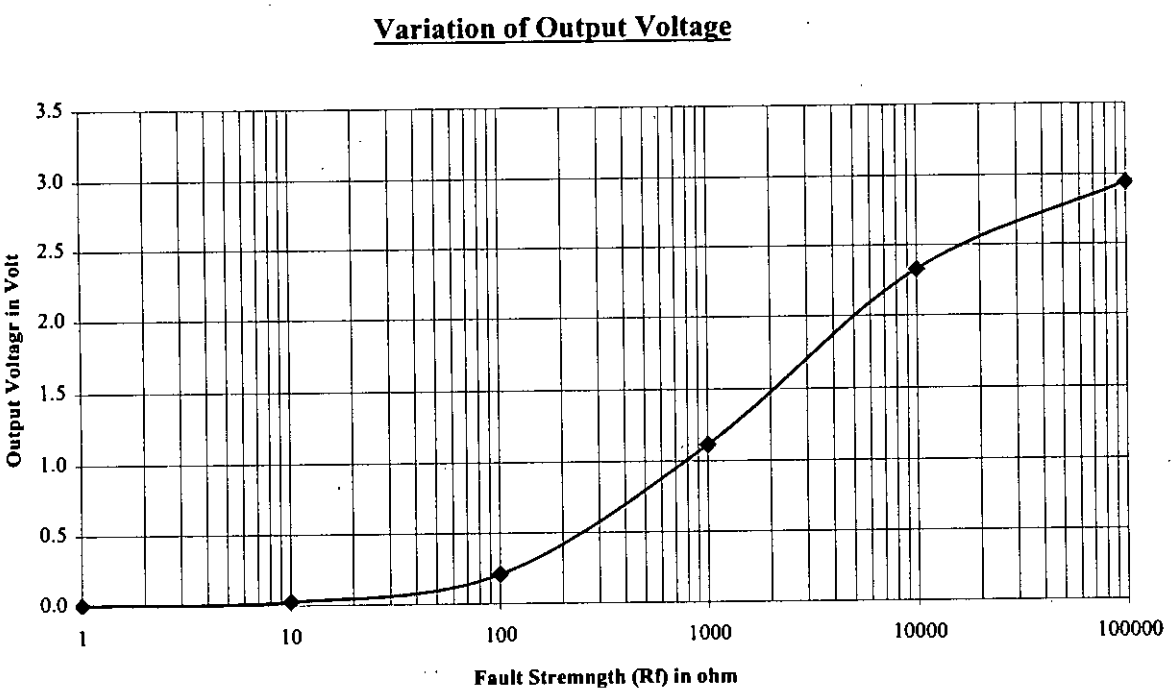


Fig 5.20: Output Voltage vs Fault Strength
(Bridging fault for M_1 (101), M_3 (110), (111) and M_5 (011))

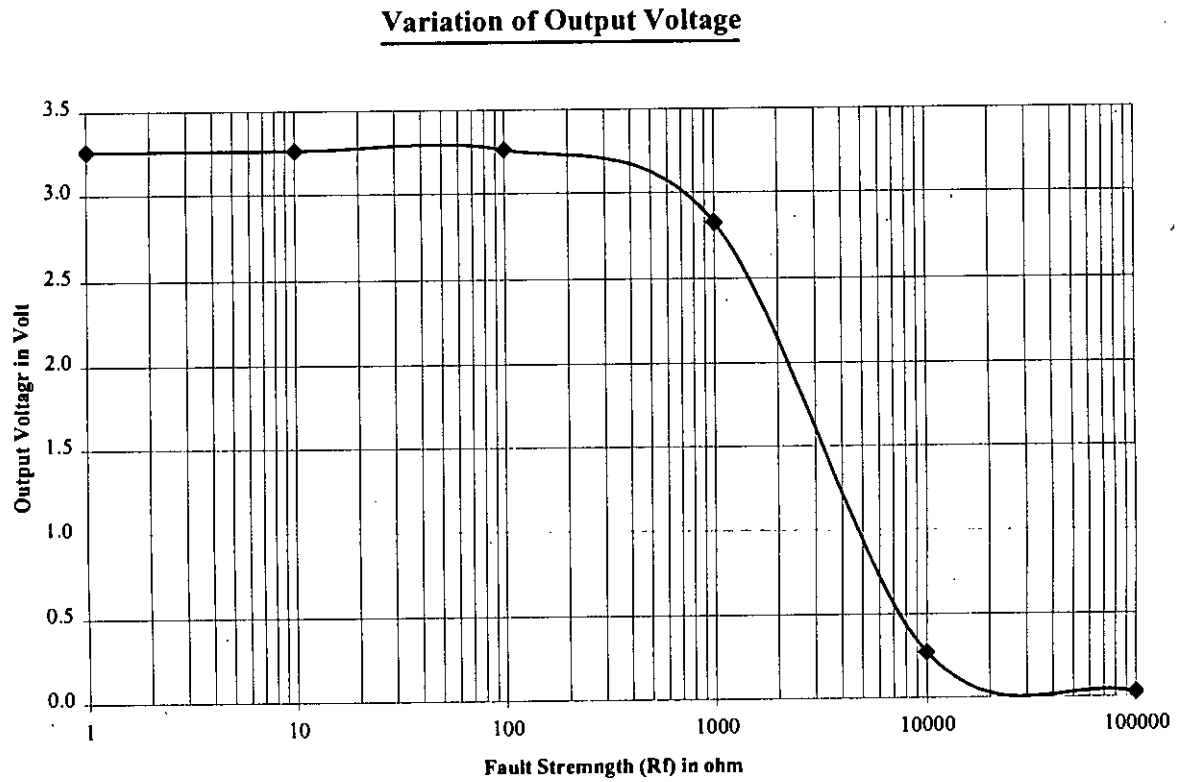


Fig 5.21: Output Voltage vs Fault Strength
(Bridging fault for M_3 (100), M_5 (000), (001) and M_7 (010))

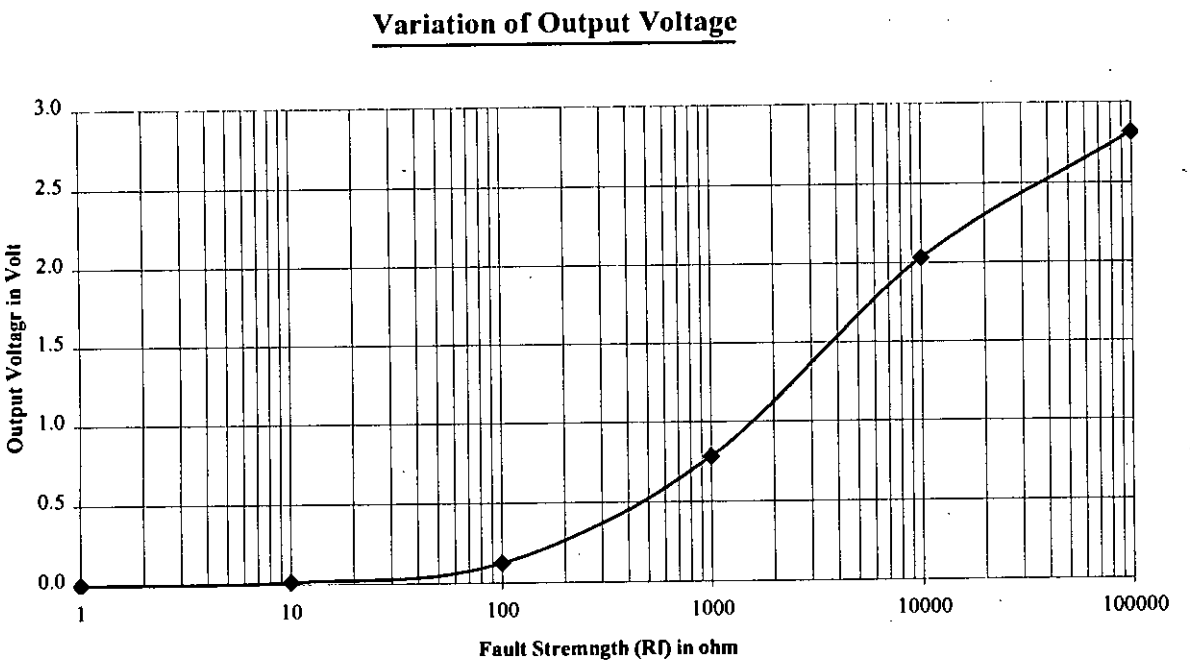


Fig 5.22: Output Voltage vs Fault Strength
(Bridging fault for M_9 (011), M_{11} (101), (110) and (111))

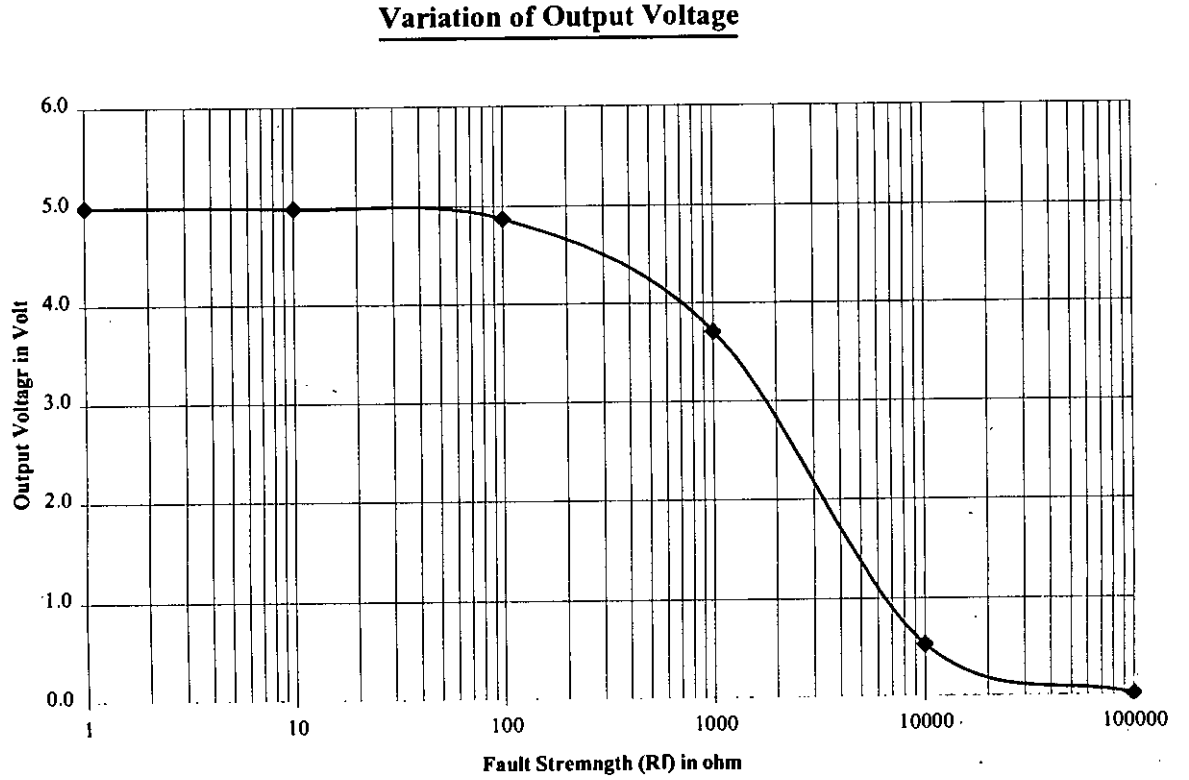


Fig 5.23: Output Voltage vs Fault Strength
(Bridging fault for M_9 (100), M_{11} (000), (001) and (010))

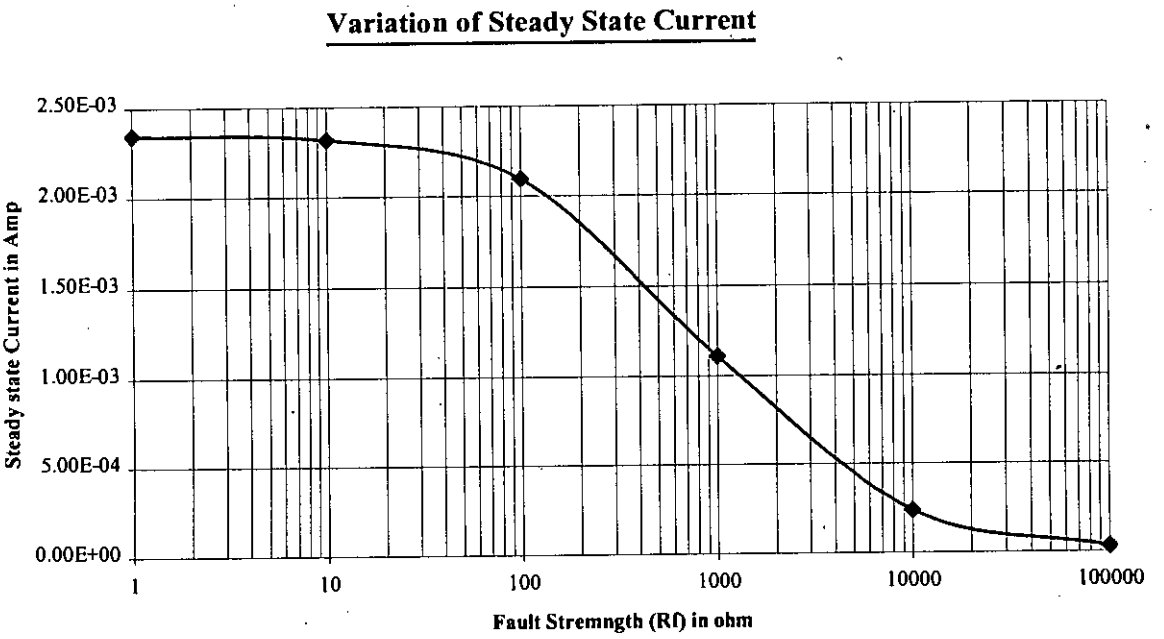


Fig 5.24: Steady State Current vs Fault Strength (Bridging fault for M_1 (101), M_3 (110), (111) and M_5 (011))

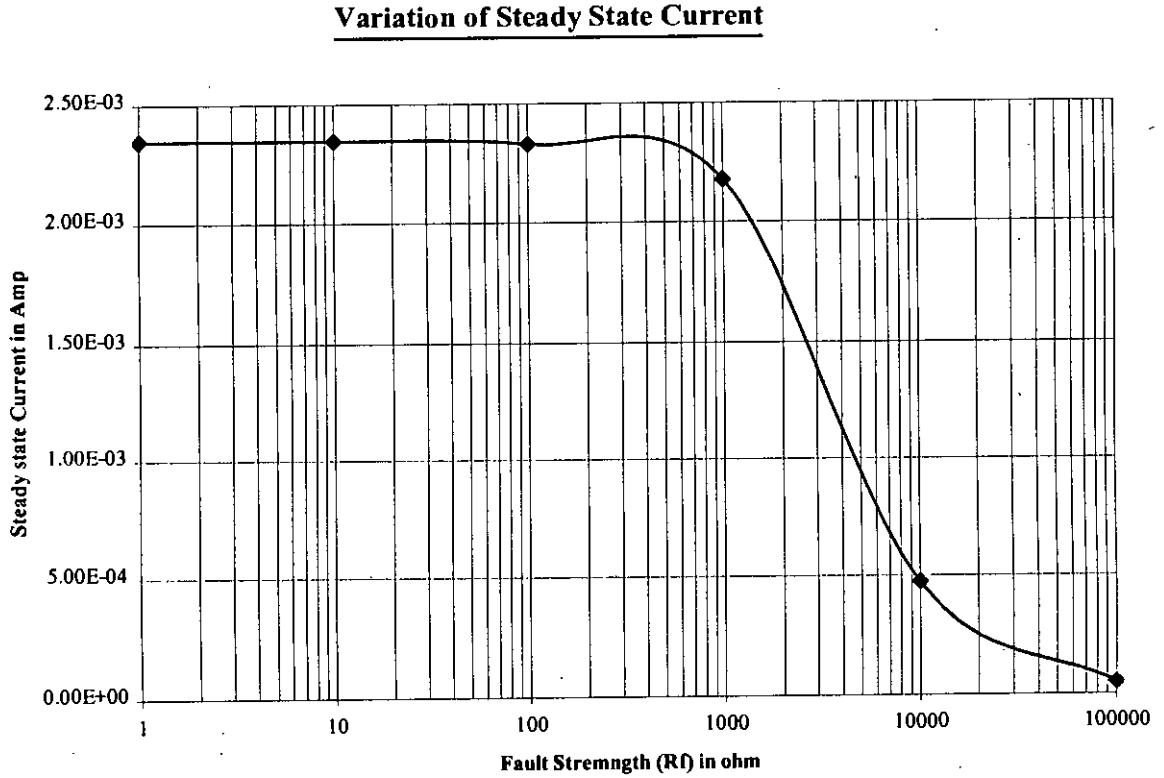


Fig 5.25: Steady State Current vs Fault Strength (Bridging fault for M_3 (100), M_5 (000), (001) and M_7 (010))

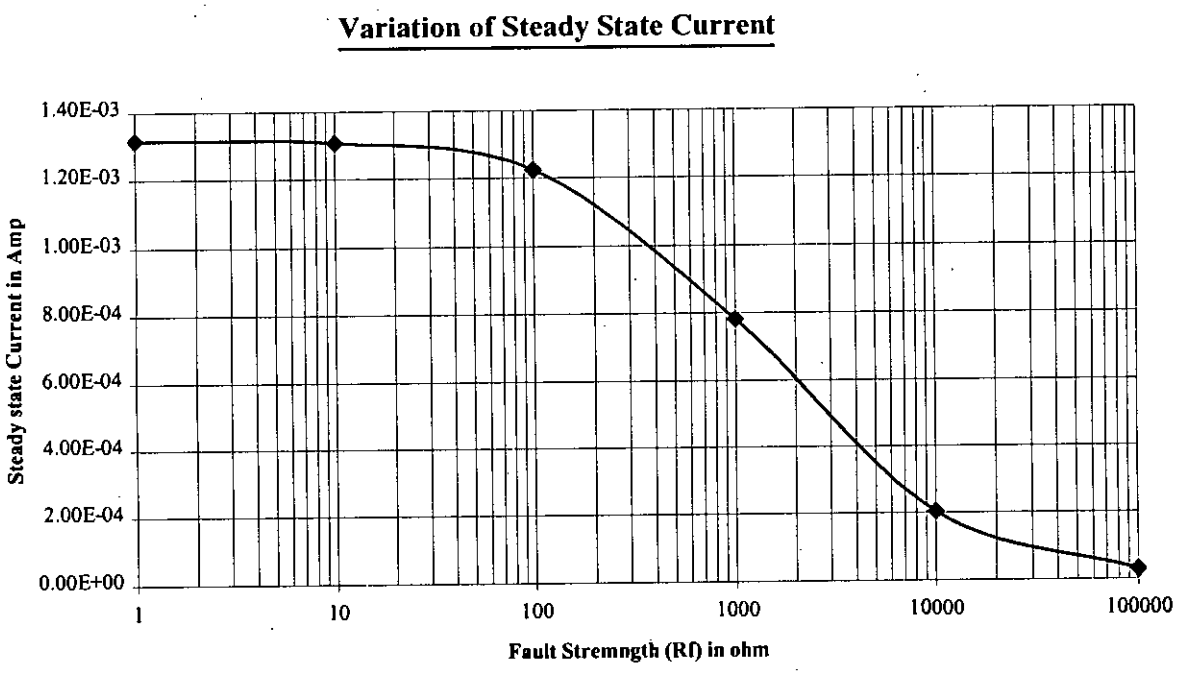


Fig 5.26: Steady State Current vs Fault Strength (Bridging fault for M_9 (011), M_{11} (101), (110) and (111))

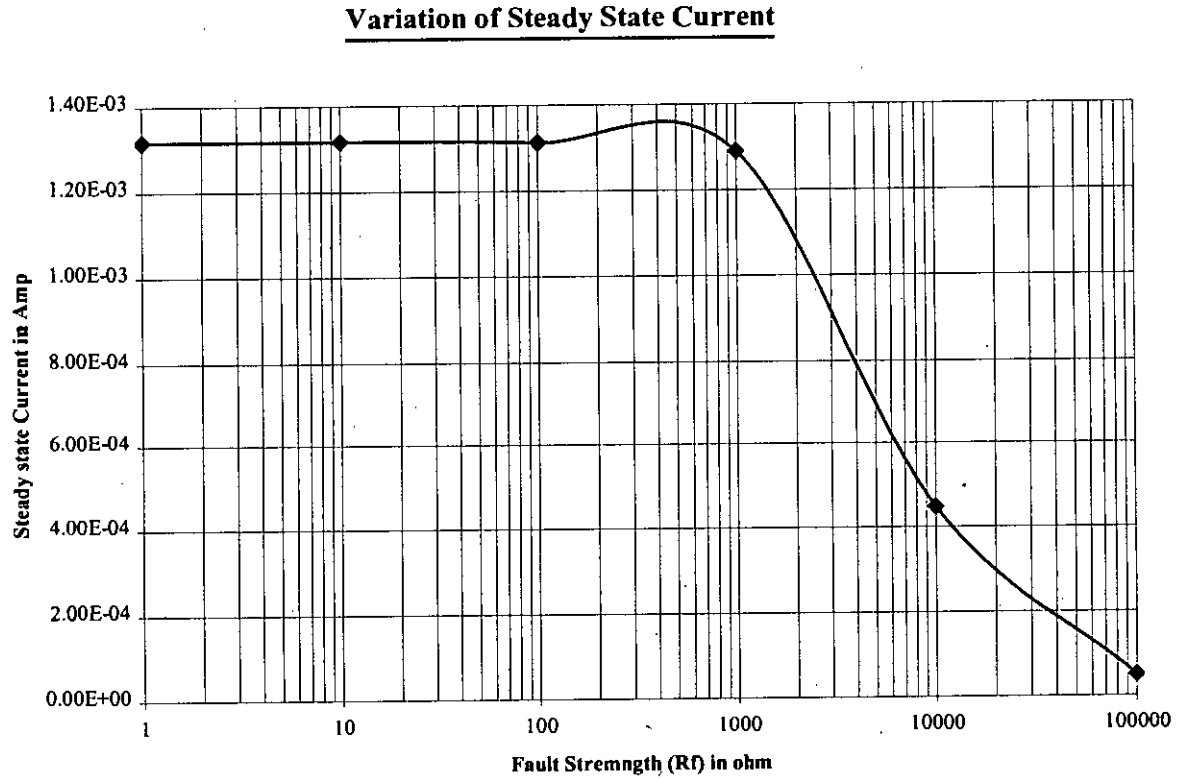


Fig 5.27: Steady State Current vs Fault Strength (Bridging fault for M_9 (100), M_{11} (000), (001) and (010))

Effects of Fault Resistance

From the results of Table 5.3, fig 5.20 - 5.23 shows, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 1 Ω to 100 kΩ, the output voltage varies from 0 to 4.999 Volt. This appreciable variation in output voltage clearly shows that the output logic level is indeterminable. This agrees with our prediction that the fault cannot be detected by logic monitoring. As seen from the table, fig 5.24 - 5.27, signal current is in the range of miliamperes compared to normal operating current of 0A. Therefore, the fault can be detected by current monitoring.

Table 5.4

The following table shows the summary of bridging faults in CPL Full Adder Carry circuit.

Summary for bridging faults in CPL Full Adder Carry Logic Circuit

Fault	Successful Test Vector	Output Logic Level (Volt)	I_{DDQ} (amp)	Logic Monitoring possible?	Current monitoring possible?
M_1	(001),(010) (011),(101)	0 to 3.265	2.943E-05 to 2.346E-03	No	Yes
M_3	(000),(100) (110),(111)	0 to 3.2667	2.943E-05 to 2.346 E-03	No	Yes
M_5	(000),(001) (011),(111)	0 to 3.2667	4.973E-05 to 2.630E-03	No	Yes
M_7	(010),(100) (101),(110)	0 to 3.2662	4.974E-05 to 2.630E-03	No	Yes
M_9	(011), (100)	0 to 4.999	1.316E-03 to 4.472E-05	No	Yes
M_{11}	(000),(001) (010),(101) (110),(111)	0 to 4.999	1.316E-03 to 4.472E-05	No	Yes

5.4 Behavior Under Single Stuck open faults

The behavior of CPL full adder carry circuits under single stuck open faults in MOS are analyzed in this section.

5.4.1 Qualitative Analysis

M_1 : (stuck open fault in M_1 of the CPL Full Adder Carry gate of fig 5.1)

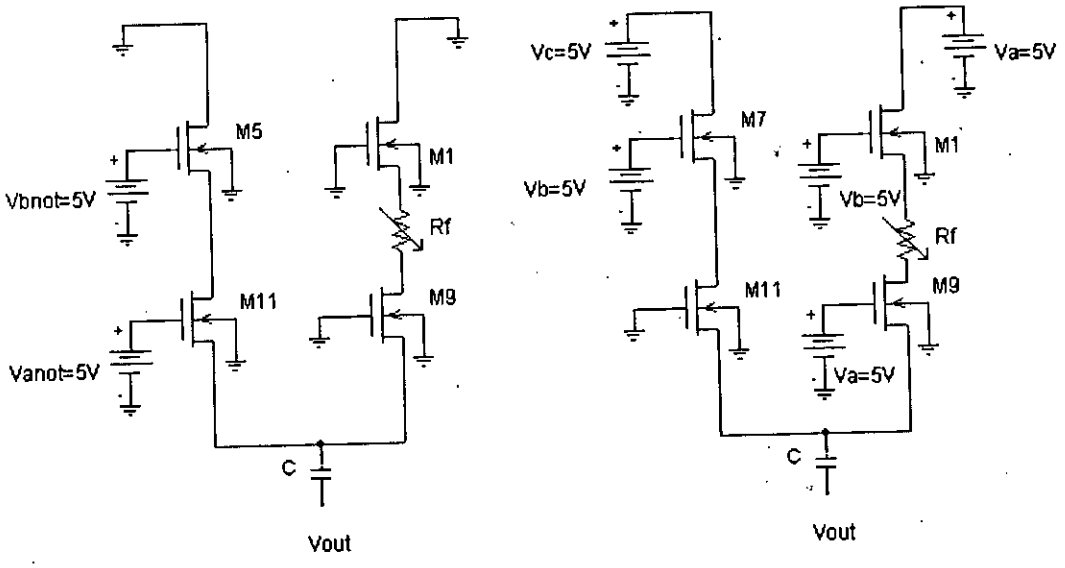
Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_1, a high resistance is inserted at the lower end of M_1 to isolate it from the rest of circuit. It is observed that when the vector (111) and (110) are applied - M_3, M_5, M_{11} turns off and M_1 remains off since it is stuck open. This conditions a non-conducting stage is produced in the full adder carry gate. Hence the (111) or (110) vector can be taken as a Test Vector for M_1 fault.

Test Vector (111):

In the unfaulted circuit, the (111) vector would produce a high output. Consequently, the vectors that produced a low output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vector (000) produces low output under both the above conditions and therefore can be considered as Initialization Vector. Applying the Initialization Vector first and then the Test Vector can detect the fault. This case is analyzed below.

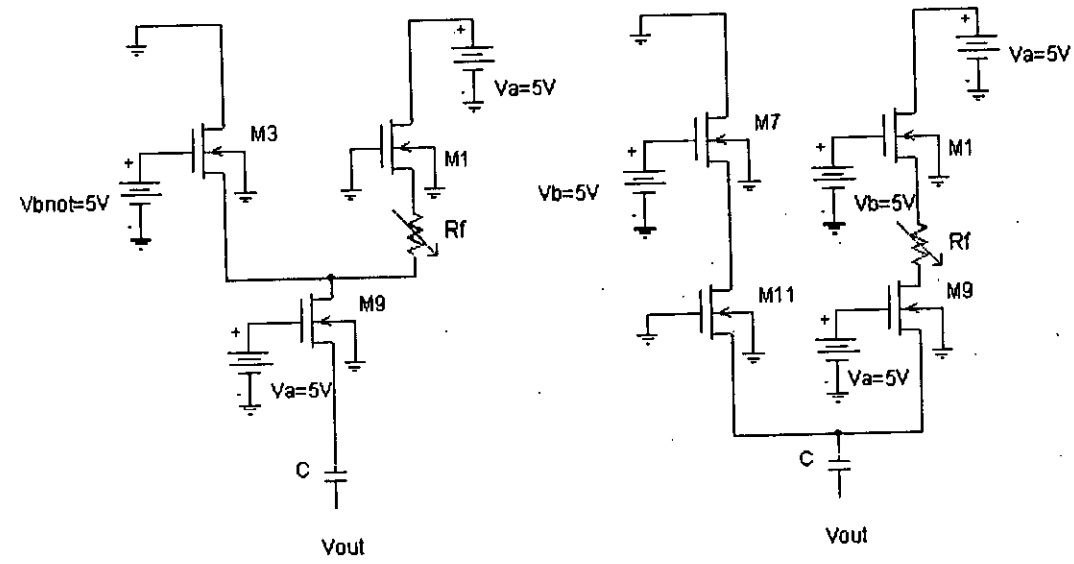
Initialization Vector (000), Test Vector (111):

When a capacitor is connected to the output terminal of the faulted gate of fig 5.28 and the vector (000) is applied, the output voltage is at 0 Volt. The Test Vector (111) is applied next, thus causing the output capacitance to be isolated from the circuit. Ideally the output capacitance retains its original state of 0 V. But practically, a current flows from the 5V power source through M_1 and the resistance R_f to charge the output capacitance to 5V. Also M_9 supplies a leakage current that charges C_{out}. These charging currents are very small since the large resistance R_f limits one and the other is only a leakage current. As a result, the time to charge the capacitance to 5V is longer than the time that would be required in an unfaulted gate. This delay in charging the output capacitance to 5 V is the fundamental criterion for faulted detection.



(a) (b)

Fig. 5.28. Equivalent circuit for stuck-open fault on MOS M_1 of CPL Full Adder CARRY circuit. (a) I.V.[000], (b) T.V.[111]



(a) (b)

Fig. 5.29. Equivalent circuit for stuck-open fault on MOS M_1 of CPL Full Adder CARRY circuit. (a) I.V.[100], (b) T.V.[110]

Test Vector (110):

In the unfaulted circuit, the (110) vector would produce a high output. Consequently, the vectors that produced a low output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vector (100) produces low outputs under both the above conditions and therefore can be considered as Initialization Vectors. Applying the Initialization Vector first and then the Test Vector can detect the fault. This case is analyzed below.

Initialization Vector (100), Test Vector (110):

When a capacitor is connected to the output terminal of the faulted gate of fig 5.29 and the vector (100) is applied, the output voltage is at 0 Volt. The Test Vector (110) is applied next, thus causing the output capacitance to be isolated from the circuit. Ideally the output capacitance retains its original state of 5 V. But practically, a current flows from the 5V power source through M_1 and the resistance R_f to charge the output capacitance to 5V. Also M_9 supplies a leakage current that charges C_{out}. These charging currents are very small since the large resistance R_f limits one and the other is only a leakage current. As a result, the time to charge the capacitance to 5V is longer than the time that would be required in an unfaulted gate. This delay in charging the output capacitance to 5 V is the fundamental criterion for faulted detection.

M_3 : (stuck open fault in M_3 of the CPL Full Adder Carry gate of fig 5.1)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_3, a high resistance is inserted at the lower end of M_3 to isolate it from the rest of circuit. It is observed that when the vector (100) and (101) are applied - M_1, M_7, M_{11} turns off and M_2 remains off since it is stuck open. This conditions a non-conducting stage is produced in the full adder carry gate. Hence the (100) or (101) vector can be taken as a Test Vector for M_3 fault.

Test Vector (100):

In the unfaulted circuit, the (100) vector would produce a low output. Consequently, the vectors that produced a high output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vectors (011), (101) (110), and (111) produce high outputs under both the above conditions and therefore can be considered

as Initialization Vectors. Applying the Initialization Vectors first and then the Test Vector can detect the fault. The analysis is same as previous case

Test Vector (101):

In the unfaulted circuit, the (101) vector would produce a high output. Consequently, the vectors that produced a low output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vector (100) produces low output under both the above conditions and therefore can be considered as Initialization Vector. Applying the Initialization Vector first and then the Test Vector can detect the fault. The analysis is same as previous case.

M_5 : (stuck open fault in M_5 of the CPL Full Adder Carry gate of fig 5.1)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_5, a high resistance is inserted at the lower end of M_5 to isolate it from the rest of circuit. It is observed that when the vector (000) and (001) are applied - M_1, M_7, M_9 turns off and M_2 remains off since it is stuck open. This conditions a non-conducting stage is produced in the full adder carry gate. Hence the (000) or (001) vector can be taken as a Test Vector for M_5 fault.

Test Vector (000):

In the unfaulted circuit, the (000) vector would produce a low output. Consequently, the vectors that produced a high output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vectors (101) and (111) produce high outputs under both the above conditions and therefore can be considered as Initialization Vectors. Applying the Initialization Vectors first and then the Test Vector can detect the fault. The analysis is same as the previous case.

Test Vector (001):

In the unfaulted circuit, the (001) vector would produce a low output. Consequently, the vectors that produced a high output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vectors (101), (110) and (111) produce high outputs under both the above conditions and therefore can be considered as Initialization Vectors. Applying the Initialization Vectors first and then the Test Vector can detect the fault. The analysis is same as in the previous case.

M_7 : (stuck open fault in M_7 of the CPL Full Adder Carry gate of fig 5.1)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_7, a high resistance is inserted at the lower end of M_7 to isolate it from the rest of circuit. It is observed that when the vector (010) and (011) are applied - M_3, M_5, M_9 turns off and M_7 remains off since it is stuck open. This conditions a non-conducting stage is produced in the full adder carry gate. Hence the (010) and (011) vectors can be taken as a Test Vector for M_7 fault.

Test Vector (011):

In the unfaulted circuit, the (011) vector would produce a high output. Consequently, the vectors that produced a low output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vector (100) produces low output under both the above conditions and therefore can be considered as Initialization Vector. Applying the Initialization Vector first and then the Test Vector can detect the fault. The analysis is similar to the previous case.

Test Vector (010):

In the unfaulted circuit, the (010) vector would produce a low output. Consequently, the vectors that produced a high output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vector (110) produces high output under both the above conditions and therefore can be considered as Initialization Vectors. Applying the Initialization Vector first and then the Test Vector can detect the fault. The analysis is similar to the previous case.

M_9 : (stuck open fault in M_9 of the CPL Full Adder Carry gate of fig 5.1)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_9, a high resistance is inserted at the lower end of M_9 to isolate it from the rest of circuit. It is observed that when the vector (100) and (101) are applied M_1, M_7, M_{11} turns off and M_9 remains off since it is stuck open. This conditions a non-conducting stage is produced in the full adder carry gate. Hence the (100) and (101) vectors can be taken as a Test Vector for M_9 fault.

Test Vector (100):

In the unfaulted circuit, the (100) vector would produce a low output. Consequently, the vectors that produced a high output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vector (011) produces high output

under both the above conditions and therefore can be considered as Initialization Vector. Applying the Initialization Vector first and then the Test Vector can detect the fault.

Test Vector (101):

In the unfaulted circuit, the (101) vector would produce a high output. Consequently, the vectors that produced a low output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vectors (000), (001), and (010) produce low output under both the above conditions and therefore can be considered as Initialization Vector. Applying the Initialization Vector first and then the Test Vector can detect the fault.

M_{11} : (stuck open fault in M_{11} of the CPL Full Adder Carry gate of fig 5.1)

Two pattern test is utilized to detect the fault. In order to model stuck open fault at M_{11}, a high resistance is inserted at the lower end of M_{11} to isolate it from the rest of circuit. It is observed that when the vector (010) and (011) are applied M_3, M_5, M_9 turn off and M_{11} remains off since it is stuck open. This conditions a non-conducting stage is produced in the full adder carry gate. Hence the (010) and (011) vectors can be taken as a Test Vector for M_{11} fault.

Test Vector (010):

In the unfaulted circuit, the (010) vector would produce a low output. Consequently, the vectors that produced a high output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vectors (101), (110) and (111) produce high output under both the above conditions and therefore can be considered as Initialization Vector. Applying the Initialization Vector first and then the Test Vector can detect the fault.

Test Vector (011):

In the unfaulted circuit, the (011) vector would produce a high output. Consequently, the vectors that produced a low output under faulted and unfaulted conditions are the Initialization Vectors for the two pattern test. Vector (100) produces low output under both the above conditions and therefore can be considered as Initialization Vector. Applying the Initialization Vector first and then the Test Vector can detect the fault.

5.4.2 SPICE Simulation Results

This section summarizes the SPICE simulation results for a single stuck open fault in the MOS devices of the CPL Full Adder Carry circuit.

Table: 5.5

SPICE Simulation result for stuck open fault in CPL Full Adder Carry.

Effect of Fault Strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_1	50 M	1	000	111	0	0
		10	000	111	0	9.027E-14
		100	000	111	0	5.799E-11
	100 M	1	000	111	0	0
		10	000	111	0	9.027E-14
		100	000	111	0	5.799E-11
	200 M	1	000	111	0	0
		10	000	111	0	9.027E-14
		100	000	111	0	5.799E-11
M_1	50 M	1	100	110	0	0
		10	100	110	0	1.893E-14
		100	100	110	3.231	1.559E-14
	100 M	1	100	110	0	0
		10	100	110	0	1.893E-14
		100	100	110	1.074	1.507E-16
	200 M	1	100	110	0	0
		10	100	110	0	1.893E-14
		100	100	110	0.049	1.783E-15
M_3	50 M	1	011	100	3.267	0
		10	011	100	3.267	6.058E-14
		100	011	100	2.870	1.922E-08
	100 M	1	011	100	3.267	0
		10	011	100	3.267	6.058E-14
		100	011	100	2.945	1.413E-07
	200 M	1	011	100	3.267	0
		10	011	100	3.267	6.058E-14
		100	011	100	3.004	2.355E-08
M_3	50 M	1	101	100	3.267	1.992E-11
		10	101	100	3.267	1.992E-11
		100	101	100	2.822	1.956E-08
	100 M	1	101	100	3.267	1.985E-11
		10	101	100	3.267	1.985E-11
		100	101	100	3.097	1.459E-07

Table: 5.5
SPICE Simulation result for stuck open fault in CPL Full Adder Carry. Effect of Fault Strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_3	200 M	1	101	100	3.264	1.985E-11
		10	101	100	3.120	1.985E-11
		100	101	100	3.097	2.435E-08
M_3	50 M	1	110	100	3.267	2.643E-11
		10	110	100	3.267	2.643E-11
		100	110	100	2.892	1.916E-08
	100 M	1	110	100	3.267	2.640E-11
		10	110	100	3.267	2.640E-11
		100	110	100	3.097	1.455E-07
	200 M	1	110	100	3.267	2.640E-11
		10	110	100	3.267	2.640E-11
		100	110	100	3.120	2.439E-08
M_3	50 M	1	111	100	3.267	2.643E-11
		10	111	100	3.267	2.643E-11
		100	111	100	2.802	1.963E-08
	100 M	1	111	100	3.267	2.640E-11
		10	111	100	3.267	2.640E-11
		100	111	100	3.098	1.459E-07
	200 M	1	111	100	3.267	2.640E-11
		10	111	100	3.267	2.641E-11
		100	111	100	3.178	2.436E-08
M_3	50 M	1	100	101	0	1.992E-11
		10	100	101	0	1.992E-11
		100	100	101	1.23	1.901E-08
	100 M	1	100	101	0	1.985E-11
		10	100	101	0	1.985E-11
		100	100	101	0.136	1.447E-07
	200 M	1	100	101	0	1.985E-11
		10	100	101	0	1.985E-11
		100	100	101	0	1.942E-08
M_5	50 M	1	101	000	3.267	1.990E-11
		10	101	000	3.267	1.989E-11
		100	101	000	2.939	5.878E-08
	100 M	1	101	000	3.267	1.985E-11
		10	101	000	3.267	1.984E-11
		100	101	000	3.098	3.098E-08
	200 M	1	101	000	3.267	1.985E-11
		10	101	000	3.267	1.984E-11
		100	101	000	3.181	1.591E-08

Table: 5.5
SPICE Simulation result for stuck open fault in CPL Full Adder Carry. Effect of Fault Strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_5	50 M	1	111	000	3.267	2.643E-11
		10	111	000	3.267	2.642E-11
		100	111	000	3.294	5.878E-08
	100 M	1	111	000	3.267	2.641E-11
		10	111	000	3.267	2.640E-11
		100	111	000	3.098	3.098E-08
	200 M	1	111	000	3.267	2.640E-11
		10	111	000	3.267	2.640E-11
		100	111	000	3.181	1.590E-08
M_5	50 M	1	101	001	3.267	1.990E-11
		10	101	001	3.267	1.989E-11
		100	101	001	2.939	5.878E-08
	100M	1	101	001	3.267	1.985E-11
		10	101	001	3.267	1.984E-11
		100	101	001	3.098	3.098E-08
	200 M	1	101	001	3.267	1.985E-11
		10	101	001	3.267	1.984E-11
		100	101	001	3.163	1.581E-08
M_5	50 M	1	110	001	3.267	2.643E-11
		10	110	001	3.267	2.642E-11
		100	110	001	2.850	5.699E-08
	100 M	1	110	001	3.267	2.641E-11
		10	110	001	3.267	2.640E-11
		100	110	001	3.004	3.003E-08
	200 M	1	110	001	3.267	2.640E-11
		10	110	001	3.267	2.640E-11
		100	110	001	3.084	1.542E-08
M_5	50 M	1	111	001	3.267	2.643E-11
		10	111	001	3.267	2.642E-11
		100	111	001	2.939	5.699E-08
	100 M	1	111	001	3.267	2.641E-11
		10	111	001	3.267	2.640E-11
		100	111	001	3.098	3.098E-08
	200 M	1	111	001	3.267	2.640E-11
		10	111	001	3.267	2.640E-11
		100	111	001	3.181	1.591E-08

Table: 5.5

SPICE Simulation result for stuck open fault in CPL Full Adder Carry.

Effect of Fault Strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_7	50 M	1	100	011	0	1.992E-11
		10	100	011	0	1.990E-11
		100	100	011	0	2.587E-12
	100 M	1	100	011	0	1.986E-11
		10	100	011	0	1.984E-11
		100	100	011	0	2.587E-12
	200 M	1	100	011	0	1.985E-11
		10	100	011	0	1.983E-11
		100	100	011	0	2.587E-12
M_7	50 M	1	110	010	3.267	2.643E-11
		10	110	010	3.267	2.642E-11
		100	110	010	2.850	5.699E-08
	100 M	1	110	010	3.267	2.641E-11
		10	110	010	3.267	2.640E-11
		100	110	010	3.004	3.003E-08
	200 M	1	110	010	3.267	2.640E-11
		10	110	010	3.267	2.640E-11
		100	110	010	3.084	1.542E-08
M_9	50 M	1	011	100	3.267	2.643E-11
		10	011	100	3.267	2.642E-11
		100	011	100	2.850	5.699E-08
	100 M	1	011	100	3.267	2.641E-11
		10	011	100	3.267	2.640E-11
		100	011	100	3.004	3.003E-08
	200 M	1	011	100	3.267	2.640E-11
		10	011	100	3.267	2.640E-11
		100	011	100	3.084	1.542E-08
M_9	50 M	1	000	101	0	1.992E-11
		10	000	101	0	1.990E-11
		100	000	101	0	2.587E-12
	100M	1	000	101	0	1.986E-11
		10	000	101	0	1.984E-11
		100	000	101	0	2.587E-12
	200 M	1	000	101	0	1.985E-11
		10	000	101	0	1.983E-11
		100	000	101	0	2.587E-12

Table: 5.5
SPICE Simulation result for stuck open fault in CPL Full Adder Carry.
Effect of Fault Strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_9	50 M	1	001	101	0	1.992E-11
		10	001	101	0	1.990E-11
		100	001	101	0	2.587E-12
	100 M	1	001	101	0	1.986E-11
		10	001	101	0	1.984E-11
		100	001	101	0	2.587E-12
	200 M	1	001	101	0	1.985E-11
		10	001	101	0	1.983E-11
		100	001	101	0	2.587E-12
M_9	50 M	1	010	101	0	1.992E-11
		10	010	101	0	1.990E-11
		100	010	101	0	2.587E-12
	100 M	1	010	101	0	1.986E-11
		10	010	101	0	1.984E-11
		100	010	101	0	2.587E-12
	200 M	1	010	101	0	1.985E-11
		10	010	101	0	1.983E-11
		100	010	101	0	2.587E-12
M_{11}	50 M	1	101	010	3.267	2.643E-11
		10	101	010	3.267	2.642E-11
		100	101	010	2.850	5.699E-08
	100M	1	101	010	3.267	2.641E-11
		10	101	010	3.267	2.640E-11
		100	101	010	3.004	3.003E-08
	200 M	1	101	010	3.267	2.640E-11
		10	101	010	3.267	2.640E-11
		100	101	010	3.084	1.542E-08
M_{11}	50 M	1	110	010	3.267	2.643E-11
		10	110	010	3.267	2.642E-11
		100	110	010	2.850	5.699E-08
	100 M	1	110	010	3.267	2.641E-11
		10	110	010	3.267	2.640E-11
		100	110	010	3.004	3.003E-08
	200 M	1	110	010	3.267	2.640E-11
		10	110	010	3.267	2.640E-11
		100	110	010	3.084	1.542E-08

Table: 5.5

SPICE Simulation result for stuck open fault in CPL Full Adder Carry.

Effect of Fault Strength

Stuck open MOS transistor	Fault Resistance R_f (Ω)	Time Interval	Sensitizing vector (V_a V_b V_c)		V_{out} (Volt)	Steady state current I_{DDQ} (amp)
			Initial Vector	Test Vector		
M_{11}	50 M	1	111	010	3.267	2.643E-11
		10	111	010	3.267	2.642E-11
		100	111	010	2.850	5.699E-08
	100 M	1	111	010	3.267	2.641E-11
		10	111	010	3.267	2.640E-11
		100	111	010	3.004	3.003E-08
	200 M	1	111	010	3.267	2.640E-11
		10	111	010	3.267	2.640E-11
		100	111	010	3.084	1.542E-08
M_{11}	50 M	1	100	011	0	1.992E-11
		10	100	011	0	1.990E-11
		100	100	011	0	2.587E-12
	100 M	1	100	011	0	1.986E-11
		10	100	011	0	1.984E-11
		100	100	011	0	2.587E-12
	200 M	1	100	011	0	1.985E-11
		10	100	011	0	1.983E-11
		100	100	011	0	2.587E-12

In this section M_1, M_3, M_5 , M_7, M_9 and M_{11} are simulated. The simulations of other MOS (M_2, M_4, M_6, M_8, M_{10} and M_{12}) are similar to the above.

Effects of Fault Resistance and Time Interval

As seen from table 5.5, the effect of fault resistance on output voltage is very prominent. As fault resistance varies from 50 MΩ to 200 MΩ, the output voltage and Steady state current has a little effect. The time interval has a great effect on the output voltage. Since Steady state current do not increase very high the current monitoring is not possible to determine the stuck open fault. But if we take lower time interval the output voltage variation gives us the fault detection.

Table 5.6

The following table shows the summary of stuck open faults in CPL Full Adder Carry circuit.

Summery for Stuck open faults in CPL Full Adder Carry Logic Circuit

Fault	Successful Two Pattern Vectors	O/P Logic Level Un-faulted	O/P Logic Level Faulted	I_{DDQ} (amp)	Logic monitoring possible?	Current monitoring possible?
M_1	(000,111)	0,1	0,0	5.799E-11	Yes	No
	(100,110)	0,1	0,0	1.559E-14	Yes	No
M_3	(011,100)	1,0	1,1	1.992E-08	Yes	No
	(101,100)	1,0	1,1	1.992E-08	Yes	No
	(110,100)	1,0	1,1	1.916E-08	Yes	No
	(111,100)	1,0	1,1	1.963E-08	Yes	No
	(100,101)	0,1	0,0	1.901E-08	Yes	No
M_5	(101,000)	1,0	1,1	5.878E-08	Yes	No
	(111,000)	1,0	1,1	5.878E-08	Yes	No
	(101,001)	1,0	1,1	5.878E-08	Yes	No
	(110,001)	1,0	1,1	5.699E-08	Yes	No
	(111,001)	1,0	1,1	5.699E-08	Yes	No
M_7	(100,011)	0,1	0,0	2.527E-12	Yes	No
	(110,010)	0,1	0,0	1.403E-13	Yes	No
M_9	(011,100)	1,0	1,1	5.699E-08	Yes	No
	(000,101)	0,1	0,0	1.992E-11	Yes	No
	(001,101)	0,1	0,0	1.992E-11	Yes	No
	(010,100)	0,1	0,0	1.992E-11	Yes	No
M_{11}	(101,010)	1,0	1,1	5.699E-08	Yes	No
	(110,010)	1,0	1,1	5.699E-08	Yes	No
	(111,010)	1,0	1,1	5.699E-08	Yes	No

5.5 Discussion

It is found that stuck-on fault on all the MOS transistor of the CARRY logic circuit can be detected by steady state current monitoring with appropriate test vectors. For some of these test vectors the fault can also be detected by logic monitoring, but in all cases this is also accompanied by a large flow of signal source current. Similarly all bridging fault can be detected by current monitoring, but no logic monitoring is possible. Stuck open fault on all the MOS transistors on the CARRY logic circuit can be detected by appropriate two pattern test. Finally it is concluded that signal source current monitoring (I_{DDQ} testing) is the best method for fault detection in CPL circuits and gives a very wide range of fault coverage.

Table 5.6

The following table shows the summary of various faults in CPL Full Adder Sum circuit.

Summary of Fault Detection of CPL Full Adder Carry Circuit

Transistor	Stuck-on Fault	Bridging Fault (G-S)	Stuck-open Fault
	Detected by	Detected by	Detected by
M_1	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
M_3	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
M_5	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
M_7	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
M_9	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
M_{11}	I_{DDQ} testing	I_{DDQ} testing	Two pattern test
Fault coverage	100% by I_{DDQ} testing	100% by I_{DDQ} testing	100% by Two pattern test

CHAPTER 6

DESIGN FOR TESTABILITY

6.1 Introduction:

The high-performance integrated circuits to day contain millions of transistor on a single chip [30]. It makes the testing difficult and time consuming. It has been predicted that testability will soon become the main design criterion for VLSI circuits. The alternative is to save area by ignoring testability, but the penalties are such that even for modest complexity (e.g. 10, 000 gates per chip) the test cost could rise by a factor of five to ten, compared with the same system designed for testability. Given the test is already a significant component of VLSI chip costs, the effects will be quite dramatic and could well cause the test costs to exceed all other production cost by a significant factor. It is therefore essential to adapt a Design-for-Testability approach in designing such complex integrated circuit in order to facilitate testing and save cost.

The commonly used design for testability approach may be categorized as follows [31-33]

(1) **ad-hoc testing** : ad-hoc testing are collection of ideas aimed at reducing the combinational explosion of testing. Common techniques involves

- Partitioning large sequential circuits,
- Adding test point,
- Adding multiplexers,
- Providing for easy state reset.

In general, ad-hoc testing techniques represent a bag of tricks developed over the years by designers to avoid the overhead of a systematic approach to testing. While these general approaches are still quite valid, process densities and chip complexities necessitate a structured approach to testing.

(2) **Scan-based approach**: The major difficulty in sequential circuit testing is in determining the internal state of the circuit. Scan design techniques are directed at improving the controllability and observability of the internal states by enabling all storage nodes to be controlled/observed via serial scan path. The insertion of very long scan path around the chip and their special interface circuitry causes hardware overhead.

(3) **Self-test and Built-in Self Test (BIST) :**

Self-test circuit are based on error-detecting codes. The general structure of a self-test circuit is shown in Fig. 6.2. It consists of a functional circuit and a checker. The inputs and the outputs of the functional circuit are encoded using a suitable code. The set of input and output vectors are each divided into two disjoint subsets

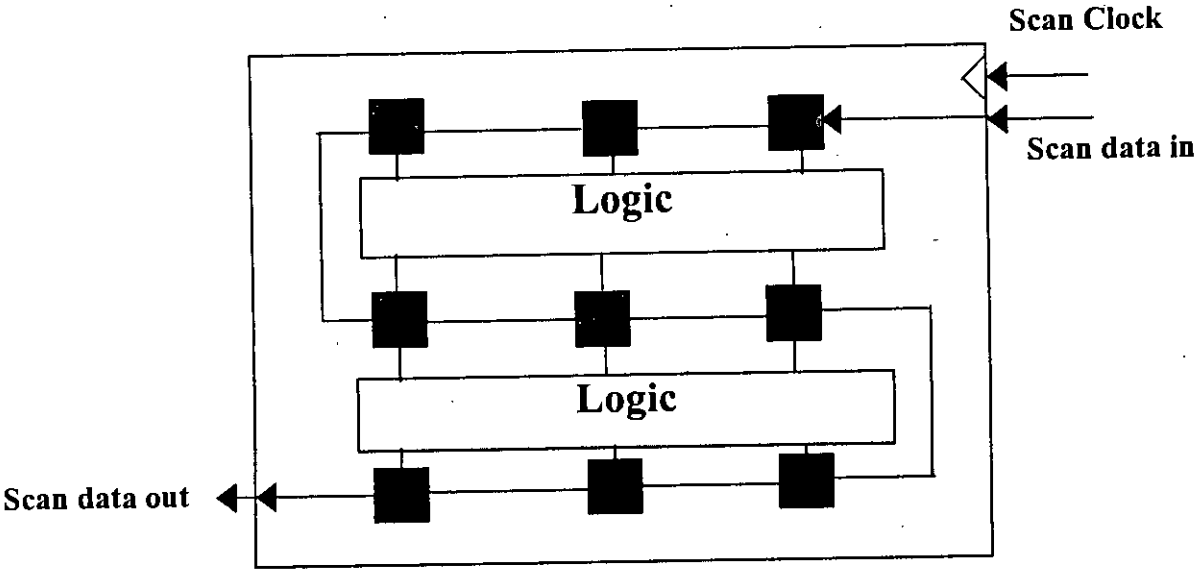


Fig. 6.1 Scan path testing.

one consisting of codewords or code space and the other consisting of non-codeword or non-code space. Under normal fault free operation the functional circuit receives a codeword from its input code space and produce a code word from its output code space. The checker checks to see if the functional circuit has produced a codeword. If a non-codeword is produced then the checker gives an error indication at its outputs.

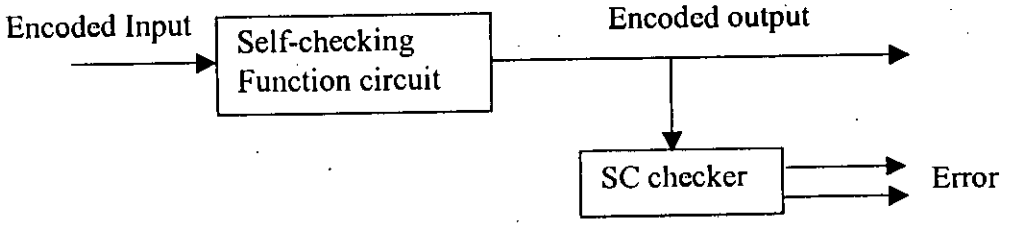


Fig. 6.2 General structure of a self-test circuit.

BIST techniques aim to effectively integrate an automatic test system into the chip design. Data compression system are currently used in BIST system and consists of making comparison on compacted test response instead of on the entire test data, which can be huge in some case. The test compaction scheme currently used most is called signature analysis. The signature of the device under test (DUT) is compared with the expected signature to determine if the DUT is fault-free. The difference between the faulty signature and a good signature may also be used to indicate the nature of the fault.

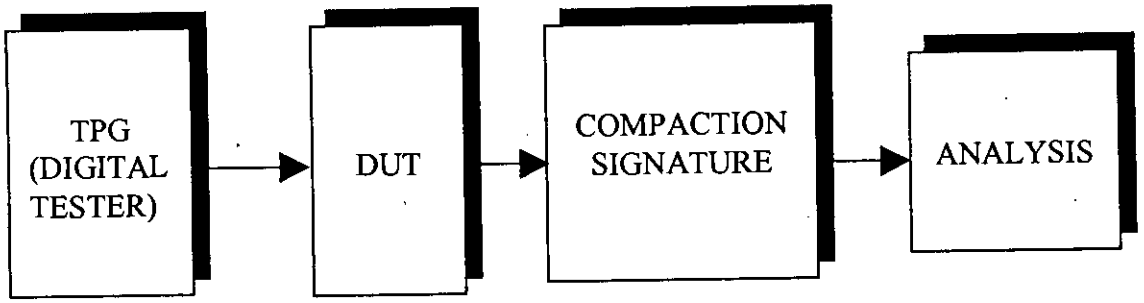


Fig. 6.3 Built-in-self-test signature analysis

Recently another approach, known as I_{DDQ} testing, has attained considerable attention and found to be very effective in CMOS IC testing [34]. The I_{DDQ} method uses steady-state supply current measurement to detect physical defects in CMOS circuits. It contributes significantly to improve circuit reliability and product quality [35, 36] and several integrated circuit (IC) manufacturer have adopted it [36-40]. In fact for CMOS circuit off-chip current testing has had enormous success in delivering high

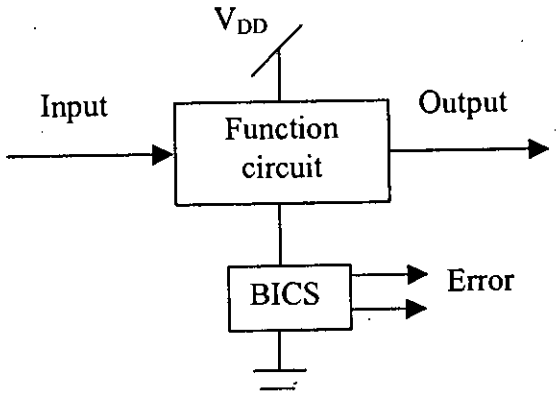


Fig. 6.4. Current monitoring online-testing configuration.

testing quality [41]. In the future, current testing will continue to be the most important part of production testing of deep-submicron VLSI chips. We will need to move from off-chip to on-chip current testing using Built-In-Current-Sensor (BICS)s. Figure 6.4 shows a configuration in which the BICS monitor the function circuit.

6.2 Designing CPL circuits for testability

The qualitative analysis and simulation results presented in chapter 3, 4 and 5 shows that for CPL basic circuits steady state supply current (I_{DDQ}) testing gives fault coverage of more than 94% for stuck-on and bridging fault. For stuck-on fault on CPL full adder circuit, the I_{DDQ} testing gives a fault coverage of 100% for both the SUM logic circuit and the CARRY logic circuit. This gives us a tremendous opportunity to use I_{DDQ} testing for fault monitoring in CPL circuits. In fact the above result shows that I_{DDQ} testing based technique is the most natural choice for adapting design for testability approach in CPL. In this thesis we have investigated several techniques to implement I_{DDQ} testing in CPL circuits.

6.2.1 Fault detection by off-chip current monitoring

For both on-chip and off-chip current testing, first the upper limit of device complexity for which current testing is applicable has to be determined. As seen from the result presented in chapter 3, the smallest increase in power supply current occurs for bridging fault. In this case, the output current under faulted condition is 0.158 mA whereas normal operating current is maximum 100 pA. The ratio of this fault current to normal operating current is $1.5X10^6$. If we consider a safety factor of 100, then for every 15000 basic CPL circuit, a current monitoring unit is required. To facilitate this the main power supply rail is divided into multiple rail each supply current to approximately 15000 basic CPL gates. One current monitoring circuit will be required for each of the VDD rail.

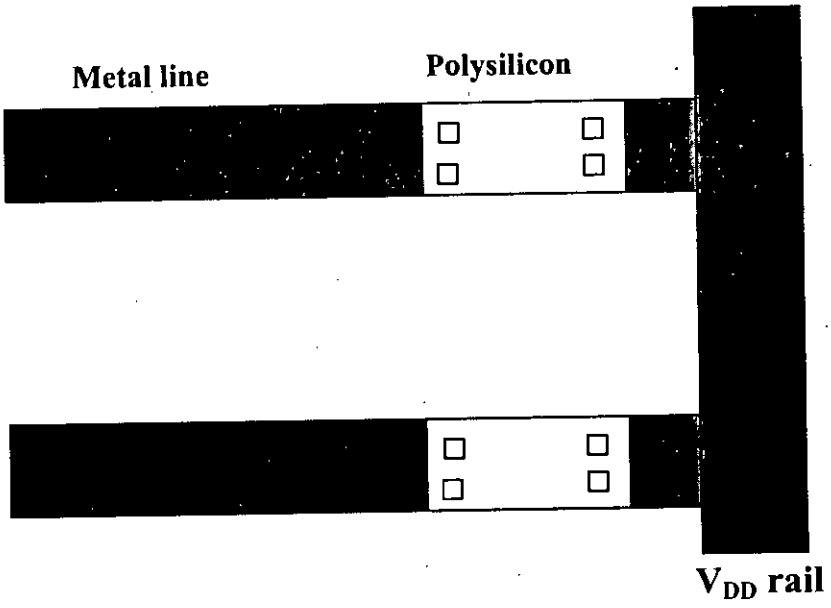


Fig. 6.5 : Layout technique for power supply routing and insertion of polysilcion resistor for off-chip I_{DDQ} testing.

For off-chip fault detection, we propose the following circuit. A small polysilicon resistor is inserted into the power rail. The resistivity of polysilicon resistor in a typical 0.25 μm process is 20 Ω/□. Therefore if we insert a polysilicon resistor of one square then the resistance of the layer is 20 Ω. The maximum normal operating current flowing through 15000 basic CPL circuit is 15000X100 pA i.e. 1.5 μA. Hence the voltage drop across the polysilicon resitor under normal operating condition is 30 μV. However for a single stuck-on or bridging fault the steady state current due to fault could be from 0.15 mA to 3.0 mA. Hence the voltage on the polysilicon resistor could vary from 3 mV to 60 mV. Hence voltage drop on polysilicon resistor on faulted condition is significantly larger than the voltage drop under normal operating condition. In off-chip fault detection scheme, the chip has a test pin on the end of the polysilicon resistor. For polysilicon metal contact, instead of a big contact, multiple contact cuts have used to reduce the effect of the variation of the contact resistance. The effect of process variations on the polysilicon resistors can be minimized by making the polysilicon squares large in area, of identical dimensions and by placing them close to each other.

The following test circuit can now be built off-chip for on line monitoring of fault on the target chip.

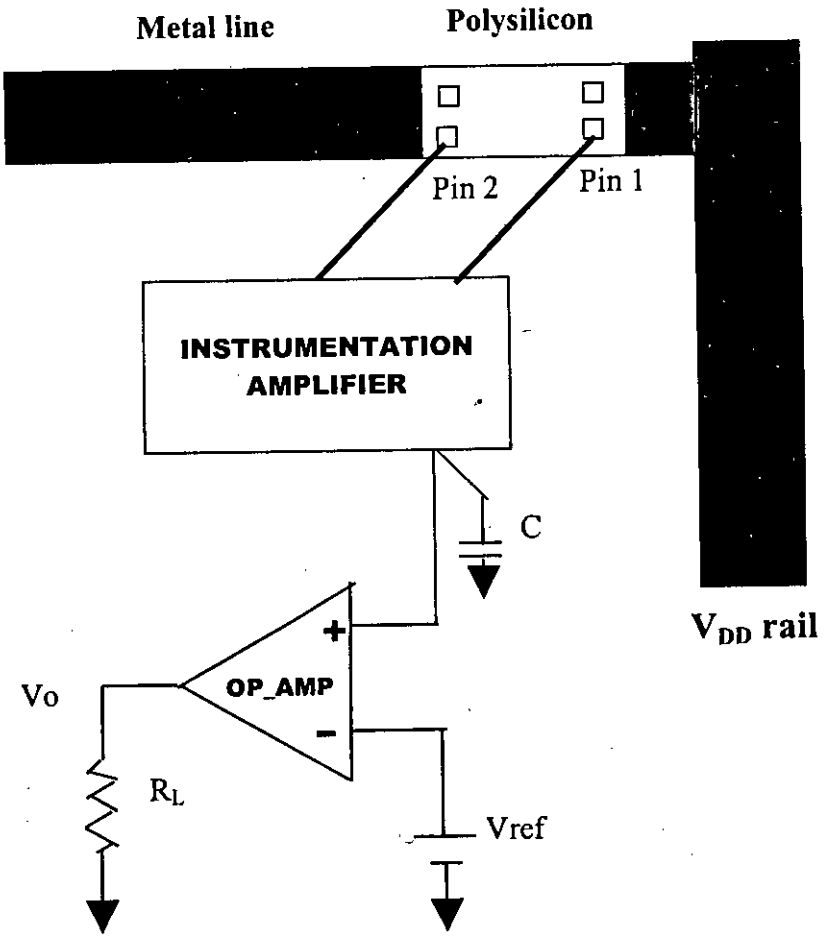


Fig. 6.6: Fault detection by off-chip steady state current monitoring (IDDQ testing.)

The instrumentation amplifier gain is adjusted to about 600 such that a 1mV differential voltage at the input is amplified to approximately 0.6V. A zener diode is used at the negative terminal of the op-amp to produce a reference voltage of 0.6V. Therefore whenever the voltage drop across the polysilicon resistor exceed 1mV the output of the op-amp becomes high indicating that a stuck-on or bridging fault have occured on the chip. For normal operating condition the output is low. Pin 1 and pin 2 of the chip are brought out to facilitate testing. The capacitor C at the output of instrumentation amplifier is incorporated to protect the system from any transient variation of input signal.

6.2.2 Fault detection by On-chip current monitoring

For fault detection with on-chip current monitoring we suggest using Built in Current Sensor (BICS). One of the best high-speed BICS design to date has been proposed by

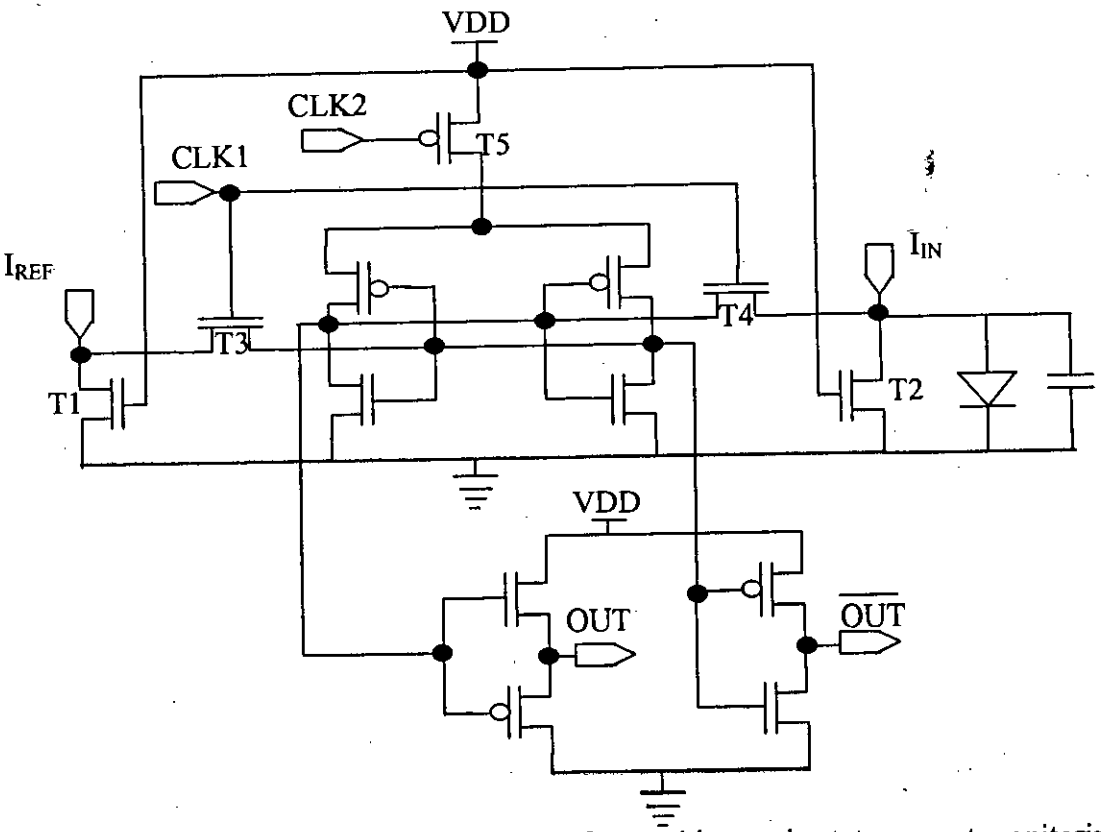


Fig. 6.7: Built in current sensor (BICS) for on chip steady state current monitoring.

Shen *et al.* [43]. This design, shown in Fig. 6.7 achieves its high performance by using a sense amplifier structure similar to the bit line sense amplifier employed in dynamic memories. The circuit under test has its ground line attached to I_{IN} for I_{DDQ} monitoring. The other side of the sensor requires a reference current, I_{REF}. The current flowing into these nodes pass through the nMOS transistor T1 and T2, biased in the linear region, which converts them to voltage. The diode acts to limit the voltage drop across T2 during the peak of the switching transient. During the CLK1 active phase, the voltage pass through the latch via T3 and T4. Then during the CLK2 active (low) phase, the latch is triggered by turning on T5, causing the latch to settle at a logic

level based upon the difference between the voltage at the two nodes. Consequently, if I_{IN} exceeds I_{REEF} at the falling edge of CLK1 (sampling time), an error is flagged.

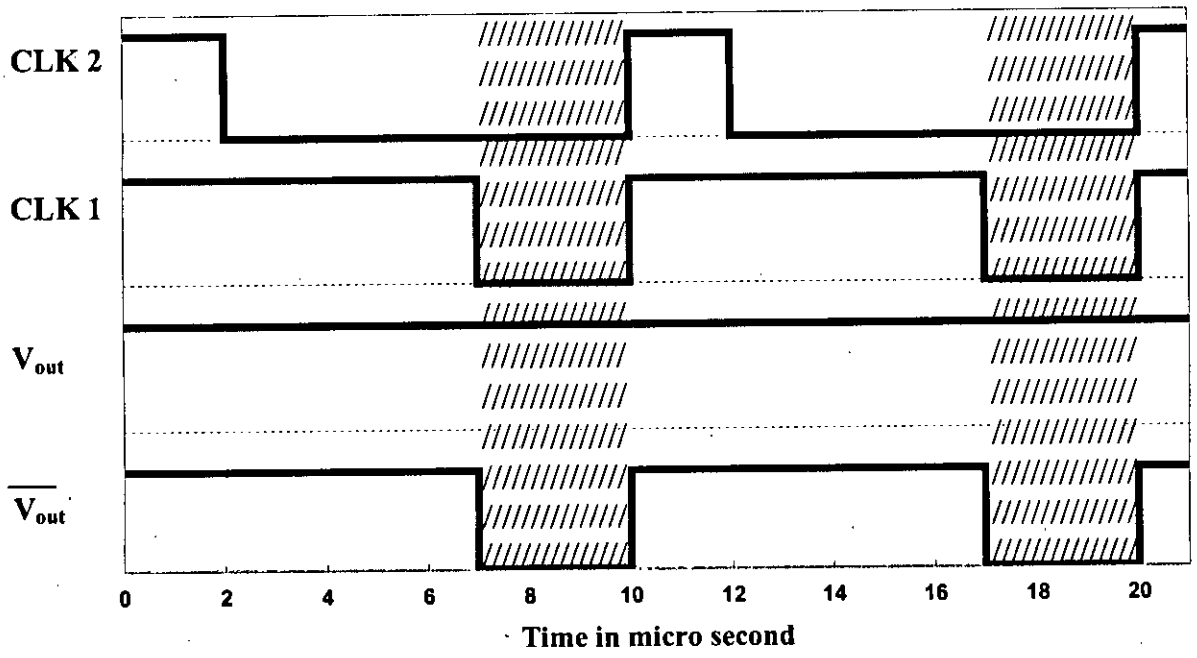


Fig 6.8 Curves of BICS for fault free circuit (I_{REF} = 1 mA, I_{IN} = 1 pA)

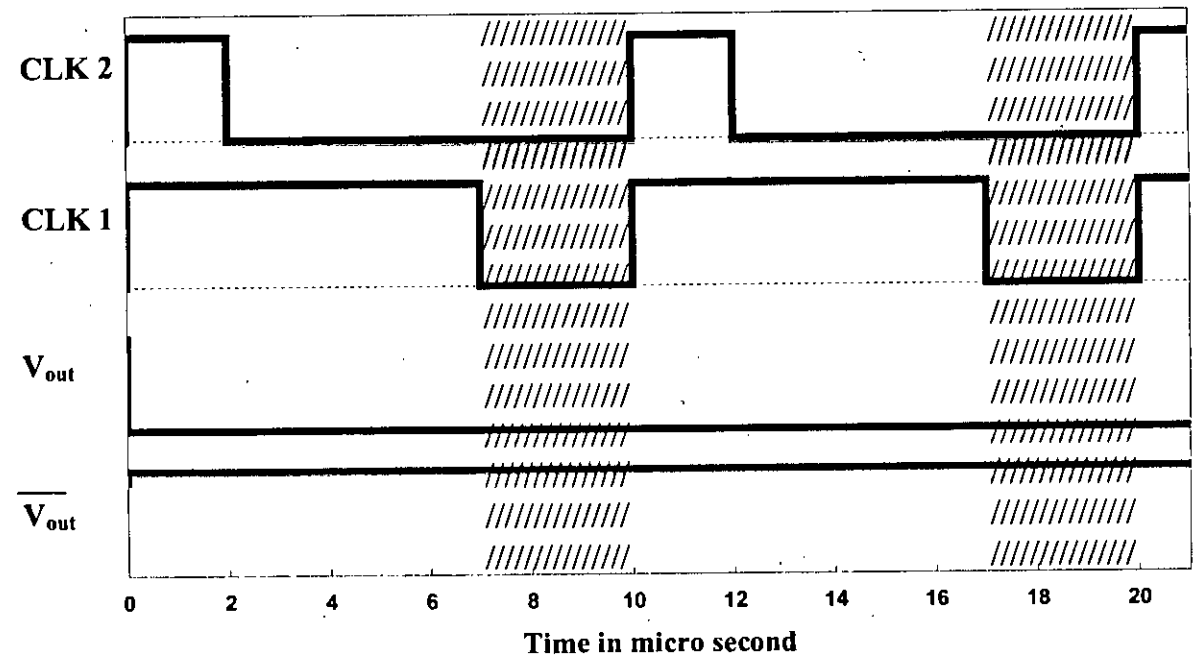


Fig 6.9 Curves of BICS for faulty circuit (I_{REF} = 1 mA, I_{IN} = 3 mA)

Shaded area is the sampling time

6.2.3 Hardware overhead for on-chip current monitoring

The BICS shown in Figure 6.7 comprises of 15 devices. One such current detector is necessary for 15000 basic gates consisting of eight transistors in each gate. Therefore the Hardware overhead = 15x100/15000 x 8 = 0.0125 %. Even if we increase the safety factor to 1000 and use one current sensor for every 1500 gates the hardware overhead is only 0.125%, which is very low. The increase in area due to the use of multiple power rail has not been taken into account in the above calculation.

CHAPTER 7

CONCLUSION

7.1 Conclusion

Testability analysis of basic complementary Pass-transistor Logic (CPL) circuits and CPL full adder SUM and CARRY circuit have been analyzed and fault characterization have been done using extensive SPICE simulation. Testability analysis of Complementary Pass Transistor Logic (CPL) gates under various single stuck faults are presented first. It is shown that all stuck-on faults in the basic CPL gates (AND/NAND, OR/NOR, XOR/XNOR) can be detected by current monitoring which is popularly known as I_{DDQ} testing but no logic monitoring is possible. Similarly all stuck-at faults between gate and source of all the MOS devices of basic CPL gates can be detected only by current monitoring. However, for stuck-at fault between gate and drain of basic CPL gates, it is shown that all faults can be detected by current monitoring, except for the MOS M_3 in AND/NAND gate and MOS M_2 in OR/NOR gates, i.e., for the MOS having same signal at the ground and the drain. It is also shown that all stuck-open fault in the basic CPL gates are detectable by logic monitoring using appropriate two-pattern test. Finally, testability analysis of CPL full adder under various single stuck fault is performed. It is found that stuck-on fault on all the MOS transistor of the SUM logic and the CARRY logic circuit can be detected by steady state current monitoring with appropriate test vectors. For some of these test vectors the fault can also be detected by logic monitoring, but in all cases this is also accompanied by a large flow of signal source current. Similarly all bridging fault can be detected by current monitoring, but no logic monitoring is possible. Stuck open fault on all the MOS transistors on the SUM and the CARRY logic circuit can be detected by appropriate two pattern test. Finally it is concluded that signal source current monitoring (I_{DDQ} testing) is the best method for fault detection in CPL circuits and gives a very wide range of fault coverage.

Finally current testing for on line fault detection in CPL VLSI chip have been proposed. Both fault detection by off the chip current monitoring and on-chip current monitoring is shown. For off-chip current monitoring a separate power supply rail for each of the approximately 15,000 gates is proposed. A small polysilicon resistor is inserted in the VDD rail. A tiny voltage drop occurs in the circuit under faulted

condition which is then connected to a signal processing circuit and gives signal under faulted condition. For on-chip current monitoring the use of use Built-In-Current-Sensor (BICS) is proposed and shown that it has negligible hardware overhead. It is expected these finding will enhance the acceptability of CPL circuits for VLSI design.

7.2 Suggestions for Future Work

In our analysis we have considered basic CPL circuits and CPL full adder SUM and CARRY logic circuits. Though it is expected that the results presented here will be valid for other types of CPL circuits, it would be interesting to extend the work to other complex CPL circuits. Another point is that in our SPICE simulations we have used SPICE level 3 MOS model parameter of a 1.2 μm process. Submicron process with SPICE BSIM3 MOS model parameters can be used to check whether there is any significant difference between steady state current under fault free and faulty condition in those conditions. Regarding the design for testability, novel current sensor with higher speed for high speed I_{DDQ} testing of CPL ULSI chips can be pursued.

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APPENDIX

MOS MODEL PARAMETERS USED FOR SIMULATION

APPENDIX II

MOS Model Parameters Used for Simulation

In this thesis the following parameters are used for the SPICE simulations:

Level	=	3
W	=	20μ
L	=	2μ
V_{To}	=	0.8
t_{ox}	=	$470x\ 10^{-10}$
N_b	=	$38x10^{14}$
X_j	=	$0.20x10^{-6}$
μ_0	=	624
U_{exp}	=	0.055
V_{max}	=	$20x10^4$
N_{eff}	=	9.8
Δ	=	2.0
C_j	=	$160x10^{-6}$
C_{jsw}	=	$430x10^{-12}$
M_j	=	0.5
M_{jsw}	=	0.33
ϕ_j	=	0.81