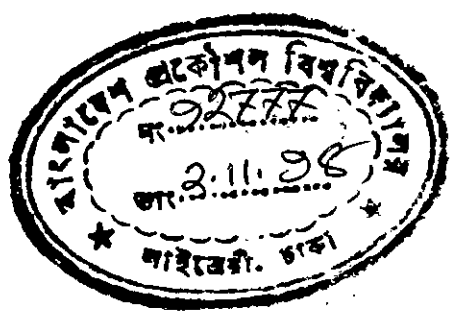
STUDY OF THRESHOLD VOLTAGE AND SUBTHRESHOLD CURRENT BEHAVIOR OF SILICON-ON-INSULATOR (SOI) MOSFETS

A thesis submitted to the Department of
Electrical & Electronic Engineering, BUET, Dhaka
in partial fulfillment of the
requirements for the degree of
Master of Science in Engineering
(Electrical & Electronic)



MOHAMMAD FAIZUL MOMEN

October 1998

DEDICATED TO MY PARENTS

APPROVAL

This thesis titled "**Study of threshold voltage and subthreshold current behavior of silicon-on-insulator (SOI) MOSFETs**" submitted by **Mohammad Faizul Momen**, Roll No. 9406209P, session 1993-94-95 to the Department of Electrical & Electronic Engineering, BUET, Dhaka has been accepted as satisfactory for the partial fulfillment of the requirements for the degree of **Master of Science in Engineering (Electrical and Electronic).**

Board of Examiners

1. **Dr. A.H.M. Zahirul Alam** — **Chairman** (Supervisor) 21.10.98
   Associate Professor
   Department of EEE
   BUET, Dhaka-1000.

2. **Dr. Enamul Basher** — Member (*Ex-officio*) 21.10.98
   Professor and Head
   Department of EEE
   BUET, Dhaka-1000

3. **Dr. A.B.M. Harunur Rashid** — Member 21.10.98
   Assistant Professor
   Department of EEE
   BUET, Dhaka-1000

4. **Dr. Farruk Ahmed** — Member (*External*) 21.10.98
   Professor
   Department of Applied Physics & Electronics
   Dhaka University, Dhaka-1000

DECLARATION

I hereby declare that this work has not been submitted elsewhere for the award of any degree or diploma.

Countersigned

(Dr. A.H.M. Zahirul Alam)

(Mohammad Faizul Momen)

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ABSTRACT

A theoretical analysis has been carried out to develop a model of the threshold voltage, V_{th} for fully depleted silicon-on-insulator (FDSOI) MOSFET with effective channel lengths down to the deep-submicrometer (below 0.25 micron) range. A simple quasi-two-dimensional approach has been used to describe the front surface potential of a SOI MOSFET. Based on the expression for front-surface electric-potential, V_{sf}, the model of the threshold voltage roll-off, ΔV_{th} of the SOI device has been developed and its response to the variation in parameters like silicon-film thickness, channel doping and drain bias (DIBL or Drain Induced Barrier Lowering effect) has been carefully studied.

With a view to producing a complete static-characteristic model of a short channel SOI MOSFET, we developed the expression for the 'free inversion areal charge density,' Q_m, solving the equation of one-dimensional effective gate-channel capacitance and a quasi-two-dimensional Poisson's equation. Using the appropriate expression of channel charge density, Q_m for various inversion conditions, separate drain current models have been developed analytically. These models, one for the weak inversion region (i.e. subthreshold current) and the other for the strong inversion region, have been carefully incorporated with the modified expression for effective channel mobility and the phenomenon of velocity overshoot. Also the effects of channel-shortening, channel length modulation and channel doping on the drain current behavior have been studied.

LIST OF FIGURES

LIST OF PRINCIPAL SYMBOLS

C_{box}	Buried oxide capacitance per unit area
C_{fox}	Front oxide capacitance per unit area
C_{gc}	Effective gate-channel capacitance per unit area
C_i	Inversion capacitance per unit area
C_{si}	Silicon film capacitance per unit area
E_c	Critical electric field
$E_{sf}(y)$	Front lateral surface electric field at y
I_{DS}	Drain current
l	Characteristic length
L	Channel length
l_v	Fitting constant
N_{ch}	Channel doping density
q	Electronic charge
Q_m	Free inversion areal charge density
T_{box}	Buried oxide thickness
T_{fox}	Front oxide thickness
T_{si}	Silicon film thickness
V_{bi}	Built in potential between source-channel or drain-channel
V_{cs}	Channel – source potential
V_{fbf}	Flat band voltage at gate
V_{fbb}	Flat band voltage at substrate
$V_{sf}(y)$	Surface potential at front oxide –silicon interface

$V_{sb}(y)$	Surface potential at buried oxide-silicon interface
V_{SL}	Long channel front surface potential
V_t	Thermal voltage, kT/q
V_{th}	Threshold voltage
V_{th0}	Threshold voltage for a long channel device
v_{sat}	Electron saturation velocity
W	Channel width
γ	Fitting parameter
ε_{si}	Permittivity of silicon
φ_B	Electron Fermi potential
φ_S	$2\varphi_B$
η	Subthreshold ideality factor
μ_0	Electron low-field mobility
μ_n^0	Electron mobility
μ_{eff}	Effective electron mobility
θ	Fitting parameter
β	$2/5U_l$
U_l	Equilibrium electron thermal voltage
α	$1/E_C = \mu_n^0 / 2v_{sat}$

CHAPTER – 1

INTRODUCTION

1.1 Prologue

The modern era of semiconductor electronics was ushered in by the invention of the bipolar transistor in 1948 by Bardeen, Brattain and Shockley at the Bell Telephone Laboratory in the USA. Prior to this invention, valve was the only device to reign in the world of electronics. Valve had many a serious problem, like its bulky size, high cost, short life-time etc. The invention of transistor in 1948 made a complete revolution in the industry of electronics. Since its emergence, the transistor by dint of its multifarious virtues has been replacing the vacuum tubes or valves in almost every field. They began to be used as rectifiers, detectors, amplifiers, oscillators, mixers, modulators etc. Some of the advantages of transistors over vacuum tubes are :

1) they are much smaller in size and so are light in weight
2) no heater or filament is required ; hence no warm-up time needed
3) very low operating voltages can be used
4) they consume little power, resulting in greater circuit efficiency
5) they are much more reliable because they are solid in construction, extremely rugged and can be made impervious to many severe environmental conditions, so they have longer life with essentially no aging effect.

In recognition of their amazing contribution to physics, the three scientists who invented transistor, were awarded the Noble prize in 1956. Transistors, in fact opened the floodgate to further developments in electronics. Within almost ten years of its discovery, the process of miniaturization of electronic equipments had gained

significant momentum and the first Integrated Circuit (IC) was realized in the year of 1959. Man's desire to conquer the space accelerated this effort even further. The purpose of miniaturization was to increase the packing density (so that many more components could be accommodated on a single chip with the same area) and to improve the circuit performance like speed, response time etc. With the advent of ICs, many circuit functions could be packed into a small place and complex electronic equipments could be employed in many applications where space and weight are critical, such as in aircraft or space vehicles. The use of valves nearly became obsolete during the sixties and newer semiconductor devices were developed day by day with prospective and promising features for various aspects, specially for circuit miniaturization. In this series, the field-effect-transistor or FET was developed in the early 1960s. Like its bipolar counterpart (bipolar transistor), the FET is a three-terminal device in which the current through two terminals is controlled at the third; however the FET device is controlled by a voltage at the third terminal (unlike the bipolar transistor which is controlled by a current). Another difference is that the FET is a unipolar device; that is, its current involves majority carriers only.

With the passage of time, field effect transistors came in several forms, e.g. JFET, MESFET and MOSFET. In a junction FET (called a JFET), the control or gate voltage varies the depletion width of a reverse-biased p-n junction. In a metal-semiconductor FET or MESFET, the junction of a JFET is replaced by a Schottky barrier. The FET that has the greatest commercial importance is the metal-oxide-semiconductor FET or MOSFET (or sometimes called MOST). Also known as insulated-gate FET, a MOSFET uses an oxide layer to separate its gate electrode from the semiconductor. Field effect transistors combine the inherent advantages of solid state devices (e.g. small size, low power consumption and mechanical ruggedness) with a very high input impedance and a square-law transfer characteristic that is specially suitable for use as voltage amplifiers. Since its invention, the field effect transistors (FET) became a superior rival to its counterpart, the bipolar junction transistor or BJT. Some features by which FET excels over BJT are as follows :

a) it exhibits a high input impedance(typically many megaohms), since the control (or gate) voltage is applied to a reverse-biased junction or Schottky barrier or across an insulator,

b) it is simpler to fabricate and occupies less space in integrated form. So it is specially suitable for integration of many devices on a single chip.

c) it is particularly well suited for controlled switching between an ON state and an OFF state and is therefore useful in digital circuits.

d) it is less noisy.

Among the members of FET family and other semiconductor devices, metal-oxide-semiconductor FET or MOSFET has gained special significance and prominence over the past two decades. The dominating factor behind such specialty is that the MOS transistor is very well suited to the IC technique, owing to the advantages that it is simpler or easier to fabricate and its size can be reduced with less degree of *small-geometry effects*. Since 'miniaturization to a further extent' is a never-ending-hunt of the modern researcher, MOSFET, in the last few years has emerged as the most important electronic device, superseding its bipolar counterpart and other devices in both sales volume and applications. MOS transistor has already confirmed its state as a better choice for use in densely packed circuits like ULSI (ultra large scale integration) circuits. Also the fact that digital circuits require only on-off response is an advantage for the MOS device and so MOS transistor is widely used in digital circuits like logic gates, registers or memory arrays.

As said earlier that IC technology was a great advancement of mankind in the world of electronics. Due to the rapid developments in integrated circuit technology starting from small scale integration(SSI), then medium scale integration(MSI), large scale integration(LSI), very large scale integration(VLSI) and now with the

most recent – ultra large scale integration (ULSI) technique – even the use of individual transistors is becoming unnecessary. The vast changes that have taken place during the last 20 years can best be understood by noting the reduction in size and price of modern computers. A small, modern minicomputer is more than 100 times smaller in size and 1/100 th of the price of a computer designed 20 years ago to do the same job. Applications of ICs are now pervasive in such consumer products as watches, calculators, automobiles, telephones, television and other home appliances.

Now, in the late nineties, the 'hunt-for-further-integration' is not only continuing but is accelerating every day. As earlier said, the metal-oxide-semiconductor FET or MOSFET has been the major device for integrated circuits over the past two decades and this was due to the fact that scaling down of the MOSFET provided high performance gain and smaller die size. The twin benefits of smaller die size (more chips per wafer and higher fractional yield) exert downward pressure on die cost . As a natural and consequential effort, industrial research has already set sight on MOSFETs of channel length of 0.1 μm and below [1]; the motivations for continued scaling include not only better speed and density but also less power consumption for integrating a complete system on a chip. There have been numerous device structures of submicrometer MOSFET reported in the literature, such as MOSFET with uniformly doped substrate (UD), delta doped MOSFET (DD), partially depleted silicon-on-insulator (SOI) MOSFET and fully depleted silicon-on-insulator (SOI) MOSFET. Among these, fully depleted SOI MOSFET (which has an additional oxide layer just below the Si film) has attracted considerable attention as a potential candidate for future VLSI / ULSI generations, because it offers superior electrical characteristics over bulk MOSFETs, such as, reduced junction – capacitances, attenuated short channel effects, improved subthreshold characteristics, increased channel mobility, reduced hot carrier effects and so on. As a consequence, submicrometer and deep submicrometer SOI circuit design and simulation are becoming increasingly important in VLSI / ULSI technology research.

1.2 Limitations of scaling down the SOI MOSFET :

As mentioned in section 1.1 that the purpose of microminiaturization is to increase the packing density and to improve the device performance like speed, response time etc. Ever since the birth of the integrated circuits, researchers have ceaselessly attempted to scale down the size of devices, and silicon-on-insulator (SOI) MOSFET has already proven to be one of the most promising devices for large-scale-integration. It is expected that the realization of 1 giga bit DRAM (dynamic random access memory) will be achieved in the near future and it will hence require the miniaturization of MOS devices approaching the deep submicron regime (below 0.25 μm)[2]. However, as MOS devices are scaled down to submicrometer dimensions, various non ideal characteristics are observed. Since these effects are due to the scaling down of dimensions, these are known as *'small geometry effects.'* These include :

1) threshold voltage variation or roll-off
2) non saturated drain current
3) sharp swing of the subthreshold current
4) drain- induced-barrier-lowering (DIBL)

It has been observed experimentally that the threshold voltage does not remain the same if the dimensions are reduced, rather it shifts downward. Moreover, the shift is very sensitive to the drain bias voltage.

As the channel length of a SOI MOS is reduced, its effective channel length becomes comparable to the depletion region near the drain when operated in saturation region; then the drain current does not remain constant with increased drain voltage, unlike that of the long channel device.

The subthreshold current in a SOI MOS (current that flows before applying the threshold voltage or even for zero gate bias) is caused by carrier diffusion from the source to drain. Like a bipolar transistor, this current is very sensitive to the base width i.e. channel length in this case. Subthreshold current is seen to increase as devices are made smaller ; also this current in a short channel device is seen to increase with increasing drain voltage due to channel length modulation.

Another effect that becomes prominent with scaling down of devices is the DIBL or *drain induced barrier lowering effect.* As the channel length continues to decrease, the drain depletion layer starts to interact with the source-channel junction to lower the source-junction potential barrier; which in turn allows electrons to be injected into the channel regardless of the gate voltage and the gate voltage thus loses control of the drain current.

1.3 REVIEW OF THE PREVIOUS WORK

The thin-film fully-depleted SOI MOS field-effect-transistor (SOI MOSFET) is considered a promising candidate for future ULSI generations due to its multifarious advantages over the bulk MOSFET. So in the recent years, this device has attracted considerable attention and a sufficient amount of research works have been reported so far which encounters the effect of scaling down on the threshold voltage roll-off, the subthreshold swing, the normal drain current etc. In FDSOI MOSFET, a strong electrical coupling of the two interfaces results in interesting behavior of the threshold voltage. This effect was reported using one-dimensional models [3]-[5]. However, threshold voltage reduction with decreasing channel length and increasing drain-source voltage is a two-dimensional effect in short channel devices. The exact solution of two-dimensional Poisson's equation in the channel

depletion region has already been reported in [6] and [7]. Analytical potential distribution models based on the infinite series methods were developed in [6]. However, such models require iterative calculations, that reduce the physical insight provided by the infinite series models.

Charge sharing approach was reported in [8] for FDSOI MOSFETs. (As the channel length is decreased, the source and drain depletion regions are brought closer together and can intrude into the channel even without bias and this way they can share the charge in the channel; this is known as charge-sharing effect). The concept of charge sharing provides physical insight into the development of the threshold voltage expression and predicts trends almost correctly. Charge sharing models predict a $1/L_{eff}$ dependent threshold voltage shift. However, the charge- sharing model assumption of constant surface potential is not valid in the range of submicrometer channel length. On the other hand, the exact solution of Poisson's equation with various approximations made for the boundary conditions lacks physical meaning (due to series solution of Poisson's equation) and is computationally inefficient.

Until recently, several analytical I-V characteristic models for SOI MOS had been developed for the purpose of circuit simulation. However, few of these models provide a complete coverage on I-V characteristics including the subthreshold regime. The recently-published models [9]-[10] are mainly restricted to the drift-diffusion model, so the velocity overshoot effect was not taken into account. Velocity overshoot is an energy transport effect; as channel length reduces, the electric field near the source rises in a steep manner which induces non-local transport effect and so enhances carrier velocity in the source end. This phenomenon is known as 'velocity overshoot' effect and it becomes obvious as the feature size is scaled into the deep submicrometer regime [11]. Also the studies published so far, concentrated on intrinsic device behavior without accounting for the source/drain resistance. As device dimensions are scaled down to the submicrometer level, these parasitic resistances become increasingly significant.

1.4 OBJECTIVES OF THE PRESENT STUDY

The main objective of this research is to develop a physics-based simple, complete and analytical submicrometer-SOI-MOSFET model for accurate simulation of digital / analog circuits. The objectives, at large are:

- To develop an accurate expression for surface-potential of a single-gate FDSOI MOSFET by using a quasi-two-dimensional approach.
- To develop an accurate model of threshold voltage for a SOI device, applicable to both submicrometer and deep submicrometer channel lengths
- To obtain the expression for free inversion areal charge density, in terms of gate and drain voltages.
- To derive an effective mobility formula, to be used in the drain current model and modified on the basis of energy-balance equation and considering velocity overshoot.
- To obtain the I-V characteristic models separately in weak inversion (for subthreshold current) and strong inversion (for normal drain current) regions, incorporating the effects of drain/source resistance, velocity overshoot, mobility reduction due to the transverse electric field and DIBL.

1.5 BRIEF INTRODUCTION TO THIS THESIS

A brief introduction to semiconductor electronics and integrated-circuit (IC) technology is presented in chapter 1, with an emphasis on MOSFET devices and a review of the research works currently going on in this field.

Chapter 2 presents sequentially a model for front-surface electric-potential using a quasi-two-dimensional Poisson's equation, then the model for threshold voltage, the model for free-inversion areal charge density, the I-V model for subthreshold regime and the I-V model for above threshold / normal operating conditions.

The results and discussions are presented in chapter 3.

Conclusion and future scope of works are presented in chapter 4.

CHAPTER-2

THEORETICAL ANALYSIS OF THRESHOLD VOLTAGE AND STATIC CHARACTERISTICS OF A FULLY DEPLETED SOI MOSFET

2.1 Overview

The Metal –Oxide-Semiconductor FET or MOSFET is a four terminal semiconductor device in which the lateral current flow is controlled by an externally applied vertical electric field. A typical MOS transistor is shown in Fig. 2.1 where the four terminals are designated as the source, gate, drain and substrate. (In most simplified analyses the effect of the substrate is neglected or it is often tied to the source and the MOS transistor is considered as a three- terminal device). The transistor shown is an n-channel MOSFET which consists of a lightly doped p-type substrate into which two highly doped n^+ regions (source and drain) are diffused. A thin (100-1000Å) insulating silicon dioxide (SiO_2) is grown over the surface of the structure and holes are cut into the oxide layer, allowing contact with the source and drain.

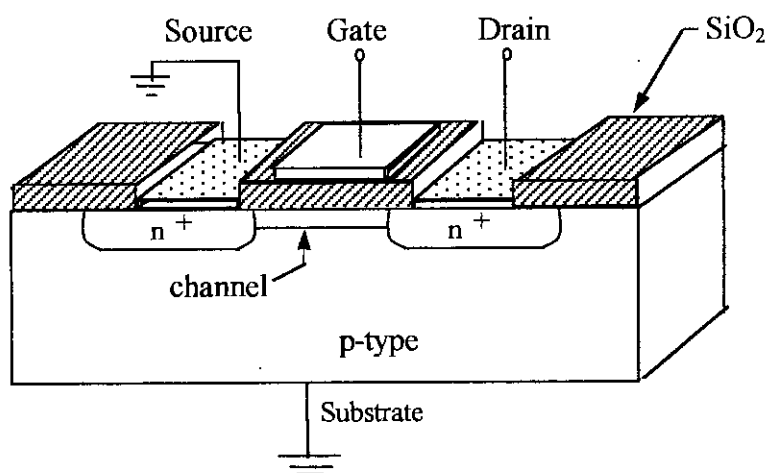


Fig. 2.1 An n-channel MOS Transistor

Then the gate electrode is overlaid on the oxide, covering the entire channel region (region between the source and drain). The gate electrode was originally metal, specifically aluminium, but is now more commonly a layer of polycrystalline silicon (referred to as polysilicon).

With no voltage applied to the gate, the two back-to-back p-n junctions between the drain and source prevent current flow in either direction . When a positive voltage is applied to the gate with respect to the substrate, electrons are induced in the semiconductor below the oxide-semiconductor interface. In fact so many electrons are attracted to the surface that an extremely thin conduction channel or inversion layer is formed between the source and drain, where the semiconductor actually changes from p to n type. Now, when a voltage is applied between the source and drain, current can flow between them and the flow (or channel conductivity) can be controlled or modulated by the vertical electric field; this is why the device is called a Field Effect Transistor or FET. For the transistor shown, the induced charge in the channel is n-type and the device is so known as an n-channel MOSFET or simply NMOS. A p-channel transistor is obtained by interchanging the n and p regions. Since the MOS gate is insulated from the channel, no dc current conducts through the oxide layer and so a MOSFET is also known as the insulated-gate field effect transistor (IGFET). The insulating oxide layer results in an extremely high input resistance ($10^{10} - 10^{15}$ ohms) for the MOSFET.

The device just described requires a voltage to be applied to the gate before the channel is formed and the drain current is enhanced by the applied gate voltage; this is why the device is called an " enhancement –type MOSFET. Sometimes, charges are deliberately introduced between source and drain by ion implantation or a channel is diffused between source and drain, with the same type of impurity as used for the source and drain diffusion. Such a normally 'ON' transistor is called a depletion-type MOSFET because a gate voltage of reverse polarity (in case of NMOS, negative) is to be applied to deplete the channel of electrons and shut the device off.

SOI MOSFET

An interesting and useful extension of the silicon MOS process can be achieved by growing very thin films of single crystal Si on insulating substrates. The Si films being very thin (100 nm) the source and drain regions can be made to extend entirely through the film to the buried insulator and as a result the junction capacitances are remarkably reduced. Such a device with silicon film sandwiched between two insulating oxide layers is known as Silicon- On -Insulator MOSFET or SOI MOS . The cross sectional view of a SOI MOS is shown in the figure 2.2.

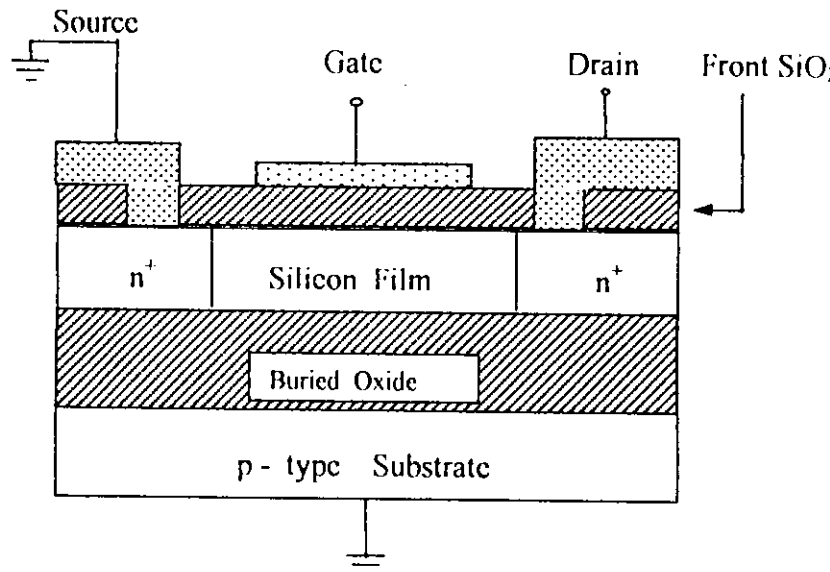
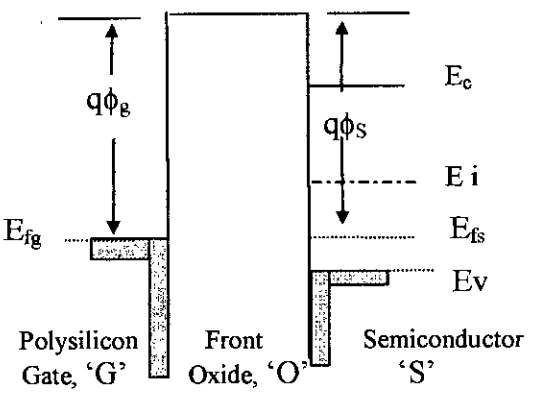


Fig. 2.2 Cross sectional view of a SOI MOSFET.

THE MECHANISM OF CHANNEL FORMATION AND THE SURFACE CHARGE CONDITIONS IN A SOI MOSFET :

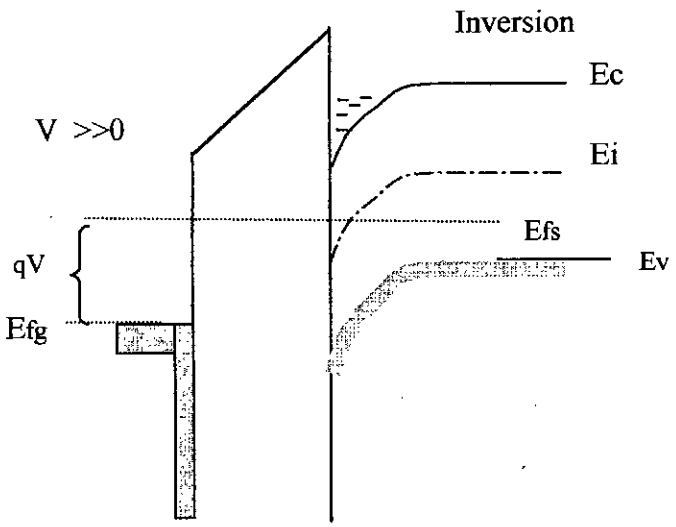
The MOS structure shown in Fig. 2.2 is basically a device containing two capacitors; one is the front capacitor with front SiO_2 as the dielectric material and the other is the buried capacitor with buried SiO_2 as the dielectric material. It is the front capacitor

which is significantly prominent and so we limit our concerns here around the conditions of front surface charge of the Si film (i.e. the charge below the interface of front SiO2- Si film). Let us firstly consider the energy –band diagram of an ideal MOS structure, as shown in Fig. 2.3. For simplicity, we have assumed that the work-functions are the same for all three parts of the front capacitor and so their energy-bands at equilibrium are flat. (The work function is defined as the work required to bring an electron from the Fermi level to the vacuum level). As shown in Fig. 2.3.a, the system is at equilibrium and $q\phi_g = q\phi_S$, ($q\phi_g$ is the modified work function for the front SiO_2-gate interface and $q\phi_S$ is the modified work function for the front SiO_2- Si interface). Another useful quantity is the $q\phi_f$ which indicates how strongly p-type the semiconductor is.



(a)

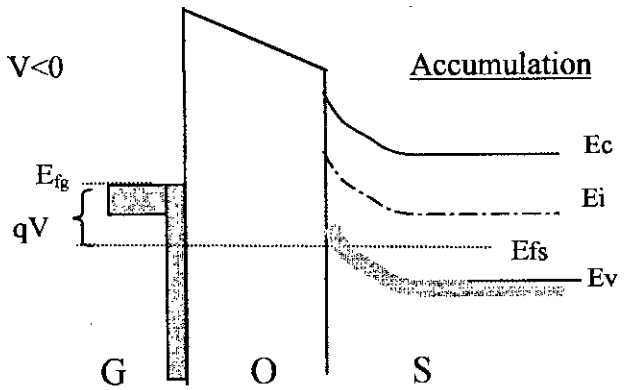
Fig. 2.3 Effects of applied voltage on the energy band diagram of ideal NMOS capacitor (a) band –diagram at equilibrium



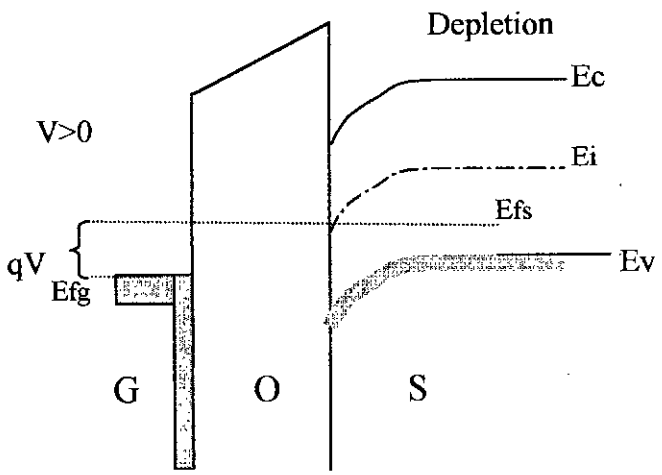
(d)

Fig. 2.3 Effects of applied voltage on the energy band diagram of ideal NMOS capacitor (d) band-diagram for a larger positive gate voltage causing inversion.

If we apply a negative gate voltage (fig. 2.3.b), a negative charge is effectively deposited on the gate and in response, an equal net positive charge or holes is accumulated at the semiconductor surface. This situation, when the hole density just below the Si surface is greater than the equilibrium density in the bulk, is known as carrier accumulation. The energy-bands of the semiconductor bend upward near the interface, leading to a larger $q\phi_f$ so that the accumulation of holes can be accommodated.



(b)



(c)

Fig. 2.3 Effects of applied voltage on the energy band diagram of ideal NMOS capacitor (b)band-diagram for negative gate voltage causing hole accumulation, (c)band-diagram for positive gate voltage causing hole depletion.

When we apply a positive voltage at the gate (fig. 2.3.c), the gate Fermi level is lowered by qV relative to its equilibrium position; as a result holes are depleted from the SiO_2 – Si interface and the semiconductor energy – bands bend downward near the surface leading to a smaller $q\phi_f$.

If we continue to increase the positive gate bias (fig. 2.3.d), the bands at the semiconductor surface bend down more sharply. In fact, a sufficiently large voltage can bend Ei below E_{fs} (i.e. negative $q\phi_f$), which is particularly an interesting case, since $E_{fs} >> Ei$ means a large electron concentration in the conduction band. In other words, the silicon surface procures the conduction properties typical of n-type material and this is done not by doping but by the inversion of the originally p-type silicon due to the applied voltage. This inversion layer is the key to MOS transistor operation. Depending on the strength of the positive gate bias, the inversion event is termed as *weak inversion*, *moderate inversion* and *strong inversion*. As long as the electron density at the surface remains smaller than hole density in the bulk, the condition is called 'weak inversion'. As soon as the two densities become equal, the onset of moderate inversion is reached, the surface potential is then $2\phi_f$. In most MOS transistor operation, it is necessary to establish a strong inversion carrier density and the criterion for strong inversion is that the surface potential becomes much greater than $2\phi_f$.

FLAT BAND AND THRESHOLD VOLTAGES

In the previous section, we assumed that the energy-band diagram is flat when the MOS is at equilibrium condition (i.e. zero gate bias). In practice, this condition is not realized because of unavoidable work-function difference and the charges in the oxide and surface states. The modified work-function of the gate-electrode is not generally equal to that of the semiconductor, so a band –bending exists in the semiconductor in order to satisfy the requirement of constant Fermi level under thermal equilibrium.

Also the charges that reside within the oxide contribute to further band – bending. So the gate voltage required to achieve the flat band condition, known as *flat band voltage*, is given by,

$V_{FB} = V_{G1} + V_{G2} = \phi'_{gs} - Q_0 / C_{fox} = (\phi'_g - \phi'_s) - Q_0 / C_{fox}$;

where, ϕ'_g is the modified work-function of gate-electrode

ϕ'_s is the modified work-function of semiconductor

Q_0 is the sum of induced charges under zero gate bias

C_{fox} is the front oxide capacitance.

In case of a SOI MOSFET, an extra gate voltage is to be applied to take care of the band-bending at buried oxide-Si interface.

Threshold Voltage

Threshold voltage is the critical voltage at which the inversion layer is formed to a significant extent, giving rise to rapid increase of the inverse charge for higher gate voltages. In other words, the threshold voltage specifies the gate voltage at the onset of strong inversion. This voltage takes into account the flat-band voltage, the moderate inversion onset-voltage (i.e. $2\phi_f$) and voltages due to depletion layer and oxide layer charges. Threshold voltage is a very significant parameter of a MOS circuit. Generally a lower threshold voltage is desirable since it allows the use of a small power- supply voltage and so lower power consumption. Lower threshold voltage also allows smaller swing during switching .

STATIC CHARACTERISTICS OF THE SOI MOSFET

A schematic diagram of an n-channel SOI MOSFET is shown in the Fig.2.4, in which bias voltages are included. To simplify our analysis, the source and the substrate have been grounded. The static characteristics of the SOI MOSFET have two distinct regions of operation. At low drain voltages, the drain to source characteristics are basically ohmic and the drain current is proportional to the drain voltage in a nearly linear fashion. This is the linear region of operation. At high drain voltages the gate voltage is neutralized and the inversion layer disappears at the drain end of the channel. The channel is then called "pinched-off" and further increase of drain voltage would not increase the drain current significantly, i.e. the drain current becomes saturated and the region of operation is called "saturation region".

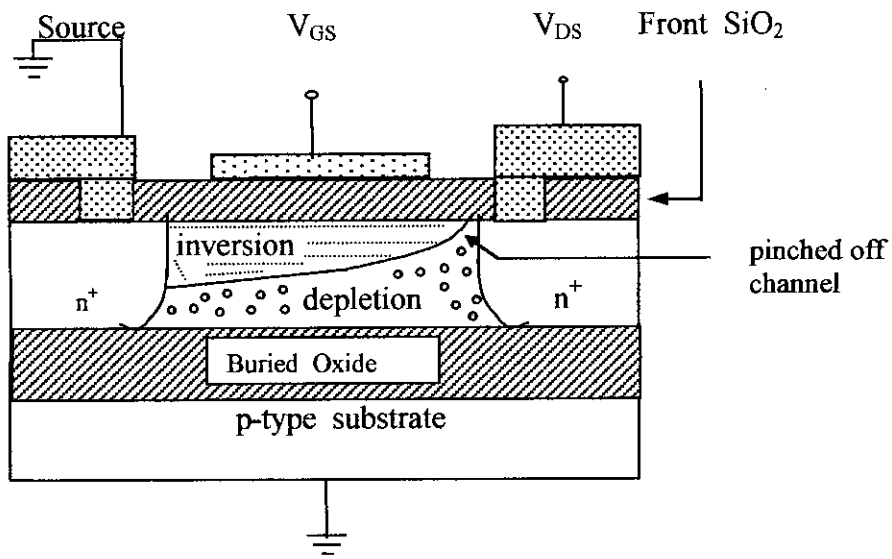


Fig. 2.4 An n-channel SOI-MOSFET operating in the saturation region

2.2 FRONT SURFACE POTENTIAL OF A SOI MOSFET

We firstly represent the channel – depletion – region of a fully depleted n-channel SOI –MOSFET by a rectangular Gaussian box as shown in fig. 2.5. Axes are so chosen that the y-axis is along the channel from source to drain and the x-axis is from the front oxide to the buried oxide. The height of the box is T_{si} and the length is Δy.

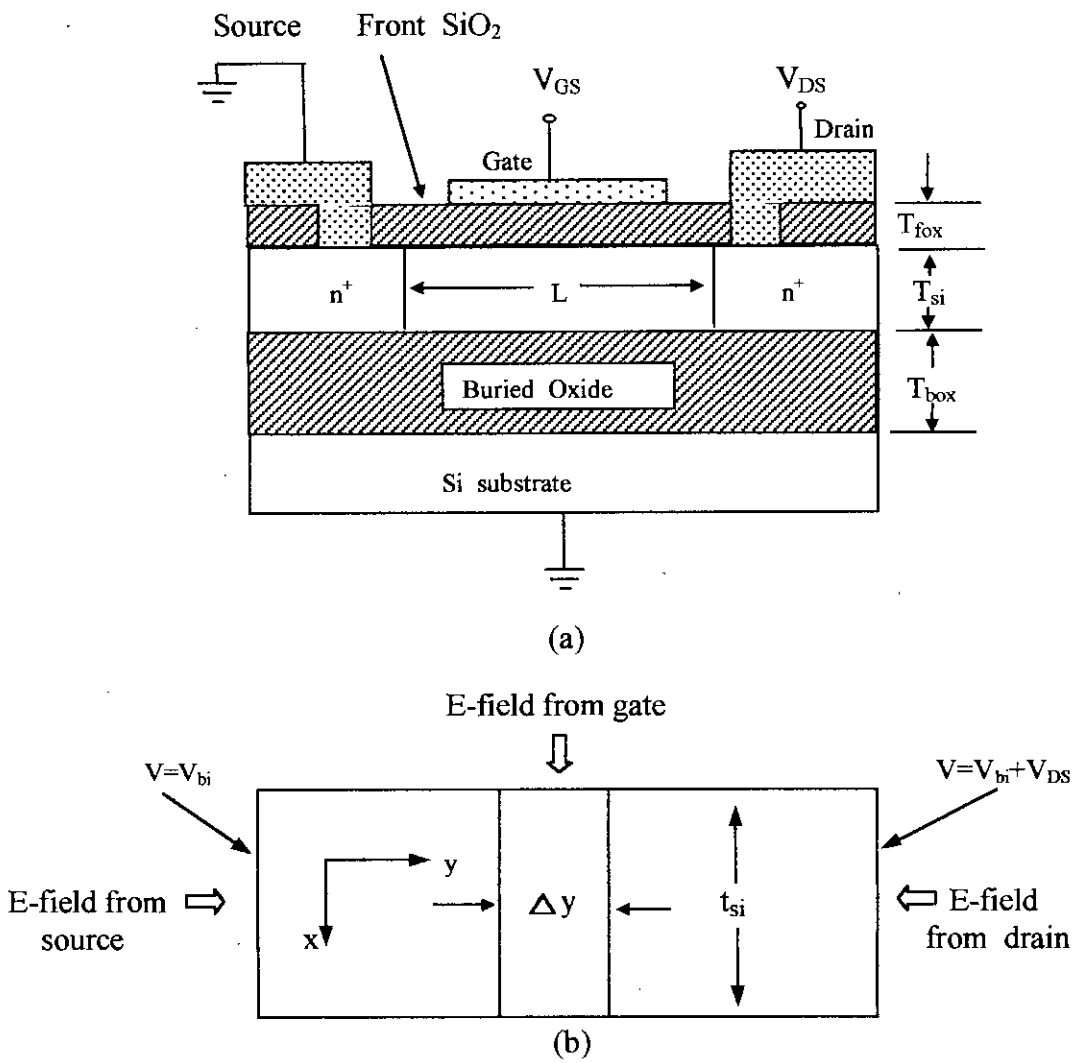


Fig. 2.5 (a) Cross-sectional view of a typical SOI-MOSFET
(b)Gaussian box representation of its channel depletion region with boundary conditions and reference direction.

By applying Gauss's law to this box and neglecting mobile carrier charge in the channel, the following equation can be derived :

$$\frac{\varepsilon_{si} T_{si}}{\gamma} \times \frac{\partial E_{sf}(y)}{\partial y} + C_{fox}\left(V_{GS} - V_{fbf} - V_{sf}(y)\right) + C_{box}\left(- V_{fbb} - V_{sb}(y)\right) = qN_{ch}T_{si} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2.1)$$

where,

ε_{si} is the silicon permittivity

T_{si} is the channel thickness

$E_{sf}(y)$ is the front lateral surface electric field

γ is a fitting parameter

C_{fox} is the front oxide capacitance

V_{GS} is the gate-source voltage

V_{fbf} is the flat-band voltage at the gate

$V_{sf}(y)$ is the channel potential at the front SiO_2 – Si interface

C_{box} is the buried oxide capacitance

V_{fbb} is the flat band voltage at the substrate

$V_{sb}(y)$ is the channel potential at the buried SiO_2 – Si interface

q is the charge of an electron

N_{ch} is the channel doping

The first term on the left hand side of equation (2.1) refers to the net electric flux entering the Gaussian box along the y – direction, the second term refers to the electric flux entering the top surface of the Gaussian box, the third term refers to the electric flux entering the bottom surface of the Gaussian box. The right hand side of the equation represents the total charge inside the Gaussian box. In deriving equation (1), we have assumed uniform electric field in the buried oxide and neglected fringing fields in the buried oxide due to source and drain.

The back- channel surface potential (V_{sb}) can be expressed in terms of the front channel surface potential (V_{sf}) by solving the 1-D Poisson's equation in the thin silicon film as following :

1-D Poisson's equation for the potential, V along the x axis

$$(\partial^2 V / \partial x^2) = q N_{ch} / \varepsilon_{si} \quad \ldots\ldots\ldots\ldots\ldots\ldots (2.2)$$

Integrating,

$$(\partial V / \partial x) = (q N_{ch} x / \varepsilon_{si}) + C_1 \quad \ldots\ldots\ldots\ldots\ldots\ldots (2.2.a)$$

At $x = 0$, $(\partial V / \partial x) = -E_{sf}$

$\therefore C_1 = -E_{sf}$

Integrating eqn. (2.2.a)

$$V = (q N_{ch} x^2 / 2\varepsilon_{si}) - E_{sf} x + C_2 \quad \ldots\ldots\ldots\ldots\ldots\ldots (2.2.b)$$

At $x = 0$, $V = V_{sf}$; So, $C_2 = V_{sf}$

Again at $x = T_{si}$, $V = V_{sb}$;

$$\text{So, } V_{sb} = V_{sf} - E_{sf} T_{si} + (q N_{ch} T_{si}^2 / 2\varepsilon_{si}) \quad \ldots\ldots\ldots\ldots (2.2.c)$$

Now we obtain the following equation by applying Gauss's law at the front SiO_2 - Si interface,

$$E_{sf}(y)\, \varepsilon_{si} = C_{fox} (V_{GS} - V_{fbf} - V_{sf}(y)) \quad \ldots\ldots\ldots\ldots (2.3)$$

By substituting (2.2.c) and (2.3) in (2.1) we obtain,

$$\frac{\varepsilon_{si} T_{si}}{\gamma} \times \frac{\partial E_{sf}(y)}{\partial y} + C_{fox}[(V_{GS} - V_{fbf} - V_{sf}(y)] + C_{box}[-V_{fbb} - \{V_{sf} - \frac{C_{fox}(V_{GS} - V_{fbf} - V_{sf}(y))T_{si}}{\varepsilon_{si}}\} + \frac{qN_{ch} T_{si}^2}{2\varepsilon_{si}}] = qN_{ch} T_{si}$$

$$\ldots\ldots\ldots\ldots (2.4)$$

Defining the thin film capacitance $\varepsilon_{si} / t_{si}$ as Csi, we obtain,

$$\frac{\varepsilon_{si} t_{si}}{\gamma} \times \frac{\partial E_{sf}(y)}{\partial y} - V_{sf}(y)\left[C_{fox} + C_{box} + \frac{C_{box} C_{fox}}{C_{si}}\right] = qN_{ch} t_{si}\left[1 + \frac{C_{box}}{2C_{si}}\right]$$

$$- C_{fox}\left(V_{gs} - V_{fbf}\right)\left(1 + \frac{C_{box}}{C_{si}}\right) + C_{box} V_{fbb} \quad \ldots\ldots\ldots\ldots \quad (2.4.a)$$

Let ,

$$\frac{1}{\tilde{C}_{ox}} = \frac{1}{C_{fox}} + \frac{1}{C_{box}} + \frac{1}{C_{si}},$$

$$\frac{1}{\tilde{C}_{box}} = \frac{1}{C_{box}} + \frac{1}{C_{si}},$$

$$\frac{1}{\tilde{C}_{fox}} = \frac{1}{C_{fox}} + \frac{1}{C_{si}},$$

$$C_{ox} = \left[C_{fox} + C_{box} + \frac{C_{fox} C_{box}}{C_{si}}\right] = \frac{C_{fox} C_{box}}{\tilde{C}_{ox}};$$

Then equation (2.4.a) becomes,

$$\frac{\varepsilon_{si} t_{si}}{\gamma} \times \frac{\partial E_{sf}(y)}{\partial y} - V_{sf}(y) C_{ox} = qN_{ch} t_{si}\left[1 + \frac{C_{box}}{2C_{si}}\right] -$$

$$C_{fox}\left[1 + C_{box} / C_{si}\right]\left[V_{gs} - V_{fbf}\right] + C_{box} V_{fbb};$$

$$\Rightarrow \frac{\varepsilon_{si} t_{si}}{\gamma C_{ox}} \times \frac{\partial E_{sf}(y)}{\partial y} - V_{sf}(y) = \frac{qN_{ch} t_{si}}{C_{ox}}\left[1 + \frac{C_{box}}{2C_{si}}\right] -$$

$$\frac{C_{fox}}{C_{ox}}\left[1 + C_{box} / C_{si}\right]\left[V_{gs} - V_{fbf}\right] + \frac{C_{box}}{C_{ox}} V_{fbb};$$

$$\Rightarrow \frac{\varepsilon_{si} t_{si}}{\gamma C_{fox}} \times \frac{\tilde{C}_{ox}}{C_{box}} \times \frac{\partial E_{sf}(y)}{\partial y} - V_{sf}(y) + V_{SL} = 0$$

$$\Rightarrow \ell^2 \frac{\partial E_{sf}(y)}{\partial y} - V_{sf}(y) + V_{SL} = 0 \qquad \ldots\ldots\ldots \text{(2.4.b)}$$

where, $\ell^2 = \frac{\varepsilon_{si} t_{si}}{\gamma C_{fox}} \times \frac{\tilde{C}_{ox}}{C_{box}}$

and $V_{SL} = \frac{C_{fox}}{C_{ox}} \left[1 + C_{box} / C_{si}\right](V_{gs} - V_{fbf}) - \frac{C_{box} V_{fbb}}{C_{ox}}$

$$- \frac{qN_{ch} t_{si}}{C_{ox}} \left[1 + \frac{C_{box}}{2C_{si}}\right]$$

$$= \frac{\left[1 + \frac{C_{box}}{C_{si}}\right]}{\left[1 + \frac{C_{box}}{\tilde{C}_{fox}}\right]} \times \left[V_{gs} - V_{fbf}\right] - \frac{\left[C_{box} / C_{fox}\right] V_{fbb}}{\left[1 + \frac{C_{box}}{\tilde{C}_{fox}}\right]}$$

$$- \frac{\left[1 + \frac{C_{box}}{2C_{si}}\right]}{\left[1 + \frac{C_{box}}{\tilde{C}_{fox}}\right]} \frac{qN_{ch} t_{si}}{C_{fox}} \qquad \ldots\ldots\ldots \text{(2.4.c)}$$

The solution of eqn. (2.4.b) with the boundary conditions of $V_{sf}(0) = V_{bi}$ and $V_{sf}(L) = V_{bi} + V_{DS}$ is

$$V_{sf}(y) = V_{SL} + (V_{bi} + V_{DS} - V_{SL}) \frac{\sinh(y / \ell)}{\sinh(L / \ell)} +$$

$$(V_{bi} - V_{SL}) \frac{\sinh[(L - y) / \ell]}{\sinh(L/\ell)} \quad \ldots\ldots\ldots (2.5)$$

In the above equation V_{SL} represents the Long Channel front surface potential, same as that defined in [7], V_{bi} is the built- in potential between the source-channel and drain-channel p-n junctions and "l" is the characteristic length defined as

$$l = \sqrt{\frac{\varepsilon_{si} t_{si} \tilde{C}_{ox}}{\eta C_{fox} C_{box}}} \; ;$$

The front channel surface potential expressed by eqn. (2.5) can be thought of as the long-channel surface potential modified by the source/drain fringing field. The effects of the variation of the lateral field in the depletion layer under the channel are incorporated through the fitting parameter γ. $E_{sf}(y)/\gamma$ can be thought of as an average lateral electric field in the channel. γ is less than one when $E_{sf}(y)$ is less than the average field and greater than one otherwise. At $V_{GS} = V_{th}$, surface lateral electric field is less than the average lateral electric field in the channel depletion region and so $\gamma < 1$. For large drain voltages, the surface lateral electric field near the drain is more than the average lateral field and hence $\gamma > 1$ as reported in [12] and [13].

2.3 THE SHORT-CHANNEL THRESHOLD VOLTAGE MODEL FOR AN FDSOI MOSFET

Here we develop a short-channel threshold voltage model for FDSOI MOSFET using a quasi-two-dimensional approach, similar to those used for modeling threshold voltage, substrate current and other hot electron phenomenons in Bulk MOSFETs[12]-[15].

For a long channel device, i.e. for $L \rightarrow \infty$, the surface potential is V_{SL} and the threshold voltage for such device, V_{th0} can be obtained from the expression of V_{SL} (eqn. 2.4.c) by setting it equal to $2\varphi_B$, where $\varphi_B = (kT/q) \ln (Nch / n_i)$:

Defining $2\varphi_B$ as φ_S,

$$\varphi_S = \frac{\left[1 + \frac{C_{box}}{C_{si}}\right]}{\left[1 + \frac{C_{box}}{\tilde{C}_{fox}}\right]} \times \left[V_{th\,0} - V_{fbf}\right] - \frac{\left[C_{box} / C_{fox}\right] V_{fbb}}{\left[1 + \frac{C_{box}}{\tilde{C}_{fox}}\right]}$$

$$- \frac{\left[1 + \frac{C_{box}}{2C_{si}}\right]}{\left[1 + \frac{C_{box}}{\tilde{C}_{fox}}\right]} \frac{qN_{ch}t_{si}}{C_{fox}}$$

$$\Rightarrow V_{th0} = V_{fbf} + \frac{\tilde{C}_{box}}{\tilde{C}_{ox}} \varphi_S + \frac{\tilde{C}_{box}}{C_{fox}} V_{fbb} + \left[1 - \frac{\tilde{C}_{box}}{2C_{si}}\right] \frac{qN_{ch}t_{si}}{C_{fox}} \quad \ldots (2.6)$$

To simplify V_{SL}, we substitute V_{th0} in V_{SL} as follows,

$$V_{SL} = \frac{\tilde{C}_{ox}}{\tilde{C}_{box}} (V_{GS} - V_{th\,0}) + \varphi_S \quad \ldots (2.6.a)$$

The front channel surface potential V_{sf} has a minimum value $V_{sf,min}$, say at $y=y_o$, which can be found by solving the eqn.

$$\left|\frac{dV_{sf}(y)}{dy}\right|_{y = y_o} = 0 \quad \text{and is given by}$$

$$y_0 = \frac{\ell}{2} \ln \left[\frac{(V_{bi} - V_{SL})e^{(L/\ell)} - (V_{bi} + V_{DS} - V_{SL})}{V_{bi} + V_{DS} - V_{SL}) - (V_{bi} - V_{SL})e^{(-L/\ell)}}\right] \quad \ldots .(2.7)$$

However, when $V_{DS} << (V_{bi} - V_{SL})$, y_0 may be approximated as follows :

$$y_0 \approx \frac{\ell}{2} \ln \left[\frac{(V_{bi} - V_{SL})e^{(L/\ell)} - (V_{bi} - V_{SL})}{V_{bi} - V_{SL}) - (V_{bi} - V_{SL})e^{(-L/\ell)}}\right]$$

$$= \frac{\ell}{2} \ln e^{(L/\ell)} = L/2 \; ; \quad \ldots\ldots\ldots .(2.7.a)$$

So, $V_{sf\,min}$ can be obtained analytically from eqn. (2.5) for $y = y_0$:

$$V_{sf\,min} = V_{SL} + \left[2\left(V_{bi} - V_{SL}\right) + V_{DS}\right]\frac{\sinh(L/2\ell)}{\sinh(L/\ell)} \; ; \quad \ldots . \; (2.7.b)$$

To determine the threshold voltage, we assume that $V_{sf\,min}$ is equal to φ_S or $2\varphi_B$ at $V_{GS} = V_{th}$ (Threshold voltage). V_{th} or Threshold voltage is defined as the gate voltage which causes $V_{sf\,min}$ to equal to $2\varphi_B$ or

$$\left(2 \frac{kT}{q} \ln \frac{N_{ch}}{n_i} \right)$$

For $V_{GS} = V_{th}$,

$$V_{sf\,min} = \varphi_S = V_{SL} + \left[2(V_{bi} - V_{SL}) + V_{DS}\right] \frac{\sinh(L / 2\ell)}{\sinh(L / \ell)}$$

$$\Rightarrow \varphi_S = \frac{\tilde{C}_{ox}}{\tilde{C}_{box}} \left(V_{th} - V_{tho}\right) + \left[(2V_{bi} + V_{DS}) - 2\left\{ \varphi_S + \frac{\tilde{C}_{ox}}{\tilde{C}_{box}} \left(V_{th} - V_{tho}\right) \right\} \right] \times \frac{\sinh(L/2\ell)}{\sinh(L/\ell)} + \varphi_S$$

Here we can define $(V_{tho} - V_{th})$ as the Threshold Voltage Shift ΔV_{th} and solve for it,

$$\frac{\tilde{C}_{ox}}{\tilde{C}_{box}} \Delta V_{th} \left[1 - \frac{2 \sinh(L / 2\ell)}{\sinh(L / \ell)} \right] = \left[2(V_{bi} - \varphi_S) + V_{DS}\right] \frac{\sinh(L / 2\ell)}{\sinh(L / \ell)}$$

$$\Rightarrow \Delta V_{th} = \frac{\tilde{C}_{box}}{\tilde{C}_{ox}} \frac{\left[2(V_{bi} - \varphi_S) + V_{DS}\right] \sinh(L / 2\ell)}{\left[\sinh(L / \ell) - 2 \sinh(L / 2\ell)\right]}$$

$$= \eta \frac{\left[2(V_{bi} - \varphi_S) + V_{DS}\right]}{2 \cosh(L / 2\ell) - 2} \qquad \ldots\ldots\ldots\ldots\ldots \quad (2.8)$$

where , $\eta = \frac{\tilde{C}_{box}}{\tilde{C}_{ox}}$

When $l << L$, the term $1/(2\cosh(L/2l)-2)$ can be approximated as $(\exp^{-L/2l} + 2\exp^{-L/l})$ [14] and threshold voltage shift can be expressed as

$$\Delta V_{th} = \eta\left[2(V_{bi} - \varphi_S) + V_{DS}\right]\left(\exp^{-L/2\ell} + 2\exp^{-L/\ell}\right) \quad \ldots\ldots (2.8.a)$$

It is worth noting that in case of a bulk-model MOSFET, the general expression for threshold voltage shift is[14]

$$\Delta V_{th} = \frac{\left[2(V_{bi} - \varphi_S) + V_{DS}\right]}{2\cosh(L/2\ell) - 2} \quad \ldots\ldots\ldots (2.9)$$

Where, l is expressed as

$$\sqrt{\frac{\varepsilon_{si} X_{dep}}{\gamma C_{fox}}}$$

So we see that the threshold voltage shift ΔV_{th} of a SOI Mosfet when compared with that of a bulk MOSFET only differs by a multiplication factor η and characteristic length l. Since $t_{si} < x_{dep}$, (x_{dep} is the depletion layer thickness) the value of l for a SOI MOSFET is less than that of a bulk MOSFET. So it can be easily deduced that the threshold voltage roll-off in FD SOI is less than that in the bulk as predicted by a shorter characteristic length in FDSOI. According to eqn. (2.8.a), a higher channel doping and thinner t_{fox}, t_{si} and t_{box} will help to suppress the V_{th} roll-off.

2.4 STATIC CHARACTERISTIC MODEL FOR SUBMICRON/DEEP SUBMICRON SOI MOSFET

2.4.1 INVERSION CHARGE PER UNIT AREA

In order to produce a complete I-V model of a FDSOI-MOSFET , we firstly develop the expression of " free inversion areal charge density" Q_m , in terms of gate and drain voltages.

The 1-D effective gate-channel capacitance, C_{gc} can be written as[16],

$$C_{gc} = -\frac{\partial Q_m}{\partial V_{GS}} = -\frac{\partial Q_{GS}}{\partial V_{GS}} \times \frac{\partial Q_m / \partial V_{sf}}{\partial Q_{GS} / \partial V_{sf}}$$

$$\approx \frac{C_{fox} C_i}{\eta^* C_{fox} + C_i} \qquad \ldots\ldots\ldots\ldots (2.10)$$

Where , C_i is the inversion layer capacitance and is given as $-\partial Q_m/\partial V$

C_{fox} is the front oxide capacitance

$\eta^* = 1 + Csi / Cfox$

Csi is the silicon film capacitance

The inversion layer capacitance, C_i can be found using the charge sheet model, which assumes that all the mobile charges are residing at the oxide-silicon interface as if the inversion layer were a two-dimensional sheet.

From 1-D Poisson's equation, we can obtain

$$\frac{d^2V}{dx^2} = \frac{qN_{ch}}{\varepsilon_{si}}\left[\exp\left(\frac{V - 2\varphi_B - V_{CS}}{V_t}\right) + 1\right] \quad \ldots\ldots\ldots (2.11)$$

where, V is the potential

V_{CS} is the channel source potential

V_t is thermal voltage, kT/q

By multiplying both sides of eqn. (2.11) with dV/dx and using the identity :

$$\frac{1}{2}\frac{d}{dx}\left(\frac{dV}{dx}\right)^2 = \frac{dV}{dx}\frac{d^2V}{dx^2}$$

we have,

$$\frac{1}{2}\frac{d}{dx}\left(\frac{dV}{dx}\right)^2 = \frac{qN_{ch}}{\varepsilon_{si}}\frac{d}{dx}\left\{V + V_t \exp\left[(V - 2\varphi_B - V_{CS}) / V_t\right]\right\}$$

Integrating the above equation with the boundary conditions $V(x=0) = V_{sf}$ and $V(x=t_{si}) = V_{sb}$, we get the expression for electric field , E(x)

$$\frac{dV}{dx} = E(x)$$

$$= \sqrt{\frac{2qN_{ch}}{\varepsilon_{si}}\left[(V_{sf} - V_{sb}) + V_t\left\{\exp\left(\frac{V_{sf} - 2\varphi_B - V_{CS}}{V_t}\right)\right\} - \exp\left(\frac{V_{sb} - 2\varphi_B - V_{CS}}{V_t}\right)\right]}$$

$\ldots\ldots\ldots\ldots (2.12)$

The free inversion charge density is

$$Q_m = -q\int_0^{tsi} ndx = -qN_{ch}\int_{Vsf}^{Vsb} \frac{\exp\left(\frac{V - 2\varphi_B - V_{CS}}{V_t}\right)}{E} dV$$

$$= qN_{ch}\left[\frac{\exp\left(\frac{V_{sf} - 2\varphi_B - V_{CS}}{V_t}\right) - \exp\left(\frac{V_{sb} - 2\varphi_B - V_{CS}}{V_t}\right)}{E}\right] \quad \ldots (2.13)$$

The inversion capacitance per unit area, C_i is defined as

$$C_i = \partial Q_m / \partial V_{sf}$$

From eqns. (2.12) and (2.13), we get

$$Ci = \frac{qN_{ch}\exp\left(\frac{V_{sf} - 2\varphi_B - V_{CS}}{V_t}\right)}{\sqrt{\frac{2qN_{ch}}{\varepsilon_{si}}}\left[V_t\left\{\exp\left(\frac{V_{sf} - 2\varphi_B - V_{CS}}{V_t}\right) - \exp\left(\frac{V_{sb} - 2\varphi_B - V_{CS}}{V_t}\right)\right\} + V_{sf} - V_{sb}\right]}$$

$$\ldots\ldots\ldots\ldots\ldots\ldots (2.14)$$

In the weak inversion region, $V_{sf} < (2\varphi_B + V_{CS})$ and $V_{sb} < (2\varphi_B + V_{CS})$; therefore eqn.(2.14) can be simplified as,

$$Ci = C'_d \exp\left(\frac{V_{sf} - 2\varphi_B - V_{CS}}{V_t}\right) \qquad \ldots\ldots\ldots\ldots\ldots\ldots (2.15)$$

where,

$$C'_d = \frac{qN_{ch}}{\sqrt{2qN_{ch}(V_{sf} - V_{sb}) / \varepsilon_{si}}}$$

In depletion and weak inversion regions, the free inversion areal charge density Q_m is almost zero and the front surface potential is constant from source to drain so that it can be taken as

$$V_{sf} = 2\varphi_B + \frac{\left[V_{GS} - (V_{th0} - \Delta V_{th})\right]}{\eta}$$

With this expression of V_{sf}, eqn. (2.15) now becomes,

$$Ci = C'_d \exp\left(\frac{V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}}{\eta V_t}\right) \qquad \ldots\ldots\ldots (2.16)$$

Here, $\eta = \dfrac{\tilde{C}_{box}}{\tilde{C}_{ox}}$

While the eqn. (2.16) is valid in the weak inversion region, it can still be substituted in eqn.(2.10) to obtain C_{gc} in the strong inversion region, because in that region,depletion layer and inversion layer capacitances are larger than the gate oxide capacitance, so that C_{gc} can be taken as C_{fox} [17] and so eqn. (2.16) does not effect the accuracy of eqn. (2.10).

Substituting eqn. (2.16) into eqn. (2.10), we get,

$$C_{gc} = -\frac{\partial Q_m}{\partial V_{GS}} = \frac{C_{fox}\tilde{C}_d \exp\left[\frac{V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}}{\eta V_t}\right]}{\eta^* C_{fox} + \tilde{C}_d \exp\left[\frac{V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}}{\eta V_t}\right]}$$

$$= \frac{\tilde{C}_d \exp\left[\frac{V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}}{\eta V_t}\right]}{\eta^*\left[1 + \frac{\tilde{C}_d}{\eta^* C_{fox}} \exp\left[\frac{V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}}{\eta V_t}\right]\right]} \quad \ldots\ldots (2.17)$$

Now integrating the above equation with respect to V_{GS} gives,

$$-Q_m = \int \frac{C'_d \exp\left[\frac{V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}}{\eta V_t}\right]}{\eta^*\left[1 + \frac{C'_d \exp\left[\frac{V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}}{\eta V_t}\right]}{\eta^* C_{fox}}\right]} dV_{GS}$$

$$= \eta C_{fox} V_t \int \frac{C'_d \exp\left[\dfrac{V_{GS} - \left(V_{th0} - \Delta V_{th}\right) - \eta V_{CS}}{\eta V_t}\right]}{\eta\eta^* C_{fox} V_t \left[1 + \dfrac{C'_d \exp\left[\dfrac{V_{GS} - \left(V_{th0} - \Delta V_{th}\right) - \eta V_{CS}}{\eta V_t}\right]}{\eta^* C_{fox}}\right]} dV_{GS}$$

Which is in the form of $\int f'(x) / f(x) = \ln f(x)$;

So we get,

$$-Q_m = \eta C_{fox} V_t \ln\left[1 + \frac{C'_d \exp\left[\dfrac{V_{GS} - \left(V_{th0} - \Delta V_{th}\right) - \eta V_{CS}}{\eta V_t}\right]}{\eta^* C_{fox}}\right]$$

$$= \eta C_{fox} V_t \ln\left[1 + \frac{C_i}{\eta^* C_{fox}}\right] \qquad \ldots\ldots\ldots\ldots (2.18)$$

This is the general expression of free inversion areal charge density, Q_m, which is valid in weak, moderate and strong inversions. Derivation of Q_m, of course, involved a drastic approximation which makes the formulation of a comprehensive I-V model possible.

Now in case of strong inversion, $V_{GS} >> (V_{th0} - \Delta V_{th}) + \eta V_{CS}$ and so we can write,

$$- Q_m \approx \eta\, C_{fox} V_t \ln\left[\frac{C_i}{\eta^* C_{fox}}\right]$$

$$\approx \eta\, C_{fox} V_t \ln\left[\exp\left\{\frac{V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}}{\eta\, V_t}\right\}\right]$$

$$= C_{fox}\left[V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}\right] \qquad \ldots\ldots (2.19)$$

In the weak inversion region , where $V_{GS} << (V_{th0} - \Delta V_{th}) + \eta V_{CS}$, eqn. (2.18) can be approximated as,

$$- Q_m \approx \eta\, C_{fox} V_t \times \frac{C_i}{\eta^* C_{fox}}$$

$$= \frac{\eta\, V_t}{\eta^*} C'_d \exp\left\{\frac{V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}}{\eta\, V_t}\right\} \qquad \text{-------} (2.20)$$

2.4.2 DRAIN CURRENT MODEL

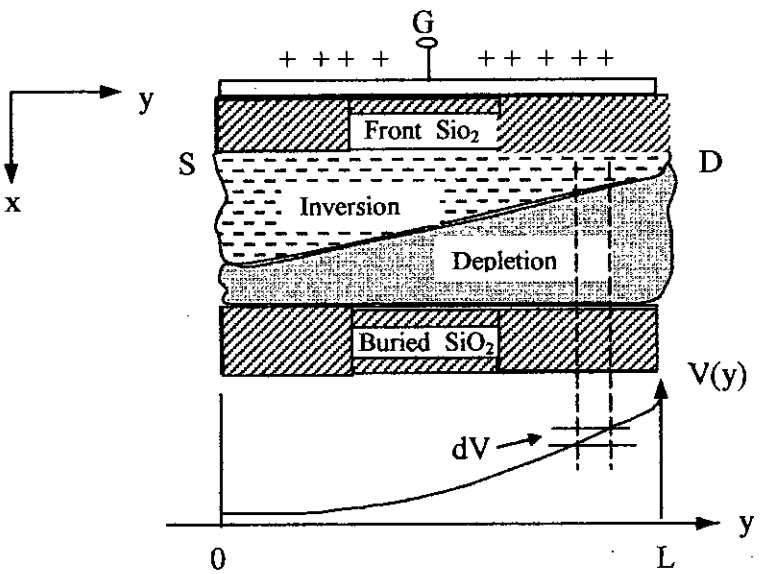


Fig. 2.6 Schematic view of the n-channel region of a SOI-Mosfet under drain bias and the variation of voltage V(y) along the conducting channel.

Since SOI mosfets are a potential candidate for the future ULSI circuitry, it is important to model the current-voltage or I-V characteristics of SOI devices with a view to exploiting their proper application. Here we develop a physics based complete but simple I-V model for an n-channel SOI-Mosfet.

The drain current of any MOS device consists of drift and diffusion components of current as expressed below,

$$I_{DS} = -W\mu Q_m \frac{dV}{dy} - W\mu V_t \frac{dQ_m}{dy} \quad \ldots\ldots\ldots (2.21)$$

here, W = effective channel width

μ = mobility of electron

Here we ignored the current component due to the gradient of electron temperature. The first term on the right hand side of eqn. (2.21) is the drift component and the second term is thediffusion component.

2.4.2.1 Effective Mobility of Electrons in the Channel

Mobility, μ is in fact a complicated function of local electric field and position. The vertical electric field that arises due to the presence of gate voltage, V_{GS} can affect the carrier mobility and this effect can be incorporated by the use of μ^0_n in place of μ_0, the maximum low-field mobility where [18]

$$\mu_n^0 = \frac{\mu_0}{1 + \theta(V_{GS} - V_{th})} \qquad \ldots\ldots\ldots\ldots \quad (2.22)$$

here, θ is a fitting parameter,

V_{th} is the threshold voltage.

An important role that can be played by θ is that the effect of source/drain resistance can be lumped into it and so the need for extra elements in circuit simulation can easily be eliminated[19]. Here to mention that as device dimensions are scaled down to the submicrometer regime , the parasitic source/drain series resistances become increasingly significant. They are especially high in fully depleted SOI owing to its thin film nature[20].

Another important modification of carrier-mobility is to be carried out due to the phenomenon of velocity overshoot. As carriers traverse along the conducting channel, they gain energy from the electric field, but their motion is frequently interrupted by collisions with impurities, phonons, crystal defects or other carriers. As the channel length decreases carriers that travel along the channel gain energy while suffer less collisions. Therefore the transient velocity may overshoot its steady-state value. This is the general definition of velocity overshoot phenomenon[18].

At a fixed drain bias, as channel length decreases, the channel electric fields increase and the electric fields in the region near the source also increase. A steep increase of the channel electric field near the source induces the non-local transport effect and so enhances the carrier velocity in the source region. In other words, carriers can gain much more energy in the source-end channel and the velocity overshoot effect becomes apparent. But as the carriers travel a specified distance along the channel, the electron temperature begins to rise and the scattering between mobile electrons and lattice increases, while in turn decreases the carrier velocity, i.e. velocity overshoot effect gradually vanishes. In fact, carrier velocity overshoot at the drain end does not lead to any observable drain current increase as it only affects the carrier distribution in the post-saturation region [21]. Incorporating the effects at small y (i.e. near the source) and at large y (i.e. near the drain), the effective mobility in the channel is approximated as,

$$\mu_{eff} \approx \frac{\mu_n^0}{1 + \beta E_y y \exp(-y / L_v) + \alpha E_y (1 - \exp(-y / L_v))} \quad \ldots\ldots (2.23)$$

where, $E_y = \frac{dV(y)}{dy}$ is the channel electric field

L_v is a fitting constant

β is equal to $2/(5U_l)$ and U_l is the equlibrium electron thermal voltage

$\frac{1}{\alpha} = E_c$, the critical field.

2.4.2.2 WEAK INVERSION AND SUBTHRESHOLD CURRENT MODEL :

In weak inversions , a low concentration of electrons are introduced in the channel and the surface potential which has a smaller magnitude , remains constant from source to drain. So the drift component of drain current is negligible in this case and the drain current is dominated by the diffusion current. So from eqns. (2.21) and (2.22) we get,

$$I_{DS} = -W\mu V_t \frac{dQ_m}{dy} \qquad \ldots\ldots\ldots\ldots \quad (2.24)$$

For weak inversions,

$$Q_m = -Q'_m \exp\left\{\frac{V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}}{\eta V_t}\right\};$$

$$\text{here, } Q'_m = \frac{\eta V_t}{\eta^*} C'_d$$

So the above equation becomes,

$$I_{DS}\left[1 + \beta E_y y \exp(-y / L_v) + \alpha E_y (1 - \exp(-y / L_v))\right] dy =$$

$$W\mu_n^0 Q'_m \exp\left\{\frac{V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}}{\eta V_t}\right\} \quad \ldots (2.25)$$

Integrating from y=0 to y=L yields,

$$I_{DS}\left[L + \alpha V_{DS} + E_y(0)\left\{\beta L_v^2\left(1 - \exp(-L / L_v)\right) - \beta L_v L \exp(-L / L_v) - \alpha L_v\left(1 - \exp(-L / L_v)\right)\right\}\right]$$

$$= W\mu_n^0 Q'_m V_t \exp\left\{\frac{V_{GS} - (V_{th0} - \Delta V_{th})}{\eta V_t}\right\} \times \left[1 - \exp\left(-\frac{V_{DS}}{V_t}\right)\right]$$

$$\ldots (2.26)$$

Since $L >> L_V$, the above equation can be approximated as,

$$I_{DS} = \frac{W\mu_n^0 Q'_m V_t \exp\left\{\frac{V_{GS} - (V_{th0} - \Delta V_{th})}{\eta V_t}\right\} \times \left[1 - \exp\left(-\frac{V_{DS}}{V_t}\right)\right]}{L + \alpha V_{DS} + E_y(0)\left(\beta L_v^2 - \alpha L_v\right)} \quad \ldots (2.27)$$

Here, $E_y(0)$ is the channel electric field as $y = 0$ and we used it here since at a distance of $y = L_V$, the electric field will not deviate very much from the electric field at $y = 0$.

The factor that accounts for velocity overshoot is $E_y(0)\{ \beta L^2_V - \alpha L_V \}$ and this being a negative term causes the drain current without overshoot to increase a bit further.

The solution for I_{DS} considering velocity overshoot is a complicated one. Let us here determine the expression for $E_y(0)$ in terms of I_{DS}.

We know from eqn. (2.21), the diffusion current is

$$I_{DS} = -W\mu_n^0 V_t \frac{dQ_m}{dy}$$

$$= -W\mu_n^0 V_t \frac{dQ_m}{dV_{GS}} \cdot \frac{dV_{GS}}{dy}$$

$$= \frac{W\mu_n^0 V_t C'_d}{\eta^*} \exp\left[\frac{V_{GS} - \left(V_{th0} - \Delta V_{th}\right) - \eta V_{CS}}{\eta V_t}\right] E_y(y)$$

At $y = 0$, $V_{CS} = 0$ and $E_y(y) = E_y(0)$; so that

$$I_{DS} = \frac{W\mu_n^0 V_t C'_d}{\eta^*} \exp\left[\frac{V_{GS} - \left(V_{th0} - \Delta V_{th}\right)}{\eta V_t}\right] E_y(0)$$

$$\Rightarrow E_y(0) = \frac{I_{DS}}{\frac{W\mu_n^0 V_t C'_d}{\eta^*} \exp\left[\frac{V_{GS} - \left(V_{th0} - \Delta V_{th}\right)}{\eta V_t}\right]} \quad \ldots\ldots\ldots (2.28)$$

Solving for I_{DS} from eqns.(2.27) and (2.28) we get,

$$I_{DS} = \frac{-B + \sqrt{B^2 - 4AC}}{2A} \quad \ldots\ldots\ldots\ldots (2.29)$$

where, $$A = \frac{\beta L_v^2 - \alpha L_v}{\left[\frac{W\mu_n^0 V_t C'_d}{\eta^*}\right] \exp\left\{\frac{V_{GS} - (V_{th0} - \Delta V_{th})}{\eta V_t}\right\}}$$

$$B = L + \alpha V_{DS}$$

$$C = -\left[\frac{W\mu_n^0 \eta V_t^2 C'_d}{\eta^*}\right] \times \exp\left\{\frac{V_{GS} - (V_{th0} - \Delta V_{th})}{\eta V_t}\right\} \times \left[1 - \exp\left(-\frac{V_{DS}}{V_t}\right)\right]$$

This is the required expression for subthreshold current considering the velocity overshoot phenomenon.

2.4.2.3 STRONG INVERSION AND DRAIN CURRENT MODEL FOR A NORMALLY ON SOI MOSFET

In the strong inversion region, the drain current is dominated by the drift current , i.e.

$$I_{DS} \cong -W\mu_{eff} Q_m \frac{dV}{dy} \qquad \ldots\ldots\ldots\ldots\ldots (2.30)$$

By the use of eqn. (2.19) for expression of Q_m in strong inversion, we get

$$I_{DS} = \frac{W\mu_n^0 C_{fox}\left[V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}\right]dv / dy}{1 + \beta E_y y \exp(-y / L_v) + \alpha E_y (1 - \exp(-y / L_v))}$$

$$\Rightarrow I_{DS}\left[1 + \beta E_y y \exp(-y / L_v) + \alpha E_y + \alpha E_y \exp(-y / L_v)\right]dy =$$

$$W\mu_n^0 C_{fox}\left[V_{GS} - (V_{th0} - \Delta V_{th}) - \eta V_{CS}\right]dv$$

Integrating the above equation from $y = 0$ to $y = L$ and simplifying we get,

$$I_{DS}\left[L + \alpha V_{DS} + E_y(0)\left\{\beta L_v^2 - \alpha L_v\right\}\right] = W\mu_n^0 C_{fox} \times$$

$$\left[\left\{V_{GS} - (V_{th0} - \Delta V_{th})\right\}V_{ds} - \frac{\eta}{2} V_{DS}^2\right]$$

$$\Rightarrow I_{DS} = \frac{W\mu_n^0 C_{fox}\left[\left\{V_{GS} - (V_{th0} - \Delta V_{th})\right\}V_{ds} - \frac{\eta}{2} V_{DS}^2\right]}{L + \alpha V_{DS} + E_y(0)\left\{\beta L_v^2 - \alpha L_v\right\}} \quad \ldots\ldots (2.31)$$

Since $(\beta L^2_V - \alpha L_V)$ is negative, this equation tells that the drain current increases as channel length decreases due to overshoot effect. For long channel devices, the velocity overshoot effect can be neglected.

Now from eqn. (2.30) for $y = 0$,

$$I_{DS} = W\mu_n^0 C_{fox}\left\{V_{GS} - (V_{th0} - \Delta V_{th})\right\}E_y(0) \quad \ldots\ldots\ldots (2.32)$$

From eqns. (2.31) and (2.32) we can solve for I_{DS} as

$$I_{DS} = \frac{-A_2 + \sqrt{A_2^2 - 4A_1A_3}}{2A_1} \quad \ldots\ldots\ldots (2.33)$$

Where,

$$A_1 = \frac{\beta L_v^2 - \alpha L_v}{W\mu_n^0 C_{fox} V_{GST}}$$

$$A_2 = L + \alpha V_{DS}$$

$$A_3 = -W\mu_n^0 C_{fox}\left[V_{GST}V_{DS} - \frac{\eta}{2}V_{DS}^2\right]$$

$$V_{GST} = V_{GS} - (V_{th0} - \Delta V_{th})$$

When V_{DS} reaches the saturation voltage V_{DSAT} and beyond, pinch-off occurs and the device is operated in the saturation mode. Then the saturation drain current becomes,

$$I_{DSAT} = \frac{-A'_2 + \sqrt{A'^2_2 - 4A'_1A'_3}}{2A'_1} \qquad \text{. . . . . (2.34)}$$

where,

$$A'_1 = \frac{\beta L_v^2 - \alpha L_v}{W\mu_n^0 C_{fox} V_{GST}}$$

$$A'_2 = L + \alpha V_{DSAT}$$

$$A'_3 = -W\mu_n^0 C_{fox}\left[V_{GST}V_{DSAT} - \frac{\eta}{2}V_{DSAT}^2\right]$$

$$V_{GST} = V_{GS} - (V_{th0} - \Delta V_{th})$$

The saturation drain voltage, V_{DSAT} is generally given as,

$V_{DSAT} = V_{GS} - (V_{th0} - \Delta V_{th})$

CHAPTER – 3

RESULTS AND DISCUSSION

Following the theoretical analysis presented in chapter-2, the models for various significant quantities like front surface potential, threshold voltage and threshold voltage shift, drain current etc. are simulated and tested on a microcomputer by computer programs. These programs written in Borland C^{++}, provide a lucid and flexible simulation-environment so that each model can be easily checked and tested from diverse point of view.

Firstly we simulate the expression for front-surface electric-potential $V_{sf}(y)$, as presented in equation (2.5). The device used for the study is a fully-depleted n-channel SOI MOSFET with a channel doping of 10^{17} cm^{-3}. The silicon-film-thickness of this device is 85nm with front oxide and buried oxide thickness of 10nm and 400nm respectively. The first simulation is set to trace the front surface potential, $V_{sf}(y)$ along the channel length or in the direction of y; (in this case we have chosen a channel length of 0.3 μm). The variation of surface potential is calculated for three different source- to- drain voltages, e.g. V_{DS}=50mv, V_{DS}=1V and V_{DS}=2V. As depicted in Fig. 3.1, it is observed that the effective channel length shrinks or contracts as the drain voltage increases. Here we define the 'effective channel length' as the length along the mask-channel where the surface potential is at best 10% higher than the minimum surface potential. This phenomenon i.e. the channel contraction due to increasing drain voltage in a short-channel device is generally termed as *channel length modulation.* This effect has been tested for three different

channel lengths (Fig.3.2), e.g. L=0.6μm, L=0.3μm and L=0.2μm, with a particular value of V_{DS}. The channel modulation by drain voltage is seen to become prominent in short channel devices. This channel-length-modulation effect has been clearly depicted in the following two Figures, Fig. 3.3 and Fig.3.4. In Fig.3.3, the channel-length-modulation has been defined graphically, where effective channel length is $(L - l_s - l_d)$; here L is the mask channel length, l_s is the distance to the nearest point from source where the surface potential is down within the range of 110% of the minimum potential and l_d is the similar distance from drain,(in this connection, we have at first calculated the minimum surface potential $V_{sf,min}$ by the use of eqns. (2.5) and (2.7).

As shown in Fig. 3.4, the modulated channel length goes on in the downward direction as the drain voltage is gradually increased (and this was predicted in Fig.3.1). Also observed is that the modulated channel length becomes very short for the shorter channel device; this may cause serious trouble considering punch-through (merging of drain depletion region with source). So the doping concentration of a shorter channel device has to be increased than that of its longer counterpart.

Simulating the surface-potential model against position along the channel with T_{si} as the parameter reveals an interesting result (Fig. 3.5). A device with larger silicon-film thickness (100nm) has a more contracted or modulated channel length than the one with smaller T_{si}. This is an important finding about silicon film thickness and more of such findings are revealed later in our research.

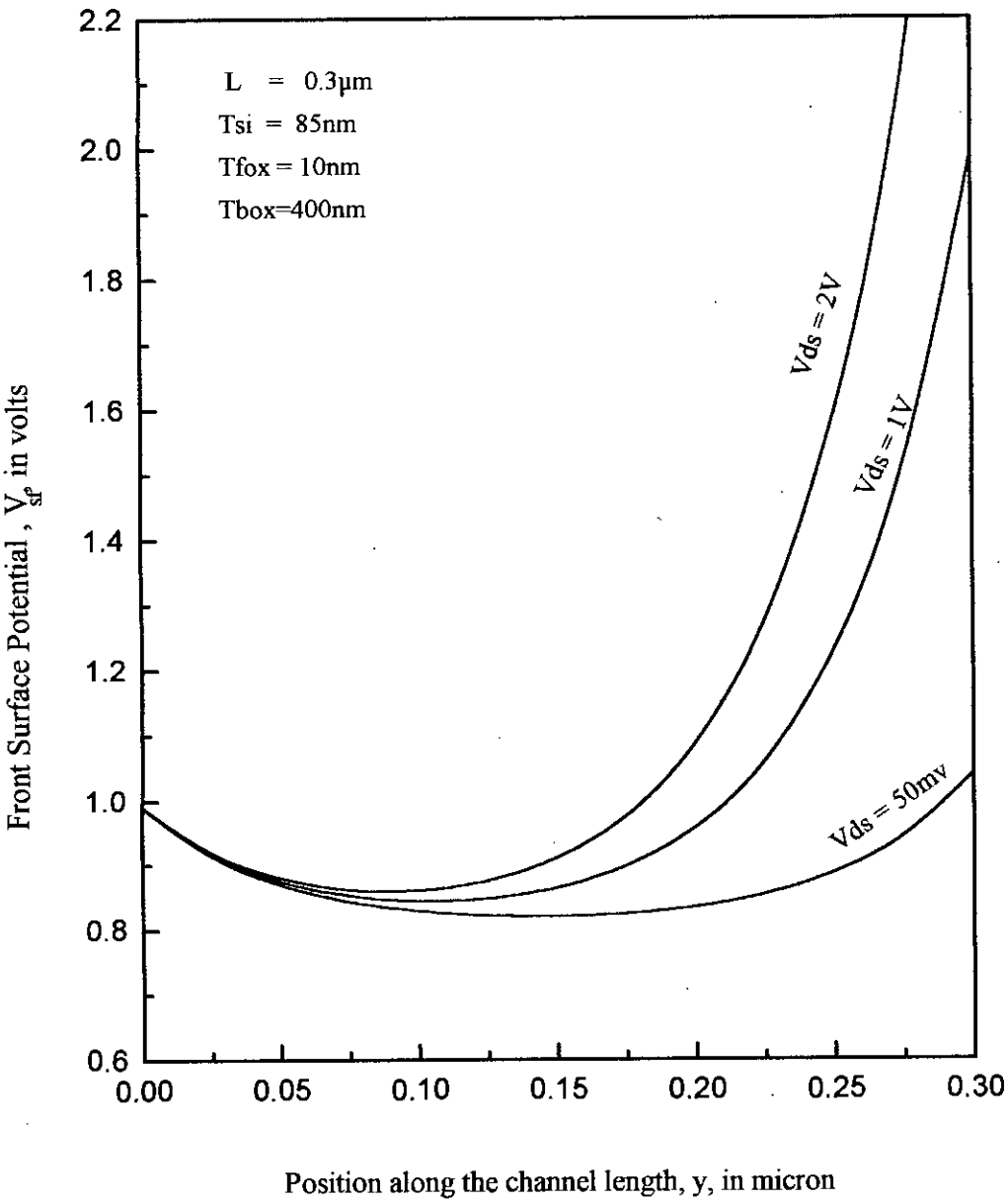


Fig. 3.1 Front surface potential along the channel at Vgs = Vtho for various drain bias

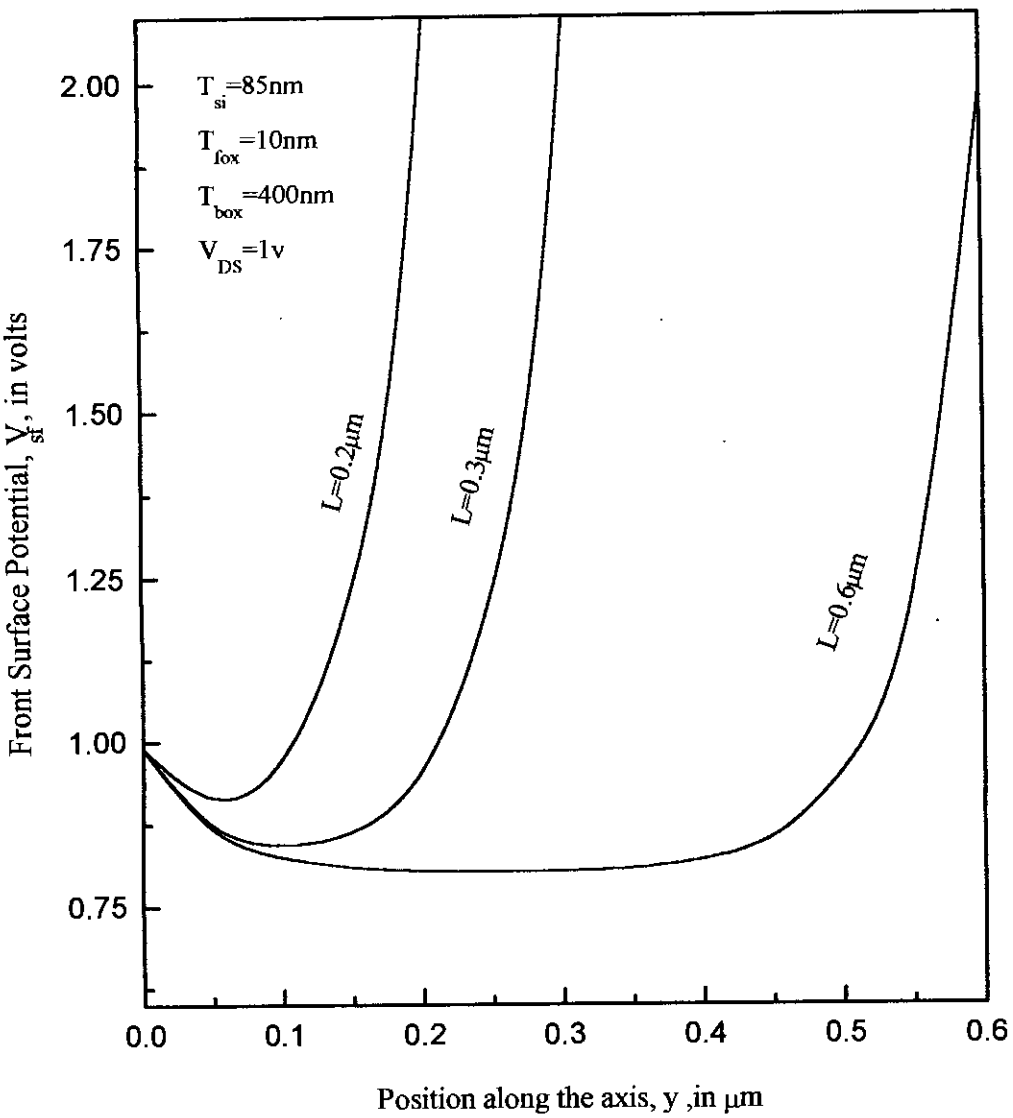


Fig. 3.2 Surface Potential for different channel lengths

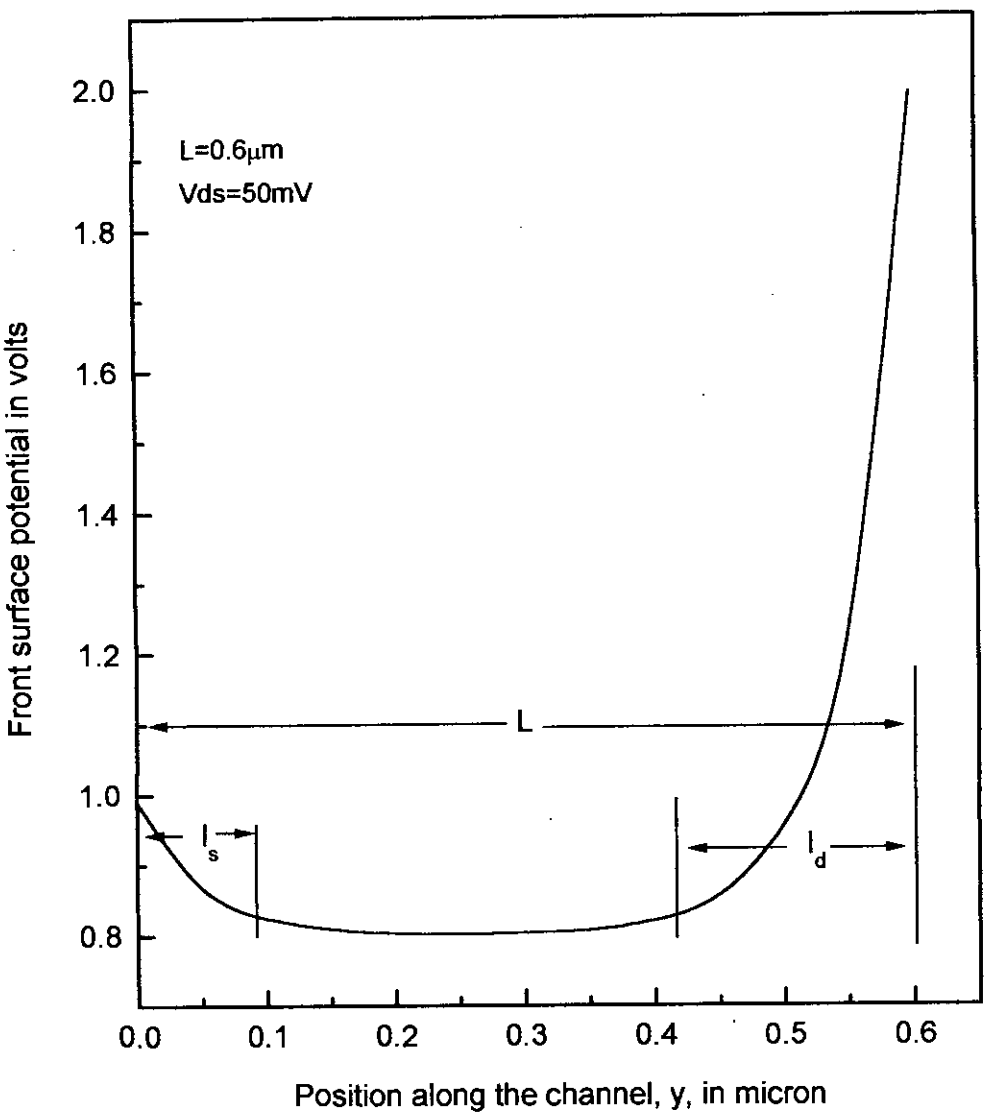


Fig. 3.3 Definition of channel length modulation

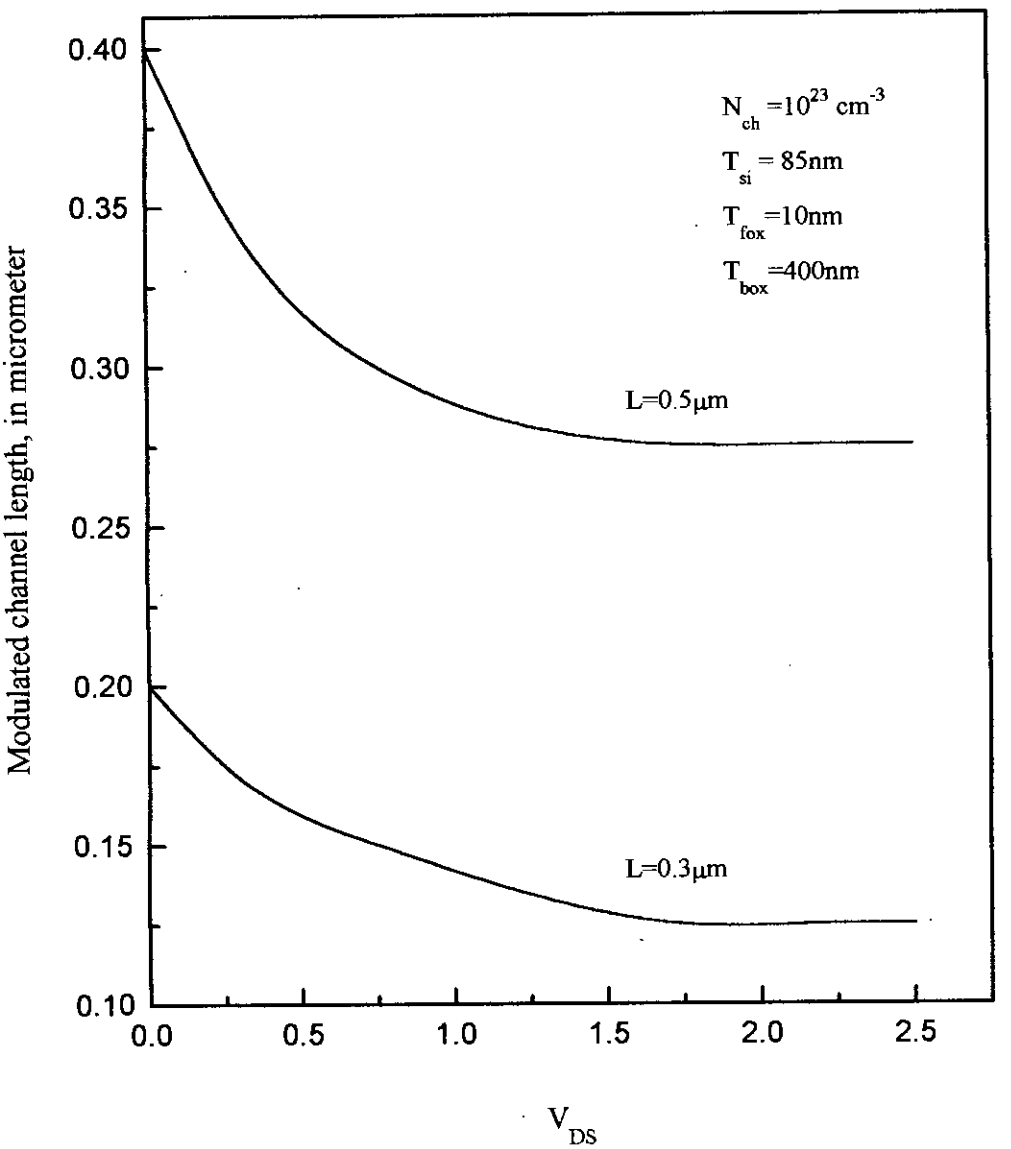


Fig. 3.4 Effect of channel length modulation on as function of drain voltage

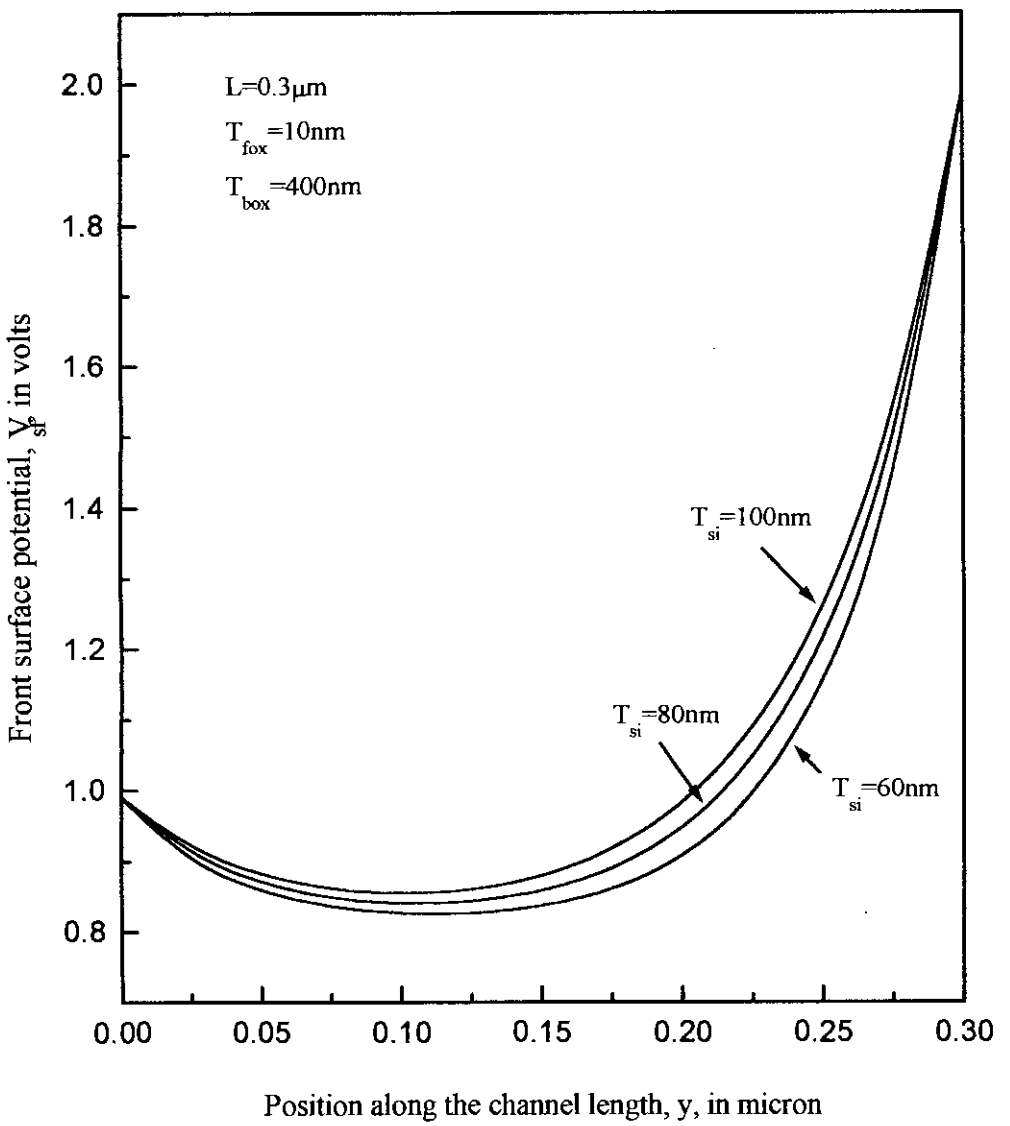


Fig. 3.5 Front surface potential for different silicon film thickness

The SOI threshold voltage model as expressed by equations (2.6) and (2.8), is simulated to observe its dependence on channel length (L), silicon-film-thickness (T_{si}) and drain voltage (V_{DS}). As depicted in Fig. 3.6, threshold voltage, V_{th}, is seriously affected at reduced channel lengths. For the long channel devices, threshold voltage is a fixed quantity; but as the device is continually scaled down, its threshold voltage tends to shift downward, a phenomenon known as *threshold voltage shift* or *threshold voltage roll-off*. A significant relation between threshold voltage of a short-channel device with its silicon-film thickness, T_{si} is observed here; as seen in Fig. 3.6, threshold voltage is more seriously affected in case of a device with larger T_{si} than the one with smaller T_{si}. Here we vary T_{si} from 60nm to 100nm in steps of 20nm each. Thicknesses of the front oxide and buried oxide layers are 10nm and 400nm respectively and the channel doping N_{ch} is 10^{17} cm^{-3}. The degree of doping used here is a reasonable one, since higher channel doping (generally $N_{ch} \geq 5\times10^{16}$ cm^{-3}) is an inevitable tool to avoid punch-through in the deep submicrometer device. The drain voltage used is 50mV. An important choice we make here and also for all the devices throughout the research is for the material of the gate; since the flat-band voltage in case of an n^+ polycrystalline silicon (or polysilicon in short) is a deep-negative quantity (about–1.15 volts), it aids in lowering of the long channel threshold voltage, V_{th0} of the n-channel device (as indicated by equation (2.6)). This is why n^+- polysilicon is selected as the gate material of our devices.

The effect of silicon-film thickness on the threshold voltage is presented in another way (Fig. 3.7). Using the equation (2.8), we calculate the threshold voltage roll-off, ΔV_{th} and plot it against channel length, with T_{si} as the parameter. The figure 3.7 clearly demonstrates the dependence of the ΔV_{th} on T_{si} as predicted before; the device with larger T_{si} shows a higher ΔV_{th} or threshold voltage shift. Smaller T_{si} in fact helps to maintain a higher doping concentration in the channel that in turn is necessary to ensure the fully-depleted condition in the subthreshold regime, especially in case of a very short channel device. Silicon films of larger thickness fail to ensure such condition and so are notoriously prominent in sense of threshold voltage roll-off. So we see here that the shift in threshold voltage from device to device include not only Short Channel Effects (SCE), but also contributions due to T_{si} variations and the thinner the T_{si}, the better the performance.

Threshold voltage variation against effective channel length with drain voltage as the parameter is also simulated, using the same equations involved in the previous simulation (eqn. (2.6) & eqn. (2.8)). The results are depicted in Fig.3.8; here it is seen that the threshold voltage in the submicron devices is a function of not only the channel length or silicon-film thickness, but also the drain voltage, V_{DS}. For a device applied with higher drain voltage shows a higher roll-off in its threshold voltage and this is obviously a result of DIBL or drain induced barrier lowering effect. As the channel length is reduced further, the drain depletion region further strengthens its interaction with the source region and the DIBL effect is more pronounced; in turn the subthreshold performance is hampered and V_{th} is lowered. The same event is simulated in another fashion (Fig. 3.9). Here the threshold voltage-profile is plotted against

drain voltage for two different channel lengths, e.g. L=0.3μm and L=0.5μm. As predicted above, the lower channel length device is associated with lower threshold voltage and this device suffers more for drain voltage variation than the device with longer channel length.

An important relation between the threshold voltage roll-off and the channel doping concentration is studied with care. The eqn. 2.8 is used in this perspective and we reveal (as indicated in Fig. 3.10) that higher doping concentration helps to suppress the *threshold voltage roll-off*, one of the dominant short channel effects (SCE). This action is more prominent in the deep submicron range; the values of doping concentration, N_{ch} we use here are 10^{17} cm^{-3} and 5×10^{17} cm^{-3} and the drain voltage is 50 mV. The curve for lower N_{ch} always resides above that for the higher one and the difference becomes significantly increasing from L=0.3μm to down below.

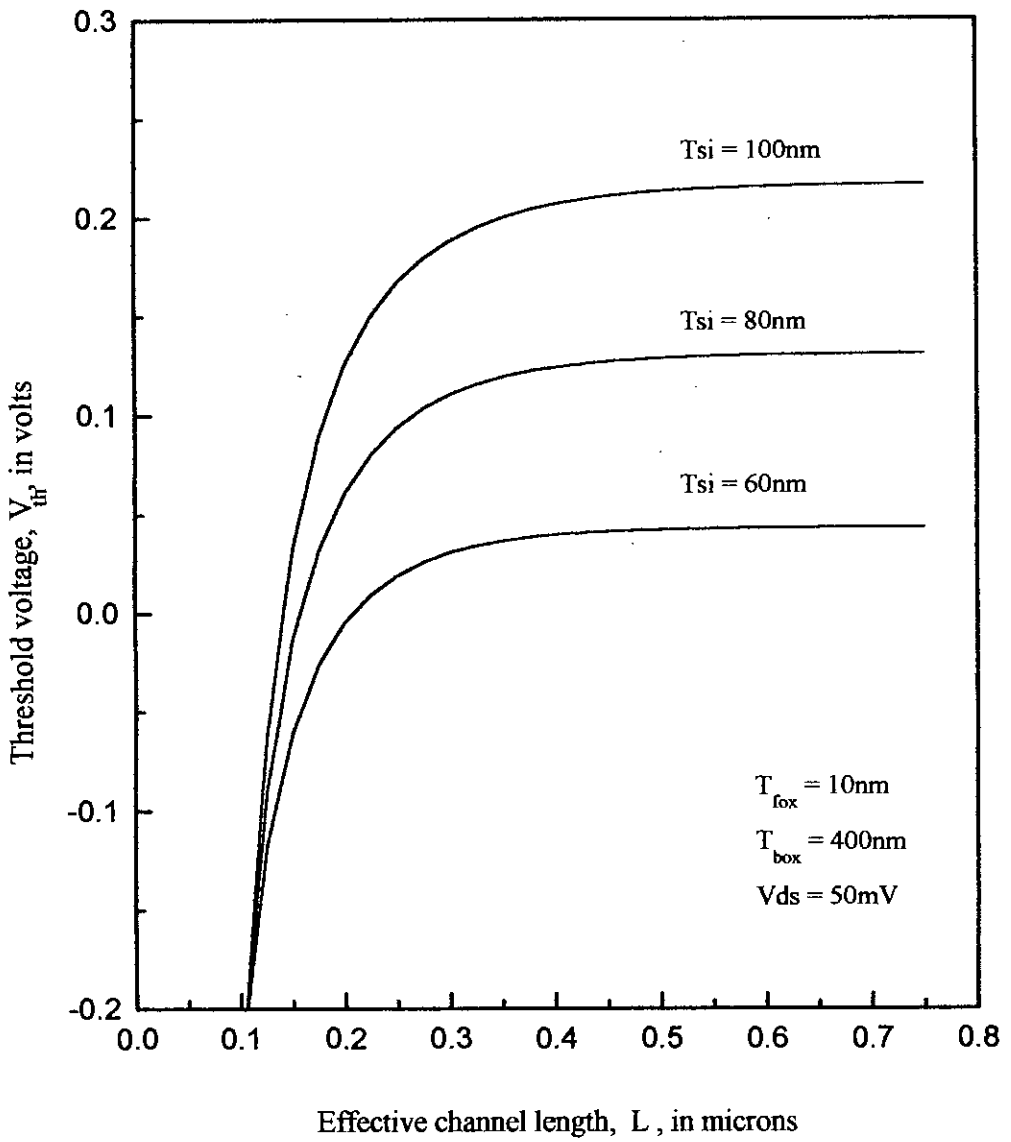


Fig. 3.6 Threshold voltage vs. channel length for different Si-film thickness

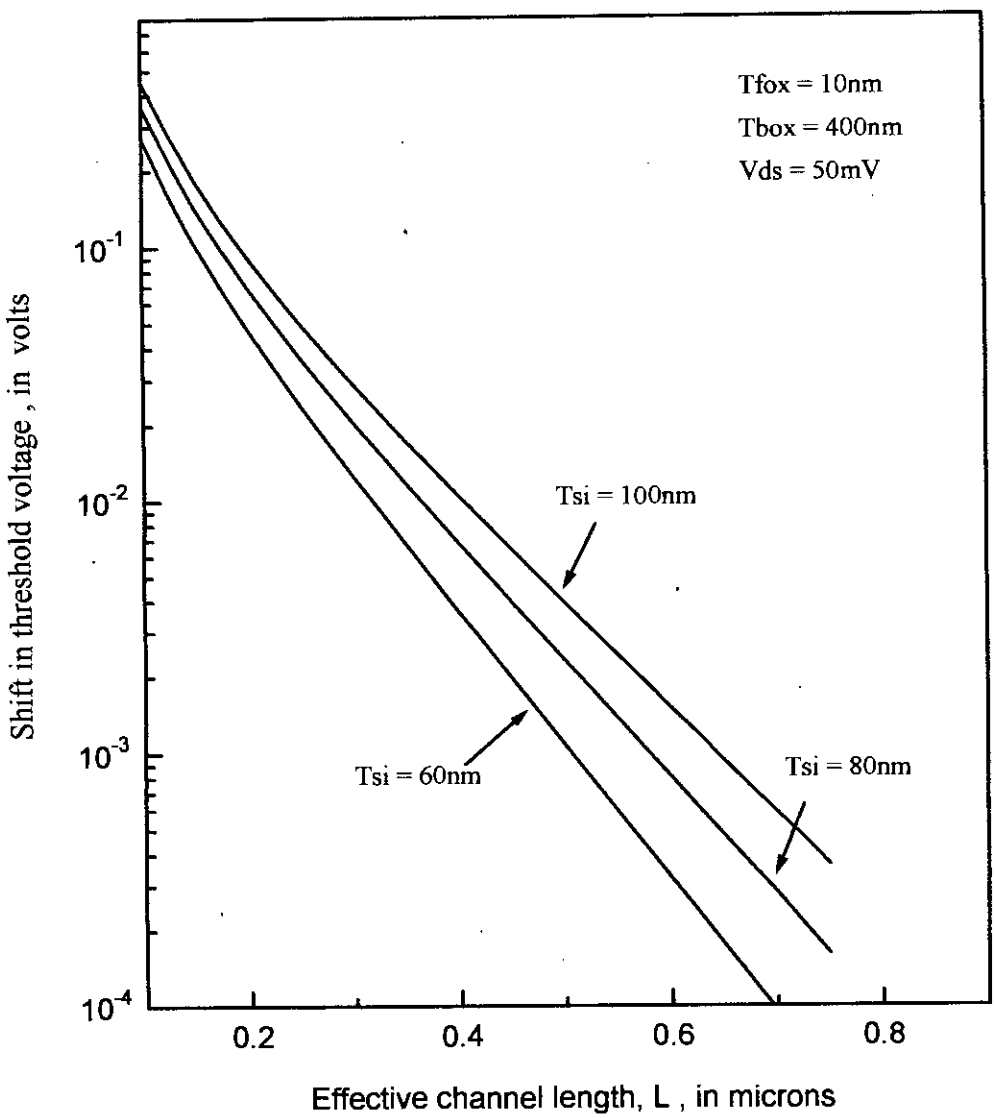


Fig. 3.7 Shift in threshold voltage vs. channel length for various Si-film thickness

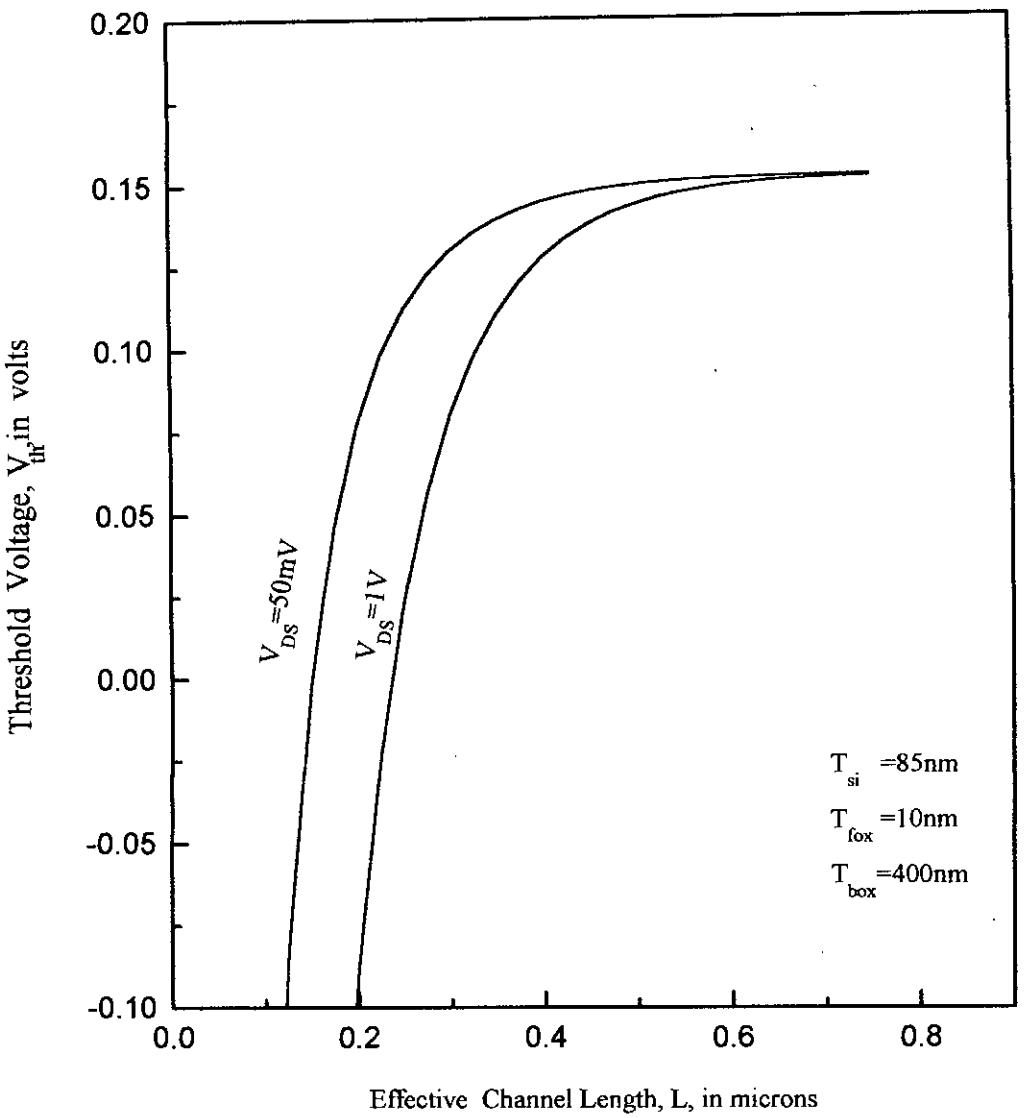


Fig. 3.8 Threshold Voltage vs. Channel Length for different Drain bias

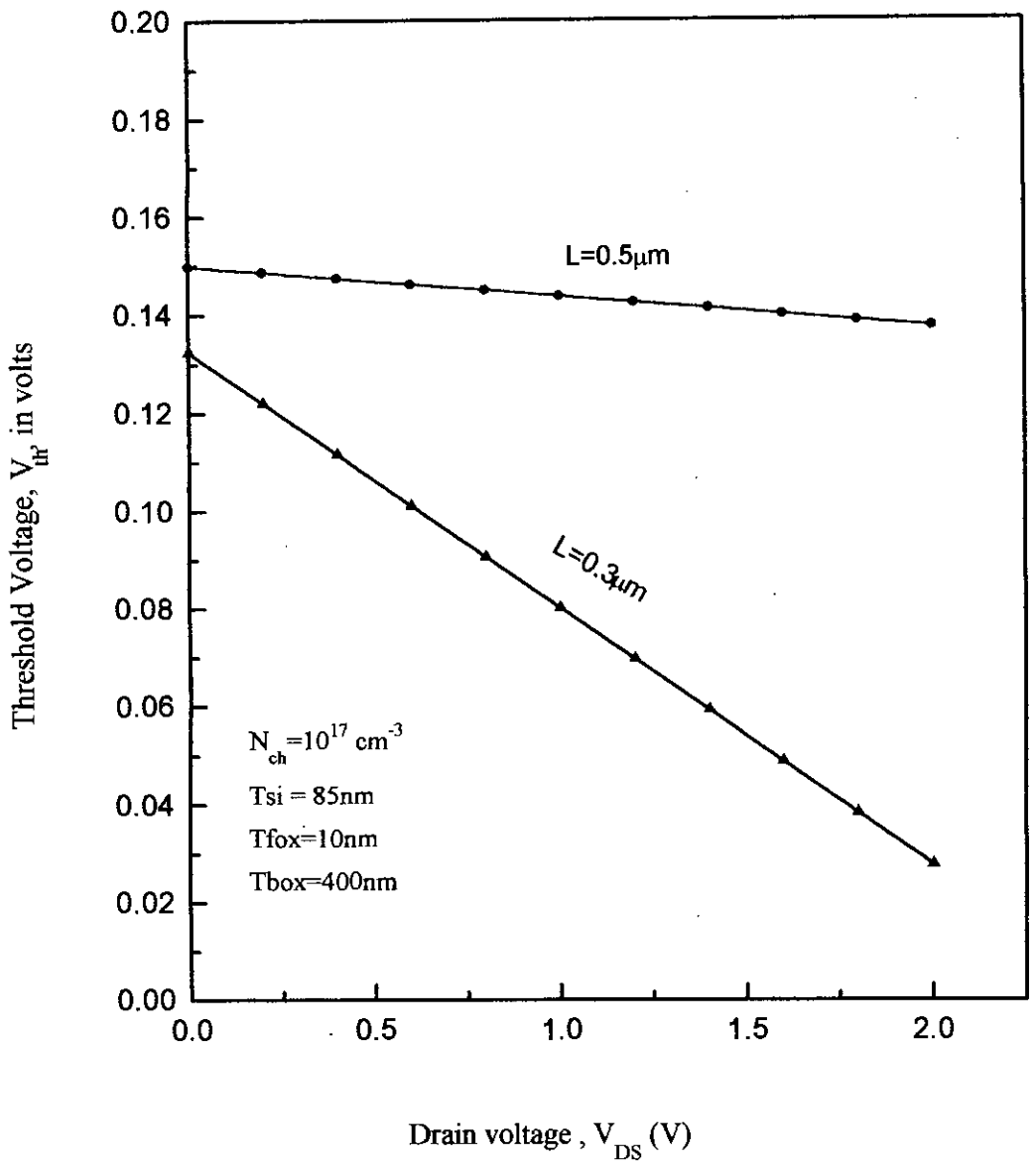


Fig. 3.9 Dependence of the threshold voltage on the drain voltage for 0.3μm and 0.5μm SOI MOSFETs

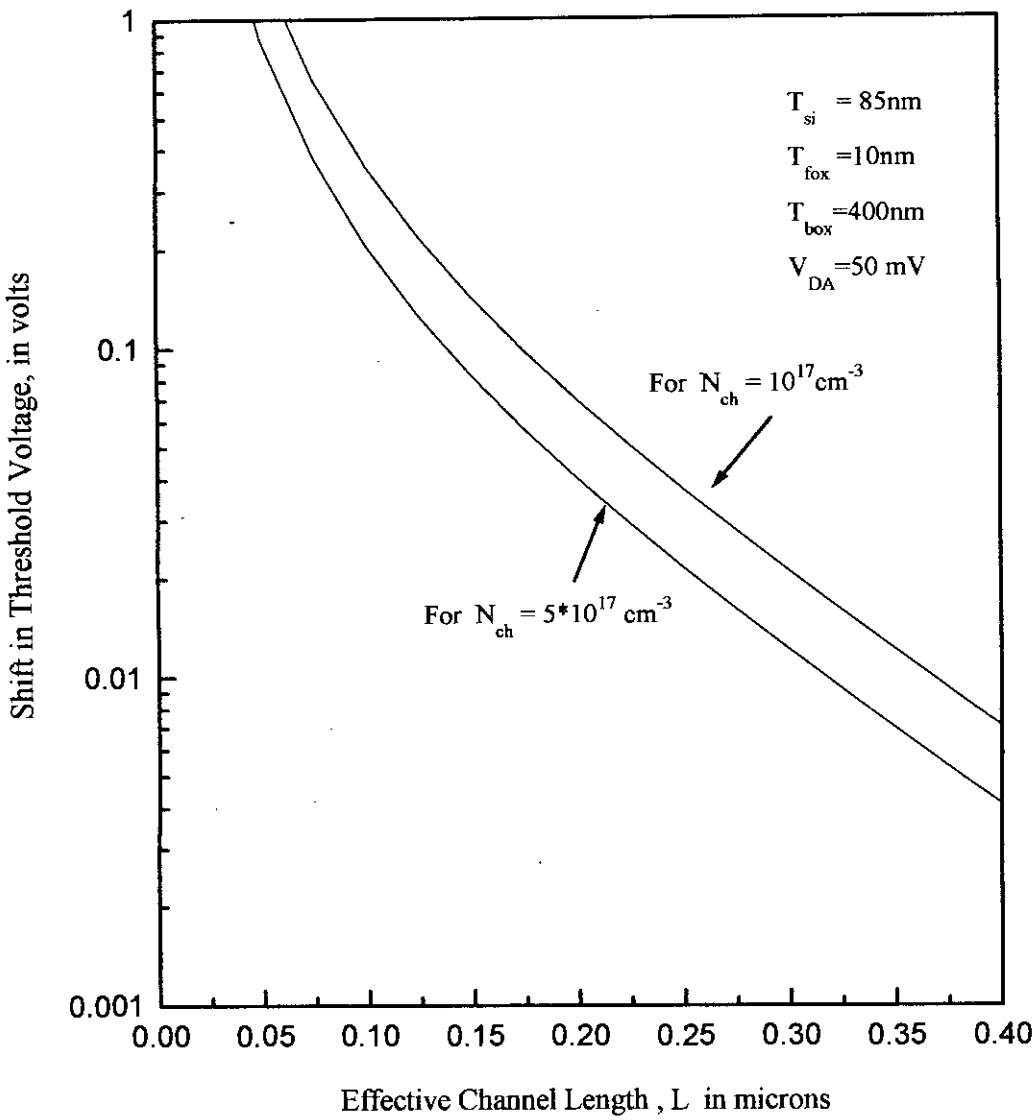


Fig. 3.10 Shift in Threshold Voltage vs. Channel Length for different channel dopings

Static characteristic models for submicron/deep submicron SOI MOSFETs have been developed in chapter 2. These models have been incorporated with the modified mobility formula (eqn. 2.23), which in fact takes into account not only the modified mobility in the channel, but also the velocity overshoot phenomenon and the effect of source/drain resistance. Special emphasis has been given on the subthreshold behavior of a SOI device in this work. Based on the expression for free inversion charge density in the weak inversion region (eqn. 2.20), the subthreshold drain current model (eqn.2.29) has been developed. This model is firstly simulated for an n-channel SOI device with a channel length of 0.3μm and channel width of 20μm. The silicon-film thickness is 85nm, while the thicknesses of front oxide and buried oxide layers are 10nm and 400nm respectively. The channel doping concentration used is 10^{17} cm^{-3}. The transfer characteristics (drain current vs. gate voltage) of such device are obtained by simulating the subthreshold current model (eqn.2.29) against gate voltage, with the drain voltage as the fixed parameter. The drain currents used are 50 mV and 1V. These characteristic curves are produced in Fig. 3.11. The drain current is seen to increase with increasing gate bias (though below the threshold voltage); and for higher the drain voltage, the currents are larger. This is expected because the higher gate voltages induce larger number of electrons and thereby increase the carrier concentration in the silicon film. Thus the drift current through the film though negligible is enhanced. Also the higher drain voltage causes larger electric field in the lateral direction and the subsequent increase in drain current.

The subthreshold output characteristics of the same device have been produced in Fig. 3.12. Here the subthreshold current has been plotted against the drain voltage, with gate voltage, V_{GS} as the parameter. The results are as expected: the drain current rises with rise in the gate voltage as well as the drain voltage. The same type of simulation is done for a device with channel length of 0.2μm. As depicted in Fig. 3.13 and Fig. 3.14, the drain current is seen to rise significantly for this shorter channel device, when compared with that of the longer counterpart (0.3μm device). The same fact has been revealed another way in Fig.3.15. Here we calculate the subthreshold current for two devices with different channel lengths (L=0.2μm and L=0.3μm), for a particular drain voltage of 1V. As predicted by the figures (Fig. 3.11- Fig. 3.14), it is seen that the off-state current of the shorter-channel device is always higher than that of the longer-channel device. This is expected because in a shorter channel device, the carrier gradient, dQ_m / dy is larger than that in a longer-channel device, due to reduction in the channel length. Since sunthreshold current is actually a diffusion current that arises due to carrier gradient, so it is found that with shortening of the channel, the current-curve is shifted upward further.

The channel length modulation has a significant effect on the subthreshold current. As shown in the output characteristics of Fig.3.16, this fact is revealed quite easily; here we plot the subthreshold drain current versus the drain voltage, V_{DS}, for a gate voltage of 0.05 volts (the long channel threshold voltage of our device is 0.15V, so the state with gate bias of 0.05V is well within the subthreshold regime). The drain current curve considering the modulation effect is well above the other one (not considering the effect) and their difference is seen to increase gradually with increasing drain bias, as is expected in case of channel length modulation. As the channel length of a device is continually reduced, the drain depletion layer penetrates more

strongly into the channel and thereby results in more contracted effective channel length; this effect becomes larger for larger drain biases. Due to this effect, known as channel length modulation, drain current is seen to rise sharply for the shorter channel devices.

Another presentation of the effect of channel length modulation on the subthreshold characteristics has been provided (Fig.3.17). Here the transfer characteristics of a SOI device with channel length of 0.3μm, have been produced, for a drain voltage of 1V. Considering the device with T_{si} (Si-film thickness) of 100nm, we observe a significant upward-shift of the current curve, when we take into account the modulation effect (as predicted before). Channel length modulation can cause such undesirably large off-state current that can even make it impossible to turn the device off at all.

An important relation between subthreshold current and silicon film thickness, T_{si} has been revealed, which is presented in the same figure (Fig.3.17) used to show the channel modulation effect. Here we vary the silicon-film thickness of the device with modulated channel length between two values e.g. T_{si}=100nm and T_{si}=80nm; we observe that the drain current is lowered for the thinner silicon-film device; so that the problematic 'short-channel-effect' – the sharp subthreshold swing can be attenuated by thinning down the SOI silicon-film. This in fact is due to the increase of doping concentration in the channel region by reducing the Si-film thickness. Here to mention that there is an astonishing relation between the subthreshold current and the doping concentration, N_{ch}. This relation for a SOI device is revealed in Fig. 3.18. Here we simulate the subthreshold current model (eqn. 2.29) to calculate the drain current against gate bias with channel doping as the fixed parameter. The device under the study is a 0.3μm SOI device with a channel width of 20μm and its drain

voltage is kept at 0.1V; the doping concentrations used here are 2×10^{17} cm^{-3}, 10^{17} cm^{-3} and 5×10^{16} cm^{-3}. It is seen that the subthreshold current falls significantly with rises in the channel doping concentration; the drain current for the upper limit of N_{ch} is quite negligible when compared to that for the lower limit.

Such a result is expected because as we continually scale down the SOI device, the more the gate loses its control over the subthreshold current due to the drain-induced-barrier-lowering (DIBL) and also for channel length modulation. The intrusion of drain depletion layer into the channel and towards the source is severely dominant in case of a device with lower channel doping concentration. The threshold voltage of such a device is pretty low and the device as is scaled down more, cannot even be shut-off yet, i.e. the transistor as if ceases to function as a switch any more. Such drawback in case of a deep submicron SOI device can be avoided by increasing the degree of its channel doping concentration, as is suggested by the Fig.3.18. The finding from Fig. 3.17 that the drain current is lowered in a smaller T_{si} device is in fact another mode of revelation obtained from Fig. 3.18; the off-state current lowering due to the use of thinner Si-film is in fact a result of increased doping concentration in the channel and this increase in concentration has been afforded not by a usual technique like ion implantation, but by reducing the thickness of the silicon film, which is a direct consequence of device scaling down. So we see that as devices are scaled down and so scaled down the silicon-film as well, the channel doping required to maintain the fully-depleted condition in the channel is automatically restored by the thinner silicon film.

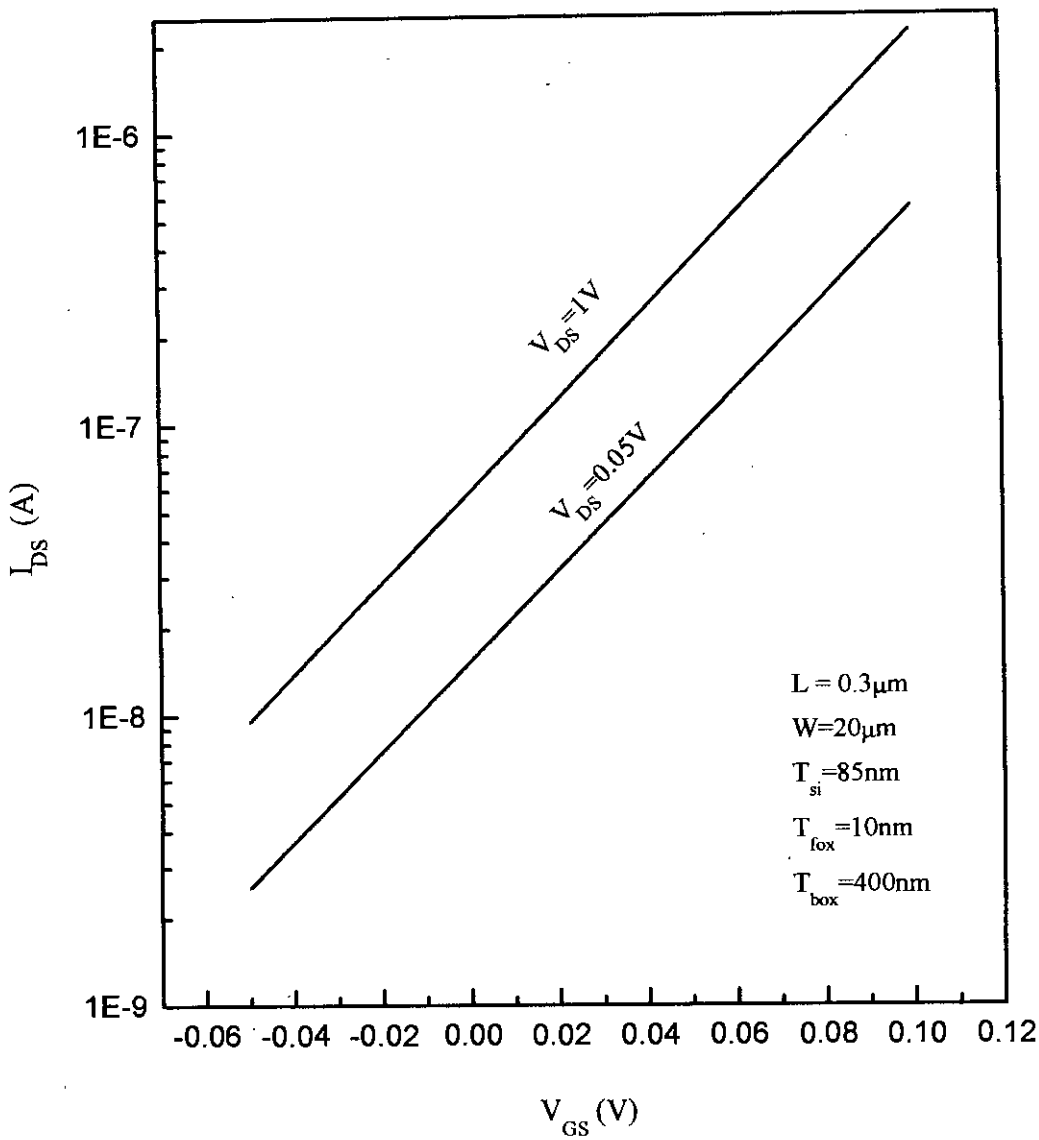


Fig. 3.11 Subthreshold Transfer characteristics of an n-channel SOI MOSFET with L=0.3μm

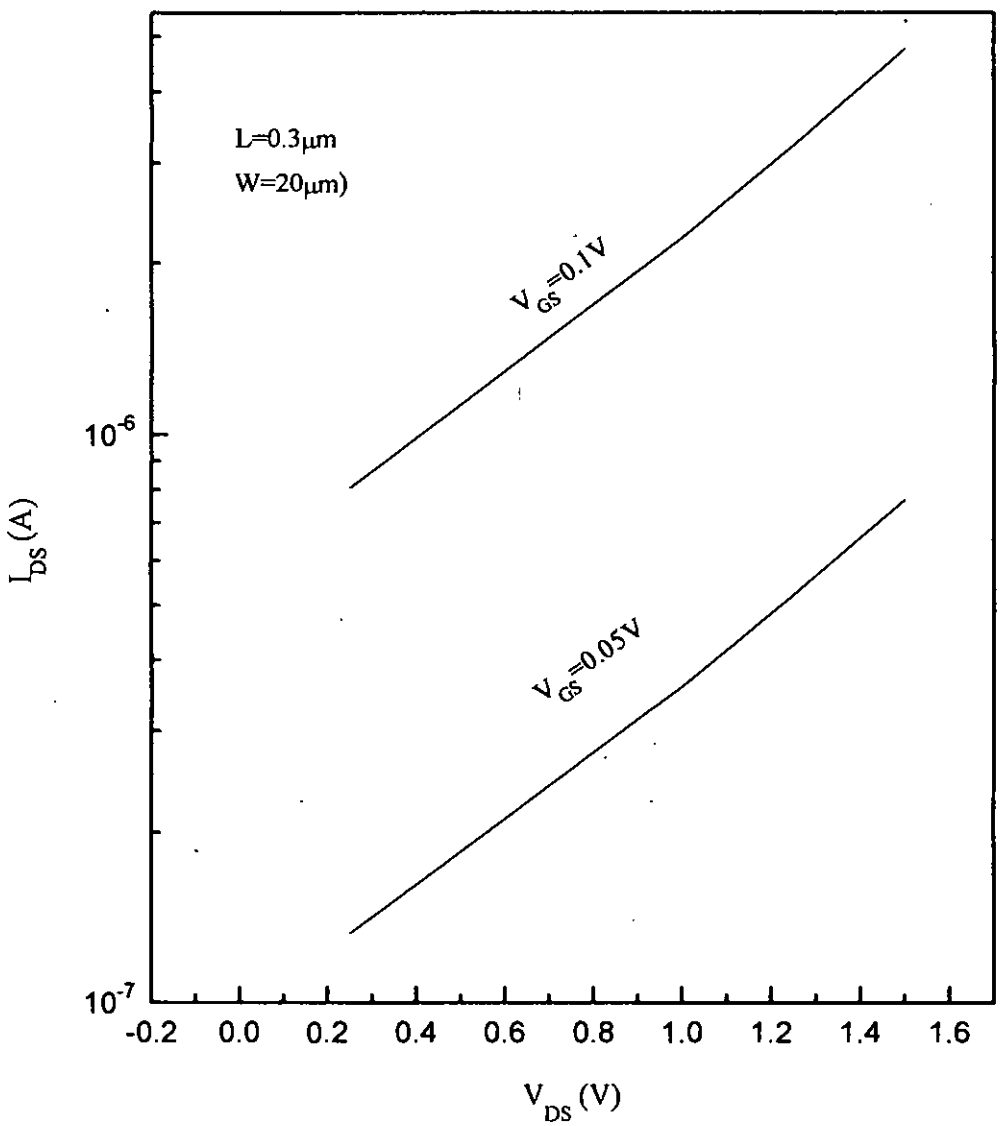


Fig. 3.12 Subthreshold output characteristics for an n-channel SOI MOSFET with L=0.3μm

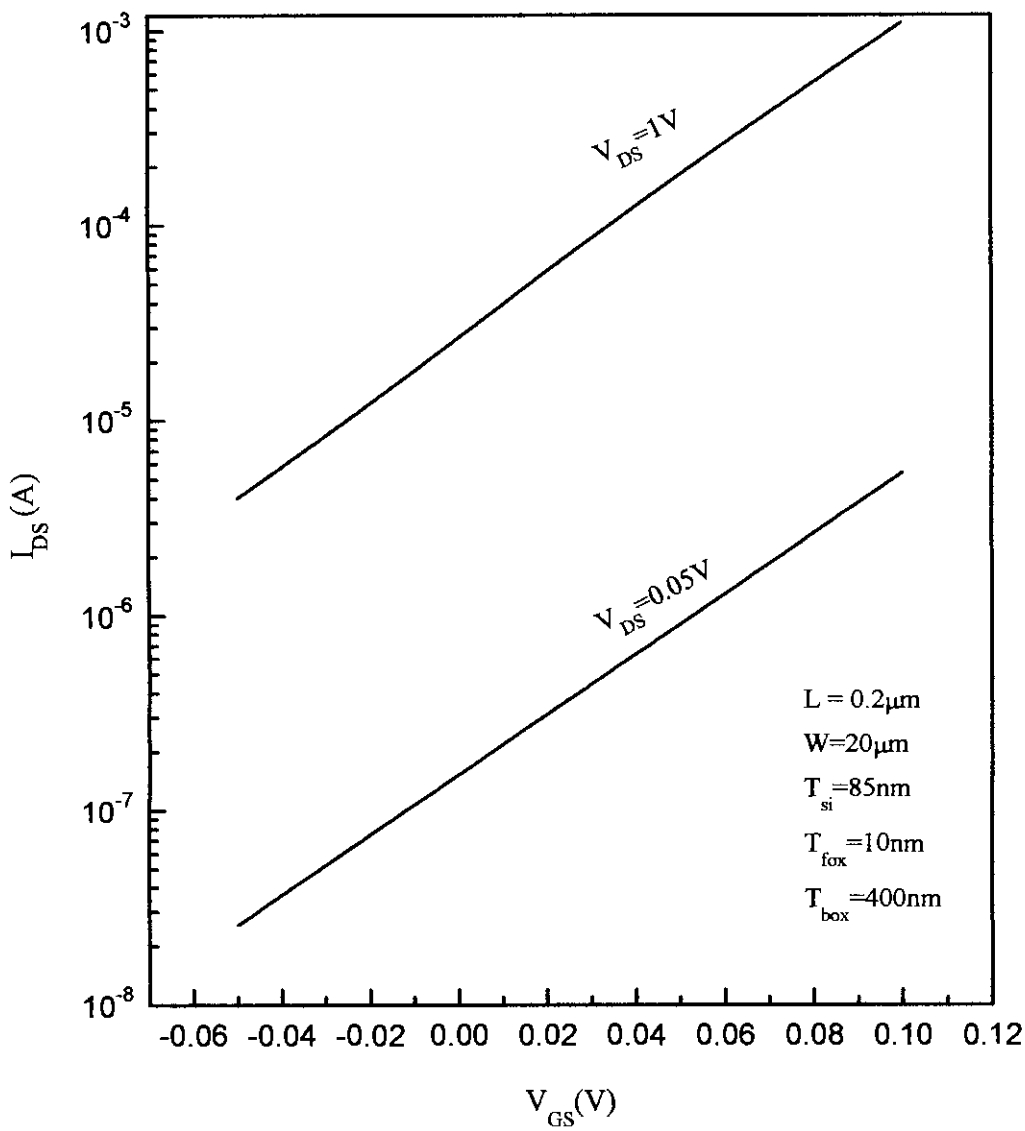


Fig. 3.13 Subthreshold transfer characteristics of an n-channel SOI MOSFET with L=0.2μm

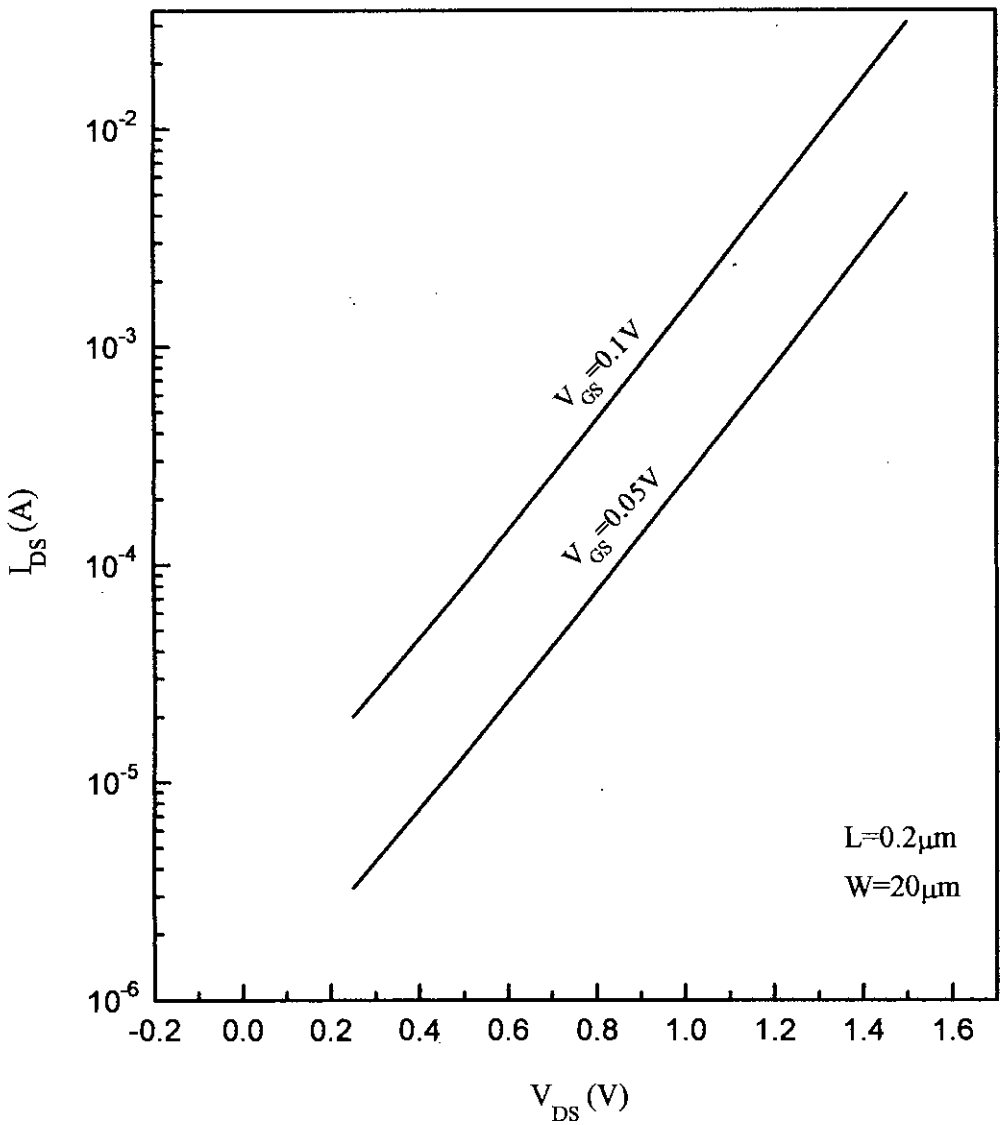


Fig. 3.14 Subthreshold output characteristics for an n-channel SOI MOSFET with L=0.2μm

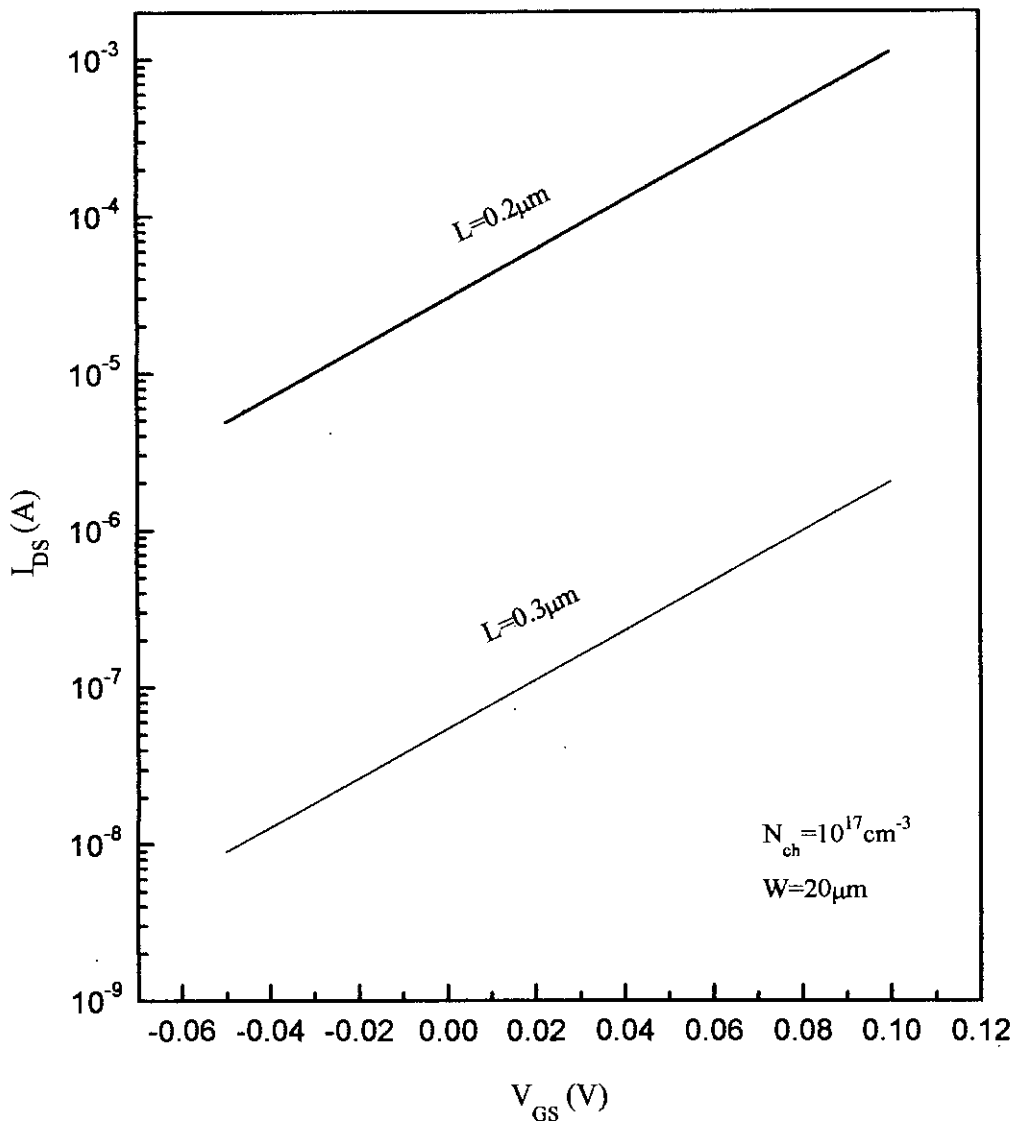


Fig. 3.15 Subthreshold drain current for two channel lengths

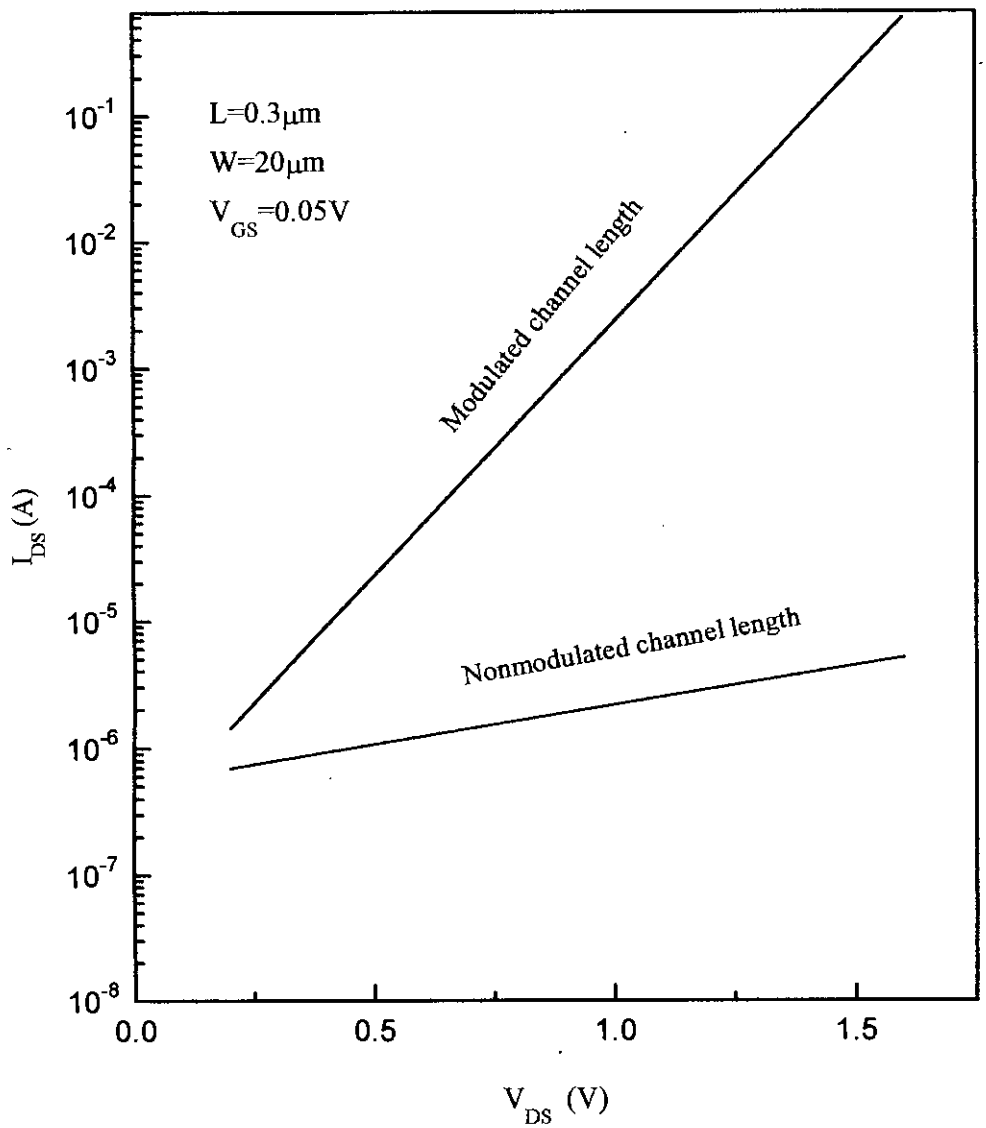


Fig. 3.16 Effect of channel length modulation on the subthreshold current for a SOI MOSFET with L=0.3μm

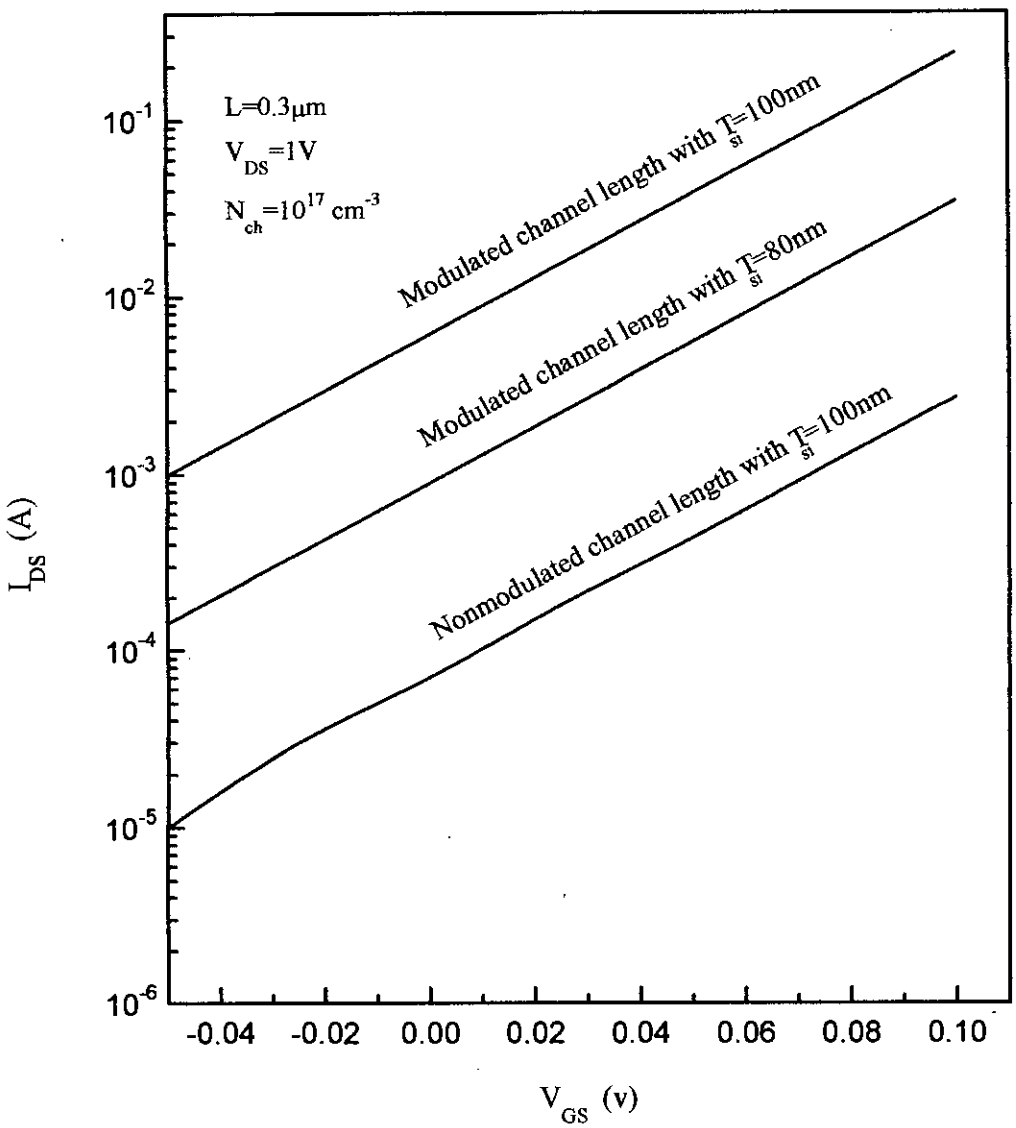


Fig. 3.17 Effects of channel length modulation and silicon film thickness on subthreshold current of a SOI MOSFET.

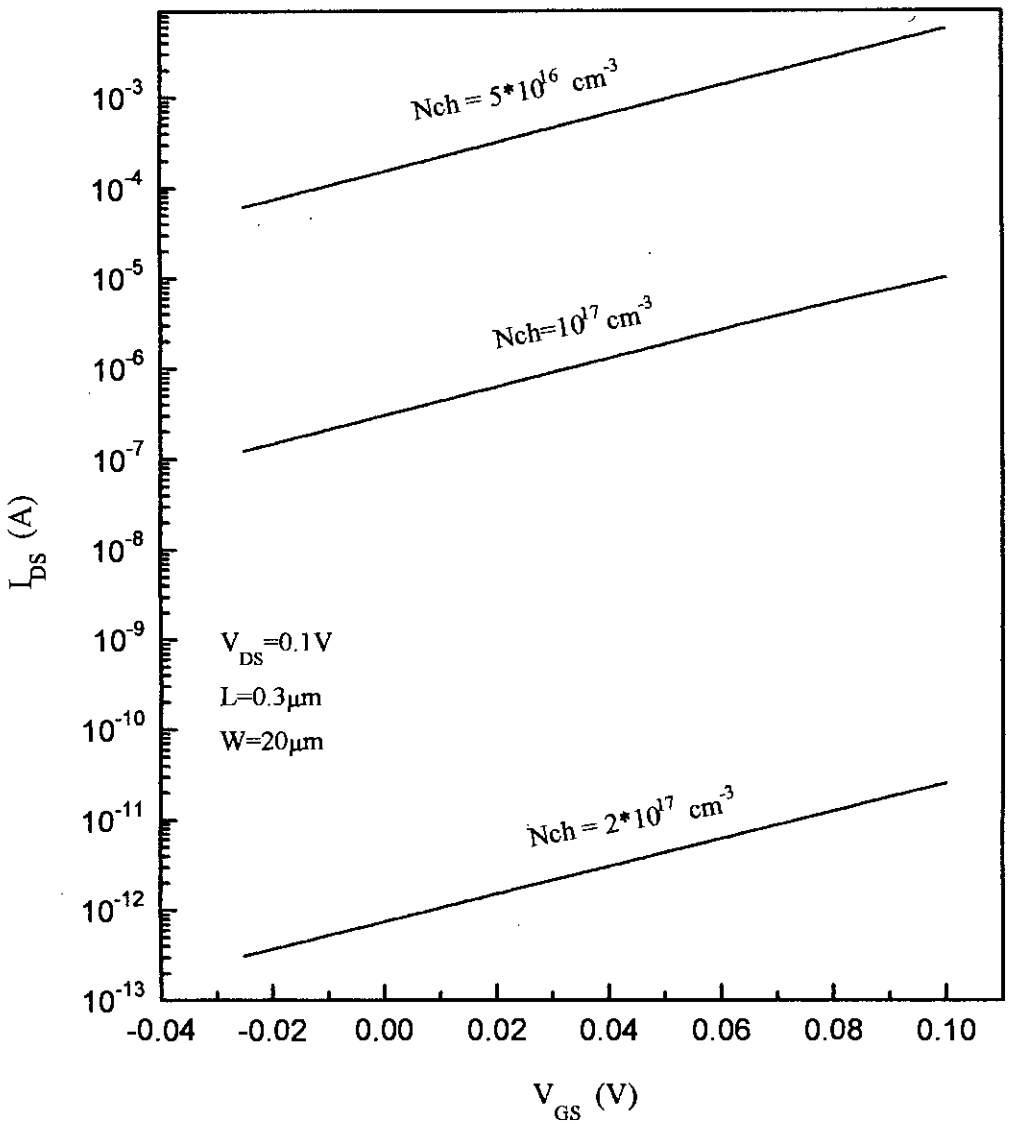


Fig. 3.18 Effects of channel doping concentration on the SOI subthreshold current

The model for drain current of a normally on SOI MOSFET (eqn.2.33 and eqn.2.34) has been simulated to reveal the output and transfer characteristics of the device in the above threshold region. The model is developed from eqn.2.19, the expression for free inversion charge density in the strong inversion or above threshold region. The velocity overshoot effect has been incorporated with this model. The model is simulated for three different channel lengths, e.g. L=0.6μm, 0.3μm and 0.1μm. The respective output (I_{DS} vs. V_{DS}) and transfer characteristics (I_{DS} vs. V_{GS}) are produced separately in Fig.3.19 – Fig.3.21. All the devices have a channel doping concentration of 10^{17} cm^{-3}. For the 0.3μm device, the thickness of silicon film, front oxide and buried oxide layers are 85nm, 10nm and 400nm respectively. The channel width is 20μm. The output characteristic curves (Fig. 3.19.a) depict two regions of transistor operation; the linear region (the region for lower drain bias) and the saturation region (higher drain bias region). In the linear region, the drain current linearly increases with the drain bias. But as the drain bias is continually increased, the gate voltage is neutralized at the drain end and the inversion layer disappears there. The channel is then said pinched-off and further increases of drain voltage would not increase the drain current significantly, i.e. the drain current is saturated. The saturation region is reached earlier for a smaller gate bias (e.g. 0.5V) and later for a higher gate bias (e.g.3V).

The transfer characteristics of the 0.3μm device are shown in Fig. 3.19.b. Here the drain current model is simulated to find the drain current for different gate

voltages, with drain voltage, V_{DS} as the fixed parameter. Two such curves are produced for two different drain voltages, viz. V_{DS}=0.1V and V_{DS}=2V. The curve for the higher drain bias is well above that for the lower drain bias and for each case, the drain current is very small for the small gate bias region or around the threshold voltage region, as is expected.

The SOI current model (eqn. 2.33 and eqn.2.34) is simulated for two other channel lengths viz. L=0.6μm and L=0.1μm. The device dimensions are adjusted as well; the Si-film thickness is 65nm for the 0.1μm device, while it is 90nm for the 0.6μm device. The front oxide and buried oxide layers of the two devices are 6nm, 300nm and 15nm, 400nm respectively. The channel width of 0.1μm MOSFET is 10μm while it is 20μm for the 0.6μm device. If we compare the corresponding characteristic curves of the three devices under study, we see that currents are larger in the shorter channel devices. This is expected because the drift current is dominant over the diffusion current in the strong inversion region and the drift current as expressed by eqn.2.30 is enhanced by the increased electric field in lateral direction for a shorter channel device.

An important aspect to be noted is that the output-current curves of the 0.1μm device seem to behave in a separate manner than the normal trend; here currents apparently show no saturation-behavior even at the higher drain biases. This is one of the short channel effects; as mentioned earlier that as device is scaled down continually, the subthreshold current becomes much larger and the threshold voltage is significantly hampered. Such distorted performance continues even in the usual saturation region. In a short channel

device, higher drain biases further minimize the effective channel length and the drain current seems to rise ceaselessly at a sharp slope.

The overall finding from the figures, Fig. 3.19 – Fig.3.21, is depicted in a compact way in Fig. 3.22. Here we plot the drain current against the channel length, L for a fixed drain bias of 1V and a fixed gate bias of 1V. The results or the observations were predicted before; drain current increases sharply with decreasing channel lengths, specially in the deep submicron region.

The effect of velocity overshoot on the drain current is depicted in the data Table 3.1. The current is seen to increase when velocity overshoot effect is considered. The situation is graphically revealed in Fig.3.23. An important aspect of the overshoot effect is that it becomes increasingly prominent with increasing drain bias. This is expected because as V_{DS} increases and L decreases, the average channel mobility and carrier velocity are enhanced further.

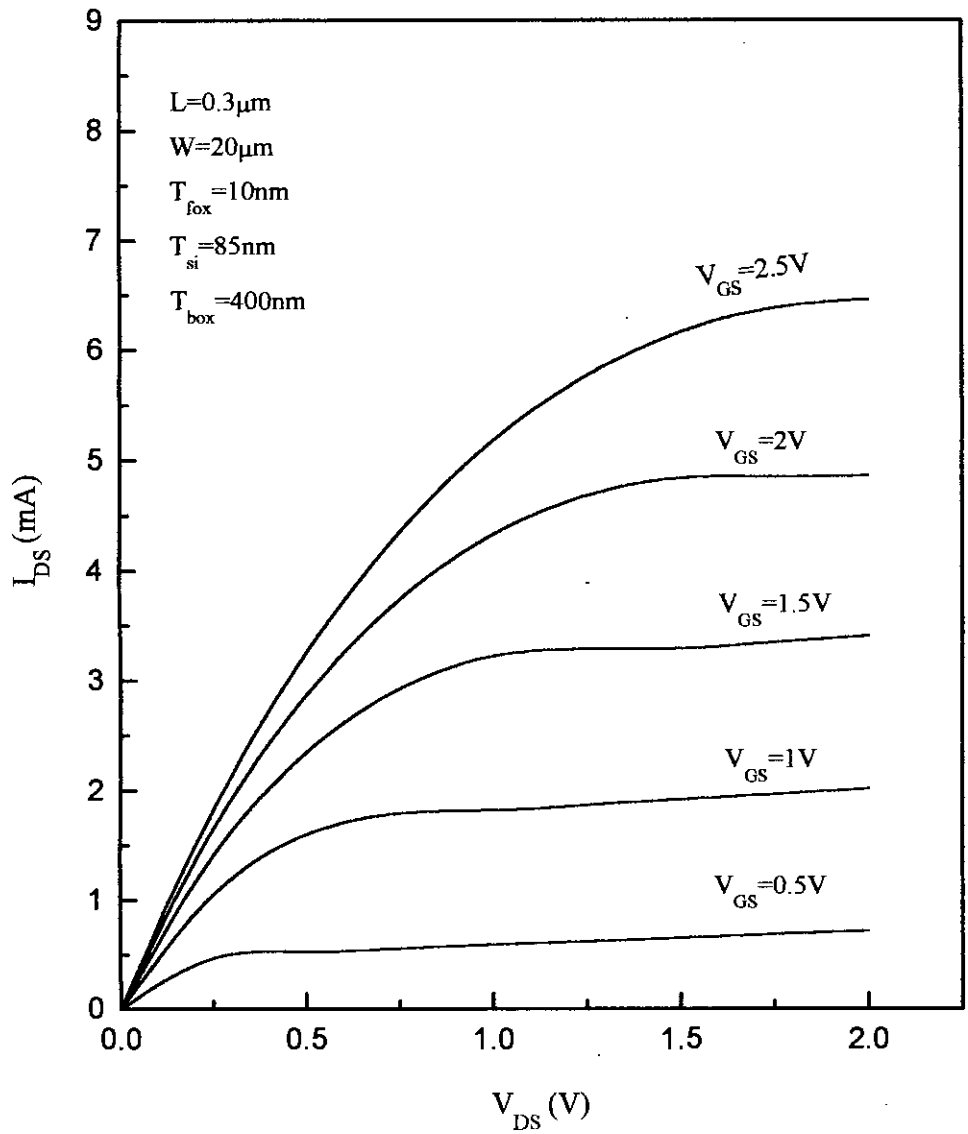


Fig. 3.19.a Ouput characteristics of an n-channel SOI MOSFET with L=0.3μm

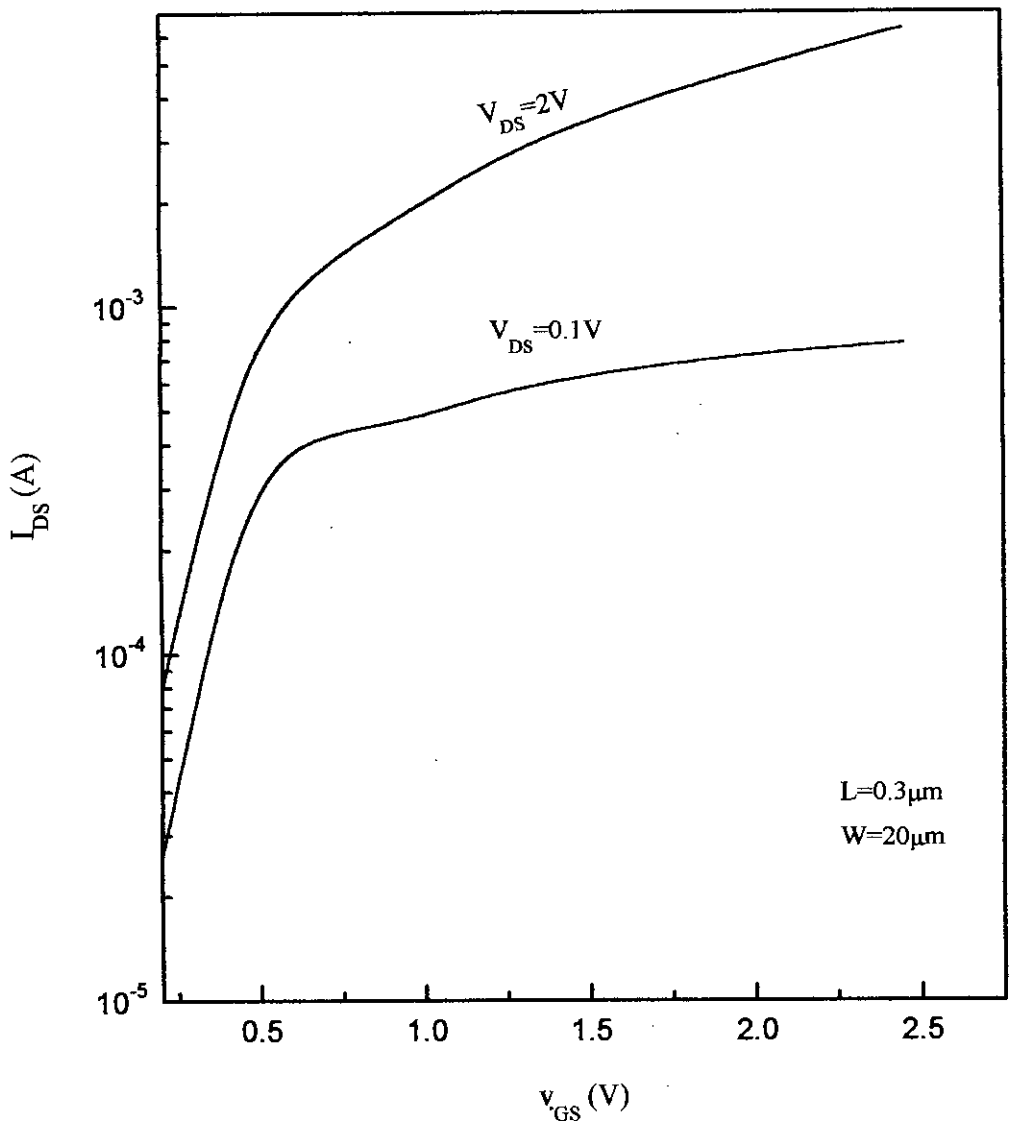


Fig. 3.19.b Transfer characteristics of an n-channel SOI MOSFET with L= 0.3μm

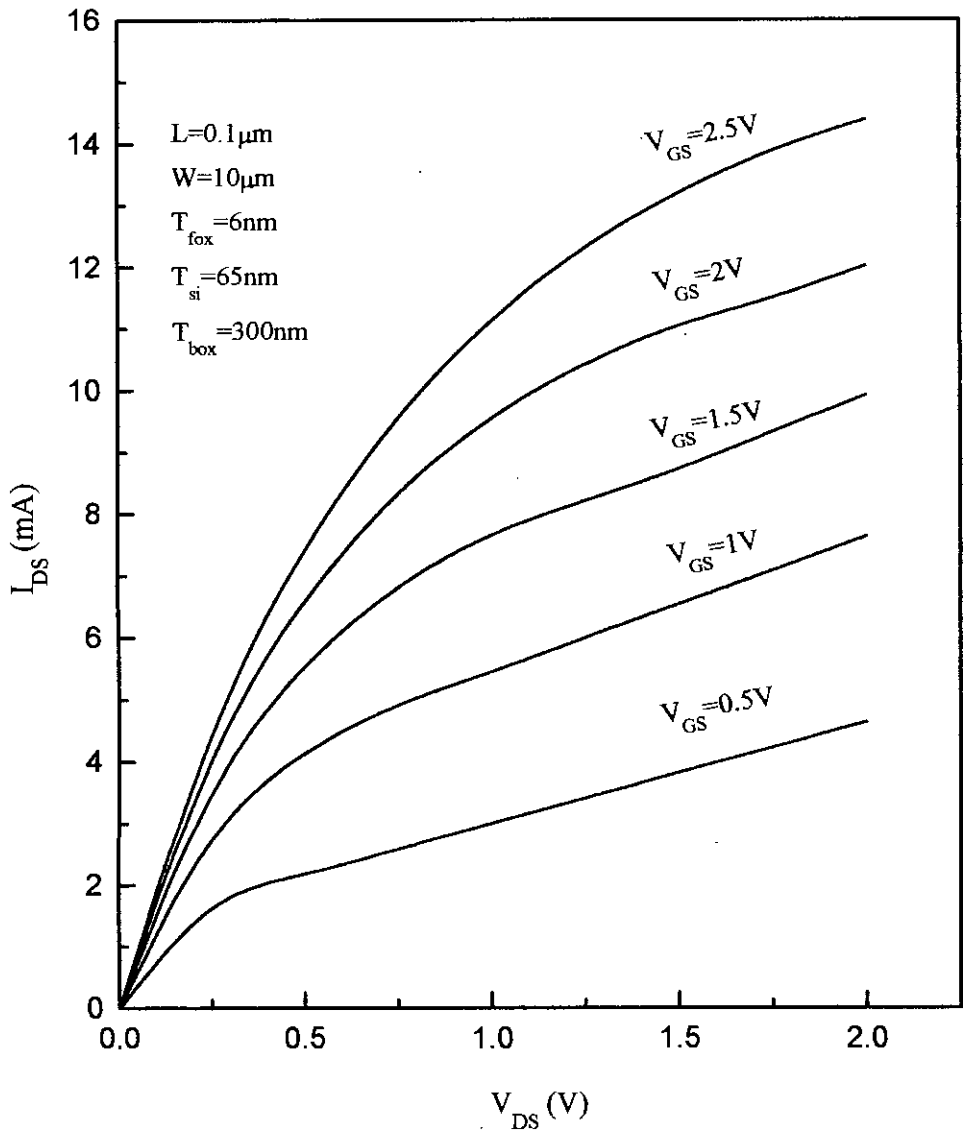


Fig. 3.20.a Output characteristics of an n-channel SOI MOSFET with L=0.1μm

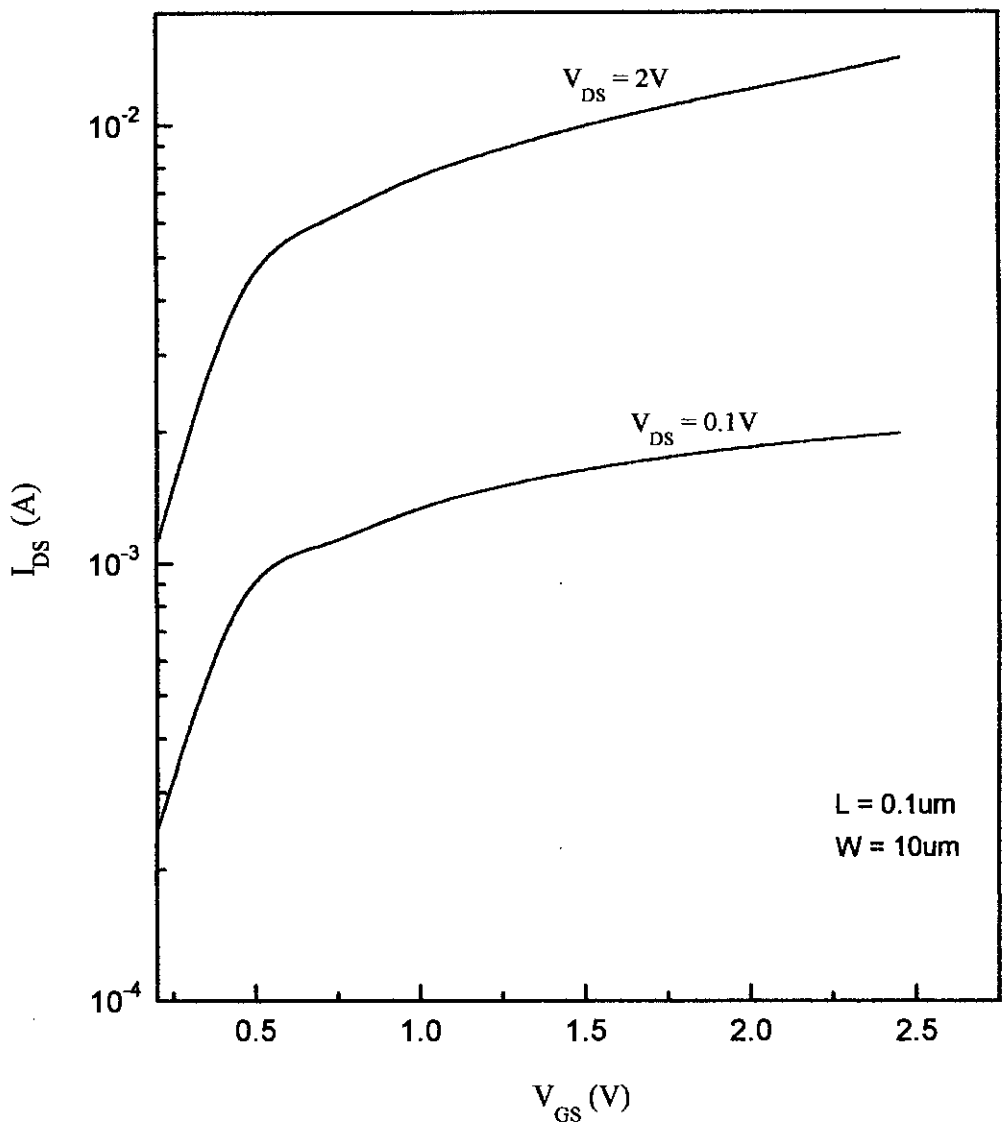


Fig. 3.20.b Transfer characteristics of an n-channel SOI Mosfet with L=0.1μm

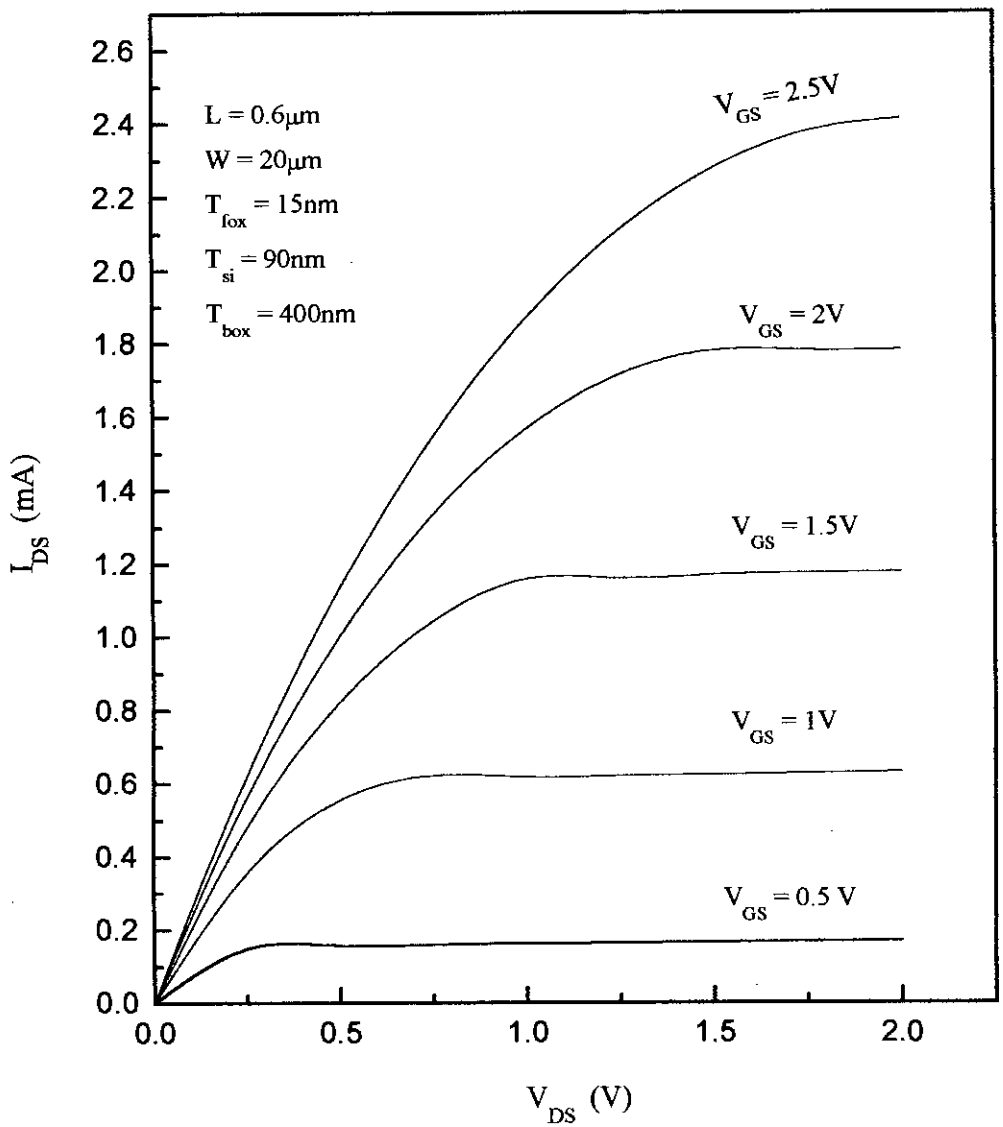


Fig. 3.21.a Output characteristics of an n-channel SOI MOSFET with L=0.6μm & W= 20μm

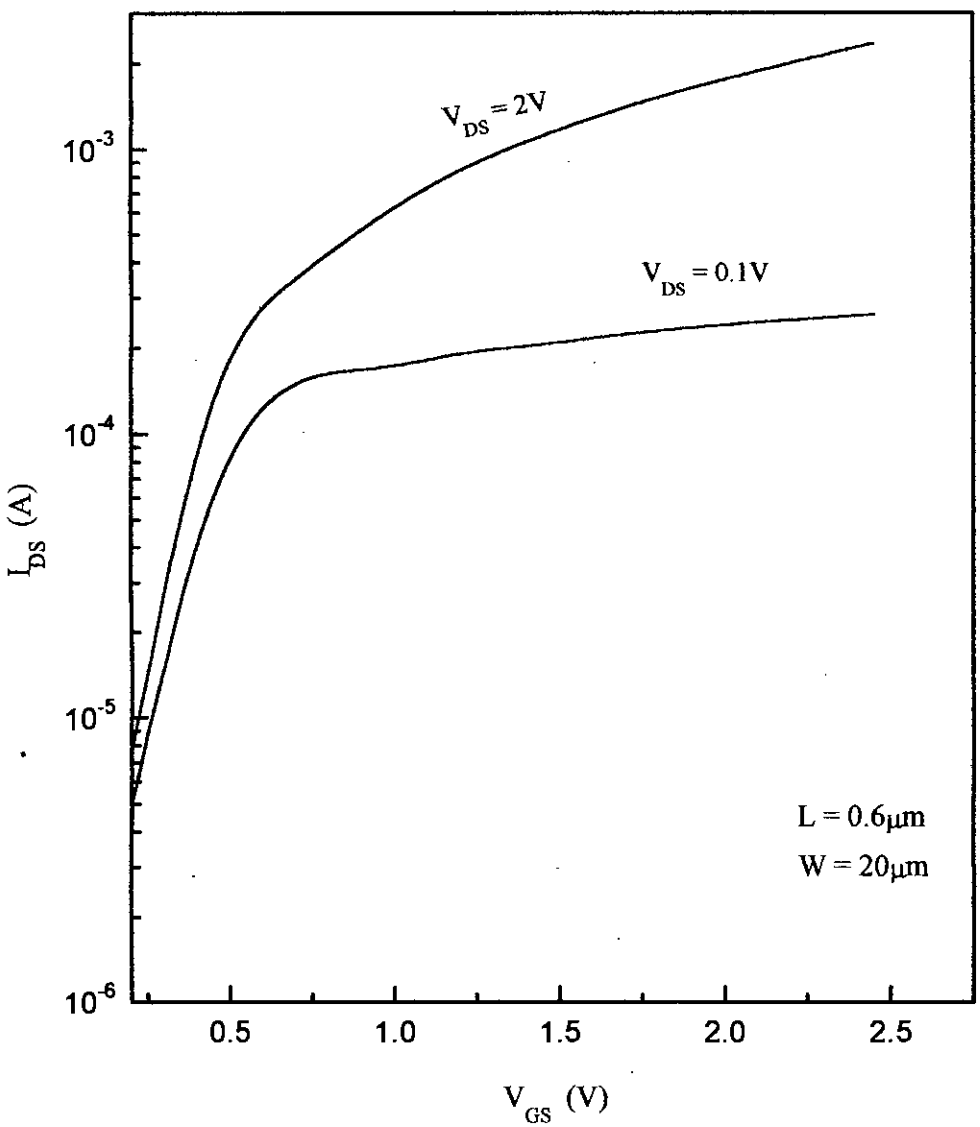


Fig. 3.21.b Transfer characteristics of an n-channel SOI MOSFET with L = 0.6μm

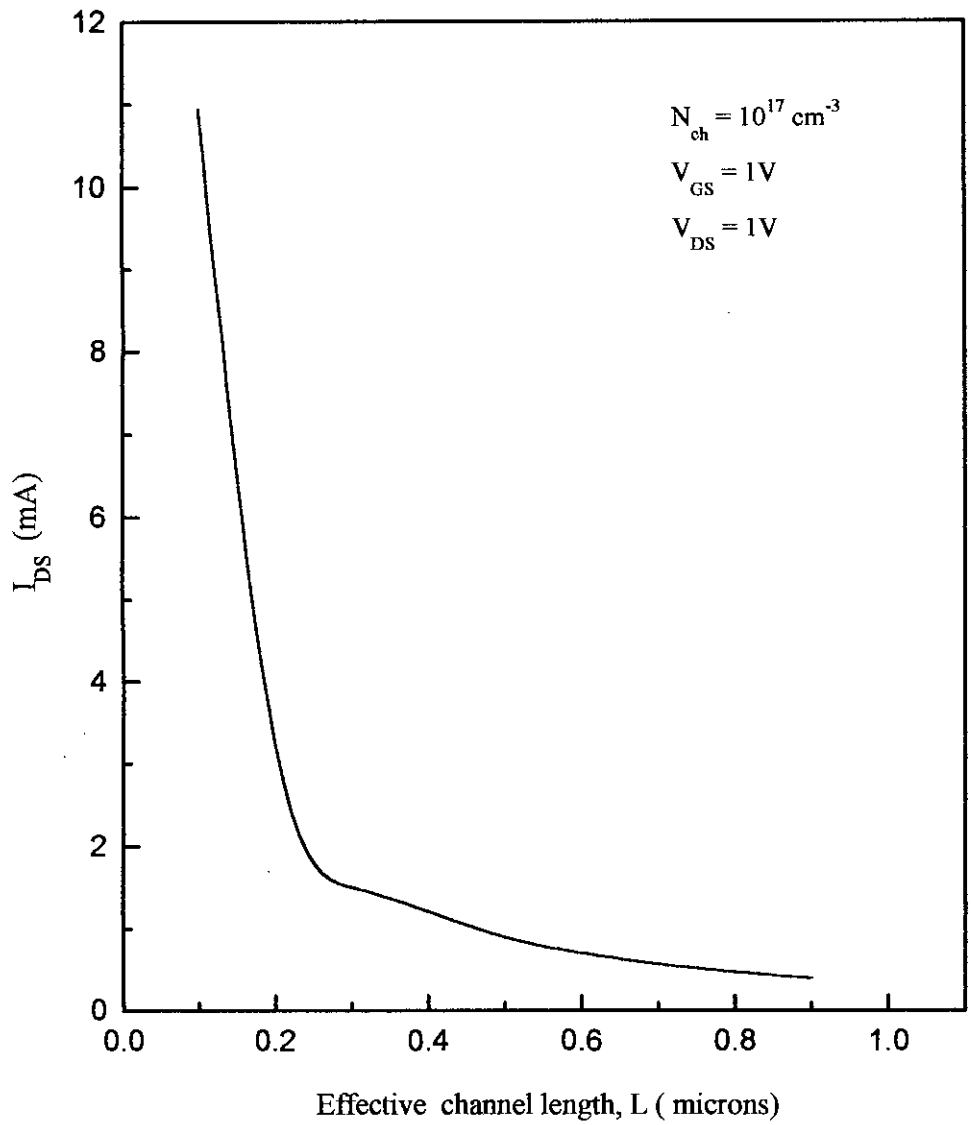


Fig. 3.22 Drain current vs. Channel length for an n-channel SOI MOSFET

V_{GS}=2V

V_{DS}, V	I_{DS}, mA	I_{DS1},mA
0.0000000	0.0000000	0.0000000
0.2500000	1.6486040	1.6480703
0.5000000	2.8655201	2.8640315
0.7500000	3.7353359	3.7329886
1.0000000	4.3220035	4.3190747
1.2500000	4.6747415	4.6715359
1.5000000	4.8320294	4.8288139
1.7500000	4.8543737	4.8503554
2.0000000	4.8776010	4.8736720
2.2500000	4.8889685	4.8839843
2.5000000	4.8903363	4.8852965

V_{GS}=2.5V

V_{DS}, V	I_{DS}, mA	I_{DS1},mA
0.0000000	0.0000000	0.0000000
0.2500000	1.8233495	1.8229813
0.5000000	3.2500212	3.2489289
0.7500000	4.3482458	4.3464131
1.0000000	5.1715118	5.1690738
1.2500000	5.7623294	5.7594742
1.5000000	6.1549008	6.1518198
1.7500000	6.3770495	6.3739136
2.0000000	6.4516373	6.4475873
2.2500000	6.4776205	6.4737648
2.5000000	6.4922633	6.4874838

V_{GS}=3V

V_{DS}, V	I_{DS}, mA	I_{DS1},mA
0.0000000	0.0000000	0.0000000
0.2500000	1.9553736	1.9551678
0.5000000	3.5455263	3.5448890
0.7500000	4.8264759	4.8253606
1.0000000	5.8433672	5.8418191
1.2500000	6.6329818	6.6310882
1.5000000	7.2255856	7.2234479
1.7500000	7.6463081	7.6430262
2.0000000	7.9161855	7.9128497
2.2500000	8.0529606	8.0486484
2.5000000	8.0807020	8.0764764

Table-3.1

I_{DS} – Drain current considering velocity overshoot

I_{DS1} – Drain current not considering velocity overshoot

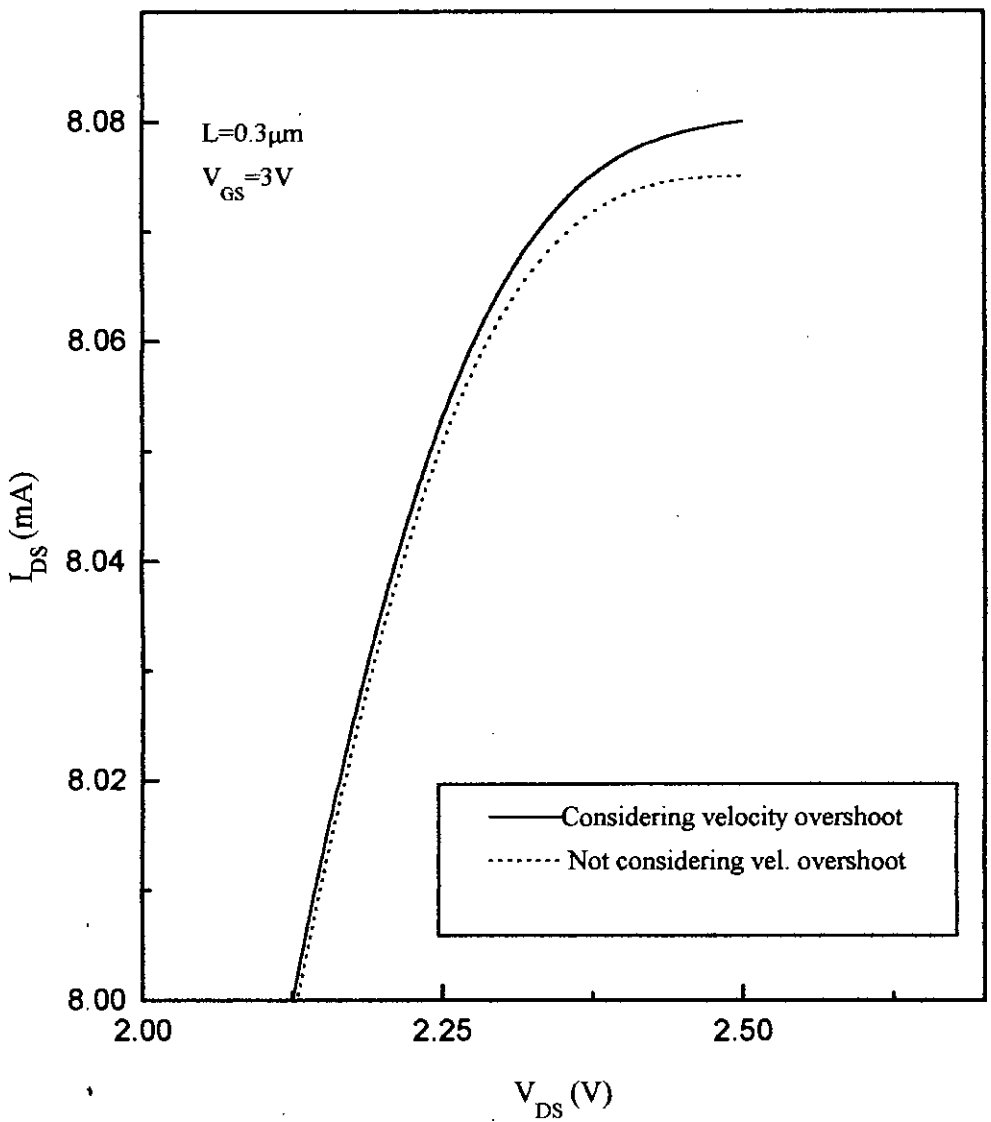


Fig. 3.23 Effect of velocity overshoot on the drain current of a SOI MOSFET

CHAPTER – 4

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORKS

4.1 Conclusions

To speed up VLSI/ULSI circuit design and simulation, it is important to model and predict circuit behavior in the early stage of technology development. To suit this purpose and since SOI MOSFET is considered to be a potential candidate for future high performance VLSI/ULSI circuitry, we have developed here a simple, analytical and complete MOSFET model for both submicrometer and deep submicrometer fully depleted SOI devices. The model developed on a quasi two-dimensional Poisson's equation uses few fitting parameters and is computationally very efficient. This overall model in fact consists of four specific models, viz. a model for the front surface potential, $V_{sf}(y)$, a model for the threshold voltage shift, ΔV_{th} and threshold voltage, V_{th}, a model for the subthreshold current and a model for the drain current of a normally ON SOI MOSFET. We have investigated the surface potential profile against some parameters and observed its dependence on drain-to-source voltage, V_{DS} and silicon-film thickness, T_{si}. Based on the profile of surface potential, we have defined '*channel length modulation*'; the channel modulation effect is seen to become increasingly prominent with increasing drain bias and the effective channel length suffers from serious contraction for the higher drain biases. It is also seen that the silicon-film thickness is able to

influence the potential profile; the thicker the Si-film, the more contracted the effective channel length becomes. For a particular drain bias and a particular Si-film thickness, the modulated-channel length is seen to suffer strongly in case of shorter channel (deep submicrometer) devices. The concept of channel length modulation has been applied later to other simulations to determine the strength of its influence.

A complete model on threshold voltage has been developed analytically and its variations with parameters like drain voltage and Si-film thickness have been estimated. It is found that threshold voltage declines for all devices that are subjected to microminiaturization or scaling down. The threshold voltage roll-off, ΔV_{th} is strongly prominent in a device applied with higher drain voltage, which is a clear indication of Drain Induced Barrier Lowering or DIBL. The effects of Si-film thickness and channel doping on ΔV_{th} are worthy of attention; the threshold voltage roll-off is seen to improve in a device, the channel of which has been doped with a higher concentration. This is due to the fact that the DIBL or channel length modulation effects are more or less suppressed by a heavily doped channel and the fully-depleted state in the subthreshold regime can be maintained as required. An astonishing benefit is seen to result by scaling down a SOI MOSFET; that is, a thinner Si-film (that may result due to device scaling) contributes to lowering the threshold-voltage-shift down. This is due to the increased doping concentration in the channel resulting from thinning down the Si-film and the advantages of higher channel-doping-concentration have been just mentioned.

We have developed a physics-based broad drain current model for a fully-depleted SOI MOSFET, that has been subjected to scaling down to submicron/deep submicron level. Based on a quasi 2-D Poisson's equation and

the expression for charge density in the inversion region, this model in deed comprises two primary models; one for the subthreshold current and the other for the drain current of a normally ON transistor. Channel length modulation, DIBL, velocity overshoot and mobility reduction due to transverse electric field have been incorporated in each of these models. The subthreshold current model (eqn. 2.29) has been treated with much care since it is one of the most suffered quantities of a shortened channel device. We have investigated the dependence of subthreshold current/off-state current on the channel doping concentration N_{ch}, channel length modulation and the silicon film thickness, T_{si}. The off-state current shows improvement (i.e. it is lowered) for a higher channel doping and for a thinner silicon-film. Thinning down the silicon-film in fact, enhances the doping concentration in the channel that result in simultaneous reduction of threshold voltage shift and also the subthreshold current. So we see that the short channel effects in a SOI device can be automatically counteracted by some extent if its silicon film is thinned down as well.

The drain current for a normally on SOI MOSFET has been simulated to reveal its various features like its response to channel shortening and velocity overshoot phenomenon. The on-state current is seen increase significantly as the channel length is reduced continually (thus ensuring an enhanced current drive) and the velocity overshoot effect is seen to behave more strongly in higher drain biases.

4.2 Suggestions for future works

The present thesis work is simple in functional form and it can be easily extended to study the subthreshold current or threshold voltage behavior of devices with channel lengths down below 0.1μm. Further modifications can be made on the models of threshold voltage and drain current to consider the other short channel effects like velocity saturation or hot carrier effects. The substrate current that results from the accelerated carriers in the high electric field near the drain can become significant in very short channel devices; this hot carrier effect then should be taken into account.

A more detailed study can be made regarding the 'DIBL effect on SOI device performance'; also the parasitic source-drain resistance effect can be independently modeled, since it becomes stronger in the shorter channel devices, specially in the deepest submicron devices.

The present model can also be used to investigate the effect of a bias applied to the back gate (a gate provided in the substrate region), with some modifications.

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