Discrete Modeling and Common Rail Powered Reliability Improving Techniques for Nanoscale CMOS Transceiver Circuits

by

Apratim Roy

DOCTOR OF PHILOSOPHY

Department of Electrical and Electronic Engineering
BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY

October 2015

The thesis entitled **"Discrete Modeling and Common Rail Powered Reliability Improving Techniques for Nanoscale CMOS Transceiver Circuits"** submitted by Apratim Roy, Student No.: 1012064001, Session: October, 2012 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of Doctor of Philosophy in Electrical and Electronic Engineering on October 31, 2015.

BOARD OF EXAMINERS

1. __________ 31/10/2015 — **Chairman** (Supervisor)
(Dr. A. B. M. Harun-Ur-Rashid)
Professor
Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology
Dhaka - 1000, Bangladesh.

2. __________ 31/10/15 — **Member** (Ex-officio)
(Dr. Taifur Ahmed Chowdhury)
Professor and Head
Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology
Dhaka - 1000, Bangladesh.

3. __________ 31/10/15 — **Member**
(Dr. Pran Kanai Saha)
Professor
Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology
Dhaka - 1000, Bangladesh.

4. __________ 31/10/15 — **Member**
(Dr. Md. Shafiqul Islam)
Professor
Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology
Dhaka - 1000, Bangladesh.

5. __________ 31.10.15 — **Member**
(Dr. Md. Anwarul Abedin)
Professor
Department of Electrical and Electronic Engineering
Dhaka University of Engineering and Technology
Gazipur, Bangladesh.

6. __________ 31.10.15 — **Member**
(Dr. Md. Forkan Uddin)
Associate Professor
Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology
Dhaka - 1000, Bangladesh.

7. __________ 31/10/15 — **Member** (External)
(Dr. Md. Ashraful Hoque)
Professor
Department of Electrical and Electronic Engineering
Islamic University of Technology
Gazipur, Bangladesh.

CANDIDATE'S DECLARATION

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

Signature of the Candidate

Apratim Roy

Dedication

To my parents and my aunt.

Acknowledgments

I begin by acknowledging the Almighty who's given me silent support during this e ort.

I would like to convey my heartiest gratitude to my supervisor Dr. A.B.M. Harun-ur-Rashid, Professor, Department of Electrical and Electronic Engineering (EEE), Bangladesh University of Engineering and Technology (BUET) for guiding me through this arduous work with his continuous guidance, suggestions, and wholehearted support. His technical and editorial expertise was indispensable to the realization of this thesis and the dissertation would not have materialized without him.

I would also like to thank the members of my doctoral committee: Prof. Dr. Taifur Ahmed Chowdhury, Head, Department of EEE, BUET, Prof. Dr. Pran Kanai Saha, Department of EEE, BUET, Prof. Dr. Md. Sha qul Islam, Department of EEE, BUET, Prof. Dr. Md. Anwarul Abedin, Department of EEE, DUET and Associate Prof. Dr. Md. Forkan Uddin, Department of EEE, BUET for their encouragement and insightful comments. In addition, I want to acknowledge the Department of Electrical and Electronic Engineering of BUET for providing laboratory and library facilities which were instrumental to the continuation of the project.

I am eternally indebted to my family for their love and support which are the forces behind whatever little accomplishments I have made in my life. I also take a moment to remember the loving memories of my grandparents who always wished the best for me.

Contents

Dedication iii

Acknowledgements iv

List of Figures ix

List of Tables xiv

Abstract 1

1 Introduction 3

1.1 Discrete Modeling for Nanoscale CMOS Architectures 3

1.2 Improvement of Reliability for CMOS Transceiver Circuits 10

1.3 Objective of the Thesis 25

1.4 Organization of the Thesis 27

2 Accurate Geometry Scalable CMOS Modeling of Low-power Nanoscale Amplifier Circuits 29

2.1 Introduction 29

2.2 Modeling of CMOS Elements 31

2.2.1 Metal-insulator-metal Capacitor 32

2.2.2 Polysilicon Resistor 35

2.2.3 Planar-spiral-symmetric Inductor 38

2.2.4 Scalable Active Device Model 42
2.3 Modeling of Nanoscale Amplifiers 44
2.4 Comparison of Performance 48
2.5 Conclusions 49

3 Common-rail Powered Reliability Improving Technique for CMOS Amplifiers 50
3.1 Introduction 50
3.2 Reliability Improving Circuits (RIC) 52
3.3 CMOS Single-supply Amplifiers with RIC 57
3.3.1 1.2-V High-gain CC Amplifier 57
3.3.2 Low-voltage CC Amplifier 59
3.3.3 1.2-V CS Amplifier 60
3.4 Results of CMOS Reliability 61
3.4.1 Improvement against Process Variation 61
3.4.2 Effect on Threshold Modification and Supply Stability . . . 61
3.4.3 Frequency Domain Analyses 66
3.4.4 Resistance against Feature Mismatches 72
3.4.5 Results for Low-voltage CC and CS Amplifiers 73
3.4.6 Comparison with Other Techniques 79
3.5 Conclusions 80

4 A Stabilization Technique for Single-ended and Differential Harmonic Oscillators 82
4.1 Introduction 82
4.2 Stability Modeling for Oscillators 84
4.2.1 Stabilizing Gate Circuit for Process Variation 84
4.3 Results of Reliability 92

4.3.1 Stabilization of LCHO 93
4.3.2 Stabilization of DLCHO 101
4.3.3 Comparison of Performance 103
4.4 Conclusions 105

5 Voltage Lowering and Gain Control Techniques for a Single-supply-driven 0.7-V Amplifier 106
5.1 Introduction 106
5.2 Front-end Architecture 108
5.2.1 Single-supply-driven Amplifier Architecture 109
5.2.2 Three-stage Amplifier without Scaled Gate Voltages 113
5.2.3 Effect of Common-drain Stage 117
5.2.4 Gain Control Technique 120
5.2.5 Small-signal Circuits 123
5.2.6 Parasitic Considerations of Architecture 126
5.2.7 Process Optimization 126
5.3 Results and Discussion 128
5.4 Comparison of Results 132
5.5 Conclusions 132

6 A Ku-band Low-power Amplifier with a Built-in Output Buffer 135
6.1 Introduction 135
6.2 Multistage Circuit Configuration 138
6.2.1 Input CG Stage 138
6.2.2 Secondary CSCG Stage 141
6.2.3 Output Buffer 145
6.2.4 Small Signal Equivalent Circuits 146
6.3 Results with Discussion 148

6.4 Performance Comparison 155
6.5 Conclusions 157

7 Conclusions 158
7.1 Summary 158
7.2 Suggestions for Future Work 160

Bibliography 162

List of Figures

1.1 Application of compound materials for various wireless technologies. 4
1.2 The scaling trend achieved by the CMOS technologies over the years. 5
1.3 Effect of scaling of the CMOS process on the number of channel dopant atoms. 17
1.4 Manifestation of dielectric thickness variation in a silicon technology. 20

2.1 Distributed RC model of MIM capacitor. 32
2.2 Input capacitance of MIM model samples. 33
2.3 Quality factor of modeled capacitors plotted against frequency. . . 35
2.4 Double-tee model of polysilicon resistor. 35
2.5 Pro les of polysilicon model samples. 36
2.6 Equivalent circuit model of planar-spiral-symmetric inductor. . . . 38
2.7 Quality factors of the inductor model. 40
2.8 Scalable composite model of an active device. 42
2.9 CMOS circuits analyzed with the models: a) matched nanoscale low-power amplifier and b) overvoltage-protected amplifier. 44
2.10 Comparison in terms of a) forward gain, noise-figure and b) input reflection, output reflection between modeled and measured results of the first amplifier. 46

2.11 Comparison between modeled and measured data of the overvoltage-protected amplifier with respect to a) forward gain, NF and b) S_{11}, S_{22}. 47

3.1 The reliability improving circuit (RIC) applied to an unmatched amplifier. 53

3.2 Application of the RIC to a) a 1.2-V common-source-gate (CC) amplifier, b) a low-voltage (0.7-V) CC amplifier, and c) a 1.2-V common-source (CS) amplifier. 58

3.3 Effect of the RIC on the 1.2-V CC amplifier's a) S_{21} and ORL, b) NF and NF_{min}. 62

3.4 Effect of the RIC on a) NF, NF_{min}, and S_{21} for the low-voltage (0.7-V) CC amplifier, b) NF, NF_{min}, and S_{21} for the 1.2-V CS topology. 63

3.5 Improvement against threshold variation in CMOS amplifier a) voltage gain and b) noise-figure. 64

3.6 Reduction of susceptibility to supply variation in terms of a) S_{21}, NF and b) I_{rail}, NF_{min}. 67

3.7 Influence of thermal pro le on noise and gain. 68

3.8 a) Gain, reflection-loss and b) noise-figures for varying process points. 69

3.9 Results of mismatch analysis in terms of noise and gain a) without and b) with the RIC. 70

3.10 Effect of variation in device a) feature length and b) feature width on the 1.2-V CC amplifier. 71

4.1 A single-ended LC tuned harmonic oscillator. 84

4.2 a) Single-ended (LCHO) and b) differential (DLCHO) harmonic oscillator architectures with stabilizing gate circuits. 88

4.3 Output response from uncompensated and stabilized harmonic oscillator circuits. 91

4.4 Output spectrum characteristics of the harmonic oscillator (LCHO). 92

4.5 Change in a) phase noise and b) period jitter against threshold shift. 94

4.6 Stabilization of a) noise and b) jitter against varying dimension. . 95

4.7 Effect of variable supply on a) N and b) J of the LCHO.. . . 96

4.8 Variation in a) phase noise and b) period jitter versus ambient thermal condition. 97

4.9 Effect of the stabilizing circuit on a) oscillation amplitude and b) frequency of oscillation. 98

4.10 a) N and b) J for the DLCHO as a function of threshold shift. 100

4.11 Compensation of a) noise and b) jitter in the DLCHO. 101

4.12 Improvement in reliability of oscillation magnitude for the differential oscillator. 102

5.1 A wireless receiver front-end housing a low-power amplifier. 109

5.2 a) An input-matched common-source-gate stage driven by a 1.2-V supply (V_{dd1}) and a separate gate voltage (V_{gate}<V_{dd1}) b) The amplifier stage driven by a single lower bias supply V_{dd2} (0.7-V). . 110

5.3 a) Noise-figure (NF) and b) input/output return-loss (IRL/ORL) for the two structures presented in Fig. 5.2. 111

5.4 The single-supply-driven CMOS amplifier architecture. 112

5.5 Effect of matching inductors on input impedance and IRL. 113

5.6 a) Forward gain and input reflection, b) NF and stability factor for single- and two-stage single-supply amplifiers. 115

5.7 The contribution of the output stage to a) forward gain, ORL, power and b) stability factor, reverse isolation, NF. 118

5.8 Effect of variable device ratios on scattering parameters. 119
5.9 The gain control technique implemented with the output stage. . 121
5.10 Regulation of gain and power requirement as a function of output control voltage. 121
5.11 Small-signal equivalent circuits for the amplifier's a) input single-supply stage, b) secondary low-voltage stage, and c) output common-drain stage. 122
5.12 The single-supply-driven architecture with possible parasitic elements generated by devices in a CMOS process. 125
5.13 Dependence of input return-loss and noise-figure on the source inductor. 127
5.14 Dependence of port reflection on the second interfacing capacitor. 128
5.15 Gain and noise parameters for the single-bias-supply architecture. 129
5.16 Port return-loss parameters obtained over K-band. 129
5.17 Clustered power gain and reverse isolation curves. 130
5.18 K_f and B_{1f} factors and standing wave ratios. 130

6.1 The 1.2-V low-power two-stage amplifier with bias and output circuits. 137
6.2 Relative Effect of the input CG block and the secondary CSCG stage on a) linear amplifier operation (GCC: gain compression curve) and b) impedance matching (input return-loss) 142
6.3 Noise contribution of di erent stages of the 1.2-V amplifier. 143
6.4 Small signal equivalent circuits for a) input CG stage and b) secondary CSCG stage. 146
6.5 The amplifier architecture with parasitic elements generated by CMOS components. 149

6.6 The Effect of the first resonating inductor on noise contribution and forward gain. 150
6.7 a) The dependence of port reflection on device size and b) selection of output current on the basis of power requirement. 151
6.8 Gain and reverse leakage for the amplifier. 153
6.9 Optimized port return-loss and standing wave ratios. 154
6.10 Degree of stability and noise for the amplifier. 155

List of Tables

2.1 Effective model resistance as a function of device geometry. 38

2.2 Effective inductance of the PSS model. 41

3.1 Performance of 1.2-V CC amplifier against feature variability. . . 72

3.2 Performance of 1.2-V CC amplifier against feature variability (contd.).73

3.3 Reliability of 0.7-V CC and 1.2-V CS topologies against threshold deviation. 74

3.4 Reliability of 0.7-V CC and 1.2-V CS amplifiers against variable supply. 75

3.5 Performance of 0.7-V CC and 1.2-V CS amplifiers with regard to process variation. 76

3.6 Performance of 0.7-V CC and 1.2-V CS amplifiers against feature variability. 77

3.7 Performance of 0.7-V CC and 1.2-V CS amplifiers against feature variability (contd.). 78

3.8 Comparison of percentage improvement in variability (PIV) achieved by reliability compensation techniques. 79

4.1 Comparison between process stabilizing techniques. 104

5.1 Comparison of the presented architecture with available amplifiers. 133

6.1 Comparative performance of submicron amplifiers. 156

Abstract

During the evolution of integrated circuits, the noise content of silicon complementary metal oxide semiconductor (CMOS) process was initially considered too high, which made compound semiconductors preferable for achieving superior high frequency characteristics. Nevertheless, rapid advancement and scaling down of CMOS technology, having started with an original intention of improving digital circuits, have allowed the development of cost-efficient monolithic silicon integrated architectures for communication. An efficient way to reduce overhead of silicon circuits further is to develop accurate models of its member elements. It can significantly reduce the number of attempts (and hence cost) required to achieve desirable performance from a prototype transceiver. This study presents a technique to accurately estimate the behavior of nanoscale CMOS circuits with geometry scalable discrete modeling. Rather than individual characterization of elements as presented in literature, the scheme attempts to predict gain, noise, and reflection-loss of integrated low-noise amplifier architectures. It reduces number of dissociated parameters by formulating dependent functions through symmetric distributed modeling. Geometry scalable empirical expressions based on physical structure and describing parasitic components, which should lower the scheme's computational complexity, are developed for elements like metal-insulator-metal (MIM) capacitor, planar-spiral-symmetric (PSS) inductor, polysilicon (PS) resistor, and active device. Results obtained with the models are compared against literature data of 1.2-V amplifier circuits where high prediction accuracy is achieved for microwave parameters (S_{21}, NF, S_{11}, S_{22}). In the next phase, the study focuses on a low-power technique to improve performance reliability of CMOS amplifiers using a integrated voltage network

for transistors. The reliability improving circuit (RIC) significantly reduces discrepancy in amplifier gain (S_{21}, VG), noise (NF/NF_{min}), and return-loss (ORL) figures (compared with other compensation techniques) resulting from variation in threshold, parasites, and supply. It performs well on both typical- (1.2-V) and low-voltage (0.7-V) platforms of a 90-nm technology and is able to maintain its consistency within a wide frequency coverage for three different architectures. The scheme's biasing arrangement is common rail powered with respect to the amplifier which permits the overall circuit to be driven from a single supply. The reliability improving scheme is also tested as a stabilizing gate circuit (SGC) to reduce deviation of ancillary transceiver blocks (e.g., harmonic oscillators) against process variation. In this case, the SGC is able to improve fidelity of parameters like oscillation amplitude, phase noise, and period jitter with a small increase in power requirement. Process related phenomena like device aging (and attendant Effects), spatial limitations, feature uncertainty, and supply ripples are covered through provision of resistance against device threshold, and power rail variation. Single-ended and differential circuits of LC tuned modified Hartley oscillators are analyzed to verify the SGC's Effectiveness for diverse front-end configurations. To reduce the probability of multiple rail variation affecting circuit behavior, the study also presents a front-end amplifier architecture with a voltage limiting technique so that it can be driven from a 0.7-V bias supply. The topology does not need scaled gate voltages and uses bias path sectioning to manage power requirement. A three-stage cascaded structure is adopted for high gain with the output common-drain block realizing a gain control mechanism. The circuit performs better in terms of power supply requirement when compared with millimeter-wave amplifiers. Moreover, the ability of an output block and an input stage to control port matching is demonstrated with the help of a multistage circuit.

Chapter 1

Introduction

1.1 Discrete Modeling for Nanoscale CMOS Architectures

Nanoscale complementary-metal-oxide-semiconductor (CMOS) integrated architectures have been the focus of numerous recent research e orts to satisfy the high commercial demand for wireless applications involving personal (IEEE 802.15.3), local (802.11), metropolitan (802.16d), and wide (802.20) area networks [1, 2]. In this respect, the transformation from analog circuits made with discrete de-vices to single package networks initially depended on III-V materials (compound semiconductors made from groups III and V of the periodic table) as they offered better integration efficiency, high mobility of carries, and minimization of substrate loss [3]. Fig. 1.1 presents the scenario of how multiple compound technologies had been applied to realize commercial high frequency wireless applications [4]. However, with the advent of submicron CMOS technologies, the situation started to change and integrated monolithic structures built in silicon have since been widely reported to avail advantages like low cost (due to manufacturing efficiency), large production output, and compatibility with millimeter-wave communication and digital baseband circuitry [5, 6]. In addition, scaling down of the silicon process has improved radio-frequency (RF) performance of

active devices (Fig. 1.2 shows the CMOS scaling trend over the years [7]) and lowered voltage-power requirement of monolithic integrated circuits (MIC). To utilize these benefits, accurate modeling becomes an essential prerequisite during CMOS IC development and as it influences prediction accuracy of computer-aided-design schemes. Additionally, estimation of a circuit's characterizing parameters at high frequencies is usually dependent on model precision of its on-chip components. Moreover, efficiency during the design phase determines the subsequent masking cost and, as a result, Effective modeling can minimize silicon production overhead by reducing the number of iterations needed to satisfy predetermined design targets. In this respect, literature has presented a number of characterization methods for CMOS circuit components where they typically have focused on individual process elements. For instance, a partially depleted device model is presented in [8] which has the capacity to simulate floating body topologies. Low power and low voltage design of a silicon circuit is facilitated with an active resistor structure in [9]. A resistor model for floating gate metal-oxide-semiconductor structures is utilized in [10] to enhance area efficiency and improve linearity. Barth et al. [11] study a silicon-on-insulator capacitor with a deep vertical trench to re ne soft error rate and critical charge limit. Electrical characterization of a dielectric ca-

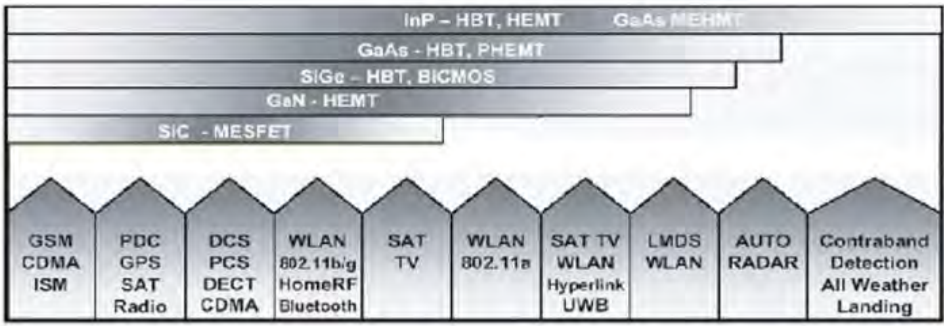


Fig. 1.1: Application of compound materials for various wireless technologies [4].

pacitor is manifested in [12] which uses alumina for better leakage current and capacitance density. Polarization dependent modeling of a CMOS capacitor is discussed in [13] to investigate the controlling factors of negative quadratic volt-age coefficient. Song et al. [14] propose an insulator capacitor model to estimate circuit behavior for different bias conditions and feature dimensions. A technique to optimize planar inductor parameters has been proposed in [15] using a physical model to account for crossover capacitance and substrate parasites. A frequency dependent model of spirals is presented in [16] to estimate the Effect of magnetic coupling with dimensional considerations. Improvement of spiral characterization is achieved over field-solver techniques in [17] with a closed form approach. These examples highlight the importance of device and circuit modeling and the thesis will attempt to address the issue, with the help of a discrete modeling approach, for nanoscale integrated CMOS architectures. Rather than single element char-

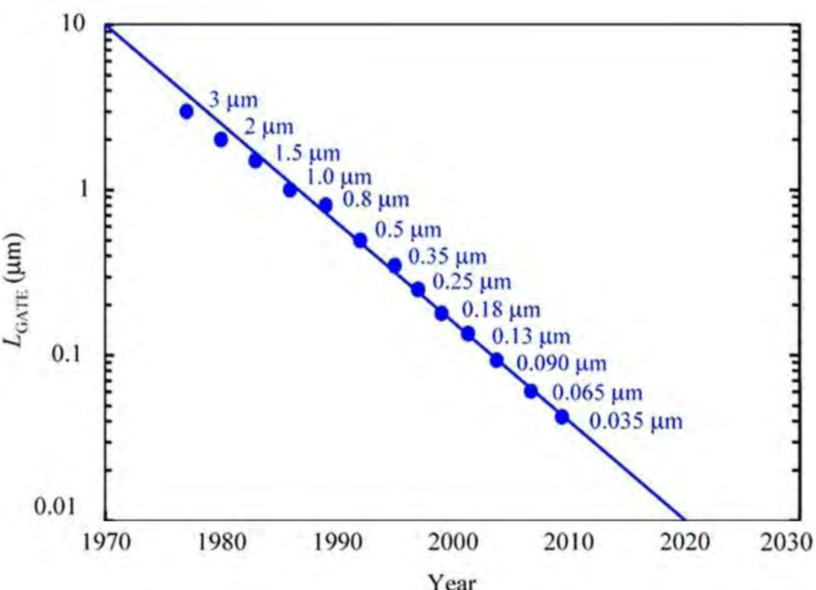


Fig. 1.2: The scaling trend achieved by the CMOS technologies over the years [7].

acterization, it will try to develop geometry scalable empirical definitions for the process elements which remain valid for the ranges required in nanoscale amplifier applications. The technique will try to exploit model symmetry to enhance computational efficiency and include distributed sections to improve its prediction accuracy for high frequency architectures.

A key factor in estimating the figures-of-merit of microwave circuits is the precision of their assumed component structures which, in turn, depends on their ability to include loss mechanisms. These issues pose more challenges when circuit characterization needs to cover entire architectures (with power and bias supplies) rather than individual passive-active elements. In this case, the formulations need to limit the number of independent model parameters without compromising on prediction accuracy and simplify their interrelationships to reduce computational complexity. Additionally, for operations at high frequency, a number of events related to delay of carrier response and output distortion may have to be taken into account for making transistor predictions [18]. Moreover, the importance of the estimation process is enhanced for next generation CMOS technologies due to a number of reasons including scaling of eld Effect transistors in deep submicron regime and incorporation of multiple functionalities on a single chip.

Modeling of Passives: Although metal-oxide-semiconductor technologies have primarily made advances (indicated by continuous scaling of features) due to their compatibility with ever popular digital electronics, they have made head-way into the market of microwave integrated circuits at the same time. One of the reasons for this is the availability of high quality passive components on the silicon platform. For example, passive capacitors are essential in many submicron monolithic architectures where they may be used as reactive elements for power amplifiers, frequency oscillators, low-noise amplifiers, data converters, frequency mixers, analog lters, intermediate-frequency lters, and switched capacitor cir-

cuits. The specific application of capacitors in these topologies often involves matching and coupling sections of the structure. Among other examples, variable capacitors (varactors) are typically required in the frequency selective tank of voltage controlled oscillators. There are a number of forms of silicon capacitors which can achieve a reasonable quality factor, namely, interdigital structure, microstrip structure, metal-oxide-semiconductor structure, and conductor-insulator-conductor structure. Among them, interdigital structures have a maximum range of about 1 pF, and microstrip structures are used for rather small components (<200 fF). On the other hand, metal-insulator-metal structures cover a wider range of reactance and can be placed between 100 fF and 20 pF. They also su er from relatively less variability against temperature and perform well in terms of achieving linear behavior. Therefore, precise models of CMOS metal-insulator-metal capacitors, which can describe their characteristics as a function of component geometry and operating frequency, have the potential to play a pivotal role in predicting behavior of circuit passives and, additionally, they can assist in achievingfirst pass design success for capacitive elements.

Whereas active devices are the principal building blocks of any digital architecture, passive elements may take the driver's seat for realization of nanoscale analog circuits. Although they can be included and connected as o -chip components for a low-frequency application, the influence of parasitic components on their behavior starts to dominate at higher frequencies. This is particularly true for inductive elements which are essential parts of any tuned circuit and found in architectures like power/low-noise amplifiers, correlators, oscillators, and filters. As the inductances required in submicron silicon circuits are typically in the range of nanohenry, they have to be implemented as on-chip elements because, other-wise, inductive parasites generated by the assembling of components can be too high for the application. The shape of this silicon inductor is crucial for determin-

ing its performance and this aspect is often dominated by fabrication limitations imposed by the process. Although the circular shape is often preferable to optimize the performance of an on-chip spiral, process requirements may allow only right spiral angles, resulting in a rectangular coil structure. In addition, generation of rectangular or square shapes is considered to be easier even with the help of basic silicon platform tools [19]. Therefore, as a compromise between the choices, modern silicon technologies usually support polygon spirals (hexagonal and octagonal) to realize inductors which retain the benefits from both structural patterns. As opposed to a passive spiral configuration, it is also possible to realize an on-chip active inductor which depends on a gyrator structure to simulate the Effect of inductance (built with a pair of back to back connected transconductors and an intermediate capacitor) [20]. However, these components, despite being area efficient, may suffer from a high noise factor and increase the architecture's power requirement. Another option is the use of inductance of bond wires which can manage a high value for quality factors. Nevertheless, their reactance is easily influenced by manufacturing variables and undesirable coupling may result from their employment. In addition, they can be ill defined over a wide range of process variation [21]. As a result, passive spiral structures have emerged as the components which are predominantly used in nanoscale analog circuits. These planar inductors are realized on silicon and gallium-arsenide substrates and exploit manufacturing techniques and process features like metal line stacking, discriminating masking of substrate, thick dielectric material, high conductivity for metal lines, and substrate with high resistivity [22]. Models for spiral inductors may be obtained by developing lumped circuit configurations and it would be useful if they are scalable with respect to multiple structural factors. It is generally considered that characterization of silicon inductors is more di cult than that of CMOS resistors and capacitors.

Submicron Device Modeling: The low frequency and dc behavior of a transistor is typically described through an intrinsic model by a CMOS process and a tested option for this model is the Berkley Short-channel Insulated-gate Field-Effect-transistor Model version 4 (BSIM4) [23]. It is a compact model which is suitable for both digital and analog systems and uses a combination of device physics and test data to characterize measured parameters. The characterization of physical events covered by BSIM4 includes channel charge density and sub-threshold swing model, carrier mobility model, subthreshold I-V model, strong inversion I-V model, drain voltage model for current saturation, gate direct tunneling current model, asymmetric junction diode models, stress Effect model, parameters for regional difference, and subthreshold slope factor. Apart from BSIM, other examples of industry employed intrinsic device models are EKV (Enz Krummenacher Vittoz) field effect transistor model, PSP (PennState Phillips) compact model, and hierarchical HiCUM (high current model) for high-speed bipolar transistor applications. After deciding on the model core, the devices need to include extrinsic components to account for parasitic elements emerging during high frequency operation. In this domain, the intrinsic model alone is not sufficient for device characterization and, as a result, subcircuits describing relevant additions have to be appended to the core structure. These subcircuits should serve as a function of device geometry i.e. be scalable within the required range while maintaining the model's prediction capacity. In addition, series resistive elements may have to be incorporated in the structure as deep submicron transistors suffer from minute voltage drops in port regions owing to semiconductor resistivity and contact Effect [24]. These appendages are comparable with channel impedance, particularly for short channel devices, and they lose their ability to significantly alter device properties for transistors placed above the submicron regime.

1.2 Improvement of Reliability for CMOS Transceiver Circuits

With the reduction in feature size for submicron silicon technologies, benefits like improved area efficiency and supply rail scaling have been achieved, but at the same time, susceptibility of nanoscale circuits to process and system variation has raised reliability issues. For instance, device threshold in a transceiver circuit may deviate from the process determined value under the influence of multiple reliability events (e.g., dopant fluctuation, bias temperature instability, hot carrier Effect, breakdown of dielectrics, CMOS aging). Threshold deviation is also the undesirable outcome of short channel limitation, which is a phenomenon able to manifest itself through conventional and reverse mechanisms. A study into the trends of process reliability analysis suggests that researchers started to characterize transistor failure events around the three-quarter point of the last century [25]. However, they focused initially on explaining the physics of the events rather than finding ways to counter their impact on the variability of figures of merit. Even during later studies, e orts were usually concentrated on quantifying device parameter deviation through measurements. The situation became more challenging during the last two decades with the introduction of improvised materials to facilitate the scaling of silicon technologies. In addition, modern submicron processes (realizing nanoscale circuits) face dimensional variability from uncontrolled parametric deviation and imperfection of manufacturing steps (related with lithography and etching phases). On top of that, factors which exist outside the architecture (e.g., supply rail and temperature stability) may have the ability to exert influence on reliability margins. These events put light on the importance of addressing process variation during the design of nanoscale circuits as the mentioned physical phenomena have the potential to affect the

lifetime of devices and packages.

The motivation behind incorporating a reliability improving technique (RIT) in a silicon circuit is to limit the fluctuation of the architecture's characterizing parameters due to process variation. Its efficacy may be judged in terms of percentage improvement in variability achieved after the RIT's inclusion in the topology. Published reports have addressed the issues involved with process reliability for various mixed-signal and digital circuits and dealt with the influence of materials/spatial-aspects on devices, physical-analytical models of technology variation, and circuit sensitivity improvement. However, investigation on power efficient voltage design techniques, which can stabilize the output of transceiver circuit blocks, remains rather limited. For example, electrical characterization of the influence of thin oxide films on transistor reliability is studied in [26]. It discusses how trap states in interfaces are passivated with the help of deuterium implantation instead of conventional hydrogen dopants. Gate oxide degradation of scaled complementary silicon devices is examined in [27] by observing time controlled defect generation (TCDG) from constant voltage stress. With the assumption of variation in activation energy following Fermi distribution, solutions for TCDG are determined from data related with gate leakage. A method to improve data retention properties of ash memory and hence reliability of silicon technologies is presented in [28] which provides resistance against channel hot carrier induced bias current limitation. To safeguard product yield and parametric reliability, a temporal degradation detection scheme is proposed in [29] which uses the control voltage of an oscillator as a dynamic performance signature. Kim et al. [30] study a leakage-current sensor serving as a process compensating technique to reduce deviation in robustness/delay and supply sensitivity. A general discussion on the impact of parameter variation on scaled silicon technologies is provided in [31] with a particular emphasis on microarchitectures to achieve

high frequency bins. Matching networks made with passive components, which are insensitive to process factors, ensure optimal noise-power match, and can be extended to broadband matching, are detailed in [32]. The influence of structural factors on dielectric breakdown in scaled silicon devices is manifested in [33] with emphasis on the mechanism of soft and other breakdown events. These illus-trations signify the importance of understanding the role of reliability improving techniques for submicron architectures which will be explored in this dissertation.

To realize an Effective RIT for a submicron receiver chain, which is built by cascading a number of milimeter-wave circuits, we have to make a relative assessment of noise and gain contribution of the individual blocks. This is com-plicated by the fact that the operating frequency of CMOS receiver front-ends has been continuously pushing upward during the last two decades [34]. As mentioned before, initial radio-frequency front-ends were predominantly designed with structures like PHEMT (pseudomorphic high electron mobility transistors, GaAs/InSb/AlSb) and HBT (heterojunction bipolar transistors, SiGe/GaAs) as they provide better noise performance (albeit with higher overhead and fabrication challenges) [35]. However, scaling down of CMOS process below 0.35- m has led to the reporting of numerous transceiver architectures in silicon [36, 38]. They have been employed as circuits suitable for applications like short-distance high-capacity wireless schemes, radar systems, and satellite communication. Ad-vantages offered by these nanoscale silicon architectures include higher performance per watt (PPW) for central processing units [39], limited power demand, high yield, and level of achievable integration for networks-on-a-chip. On the issue of the relative importance of CMOS transceiver blocks, the low-noise amplifier (LNA) which follows the antenna-filter section of a front-end proves to be the overall performance determining component. This amplifier determines the entire receiver's noise sensitivity and controls noise-figure (NF) of the following

blocks by its bandwidth limited forward gain. Additionally, the amplifier's in-put port has to be matched to an ideal characteristic impedance to interface it efficiently with the preceding segment. Regulation of port impedance remains as an important design issue as it controls the extent of attenuation when signal is transferred between the transceiver blocks. To complete the design of this amplifier, a number of trade-o s between factors like power limit, noise level, and gain have to be considered for optimization of performance. Consequently, a multistage topology may be employed to realize a high-gain low-noise front-end with its multiple stages adopting a combination of common-gate, common-drain, and common-source blocks. In addition, as the silicon process scales down, simultaneous lowering of supply voltage helps to curtail receiver power requirement and voltage demand can be relaxed even further if the chain can be driven from a single supply rail. Literature on reported sub-180nm amplifiers shows that, in addition to the main voltage rail, the circuits typically include multiple lower gate signals to place active devices in suitable modes. As a result, the package requires multiple regulated rails which result in an increased probability of supply ripples affecting circuit behavior. At the same time, the gain boasted by the amplifier needs to be sufficient as the received signal can be a variable and possess a rather small power rating. Therefore, the front-end would be able to cover a wider range of signal strength if it can house a gain control mechanism. In conclusion, the pivotal role played by the low-NF amplifier on overall transceiver performance means that an efficient reliability improving circuit for the nanoscale amplifier will positively influence and stabilize the front-end's behavior.

Categories of Unreliability Events: The downscaling of CMOS process, which has often been cited as aggressive, has been fueled by a number of technical and commercial reasons like improving circuit speed, raising number of devices per chip, curtailing power demand, and achieving better cost efficiency. How-

ever, practical limitations like reliability events started to affect this trend even before gate lengths became literally comparable with atomic dimensions, thus making additional scaling physically impossible. The technology's progress is also influenced by practical considerations involving matters like development cost, performance ceiling, and yield sufficiency. This subsection brie y discusses the classification of reliability events which appear as drawbacks as we move into the realm of nanoscale devices and circuits. Generally speaking, silicon reliability features can be divided into two categories: spatial unreliability and sequential unreliability, and both of them contribute to different aspects of process variation [40]. Time-related sequential unreliability issues have branches like CMOS aging and transient occurrences while spatial unreliability includes systematic effects and arbitrary perturbations. Silicon process variations can additionally be classified according to their relation with intrinsic events and foundry induced deviation. In this case, the former mechanism is attributed to constraints of device physics and the later mechanism can be associated with imperfections of manufacturing steps and process limitations. One of the first time dependent unreliability issues to be studied in literature was time dependent breakdown of dielectrics which became important as oxide layer was thinned down to atomic dimensions [41]. It was observed that, scaling of oxide increased the Effect of gate electric field and allowed injection of hot carriers to take place, thus degrading transistor performance. To walk around the limitations faced by a scaled silicon process, researchers tried out modification of materials and device construction. Yet, there were cases where the alteration had an adverse impact on reliability issues (e.g., negative and positive bias temperature instability) [40]. These experiences ensured that process variation was treated as a separate field for submicron technologies as the topologies became more sensitive to the Effects of parameter fluctuation. Moreover, the possibility of device features to be located within a

probable spread have to be taken into account to estimate the tolerance of circuit output and guarantee an acceptable yield. As the reliability events ultimately produce deviation in parameters like device threshold and feature, more investigation is required on circuit techniques which can work as process compensation schemes without compromising on overall performance.

Sequential reliability issues (SQRI) are dependent on time and controlled by a number of ambient/operating conditions (e.g., die temperature, voltage inputs, action of neighboring systems). They can be related to the natural degradation of circuit performance over its lifetime (referred to as CMOS aging) and short duration transient events. Examples of SQRIs include hot carrier Effect (HCE), negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), time dependent breakdown of dielectrics (TDBD), and random telegraph noise (RTN). In contrast, spatial reliability issues (SPRI) are independent of time and controlled by manufacturing parameters, technology limitations, process materials, and architectural geometry. Even a newly fabricated prototype can manifest the Effect of these events. The dominant examples of SPRI involve line width/edge roughness (LWER), dopant perturbation (DP), dielectric thickness variations (DTV), and gradient Effects (GE). In the next subsection, the mechanisms of dominant reliability events behind process variation are brie y explained.

Hot Carrier Effects (HCE): For a CMOS technology, the term `hot carrier' refers to carrier particles in the MOS device which attain a relatively high amount of kinetic energy from being driven through a strong electric field. Physicists have identified four different types of energetic carriers up to now which may be categorized as channel hot carriers, secondary generated hot carriers, substrate hot carriers, and drain avalanche hot carriers. The higher energy of these particles allows them to enter undesirable regions of the device where they can create

trapped charges and interface states. Ultimately, the consequence of these defects is the alteration of parameters like threshold voltage and process transconductance. The threshold deviation due to hot carrier Effects is generally described with the help of a time dependent power law [40]:

$$\Delta V_t \propto \frac{1}{\sqrt{L_e}} exp^{(\alpha_1 E_{ox})} exp^{(-\frac{\alpha_2}{E_m})} {t_s}^n. \tag{1.1}$$

In this equation, n is the rate coefficient (with various values), E_{ox} is the oxide electric field, E_m is the maximum value of lateral electric field, t_s is modeled as the stress time, and The image part with relationship ID rId10 was not found in the file. are process dependent factors. The equation suggests that hot carrier Effect has strong (exponential) dependence on oxide electric field and lateral electric field. Alternatively, the threshold deviation model may be expressed as a function of electron mean free path ( ), energy of trap generation ( ), and inversion charge (Q_{inv}) [42]

$$\Delta V_t \propto \sqrt{Q_{inv}} exp^{(\frac{E_{ox}}{E_1})} exp^{(-\frac{\phi_{tg}}{\lambda_e q E_m})} {t_s}^n \tag{1.2}$$

where E_1 is also a process dependent factor. Hot carriers can be a problem for both n- and p-channel devices, as it affects NMOS parameters directly and influences PMOS bias temperature instability. The techniques which have been adopted to counter hot carriers have included graded junctions and lower supplies which reduce the probability of carriers assuming high kinetic energy. In addition, the use of high dielectric-constant metal gate (HKMG) process may make the dielectric layer less susceptive to intrusion of carrier traps. Nevertheless, energetic carriers remain as a stability concern for scaled silicon technologies.

Dopant Perturbation: Dopant perturbation (DP) refers to a phenomenon where variation of impurity concentration in the channel region results in alteration of device properties like turn-on voltage. It is an event which is particularly susceptible to channel scaling and has been termed as one of the significant sources

of process variation for active devices. As the total number of dopant atoms in the channel region decreases for smaller devices (the trend is demonstrated with the help of Fig. 1.3), the impact of dopant profile fluctuation becomes more visible on device behavior. Although a few compensating engineering steps (e.g., retrograde doping) have been proposed against DP, their Effectiveness is found to be limited for processes below 180-nm [44]. Impact of DP primarily manifests itself with a spread of device threshold and is influenced by relative position of dopants and disparity of distribution in the channel. In this respect, literature has reported that more than half of total threshold variation for silicon devices can be attributed to dopant shifts in sub-100nm technologies [45]. The deviation of device threshold obtained from an analytical model of arbitrary dopant fluctuation was initially derived as [46]

$$\Delta V_t \propto q \frac{t_{de}}{\epsilon_{de}} \frac{\sqrt{N W_{dep}}}{\sqrt{L_e}}. \qquad (1.3)$$

Here N is the number of dopant atoms in the channel, q is the carrier charge, W_{dep} is the depletion layer width under gate, L_e is the Effective channel length,

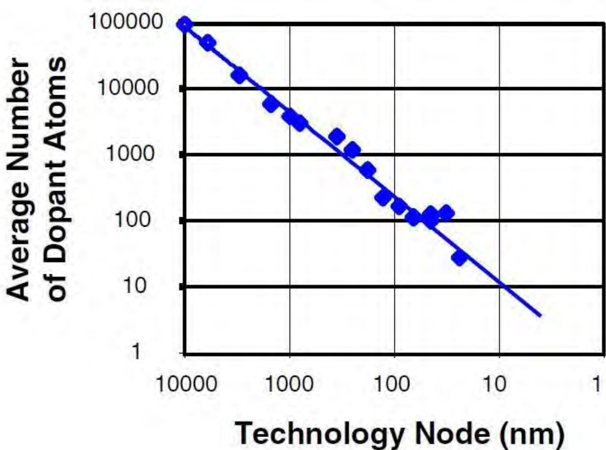


Fig. 1.3: Effect of scaling of the CMOS process on the number of channel dopant atoms [43].

and is the dielectric permittivity. The expression was later modified with a correction factor for uniform doping:

$$\Delta V_t \propto \frac{2}{\sqrt{3}} q \frac{t_{de}}{\epsilon_{de}} \frac{\sqrt{N W_{dep}}}{\sqrt{L_e}}. \tag{1.4}$$

Among the control factors of this expression, feature size exerts a dominating influence which may result in a disagreement between predicted deviation and measured data for short channel devices. A more frequently used statement of threshold deviation may be derived from the overall variation in total depletion charge (which reflects dopant perturbation) in the form of [47]

$$\Delta V_t \propto \frac{t_{de}}{\epsilon_{de}} \frac{\sqrt[4]{N}}{\sqrt{L_e}} \frac{\sqrt[4]{4q^3 \phi_B \epsilon_{si}}}{2} \tag{1.5}$$

$$\phi_B = 2k_B T \ln(\frac{N}{n_i}). \tag{1.6}$$

Here k_B is the Boltzmann constant, n_i is the intrinsic carrier concentration, and is the permittivity of silicon. To have an understanding of the impact of these mechanisms on process variation, it may be noted that ratio of dielectric thickness to permittivity and dopant concentration decreases with technology scaling. However, Effective channel area is reduced at the same time and, as a result, process variation induced by dopant perturbation becomes evident for scaled CMOS processes.

Line Width-Edge Roughness (LWER): The distortion occurring along the edge of an active layer is usually termed as line edge roughness (LER) and, consequently, LER occurring along both edges of the layer leads to variation in feature width and is called line width roughness (LWR). Although DP is often cited as the dominant source of transistor deviation, it is predicted that LWER could take its place as features are pushed below the 65-nm line. LWER is mainly due to the limitation of the etching process which, in turn, is related with the source used for subwavelength lithography. Initially, source wavelength in a CMOS process

was scaling with feature size, but it has been fixed at a constant position (193-nm) for deep submicron generations (below 130-nm). The main Effect of LWER gets visible for cases of gate patterning which ultimately result in modification of device threshold and subthreshold current. To complicate things further, al-though aspects of etching technology have been improving continuously, process deviation induced by LWER does not decrease in a proportionate manner. The physical events causing this phenomenon include photon flux variation, finite size of dissolved resist polymers, and distribution of resist chemicals, but their relative contribution is yet to be quantified. In addition, LWER is partly attributed to photon shot noise which is described in terms of deviation of intensity () during the lithography process. It is typically calculated with the help of characteristics of Poisson distribution [48]:

$$\frac{\delta_I}{< I >} = \frac{1}{\sqrt{< N_{ph} >}} = \frac{\delta_{N_{ph}}}{< N_{ph} >} = [< I > At\frac{\lambda}{ch}]^{-\frac{1}{2}} \tag{1.7}$$

$$I = (\frac{N_{ph}}{At})(\frac{ch}{\lambda}). \tag{1.8}$$

Here is the source wavelength, h is the Planck constant, Nph is the number of photons which travel over an area of A over the time frame t and < Nph > is the expectation value of the photon population. The probability of availability of Nph photons can also be described by the Poisson distribution of binomial equations:

$$P(N_{ph}) = [\frac{(Lt)^{N_{ph}}}{N_{ph}!}]e^{-Lt}. \tag{1.9}$$

Here L is the average rate of photons emitted per unit time from the source and it is assumed that Lt remains a finite quantity as Nph approaches infinity.

Dielectric Thickness Variation: Dielectric thickness variation (DTV) is an issue which becomes apparent as area of the gate dielectric material is scaled down. It can be ascribed to surface roughness of the oxide-silicon interface at atomic level of a CMOS platform [49]. Even for next generation devices

using HKMG technology, DTV becomes a problem due to roughness of multi-ple interfaces existing between combinations like metal-gate/dielectric-layer and dielectric-layer/substrate. A manifestation of this phenomenon is presented with the help of a cross-sectional diagram of a silicon technology in Fig. 1.4. Research has shown that threshold variability from DTV can be observed independently from Effects like DP and LWER. Although this type of threshold fluctuation is primarily accompanied by deviation in tunnelling leakage current, other physical Effects of the event may include variation of drive current and carrier mobility. In this respect, the relationship between dielectric thickness variation ( ) and deviation of gate current ( ) may be derived using the law of propagation of error [51]

$$\frac{\Delta_{I_{gt}}}{I_{gt}} = k\Delta_{t_{de}} = \frac{[(\frac{\partial I_{gt}}{\partial t_{de}})^2 \Delta^2_{t_{de}}]^{\frac{1}{2}}}{I_{gt}}. \quad (1.10)$$

Here k is a constant which is dependent on dielectric voltage, potential of barrier, and Effective mass of electron. Apart from DTV, non-ideal features involving gate dielectric may also arise from defects like oxide trapped charges and traps in the interface. In addition, advanced processes using HKMG devices have the potential to exacerbate the Effect of fixed charges in oxide. It may also lead to

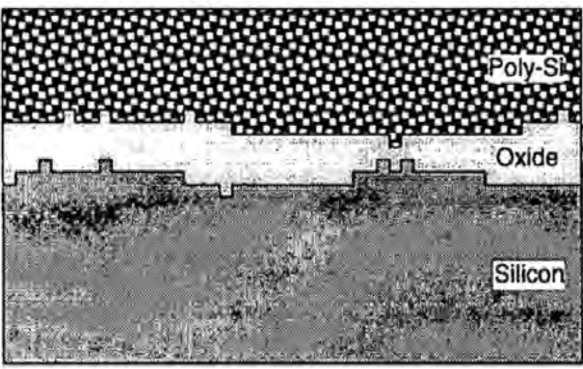


Fig. 1.4: Manifestation of dielectric thickness variation in a silicon technology [50].

fast transient charge-trapping and result in degradation of device parameters.

Time Dependent Breakdown of Dielectrics (TDBD): Breakdown of dielectric material was observed as a degrading mechanism even in older CMOS processes with thicker oxides (>10-nm) but the underlying complex mechanism was not well understood. However, the situation started to change during the nineties as the improved silicon platforms allowed a wider variety of oxide dimensions to be employed. In this respect, it was found that the gate drive of a device primarily depends on gate voltage and dielectric thickness and is governed by Fowler-Nordheim tunneling for thick-oxides and quantum tunneling for thin-oxides (and lower voltages) [52]. Depending on the strength of applied electric field and aging, the dielectric sees an accumulation of different types of defects like recombination centers, carrier traps, and interface states. Additionally, the mechanisms of defect generation include trap creation from anode degradation at low voltages and hole-injection/impact-ionization for induced defects at higher voltages. With the passage of time, the extent of damage to the dielectric is manifested by parameters like stress induced leakage current and ultimately leads to soft, progressive, or hard breakdown (SBD/PBD/HBD). Here, different modes of the mentioned breakdowns may occur independently or one following the other. For SBD, the increase in gate injection is rather slow and the device remains functional with degraded dielectric properties and increased gate noise. For submicron technologies below 180-nm (E_{ox}>2.4 MV/cm), SBD and PBD seem to be the dominant mechanisms behind dielectric degradation. Generally, the time to breakdown (T_{bd}) is defined with the help of instantaneous value of current density through gate dielectric (J_g). If Q_{bd} is the time integrated dielectric current density (which flows until the breakdown of dielectric), the following relationship will hold for constant voltage stress for thin oxides (where current changes very little before

breakdown) [52]:

$$T_{bd} = \frac{Q_{bd}}{J_g}. \tag{1.11}$$

On the other hand, in case of hard breakdown, the cumulative density function for time to breakdown F (T_{bd}) may be described with the help of Weibull probability distribution [53]

$$F(T_{bd}) = 1 - exp[-(\frac{T_{bd}}{\alpha})^{\beta}] \tag{1.12}$$

where and are process dependent factors, and typically, is called the characteristic life and is called the Weibull slope or slope parameter.

Bias Temperature Instability: Bias temperature instability (BTI) is another unreliability issue which affects all types of field Effect transistors after continuous operation at high temperatures. Two different forms of bias temperature instability have been experimentally verified: negative BTI (NBTI) and positive BTI (PBTI). Among the two, research on NBTI has been carried out for a longer period of time which shows that it can create threshold deviation across typical process, silicon oxynitride process, and next generation transistor structures. The mechanism behind BTI is not well understood and possible explanations have included build-up of charge in dielectric, interface states at oxide channel juncture, hole capturing by defects, and electron trapping by dielectric traps. Certain process steps like nitridation and surface channel devices are also believed to cause progression of BTI induced degradation. Historically, first attempts to explain bias temperature instability depended on reaction diffusion theory rather than charge trapping. It was able to explain the dependence of degradation on time adequately but fell short while trying to expound features of recovery. According to it, normalized reaction diffusion induced variation takes the form of [54]

$$\frac{\Delta V_t(t_s, t_r)}{\Delta V_t(t_s, 0)} = \frac{1}{1 + (\frac{t_r}{t_s})^{\frac{1}{2}}}. \tag{1.13}$$

Here, t_S and t_r are stress time and relaxation time. The equation assumes universal recovery where threshold deviation depends on the ratio of t_S and t_r, and the relationship is normalized with respect to its value at stress end point. But this supposition opposed observations which suggested that recovery progresses without depending on stress time and becomes operational even before stress end point. Therefore, more recent models of BTI assume a combination of a fixed element and a rectifiable part for process deviation. If n_f and n_r are rate coefficients for the fixed and the rectifiable parts, E_a is the activation energy, m_f is another constant for fixed degradation, and The image part with relationship ID rId32 was not found in the file. are process dependent factors, the threshold deviation model can be written as [55]

$$\Delta V_t \propto [exp^{(\delta_1 V_{gs})} t^{n_f} + {V_{gs}}^{\delta_2}\{m_f + n_r log(t)\}] exp^{(-\frac{E_a}{k_B T})} \qquad (1.14)$$

where the equation remains valid if the stress voltage remains unchanged.

Short Channel Limitation: Devices of a silicon technology may also suffer from modification of threshold and drift characteristics as a result of short channel limitations (SCL). SCL becomes a factor for field effect devices when its channel size becomes comparable with the width of junction depletion layers. It can be understood by the fact that channel depletion charge is not only balanced by gate charge, it is also partially adjusted by charge in source/drain junctions which, in turn, is strongly correlated with channel size. Consequently, device reliability may be influenced as channel limitation affects parameters which are supposed to remain invariable against bias condition and feature dimension. In addition, the physical phenomena through which SCL can manifest itself can be as varied as velocity saturation, scattering at surface, ionization by impact, and drain induced lowering of barrier. The threshold modification due to short channel limitation

can be approximated as [56]

$$\Delta V_t \propto (\frac{x_j}{2L_e})\sqrt{2q\epsilon_{si}N|2\phi_f|}[(\sqrt{1+\frac{2x_d}{x_j}}-1)+(\sqrt{1+\frac{2x_s}{x_j}}-1)]. \quad (1.15)$$

According to the formulation, the modification remains proportional to the factor of and becomes negligible for the condition . Here and are the depth of depletion regions associated with drain and source junctions, $_f$ is the fermi potential, and x_j is the junction depth at the edges of source and drain diffusion regions, which are modeled as quasi-circular arcs.

Supply and Temperature Variation: Apart from the phenomena related with device physics, CMOS reliability is also a ected by operation-related and ambient factors like supply and temperature variation. Involvement of aggressive scaling, design for high performance, higher operating frequencies, combination of multiple functionalities, and rising power density increase the probability of signi cant intra-die thermal variation. Among operating factors, continuous circuit operation can lead to supply noise and ultimately supply uctuation [57]. Moreover, silicon supply reliability may have a correlation with the architecture's voltage conditions. As companion to the main supply rail, CMOS structures typically require a number of scaled gate signals to place transistors in a suitable mode. If their number can be truncated, it would relax the circuit's voltage requirements and limit the combined upshot of multiple rail stability on overall performance. On the other hand, circuit induced variation of temperature may obtain the ability to produce nonuniform substrate thermal pro le and thermal gradients in the architecture. These uctuations have an impact on a number of circuit mechanisms including device transconductance and leakage current. Leak-age current is one of the non-ideal factors which may account for about a tenth of system's power requirement and its contribution is projected to increase by mul-tiple times for the future silicon technologies [58]. This phenomenon can have two

distinct sources: subthreshold leakage and gate leakage components. Subthreshold leakage was considered as the dominant source for older processes but gate leakage becomes equally important for technologies with scaled dielectric layers. In addition, fluctuation of operating and ambient factors has an influence on an architecture's current rating, which in turn determines several figures of merit for the circuit. As a result, system reliability is affected by unexpected deviation of supply voltage and system temperature.

The reliability events described in the previous subsections have the potential to significantly degrade circuit consistency, may lead to unacceptable circuit variation, and highlight the importance of considering process deviation during design phases of a CMOS system. Under such circumstances, a reliability improving technique may be included in circuits of a transceiver to reduce variation of the system's figures of merit. In case of submicron amplifiers, these RITs need to work with different voltage ratings and stabilitate characterizing parameters against deviation of process and system factors. In addition, it will be beneficial if the compensation technique can be adapted as a stabilizing mechanism for other blocks of the transceiver (e.g., oscillators) where it will face the challenge of improving the variability of a different set of frequency-dependent parameters.

1.3 Objective of the Thesis

1. The objective of this thesis includes devising a discrete modeling technique of and establishing common rail powered reliability improving techniques for nanoscale silicon transceiver circuits. At first, it will attempt to develop a scheme to accurately predict characteristics of complementary-metal-oxide-semiconductor (CMOS) circuits through geometry scalable modeling of their discrete components. It will focus on forecasting of noise, loss,

and gain parameters for complete architectures (e.g., low-noise amplifiers) rather than separate characterization of circuit elements (passives, transistors). It will try to regulate number of independent parameters needed for model equation formulation with symmetry of distributed model structures and through exploitation of parameter interdependency. Compact equations based on empirical modeling will be developed for devised equivalent-circuits of metal-insulator-metal capacitors (MIMC), planar-spiral-symmetric inductors (PSSI), polysilicon resistors (PSR), and active transistors. The models will cover the size of devices required in reported nanoscale CMOS circuits and modeled results will be compared against literature data for verification.

2. Additionally, the thesis will focus on a common rail powered technique to improve performance reliability of CMOS circuits through a shared bias network for active devices. The reliability improving circuit (RIC) will try to increase the stability of a topology's amplification (voltage gain, forward gain), noise (noise figure, minimum noise figure), and port loss (input/output reflection) against variation of process and voltage. It will be verified for a number of front-end architectures which will ensure that the RIC remains compatible with a wide range of isolation, noise, linearity, and gain requirements.

3. To investigate the reliability improving scheme's Effectiveness for additional transceiver blocks, it will be applied as a stabilizing gate circuit (SGC) to a harmonic oscillator against aspects of technology and system deviation. Without incurring significant power penalties, the SGC will attempt to im-prove the consistency of important oscillator parameters like phase noise, period jitter, and oscillation amplitude. Various phenomena related to pro-

cess fluctuation will be addressed through consideration of device threshold, feature dimension, and power rail variation. The technique will try to be efficient for a wide range of o set frequencies and it will be compared with reported compensation mechanisms.

4. As part of improving supply induced circuit reliability, the thesis will present techniques for a front-end amplifier which will allow it to be powered from a single low-voltage supply (reducing the probability of multiple rail variation of affecting circuit behavior). A gain control mechanism will be realized with an output block where the employment of a control voltage would achieve gain regulation. The inclusion of input common gate stages and buffer sections will be tried for a multistage circuit so that we could improve the probability of port reflectance remaining within design limits.

1.4 Organization of the Thesis

The dissertation consists of seven chapters. Chapter 1 focuses on the background of the research problem to clarify the motivation behind the initiative. It includes discussion on discrete modeling challenges of nanoscale complementary-metal-oxide-semiconductor circuits and process reliability of silicon transceiver components. The physical events which may lead to process unreliability are brie y explained. Additionally, an outline of objectives of the study is included.

In Chapter 2, a technique is presented to accurately estimate high frequency behavior of submicron amplifier circuits with geometry scalable discrete modeling. The scheme simplifies model formulae using dependent functions and symmetric modeling and modeled results are verified against literature data.

Chapter 3 demonstrates a low-power technique to improve performance reliability of nanoscale CMOS amplifiers. It permits the overall circuit to be driven

from a common supply rail and provides resistance against Effects of process and system variation.

In Chapter 4, a stabilizing gate circuit (SGC) is presented which reduces deviation of radio-frequency parameters of harmonic oscillators (improving their circuit reliability). The mechanism improves fidelity of oscillation amplitude, phase noise, and period jitter of single-ended and differential tuned oscillator structures.

Chapter 5 discusses an amplifier architecture with a voltage lowering technique to limit its susceptibility to supply induced circuit unreliability. The topology avoids use of scaled gate voltages and a gain control mechanism is realized with the output block of a cascaded structure.

In Chapter 6, a buffered amplifier suitable for applications requiring high degree of port isolation is devised. It demonstrates how optimization of an input stage and a load-port section may improve the architecture's port loss without burdening its noise contribution and power demand.

The thesis is finally concluded in Chapter 7 by presenting a summary of the research work and providing suggestions for future work.

Chapter 2

Accurate Geometry Scalable CMOS Modeling of Nanoscale Low-power Amplifier Circuits

2.1 Introduction

Silicon complementary-metal-oxide-semiconductor (CMOS) process was originally developed for digital applications and its use in analog integrated circuits was rather limited because of noise contribution of silicon devices at higher frequencies [59]. Therefore, when priority was given to ensuring superior high frequency behavior, processes based on compound semiconductors were usually preferred. However, scaling down of silicon technologies and concomitant improvement in process steps have reversed the situation and various monolithic integrated circuits have been reported in silicon for applications like oscillators, low-power amplifiers, bandpass filters, and correlators/mixers [60, 61]. At the same time, radio-frequency features of active CMOS devices have been continually improving with high unity gain frequencies being achieved by sub-180nm transistors [62,63]. In addition, apart from being compatible with existing digital foundry, CMOS technologies promote benefits like large manufacturing output and lower cost. Developing geometry scalable and accurate models of silicon elements can further facilitate this reduction of overhead as it may improve the efficiency of planning

and design phase of nanoscale transceiver circuits [64, 65]. Moreover, practical usefulness of the scheme will be improved if, rather than individual element characterization, the models can predict the behavior of entire circuits consisting of passive and active devices.

Recent literature has presented some modeling examples of CMOS elements [66{71] and, in most cases, they have concentrated on characterizing a specific component over a frequency range. In addition, when these models are based on device physics, inclusion of detailed material properties can make them burden-some for the estimation process. For example, models of 180-nm metal-oxide-semiconductor varactor and capacitor have been proposed in [66] which can pre-dict admittance parameters for frequencies up to 6 GHz. A distributed capacitor model which is able to forecast impedance matrix parameters has been verified in [67]. Modeling of CMOS power devices is discussed in [68] in relation to trade-o s associated with maintaining power efficiency and development of matching networks. Transistor modeling for radio-frequency design is also addressed in [69] in order to analyze thermal and frequency-dependent noise behavior. The concept of design space exploration for on-chip inductors is introduced in [70] with the help of closed-form mechanisms. Development of expressions of physical at-tributes for various shapes of planar inductors has been the focus of [71]. In contrast, this chapter presents a discrete modeling technique for metal-insulator-metal (MIM) capacitors, planar-spiral-symmetric (PSS) inductors, polysilicon (PS) resistors, and active transistors (AT) in order to estimate the behavior of 90-nm CMOS amplifier circuits. The scheme exploits interdependency of parasitic components to simplify device expressions and reduces number of independent functions through symmetric modeling. Equivalent-circuit equations are derived with geometry scalable empirical modeling on the basis of physical structures and incorporating associated parasites. They should be able to lower computational

complexity of the estimation process as they do not depend on detailed device properties for formulation. They are scalable with relevant geometric features, consistent with size of elements needed in nanoscale amplifier circuits, and use simple fitting factors to account for extraneous Effects in the structure. RF performance estimated by the discrete modeling approach (DMA) is compared with measured amplifier data collected from literature [72]. They predict the behavior of two high-gain/overvoltage-protected C-band amplifiers which manage 12.4-13.4 dB peak gain with low power (9 mW) and noise (2.7-2.9 dB) readings. The results suggest that the technique, which is based on parasitic models simplified by dependent functions, can characterize integrated amplifier architectures with relatively low computational cost.

The chapter is organized in the following way. Section 2.2 demonstrates silicon MIM, PSS, PS, and AT models and documents their behavior. Two high-gain and/or pulse-protected 1.2-V amplifiers are presented in Section 2.3 for testing of the models. High frequency parameters of complete circuits are estimated in Section 2.4 and verified against measured results. Finally, conclusions of the work are summarized in Section 2.5.

2.2 Modeling of CMOS Elements

In this section, silicon models are presented for active and passive CMOS components which are needed in nanoscale transceiver circuits. The models include appended elements representing junction (depletion) capacitance, thermal loss, substrate loss, coil parasites, high-frequency Effects, and parasitic capacitance (between active layer and substrate). At first, equivalent circuit analyses are completed for passive devices like MIM capacitor, PS resistor, and PSS inductor. Then, a scalable model for an active device is developed with the inclusion of

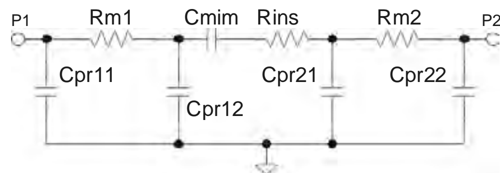


Fig. 2.1: Distributed RC model of MIM capacitor.

extrinsic RC elements with defined parameters. Finally, the geometry scalable simple models are employed to estimate measured behavior of 90-nm circuits to verify the accuracy of the modeling scheme.

2.2.1 Metal-insulator-metal Capacitor

A metal-insulator-metal (MIM) capacitor is often preferred for microwave transceiver circuits over other forms of silicon capacitors because of its quasilinear behavior against frequency and relatively high quality factor [73]. It uses a strip of dielectric lm (insulator) packed between two electrodes made with metal layers and produces values of significant picofarads. It can be used as a passive component for input-output matching circuits, signal coupling, power supply protection, resonance tanks, and feedback connections in monolithic integrated circuits. In a submicron amplifier architecture, capacitors typically serve as parts of load banks and impedance matching networks (at ports). Study of literature on nanoscale CMOS amplifiers shows their on-chip capacitors having values in the <8 pF range [72, 75-79], indicating that they could be adequately covered with an appropriate model of MIM capacitor.

The two-port RC (resistive-capacitive) model of MIM capacitor utilized in this study is presented in Fig. 2.1. In this circuit, C_{mim} represents the primary capacitive element created by placing two conductors on both sides of an insulating layer. Parasites associated with top and bottom electrodes are repre-

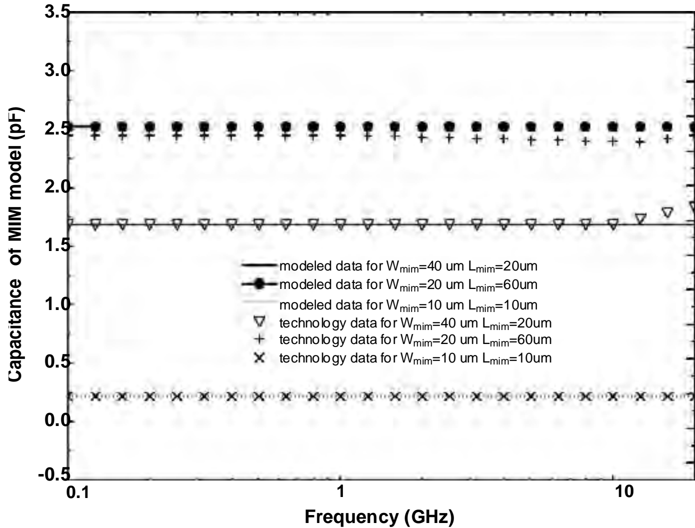


Fig. 2.2: Input capacitance of MIM model samples.

sented by R_{m1} and R_{m2} and thermal dielectric loss is accounted for with a series component R_{ins}. Four shunt elements are included in the structure to simulate substrate Effect as part of distributed modeling. They are indicative of capacitive parasites which exist between top and bottom metal layers and substrate. No resistive element is included in the shunt paths as thermal substrate loss is not considered in this MIM model. The inclusion of distributed sections in the structure improves its ability to capture the high frequency behavior of the element in integrated architectures. In this case, model equations are developed in terms of length (L_{mim}) and width (W_{mim}) of metal plates in the MIM structure. They are developed through geometry scalable empirical modeling as used in literature examples like [14]. These expressions, which are able to describe model behavior as a function of structural pattern, take the approximated form of

$$R_{m1} = \frac{20.35}{L_{mim}W_{mim}} - \frac{1.67}{(lnL_{mim})^2(lnW_{mim})^2}\ \Omega \tag{2.1}$$

$$R_{m2} = 0.67[\frac{125.9}{(L_{mim})^{0.5}W_{mim}} - \frac{230.3}{L_{mim}W_{mim}}]\ \Omega \tag{2.2}$$

$$R_{ins} = 0.5R_{m2} \tag{2.3}$$

$$C_{mim} = 3.71m + 0.5(W_{mim} + L_{mim}) + 2.05(L_{mim}W_{mim})\ fF \tag{2.4}$$

$$C_{pr11} = C_{pr12} = \frac{1}{3}[0.972 + 0.267(W_{mim} + L_{mim}) + 0.024(L_{mim}W_{mim})]\ fF \tag{2.5}$$

$$C_{pr21} = C_{pr22} = 0.5C_{pr11}. \tag{2.6}$$

Here L_{mim} and W_{mim} are expressed in um and the definition of R_{m2} includes a fitting parameter when the model is included in a complete circuit (assigning an optimized value to this factor can account for extraneous losses). C_{pr21}, C_{pr22}, and R_{ins} are defined as dependent parameters to simplify device expressions and reduce model complexity without compromising on estimation accuracy. The model remains valid when L_{mim} resides in the range of 5~60 um and W_{mim} has a dimension coverage of 5~100 um (which are expected dimensions of submicron capacitors). For example, if L_{mim} is set to 5 um, variation of W_{mim} over the full range (5~100 um) achieves modeled capacitance values of 0.05-1.1 pF. As C_{mim} scales directly with the features, setting L_{mim} to 20 um elevates this range to 0.22-4.2 pF. Over its full coverage, the model can produce 0.05-12 pF passive elements which are consistent with reported data on conductor-insulator capacitance and sufficient for size of capacitors required in nanoscale amplifiers. Moreover, the expressions should be able to reduce the computational complexity of the estimation process as compared to conventional technology models. Fig. 2.2 illustrates input capacitance produced by different MIM model dimensions over a frequency range of 0.1-20 GHz. To get an assessment of the model's power efficiency, its quality factor (Q_{mim}) is approximated with the following equation:

$$Q_{mim} = \frac{1}{\omega(R_{total})(C_{total})}. \tag{2.7}$$

When plotted as a function of device geometry in Fig. 2.3, sampled Q_{mim} achieves reasonable values of 10-390 between 1 and 10 GHz. Data obtained with the

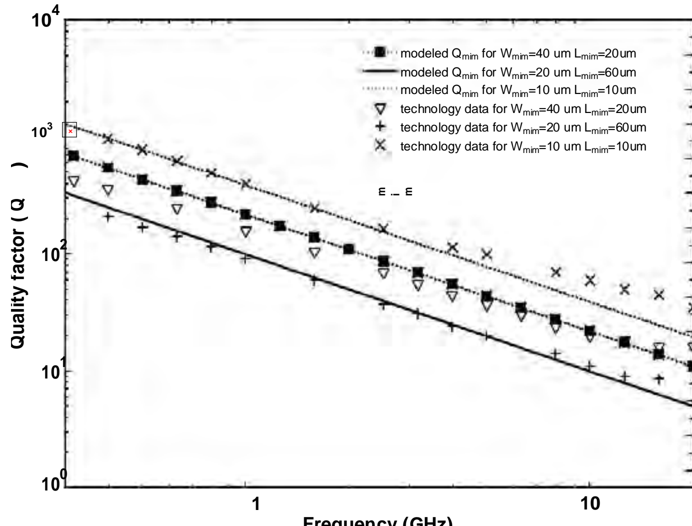


Fig. 2.3: Quality factor of modeled capacitors plotted against frequency.

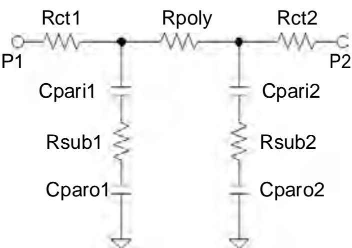


Fig. 2.4: Double-tee model of polysilicon resistor.

modeling technique remain reasonably consistent when compared with measured results of a 90-nm CMOS foundry [74] in the same figures.

2.2.2 Polysilicon Resistor

Polysilicon (PS) resistors are often considered suitable for nanoscale silicon circuits as they have smaller parasitic components as compared to other on-chip resistors. They are compatible with BiCMOS and CMOS processes and is able to offer high sheet resistance (ohms/square) [80]. Moreover, the resistivity of

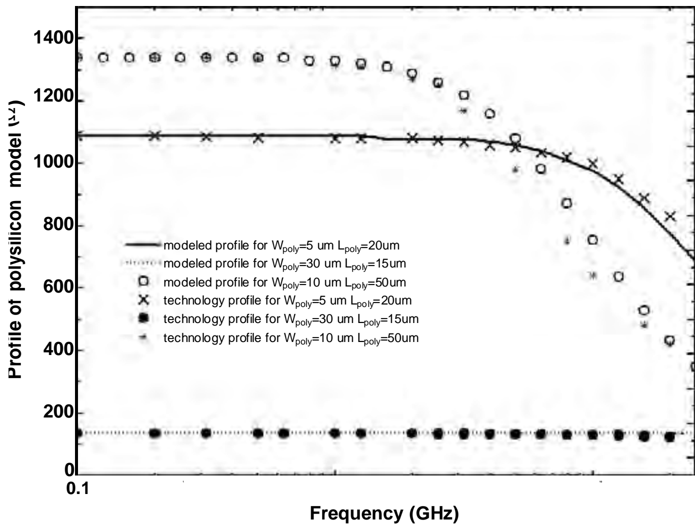


Fig. 2.5: Pro les of polysilicon model samples.

the structure is controlled by amount of doping in poly layers and grain boundaries present in deposits. Unlike di used (MOS) resistors, its inherent substrate parasites are not dependent on rating of bias voltages. PS layers occupy a relatively smaller area in traditional technologies and their temperature dependence is weaker than that of well and implanted resistors. Metal resistors are often dominated by variation of layer thickness which is not the case for poly resistors and, as a result, amount of conductivity modulation in the latter remains minimal. In addition, poly resistors are not dominated by piezoresistive Effect and can produce both small and large impedance values [81, 82].

Fig. 2.4 shows the polysilicon resistor model employed in this study. It has been developed to cover the range of resistance (0.05-20 k) required in reported amplifier circuits [75{79]. The equivalent circuit utilizes a double-tee RC network where resistive contribution of the poly layer is represented by R_{poly}. Peripheral resistance at the two ends of the poly deposit is accounted with R_{ct1} and R_{ct2}.

R_{sub} elements are included in the model to represent resistive loss in dielectric

base and substrate. Parasitic capacitors associated with the polysilicon layer and its oxide base are considered for the inclusion of C_{pari} and C_{paro}. An RCR branch on both sides of R_{poly} creates the two tee circuits of the model. Symmetry is maintained (with respect to R_{poly}) with the placement of R_{ct}, R_{sub}, and C_{par} elements to reduce the number of uncorrelated parameters. The components are assumed to be scalable with width and length of the deposited polysilicon layer (W_{poly} and L_{poly}). The geometry scalable empirical equations for the equivalent circuit are approximated as

$$R_{poly} = \frac{0.9L_{poly}}{3.389(W_{poly}) - 0.125}\ k\Omega \tag{2.8}$$

$$R_{ct1} = R_{ct2} = 591.2[exp(\frac{0.076}{W_{poly}}) - 1]\ \Omega \tag{2.9}$$

$$R_{sub1} = R_{sub2} = \frac{16.48}{L_{poly}W_{poly}} - \frac{30.49}{(L_{poly})^2 exp(W_{poly})}\ k\Omega \tag{2.10}$$

$$C_{pari1} = C_{pari2} = 0.5045L_{poly} + 0.7162(\frac{W_{poly}}{\sqrt{L_{poly}}})\ fF \tag{2.11}$$

$$C_{paro1} = C_{paro2} = 2C_{pari1}. \tag{2.12}$$

In these equations, L_{poly} and W_{poly} are expressed in a unit of um and a set of C_{par} elements are defined with dependent functions to simplify the model. With 1 um poly width, if L_{poly} scales from 1 to 100 um, the model can achieve an Effective resistance of approximately 0.3-28 kΩ. In comparison, if length to width ratio of the structure is reduced with increasing W_{poly} (1-60 um, L_{poly}=5 um), Effective model resistance drops from 1.4 k to 25Ω. For this circuit, capacitive parasites (C_{par}) are assumed to be smaller as compared to their counterparts in the MIM model. Table 2.1 presents Effective resistance of sample polysilicon models as a function of device geometry (within its range) and frequency dependent pro les of the two port equivalent circuit are illustrated in Fig. 2.5 along with technology data [74] obtained with similar features.

Table 2.1: Effective model resistance as a function of device geometry.

W_{poly} (um)	L_{poly} (um)	$\sim R_{model}$ (Ω)
1	60	16645.8
1	10	2860.8
5	20	1090.1
5	50	2695.1
10	90	2408.6
30	15	136.3
10	50	1342.6

2.2.3 Planar-spiral-symmetric Inductor

Spiral inductors play a critical role in determining RF performance of CMOS transceiver architectures where they are employed as part of load banks, tuned sections, band-pass lters, port matching circuits, and feedback networks. In these circuits, the on-chip planar spiral has to produce necessary reactance and reasonable quality factor simultaneously for ensuring optimum behavior. Addi-tionally, often polygon structures have to be adopted to satisfy restrictions of component angles which is further facilitated with symmetric realization of the

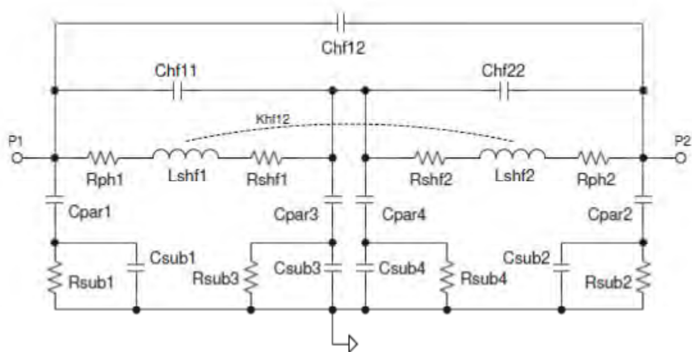


Fig. 2.6: Equivalent circuit model of planar-spiral-symmetric inductor.

spiral. As cost of tuned circuits is directly correlated with these spiral coils, their modeling has the potential to play an important role in limiting silicon manufacturing overhead.

The equivalent circuit of a planar-spiral-symmetric (PSS) inductor is illustrated in Fig. 2.6 which employs cascaded pi networks to represent different sections and distributed characteristics of a spiral. Each pi-shaped section is modeled with an RLC network including elements standing for coil parasites. L_{shf} represents the inductance of spiral sections and mutual inductive coupling between coil parts is modeled with the coefficient K_{hf12}. Thermal loss in the spiral is accounted with R_{shf} and peripheral resistance of each section (generated by underpass, contacts) creates the R_{ph} components. These parameters are de ned in this study in terms of outer diameter of the spiral (D_{sind}) and number of turns in the planer coil (N_{sind}). To reduce model complexity, other characterizing features like gap between spiral lines are assumed to have constant values. Among capacitive parasites, coupling capacitance between segments of each spiral section is modeled with C_{hf11} and C_{hf22}. Similarly, parasites created between different spiral sections are responsible for C_{hf12}'s inclusion. Parasitic components, which link each coil section to the substrate, are modeled through h-circuits which are initiated with C_{par}, and completed with R_{sub} and C_{sub}, standing for elements representing overall substrate Effect. The assumption of a planar symmetric structure allows the cascaded sections to be identical and avoid the use of multiple single-ended coil parts to achieve symmetry. Analytical equations for the spiral inductor take the form of

$$C_{hf11} = C_{hf22} = 1.378 - 0.1D_{sind} + N_{sind}(0.658 + 0.067D_{sind}) \quad fF \tag{2.13}$$

$$C_{hf12} = 7.59 + 0.067D_{sind} \quad fF \tag{2.14}$$

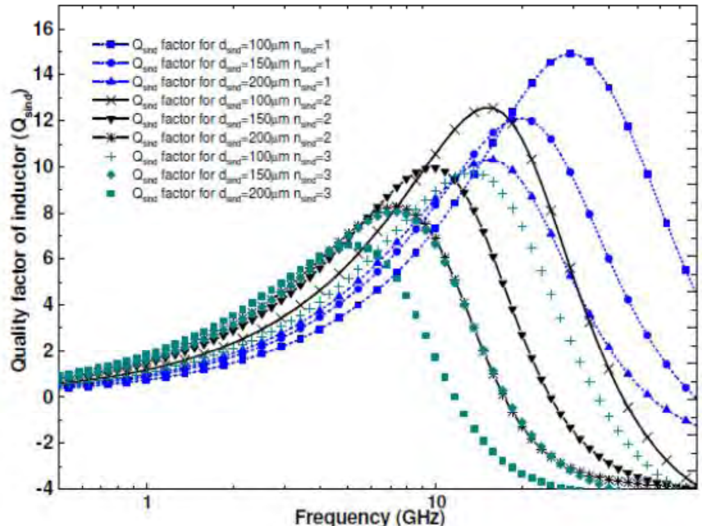


Fig. 2.7: Quality factors of the inductor model.

$$R_{shf1} = R_{shf2} = 397 + 0.152D_{sind} + (6.565D_{sind} - 408)N_{sind} \quad m\Omega \tag{2.15}$$

$$R_{ph1} = R_{ph2} = 0.11(N_{sind} - 1)\ \Omega \tag{2.16}$$

$$L_{shf1} = L_{shf2} = x_1(D_{sind})^{x_2} + x_3 \quad nH \tag{2.17}$$

$$\begin{aligned} \{x_1, x_2, x_3\}_{(N_s=1)} &= \{0.375m, 1.087, -16.15m\} \\ \{x_1, x_2, x_3\}_{(N_s=2)} &= \{0.774m, 1.168, -70.4m\} \\ \{x_1, x_2, x_3\}_{(N_s=3)} &= \{2.45m, 1.075, -228.2m\} \end{aligned} \tag{2.18}$$

$$K_{hf12} = 0.952 + 2.38mN_{sind} + 0.0379mD_{sind} \tag{2.19}$$

$$C_{par1} = C_{par2} = 0.164 + N_{sind}(0.274 - 0.795N_{sind} + 0.061D_{sind}) + 4.52mD_{sind} \quad fF \tag{2.20}$$

$$C_{par3} = C_{par4} = 0.208 + N_{sind}(0.71 - 1.86N_{sind} + 0.142D_{sind}) + 0.0123D_{sind} \quad fF \tag{2.21}$$

$$C_{sub1} = C_{sub2} = 0.5C_{par1} \tag{2.22}$$

$$C_{sub3} = C_{sub4} = 0.5C_{par3} \tag{2.23}$$

Table 2.2: Effective inductance of the PSS model.

D_{sind} (um)	N_{sind}	L_{sind} (nH)
300	1	0.68
200	2	1.21
300	2	2.12
200	3	1.69
300	3	3.58

$$R_{sub1} = R_{sub2} = x_4(D_{sind})^{x_5} + x_6 \;\; \Omega \tag{2.24}$$

$$\{x_4, x_5, x_6\}_{(N_s=1)} = \{83.08k, -1.087, 15.09\}$$

$$\{x_4, x_5, x_6\}_{(N_s=2)} = \{168.5k, -1.368, 28.72\} \tag{2.25}$$

$$\{x_4, x_5, x_6\}_{(N_s=3)} = \{92.26k, -1.23, 16.79\}$$

$$R_{sub3} = R_{sub4} = x_7(D_{sind})^{x_8} + x_9 \;\; \Omega \tag{2.26}$$

$$\{x_7, x_8, x_9\}_{(N_s=1)} = \{35.61k, -1.087, 6.468\}$$

$$\{x_7, x_8, x_9\}_{(N_s=2)} = \{72.21k, -1.368, 12.31\} \tag{2.27}$$

$$\{x_7, x_8, x_9\}_{(N_s=3)} = \{39.54k, -1.23, 7.198\}.$$

Symmetric circuit structure helps to limit number of independent model parameters for the inductor and dependent representation is used for the C_{sub} elements to allow model simplification. As reported low-power submicron am-pli ers (<6 dB NF) employ small inductors for loading and matching (0.1-4 nH) [72,75,76,78,79], the model adopts a range of 100-300 um and 1-3 for D_{sind} and N_{sind}, respectively, which allows it to generate necessary Effective reactance for low-noise circuits.

Fig. 2.7 presents a set of quality factor curves (Q_{sind}) obtained with the planar-symmetric-spiral model. It shows that peak Q_{sind} values of 7-15 can be achieved in the presented domain with a wide range of peak frequencies. To estimate quality factors, the inductor model is included in a two port circuit which predicts Q_{sind} (with the conventional two port definition) and effective

inductance (L_{sind}) with the help of imaginary and real parts of admittance or impedance parameters:

$$Q_{sind} = -\frac{Y_{11}(I)}{Y_{11}(\Re)} \tag{2.28}$$

$$L_{sind} = \frac{Z_{11}(I)}{2\pi f}. \tag{2.29}$$

Consequently, Table 2.2 documents sample values of calculated Effective inductance as a function of model geometry.

2.2.4 Scalable Active Device Model

The study uses a scalable model for transistors to address the limitations of active device modeling, which is a major concern in maintaining accuracy of nanoscale circuit simulation. A typical compact model of a metal oxide semiconductor de-vice is usually realized with parameters extracted at low frequencies [68]. However, devices suitable for high-frequency CMOS circuits need to include the Effect of additional junction parasites in the model. Keeping that in mind, the study realizes a scalable model (SM) which is presented in Fig. 2.8 and defined for

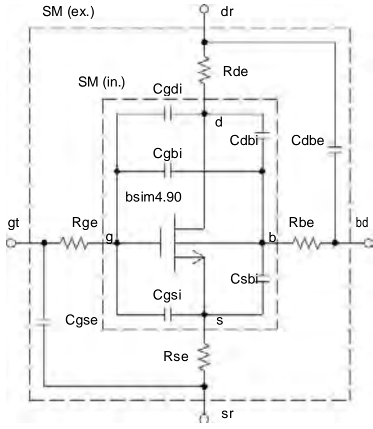


Fig. 2.8: Scalable composite model of an active device.

W_{sm}=25-300 um, covering typical device size required in transceiver amplifier circuits [75-78]. It is built upon a BSIM4 90-nm MOS model core where C_{gsi}, C_{gdi}, C_{sbi}, and C_{dbi} represent inherent junction parasites [23]. Among others, the defined model core includes the Effects of asymmetric/bias-dependent modeling, charge partition, gate-induced drain leakage, gate dielectric tunneling current, high-speed considerations, and asymmetric source/drain junctions. On the other hand, the overall scalable model is developed as a function of device width (W_{sm}) and number of fingers (NF). It assumes small extrinsic elements at the transistor terminals (R_{ge}, R_{se}, R_{de}, and R_{be}) to account for losses not predicted by the core.

C_{gse} is included due to high-frequency fringe parasites associated with MOS gate and source terminals. C_{dbe} performs a similar function for drain and body terminals of the device. In addition, core and external sections of the scalable model are designated as SM(in.) and SM(ex.). The estimated expressions of defined parameters of the external section are as follows.

$$R_{se} = R_{be} = \frac{8.15}{7.88m + \frac{0.242W_{sm}}{5}}\ \Omega \tag{2.30}$$

$$R_{de} = \frac{9.85}{\frac{0.252W_{sm}}{5} - 0.0183}\ \Omega \tag{2.31}$$

$$R_{ge} = \frac{18.6}{\frac{2.154W_{sm}}{5} - 10.379}\ \Omega \tag{2.32}$$

$$C_{gse} = 5.33[0.2093W_{sm} - 0.0489](\frac{W_{sm}}{10NF})\ fF \tag{2.33}$$

$$C_{dbe} = 0.0176[0.118W_{sm} + 0.409)](\frac{W_{sm}}{10NF})\ fF. \tag{2.34}$$

In these equations, W_{sm} has a unit of m and the resistive components need to include a tting factor when the transistor is placed in a CMOS circuit (which can model the Effect of extraneous losses associated with an active device). In the next section, the presented models are utilized to estimate the behavior of two 90-nm C-band low-power amplifiers.

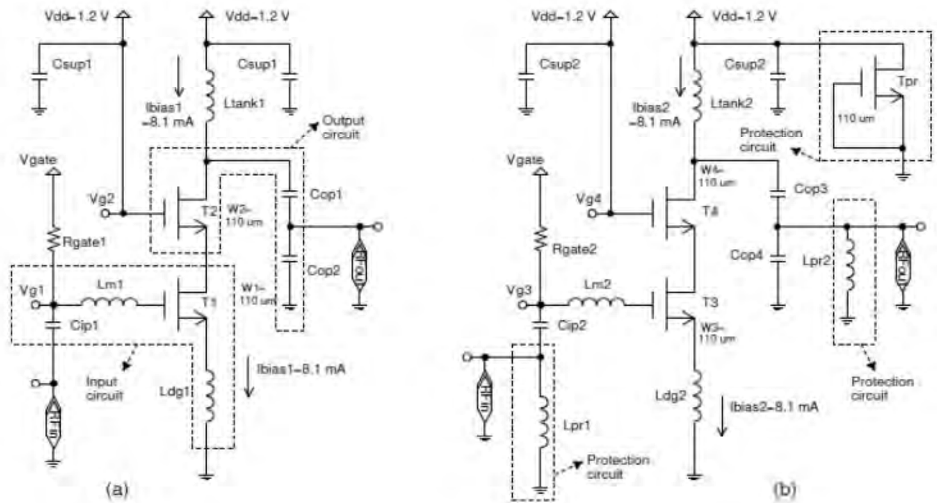


Fig. 2.9: CMOS circuits analyzed with the models: a) matched nanoscale low-power amplifier and b) overvoltage-protected amplifier.

2.3 Modeling of Nanoscale Amplifiers

The objective of the models developed in this chapter is to estimate the microwave behavior of transceiver amplifier circuits. With that view, the models are employed to analyze the performance of two reported 90-nm low-noise amplifier (LNA) circuits [72] with an RF simulator. The architectures consist of active and passive elements which fall within the models' range. Their topologies are illustrated with the help of Fig. 2.9(a) and Fig. 2.9(b). These structures are suitable for implementing low-dissipation low-NF front-ends with a supply rail. The first LNA aims to provide high power gain and port isolation while the second architecture includes passive on-chip protection against electrostatic discharge (which becomes a design issue as gate oxides are scaled down). Fig. 2.9(a) shows back to back connected common-source (CS) and common-gate (CG) stages which realize a cascode structure with two transistors. These devices are of identical size and powered by a main supply voltage of 1.2-V. The input CS transistor (T_1) is biased with a smaller gate supply (V_{gate}). Overall bias current drawn from V_{dd}

is 8.1 mA which results in a power dissipation of 9.7 mW for the amplifier. The LNA's input port is matched to a preceding component (~50 Ω) with an input coupling element C_{ip1} and a gate inductor L_{m1} which cancel the capacitive part of input impedance (Z_{in}). Additionally, adjustment of $Z_{in}(R)$ is managed with a small source inductor L_{dg1} which introduces modification of gain [83]. The cascode device T_2 is biased with the supply rail (V_{dd}) and a CC (double capacitive) circuit at RF_{out} port (C_{op1} and C_{op2}) forms the load with L_{tank1} and manages output impedance.

Fig. 2.9(b) presents the second nanoscale architecture which incorporates reactive and active protection circuits into the low-power amplifier. Its core transistors (T_3 and T_4) are equivalent in size and drain a similar amount of power from the supply rail (9.7 mW) as compared to the first amplifier. It also includes an isolating resistor (R_{gate2}) to deliver V_{gate} to the input of the driving device and houses a supply capacitor (C_{sup2}) to protect the circuit from possible noise of the voltage rail. The inductor of its input protection circuit (L_{pr1}) cancels parasites associated with RF_{in} port and its own resistive component makes a parallel circuit with matched input impedance. L_{pr1} protects the gate oxide of input driving transistor by allowing large voltage drops across it (in response to discharge pulses). This permits excess voltage at the gate of T_3 to be kept below the breakdown level. L_{pr2} introduces overvoltage protection in a similar fashion for the output port. A relatively long channel gate-source shorted de-vice T_{pr}, which is not a part of the amplifying circuit, is connected to the V_{dd} rail to safeguard it from discharge pulses. Input and output matching circuits of the overvoltage-protected amplifier use components similar to the first nanoscale amplifier. Measured data of the two 90-nm amplifiers (indicative of their performance) are collected from literature to compare them with results obtained with the geometry scalable discrete modeling approach.

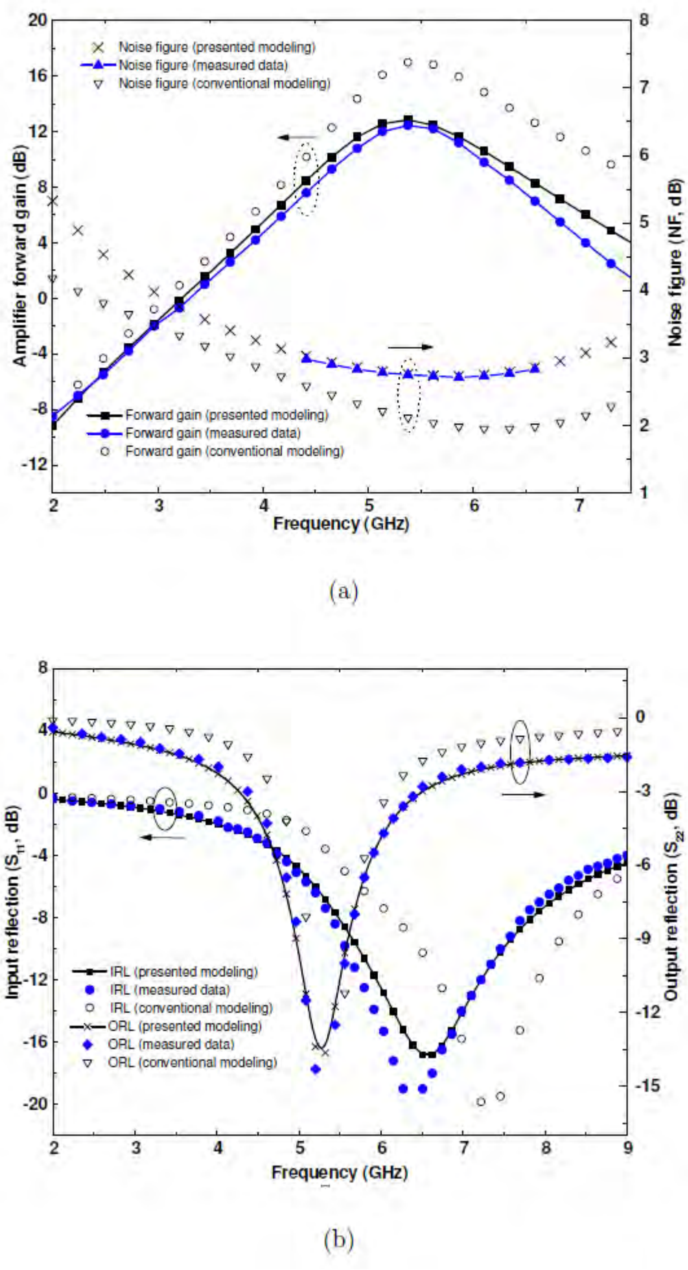


Fig. 2.10: Comparison in terms of a) forward gain, noise-figure and b) input reflection, output reflection between modeled and measured [72] results of thefirst amplifier.

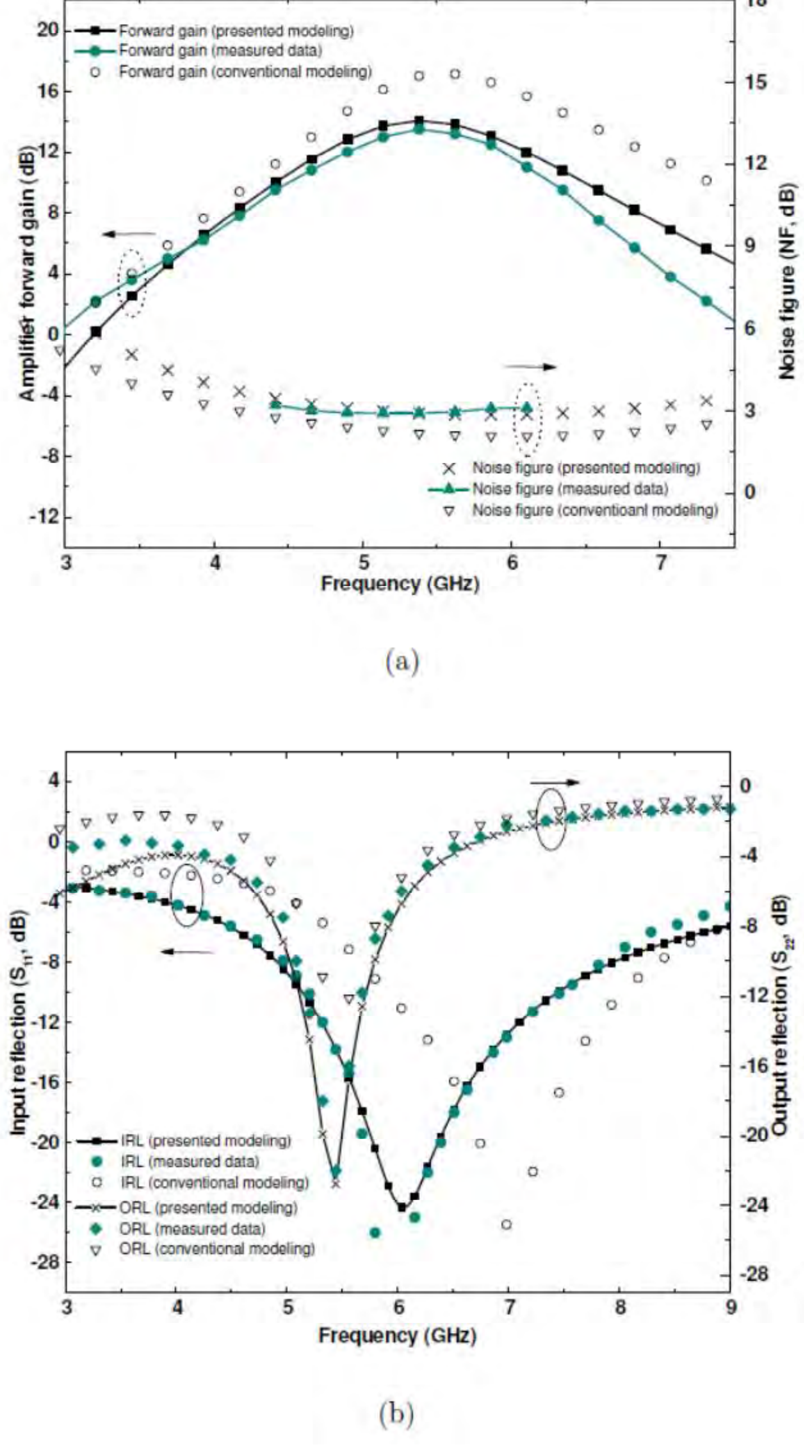


Fig. 2.11: Comparison between modeled and measured [72] data of the overvoltage-protected amplifier with respect to a) forward gain, NF and b) S_{11}, S_{22}.

2.4 Comparison of Performance

The results obtained with the presented low-cost modeling approach (DMA) and a 90-nm CMOS technology and measured microwave parameters of the first low-power amplifier are illustrated with the help of Fig. 2.10(a) and Fig. 2.10(b). Fig. 2.10(a) demonstrates noise and gain figure curves where modeled (DMA) forward gain has a peak of 12.8 dB at 5.4 GHz with a 3-dB bandwidth (BW) of

4.6-6.2 GHz. Noise-figure (NF) of the amplifier remains below 3.6 dB within the C band (4-8 GHz). Bandwidth limited NF has a centered minimum of 2.73 dB which is raised to 2.77 dB and 2.96 dB at the two edges of BW. Gain performance assessed from measured data is consistent with DMA results with a peak gain of 12.4 dB (difference: 3.2%) and a bandwidth of 4.7-6.1 GHz. In addition, measured NF has a reading of 2.70 dB at peak gain frequency and is indicative of greater model accuracy (matching: 98.9%). Reflection-loss at the amplifier ports is demonstrated in Fig. 2.10(b) for S, C, and X band frequencies. In case of input reflection (S_{11}), DMA and measured data are better than -3.4 dB and -3.7 dB over their message bandwidths, respectively. On the other hand, BW limited output reflection (S_{22}) is lower than -3.8 dB and -4.0 dB for the two sets of data, indicating they are consistent around the center frequency.

Fig. 2.11(a) and Fig. 2.11(b) document comparative results for the second C-band amplifier with reactive-active protection circuits. It achieves a better input matching performance than the first LNA which leads to a marginally higher forward gain. It is noticeable that range of bandwidth is not significantly influenced with the inclusion of pulse-protection elements in the front-end. The modeled (DMA) circuit has a gain of 13.9 dB at 5.53 GHz whereas the measured peak of 13.4 dB is located at 5.5 GHz (matching: 96.3%). Measured NF for the overvoltage-protected circuit is 2.95 dB at peak gain frequency whereas centered

NF for the DMA circuit has a value of 2.86 dB (error: 3.1%). For both measured and simulated (DMA) data, NF remains better than 3.2 dB over the circuit bandwidth. In case of output reflection (S_{22}), the two curves remain consistent with each other over the 4-9 GHz frequency range. As a result, S_{22} approaches -19 dB around the operating points and stays below -4.5 dB over both bandwidths. Correspondence between the two sets of data is also maintained for input return-loss (S_{11}) with measured and DMA readings near 5.5 GHz being registered as -14.4 dB and -14.6 dB, respectively. On the basis of these results, it can be said that the presented scheme, which is based on distributed parasitic models, is able to accurately estimate CMOS characteristics of integrated amplifier circuits with low computational complexity.

2.5 Conclusions

A geometry scalable modeling technique of nanoscale submicron amplifier circuits (comprising active/passive components and bias/gate supplies) is presented in this chapter. Modeled characterizing parameters of circuits are compared against literature data showing good prediction accuracy. The scheme limits number of required independent parameters by symmetric modeling and simplifies model expressions by utilizing interdependency of parasites. Analytical empirical equations capable of device characterization at low computational cost are derived for CMOS elements (spiral planar inductors, active devices, metal insulator capacitors, and polysilicon resistors) needed in a front-end amplifier architecture. The equations are scalable with feature size of RLC and transistor elements and cover expressions for parasites generated from process considerations. The models have been tested with two 90-nm low-power amplifier topologies where modeled results prove to be consistent with relevant experimental figures (noise, reflectance, gain).

Chapter 3

Common-rail Powered Reliability Improving Technique for CMOS Amplifiers

1.5 Introduction

As submicron CMOS technologies are reducing feature size to improve integration efficiency and ease supply burden, on-chip integrated circuits are becoming more vulnerable to performance issues arising from process, technology, and system variation [84, 85]. For example, active devices in a transceiver circuit may suffer from altered turn-on voltage due to silicon aging [86] and random dopant perturbations [87]. Typical and reverse short channel limitations can aggravate this problem as nanoscale nodes get smaller in feature size [88]. In addition, speed of devices has the potential to be affected by uncontrolled parametric deviation and scaling down of technology. On top of that, variability of manufacturing steps like mechanical polishing, lithography, etching, and spatially changing pattern density can alter predetermined component dimensions in small degrees [89]. Besides, ambient factors like die temperature fluctuation and ripples in supply rail play a role in setting of design tolerance limits [90]. The presented phenomena highlight the importance of considering process and system variation during design phases of CMOS systems

The objective of including a reliability improving circuit (RIC) in a CMOS architecture is to reduce variation in the system's figures of merit (FOM). In this respect, recent literature has addressed the issue of improving tolerance to process variability for devices and mixed-signal circuits [86], [91{103]. For example, a reliability sensitive silicon power amplifier is presented in [86] which can be integrated with a Wi-Fi receiver to mitigate discharge/aging issues. The dependence of hot carrier reliability (HCR) on contact spacing (source/drain) and its subsequent effect on device behavior (in a radiation environment) have been discussed in [91]. A compact model for transistor degradation due to channel hot carriers and thermal instability is proposed in [92]. The formulation of a scalable technique has been demonstrated in [93] for analysis of large circuit delay degradations (due to HCR). A current source based process-voltage sensing circuit is discussed in [94] to improve the stability of a power amplifier's efficiency. The ability of a double resonant network to reduce voltage stress on silicon devices is studied in [95]. Drego et al. [96] documents the implication of threshold voltage variation for scaling of supply voltage and the effect of adaptive body voltage on an externally gate biased input device has been demonstrated in [97]. A bank of digitally switchable capacitors is employed by [98] in an effort to provide resistance against variation in amplifier performance. A self healing front-end is developed in [99] using a reconfigurable architecture against varying process factors. The capacity of a feedback network to stabilitate gain is manifested in [100] for a 5 GHz amplifier. To achieve the same effect, a temperature compensation technique is presented in [101] for a wideband code division multiple access (WCDMA) amplifier. The concept of self-calibration for a mixed-signal high speed digital-to-analog converter (DAC) is introduced in [102] using trimming of analog current. Transistor sizing techniques are proposed in [103] to counter negative bias temperature instability (NBTI) in ip-ops and digital circuits.

Additionally, [104] demonstrates how reliability considerations can affect the RF potential of a submicron technology. These examples evince the necessity of developing process compensation mechanisms which are compatible with CMOS architectures.

This chapter presents a low-power reliability improving circuit (RIC) for nanoscale front-end amplifiers using a multisection integrated bias scheme. It utilizes a shared voltage network for transistors enabling the amplifier to avoid external sources other than the main supply rail. The RIC is tested for three CMOS amplifier topologies with different voltage ratings (1.2-V and 0.7-V) suitable for low-noise front-ends. It is able to stabilitate their performance significantly against variation of process factors and supply. Compatibility with diverse architectures allows the circuit to satisfy a broad range of noise, gain, isolation, and linearity requirements. The chapter is organized in the following way. Section 3.2 presents the common-rail powered reliability improving scheme and explains its mechanism. Three single-supply amplifier configurations are presented in Section 3.3 which can be integrated with the RIC. The results of improvement in reliability of performance (in terms of parameters like noise-figure, forward gain, voltage gain, return-loss) and comparison between compensation techniques are demonstrated in Section 3.4. Section 3.5 documents conclusions of the work.

2.2 Reliability Improving Circuits (RIC)

A submicron circuit can be subjected to modification of process parameters, device threshold, and element features (dimensions of on-chip components) during fabrication stages and service in systems. As a result, performance determining figures of the circuit undergo differing degrees of fluctuation, which may compromise the reliability of the circuit output. Apart from manufacturing deviations,

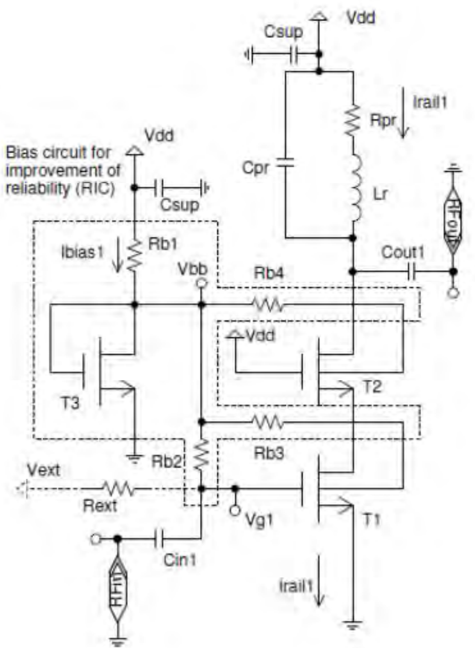


Fig. 3.1: The reliability improving circuit (RIC) applied to an unmatched amplifier.

a transceiver may also have to face variable ambient-voltage factors like changing system temperature and regulation of dc supply. A reliability improving circuit (RIC) aims to enhance the stability of a CMOS structure against these variables and, in the process, make it more robust against performance degradations.

The low-power RIC studied in this chapter is suitable for use in CMOS amplifiers necessary in transceiver circuits and applied to a low-noise amplifier (LNA) to minimize variation in figures-of-merit like forward gain (S_{21}), noise-figure (NF/NF_{min}), power requirement, and return-loss (RL). The RIC is presented in Fig. 3.1 where it attempts to limit process induced increase in amplifier noise and drop of power gain by regulating bias condition of devices through a shared voltage network. The figure shows the RIC being applied to an unmatched common-source-gate amplifier, which is a structure built on a pair of transistors. Typically in a cascode topology, the driving transistor (T_1) is biased

with an external gate voltage (V_{ext}) and the isolating transistor (T_2) is biased from the main supply rail (V_{dd}). In contrast, the RI circuit of Fig. 3.1 uses a diode connected device to produce the gate voltage from V_{dd} which makes the separate dc supply V_{ext} redundant. The values of bias voltage (V_{bb}) and current (I_{bias1}) can be regulated by the relatively small resistor R_{b1} and the size of T_3. This network has three branches formed by separate resistors (R_{b2}-R_{b4}) so that the voltage circuit remains isolated from amplifier core. Apart from providing the input device's gate signal, it also delivers substrate voltages for core amplier transistors. The supply capacitor C_{sup} is added to protect the circuit from ripples of V_{dd} rail. Here, L_r is the amplifier's resonating drain inductor and R_{pr},

C_{pr} are its parasitic elements. V_{dd} and other bias signals ultimately determine the amplifier's core tree current (I_{rail1}) and the corresponding small signal gain. Thus, the RIC is able to generate necessary bias signals from a single supply rail (V_{dd}), eliminating the necessity for smaller supply voltages.

Among all receiver circuit components, process variation has the most prominent effect on features of silicon transistors [105, 106]. For example, sequential and spatial reliability phenomena (e.g., aging of devices, breakdown of oxide, hot carrier effect, and fluctuation of channel dopant profiles) can lead to deviations in transistor threshold voltage. In the presented mechanism, the biasing device allows control of the voltage regulating current which will not be possible with the external supply V_{ext}. In addition, employing a >3 kΩ resistor (R_{b2}) separates small signal operation from the biasing arrangement. If the transistors of the circuit have nearly equal V_{gs} ratings (voltage stress), their device thresholds (V_t) are expected to deviate from base value in a similar fashion. In this setup, overdrive voltages of T_3 and T_1 are controlled by the appended circuit and gate of T_2 is provided with a fixed bias. If the device threshold of T_3 increases, it would reduce its available overdrive voltage and drain current I_{bias1} will suffer. As a result, the

drop across R_{b1} will be reduced, leading to an increase in T_3's gate-source voltage and restoration of its branch current. Thus, the configuration is able to regulate its drain current against the variable effect of stress conditions. In addition, when device threshold for the input transistor is raised, it tends to reduce the amplifier tree current (I_{rail1}). However, I_{bias1} is lowered simultaneously, and overdrive voltage for T_1 (V_{od1}) is brought back near design level. During the process, the gate current for T_1 (which is very small) and the bias resistors do not influence bias voltages significantly. In this manner, the RIC is able to compensate for possible fluctuations in the amplifier's rated current. Note that, the self-regulation can also account for decrease in device turn-on voltage. If device threshold for the transistors is lowered, it would raise their drain currents which, in turn, will bring down gate-source voltages for the transistors. This way, the RIC can contribute to furthering the reliability of CMOS circuits against outcomes of process variation. The concept of improvement in circuit consistency can be extended against alteration of other process related parameters like feature size and device parasites. As these factors may affect and moderate current values, the resulting modification in performance is compensated by the scheme in the same manner as described before. Consequently, a stabilized nanoscale amplifier can maintain regulated bias/tree currents and reduce variation of its RF parameters. The device voltage equations of the structure can be approximated with the following expressions:

$$V_{od1} = V_{gs1} - V_{t1} = V_{dd} - R_{b1}I_{bias1} - R_{b2}I_{g1} - V_{t1} \tag{3.1}$$

$$V_{od2} = V_{gs2} - V_{t2} = V_{dd} - V_{s2} - V_{t2} \tag{3.2}$$

$$V_{od3} = V_{gs3} - V_{t3} = V_{dd} - R_{b1}I_{bias1} - V_{t3}. \tag{3.3}$$

If amplifier transistors are operating in a region of saturation, their drain currents

can then be estimated from

$$I_{rail1} = \frac{\beta_n W_1}{2L_1}(V_{dd} - R_{b1}I_{bias1} - R_{b2}I_{g1} - V_{t1})^2 \tag{3.4}$$

$$I_{bias1} = \frac{\beta_n W_3}{2L_3}(V_{dd} - R_{b1}I_{bias1} - V_{t3})^2 \tag{3.5}$$

where $_n$ is the process dependent transconductance factor for transistors.

Apart from process variation due to aging, transistors of the amplifier also suffer from events like short channel limitation and dielectric thickness variation as their feature size is scaled by a submicron process. These phenomena may also modify the device threshold with respect to the process determined base and be addressed by the RIC. As the biasing device of the presented circuit settles voltages without participating in RF operation, it does not face restrictions on its feature size. On the other hand, the substrate bias connections provided by the same RIC further improve the limitation imposed on transistors by process and threshold fluctuation. It can be explained by defining the driving threshold as a function of its source-substrate bias (Vsb1)

$$V_{t1} = V_{t10} + \Delta V_{t1}. \tag{3.6}$$

Here, V_{t10} is the nominal value of process-dependent turn-on voltage for V_{sb1}=0 and a small drain-source voltage. The threshold deviation (V_{t1}) due to body effect in silicon transistors maintains the following relationship [107]

$$\Delta V_{t1} \approx \gamma_1(\sqrt{V_{sb1} + 2\phi_{F1}} - \sqrt{2\phi_{F1}}). \tag{3.7}$$

Here, ϕ_{F1} and γ_1 are fermi voltage (potential across the depletion region when a channel is present) and body coefficient for the driving transistor which are dependent on intrinsic carrier concentration (N_{i1}), substrate dopant density (N_{s1}), and gate capacitance per unit area (C_{ox1}). Their expressions take the form of

$$\phi_{F1} = ln(\frac{N_{s1}}{N_{i1}})(\frac{k_B T}{q}) \tag{3.8}$$

$$\gamma_1 = \frac{\sqrt{2\varepsilon_s q N_{s1}}}{C_{ox1}}. \tag{3.9}$$

With the bias scheme providing dual responsive substrate bias for T_1 and T_2, their source is expected to be at a lower potential. As a result, the V_t term of the stabilized circuit senses and helps to regulate threshold modification of nanoscale transistors and improve reliability of performance (against varying process factors).

The effect of the scheme in compensating supply rail deviation can be understood by analyzing the influence of V_{dd} on the bias signal of an RIC integrated amplifier. Using Eq. (3.5), V_{bb} for the improved amplifier can be modeled as

$$V_{bb} = V_{dd} - \frac{\beta_n W_3 R_{b1}}{2L_3}(V_{dd} - R_{b1} I_{bias1} - V_{t3})^2. \tag{3.10}$$

On the basis of this equation, an expression for V_{bb} can be obtained as

$$\Delta V_{bb} = [1 - \frac{\beta_n W_3 R_{b1}}{L_3}(V_{dd} - R_{b1} I_{bias1} - V_{t3})]\Delta V_{dd} \tag{3.11}$$

which represents possible enhancement of supply rail stability provided by the reliability improving technique. As a result, the stabilized architecture will be expected to face less deviation in bias signals (and FOMs) in the face of supply variation.

2.2.4 CMOS Single-supply Amplifiers with RIC

2.4 1.2-V High-gain CC Amplifier

The effectiveness of the proposed reliability improving circuit (RIC) is tested with three low-power CMOS amplifiers presented in Fig. 3.2 and designed with a 90-nm technology. These topologies can cover a wide range of design requirements for a receiver in terms of gain (S_{21}), power, port isolation, noise-figure (NF/NF_{min}), linearity range, and input/output reflection-loss (IRL/ORL). Fig. 3.2(a) presents

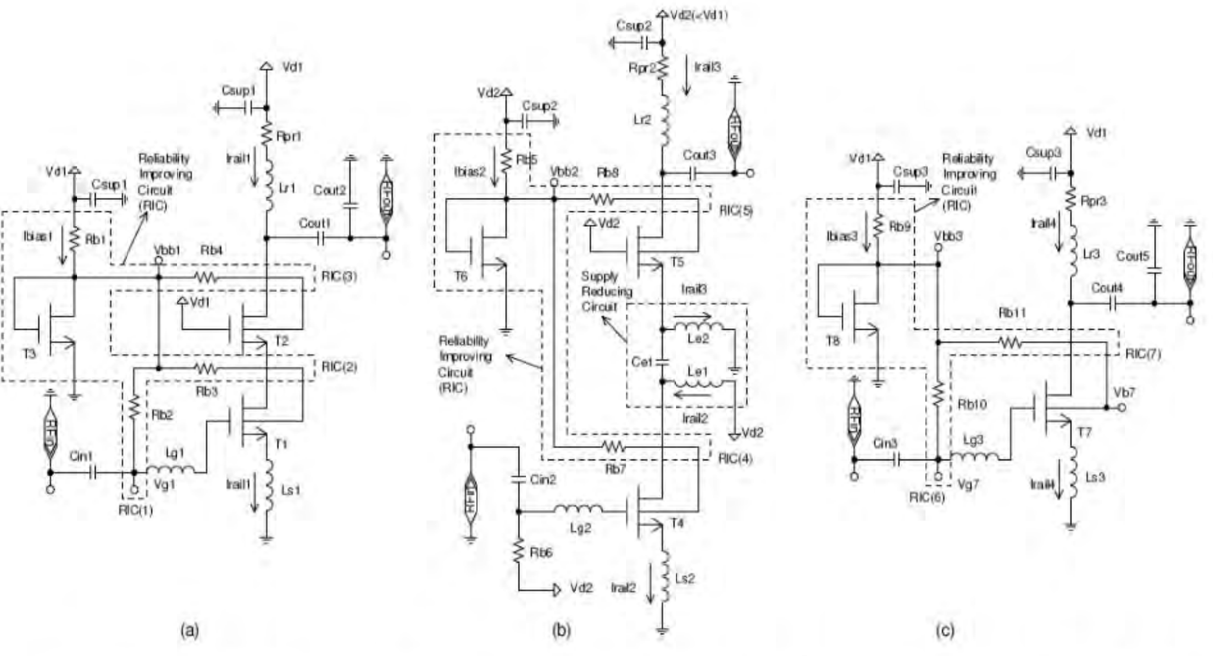


Fig. 3.2: Application of the RIC to a) a 1.2-V common-source-gate (CC) amplifier, b) a low-voltage (0.7-V) CC amplifier, and c) a 1.2-V common-source (CS) amplifier.

a matched common-source-gate (cascode, CC) amplifier including the multisection RIC and driven by the supply rail V_{d1} (1.2-V). Its two core transistors are identical in size (40 m) and L_{r1} is employed to settle its peak gain frequency in K-band. The biasing gate-drain-shorted transistor T_3 is not part of the amplifying circuit. It determines the bias current I_{bias1} along with the resistor R_{b1}. The three branches of the RIC are separated by 3.2 k resistors (R_{b2}-R_{b4}) and designated as RIC(1), RIC(2), and RIC(3), respectively. The scheme generates its bias signal V_{bb1} from the 1.2-V supply rail V_{d1}. The core current of the compensated amplifier (I_{rail1}) is settled to 3.28 mA, including an additional power requirement of 0.9 mW for the RIC. The amplifier's input matching network is made with two inductors (L_{s1} and L_{g1}), a coupling-cum-matching capacitor (C_{in1}), and gate parasites of the input device. In contrast, it has a capacitive output network (C_{out1} and C_{out2}) which, along with drain parasites of the isolating transistor, serves as part of the resonating tank. Peak gain, center NF, IRL, ORL, and NF_{min} for the externally gate-biased 1.2-V CC amplifier are 11.1 dB, 3.21 dB, -10.7 dB, -17.3 dB, and 3.15 dB, while the respective parameters settle to 11.4 dB, 3.19 dB, -11.1 dB, -21.2 dB, and 3.12 dB after including the RIC.

1.6 Low-voltage CC Amplifier

As supply voltage gets smaller with the scaling down of process (or even within the same process node), silicon CMOS circuits tend to become more susceptible to events related to system variation. To verify the presented circuit's effectiveness in such cases, a low-voltage CC amplifier (V_{d2}=0.7-V) is demonstrated in Fig. 3.2(b). A CC amplifier, when being driven by a typical 90-nm supply (V_{d1}=1.2-V), requires a smaller gate supply for the driving transistor. This situation can be averted with the low-voltage RIC inclusive CC architecture of Fig. 3.2(b). Here, insertion of a supply reducing circuit (SRC) sections the bias path for the

transistors so that they can powered with separate currents (I_{rail2} and I_{rail3}). It allows core devices to be biased by the same supply at gate and drain terminals. T_4 and T_5 have the same aspect ratio like their counterparts in the 1.2-V CC amplifier. The SRC is placed between two stacked circuits (common-source and common-gate) and made with inductors L_{e1}, L_{e2} and a coupling capacitor C_{e1}. The RIC, in this case, is designed with T_6 which produces the bias signal V_{bb2} from the scaled supply rail. Now the scheme does not have to provide for the gate signal of T_4 as both core transistors can be gate biased by the main supply V_{d2}. As a result, the low-voltage CC amplifier can be powered from a single scaled rail. For this topology, the RIC delivers biasing signals through R_{b7} and R_{b8} and its two sections are designated as RIC(4) and RIC(5). Power demand of the RIC network in this low-voltage amplifier is around 1 mW. On the other hand, output return-loss (ORL) is managed by the coupling capacitor C_{out3} (without additional passive elements) and the load (tank) reactance. The resonating load inductor is slightly larger than its 1.2-V counterpart and the load settles its operating frequency in lower K-band.

2.3 1.2-V CS Amplifier

The RIC is also tested with a matched common-source (CS) amplifier, as shown in Fig. 3.2(c), which can be utilized in a receiver when priority is given to limiting noise ceiling and wider linear behavior. In contrast, the CC amplifiers are employed when better reverse port isolation and higher forward gain are preferred. The CS amplifier is powered by a single 40 m transistor (T_7). The diode connected device in the RIC generates the voltage V_{bb3} from the 1.2-V main supply (V_{d1}). Two branches of the reliability improving circuit RIC(6/7) bias the driving transistor through R_{b10} and R_{b11}. In this case, core tree current with the bias circuit (I_{rail4}) is 3.02 mA and additional power consumption incurred

by the RIC is only 0.7 mW. Peak gain, center IRL, ORL, NF, and NF_{min} before appending the stabilizing network are 8.97 dB, -5.4 dB, -13.4 dB, 2.74 dB, and 2.57 dB for the CS amplifier. With the RIC's addition, these parameters are modified to 9.65 dB, -4.9 dB, -13.6 dB, 2.71 dB, and 2.54 dB.

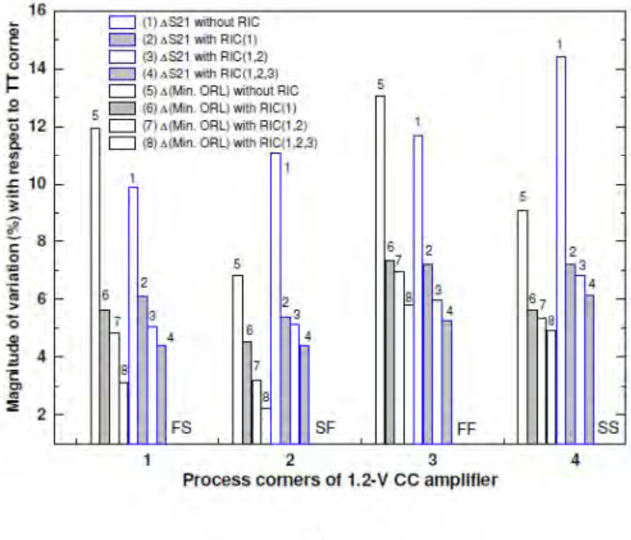
In the next section, results related to improvement in the reliability of the architectures against process, supply, and ambient variation are presented.

2.2.5 Results of CMOS Reliability

The 0.7-1.2 V amplifier architectures and reliability improving circuits (RIC) are designed with a 90-nm technology which is a CMOS process with supported minimum gate length of 0.08-0.1 m.

2.5 Improvement against Process Variation

The performance reliability of a CMOS amplifier is said to be improved as fluctuation of its RF parameters (gain, noise-figure, return-loss) is decreased against variable process factors. Fig. 3.3(a) highlights this point by illustrating the RIC's effect on percentage magnitude of variation in forward gain (S_{21}) and output reflection-loss (ORL). When data are obtained for the 1.2-V CC topology for various process corners, it shows the RIC being able to reduce FOM variation resulting from movement between process points. As the setup moves from TT to FF point, variation in peak gain is truncated from 11.71% to 7.21% (a reduction of 39%) after the addition of RIC(1). With the inclusion of other bias sections, gain disparity is decimated even further from 7.21% to 5.26% (a reduction of 27%). In comparison, shift in minimum ORL drops from 13.07% to 7.34% with the addition of RIC(1) and from 7.3% to 5.8% after appending RIC(2,3) to the circuit. In a similar manner, improvement in stability is observed in varying degrees as the circuit moves through other process corners. Change in noise



(a)

(b)

Fig. 3.3: Effect of the RIC on the 1.2-V CC amplifier's a) S_{21} and ORL, b) NF and NF_{min}.

parameters (NF and NF_{min}) is also stabilized by significant margins, as shown for the amplifier in Fig. 3.3(b). When the circuit shifts to SF and SS points

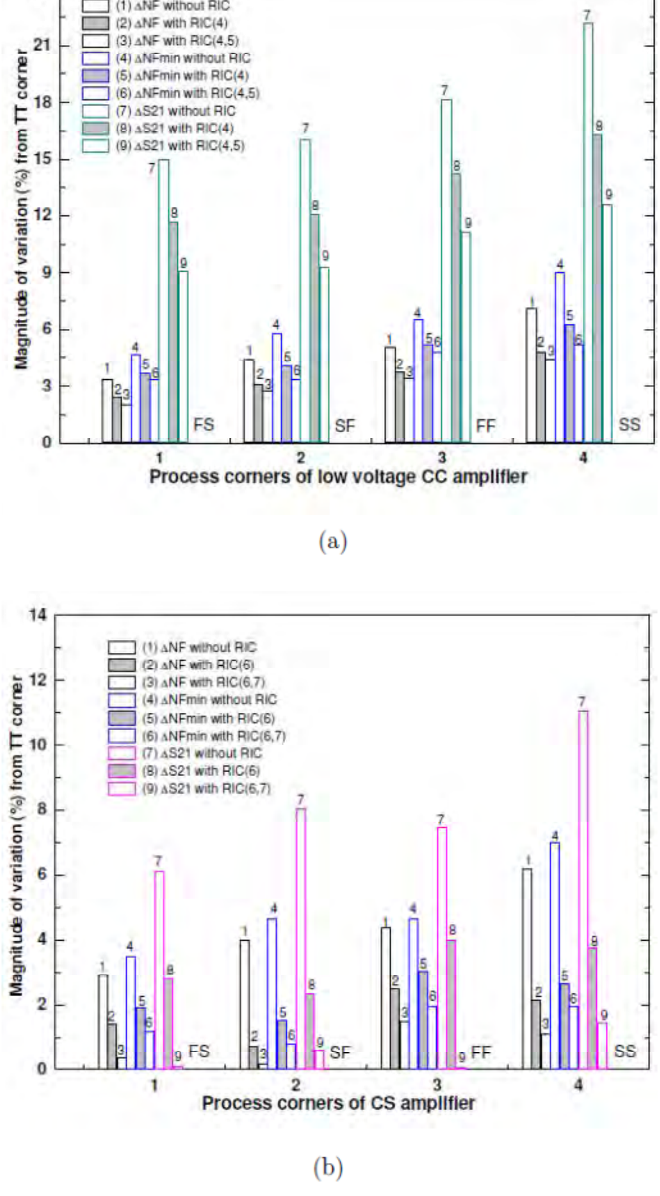


Fig. 3.4: Effect of the RIC on a) NF, NF_{min}, and S_{21} for the low-voltage (0.7-V) CC amplifier, b) NF, NF_{min}, and S_{21} for the 1.2-V CS topology.

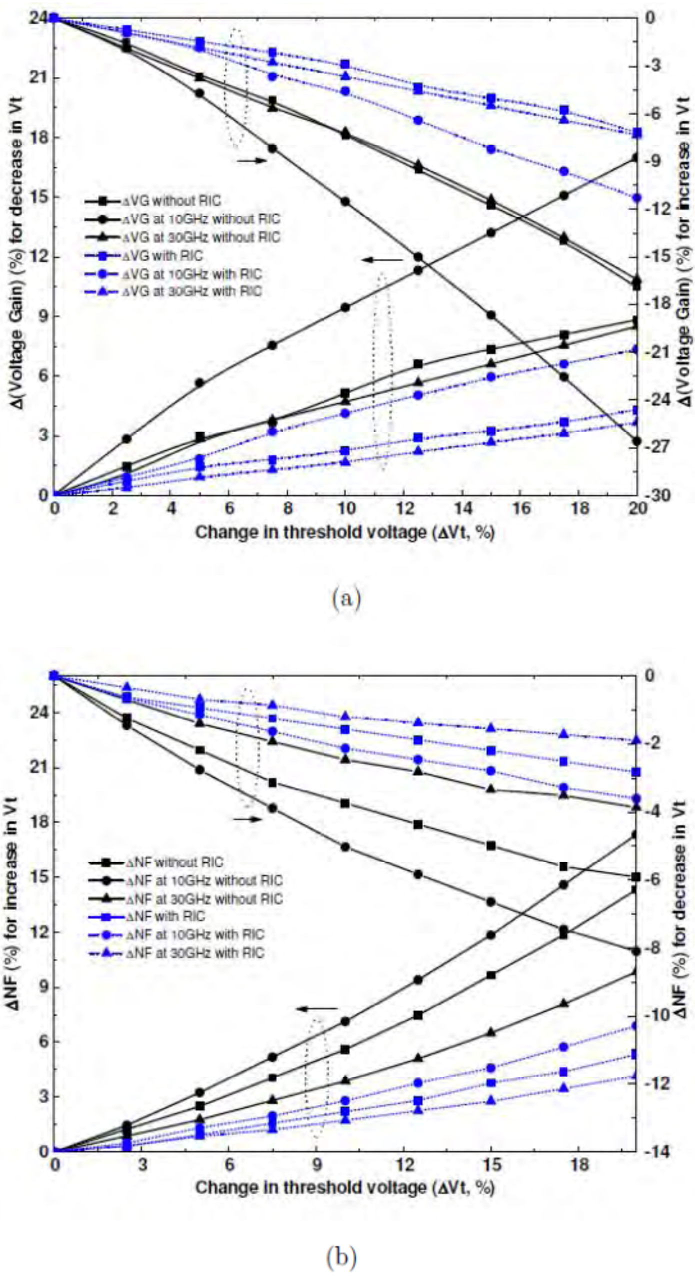


Fig. 3.5: Improvement against threshold variation in CMOS amplifier a) voltage gain and b) noise-figure.

from typical settings, percentage increase in NF (with respect to base values) is 7.48% and 10.28% for the uncompensated amplifier which plummets to 3.45% and 5.02% for the front-end after the RIC's integration (reductions of 54% and 51%).

The effect of the stability boosting network on the low-voltage CC LNA and the low-NF CS amplifier are demonstrated with the help of Fig. 3.4(a) and Fig. 3.4(b). As the supply voltage gets smaller for a silicon circuit, gain becomes more prone to violating design limits due to technology and system variables. This is manifested with the unstabilized low-voltage (0.7-V) CC amplifier suffering from larger changes (14.9-22.1%) in peak gain (as the process shifts between points) whereas the corresponding figure was <14% for the uncompensated 1.2-V CC amplifier. Even with this constraint, the technique manages to improve constancy of S_{21}, NF, and NF_{min}, as manifested in Fig. 3.4(a). Moreover, the mechanism achieves better regulation for the 1.2-V CS amplifier as compared to other topologies. As the situation is presented in Fig. 3.4(b), noise and gain reliability is made better through cutbacks of 2.3-9.6% in variability (reductions of 58-98%).

3.2 Effect on Threshold Modification and Supply Stability

The RIC's effectiveness in maintaining consistency of CMOS performance is further evaluated with Fig. 3.5(a) and Fig. 3.5(b) which document amplifier parameters against threshold variation. Device threshold may be subjected to modifications as chips get older and from electrical stress related degradations. It may also be influenced by unreliability events related with process limitations. Fig. 3.5(a) shows how voltage gain (VG) of the 1.2-V CC amplifier reacts when device threshold is modified by a margin of up to 20%. The results are evaluated over a

wide range including the amplifier's center point in K-band, and they present degree of variation and margin of improvement at different frequencies. Ultimately, the regulatory scheme enhances gain stability by margins of up to 15.3% over the entire range. Increase in noise-figure is also well compensated, as demonstrated in Fig. 3.5(b), where the RIC's effect becomes more apparent as percentage change in device threshold increases.

One of the design concerns which may affect an amplifier's stability is fluctuations in its supply voltage. Because, if the supply rails are not well regulated, they may have ripples around the base voltage level. Fig. 3.6(a) and Fig. 3.6(b) illustrate the resulting situation for the 1.2-V CC amplifier in terms of change in forward gain (S_{21}), NF, NF_{min}, and tree current (I_{rail1}). According to the readings, for the same degree of uncompensated supply instability, NF varies by a greater margin when V_{d1} is lowered as opposed to the situation when V_{d1} is increased. However, NF becomes balanced in this respect after the addition of the regulating network. The same improvement in circuit constancy is also observed in Fig. 3.6(b) through the clustering of NF_{min} curves.

The effect of thermal pro le on noise- and gain figures is the subject of Fig. 3.7 which shows absolute variation of RF parameters in dB (rise of NF and drop of gain) for the 1.2-V CC amplifier. The bias network does not seem to affect the rate of change of gain (apart from an increase of 0.3 dB in peak gain) but increase in noise-figure slows down after its addition as thermal condition is elevated beyond typical ambient readings.

2 Frequency Domain Analyses

In the next step, the architectures are investigated in the frequency domain with process corner and monte carlo analyses. Fig. 3.8(a) shows the case for S_{21} and ORL of the 1.2-V CC amplifier and Fig. 3.8(b) presents the situation with

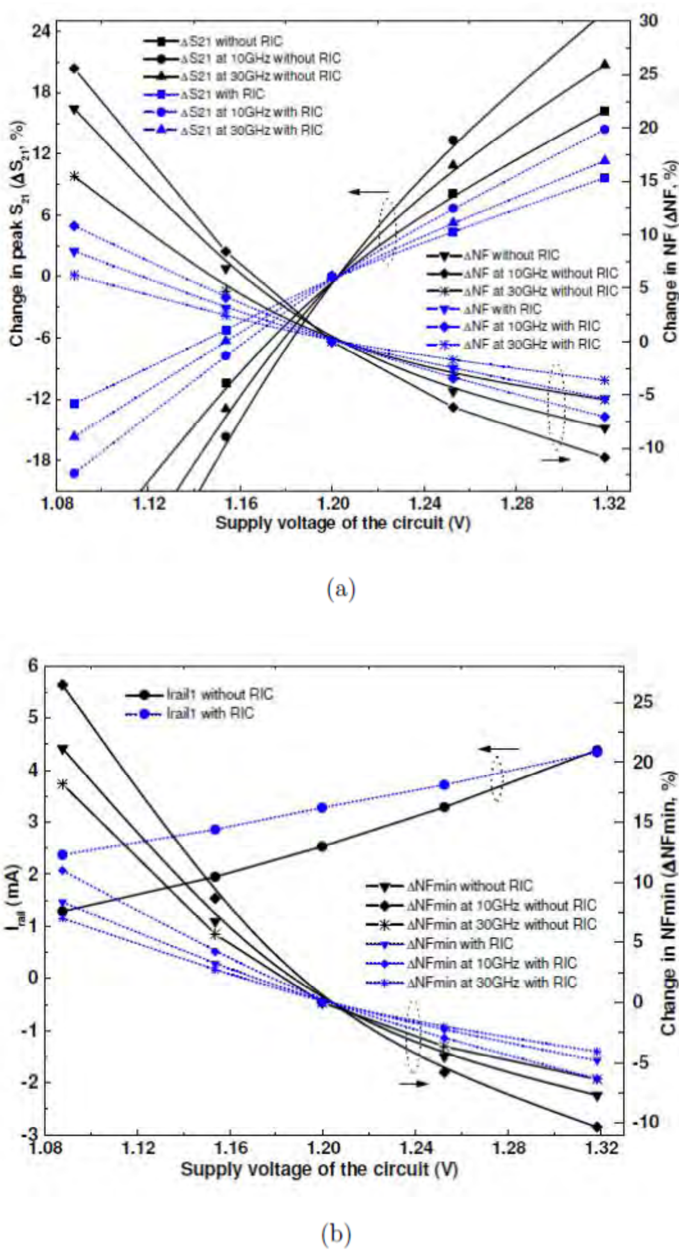


Fig. 3.6: Reduction of susceptibility to supply variation in terms of a) S_{21}, NF and b) I_{rail}, NF_{min}.

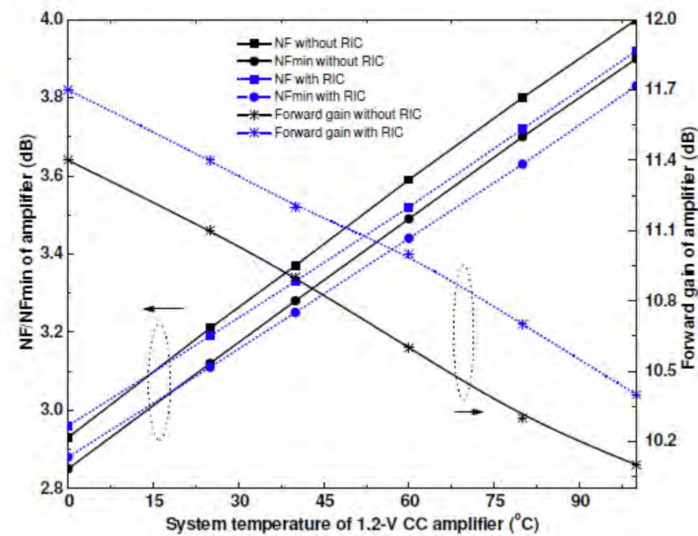


Fig. 3.7: Influence of thermal pro le on noise and gain.

noise-figures of the CS amplifier. Both of them indicate a betterment of CMOS reliability without degradation of performance. In case of the CC amplifier, magnitude of peak gain spread is reduced from 10.0-14.4% to 4.4-6.1% (a decrease of up to 61%), and reduction of NF spread for the CS amplifier is from 2.9-6.2% to 0.4-1.5% (a drop of 46-74%).

Monte carlo (MC) analysis is useful to estimate the effect of random mismatch of parameters in a nanoscale circuit which may arise as a result of technology variation. Fig. 3.9(a) shows the spread in noise and gain curves resulting from Monte Carlo simulation. They are obtained from the 1.2-V CC architecture when it is powered from an external supply without the RIC. The figure shows peak gain and NF_{min} spreads of -16.5 12.6% and -11.1 10.5%, respectively. After stability improving circuits are incorporated, the corresponding set of curves are illustrated in Fig. 3.9(b). The analysis is performed assuming that statistical probability is not dominated by the least performing result arising from process related mismatches. Accordingly, extent of forward gain and noise spreads comes

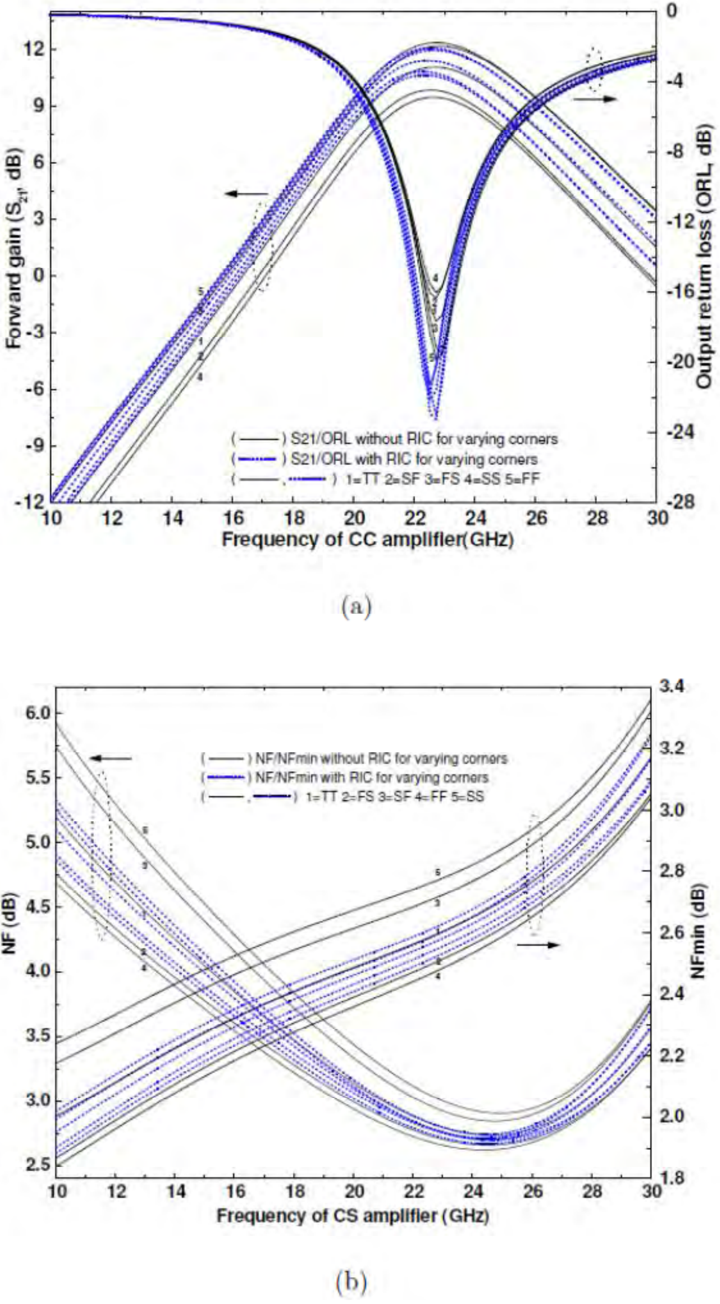


Fig. 3.8: a) Gain, reflection-loss and b) noise-figures for varying process points.

down to -4.4 6.1% and -6.4 6.7% after the RIC's inclusion. These outcomes point to a significant betterment in reliability against technology variation.

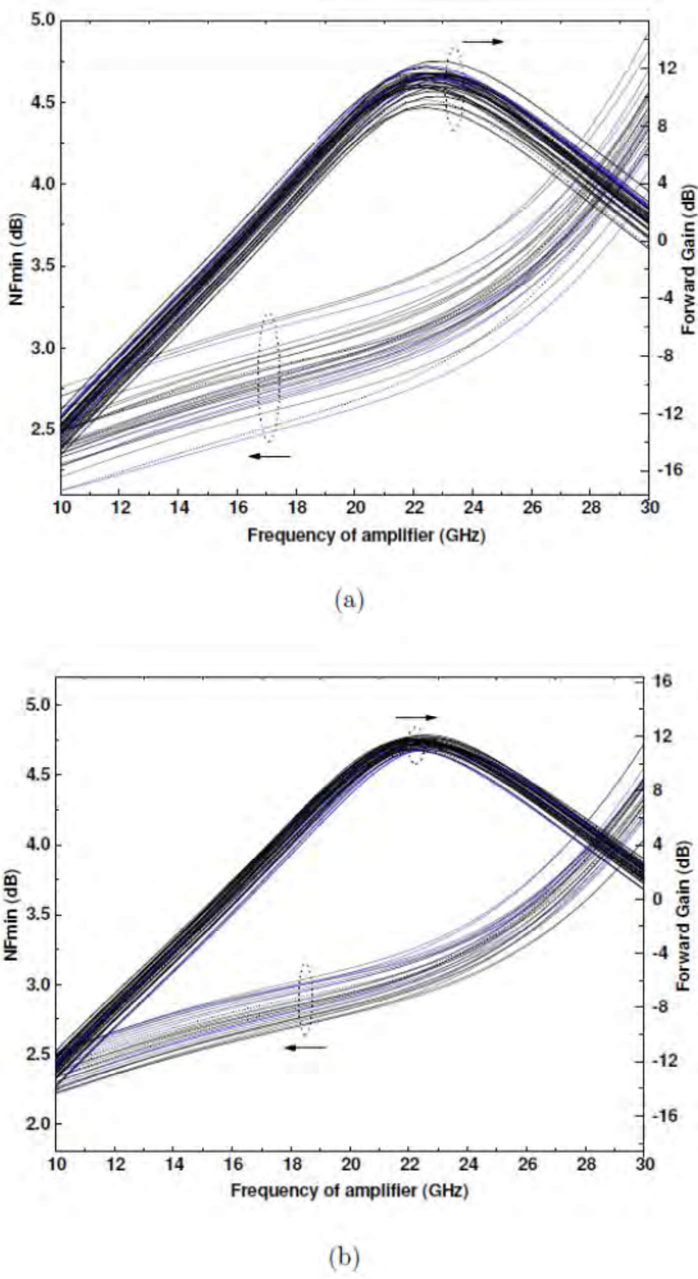


Fig. 3.9: Results of mismatch analysis in terms of noise and gain a) without and b) with the RIC.

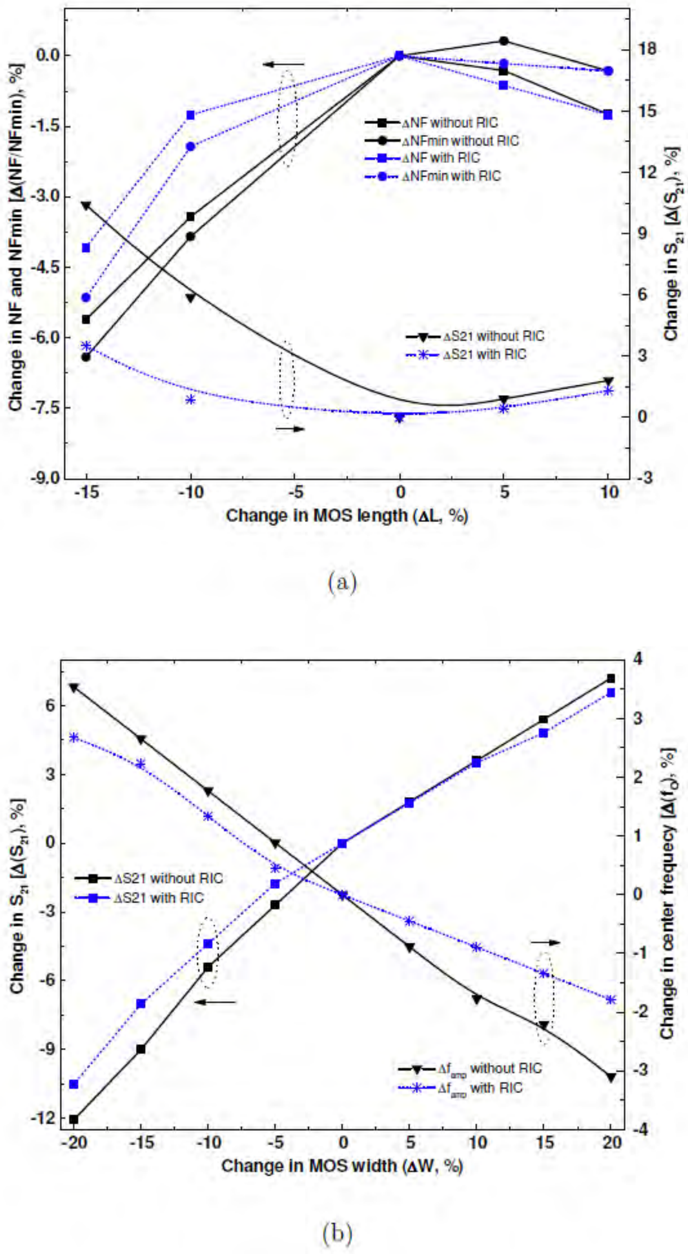


Fig. 3.10: Effect of variation in device a) feature length and b) feature width on the 1.2-V CC amplifier.

Table 3.1: Performance of 1.2-V CC amplifier against feature variability.

Param. spread (%)	ΔNF(%) w.o. RIC for W(C_{in1})*	ΔNF(%) with RIC for W(C_{in1})*	ΔNF(%) w.o. RIC for W(C_{out1})*	ΔNF(%) with RIC for W(C_{out1})*
0	9.97	5.54	9.97	5.33
10	10.23	5.33	10.09	5.58
20	11.84	7.84	10.28	5.71

* W(C_x) stands for width of silicon capacitors

3.4.3 Resistance against Feature Mismatches

The 1.2-V CC amplifier is also analyzed for variability of dimensions and its effect on design parameters. It is relevant because feature size of active elements may deviate from specified design values due to imperfections of fabrication steps. To understand this point, the effect of variable device feature length on noise and peak gain is addressed in Fig. 3.10(a). It shows the scheme to be more effective when dimensional variation results in decrease of feature size. Fig. 3.10(b) shows how change in a core device width may affect the amplifier's center frequency and corresponding power gain. In this case, the RIC's influence is less prominent as compared to other instances of reduction in process induced deviation. Next, the upshot of variation in the distribution of inductor outer width ($X_{Ls/r/g}$) and capacitor width ($W_{Cin/out}$) is modeled through monte carlo analysis and corresponding results for NF and S_{21} are summarized in Tables 3.1 and 3.2. In Table 3.1 and the following tables, percentage of deviation is calculated with respect to parameters obtained without process variation. The tables support the notion that the reliability enhancing network strengthens resistance of CMOS amplifiers against component mismatch

Table 3.2: Performance of 1.2-V CC amplifier against feature variability (contd.).

Param. spread (%)	ΔS_{21}(%) w.o. RIC for $X(L_{s1})^*$	ΔS_{21}(%) with RIC for $X(L_{s1})^*$	ΔS_{21}(%) w.o. RIC for $X(L_{r1})^*$	ΔS_{21}(%) with RIC for $X(L_{r1})^*$
0	12.61	9.65	12.61	9.65
5	11.71	7.89	12.52	9.65
10	10.81	7.02	12.43	8.77

* $X(L_x)$ stands for overall outer dimension of inductors

3.4.4 Results for Low-voltage CC and CS Amplifiers

In the three previous subsections, results showing reduction of process related performance discrepancies have been presented mostly for the 1.2-V CC amplifier. These analyses are also applied to the low-voltage CC amplifier and the 1.2-V CS architecture. In these cases, the RIC's contribution is demonstrated with selected results documented through Table 3.3 - Table 3.7. According to them, change of gain due to threshold deviation can be reduced by 0.81-6.82% and 0.88-16.21% for 0.7-V CC and 1.2-V CS amplifiers, respectively. The 0.7-V CC topology proves to be more susceptible to uncertainty of supply voltage and the 1.2-V CS circuit achieves better regulation against varying corner points. The results underline that, despite being powered by a scaled main supply, the 0.7-V CC amplifier is able to stabilitate its microwave figures with the help of the RIC. The 1.2-V CS structure also achieves significant furtherance in reliability and its margin of improvement can be higher than the other two architectures. So, it is evident that the scheme functions well with and is able to improve CMOS consistency of diverse front-end topologies.

Table 3.3: Reliability of 0.7-V CC and 1.2-V CS topologies against threshold deviation.

Architecture	0.7-V CC		0.7-V CC		1.2-V CS		1.2-V CS	
Threshold Deviation (%)	$\|\Delta NF\|$(%) w.o. RIC	$\|\Delta NF\|$(%) with RIC	$\|\Delta VG\|$(%) w.o. RIC	$\|\Delta VG\|$(%) with RIC	$\|\Delta NF\|$(%) w.o. RIC	$\|\Delta NF\|$(%) with RIC	$\|\Delta VG\|$(%) w.o. RIC	$\|\Delta VG\|$(%) with RIC
2.5	1.01	0.68	2.55	1.74	0.73	0.18	1.59	0.71
5.0	2.36	1.37	5.09	3.49	1.82	0.37	3.97	0.99
7.5	3.38	2.05	7.77	5.35	2.92	0.55	5.56	1.28
10.0	4.73	2.73	10.59	7.22	4.01	0.74	7.94	1.63
12.5	6.42	3.75	13.40	9.34	5.11	0.92	10.32	1.99
15.0	8.11	4.78	16.35	11.33	6.57	1.11	13.49	2.27
17.5	10.14	5.80	19.30	13.45	8.03	1.29	15.87	2.55
20.0	11.82	6.83	22.39	15.57	9.49	1.66	19.05	2.84

Table 3.4: Reliability of 0.7-V CC and 1.2-V CS amplifiers against variable supply.

Archi- tecture	0.7-V CC		0.7-V CC		1.2-V CS		1.2-V CS	
Change of supply voltage (%)	$\lvert\Delta \mathrm{NF}\rvert$(%) w.o. RIC	$\lvert\Delta \mathrm{NF}\rvert$(%) with RIC	$\lvert\Delta S_{21}\rvert$(%) w.o. RIC	$\lvert\Delta S_{21}\rvert$(%) with RIC	$\lvert\Delta \mathrm{NF}\rvert$(%) w.o. RIC	$\lvert\Delta \mathrm{NF}\rvert$(%) with RIC	$\lvert\Delta S_{21}\rvert$(%) w.o. RIC	$\lvert\Delta S_{21}\rvert$(%) with RIC
9.9	7.09	4.44	28.17	18.75	5.84	3.69	11.48	3.94
4.4	4.05	2.39	14.42	9.56	3.28	1.85	6.35	3.21
-3.8	6.08	4.10	18.96	12.75	4.38	2.21	8.14	4.04
-9.3	19.59	13.31	51.00	35.42	13.50	5.54	12.71	11.09

Table 3.5: Performance of 0.7-V CC and 1.2-V CS amplifiers with regard to process variation.

Archi-tecture	0.7-V CC		0.7-V CC		1.2-V CS		1.2-V CS	
Process corner	$\|\Delta S_{21}\|(\%)$ w.o. RIC	$\|\Delta S_{21}\|(\%)$ with RIC	$\|\Delta \mathrm{NF}\|(\%)$ w.o. RIC	$\|\Delta \mathrm{NF}\|(\%)$ with RIC	$\|\Delta S_{21}\|(\%)$ w.o. RIC	$\|\Delta S_{21}\|(\%)$ with RIC	$\|\Delta \mathrm{NF}\|(\%)$ w.o. RIC	$\|\Delta \mathrm{NF}\|(\%)$ with RIC
FS	14.95	9.07	3.38	2.05	6.13	0.10	2.92	0.37
SF	16.02	9.31	4.39	2.73	8.03	0.62	4.01	0.18
FF	18.16	11.15	5.07	3.41	7.47	0.05	4.38	1.48
SS	22.16	12.62	7.09	4.44	11.04	1.45	6.20	1.11

* ΔS_{21} and ΔNF are calculated with respect to TT corner

Table 3.6: Performance of 0.7-V CC and 1.2-V CS amplifiers against feature variability.

Archi-tecture	0.7-V CC		0.7-V CC		1.2-V CS	
Param. spread (%)	ΔNF(%) w.o. RIC for W(C_{in2})	ΔNF(%) with RIC for W(C_{in2})	ΔNF(%) w.o. RIC for W(C_{out3})	ΔNF(%) with RIC for W(C_{out3})	ΔNF(%) w.o. RIC for W(C_{out4})	ΔNF(%) with RIC for W(C_{out4})
0	8.45	5.80	8.45	5.63	9.12	5.17
10	9.12	6.14	8.78	5.80	9.12	4.80
20	9.46	8.53	8.45	5.94	9.20	5.17

* W(C_x) stands for width of capacitors

Table 3.7: Performance of 0.7-V CC and 1.2-V CS amplifiers against feature variability (contd.).

Archi- tecture	0.7-V CC		0.7-V CC		1.2-V CS		1.2-V CS	
Param. spread (%)	ΔS_{21}(%) w.o. RIC for X(L_{s2})	ΔS_{21}(%) with RIC for X(L_{s2})	ΔS_{21}(%) w.o. RIC for X(L_{r2})	ΔS_{21}(%) with RIC for X(L_{r2})	ΔS_{21}(%) w.o. RIC for X(L_{s3})	ΔS_{21}(%) with RIC for X(L_{s3})	ΔS_{21}(%) w.o. RIC for X(L_{r3})	ΔS_{21}(%) with RIC for X(L_{r3})
0	22.56	10.54	22.43	10.66	10.48	3.63	10.59	3.63
5	21.23	8.82	23.23	9.44	11.48	4.66	11.48	4.66
10	19.76	10.91	22.96	9.68	12.60	6.74	12.60	4.87

* X(L_x) stands for overall outer dimension of inductors

Table 3.8: Comparison of percentage improvement in variability (PIV) achieved by reliability compensation techniques.

Ref.	Topology	Supply	PIV (Type of process variation, Parameter for amplifier)
This work	LNA	1.2 V	1.55~8.78 (VTV[1], NF[7]) 2.75~12.31 (VTV[1], Gain) 1.59~8.31 (VTV[1], NF_m[8]) 3.72~5.26 (VPC[2], NF[7]) 6.45~8.27 (VPC[2], Gain) 3.7~16.7 (VS[3], Gain)
[94]	PA	2.5 V	0.23~0.82 (VTV[4], P_s[9]) 1.68~2.42 (VPC[2], P_s[9]) 0.28~0.79 (VS[3], P_s[9])
[97]	LNA	1.0 V	1.3~5.7 (VTV[1], NF[7]) 0.77~2.5 (VTV[1], Gain) 0.8~4.7 (VTV[1], NF_m[8])
[98]	LNA	-	>8.4[5] (VPC[2], NF[7]) >1.4[5] (VPC[2], Gain)
[99]	LNA	1.8 V	0.22[5,6](VPC[2], NF[7]) 3[6](VPC[2], Gain)
[100]	LNA	1.2 V	0.3~4.1 (VS[3], Gain)

[1] Against variation in device threshold (5-20%)
[2] Against variation in process corners (ff, tt, ss)
[3] Against variation in supply voltage (4-10%)
[4] Against variation in device threshold (4-8%)
[5] Indicating increase in variability
[6] Expressed in dB
[7] Noise-figure
[8] Minimum noise-figure
[9] Saturation power

1.7 Comparison with Other Techniques

Table 3.8 compares the reliability improving circuit (RIC) for the 1.2-V CC amplifier with literature related to process compensation [94], [97{100]. Percentage improvement in variability (PIV) is tabulated for the examples which gives an estimation about the effectiveness of compensation techniques. The selected mechanisms are compatible with various CMOS transceiver circuits and help to maintain consistency of performance against variation of device threshold (VTV), supply rail (VS), and process corners (VPC). The topologies include low-noise

amplifier (LNA) and power amplifier (PA) architectures and stability of RF parameters like noise-figure (NF), peak forward gain, minimum NF (NF_m), and saturation output power (P_s) are considered. In terms of noise behavior, the proposed circuit reduces noise variability by up to 8.8% against threshold variation and 5.3% against variable corners. Significant reduction in changeability is also realized for NF_m (for threshold variation) and its improvement (up to 8.3%) is comparable with that of NF. In contrast, the scheme of [97] truncates NF and NF_m variabilities by up to 5.7% and 4.7% for deviation of device threshold in an amplifier. For the RIC, maximum improvement in variability is obtained for peak gain (up to 16.7%) against a varying supply and reduction in gain deviation against VPC and VTV is up to 8.3% and 12.3%, respectively. So, the RIC will increase the constancy of a front-end's gain pro les. On the other hand, the mechanisms of [97] and [100] are able to improve gain fluctuation by <2.5% and <4.1% against alteration of device threshold and supply voltage. Compensation circuits for LNAs are realized in [98{100] with the help of features like switchable capacitance, reconfigurability, and feedback schemes. The techniques of [94] and [99] achieve best results for varying process corners and the mechanism of [100] works against ripples in supply rail. The scheme of [97] has a more prominent effect on NF variability and its gain regulation is less effective. The circuits under discussion use 1.0-2.5 V supply rails and similar types of process variation are considered for them. Additionally, the references are selected to focus on front-end circuit architectures (CMOS amplifiers).

2.4 Conclusions

A reliability improving technique with low-power requirement is presented in this chapter which can notably improve the consistency of CMOS amplifier perfor-

mance versus process and system variation. It provides resistance against deviation of microwave parameters by regulating the design's current through a shared network which is powered from the amplifier's main supply rail. Variability of process is covered by including threshold deviation, dimensional effect, supply regulation, and corner analysis in the study, where simulation results show the technique stabilizing gain/noise parameters (NF, ORL, NF_{min}, VG, S_{21}) against mismatches. The technique is compatible with common-source, typical-voltage cascode, and low-voltage cascode front-ends (on a 90-nm technology platform) and, generally, the CS architecture manages the most improved reliability figures.

Chapter 4

A Stabilization Technique for Single-ended and Differential Harmonic Oscillators

1.8 Introduction

With scaling down of feature size in complementary-metal-oxide-semiconductor (CMOS) technology, statistical process variability is starting to exert a greater influence on radio-frequency circuit performance [108, 109]. Therefore, understanding the relationship between circuit reliability and process variation becomes pivotal during the design phase of a high frequency architecture [110-112]. In this regard, variables involved with a silicon process are typically attributed to physical events, imperfection of fabrication steps, and stability of ambient conditions and power rail. In addition, variability of technology may result from phenomena like line width roughness, dielectric traps, channel carriers in a high field, bias temperature instability, dopant fluctuation, and oxide pro le variation [113-120]. Under these circumstances, a stabilization technique becomes desirable for a transceiver circuit to improve fidelity of its microwave parameters without degradation of performance. Moreover, when incorporated, these techniques may have the potential to ease the restrictions imposed by electrical stress and feature variability and reduce the influence of long term modification of tran-

sistor parameters [43,121,122]. Keeping these issues in mind, this chapter focuses on the reliability of oscillator blocks in nanoscale transceiver circuits whereas the last chapter addressed the stability of front-end amplifiers.

Recent literature has discussed about the effect of process variation on CMOS devices and presented examples of stability controlling mechanisms for analog/mixed-signal/digital topologies [123{130]. For example, intrinsic parameter modification of bulk transistors due to discrete dopants and disparity of line-edge/oxide-pro le is studied in [123]. Time dependent variability is discussed in [124] with attention to runtime monitoring of embedded systems. How optimization of energy delay product can determine setup time of ip- ops and make them aware of bias temperature instability is presented in [125]. A phase-locked loop (PLL) based sensor is proposed in [126] to detect process, voltage, and temperature (PVT) deviation while relaxing temporal reliability constraints. Dynamic frequency and voltage scaling schemes are studied in [127] which are based on runtime adaptability to PVT factors and fast transient tolerance. Mixed mode simulation is employed by [128] to investigate the effect of adaptive body voltage on a Colpitts oscillator. An automatic tuning scheme capable of making LC bandpass filters impervious to input amplitude mismatches is demonstrated in [129]. The use of a leakage reduction solution (power gating) in [130] reduces the effect of bias instability and synthesizes low-leakage circuits. These examples underline the importance of stabilizing techniques for architectures used in on-chip communication circuitry.

This chapter presents a gate stabilizing mechanism to reduce the variability of RF parameters of inductor-capacitor (LC) tuned harmonic oscillators. The technique is compatible with single-ended and differential modified Hartley oscillator architectures (LCHO and DLCHO) which makes it suitable for quadrature channel receivers. The scheme uses regulation of bias currents to reduce sensitivity of key oscillator parameters to process induced change of device threshold and other

features. Analytical discussion is provided to explain the stabilization of a signal generator's oscillation magnitude, phase noise, and period jitter. Environmental and supply variables like stability of power rail and thermal pro le are covered and the results are verified with CMOS device parameters. The technique can compensate against a wide range of system imperfections and improve variability of noise, jitter, and oscillation by up to 34 dBc/Hz, 76 fs, and 960 mV, respectively. The chapter is organized in the following way. Section 4.2 provides discussion on modeling of oscillator stability. The stabilizing gate circuit (SGC) and its regulation mechanism are explained for two LC tuned harmonic oscillators. Results showing improvement in oscillator variability are presented in Section 4.3 and compared with process stabilizing schemes. Finally, the conclusions of the study are summarized in Section 4.4.

2.5 Stability Modeling for Oscillators

An oscillator is one of the basic building blocks required in microwave transceiver architectures and its reliability is addressed in this study. Fig. 4.1 shows a single-ended LC tuned modified Hartley oscillator (LCHO) with power rail and

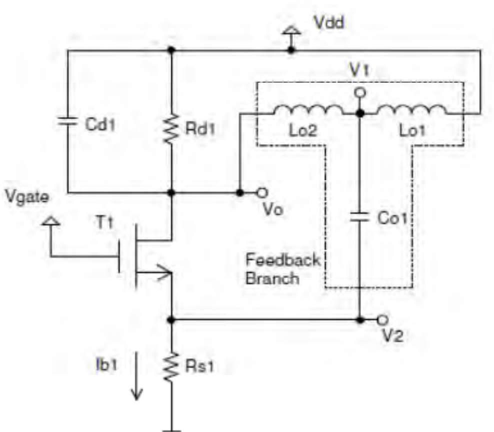


Fig. 4.1: A single-ended LC tuned harmonic oscillator.

gate bias supplies. The circuit is built as a single fet oscillator where the output is fed back to the source to satisfy the phase shift criterion of oscillation. It is designed with the transistor T_1 being powered from a 2.5-V power rail (V_{dd}). An RC tank is realized with R_{d1} and C_{d1}, V_{gate} serves as a separate gate supply, and the core current (I_{b1}) is tuned with the smaller resistor R_{s1}. A pair of inductors (L_{o1} and L_{o2}) and a feedback element (C_{o1}) are employed to realize the feedback network where one end is connected to the input device's drain terminal (V_0) and the other end (V_2) is connected to the common-gate transistor source. Frequency selection of the harmonic oscillator is controlled by the tank capacitor (C_{d1}) and the reactive elements in the feedback network (L_{o1}, L_{o2}, and C_{o1}). The resistive element R_{d1} does not control the frequency, rather it influences the circuit's output signal amplitude. Ideally, the nodal signals of the topology (V_o, V_1, V_2) can be expressed as

$$V_o = V_{dd} + V_{os}[cos(2\pi f_{os}t)] \tag{4.1}$$

$$V_1 = V_{dd} + a[cos(2\pi f_{os}t)] \tag{4.2}$$

$$V_2 = a[cos(2\pi f_{os}t)] + b \tag{4.3}$$

where V_{os} is the oscillation amplitude, f_{os} is the oscillation frequency, and a, b are circuit dependent constants. The fundamental oscillatory component of the single-ended LC tuned oscillator is primarily dependent on the feedback network's passive elements and can be approximated by [131]

$$f_{os} = \frac{1}{2\pi}\frac{1}{\sqrt{(L_{o1} + L_{o2})C_{d1} + C_x L_{o2}}} \tag{4.4}$$

where C_x is determined by the feedback capacitor (C_{o1}) and parasitic capacitance (C_{par}) associated with the principal transistor:

$$C_x = \frac{C_{par}C_{o1}}{C_{par} + C_{o1}}. \tag{4.5}$$

As physical phenomena related with process deviation can a ect the total para-sitic contribution of an active device, variability of the oscillator output is often dependent on them. In addition, oscillation amplitude of the LCHO is directly controlled by the bias current I_{b1} and the device's region of operation. As a result, stabilization of bias current improve the constancy of oscillation magnitude and the LC tuned topology generally maintains the following relation [132]

$$V_{os} \propto \sqrt{2I_{b1}}. \tag{4.6}$$

Among the noise components of an oscillator, phase noise is generated from spurious spectral components around the fundamental frequency. Ideally, tones produced by a harmonic oscillator are supposed to be localized but the existence of phase noise spreads signal power to surrounding frequencies. It plays a role behind increase in rate of error in a communication system and is also involved with interference between channels. For an LC tank oscillator which uses a feedback circuit, phase noise (N_p, in dBc/Hz) can be obtained from power spectrum density around the rst harmonic and is approximated by [133]

$$N_p(\Delta f) = 10\log[\frac{Lf_{os}^2}{2\{\pi^2 L^2 f_{os}^4 + (\Delta f)^2\}}] \tag{4.7}$$

where L is the Lorentz constant and f is the o set frequency. For suitable offset frequencies and assuming white noise sources, the function can be further simplified to

$$N_p(\Delta f) \approx 10\log[\frac{L{f_{os}}^2}{2(\Delta f)^2}]. \tag{4.8}$$

The following condition needs to be satisfied for the previous expression to be valid:

$$L\pi {f_{os}}^2 \ll \Delta f \ll f_{os}. \tag{4.9}$$

If mean square values of shot and flicker noise currents of the device are represented by I_s^2 and I_f^2, their relationship with the bias point [134] can be formu-

lated as

$$\bar{I_s}^2 = f(qI_{b1}) \tag{4.10}$$

$$\bar{I_f}^2 = f(kI_{b1}{}^{\alpha}) \tag{4.11}$$

where k and are device constants. As a result, when all noise sources are considered, oscillator noise becomes dependent on the architecture's power rail and bias rating. Consequently, regulation of bias current achieves the ability to control the architecture's noise performance.

Period jitter (J_p) is another important figure of merit for an oscillator circuit as it is indicative of stability of a periodic signal in frequency domain and is also a measure of uncertainty in time domain for the short term. This parameter, together with phase noise, determines the extent of perfection for synchronization mechanisms. Assuming that phase noise spectrum is defined for a harmonic oscillator, an expression of period jitter can be obtained as a function of o set frequency [135]:

$$J_p(\Delta f) \approx \sqrt{\frac{2(\Delta f)^2 N_p{}'}{f_{os}{}^3}}. \tag{4.12}$$

Here $N_p{}^0$ is a measure of phase noise density at o set frequencies placed well below the point of oscillation.

2.2.6 Stabilizing Gate Circuit for Process Variation

Fig. 4.2 presents two (single-ended and differential) LC tuned oscillator architectures (LCHO and DLCHO) with integrated stabilizing gate circuits (SGC). In the single-ended topology, the SGC replaces the gate supply with a gate-drain shorted device which decides the bias point with its feature width. The selection of suitable RC tank elements (R_{d1} and C_{d1}) and bias current ensures that inclusion of the SGC does not significantly alter the oscillator parameters. Fig. 4.2(b) realizes a differential configuration of the stabilized LCHO where coupling of two

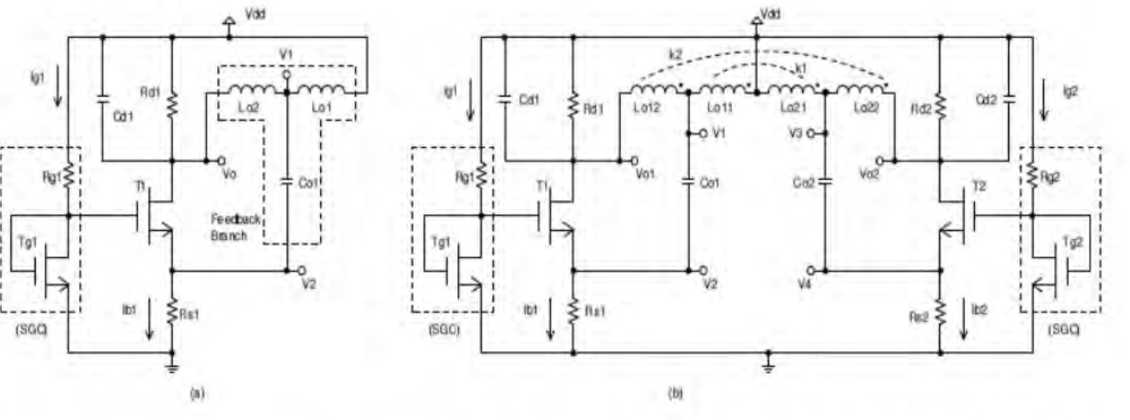


Fig. 4.2: a) Single-ended (LCHO) and b) differential (DLCHO) harmonic oscillator architectures with stabilizing gate circuits.

pairs of inductors (Lo11, Lo21 and Lo12, Lo22) ensures the architecture's differential operation. The output signal is collected across nodes Vo1, Vo2 and the topology has good cyclostationary noise features. The circuit's differential nature makes it compatible with front-ends requiring less second order distortion and rejection of common-mode noise.

Among RF circuit elements, transistors are often more susceptible to the multitude of varieties of process variation. For example, short channel limitation (SCL) and reverse SCL can push a device's threshold (V_t) away from the process determined level. In addition, feature size of a transistor may differ from the design value after the numerous steps of fabrication flow. Moreover, generation of hot carriers from impact ionization can create trapped charges in and interface states under a device's oxide layer. These phenomena may alter drain current and in uence phase noise in an oscillator circuit. Other factors which can modify device threshold include variability of oxide thickness, silicon dopant perturbation, and temporal effects (device aging). The SGC provides the oscillator a way to regulate core bias current against these variables. If the driving transistor has a feature size which is higher than the design value, it may raise the current I_{b1} leading to unexpected changes in the RF performance. However, the SGC current

I_{g1} is raised at the same time, assuming similar patterning for local devices, which brings down the overdrive voltage available at driving gate and leads to stabilization of the bias current. In a similar manner, if process disparity increases the turn-on voltage of T_1, it would curtail its effective overdrive voltage V_{od1}. But the corresponding drop in bias current is compensated as the drop across R_{g1}

(due to SGC current) is reduced simultaneously and the overdrive voltage is re-stored. In a similar manner, the compensation scheme can account for reduction in feature dimension and device threshold. If feature width of the oscillatory transistor is scaled, the I_{g1} current drops as well and gate-source voltage of T_1 is

compensated. Similarly, process induced decrease in device threshold alters the oscillator branch currents and stability of oscillator performance is maintained. The current equations of the compensated LCHO take the form of

$$I_{g1} = \frac{1}{2}\frac{\beta_{g_1} W_{g_1}}{L_{g_1}}(V_{dd} - R_{g1}I_{g1} - V_{tg_1})^2 \tag{4.13}$$

$$I_{b1} = \frac{1}{2}\frac{\beta_1 W_1}{L_1}(V_{dd} - R_{g1}I_{g1} - V_{s1} - V_{t1})^2 \tag{4.14}$$

where $_x$ is the input transconductance of transistors in the architecture. Here, improvement of bias current variability helps to stabilize the magnitude of oscillation as it follows from Eq. (4.6)

$$\Delta V_{os} = \frac{m\Delta I_{b1}}{\sqrt{2I_{b1}}} \tag{4.15}$$

where m is a constant of proportionality. Moreover, the relationships of Eq. (4.10) and Eq. (4.11) suggest that the stabilizing circuit would reduce process induced variability of phase noise and period jitter.

Additionally, the SGC is able to limit wandering of transistor gate signal due to ripples in the supply rail (V_{dd}). For the uncompensated LCHO, the V_{gate} signal is isolated from the power rail and cannot respond to supply induced alteration of bias current which is given by

$$\Delta I_{b1} = \frac{\beta_1 W_1 \Delta V_{dd}}{L_1}(V_{dd} - R_{g1}I_{g1} - V_{s1} - V_{t1}). \tag{4.16}$$

On the other hand, the stabilized oscillator shows more responsiveness to V_{dd} as the SGC is able to sense any modification of I_{b1} caused by the supply. Reduced variation of the driving gate signal in a compensated oscillator can be estimated from

$$\Delta V_{g1} = \Delta V_{dd}[1 - \frac{\beta_{g_1} W_{g_1} R_{g1}}{L_{g_1}}(V_{dd} - R_{g1}I_{g1} - V_{tg_1})]. \tag{4.17}$$

These stabilizing mechanisms work in a similar manner for the differential oscillator built with two tuned half circuits.

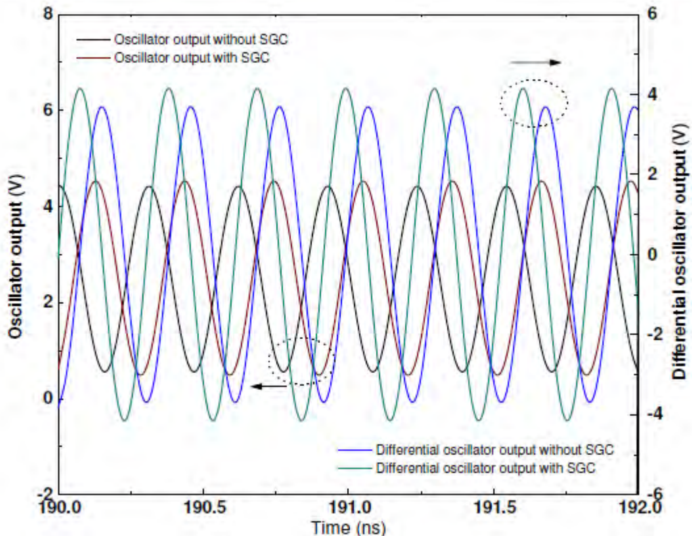


Fig. 4.3: Output response from uncompensated and stabilized harmonic oscillator circuits.

The simulated output signals from the LCHO and the DLCHO are presented in time domain in Fig. 4.3 where it is noticeable that the stabilizing gate circuit does not have a significant influence on oscillation frequency. Sinusoidal output from the uncompensated LCHO varies from 0.51-V to 4.49-V with f_{os}= 3.249 GHz and V_{os}=1.99-V. Stable oscillation is maintained after the addition of the SGC with f_{os}=3.256 GHz and V_{os}= 2.08-V. For the differential circuit (DLCHO), higher magnitude of oscillation is attained due to the two half circuits. Oscillation magnitude and frequency for the DLCHO without the SGC are 3.80-V and 3.274 GHz, respectively, and like its single-ended counterpart, the compensated differential circuit (f_{os}=3.278 GHz) demonstrates improved reliability of oscillator parameters.

In addition, the presented oscillator circuits achieve a reasonable range of phase noise (PN) with the uncompensated LCHO managing a PN of -111.5 dBc/Hz at an offset frequency of 0.1 MHz. After appending the stabilizing cir-

cuit, PN for the LCHO remains at -111.4 dBc/Hz for the same offset frequency. For an extended range of o set frequencies (f=1KHz 1MHz), phase noise for the oscillators remains lower than -59.5 dBc/Hz and -54.6 dBc/Hz with and with-out the SGC, respectively. In case of the differential circuit (DLCHO), PN for the mentioned range of o set frequencies is smaller than -58.8 dBc/Hz and -61.9 dBc/Hz before and after the addition of the stabilizing technique (-115.1 dBc/Hz and -114.6 dBc/Hz at f=0.1 MHz).

2.6 Results of Reliability

The proposed circuits are analyzed with 90-nm complementary metal oxide semiconductor (CMOS) device models using an RF simulator. The devices support a minimum gate length of 0.08-0.1 m and include features like shallow trench isolation stress model, gate tunneling current model, and gate induced drain leakage current model. The simulator determines the steady-state behavior of oscillator architectures with a variant of harmonic balance analysis (HBA). Rather than

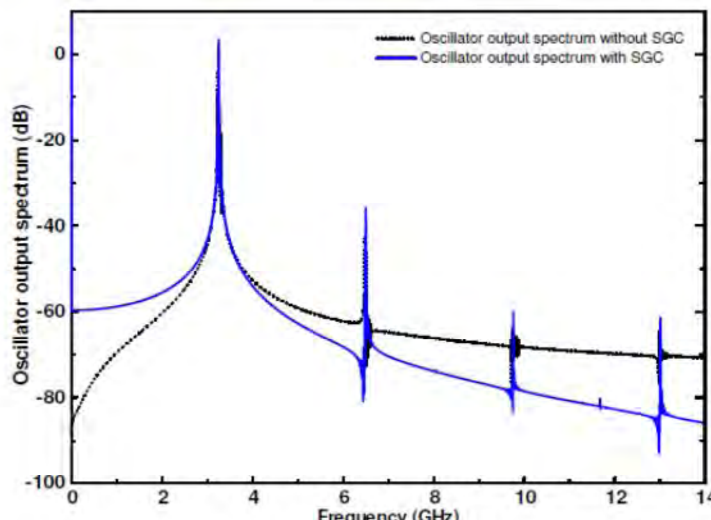


Fig. 4.4: Output spectrum characteristics of the harmonic oscillator (LCHO).

using the help of any stimulus, HBA uses an initial value of base frequency to run an autonomous analysis. It exploits a nonlinear algorithm and depends on careful initialization to avoid invalid or degenerate solutions (where all non dc figures are zero). A two tier Newton approach is employed to find the probe voltages and small-signal admittance analysis estimates the point of oscillation. A voltage probe (internally applied) contributes to this estimation process by assuming its source resistance to be a short circuit at oscillation frequency. This form of HBA is also capable of phase noise analysis which allows an assessment of the effect of device noise around the point of oscillation.

In the next subsection, the uncompensated LC tuned Hartley oscillator (LCHO) is compared with the LCHO with stabilizing gate circuit. An evaluation of the improvement in fidelity of oscillator parameters is provided against process and system variation. The LCHO without compensation is powered by a current of 7.09 mA (drawn from V_{dd}) which is changed to 7.33 mA with the stabilizing network's inclusion. Fig. 4.4 presents the output spectrum characteristics of the harmonic oscillator (LCHO) without and with the stabilizing technique.

3.3 Stabilization of LCHO

Fig. 4.5 presents the quantification of change in phase noise and period jitter of the LCHO (N and J) as a function of variation in device threshold. A 5-20% change of turn-on voltages and o set frequencies in the 1 kHz 1 MHz range are considered during the analysis. Before compensation, overall increase in phase noise can reach up to 8.1 dBc/Hz for the entire range of o set frequencies (presented in Fig. 4.5(a)). With the inclusion of the SGC, divergence is reduced with N spanning over a much smaller range (<0.2 dBc/Hz). So the stabilizing circuit is able to reduce phase noise variability by a margin of up to 4.16 dBc/Hz at f=1 MHz and 22.8 dBc/Hz at f=1 KHz. It indicates that as offset frequencies

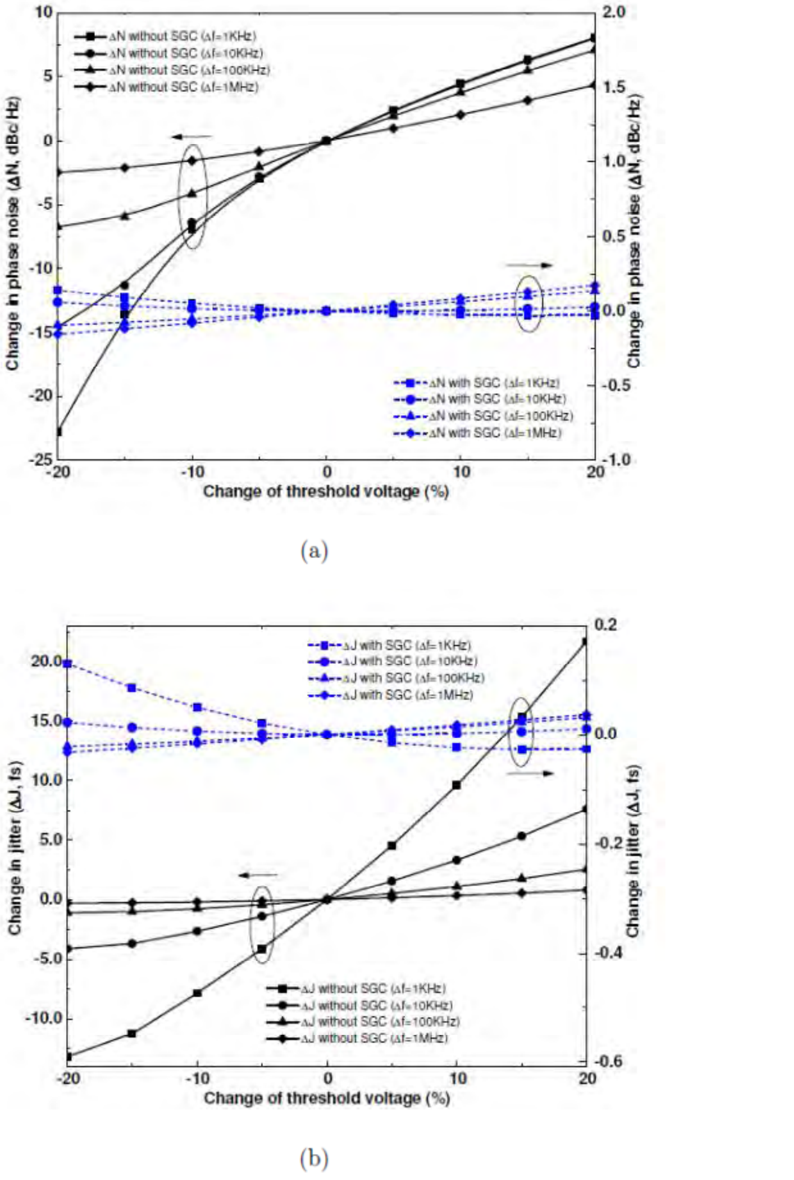


Fig. 4.5: Change in a) phase noise and b) period jitter against threshold shift.

get smaller, variation in phase noise is increased for an uncompensated circuit. According to Fig. 4.5(b), period jitter of the topology may increase by 0.15 21.7

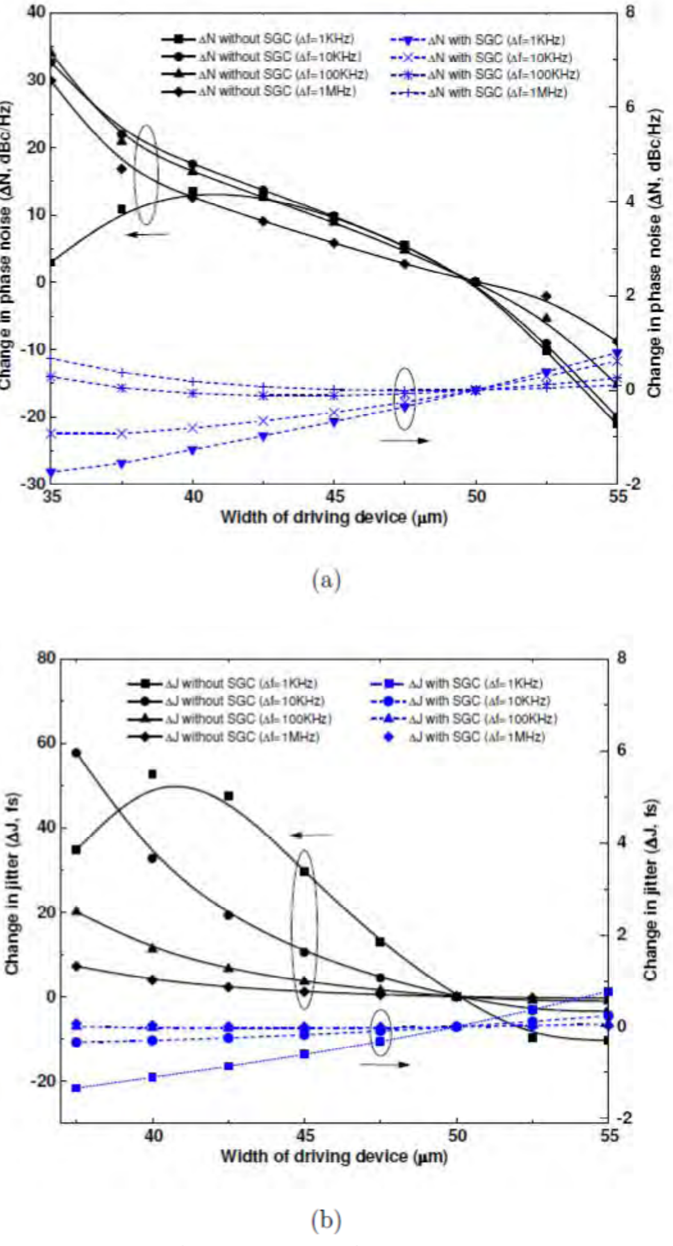


Fig. 4.6: Stabilization of a) noise and b) jitter against varying dimension.

fs without the stabilizing circuit. In contrast, increase in jitter is reduced to <0.13 fs with the introduction of compensation (against threshold deviation).

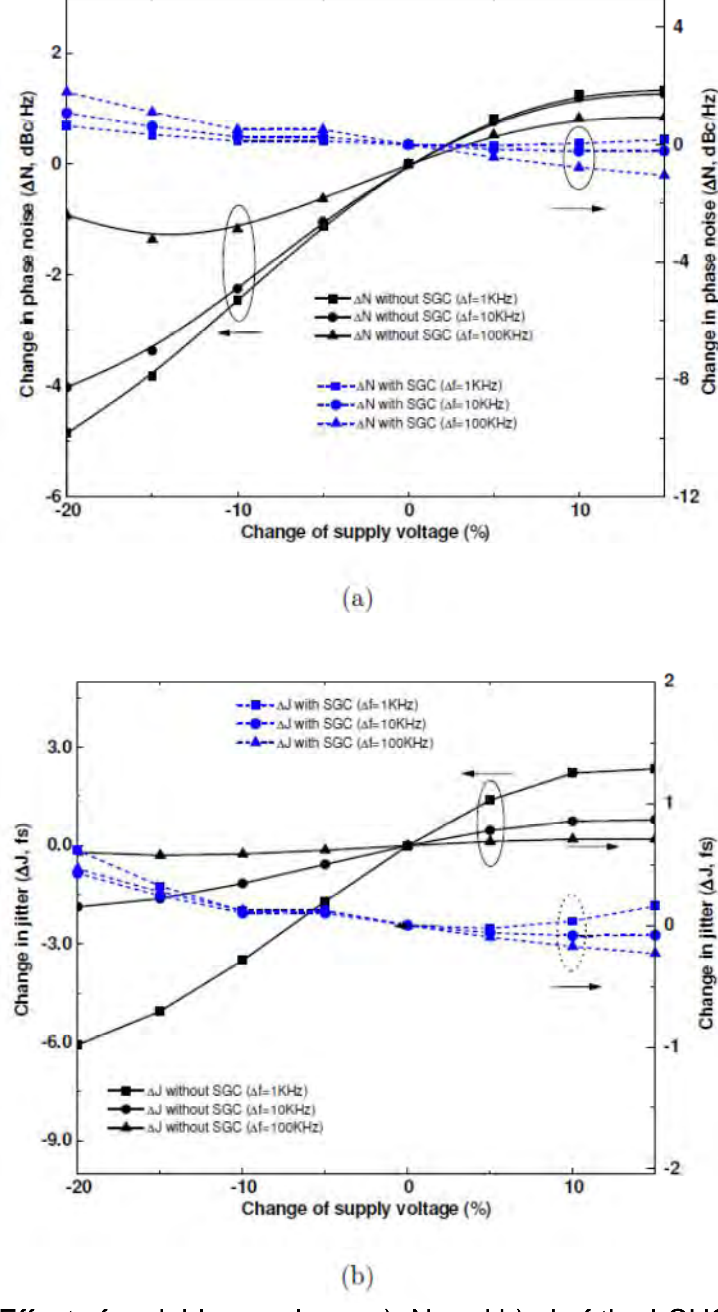


Fig. 4.7: Effect of variable supply on a) N and b) J of the LCHO.

Variation of noise and jitter is also calculated for the LCHO while feature of the driving transistor is varied in Fig. 4.6(a) and Fig. 4.6(b). Over the

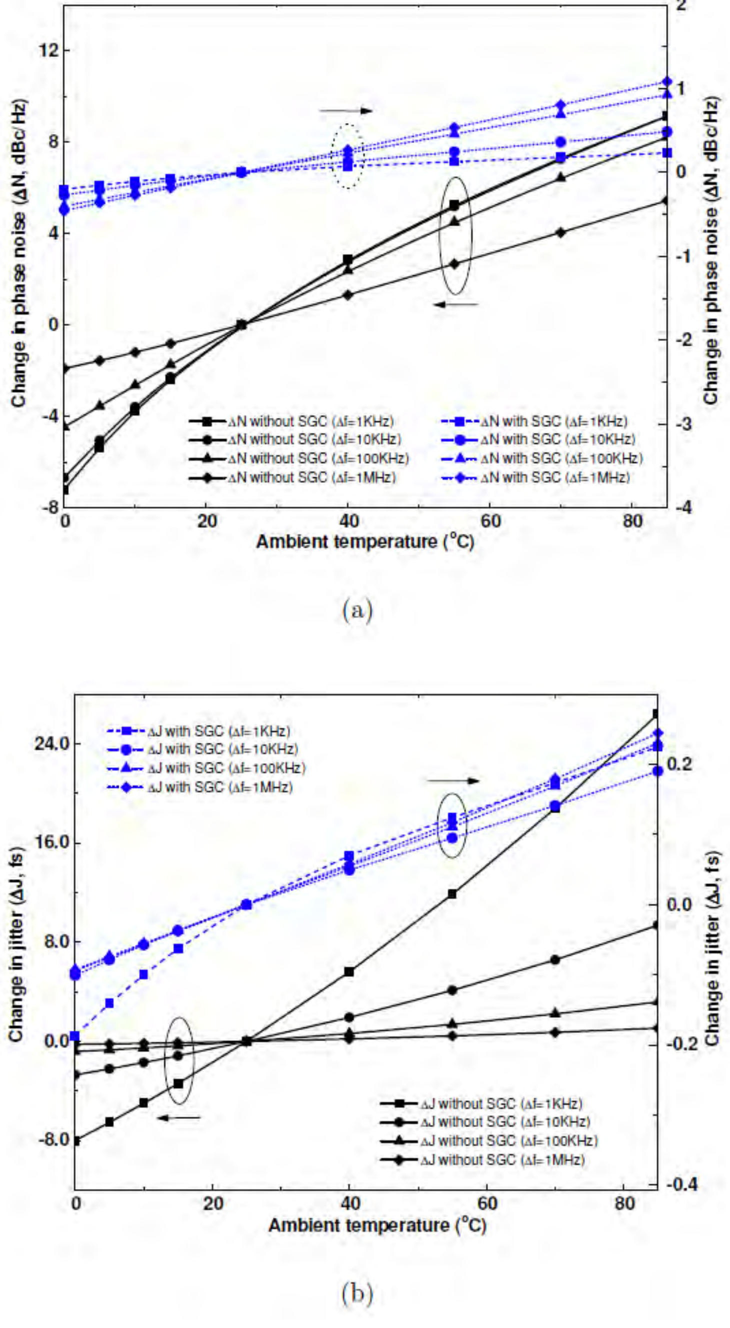


Fig. 4.8: Variation in a) phase noise and b) period jitter versus ambient thermal condition.

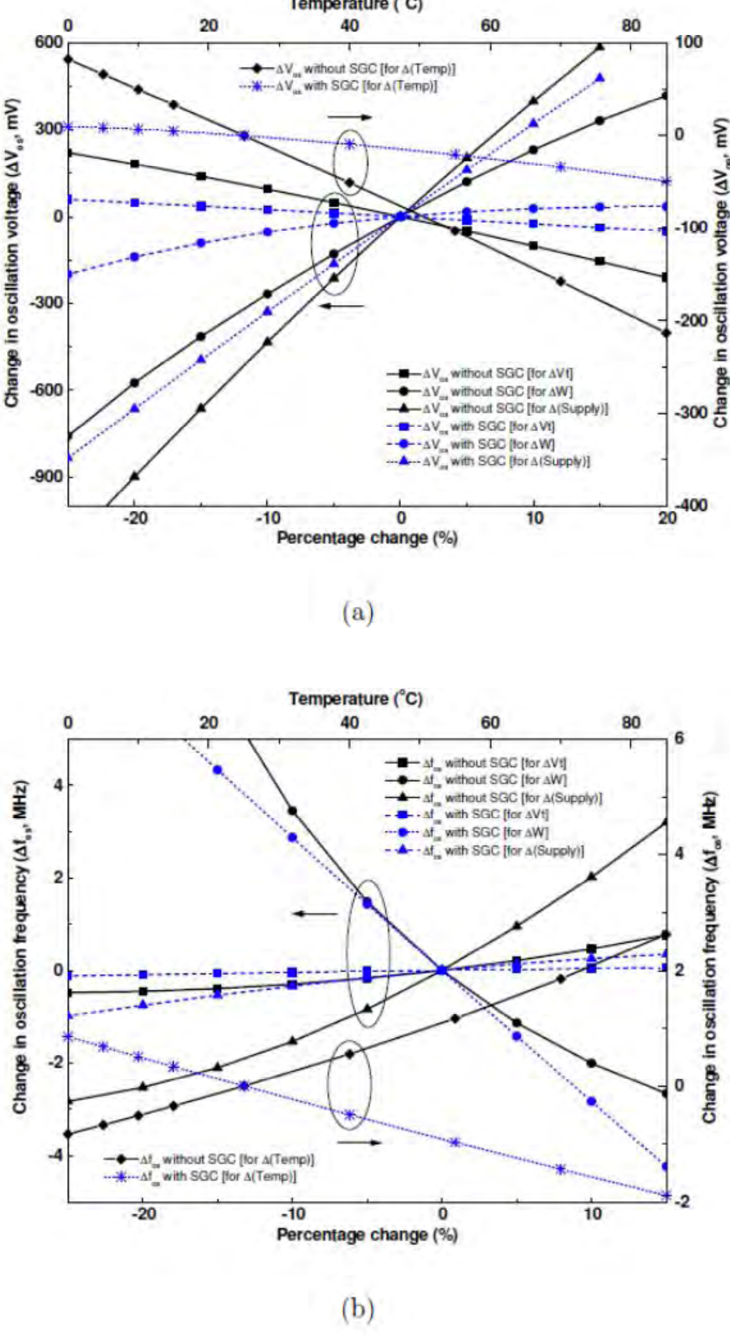


Fig. 4.9: Effect of the stabilizing circuit on a) oscillation amplitude and b) frequency of oscillation.

considered range, N can have values between 2.1-33.9 dBc/Hz with an external gate supply. Conversely, the extent of variability is truncated to <1.73 dBc/Hz with the stabilizing circuit. For various offset frequencies, maximum increase in jitter inhabits the 7.3-57.7 fs range without SGC whereas J remains lower than 1.33 fs after compensation is introduced.

As manifested with the help of Fig. 4.7, the SGC improves the oscillator's consistency against variation of supply rail. It may be noted that, the effect of supply rail on N is less prominent as compared to that of threshold voltage and device dimension. In this case, N for the uncompensated oscillator is <4.86 dBc/Hz and the margin is improved to <1.79 dBc/Hz with the SGC's addition. In a similar fashion, maximum change in period jitter is reduced from 6.08 fs to 0.62 fs with the technique's help. Change in thermal pro le is another major source of PVT deviation and the SGC is also able to improve the oscillator's constancy against this environmental factor. Fig. 4.8(a) and Fig. 4.8(b) show that, when temperature is elevated, increase of phase noise and jitter can reach up to 9.1 dBc/Hz and 26.4 fs for an ordinary oscillator. On the other hand, the stabilizing circuit shrinks these ranges down to <1.08 dBc/Hz and <0.24 fs, respectively.

The effect of disparity in process (threshold), feature, voltage (supply), and thermal pro le on the magnitude of oscillation is illustrated with the help of Fig. 4.9(a) where improvement in stability is observed in different extents for each of the studied variables. Against threshold deviation, maximum voltage degradation is lowered from 10.6% to 2.4% over the considered range. For feature and supply, the margins of improvement are 28.6% and 17.3%, respectively. In addition, voltage degradation can be stabilized by up to 163.9 mV (betterment of variability: 8.3%) against fluctuating system pro les (0-85°C). Fig. 4.9(b) demonstrates the extent of deviation of oscillation frequency against the same

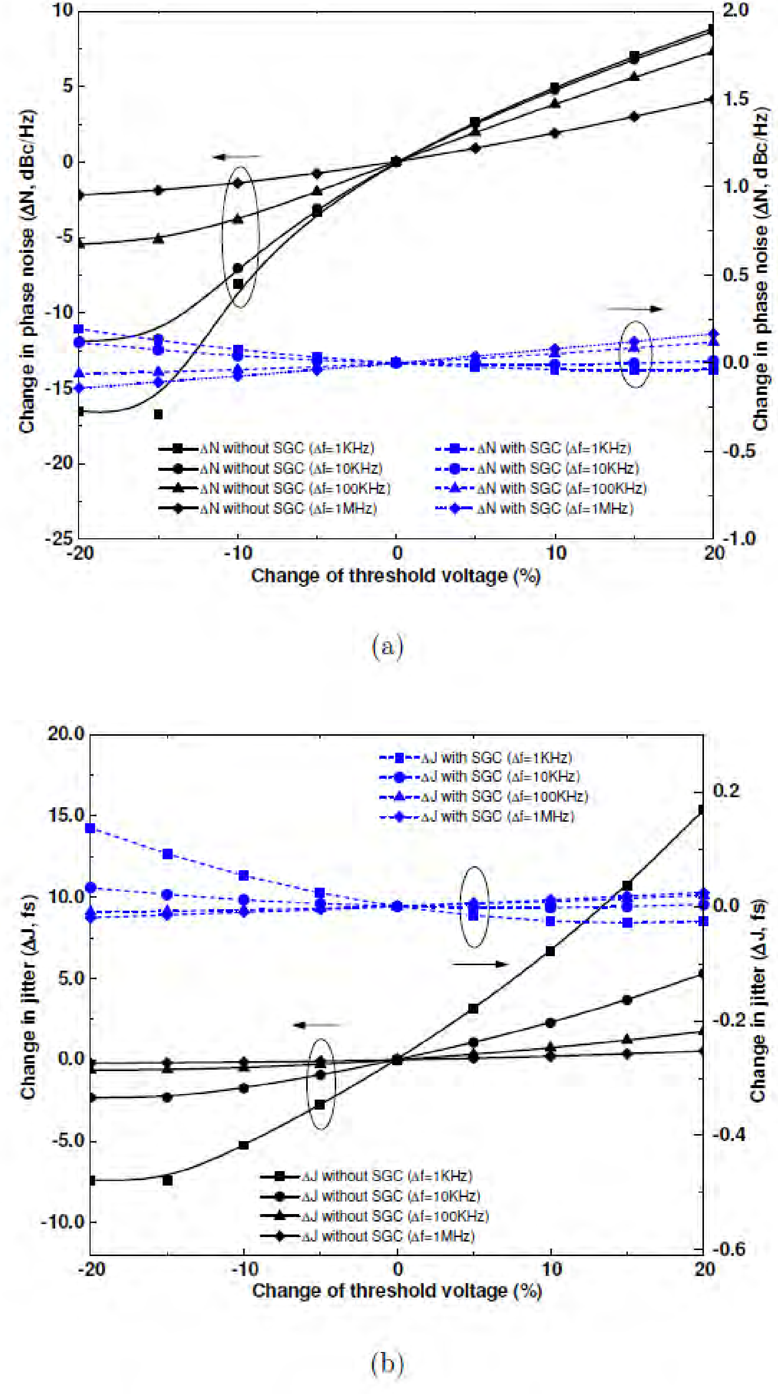


Fig. 4.10: a) N and b) J for the DLCHO as a function of threshold shift.

process factors where the best improvement is obtained for a variable supply voltage.

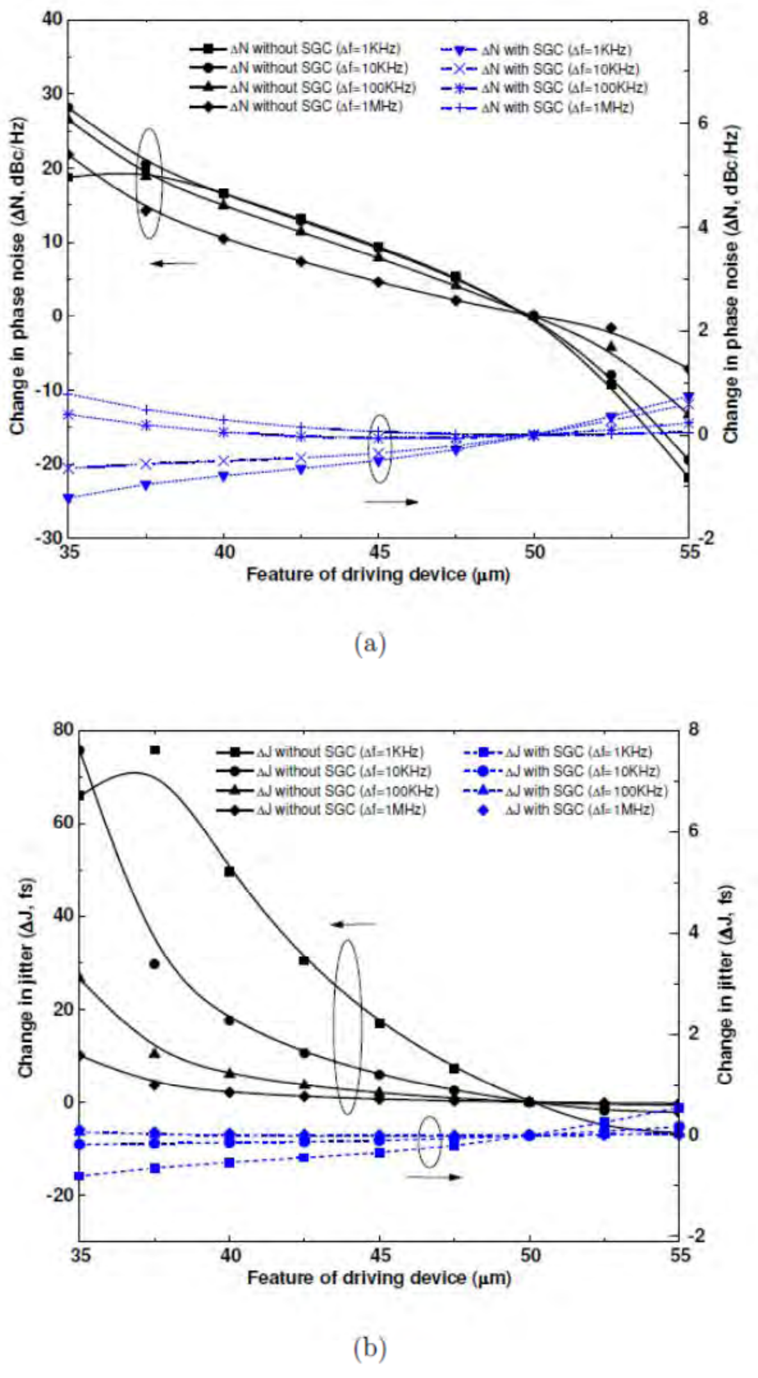


Fig. 4.11: Compensation of a) noise and b) jitter in the DLCHO.

3 Stabilization of DLCHO

To understand the effect of the stabilizing circuit on the reliability of a differential oscillator, RF parameters of the typical differential LC oscillator (DLCHO)

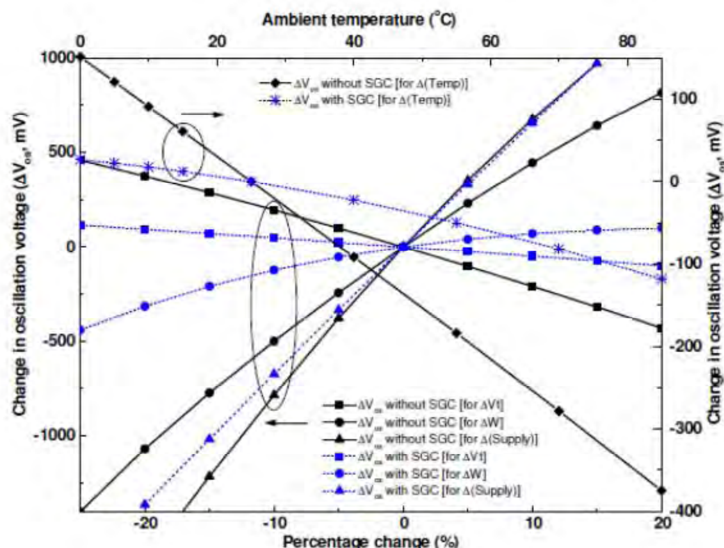


Fig. 4.12: Improvement in reliability of oscillation magnitude for the differential oscillator.

are compared with those of a compensated DLCHO. In this case, the oscillator current (with two half circuits) is changed from 13.85 mA to 14.66 mA with the incorporation of the stabilizing network.

Fig. 4.10 documents N and J for the DLCHO as a function of o set frequency and threshold shift. Before compensation, overall maximum increase in phase noise resides between 4.1 and 8.9 dBc/Hz for the topology. This range is curtailed to 0.12-0.2 dBc/Hz with the SGC's inclusion. The stabilizing circuit is also able to limit undesirable changes in differential jitter with its margin of rise dropping from 0.1 15.4 fs to <0.14 fs. When device width is varied, change in N_p and increase in J_p for the uncompensated DLCHO are 1.6-28.1 dBc/Hz and 0.24-75.8 fs, as presented in Fig. 4.11. The SGC is able to keep these parameters below 1.21 dBc/Hz and 0.8 fs, respectively. Similar to its single-ended counterpart, magnitude of oscillation is also stabilized for the DLHCO with the help of the proposed technique, as shown in Fig. 4.12. Therefore, it can

be said that the stabilizing mechanism is compatible with both single-ended and differential configurations of LC tuned harmonic oscillators.

When the effect of the proposed stabilization method is analyzed for frequency tuning it shows that the technique does not have a significant influence against variation of frequency selecting elements (tank capacitor C_{d1} and feedback elements L_{o1}, L_{o2}). As a result of 20% variation in L_{o1}, deviation of oscillation frequency for the uncompensated LCHO resides between -4.7% and 5.4%. In contrast, the corresponding values for the stabilized oscillator lies between -4.4% and 5.4%. Similarly, a variable tank capacitor (C_{d1}) results in a drop in oscillation frequency of up to 8.5% and 8.6%, respectively, before and after the addition of the stabilizing technique. The impact of process variation on the reliability of harmonic oscillator is also examined with the help of monte carlo (MC) study for the LCHO topology. MC analysis can approximate variation in circuit performance due to random deviation in process and device parameters. It reveals that before the addition of the SGC, standard deviation (SD) of oscillation amplitude for the harmonic oscillator (LCHO) is 0.237 V for valid oscillations. With the introduction of the stabilizing technique, the SD comes down to 0.058 V. MC analysis for the improved oscillators also reveal a stable oscillation frequency (f_{os}). Accordingly, the SGC results in a mean value and SD of 3.254 GHz and 16.28 MHz for the point of oscillation whereas mean value and SD of f_{os} for valid oscillations of the uncompensated oscillator are 3.244 GHz and 18.40 MHz, respectively.

3.4.4 Comparison of Performance

To compare the SGC (applied to the LCHO) with reported process stabilizing techniques [128, 136{138], Table 4.1 documents simulation results outlining reduction in parameter variability (RPV) achieved by the mechanisms. Percentage

Table 4.1: Comparison between process stabilizing techniques.

Ref.	RPV	Type of variation	Circuit parameter
This work	1.8∼8.1%	VT[1]	OA[6]
This work	2.5∼6.0%	VS[2]	OA[6]
This work	0.8∼4.2%	VT[1]	PN[7]
[128]	0.8∼2.1%	VT[3]	PN[7]
[136]	0.3∼0.8%	VS[2]	OP[8]
[136]	0.2∼0.8%	VT[4]	OP[8]
[137]	0.3∼4.1%	VS[2]	GA[9]
[138]	<6.8%	VH[5]	GA[9]

[1] Threshold variation (5-20%)
[2] Supply variation (4-10%)
[3] Threshold variation (10%)
[4] Threshold variation (4-8%)
[5] Temperature variation (0-60°C)
[6] Oscillation amplitude
[7] Phase noise
[8] Output power
[9] Circuit gain

improvement is estimated in terms of RF parameters like oscillation amplitude, phase noise (OA/PN, for harmonic oscillators), output power (OP, for power amplifiers) and forward gain (GA, for low-noise amplifiers). The documented techniques improve circuit stability against variation of device threshold (VT), power supply (VS), and temperature (VH). Among them, the mechanism presented in this work reduces variability of oscillation magnitude by up to 6.0% against variable supply and 8.1% against variable threshold. Additionally, improvement of phase noise deviation is realized by up to 4.2% versus threshold deviation. In comparison, the technique of [128] lowers variability of phase noise by up to 2.1% against threshold variation. The circuits of [137] and [138] improve gain deviation by <4.1% and <6.8% against supply and temperature variation and the

mechanism of [136] stabilizes output power for deviating supply and threshold. The table verifies the effectiveness of the proposed technique in improving circuit reliability against process and system induced variation.

4.4 Conclusions

This chapter realizes a reliability improving technique for nanoscale CMOS harmonic oscillators in the form of a stabilizing gate circuit. It utilizes the current dependence of key oscillating parameters like oscillation magnitude, timing jitter, and phase noise to truncate their process variability. Differential and single-ended architectures of modified harmonic oscillators, which achieve lower than -59 dBc/Hz and -55 dBc/Hz phase noise for 1KHz-1MHz o set frequencies, are tested with the technique. The scheme imposes a relatively small burden on power rating and does not modify output spectrum characteristics significantly. Variation of the circuits' figures of merit is analyzed against deviation in aspects of process (threshold, feature) and system (supply). The results suggest significant stabilization of the sensitivity of oscillator parameters (against stress factors) when compared with previous compensation techniques.

Chapter 5

Voltage Lowering and Gain Control Techniques for a Single-supply-driven 0.7-V Amplifier

1.9 Introduction

Because of cost-efficiency, low power demand, and high level of achievable integration, submicron silicon technologies have been widely employed for realizing integrated systems for networks-on-a-chip [139{141]. Despite the earlier dominance of high-end foundries using group III-V materials, silicon CMOS is now considered the preferred choice for digital and radio-frequency circuits owing to its higher achievable performance-per-watt (PPW) [142{145]. Additionally, there have also been reports of wireless transceiver standards in silicon where demand for higher data rate is continually pushing up operating frequencies [146,147]. For example, recent literature has documented millimeter-wave CMOS receivers operating in 12-26 GHz bands which are suitable for high-capacity wireless schemes, satellite communication related circuitry, and radar systems [148{153].

Among nanoscale transceiver circuits, a microwave low-NF (noise-figure) amplifier (LNA) typically features in the receiving front-end section of a wireless transceiver. This amplifier, depending on its bandwidth limited forward gain, determines overall noise sensitivity of the following receiver section [150]. In re-

sponse to the demand for high data rate communication, several 90-180 nm CMOS amplifiers operating within or near the K-band have been reported [75,154{159]. They have included low-voltage 20.5 GHz body-biased amplifiers [154], front-ends with high small signal power gain (20-28 dB) [75,155,156], and LNAs with noise-figure ceilings of 2.9-6.1 dB [75,155{159]. These circuits are designed with bias rails of 1.0-1.8 V which result in power requirements ranging from 8 to 36 mW [75,155{159]. As companion to the main supply rail, they typically require a number of scaled gate voltages (two to six) to bias transistors in a suitable mode of operation. As a result, the number of required voltage rails is increased which raises the scope for multiple supply variability to be a factor (and it may necessitate the inclusion of more regulated supplies in the architecture). Additionally, as signal power received by a front-end can be very small, the amplifier needs to boost it sufficiently with available power gain. Therefore, if a gain control mechanism is supported by the low-NF circuit, it would be able to cover a wider range of signal strength and should be a desirable addition to the architecture.

As part of improving circuit reliability induced by multiple supply variation, this chapter proposes a K-band amplifier structure which can be driven by a single power supply without separate gate signals. It employs a sectioning mechanism for the bias path to lessen the burden on system power rail (0.7-V) and reduce power dissipation and packaging requirements. A three-stage cascaded topology is used to improve port isolation and overall gain with the output common-drain block being designed for port matching and stability enhancement. With the help of an output control voltage, a gain regulation technique is introduced to the architecture which can regulate bandwidth limited gain by up to 6 dB for a small increase in power demand (1.27 mW). A single-supply 0.7-V circuit using the presented low-voltage mechanisms is analyzed with a 90-nm technology delivering 3 dB NF and high forward gain within a K-band bandwidth spanning

over 1.7 GHz. Port return-losses achieve best figures of -19.2 dB and -26.1 dB (at input and output) and the architecture has an estimated area requirement of 0.62 mm^2. The chapter is organized as follows. Section 5.2 introduces architectural considerations for a wireless receiver and describes the presented single-bias-supply multistage amplifier. The improvement of front-end performance by an output stage is explained and a gain regulation technique is presented. Small signal circuit analyses, parasitic considerations, and effect of process variation are discussed for the topology. Section 5.3 documents results for a 0.7-V amplifier using the single-supply-driven architecture. Section 5.4 compares results of the presented circuit with reported data which illustrates the low-voltage design's merits. Section 5.5 concludes this chapter with general discussions.

2.6 Front-end Architecture

A receiver architecture including a K-band front-end which is able to exploit benefits of heterodyne and direct-conversion schemes simultaneously [75] is presented in Fig. 5.1. The front-end performance, which follows a receiving antenna and an RF filter (for separating channel noise), is dependent on the low-power amplifier as the latter determines achievable receiver NF and range of linear behavior. A direct-conversion circuit can be helpful in this situation as it employs a single down-conversion step for extracting baseband signal and avoids use of power-hungry intermediate filters. On the other hand, a heterodyne structure walks around oscillator leakage and signal o set problems of a direct-conversion design but increases circuit burden and hardware complexity for the overall receiver.

In Fig. 5.1, the initial band-selection filter rejects spurious elements present in the captured signal and the subsequent front-end realizes a dual-end output with the help of a differential mixer. Overall receiver (front-end) gain is settled by

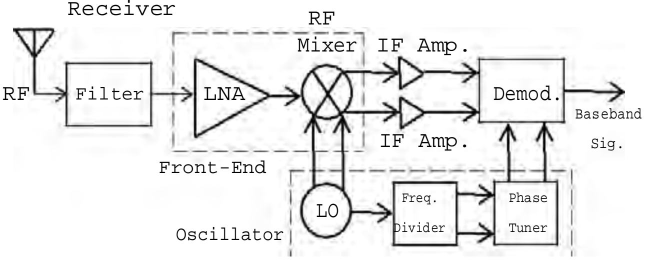


Fig. 5.1: A wireless receiver front-end housing a low-power amplifier.

employing single- or multistage amplifiers and using conversion gain of the mixer. If the LNA is operating in the middle portion of K-band, then the signal oscillator (LO) needs to generate an excitation in the left band section so that intermediate circuits managing the dual-end output can have a suitable sliding frequency. The oscillator section also houses a frequency divider circuit to drive the demodulator block and a phase tuner to cover errors arising from mismatches. The combination of divider and tuner ultimately delivers phase aligned signals to the demodulator which can include in- and quadrature-phase down-converters and produces the decoded baseband signal. A single-supply-driven amplifier which is suitable for relaxing voltage and power requirements of such a receiver is presented in the next subsection.

2.2.7 Single-supply-driven Amplifier Architecture

A voltage lowering strategy for a low-NF receiver amplifier is presented in Fig. 5.2 which permits the front-end to be driven from a single bias supply of 0.7-V without additional gate signals and bias arrangements. Fig. 5.2(a) shows a regular input-matched common-source-gate (cascode) amplifier which is typically driven by a 1.2-V power supply (V_{dd1}) for 90-nm active devices (T_1 and T_2). To bias the transistors, the main power rail delivers the gate voltage of T_2 and a separate lower gate supply ($V_{gate} < V_{dd1}$) is needed for driving device T_1. L_{s1}

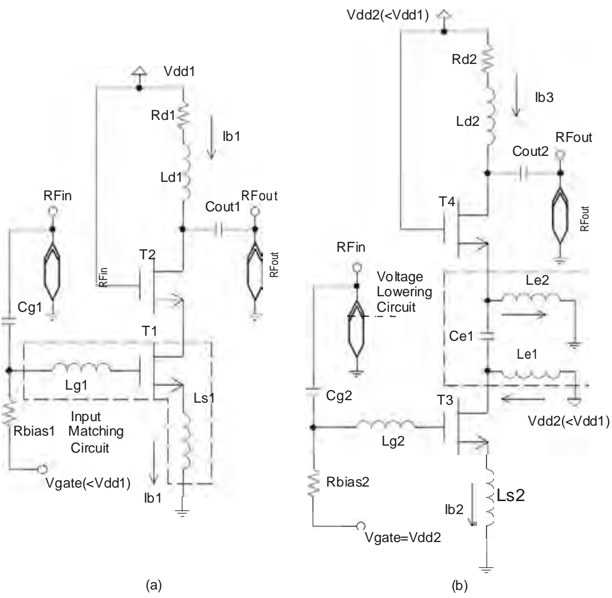
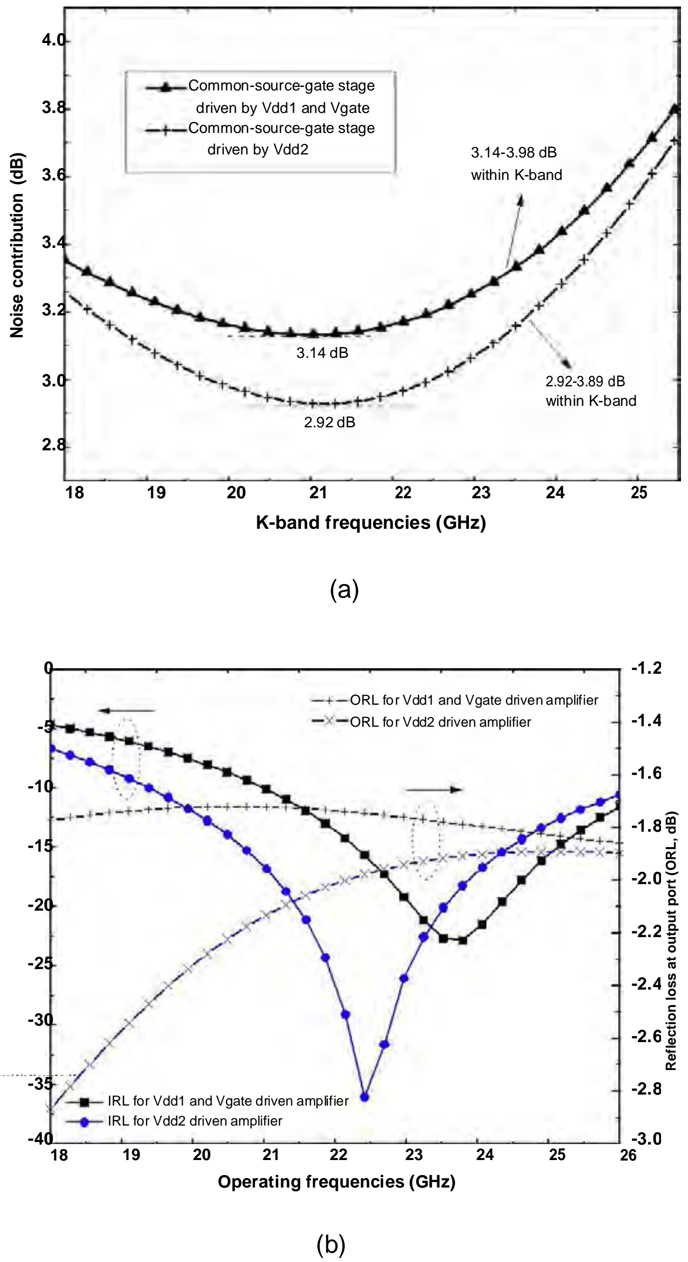


Fig. 5.2: a) An input-matched common-source-gate stage driven by a 1.2-V supply (V_{dd1}) and a separate gate voltage ($V_{gate}<V_{dd1}$) b) The amplifier stage driven by a single lower bias supply V_{dd2} (0.7-V).

and L_{g1} are parts of source degeneration and input matching network and the transistors have a common bias tree current (I_{b1}). To center this single-stage operation near the left edge of K-band, the devices need to have a channel width of 40 m. In this situation, reducing the supply voltage can limit the front-end's power requirement and allow the circuit to be driven from a single and scaled power supply. To meet this objective, a sectioning network made with an LC circuit (L_{e1}, C_{e1}, and L_{e2}) is appended to the bias path in Fig. 5.2(b). It allows the principal devices to be supported by two separate bias currents ($I_{b2=3}$) while

T_3 can have a gate signal (V_{gate}) which is identical to the amplifier's main supply (V_{dd2}). Here the pathway is sectioned with L_{e1}, L_{s2} forming the way for T_3 and L_{d2}, L_{e2} establishing the path for T_4. Depending on size of devices and passive elements, I_{b2} and I_{b3} can have similar or slightly different ratings, increasing the



(a)

(b)

Fig. 5.3: a) Noise-figure (NF) and b) input/output return-loss (IRL/ORL) for the two structures presented in Fig. 5.2.

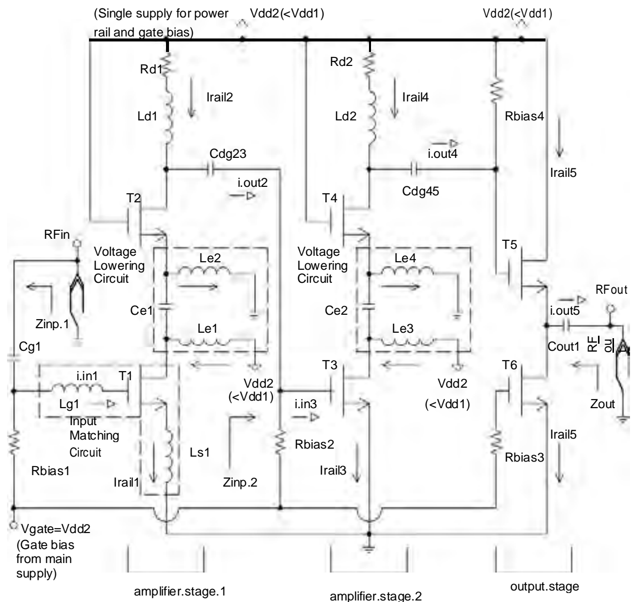


Fig. 5.4: The single-supply-driven CMOS amplifier architecture.

flexibility of the bias setup.

This single-supply circuit would increase the amplifier's area requirement and relevant parameters are determined to understand its effect on noise and matching performance. The technique allows independent matching of active devices and, consequently, NF for a single stage is improved by 0.22 dB, as suggested by Fig. 5.3(a). The supply voltage (V_{dd2}) is reduced with respect to a regular rail (V_{dd1}=1.2 V) and reasonable input matching is maintained for a larger band of frequencies. Fig. 5.3(b) shows that input return-loss (IRL) for the traditional amplifier driven by V_{dd1} and V_{gate} is <-8 dB within the bandwidth (BW) of 20.2-27.5 GHz with a minimum peak of -22.7 dB. On the other hand, IRL for the single-supply stage of Fig. 5.2(b) is <-8 dB for a wider BW of 18.6-27.6 GHz. In the presence of a single coupling capacitor (C_{out2}), ORL is still marginally improved from -1.72 -1.86 dB to -1.89 -2.86 dB within K-band for the low-

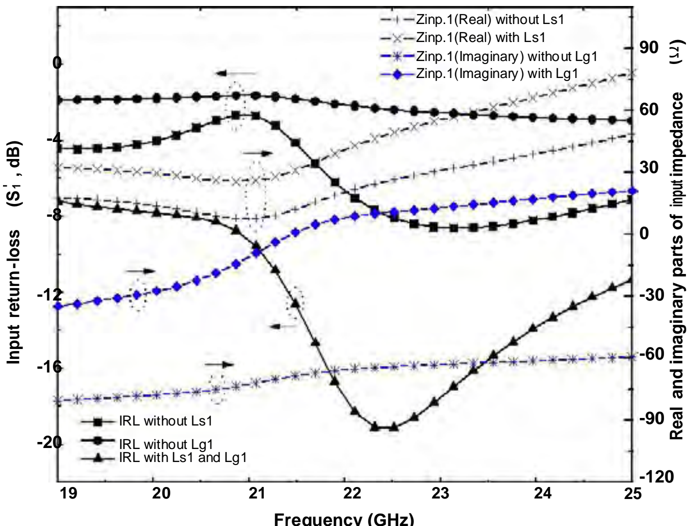


Fig. 5.5: Effect of matching inductors on input impedance and IRL.

voltage front-end.

2.7 Three-stage Amplifier without Scaled Gate Voltages

As the single common-source-gate stage in Fig. 5.2(b) can only provide low to moderate gain in K-band, a high-gain circuit needs to have multiple cascaded blocks to deliver the required pro le. For this reason, the low-power architecture is extended in Fig. 5.4 with two voltage-lowered single-supply stages to boost gain (at reduced voltage requirement) and an output common-drain block to facilitate matching and gain regulation. The power rail and gate signals of all stages and transistors are supported by the scaled 0.7-V bias supply (V_{dd2}). As a result, the architecture does not need separate gate voltages or integrated bias mechanisms. Here, source reactance is provided only for the input stage (amplifier.stage.1) with

L_{s1}, C_{gs1}, and L_{g1} forming the input matching circuit. Apart from degenerating gain, the small inductor L_{s1} regulates the real part of input port impedance

$Z_{inp:1}$ which, in turn, controls the magnitude of IRL. On the other hand, C_{g1}

and L_{g1} settle the frequency where IRL achieves its peak by changing the zero crossing point of $Z_{inp:1}$(I). As shown in Fig. 5.5, the value of $Z_{inp:1}$(<) without L_{s1} resides within 16.1-24.5 between 20 and 22 GHz. Similarly, the imaginary element of $Z_{inp:1}$ in the absence of L_{g1} is >-59j , thus preventing IRL from being centered around the desired frequency. After the addition of the reactive source component, $Z_{inp:1}$(<) is raised to 27.3-46.4 (approaching 50) within 20-22 GHz. At the same time, L_{g1} forces $Z_{inp:1}$(I) to cross 0j at 21.3 GHz and correspondingly peak S_{11} is reduced to -19.2 dB. In this way, the input circuit manages power matching for the first low-voltage stage with resistive elements of inductors [160]:

$$R_{inp.1} \approx R_{s1} + R_{g1} + \omega_{t1} L_{s1} \tag{5.1}$$

where R_{s1} and R_{g1} stand for resistive components of the coils and $!_{t1}$ is the in-put stage's effective corner frequency. In contrast, noise matching is achieved by adjusting the driving transistor size which also regulates effective transconductance of the first 0.7-V stage (g_{m1}). If k_{in} is a factor characterizing device noise and C_{gs1}, C_{gd1} are parasitic elements of the driving transistor, optimum noise resistance of the first stage can be expressed as [160]

$$R_{inp.1_{noise}} \approx R_{s1} + R_{g1} + \frac{k_{in} f_{t1}}{g_{m1} f} \tag{5.2}$$

$$\Rightarrow R_{inp.1_{noise}} \approx R_{s1} + R_{g1} + \frac{k_{in}}{\omega(C_{gs1} + C_{gd1})}. \tag{5.3}$$

Input matching with these elements in the K-band is challenging because the port may contribute parasites to the matching network. Ultimately, minimum noise factor of the input stage can be approximated with the following equation [161]

$$NF_{stg.1_{min}} = 1 + 2G_{n,amp}[R_{core,amp} + R_{inp.1_{noise}} + Z_{11}(\Re)] \tag{5.4}$$

where Z_{11} is obtained from an impedance matrix of the matching network formed by L_{s1}, L_{g1} and $G_{n,amp}$ is input noise conductance of the amplifier core. Here,

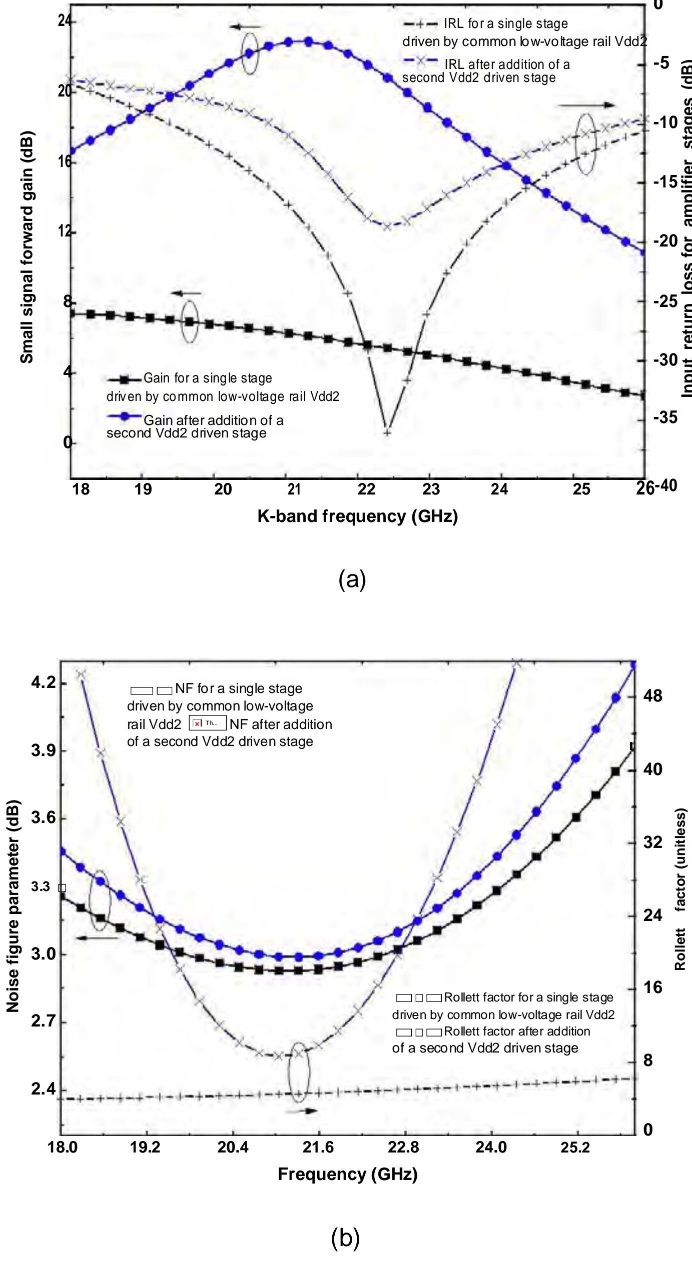


Fig. 5.6: a) Forward gain and input reflection, b) NF and stability factor for single- and two-stage single-supply amplifiers.

the complex Z_{11} parameter of the equation may be obtained as

$$Z_{11} = R_{s1} + R_{g1} + j\omega(L_{s1} + L_{g1}). \tag{5.5}$$

The path created by L_{e1} and L_{s1} (through T_1) draws 1.73 mW power from the V_{dd2} supply. The two branching inductors (L_{e1} and L_{e2}) are not identical in size and face a difference of 0.2 mA in currents (I_{rail1} and I_{rail2}). The cascode load inductor L_{d1} is able to maintain a <8 dB forward gain within K-band for the single-stage amplifier. The coupling capacitor C_{e1} placed between two bias current paths is smaller than the interfacing capacitor C_{dg23} as the latter has to support interstage matching. The second low-voltage branched stage (amplifier.stage.2) for the presented amplifier is identical in structure with respect to the input stage except for a simplified input matching network. I_{rail3} now has a single inductor in the bias path and draws 1.77 mW from the low-voltage power rail. C_{dg45} is built with an interfacing capacitor to support matching with an output common-drain stage. The effect of the inclusion of a second single-supply stage on overall amplifier performance is illustrated in Fig. 5.6(a) and 5.6(b) in terms of gain, noise, return-loss, and stability figures. The peak gain is improved by 15.5 dB with the peak being located at 21.3 GHz. Input return-loss (IRL) remains <-8 dB within the 19.8-26.5 GHz bandwidth after the addition of the second single-supply stage. Careful noise matching ensures that NF increases only by 0.1 dB over the bandwidth. Rollett stability factor is clearly improved with a domain range which is >8.7 as compared to its K-band coverage for the single-stage circuit (4.1-6.4).

To obtain an expression of noise factor for the second amplifier stage ($NF_{stg:2}$), source resistance faced by the driving device is represented as R_{S3} and $_4$ is defined as a parameter governed by bias conditions of T_4. If effect of the voltage lowering circuit is excluded and g_{d04} is the drain-source conductance of T_4 at zero drain-

source voltage, $NF_{stg:2}$ can be approximated as [162]

$$NF_{stg.2} \approx (\gamma_4 g_{do4} R_{s3})(\frac{\omega}{\omega_{t2}})^4 (1 + \frac{\omega_t L_{s2}}{R_{s3}})^2. \tag{5.6}$$

With these functions, overall noise factor for the cascaded two-stage amplifier [163] can be derived as

$$NF = 1 + (NF_{stg.1} - 1) + (\frac{NF_{stg.2} - 1}{A_{p,stg.1}}) \tag{5.7}$$

where $A_{p;stg:1}$ is available power gain of the input stage.

3.4 Effect of Common-drain Stage

An output common-drain stage is incorporated in the architecture to provide the front-end with output matching while regulating its forward gain. This output stage includes a current source implemented by a device in saturation with a constant gate-source voltage. The common bias supply delivers a gate signal for it through R_{bias3}. In addition, two large resistors of the same network provide gate voltages for driving transistors in the first two blocks (T_1 and T_3). V_{dd2} also serves as the power rail for the common-drain device T_5 and determines the output bias current I_{rail5}. A port capacitor C_{out1} is included in the design to support the dual purpose of signal coupling and port matching. This output stage is expected to match the loading effect of a receiver block which may follow the front-end.

The impedance seen by a load following the amplifier has two components which can be attributed to the current source device and the common-drain transistor. Among them, the contribution of T_6 (Z_{out2}) can be approximated from its source resistance (R_{s6}) and transconductance ($g_{m:T6}$). If r_{o6} stands for intrinsic device output resistance then [164]

$$R_{out2} = R_{s6}(1 + g_{m.T_6} r_{o6}) + r_{o6}. \tag{5.8}$$

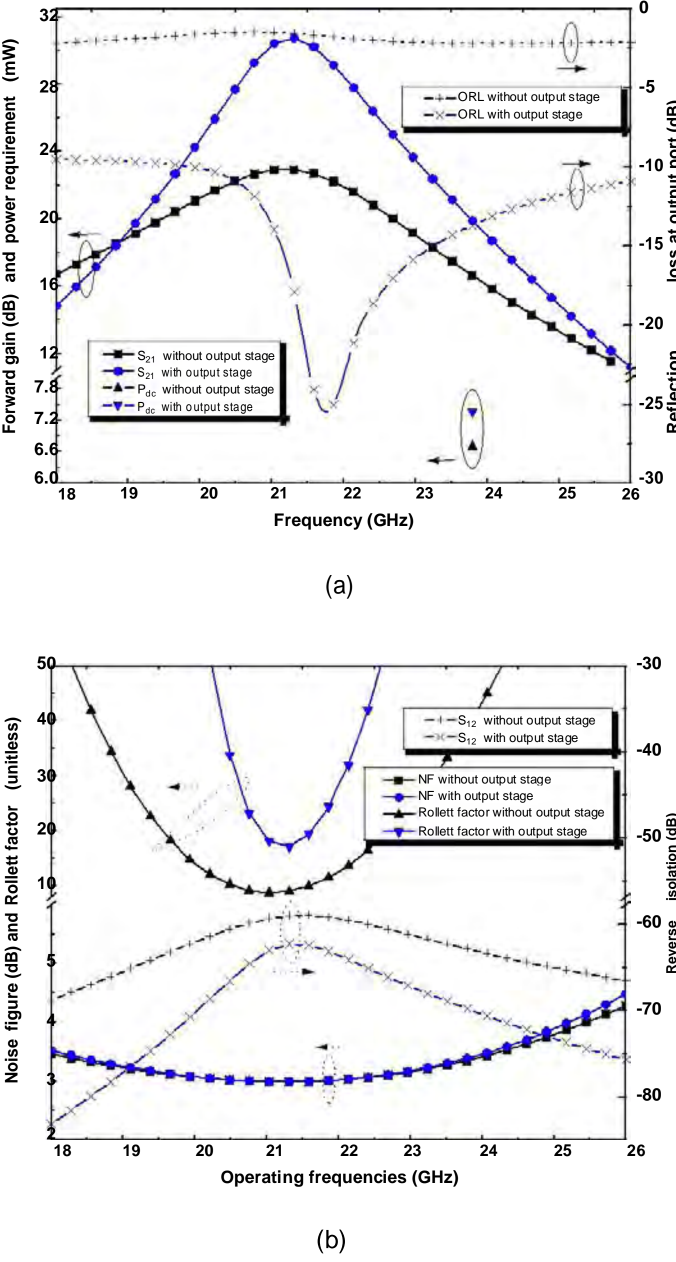


Fig. 5.7: The contribution of the output stage to a) forward gain, ORL, power and b) stability factor, reverse isolation, NF.

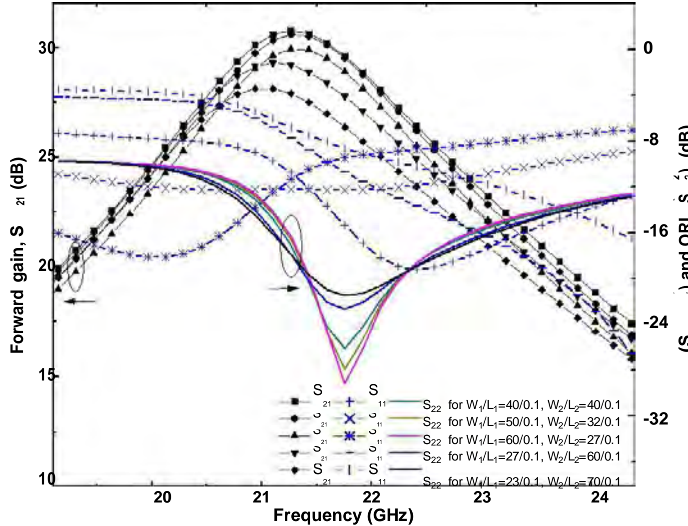


Fig. 5.8: Effect of variable device ratios on scattering parameters.

In contrast, the common-drain contribution can be estimated as

$$R_{out1} = r_{o5} || \frac{1}{g_{m.T_5}}. \tag{5.9}$$

If $1{=}g_{m:T5}$ is designed suitably, device size in the output stage can be used to adjust reflection-loss incurred at load port

$$Z_{out}(\Re) = R_{out1} || R_{out2} \approx \frac{1}{g_{m.T_5}}. \tag{5.10}$$

The contribution of the output block to the amplifier's overall performance (port matching, isolation, noise, power, and gain) is depicted through Fig. 5.7(a) and Fig. 5.7(b). They present the front-end's behavior before and after the inclusion of the common-drain stage. The output section significantly influences port matching, gain, and reverse isolation while increasing NF by <0.2 dB over the K-band. Forward gain is improved by a margin of 4-8 dB within 20-23 GHz and power demand is raised by <1 mW. The effect is most prominent on reflection-loss incurred at output (ORL) which is <-11 dB over the bandwidth

(with a centered peak at 21.8 GHz). ORL without the output block presents a flatter pro le and incurs larger losses (>-2.19 dB). The overall amplifier offers a barrier against reverse leakage (estimated from S_{12}) which reaches up to -83.2 dB near 18 GHz. In contrast, S_{12} for the two-stage amplifier has a best figure of -68.8 dB for the same frequency. Moreover, the minimum reading of stability factor increases from 8.7 by a value of 8.4 near the 21 GHz mark. At the same time, NF pro le is not degraded significantly over the 19-23 GHz range.

It is useful to investigate the effect of variation in aspect ratios of a single amplifier stage (W_1/L_1 and W_2/L_2) on scattering characteristics of the overall amplifier structure. Fig. 5.8 presents the amplifier's S_{21}, S_{22}, and S_{11} parameters for different combinations of device sizes in the input stage. It shows that, peak forward gain remains adequately high as device ratios of the input stage are varied. At the same time, output return-loss (S_{22}) remains lower than -10.2 dB over the bandwidth. The figure justifies the sizing of the transistors to minimize reflection-loss at both ports while maintaining a high power gain. In addition, it indicates that device ratios can be changed while maintaining certain good features of a common-source-gate stage, which is not typically the case for classical cascode amplifiers.

4 Gain Control Technique

The previous section manifests that overall gain of the single-supply circuit can be regulated with the help of an output common-drain stage. This creates an opportunity to introduce a gain control technique to the proposed architecture with the help of a control voltage ($V_{control}$), as shown in Fig. 5.9. This signal can manipulate I_{gain} and regulate small-signal gain at the expense of a small increase in power dissipation. It can also adjust the amount of reflection-loss incurred at load port. In this way, the output stage serves the dual purpose of modulating

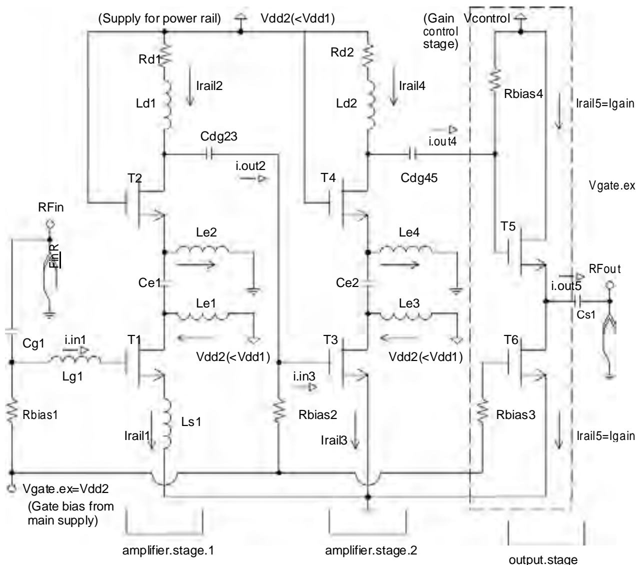


Fig. 5.9: The gain control technique implemented with the output stage.

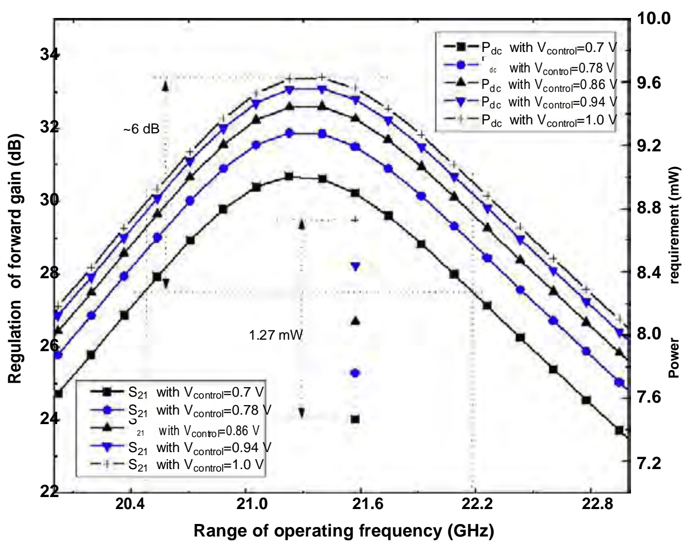


Fig. 5.10: Regulation of gain and power requirement as a function of output control voltage.

gain coverage and managing port reflectance. Fig. 5.10 illustrates the regulation of gain that can be achieved when $V_{control}$ is varied by a small margin. Between

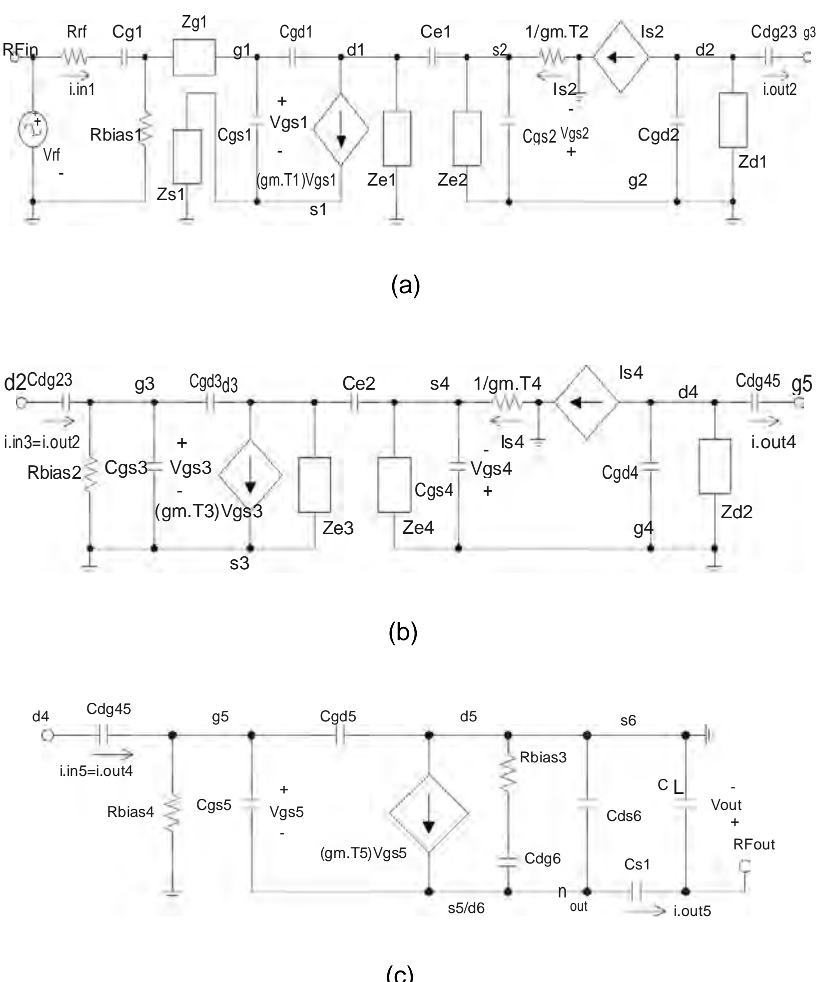


Fig. 5.11: Small-signal equivalent circuits for the amplifier's a) input single-supply stage, b) secondary low-voltage stage, and c) output common-drain stage.

20.5 and 22.2 GHz, simulated forward gain has values covering 6 dB where peak S_{21} is spread over 3 dB. The change in $V_{control}$ results in P_{dc} ratings which can reach up to 8.64 mW (an increase of 1.27 mW). Input matching and noise performance remain largely unaffected during regulation while peak frequency for ORL shifts between 21.7 and 22.9 GHz. In addition, ORL is <-8 dB for most of the K-band and minimum output reflection stays below -21 dB.

3.4.5 Small-signal Circuits

The small-signal equivalent circuits for the three-stage single-supply architecture of Fig. 5.4 are presented in Fig. 5.11(a)-5.11(c). Fig. 5.11(a) shows the input common-source-gate stage with voltage lowering elements Z_{e1} and Z_{e2}. Coupling is established between common-source (CS, realized by T_1) and common-gate (CG, formed by T_2) sections of the first stage through the element C_{e1}. The input matching network is formed through parasites of driving device (C_{gs1}) and matching impedances (Z_{g1}, Z_{s1}). The high value of R_{bias1} segregates it from the small-signal operation. CS and CG transistors of the input stage are defined by voltage- and current-controlled current sources and device transconductance $g_{m:T1=2}$. Gate parasite of the input device (C_{gs1}) sees a Thevenin's resistance (R_{gs1}) which consists of R_{bias1}, Z_{g1}(<), and Z_{s1}(<). In contrast, equivalent resistance seen by the linking parasite C_{gd1} takes the form of [165]

$$R_{gd1} = (1 + R_{drain1} g_{m.T_1}) R_{gs1} + R_{drain1} \qquad (5.11)$$

where R_{drain1} is the resistance faced by drain terminal of T_1 (including the real part of Z_{e1}). The input capacitor for the CG stage (C_{gs2}) principally sees Z_{e2}(<) and $1=g_{m:T2}$ as a Thevenin's resistance (R_{in2}):

$$R_{in2} \approx Z_{e2}(\Re) + 1/g_{m.T_2}. \qquad (5.12)$$

In contrast, impedance seen by Cgd2 can be expressed as

$$Z(C_{gd2}) \approx Z_{d1} \parallel (R_{bias2} + \frac{1}{j\omega C_{dg23}}) \qquad (5.13)$$

where R_{bias2} is the second input bias resistor and this frequency dependent function is primarily dominated by Z_{d1}. Consequently, corner frequency for the input single-supply stage takes the approximated form of

$$f_{stg.1} \approx \frac{1}{2\pi[R_{gs1}C_{gs1} + R_{gd1}C_{gd1} + R_{in2}C_{gs2} + R_{out2}C_{gd2}}] \qquad (5.14)$$

where R_{out2} is contributed by the interstage impedance $Z(C_{gd2})$.

Fig. 5.11(b) shows an equivalent circuit for the second low-voltage gain-boosting stage which is similar to the input block except that the latter's input circuit is replaced by an interfacing capacitor C_{dg23}. Therefore, Thevenin's resistance for C_{gs3} is somewhat simplified. R_{gd3} and R_{in4} will have expressions which are similar to the ones for the input stage and the corner point can be determined as

$$f_{stg.2} \approx \frac{1}{2\pi[R_{gs3}C_{gs3} + R_{gd3}C_{gd3} + R_{in4}C_{gs4} + R_{out4}C_{gd4}]} \tag{5.15}$$

where R_{out4} will be dominated by the contribution of Z_{d2}

The port-matching and gain-regulating output stage is presented as a small-signal circuit in Fig. 5.11(c). The current source in this stage does not require a dependent source representation and the common-drain device has a transconductance of gm:T. Moreover, equivalent capacitance faced by the output node of this circuit (nout) can be written as

$$C_{out} \approx C_{dg6} + C_{ds6} + C_L \tag{5.16}$$

where C_L accounts for the load which follows an amplifier in the front-end. Additionally, gain provided by the output block behaves like a function of device transconductance [166]:

$$A_{v.out} \approx \frac{g_{m.T_5} + sC_{gs5}}{g_{m.T_5} + sC_{gs5} + sC_{out} + g_{out}} \tag{5.17}$$

$$g_{out} = g_{mb5} + g_{ds5} + g_{ds6}. \tag{5.18}$$

Here, the factor g_{out} is defined by backgate transconductance (g_{mb5}) and drain conductances (g_{ds5} and g_{ds6}) and may be excluded from the circuit for simplicity. Ultimately, the operating bandwidth of the output stage is determined by its pole frequency which can be approximated by [166]

$$f_{p,stg.3} = \frac{g_{m.T_5} + g_{out}}{2\pi(C_{gs5} + C_{out})}. \tag{5.19}$$

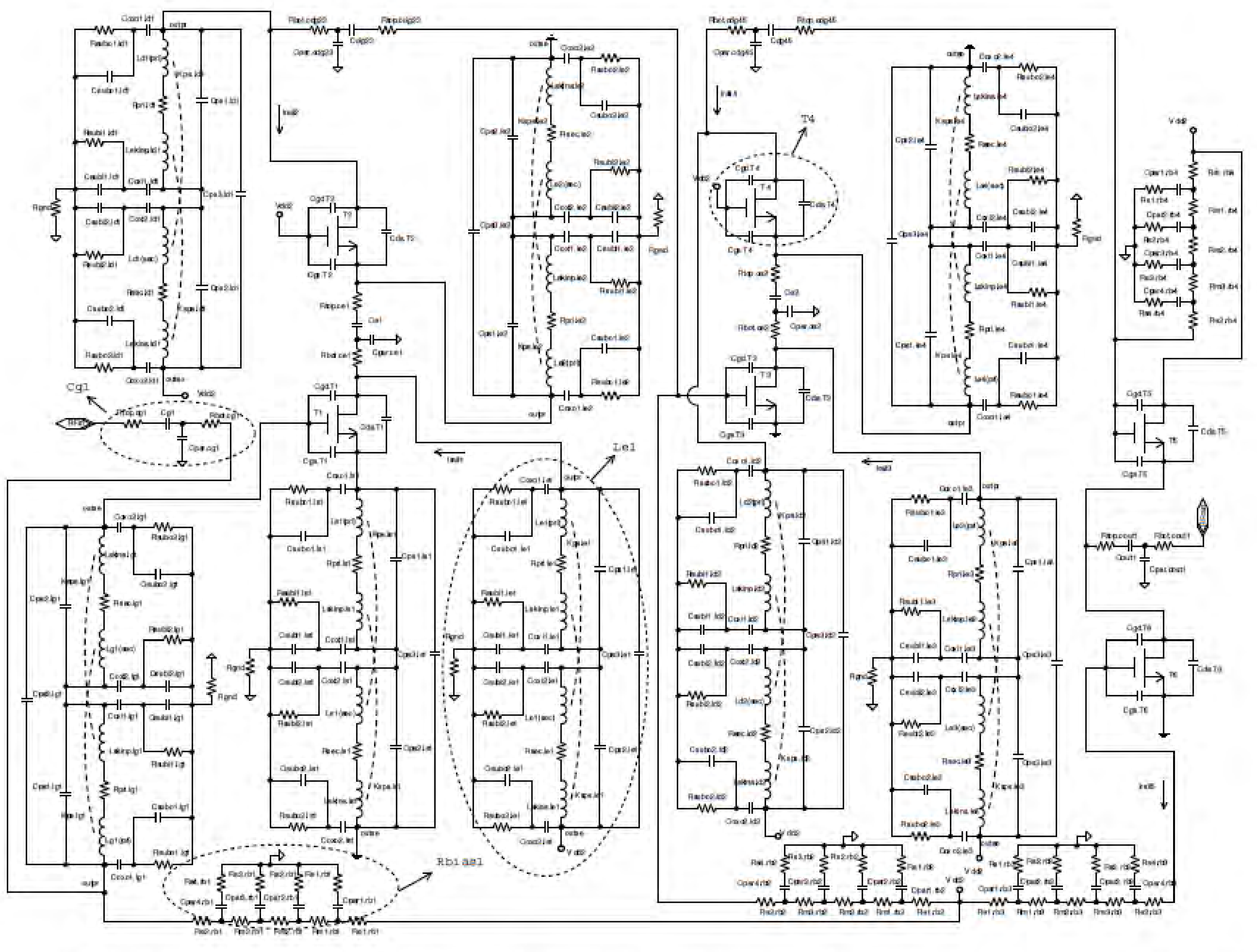


Fig. 5.12: The single-supply-driven architecture with possible parasitic elements generated by devices in a CMOS process.

4.5 Parasitic Considerations of Architecture

A critical point to accurately predict the behavior of a high frequency architecture is the inclusion of parasitic elements during the analysis phase. For a silicon process, a number of extraneous parts have to be appended to core amplifier components to obtain an appropriate parasitic circuit. The single-supply-driven amplifier is presented in Fig. 5.12 with the inclusion of active/passive parasitic contributions. The amplifier includes six n-type field-effect transistors for the trees (T_1 T_6) and their RF circuit incorporates parasitic junction capacitors. Total parasitic capacitance contributed by gate and drain terminals of T_1-T_4 is estimated to be 35 fF and 16 fF, respectively. In case of source junction, capacitive parasites are expected to add up to around 25 fF. Moreover, parasitic capacitance for transistor junctions in the output stage (T_5, T_6) amounts to a predicted range of 20-43 fF. In addition, the parasitic circuits of the passive elements are also presented in the structure.

5.2.7 Process Optimization

Effect of process mismatch on the single-supply-powered topology is investigated through monte carlo analysis (MCA). It allows an assessment of variation in gain, matching, and NF which may result from fluctuation in process parameters. The basic MCA results indicate that peak gain and minimum NF can deviate by up to 2.4 dB and 0.2 dB, respectively, from design values. This translates into a change of about 7% and 4% with respect to centered crest and trough of S_{21} and NF. During MCA, IRL and ORL peaks register values better than -18 dB and -17 dB over the 19-24 GHz bandwidth.

The principal matching component of the circuit's input stage is a small inductor which regulates return-loss at RF_{in} with degeneration of gain. Its opti-

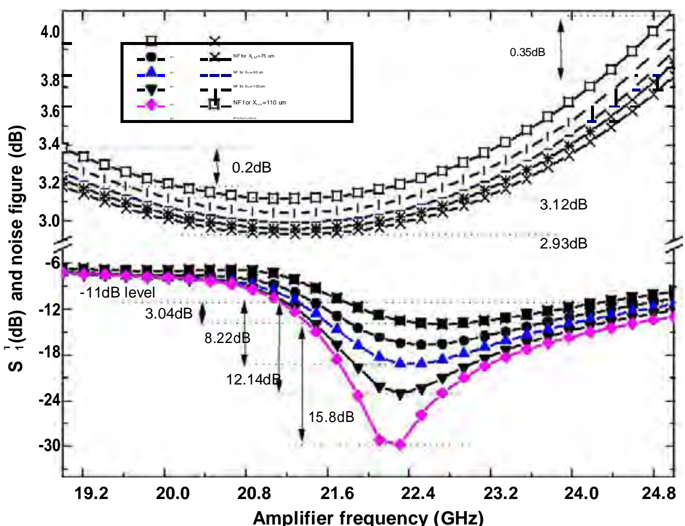


Fig. 5.13: Dependence of input return-loss and noise-figure on the source inductor.

mization is presented in Fig. 5.13 where design range of its outer width (X_{Ls1}) is selected as 75-120 m. Within this range, peak input return-loss (S_{11}) for the circuit always remains better than -11 dB and becomes smaller as width is in-creased. On the other hand, noise contribution of input stage remains reasonably small and minimum NF is <3 dB when selected width stays between 75 m and 100 m. For larger inductors, NF starts to rise sharply for operating frequencies above 22 GHz. Ultimately, minimum IRL can be tuned between -14 dB and -30 dB with this element.

Various reactive elements attached to or between core amplifier stages in u-ence the reflection-loss incurred at amplifier ports (S_{11} and S_{22}). In this regard, the interfacing capacitor before the output stage (C_{dg45}), while being used as a matching component, needs to possess a sufficiently high value for coupling of signals. Fig. 5.14 shows how IRL and ORL are manipulated with this linking element in terms of magnitude and peak frequency. Without changing the center of input matching, the capacitor can reduce minimum IRL from about -16 dB to

around -20 dB. It exerts a greater pull on ORL and is able to move its peak from about 24 GHz to 20 GHz. With a <1 dB change in gain, port return-losses can be regulated and ultimately centered between 21 GHz and 23 GHz. Other amplifier components are optimized in a similar fashion and corresponding results are summarized in the next section.

5.3 Results and Discussion

In this section, the optimized amplifier architecture, which can be driven by a 0.7-V bias-supply, is analyzed with a 90-nm CMOS technology. As the simulation package, an RF simulator is employed to obtain the characterizing parameters. The same low-voltage supply can provide biasing and work as power rail for the topology.

Forward Gain and Noise: Voltage gain (no-load) for the single-supply-driven three-stage circuit is presented in Fig. 5.15 attaining a peak near 21 GHz. It

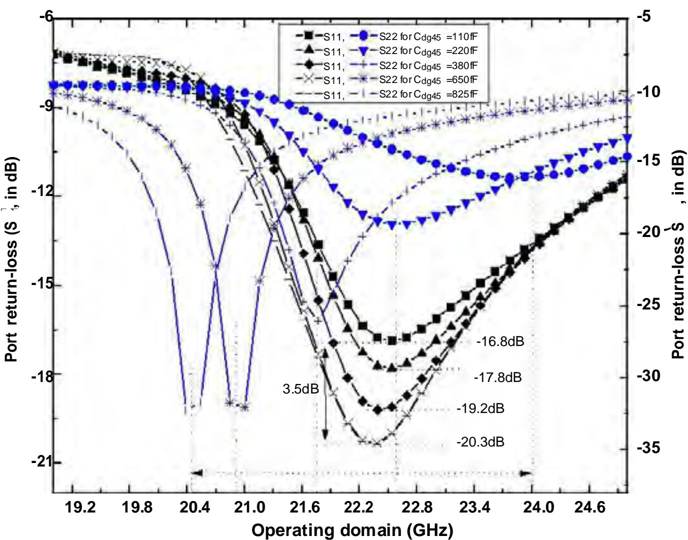


Fig. 5.14: Dependence of port reflection on the second interfacing capacitor.

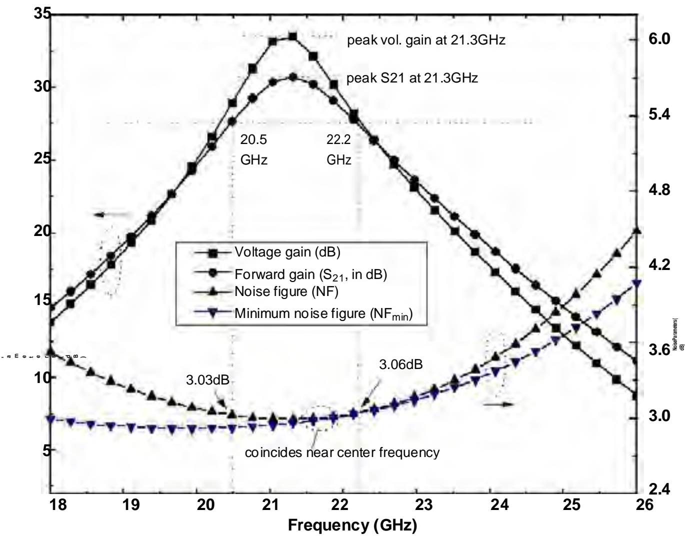


Fig. 5.15: Gain and noise parameters for the single-bias-supply architecture.

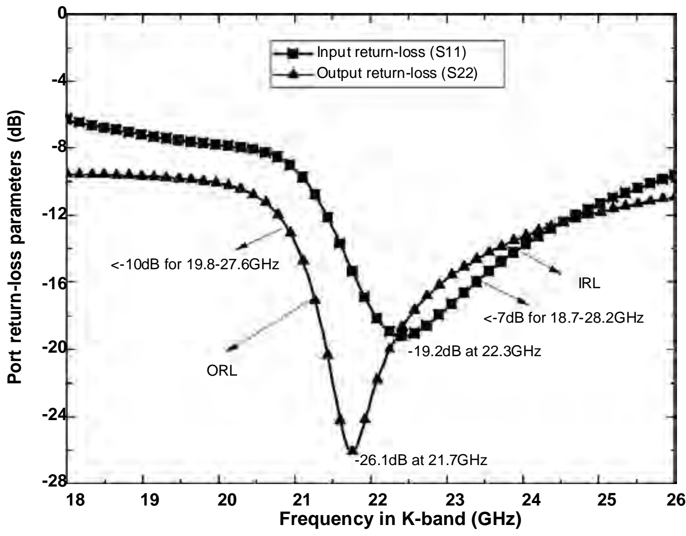


Fig. 5.16: Port return-loss parameters obtained over K-band.

also shows the circuit's small-signal forward gain (S_{21}) having its peak settled in the lower portion of K-band (21.3 GHz). The structure's 3-dB bandwidth spans 20.5-22.2 GHz and it has >25 dB gain coverage within 20-23 GHz. With

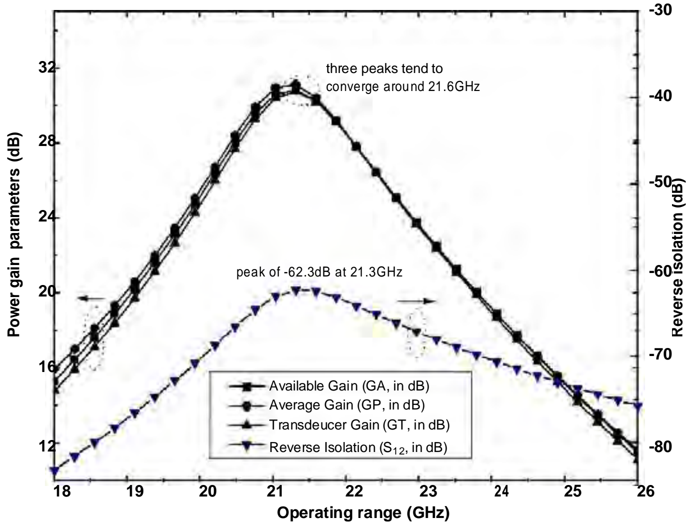


Fig. 5.17: Clustered power gain and reverse isolation curves.

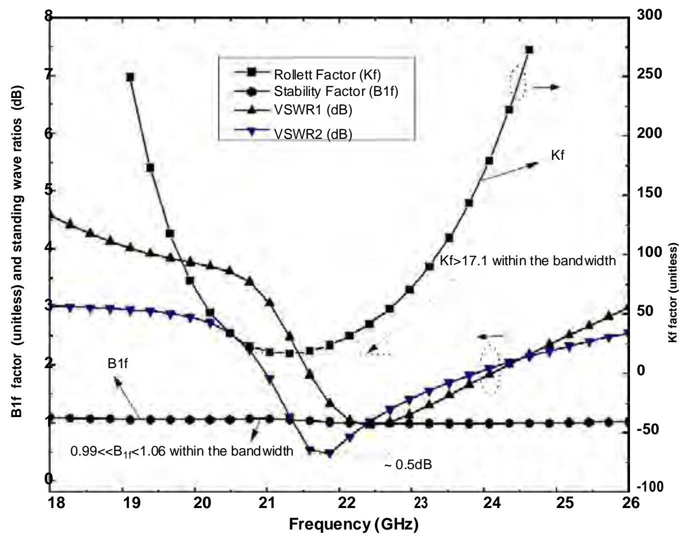


Fig. 5.18: K_f and B_{1f} factors and standing wave ratios.

matching provided by bias path elements, its noise-figure remains below 3.1 dB and NF curve coincides with plot of NF_{min} near the center frequency.

Return-Loss at Ports: Imaginary and real components of the circuit's input

impedance are adjusted with interfacing passives, an input LCL branch, and device sizing while an output stage and a coupling capacitor regulate the load port. After optimization, minimum return-loss (S_{11}) settles to -19.2 dB near 22.3 GHz for RF_{in}. In comparison, peak S_{22} for output port is -26.1 dB at 21.7 GHz. In addition, S_{11} registers results better than -7 dB over a bandwidth of 18.7-28.2 GHz and loss represented by S_{22} is <-10 dB for a coverage of 19.8-27.6 GHz. Over the 3-dB bandwidth, domain values of S_{11} and S_{22} are <-8 dB and <-11 dB, respectively.

Power Gain and Isolation: Power gain for an RF circuit is typically divided in three categories depending on addition of port matching stages with core network. Low estimated reflectance at ports (which is indicative of good matching) leads the three power gain peaks to converge near the operating point in Fig. 5.17 (around 21.6 GHz). Here, available gain (GA) covers a range of >28.1 dB over the 3-dB message bandwidth. In addition, average (GP) and transducer (GT) gain parameters reside in domains which are >28.4 dB and >27.7 dB, respectively. The figure also reports reverse isolation (S_{12}) to be <-62.3 dB, indicating insignificant small-signal leakage.

Stability Factors and Standing Wave Ratio: The condition of Rollett stability demands that K_f factor for the architecture should have a value greater than 1 within its bandwidth [167]. As argued by Fig. 5.18, K_f for the single-supply-driven circuit is >17.1 for bandwidth frequencies. Moreover, the bandwidth defined secondary stability factor (B_{1f}) occupies the range of $0.99 < B_{1f} < 1.06$ and sufficiently fulfills the condition necessary for stable behavior. The amplifier's voltage standing wave ratios (VSWR), when obtained at driving and load ports, approach minima of 1.0 dB and 0.5 dB near the center frequency. The area occupied by the multistage architecture, as estimated from circuit dimensions, is 0.62 mm^2 (without probe pads).

5.4 Comparison of Results

To allow a comparison between the presented single-supply-architecture and available CMOS front-ends, a synopsis of simulated results from millimeter-wave amplifiers [154], [168{173] is prepared in the form of Table 5.1. It shows that the proposed technique may allow a nanoscale amplifier to be driven by a single bias supply whereas number of bias voltages used by the other designs varies between two and six. The presented mechanism helps to avoid the use of extra bias circuits (or gate signals) and keep the power demand below 8 mW. The architecture achieves a relatively at bandwidth noise pro le which varies by only 0.1 dB whereas variation in NF for the other circuits reaches up to 1.4 dB. These results suggest that the presented techniques can allow a high-gain front-end to be powered by a single low-voltage supply (at good gain-per-watt ratings) and may reduce the probability of multiple rail stability affecting circuit variation.

5.5 Conclusions

This chapter presents a multistage CMOS amplifier architecture which reduces the impact of supply variability by allowing the circuit to be powered without separate gate signals. With the employment of a voltage lowering mechanism, the topology is able to use a single voltage rail for all devices of three amplifier stages. The technique is validated through a K-band amplifier on a 90-nm technology platform. The contribution of the individual stages is illustrated separately and the overall design manages high forward gain and 1.7 GHz 3-dB bandwidth (dc current rating for the scaled 0.7-V rail is 10.5 mA). In addition, a gain and port regulation mechanism is realized by the output stage without unduly affecting the circuit's noise performance (NF: 3 dB). Comparison with submicron low-voltage amplifiers shows that the presented schemes manage high-gain behavior

Table 5.1: Comparison of the presented architecture with available amplifiers.

References	[154][a]	[168]	[169]	[170]	[171]	[172]	[173][b]	This Work
No. of Bias Supplies	3	4	2	2	6	4	2	1
Supply Voltage (V)	0.6	1.8	1.8	1.2	1.5	1.2	1.8	0.7
Power (mW)	7.1	20	24	14	25.6	16	10	7.4
Noise Figure (dB)	3.1	3.9	3.5	2.6	3.3	2.7	3.5	3.0
Center Freq. (GHz)	20.5	10	10.2	5	7	8	22.5	21.3
Process (nm)	180	180	180	65	180	90	180	90
Min. S_{11} (dB)	-23	-20	-12.5	-17.5	$<$-30	-32	-50	-19.2
Min. S_{22} (dB)	-24	-22	–	–	-12	-32	–	-26.1
Max. NF (dB)	4.0	5.0	3.5	4.0	3.4	3.7	–	3.1

[a] Estimated from chip data
[b] Estimated from LNA+Mixer data
* With probe pads

with a smaller number of independent supply rails.

Chapter 6

A Ku-band Low-power Amplifier with a Built-in Output Buffer

1.10 Introduction

Silicon CMOS process is often preferred by the communication industry for building reliable high-performance transceiver circuits due to its achievable integration density and low cost [174]. In addition, large bandwidth requirements for wire-less standards are pushing silicon integrated circuits towards higher operating frequencies [175]. For example, the 2.4-5.2 GHz frequency range in S- and C-bands has been heavily used by radio transmitters, which entails drawbacks like higher probability of co-channel interference. To avoid such problems and diversify spectrum usage, concerned authorities like the FCC (Federal Communications Commission, a regulatory body of North America) has advocated research on un-licensed applications exploiting K_u- and K-bands (12-26 GHz) in the microwave range [176{179].

As mentioned in earlier chapters, heterojunction devices can facilitate the process of moving to higher frequencies by offering advantages like better insulation of substrate and high gain [180{182]. Among them, GaAs substrates are robust and can have large diameters whereas InP substrates perform better above S-band. Other benefits of PHEMTs (high electron mobility transistors) and HBTs

(hybrid bipolar transistors) employing compound materials include operation at high/low voltages, high power density, good noise properties, and flexibility of wafer size. On the downside, they still face price constraint and/or performance limitation depending on the choice of substrate [143]. On the other side of the coin, reports on nanoscale CMOS transceiver circuits have shown that features of heterojunction circuits can be replicated to some extent by silicon technology with the help of process scaling and manufacturing techniques. In this respect, the design of silicon low-noise amplifiers (LNA) at high frequencies, which control gain and noise of a receiver front-end, has received attention [183-185]. For exam-ple, [183] presents a 3.1-10.6 GHz amplifier managing 4.5-6.2 dB noise-figure (NF) and 13.2 dB peak gain. In [185], a 2.45 dB (NF) current-reused two-stage amplifier reaches 20 dB gain but its power demand (P_{dc}) is pushed to 26.4 mW. The front-ends proposed in [75], [183], [185] have NF and P_{dc} ranges of 2.45-6.2 dB and 23-28.8 mW, respectively. These low-power C, K_u, and K-band amplifiers can be critical components for a variety of applications including gigahertz range wireless communication, space-based radar arrays (used in the stratosphere), and multi-media services (for wireless local area networks) [185]. However, it still remains a challenging job to achieve simultaneous improvement in the amplifier's forward gain, overall NF, power demand, linearization, and port impedance matching. Therefore, a number of trade-o s have to be considered during the design phase to balance out different design objectives for the amplifier. For example, despite an increase in P_{dc}, signal measurement from circuit ports can be facilitated if an output Buffer can be integrated with the amplifier.

In this chapter, a K_u-band low-NF (3.25 dB) high forward gain amplifier designed with a 0.09- m CMOS process is presented. The amplifier has two cascaded gain stages and an integrated output Buffer (with a current source). Its input common-gate stage and load-port source-follower are optimized to improve

the front-end's port matching, gain, and linearity without unduly degrading the noise contribution. The amplifier is suitable for satellite applications and spends 7.69 mA current from a 1.2-V supply. In addition, matching provided by output Buffer and input CG stage makes the reflection-losses lower than -10 dB at both ports. It is expected that the inclusion of the input and the output stages would assist the circuit's port reflectance to remain within reasonable limits against process variation factors. With the help of a low-cost silicon technology, the architecture manages reasonable performance-to-power ratio when compared with reported amplifiers. The chapter is organized as follows. Section 6.2 explains the presented circuit and its utilization of input-output blocks with explication of performance improvement and equivalent circuits. The results are discussed in Section 6.3 and Section 6.4 compares the circuit with examples from literature. The discussions are concluded in Section 6.5.

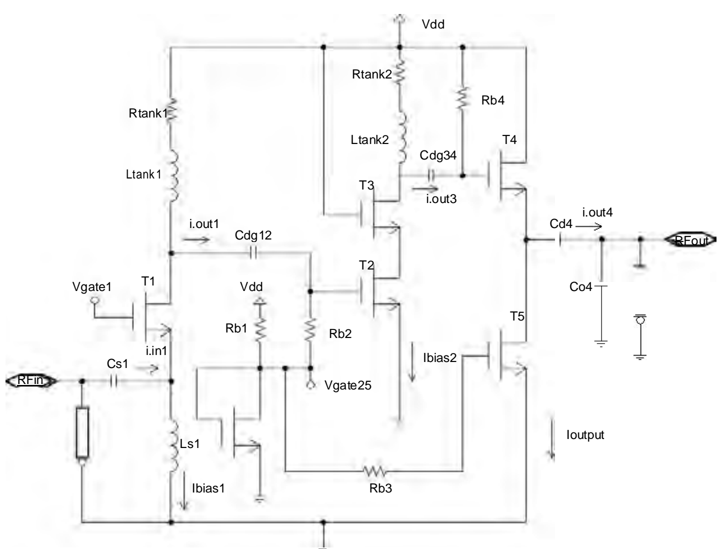


Fig. 6.1: The 1.2-V low-power two-stage amplifier with bias and output circuits.

2.7 Multistage Circuit Configuration

The 1.2-V two-stage (CG-CSCG) amplifier topology with an output Buffer for matching the loading effect is presented in Fig. 6.1. A multistage CMOS amplifier typically employs a common-source (CS) block as the input stage in order to minimize the noise contribution of the front-end. However, for the presented architecture, a common-gate (CG) block is selected to perform the task of matching at input port as it remains relatively stable in the face of PVT variation and extends the upper limit of input power for which the circuit behaves in a linear manner [186]. Therefore, the input stage is implemented through a CG transistor in saturation (T_1) and the following stage (a CSCG block) is realized with two stacked devices (T_2, T_3). Finally, the built-in output circuit, which enhances the front-end's gain and stability and interfaces its load port with the subsequent section, takes the form of a Buffer (built on T_4) and its current is controlled through an active source (formed by T_5).

2.2.8 Input CG Stage

The input common-gate block of the circuit is intended to allow impedance match-ing over a wide range of frequencies. The impedance of this input transistor can be approximated as

$$Z_{in.T_1} = \frac{1}{g_{m.T_1} + j\omega c_{gs.T_1}} \quad (6.1)$$

where $c_{gs:T1}$ is the parasitic contribution of the input transistor which influences the design's matching performance. It is matched with a degenerating inductor while the size of input device adjusts the transconductance $g_{m:T1}$. This process assists the removal of third-order distortion components from the output signal through the common-gate stage. Moreover, the front-end may be adapted into a narrowband amplifier if provision of multiband feedback is allowed with the input

section [187]. In this case, the input CG block manages to achieve a K_u-band noise-figure below 3 dB without extra noise cancelation circuits. A simplified noise factor of this stage, which becomes applicable after the input is matched to the desired characteristic impedance, takes the form of [188]

$$NF_{in} = 1 + \frac{\gamma_1}{\alpha_1} + \frac{4R_{s1}}{R_{d.T_1}} \quad (6.2)$$

where R_{s1} is the source resistance (which precedes the amplifier) and $R_{d:T1}$ is the equivalent load resistance seen by drain terminal of the input transistor. On the other hand, $_1$ is a channel thermal-noise coefficient and $_1$ is a process-dependent factor which usually has a value less than 1. The tuning inductor of the input stage and the input impedance of the following block are adjusted so as to settle

$R_{d:T1}$ to a value which will improve the amplifier's noise performance. At the same time, the load tank is set to allow the center frequency of the front-end to be located in the K_u-band. Consequently, the input CG device offers a relatively low input impedance whereas a CS input block introduces a higher impedance and needs to be matched by extra circuits. Because the gate-drain parasitic element is not in play for the input stage, its reverse isolation is also improved. The capacitor C_{s1} in conjunction with the gate-source parasite of the front device provides matching with the expected impedance (offered by a preceding circuit). In addition, an inductor (L_{s1}) is added at the source of the input device to adjust the impedance seen at higher operating frequencies. C_{s1} also couples the driving signal received at RF_{in} with the input device and L_{s1} influences the stage's noise-figure through noise matching. The operating frequency of the amplifier is placed near 14 GHz with the inductor L_{tank1} forming a resonance bank with the linking capacitor C_{dg12} (placed between the two stages) and parasitic elements of the input device. As loss inducing spiral inductors will typically be used for L_{tank1}, its resistive parasite is represented by R_{tank1} (which may also affect the quality factor of the

reactance). The input transistor is relatively small in size (50 m) and biased with a gate voltage (V_{gate1}) which results in a 3.24 mA core current (I_{bias1}). If $R_{spar:T1}$ represents the parasitic resistance connected with the source terminal of T_1 and is a gate-noise coefficient [183], a more well-defined process-dependent noise factor of the input stage may be expressed as

$$NF_{T_1} = 1 + \frac{\gamma_1}{\alpha_1}\left(\frac{R_{spar.T_1} g^2_{gate.T_1}}{g_{m.T_1}} + \frac{1}{g_{m.T_1} R_{spar.T_1}} + \frac{2g_{gate.T_1}}{g_{m.T_1}}\right) + \delta g_{gate.T_1} R_{spar.T_1} \tag{6.3}$$

where α_1 may be defined by the ratio of $g_{m.T_1}$ to drain-source conductance at zero drain bias voltage ($g_{d0.T_1}$)

$$\alpha_1 = \frac{g_{m.T_1}}{g_{d0.T_1}}. \tag{6.4}$$

In equation (6.3), gate conductance of the input device (ggate:T1) is determined from its parasitic elements:

$$g_{gate.T_1} = \frac{c^2_{gs.T_1}\omega^2}{5g_{d0.T_1}}. \tag{6.5}$$

These expressions indicate how the common-gate stage controls the extent of in-put matching and noise-response at the concerned frequencies. Alternatively, if a common-source stage were used at the input, it would typically have employed a reactive series-shunt circuit (LC ladder) for matching the driving port. As a result, the extent of power transfer would have been a strong function of parasitic elements contributed by the input transistor. By replacing the CS block with a common-gate stage, the parasites associated with the gate terminal are incorporated in the resonating tank, thus making it easier to limit their degrading effects. The CG block in a cascaded structure is also expected to improve the range of linear operation and provide stability against impedance mismatch to a certain extent. To illustrate these effects, the input CG amplifier and the

secondary CSCG block have been analyzed with necessary matching and tuning components on a 90-nm platform. Fig. 6.2(a) shows the range of linearity achieved by the two stages individually in terms of third-order intermodulation product. The maximum limit of input power for the first stage without moving into a non-linear region is wider than the ceiling for the second stage. Stabilization of impedance mismatch is reflected in the wideband matching achieved by the input amplifier stage, as shown in Fig. 6.2(b). Its input reflection-loss (IRL, S_{11}) remains lower than -9 dB for a wide spectrum. On the other hand, IRL for the secondary CSCG block proves to be better than -2.5 dB for a smaller bandwidth. Ultimately, simultaneous power and noise matching are needed for the cascaded amplifier despite a limitation on the lower limit of noise factor imposed by the input stage's transconductance and channel thermal-noise coefficient [174]. This would be evident if the results show that the amplifier's noise-figure is minimized near the center point (~14 GHz) and power matching limits its reflectance near the same frequency.

2.8 Secondary CSCG Stage

The second stage of the amplifier is realized by stacking a CG transistor T_3 (20 m) on top of a CS device T_2 (60 m) to form a cascode block which provides the overall front-end with adequate gain in the concerned range. The CSCG topology is selected to improve the amplifier's frequency response and the degree of isolation between ports. Moreover, the relative noise contribution of the CG device is managed by controlling its gate width and bias current which regulate the channel noise for the transistors. The topology also reduces Miller effect of its input transistor and secures enhanced port isolation to ensure that input and output matching can be done independently by passive networks. At the same time, the insulating transistor offers a relatively high output impedance

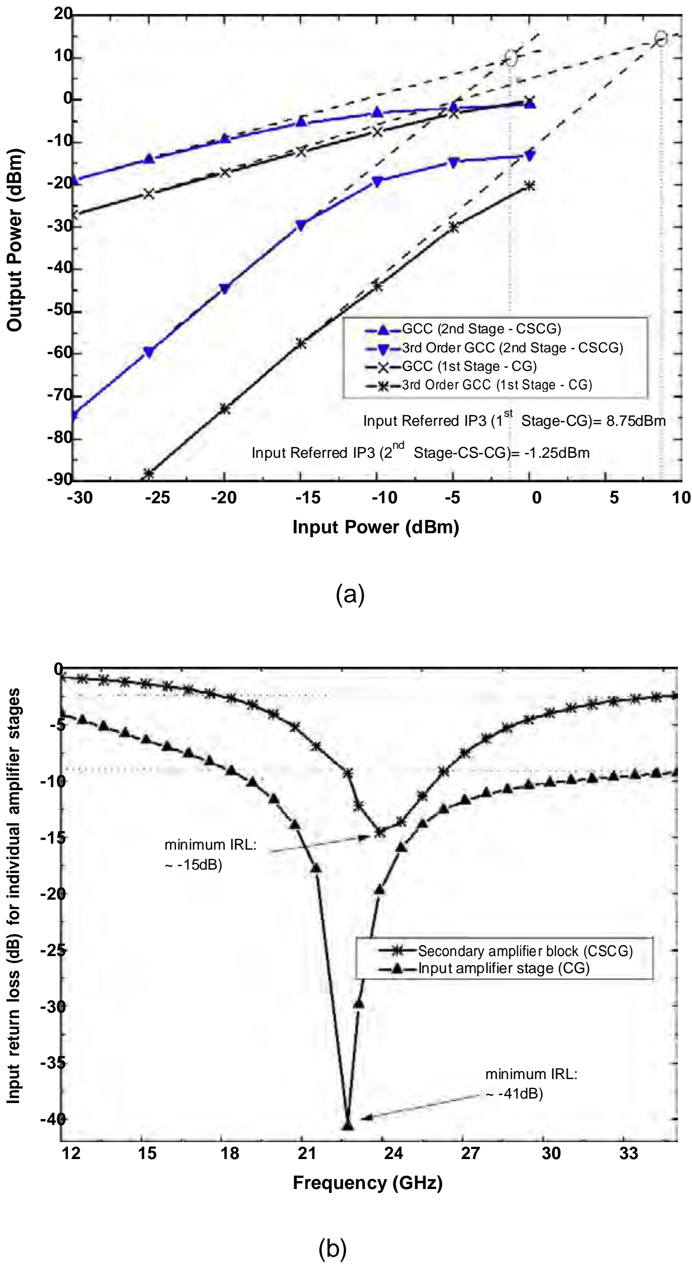


Fig. 6.2: Relative effect of the input CG block and the secondary CSCG stage on a) linear amplifier operation (GCC: gain compression curve) and b) impedance matching (input return-loss)

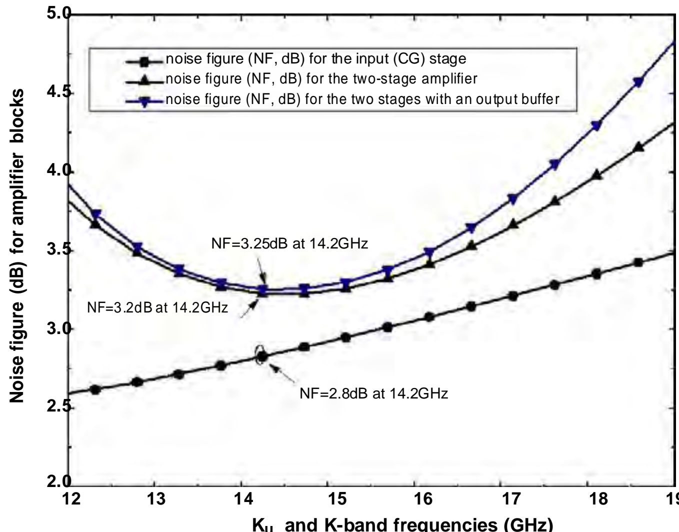


Fig. 6.3: Noise contribution of different stages of the 1.2-V amplifier.

at its drain terminal. The absence of inductive source-degeneration means that gain degradation is minimized for the amplifier stage while interstage matching is achieved with linking capacitors and device parasites. To achieve a relatively at bandwidth over the frequencies of interest (K_u-band), the second stage is designed with its peak gain frequency at a higher spectrum as compared to the input CG block. With that objective, parallel resonance between tank inductor of the input stage and associated parasites maximizes its gain over 10-12 GHz. On the other hand, load of the second stage and adjoining parasites perform a similar function over the domain of 13-15 Ghz. Finally, the reactive elements placed in between the stages are adjusted to center the gain in the upper portion of K_u-band. At the same time, the second stage is optimized to bring down the noise factor of the overall amplifier by limiting its own noise contribution. As shown with simulated noise performances in Fig. 6.3, NF of the input (CG) stage is 2.8 dB near the center point (14.2 GHz) and the noise ceiling is pushed up to 3.25 dB after the addition of the second block and the output Buffer. This

Buffer is expected to drive the load capacitance and also assist measurement of signals at the output port. A bias device (T_{dc}) supplies the gate voltage for the output source which, along with the source transistor, ultimately controls the third branch current. Here, R_{b3} serves as the insulating resistor for the gate of the current source. The capacitor C_{d4} couples the output excitation with the load port (RF_{out}) and forms an output circuit (along with the capacitor C_{o4}). T_{dc} also provides the gate voltage for the second stage's driving transistor where R_{b2} serves as another insulating resistor. In contrast, R_{b1} controls the current for T_{dc} which has a design value of 0.28 mA. This bias arrangement helps to reduce the number of external supplies needed for the amplifier circuit. The inductor L_{tank2} resonates with parasitic and linking elements present at drain and gate of T_3 and T_4, respectively, and tunes the second stage. In addition, the tank uses a small series element R_{tank2} apart from the inductor's parasitic contributions. The bias current for the second stage is 2.58 mA (which is lower than I_{bias1} for the input CG block) and C_{dg34} couples the CSCG section with the following source-follower. If $g_{d0:T3}$ represents the drain-source conductance of T_3 at zero drain bias voltage, $R_{spar:T2}$ is the resistance seen at the source of T_2, and Υ_{T3} is a factor defined by bias voltages of T_3, noise factor of the CSCG stage can be expressed as [189]

$$NF_{T_{2-3}} \approx (\gamma_{T_3} g_{d0.T_3} R_{spar.T_2})(\frac{\omega}{\omega_T})^4 (1 + \frac{\omega_T L_{s2}}{R_{spar.T_2}})^2 \qquad (6.6)$$

where $_T$ is the stage's transit frequency. In this expression, the reactive contribution will be reduced if a source inductor is absent in the second amplifier stage. Using these definitions, a composite noise factor for the amplifier can be derived with the help of equations (6.3) and (6.6).

Apart from improving the degree of port-isolation, the CSCG stage also boosts the stability of the LNA in the concerned range of frequencies. However, a common problem for the CSCG circuit is its noise contribution at higher frequencies

resulting from the existence of parasitic elements at cascade node. That aspect is managed by device sizing, interstage matching, and careful selection of process elements in the resonating tank, which bring down the minimum noise-figure for the overall amplifier. Additionally, the gain is bolstered by the second circuit near the center point with respect to the contribution of the input (CG) stage. Meanwhile, sufficient gain provided by the amplifier's first stage ensures that the effect of noise accumulated in the second stage remains limited.

3.5 Output Buffer

The Buffer employed in the amplifier, if properly calibrated, may help to drive output testing equipments for the load port. Moreover, in a wireless transceiver, a low-noise amplifier is usually followed by a processing block and the Buffer helps to interface the loading effect of this component. It is designed with a branch current (I_{output}) of 1.61 mA provided by the current source. Apart from the two core stage ratings, this branch current serves as the third determining factor for the circuit's power dissipation. It is selected so as to match the expected output impedance without going over the 10 mW limit for overall power. In order to minimize reflection-loss, the target for S_{22} is set around -20 dB at 14 GHz. The magnitude of I_{output} is controlled by sizing the source device when it has a fixed gate voltage. In addition, the parasitic capacitance of the Buffer transistor becomes a part of the load circuit for the amplifier. In the next step, the contribution of the output circuit to overall gain and noise performance is analyzed by studying the amplifier's simulated performance before and after the inclusion of this circuit. It is observed that the load stage is able to significantly influence the design's power gain, port matching, and Rollet stability while adding about 1.9 mW to P_{dc} and 0.1 dB to noise-figure. To be precise, it improves peak power gain by up to 9.8 dB in the 14-15 GHz range and increases base value of Rollet (K_f) factor from

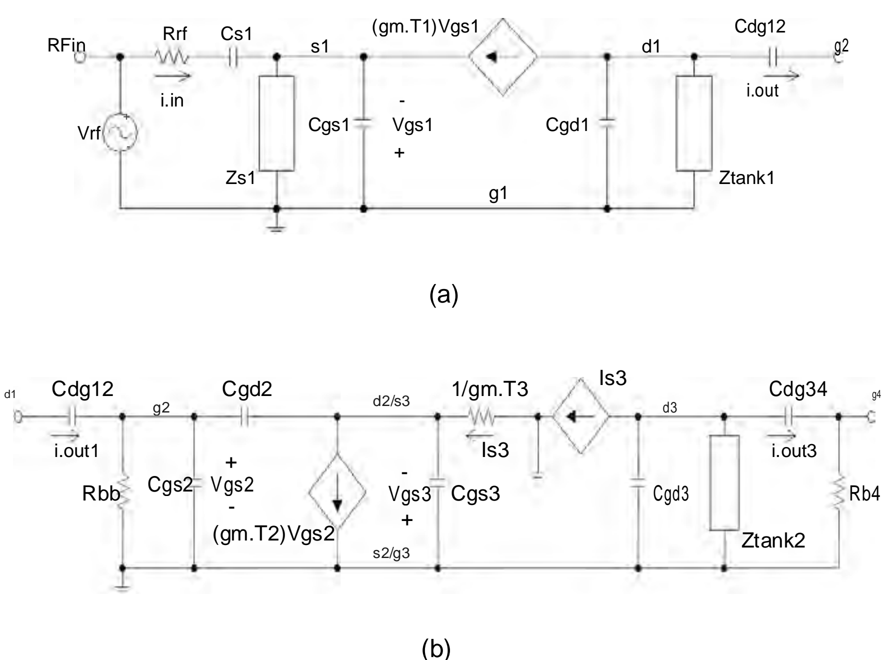


Fig. 6.4: Small signal equivalent circuits for a) input CG stage and b) secondary CSCG stage.

7.9 to 9.7 in the K_u-band. As the output stage is specifically expected to match the following impedance, it is important to study its effect on output return-loss (ORL) which covers a range of -10.3 -22.5 dB after the circuit's inclusion (previously, the range was <-2.3 dB). However, the load circuit degrades input matching to some extent as the input return-loss (IRL) is slightly increased over the bandwidth. The improvement in maximum reverse isolation is about 1.6 dB near the center frequency but insulation is enhanced by a greater amount (up to 16 dB) over the widened frequency coverage of 10-19 GHz.

5 Small Signal Equivalent Circuits

The small signal equivalent circuit for the input (CG) stage of the core amplifier is shown in Fig. 6.4(a) including high-frequency parasitic elements contributed

by the transistor. Here, R_{rf} is the impedance offered by the source which delivers driving current to the amplifier (i_{in1}). The input return-loss for the amplifier is determined by matching between Z_{s1}, C_{s1}, and C_{gs1} (parasite of T_1). On the other hand, the center point is set by a resonance tank at the CG output, which is dominated by the inductor L_{tank1}. Other direct and virtual elements of the tank are C_{gd1} (contributed by T_1), C_{dg12} (linking capacitor), and C_{stage2} (offered by the following stage). Additional transistor parasitic elements are excluded from this circuit to simplify the analysis. Here, V_{gs1} is the driving signal of the CG stage and $g_{m:T1}$ is the input transistor's transconductance. In the figure, the approximate equivalent impedance seen by C_{gd1} takes the form of

$$Z_{C_{gd1}} \approx Z_{tank1} \parallel (\frac{1}{j\omega C_{dg12}} + R_{bb}) \tag{6.7}$$

where Z_{tank1} is the high-frequency impedance offered by the CG load. In addition, the Thevnin's impedance presented to C_{gs1} can be written as

$$Z_{C_{gs1}} = (R_{rf} + \frac{1}{j\omega C_{s1}}) \parallel Z_{s1} \parallel \frac{1}{g_{m.T_1}} \tag{6.8}$$

where Zs1 is contributed by Ls1 and gm:T1 is offered by the active device in the equivalent circuit. Ultimately, gain and corner frequency of the first CG stage will depend on $Z(C_{gs1})$, $Z(C_{gd1})$, and associated parasitic elements. Therefore, the input corner frequency may be expressed as [190]

$$f_{cg} \approx \frac{1}{2\pi[R_{C_{gd1}} C_{gd1} + R_{C_{gs1}} C_{gs1}]} \tag{6.9}$$

where R_{Cgd1} and R_{Cgs1} represent Thevnin's equivalent resistance obtained from impedance functions. Fig. 6.4(b) presents the high-frequency equivalent circuit for the second (CSCG) stage of the core amplifier which forms a stacked configuration. For the CS block (formed by T_2), R_{bb} models the effect of the bias resistors. The stacked CG block (implemented by T_3 or transconductance $g_{m:T3}$)

is represented by a current controlled current source. In this case, the impedance Z_{tank2} incorporates the contribution of the second tank elements. In the figure, C_{gs2} is expected to see a Thevnin's resistance which has contributions from R_{bb}. On the other hand, the resistance seen by the capacitor C_{gd2} (=R_{gd2}) can be approximated with the formula

$$R_{gd2} = (1 + R_{d2} g_{m.T_2}) R_{bb} + R_{d2} \tag{6.10}$$

where R_{d2} is the total resistance seen by the drain of T_2, which also dominates the Thevnin's resistance (R_{gs3}) faced by the parasite C_{gs3}. Now, the impedance presented to C_{gd3} can be estimated as

$$Z_{C_{gd3}} \approx (R_{b4} + \frac{1}{j\omega C_{dg34}}) \parallel Z_{tank2} \tag{6.11}$$

where R_{b4} is the Buffer input resistance. Consequently, the expression of corner frequency for the second CSCG stage is written as

$$f_{cascode} \approx \frac{1}{2\pi[R_{bb}C_{gs2} + R_{gd2}C_{gd2} + R_{d2}C_{gs3} + R_{C_{gd3}}C_{gd3}}]. \tag{6.12}$$

After cascading the two core stages of the amplifier, the built-in output block is expected to facilitate the testing phase of the design by driving measuring equipments. Alternatively, it matches the load port to the characteristic impedance of the following receiver block. During the process, the overall power requirement for the design remains below 10 mW. Finally, a detailed diagram of the presented amplifier which includes expected parasitic elements of silicon components is presented in Fig. 6.5.

3.4.6 Results with Discussion

The design objectives of the presented amplifier are selected on the basis of trends in CMOS low-noise front-ends. As the topology is based on a two-stage Buffered

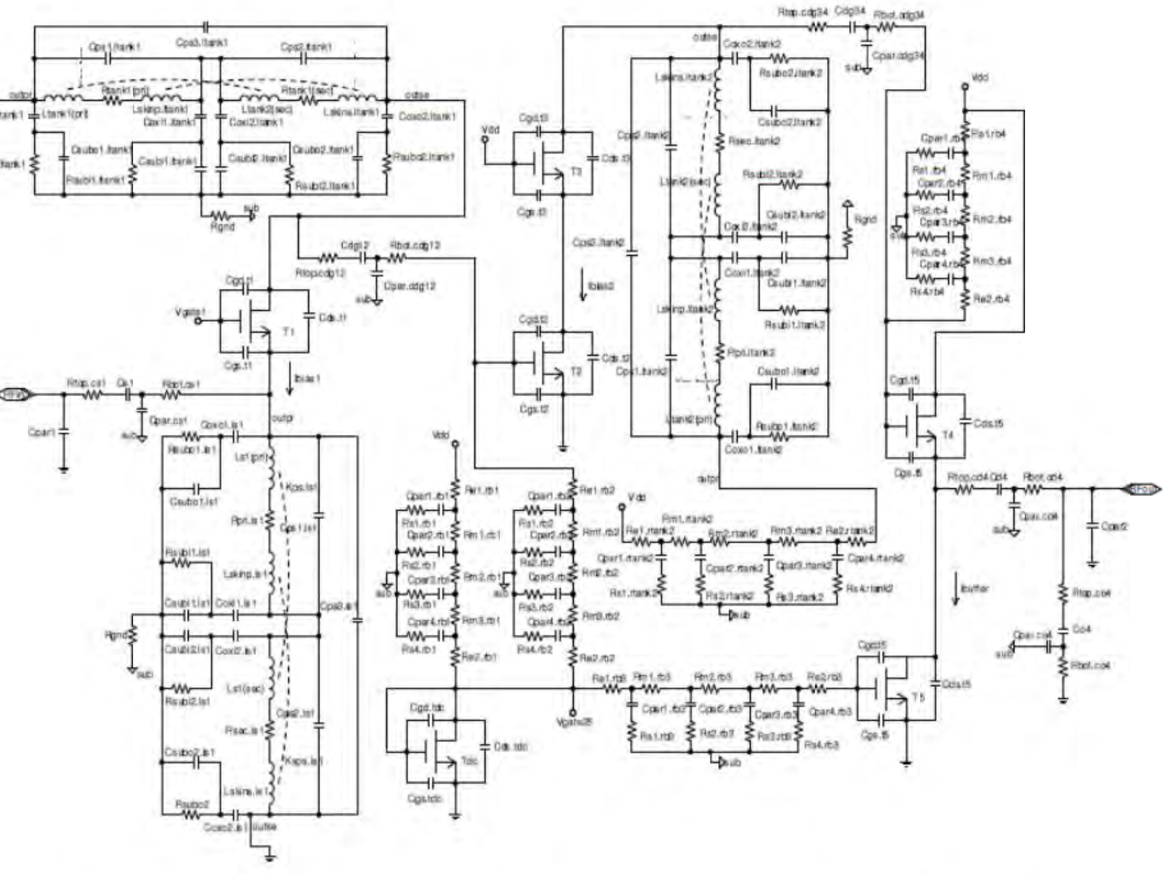


Fig. 6.5: The amplifier architecture with parasitic elements generated by CMOS components.

amplifier, power dissipation limit for the design is set around 10 mW. Port matching is expected to be better than -10 dB over the bandwidth and the noise-figure ceiling is set at 4 dB. The gate voltages are expected to be kept below 1-V and the bias currents are carefully selected for CG and CSCG stages. The proposed circuit is simulated with a 90-nm silicon process and satisfies the design criteria after process optimization is performed.

Process Optimization: In the presented architecture, the sizing of the input stage is governed by bias current and noise/matching considerations at port RF_{in}. The crucial matching component of the first (CG) stage is the inductor L_{s1}, as it regulates port impedance and controls noise-figure through its pull over forward gain. When the design range for L_{s1} is selected as 0.39-2 nH, minimum input return-loss (S_{11}) remains better than -25 dB for smaller values of the range. In addition, if L_{s1} remains within 0.64-1 nH, noise contribution of the first stage is minimized within the desired range. However, for larger source reactance, NF starts to rise sharply as the operating frequency becomes higher. Another reactive

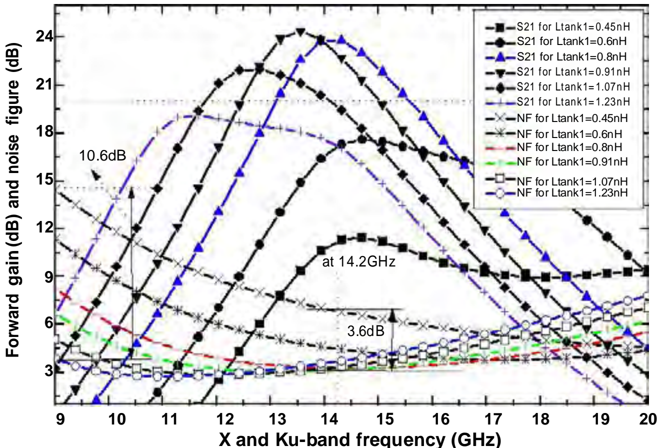


Fig. 6.6: The effect of the first resonating inductor on noise contribution and forward gain.

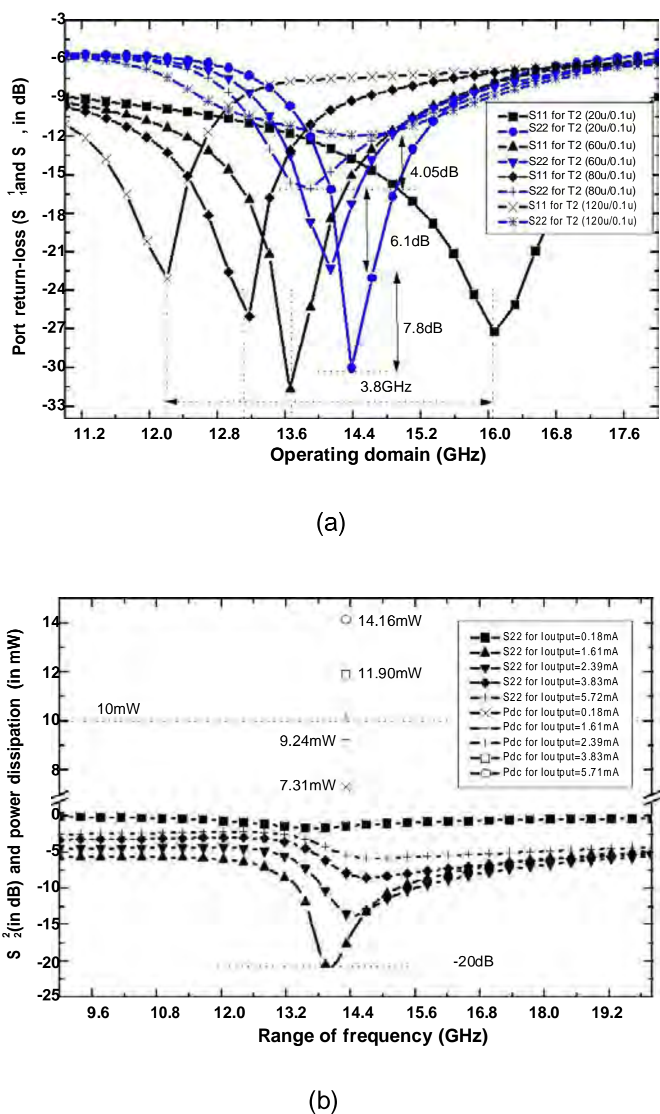


Fig. 6.7: a) The dependence of port reflection on device size and b) selection of output current on the basis of power requirement.

element which directly influences the CG stage's noise share and operating bandwidth is the resonating inductor L_{tank1} (its influence on amplifier performance is shown in Fig. 6.6). Peak forward gain (S_{21}) crosses 20 dB in the vicinity of 14 GHz for a narrow range of its design values. For smaller reactance, the bandwidth

starts to flatten out and the noise level reaches up to 14 dB for X- and K_u-band frequencies (9-16 GHz). Other reactive elements attached to the input stage also take part in controlling the input reflection-loss. In the second circuit, the size of

T_2 contributes to the determination of effective transconductance for the CSCG stage. At the same time, it is able to manipulate the amount of port reflectance. As presented in Fig. 6.7(a), there is a sharp movement in the peak frequency of S_{11} curves against variable dimensions of this device. For the same variable, peak return-loss lowers down without any rapid change in the peak frequency of

S_{22} plots. Therefore, an optimum device ratio may lead the two sets of figures to converge around 14-GHz where their reflectance will be minimized. As already mentioned, apart from core bias currents, output current is also a determining factor for the circuit's overall dissipation. Fig. 6.7(b) plots the power expended by the amplifier and its port return-loss for variable output currents. While min-imizing the port reflectance, the parameter is kept at a level which keeps the design's power requirement below 10 mW. Like the mentioned instances, other amplifier components are optimized in a similar fashion and overall results are summarized in the next section.

Forward Gain and Reverse Insulation: The voltage gain provided by the multistage low-noise amplifier is presented in Fig. 6.8. It attains a peak near 13.9 GHz and follows the pattern of scattering parameters representing small signal forward gain (S_{21}). Initially, the common-gate (CG) input stage alone is only able to manage moderate gain. However, after adding the secondary stage with an output section, peak S_{21} manages better pro les near the lower edge of K_u-band (14.2 GHz). Here, the 3-dB bandwidth for the amplifier extends from 13.2 to 15.4 GHz. To achieve these patterns, a source inductor has been included with the input stage but the same has been excluded from the secondary block. Additionally, the CSCG block is expected to provide significant resistance against

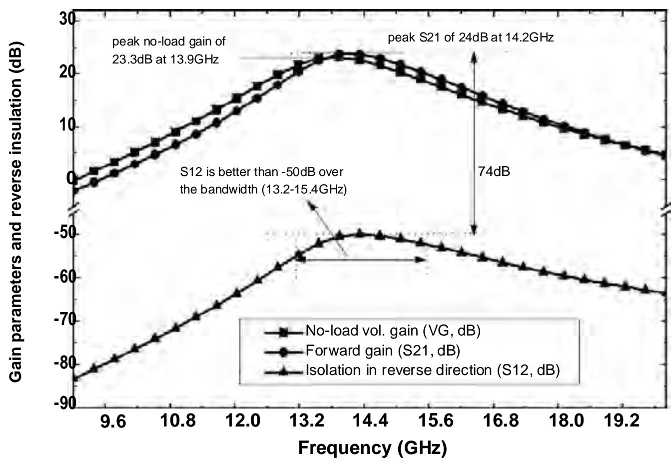


Fig. 6.8: Gain and reverse leakage for the amplifier.

reverse signal leakage for the LNA. Therefore, bandwidth limited reverse insulation (S_{12}), also plotted in Fig. 6.8, resides in the range of -50 -57 dB with its peak position coinciding with the amplifier's center frequency.

Port-reflection and Standing Wave Ratio: It is desirable that signal loss due to reflectance at amplifier ports is minimized for a microwave amplifier with port matching circuits. For this design, the matching networks are implemented through sizing of devices, appending an LC circuit to the RF_{in} port (L_{s1} and C_{s1}), intermediate passives, and connecting a double capacitive circuit at the output (C_{d4} and C_{o4}). Fig. 6.9 shows that reflection-loss at the input port (IRL) is <-10 dB over a 3.8 GHz bandwidth spanning between 11.4 and 15.2 GHz. On the other hand, output-port reflection-loss (ORL) is smaller than -10 dB over a narrower range of frequencies (13.3-15.2 GHz). As expected, the voltage standing wave ratios (VSWR) at amplifier ports are minimized near the peak position of reflection-loss curves. The minima of $VSWR_1$ and $VSWR_2$ are estimated to be 0.05 dB at 13.7 GHz and 0.09 dB at 14.2 GHz, respectively. Similarly, the troughs for IRL and ORL are located at frequencies of 13.7 and 14.1 GHz, in that order.

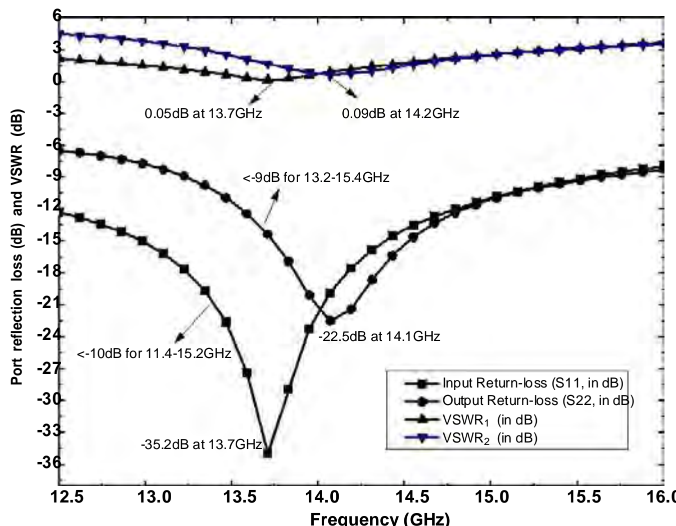


Fig. 6.9: Optimized port return-loss and standing wave ratios.

On the other hand, the reflectance at peak gain frequency is -17.6 and -21.5 dB at input and load ports.

Noise and Stability Factors: After a number of process considerations (which are necessary for port-matching and gain-bandwidth adjustment) are addressed for the amplifier, stable (oscillation-free) behavior at operating frequencies emerges as a design concern. And for a microwave amplifier, expected stability may be estimated with the help of the Rollet factor (K_f), a term which is defined with scattering parameters [167]:

$$K_f = \frac{1 + |S_{22}S_{11} - S_{21}S_{12}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} \tag{6.13}$$

$$K_f > 1 \; over \; bandwidth \; (for \; stability). \tag{6.14}$$

Additionally, a secondary factor (B_{1f}) can be defined with the same terms which may also serve as an indicator of the absence of spurious signal components in the produced signal:

$$B_{1f} = 1 - |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{22}|^2 + |S_{11}|^2. \tag{6.15}$$

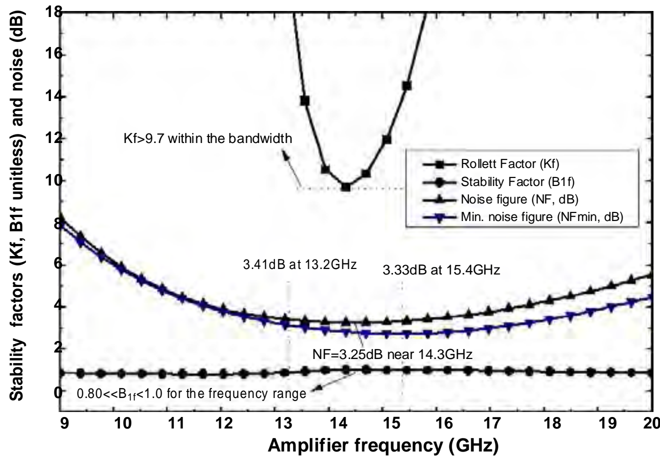


Fig. 6.10: Degree of stability and noise for the amplifier.

For the presented low-noise amplifier, $K_f > 9$ and $0.8 < B_{1f} < 1$ over the utilized spectrum of 13.2-15.4 GHz (see Fig. 6.10). In addition, simultaneous power and noise matching are provided by the reactive elements in the K_u-band, while bias current ratings are carefully selected to lower down the noise ceiling. As a result, noise-figure for the amplifier stays within 3.25-3.41 dB over its message band-width. At the same time, noise parameter at the amplifier's peak gain frequency is predicted to be 3.26 dB. The area expected to be covered by the amplifier (without measuring bond-pads) is 0.196 mm^2, as estimated from component dimensions.

4.6 Performance Comparison

The 1.2-V nanoscale circuit is compared with the performance of reported mil-limeter wave amplifiers in Table 6.1 where a summary of simulated results [75], [191{195] is documented. To evaluate designs built on different scales of the sil-icon CMOS process, a composite figure of merit parameter (FM_1) is calculated

Table 6.1: Comparative performance of submicron amplifiers.

Ref.	Center Freq. (GHz)	Power (mW)	Center S_{11} (dB)	Center S_{22} (dB)	Peak Gain (dB)	NF (dB)	Supply (V)	Core area (mm^2)	FM_1
This Work	14.2	9.2	-17.6	-21.5	24	3.25	1.2	0.196	11.3
[75]	24[2]	29	-15.5[2]	–	29[2]	3.5[1]	1.8	1.32[2*]	6.86
[191]	5.6	6.3	<-15	<-10	20	2.7	1.8	–	6.58
[192]	9.5	13.9	<-8.7	<-10.9	13.1	2.7	1.8	–	3.32
[193]	23	7.2	<-12	–	11	3.9	1.8	0.128	9.01
[194]	23.5	12.6	<-12	<-15	12.5	4.5	0.8	0.385	5.11
[195]	5.7	17.2	-36	<-21.2	20.7	3.08	1.8	–	2.23

[*] Including probe pads
[1] Estimated from NF of front-end
[2] For entire front-end

for the circuits and included in the table:

$$FM_1 = \frac{S_{21}(dB)\ Freq.(GHz)}{Power(mW)\ NF(dB)}. \quad (6.16)$$

5.2.8 Conclusions

A two-stage (CG-CSCG) K_u-band CMOS amplifier is presented in this chapter with a load port stage providing gain boosting and matching. The contribution of the input CG stage in improving the amplifier's reflection-loss and linear behavior and that of the output block with respect to improving overall stability (without high power penalty) are explained. When analyzed with a 90-nm silicon process, isolation between the ports remains high (better than -50 dB) and minimum NF becomes 3.25 dB. Wideband matching achieves low input/output return-loss (IRL/ORL) for the amplifier (-10 -35 dB and -9 -23 dB, respectively). Simulated results are compared against other CMOS front-ends and the port circuits of the multistage architecture are expected to improve its ability of regulating matching parameters.

Chapter 7

Conclusions

1.11 Summary

In this thesis, a discrete modeling technique of low-noise complementary metal oxide semiconductor amplifier circuits comprising active/passive components and bias/gate supplies is presented. The scheme minimizes number of required autonomous parameters by symmetric modeling and simplifies model expressions by exploiting interdependency of equivalent circuit components which lower their computational cost. The formulae can be scaled with feature size of RLC and transistor elements and incorporate parasites generated from silicon considerations. The models have been tested with two 90-nm low-power amplifier topologies where modeled results (NF, gain) achieve errors lower than 3.5%. Analytical scalable equations capable of device characterization are formulated with the help of geometry scalable empirical modeling for CMOS elements (inductors, devices, capacitors, and resistors) needed in a nanoscale transceiver architecture.

The thesis also proposes a low-power reliability improving circuit (RIC) which can significantly enhance the consistency of amplifier performance against process and system variation. As RIC and amplifier sections are powered from a common voltage rail, it enables the overall single-supply

circuit to avoid additional supplies. It supports low and typical voltage ratings of the 90-nm platform and achieves peak regulation for the CS architecture. Microwave performance reliability with and without RIC are analyzed over a wide frequency range in terms forward gain, NF, return-loss, NF_{min}, and voltage gain.

In addition, the technique is tested as a stabilizing gate circuit to improve fidelity of harmonic oscillators. Analytical modeling of oscillator stability is provided to explain how the current regulation scheme can improve process consistency. The mechanism is able to compensate against the effects of a wide range of phenomena (related with manufacturing, physical, and operating variables) including hot carriers, device aging, feature variation, and supply uncertainty. The scheme is verified with two different architectures (single-ended and differential) of modified Hartley oscillators (phase noise: -112 -115 dBc/Hz at f=0.1 MHz). The results indicate that the technique significantly reduces sensitivity of key oscillator parameters to process and system deviation.

Additionally, a three-stage amplifier architecture with reduced probability of multiple supply variation affecting circuit behavior is presented (it curtails the number of required bias supplies). It includes a branching circuit for voltage lowering and realizes a gain regulation mechanism with a control voltage. Cascading of sectioned common-source-gate blocks lowers the topology's power demand while improving its port isolation. Comparison with submicron amplifiers shows that the proposed architecture manages low-voltage and high-gain behavior with reduced supply requirements. The ability of an output circuit and an input common-gate stage of regulating port matching of a multistage amplifier is also discussed.

2.9 Suggestions for Future Work

The reliability improving techniques sponsored in this dissertation are dependent on stabilization of voltage conditions in the circuit through the manipulation of appended networks which sometimes requires independent biasing of substrates. These choices still leave room for alternatives concerning simultaneous reduction of variation in performance determining figures and substrate requirements. Rather than depending on an all-analog realization of the receiver front-end, digital blocks could be incorporated in the structure to improve its tolerance to noise which is expected to enhance its noise figure reliability. Inclusion of digital RIT sections also create the opportunity to introduce settling techniques like employment of reconfigurable architectures for self-detection of unacceptable variation, allowing self-calibration for mixed signal circuits, and using digitally switchable networks against varying process conditions. In addition, emphasis may be pro-vided on the correct detection of degrading process-voltage-temperature deviation with the help of separate sensor networks in the circuits. More investigation may be performed on analog stability enhancement schemes using optimization of de-vice sizing and development of process tolerant core architectures. The thesis attempted to address supply reliability through the design of topologies which limit the number of required independent supplies. It may be explored if the same effect can be achieved by appending deviation-tolerant sections to conventional multiple voltage driven structures. The reliability analyses may also be carried out with the inclusion of layouts in the design. For the modeling section, in addition to front-end amplifiers, discrete modeling schemes may be tried out for the estimation of parameters of back-end circuits which may require a different range of passive components. It assumes that the simplicity of the expressions would reduce the computational cost for the analyzer where a more structured

analysis of modeling efficiency could be developed. It may also be useful to characterize the relative merits and limitations of contiguous and discrete prediction techniques.

Bibliography

3.6 P. Bahl, A. Hassan, Method for wireless capability discovery and protocol negotiation, and wireless device including same, U.S. Patent 6,957,086, issued Oct. 18, 2005.

3.7 P. Zhang, S. J. Lee et al., CMOS RF IC design challenges, in Proc. 7th Int. Conf. on Solid-State and Integrated Circuits Tech. (ICSICT), pp. 1276-1281, 2004.

3.8 B. Matinpour et al., K-band receiver front-ends in a GaAs metamorphic HEMT process, IEEE Trans. Microwave Theory Techniques, vol. 49, no. 12, Dec. 2001, pp. 2459-2463.

3.9 Semiconductor Industry Association, International Technology Roadmap for Semiconductors (ITRS), 2003.

3.10 K. M. Ho, D. Shin, G. M. Rebeiz, X-band phased array development on te on laminates with CMOS RFIC receivers, in Proc. Int. Symp. on Antennas and Propagation, pp. 565-568, 2011.

3.11 S. Lee, S. Sim, S. Hong, A CMOS Ultra-wideband radar transmitter with pulsed oscillator, in Proc. IEEE Radio Frequency Integrated Circuits Symp., pp. 509-512, 2010.

6 A. Levi, Towards Quantum Engineering, Proceedings of the IEEE, vol. 96, no. 2, Feb. 2008, pp. 335-342.

7 G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. van Langevelde, G. D. J. Smit, A. J. Scholten, D. B. M. Klaassen, PSP: An advanced surface-potential-based MOSFET model for circuit simulation, IEEE Trans. Electron Devices, vol. 53, no. 9, Sep. 2006, pp.1979-1993.

8 C. Popa, Tunable CMOS resistor circuit with improved linearity based on the arithmetical mean computation, in Proc. 15th Mediterranean Electrotechnical Conf., pp. 1379-1382, 2010.

9 C. Popa, A new FGMOS active resistor with improved linearity and increased frequency response, in Proc. IEEE Conf. Microelectronics, Electronics and Electronic Tech., pp. 84-87, 2006.

10 J. E. Barth, K. Bernstein, E. H. Cannon, F. R. White, Deep trench capacitor for SOI CMOS devices for soft error immunity, U.S. Patent 7,989,865, issued Aug. 2, 2011.

11 E. Hourdakis, A. G. Nassiopoulou, High performance MIM capacitor using anodic alumina dielectric, Microelectronic Engineering, vol. 90, 2012, pp. 12-14.

12 T. H. Phung, P. Steinmann, R. Wise, Y.-C. Yeo, C. Zhu, Modeling the Negative Quadratic VCC of in MIM Capacitor, IEEE Electron Device Lett., vol. 32, no. 12, 2011, pp. 1671-1673.

13 S.-S. Song, J. Han, M. Je, K. Han, H. Shin, RF Modeling of an MOS Varactor and MIM Capacitor in 0.18- m CMOS Technology, J. Korean Physical Society, vol. 41, no. 6, Dec. 2002, pp. 922-926.

3.4.7 C. P. Yue, S. S. Wong, Physical modeling of spiral inductors on silicon, IEEE Trans. Electron Devices, vol. 47, no. 3, Oct. 2000, pp. 560-568.

3.4.8 J. Sieiro et al., A physical frequency-dependent compact model for RF in-tegrated inductors, IEEE Trans. Microwave Theory Techniques, vol. 50, Jan. 2002, pp. 384-392.

3.4.9 A. Nieuwoudt, M. McCorquodale, R. Borno, Y. Massoud, Accurate analyti-cal spiral inductor modeling techniques for e cient design space exploration, IEEE Electron Device Lett., vol. 27, no. 12, Dec. 2006, pp. 998-1001.

3.4.10 M. Miura-Mattausch, H. Ueno, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, T. Kage, S. Miyamoto, MOSFET modeling for RF-CMOS design, in Proc. Asia and South Paci c Design Automation Conf., pp. 482-490, 2004.

3.4.11 J. Chen, J. J. Liou, On-chip spiral inductors for RF applications: an overview, J. Semiconductor Technology and Science, vol. 4, no. 3, 2004, pp. 149-167.

3.4.12 F. Yuan, CMOS active inductors and transformers: principle, implementa-tion, and applications, Springer Science & Business Media, 2008.

3.4.13 H. Khatri, S. G. Prasad, E. L. Lawrence, Integrated RF interference suppres-sion lter design using bond-wire inductors, IEEE Trans. Microwave Theory Techniques, vol. 56, no. 5, 2008, pp. 1024-1034.

3.4.14 A. Zolfaghari, A. Chan, B. Razavi, Stacked inductors and transformers in CMOS technology, IEEE J. Solid-State Circuits, vol. 36, no. 4, pp. 620-628, Apr. 2001.

3.4.15 Berkeley short-channel insulated-gate FET model [Online], Available: http://www-device.eecs.berkeley.edu/bsim.

4.7 Y. Cheng, M. J. Deen, C. H. Chen, MOSFET modeling for RF IC design, IEEE Trans. Electron Devices, vol. 52, no. 7, pp. 1286-1303, July 2005.

4.8 G. Groeseneken et al., Trends and perspectives for electrical characterization and reliability assessment in advanced CMOS technologies, in Proc. European Solid-State Device Research Conf., pp. 64-72, 2010.

4.9 J.-S. Lee, Improving performance and reliability of MOS devices using deu-terium implantation, Intech Publishers, pp. 15-16, 2010.

4.10 J.-S. Lee, Modeling of time-dependent defect generation during constant voltage stress for thin gate oxide of sub-micron MOSFET, Japan. J. Applied Physics, vol. 47, no. 1, pp. 19-22, 2008.

4.11 T. A. Rost, K. C. Harvey, Method for improving performance and reliability of MOS technologies and data retention characteristics of ash memory cells, U.S. Patent No. 6,221,705, issued 2001.

4.12 K. Kang, S. P. Park, K. Kim, K. Roy, On-chip variability sensor using phase-locked loop for detecting and correcting parametric timing failures, IEEE Trans. Very Large Scale Integration Systems, 2010, vol. 18, no. 2, pp. 270-280.

4.13 C. H. Kim, K. Roy, S. Hsu, R. Krishnamurthy, S. Borkar, A process variation compensating technique with an on-die leakage current sensor for nanometer scale dynamic circuits, IEEE Trans. Very Large Scale Integration Systems, vol. 14, no. 6, pp. 646-649, 2006.

4.14 S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, V. De, Param-eter variations and impact on circuits and microarchitecture, in Proc. 40th Annual Design Automation Conf., 2003, pp. 338-342.

5.2.9 F. Cheng, R. J. Weber, A novel process-variation insensitive network for on-chip impedance matching, in Proc. Int. Symp. on Commun. and Inf. Technol., Oct. 2004, pp. 43-46.

5.2.10 E. Wu, E. Nowak, J. Aitken, W. Abadeer, L. K. Han, S. Lo, Structural de-pendence of dielectric breakdown in ultra-thin gate oxides and its relationship to soft breakdown modes and device failure, in Int. Electron Devices Meeting Tech. Dig., pp. 187-190, 1998.

5.2.11 W.-Z. Chen, T.-Y. Lu, W.-W. Ou, S.-T. Chou, S.-Y. Yang, A 2.4 GHz reference-less receiver for 1 Mbps QPSK demodulation, IEEE Trans. Circuits and Systems I, vol. 59, pp. 505-514, 2012.

5.2.12 B.-W. Min, G. M. Rebeiz, Ka-band SiGe HBT low phase imbalance di er-ential 3-bit variable gain LNA, IEEE Microwave Wireless Component Lett., vol. 18, pp. 272-274, 2008.

5.2.13 Y.-H. Chen, H.-H. Hsieh, L.-H. Lu, A 24-GHz receiver front-end with an LO signal generator in 0.18- m CMOS, IEEE Trans. Microwave Theory Tech-niques, vol. 56, pp. 1043-1051, 2008.

5.2.14 I.-Y. Lee, S.-J. Yun, S.-M. Oh, S.-G. Lee, A low-parasitic and common-centroid cross-coupled CMOS transistor structure for high-frequency VCO design, IEEE Electron Device Lett., vol. 30, pp. 532-534, 2009.

5.2.15 M. Chen, J. Lin, A 0.1-20 GHz low-power self-biased resistive-feedback LNA in 90 nm digital CMOS, IEEE Microwave Wireless Components Lett., vol. 19, pp. 323-325, 2009.

5.4 W. G. Dan, D. Dobberpuhl, Y. L. Allmon, N. L. Rethman, Designing high performance CMOS microprocessors using full custom techniques, in Proc. 34th Design Automation Conf., June 1997, pp. 1-6.

5.5 E. Maricau, G. Gielen, Analog IC reliability in nanometer CMOS, Springer Science & Business Media, 2013.

5.6 P. Solomon, Breakdown in silicon oxide - a review, J. Vacuum Science and Technology, vol. 14, no. 5, 1977, pp. 1122-1130.

5.7 W. Wang, V. Reddy, A. T. Krishnan, R. Vattikonda, S. Krishnan, Y. Cao, Compact modeling and simulation of circuit reliability for 65-nm CMOS technology, IEEE Trans. Device Materials Reliab., vol. 7, no. 4, 2007, pp. 509-517.

5.8 K. Kuhn, C. Kenon, A. Kornfeld, M. Liu, A. Maheshwari, W.-K. Shih, S. Sivakumar, G. Taylor, P. Vander Voorn, K. Zawadzki, Managing process variation in Intels 45 nm CMOS technology, Intel Technology Journal, vol. 12, no. 2, pp. 93-109, Jun. 2008.

5.9 H.-S. Wong, Y. Taur, D. J. Frank, Discrete random dopant distribution e ects in nanometer-scale MOSFETs, Microelectronics and Reliability, vol. 38, no. 9, Sep. 1998, pp. 1447-1456.

5.10 K. J. Kuhn, Reducing variation in advanced logic technologies: Approaches to process and design for manufacturability of nanoscale CMOS, in Proc. Int. Electron Devices Meeting, pp. 471-474, 2007.

5.11 K. R. Lakshmikumar, R. A. Hadaway, M. A. Copeland, Characterization and modeling of mismatch in MOS transistors for precision analogue design, IEEE J. Solid State Circuits, vol. 21, pp. 1057-1066, 1986.

5.5 T. Mizuno, J.-I. Okamura, A. Toriumi, Experimental study of threshold voltage uctuation due to statistical variation of channel dopant number in MOSFETs, IEEE Trans. Electron Devices, vol. 41, pp. 2216-2221, 1994.

5.6 C. A. Mack, Field guide to optical lithography, SPIE Press, Bellingham, WA, 2006.

5.7 S. M. Goodnick, D. K. Ferry, C. W. Wilmsen, Surface roughness at the Si(100)-SiO_2 interface, Physical Review, vol. 32, no. 12, pp. 8171-8182, Dec. 1985.

5.8 A. Asenov, S. Kaya, E ect of oxide interface roughness on the threshold voltage uctuations in decanano MOSFETs with ultrathin gate oxides, in Proc. Int. Conf. Simulation of Semiconductor Processes and Devices, pp. 135-138, 2000.

5.9 M. Koh, W. Mizubayashi, K. Iwamoto, H. Murakami, T. Ono, M. Tsuno, T. Mihara, K. Shibahara, S. Miyazaki, M. Hirose, Limit of gate oxide thickness scaling in MOSFETs due to apparent threshold voltage uctuation induced by tunnel leakage current, IEEE Trans. Electron Devices, vol. 48, no. 2, 2001, pp. 259-264.

5.10 J. H. Stathis, Physical and predictive models of ultrathin oxide reliability in CMOS devices and circuits, IEEE Trans. Device Materials Reliab., vol. 1, no. 1, 2001, pp. 43-59.

5.11 R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, H. E. Maes, A consistent model for the thickness dependence of intrinsic breakdown in ultra-thin oxides, in Int. Electron Devices Meeting Dig., 1995, pp. 866.

5.6 T. Grasser, B. Kaczer, W. Goes, H. Reisinger, T. Aichinger, P. Hehenberger, P-J. Wagner et al., The paradigm shift in understanding the bias temperature instability: from reaction-di usion to switching oxide traps, IEEE Trans. Electron Devices, vol. 58, no. 11, 2011, pp. 3652-3666.

5.7 T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, M. Nelhiebel, A two-stage model for negative bias temperature instability, in Proc. IEEE Int. Reliab. Physics Symp., pp. 33-44, 2009.

5.8 F. D'Agostino, D. Quercia, Short-channel e ects in MOSFETs, Introduction to VLSI design, 2000.

5.9 H. Su, F. Liu, A. Devgan, E. Acar, S. Nassif, Full chip leakage estima-tion considering power supply and temperature variations, in Proc. ACM Int. Symp. Low Power Electronics and Design, pp. 78-83, 2003.

5.10 J. F. Freijedo, J. Semiao, J. J. Rodriguez-Andina, F. Vargas, I. C. Teixeira, J. P. Teixeira, Modeling the e ect of process, power-supply voltage and tem-perature variations on the timing response of nanometer digital circuits, J. Electronic Testing, vol. 28, no. 4, 2012, pp. 421-434.

5.11 H. Iwai, RF CMOS Technology, in Proc. Asia-Paci c Radio Science Conf., pp. 296-298, 2004.

5.12 Q. Zou, K. Ma, K. S. Yeo, W. M. Lim, Design of a Ku-band low-phase-noise VCO using the dual LC tanks, IEEE Trans. Circuits and Systems II, vol. 59, no. 5, pp. 262-266, May 2012.

5.13 P.-Z. Rao, T.-Y. Chang, C.-P. Liang, S.-J. Chung, An ultrawideband high-linearity CMOS mixer with new wideband active baluns, IEEE Trans. Mi-crowave Theory Techniques, vol. 57, pp. 2184-2192, 2009.

[62] P. H. Woerlee, M. J. Knitel, R. Langevelde et al., RF-CMOS performance trends, IEEE Trans. Electron Devices, vol. 48, no. 8, pp. 1776-1782, Aug. 2001.

[63] L. F. Tiemeijer, R. J. Havens, R. de Kort et al., Record RF performance of standard 90 nm CMOS technology, in Very Large Scale Int. Cir. Symp. Tech. Dig., 2004, pp. 441-444.

[64] T. Grasser, Advanced Device Modeling and Simulation, Singapore: World Scienti c, 2003.

[65] N. Arora, Mosfet Modeling for VLSI Simulation: Theory And Practice, Sin-gapore: World Scienti c, 2007.

[66] S.-S. Song, J. Han, M. Je, K. Han, H. Shin, RF Modeling of an MOS Var-actor and MIM Capacitor in 0.18- m CMOS Technology, J. Korean Physical Society, vol. 41, no. 6, pp. 922-926, Dec. 2002.

[67] J. Mondal, An experimental veri cation of a simple distributed model of MIM capacitors for MMIC applications, IEEE Trans. Microwave Theory Tech-niques, vol. 34, no. 4, pp. 403-408, April 1987.

[68] D. A. Chan, CMOS power device modeling and ampli er circuits, PhD Dis-sertation, Dept. Elect. Comp. Eng., U. Illinois Urbana-Champaign, Urbana IL, 2010.

[69] M. Miura-Mattausch, H. Ueno, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, T. Kage, S. Miyamoto, MOSFET modeling for RF-CMOS design, in Proc. Asia and South Paci c Design Automation Conf. (ASP-DAC), pp. 482-490, Jan. 2004.

[70] A. Nieuwoudt, M. McCorquodale, R. Borno, Y. Massoud, Accurate analytical spiral inductor modeling techniques for e cient design space exploration, IEEE Electron Device Lett., vol. 27, no. 12, pp. 998-1001, Dec. 2006.

[71] S. Mohan, M. del Mar Hershenson, S. Boyd, T. Lee, Simple accurate expres-sions for planar spiral inductances, IEEE J. Solid-State Circuits, vol. 34, no. 10, pp. 1419-1424, Oct. 1999.

[72] D. Linten, S. Thijs, M. Natarajan, P. Wambacq, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Donnay, S. Decoutere, A 5-GHz fully integrated ESD-protected low-noise ampli er in 90-nm RF CMOS, IEEE J. Solid-State Cir-cuits, vol. 40, no. 7, pp. 1434-1442, Jul. 2005.

[73] X. Z. Xiong, V. F. Fusco, A comparison study of EM and physical equivalent circuit modeling for MIM CMOS capacitors, Microwave and Optical Technology Letters, vol. 34, no. 3, pp. 177-181, Aug. 2002.

[74] IBM 90-nm CMOS Process.

[75] Y.-H. Chen, H.-H. Hsieh, L.-H. Lu, A 24-GHz receiver front-end with an LO signal generator in 0.18- m CMOS, IEEE Trans. Microwave Theory Tech-niques, vol. 56, no. 5, pp. 1043-1051, May 2008.

[76] Y.-C. Chen, C. H. Wang, Y.-S. Lin, Low-power 24 GHz CMOS receiver front-end using isolation enhancement technique for automatic radar systems, Microwave and Optical Technology Letters, vol. 54, no. 6, pp. 1471-1476, Jan. 2012.

[77] Y. Terry, M. Gordon, K. Yau, M. Yang, S. Voinigescu, 60-GHz PA and LNA in 90-nm RF-CMOS, in Proc. IEEE Radio Frequency Integrated Circuits Symp., pp.11-13, Jun. 2006.

[78] M. Okushima, J. Borremans, D. Linten, G. Groeseneken, A DC-to-22 GHz 8.4mW compact dual-feedback wideband LNA, in Proc. IEEE Radio Fre-quency Integrated Circuits Symp., pp. 295-298, Jun. 2009.

[79] M. Huang, J.-H. Tsai, T.-W. Huang, A 917- W Q-band transformer-feedback current-reused LNA using 90-nm CMOS technology, in IEEE MTT-S Int. Microwave Symp. Digest, pp. 1-3, Jun. 2012.

[80] P. E. Allen, D. Holberg, CMOS Analog Circuit Design, Elsevier, 2011.

[81] A. Hastings, The art of analog design, New Jersey: Prentice Hall, 2001.

[82] P. R. Gray, P. J. Hurst, R. G. Meyer, S. H. Lewis, Analysis and Design of Analog Integrated Circuits, New York: Wiley, 2001.

[83] D. K. Shae er, T. H. Lee, A 1.5-V 1.5-GHz CMOS low noise ampli er, IEEE J. Solid-State Circuits, vol. 32, no. 5, pp. 745-759, May 1997.

[84] T. Nigam, CMOS reliability: From discrete device degradation to circuit aging, in Proc. Int. Symp. VLSI Design, Automation, and Test, April 2013, pp. 1.

[85] M. White, Scaled CMOS reliability and considerations for spacecraft sys-tems: Bottom-up and top-down perspectives, in Proc. Int. Reliab. Physics Symp., April 2012, pp. 4B-4.1-4.5.

[86] M. Ruberto, O. Degani, S. Wail, A. Tendler, A. Fridman, G. Goltman, A reliability-aware RF power ampli er design for CMOS radio chip integration, in Proc. Int. Reliab. Physics Symp., April-May 2008, pp. 536-540.

[87] P. Andrei, L. Oniciuc, Suppressing random dopant-induced uctuations of threshold voltages in semiconductor devices, J. Applied Physics, vol. 104, no. 10, pp. 104508-104510, Nov. 2008.

[88] N. C.-C. Lu, J. M. Sung, Reverse short-channel e ects on threshold voltage in submicrometer salicide devices, IEEE Electron Device Lett., vol. 10, no. 10, pp. 446-448, Oct. 1989.

[89] M. Orshansky, S. Nassif, D. Boning, Design for manufacturability and sta-tistical design: a constructive approach. New York: Springer, 2008.

[90] G. Zhang, M. S. Mora, R. Farrell, A built-in-test circuit for functional ver-i cation & PVT variations monitoring of CMOS RF circuits, in Proc. IET Irish Signals and Systems Conf., June 2006, pp. 217-222.

[91] R. Arora, K. A. Moen, A. Madan, J. D. Cressler, E. X. Zhang, D. M. Fleet-wood, R. D. Schrimpf, A. K. Sutton, H. M. Nayfeh, Impact of body tie and source/drain contact spacing on the hot carrier reliability of 45-nm RF-CMOS, Int. Integrated Reliab. Workshop Final Report, Oct. 2010, pp. 56-60.

[92] C. Ma, H. J. Mattausch, M. Miyake, T. Iizuka, M. Miura-Mattausch, K. Mat-suzawa, S. Yamaguchi, Compact reliability model for degradation of advanced p-MOSFETs due to NBTI and hot-carrier e ects in the circuit simulation, in Proc. Int. Reliab. Physics Symp., April 2013, pp. 2A.3.1-2A.3.6.

[93] J. Fang, S. S. Sapatnekar, Incorporating hot-carrier injection e ects into timing analysis for large circuits, IEEE Trans. Very Large Scale Integrated Systems, vol. 99, no. 1, Jan. 2014.

[94] J. S. Yuan, E. Kritchanchai, Power ampli er resilient design for process, voltage, and temperature variations, Microelectronics Reliab., vol. 53, no. 6, pp. 856-860, 2013.

[95] S. Yonghoon, S. Lee, E. Cho, J. Lee, S. Nam, A CMOS Class-E power ampli- er with voltage stress relief and enhanced e ciency, IEEE Trans. Microwave Theory Techniques, vol. 58, no. 2, pp. 310-317, 2010.

[96] N. Drego, A. Chandrakasan, D. Boning, Lack of spatial correlation in MOS- FET threshold voltage variation and implications for voltage scaling, IEEE Trans. Semiconductor Manufacturing, vol. 22, no. 2, pp. 245-255, May 2009.

[97] Y. Liu, J.-S. Yuan, CMOS RF low-noise ampli er design for variability and reliability, IEEE Trans. Device Materials Reliab., vol. 11, no. 3, pp. 450-457, Sep. 2011.

[98] C. Yike, B. Chi, M. Liu, Y. Zhang, Y. Li, Z. Wang, Process variation com- pensation of a 2.4 GHz LNA in 0.18 um CMOS using digitally switchable capacitance, in Proc. Int. Symp. Circuits Systems, May 2007, pp. 2562-2565.

[99] J. Karthik, Q. Khan, B. Chi, W. Beattie, Z. Wang, P. Chiang, A self- healing 2.4 GHz LNA with on-chip S_{11}/S_{21} measurement/calibration for in-situ PVT compensation, in Proc. IEEE Radio Frequency Integrated Circuits Symp., May 2010, pp. 311-314.

[100] M. Y. Mukadam, O. G. Filho, Z. Xuan, A. B. Apsel, Process variation compensation of a 4.6 GHz LNA in 65nm CMOS, in Proc. Int. Symp. Circuits Systems, May-June 2010, pp. 2490-2493.

[101] Y. Wu, C. Shi, M. Ismail, H. Olsson, Temperature compensation design for a 2.4GHz CMOS low noise ampli er, in Proc. Int. Symp. Circuits Systems (ISCAS), May 2000, pp. 323-326.

[102] Q. Dong, F. Sheng, L. Ran, X. Renzhong, Y. Ting, H. Zhiliang, A current-steering self-calibration 14-bit 100-MSPs DAC, Journal of Semiconductors, vol. 31, no. 12, pp. 125007-(1-5), Dec. 2010.

[103] H. Abrishami, S. Hatami, B. Amelifard, M. Pedram, NBTI-aware ip- op characterization and design, in Proc. ACM Great Lakes Symp. on Very Large Scale Int. Cir., 2008, pp. 29-34.

[104] J. Scholvin, D. R. Greenberg, J. A. Del Alamo, RF power potential of 90 nm CMOS: device options, performance, and reliability, in Int. Electron Devices Meeting Tech. Dig., Dec. 2004, pp. 455-458.

[105] F. Schwierz, RF transistors: Performance trends versus IRTS targets, in Proc. 6th Int. Caribbean Conf. Devices, Circuits and Systems, April 2006, pp. 195-200.

[106] L. Chang, Y.-K. Choi, D. Ha, P. Ranade, S. Xiong, J. Bokor, C. Hu, T.-J. King, Extremely scaled silicon nano-CMOS devices, Proc. IEEE, vol. 91, no. 11, pp. 1860-1873, Nov. 2003.

[107] Y. Taur, T. Ning, Fundamentals of Modern VLSI Devices, Cambridge Uni-versity Press: UK, 2002.

[108] S. Markov, L. Gerrer, F. Adamu-Lema, S. Amoroso, A. Asenov, Time domain simulation of statistical variability and oxide degradation including trapping/detrapping dynamics, in Proc. Int. Conf. Simulation of Semicond. Processes and Devices, pp. 157-160, Sep. 2012.

[109] A. Asenov, A. R. Brown, J. H. Davies, S. Kaya, G. Slavcheva, Simulation of intrinsic parameter uctuations in decananometer and nanometer-scale MOS-FETs, IEEE Trans. Electron Devices, vol. 50, pp. 1837-1846, 2003.

[110] G. Gielen, P. De Wit, E. Maricau, J. Loeckx, J. Martin-Martinez, B. Kaczer, et al., Emerging yield and reliability challenges in nanometer CMOS technolo-gies, in Proc. Design, Automation and Test in Europe (DATE), pp. 1322-1327, 10-14 Mar. 2008.

[111] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, V. De, Pa-rameter variations and impact on circuits and microarchitecture, in Proc. 40th ACM Design Automation Conf., pp. 338-342, Jun. 2003.

[112] G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy, A. Asenov, Simulation study of individual and combined sources of intrinsic parameter uctuations in conventional nano-MOSFETs, IEEE Trans. Electron Devices, vol. 53, pp. 3063-3071, 2006.

[113] Z. Chen, K. Hess, J. Lee, J. W. Lyding, E. Rosenhaum, I. Kizilyalli, S. Chetlur, R. Huang, On the mechanism for interface trap generation in MOS transistors due to channel hot carrier stressing, IEEE Electron Device Lett., vol. 21, no. 1, pp. 24-26, Jan. 2000.

[114] E. Li, E. Rosenbaum, L. F. Register, J. Tao, P. Fang, Hot carrier induced degradation in deep submicron MOSFETs at 100 C, in Proc. Int. Rel. Phys. Symp., 2000, pp. 103-107.

[115] A. Asenov, S. Kaya, A. R. Brown, Intrinsic parameter uctuations in de-cananometer MOSFETs introduced by gate line edge roughness, IEEE Trans. Electron Devices, vol. 50, no. 5, pp. 1254-1260, 2003.

[116] B. Kaczer, R. Degraeve, M. Rasras, K. Van de Mieroop, P. J. Roussel, G. Groeseneken, Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability, IEEE Trans. Electron Devices, vol. 49, no. 3, pp. 500-506, 2002.

[117] P. Andrei, L. Oniciuc, Suppressing random dopant-induced uctuations of threshold voltages in semiconductor devices, J. Applied Physics, vol. 104, no. 10, pp. 104508-104510, Nov. 2008.

[118] T. Grasser, B. Kaczer, W. Goes, H. Reisinger, T. Aichinger, P. Hehenberger et al., Recent advances in understanding the bias temperature instability, Int. Electron Devices Meeting Tech. Dig., pp. 85-88, 2010.

[119] J. H. Stathis, S. Zafar, The negative bias temperature instability in MOS devices: A review, Microelectron. Reliab., vol. 46, no. 24, pp. 270-286, Feb. 2006.

[120] Y. Ye, S. Gummalla, C.-C. Wang, C. Chakrabarti, Y. Cao, Random variability modeling and its impact on scaled CMOS circuits, J. Comput. Electron., vol. 9, no. 3-4, pp. 108-113, 2010.

[121] T. E. Turner, Design for reliability, in Proc. Int. Phys. Failure Anal., 2006, pp. 257-264.

[122] S. V. Kumar, C. H. Kim, S. S. Sapatnekar, Impact of NBTI on SRAM read stability and design for reliability, in Proc. 7th Int. Symp. Quality Electron Design, 2006, pp. 210-218.

[123] G. Panagopoulos, K. Roy A three-dimensional physical model for Vth vari-ations considering the combined e ect of NBTI and RDF, IEEE Trans. Elec. Dev., vol. 58, pp. 2337-2346, 2011.

6.6 A. Papanikolaou, Reliability issues in deep deep submicron technologies: Time-dependent variability and its impact on embedded system design, in Proc. Int. Conf. Very Large Scale Integration, 2006, pp. 342-347.

6.7 H. Abrishami, S. Hatami, M. Pedram, Multi-corner, energy-delay optimized, NBTI-aware ip- op design, in Proc. Int. Symp. Quality Electronic Design, 2010, pp. 652-659.

6.8 K. Kang, S.P. Park, K. Kim, K. Roy, On-chip variability sensor using phase-locked loop for detecting and correcting parametric timing failures, IEEE Trans. Very Large Scale Integrated Systems, 2010, pp. 270-280.

6.9 D. Bull, S. Das, K. Shivashankar, G. S. Dasika, K. Flautner, D. Blaauw, A power-e cient 32 bit ARM processor using timing-error detection and correction for transient-error tolerance and adaptation to PVT variation, IEEE J. Solid-State Circuits, vol. 46, pp. 18-31, Jan. 2011.

6.10 J. Yuan, S. Chen, A simulation study of Colpitts oscillator reliability and variability, IEEE Trans. Device Materials Reliab., vol. 12, pp. 576-581, Sep. 2012.

6.11 F. Bahmani, T. Serrano-Gotarredona, E. Snchez-Sinencio, An accurate automatic quality factor tuning scheme for second-order LC lters, IEEE Trans. Circuits Systems I, Reg. Papers, vol. 54, no. 4, pp. 745-756, Apr. 2007.

6.12 A. Calimera, E. Macii, M. Poncino, NBTI-aware power gating for concur-rent leakage and aging optimization, in Proc. Int. Symp. Low Power Electron-ics and Design, pp. 127-132, Aug. 2009.

7.3 S.-H. Lee, Y.-H. Chuang, S.-L. Jang, C.-C. Chen, Low-phase noise hartley di erential CMOS voltage controlled oscillator, IEEE Microwave Wireless Components Lett., vol. 17, no. 2, pp. 145-147, Feb. 2007.

7.4 S. R. Ardali, S. G. Samani, B. Arzanifar, Oscillation amplitude analysis of MOS hartley oscillator using a general model, J. Int. Circuits Systems, vol. 6, no. 1, pp. 60-67, 2011.

7.5 A. Demir et al., Phase noise in oscillators: a unifying theory and numerical methods for characterization, IEEE Trans. Circuits Systems I, vol. 47, no. 5, 655-674, May 2000.

7.6 P. Horowitz, H. Win eld, The Art of Electronics, 2nd edition. Cambridge (UK): Cambridge University Press, 1989.

7.7 M. S. McCorquodale, M. K. Ding, R. B. Brown, Study and simulation of CMOS LC oscillator phase noise and jitter, in Proc. IEEE Int. Symp. Circuits Systems, pp. 665-668, 2003.

7.8 J. S. Yuan, E. Kritchanchai, Power ampli er resilient design for process, voltage, and temperature variations, Microelectronics Reliab., vol. 53, no. 6, 856-860, 2013.

7.9 M. Y. Mukadam, O. G. Filho, Z. Xuan, A. B. Apsel, Process variation compensation of a 4.6 GHz LNA in 65nm CMOS, in Proc. IEEE Int. Symp. Circuits Systems, May-June 2010, pp. 2490-2493.

7.10 Y. Wu, C. Shi, M. Ismail, H. Olsson, Temperature compensation design for a 2.4 GHz CMOS low noise ampli er, in Proc. IEEE Int. Symp. Circuits Systems, 2000, pp. 323-326.

[139] T.-K. Nguyen, S.-K. Han, S.-G. Lee, Ultra-low-power 2.4 GHz image-rejection low-noise ampli er, Electronics Letters, vol. 41, no. 15, pp. 842-843, July 2005.

[140] S. Delmas-Bendhia, F. Caignet, E. Sicard, M. Roca, On-chip sampling in CMOS integrated circuits, IEEE Trans. Electromagnetic Compatibility, vol. 41, no. 4, pp. 403-406, Nov. 1999.

[141] H.-H. Hsieh, L.-H. Lu, A CMOS 5-GHz micro-power LNA, in Proc. IEEE Radio Frequency Integrated Circuits Symp., June 2005, pp. 31-34.

[142] M. Horstmann, M. Wiatr, A. Wei, J. Hoentschel, T. Feudel, T. Scheiper, R. Stephan, M. Raab, Advanced SOI CMOS transistor technology for high per-formance microprocessors, Solid-State Electronics, vol. 53, no. 12, pp. 1212-1219, Dec. 2009.

[143] C.-H. Lien, K.-L. Deng, C.-C. Liu, H.-S. Chou, H. Wang, K_a band mono-lithic GaAs PHEMT circuits for transceiver applications, in Proc. IEEE Asia-Paci c Microwave Conference, Dec. 2000, pp. 1171-1174.

[144] J. B. Hacker, J. Bergman, G. Nagy, G. Sullivan, C. Kadow, H.-K. Lin, A. C. Gossard, M. Rodwell, B. Brar, An ultra-low power InAs/AlSb HEMT Ka-band low-noise ampli er, IEEE Microwave Wireless Components Lett., vol. 14, no. 4, pp. 156-158, Apr. 2004.

[145] W. G. Dan, D. Dobberpuhl, Y. L. Allmon, N. L. Rethman, Designing high performance CMOS microprocessors using full custom techniques, in Proc. 34th Design Automation Conf., June 1997, pp. 1-6.

[146] H. Samavati, H. R. Rategh, T. H. Lee, A 5-GHz CMOS wireless LAN receiver front end, IEEE J. Solid-State Circuits, vol. 35, pp. 765-772, May 2000.

[147] H. Darabi, A. A. Abidi, A 4.5-mW 900-MHz CMOS receiver for wireless paging, IEEE J. Solid-State Circuits, vol. 35, pp. 1085-1096, Aug. 2000.

[148] W.-L. Chen, S.-F. Chang, G.-W. Huang, Y.-S. Jean, T.-H. Yeh, A Ku-band interference-rejection CMOS low-noise ampli er using current-reused stacked common-gate topology, IEEE Microwave Wireless Comp. Lett., vol. 17, no. 10, pp. 718-720, Oct. 2007.

[149] E. Monaco, M. Borgarino, F. Svelto, A. Mazzanti, A 5.2 mW Ku-band CMOS injection-locked frequency doubler with di erential input/output, in Proc. of IEEE Custom Integrated Circuits Conf., pp. 61-64, 13-16 Sept. 2009.

[150] X. Guo, K. K. O, A power e cient di erential 20-GHz low noise ampli er with 5.3-GHz 3-dB bandwidth, IEEE Microwave Wireless Comp. Lett., vol. 15, pp. 603-605, Sept. 2005.

[151] J. Jin, S. Hsu, A 0.18 m CMOS balanced ampli er for 24-GHz applications, IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 440-445, Feb. 2008.

[152] K.-W. Yu, Y.-L. Lu, D.-C. Chang, V. Liang, M. F. Chang, K-band low-noise ampli ers using 0.18 m CMOS technology, IEEE Microwave Wireless Comp. Lett., vol. 14, pp. 106-108, March 2004.

[153] S.-C. Shin, M.-D. Tsai, R.-C. Liu, K.-Y. Lin, H. Wang, A 24-GHz 3.9-dB NF low-noise ampli er using 0.18 m CMOS technology, IEEE Microwave Wireless Comp. Lett., vol. 15, no. 7, pp. 448-450, July 2005.

[154] T.-P. Wang, A low-voltage low-power K-band CMOS LNA using dc current-path split technology, IEEE Microwave Wireless Comp. Lett., vol. 20, no. 9, pp. 519-521, Sept. 2010.

[155] Y. Cao, V. Issakov, M. Tiebout, A 2 kV ESD-protected 18 GHz LNA with 4 dB NF in 0.13 m CMOS, in Int. Solid-State Circuit Conf. Tech. Dig., Feb. 2008, pp. 194-195.

[156] E. Adabi, B. Heydari, M. Bohsali, A. M. Niknejad, 30 GHz CMOS low noise ampli er, in Proc. IEEE Radio Frequency Integrated Circuits Symp., 2007, pp. 625-628.

[157] C. C. Chen, H. Y. Yang, Y. S. Lin, A 21-27 GHz CMOS wideband LNA with gain and group-delay using standard 0.18 m CMOS technology, in Proc. Radio Wireless Symp., 2009, pp. 586-589.

[158] J. F. Yeh, C. Y. Yang, H. C. Kuo, H. R. Chuang, A 24 GHz transformer-based single-in di erential-out CMOS low-noise ampli er, in Proc. IEEE Ra-dio Frequency Integrated Circuits Symp., 2009, pp. 299-302.

[159] A. Sayag, S. Levin, D. Regev, D. Z ra, S. Shapira, D. Goren, D. Ritter, A 25 GHz 3.3 dB NF low noise ampli er based upon slow wave transmission lines and the 0.18 m CMOS, in Proc. IEEE Radio Frequency Integrated Circuits Symp., 2008, pp. 373-376.

[160] M. Khanpour, K. W. Tang, P. Garcia, S. P. Voinigescu, A wideband W-band receiver front-end in 65-nm CMOS, IEEE J. Solid-State Circuits, vol. 43, no. 8, pp. 1717-1730, Aug. 2008.

[161] S. Iversen, The e ect of feedback on noise gure, Proc. IEEE, vol. 63, no. 3, pp. 540-542, Mar. 1975.

[162] W. Guo, D. Huang, The noise and linearity optimization for a 1.9-GHz CMOS low noise ampli er, in Proc. IEEE Asia-Paci c Conf., Aug. 2002, pp. 253-257.

[163] T. H. Lee, The Design of CMOS Radio Frequency Integrated Circuits, Cam-bridge Univ. Press, Cambridge, U.K., 1998.

[164] R.-M. Weng, M,-L. Fan, M.-J. Zeng, A 5.9mW full-band low-noise-ampli er for ultra-wideband systems, in Proc. IEEE Int. Symp. Circuits and Systems, pp. 1931-1934, May 2012.

[165] R. Spencer, M. Ghausi, Introduction to Electronic Circuit Design, First Ed., Pearson Education Inc., 2003.

[166] D. J. Comer, D. T. Comer, Fundamentals of Electronic Circuit Design, First Ed., John Wiley & Sons, New York, 2003.

[167] B. Leung, VLSI for Wireless Communication, First Ed., Prentice Hall India, New Delhi, 2002.

[168] C.-F. Liao, S.-I. Liu, A broadband noise-canceling CMOS LNA for 3.1-10.6 GHz UWB receiver, in Proc. Custom Integrated Circuits Conf., pp. 161-164, Sept. 2005.

[169] R. K. Pokharel, A. I. A. Galal, O. Nizhnik, H. Kanaya, K. Yoshida, Design of at gain and low noise gure LNA for 3.1-10.2 GHz band UWB applications in 0.18 m CMOS process, in Proc. IEEJ Int. Workshop on AVLSI, pp. 161-164, 2008.

[170] S. C. Blaakmeer, E. A. Klumperink, B. Nauta, D. W. Leenaerts, An induc-torless wideband balun-LNA in 65 nm CMOS with balanced output, in Proc. European Solid State Circuits Conf., pp. 364-367, Sept. 2007.

[171] H.-I Wu, R. Hu, C. F. Jou, Complementary UWB LNA design using asymmetrical inductive source degeneration, IEEE Microwave Wireless Comp. Lett., vol. 20, no. 7, pp. 402-404, July 2010.

[172] M. M. Reja, K. Moez, I. Filanovsky, An area-e cient multistage 3.0- to 8.5-GHz CMOS UWB LNA using tunable active inductors, IEEE Trans. Circuits and Systems-II, vol. 57, no. 8, pp. 587-591, Aug. 2010.

[173] Y.-C. Chen, C. H. Wang, Y.-S. Lin, Low-power 24 GHz CMOS receiver front-end using isolation enhancement technique for automatic radar systems, Microwave Optical Technology Lett., vol. 54, no. 6, pp. 1471-1476, Jan. 2012.

[174] X. Guan, A. Hajimiri, A 24-GHz CMOS front-end, IEEE J. Solid State Circuits, vol. 39, pp. 368-373, Feb. 2004.

[175] S. Wu, B. Razavi, A 900-MHz/1.8-GHz CMOS receiver for dual band ap-plications, IEEE J. Solid-State Circuits, vol. 33, pp. 2178-2185, Dec. 1998.

[176] W.-L. Chen, S.-F. Chang, K.-M. Chen, G.-W. Huang, J.-C. Chang, Tem-perature e ect on Ku-band current-reused common-gate LNA in 0.13 m CMOS technology, IEEE Trans. Microwave Theory Techniques, vol. 57, no. 9, pp. 2131-2138, Sept. 2009.

[177] C. Cao et al., A 24-GHz transmitter with an on-chip antenna in 130-nm CMOS, in IEEE Very Large Scale Int. Cir. Symp. Tech. Dig., Jun. 2006, pp. 148-149.

[178] A. W. L. Ng et al., A 1-V 24-GHz 17.5-mW phase-locked loop in a 0.18-m CMOS process, IEEE J. Solid-State Circuits, vol. 41, no. 6, pp. 1236-1244, Jun. 2006.

[179] A. Natarajan, A. Komijani, A. Hajimiri, A fully integrated 24-GHz phase-array transmitter in CMOS, IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2502-2514, Dec. 2005.

[180] D. L. Ingram, L. Sjogren, J. Kraus, M. Nishimoto, M. Siddiqui, S. Sing, K. Cha, M. Huang, R. Lai, A highly integrated multi-functional chip set for low cost K_a-band transceiver, in Proc. IEEE Radio Frequency Integrated Circuits Symp., Jun. 1998, pp. 227-230.

[181] Y. Mimino, M. Hirata, K. Nakamura, K. Sakamoto, Y. Aoki, S. Kuroda, High gain-density K-band P-HEMT LNA MMIC for LMDS and satellite com-munication, in IEEE MTT-S Int. Microwave Symp. Dig., vol. 1, Jun. 2000, pp. 17-20.

[182] C. Meliani et al., GaAs HBT low power 24 GHz downconverter with on-chip local-oscillator, in Proc. IEEE European Microwave Integrated Circuits Conf., Sep. 2006, pp. 141-144.

[183] B. Park, S. Choi, S. Hong, A low-noise ampli er with tunable interference rejection for 3.1 to 10.6-GHz UWB systems, IEEE Microwave Wireless Com-ponents Lett., vol. 20, no. 1, pp. 40-42, Jan 2010.

[184] H. I. Wu, R. S. Fan, C. F. Jou, A 0.7-V transformer-feedback CMOS low-noise ampli er for 5GHz wireless LAN, Progress in Electromagnetics Re-search, vol. 3, no. 7, pp. 968-970, May 2007.

[185] C. Y. Cha, S. G. Lee, A 5.2 GHz LNA in 0.35 m CMOS utilizing inter-stage series resonance and optimizing the substrate resistance, in Proc. European Solid-State Circuits Conf., Sep. 2002, pp. 339-342.

[186] X. Li, S. Shekhar, D. J. Allstot, G_m-boosted common-gate LNA and di er-ential colpitts VCO/QVCO in 0.18- m CMOS, IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2609-2619, Dec. 2005.

[187] A. Liscidini, M. Brandolini, D. Sanzogni, R. Castello, A 0.13 m CMOS front-end for DCS1800/UMTS/802.11b-g with multi-band positive feedback low noise ampli er, in Dig. of Tech. Papers IEEE Symp. on Very Large Scale Int. Cir., Jun. 2005, pp. 406-409.

[188] C. F. Liao, S. I. Liu, A Broadband Noise-Canceling CMOS LNA for 3.1-10.6 GHz UWB Receivers, IEEE J. Solid-State Circuits, vol. 42, no. 2, pp. 329-339, Feb. 2007.

[189] W. Guo, D. Huang, The noise and linearity optimization for a 1.9-GHz CMOS low noise ampli er, in Proc. IEEE Asia-Paci c Conf., Aug. 2002, pp. 253-257.

[190] M. H. Rashid, Microelectronic Circuits: Analysis and Design, Second Ed., Cengage Learning, Stamford, 2011.

[191] S. Shekhar, J. S. Walling, S. Aniruddhan, D. J. Allstot, CMOS VCO and LNA using tuned-input tuned-output circuits, IEEE J. Solid State Circuits, vol. 43, no. 3, pp. 1177-1186, May 2008.

[192] Z.-Y. Huang, Y.-T. Hung, C. C. Huang, M. P. Chen, A 0.18 m CMOS current reused low noise ampli er with gain compensation for ultra wideband wireless receiver, in Proc. 23rd Int. Technical Conf. on Circuits Systems, July 2008, pp. 437-440.

[193] Y.-L. Wei, S. H. Hsu, J.-D. Jin, A low-power low-noise ampli er for K-band applications, IEEE Microwave Wireless Components Lett., vol. 19, no. 2, pp. 116-118, Feb. 2009.

[194] J.-D. Jin, S. H. Hsu, A K-band low-noise ampli er in 0.18 m CMOS technology for sub-1V operation, Microwave Optical Technology Letters, vol. 51, no. 9, pp. 2202-2204, Sep. 2009.

[195] H. C. Lai, Y. M. Lin, A low noise gain-variable LNA for 802.11a WLAN, in Proc. IEEE Conf. on Electron Devices and Solid State Circuits, Dec. 2007, pp. 973-976.

List of Publications

1. A. Roy, A.B.M.H. Rashid, \Common-rail powered reliability improving technique for single-supply CMOS ampli ers", IET Circuits, Devices and Systems, Vol. 9, No. 3, pp 141-151, 2015.

2. A. Roy, A.B.M.H. Rashid, \A stabilization technique for single-ended and di erential harmonic oscillators", Springer Circuits, Systems, and Signal Processing, Vol. 34, No. 11, pp 3409-3429, 2015.

3. A. Roy, A.B.M.H. Rashid, \Accurate geometry scalable complementary metal oxide semiconductor modelling of low-power 90 nm ampli er cir-cuits", IET J. of Engineering, Vol. 2014, pp. 1-8, doi: 10.1049/joe.2014.0002.

4. A. Roy, A.B.M.H. Rashid, \\Voltage lowering and gain control techniques for a single-supply-driven 0.7 V ampli er", Taylor-Francis International Jour-nal of Electronics, Vol. 102, No. 9, 1535-1559, 2014.