AN INVESTIGATION INTO SOME

METAL-SILICON SCHOTTKY BARRIER DIODES

BY

MD. SHAMSUL ALAM

A THESIS

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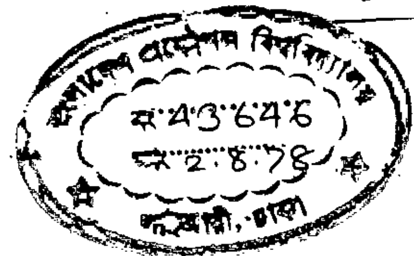

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CERTIFICATE

This is to certify that this work has been done by me and it has not been submitted elsewhere for the award of any degree or diploma. A paper entitled "Barrier Heights and Interface Effects in Silicon Schottky Diodes" was presented at the 3rd Annual Conference of the Association for the Advancement of Science, Bangladesh, held at Chittagong, January, 8-12, 1978.

Countersigned:

21.6.78 21.6.78

(Supervisor) (Signature of the candidate)

Accepted as satisfactory for partial fulfilment of the requirement for the Degree of M.Sc.(Engg.) in Electrical Engineering.

Examiners:

1. (Professor A.M.Patwari) 21.6.78		CHAIRMAN
2. (Professor M.Shamsul Huq) 21.6.78		EXTERNAL MEMBER
3. (Professor A.M.Zahoorul Huq)		MEMBER
4. (Professor Shamsuddin Ahmed) 21.6.78		MEMBER

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ABSTRACT

Schottky barrier diodes are obtained by the contact of a metal to a semiconductor. The barrier height and the ideality parameter are the two parameters which determine the quality of these diodes. Schottky diodes have been fabricated on both n-type and p-type silicon and their physical behaviours have been derived from current-voltage (I-V) and capacitance -voltage (C-V) measurements. Aluminium, silver and gold were used as metal contacts. Also a combination of two metals have been used as metal contact.

Methods have been developed to control the barrier height which is very important because a particular application may need a preset value of barrier height. By heat-treatment, the aluminium n-type silicon barrier height can be increased and aluminium p-type silicon barrier height can be decreased. Silver and gold barriers did not show any significant change in barrier with high-temperature heat-treatment. Also control of barrier height in the higher range was obtained by deposition of aluminium and gold in succession on silicon. Freshly prepared barrier on n-type silicon was higher and on p-type silicon was lower than their known values, which revealed that fixed positive charges were present at metal-semiconductor interface.

The ideality parameter was found to deviate largely from unity. Increased value of ideality parameter was attributed to the thicker interfacial oxide layer. Interface-states density has been calcuated from I-V and C-V data and was found to increase slightly with reverse bias. The normal barrier height values were in the close agreement with results already published.

LIST OF SYMBOLS

Symbol	Meaning
A^{*}	Richardsons Constant, $A/cm^2/{}^oK^2$
A^{**}	Effective Richardsons Constant, $A/cm^2/{}^oK^2$
C	Depletion Layer Capacitance, F/cm^2
D	Diffusion constant, cm^2/sec.
E	Electric field, V/cm.
E_c	Lowest energy level in conduction band, ev.
E_F	Fermi energy, ev.
E_g	Band gap, ev.
E_v	Highest energy level in Valence band, ev.
h	Planck's Constant, 6.624×10^{-34} Joules/sec.
J	Current density, A/cm^2
J_s	Saturation current density, A/cm^2.
I	Current, A.
I_s	Saturation current, A.
K	Boltzman's constant, 8.62×10^{-5} $ev/{}^oK$.
L_p/L_n	Diffusion Length of hole/electron, cm.
m_o	Free electron mass.
m^{*}	Effective mass of electron.
N_D/N_A	Shallow, donor/acceptor impurity, cm^{-3}.
N_D/N_A	Shallow, donor/acceptor impurity, cm^{-3}.
N^{f+}	Fixed positive charge density at the interface, , cm^{-2}.
N_t	Concentration of traps, cm^{-3}.
n	Ideality parameter.
n_i	Intrinsic concentration of semiconductor cm^{-3}.

τ	Minority carrier life-time.
$n_{(x)}$	Electron concentration as a function of x in depletion layer, cm^{-3}.
N_{ss}	Density of surface states, $cm^{-2}\ ev^{-1}$.
N_{sb}	Surface-states equilibrium with silicon, $cm^{-2}\ ev^{-1}$.
N_{sa}	Surface-states equilibrium with metal, $cm^{-2}\ ev^{-1}$.
q	Electronic charge, 1.602×10^{-19} col.
T	Temperature ^oK
V	Applied potential, V .
v_T	Transport velocity, cm/sec.
V_{bio}	Built-in or Diffusion potential at zero applied field, V.
V_{bi}	Built-in-potential, V.
V_n/V_p	Depth of Fermi Level below conduction band (n-type) or above valence-band (p-type), V.
W	Width of depletion layer, cm.
ϵ_s	Permittivity of the semiconductor, f/cm.
ϵ_i	Permittivity of interfacial oxide layer, /cm.
ρ	Charge density, $col./cm^2$.
δ	Thickness of interfacial oxide layer, $^o A$.
ϕ_{Bno}/ϕ_{Bpo}	Zero field barrier height of n-type/p-type semiconductor, V
ϕ_{Bn}/ϕ_{Bp}	Barrier height of n-type/p-type semiconductor, V.
ϕ_o	Energy level at the surface of silicon, v.
$\Delta\phi$	Image Force barrier lowering, V.
ϕ_m	Metal work function, V.
ϕ_g	Band gap, $= E_g/q$, V.
χ	Electron affinity of semiconductor, V.
γ	Minority carrier injection ratio,
μ_n/μ_p	Mobility of electrons/holes.

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CHAPTER - ONE

INTRODUCTION

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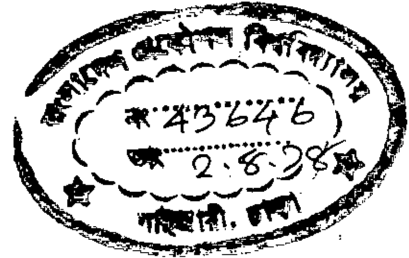


1.1 INTRODUCTION

In recent years much interest has been shown in the study of properties of metal-semiconductor contacts because of its wide field of applications. Metal-Semiconductor contacts can be classified into two groups according to their current-voltage characteristics. Those contacts exhibiting rectifying behaviour are called schottky barrier diodes and those with linear current-voltage characteristics are called ohmic contacts. Schottky barriers are generally obtained by metal contacts on lightly doped semiconductor and the ohmic contacts are achieved by the contact of metal on comparatively heavily-doped semiconductors.

Schottky barrier diodes are found to be useful as devices in electronic applications as well as in the studies of fundamental physical parameters. In such diodes the minority carrier effect is virtually eliminated making it suitable for applications in microwave frequencies. Important information on deep level impurities, impact ionisation co-efficient and band structure in semiconductors can be obtained with the help of Schottky barriers.

Though metal-semiconductor contacts are older than p-n junctions, the development in this field was slow for a long time. However, recent advances in planer technology of ideal contacts renewed great interest in the development of Schottky barriers. At present it is possible to fabricate Schottky barriers with reliable and near-ideal electrical characteristics which are reproducible.

These advantages are widely exploited in integrated circuit processing. Thus it is now cheaper and economical to produce discrete Schottky barrier devices.

The metal-semiconductor contacts are now occupying a major place among the devices used in modern electronic systems. The greatest advantage that it offers is the reduction of storage time due to the absence of minority carriers. This makes it an ideal device for applications in microwave frequencies as switching devices[1], mixers and varactor [2]. Because of its simplicity in processing and excellent noise performance to other devices the aluminium Schottky barrier with oxide overlap has been found to be superior[3] to those of others. In the field-effect transistor it is used as the gate[4]. An important application of Schottky barrier is in integrated circuit where it performs various gating and clamping functions. The reduced forward voltage in this diode results in reduced fan-out along with increased noise immunity[5]. It is also widely used as a collector clamp of n-p-n transistors in order to reduce the switching time[6]. Schottky barriers have also found useful applications in microstrip integrated circuits,[7], Solar cells [8], and in many others as are reported in literature[9],[10], [11], [12].

Barrier height and ideality parameter are the two parameters which determine the quality of Schottky diodes. Theoretically one should be able to obtain a range of barrier heights for various applications by selecting suitable metals and semiconductors having appropriate work functions. However, in practice the presence of the interface states and a thin interfacial layer make the system

less controllable. The fact that these interface parameters cannot be controlled precisely makes the system barrier height and the ideality parameters to deviate from predicted values. So a simple scheme that can control the barrier height to suit a particular application keeping at the same time the ideality parameter very close to unity, is needed to be developed.

1.2 BRIEF LITERATURE REVIEW:

The metal-semiconductor rectifier is known to be the oldest solid-state device used in Electronics. Braun[13] in 1874 first reported the asymmetrical nature of conduction between metal point and crystal like lead sulphide. In 1906 pickard[14] took a patent for silicon point contact rectifier and in 1907 Pierce[15] fabricated diodes by sputtering metals to different semiconductors. The point contact rectifiers were extensively used in early days of radio. In 1931 Wilson[16] formulated the transport theory of semiconductors based on the band theory of solids which was applied to metal- semiconductor contact. But the correct physical model was forwarded by Schottky[17] in 1938 and hence the name Schottky diode. In the same year, Mott[18] devised an appropriate model for swept out metal-semiconductor known as Mott barrier. Bardeen in 1947[19] pointed out the presence of surface states which determined the rectifying property of such devices. Then p-n junction diode was discovered in Bell laboratories and since then almost all the research in the field of semiconductor was directed toward the understanding, fabrication and development of junction devices. In early 1960's research interest started to grow again in the development

of the metal semiconductor contacts as Schottky barrier devices A large number of useful research works has been reported in literature. An up-to-date survey of the more important publications is being presented in this section. The objective and main findings of each of the publications are briefly outlined here in a chronological order.

The Pioneering work in this field was done by Archer and Atalla[20] who obtained the barrier heights of different metals on silicon. In 1962 Macdonald[21] obtained a precise digital-computer solution to the diffusion equation for the idealised one-carrier metal-semiconductor junction problem which was idealised by omitting the effects of traps, image forces, tunnelling, recombination, breakdown phenomenon and hot electrons. He considered a situation similar to that of Wagner[22] and Schottky and Spenke[23] and obtained more accurate results for static I-V characteristics, dist.-dependance of field electrostatic potential and quasi Fermi level potentials.

In 1963 Goodman[24] pointed out the factors responsible for the deviation of the diode from the ideal case. He identified these factors to be the series resistance, traps in the depletion layer, the insulating interfacial layer and the edge effect. He illustrated these effects on gold-plated contacts on CdS and derived a correct expression for using the differential capacitance method for the measurement of barrier height. Khange[25] studied gold-silicon system of different resistivities. Low resistivity silicon resulted in an excess current which he attributed to space charge recom-

bination. Below room temperature the reverse current was dominated by excess current due to recombination-generation and at high temperature image force effect reduced barrier height. He obtained barrier height of 0.8 V by using current-voltage (I-V), capacitance-voltage(C-V) and photoelectric methods. In the same year Spitzer and Mead[26] evaporated different metals on cleaned(chemically and vacuum cleaved) n-type CdS and p-type GaAs. Barrier height for GaAs showed little dependence on metal work function and for CdS the barrier height depended on metal but deviated from predicted theory. He concluded that the barrier height values were very sensitive to the surface preparation. A comparison of these values with those obtained by Archer and Attala[20], showed larger deviations.

Cowley and Sze[27] (1965)found the dependence of the barrier height on the metal work function, density of surface states and thickness of the interfacial layer. Their derivation was based upon the assumptions that extremely thin inter-facial layer was transparent to electrons and that the surface-states were only the factor which influenced the barrier height of the semiconductor. Barrier height data and metal work function were fitted by the least square method for Si, GaP and CdS and the results were compared with those of Archer and Atalla[20]. Padovani and Sumner[28] in 1965 analysed the gold-GaAs system replacing KT by $K(T + T_o)$ in the thermonic equation whence T_o was found to be $50^oC \pm 5^oC$. The obtained barrier height was equal to $0.89 \pm .05$ volt.

In 1965 Crowell[29] modified the Richardon's constant for thermionic emission in vacuum by considering tensor masses of carriers.

For semiconductor having energy band with ellipsoidal constant energy surfaces in momentum space, the Richardson's constant changes depending on the planes of crystal surfaces. The values obtained agreed well with experimental values. At the same time Scharfetter[30] investigated the effect of minority carrier injection under moderate as well as high injection conditions. For Schottky diodes an injection ratio γ defined as the ratio of minority carrier current to total current was found to increased with forward current. This was due to increase in drift transport of electric field in the quasi-neutral region. He found that below a critical value of current density, γ was given by diffusion equation and its value was small. Beyond this critical value, the value of γ increased linearly with the electric field.

In 1966 Crowell and Sze[31] combined the thermionic emission(T) theory and Schottky diffusion (D) theory into a single thermionic-diffusion (T-D) theory which included the image force barrier lowering. A low electric field limit for application of this theory was estimated considering phonon-induced back Scattering near the potential energy maxima. The high electric field limit of the validity of thermionic emission theory was found to be due to quantum-mechanical reflection and tunnelling. Predicted value of ideality parameter was higher than unity because of field dependence of barrier height. At the same time Mead [32] published a review paper on Schottky barriers. A qualitative explanation of the type of contact to be expected at an arbitrary metal-semi- conductor interface was presented in his paper.

In 1968 Turner and Rhoderick[33] found the barrier height of a number of metal contacts to n-type silicion. They showed that the initial values of barrier heights depended upon the methods of surface preparation and these values changed slightly with time. They showed that the final value was independent of surface preparation and depended mainly upon the metal work function. However in the case diodes where depositions are made on cleaved surfaces, the barrier height did not show any ageing. In 1968 Padovani[34] showed that at room temperature the reverse current in lightly doped GaAs gold Schottky barriers was dominated by thermionic emission from the metal and that the barrier height did not depend upon the applied bias as was expected from the effect of simple image force lowering. Random variation of barrier height lowering together with its temperature dependence as observed from device to device however remained unexplained.

Yu and Mead[35] in 1970 worked on aluminium barriers. They observed that in silicon the barrier height was 0.69 $\pm$.01 v. Thermionic emission theory was found to be valid in this case. With low temperature heat treatment, the barrier height was found to decrease slightly. Noise and switching behaviours were determined and it was concluded that such a diode was useful as a discrete device. Moreover this could be used in integrated circuits as a Schottky contact. In 1970 Archer and Yep[36] experimentally showed that within the range of doping of 10^{14} to 10^{19} cm^{-3}, the barrier height was independent of doping as was found in the case of gold-silicon

barrier obtained by both etch-polished and vacuum-cleaved interface. Results obtained from C-V and photoelectric measurements were explained in terms of a simple model having interface of thickness δ. This finally led to a limit of the interfacial parameters given by $(\epsilon_i/\delta) + 1.8 \times 10^{-6}\ N_{ss} \geqslant 3.8 \times 10^{8}\ cm^{-1}$, where ϵ_i was the permittivity of interfacial layer, and N_{ss}, the surface states.

In 1971 Smith and Rhoderick[37] found that barriers with p-type silicon were generally lower than those with n-type. Gold barrier was so low that it was apparently ohmic. The ideality parameter was found to be about 1.1. The variations of barrier height with metal work function indicated that the surface states parameters were primarily responsible. Crowell and Beguwala[38] calculated ideality parameter,(n) and saturation current density(J_s) using parabolic band bending. It was found that the quasi-Fermi level in both forward and reverse bias was discontinuous at the interface. Under moderate bias the electron imref was nearly constant through the depletion region. In reverse bias imref deviates from constancy for applied bias in excess of KT/q. In 1971 Card and Rhoderick[39] conducted a theoretical and experimental study of metal-silicon system separated by interfacial oxide layer. A generalised approach was considered where the interface states communicated with both metal and semiconductor. Amount of current was explained by a transmission co-efficient which was also a function of thickness of interfacial layer.

In 1972 Tanta porn[40] used an interative computer method for finding values of six parameters including barrier height from the measurements of temperature, current and voltage of metal-semi conductor-metal system. With no prior assumptions the output parameters emerged as natural iterative solutions. Thanailakis and Northrop[41] determined metal-germanium barrier heights. Aluminium-germanium barrier showed slight aging and density of surface states was found to be 2×10^{13} ev^{-1} cm^{-2}. Barrier height was found to be independent on impurity concentration of germanium.

In 1973 Card and Rhoderick [42] investigated the effect of interfacial layer on minority carrier injection ratio, γ . Inclusion of thin oxide layer favoured reduction of barrier height. The flow of the minority carrier was explained to be due to tunnelling from metal to semiconductor. The authors obtained values of γ for different thickness of oxide interfacial layers.

In 1974 Patwari and Hartnagel[43] studied aluminium- GaAs and Nickel-GaAs Schottky barriers under non-ideal surface conditions. The aim of the study of damaged surface Schottky barrier was to find out whether any economy could be achieved with surfaces of the semiconductors whose surfaces were slightly damaged, and whether these were useful as devices. Results showed that damage and pitting effectively reduced the barrier height along with slight increase of the ideality parameter.

In 1976 Sinha et al[44] found out barrier height and ideality parameter of Schottky diodes made on n-GaAs metallised with Ti

and Pt/Ti. Also the effect of temp. upto 500°C was investigated. Taylor and Morgan[45] studied the effect of radiation induced damage caused to Ni- GaAs Schottky diodes. This damage produced defect levels and led to increased band bending. An excess current was observed in I-V characteristics which was thought to be due to recombination-generation. At higher reverse bias a trap assisted tunnelling was observed. Barrier height and ideality parameter were found to be higher.

In 1976 Shanon [46] used ion-implantation techniques to obtain doped surface of silicon in Ni-Si barrier. He showed that doping of the surface by antimony atoms decreased barrier height for n-type silicon whereas doping of p-type material by the same metal increased the barrier height. This change in barrier height- depending upon the depth of doped surface layer were explained by suitable equation and thus the control of barrier height was achieved.

Wilkinson et al[47] (1977) performed experiments on Ti-Si barrier at higher current density. They showed that the value of n depended upon band bending according to theory of Crowell and Beguwala[38]. Accurate determination of séries resistance was said to be important because it was found that the ideality parameter, n and the current density, J_s were very sensitive to it.

Recently Borrego et al[48] (1977) presented a model for determining surface-state density of Schottky diodes directly from I-V and C-V measurements. The interface state density for gold-GaAs barrier was calculated to be of the order of 2 $\times 10^{13}$ $ev^{-1} cm^{-2}$. The

effects of image force barrier lowering and deep level impurities were considered. Thermionic emission theory was found to be satisfactory except at the reverse bias where a nonthermionic current was observed. This was attributed to enhanced field emission from the traps.

From the very brief review of the papers as presented here a few observations can be made. Almost all the works refer exclusively to n-type semiconductors. Very few works are available with p-type semiconductor because of the fact that the barriers with p-type material were smaller and measurements were difficult. It is noted that extensive works have been done with GaAs[49]. This is passibly because GaAs has very high electron mobility. At present various metal-silicides are evoking interest of engineers. It is observed that barrier height data are more abundantly available in literature but few satisfactory models are available to explain the higher values of the ideality parameters.

As regards metals used in Schottky diodes, aluminium and gold have been used, of which aluminium extensively because it is cheaper and also easier to evaporate, though gold contacts are more stable. Some research interest is also observed with metals like titanium, platinum and nickel.

1.3. SCOPE OF THE THESIS

The purpose of this thesis is to investigate the fabrication process so that Schottky diodes can be fabricated with controlled barrier height. Control of Schottky barrier height by doping the semiconductor by ion-implantation [46] produces defect levels [45] in semiconductor. So a simpler and inexpensive method is sought to that a preset value of barrier height can be obtained by proper choice of the metal, the semiconductor and controlling the fabrication process. Thus a small value of barrier height would be used for a fast detector where level of signal is low and a high value of barrier height would be achieved in a photo-diode.

So investigations were carried with varied process of fabrication with respect to semi-conductor surface preparation, sequence of metal deposition, heat treatment and ohmic contacts. Silver-tin, gold and gold alloy ohmic contacts were used. Aluminium, silver, gold, gold-aluminium and gold-antinomy as Schottky metal contacts have been investigated.

A theoretical formulation on this subject is given within the first three chapters of which chapter -1 deals with the brief account of the some works done in this field. Chapter-2 gives basic physics of barrier formation along with derivations for barrier height and interface parameters. Chapter-3 deals with the current-transport theory across the barrier. Fabrication process description for different diode series and their measurements are included in Chapter-4. All the results are summarised in chapter-5, including the

discussions considering all important and related factors. Conclusions of the thesis along with a few suggestions for further research in this field have been given in chapter-6.

Thus the state-of-art of fabrication of Schottky barrier diodes has been established in our new Micro-electronics laboratory. A new scheme of controlling the barrier height has been introduced where the effect of surface electric field is considered to be dominant. Image force barrier lowering effect is included in deriving the barrier height. Results are based upon the measurements of current -voltage (I-V) and capacitance-voltage (C-V) of the diodes. Larger values of ideality parameter are explained with the help of a model where interfacial layer is thicker. The effect of series resistance was included in processing the current voltage and capacitance-voltage data. Minority carrier current has not been considered as it is negligible as predicted theoretically.

CHAPTER - TWO

AN INTRODUCTION TO THE SCHOTTKY BARRIER

2.1 PRELIMINARIES:

The potential barrier formed at a metal-semiconductor contact is primarily a function of metal work function, electron affinity of the semiconductor and semiconductor surface states. In this chapter the fundamental process of formation of the barrier has been explained together with the derivation of an expression for the barrier height values considering the inter-facial oxide layer. The effect of image force lowering of barrier has also been taken into consideration in the derivation. The solution of Poisson's equation gave the width and capacitance of the depletion layer. The method of obtaining the barrier height and impurity concentration from capacitance-voltage (C-V) measurement are based upon the deductions given in this chapter. The density of surface states may be determined from current-voltage (I-V) and capacitance-voltage (C-V) measurements according to the formulation given later in this chapter.

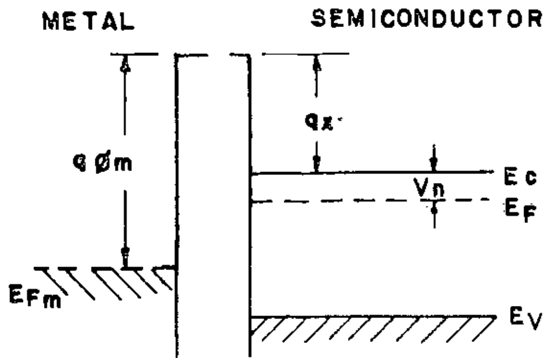
2.2. FORMATION OF SCHOTTKY BARRIER

When a metal is braught into an intimate contact with a semiconductor, the valence band and conduction band of the semiconductor is braught into definite energy relationship with the Fermi level in the metal. The energy band diagram is shown in figure-2.1. (a) where the metal and the semiconductor are separated. If a wire is now connected between them the electrons of the semiconductor will pass to the metal and their Fermi levels are forced into coincidence. An electric field would then result in the gap because there must be negative charges on the metal side balanced by posi-

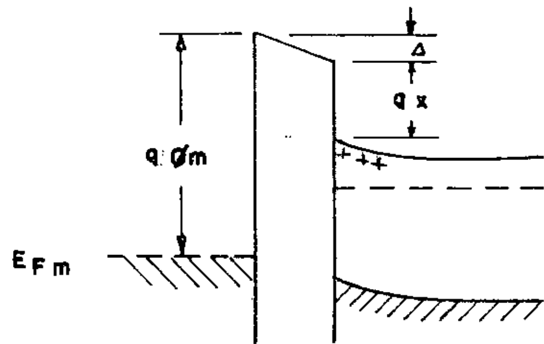
tive charges on the semiconductor side. Because the concentration of donors for an n-type semiconductor is many order of less in magnitude than the concentration of electrons occupy an appreciable thickness and band in semiconductor is bent upward as shown in figure -2.1(b). As the metal and semiconductor approach each other the drop in electrostatic potential (Δ) associated with field gap tend to be zero if the field is to remain finite. Finally when the gap becomes truely zero (i.e. perfect contact), the potential across the thin layer separating them disappears altogether as shown in figure 1(d) leaving behind only the barrier arising from band-bending. Evidently in the limit of perfect contact the following relationship derived by Schottky[17] holds good.

$$\phi_{Bn} = \phi_m - \chi \qquad (2.1)$$

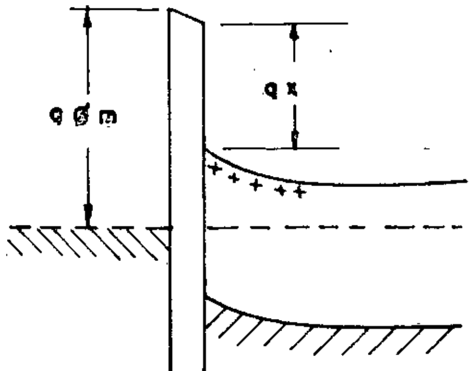
The semiconductor in figure 2.1(a) possesses no net charge at the surface. However the discontinuities in the lattice at the surface of the crystal produce in most semiconductor a number of possible energy states which are localised at the surface and usually there lies a number of states within the forbidden band. Depending on the density of these states, called surface-states, at equilibrium may either exceed or fall short of the number necessary to preserve the local charge neutrality. Bardeen [19] was the first to point out that the effect of surface-states on the height of pot.barrier. Surface-states are usually continuously distributed in energy within the forbidden band and are characterised by a neutral level, ϕ_0 which is such that if the surface-states are occupied upto ϕ_0 and empty above ϕ_0, the surface is electrically neutral. In case



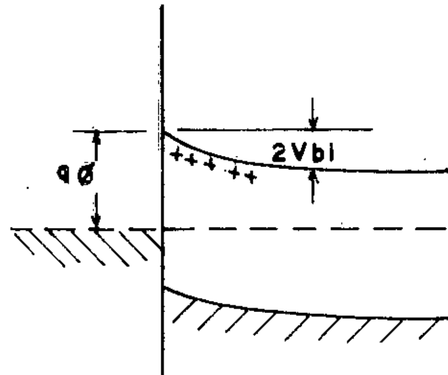
(a) NEUTRAL AND ISOLATED



(b) ELECTRICALLY CONNECTED

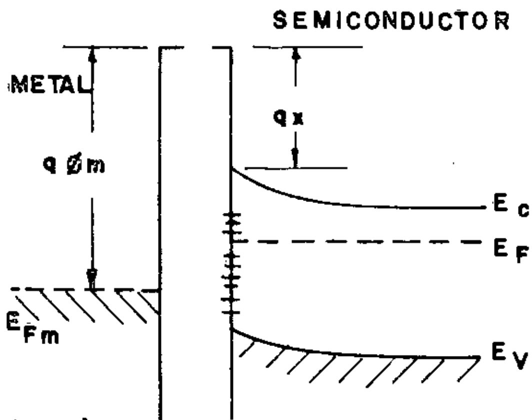


(c) SEPERATED BY NARROW GAP

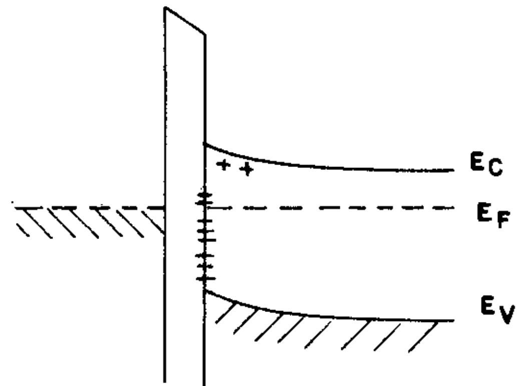


(d) PERFECT CONTACT

FIGURE 2.1 FORMATION OF SCHOTTKY BARRIER FROM METAL AND SEMICONDUCTOR.



(a) NEUTRAL AND ISOLATED



(b) CONNECTED ELECTRICAL WITH THIN INTERFACIAL LAYER.

FIGURE 2.2 SCHOTTKY BARRIER FORMATION WITH SURFACE STATES.

when $q\phi_o < E_F$ as shown in figure-2.2. There is net positive charge at the surface-states and the depletion region is not as wide as when there are no surface-states and the barrier height is reduced. Alternatively if $q\phi_o > E_F$ there is a net negative charge at the surface states and the barrier height is increased.

In a p-type semiconductor the position is reverse and for ideal contact, the barrier height is given by

$$\phi_{Bp} = \frac{E_g}{q} - (\phi_m - \chi) \tag{2.2}$$

And thus the sum of the barrier heights for an n-type and a p-type semiconductor is expected to be equal to the energy band gap i.e.

$$q(\phi_{Bp} + \phi_{Bn}) = E_g \tag{2.3}$$

2.3 CAPACITANCE AND WIDTH OF DEPLETION LAYER:

The potential within the depletion region is obtained from the solution of Poisson's equation $d^2V/dx^2 = -\rho/\epsilon$ with appropriate bounding conditions. The boundary conditions are known from the knowledge of energy-band relationship. The energy band diagram for n-type and p-type semiconductors are shown in figure-2.3 under different biasing conditions.

The metal-semiconductor barrier is identical to that of an one-sided abrupt junction. Thus for an n-type semiconductor having donor concentration N_D, we have charge density

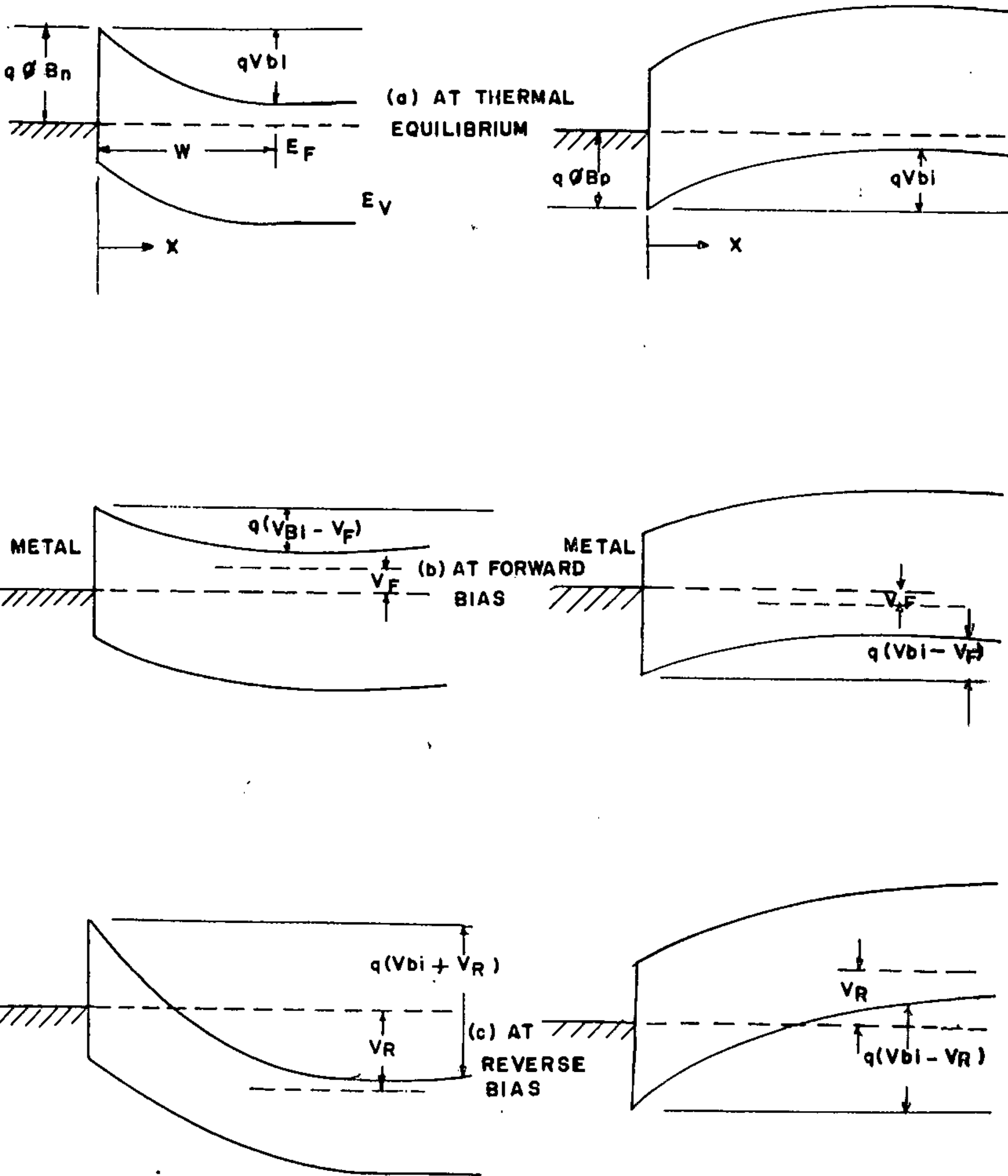


FIGURE 2·3 ENERGY BAND DIAGRAM OF METAL n-TYPE & METAL p-TYPE SEMICONDUCTOR UNDER DIFFERENT BIASING CONDITIONS.

$$\rho = q\,N_D \qquad \text{for} \quad x < W$$
$$= 0 \qquad \text{for} \quad x > W \qquad (2.4)$$
$$\text{and } \frac{dV}{dx} = 0,\; V = -\phi_{Bn} \text{ for } x = W$$

Where W is width of the depletion layer. Integrating Poisson's equation we get electric field.

$$\mathcal{E}(x) = +\,q\,N_D\,(W-x)$$
$$= \mathcal{E}_m - \frac{q\,N_D}{\epsilon_s}\,x$$

Integrating again, the potential is given by

$$V(x) = \frac{qN_D}{\epsilon_s}\,(Wx - \tfrac{1}{2}x^2) - \phi_{Bn}$$

Width of depletion layer is given by(51)

$$W = \left[\frac{2}{qN_D}\epsilon_s(V_{bi} - V - KT/q)\right]^{1/2} \text{cm} \qquad (2.5)$$

Where KT/q arises from the contribution of the mobile carriers to the electric field and is the correction applied by Goodman(24).
The maximum electric field $\mathcal{E}_m$ is then given by

$$\mathcal{E}_m = \mathcal{E}(x=0) = \sqrt{2qN_D\epsilon_s(V_{bi}-V-kT/q)} \quad \text{V/cm} \qquad (2.6)$$

The space charge per unit area of the semiconductor

$$Q_{sc} = qN_DW = \sqrt{2q\epsilon_sN_D(V_{bi}-V-kT/q)} \ \text{coul./cm}^2 \qquad (2.7)$$

Hence the capacitance C per unit area

$$C = dQ_{sc}/dV = \sqrt{\frac{q\epsilon_sN_D}{2(V_{bi}-V-kT/q)}} = \epsilon_s/W \quad \text{f/cm}^2 \qquad (2.8)$$

$$\text{or} \qquad 1/C^2 = \frac{2(V_{bi}-V-kT/q)}{q\epsilon_sN_D} \qquad (2.9)$$

where C is the capacitance per unit area.

2.4 THE IMAGE FORCE BARRIER LOWERING:

A charged particle close to a conducting plane produces an electrostatic force as if there were an equal and opposite charge at the mirror image of the particle . This image charge being of opposite sign lowers the potential energy of the body. In Schottky barrier this effect is called Schottky effect which reduces the height of the potential barrier and this illustrated in figure-2.4.

An electron at a distance x from metal surface, the attractive force due to image charge is

$$F = \frac{-q^2}{4\,(2x)^2 \epsilon_s} = \frac{-q^2}{16\, \epsilon_s x^2} \qquad (2.10)$$

Due to electric field within depletion layer, the total potential energy

$$PE\,(x) = \frac{q^2}{16\pi\epsilon_0 x} + q\,\mathcal{E}x$$

To find the amount of lowering of the barrier this equation is differentiated and set to zero, which yields the following condition

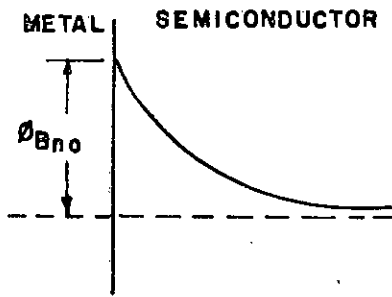
$$X_m = \sqrt{\frac{q}{16\,\pi\epsilon_0 \mathcal{E}}} \quad \text{cm} \qquad (2.11)$$

The amount of barrier lowering is given by,

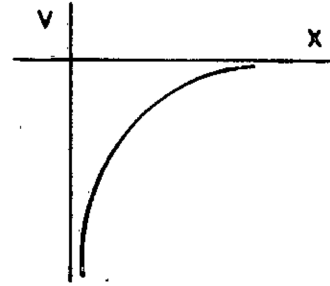
$$\Delta\phi = \sqrt{\frac{q\,\mathcal{E}}{4\pi\epsilon_s}} = 2\mathcal{E}\, x_m \qquad (2.12)$$

Where $\Delta\phi$ is caused by maximum electric field $\mathcal{E}_m$ within the depletion region. Substituting $\mathcal{E}_m$ from equation -(2.6) in equation-(2.12) we get

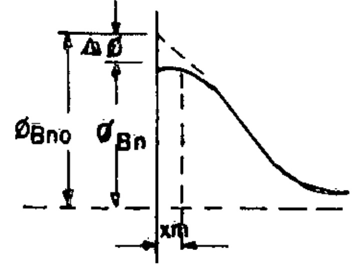
$$\Delta\phi = \left[\frac{q^3\, N_D\, (V_{bi} - V - KT/q)}{8\, \pi^2 \epsilon_s^3}\right]^{1/4} \qquad (2.13)$$



(a) SCHOTTKY BARRIER



(b) IMAGE POTENTIAL



(c) RESULTANT BARRIER

FIGURE 2.4 IMAGE FORCE BARRIER LOWERING

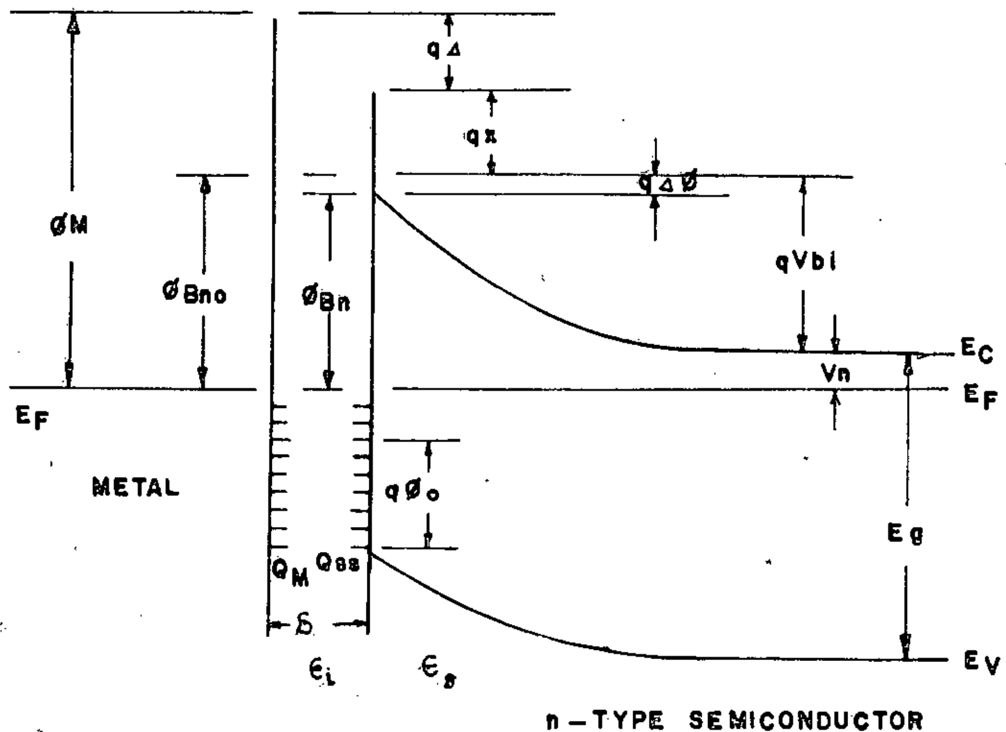


FIGURE 2.5 ENERGY BAND DIAGRAM OF A METAL n-TYPE SEMICONDUCTOR WITH AN INTERFACIAL LAYER

Because of this $\Delta\phi$, the reverse current-voltage (I.V) characteristic does not show saturation and in the forward direction the barrier height is increased slightly.

2.5 BARRIER HEIGHT AND THE SURFACE STATES:

The detailed energy band diagram of a metal- n-type barrier with an inter-facial layer is shown in figure-2.5. The following assunptions[27] are made in deriving the expression of barrier height.

a) In an intimate contact, the interfacial layer is of few atomic distance so that it is transparent to electrons and it can withstand potential.

b) The surface states per unit area per electron-volt at the interface are the properties of semiconductor only.

For most semiconductors $q\phi_0 < E_F$ i.e. the surface-states are acceptor-like whose density is N_{ss}. Thus surface charge density on the semiconductor.

$$Q_{ss} = - q N_{ss} (E_g - q\phi_o - q\phi_{Bn} - q\Delta\phi) \qquad (2.14)$$

The space charge formed in the depletion layer at thermal equilibrium is obtained from equation (2.7)

$$Q_{sc} = 2q\epsilon_s N_D (\phi_{Bn} - V_n + \Delta\phi - KT/q)^{1/2} \quad \text{Coul/cm}^2 \qquad (2.15)$$

In the absence of any space charge in the interfocial layer, the total equivalent charge density on the semiconductor surface is exactly equal and opposite to Q_M developed on the metal surface. Thus

$$Q_M = -(Q_{ss} + Q_{sc}) \tag{2.16}$$

Applying Gauss' Law to the surface charge on the metal and semiconductor, the applied potential across the interfacial layer is given by,

$$\Delta = -\delta Q_M/\epsilon_i \tag{2.17}$$

Also from energy band diagram

$$\Delta = \phi_m - (\chi + \phi_{Bn} + \Delta\phi)$$

Eliminating Δ from equation (2.14), (2.15) and (2.16) we obtain.

$$(\phi_m - \chi) - (\phi_{Bn} + \Delta\phi) = \left\{ \frac{2q\epsilon_s N_D}{\epsilon_i^2} (\phi_{Bn} - V_n - KT/q) \right\}^{1/2}$$

$$- \frac{q N_{ss} \delta}{i} (E_g - q\phi_o - q\phi_{Bn} - q\Delta\phi) \tag{2.18}$$

Let us define two constants as

$$C_1 \equiv 2q\epsilon_s N_{ss}\delta^2/\epsilon_i^2$$
$$C_2 \equiv \epsilon_i/(\epsilon_i + q^2\delta N_{ss}) \tag{2.19}$$

Thus equation (2.18) can be written as

$$\phi_{Bn} = \left[C_2(\phi_m - \chi) + (1-c_2)\left(\frac{E_g}{q} - \phi_o\right) - \Delta\phi \right]$$
$$+ \left\{ \frac{C_2^2 C_1}{2} - C_2^{3/2} \left[C_1(\phi_m - \chi) + (1-C_2)\left(\frac{E_g}{q} - \phi_o\right)\frac{C_1}{C_2} - \frac{C_1}{C_2}(V_n + KT/q) + \frac{C_2 C_1^2}{4} \right]^{1/2} \right\} \tag{2.20}$$

For $\epsilon_s = 10\epsilon_i$, $\epsilon_i = \epsilon_0$ and $N_D \nless 10^{18}$ cm^{-3}, C_1 is and the order of ·01 V, with the approximation that for clean condition

δ is of the order of 4 to 5 °A. Thus the term within the second bracket in equation (2.20) is negligible and the equation reduces to

$$\phi_{Bn} = C_2 (\phi_m - \chi) + (1 - C_2)(\phi_g - \phi_o) - \Delta\phi \qquad (2.21)$$

Similarly we can derive the barrier height for a p-type semiconductor and this is given by,

$$\phi_{Bp} = C_2 (\phi_g + \chi - \phi_m) + (1 - C_2)\phi_o - \Delta\phi \qquad (2.22)$$

where $\phi_g = E_g/q$

Barrier height can be obtained experimentally from $1/C^2$ Vs. V plot according to equation (2.9). The density of the interface states can be evaluated by the model of Borrego et al [48] (App-A) as follows.

$$N_{ss} = \frac{C}{q(n_F - 1)} \quad \text{for forward bias}$$

$$= \frac{C(n_R - 1)}{q} \quad \text{for reverse bias} \qquad (2.23)$$

where $n_{F,R} = \frac{q}{KT} \quad \frac{V}{(\ln I_{F,R})}$

and n_F and n_R can be found from current-voltage plot in forward and reverse conditions respectively.

CHAPTER - THREE

CHARGE-TRANSPORT THEORY OF SCHOTTKY BARRIER DIODES

3.1 PRELIMINARIES:

Current flow in a Schottky barrier diode is due to majority carriers in constrast to p-n junction diode where current is determined by minority carriers. Several theories approaches exist for finding the amount of current flow across the Schottky barrier. First is the diffusion theory which was proposed in 1939 by Wagner[22] Schottky and Spenke[23]. According to this theory current is limited by the process of drift and diffusion. In 1942 Bethe[32] formulated the thermionic emission theory according to which current was assumed to be limited by thermionic emission. Crowell and Sze[31] combined these two theories into a single thermionic-diffusion theory in which the effect of image force barrier lowering was also considered. Several other theories which are just modification of above theories and suited to particular condition exist. Besides there are emperical approaches for determination of behaviour of the diodes. Some of these will be discussed in the last article of this chapter.

3.2 THERMIONIC-EMISSION THEORY:

This is Bethe's model commonly known as diode model and is based upon the following assumptions:- (i) the mean free path should be greater than the distance in which barrier height falls by an amount KT from its maximum value. (ii) the effect of image force is neglected.

The current density due to electrons crossing over the potential barrier ϕ_{Bn} and flowing to metal from semiconductor under the application of potential V is given by[52]

$$J_{sm} = A_o^* T^2 \exp\left(\frac{-q\,\phi_{Bn}}{KT} \right) \exp\left(\frac{qV}{KT} \right) \qquad (3.1)$$

Where A_o^* is Richardson's constant for Thermionic emission in vaccum and is given by
$A_o^* = 4\pi q m^* K^2 / h^3$

Here m^* is the electron effective mass considered as a scalor quantity. But actually effective mass is tensor quantity and therefore depends upon the crystallographic orientation of emitting surfaces. For multiple-valley in energy band of silicon the appropriate Richardson's constant A* associated single-energy minimum was given by Crowell[29] as

$$\frac{A^*}{A_o^*} = \frac{1}{m_o}\left(l_1^2 m_y^* m_z^* + l_2^2 m_z^* m_x^* + l_3^2 m_x^* m_y^*\right)^{1/2}$$

-------(3.2)

where l_1, l_2, and l_3 are the direction cossine of the normal to the emitting plane relative to the principal axes of the ellipsoid and m_x^*, m_y^* and m_z^* are the components of effective tensor mass.

Since the barrier for the electrons moving from the metal to the semiconductor remains the same, the current flowing into semiconductor is thus unaffected by applied potential. Thus

$$J_{ms} = - A^* T^2 \exp\left(\frac{-q\phi_{Bn}}{KT}\right)$$

Total current, density $J' = J_{ms} + J_{sm}$

$$J = \left(A^* T^2 \exp\left(\frac{-q\phi_{Bn}}{KT}\right)\right)\left[\exp\left(\frac{qV}{KT}\right) - 1\right] \qquad (3.3)$$

$$= J_{sT}\left[\exp\left(\frac{qV}{KT}\right) - 1\right] \qquad (3.4)$$

where $J_{sT} = A^* T^2 \exp\left(\frac{-q\phi_{Bn}}{KT}\right)$, is called saturation current density for thermionic emission.

3.3. DIFFUSION THEORY:

This theory is based upon the following assumptions.

(i) The barrier height is much greater than KT ;

(ii) The effect of electron collision within depletion region is included ;

(iii) The carrier concentration of the ends of the Semiconductor, are unaffected by current flow and

(iv) The impurity concentration of the Semiconductor is non-degenerate.

The total current is the sum of drift and diffusion currents and is given by

$$J = q\left[n(x)\mu\mathcal{E} + D_n\, \partial n(x)/\partial x\right]$$
$$= q\, D_n\left[\frac{-q\,n(x)}{KT}\frac{\partial V(x)}{\partial x} + \frac{\partial n(x)}{\partial x}\right] \qquad (3.5)$$

together with the following boundary conditions:

$$q V(0) = -q\,(V_n + V_{bi}) = -q\,\phi_{Bn}$$
$$q V(w) = -q V_n - q V$$
$$n(0) = N_c \exp\frac{-E_c(0) - E_F}{KT} = N_c \exp\left(\frac{-q\phi_{Bn}}{KT}\right) \qquad (3.6)$$
$$n(w) = N_c \exp(-q V_n/KT)$$

Substatuting the boundary conditions in equation (3.5) and replacing W in terms of $V_{bi} + V$ lead to the following expression.

$$J = \frac{q^2 D_n N_c}{KT}\left[\frac{q(V_{bi} - V)2N_D}{\epsilon_s}\right]^{1/2} \exp\left(\frac{-q\phi_{Bn}}{KT}\right)\frac{\exp(qV/KT) - 1}{1 - \exp\left[-\frac{2q(V_{bi} - V)}{KT}\right]}$$

Where V, the applied potential is positive for forward bias and negative for reverse bias. Since $qV_{bi} \gg KT$, the exponential term in denuminator can be neglected for reverse voltages and small forward voltages, thus we get.

$$J = \frac{q^2 D_n N_c}{KT}\left[\frac{q(V_{bi}-V)2N_D}{\epsilon_s}\right]^{1/2}\exp\left(\frac{-q\phi_{Bn}}{KT}\right)\left[\exp\left(\frac{qV}{KT}\right)-1\right] \quad (3.7)$$

$$= J_{SD}\left[\exp\left(\frac{qV}{KT}\right)-1\right] \quad (3.8)$$

$$\text{where } J_{SD} = q^2\frac{N_c D_n}{KT}\left[\frac{q(V_{bi}-V)2N_D}{\epsilon_s}\right]^{1/2}\exp\left(\frac{-q\phi_{Bn}}{KT}\right)$$

Saturation current in diffusion theory varies more rapidly with voltage but is less sensitive to temperature in comparison with the saturation current in thermionic-emission theory.

3.4 OTHER THEORIES

Crowell and S_{ze} (31) synthesised thermionic emission theory and diffusion theory into thermionic- diffusion theory. They derived the current transport equation from the boundary condition of thermionic recombination velocity, v_R , near the metal-semiconductor interface. In addition, effects of electron-phonon Seattering(53) and quantum-mechanical reflection(54) at the interface are incorporated. The electron optical-phonon Scettering between the barrier energy maximum and metal predicts a low field limit for applying the thermionic emission theory i.e. for assuming that the metal actsas a perfect sink for carriers which cross the potential maximum in the direction of the metal. The effect of quantum-mechanical reflection and quantum tunnelling on the recombination velocity predicts the high field of validity of thermionic emission theory and the onset of thermionic-field emission. The complete expression for J-V characteristics taking into account of these two factors is given by

$$J = J_s \left[\exp\left(\frac{qV}{KT}\right) - 1 \right]$$

Where $J_S = A^{**} T^2 \exp(-q\phi_{Bn}/KT)$

and A** is called effective Richardson's constant (3.9)
(Appendix -B)

Thus at room temperature the semiconductors having impurity concentration below 10^{17} cm^{-3}, the current transport mechanism in Schottky diodes is due to thermionic emission of majority carriers.

These theories are derived considering the barrier height is constant and contact is such that the interfacial layer is very thin. But in practice, diodes fabricated do not fit to the theoritcal expression of equation (3.9) exactly because of nonuniformity in semiconductor space charge, thicker interfacial oxide layer, minority carrier injection and recombination generation in the depletion region. However, it is found that all the experimental resul s could be fitted to the following well-accepted equation

$$I = I_s \exp\ (qV/nKT) \text{ for} \qquad (3.10)$$

biases $V > 3KT/q$, where n is called the ideality parameter which varies in the range unity to 10 and I_s is the saturation current.

So far we have considered only the majority carriers. The effect of minority carrier was investigated by the model of Schar-fetter[30]. Magnitude of minority carrier injection was measured by Y_u and Snow[55]. The minority carrier injection(App- D)

was measured to be very small and current was primarily due to the majority carriers. Also the existence of recombination generation current was detected by Yu and Snow[55] and Sinha[44] which is important in low current levels otherwise negligible.

Card and Rhoderick[39] derived a model on Schottky barrier current where interfacial layer is thick. They assumed two types of interface states one is N_{sa} and another is N_{sb}. The oxide layer which was intentionally introduced was supposed to form a barrier of average height ψ Transmission component of electron tunnel was dependent upon $\psi^{1/2}$ and thickness of the oxide layer, Thus the equation was derived

$$J = A^{**}T^2 \exp(-\psi^{1/2}\delta) \exp\left(\frac{-q\phi_{Bn}}{KT}\right)\left[\exp\left(\frac{qV}{nKT}\right)-1\right]$$

where n was given by (Appendix C) (3.11)

$$n = 1 + \frac{(\delta/\epsilon_i)\left(\frac{\epsilon_s}{W} + q N_{sb}\right)}{1+(\delta/\epsilon_i)\, q N_{sa}}$$

If all the interface states communicates with the semiconductor, then $N_{sa} \rightarrow 0$ and we get

$$n = 1 + \frac{\delta}{\epsilon_i}\left(\frac{\epsilon_s}{W} + q N_{sb}\right) \tag{3.12}$$

We have neglected in all cases the effect of traps, but in practice generally the deep level impurities are found to be present. They contribute to change of interface states and capacitance of the diode.

CHAPTER - FOUR

FABRICATION OF SCHOTTKY DIODES AND MEASUREMENTS

4.1 PRELIMINARIES:

In this chapter the process of fabrication of reproducible Schottky barrier diodes have been described. All of them were obtained by vacuum deposition of metals on cleaned surfaces of doped semiconductor wafers. The vacuum system was Edwards-306 coating unit fitted with a film thickness monitor having an accuracy of one angstrom Deposition of metals [62] were carried out at residual pressures in the range of 10^{-5} to 5×10^{-6} torr, and liquid nitrogen was used as trap. Both n-type and p-type silicons were used. Fabrication of diodes started with chemical cleaning of the silicon substrates. The substrates had doped epitaxial layers. The current-voltage (I-V) and capacitance-voltage (C-V) measurements were performed on the diodes. A X-Y plotter and a radio-frequency bridge were used in measurements.

4.2 FABRICATION PROCESS:

In general the following steps were followed in the fabrication process-

i) Chemical cleaning of the substrates.

ii) Preparation of ohmic contact.

iii) Preparation of metal contact and

iv) Dicing, mounting and load connection.

4.2.1 Chemical Cleaning:

The epitaxial layer side of the substrates was already mirror polished . These were cleaned chemically where some variations were introduced e.g. some of them were slightly etched and some were not. Thus we devide this

step into two categories.

(a) - Ultrasonic cleaning in methanol for 3 minutes.

- Boiling in mixture of methanol and acetone .
- Rinsing in acetone.
- Drying at $80^{\circ}C$.

(b) - Ultrasonic cleaning in methanol for 3 minutes.

- Etching in the solution of 1 part hydrofloric acid, 5 parts nitric acid and 12 parts of acetic acid by volume (1 HF : 5 HNO_3 : 12 cH_3 COOH) for 1-4 minutes.
- Washing in deionised water.
- Ultrasonic cleaning in methanol for 3 minutes.
- Rinsing in acetone.
- Drying at $80^{\circ}C$.

4.2.2. Ohmic Contact: The n-type subtrates which were $n^{\pm}n$ type had their backside unpolished . Well-known silver-tin contact was applied. Tin and silver were deposited in sequence of $200^{\circ}A$ and $2000^{\circ}A$ respectively at a pressure of 10^{-5} torr and then alloyed in vacuum (10^{-2} torr) at $600^{\circ}C$ for one minute.

The p-type substrates were both p-type and p^{+}- p-type . The ohmic contact was obtained by gold or gold-aluminium alloy. Some of the p^{+} -p substrates were gold deposited ($1000^{\circ}A$) in vacuum (10^{-5} torr) and then heated at $550^{\circ}C$ for 5 minutes in a chamber having a pressure of 10^{-2} torr. And rest of these were given contact of aluminium gold which were deposited in succession of $100^{\circ}A$ and $1000^{\circ}A$ respectively and then alloyed at $450^{\circ}C$ for 4 minutes in a chamber

with a pressure of 10^{-2} torr. This process gave reproducible contact and contact with a large contact area, they were ohmic.

4.2.3 Schottky Metal Contact: This was done by various metal such as aluminium, gold, silver, aluminium-gold and antimony-gold. Metals were deposited through metal masks to give a few circular contacts at residual pressure in the range of 5×10^{-6} torr to 10^{-5} torr. Thickness of metal film was varied in the range of 1000 ^{o}A to 2000°A and the rate of deposition was in the range 10 -20°A/sec. The list of diode-series fabricated are given in table 4.1 in which conditions of each process have been shown. Generally the metal contacts were heated at 120°C to have a stable contact. For aluminium-gold and antimony-gold system, aluminium or antimony was deposited with a thickness of 50°A before the deposition of gold. Then gold was deposited of thickness 1000°A.

4.2.4 Dicing Mounting and Lead Connection: The Schottky diodes were separated by dicing with the help of a diamond pencil and were mounted on thin glass slides with adhesives of silver preparation. And the wires were connected on both sides of diodes with silver pastes. A sectional view of such a diode is given in figure-4.1.

Heat-treatment of the diodes were performed in a furnace where they were heated at certain temperature for 3 to 5 minutes and were left there for about one hour. Then the samples were taken out to be cooled in atmospheric condition for at least 15 minutes. In this way a slow cooling was achieved.

TABLE- 4.1

Sl. no.	Diode series	Chemical cleaning by process (a) or (b)	Type of semi-conductor	Type of ohmic contact	Schottky Metal contact	Pressure of deposition in torr	Area of contact in cm^2	Heat treatment if any
1.	S8	(a)	n^+ -n	Silver-tin	Silver	10^{-5}	0.05	X
2.	S10	(a)	n^+ -n	Silver-tin	Aluminium	8×10^{-6}	0.05	X
3.	S19	(a)	p^+ -p	Gold	Silver	$7x10^{-6}$	0.018	X
4.	S20	(a)	p^+- p	Gold	Aluminium	10^{-5}	0.018	450°C
5.	S21	(b)	n^+ -n	Silver-tin	Aluminium	$6x10^{-6}$	0.018	400°C
6.	S23	(b)	p	Gold	Aluminium	$6x10^{-6}$	0.018	X
7.	S24	(b)	n^+ -n	Silver-tin	Gold	$6x10^{-6}$	0.018	450°C
8.	S27	(b)	p^+ -p	Gold	Gold	$7x10^{-6}$	0.018	120°C
9.	S30	(b)	n^+ -n	Silver-tin	Gold	$6x10^{-6}$	0.018	x
10.	S31 n	(b)	n^+ -n	Silver-tin	Aluminium	$8x10^{-6}$	0.018	0.600°C

TABLE-4.1 (Contd)

Sl. No.	Diode series	Chemical cleaning by process (a) or (b)	Type of semi-conductor	Type of ohmic contact	Schottky Metal contact	Pressure of deposition in torr	Area of contact in cm^2	Heat treatment if any
11	S31 p	(b)	$p^+ - p$	Gold	Aluminium	$8x10^{-6}$	0.018	0-600°C
12	S32 n	(b)	$n^+ - n$	Silver-tin	Gold -aluminium	$5x10^{-6}$	0.018	0-600°C
13	S32 p	(b)	$p^+ - p$	Gold - Aluminium	Gold-Aluminium	$5x10^{-6}$	0.018	200°C
14	S33 n	(b)	$n^+ - n$	Silver-tin	Gold-Antimony	$6x10^{-6}$	0.018	0-500°C
15	S33p	(b)	$p^+ - p$	Gold-Aluminium	Gold-Antimony	$5x10^{-6}$	0.018	120°c

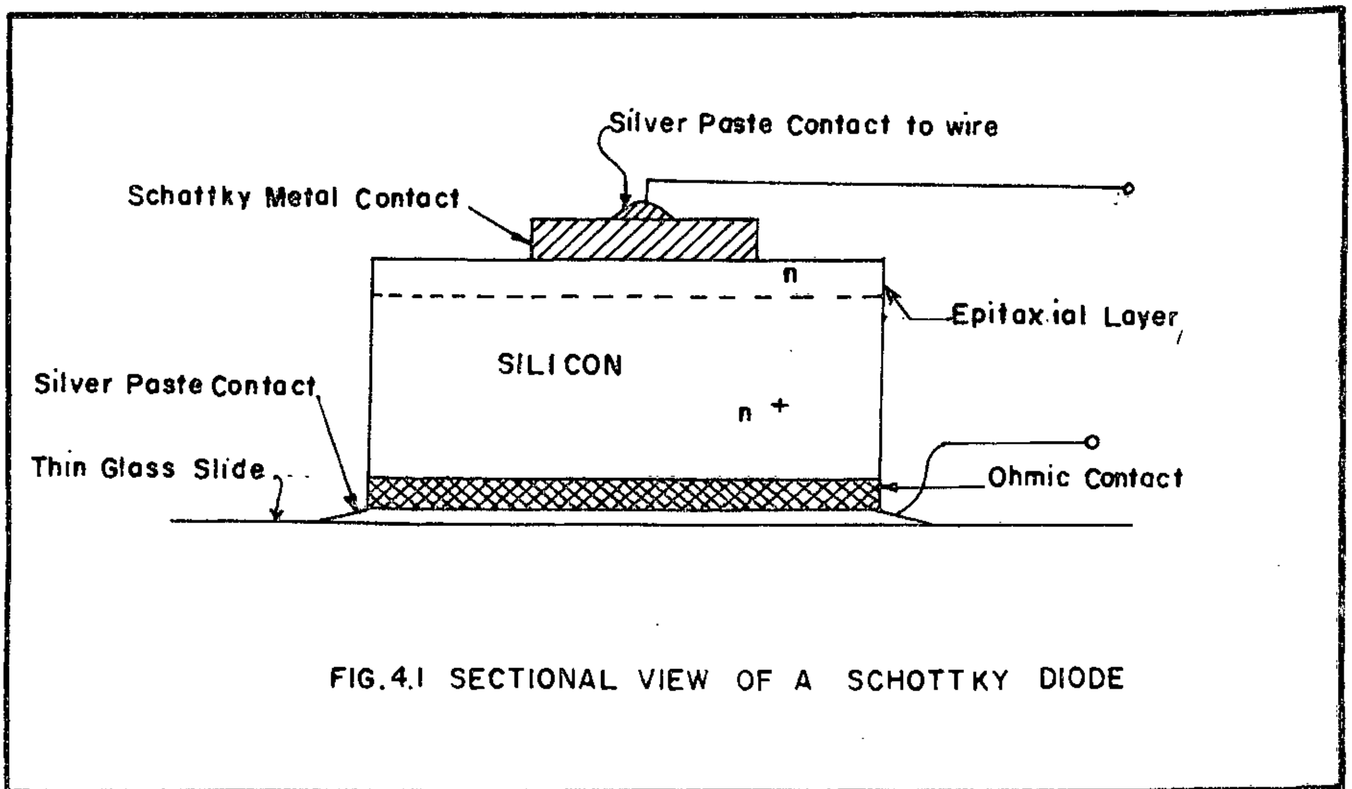


FIG. 4.1 SECTIONAL VIEW OF A SCHOTTKY DIODE

4.3 MEASUREMENTS:

Current-voltage (I-V) and Capacitance-voltage (C-V) measurements were performed on the Schottky diode in order to find out the parameters e.g. barrier height, ideality parameter, series resistance and interface-states density etc. A low frequency equivalent circuit of a Schottky diode is given in figure -4.2 where R_s represents the series resistance, R is the diode resistance and C is the capacitance of the diode. R_s is the sum of resistance of quosi-neutral region (within epitaxial layer), the spreading resistance of the barrier and the contact resistance due to ohmic contact.

4.3.1 CURRENT -VOLTAGE MEASUREMENT:

I-V measurements was performed on the diodes both in forward and reverse directions. These were obtained directly on a x-y plotter. The forward-characteristics were drawn upto 500 mV and reverse characteristics were drawn upto 4/5 volts. The value of barrier height ϕ_B and ideality parameter, n can be obtained from the plot of LogI Vs V in forward direction according to the following equation (4.1). Log I Vs. V plots were straight lines.

$$\phi_B = \frac{KT}{q} \ln \left(\frac{SA^{**} T^2}{I_s} \right) \qquad (4.1)$$

and $$n = \frac{q}{KT} \cdot \frac{\partial V}{\partial (\ln I)}$$

The effective Richardson's constant A** is function of electric field at the interface. In the range of electric field of

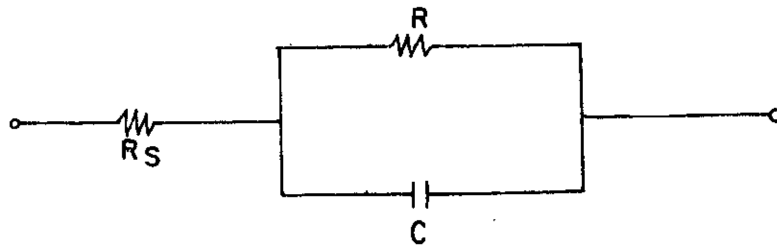


FIG. 4.2 EQUIVALENT CIRCUIT OF SCHOTTKY DIODE

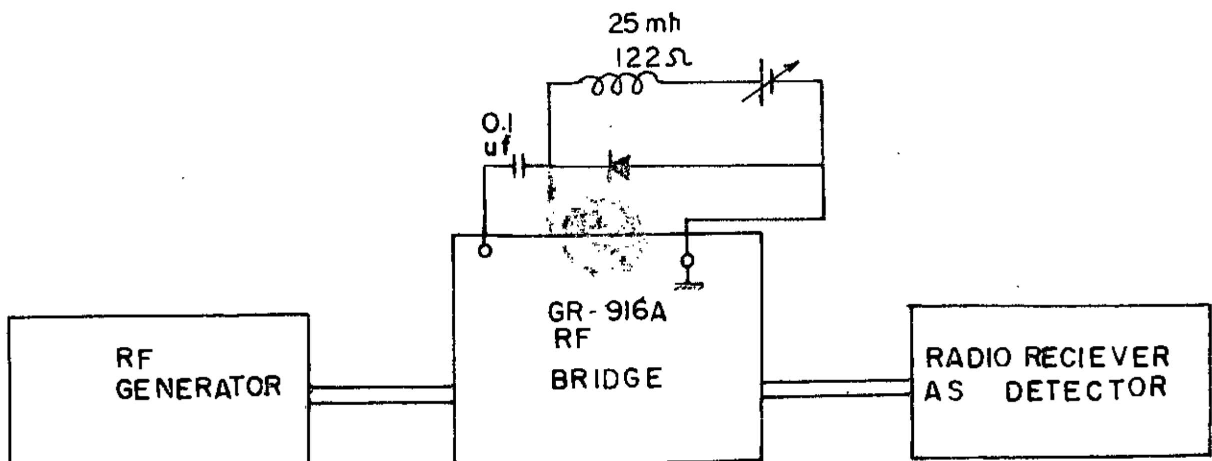


FIG. 4.3 SET UP FOR CAPACITANCE MEASUREMENT

10^4 to 2×10^5 V/cm, A** is given by (Appendix-B)

$$A^{**} = 115 \quad amp/cm^2/{}^oK^2 \quad ......\text{for electrons}$$

$$= 30 \quad amp/cm^2/{}^oK^2 \quad ......\text{for holes}.$$

Diode Series resistance R_s was measured by biasing the diodes far beyond the diode region, usually above 5 ma.

4.3.2 CAPACITANCE -VOLTAGE MEASUREMENT [24]

Diode capacitance, C was measured with a small ac voltage superimposed upon the reverse bias. Straight line was obtained by plotting $1/C^2$ versus the reverse voltage. The barrier height is derived from the intercept V_i of this plot and the impurity concentration of the semiconductor is found from the slope of the straight line plot according to following equation (4.2).

$$\phi_{Bn} = V_i + V_n + KT/q - \Delta\phi$$

$$N_D = \frac{2}{q\,\epsilon_s} \quad \frac{-dV}{d(1/C^2)} \qquad (4.2)$$

Where C is the capacitance per unit area.

However, when deep level impurities are present, these levels are filled upto quasi-Fermi level under forward bias condition and their space charge density is simply given by N_D. But under the reverse bias, the traps empty down to a certain level below conduction band and the space charge is nonuniform and their density is given by $N_D + N_t$, where N_t is deep level impurity concentration. Thus Goodman[24] showed that

$$\frac{d(1/C^2)}{dV} = \frac{-2}{q N_D \epsilon_s} \quad \text{for forward bias}$$

$$\frac{d(1/C^2)}{dV} = \frac{-2}{q (N_D + N_t) \epsilon_s} \quad \text{for large reverse bias} \qquad (4.3)$$

Thus when the traps are present, the plot of $1/C^2$ Vs. V does not show just one straight line, instead it gives two straight lines. The slope of the straight line in forward bias and small reverse bias is determined by the shallow impurity and at large reverse bias the slope is different and is due to sum of shallow and deep level impurities.

The experimental set-up for capacitance measurement has been shown in figure 4.3 where the biasing to the diode is done external to the bridge. GR-916A radio-frequency bridge was used where the lead capacitance correction were provided. Measurement was carried out at 1 MH_z because with such a high frequency the traps cannot respond. The bridge measures the series resistance and series capacitance directly and these values were transformed into parallel resistance R_p and parallel capacitance C_p. Diode resistance R and capacitance C may be calculated from the following equations:-

$$\frac{1}{R_p} = \left[\frac{1}{R}\left(\frac{R_s}{R} + 1\right) + \omega^2 R_s C^2\right] / \left[\left(\frac{R_s}{R} + 1\right) + \omega^2 R_s^2 C^2\right]$$

$$C_p = C / \left[\left(\frac{R_s}{R} + 1\right) + \omega^2 R_s^2 C^2\right]$$

Thus when $R_s/R \ll 1$ and $w^2 R_s^2 C^2 \ll 1$, then

$$C \cong C_p \tag{4.4}$$

These two conditions are satisfied because under, reverse bias $R_s/R \ll 1$ and diode capacitance is smaller than a nanofarad.

Also it can be derived that

$$1/C_p^2 = \frac{(2 (V_{bi} - V - KT/Q))}{Sq\epsilon_s N_D} + 2\omega^2 R_s^2 \tag{4.5}$$

Where S is the area of diode. Thus when the values of C_p are used to plot $1/C^2$ vs. reverse voltage, it is observed that the actual intercept with voltage axis is changed by an amount equal to $2\omega^2 R_s^2$ though the slope of the straight line plot remains the same. So a correction which is equal to $2\omega^2 R_s^2$ was accounted to find out $1/C^2$.

CHAPTER - FIVE

RESULTS AND DISCUSSIONS

RESULTS AND DISCUSSIONS:

Barrier heights (ϕ_B) and ideality parameters(n) of the diodes have been derived from the plot of log I Vs V in forward direction and using the equation (4.1). The intercept and slope of the straight line plot determine saturation current and ideality parameter respectively. These plots of log I Vs. V for the diodes whose metal contacts have been made with single metal deposition are given in figures -5.5 to 5.8. The points of these straight line plot are obtained from the I-V plots in figures 5.1 to 5.4. All these plots are shown for both forward and reverse biases, $1/c^2$ Vs reverse bias plot of these diodes are given in figures 5.9 to 5.12. The intercept (V_i) with the voltage axis has been used to find out barrier height according to equation (4.2). The density of shallow and deep level impurities have been derived from the slopes of the straight lines in $1/C^2$ vs reverse bias plots according to equation (4.3). All these results have been shown in Table-5.1 along with the series resistances of the diodes. The rectification property of the diodes can be visualised from the photographs of I-V characteristic was taken from HewlletPackard oscilloscope as in figure 5.20 (A-P). Reverse characteristics at higher voltages and breakdown voltages have not been shown as they are not important for Schottky diodes.

TABLE- 5.1.

Diode Series	Series Resistance in Ohms	Barrier Height in volt ϕ_B, I-V	Barrier Height in volt (C-V)	Ideality parameter n	Impurity concentration N_D/N_A in cm^{-3}	Concentration of traps, if any, cm^{-3}
ALUMINIUM BARRIER						
S10	32	0.675	0.68	3.76	3.68×10^{15}	1.1×10^{15}
S20	65	0.575	0.57	2.07	6.70×10^{15}	2.5×10^{15}
S21	30	0.775	0.77	1.73	4.84×10^{16}	x
S23	105	0.660	0.625	1.90	3.06×10^{15}	x
SILVER BARRIER						
S8	64	0.76	0.78	2.80	3.824×10^{15}	3.32×10^{14}
S19	42	0.652	0.63	1.93	7.36×10^{15}	x
GOLD BARRIER						
S24	30	0.74	0.78	1.99	3.89×10^{16}	6.1×10^{15}
S30	23	0.72	0.74	1.90	2.63×10^{16}	2.45×10^{15}

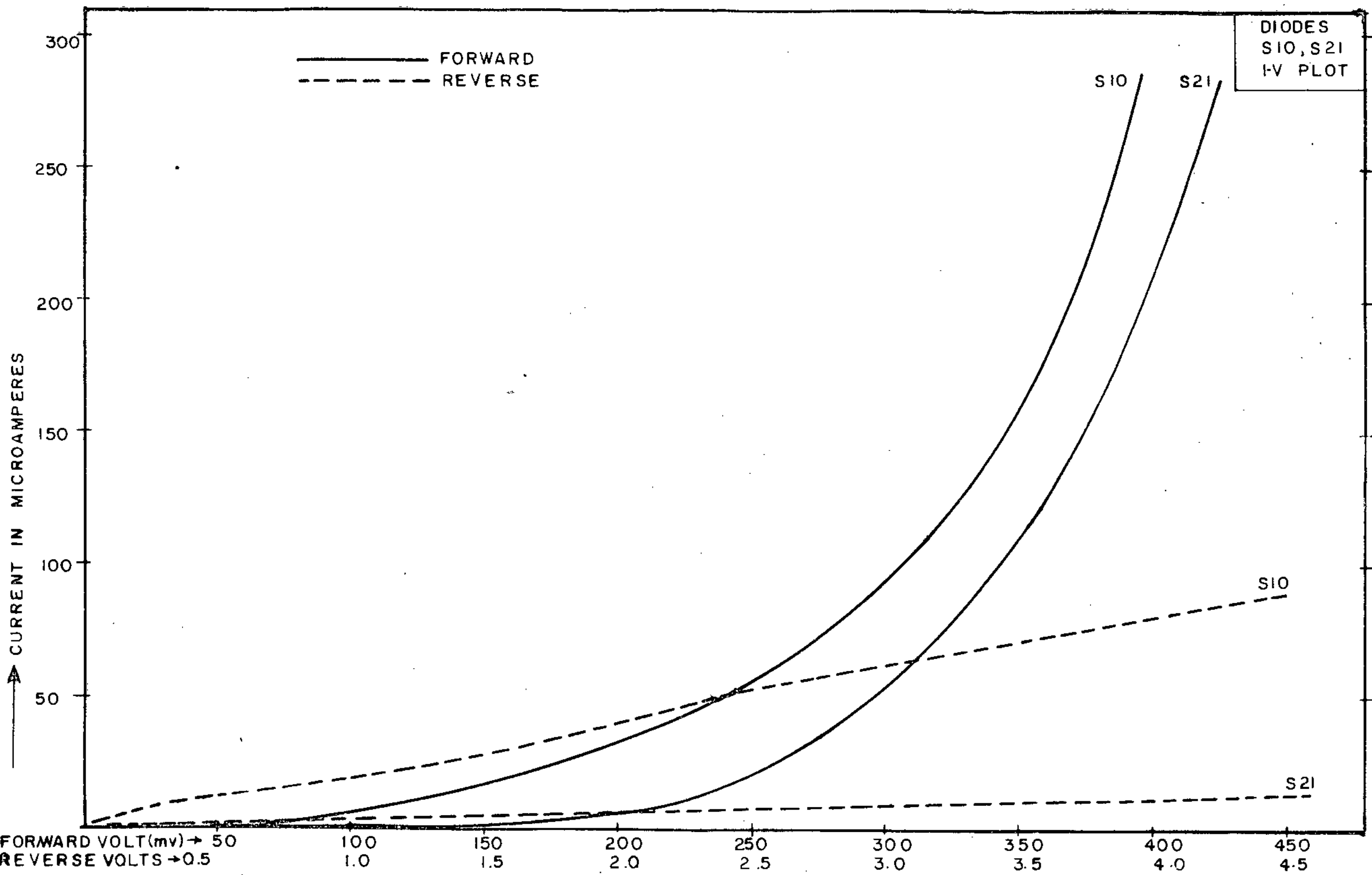


FIG. 5·1 CURRENT-VOLTAGE CHARACTERISTICS OF ALUMINIUM-N-TYPE SILICON SCHOTTKY DIODES

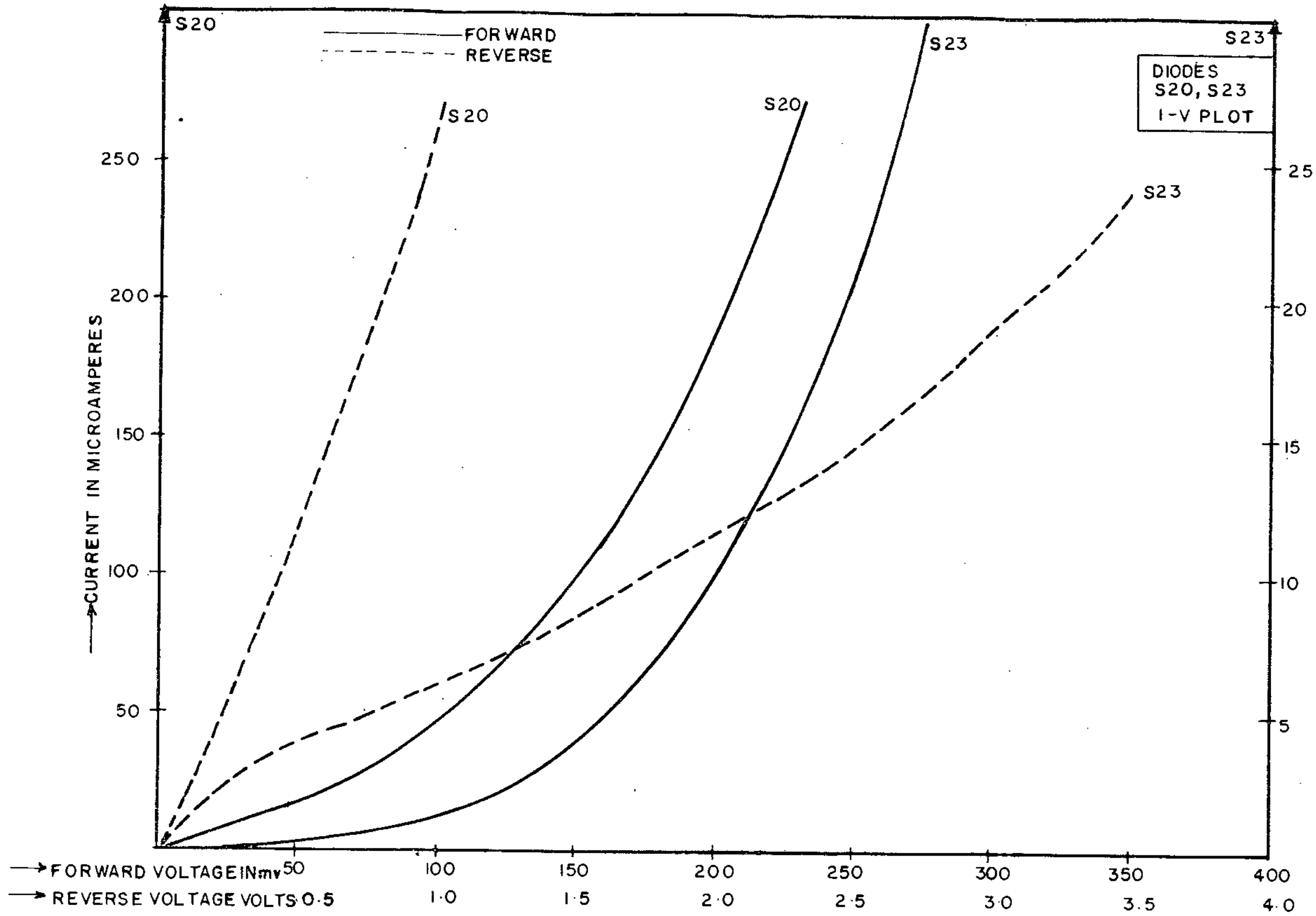


FIGURE: 5·2 CURRENT– VOLTAGE CHARACTERISTICS OF ALUMINIUM-P-TYPE SILICON SCHOTTKY DIODES

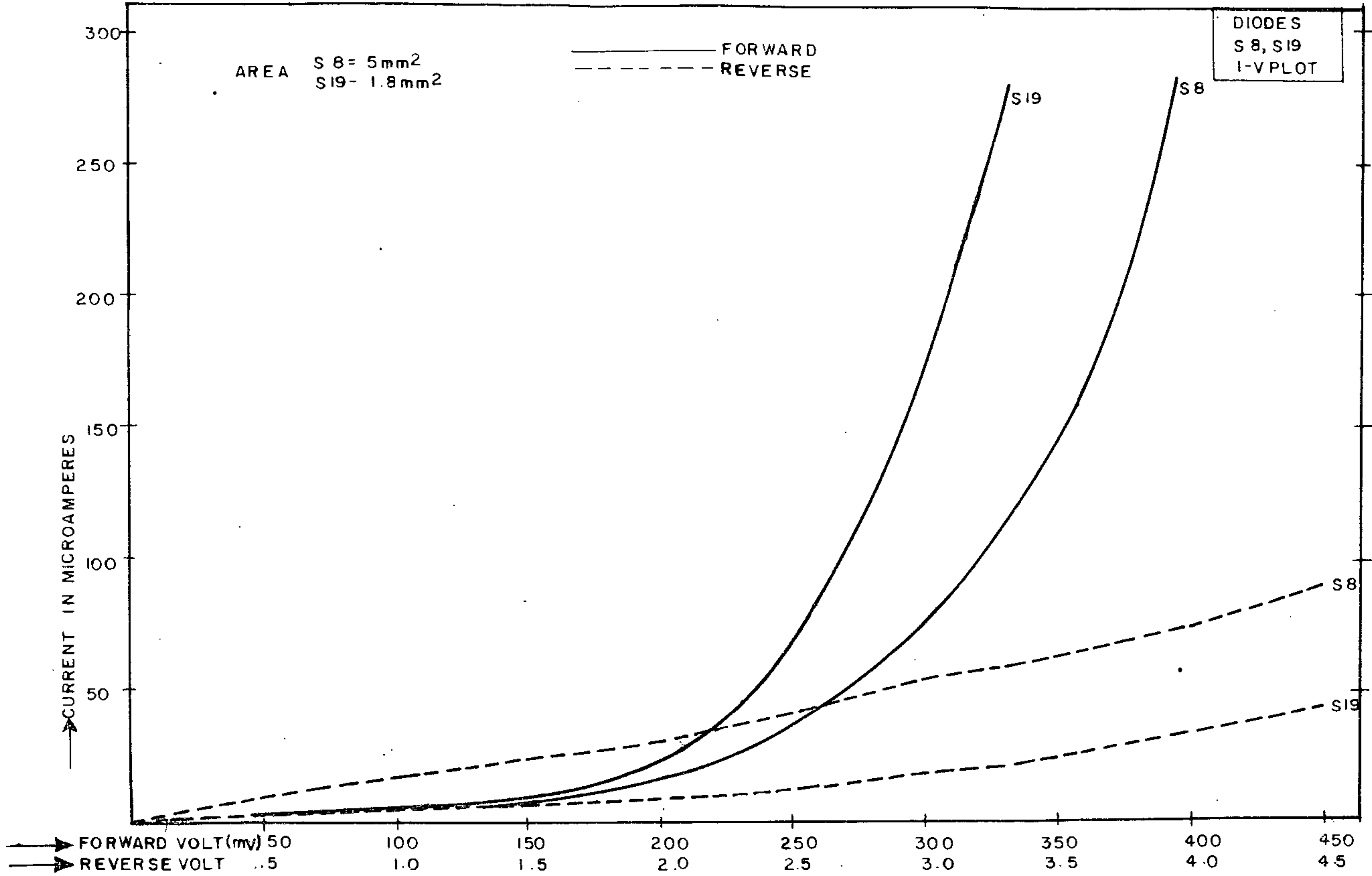


FIGURE 5.3 CURRENT-VOLTAGE CHARACTERISTICS OF SILVER-SILICON SCHOTTKY DIODES.

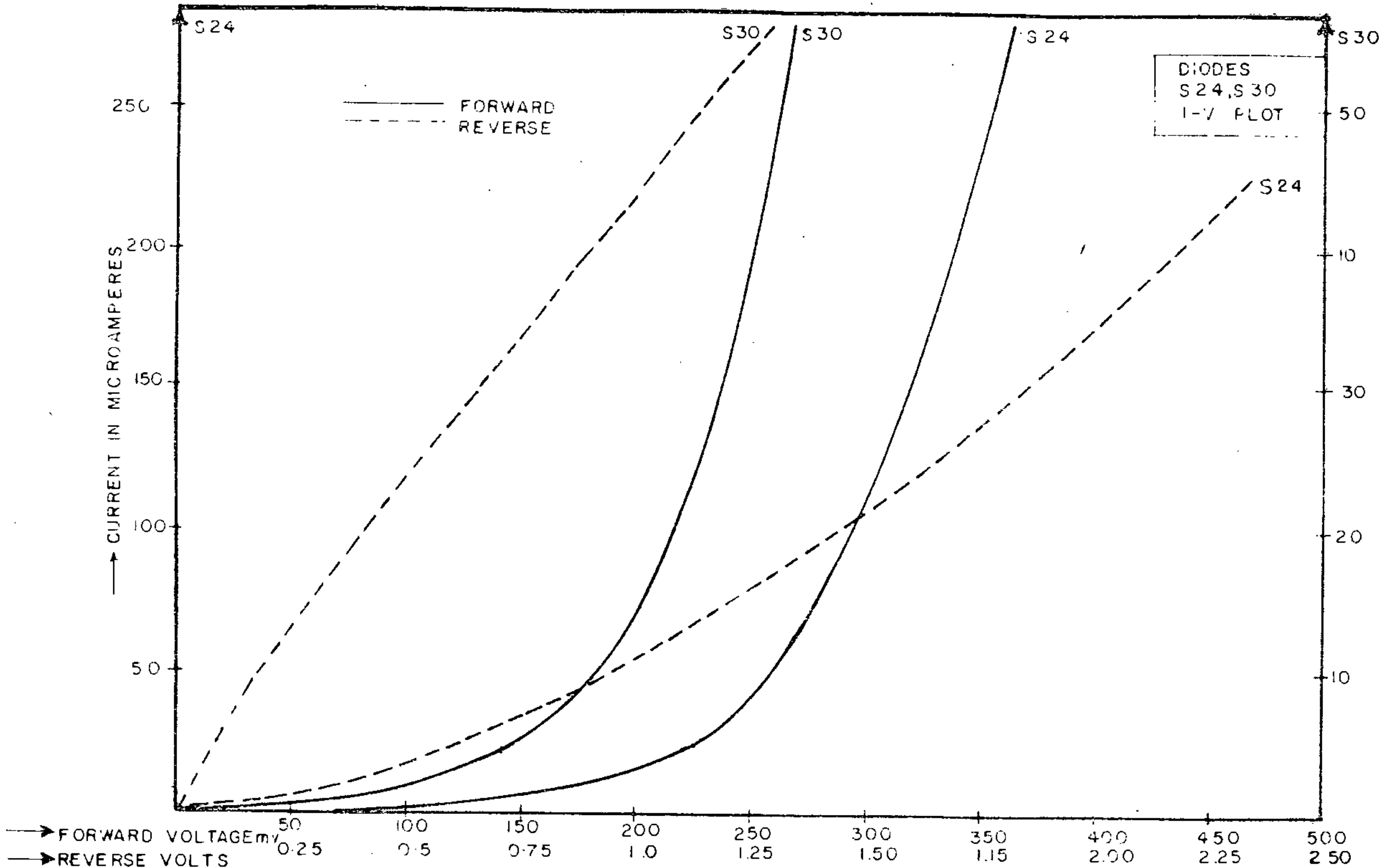


FIGURE : 5.4 CURRENT-VOLTAGE CHARACTERISTICS OF GOLD-N-TYPE-SILICON SCHOTTKY DIODES.

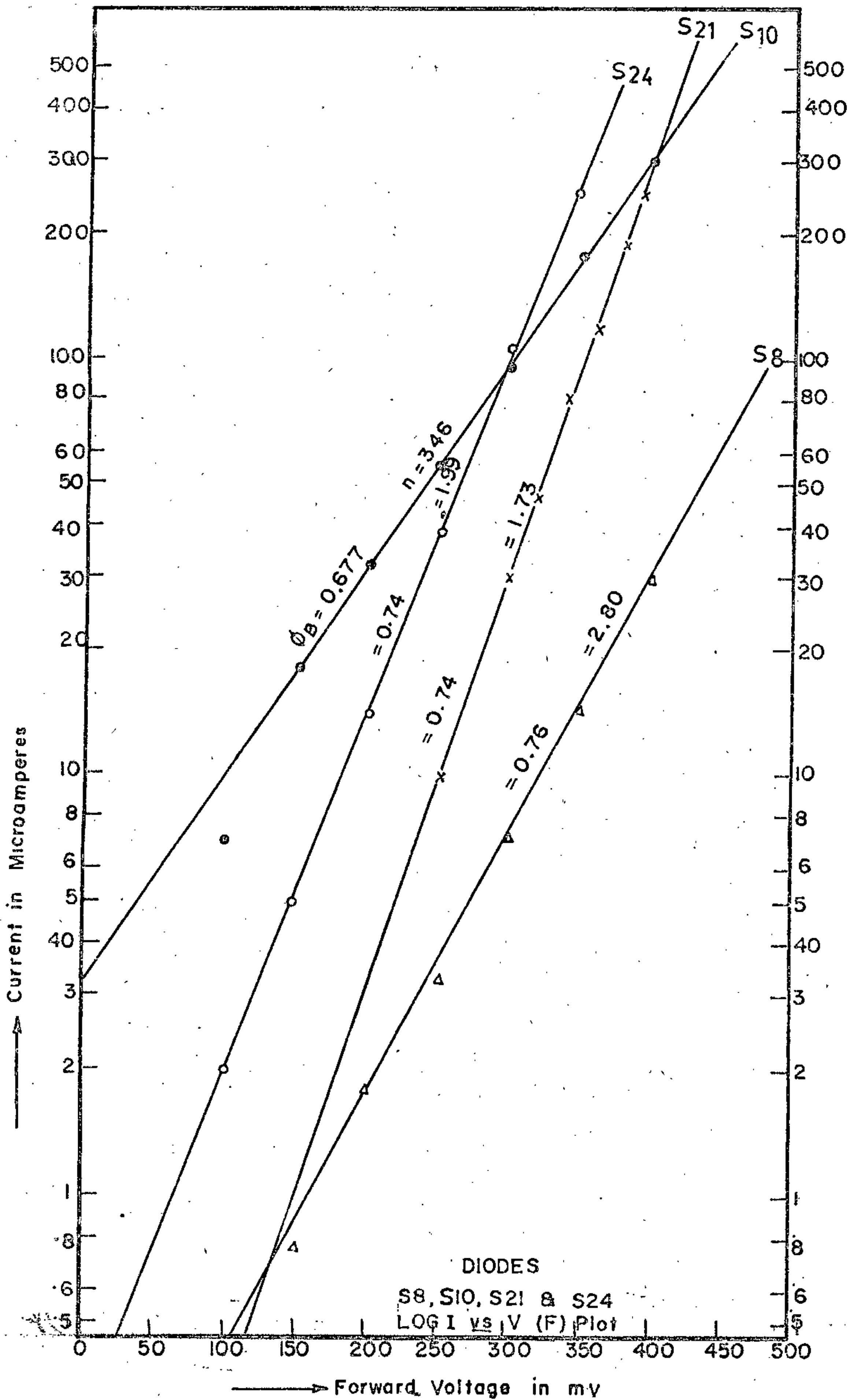


FIG.-5.5 LOG I VERSUS FORWARD VOLTAGE FOR SCHOTTKY DIODES

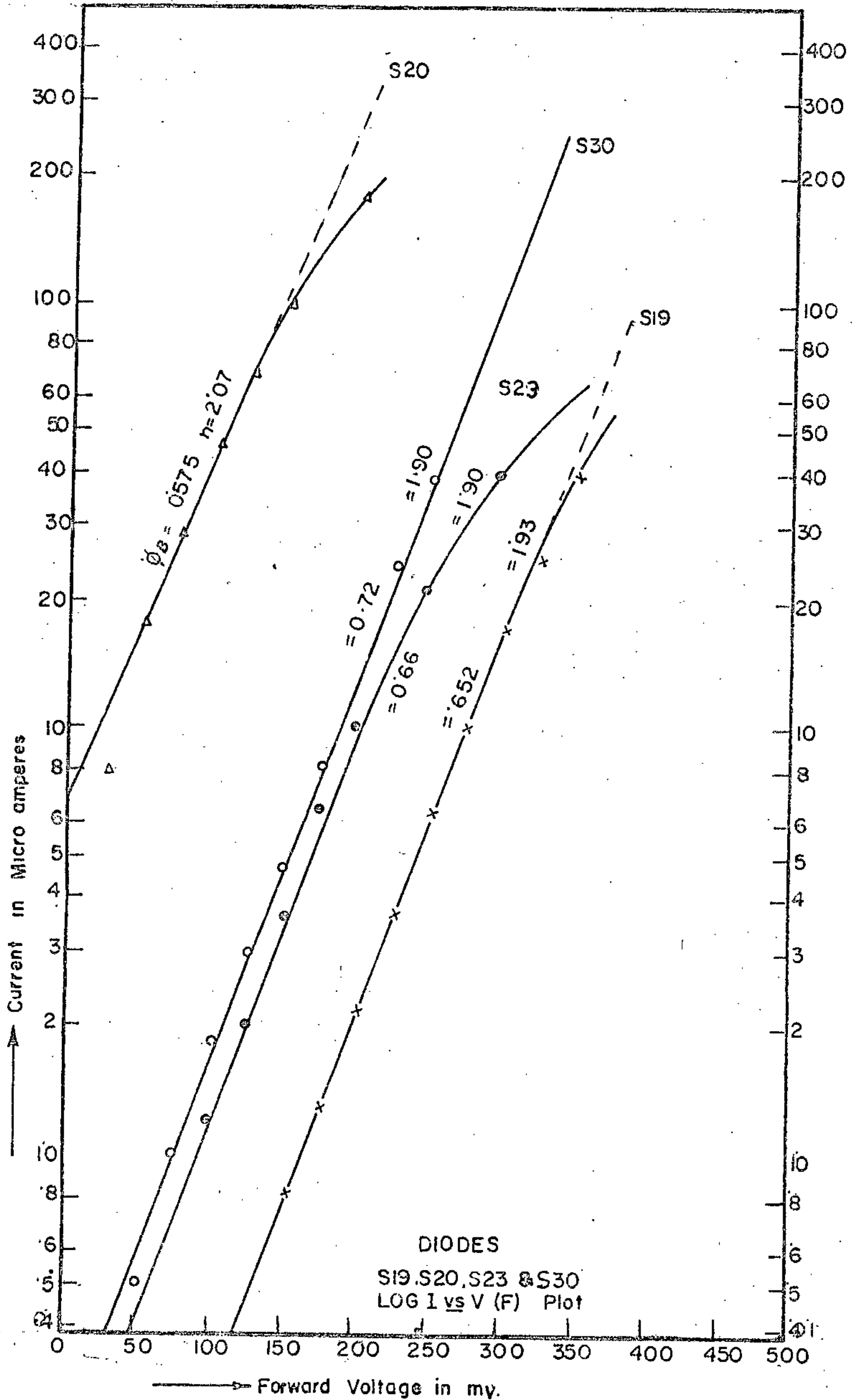


FIG. 5.6 LOG I VERSUS FORWARD VOLTAGE FOR SCHOTTKY DIODES

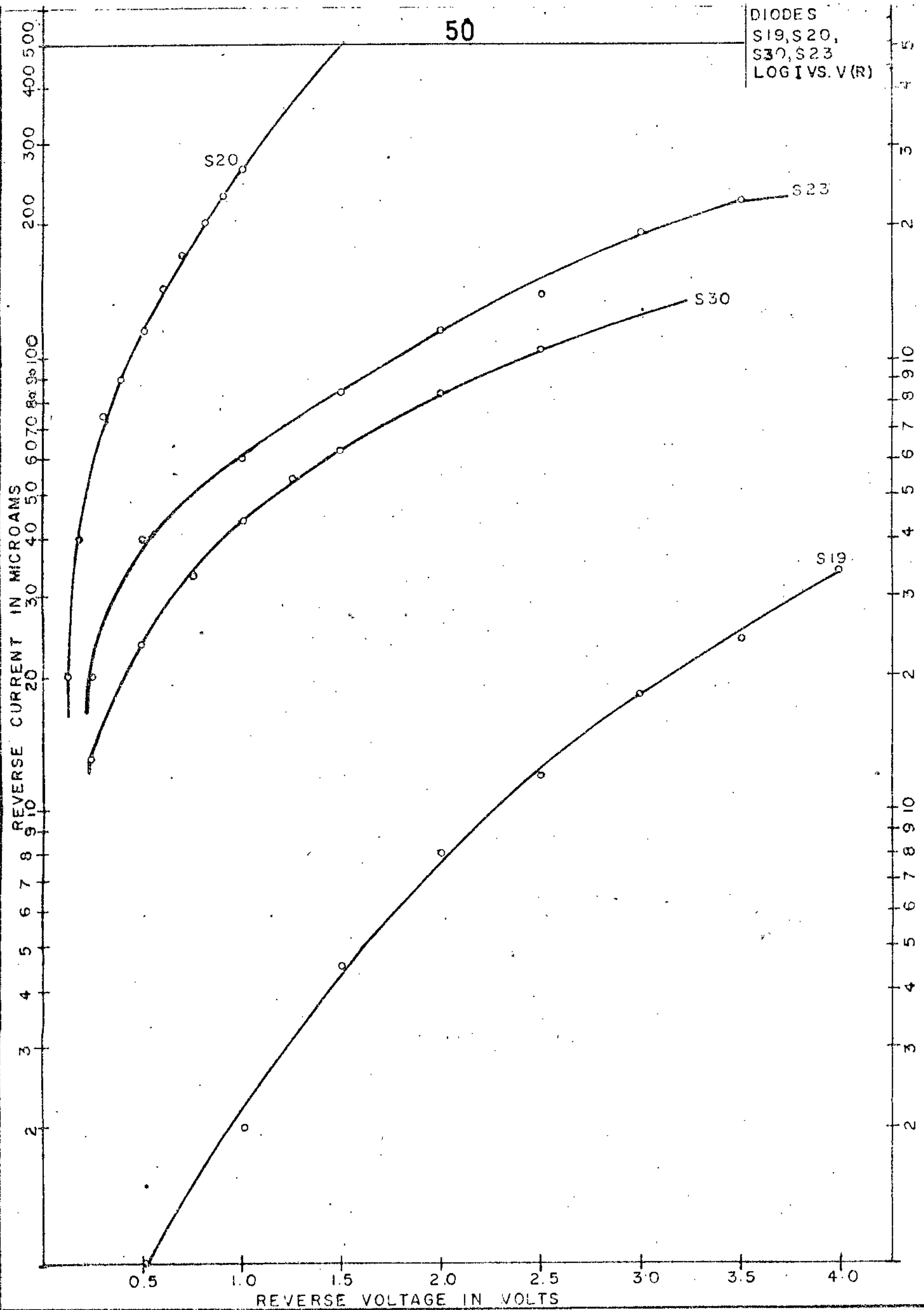


FIGURE 5.7 LOG I VERSUS REVERSE VOLTAGE FOR SCHOOTTKY DIODES

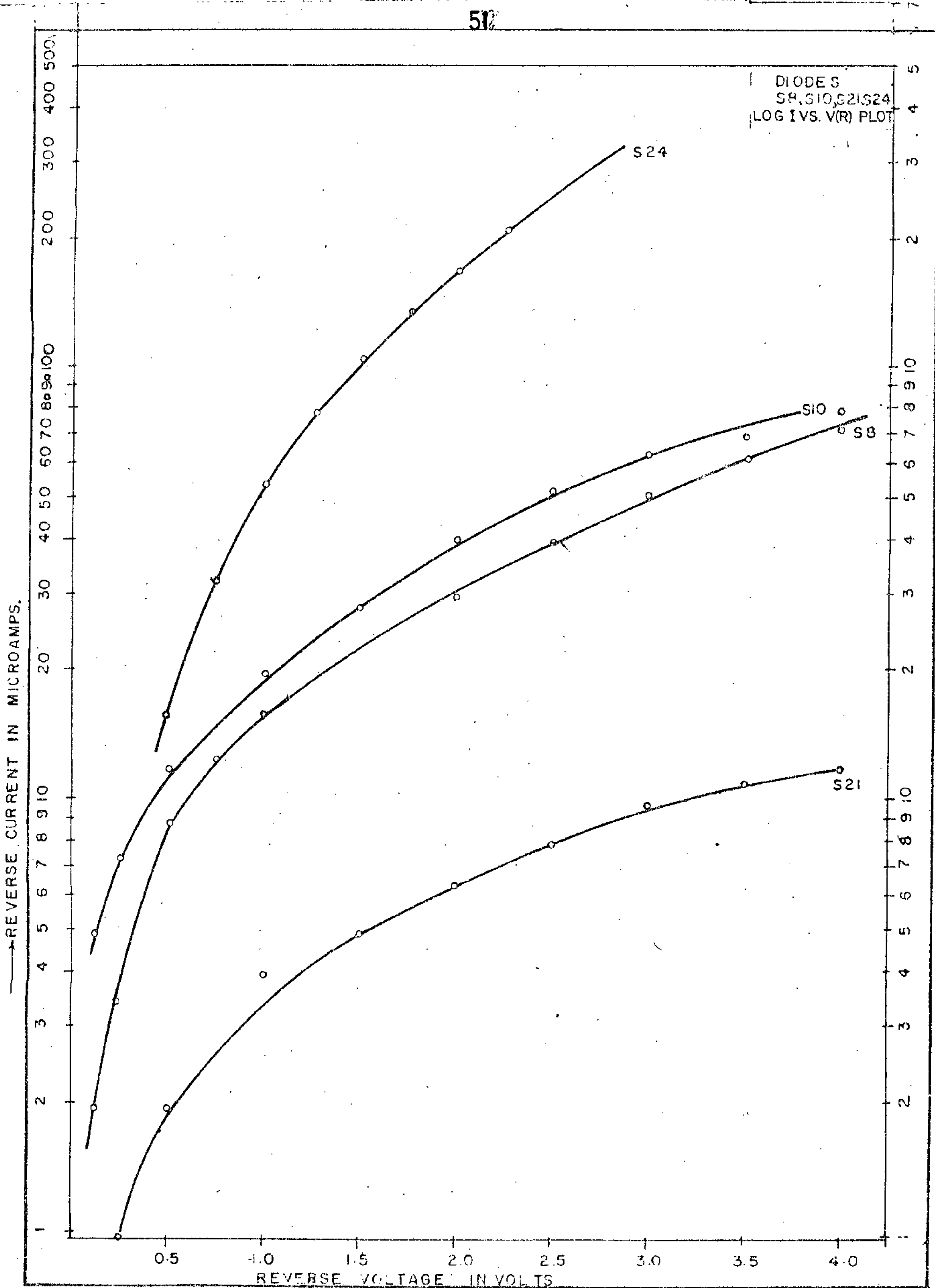


FIGURE 5.8. LOG I VERSUS REVERSE VOLTAGE SCHOTTKY DIODES

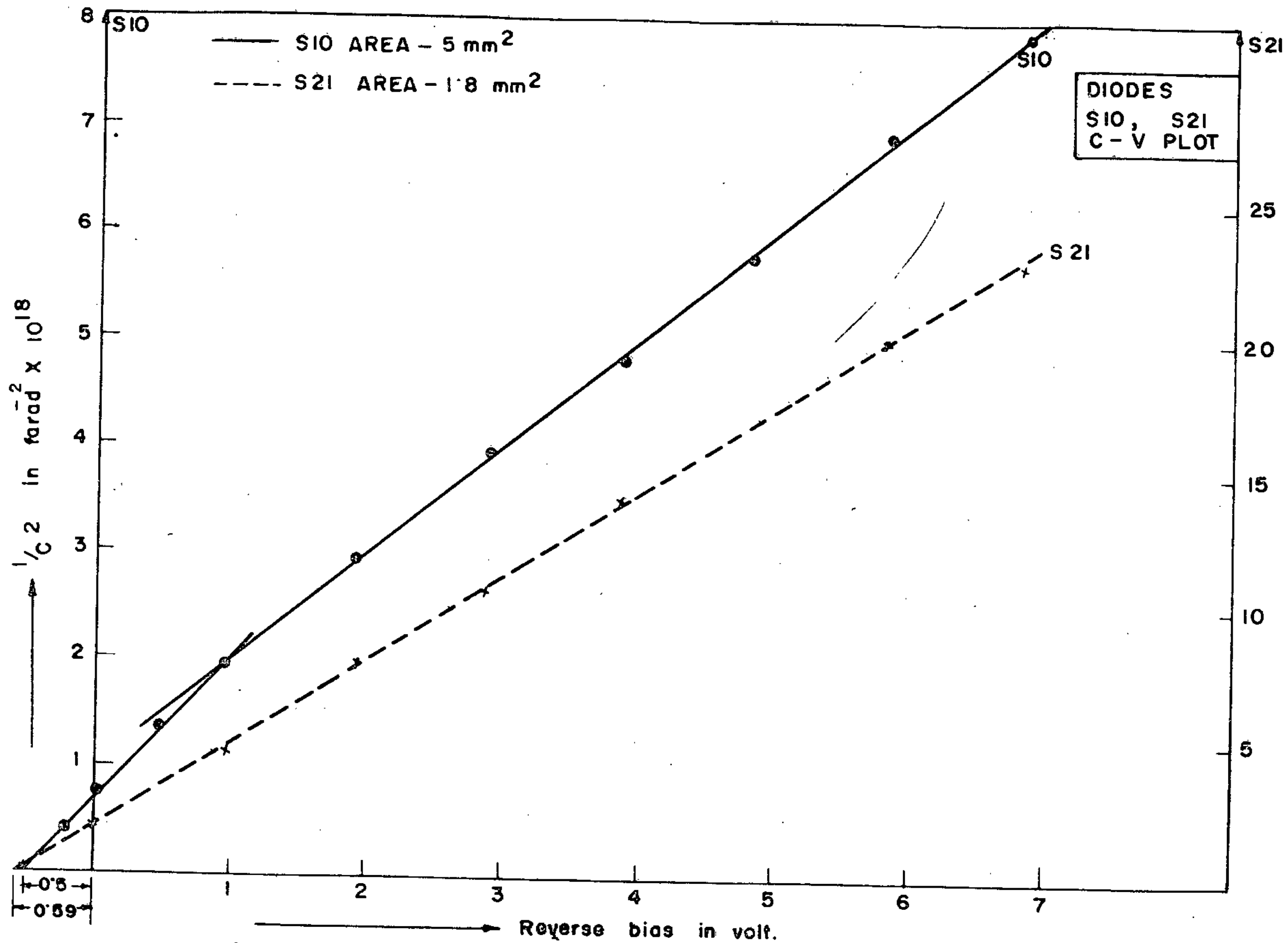


FIGURE 5·9 $1/C^2$ VERSUS REVERSE FOR ALUMINIUM – n – TYPE SILICON SCHOTTKY DIODES.

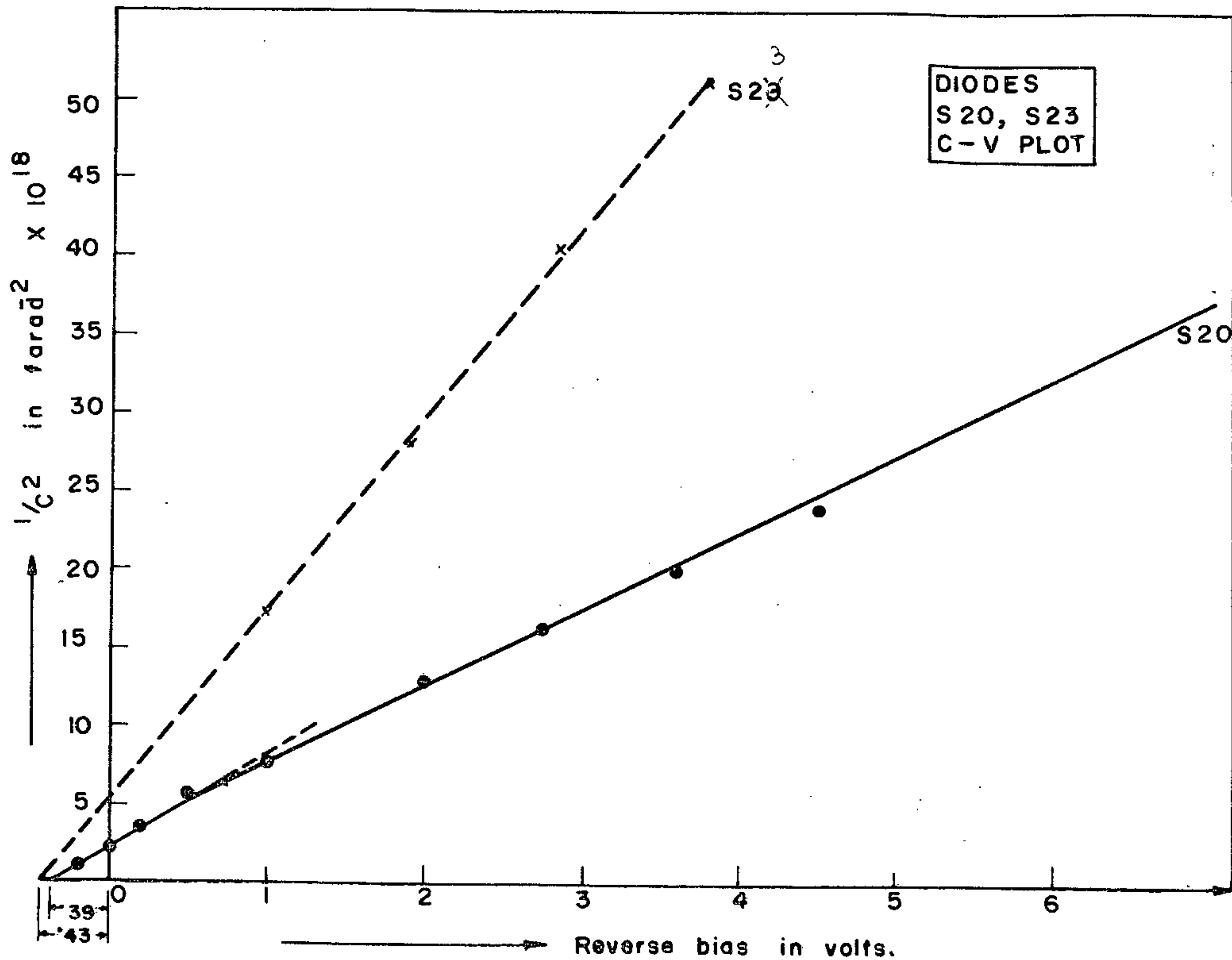


FIGURE 5·10 $^{1}/_{C^2}$ VERSUS REVERSE VOLTAGE FOR ALUMINIUM-p-TYPE SEMICONDUCTOR SCHOTTKY BARRIER.

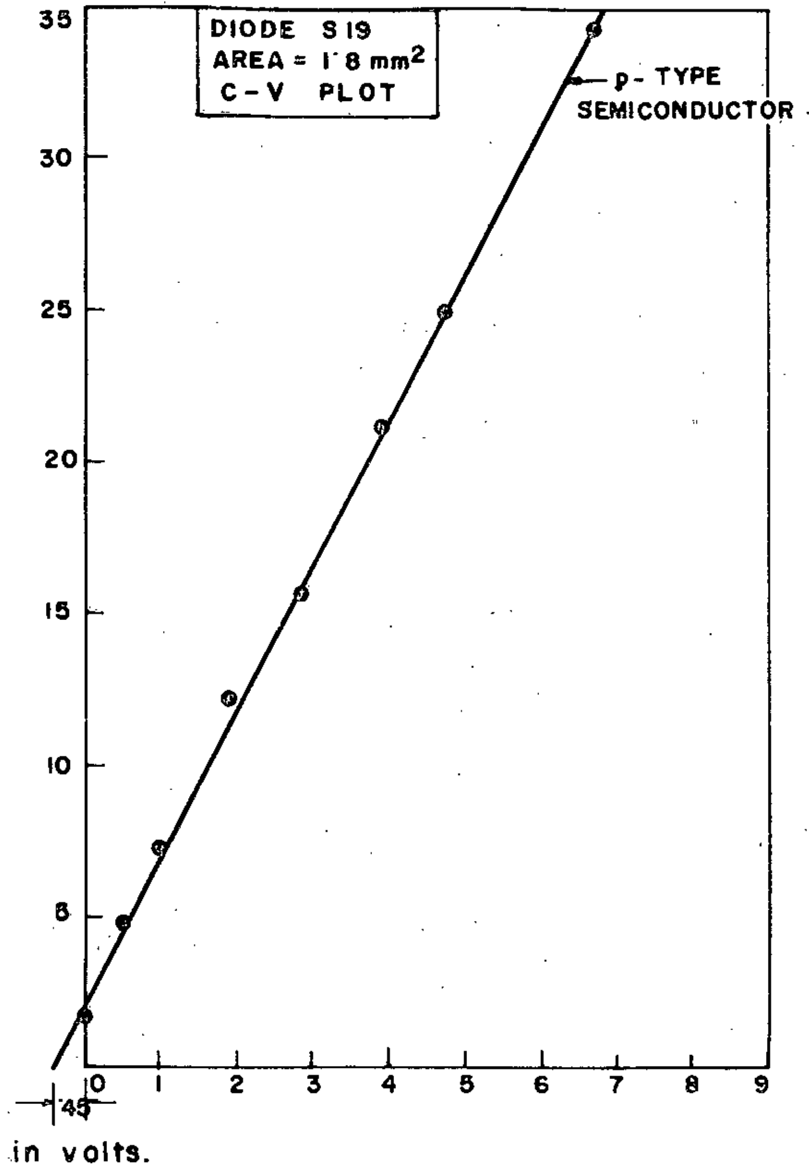
DIODE S8
AREA = 5 mm 2
C – V – PLOT

n - TYPE
SEMICONDUCTOR

$^1/_{C^2}$ in $farad^{-2}$ x 10^{18}

0 1 2 3 4 5 6 7 8 9

0·6



Reverse bias in volts.

FIGURE 5·11 $^1/_{C^2}$ VERSUS REVERSE VOLTAGE FOR SILVER – SILICON SCHOTTKY DIODES.

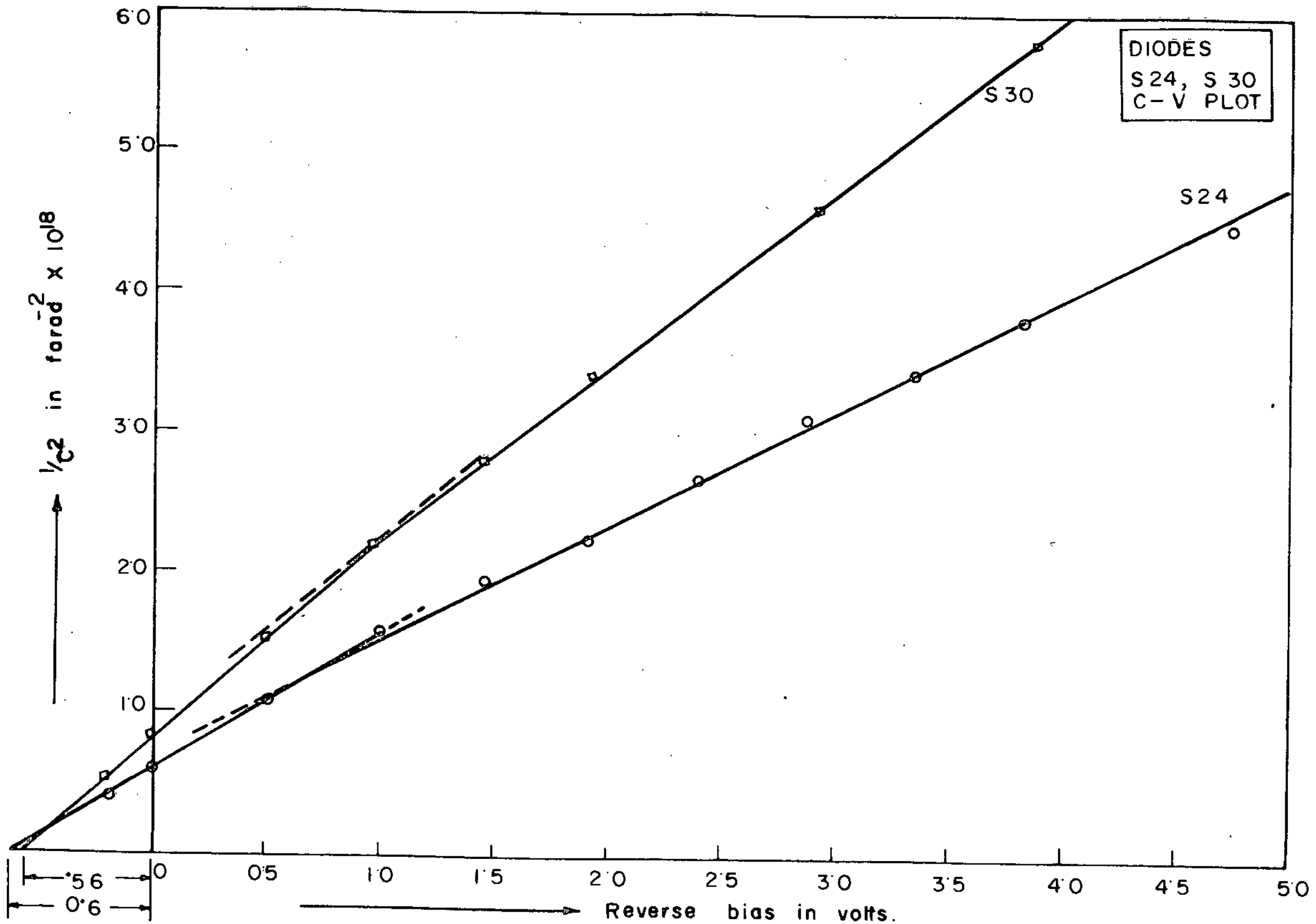


FIGURE 5·12 $1/C^2$ VERSUS REVERSE VOLTAGE FOR GOLD-n-TYPE SILICON SCHOTTKY DIODES.

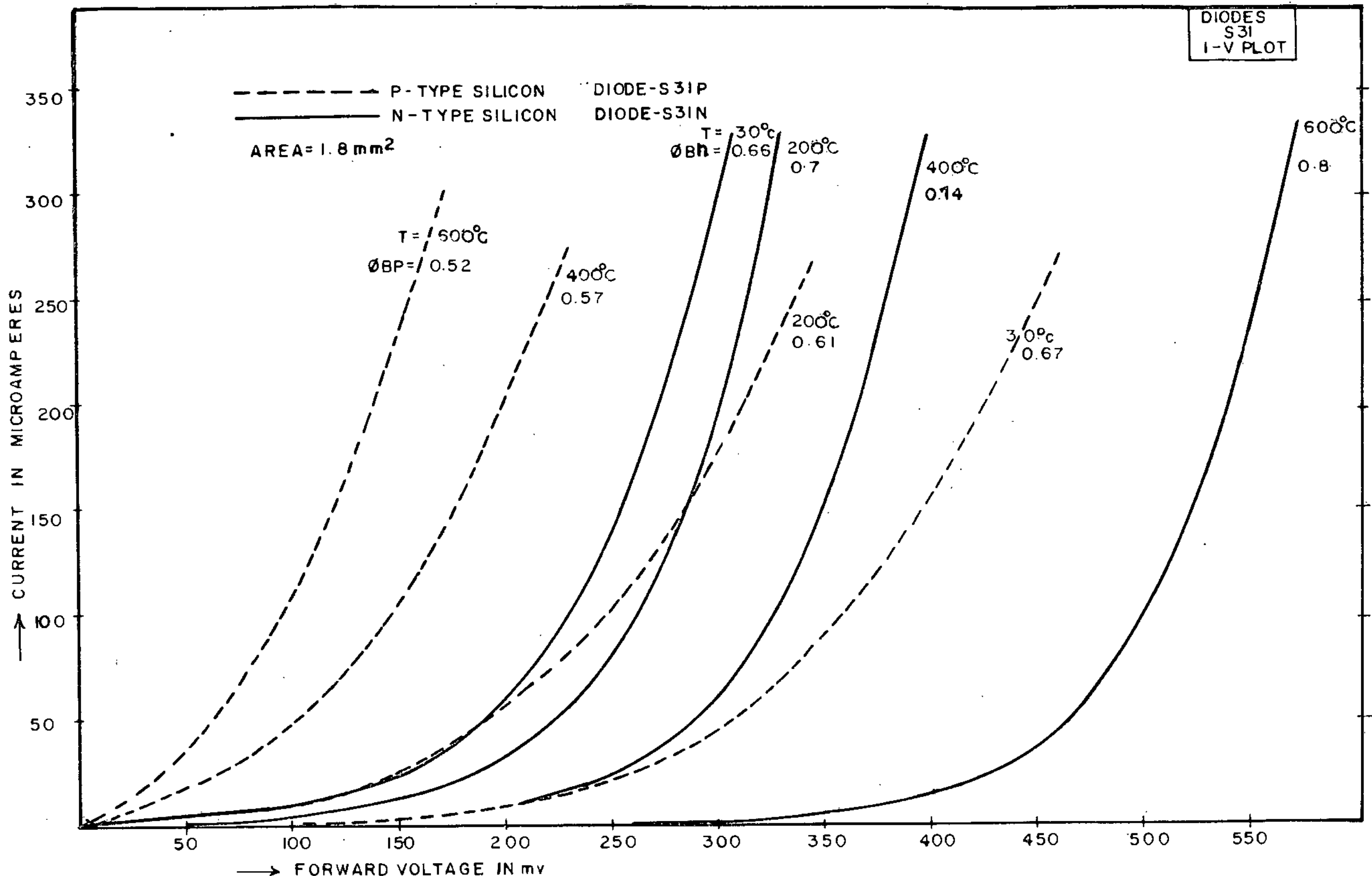


FIGURE 5.13 FORWARD CURRENT-VOLTAGE CHARACTERISTICS OF ALUMINIUM SILICON SCHOTTKY DIODES UNDER HEAT TREATMENT.

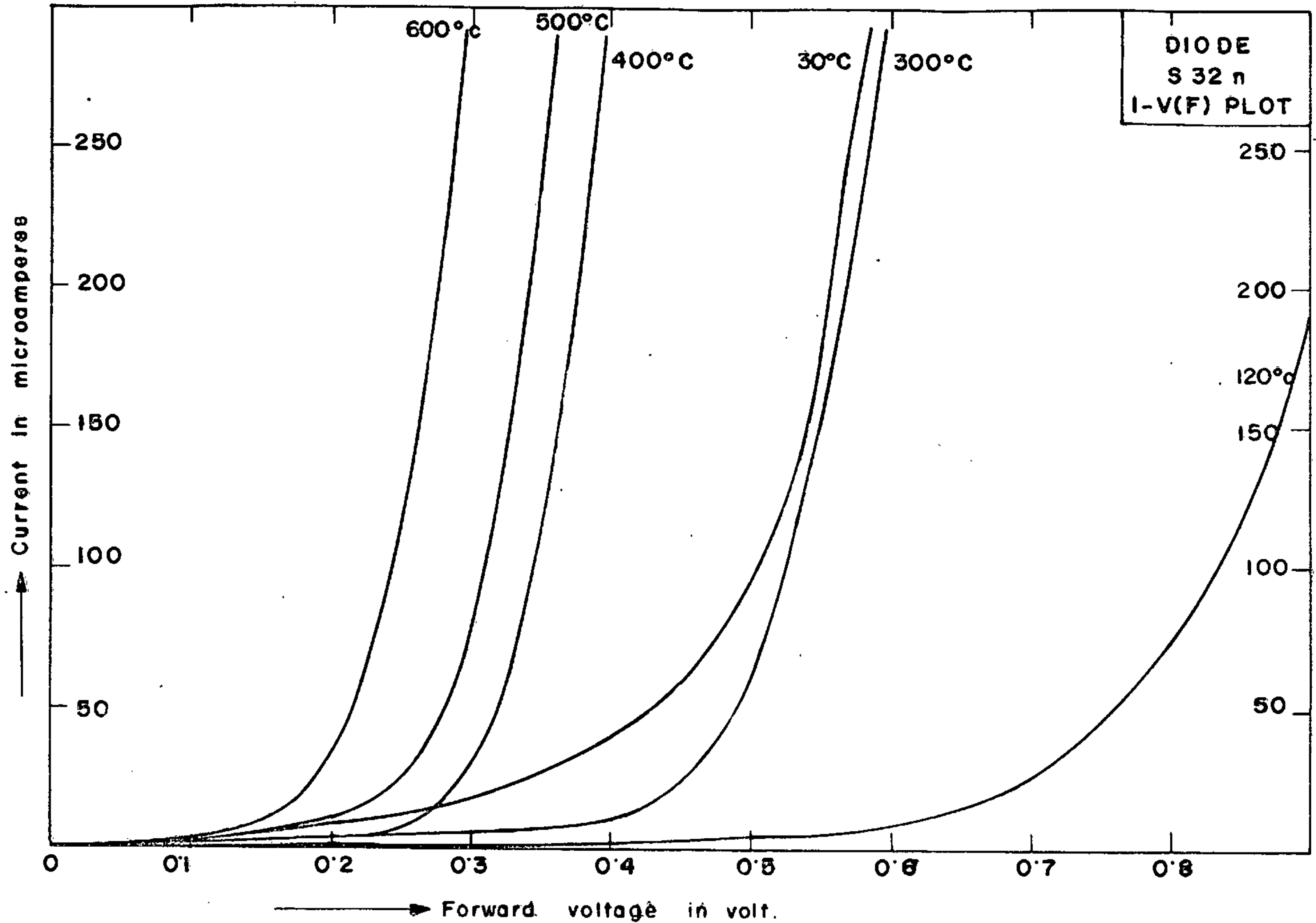


FIGURE 5·14 FORWARD CURRENT VOLTAGE CHARACTERISTICS OF GOLD—ALUMINIUM—n—TYPE SILICON SCHOTTKY DIODE UNDER HEAT TREATMENT.

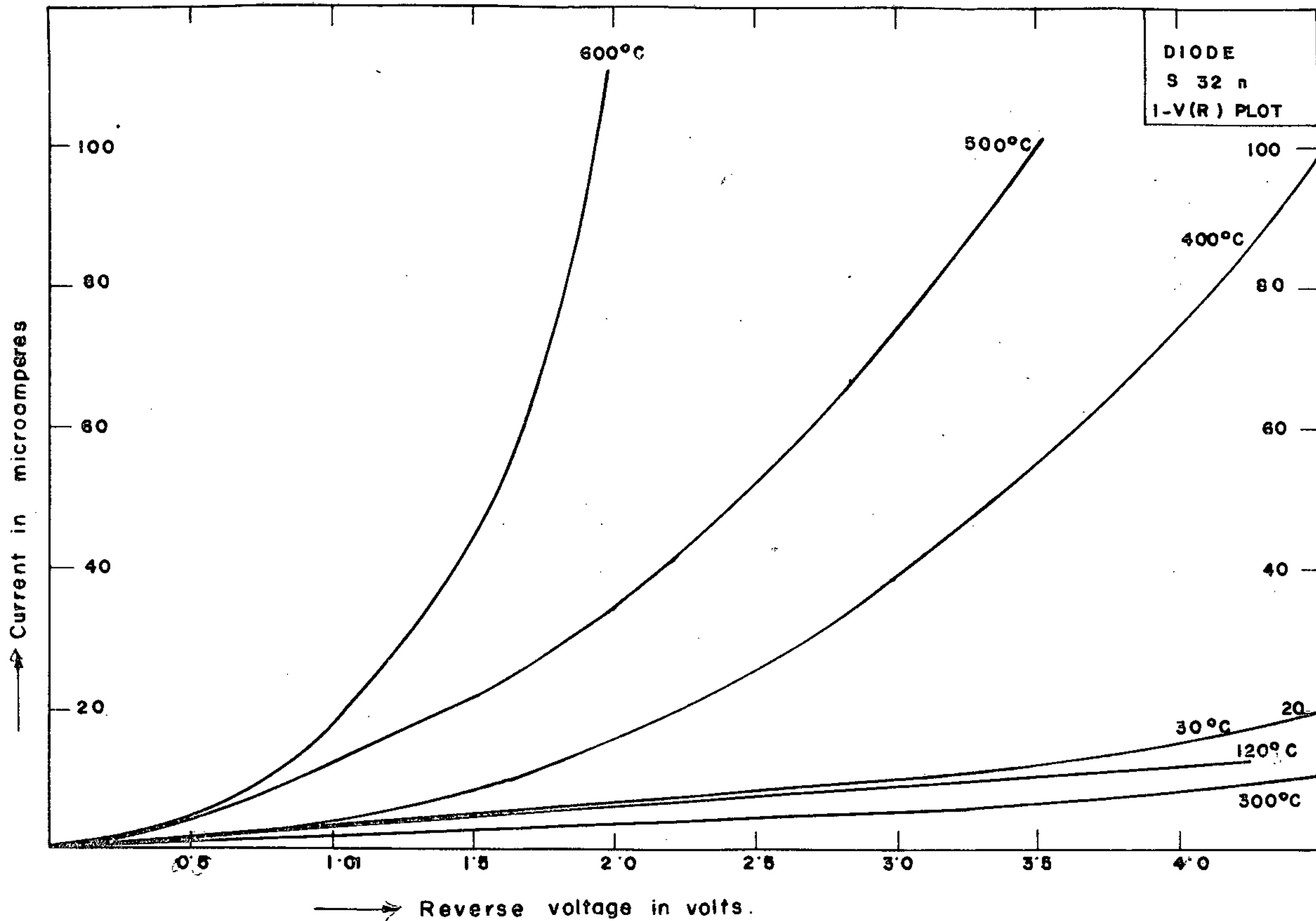


FIGURE 5.15 REVERSE CURRENT VOLTAGE CHARACTERISTICS OF GOLD – ALUMINIUM – n – TYPE SILICON SCHOTTKY DIODE UNDER TREATMENT.

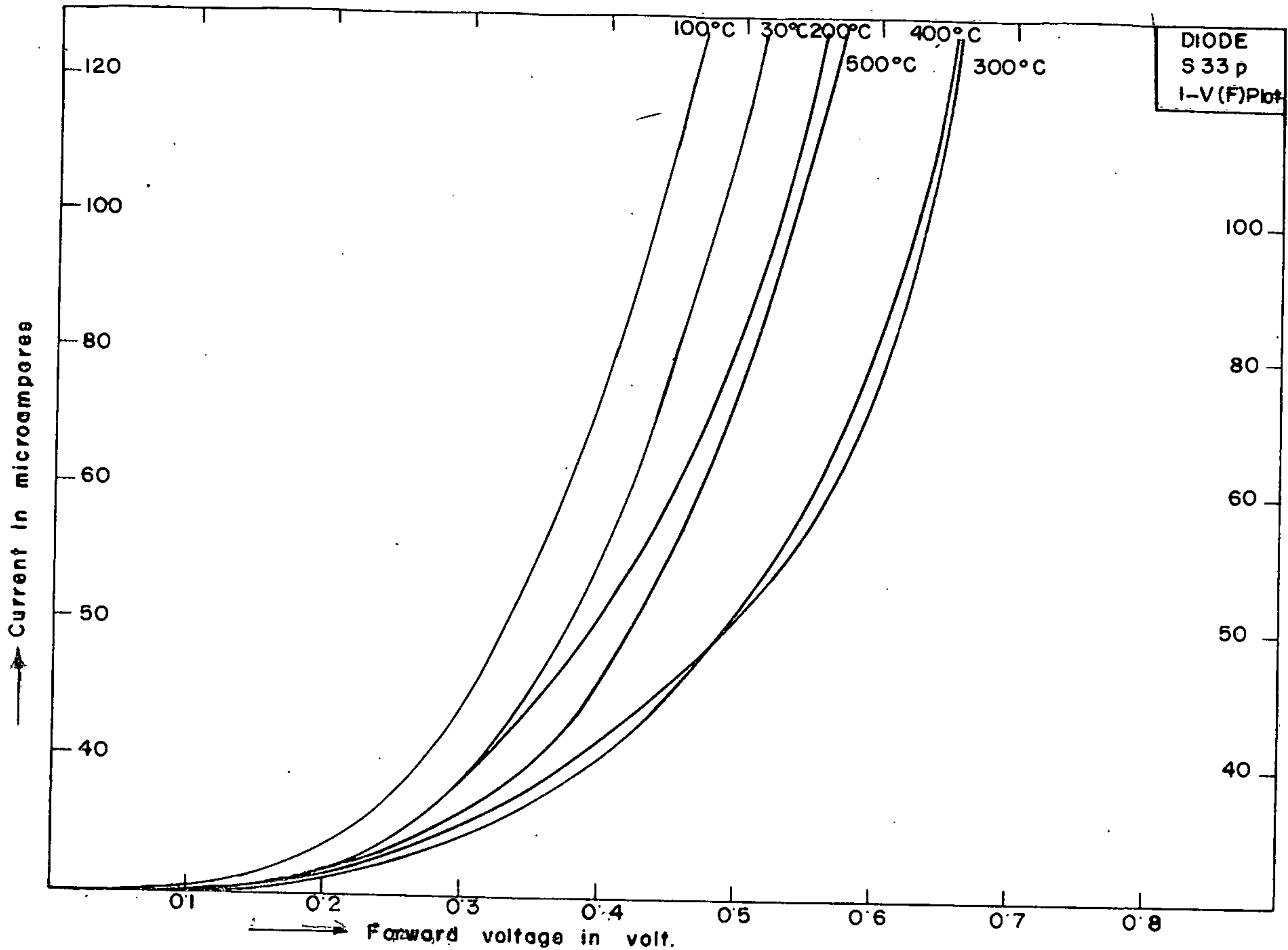


FIGURE 5·16 FORWARD CURRENT VOLTAGE CHARACTERISTICS OF GOLD - ANTIMONY—P —TYPE SILICON SCHOTTKY DIODE UNDER HEAT TREATMENT.

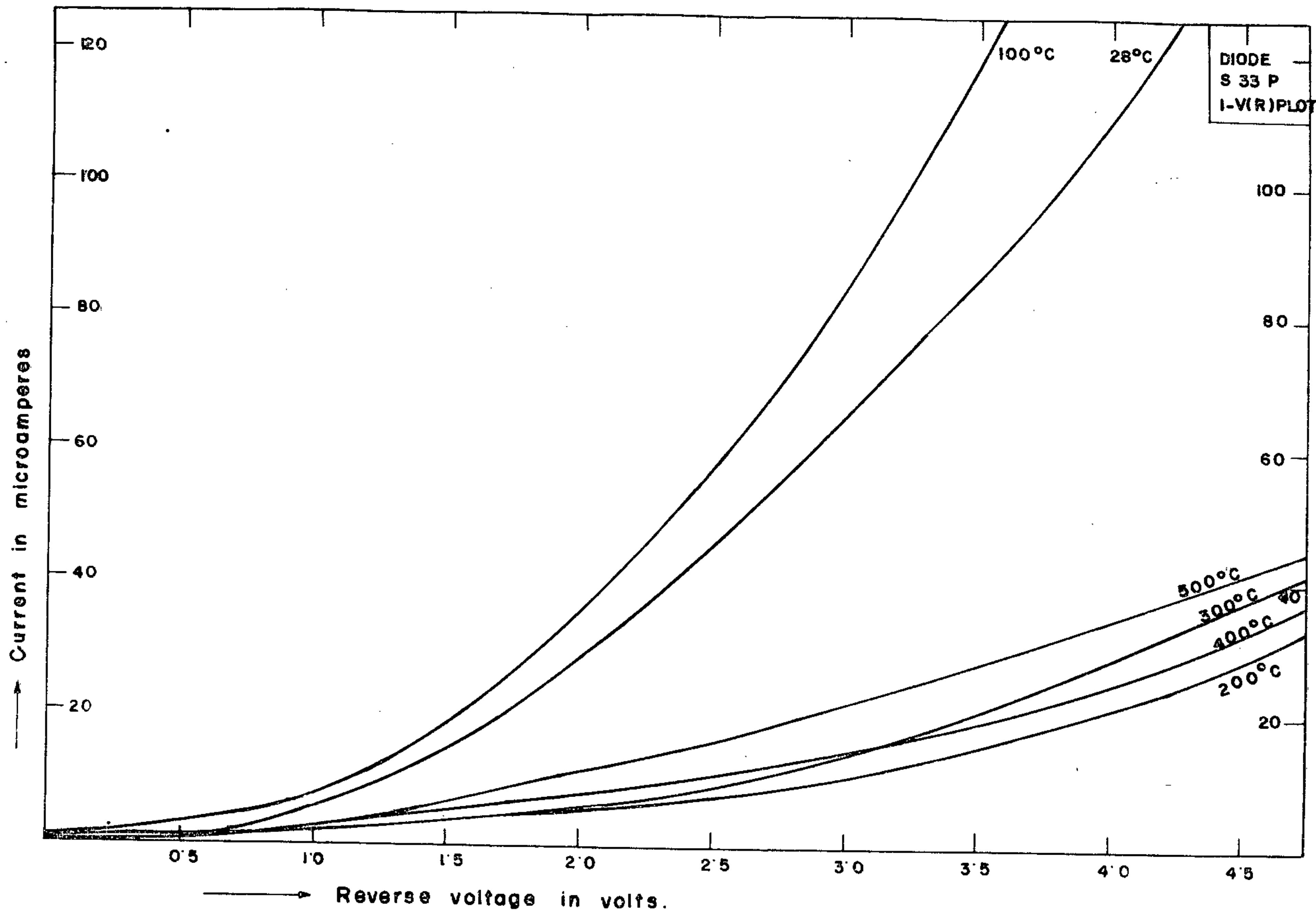


FIGURE 5.17 REVERSE CURRENT VOLTAGE CHARACTERISTICS OF GOLD-ANTIMONY—P-TYPE SILICON SCHOTTKY DIODE UNDER HEAT TREATMENT.

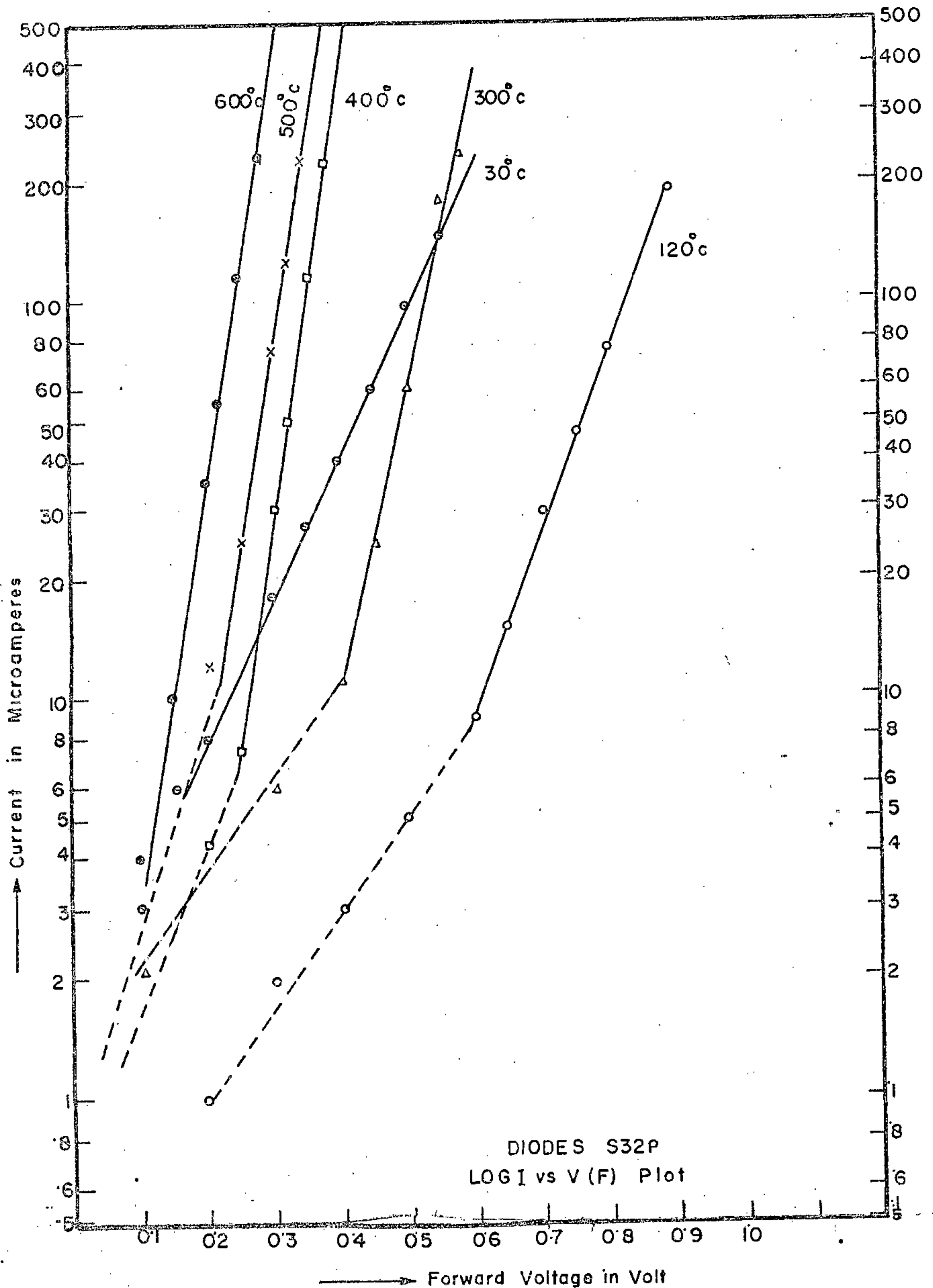


FIG. 5.18 LOG I VERSUS FORWARD VOLTAGE FOR GOLD-ALUMINIUM n-TYPE SILICON SCHOTTKY DIODES.

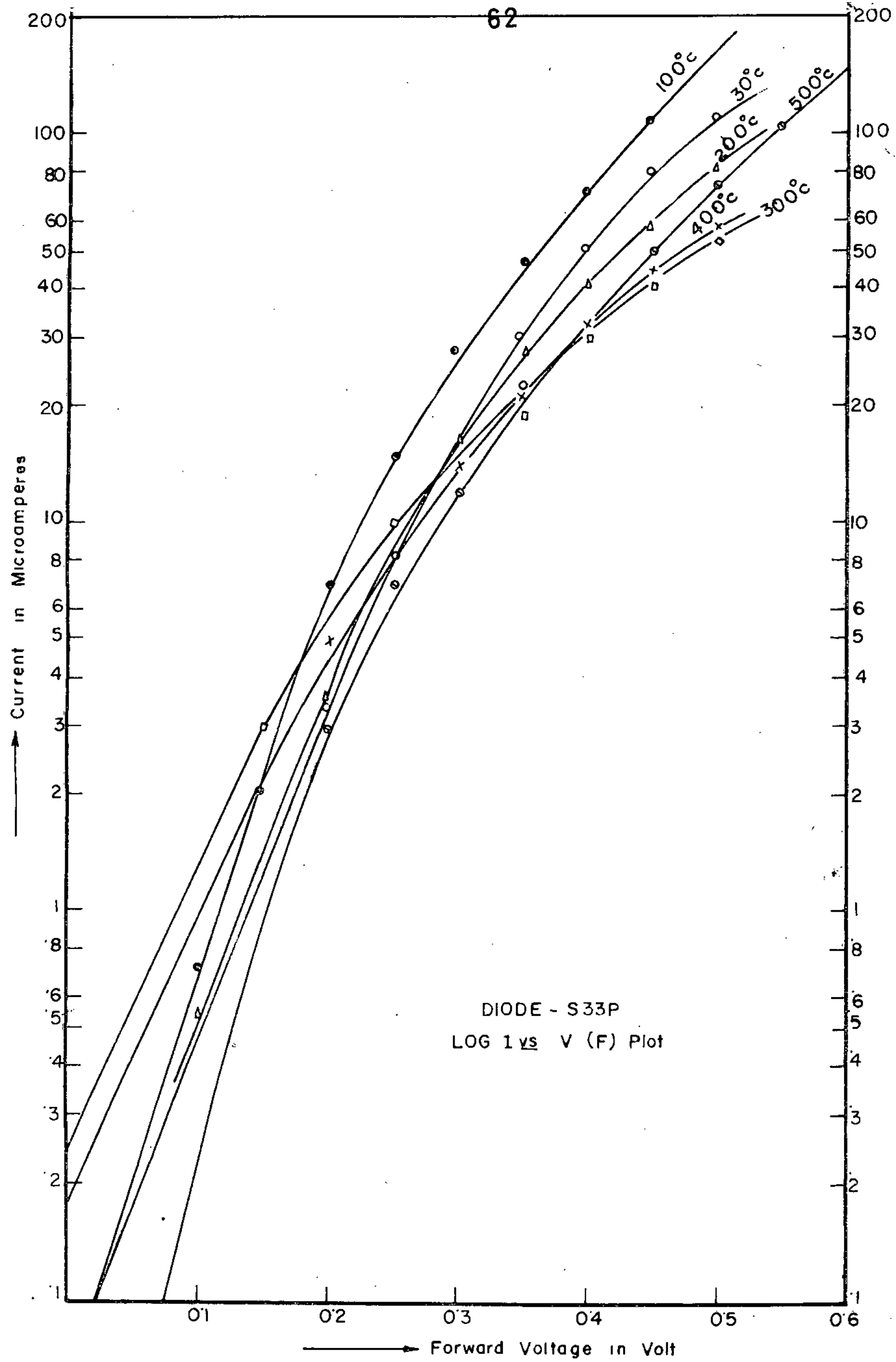
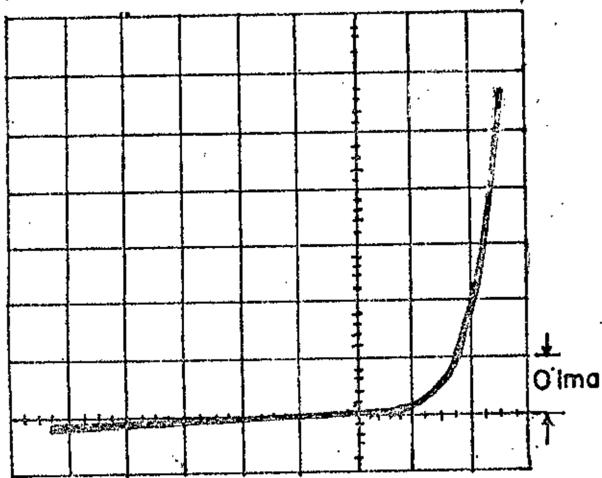
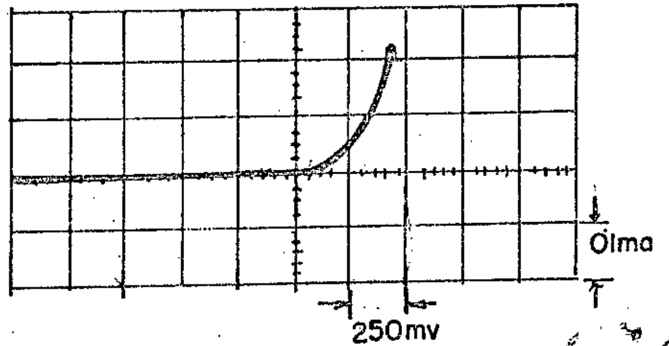


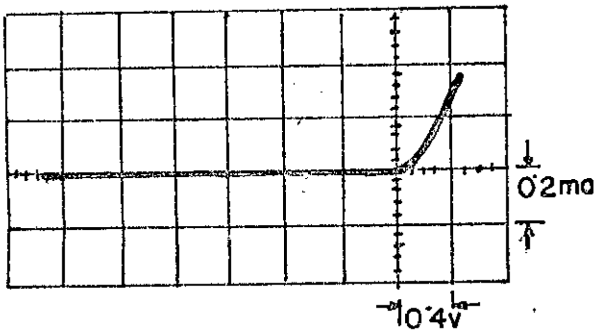
FIG.5.19 LOG I VERSUS FORWARD VOLTAGE FOR GOLD-ANTIMONY P-TYPE SILICON SCHOTTKY DIODES.



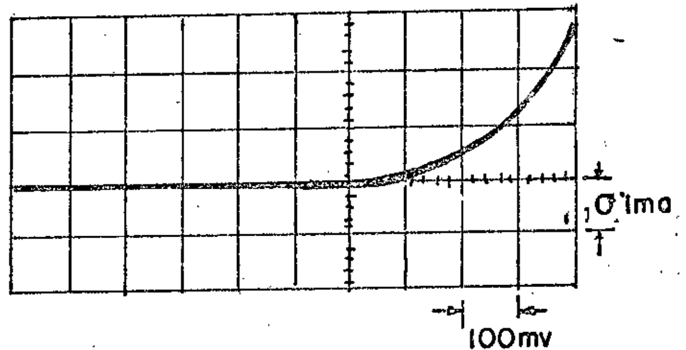
A: DIODE - S8



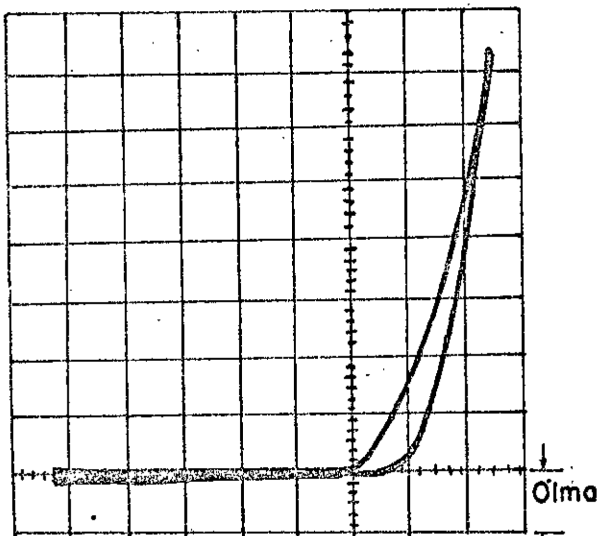
B: DIODE - S10



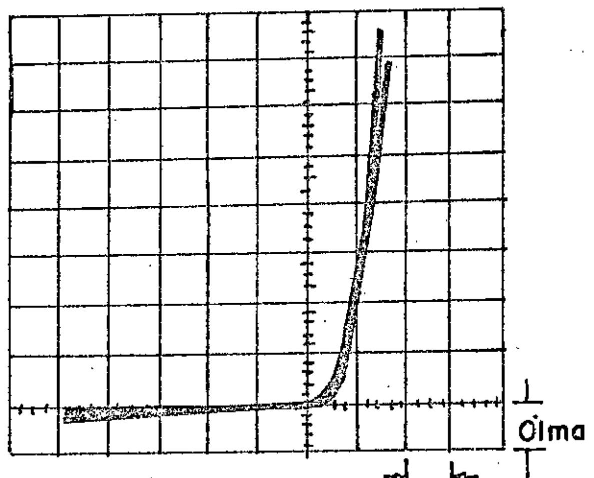
C: DIODE - S21



D1: p.n. JUNCTION



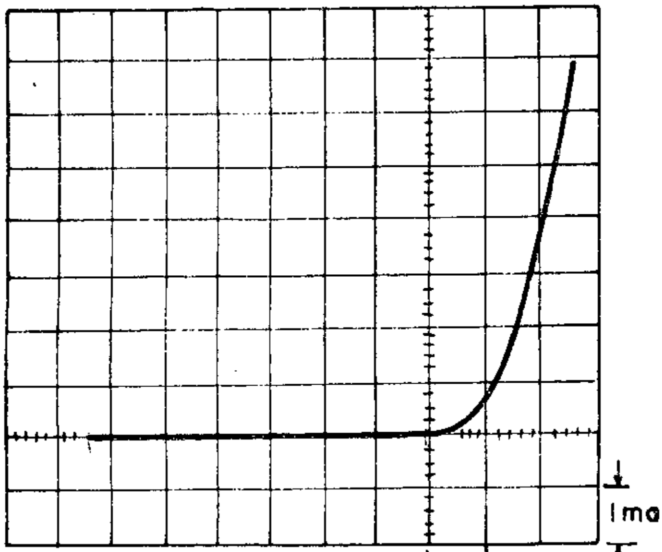
D2: DIODE - S23 (Upper)
S10 (Lower)



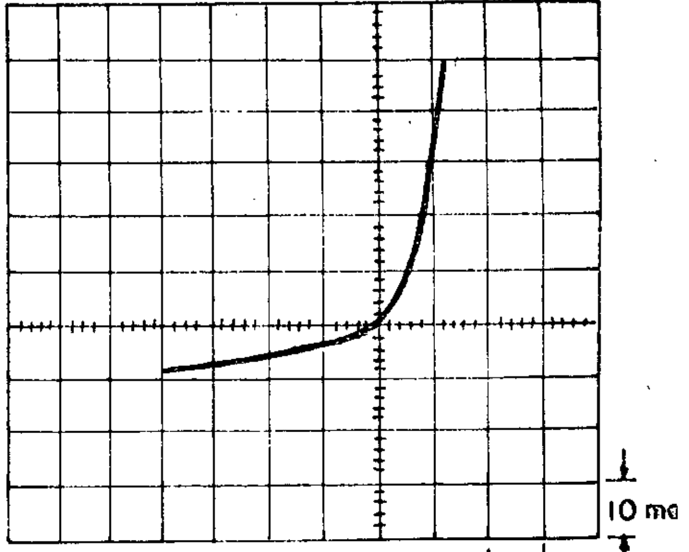
D3: DIODE - S10 (Upper)
S21 (Lower)

FIGURE-5.20 VOLT-AMP. CHARACTERISTICS OF SCHOTTKY DIODES

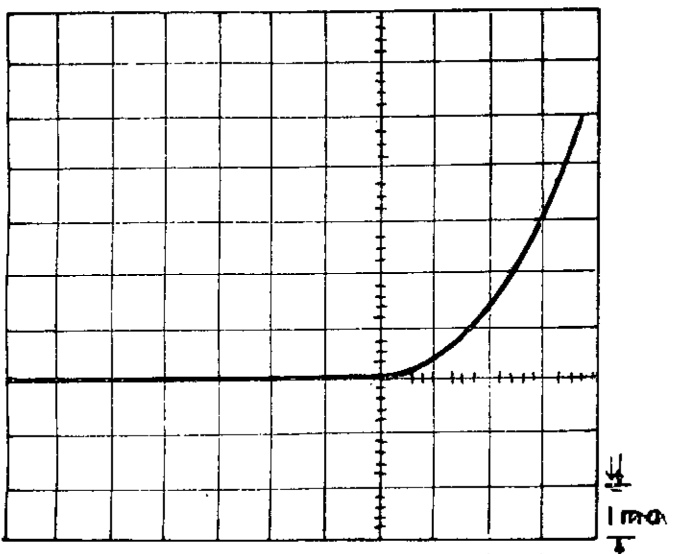
43646



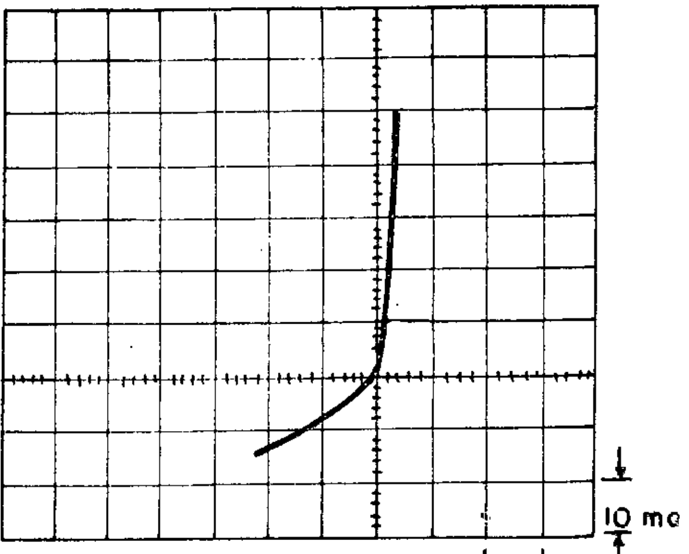
E: DIODE - S19



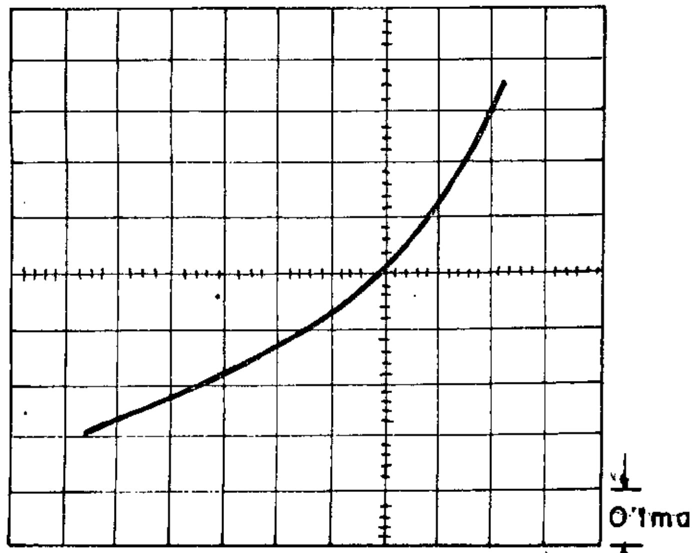
F: DIODE - S24



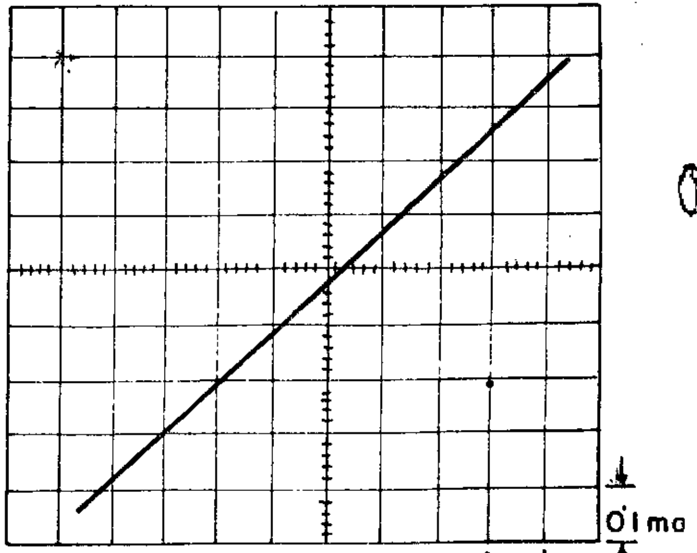
G: DIODE - S 23



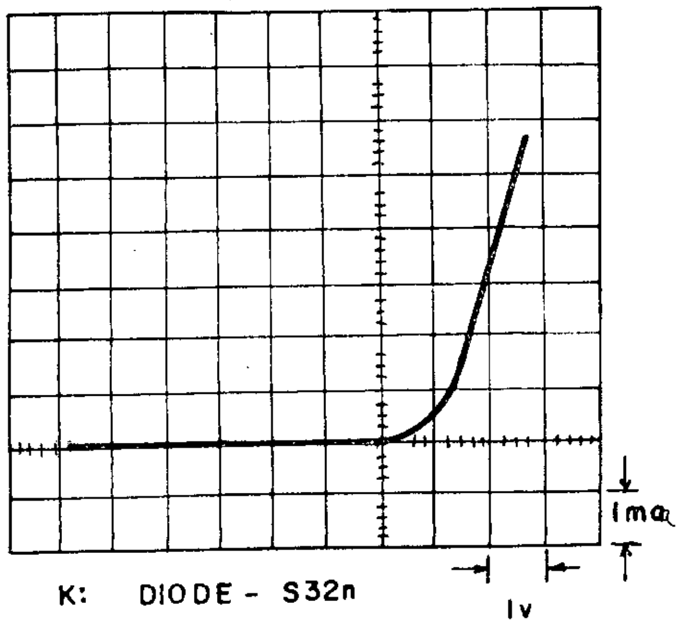
H: DIODE - S30



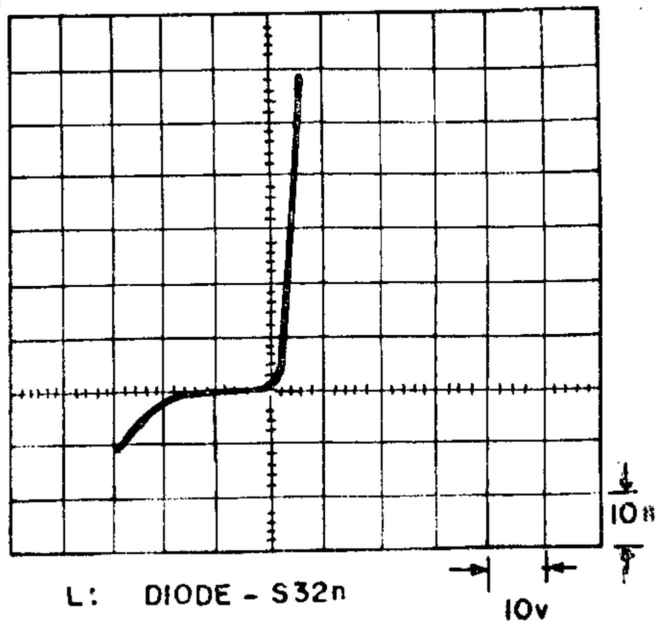
I: SAMPLE - S27



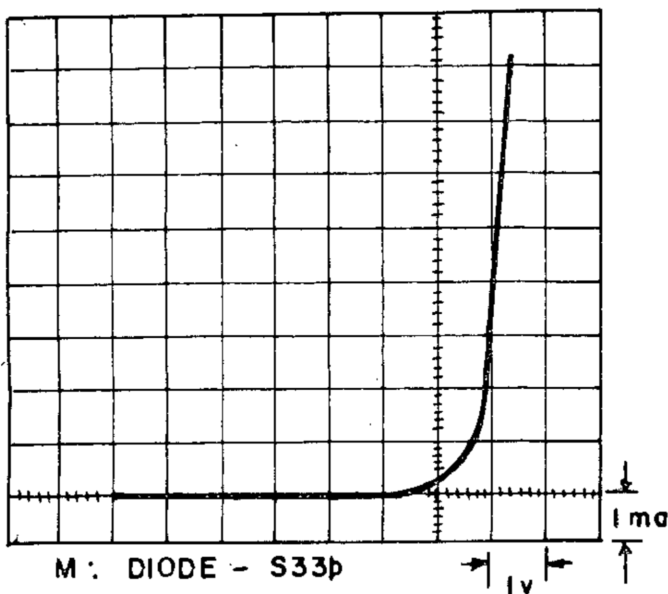
J: SAMPLE - S27 (120°C)



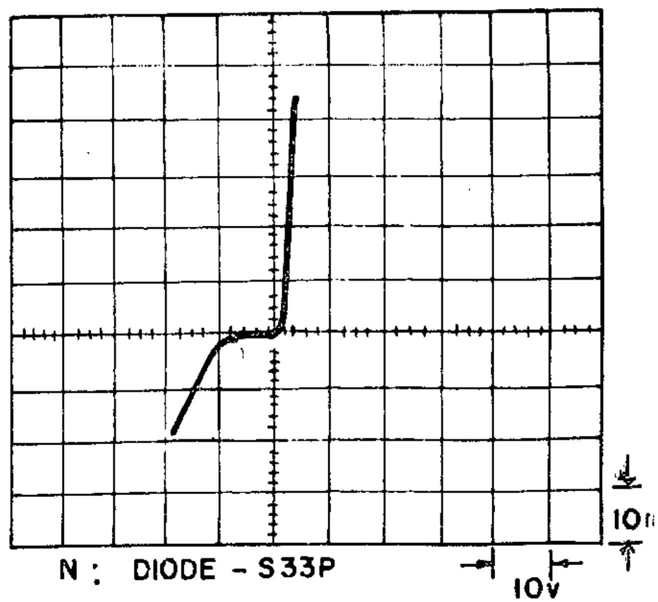
K: DIODE - S32n



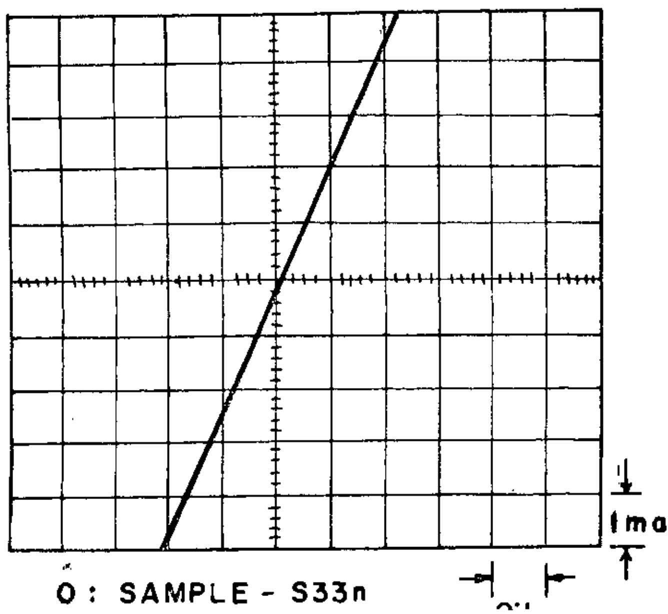
L: DIODE - S32n



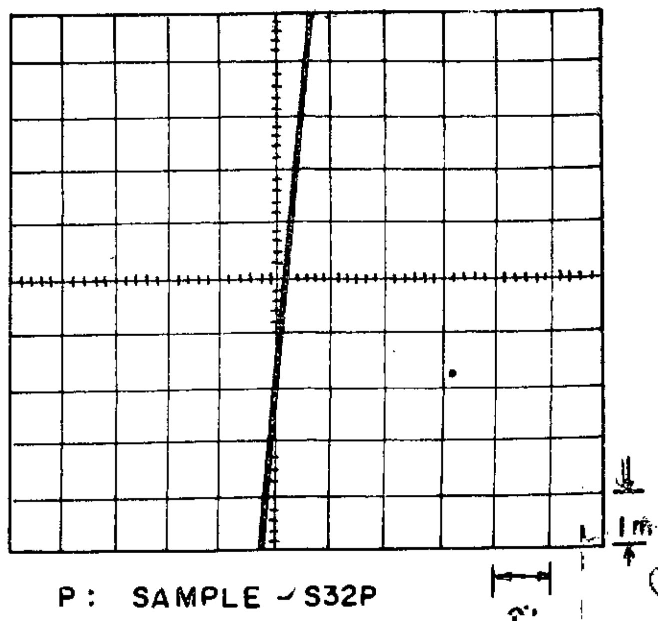
M: DIODE - S33p



N: DIODE - S33P



O: SAMPLE - S33n


P: SAMPLE - S32P

Interface states density has been estimated using the equation (2.23) at the reverse voltages. The quantity n_F is the same quantity as **n** and n_R is a similar quantity except in reverse direction. The capacitance at two reverse voltages were calculated from $1/C^2$ vs. reverse bias plots. The calculated values of inter-face- states density have been shown in Table-5.2. The thickness of interfacial oxide layer has been calculated from the model of Card and Rhoderick according to equation (3.12). In these calculations the permittivity of the oxide layer ϵ_i has been taken equal to (= 8.8542×10^{-14} f/cm).The dielectric constant of bulk Silicon dioxide is 3.9 but that of the interfacial oxide layer is different from bulk S_iO_2, it was assumed that $\epsilon_i = \epsilon_o$ as used by Sze(51) and Pulfrey(50). Also the resistivities corresponding to Shallow impurities of silicon used in fabrication of the diodes have been calculated and shown in Table 5.2.

TABLE 5.2

Diode series	Interface State Density N_{sb} in $cm^{-2}\ cv^{-1}$ at reverse voltages 0.5 v	2.0 V	Thickness of Interfacial layer in $\AA$	Resistivity in Ω-cm.
S8	2.35×10^{12}	6.34×10^{12}	15.78	0.7
S10	3.27×10^{12}	4.80×10^{12}	28.39	0.65
S19	3.76×10^{12}	3.07×10^{12}	13.3	1.80
S20	2.86×10^{12}	5.05×10^{12}	11.8	2.10
S21	3.0×10^{12}	4.07×10^{12}	12.4	0.15
S23	9x1012	1.88×10^{13}	2.5	4.40
S24	3.12×10^{12}	8.82×10^{12}	6.2	0.20
S30	5.84×10^{12}	1.47×10^{13}	3.4	0.25

The aluminium barrier was studied elaborately. The experimental results in Table-5.1 show that the barrier height obtained by I-V and C-V methods agree fairly well with each other. Freshly prepared aluminium barrier on n-type material (S10) is 0.675V which is slightly less than the expected value of 0.7V. Also freshly prepared aluminium barrier on p-type silicon (S23) the barrier height is 0.625V which is higher than the nominal value of 0.55V. This is due to the fact that interfacial oxide layer contains positive charges[57] which are immobile to the applied potential. The presence of fixed positive charges has also been mentioned by Card and Rhoderick [39]. The positive charges were found to be present in the form of positively charged Sodium (Na^+) and Potassium (K^+) ions[58]. Also presence of some stable positive charges are found at $S_i - S_iO_2$ interface which arises due to nonstoichiometric silicon-oxygen structure at the interface. If these positive charges are concentrated at the interface then a deviation of barrier height $\partial\phi_B$ can be given by $\partial\phi_B = q\, N^+\delta/\epsilon_i$ where N^+ is the density of positive charges. Thus a deviation of 0.1V arising due to a δ=10 Å gives the number of positive charges present to be of the order of 10^{13} cm^{-2}.

Heat-treatment of aluminium-n-type silicon barrier showed that ϕ_{Bn} increased upto 0.77V when heated to 400°C for 4-5 minutes as in diode S21. And aluminium p-type silicon barrier (S20) showed that ϕ_{Bp} decreased from 0.625 V to 0.57 V when heated at 450°C for 3 to 5 minutes. In all cases the samples were cooled slowly by leaving them in the furnace at least for an half an hour.

This effect showed that heat-treatment cause some of the fixed positive charges to be removed from the interface. But the dominant effect was that a high-temperature heat-treatment causes formation of an aluminium-silicon phase which on cooling becomes a silicon surface highly doped with aluminium. Thus in a n-type barrier a p-type surface layer was formed which reduced the semiconductor surface electric field and thus increasing the barrier height. But this gave better reverse characteristics because of lesser effect of image force barrier lowering. And in p-type barrier the aluminium doped silicon interface increased the semiconductor surface electric field which reduced the barrier height, consequently deteriorating the reverse characteristics. This has been varified with diodes S31n and S31P where the same sample was heated at high temperatures (0–600°c) as shown in figure -(6.13).

Freshly prepared gold barrier showed similar characteristics as aluminium barrier. ϕ_B with heat treatment showed a little change because no acceptor- like layer was found there. Slight change of barrier height was attributed to removal of some of the positive charges in the oxide of silicon. The p-type gold barrier was different to obtain at room temperature. A freshly prepared p-type gold-barrier showed ohmic nature as seen in figure -5.20(I) which quickly turned to ohmic contact at 120°C as shown in figure -5.20(J).

Similarly freshly prepared silver barrier contained fixed positive charges in the oxide layer. No noticeable effect of heat-

treatment on barrier height was observed rather it gave better reverse characteristics.

In samples S32 and S33 two metals were deposited in succession. Aluminium-gold were deposited upto a thickness of 50°A and 1000°A respectively on n-type (S32n) and also on p-Type (S.32 p) silicon. In S32n diode the barrier was initially low but increased upon heat treatment. Heat treatment upto 400°C, the log Vs. V plot (Figure-5.17) showed two slopes in forward direction where the straight line at lower voltage the barrier was aluminium-like and at higher voltage it behaved like a gold barrier. Heat-treatment at high temperature eventually turned it into a gold-barrier having high barrier height. This was explained dueto formation of an aluminium-doped silicon interface between gold and silicon. This aluminium-gold barrier(S32p) with p-type silicon turned into good ohmic contact by heat-treatment at 120°C as evident from figure 5.20(p). Reverse characteristics in S32n was found to be better because of the same reason as in diode S21. This became clear from a study of the figure 5.20(L) and **5.20 (K)** where reverse characteristics showed good result upto 12 V. Similarly in diode- S33p where antimony and gold were deposited upto thickness 100°A and 1000°A respectively, did not show any significant change in the value of barrier height (fig.5.19) with heat-treatment. But such contact (S33n) with n-type silicon resulted in ohmic contact at 300°C as shown in figure 5.20(O).

The ideality parameters n of the diodes were inferior compared to the of near-ideal values. As in the model of Card and

Rhoderick (App- B) here also larger values of n was a function of thickness of interfacial oxide layer. Heat-treatment did not show any noticeable change in value of n except in S32n and S33p diodes where the condition was different because of formation of an alloy and a layer of silicon doped with n-type or p-type impurity at the interfaces. From Table -5.2 it is seen that the oxide layer is thick enough so it was assumed that interface state density communicated with silicon only. It was also observed that the thickness of oxide layer was nonuniform because this oxide layer had developed in atmospheric condition. Moreover it is assumed that the interface state density is independent of thickness of oxide layer [57] but was found to be slightly dependent upon reverse bias.

The reverse characteristics were found to be deteriorated in gold barriers - S24 and S30 because of their enhanced effect of image force barrier lowering($\Delta\phi$). This is due to the fact that they had higher doping of the substretes as seen in Table 5.1. Also dominant effect of image force lowering is observed in diode S-20 because this diode was heat-treated at high temperature as a result aluminium doping of silicon increased the doping of silicon surface. For build-in potential of V_{bi} = 0.5V, $\Delta\phi$ is about 15 mV and with applied voltage of V = 1 volt in reverse direction $\Delta\phi$ increases to 25 mV. Thus it shows that though theoritically this effect caused by applied potential is of second order, the leakage along the edge of the surface of the semiconductor makes it more important in practice resulting in the deterioration of the reverse characteristics.

The presence of traps have been detected in a number of samples as shown in Table 5.1. Their presence affected the density of semiconductor surface-states and the reverse current of the diodes. The emptying and filling of trap levels are bias dependent. The largest number of traps were found in gold barriers and these diodes showed deteriorated reverse characteristics as shown in fig. 5.4 because of possible emission from the traps level under the influence of increased field at the interface due to reverse bias. Recombination and generation within the depletion layer had not been studied, but their effect could not be neglected because the ideality parameter n was large. Also surface-states accenuates recombination [59]. Similarly generation also was responsible for increased reverse current.

The effect of minority carrier injection ratio γ becomes important at high current density. For a certain value of current the ratio J/J_o would be highest for gold-silicon barrier and the ratio J/J_o determines the ratio γ/γ_o , (where J_o and γ_o are two constants those are defined in appendix -D). It was found[30] that in gold-silicon barrier that in order to have a γ equal to 5%, it would require the current density to be 350 amp/cm^2. But such high value of current density is far beyond the useable range of such diodes. So the effect of γ had not been considered.

CHAPTER - SIX

CONCLUSIONS AND RECOMMENDATIONS

6.1 CONCLUSIONS AND RECOMMENDATIONS

Reproducible Schottky barrier diodes with controlled barrier height have been fabricated within the limited scope of our Micro-electronics Laboratory. Though the fabrication process that has been adopted as presented in this thesis may not be suitable for fabrication of discrete microwave Schottky diode, but the results of this thesis would be extremely useful in fabrication of Schottky barrier solar cells which is at present a promising device for solar energy conversion. Author has, however, also investigated the ohmic contacts those could be used in further researches in this laboratory. The fabrication process of some of the authors(60) may seen to be sophisticated but they are suitable for fabrication of microwave diodes where geometry and area of metal contact are precisely controlled. The work on Schottky diodes of this thesis emphasised on the control of a physical parameter, the barrier height.

Aluminium was found to be most suitable metal because of its barrier with n-type silicon was controllable over a range of 0.67 to 0.8V and the barrier with p-type silicon was also controllable but over the range 0.5V to 0.65V. The control action was obtained by heat-treatment after the fabrication procedure. Control of barrier above 0.8V was obtained by barrier formed by metals aluminium and gold deposited in succession. Gold and silver barrier did not show any reproducible variation with heat-treatment rather they were stable after initial heat-treatment when a slight

change took place. In all the cases the freshly prepared barrier with p-type silicon showed higher value of barrier height and with n-type showed the lower value of barrier height compared to their known values. This confirmed the presence of fixed positive charges whose density was found to be of the order of $10^{12}/cm^2$.

Ideality parameters of the diodes were around two. Such high value of n was because of presence of oxide layer that grows on silicon when left in atmospheric condition of our country for long time. Metal-oxide- Schottky barrier theory has been applied to find out the thickness of this inter-facial oxide layer δ. The obtained value of δ varied over a range of about 3-30 μ, thus indicating the nonuniform growth of oxide layer. Interface-state density calculated from the diodes were of the order of 10^{12}- 10^{13}, ev^{-1}, cm^{-2}. They were assumed to be independent of thickness of inter-facial oxide layer and in communication with the silicon only. The density of the states were found to increase slightly with reverse bias upto a few volts. This was because of presence of the traps in most of the samples. The trap concentrations have been calculated. They increased the reverse current in addition to the effect of image force barrier lowering.

From the results of this thesis it is suggested that if an improved value of ideality parameter is desired then one would need substrates without having an epitaxial layer but polished mechanically just before the chemical cleaning. A near-ideal value

of ideality parameter could be achieved if freshly prepared epitaxial layer of silicon is provided. Reduction of the diodes series resistance is important. This may be attained by ohmic contacts obtained by alloying in an hydrogen atmosphere.

Diodes with improved reverse characteristics would be obtained if the edge leakage current component is eliminated by applying a metal guard ring around the metal contact. The edge effect is significant for diodes of larger sizes and should always be taken in consideration.

In order to make these diodes to be useful in microwave frequencies as discrete devices it would be, necessary to reduce the area of the diodes significantly, about 50-100 μ diameter of metal contact. Also fine wire bounding facility has to be provided in the Laboratory. For superior quality of Schottky diodes it is suggested that GaAs should be used because it does not oxidise so easily as silicon andthis is very important specially in the climatic condition of Bangladesh.

6.2 THE SCOPE OF FUTURE WORKS:

At present a great deal of works are in progress (61,(62) on the fabrication of efficient Schottky solar cell because of its comparable conversion efficiency with that of the p-n junction photo-diode, and the simplicity of its fabrication. Schottky solar cell is a Schottky barrier diode where additional features are incorporated so that it can absorb sufficient solar radiationand the photo-

excited electrons can surmount the barrier. By proper choice of metal and antireflection coating it may be possible to fabricate such cell with higher conversion efficiency. Such a program of research can be readily taken from the information obtained in this thesis. The increased barrier height is an asset for a solar cell because both the open circuit voltage and power conversion efficiency are positively affected by the increase in the barrier height. Also the ideality parameter of a value of around two would also be advantageous for Schottky solar cell.

Pulfrey and Mcouat[63] have shown that the maximum value of power conversion efficiency can be attained by fabricating a barrier on a p-type silicon having the barrier height as high as 1V. Such a high value of barrier height can be achieved by the process described in this thesis but with the addition of a step of oxidation. Thus a thicker interfacial layer at the interface would result in a high barrier height as expected from the model of Card and Rhoderick[39].

In addition to the simplicity of fabrication of Schottky Solar diode, the cost reduction would be still more important for its terrestrial application. So another step involves similar study that would be done with thin polycrystalline silicon film. Within the existing facily of the laboratory in Electrical Engineering Department, BUET, it is well possible to study the Schottky solar cell's adaptability to polycrystalline thin silicon films. It is therefore suggested that further research may be undertaken in the field of Solar Cells using Silicon Schottky diode as the basic device.

APPENDICES

Appendix-A

INTERFACE STATE DENSITY FROM C-V AND I-V CHARACTERISTICS (48)

The interface state model as followed by Borrego includes the image force barrier lowering whose effect is to increase the barrier height in forward bias and decrease ϕ_B in reverse bias. Assuming that interfacial oxide layer is very thin that it is not considered explicitly and hence the electrons in the interface states are in equilibrium with the metal, the relationship between the magnitude of the surface states charge density Q_{ss} and density of interface states is given by

$$N_{ss} = - \frac{1}{q} \frac{d\,Q_{ss}}{d\,\phi_B} \qquad (A-1)$$

Since neither Q_{ss} nor ϕ_B is a quantity which can be controlled directly in a Schotky diode, it is necessary to evaluate the functional dependence of Q_{ss} and of ϕ_B upon an appropriate directly controlable variable. The applied terminal voltage is such a variable since the voltage dependence of Q_{ss} can be determined from C-V characteristics and the voltage dependence of ϕ_B can be determined from either from I-V characteristics or photo-electric measurement. Here two methods of evaluating the equation (A-1) will be presented using, the measured I-V and C-V characteristics of Schotky diodes.

To determine the charge density Q_{ss} as a function of the applied voltage V the electric field at the interface is obtained from high frequency C-V data taking into account the presence of deep donor level. The charge density Q_{ss} is related to the electric field E_s at the interface by the equation

$$Q_{ss} = \epsilon_s E_s \qquad (A-2)$$

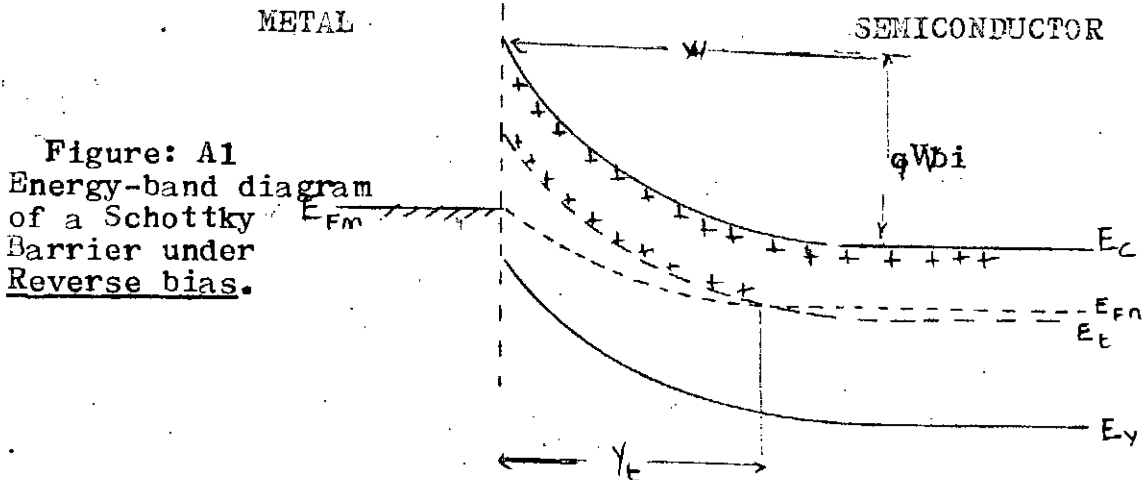


Figure: A1
Energy-band diagram of a Schottky Barrier under Reverse bias.

From energy band diagram of fig.A-1 an increase in the voltage across the depletion layer ΔV_{bi} uncovers a charge $q\, N_t\, y_t$ and a charge $qN_D \Delta W$,

$$\text{So that } \Delta E_s = \frac{q\, N_t}{s} \Delta Y_t + \frac{q\, N_D}{\epsilon_s} \Delta W \qquad \text{(A-3)}$$

Where N_t is the deep donor density and N_D is shallow donor density, the increase in voltage ΔV_{bi} is

$$\Delta V_{bi} = \frac{q N_t\, y_t}{\epsilon_s} \Delta Y_t + \frac{q\, N_D\, W}{\epsilon_s} \Delta W \qquad \text{(A-4)}$$

Where Y_t is given by

$$W - y_t = \left[\frac{2\, \epsilon_s\, V_t}{q\, N_D} \right]^{1/2} \qquad \text{(A.5)}$$

and $q\, V_t$ represents the energy difference between the deep donor level and the Fermi level in the bulk. Assuming that the deep donor level does not respond at high frequency depletion layer capacitance C is given by

$$C = \frac{S\epsilon_s}{W} \qquad \text{(A-6)}$$

Where S is the area of the diode ross-section. It follows from equation (A.2) to (A.6) that

$$\Delta Q_{ss} = \frac{C}{S} \frac{\partial V_{bi}}{\partial V} \Delta V - q\, N_t \left(\frac{2\epsilon_s\, V_t}{q\, N_D} \right)^{1/2} \frac{\partial C}{\partial V} \Delta V \qquad \text{(A.7)}$$

Although the change is in ϕ_B with bias is small we may write

$$\frac{\partial V_{bi}}{\partial V} = -1 + \frac{1}{q} \frac{\phi_B}{V} \qquad (A.8)$$

So equation A.7 by means of equation- A.8 can be written as follows:

$$\Delta Q_{ss} = \epsilon_s \Delta E_s = -\frac{c}{S} \Delta V + \frac{1}{q} \frac{c}{S} \Delta \phi_B - q N_t \left(\frac{2\epsilon_s V_t}{q N_D} \right)^{1/2} \frac{\partial \ln C}{\partial V} \Delta V \qquad (A.9)$$

Integrating above equation between 0 and V, the change in stored charge is obtained.

$$Q_{ss}(V) - Q_{ss}(0) = -\frac{1}{S} \int_0^V C \, dV + \frac{1}{qS} \int_{\phi_B(0)}^{\phi_B(V)} C \, d\phi_B + q N_t \left(\frac{2\epsilon_s V_t}{q N_D} \right)^{1/2} \ln \frac{C(0)}{C(V)} \qquad (A.10)$$

Since the change is barrier height with voltage is usually small (less than 0.05 ev for a change of voltage of several volts), the second term can be appoximated by the average value of capacitance times the change in barrier height, Using this approximation equation(A.10) can be written as :

$$Q_{ss}(V) - Q_{ss}(0) = \epsilon_s \left[E_s(v) - E_s(0) \right]$$

$$= -\frac{1}{S} \int_0^V C \, dV + \frac{1}{qS} \frac{\left[c(v) + c(0) \right] \left[\phi_B(V) - \phi_B(0) \right]}{2}$$

$$+ q N_t \left(\frac{2 V_t}{q N_D} \right)^{1/2} \ln \frac{C(0)}{C(V)} \qquad (A.11)$$

The last term of above equation (A.11) represents the contribution to the surface charge density by the charge of the deep donors which is uncovered within the depletion region. In addition,

We have $Q_{ss}(0) = \frac{q\,(N_D + N_t)\,\epsilon_s\,S}{C(o)} - q\,N_t\left(\frac{2\epsilon_s\,V}{q\,N_D}\right)^{1/2}$ (A.12)

assuming that the deep level is uncovered at zero bias. If the charge is the deep donor level is negligible at zero bias, $Q_{ss}(o)$ can be expressed as:

$$Q_{ss}(o) = \frac{2\,C(o)\,V_{bi}(o)}{S} \qquad (A.13)$$

Where $V_{bi}(o)$ is the diffusion or contact potential.

The dependence of the barrier height ϕ_B upon the applied voltage is determined from I-V characteristics. Assuming that the current in Schottky barrier is due to thermionic emission, the relationship between I/S and applied voltage V taking into account image force barrier lowering, is given by

$$J = \frac{I}{S} = A^{**}\,T^2 \exp\frac{\phi_B - q\,\beta\,(E_s)^{1/2}}{KT}\left[\exp\left(\frac{qV}{KT}\right) - 1\right] \qquad (A.14)$$

where β is the image force lowering constant is given by:

$$\beta = \left(\frac{q}{4\pi\epsilon_s}\right)^{1/2} \qquad (A.15)$$

The leakage current I_s is obtained by extrapolating the curve of $\ln$ I Vs. V at forward bias ($V > 4\,KT/q$) to $V = 0$:

$$J_s = \frac{I_s}{S} = A^{**}\,T^2 \exp\left[\frac{-\phi_B(o) - q\,\beta\sqrt{E_s(o)}}{KT}\right] \qquad (A.16)$$

The change in barrier height at any voltage V can be obtained from equation (A.14) and (A.16) and is given by:

$$\Delta\phi_B = q\,\beta\,\Delta(\sqrt{E_s}) - KT\,\ln\frac{1}{I_s\left[\exp.\left(\frac{qv}{KT}\right) - 1\right]} \qquad (A.17)$$

Where $\Delta\phi_B = \phi_B(V) - \phi_B(o)$ and $\Delta\sqrt{E_s} = \sqrt{E_s(V)} - \sqrt{E_s(O)}$ ..... (A.18)

Using equation (A.11) and (A.17), the dependence of Q_{ss} upon ϕ_B is determined from I-V and C-V characteristics. Once Q_{ss} is known as a function of ϕ_B, N_{ss} is determined from equation (A.1).

It should be noted that N_{ss} can also be evaluated without determining, I_s. Since Q_{ss} and ϕ_B are functions of applied voltage V_1 it follows that

$$\frac{d\, Q_{ss}}{d\, \phi_B} = (\partial Q_{ss} / \partial V) \;/\; (\partial Q_B / \partial_v)$$

The numerator equation A.19 is obtained from equation A.9 and it is given by

$$\frac{\partial Q_{ss}}{\partial V} = -\frac{C}{S} + \frac{1}{q}\;\frac{C}{S}\;\frac{\partial \phi_B}{\partial V} - q\, N_t \left(\frac{2\, s\, V_t}{q\, N_D}\right)^{1/2} \frac{\partial \ln C}{\partial V} \tag{A.20}$$

The change in barrier height with voltage, the denomination of equation A.19 can be obtained by taking the derivative of equation A.17 with respect to voltage. Introducing the ideality factor n, defined as

$$\frac{1}{n} = (kT/_q)\;\frac{\partial \ln I_{F,R}}{\partial V_{F,R}} \tag{A.21}$$

Where I_F, I_R and V_F, V_R are the currents and voltages in forward and reverse bias respectively, we obtain

$$\frac{1}{q}\;\frac{\partial \phi_B}{\partial V_F} = \frac{-1}{n} + \beta\frac{\partial \sqrt{E_s}}{\partial V_F} + \frac{1}{1-\exp(-qV_F/kT)} \tag{A.22}$$

$$\frac{1}{q}\;\frac{\partial \phi B}{\partial V_R} = \frac{-1}{n} + \beta\,\frac{\partial \sqrt{E_s}}{\partial V_R} + \frac{1}{\exp.\left(\frac{qV_R}{KT}\right) - 1} \tag{A.23}$$

Substituting equation (A-2), (A.22) and (A.23) into (A.19) gives $d Q_{ss} / d\phi_B$.

Thus N_{ss} reduces to simple expression in terms of capacitance C and ideality parameter for biases of $V > 4 kT/q$, we have now

$$N_{ss} = \frac{\frac{C}{q_S}\left(1 - n\beta \frac{\partial \sqrt{E_s}}{\partial V_F}\right) + n N_t \sqrt{\frac{2 \epsilon_s V_t}{q N_D}} \frac{\partial \ln C}{\partial V_F}}{\left(n - 1 + n\beta \frac{\partial \sqrt{E_s}}{\partial V_F}\right)} \tag{A.24}$$

for forward bias and :

$$N_{ss} = \frac{\frac{C}{qs}\left(n - 1 + n\beta \frac{\partial \sqrt{E_s}}{\partial V_R}\right) - N_t n \sqrt{\frac{2 \epsilon_s V_t}{q N_D}} \frac{\partial \ln C}{\partial V_R}}{1 - n \frac{\partial \sqrt{E_s}}{\partial V_R} \beta} \tag{A.25}$$

for reverse bias

If the effect of image force barrier lowering and the effect of deep donors are neglected, equation(A.24), and (A.25) reduces to simple form as follows:

$$N_{ss} = \frac{C}{q\, S\, (n-1)} \quad \text{for forward bias}$$

$$= \frac{C\,(n-1)}{q\, S} \quad \text{for reverse bias}$$

(A.26).

APPENDIX -B

EFFECTIVE RICHARDSON'S CONSTANT A^{**} (31)

The complete expression of current voltage (J-V) characteristics taking into account the effect of back-Scattering by electron optical phonons at the potential energy maxima and the effect of quantum mechanical reflection of electrons by the Schottky barrier and also the effect of tunneling of electrons through the barrier as derived by Crowell and Sze (31) is given by

$$J = J_s \exp\left[\left(\frac{qV}{KT}\right) - 1\right] \qquad (B.1)$$

$$J_s = A^{**} T^2 \exp\left(\frac{-q\,\phi_{Bn}}{KT}\right) \qquad (B.2)$$

$$\text{Where } A^{**} = \frac{f_p f_q A^*}{(1 + f_p f_q V_R/U_D)} \qquad (B.3)$$

f_p is the probability of electron emission over the potential maximum considering optical phonon scattering and is given by

$$f_p \simeq \exp\left(-x_m/\lambda\right) \qquad (B.4)$$

and it is observed that for small fields (corresponding to large x_m) and high temperatures (corresponding to small mean free path λ) there is a considerable reduction of the emission probabliy as explained from equation- (B.4). A value of f_p less than unity implies that V_R should be replaced by a smaller recombination velocity $f_p V_R$. A value of f_p less than 0.7 is indicative of failure of the thermionic emission theory:

The quantity f_q takes the effect of the fact that energy distribution of carriers is further distorted from a Maxwellian distribution because of quantum mechanical reflection by the ba-

barrier and also due to the tunneling through the barrier when f_Q is defined as a theoretical ratio of total current flow considering these two effects to current flow neglecting these effects. f_Q is a function of electric field which rises rapidly near 10^5 V/cm at room temperature which marks the transition between thermionic (T) and thermionic-field (T-F) emission.

Thus the probabilities f_p and f_q set a limit of high field and a low field limit to apply the thermionic emission theory. The limit being $2x10^2$ to 4×10^5 V/Cm for Silicon. The calculated value of A** for metal- Si system at room temperature is given in figure B-1. It is noted that in between the field range 10^4 to $2x10^2$ V/cm , A** remains essentially constant.

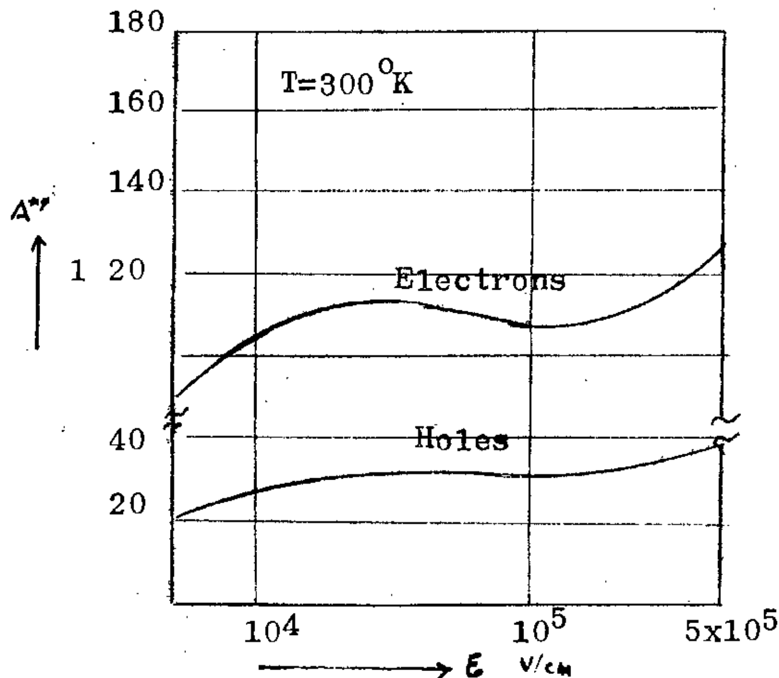


Figure: B1

Calculated Value of A** Vs. Electric Field in a Metal-Silicon Schottky Diodes.

APPENDIX-C

THE EFFECT OF METAL-OXIDE-SEMICONDUCTOR POTENTIAL DISTRIBUTION ON THE VALUE OF IDEALITY PARAMETER (39)

At the metal semiconductor interface a potential difference can be sustained. This potential was assumed to be bias dependent and gives rise to reduced dependence of the semiconductor surface potential on the applied bias. Thus the diffusion potential in the semiconductor is altered by the presence of the insulator. This is expected even for a charge free film, but the effect would be more pronounced as a result of fixed charge (or very slow states) in oxides on silicon. The energy band diagram of the chemically prepared Schottky barrier (MOS contact) is shown in figure -C.1.

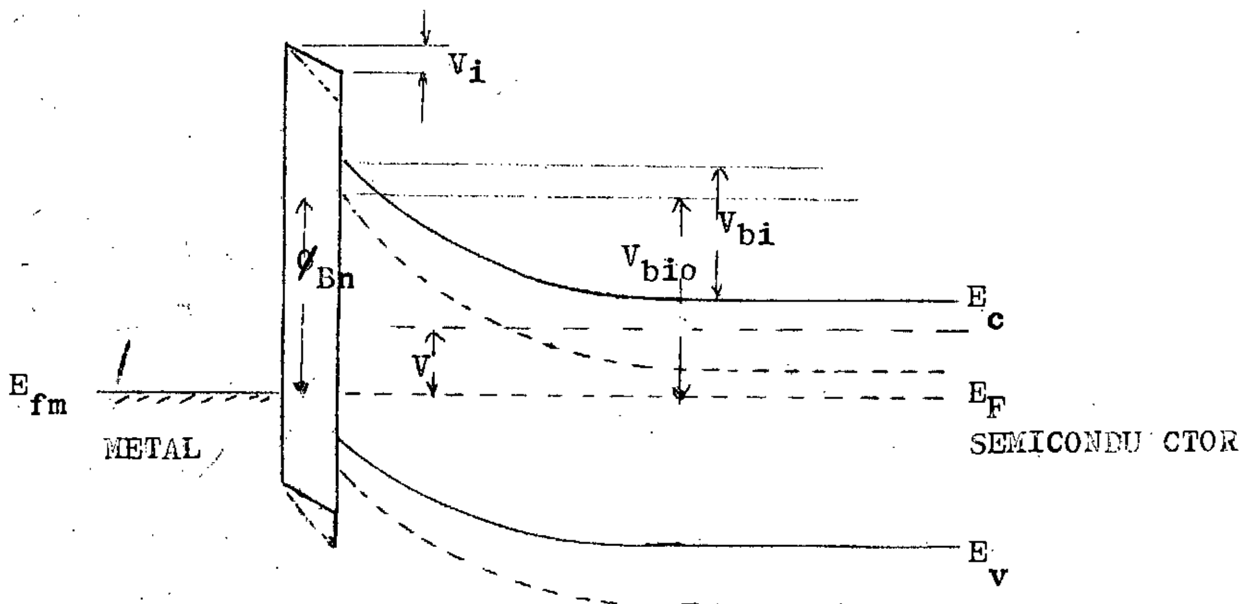


Figure-C-1 Energy band diagram of Schottky MOS contact under zero bias (------) and under forward bias (———)

It is assumed that the contribution to the value of n from other mechanism (such as a recombination currents) are very small.

The static potential distribution through the contact is affected by the presence of the oxide film. Gauss's theorem states that the field in the insulator and that just inside the semiconductor are in the proportion ϵ_s/ϵ_i unless there is a surface charge density at the interface. However the charge density can arise through a net charge in interface states or through mobile carriers accumulated at the semiconductor surface. The charging of interface states takes place by (a) electrones tunneling between the states and the metal and by (b) interaction with the electrones in the conduction and valance bands of the semi conductors. The population of these states is chiefly determined by the process which takes place most readily.

The surface potential is better known as diffusion potential, V_{bi} whose zero field value is represented as V_{bio}. The change in surface potential may be related to the applied potential by

$$n = - V/\Delta V_{bi} \qquad (C.1)$$

where V_{bi} is the change in surface potential as a result of the applied bias V. ΔV_{bi} and change in oxide potential ΔV_i are negative for forward bias. Using $\Delta V = -(\Delta V_{bi} + \Delta V_i)$ enables equation (C.1) to be written in differential form

$$\frac{1}{n(v)} = -\frac{dV_{bi}}{dV} = 1 + \frac{dV_i}{dV} \qquad (C_o 2)$$

Applying Gauss's Law to the surface charge on the metals we get

$$\Delta v_i = - \delta \left(\frac{Q}{\epsilon_i} \right) \qquad (C_o 3)$$

Also $$Q_M + Q_{ss} + Q_{sc} = 0 \qquad (C_o 4)$$

Thus equation- (A3.3) becomes

$$V_i = \frac{\delta}{\epsilon_i} \left(\Delta Q_{sc} + \Delta Q_{ss} \right) \qquad (C_o 5)$$

Taking derivatives

$$\frac{dV_i}{dV} = \frac{\delta}{\epsilon_i} \frac{d}{dV} \left(Q_{sc} + Q_{ss} \right) = \frac{\delta}{\epsilon_i} \left(\frac{dQ_{sc}}{dV_{bi}} \frac{dV_{bi}}{dV} + \frac{dQ_{ss}}{dV} \right) \qquad (C_o 6)$$

From the depletion approximation

$$\frac{d\, Q_{sc}}{d\, V_{bi}} = \frac{\epsilon_s}{W} \qquad (C_o 7)$$

It is assumed that the interface states can be subdivided into two groups. The states in one of these groups are in equilibrium with metal and those in the other group are in equilibrium with the semiconductor.

For interface states that equilibrates with the metal, the change in occupancy is determined by change in energy of the states relative to the Fermi energy in the metal ; that is by dVi,so

that $\frac{\partial Q_{ss}}{\partial V_i} = q\,N_{sa}$. For interface states that equilibrates with the semi-conductor, the change in occupancy is determined by the change in energy of the states relative to the Fermi-level in the semiconductor; that by dV_{bi}, so that $\partial Q_{ss}/\partial V = q\,N_{sb}$.

In general
$$\frac{dQ_{ss}}{dV} = \frac{\partial Q_{ss}}{\partial V_i}\frac{dV_i}{dV} + \frac{\partial Q_{ss}}{\partial V_{bi}}\frac{dV_{bi}}{dV} = q\,N_{sa}\left(\frac{n-1}{n}\right) - q\,\frac{N_{sb}}{n} \qquad (C.8)$$

Substituting (C.8) into expression (C.6) and rearranging gives

$$n = 1 + \frac{(\delta/\epsilon_i)\,(\epsilon_s/W + q\,N_{sb})}{1 + (\delta/\epsilon_i)\,q\,N_{sa}} \qquad (C.9)$$

If the density of interface states are sufficiently small so as not to influence the potential distribution (A2.9) becomes

$$n = 1 + \frac{\delta\,\epsilon_s}{W\,\epsilon_i} \qquad (C.10)$$

For the case where all the interface states equilibrates with semiconductor, that is $N_{sa} \rightarrow 0$, (C.9) reduces to

$$n = 1 + \frac{\delta}{\epsilon_i}\left(\frac{\epsilon_s}{W} + q\,N_{bs}\right) \qquad (C.11)$$

This is the result for thick oxides, since the communication of the interface states with the metal (by tunnelling) decreases with δ.

APPENDIX- D

MINORITY CARRIER INJECTION RATIO[30]

The Schottky barrier diode is majority carrier device under low-injection condition. At sufficiently large forward bias, the minority carrier injection ratio increases with current due to the enhancement of the drift-field component, which becomes much larger than the diffusion current.

At steady-state, the one dimensional continuity and current density equation for minority carrier are given by

$$0 = \frac{P_n - P_{no}}{\tau_p} - \frac{1}{q}\frac{\partial J_p}{\partial x} \qquad (D.1)$$

$$J_p = q \mu_p p_n \mathcal{E} - q D_p \frac{\partial p_n}{\partial x} \qquad (D-2)$$

Considering the energy band diagram as shown in figure D-1 where x_1 is the boundary of depletion layer and x_2 occurs at the interface between the n-type epitoxial layer and n + substrate. From the rectifying theory, the minority carrier density at X is given by

$$P_n(x_1) = P_{no} \exp\left[\left(\frac{qV}{KT}\right) - 1\right] = \frac{n_i^2}{N_D}\left[\exp\left(\frac{qV}{KT}\right) - \right] \qquad (D.3)$$

and

$$P_n(x_1) = \frac{n_i^2}{J_s} \frac{J}{N_D} \qquad (D.4)$$

The boundary condition on $P_n(x)$ and $X = x_2$ can be stated in terms of transport velocity, $V_T = D_p / L_p$, for the minority carriers

$$J_p(x_2) = qv_T P_n = q\left(\frac{D_p}{L_p}\right) p_{no}\left[\exp\left(\frac{qv}{KT}\right) - 1\right] \quad \text{for } L \ll L_p \qquad (D.5)$$

For low injection conditions, the minority carrier drift component is negligible in comparison with diffusion term and the injection ratio γ is given by

$$\gamma = \frac{J_p}{J_p + J_n} \simeq \frac{J_p}{J_n} = \frac{q n_i^2 D_p}{N_D L_p A^{**} \exp\left(-\frac{q\phi B_n}{KT}\right)} \qquad (D.6)$$

For gold- n-type silicon this ratio is generally less than 0.1% at room temperature.

For sufficiently large forward bias, however the electric field causes a significant carrier drift current component which eventually determines the minority carrier current. From equation (3.7) (D..2) and (D.4) we obtain for high-current limiting condition.

$$\gamma = \frac{J_p}{J_n} \approx \frac{n_i^2}{N_D^2} \left(\mu_p / \mu_n\right) \frac{J}{J_s} \qquad (D.7)$$

For example, a gold n-type silicon diode with $N_D = 10^{15}$ cm^{-3} and $J_s = 5 \times 10^{-7}$ Amp/cm^2 would be expected to have an injection ratio of about 5%. at a current density of 350 amp/cm^2. The

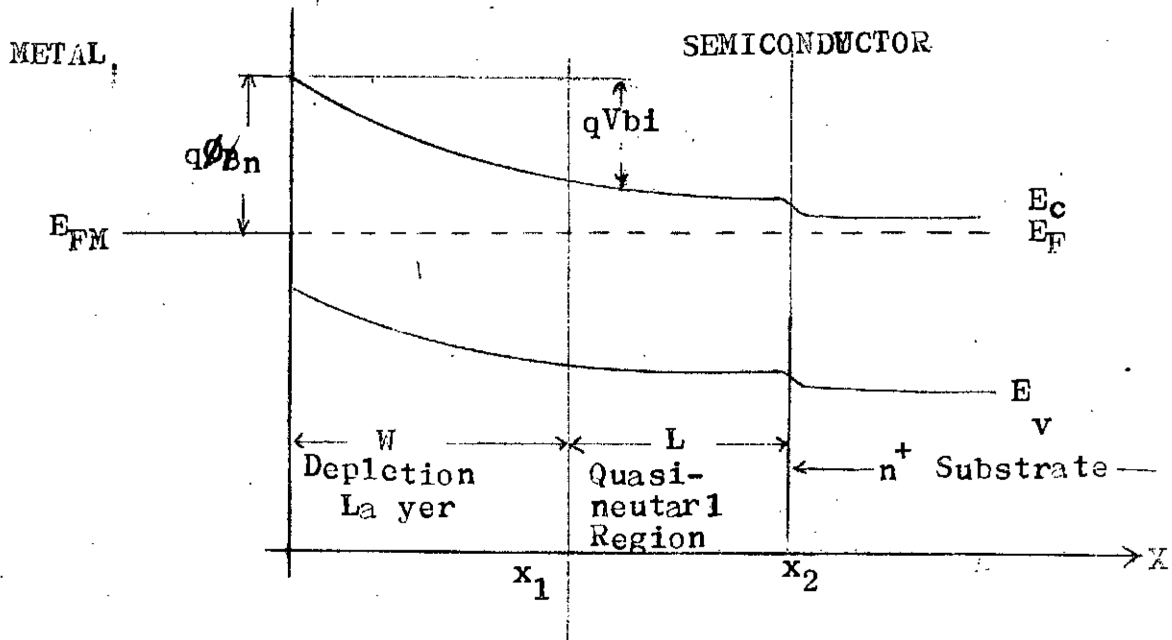


Figure D- 1 Energy band diagram of an eptaxial Schottky barrier.

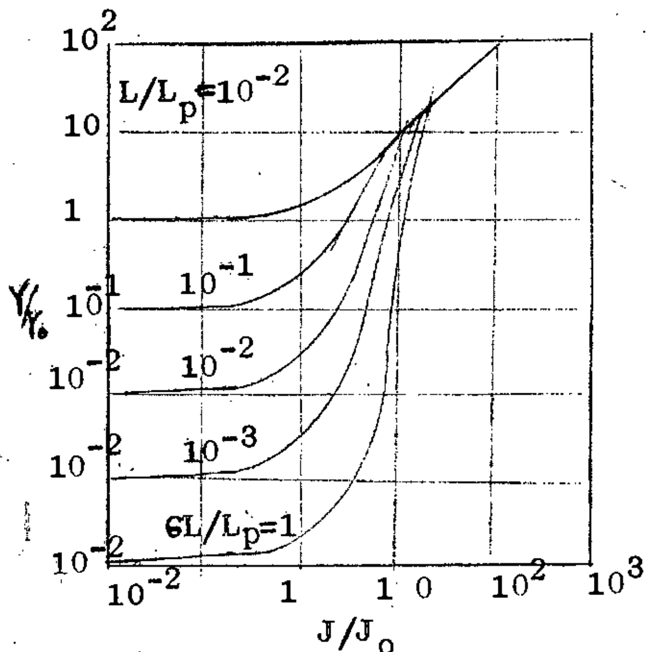


Figure D- 2 Normalised minority carrier injection ratio versus normalised current density.

The intermediate cases have been considered by Schar-fetter and computed results shown in Fig. D.2 where normalization factors are given by

$$J_o = \frac{q\ D_n\ N_D}{L} \qquad (D.8)$$

$$\gamma_0 = \frac{q\ D_p\ n_i^2}{N_D\ L\ J_s} \qquad (D.9)$$

It is clear from Fig.(D.2) that in order to reduce the minority carrier injection ratio one must use a metal-semiconductor system with large N_D, large J_s (corresponding to small barrier height) and small n_i (corresponding to large band gap).

The minority carrier stored charge per unit area (Q) for Schottky diode made upon epitaxial layer depend upon the characteristics of the epi-substrate interface and can become significant when the interface is highly reflecting. For large applied bias and negligible bulk recombination the stored charge per unit area is given by $Q = \frac{q n_i^2\ D_p\ J}{N_D\ J_s\ \sigma}$ where σ is surface recombination velocity. In measurement the interface is not found to be reflecting but is characterized by a recombination velocity of about 2000 cm/sec. This value applied to 5 ohms.cm. silicon-gold diode yield storage of about 1/3 nano sec.

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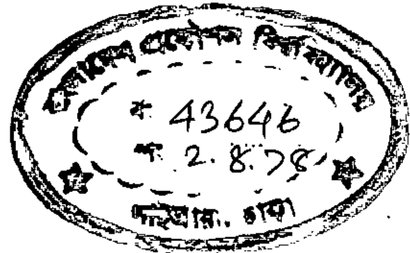
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