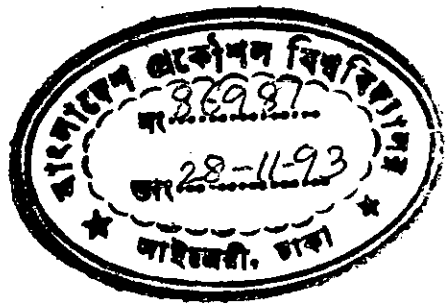
ANALYTICAL MODELLING OF BREAKDOWN IN SHORT CHANNEL MOSFET's



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The thesis ANALYTICAL MODELLING OF BREAKDOWN IN SHORT CHANNEL MOSFET's submitted by Md. Tanvir Quddus, Roll No. 901327P, Session '88-89 to the Electrical and Electronic Engineering Department of B.U.E.T. has been accepted as satisfactory for partial fulfilment of the requirements for the degree of Master of Science in Engineering (Electrical and Electronic).

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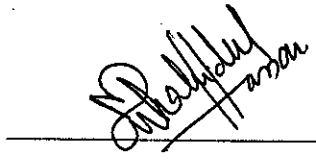

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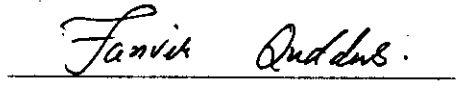

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ABSTRACT

MOSFETs are used extensively in VLSI Technology specially in various digital circuits such as microprocessors, semiconductor memories etc. Since the birth of the IC fabrication the need for the reduction of device dimensions is driven by the requirement that IC of high complexity can be fabricated. The purpose of microminiaturization of the MOSFET is not only to increase the packing density but also to improve the circuit performance. The fundamental issue of downsizing the MOS transistor is to preserve the long channel characteristics after miniaturization. But as the dimension of the MOSFET is reduced, departure from the long channel behaviour occur due to various undesirable short channel effects./Among the various short channel problems, avalanche induced breakdown due to hot carriers produced by impact ionization is a major one. The drain characteristics of the short channel MOSFET exhibits a rapid rise in the current due to this destructive phenomena which leads to the destruction of the device./So the study of short channel MOSFET along with the physics in the avalanche induced breakdown regime is very important from the design point of view. A number of breakdown models have been developed for short channel MOSFET in the last few years. In this thesis a simple analytical breakdown model incorporating the physics of the breakdown has been presented. This model not only establishes the relation between different voltage and current of the MOSFET but also demonstrates the ability to represent various short channel effects. The model also shows that the primary phase of breakdown is initiated by excess channel current whereas the secondary phase is due to emitter current and both these currents again strongly depend on the flow of substrate current.

CONTENTS

LIST OF FIGURES

LIST OF SYMBOLS

1.	V_T	V	Threshold voltage.
2.	ϕ_f	V	Fermi potential.
3.	ϕ_{si}	V	Surface potential at strong inversion.
4.	ψ_s	V	Surface potential.
5.	w	m	Depletion width.
6.	W_S	m	Source depletion width.
7.	W_D	m	Drain depletion width.
8.	ε_x	Vm^{-1}	Normal electric field.
9.	ε_y	Vm^{-1}	Lateral electric field.
10.	Q_I	Cm^{-2}	Inversion layer charge.
11.	Q_B	Cm^{-2}	Bulk charge.
12.	Q_S	Cm^{-2}	Surface charge.
13.	I_m	A	Multiplication current.
14.	l	m	Effective channel length.
15.	Z	m	Channel width.
16.	μ_p	$m^2V^{-1}s^{-1}$	Hole mobility.
17.	μ_n	$m^2V^{-1}s^{-1}$	Electron mobility.
18.	ϵ_s	Fm^{-1}	Permittivity of silicon.
19.	α_1		Empirical constant.
20.	α_2		Empirical constant.
21.	α_3		Empirical constant.
22.	v_d	ms^{-1}	Drift velocity.
23.	d_j	m	Junction depth.
24.	d	m	EPR thickness.
25.	N	m^{-3}	Substrate doping.
26.	N_{SD}	m^{-3}	Source and drain Doping.

27.	$\hat{V}_T$	V	Short channel threshold.
28.	τ_n	s	Electron lifetime.
29.	L_n	m	Electron diffusion length.
30.	L_p	m	Hole diffusion length.
31.	V_{DS}	V	Drain source voltage.
32.	V_{GS}	V	Gate source voltage.
33.	V_{GB}	V	Gate bulk voltage.
34.	V_{SB}	V	Source bulkvoltage.
35.	U_T	V	Thermal voltage.

LIST OF ABBREVIATIONS

1.	QNR	Quasi neutral region.
2.	EBE	Enhanced body effect.
3.	EPR	Equipotential region.
4.	VDT	Voltage doping transformation.

CHAPTER 1

INTRODUCTION

1.1 Short channel MOSFETs

A MOSFET is a four terminal device in which the lateral current flow is controlled by an externally applied vertical electric field. A typical n-channel enhancement MOSFET consists of a relatively lightly doped p type substrate into which two heavily doped n^+ regions are diffused which act as source and drain respectively. The region of inversion layer of mobile electrons between source and drain is the channel and a thin layer of insulating material separates the channel from the metal gate electrode. The metal area of the gate in conjunction with the insulating dielectric oxide layer and the semiconductor channel form a parallel plate capacitor. The voltage applied to the gate controls the carriers in the conduction channel and thus controls the conductivity of the device.

The threshold voltage V_T of a MOSFET is defined as the minimum voltage required to induce the conduction channel. When a gate voltage equal to V_T is applied to a MOSFET it produces a downward bending of the energy band-diagram at semiconductor-oxide interface and causes the midgap energy E_i to cross over

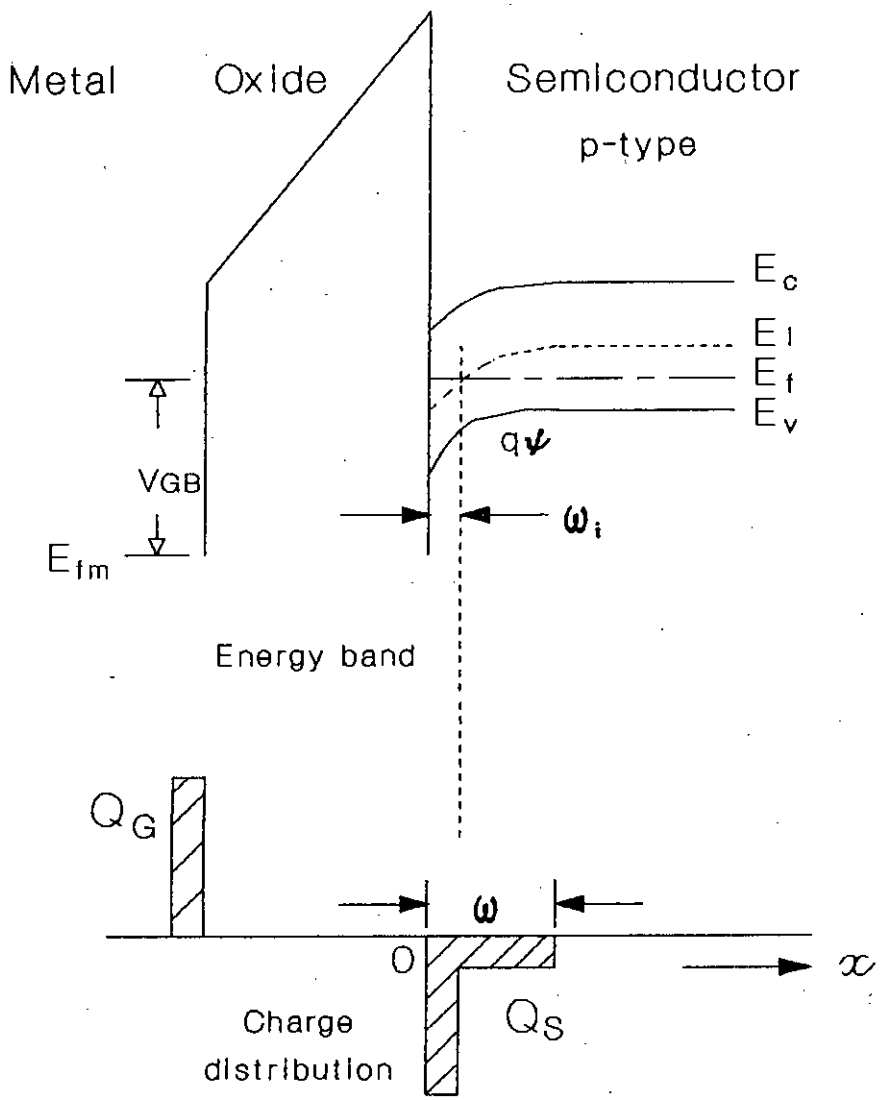


Fig. 1.1. Energy band and charge distribution diagram of a MOSFET.

the constant fermi level by an amount ϕ_f at or near the silicon surface (Fig. 1.1) (Fig. 1.2). When this happens an inversion layer of width w_i is formed at the silicon surface in which the electron density is equal to the hole density in the bulk because the electron and the hole density in the substrate is given by

$$n = n_i e^{\frac{E_F - E_I}{KT}} \tag{1.1}$$

and

$$p = n_i e^{\frac{E_I - E_F}{KT}} \tag{1.2}$$

where, n_i is the intrinsic carrier concentration, E_F is the fermi energy level and E_I is the intrinsic energy level . The values of E_F and E_I are given by

$$E_F = -q\phi_f \tag{1.3}$$

and

$$E_I = -q\psi \tag{1.4}$$

where , ϕ_f and ψ are the potential of the fermi and the intrinsic level respectively. This condition is defined as the onset of the strong inversion and the surface potential ψ_s under this condition is given by

$$\psi_s = 2\phi_f = \phi_{si} \tag{1.5}$$

The left side of X_I (Fig. 1.2) remains n type whereas the the right side remains

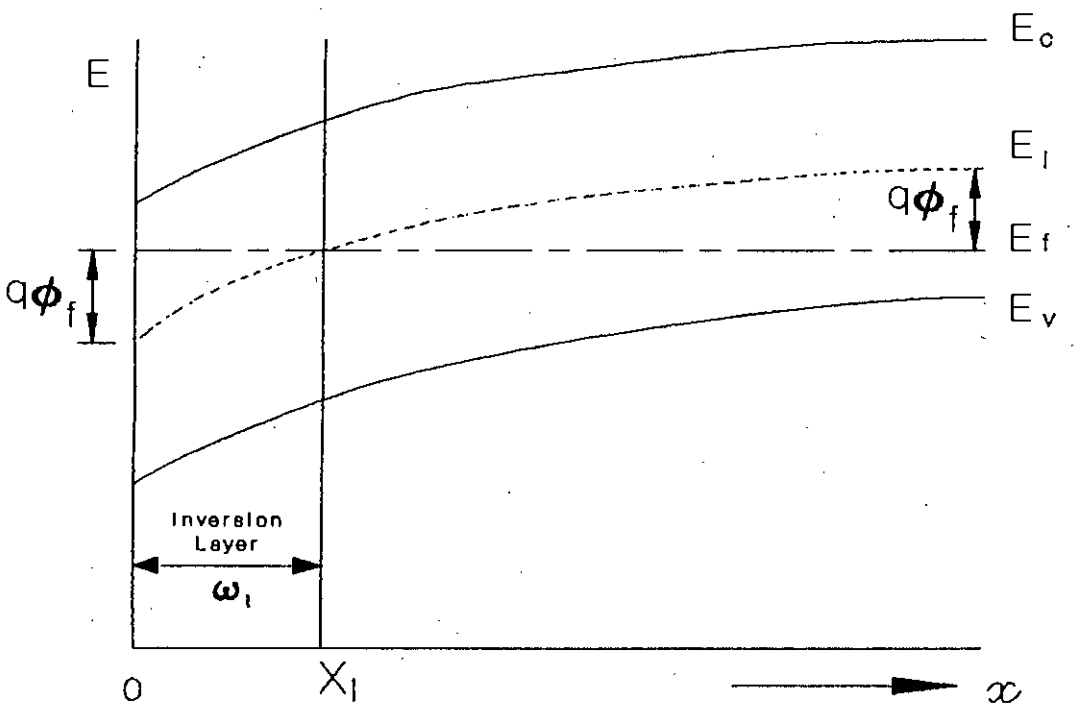


Fig. 1.2. Energy band diagram of a MOSFET at the onset of strong inversion.

p type. So, at the left side of X_I a region of inversion layer of width w_i and at the right side of X_I a surface depletion region of width w is produced which extends upto bulk. The depletion layer width w and bulk charge Q_B is given by

$$w = \sqrt{\frac{2\epsilon_s \psi_s}{qN_A}} \tag{1.6}$$

and

$$Q_B = -qN_A w \tag{1.7}$$

where, N_A is the doping density of the substrate.

The charge balance equation in the surface region of a MOSFET can be written as

$$\begin{aligned} Q_S &= Q_I + Q_B \\ &= Q_G \end{aligned} \tag{1.8}$$

where, Q_S, Q_I, Q_G are total charge, inversion layer charge and gate charge respectively.

The applied gate voltage V_G in a MOSFET is shared by the flat band voltage V_{FB}, surface potential ψ_s and voltage across the oxide V_o and is given by

$$\begin{aligned} V_{GB} &= V_{FB} + \psi_s - \frac{Q_S}{C_o} \\ &= V_{FB} + \psi_s + \gamma\sqrt{\psi_s} \end{aligned} \tag{1.9}$$

where,

$$\gamma = \frac{\sqrt{2q\epsilon_s N_A}}{C_o} \tag{1.10}$$

In this equation C_o is the oxide capacitance per unit area and is given by

$$C_o = \frac{\epsilon_{ox}}{t_{ox}} \tag{1.11}$$

where, t_{ox} is the oxide thickness.

From the expression of the gate voltage the threshold voltage can be represented as

$$V_T \equiv V_{FB} + \psi_s - \frac{Q_B}{C_o} \tag{1.12}$$

where, $\psi_s = 2\phi_f$

At the onset of strong inversion $Q_I \ll Q_B$, therefore, equation (1.8) reduces to $Q_S = Q_I + Q_B \approx Q_B$. Now the inversion layer charge at a gate voltage above threshold is given by

$$Q_I = -C_o(V_{GB} - V_T) \tag{1.13}$$

When a positive gate voltage greater than V_T is applied to the gate with respect to substrate, positive charge in effect is deposited on the metal and in response, negative charge is induced in the semiconductor below the semiconductor-oxide interface by the formation of a depletion region of immobile negative charge and a surface region of a very thin layer containing mobile electrons. These thin layer of induced electron form the effective channel of the MOSFET and the effect of gate voltage is to vary the conductance of this induced channel for a low drain to source

voltage. When a drain voltage V_{DS} greater than saturation voltage V'_{DS} is applied between drain and source, the electron density near the drain will be reduced at $V_{DS} > V'_{DS}$, pinch-off will occur near the drain. After the pinchoff of the channel the effective channel length of a MOSFET differs from its physical channel length. Depending on the physical length of the channel MOSFETs are catagorised into long and short channel MOSFET. When the channel length L is much longer than the sum of source and drain depletetion widths $(W_S + W_D)$ (Fig. 2.3) then it is called long channel MOSFET and when $L \lesssim (W_S + W_D)$ then the MOSFET is called short channel MOSFET . The depletion widths W_S and W_D are controlled by bias voltage V_{DB} and V_{SB} respectively where V_{DB} represents drain-bulk bias and V_{SB} the source bulk bias. In short channel MOSFETs the difference between effective and physical channel length increases with the increase of drain source voltage, wheras in long channel it almost remains constant.

The main applications of MOSFET are in VLSI technology, specially in case of digital system such as semiconductor memories, long shift registers , microprocessors etc. To fabricate integrated circuits of high complexity, to increase the packing density and to improve the circuit performance it is required to reduce the size of a MOSFET. But when the device dimensions are reduced by reducing the channel length, the behaviour of the MOSFET departs from the long channel behaviour and we have to consider the short channel effects which arises due to two dimensional potential distribution and high electric field in the channel region.

1.2 Short-channel effects of a MOSFET

When the length of the channel is sufficiently long then the edge effects along the sides of the channel can be neglected and the electric field lines are everywhere

perpendicular to the surface i.e. they had components only along the x direction and a one dimensional analysis is sufficient. But when the length of the channel is reduced, the depletion layer widths of drain and source junctions become comparable to the channel length and a significant part of the electric field lines will have components along both x and y direction. The latter being the direction along the channel length. Hence a two dimensional analysis will be needed for the analysis of short channel MOSFET. Thus, unlike the long channel MOSFET the potential distribution in the short channel MOSFET depends on both the normal field ε_x (controlled by the gate voltage and back-surface bias) and the lateral field ε_y (controlled by the drain bias). This two dimensional potential results in degradation of the subthreshold behaviour, dependence of the threshold voltage on channel length, biasing voltages and failure of current saturation due to punch through. If the channel is both short and narrow then a three dimensional analysis becomes necessary. Though three dimensional analysis is accurate it is very complex and can be replaced by a simple model for effecient calculation by using empirical approximations and by examining separate phenomena one at a time. The short channel effects can be summarized as i) the edge effects along the sides of the channel at source and drain ii) channel length modulation iii) velocity saturation effects iv) hot carrier effects.

In short channel MOSFET the charges at drain and source edges must be taken into account while calculating the threshold voltage of the MOSFET. Again in short channel MOSFET the lateral extension of the depletion layer region reduces the effective channel length after the channel is pinched off which is known as channel length modulation. When the lateral electric field is increased, the channel mobility becomes field dependent and eventually velocity saturation occurs. If the field is increased further carrier multiplication near the drain occurs leading to substrate current and bipolar transistor action. High field also cause hot carrier injection into

the oxide, leading to oxide charging and subsequent threshold voltage shift. These are the short channel effects of a MOSFET which complicate the device operation and degrade device performance and should be eliminated or minimised so that a physical short channel device can preserve the electrical long channel behaviour and at the same time can maintain its desirable features.

1.3 Effect of substrate bias

In a MOSFET generally the source is connected to the substrate and both terminals are grounded. But when a negative V_{BS} is applied to the p type substrate (body) with respect to the source (n^+) a reverse bias voltage V_{SB} will be induced between the channel and the body junction and also between the source and the substrate junction. In this case the inversion layer-substrate combination will act as a field induced n^+p junction and the source substrate junction will act as a regular pn junction . In either case, the depletion region is widened and the threshold voltage required to achieve inversion must be increased to accomodate the larger Q_B.

When a voltage V_{SB} is applied between the source and substrate the bias will shift the quasi fermi level at the source by V_{SB} . So the surface potential at the source during strong inversion can be modified as

$$\psi_s = V_{SB} + \phi_{si} \tag{1.14}$$

When V_{SB} is zero the surface potential and the charge in the space charge layer is given by

$$\psi_s = 2\phi_f \tag{1.15}$$

and

$$\begin{aligned} Q_B &= -qN_A w \\ &= -(2q\epsilon_s N_A \phi_{si})^{1/2} \end{aligned} \tag{1.16}$$

For an arbitary reverse bias voltage V_{SB}, the bulk charge becomes

$$Q_B = -[2q\epsilon_s N_A (V_{SB} + \phi_{si})]^{1/2} \tag{1.17}$$

Therefore, the increased differential charge is

$$\Delta Q_B = -(2q\epsilon_s N_A)^{1/2}[(V_{SB} + \phi_{si})^{1/2} - \phi_{si}^{1/2}] \tag{1.18}$$

To reach the strong inversion , the applied gate voltage must be increased to compensate for ΔQ_B. Therefore,

$$\begin{aligned} \Delta V_T &= -\frac{\Delta Q_B}{C_o} \\ &= \frac{(2q\epsilon_s N_A)^{1/2}}{C_o}[(V_{SB} + \phi_{si})^{1/2} - \phi_{si}^{1/2}] \end{aligned} \tag{1.19}$$

When a positive V_{BS} is applied to the substrate with respect to source then the situation will be reversed. The source-substrate and channel-substrate junction both will be forward biased and to maintain the charge balance equation the inversion layer charge must be increased, whereas, the depletion layer charge is decreased. So in an n channel MOSFET, V_{BS} must be zero or negative to avoid the forward bias of the source junction.

1.4 Characteristics of short channel.MOSFET

When the dimensions of a MOSFET are reduced the distinct features are seen in device characteristics. First the drain current is found to increase with the drain voltage due to channel length modulation beyond pinch-off. This is in contrast with the I-V curve of a long channel MOSFET, where the drain current becomes constant after the pinch-off condition. But the output current in short channel MOSFET does not saturate. The second feature of a short channel MOSFET can be seen in the subthreshold region where the gate losses control over the drain current. In other words, the output drain current can't be reduced to zero i.e. can't be turned off. The third feature is that due to the presence of velocity saturation the drain current in short channel MOSFET for a fixed drain-source voltage is smaller than the corresponding drain current in long channel MOSFET. The fourth distinct feature of a short channel MOSFET is the shift of its threshold voltage with the channel length as well as drain bias voltage. Whereas, the threshold voltage of a long channel MOSFET is not a function of either drain bias or channel length.

1.5 Hot carrier effect and avalanche breakdown

At relatively small V_{DS}, high electric field will exist in the drain depletion region and electron hole pairs will be generated due to impact ionization. The mechanism of avalanche breakdown of a junction involves the impact ionization of host atoms by energetic carriers. Normal lattice-scattering event can result in the creation of electron-hole pair if the carrier being scattered has sufficient energy. If a large reverse voltage is applied across a p-n junction, the electric field in the transition region becomes large and an electron entering from the p side may be accelerated

to high kinetic energy to cause an ionizing collision with the lattice. A single such interaction results in carrier multiplication. The degree of multiplication can become very high if carriers generated within the transition region also have ionizing collisions with the lattice. This is an avalanche process, since each incoming carrier can initiate the creation of a large number of new carriers.

In the reverse bias drain to substrate junction, the electric field may be quite high in short channel device. Carriers that are injected into the depletion layer are accelerated by the high field, and some of them may gain enough energy to cause impact ionization. These carriers have higher energy than thermal energy and are called hot carriers. Most of the electrons generated by the avalanche multiplication are normally attracted by the drain and the holes generated by multiplication can flow to the subtrate, giving rise to a large substrate current (Fig 1.3). The situation is further complicated by the fact that the region between the source and drain can act like the base of a bipolar npn transistor, with the source acting as the emitter and the drain as the collector. Now if the substrate current produces a voltage drop in the substrate material of the order 0.7 V, the substrate-source pn junction will conduct significantly. Electrons can be injected from the source to the substrate, just like electrons injected from emitter to base in an npn transistor. These electrons can in turn, gain sufficient energy as they travel toward the drain to cause additional impact ionization and create new electron-hole pairs. This constitutes a positive feedback mechanism, which can sustain itself if the drain voltage exceeds a certain value. This is observed externally as breakdown causing current values higher than normally expected.

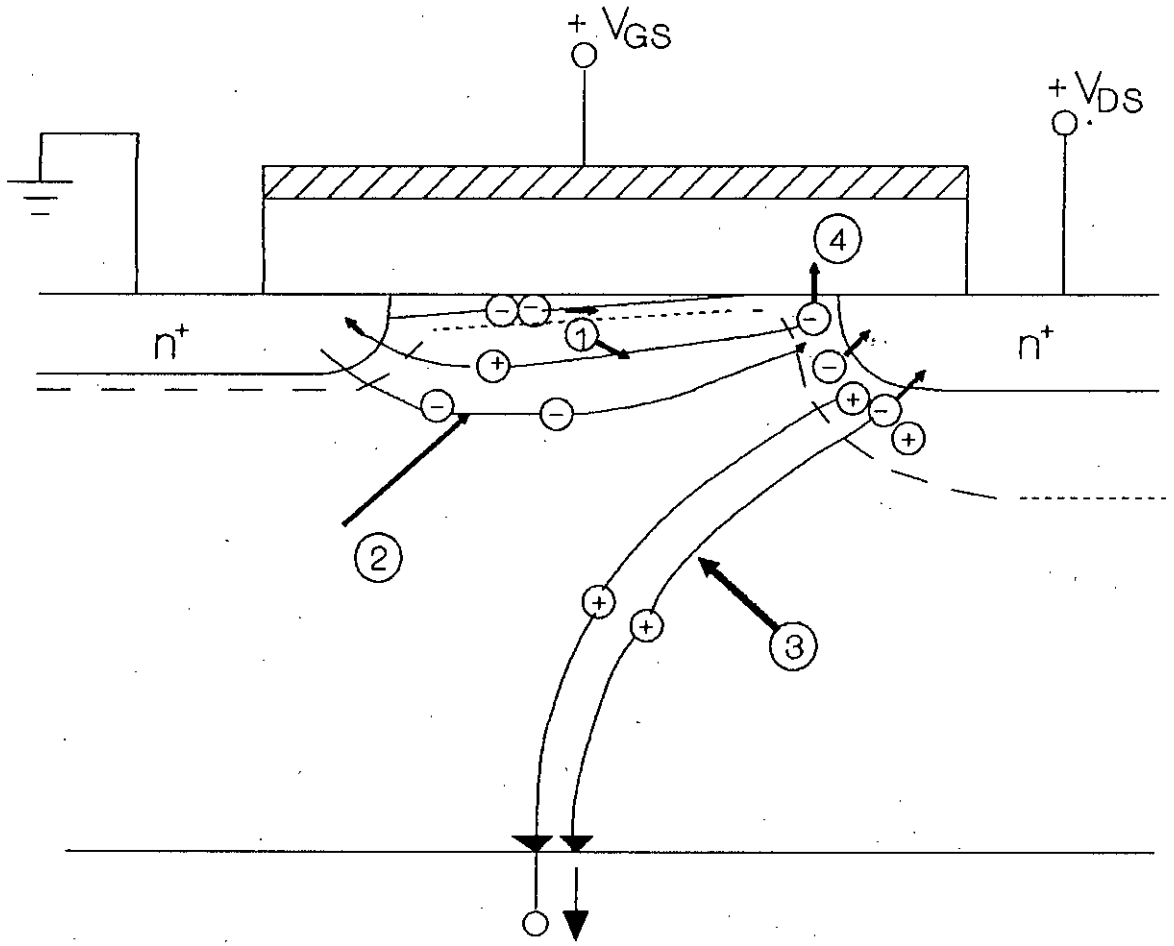


Fig. 1.3. Effect of hot carrier in short channel MOSFET.

(1) Holes reaching the source
(2) Electron injection from the source
(3) Substrate hole current
(4) Electron injection into the oxide

1.6 Review of recent works on the breakdown of MOSFET

A number of analytical and numerical models on the breakdown of short channel MOSFET have been developed in the last few years. D.P Kennedy and A. Phillips [6] in 1973 first developed a source drain breakdown model and suggested that the positive feedback effect involving bipolar transistor action is the main breakdown mechanism in short channel MOSFET. But in his work the dependence of breakdown on biases and geometries were not investigated. In 1977 T. Toyabe [7] developed a two dimensional avalanche breakdown model of short channel MOSFET and concluded that the breakdown in short channel MOSFET occurs when the voltage across the source-substrate junction is of the order of 0.7 V. Later in 1978 he proposed a numerical model of avalanche breakdown which is a modified version of his previous model. E. Sun [8] in his breakdown model of short channel MOSFET showed that the turning on of the source substrate junction is not a sufficient condition for breakdown. Later Fu-Chieu Hsu, Simon Tam [9] derived a simple analytical breakdown model that combines the effects due to ohmic drop caused by the substrate current and the positive feedback effect of the substrate lateral bipolar transistor. They pointed out that drain source breakdown in most short channel MOSFETs is neither simple junction avalanche breakdown nor source to drain punchthrough but avalanche-induced breakdown and two conditions must be satisfied before the breakdown can occur. One is the emission of minority carrier into the substrate from the source and the other is sufficient avalanche multiplication to cause significant positive feedback. Wolfgang Muller [18] analysed MOS transistor in avalanche multiplication region for different doped transistor at varying channel lengths. In his work ionization integrals, internal body effect and parasitic bipolar turn-on have been investigated in dependence of channel doping profile and substrate doping level. He suggested that a deep channel implant in devices with

high resistivity substrate improves the source barrier and lower substrate resistivity to shift the bipolar trigger voltage to higher drain voltage of the order of 1-2 V.

Chenming Hu [10] in 1982 showed that a phenomena of second breakdown similar to that in bipolar transistor can also occur in vertical power MOSFET. A good agreement between measured and calculated values based on his analysis was achieved over a wide range of device parameters. In 1983 Hsu [11] presented a simplified model which is an extended version of his previous work. In this work Hsu included the effects of those carriers injected from the source into the substrate and collected by the drain. He also incorporated substrate conductivity modulation to account for the behaviour of the substrate current and current collected at nearby junction in the breakdown region. Tomasz Skotnicki, Gerard Merckel [20] revealed in 1989 that the physics of multiplication induced breakdown is eventually different from what the previous authors have reported. They proposed that two consecutive phases of breakdown, enhanced body effect and parasitic bipolar action have to be treated differently. They also showed that enhanced body effect can't be replaced by ordinary body effect resulting from the external positive bulk bias. Similarly they proposed an unconventional mode of biasing of the bipolar transistor and took into account the effect of variable geometry of the substrate to incorporate the variation of substrate resistance with drain source voltage. Tomasz resolved the shortcomings of the work done by the previous authors who failed to explain the constant substrate voltage with the increase of substrate current and limit its value to 0.7 V to match the measured I-V characteristics of the MOSFET in the breakdown region which leads to a number of contradictions. The first contradiction is that the substrate voltage remains fixed while substrate current is increasing and substrate resistance is fixed. The second contradiction is the saturation of substrate current as reported by some authors which is in complete disagreement with the measured substrate current. The third contradiction is that the saturation of sub-

strate current implies almost constant drain current which is also contradictory to the rapid increase of drain current with V_{DS}.

1.7 Summary of the thesis

A number of different models have been developed so far to find the drain characteristics of a short channel MOSFET in the multiplication breakdown region. Different authors have used different approaches to develop their models. But most of the reported works failed to incorporate the exact physical mechanism that drives a short channel MOSFET in the breakdown region. In this thesis, an analytical model comprising of a detailed physics of a short channel MOSFET in its avalanche multiplication region is presented. The main model consists of four small different models namely channel current model $I_{\mathbf{ch}}$, excess channel current model $\triangle I_{\mathbf{ch}}$, the substrate current model $I_{\mathbf{sub}}$ and the emitter current model $I_{\mathbf{e}}$. Various short channel effects have been taken into account while developing these models.

In the first chapter of this thesis, the literature survey of a MOSFET including its threshold voltage, body (substrate bias) effect and various undesirable effects have been undertaken. The effect of hot carrier and substrate current produced by the mechanism of avalanche multiplication that drives a short channel MOSFET into the breakdown mode have been described briefly in this chapter. Recent works carried out by various authors on the breakdown of short channel MOSFET are also reviewed in this chapter.

In chapter 2, a detailed analysis of the breakdown model along with the physics is presented to find the I-V characteristics of a short channel MOSFET . The total drain current in the avalanche multiplication region consists of four different cur-

rent components i) conventional channel current due to electron flow from source to drain ii) excess channel current due to threshold lowering iii) substrate current due to hole produced by avalanche multiplication iv) emitter current due to bipolar action of the MOSFET. For the channel current model a simple but efficient method is used where the change of threshold voltage with drain source voltage and channel length have been taken into account. An accurate substrate current model is developed where the effect of junction depth, oxide thickness, drain voltage, substrate doping on multiplication factor have been incorporated. In developing the emitter current model the effective channel length is represented by an analytical one and later an empirical expression is derived to find the complete drain and substrate characteristic of the short channel MOSFET.

In chapter 3 of the thesis the drain and substrate characteristics based on the analytical model developed in chapter 2 and a computer programme scheme to study the characteristics are presented.

The final chapter contains the concluding remarks with suggestions for further work on this topic.

CHAPTER 2

ANALYTICAL BREAKDOWN MODEL OF SHORT CHANNEL MOSFET

2.1 Introduction

The mechanism of bipolar induced breakdown due to impact ionization in short channel MOSFET has been studied by many authors [6-11, 20]. In this thesis an analytical model is presented. This model can be applied for a wide range of MOSFET channel lengths to find different I-V characteristics of the MOSFET.

The physics of the avalanche induced breakdown problem along with different current components has been illustrated in Fig. 2.1 for an n channel MOSFET. Channel electrons that travel through the high field avalanche region cause impact ionization. The electric field in the high-field region sweeps the electron generated by impact ionization into the drain and holes into the bulk. The holes created at the high field avalanche region first causes a reduction in the channel region depletion width and thus lowers the threshold voltage $\hat{V}_T$ of the MOSFET and then the ohmic drop caused by the hole flowing through the high resistivivity substrate forward biases the source junction to initiate the bipolar action of the MOSFET and

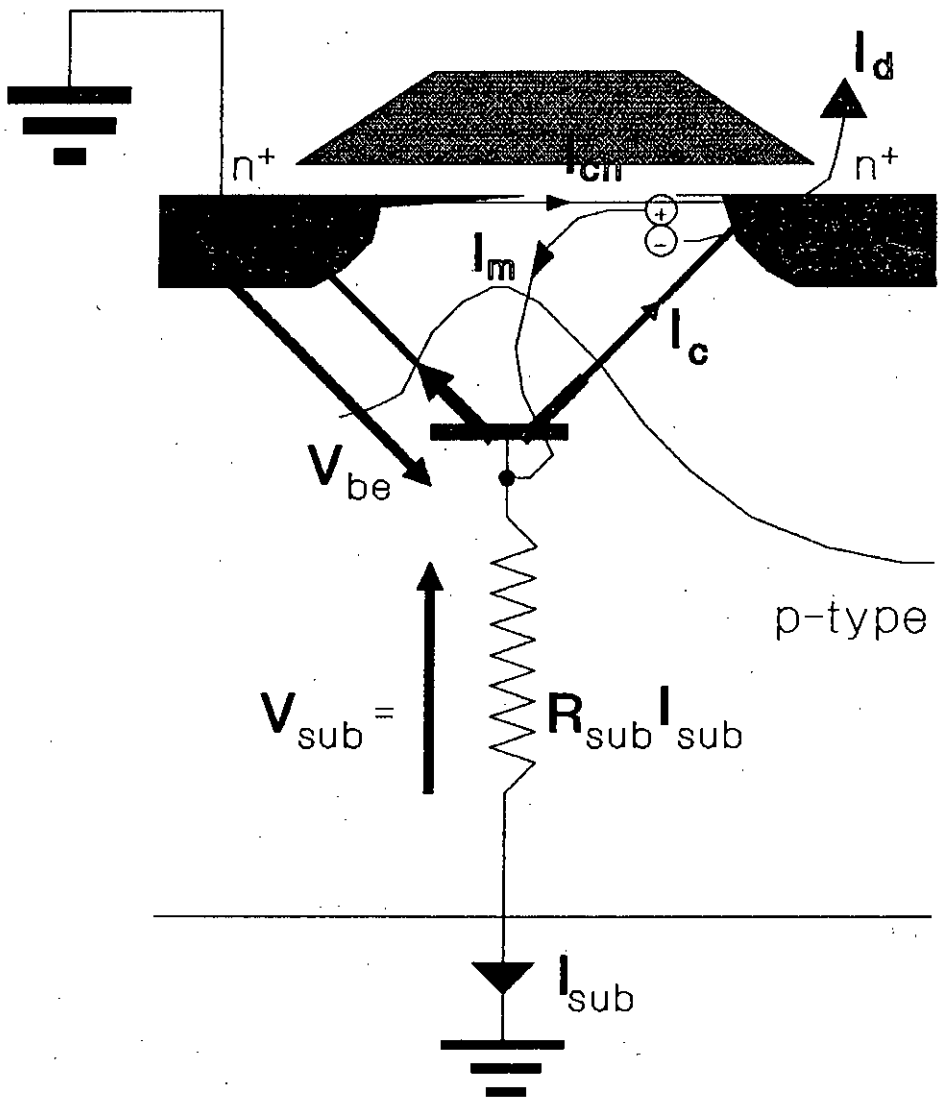


Fig. 2.1 Current components with bipolar induced breakdown in short channel MOSFET.

hence cause it to inject electrons. Part of these injected electrons travel to the drain junction and will further be multiplied by the drain field, causing positive feedback action. So after the bipolar turn-on of the MOSFET the drain current I_d consists of three components of current i) channel current I_{ch} , ii) excess channel current ΔI_{ch} due to threshold lowering of the MOSFET and iii) the collector current I_c of the bipolar npn transistor . On the other hand, the hole current I_m due avalanche multiplication consists of base current I_b and the substrate current I_{sub}. From the equivalent circuit (Fig. 2.2) of a MOSFET after the bipolar turn on, the necessary equations relating different current components can be represented as follws,

$$I_d = M(I_c + I_{ch} + \Delta I_{ch}) \quad (2.1)$$

$$I_m = (M-1)(I_c + I_{ch} + \Delta I_{ch}) \quad (2.2)$$

where, M is the multiplication factor. From equations (2.1) (2.2) and (fig 2.5) we get

$$I_m = I_{sub} + I_b = (1 - \frac{1}{M})\, I_d \quad (2.3)$$

But the drain current is related to substrate current as follows (from equation 2.1 and 2.2)

$$\begin{aligned} I_d &= M(I_c + I_{ch} + \Delta I_{ch}) \\ &= I_m + I_c + I_{ch} + \Delta I_{ch} \end{aligned}$$

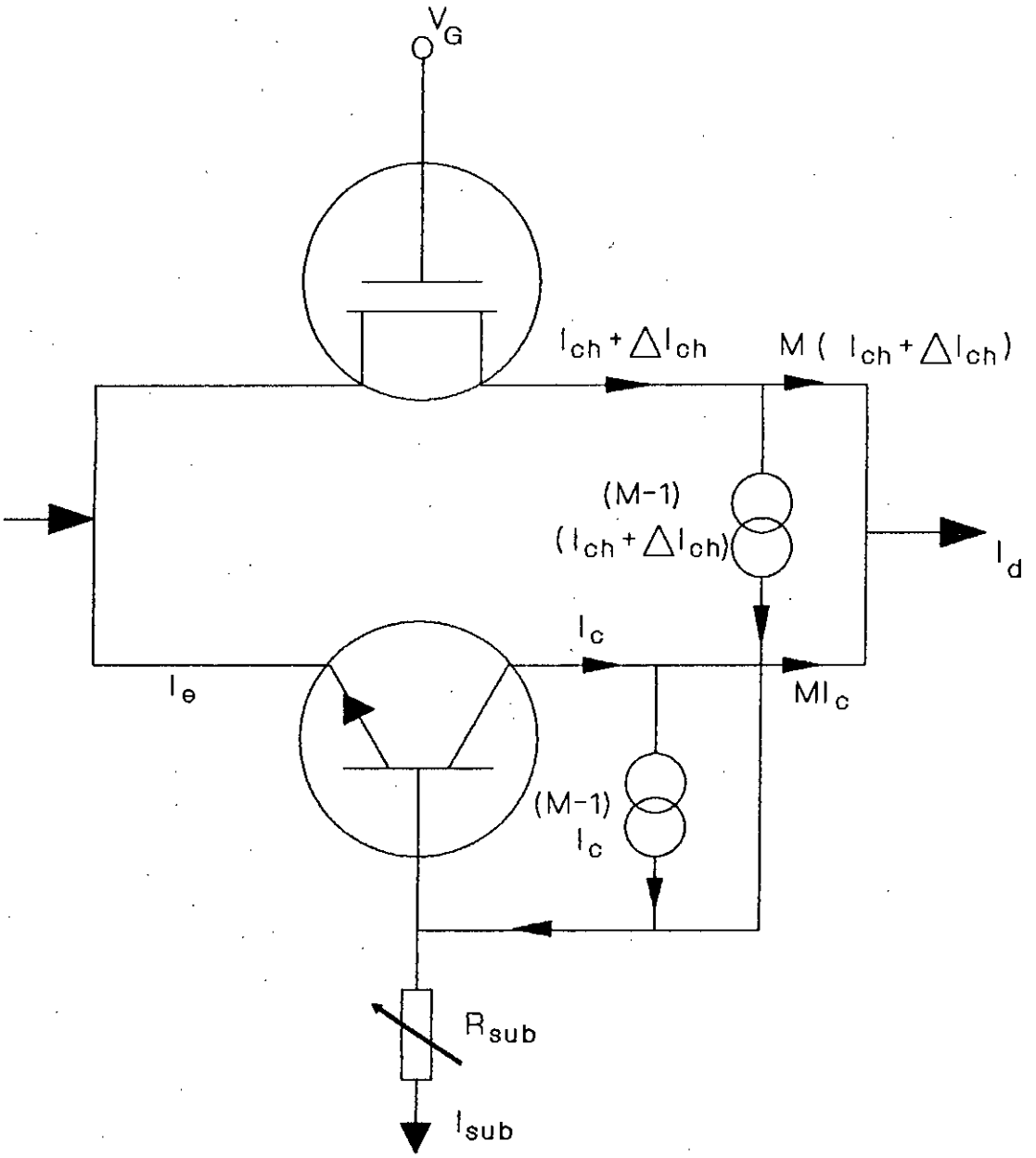


Fig. 2.2 Equivalent circuit of a short channel MOSFET after the bipolar turn on.

$$
\begin{aligned}
&= I_{sub} + I_b + I_c + I_{ch} + \Delta I_{ch} \\
&= I_{sub} + I_e + I_{ch} + \Delta I_{ch} \\
&= I_{sub} + I_s
\end{aligned} \tag{2.4}
$$

where, I_e is the emitter current and I_s is the source current and is given by

$$
I_s = I_{ch} + \Delta I_{ch} + I_e \tag{2.5}
$$

So from equation (2.4) and (2.5) the expression for substrate current can be given by the relation

$$
I_{sub} = (1 - \frac{1}{M})\,(I_{sub} + I_s) - I_b \tag{2.6}
$$

If the multiplication factor M can be found we shall be able to find the substrate current I_{sub}.

2.2 Enhanced Body Effect

The breakdown in short channel MOSFET is not a simple junction avalanche breakdown rather it is a breakdown induced by avalanche multiplication. Two consecutive phases of breakdown occur in such a small channel MOSFET. First, the rise in drain current is caused by the enhanced body effect (EBE) and then the sharp rise in drain current is initiated by the parasitic bipolar action of the MOSFET. The physical mechanism of the enhanced body effect is that the holes, multiplied in the drain junction, bias the substrate spreading resistance when flowing towards the substrate terminal. This bias corresponds to a reduction in the channel region depletion width from w_o which corresponds ($I_{sub} = 0$) to w and thus releases a

certain amount of bulk charge Q_B of ionized impurities, which was initially tied by the gate field. This reduction in bulk charge of the amount ΔQ_{BS} implies a threshold lowering of the MOSFET and enhancement of inversion layer charge by the amount ΔQ_{BS} so as to preserve the overall charge neutrality ,

$$\begin{aligned} Q_B + Q_I &= Q_G \\ &= C_o\,(V_{GB} - \psi_s) \\ &= const. \end{aligned} \tag{2.7}$$

This enhanced body effect is quite different from the body effect resulting from the applied external positive biasing of the bulk (body) which also causes a reduction in threshold voltage. But the difference between these two body effects results from the fact that the ordinary body effect does not involve any electric field in the bulk whereas, the enhanced body effect EBE requires a nonvanishing electric field in the bulk, necessary to drive the substrate current. In case of EBE, the variation in potential in the bulk no longer disappears along the depth from depletion edge boundry to the substrate terminal and the substrate current in the bulk flows due to drift of the holes rather than diffusion. The holes after multiplication spread towards the bulk and follow the doping distribution ($p = N$) which makes the gradient of concentration along the depth of the MOSFET zero and leads to zero diffusion current in the bulk. The nonzero electric field required to ensure the drift of holes is given by

$$E = \frac{I_{\mathbf{sub}}}{q\mu_p N l Z} \tag{2.8}$$

In the equation l accounts for the lateral spreading of the substrate current and

is given by (Fig. 2.3)

$$l = L - (l_s + l_d) \tag{2.9}$$

where, L is the physical channel length of the MOSFET and

$$l_s \approx \sqrt{\frac{2\epsilon_s}{qN_A}(V_{bi} - \psi_s)}$$

$$l_d \approx \sqrt{\frac{2\epsilon_s}{qN_A}(V_{bi} - \psi_s + V_{DS})}$$

2.3 Channel current model

In this section first the channel current model for a long channel MOSFET is developed and by some modifications to this model a channel current model for a short channel MOSFET is derived. With strong inversion guaranteed at the source end of the channel the drain end will also be strongly inverted. With both channel ends strongly inverted, the application of bias voltage V_{SB} at the source end and V_{DB} at the drain end will shift the quasi fermi level at the corresponding end by V_{SB} and V_{DB} respectively. The corresponding surface potentials at the ends can be represented as

$$\psi_{SO} = \phi_{si} + V_{SB} \tag{2.10}$$

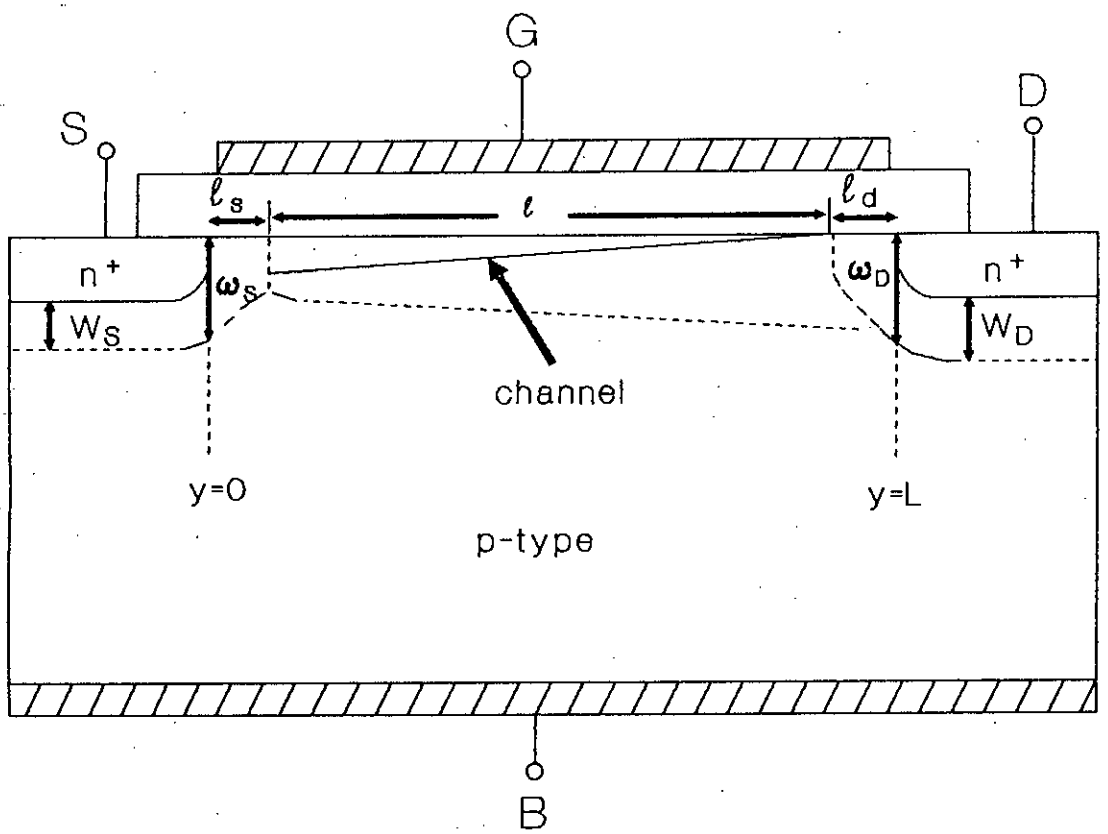


Fig. 2.3. Simplified diagram of an n-channel MOSFET.

$$\psi_{SL} = \phi_{si} + V_{DB} \tag{2.11}$$

where ψ_{SL} and ψ_{SO} are the surface potential at the drain and source end respectively. In strong inversion the concentration of carriers in the channel region is high and there is a significant variation in surface potential from ψ_{SO} at the source end to ψ_{SL} at the drain end. Hence, the channel current is predominantly due to drift mechanism of the carrier rather than diffusion as the gradient of concentration along the channel is small. The drift component of the channel current along the channel due to variation in surface potential $\psi_s(y)$ determines the channel current $I_{\mathbf{ch}}$ in strong inversion.

$$I_{\mathbf{ch}} = \mu Z(-Q_l)\frac{d}{dy}\psi_s(y) \tag{2.12}$$

where, Z is the width of the channel.

But the variation of surface potential ψ_s can be represented as

$$I_{\mathbf{ch}} = \mu Z(-Q_l)\frac{d}{dy}\psi_s(y) \tag{2.13}$$

where, with channel length L

$$V_{CB}(y) = V_{SB}, \qquad y = 0$$

$$V_{CB}(y) = V_{DB}, \qquad y = L$$

Now,

$$I_{\mathbf{ch}} = \mu Z(-Q_I)\frac{d}{dy}V_{CB} \tag{2.14}$$

The inversion layer charge Q_I is given by

$$\begin{aligned} Q_I &= -C_o(V_{GB} - V_{FB} - \psi_s + \frac{Q_B}{C_o}) \\ &= -C_o(V_{GB} - V_{FB} - \phi_{si} - V_{CB} - \gamma\sqrt{\phi_{si} + V_{CB}}) \end{aligned} \tag{2.15}$$

where, the depletion layer charge Q_B is

$$Q_B = -C_o\gamma\sqrt{\phi_{si} + V_{CB}} \tag{2.16}$$

and

$$\frac{Q_B}{C_O} = -\gamma\sqrt{\phi_{si} + V_{CB}} \tag{2.17}$$

By expanding the equation (2.17) into Taylor series around $V_{CB} = V_{SB}$ we get

$$-\frac{Q_B}{C_o} \approx \gamma\sqrt{\phi_{si} + V_{SB}} + \gamma\frac{(V_{CB} - V_{SB})}{2\sqrt{\phi_{si} + V_{SB}}} \tag{2.18}$$

$$\approx \gamma\sqrt{\phi_{si} + V_{SB}} + \delta_1(V_{CB} - V_{SB}) \tag{2.19}$$

where,

$$\delta_1 = \frac{\gamma}{2\sqrt{\phi_{si} + V_{SB}}}$$

The value of δ_1 is modified again by δ for the best fitting of the curve. The value of δ is

$$\delta = \frac{d_2\gamma}{2\sqrt{\phi_{si} + V_{SB}}}$$

where, d_2 varies from 0.5 to 0.8 [12]

Now, the expression for the inversion layer charge Q_I becomes

$$\begin{aligned} Q_I &= -C_o\left[V_{GB} - V_{FB} - \phi_{si} - \gamma\sqrt{\phi_{si} + V_{SB}} - \delta(V_{CB} - V_{SB}) - V_{CB}\right] \\ &= -C_o\left[(V_{GB} - V_{SB}) - V_{FB} - \phi_{si} - \gamma\sqrt{\phi_{si} + V_{SB}} - (1+\delta)(V_{CB} - V_{SB})\right] \\ &= -C_o\left[(V_{GS} - V_T) - (1+\delta)(V_{CB} - V_{SB})\right] \end{aligned} \tag{2.20}$$

In equation (2.20) the threshold voltage taking the effect of body bias V_{SB} is given by

$$V_T = V_{FB} + \phi_{si} + \gamma\sqrt{\phi_{si} + V_{SB}}$$

The channel current I_{ch} from equation (2.12) is

$$I_{ch} = \mu Z(-Q_I)\frac{dV_{CB}}{dy} \tag{2.21}$$

$$\int_o^L I_{ch}\, dy = \int_o^L \mu Z(-Q_I)\frac{dV_{CB}}{dy}dy \tag{2.22}$$

i.e.,

$$I_{ch}L = \int_{V_{SB}}^{V_{DB}} \mu Z(-Q_I)dV_{CB} \tag{2.23}$$

With $V_{DB} = V_{DS} + V_{SB}$ and $V_{GB} = V_{GS} + V_{SB}$ the channel current after integration of equation (2.23) is obtained as

$$I_{ch} = \frac{Z\mu C_o}{L}\left[(V_{GS} - V_T)V_{DS} - .5(1+\delta)V_{DS}^2\right] \tag{2.24}$$

By taking the effect of normal component of the electric field on the mobility of electrons in the inversion layer that leads to acceleration of electrons toward the oxide-interface we get the effective mobility μ_{eff} [4]

where,

$$\mu_{eff} = \frac{\mu_o}{1 + \theta(V_{GS} - V_T) + \theta_B V_{SB}}$$

The expression of the channel current I_{ch} with μ replaced by μ_{eff} becomes

$$I_{ch} = \frac{Z\mu_{eff}C_o}{L}\left[(V_{GS} - V_T)V_{DS} - .5(1+\delta)V_{DS}^2\right] \qquad (2.25)$$

The expression of the channel current is valid upto saturation voltage V'_{DS}, beyond which the channel is pinched off and the current is saturated.

Accordingly,

$$I_{ch} = \frac{Z\mu_{eff}C_o}{L}\left[(V_{GS} - V_T)V_{DS} - .5(1+\delta)V_{DS}^2\right] \quad for\ V_{DS} \leq V'_{DS} \qquad (2.26)$$

$$= I'_{ch} \quad for\ V_{DS} > V'_{DS} \qquad (2.27)$$

where, I'_{ch} is the channel current I_{ch} at a drain source voltage V'_{DS} obtained from equation (2.26) . This is the channel current model for a long channel MOSFET and by considering various short channel effects the corresponding model for the short channel MOSFET can be obtained from this model.

For a short channel MOSFET which is also narrow , a three dimensional analysis is required for obtaining the accurate channel characteristics. Such an analysis involves the solution of three dimensional Poisson's equation and is very complex. However, for efficient calculation a simple channel current model can be developed

by taking into consideration the follwing short channel effects simultaneously in the long channel model and combining them in a single model.

The various short channel effects are : i) Effect of velocity saturation. ii) Effect of channel length modulation. iii)Effect of channel length L on effective threshold. iv) Effect of drain source voltage V_{DS} on effective threshold. v) Effect of width Z of the channel on effective threshold.

2.3.1 Velocity saturation effect

In the channel current model developed for the long channel MOSFET, it is assumed that the lateral (horizontal) component ε_y of the electric field is small enough so that the drift velocity of the carrier v_d is proportional to ε_y. But in case of short channel MOSFET this relation is violated due to high value of electric field ε_y and the previously developed channel current model for long channel MOSFET requires some modifications. Actually the velocity of carriers in the inversion layer of short channel MOSFET saturates at a high value of electric field ε_y and does not increase with the electric field (Fig. 2.4) due to the generation of phonons by the scattering collision of the carriers with the lattice. So the drift velocity is modified as

$$|v_d| = \mu|\varepsilon_y| \qquad for|\varepsilon_y| \ll \varepsilon_c \tag{2.28}$$

$$= v_{dmax} \qquad for|\varepsilon_y| \gg \varepsilon_c \tag{2.29}$$

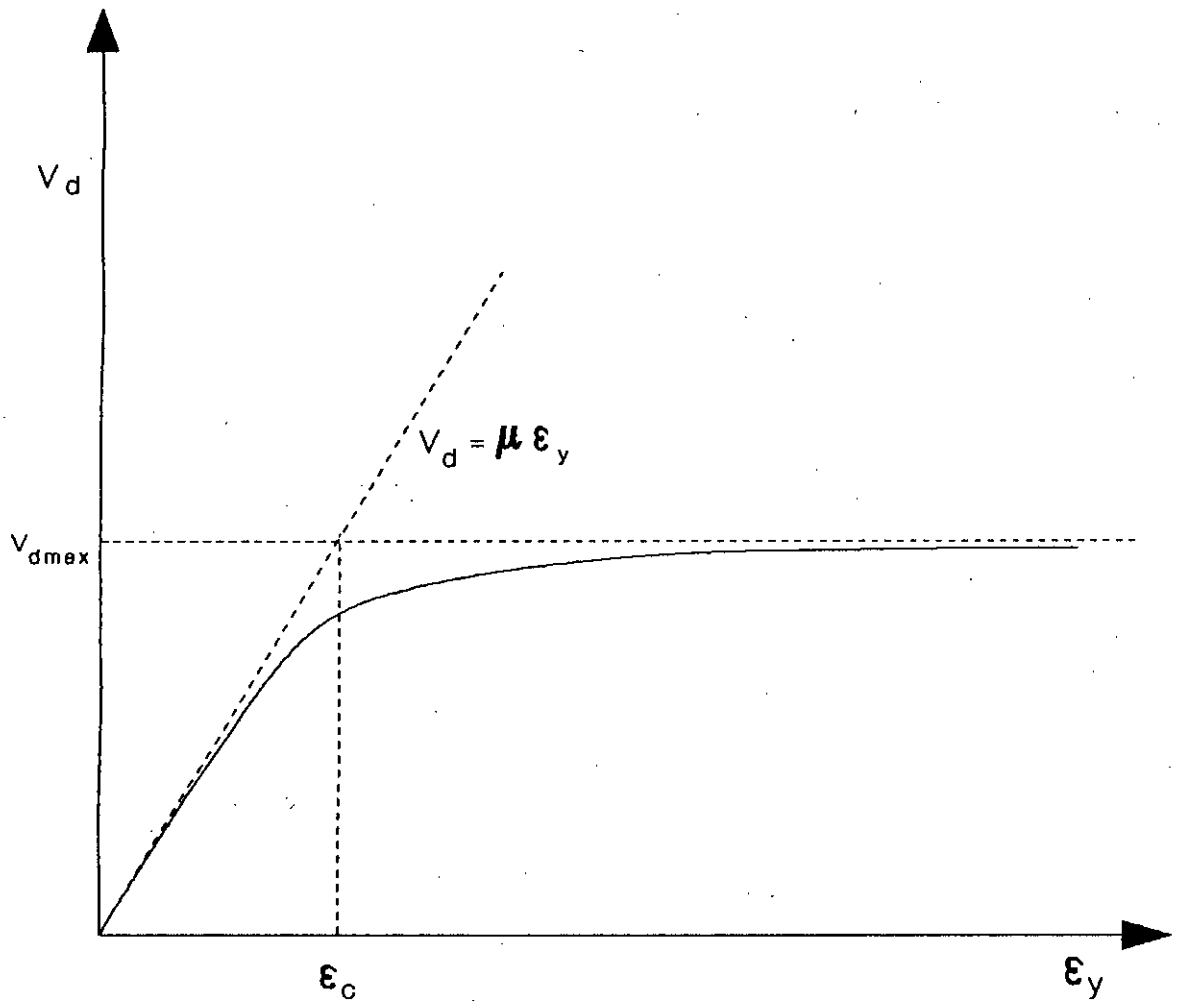


Fig. 2.4 Carrier velocity vs. lateral component of electric field.

where, ε_c is the critical field and is given by

$$\varepsilon_c = \frac{v_{dmax}}{\mu} \tag{2.30}$$

A single expression of drift velocity $v_d(y)$ can be obtained from equation (2.28) and (2.29) and is given by

$$v_d = v_{dmax}\frac{\varepsilon_y/\varepsilon_c}{1+\varepsilon_y/\varepsilon_c} \tag{2.31}$$

where, the lateral electric field ε_y is given by

$$\varepsilon_y = \frac{dV_{CB}}{dy} \tag{2.32}$$

Hence, $v_d(y)$ is given by

$$\begin{aligned} v_d(y) &= v_{dmax}\frac{(1/\varepsilon_c)(dV_{CB}/dy)}{1+(1/\varepsilon_c)(dV_{CB}/dy)} \\ &= \mu\,\frac{dV_{CB}/dy}{1+\ (dV_{CB}/dy)(1/\varepsilon_c)} \end{aligned} \tag{2.33}$$

Now, the channel current of long channel MOSFET will be modified due to velocity saturation effect in short channel MOSFET as below,

$$I_{ch} = Z(-Q_I)\mu\frac{dV_{CB}/dy}{1+(dV_{CB}/dy)(1/\varepsilon_c)} \tag{2.34}$$

Integrating both sides of the equation and after some simplification we ultimately get the channel current I_{ch} including velocity saturation.

$$\int_o^L I_{\mathbf{ch}}\, dy \; + I_{\mathbf{ch}} \int_{V_{SB}}^{V_{DB}} dV_{CB}\,(1/\epsilon_c) \; = Z\mu \int_{V_{SB}}^{V_{DB}} (-Q_I) dV_{CB} \tag{2.35}$$

Upon integration the channel current $I_{\mathbf{ch}}$ becomes

$$I_{\mathbf{ch}} = \frac{Z}{L} \quad \frac{\mu}{1 + V_{DS}/(L\epsilon_c)} \quad \int_{V_{SB}}^{V_{DB}} (-Q_I) dV_{CB} \tag{2.36}$$

where,

$$V_{DB} - V_{SB} = V_{DS}$$

Comparing with equation (2.23) the channel current expression in all the non-saturation region taking the effect of velocity saturation can be modified as follows

$$I_{\mathbf{ch,\ including\ velocity\ saturation}} = \frac{I_{\mathbf{ch,\ not\ including\ velocity\ saturation}}}{1 + \; V_{DS}/(L\epsilon_c)} \tag{2.37}$$

2.3.2 Effect of L, V_{DS}, Z on threshold voltage

The threshold voltage of a long channel MOSFET is given by

$$\begin{aligned} V_T &= V_{FB} + \phi_{si} - \frac{Q_B}{C_O} \\ &= V_{FB} + \phi_{si} + \gamma\sqrt{\phi_{si} + V_{SB}} \end{aligned} \tag{2.38}$$

where Q_B is the depletion region charge and is given by

$$Q_B = -qN_A w \quad \bullet$$

where, w is the depletion width.

The total charge that is contributing to the threshold in equation (2.38) is ZLQ_B, the charge represented by rectangle with width Z and length L. But in short channel MOSFET, a part of this charge is shared by drain and source such that only the area inside the trapezoid (Fig. 2.5) is controlled by gate and the charge inside it contributes to the actual threshold of the short channel MOSFET. So the actual bulk charge Q'_B will be less than Q_B and is given by

$$\begin{aligned} Q'_B &= Q_B \left(\frac{L+L'}{2}\right) \frac{Z\,w}{Z\,L\,w} \\ &= Q_B \ \frac{L+L'}{2\,L} \end{aligned} \tag{2.39}$$

But

$$\begin{aligned} \frac{L+L'}{2\,L} &= 1-(\sqrt{1+\frac{2w}{d_j}}-1)\,\frac{d_j}{L} \\ &\approx 1-\frac{d_j}{L}\left[1+(\frac{1}{2}).\frac{2\,w}{d_j}+\cdots-1\right] \\ &\approx 1-\frac{w}{L} \end{aligned} \tag{2.40}$$

The validity of the expression for the effective charge Q'_B can be extended by introducing an empirical constant α_1

$$Q'_B = Q_B(\,1-\ \frac{\alpha_1\,w}{L}) \tag{2.41}$$

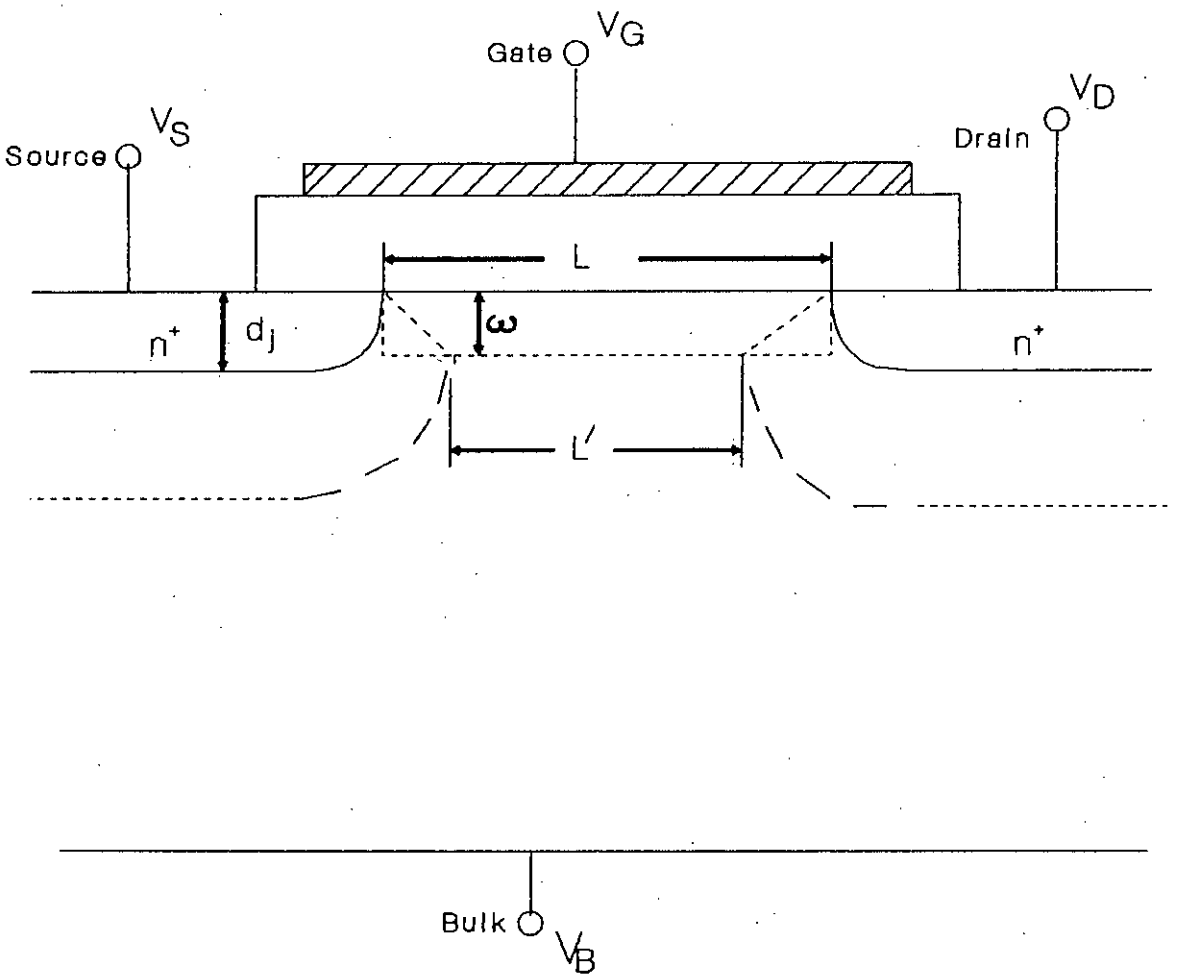


Fig. 2.5 Charge sharing model of a MOSFET.

i.e.

$$\frac{Q'_B}{Q_B} = (1 - \frac{\alpha_1 w}{L}) \tag{2.42}$$

Now the reduction in threshold voltage ΔV_T due to significant charge sharing at drain and source end in short channel MOSFET is given by

$$\begin{aligned} \Delta V_T &= \frac{Q_B}{C_o} - \frac{Q'_B}{C_o} \\ &= \frac{Q_B}{C_o}(1 - \frac{Q'_B}{Q_B}) \\ &= \gamma \sqrt{\phi_{si} + V_{SB}} \, (\frac{\alpha_1 w}{L}) \end{aligned} \tag{2.43}$$

Replacing the values of $\gamma = \frac{\sqrt{2\epsilon_s N_A}}{C_o}$ and $C_o = \frac{\epsilon_{ox}}{t_{ox}}$ in equation (2.43) we get

$$\Delta V_T = 2\,\alpha_1 \frac{\epsilon_s}{\epsilon_{ox}} \frac{t_{ox}}{L} (\phi_{si} + V_{SB}) \tag{2.44}$$

This expression is valid when drain source voltage $V_{DS} = 0$ so that depletion width w_S at the source end and the depletion width at the drain end w_D are equal and we can assume a uniform depletion width along the channel. For a drain source voltage greater than 0 the depletion region width around the drain end will widen and the trapezoid assumption will lead erroneous result. Considering an average depletion width of $\frac{w_S + w_D}{2}$ the effective charge Q'_B from equation (2.41) is given by

$$Q'_B = Q_B \left(1 - \frac{w_S + w_D}{2} \frac{\alpha_1}{L}\right) \tag{2.45}$$

where,

$$w_S = \sqrt{\frac{2\,\epsilon_s\,(\phi_{si} + V_{SB})}{q\,N_A}} = \zeta\sqrt{\phi_{si} + V_{SB}} \tag{2.46}$$

$$w_D = \sqrt{\frac{2\,\epsilon_s(\phi_{si} + V_{DB})}{q\,N_A}} = \zeta\sqrt{\phi_{si} + V_{DB}} \tag{2.47}$$

and

$$\zeta = \sqrt{\frac{2\epsilon_s}{q\,N_A}}$$

But, the average depletion width can be approximated as

$$\begin{aligned}
\frac{w_S + w_D}{2} &= \frac{\zeta}{2}\left(\sqrt{\phi_{si} + V_{SB}} + \sqrt{\phi_{si} + V_{DB}}\right) \\
&= \frac{\zeta}{2}\left[\sqrt{\phi_{si} + V_{SB}} + \sqrt{\phi_{si} + V_{SB} + V_{DS}}\right] \\
&= \frac{\zeta}{2}\left[\sqrt{\phi_{si} + V_{SB}} + \sqrt{\phi_{si} + V_{SB}}\left(1 + \frac{V_{DS}}{\phi_{si} + V_{SB}}\right)^{1/2}\right] \\
&\approx \frac{\zeta}{2}\left[\sqrt{\phi_{si} + V_{SB}} + \sqrt{\phi_{si} + V_{SB}}\left(1 + \frac{1}{2}\,\frac{V_{DS}}{\phi_{si} + V_{SB}}\right)\right] \\
&\approx \zeta\left(\sqrt{\phi_{si} + V_{SB}} + \alpha_2\frac{V_{DS}}{\sqrt{\phi_{si} + V_{SB}}}\right)
\end{aligned} \tag{2.48}$$

So, after some simplification the general expression for threshold reduction ΔV_T due to charge sharing in short channel MOSFET, incorporating the effect of drain source voltage V_{DS}, can be obtained as follws :

$$\begin{aligned}
\Delta V_T &= \frac{\Delta Q_B}{C_o} \\
&= \frac{Q_B}{C_o} - \frac{Q_B}{C_o}
\end{aligned}$$

$$
\begin{aligned}
&= \frac{Q_B}{C_o}\left(1-\frac{Q'_B}{Q_B}\right) \\
&= \gamma\sqrt{\phi_{si}+V_{SB}}\left(\frac{\alpha_1}{L}\,\frac{w_S+w_D}{2}\right) \\
&= 2\alpha_1\frac{\epsilon_s}{\epsilon_{ox}}\frac{t_{ox}}{L}\left[(\phi_{si}+V_{SB})+\alpha_2 V_{DS}\right]
\end{aligned}
\tag{2.49}
$$

If the width of the channel Z in a short channel MOSFET is narrow then the depletion region (Fig. 2.6) on the sides of the channel is comparable to the total depletion region volume and cannot be neglected and this charge on the sides should be added to Q_B to find the effective charge $\hat{Q}_B$. Now the increase in threshold ΔV_{T1} due to narrow channel width is given by

$$
\Delta V_{T1} = \left(\frac{\hat{Q}_B}{Q_B} - 1\right)(\gamma\sqrt{\phi_{si}+V_{SB}}) \tag{2.50}
$$

If we assume the side parts of the depletion region is an area of quarter circle cross section then charge Q''_B inside the region is given

$$
\begin{aligned}
\frac{Q''_B}{Q_B} &= \frac{2\,(\pi/4)\,w^2 L}{Z\,L\,w} \\
&= \frac{w\,\pi}{2\,Z}
\end{aligned}
\tag{2.51}
$$

By introducing an empirical constant the total effective charge $\hat{Q}_B$ can be represented as

$$
\hat{Q}_B = Q_B\left(1+\alpha_3\frac{\pi}{2}\frac{w}{Z}\right) \tag{2.52}
$$

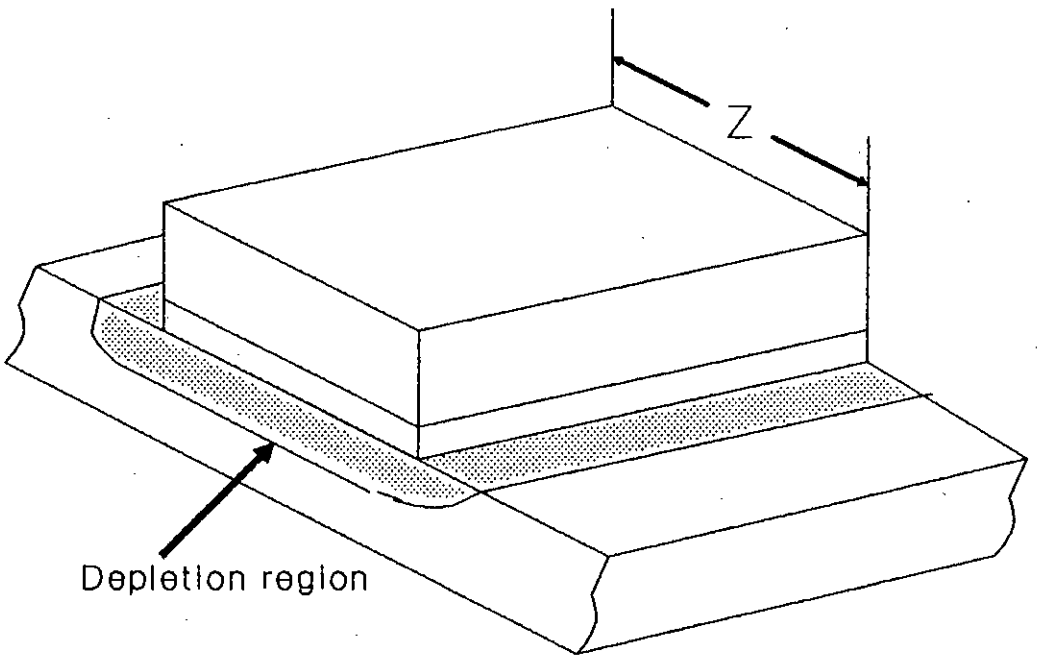


Fig. 2.6 Effect of fringing field in narrow channel MOSFET.

So the change in threshold voltage from (2.50) is given by

$$\Delta V_{T1} = \gamma\sqrt{\phi_{si} + V_{SB}} \left(\frac{\alpha_3\, \zeta\, \pi}{2Z} \sqrt{\phi_{si} + V_{SB}}\right) \tag{2.53}$$

Replacing the values of $w = \zeta\sqrt{\phi_{si} + V_{SB}}$, $C_o = \frac{\epsilon_{ox}}{t_{ox}}$ and $\gamma = \frac{(2\, q\, \epsilon_s\, N_A)^{1/2}}{C_o}$ in equation (2.53) the ultimate increase in thresold voltage is given by

$$\Delta V_{T1} = \alpha_3 \pi \frac{\epsilon_s}{\epsilon_{ox}} \frac{t_{ox}}{Z} (\phi_{si} + V_{SB}) \tag{2.54}$$

Combining the effect of L, V_{DS} and Z on the long channel threshold voltage V_T the expression of effective thresold voltage $\hat{V}_T$ for short channel MOSFET is

$$\hat{V}_T = V_T - \Delta V_T + \Delta V_{T1} \tag{2.55}$$

2.3.3 Channel length modulation

In a MOSFET at a certain drain source voltage V'_{DS} the channel is pinched off . At the pinchoff point zero inversion layer charge is situated at the drain end of the channel. If drain source voltage V_{DS} is increased beyond V'_{DS} then the depletion region at the drain substrate region starts to increase. This lateral extension of the depletion region into the channel beyond pinch off reduces the effective channel length. Since the depletion region is bias dependent it changes with drain source voltage and thus modulates the effective channel length. This change in channel

length due to bias voltage is negligible in long channel MOSFET, whereas, in short channel MOSFET it is comparable to the length of the MOSFET itself. So like the long channel MOSFET the current in short channel MOSFET does not saturate after pinchoff, rather it increases after saturation due to the fact that the channel current is inversely proportional to the channel length. So if $I'_{\mathbf{ch}}$ is the channel current at saturation voltage V'_{DS} then the channel current $I_{\mathbf{ch}}$ after saturation is

$$\begin{aligned} I_{\mathbf{ch}} &= I'_{\mathbf{ch}} \frac{1}{(1 - \Delta L/L)} \\ &\approx I'_{\mathbf{ch}} \left(1 + \frac{\Delta L}{L} \right) \end{aligned} \tag{2.56}$$

The value of ΔL can be found in the following way by solving an one dimensional Poisson's equation with appropriate boundary condition (Fig. 2.7) in the pinchoff region near drain end.

$$\begin{aligned} \frac{d\varepsilon_y}{dy} &= \frac{q}{\epsilon_s} N_A \\ \Rightarrow \varepsilon_y &= \varepsilon_0 + \frac{qN_A}{\epsilon_s} y \\ &= E_{SAT} + \frac{qN_A}{\epsilon_s} y \end{aligned} \tag{2.57}$$

$$\int_0^{\Delta L} d\psi_y = \int_0^{\Delta L} -\left(E_{SAT} + \frac{qN_A}{\epsilon_s} y \right) dy \tag{2.58}$$

So,

$$V_{DS} - V'_{DS} = -E_{SAT}\, \Delta L - \frac{1}{2}(\Delta L)^2 \frac{qN_A}{\epsilon_s} \tag{2.59}$$

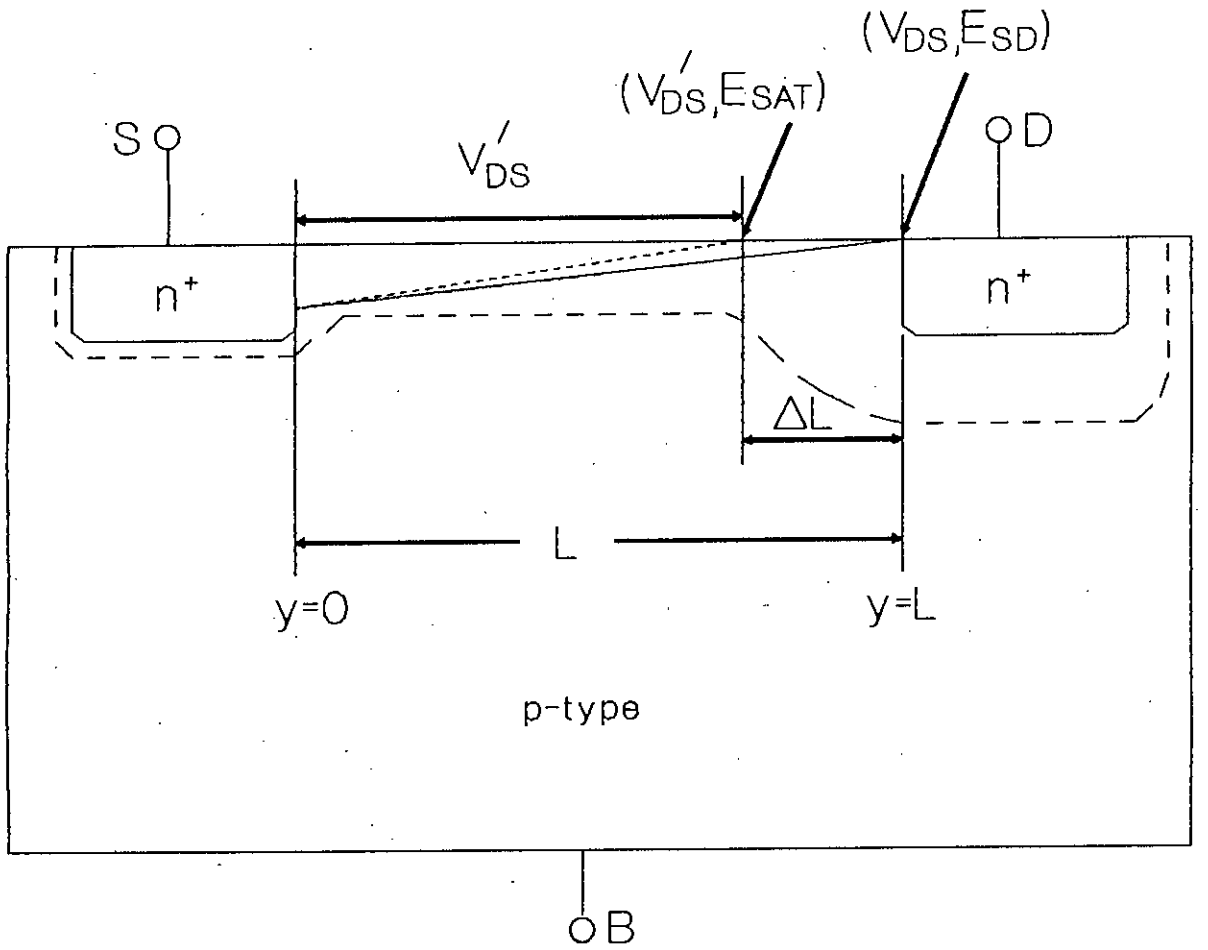


Fig. 2.7 Channel length modulation of a MOSFET.

Solving equation (2.59) for ΔL, ΔL can be written as

$$\Delta L = \sqrt{\frac{2\epsilon_s}{qN_A}}\left[\sqrt{\phi_D + (V_{DS} - V'_{DS})} - \sqrt{\phi_D}\right] \tag{2.60}$$

On the other hand,

$$\begin{aligned}\frac{\Delta L}{L} &= \sqrt{\frac{2\epsilon_s}{qN_A}}\,\frac{1}{L}\left[\sqrt{\phi_D}\left(1 + \frac{1}{2}\,\frac{V_{DS} - V'_{DS}}{\phi_D} + \cdots\right) - \sqrt{\phi_D}\right] \\ &= \sqrt{\frac{2\epsilon_s}{qN_A}}\,\frac{1}{L}\,\frac{V_{DS} - V'_{DS}}{2\sqrt{\phi_D}} \\ &= \frac{V_{DS} - V'_{DS}}{V_A}\end{aligned} \tag{2.61}$$

where,

$$\phi_D = \frac{\epsilon_s\, E_{SAT}^2}{2\, q\, N_A}$$

and

$$V_A = \frac{2\sqrt{\phi_D}\, L\sqrt{qN_A}}{\sqrt{2\epsilon_s}} = E_{SAT}\, L$$

From equations (2.56) and (2.61) the channel current I_{ch} after saturation is

$$I_{ch} = I'_{ch}\left(1 + \frac{V_{DS} - V'_{DS}}{V_A}\right) \tag{2.62}$$

Finally, by combining all the effects of short channel MOSFET that have been described in this section and recalling the channel current model of a long channel MOSFET from equations (2.26) and (2.27) ,the channel current model for short channel MOSFET can be represented as follws :

For a drain source voltge $V_{DS} \leq V'_{DS}$ the channel current $I_{\mathbf{ch}}$ is

$$I_{\mathbf{ch}} = \frac{\mu_0 C_o \frac{W}{L} \left[\{ V_{GS} - \hat{V}_T(V_{DS}) \} V_{DS} - .5(1+\delta) V_{DS}^2 \right]}{\left[1 + \theta \{ V_{GS} - \hat{V}_T(V_{DS}) \} + \theta_\beta V_{SB} \right] \left[1 + V_{DS}/(L\epsilon_c) \right]} \quad (2.63)$$

$$= \frac{\mu_{eff} C_o \frac{W}{L} \left[V_{G1} V_{DS} - .5(1+\delta) V_{DS}^2 \right]}{\left[1 + \frac{V_{DS}}{V_c} \right]} \quad (2.64)$$

where,

$$\mu_{eff} = \frac{\mu_0}{\left[1 + \theta \{ V_{GS} - \hat{V}_T(V_{DS}) \} + \theta_\beta V_{SB} \right]}$$

$$and \quad V_{G1} = V_{GS} - \hat{V}_T(V_{DS})$$

$$and \quad V_c = L\epsilon_c$$

For a drain source voltage $V_{DS} > V'_{DS}$ the channel current $I_{\mathbf{ch}}$ is

$$I_{\mathbf{ch}} = I'_{\mathbf{ch}} \left(1 + \frac{V_{DS} - V'_{DS}}{V_A} \right)$$

$$= \frac{\mu_0 C_o \frac{W}{L} \left[\{ V_{GS} - \hat{V}_T(V'_{DS}) \} V'_{DS} - .5(1+\delta) V'^2_{DS} \right]}{\left[1 + \theta \{ V_{GS} - \hat{V}_T(V'_{DS}) \} + \theta_\beta V_{SB} \right] \left[1 + \frac{V'_{DS}}{V_c} \right]} \left(1 + \frac{V_{DS} - V'_{DS}}{V_A} \right) \quad (2.65)$$

Now, we have to focus on the saturation voltage V'_{DS} which still remains to be found. Neglecting the dependence of $\hat{V}_T$ on V_{DS} and equating the expression $\frac{dI_{\mathbf{ch}}}{dV_{DS}}$ of equations (2.64) and (2.65) at $V_{DS} = V'_{DS}$, we get a transcendental equation after the follwing simplification. By solving the equation numerically we can get the satuartion voltage V'_{DS}.

$$\left(1+\frac{V'_{DS}}{V_c}\right)\left\{V_{G1}V'_{DS}-\frac{1}{2}(1+\delta)V'^2_{DS}\right\}$$

$$= V_A\left[(1+\frac{V'_{DS}}{V_c})\{V_{G1}-V'_{DS}(1+\delta)\}\right]$$

$$- \frac{1}{V_c}\left[\{V_{G1}V'_{DS}-\frac{1}{2}(1+\delta)V'^2_{DS}\}\right]$$

$$= V_A\left[V_{G1}-\frac{V'^2_{DS}}{2V_c}(1+\delta)-V'_{DS}(1+\delta)\right] \quad (2.66)$$

2.4 Substrate current model

In a short channel MOSFET the substrate current is composed of holes generated by impact ionization in the drain region due to high lateral electric field. This current is detectable when the drain source voltage V_{DS} is one or two volts above V'_{DS}. The substrate current is a function of multiplication factor M as shown in equation (2.6). But the general expression of multiplication factor M is given by [25]

$$1-\frac{1}{M} = \int_{x_n}^{x_p}\alpha_n\, exp\left[-\int_x^{x_p}(\alpha_n-\alpha_p)\,dx'\right]\,dx$$

$$= \int_0^{\Delta L}\alpha_{eff}\,dx \quad (2.67)$$

But

$$\alpha_{eff} = A_i\, e^{-\frac{B_i}{E}} \quad (2.68)$$

where, E is the lateral (y direction) electric field (fig 2.2) α_n, α_p , are the ionization rates for electron and hole respectively and A_i and B_i are the ionization coefficients.

$$\int_0^{\Delta L} \alpha_{eff}\, dy = \int_0^{\Delta L} A_i\, e^{-\frac{B_i}{E}}\, \frac{dy}{dE}\, dE \tag{2.69}$$

$$\approx \left|\frac{dy}{dE}\right|_{E_{SD}} A_i \int_{E_{SAT}}^{E_{SD}} e^{-\frac{B_i}{E}}\, dE \tag{2.70}$$

$$\approx A_i \left|\frac{dy}{dE}\right|_{E_{SD}} \left[E^2 + e^{-\frac{B_i}{E}} \left(1 - \frac{2}{B_i}E + 6\frac{E^2}{B_i^2}\right)\right]_{E_{SAT}}^{E_{SD}}$$

$$\approx \frac{A_i}{B_i} E_{SD}^2 \left|\frac{dy}{dE}\right|_{E_{SD}} \left(1 - 2\frac{E_{SD}}{B_i} + 6\frac{E_{SD}^2}{B_i^2}\right) e^{-\frac{B_i}{E_{SD}}}$$

$$- \frac{A_i}{B_i} E_{SAT}^2 \left|\frac{dy}{dE}\right|_{E_{SD}} (1 - 2\frac{E_{SAT}}{B_i} + 6\frac{E_{SAT}^2}{B_i^2})\, e^{-\frac{B_i}{E_{SAT}}}$$

$$\approx (C_1 - C_2) \tag{2.71}$$

Since, the lateral electric field E in the channel increases sharply toward the drain and the substrate current is very strongly dependent on the field, equation (2.69) reduces approximately to (2.70).

From equations (2.67) and (2.71) we get

$$1 - \frac{1}{M} = C_1 - C_2 \tag{2.72}$$

where,

$$C_1 = \frac{A_i}{B_i} E_{SD}^2 \left|\frac{dy}{dE}\right|_{E_{SD}} \left(1 - 2\frac{E_{SD}}{B_i} + 6\frac{E_{SD}^2}{B_i^2}\, e^{-\frac{B_i}{E_{SD}}}\right) \tag{2.73}$$

and

$$C_2 = \frac{A_i}{B_i} E_{SAT}^2 \left|\frac{dy}{dE}\right|_{E_{SD}} \left(1 - 2\frac{E_{SAT}}{B_i} + 6\frac{E_{SAT^2}}{B_i^2}\, e^{-\frac{B_i}{E_{SAT}}}\right) \tag{2.74}$$

The substrate current can be represented From equation (2.6)

$$I_{sub} = (C_1 - C_2)\, (I_{sub} + I_s) - I_b \tag{2.75}$$

The lateral electric field E can be related to drain source voltage [21] as,

$$E = \sqrt{A^2\,(V - V'_{DS})^2 + E^2_{SAT}} \tag{2.76}$$

where,

$$A = \sqrt{\frac{\epsilon_{ox}/\epsilon_{si}}{t_{ox}\,\{(d_j + .01(V - V'_{DS})(d_1 - d_j)\}}}$$

and

$$d_1 = \sqrt{(\frac{2\,\epsilon_s}{q\,N_{sub}})\,(V'_{DS} + 2\phi_f)}$$

$$\frac{dE}{dy} = \frac{dE}{dV}\,\frac{dV}{dy} = E\,\frac{dE}{dV} \tag{2.77}$$

From equations (2.72), (2.73), (2.74) and (2.76) we find that the multiplication factor M is a strong function of lateral electric field near the drain junction and thus is a function of drain source voltage V_{DS}, oxide thickness t_{ox}, junction depth d_j and substrate doping N_{sub}. The substrate current can be found from equation (2.75) by knowing the parameters C_1 and C_2 . The essential variables required to evaluate these parameters are the electric field E_{SD} and the gradient of electric field $\left|\frac{dE}{dy}\right|_{E_{SD}}$ at the drain end of the channel which can be found in the follwing way.

$$\begin{aligned}
\frac{dE}{dV} &= \frac{d}{dV}\{\, A^2\,(V - V'_{DS})^2 \,+ E^2_{SAT}\}^{1/2} \\
&= \frac{(V - V'_{DS})}{E}\, A^2 \left[\, 1 + (V - V'_{DS})\, \frac{1}{A}\, \frac{dA}{dV}\right] \\
E\,\frac{dE}{dV} &= (V - V'_{DS})\, A^2 \left[\, 1 + \frac{1}{A}\frac{dA}{dV}\ (V - V'_{DS})\right] \qquad (2.78)
\end{aligned}$$

Putting $x_1 = \frac{\epsilon_{ox}}{\epsilon_s}$ *and* $y_1 = t_{ox}\{\, d_j + .01(V_{DS} - V'_{DS})(d_1 - d_j)\}$

$$\begin{aligned}
\frac{dA}{dV} &= -\frac{x_1^{1/2}}{y}\, \frac{d}{dV}(y_1^{1/2}) \\
&= -\frac{(x_1^{1/2}/y_1^{1/2})}{2\, y_1}\frac{d}{dV}\left[\, t_{ox}\, \{d_j + .01(V - V'_{DS})(d_1 - d_j)\}\right] \\
&= -\frac{A}{2y_1}\, t_{ox}\, \{.01\ (d_1 - d_j)\} \\
\Rightarrow \frac{1}{A}\,\frac{dA}{dV} &= \frac{1}{2y_1}\, t_{ox}\, \{\ .01(\ d_1 - d_j)\} \\
&= -bA^2 \qquad (2.79)
\end{aligned}$$

where,

$$b = \frac{1}{2}\ 0.01\ (d_1 - d_j)\ \epsilon_s\ \frac{t_{ox}}{\epsilon_{ox}}$$

From equation (2.76), (2.77) and (2.79) we get

$$\frac{dE}{dy} = A^2(V - V'_{DS})\left[\ 1\ - bA^2(V - V'_{DS})\right] \qquad (2.80)$$

The lateral electric field E_{SD} and the gradient $\left|\frac{dE}{dy}\right|_{E_{SD}}$ at the drain end can be found by replacing V in equation (2.76) and (2.80) by V_{DS}.

2.5 Excess channel current model

Due to the enhanced body effect EBE (Fig. 2.8) the enhancement of the inversion is achieved through a excess channel current $\Delta I_{\mathbf{ch}}$ injection in addition to the conventional channel current $I_{\mathbf{ch}}$. This excess channel current corresponds to an equivalent threshold lowering of $V_{\mathbf{th}}$ which is equal to:

$$-\Delta V_{\mathbf{th}} = \frac{-\Delta Q_{BS}}{C_o} = \frac{q}{C_o}\int_w^{w_o} N^*(x)\,dx \tag{2.81}$$

and consequently the excess channel current $\Delta I_{\mathbf{ch}}$ is given by

$$\Delta I_{\mathbf{ch}} \equiv I_{\mathbf{ch}} \mid_{\hat{v}_T+\Delta V_{\mathbf{th}}} - I_{\mathbf{ch}} \mid_{\hat{v}_T} \tag{2.82}$$

where, the symbol $N^*(x)$ represents the transformed doping profile which replaces the real doping profile $N(x)$ in short channel case according to VDT technique[16]. The VDT technique allows the two dimensional Poisson's equation, inherent in short channel MOSFET to be reduced to one dimensional form. According to [16] $N^*(x)$ is given by

For $x \leq \lambda$

$$N^*(x) = N_s^* \tag{2.83}$$

$$= N_s - \frac{2\epsilon_s}{qL_{ef}^2}\left[V_{DS} + 2\left(V_{\mathbf{bi}} - 2\phi_f\right) + 2\sqrt{(V_{\mathbf{bi}} - 2\phi_f)(V_{DS} + V_{\mathbf{bi}} - 2\phi_f)}\right] \tag{2.84}$$

$$= N_s - V \tag{2.85}$$

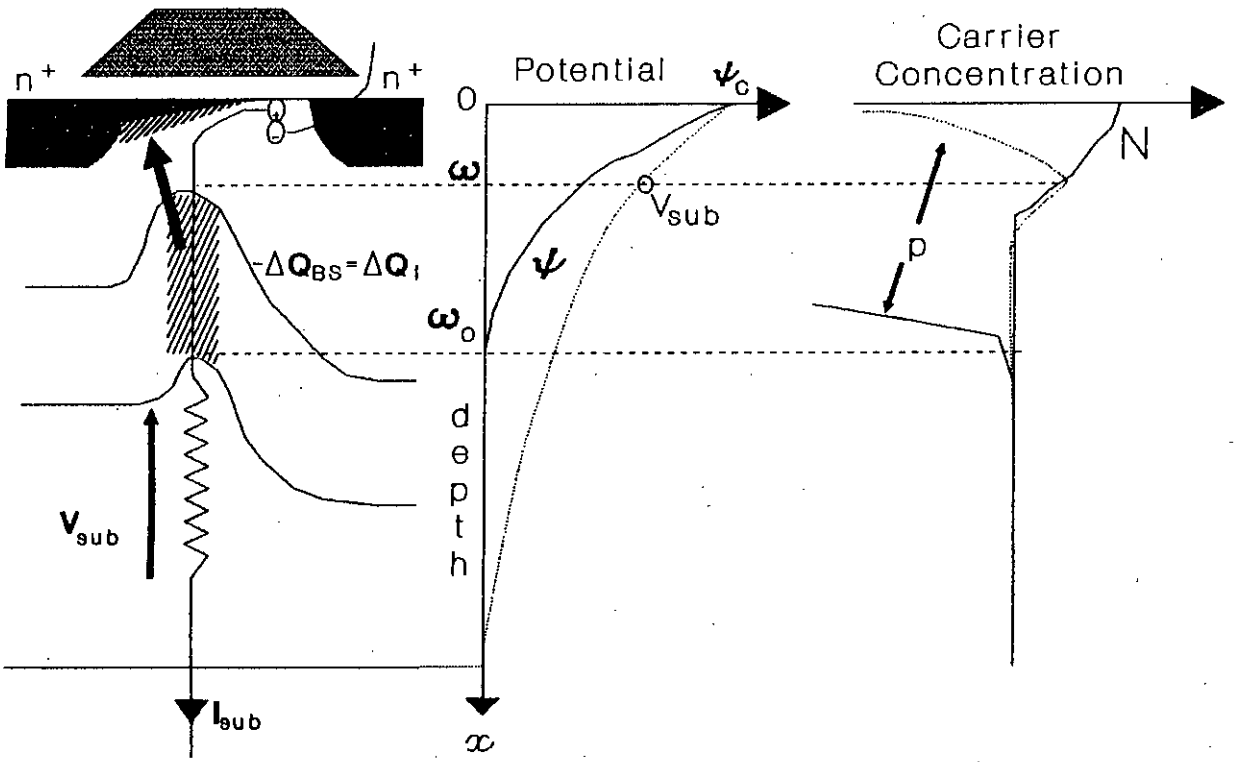


Fig.2.8. Schematic illustration of the EBE phase with corresponding potential and carrier distribution.

For $x > \lambda$

$$N^*(x) = N_B \tag{2.86}$$

Here, N_s, N_B and λ are the parameters of the box approximation of the doping profile and stand, respectively for the surface and bulk box doping concentrations, and the range of the surface enhanced doping, $V_{\rm bi}$ is the built in potential of the source bulk junction. For most practical case the depletion width w_o at a substrate current ($I_{\rm sub} = 0$) is less or equal than the λ i.e $w_o \leq \lambda$

where,

$$w_o = w(I_{\rm sub} = 0) = \sqrt{\frac{2\epsilon_s \psi_c}{qN_s^*}} \tag{2.87}$$

By using the VDT technique, $\Delta V_{\rm th}$ can be found by solving a one dimensional Poisson's equation with appropriate boundry condition of potential ψ_w and field E_w at the depletion edge boundry which is shown below. The threshold lowering $\Delta V_{\rm th}$ due to substrate current is related to depletion width w at a particular substrate current and w_o by the following expression.

$$\Delta V_{\rm th} = -\frac{q}{C_o} N_s^*(w_o - w) \qquad for \quad I_{\rm sub} \leq I_{\rm subt} \tag{2.88}$$

where, $I_{\rm subt}$ corresponds to the substrate current which causes the depletion layer to dissappear completely ($w \rightarrow 0$).

The surface potential at the silicon surface $x = 0$ is given by

$$\psi_c \equiv 2\phi_f + V_{SB} = \psi(0) \tag{2.89}$$

$$\frac{d\varepsilon_x}{dx} = -\frac{q\ N_a^*}{\epsilon_s} \tag{2.90}$$

Upon integration

$$\varepsilon_x = \varepsilon_o - \frac{qN_a^*}{\epsilon_s}\ x \tag{2.91}$$

By putting boundary conditions

$$\varepsilon_o = E_w + \frac{qN_a^*}{\epsilon_s}\ w \tag{2.92}$$

Using equation (2.91) and (2.92) we get

$$\psi_o = \psi_c = \psi_w + wE_w + \frac{1}{2}\frac{qN_a^*}{\epsilon_s}w^2 \tag{2.93}$$

The boundary conditions are as follows :

$$\psi_w = R_{sub}\ I_{sub} \tag{2.94}$$

$$E_w = \frac{r}{l}\ I_{sub} \qquad [from\ equation\ (2.8)] \tag{2.95}$$

where,

$$r = (q\mu_p NZ)^{-1}$$

R_{sub} is the substrate resistance which is a function of the substrate current I_{sub} when $I_{sub} > I_{subt}$ and is equal to a constant value R_{subt} when $I_{sub} \leq I_{subt}$.

Rearranginging the equation (2.93)

$$w^2 + w\left(\frac{2\epsilon_s E_w}{qN_s^*}\right) + \frac{2\epsilon_s}{qN_s^*}(\psi_w - \psi_c) = 0 \tag{2.96}$$

Solving the equation we get the depletion layer width w in terms of w_o

$$\begin{aligned} w &= -\frac{1}{2}\frac{2E_w\epsilon_s}{qN_s^*} + \frac{1}{2}\sqrt{\left(\frac{2E_w\epsilon_s}{qN_s^*}\right)^2 - 4\frac{2\epsilon_s}{qN_s^*}(\psi_w - \psi_c)} \\ &= -\frac{\epsilon_s r\, I_{sub}}{q\, l\, N_s^*} + \sqrt{\left(\frac{\epsilon_s\, r\, I_{sub}}{qlN_s^*}\right)^2 + \left(\frac{2\epsilon_s\psi_c}{qN_s^*}\right)^2 \psi_c\left(1 - \frac{\psi_w}{\psi_c}\right)} \\ &= \sqrt{\left(\frac{\epsilon_s\, r\, I_{sub}}{qlN_s^*}\right)^2 + w_o^2\left(1 - \frac{R_{sub}\, I_{sub}}{\psi_c}\right)} - \frac{\epsilon_s\, r\, I_{sub}}{qlN_s^*} \end{aligned} \tag{2.97}$$

where,

$$w_o = w(I_{sub} = 0) = \sqrt{\frac{2\epsilon_s\psi_c}{qN_s^*}} \tag{2.98}$$

From equation (2.88) and (2.97) we find that depletion width w decreases and the $|\Delta V_{th}|$ value increases with the increase of substrate current. The value of $|\Delta V_{th}|$ will reach its maximum value when the depletion edge reaches the boundary of inversion layer w_i or in other words the Si surface since ($w_i \cong 0$). Under this condition the depletion width ($w = 0$) and the corresponding substrate current is given by

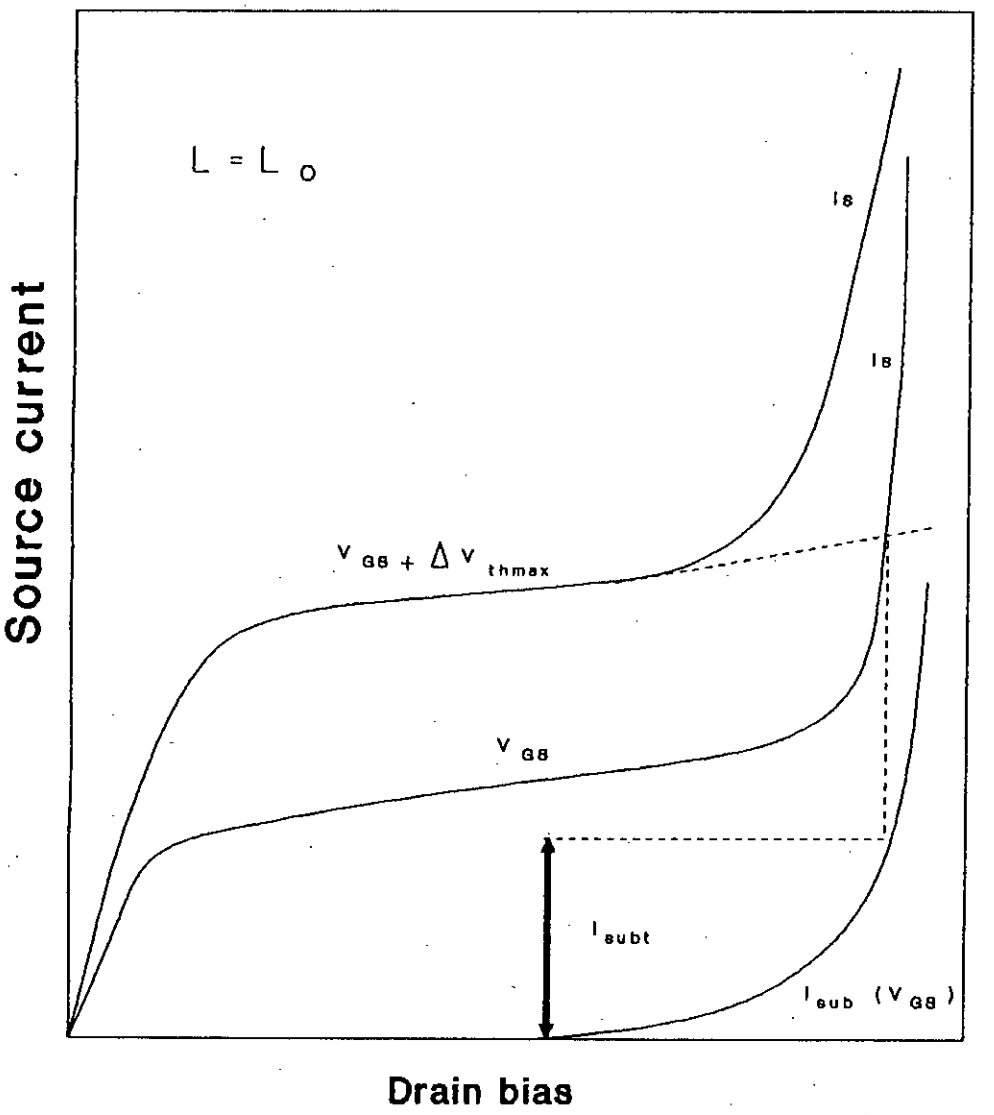


Fig. 2.9. Illustration of the method of extracting the I_{subt} Current.

$$I_{\mathbf{subt}} = \frac{\psi_c}{R_{\mathbf{subt}}} \tag{2.99}$$

where, $R_{\mathbf{subt}}$ is the substrate resistance which corresponds ($w \rightarrow 0$). During the EBE phase the substrate resistance $R_{\mathbf{sub}}$ equals the $R_{\mathbf{subt}}$, the resistance of the bulk, but in the bipolar phase it varies with d, thickness of equipotential region (EPR). So in the EBE phase the expression of substrate resistance can be represented by the following empirical relation [Appendix A]

$$R_{\mathbf{sub}} \cong R_{\mathbf{subt}} = R_0 + k_L(L_0/L - 1) \tag{2.100}$$

2.5.1 Transition phase

The operational phase when the depletion layer vanishes at a substrate current $I_{\mathbf{sub}} = I_{\mathbf{subt}}$ and the threshold voltage $\hat{V}_T$ reaches its minimum value is the transition phase (Fig. 2.10). This corresponds to the maximal threshold voltage reduction $|\triangle V_{\mathbf{thmax}}|$ where

$$\left|\triangle V_{\mathbf{thmax}}\right| = -\frac{\triangle Q_{BSmax}}{C_o}$$

and

$$\triangle Q_{BSmax} = -q \int_o^{w_o} N^*(x)dx$$

In the transition phase the normal electric field E vanishes at the inversion layer boundary w_i and the potential at this boundry become ψ_c since the electric field

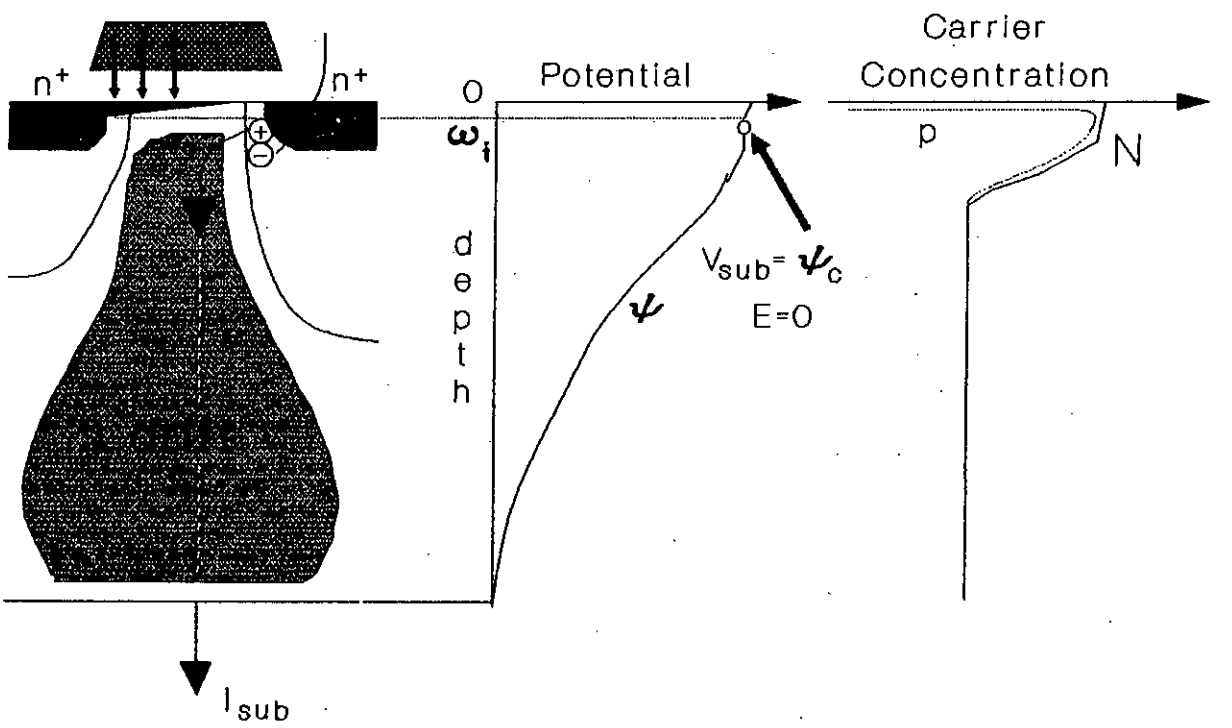


Fig. 2.10. Schematic illustration of the transition phase with corresponding potential and carrier distribution.

lines originating from the gate terminate within the inversion layer and there is no free charge available which can change the boundary condition. In the transition phase the bulk below the inversion region also becomes quasineutral, i.e $p \cong N$ and is denoted as QNR (Quasi neutral region).

2.6 Emitter current model

After the transition phase the MOSFET enters in its bipolar phase (Fig. 2.11) . When the substrate current I_{sub} exceeds I_{subt} , the current at transition phase, the excess holes due to avalanche multiplication is neutralised by injection of electrons from source junction in order to preserve the charge neutrality condition. The region where the bipolar action takes place is EPR (Equipotential region) because of the constant potential. This region of EPR acts as the base of the npn transistor formed by the source, substrate and drain of the MOSFET where source acts as the emitter and drain as the collector. EPR is a perfectly neutral $(p - n - N = 0)$ and the normal field E at its upper boundary vanishes, the potential ψ_c is reproduced throughout the EPR. But the potential at the upper boundary of EPR near the source junction is $\psi = \psi_c + \delta\psi \approx \psi_c$ and $\delta\psi$ increases with increase of EPR thickness d and the electric field at this boundary is slightly greater than 0. So the potential at the upper boundary near the source junction rises very slowly with increasing carrier concentration.

As a result the substrate current in the EPR is due to diffusion mechanism, whereas, in the bulk below the EPR it is due to drift mechanism. In the bipolar phase, concentration gradient occurs in both horizontal and vertical direction. The concentration gradient $\frac{\Delta p}{d}$ is responsible for the substrate current and $\frac{\Delta n}{l}$ is responsible of the emitter current due to electrons. The components of emitter current are

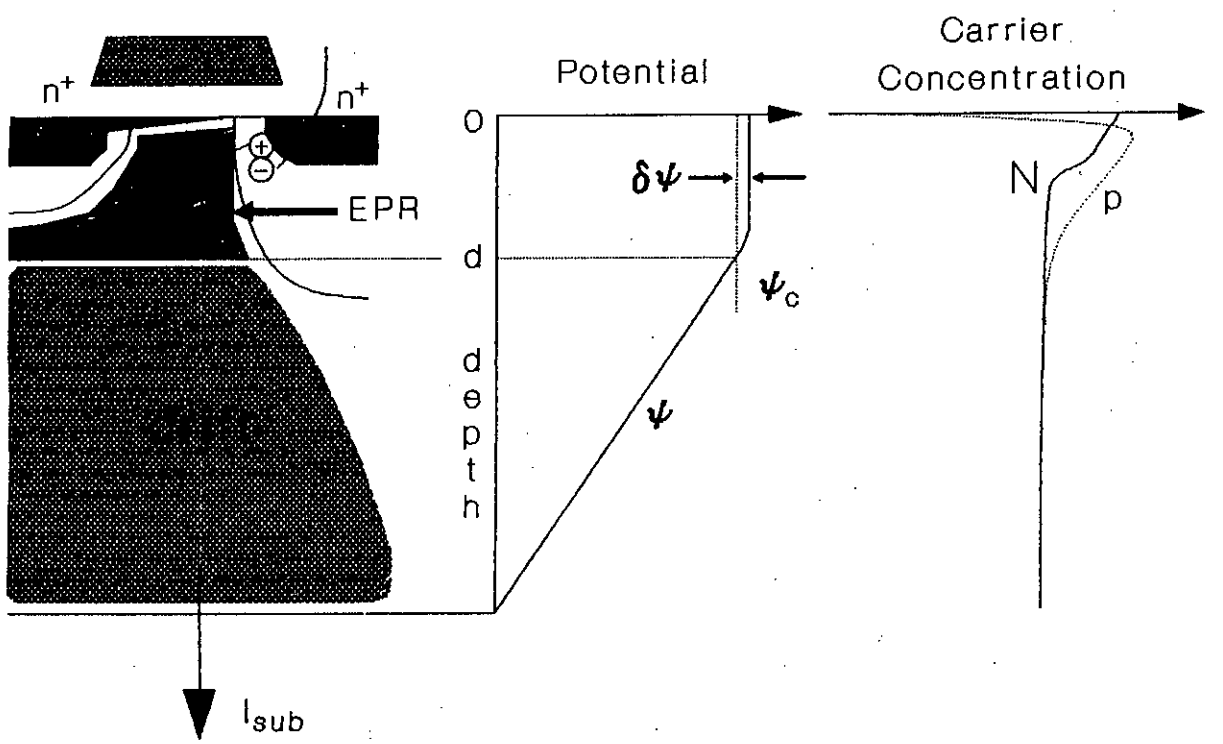


Fig. 2.11 Schematic illustration of the bipolar phase with corresponding pontential and carrier distribution.

I_{nSB} and I_{pBS} of which I_{nSB} is due to excess electrons injected into EPR (base) from source and I_{pBS} is the excess holes injected from the EPR into the source.

$$I_{sub} \cong q\mu_p U_T \frac{\Delta p}{d} lZ \tag{2.101}$$

The neutrality condition implies

$$\Delta n = \Delta p = \frac{d}{q\mu_p U_T lZ} I_{sub} \tag{2.102}$$

Considering a typical n^+p junction of source and EPR, different current components can be expressed as follows

$$\begin{aligned} I_{nSB} &= q\mu_n U_T \frac{\Delta n}{l} Zd \\ &= \frac{\mu_n}{\mu_p} \left(\frac{d}{l}\right)^2 I_{sub} \end{aligned} \tag{2.103}$$

and

$$\begin{aligned} I_{pBS} &= q\mu_p U_T \frac{N_s}{N_{SD}} \frac{\Delta n}{L_p} Zd \\ &= \frac{N_s}{N_{SD}} \frac{d^2}{l\, L_p} I_{sub} \end{aligned} \tag{2.104}$$

Not all of the electrons carried by the I_{nSB} arrive at the drain terminal. Some of them will recombine with holes and thereby will constitute recombination current I_{rec}

$$
\begin{aligned}
I_{\mathbf{rec}} &= \frac{\triangle Q_n}{\tau_n} \\
&= \frac{1}{2}\frac{\mu_n}{\mu_p}\left(\frac{d}{L_n}\right)^2 I_{\mathbf{sub}}
\end{aligned}
\tag{2.105}
$$

where, $\triangle Q_n = \frac{q\triangle n d l Z}{2}$ and $L_n = (\tau_n \mu_p U_T)^{1/2}$

The emitter current $I_{\mathbf{e}}$ and the base current $I_{\mathbf{b}}$ after some simplification are given by

$$
\begin{aligned}
I_{\mathbf{e}} &= I_{\mathbf{nSB}} + I_{\mathbf{pBS}} \\
&= q\mu_n U_T \left(\frac{\triangle n}{l} + \frac{\mu_p N_s \triangle n}{\mu_n N_{SD} L_p}\right) Zd \\
&= \left(\frac{\mu_n}{\mu_p} + \frac{lN_s}{L_p N_{SD}}\right)\left(\frac{d}{l}\right)^2 I_{\mathbf{sub}}
\end{aligned}
\tag{2.106}
$$

$$
\begin{aligned}
I_{\mathbf{b}} &= I_{pBS} + I_{rec} \\
&= I_{\mathbf{m}} - I_{\mathbf{sub}} \\
&= \left(\frac{N_s L_n^2}{N_{SD} l L_p} + \frac{1}{2}\frac{\mu_n}{\mu_p}\right)\left(\frac{d}{L_n}\right)^2
\end{aligned}
\tag{2.107}
$$

Comparing with the base of the conventional bipolar transistor the EPR (base of the parasitic bipolar transistor) has a structure of variable geometry. EPR actually emerges at the silicon surface and expands towards the bulk as well as below source and drain domains to absorb as much as of the bulk spreading resistance to maintain the constant potential $V_{\mathbf{sub}} = R_{\mathbf{sub}} I_{\mathbf{sub}} = \psi_c = \phi_{si} + V_{SB}$ at its bottom edge (Fig.

2.12). The self adjusting mechanism leads to the decrease in R_{sub} reciprocal to I_{sub} and takes place through a change in geometry of the EPR. After the transition phase the biasing of the base emitter junction V_{be} increases with $\delta\psi$ which increases with the increasing size (d) of EPR and is given by

$$V_{be} = V_{sub} + \delta\psi - V_{SB} = 2\phi_f + \delta\psi \tag{2.108}$$

At the transition point $\delta\psi = 0$, $V_{sub} = \psi_c$, $V_{be} = 2\phi_f$ and before the transition phase $\delta\psi = 0$, $V_{sub} = R_{subt} I_{sub}$, $V_{be} = V_{sub} - V_{SB}$.

An explicit expression for V_{be} can be obtained by equating the mean excess concentration Δn of electrons as given by the diode theory and by equation (2.102).

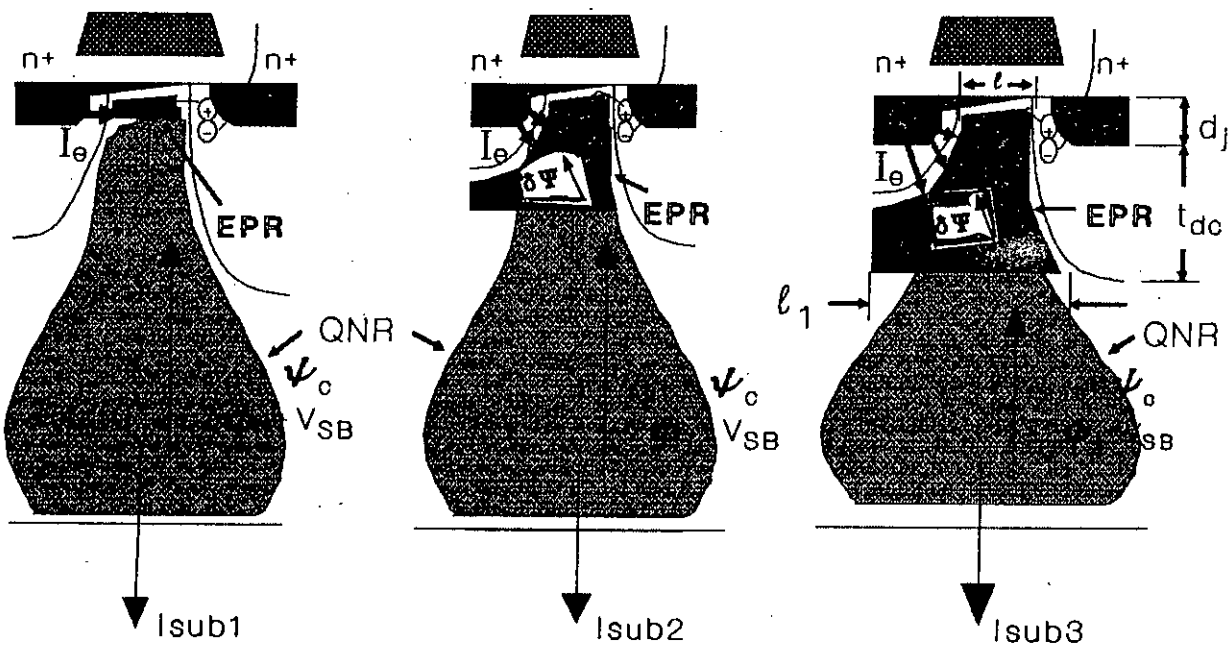
$$\Delta n = \frac{n_i^2}{N}\left[exp(\frac{V_{be}}{U_T}) - 1\right] = \frac{d}{q\mu_p U_T l Z}\, I_{sub} \tag{2.109}$$

Or

$$V_{be} = U_T\, ln\left(1 + \frac{dN I_{sub}}{q\mu_p U_T n_i^2 l Z}\right) \tag{2.110}$$

In the transition phase when $I_{sub} \rightarrow I_{subt}$ and $d \rightarrow d_t$, the voltage V_{be} is given by

$$V_{be} = 2\phi_f$$



Isub3 > Isub2 > Isub1
Rsub3 < Rsub2 < Rsub1

Fig. 2.12. Schematic diagram of the evolution of EPR.

(a) EPR emerging at the silicon surface.

(b) EPR expands towards the bulk.

(c) EPR expands below the source and drain domain.

$$= U_T \, ln(\frac{N_B N}{n_i^2}) \cong 0.7 \; V \qquad (2.111)$$

We Summarize the variation of V_{be} as follows

$$V_{be} = R_{subt} I_{sub} - V_{SB} \qquad for \;\; I_{sub} \leq I_{subt} \qquad (2.112)$$

$$= U_T \, ln\left(1 + \frac{d \, N I_{sub}}{q \mu_p U_T n_i^2 l Z}\right) \qquad for \;\; I_{sub} > I_{subt} \qquad (2.113)$$

From equation (2.112) and (2.113) we find that V_{be} increases linearly in the EBE phase until it reaches the value ϕ_{si} at the transition phase beyond which the increase slows down but does not vanish completely rather it increases logarithmically as shown by equation (2.113).

In the last part of the section we have to focus on d (EPR thickness) to find its variation as a function of substrate current. From the well known relation of resistance $R = \rho \frac{T}{A}$ we can find a linear relation between R_{sub} and d. Here the substrate resistance is $R_{sub} = \frac{\rho(T-d)}{A}$ which decreases with the increase of d. Choosing two different values of d such as d_t and $d_j + t_{dc}$ and knowing the corresponding substrate resistance R_{subt} and R_{subc} at these two depths of EPR we can develop the relation (2.114) between R_{sub} and I_{sub} which is valid for $I_{sub} > I_{subt}$

$$d = d_t + (d_j + t_{dc} - d_t) \frac{R_{subt} - R_{sub}}{R_{subt} - R_{subc}}$$

$$= d_t + (d_j + t_{dc} - d_t) \frac{R_{subt} - \frac{V_t}{I_{sub}}}{R_{subt} - R_{subc}} \qquad (2.114)$$

The value of d_t, the EPR thickness at the transition phase, can be determined from the following equations.

$$\frac{\psi_c}{R_{\text{subt}}} = I_{\text{subt}} = q\mu_p U_T \frac{\Delta p_t}{d_t} Zl \tag{2.115}$$

Substituting the value of V_{be} at the transition phase with $2\phi_f$ from equation (2.111) into (2.109) we get Δn_t

But

$$\Delta p_t = \Delta n_t = N_B - \frac{n_i^2}{N} \tag{2.116}$$

The value of d_t is given by

$$d_t = q\mu_p U_T \left(N_B - \frac{n_i^2}{N} \right) \frac{R_{\text{subt}}}{\psi_c} Zl \tag{2.117}$$

Finally, we have to consider the situation when EPR expands towards the bulk as well as below the source and drain domains i.e $d > d_j$. The analysis upto this point is valid for $d \leq d_j$. But In the case of $d > d_j$ the geometry of EPR become very complex and we have to consider the composition of 2 bipolar transistor connected in parallel. The width and the cross-sectional area of the base of the upper transistor are l and Zd_j and those of the lower one are l_1 and $Z(d - d_j)$ where $l_1 = l + l_m$. Parameter l_m accounts for the encroachment of the EPR underneath the source domain. The variation of l_1 with substrate current I_{snb} can be made by developing an empirical expression of l_m [Appendix B] to fit the curve in the upper region of the drain characteristics. Upon this basis appropriate current expression for I_{b} and

I_e can be derived for the two transistors in an analogical manner as it has been done in (2.107) and (2.106) i.e.

$$I_e = I_{e1} + I_{e2} \tag{2.118}$$

$$I_b = I_{b1} + I_{b2} \tag{2.119}$$

where,

$$I_{e1} = \left(\frac{\mu_n}{\mu_p} + \frac{l\ N_s}{L_p\ N_{SD}}\right)\left(\frac{d_j}{l}\right)^2 I_{sub} \tag{2.120}$$

$$I_{e2} = \left(\frac{\mu_n}{\mu_p} + \frac{l_1\ N_s}{L_p\ N_{SD}}\right)\left(\frac{d - d_j}{l_1}\right)^2 I_{sub} \tag{2.121}$$

and

$$I_{b1} = \left(\frac{1}{2}\frac{\mu_n}{\mu_p} + \frac{N_s\ L_n^2}{l\ L_p\ N_{SD}}\right)\left(\frac{d_j}{L_n}\right)^2 I_{sub} \tag{2.122}$$

$$I_{b2} = \left(\frac{1}{2}\frac{\mu_n}{\mu_p} + \frac{N_s\ L_n^2}{l_1\ L_p\ N_{SD}}\right)\left(\frac{d - d_j}{L_n}\right)^2 I_{sub} \tag{2.123}$$

2.7 Conclusions

In this chapter, a detailed analysis of the short channel MOSFET in the avalanche induced breakdown region is presented. The physics of the enhanced body effect and the bipolar transitor action have been distinguished in the analysis. The difference between the ordinary body effect and the enhanced body effect has been considered carefully. The conventional channel current is derived by considering various short channel effects. A brief description of various short channel effects has also been

presented in this chapter. The multiplication model used to find the substrate current has taken into account the effect of junction depth, doping concentration, drain source voltage, and oxide thickness on the lateral electric field near the drain region. The excess channel current model is developed by using VDT technique which replaces the two dimensional Poisson's equation, inherent in short channel MOSFET by a one dimensional equation .

CHAPTER 3

MODEL IMPLEMENTATION AND RESULTS

3.1 Introduction

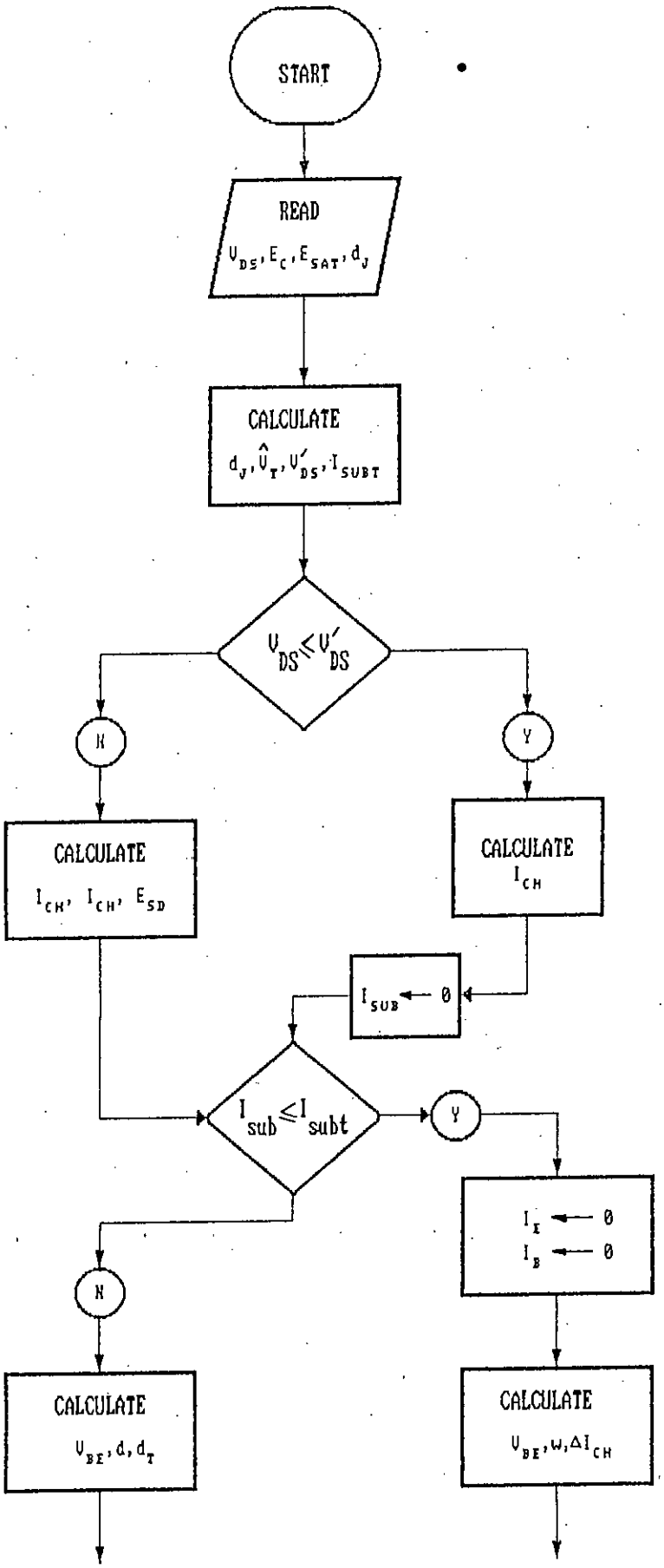
The drain characteristics of a short channel MOSFET opertating in the avalanche multiplication regime depends strongly on the flow of substrate current. Actually the drain current in this region consists of four different current components i) I_{ch}, ii) I_{snb}, iii) ΔI_{ch}, iv) I_e . But excess channel current ΔI_{ch} and emitter current I_e are function of substrate current I_{snb} . The substrate current on the other hand depends on the hole generation in the depletion region near the drain end of the MOSFET. The degree of multiplication determines the hole current and the multiplication factor M strongly depends on the lateral electric field E_{SD} at the drain end of the MOSFET. The electric field E_{SD} increases with the increase of drain source voltage V_{DS} . By using a multiplication model as presented in section 2.4 the substrate current can be obtained for a particular V_{DS} . Knowing the substrate current I_{snb} the excess channel current ΔI_{ch} and the emitter current I_e can be calculated at the corresponding voltage with the help relevant equations derived in the second chapter.

A computer program is developed to study the different characteristics of the MOSFET. The equations which are used for obtaining the characteristics are based on the analytical model developed in chapter 2. In the following section of this chapter we have developed an algorithm of the computer program for model simulation which is represented briefly and sequentially.

3.2 Analysis of the Computational method used

The drain current $I_{\mathbf{d}}$ of the short channel MOSFET is the sum of $I_{\mathbf{ch}}$, $I_{\mathbf{sub}}$, $\Delta I_{\mathbf{ch}}$, $I_{\mathbf{e}}$. The relevant equations required to get these current components are derived in chapter 2. The flowchart of the computational method used to obtain the $I_{\mathbf{d}}$ versus V_{DS} characteristic is shown in (Fig. 3.1). The steps of the total algorithm are shown below :

1. Start the program.
2. Read the necessary parameters like drain source voltage V_{DS}, critical field E_c, field at saturation E_{SAT}, junction depth d_j, oxide thickness t_{ox} and doping concentration of substrate N .
3. Calculate the short channel threshold $\hat{V}_T$ and the saturation voltage V'_{DS}, $R_{\mathbf{subt}}$, $I_{\mathbf{subt}}$.
4. Compare V_{DS} with V'_{DS}. If V_{DS} is less than the saturation voltage V'_{DS} then calculate channel current $I_{\mathbf{ch}}$ and assign the value of substrate current $I_{\mathbf{sub}}$ equal to zero.
5. Calculate the current $I_{\mathbf{ch}}$ at saturation voltage V'_{DS} and then channel current $I_{\mathbf{ch}}$. Also calculate the lateral electric field E_{SD} at drain end and then find


START
READ
$V_{DS}, E_C, E_{SAT}, d_J$
CALCULATE
$d_J, \hat{V}_T, V'_{DS}, I_{SUBT}$
$V_{DS} \leq V'_{DS}$
N
Y
CALCULATE
I_{CH}, I_{CH}, E_{SD}
CALCULATE
I_{CH}
$I_{SUB} \leftarrow 0$
$I_{sub} \leq I_{subt}$
Y
N
$I_E \leftarrow 0$
$I_B \leftarrow 0$
CALCULATE
V_{BE}, d, d_T
CALCULATE
$V_{BE}, w, \Delta I_{CH}$

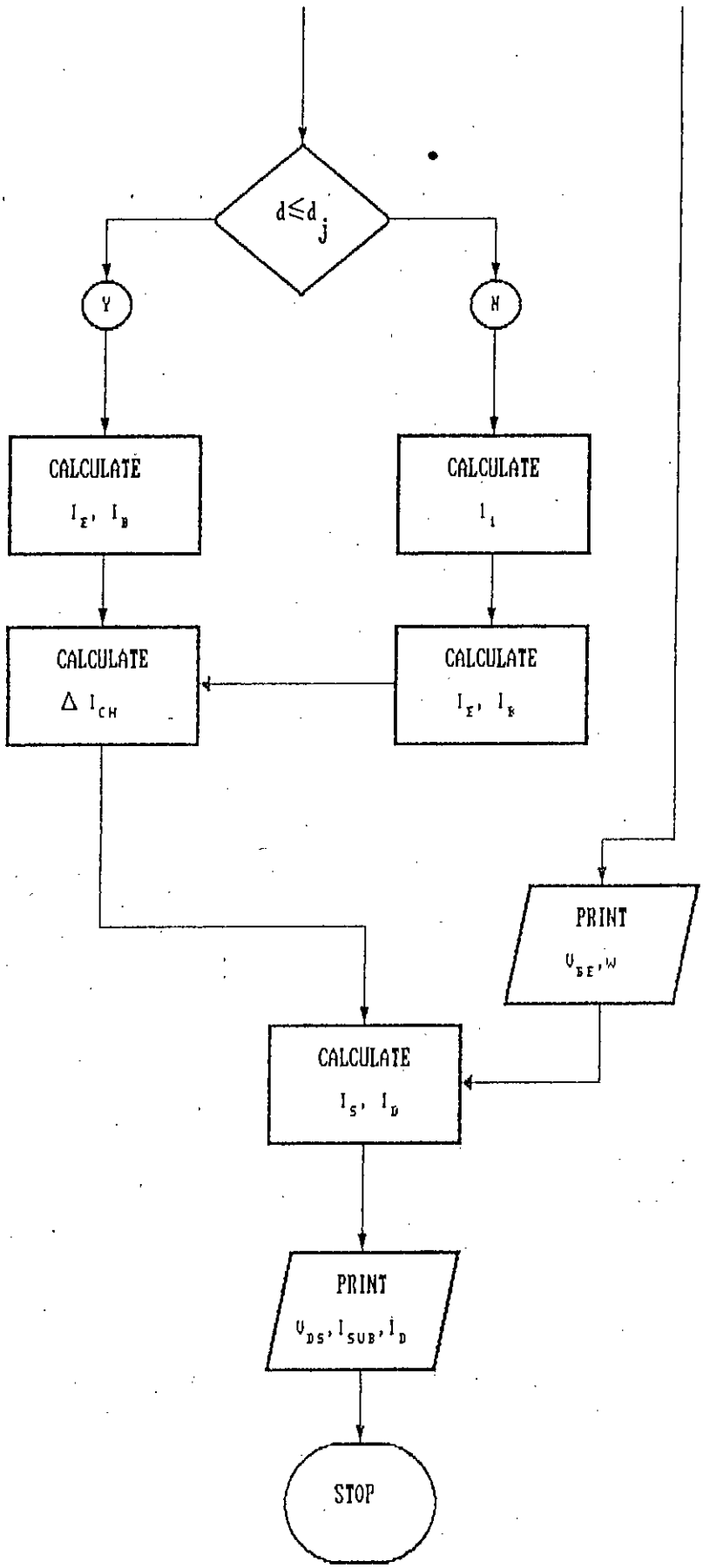


Fig. 3.1. A flowchart illustrating the procedure for computing current voltage characteristics.

the substrate current I_{sub} .

6. If I_{sub} is less than or equal to I_{subt} then (a) assign base and emitter current equal to zero i.e $I_b = 0$, $I_e = 0$ (b) Calculate base emitter voltage V_{be}, depletion width w, and excess channel current ΔI_{ch} (c) print depletion width w and return to step 12 .

7. Calculate base emitter voltage V_{be}, the depth of EPR d, and thickness of EPR at tranisition phase d_t .

8. If d is less than or equal to junction depth d_j then calculate I_b, I_e .

9. Calculate the excess channel current ΔI_{ch} .

10. Calculate the EPR length l_1 at a depth $d > d_j$.

11. Calculate I_b and I_e and return to step 9 .

12. Calculate and print drain current I_d and source current I_s .

13. Stop .

Using equation (2.55) the short channel threshold $\hat{V}_T$ is calculated at a particular drain source voltage V_{DS} for a fixed channel length L. Then the saturation voltage V'_{DS} which varies both with the channel length L and V_{GS} is calculated from (2.66) by applying regula falsi method. If V_{DS} is less than or equal to V'_{DS} then I_{ch} is calculated from (2.64). Otherwise first I'_{ch} is calculated from equation (2.63) and then I_{ch} and E_{SD} are calculated from (2.65) and (2.76) respectively. The substrate current I_{sub} is then obtained from equation (2.75) with the help of regula falsi method. If $I_{sub} > I_{subt}$ then V_{be}, d, d_t are calculated from equation (2.113), (2.114) and (2.117) respectively, whereas, for $I_{sub} \leq I_{subt}$, V_{be}, w and ΔI_{ch} are calculated using equation (2.112), (2.97) and (2.82) respectively. If d is less than or

equal to d_j then I_e and I_b are found from equation (2.106) and (2.107). For a value of d greater than d_j, I_e and I_b are calculated from equations (2.118) and (2.119) after calculating l_1 and ΔI_{ch} from equation (2.82) with $I_{sub} = I_{subt}$. Finally, the drain current I_d and the source current I_s are calculated from equations (2.4) and (2.5).

Besides the main programme two separate programmes have been developed to find l_1 as a function of L and V_{DS}. By using the data found from the extrapolation of I_d vs. V_{DS} and I_{sub} vs. V_{DS} curve we extract the value of l_1 at different V_{DS} for a fixed channel length L from the first programme. Regula falsi method is used in the programme to extract the necessary data. The second programme is used to find the mathematical expression of l_1 in terms of L and V_{DS} using the necessary data obtained from the first programme. In the second programme the coefficient a, a_1, a_2, b_1, b_2 are found using matrix inversion subprogramme.

3.3 Results and Discussions

The analytical model developed in chapter 2 is used to find various characteristics of a short channel MOSFET.

3.3.1 Threshold and saturation voltage

Threshold and saturation voltage are two very important parameters to find the channel current of a short channel MOSFET as they are dependent on channel length. Fig. 3.2 shows the effect of channel length on threshold voltage and Fig. 3.3 shows the effect of channel length on saturation voltage of a MOSFET. Fig.

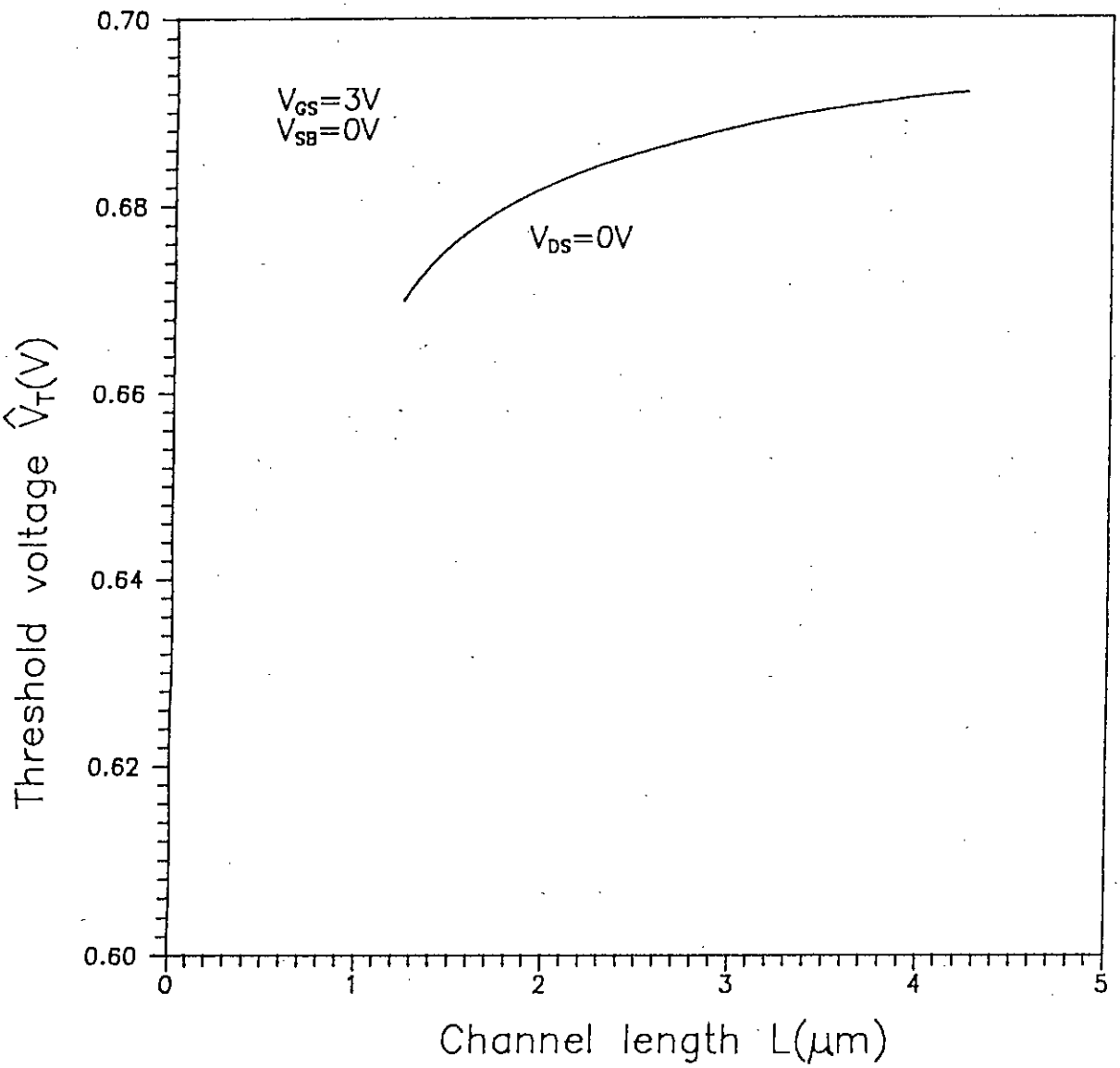


Fig. 3.2. Effect of channel length on threshold voltage of a MOSFET.

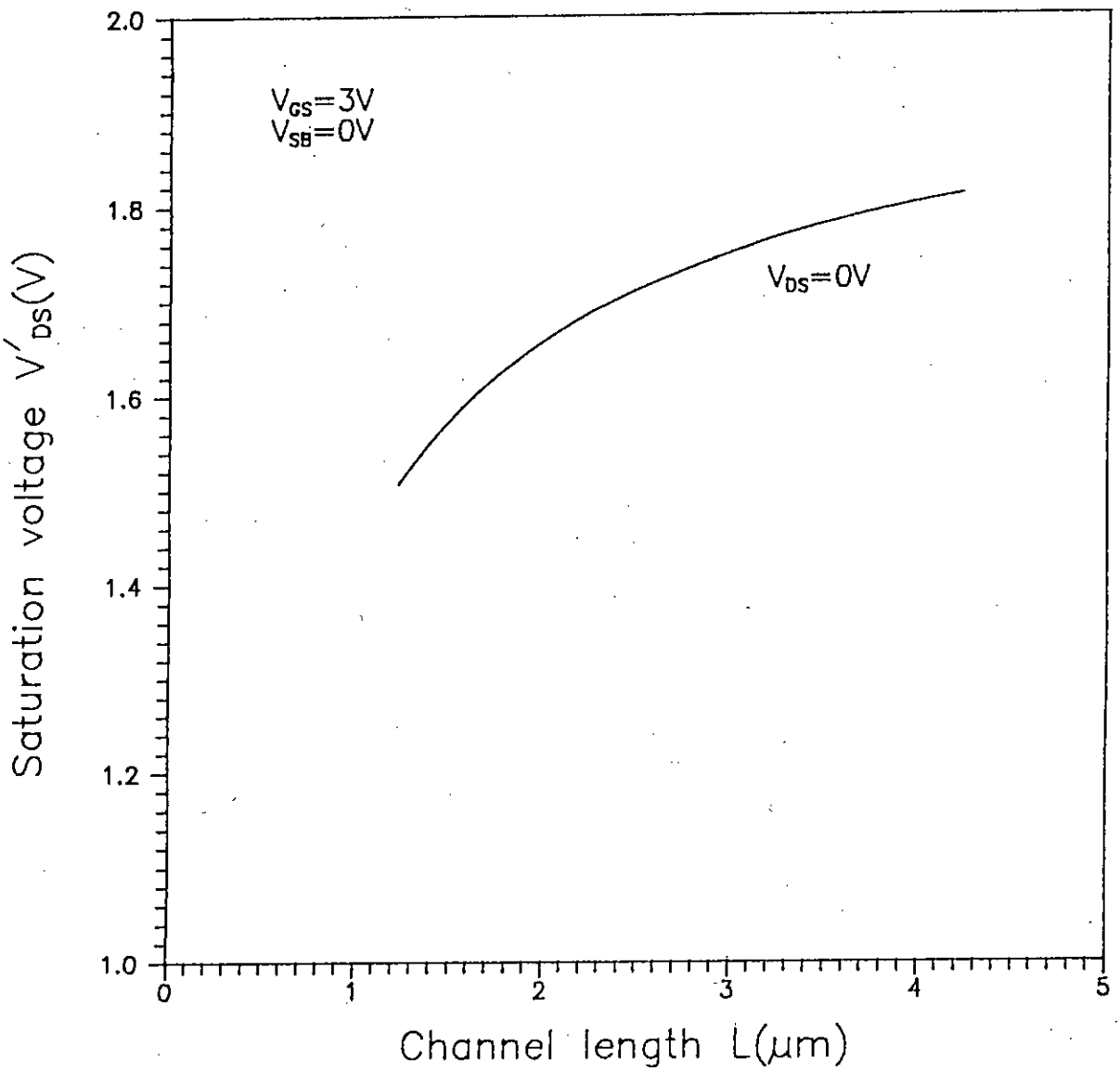


Fig. 3.3. Effect of channel length on saturation voltage of a MOSFET.

3.2 shows that when the channel length decreases the threshold voltage $\hat{V}_T$ of the MOSFET decreases for a fixed drain source voltage. This is due to the fact that for a fixed drain source voltage ΔV_T increases, with decrease of L as given by equation (2.49). So the short channel threshold $\hat{V}_T$ decreases as L decreases when V_{DS} is fixed. The physical explanation for the reduction in threshold due to lowering of the channel length lies in the fact that as the channel length decreases the depletion charge at source and drain ends widen and become comparable to the depletion charge Q_B controlled by the gate. As a result the threshold gate voltage required to achieve inversion must decrease to accomodate smaller Q_B. Again as the threshold decreases with the decrease of channel length, the saturation voltage V'_{DS} also decreases with the decrease of channel length.

3.3.2 Channel current

Fig. 3.4 shows the channel current $I_{\mathbf{ch}}$ vs. V_{DS} characteristics for a series of MOSFET at a particular V_{GS} differing only in electrical channel lengths. For higher channel length L, the channel current is lower for a fixed drain source voltage. The situation can be explained from equation (2.64) and (2.65). We can see from those equations that the channel current is inversely proportional to channel length L. Fig. 3.5 shows the channel current $I_{\mathbf{ch}}$ vs. V_{DS} characteristics for a higher V_{GS} than that of Fig. 3.4. For higher V_{GS} the channel current $I_{\mathbf{ch}}$ must be higher as can be shown from equation (2.64) (2.65) for the same V_{DS} and L.

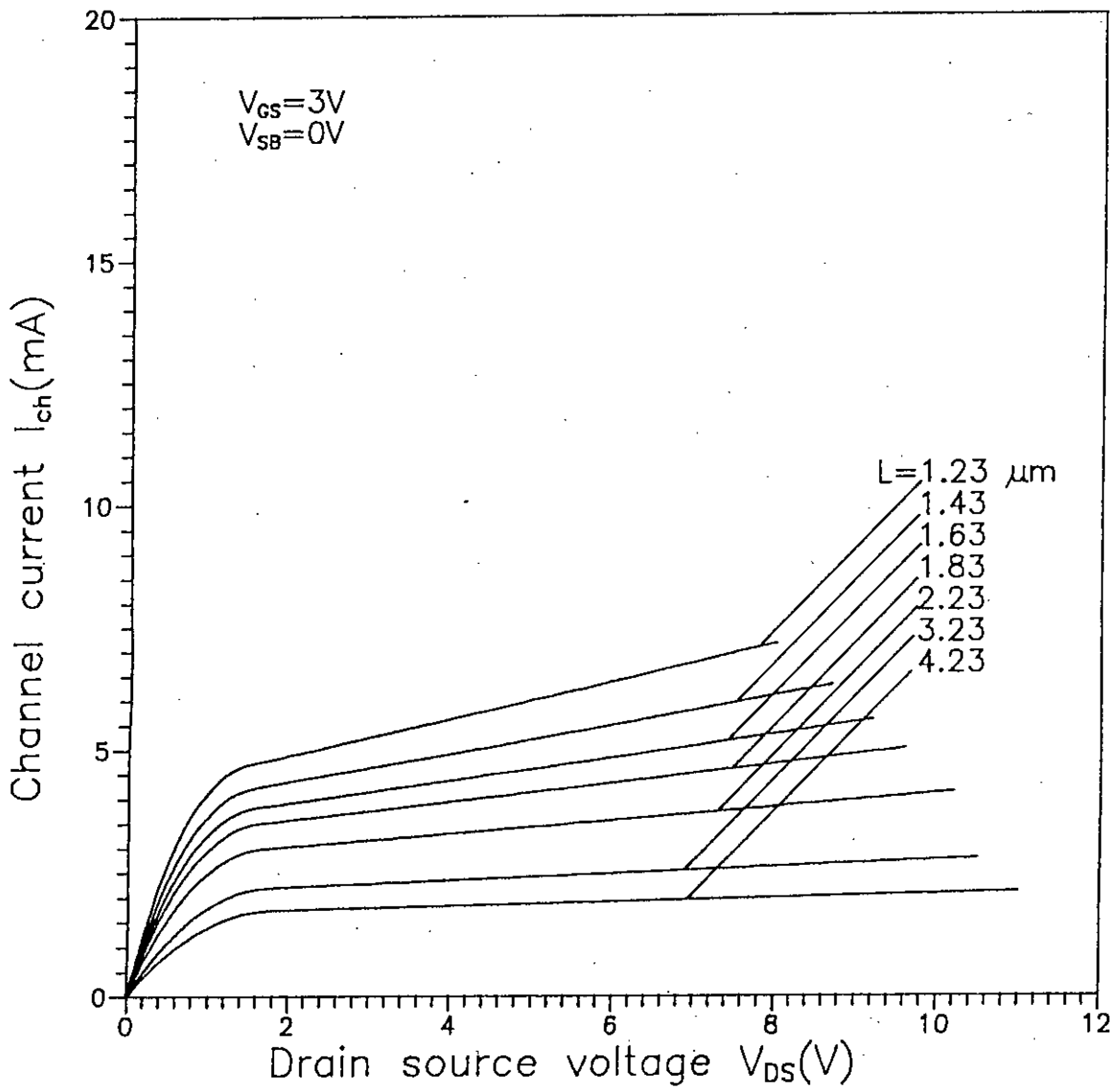


Fig. 3.4. Channel current vs. drain source voltage characteristics for V_{GS}=3V.

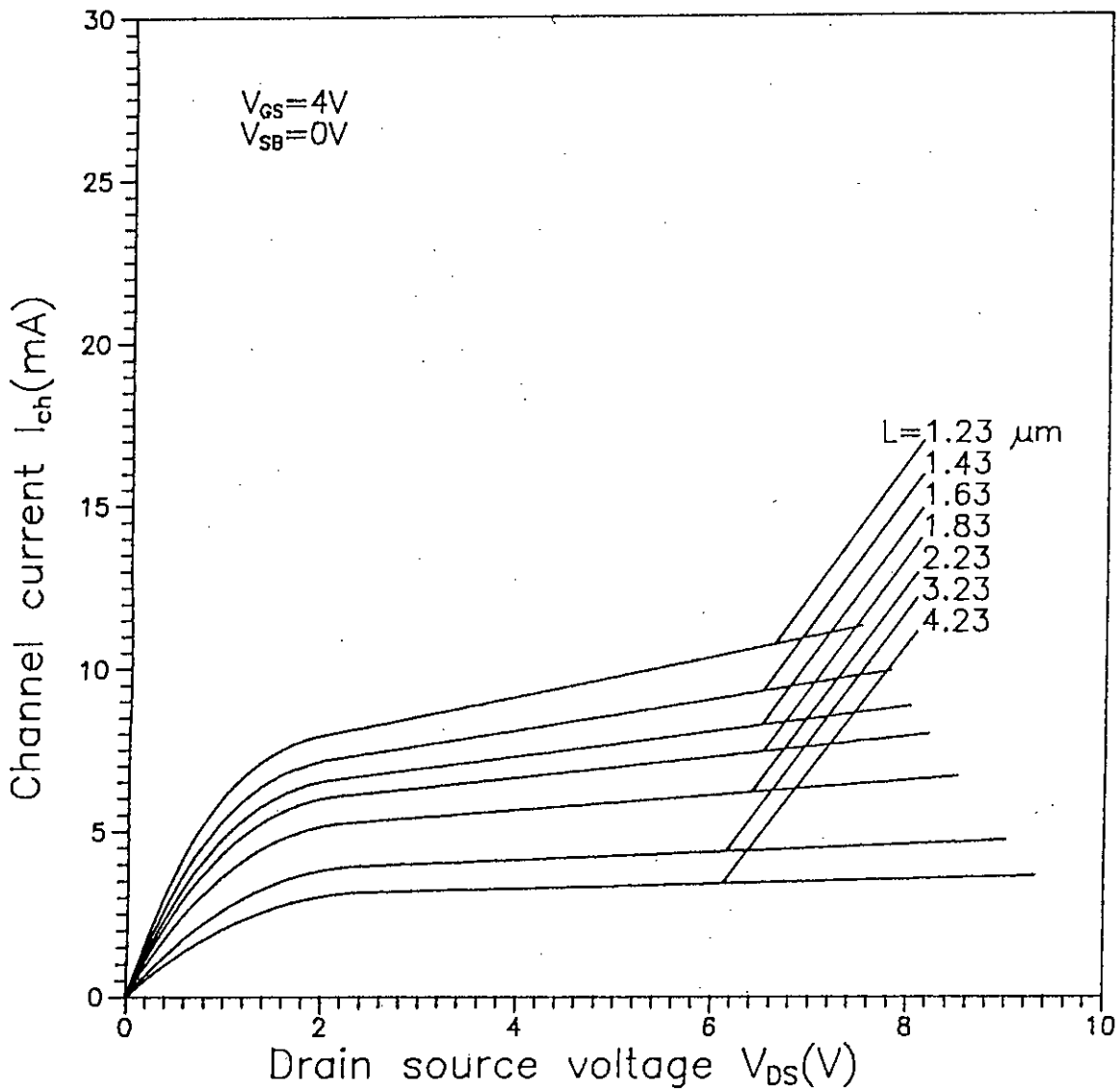


Fig. 3.5. Channel current vs. drain source voltage characteristics for V_{GS}=4V.

3.3.3 Lateral electric field and substrate current

Lateral electric field in a short channel MOSFET is a strong function of drain source voltage V_{DS}. The electric field E_{SD} near drain end of the channel at pinchoff or saturation point is given by E_{SAT} and must increase with V_{DS} beyond pinchoff. This can be explained from equation (2.76). For a fixed channel length and substrate doping V'_{DS} is fixed. The parameter A although decreases with V_{DS} but the increase of the term $(V_{DS} - V'_{DS})$ with V_{DS} overcompensates the decrease and ultimately the product of the two increases with V_{DS}. So the electric field E_{SD} increases with V_{DS} and the plot shown in Fig. 3.6 agrees well with the fact.

Fig. 3.7 and 3.8 show the variation of substrate current $I_{\mathbf{sub}}$ with V_{DS} for two different values of V_{GS} for a series of MOSFET differing only in channel lengths. These plots show that the substrate current increases with V_{DS} which is quite obvious and can be explained from equation (2.75) and (2.76). The substrate current is a strong function of multiplication factor M as shown from (2.75). The multiplication factor M on the other hand increases with V_{DS} due to the increase of E_{SD} with V_{DS} as given by equation (2.76) and (2.80). These facts justify the increase of substrate current with V_{DS}. The effect of V_{GS} on substrate current can be explained by considering two conflicting factors. The substrate current $I_{\mathbf{sub}}$ depends on both ionization rate α_{eff} and channel current $I_{\mathbf{ch}}$ [3]. When V_{GS} increases $I_{\mathbf{ch}}$ increases but α_{eff} decreases due to the decrease of electric field E_{SD}. The decrease in E_{SD} is due to the increase of V'_{DS} with V_{GS}. The increase in channel current tends to increase the substrate current $I_{\mathbf{sub}}$, whereas, the decrease in α_{eff} tends to decrease the substrate current $I_{\mathbf{sub}}$. Ultimately the substrate current for a fixed drain source voltage is determined by the factor of the two which dominates the other.

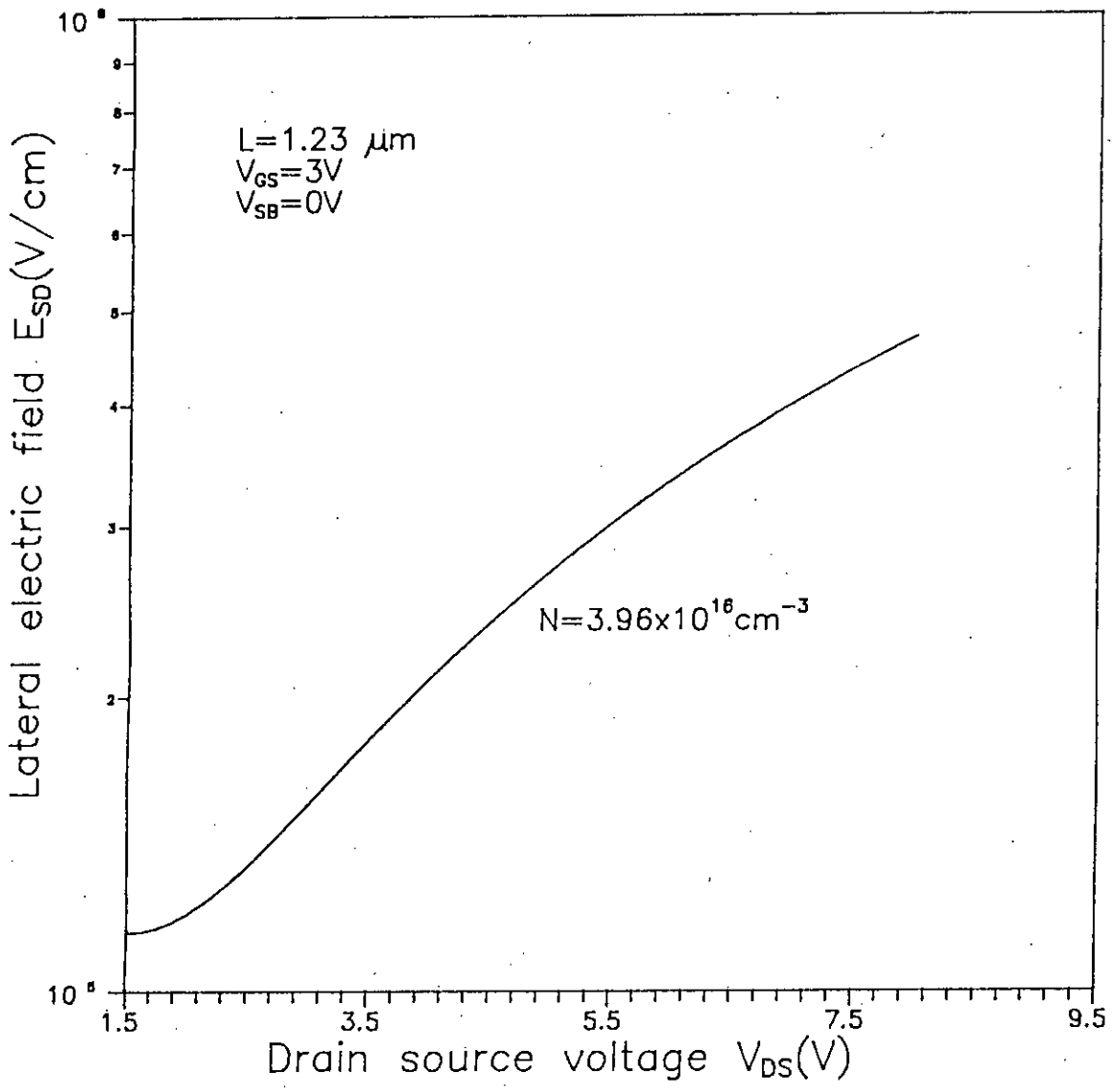


Fig. 3.6. Effect of drain source voltage on lateral electric field.

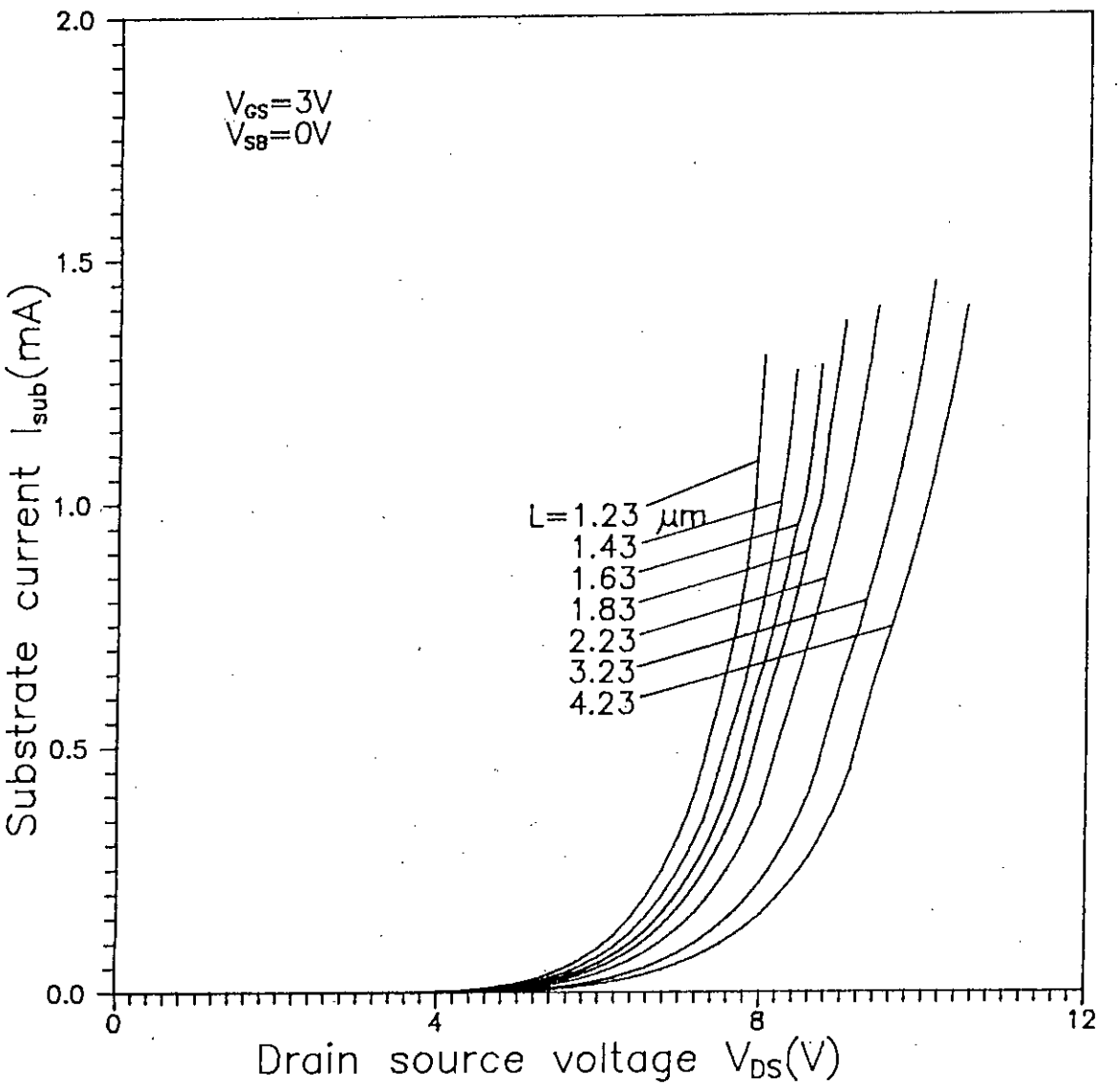


Fig. 3.7. Substrate current vs. drain source voltage characteristics for V_{GS}=3V.

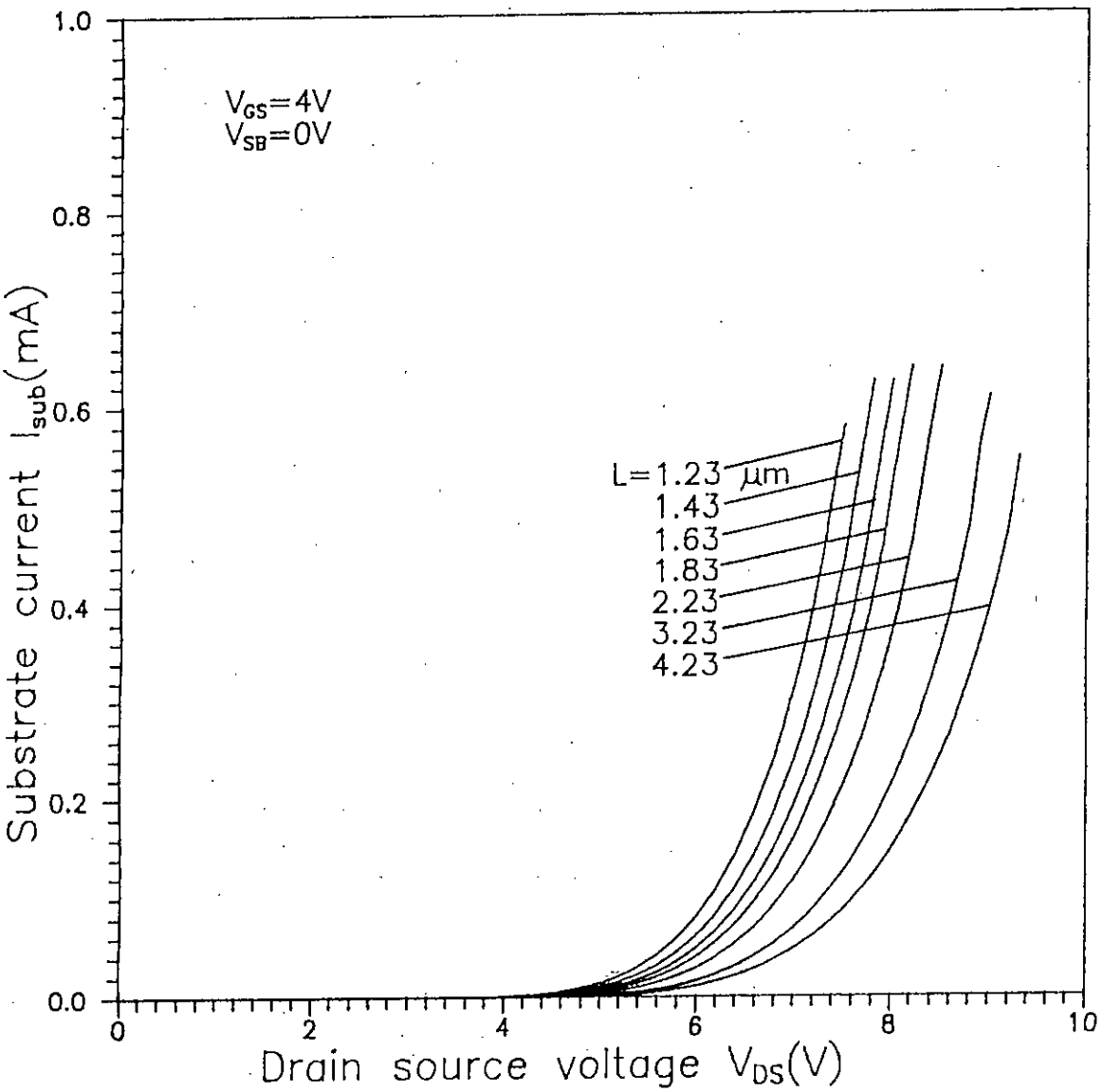


Fig. 3.8. Substrate current vs. drain source voltage characteristics for V_{GS}=4V.

3.3.4 Depletion width and the combined channel current

Fig. 3.9 shows the variation of depletion width w with substrate current $I_{\mathbf{sub}}$. The depletion width w decreases with the increase of substrate current $I_{\mathbf{sub}}$ which can be explained by equation (2.97). The depletion width w is a function of $I_{\mathbf{sub}}$ for a fixed w_o and decreases with the increase of $I_{\mathbf{sub}}$ due to the decrease of the second term of the square root portion of equation (2.97). The increase in substrate current corresponds to a increase in the number of holes which causes a reduction in depletion width w.

Fig. 3.10 shows the effect of substrate current $I_{\mathbf{sub}}$ on threshold voltage $\hat{V}_T$ of a short channel MOSFET. The plot shows that $\hat{V}_T$ starts to decrease appreciably after a certain V_{DS}. The reason for such a rapid decrease can be attributed to the generation of substrate current at that certain voltage V_{DS}. We can see from equation (2.88) that the reduction in threshold $\Delta V_{\mathbf{th}}$ increases as w decreases. But from Fig. 3.9, w decrases with the increase of $I_{\mathbf{sub}}$. So, the short channel thresold $\hat{V}_T$ decreases as $I_{\mathbf{sub}}$ increases.

The combined channel current $I_{\mathbf{che}}$ of the MOSFET is the sum of channel current $I_{\mathbf{ch}}$ and the excess channel current $\Delta I_{\mathbf{ch}}$. The channel current $I_{\mathbf{ch}}$ increases with V_{DS} but the excess channel current $\Delta I_{\mathbf{ch}}$ increases with V_{DS} upto transition phase due to threshold lowering $\Delta V_{\mathbf{th}}$ as given by equation (2.82) and then saturates because of zero depletion width $w = 0$ reaching at the transition phase. After the transition phase the combined channel current $I_{\mathbf{che}}$ almost saturates due to constant value of $\Delta I_{\mathbf{ch}}$ and a slight increase in $I_{\mathbf{ch}}$ with V_{DS}. The plot 3.11 shows the variation of $I_{\mathbf{che}}$ with V_{DS}.

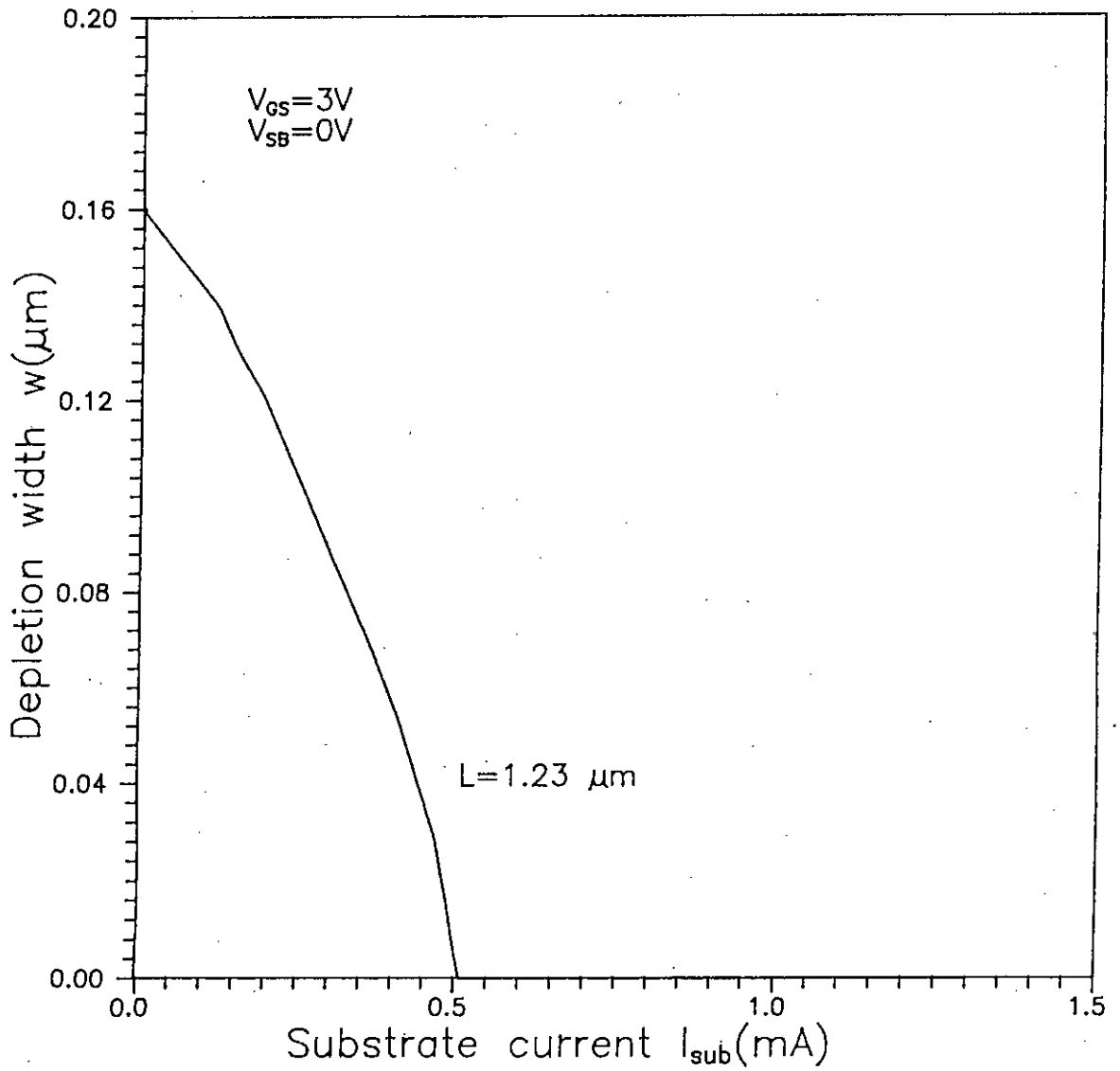


Fig. 3.9. Effect of substrate current on depletion width.

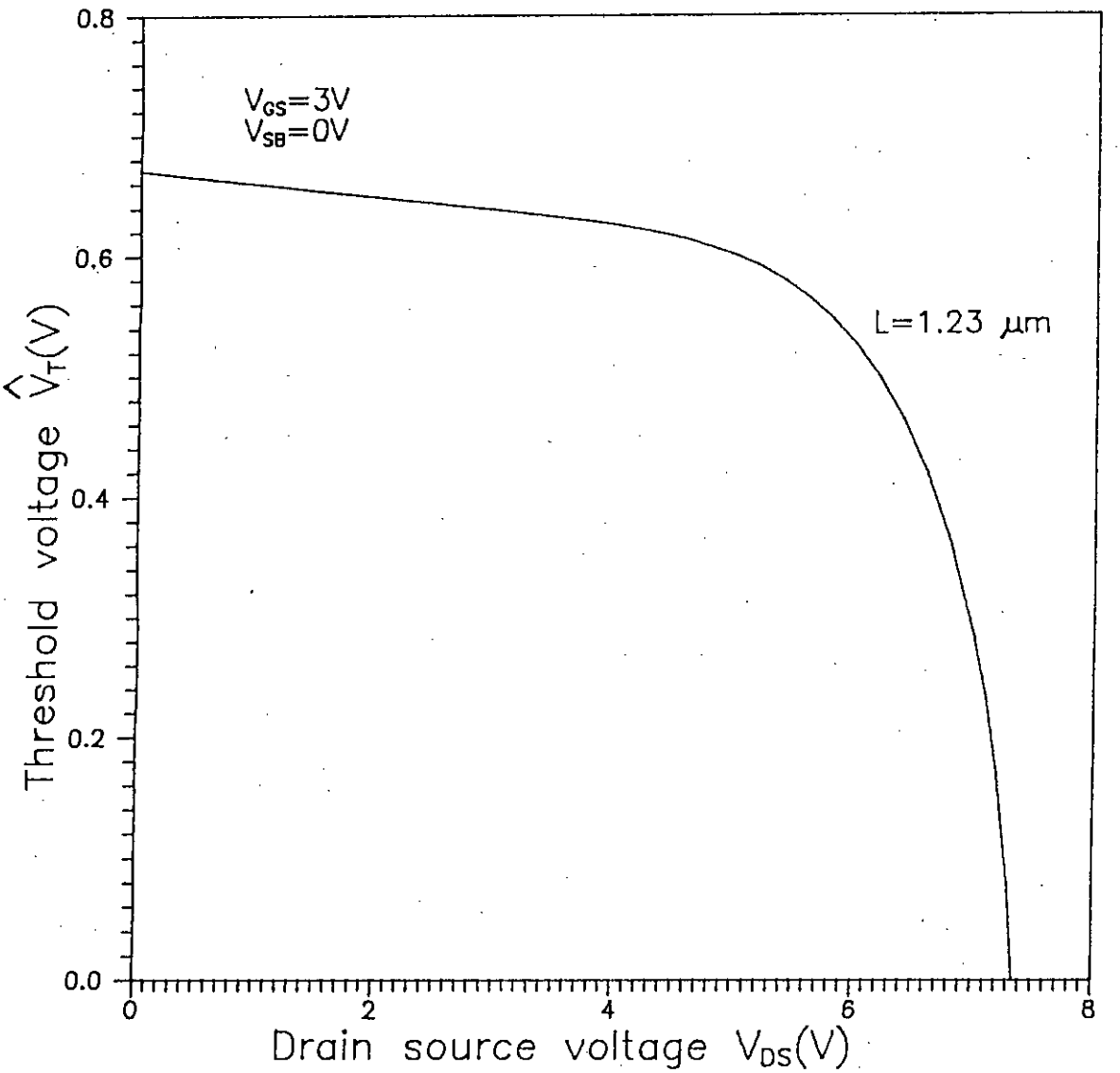


Fig. 3.10. Effect of drain source voltage on threshold voltage of a MOSFET.

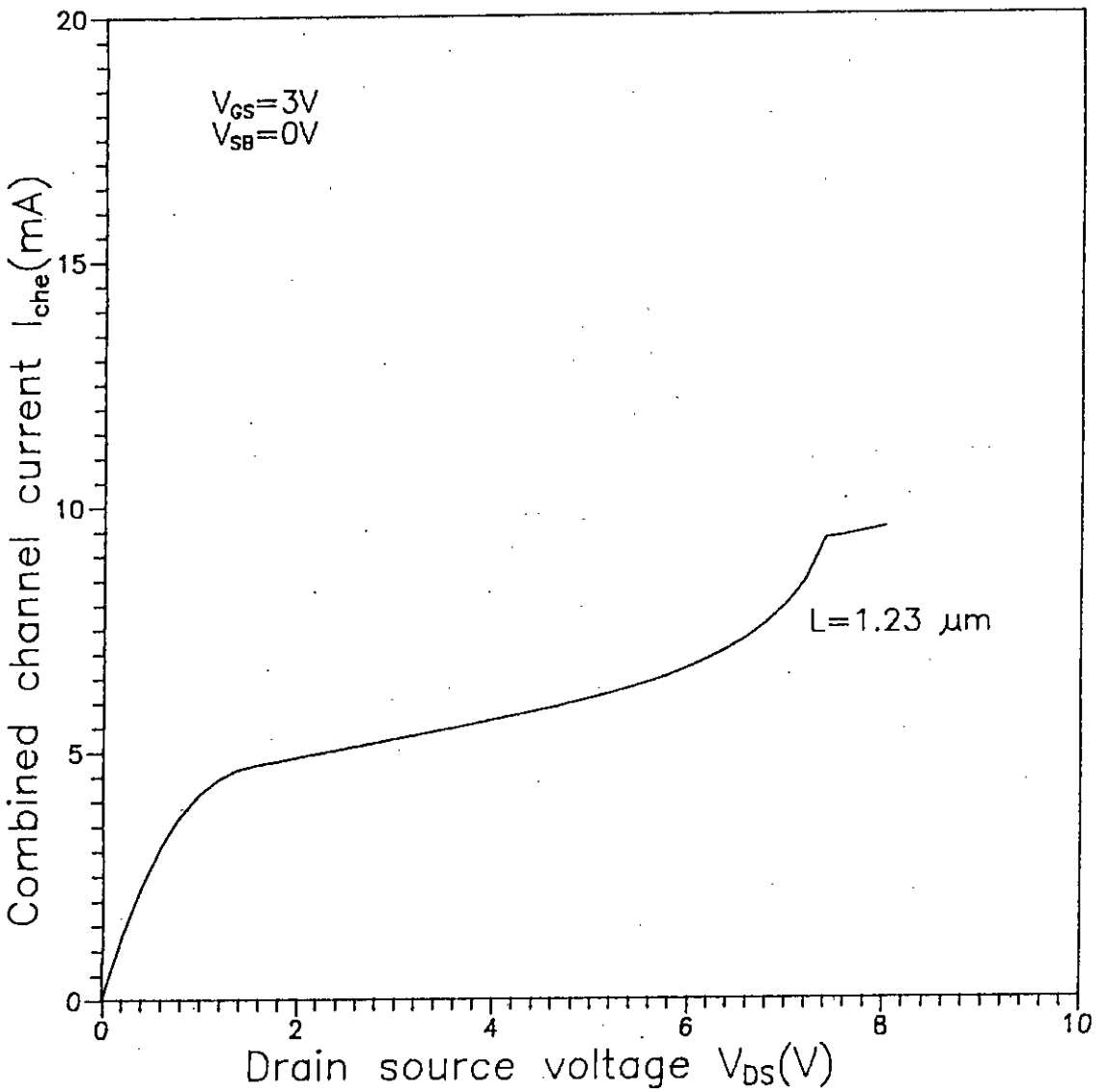


Fig. 3.11. Effect of drain source voltage on combined channel current.

3.3.5 Base emitter voltage and substrate resistance

Fig. 3.12 shows the dependence of base emitter voltage V_{be} of the MOSFET on I_{sub} after the bipolar turn on. The base emitter voltage V_{be} increases linearly with I_{sub} upto the substrate current I_{subt} and then the increase in V_{be} slows down. The behaviour can be explained by equation (2.112) and (2.113) respectively where V_{be} is governed by the first equation before the transition phase and by the second equation after the transition phase. The second equation shows the logarithmic variation of V_{be} with I_{sub} after the transition phase.

The Fig. 3.13 shows the variation of R_{sub} with EPR thickness d. The substrate resistance R_{sub} should decrease with the increase of d as given by equation (2.114). The plot 3.13 agrees well with equation (2.114). The decrease of R_{sub} with the increase in d is due to the reduction in the length of the substrate material with the evolution of EPR.

3.3.6 Drain current

The drain current of the MOSFET is the sum of I_{ch}, ΔI_{ch}, I_e and I_{sub}. Fig. 3.14 shows the drain current I_d vs. V_{DS} characteristic for a series of conventional MOSFETs differing only in electrical channel lengths. The drain current I_d slowly increases upto a certain V_{DS} and then it increases rapidly with V_{DS} to cause the breakdown of the MOSFET. The voltage around which this change takes place corresponds the transition phase of the MOSFET. The initial up-bending of the drain characteristic before the transition phase is caused by the excess channel current ΔI_{ch} and the rapid rise in drain current after the transition phase is caused by the emitter current I_e. From equation (2.82) and (2.106) we can see that both ΔI_{ch}

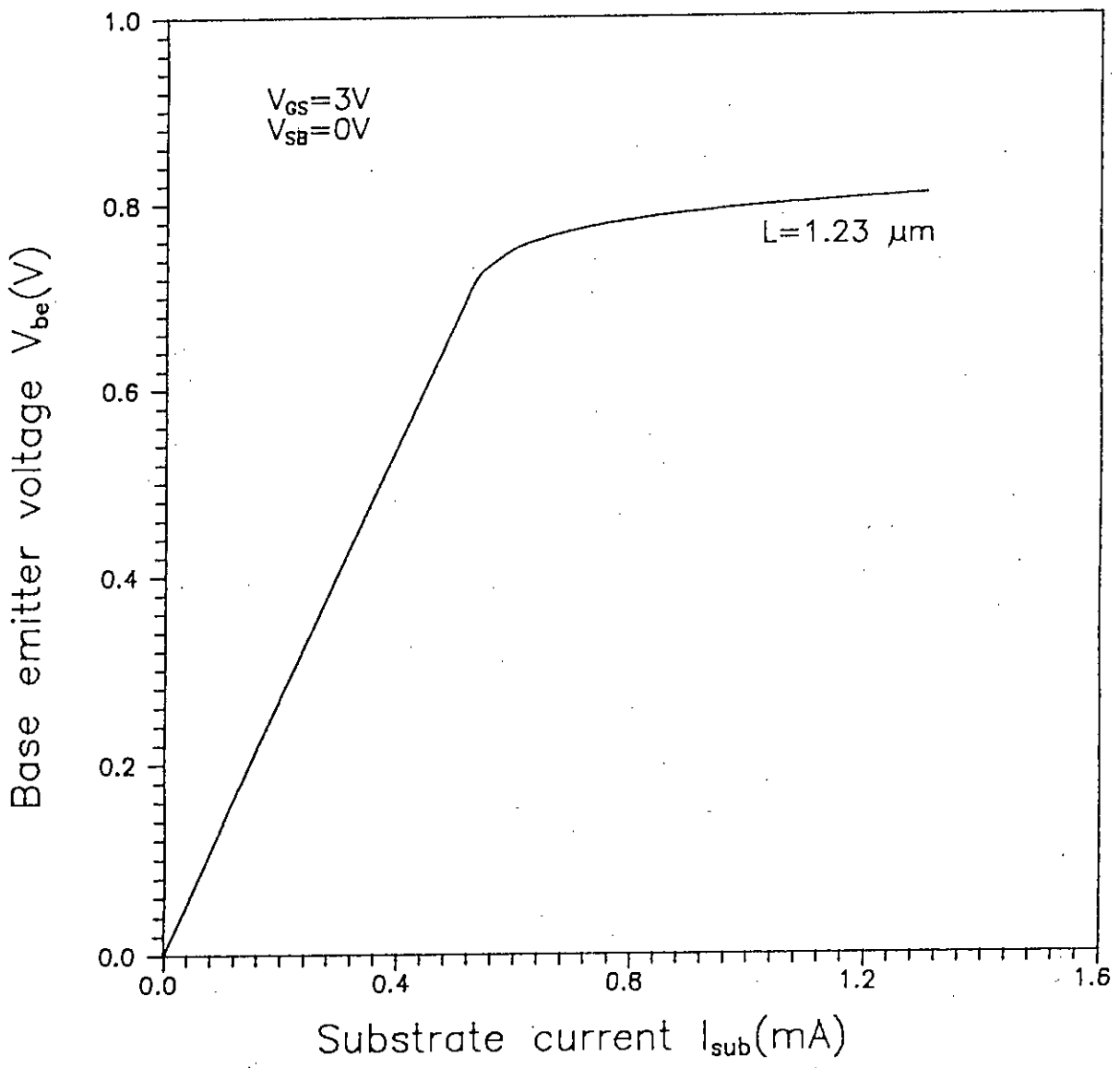


Fig. 3.12. Effect of substrate current on base emitter voltage.

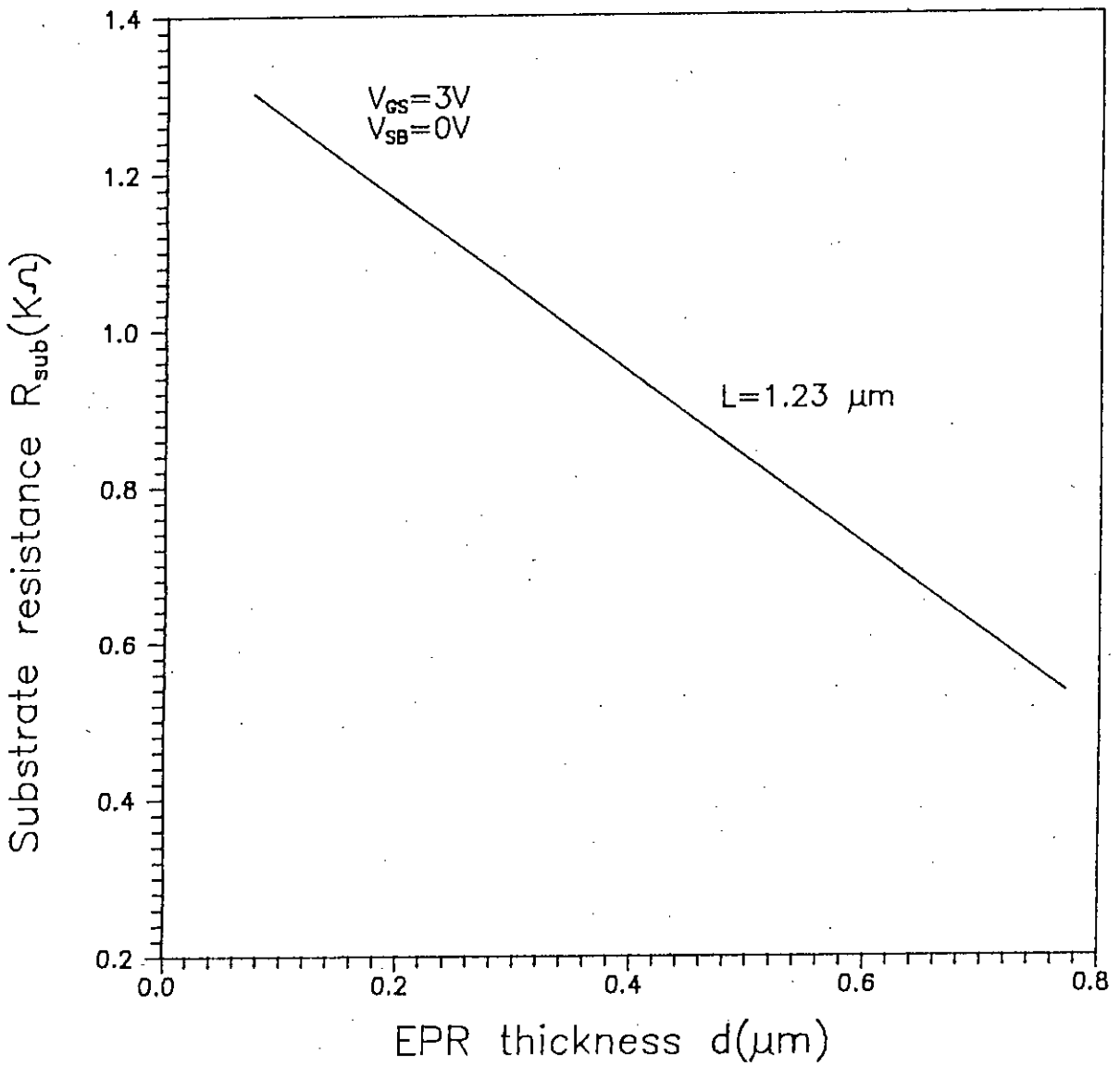


Fig. 3.13. Effect of EPR thickness on substrate resistance.

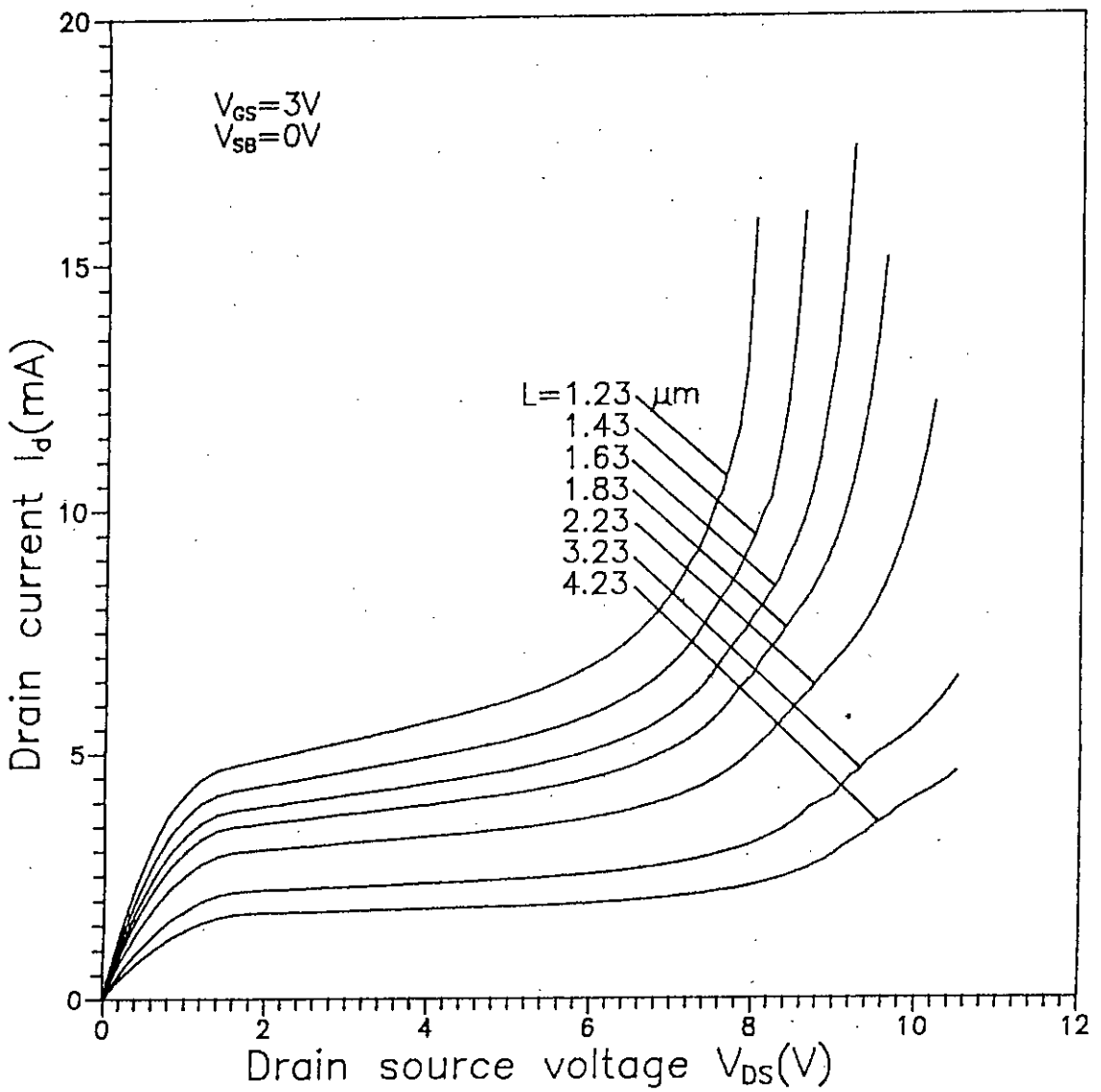


Fig. 3.14. Drain current vs. drain source voltage characteristics.

and I_e are function of substrate current. As the substrate current I_{sub} increases with V_{DS} the excess channel current ΔI_{ch} increases slowly but the emitter current I_e increases rapidly according to the nature of the equation (2.82) and (2.106) respectively.

3.4 Conclusions

In this chapter different short channel effects have been presented. The drain and substrate characteristics for different operating conditions are studied by using the model presented in chapter 2. A computer programme is developed based on the algorithm illustrated in the chapter. The results based on the model presented in chapter two show that the multiplication induced substrate current is the main reason that leads to the breakdown of the short channel MOSFET. The major components of the drain current that contribute to this breakdown phenomena are excess channel current ΔI_{ch} and emitter current I_e both of which are determined by the substrate current I_{sub}. But the substrate current I_{sub} again depends on the source current I_s and the multipliaction factor M which is a strong function of electric field E_{SD} at the drain end.

CHAPTER 4

Conclusions and Suggestions

4.1 Conclusions

In this work, an analytical model of breakdown in short channel MOSFET is presented. Modelling of device aims at relating physical device parameters to device terminal characteristics. Simple and accurate device models are needed to predict the performance of the device. But accurate modelling of a device is very difficut and complex. There is always a trade-off between accuracy and complexity. A number of different models have been developed in the last few years. But most of those models did not take into account the actual physical effects occuring during the avalanche induced breakdown in short channel MOSFET. In this work a complete physics along with a simple analytical model is presented. By taking various short channel effects simultaneously and then combinning them into a single analytical model the drain and substrate characteristics are obtained in the avalanche-induced multiplication region. An accurate substrate current model and a simple channel current model is used to find the different characteristics of the short channel MOSFET for a wide range of device parameter.

The holes produced by avalanche multiplication due to high field at the drain depletion region causes a substrate current to flow in a short channel MOSFET which ultimately degrades the device performance and finally causes the destruction of the device. The breakdown in MOSFET can be prevented by increasing I_{subt} current needed to initiate the bipolar action by reducing R_{sub} as given by equation (2.99). The increase in I_{subt} corresponds to a shift of the drain characteristics towards higher drain biases. The reduction in R_{sub} can be achieved by doping the substrate heavily. Increasing the bulk doping concentration leads to the undesirable snap back characteristics of a MOSFET. So, the deep channel implant is the most appreciable one to achieve the reduction in R_{sub} instead of the overall doping increase. This also prevents the punchthrough of the channel.

4.2 Suggestions

In this work the channel current model is developed by one dimensional analysis. However the breakdown physics in short channel MOSFET along with various short channel effects are three dimensional which is extremely difficult to approach analytically. The present model can be improved by three dimensional analysis in the near future. The substrate resistance can be replaced by an accurate analytical expression and an accurate physics may also be developed to find the variation of l_1 with L and V_{DS} analytically at a EPR depth of $d > d_j$. Finally, an entirely non-iterative breakdown model may be developed in future to predict the breakdown characteristics of the short channel MOSFET.

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APPENDIX A

Determination of the expression of l_m as a function of L and V_{DS}

Let us consider that x, y, z represents L, V_{DS}, l_m of the work presented in this thesis respectively. Now z can be expressed in terms of x and y by the following two degree polynomial.

$$z = a + a_1x + a_2x^2 + b_1y + b_2y^2 \qquad A.1$$

The determination of the coefficients $a, a_1, a_2, a_3, b_1, b_2$ can be performed by using the least square method. In the least square method the square of the error E between the function to be approximated and the approxmimating function is minimized. The minimization of E can accomplished by setting the partial derivatives of E with respect to each of the coefficients equal to zero, where E is given by

$$E = Err^2 = \{z - (a + a_1x + a_2x^2 + b_1y + b_2y^2)\}^2 \qquad A.2$$

Now accordingly by putting $\frac{\partial E}{\partial a} = 0$, $\frac{\partial E}{\partial a_1} = 0$, $\frac{\partial E}{\partial a_2} = 0$, $\frac{\partial E}{\partial b_1} = 0$, $\frac{\partial E}{\partial b_2} = 0$ we get the following equations

$$na + a_1\sum_{i=1}^{n} x_i + a_2\sum_{i=1}^{n} x_i^2 + b_1\sum_{i=1}^{n} y_i + b_2\sum_{i=1}^{n} y_i^2 = \sum_{i=1}^{n} z_i \qquad A.3$$

$$a\sum_{i=1}^{n} x_i + a_1\sum_{i=1}^{n} x_i^2 + a_2\sum_{i=1}^{n} x_i^3 + b_1\sum_{i=1}^{n} x_iy_i + b_2\sum_{i=1}^{n} y_i^2x_i = \sum_{i=1}^{n} z_ix_i \qquad A.4$$

$$a\sum_{i=1}^{n} x_i^2 + a_1\sum_{i=1}^{n} x_i^3 + a_2\sum_{i=1}^{n} x_i^4 + b_1\sum_{i=1}^{n} x_i^2y_i + b_2\sum_{i=1}^{n} y_i^2x_i^2 = \sum_{i=1}^{n} z_ix_i^2 \qquad A.5$$

$$a\sum_{i=1}^{n} y_i + a_1\sum_{i=1}^{n} x_iy_i + a_2\sum_{i=1}^{n} x_i^2y_i + b_1\sum_{i=1}^{n} y_i^2 + b_2\sum_{i=1}^{n} y_i^3 = \sum_{i=1}^{n} z_iy_i \qquad A.6$$

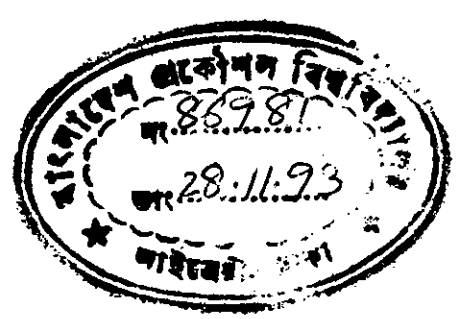
$$a\sum_{i=1}^{n} y_i^2 + a_1\sum_{i=1}^{n} x_iy_i^2 + a_2\sum_{i=1}^{n} x_i^2y_i^2 + b_1\sum_{i=1}^{n} y_i^3 + b_2\sum_{i=1}^{n} y_i^4 = \sum_{i=1}^{n} z_iy_i^2 \qquad A.7$$

Rearranging the equations in matrix form we find

$$\begin{bmatrix} n & \sum x_i & \sum x_i^2 & \sum y_i & \sum y_i^2 \\ \sum x_i & \sum x_i^2 & \sum x_i^3 & \sum x_i y_i & \sum x_i y_i^2 \\ \sum x_i^2 & \sum x_i^3 & \sum x_i^4 & \sum x_i^2 y_i & \sum y_i^2 x_i^2 \\ \sum y_i & \sum x_i y_i & \sum x_i^2 y_i & \sum y_i^2 & \sum y_i^3 \\ \sum y_i^2 & \sum x_i y_i^2 & \sum x_i^2 y_i^2 & \sum y_i^3 & \sum y_i^4 \end{bmatrix} \begin{bmatrix} a \\ a_1 \\ a_2 \\ b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} \sum z_i \\ \sum z_i x_i \\ \sum z_i x_i^2 \\ \sum z_i y_i \\ \sum z_i y_i^2 \end{bmatrix}$$

$$\Rightarrow \begin{bmatrix} a \\ a_1 \\ a_2 \\ b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} n & \sum x_i & \sum x_i^2 & \sum y_i & \sum y_i^2 \\ \sum x_i & \sum x_i^2 & \sum x_i^3 & \sum x_i y_i & \sum x_i y_i^2 \\ \sum x_i^2 & \sum x_i^3 & \sum x_i^4 & \sum x_i^2 y_i & \sum y_i^2 x_i^2 \\ \sum y_i & \sum x_i y_i & \sum x_i^2 y_i & \sum y_i^2 & \sum y_i^3 \\ \sum y_i^2 & \sum x_i y_i^2 & \sum x_i^2 y_i^2 & \sum y_i^3 & \sum y_i^4 \end{bmatrix}^{-1} \begin{bmatrix} \sum z_i \\ \sum z_i x_i \\ \sum z_i x_i^2 \\ \sum z_i y_i \\ \sum z_i y_i^2 \end{bmatrix} = A^{-1}[K] \qquad A.8$$

So by performing the operation of A^{-1} the cofficients can determined from equation A.8 . Knowing the coefficients the variation of l_m with V_{DS} and L can be obtained.



APPENDIX B

Determination of substrate resistance R_{sub} in EBE phase

To find the variation of R_{sub} with channel length L we rely on the following mathematical relation

$$R_{subt} = R_{sub} = R_o + (\frac{L_o}{L} - 1)\, K_L \qquad \text{B.1}$$

where R_o is the resistance of the MOSFET with channel length $L = L_o$, and K_L can be determined by the following simple methodology. The substrate resistance $R_{sub}(= R_{subt})$ of a MOSFET with $L = L_o$ can be extracted from its two I_s versus V_{DS} characteristics corresponding to 2 different V_{GS} as shown in (Fig. 2.9). The extrapolation of the saturation portion of the I_s curve (related to $V_{GS} + \Delta V_{thmax}$) as far as the intersection with curve (related to V_{GS}) gives the drain voltage corresponding to the transition phase . The latter allows to determine I_{subt} for $L = L_o$ from I_{sub} versus V_{DS} characteristic. Knowing I_{subt} we can find $R_{sub} = R_{subt} = R_o$ from the following relation

$$R_{subt} = \frac{V_s}{I_{subt}} \qquad \text{B.2}$$

Now by repeating the same procedure to MOSFET of length $L \neq L_o$ the coefficient K_L can be calculated from the difference of $(R_{subt} - R_o)$ according to equation B.1.